USB 2.0 - UTMI Snap On Board

Reference Manual

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The IP was not developed for or intended for use in any specific customer application. The firmware/software of the device may have to be adapted to the specific intended modalities of use or even replaced by other firmware/software in order to ensure flawless function in the respective areas of application.

Performance data may depend on the operating environment, the area of application, the configuration, and method of control, as well as on other conditions of use; these may deviate from the technical specifications, the Design Guide specifications, or other product documentation. The actual performance characteristics can be determined only by measurements subsequent to integration.

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About this Manual

Introduction

This manual provides component details of the the USB 2.0 - UTMI Snap On board. Table below shows the revision history of board's reference manual.

Version	Date	Description
1.7	May 2008	• Updated features section
1.6	May 2008	• Added note on output logic level in Expansion Connector section in Chapter 2.
1.5	March 2008	• Changed Photograph of the board
1.4	December 2007	• Changed pin configuration of Santa Cruz Headers JP2 and JP3
1.3	October 2007	• Updated user guide as per the board version 4.0.
1.2	September 2007	• Added code for the board, Modified version history & Document part no.
1.1	May 2006	• First Publication of the Reference Manual

How to find Information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Shift + Ctrl + N to open to the Go To Page dialog box.
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Typographic Conventions

This reference manual uses the typographic conventions as shown below:

Visual Cue	Meaning
Bold Type with Initial Capital letters	All headings and Sub headings Titles in a document are displayed in bold type with initial capital letters; Example: **Board Components, Featured Device.**
Bold Type with Italic Letters	All Definitions, Figure and Table Headings are displayed in Italics. Examples: **Figure 2-1. USB 2.0 UTMI Snap On Board Components**, **Table 2-1. USB 2.0 - UTMI Snap On Board Components & Interfaces**
1., 2.	Numbered steps are used in a list of items, when the sequence of items is important. such as steps listed in procedure.
•	Bullets are used in a list of items when the sequence of items is not important.
☞	The hand points to special information that requires special attention
CAUTION	The caution indicates required information that needs special consideration and understanding and should be read prior to starting or continuing with the procedure or process.

Visual Cue	Meaning
	The warning indicates information that should be read prior to starting or continuing the procedure or processes.
	The feet direct you to more information on a particular topic.

Contents

1. Introduction

The USB 2.0 - UTMI snap on board is designed to provide connectivity between USB 2.0 host controller (computer) and UTMI compatible USB 2.0 function IP core. The Snap On board provides a fast, versatile, and easy-to-use communication path for data exchange between the device and host.

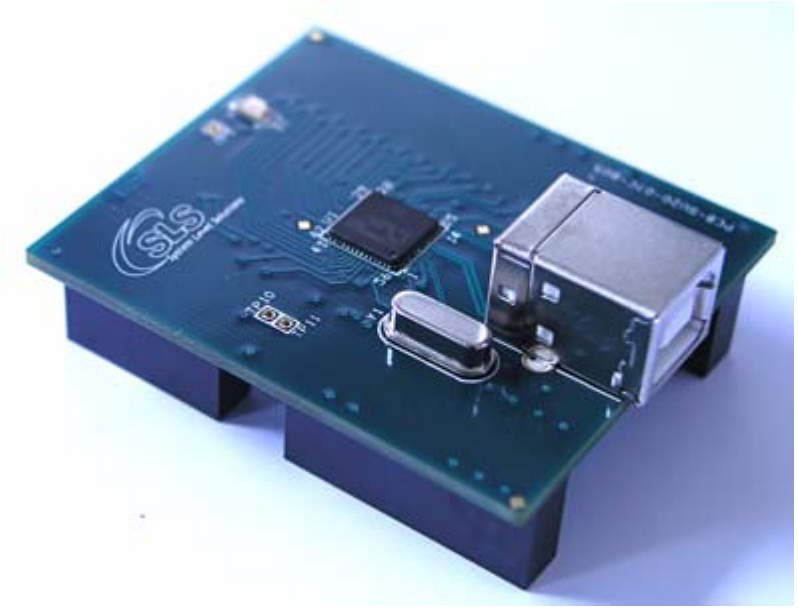
Features

USB 2.0 - UTMI snap on board is featured with:

- UTMI PHY Chip - Cypress CY7C68000
- Supports both Full Speed (12Mbps) and High Speed (480Mbps) USB operation
- Supports 8-bit bidirectional, 8-bit unidirectional and 16-bit bidirectional data interface
- Supports 16-bit 30MHz and 8-bit 60MHz interface
- USB B-type connector
- Dedicated crystal oscillator of 24 MHz for PHY chip
- One status LED
- Standard Santa Cruz interface support

Figure 1-1. shows the USB 2.0 - UTMI Snap On board angle view.

Figure 1-1. USB 2.0 - UTMI Snap On Board Angle View



The board works seamlessly with SLS USB 2.0 IP cores. For more information, visit http://www.slscorp.com/pages/ipusb2sls.php

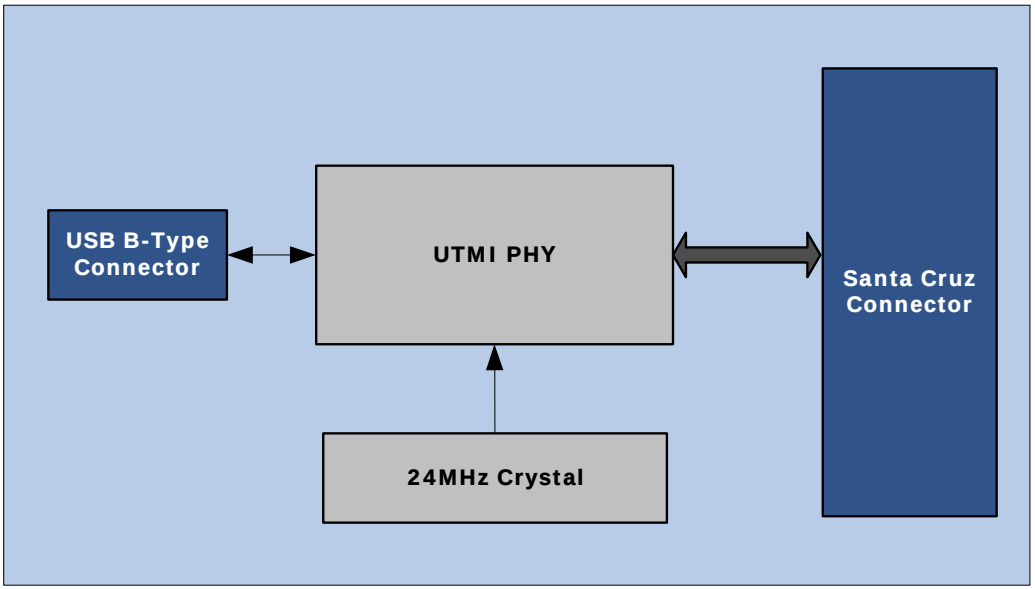
Block Diagram

USB 2.0 Snap On board includes following components:

- USB B-type Connector
- PHY Chip (Physical Layer Transceiver)
- Crystal of 24 MHz for PHY chip
- User LED (D1)
- Headers (F), JP2, JP3, JP4

☞ The three headers JP2, JP3, JP4 are Female headers on USB 2.0 snap on board which snaps on santacruz connectors. Figure 1-2. below shows functional diagram of USB 2.0 snap on board.

Figure 1-2. USB 2.0 - UTMI Snap On Board Functional Diagram



Next chapter explains overview of all the board components.

2. Board Components

This section contains brief overview of the important components on the USB 2.0 - UTMI Snap On Board. Figure 2-1. below shows the components on the Snap On Board.

Figure 2-1. USB 2.0 - UTMI Snap On Board - Components

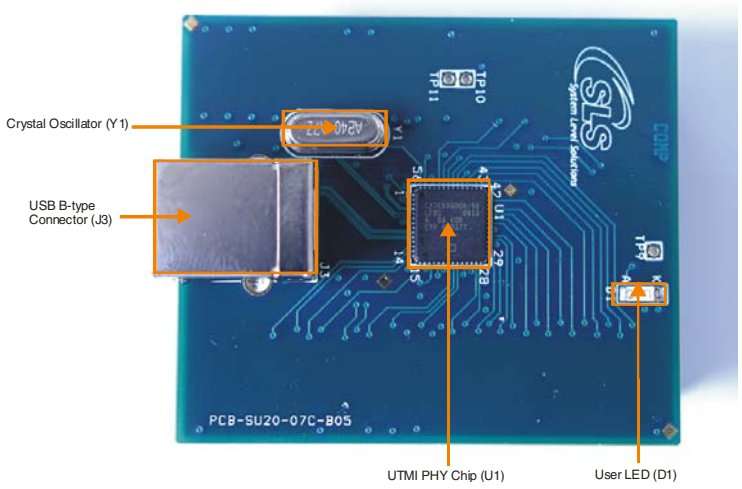


Table 2-1 below shows the summary of the board's components.

Table 2-1. USB 2.0 - UTMI Snap On Board Components & Interfaces

Board Reference	Name	Description	Page
Featured Device			
U1	CY7C68000A	UTMI (USB2.0 Transceiver Macro-cell Interface) -- PHY Chip	5
User Interfaces			
J3	USB 2.0 Connector	One USB 2.0 Device Connector (B-Type)	9

Table 2-1. USB 2.0 - UTMI Snap On Board Components & Interfaces

Board Reference	Name	Description	Page
Expansion Connectors			
JP2, JP3, JP4	Expansion Prototype Connector	These are the three female connectors used for mounting daughter card (In this case its USB2.0 Snap On Board) on the Development Kit having standard Santa Cruz short expansion male interface.	10
LEDs			
D1	User LED	User can use this LED to indicate any I/O Signals or debugging.	12
Clocks			
Y1	Crystal	Generates 24Mhz clock as an input for PHY Chip.	12

Featured Device

PHY Chip (U1)

USB 2.0 Snap On board contains PHY Chip which is physical layer transceiver. We used CY7C68000A PHY Chip which Contains 56 pins Operating at 3.3 volts to meet low voltage and low power requirements. This PHY Chip is a USB 2.0 transceiver, serial/deseriallizer, to a parallel interface of whether 16-bits at 30MHz or eight bits at 60MHz. It provides high speed physical layer interface that operates at a maximum allowable USB 2.0 bandwidth. This allows the system designer to keep the complex high speed analog USB components external to the digital ASIC/FPGA which decreases development time and associated risk. The Figure 2-1. displays the PHY Chip on the board.

The PHY chip is an ideal choice for physical layer transceiver of USB2.0 applications. Table 2-2 displays PHY Chip signals with its type & functionality.

Table 2-2. PHY Chip Signals

Pin #	Pin Name	Type	Pin Function
1	TXREADY	Output	**Transmit Data Ready**. If TXValid is asserted, the SIE must always have data available for clocking in to the TX Holding Register on the rising edge of the clock.
2	NSUSPEND	Input	**Suspend**. Places the Phy Chip in a mode that draws minimal power from supplies. Shuts down all blocks not necessary for Suspend/Resume operation.
3	RESET	Input	**Active High Reset**. Resets the entire chip.
4,8	AVCC	Power	**Analog VCC**
5	XTALOUT	Output	**Crystal Output**. Connect this signal to a 24Mhz crystal.
6	XTALIN	Input	**Crystal Input**. Connect this signal to a 24Mhz crystal.
7,11	AGND	Power	Analog Ground
9	DPLUS	I/O/Z	USB D + Signal
10	DMINUS	I/O/Z	USB D -Signal
12	XCVERSELECT	Input	**Transceiver Select**. This signal selects between the Full Speed (FS) and the High Speed (HS) transceivers: 0: HS transceiver enabled 1: FS transceiver enabled
13	TERMSELECT	Input	**Termination Select**. This signal selects between the Full Speed (FS) and the High Speed terminations: 0: HS termination 1: FS termination
14,15	OPMODE0/1	Input	**Operation Mode**. These signals select among various operational modes: 0 0: Normal Operation 0 1: Non- driving 1 0: Disable Bit Stuffing and NRZI encoding 1 1: Reserved
16,20,30,42,53,57	GND	Ground	Ground

Table 2-2. PHY Chip Signals

Pin #	Pin Name	Type	Pin Function
18,19	LINESTATE0/1	Output	**LineState**. These signals reflect the current state of the single-ended receivers. They are combinatorial until a “usable” CLK is available then they are synchronized to CLK. They directly reflect the current state of the D+(LineState0) and D- (LineState1) D- D+ 0 0: SE0 0 1: “J” State 1 0: “K” State 1 1: SE1
21	RXVALID	Output	**Receive Data Valid.** Indicates data bus has valid data.
22	RXACTIVE	Output	**Receive Active.** Indicates that the receive state machine has detected SYNC and is active.
23	RXERROR	Output	Receive Error. 0: Indicates no error 1: indicates receive error has been detected.
24	TRI_STATE	Input	**Tri-state Mode Enable** Places the CY7C68000A into Tri-state mode which tri-states all outputs and IO’s. Tri-state Mode can only be enabled while suspended. 0: Disables Tri-state Mode 1: Enables Tri-state Mode
25,35,40,47	RSVD1/2/3/4	Input	Reserved
26	DATA15	I/O	**Bidirectional Data Bus** This bidirectional bus is used as the upper eight bits of the data bus when in the 16-bit mode, and not used when in the 8-bit bidirectional mode. Under the 8-bit unidirectional mode these bits are used as outputs for data, selected by the TxValid signal.
27	DATA14	I/O	
29	DATA13	I/O	
31	DATA12	I/O	
33	DATA11	I/O	
34	DATA10	I/O	
36	DATA9	I/O	
37	DATA8	I/O	

Table 2-2. PHY Chip Signals

Pin #	Pin Name	Type	Pin Function
38	DATA7	I/O	**Bidirectional Data Bus** This bidirectional bus is used as the entire data bus in the 8-bit bidirectional mode or the least significant eight bits in the16-bit mode. Under the 8-bit unidirectional mode, these bits are used as inputs for data, selected by the RxValid signal.
39	DATA6	I/O	
41	DATA5	I/O	
43	DATA4	I/O	
44	DATA3	I/O	
46	DATA2	I/O	
48	DATA1	I/O	
49	DATA0	I/O	
17,28,32,45,55	VCC	Power	Connected to 3.3 V
50	CLK	Output	**Clock**. This output is used for clocking the parallel data (receive and transmit) on the data bus.
51	DATABUS16_8	Input	**Data Bus 16_8**. Selects between 8 and 16 bit data transfers. 1: 16-bit data path operation enabled. CLK = 30Mhz. 0: 8-bit data path operation enabled. When Uni_BIdi = 0, D[8:15] are undefined. When Uni_BIdi = 1, D[0:7] are valid on RxValid and D[8:15] are valid on TxValid. CLK = 60Mhz. *Note*: **DataBus16_8** is static after Power-on Reset (POR) and is only sampled at the end of Reset.
52	UNI_BIDI	Input	**Driving this pin HIGH enables the unidirectional mode when the 8-bit interface is selected**. Uni_Bidi is static after power on reset (POR).

Table 2-2. PHY Chip Signals			
Pin #	Pin Name	Type	Pin Function
54	TXVALID	Input	**Transmit Valid**. Indicates that the data bus is valid.
56	VALIDH	I/O	**ValidH**. This signal indicates that the high-order bits of a 16-bit data word presented on the Data bus are valid. • When **DataBus16_8** = 1 and **TXValid** = 0, **ValidH** is an output, indicating that the high order receive data byte on the Data bus is valid. • When **DataBus16_8 = 1** and **TXValid** = 1, ValidH is an input and indicates that the high order transmit data byte, presented in the Data bus by the transceiver, is valid. • When **DataBus16_8** =0, **ValidH** is undefined. The status of the receive low-order data byte is determined by RxValid and are presented on D0-D7.

User Interface

This section describes user interfaces which includes USB 2.0 B-Type Connector.

USB B-Type Connector (J3)

USB 2.0 Snap On board incorporates USB B-Type Connector connected with PHY chip. Figure 2-1. displays the USB B-Type connector on the board.

Pin mapping of connector with PHY chip is shown in Table 2-3

Table 2-3. USB B-Type Connector to PHY Chip Connection		
Connector Pin #	Signal	PHY Chip Pin #
1	VBUS	--
2	D-	10
3	D+	9
4	GND	--

Expansion Connectors

This section describes the expansion connectors on the USB 2.0 Snap On board.

Expansion Prototype Connectors (JP2,JP3,JP4)

Headers JP2, JP3, and JP4 collectively form the standard-footprint called Santa Cruz short expansion headers (female), which are 14 pins, 40pins and 20 pins respectively. These are mechanically stable connections that can be used for mounting daughter card (USB 2.0 Snap On Board) on to any Development Kit having standard Santa Cruz short expansion male interface.

The expansion prototype connector interface includes

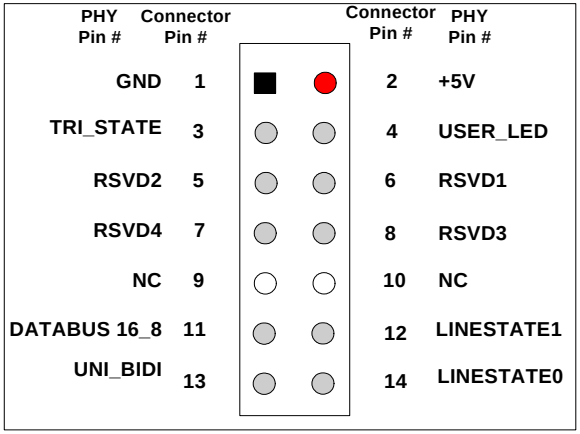
- 74 pins for prototyping (Out of which 43 I/O pins connect to user I/O pins and 3 dedicated clock pins on the Cyclone device)
- An Active LOW Power On Reset signal
- Five regulated 3.3V power-supply pins (1A total max load)
- One regulated 5V power-supply pin. (1A total max load)
- Numerous ground connections

The output logic level on the expansion prototype connector pins is +5 Volts for the UP3 board but for all other host boards, it may vary.

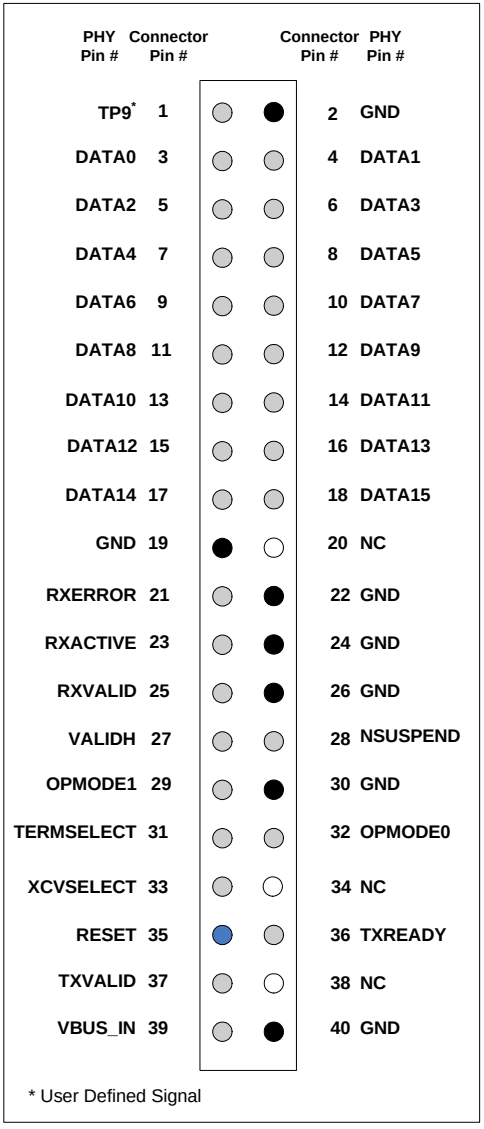
Figure 2-2. shows the pin description of the connectors JP2, JP3 & JP4.

Figure 2-2. Pin Description of Expansion Prototype Connector-JP2,JP3,JP4

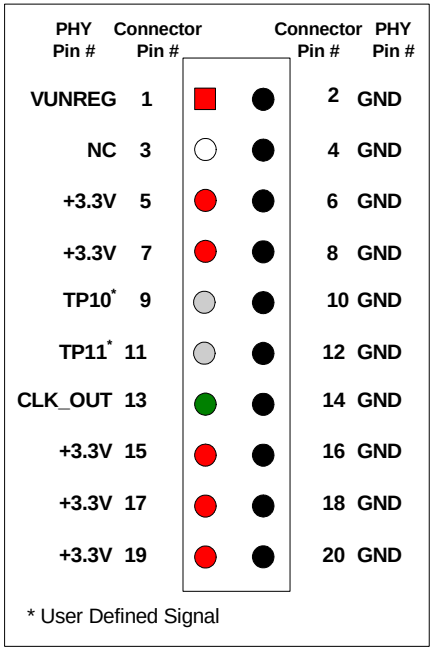
JP2



JP3



JP4



LEDs

This section describes the User LED (D1) on the USB 2.0 Snap on board.

User LED (D1)

The USB 2.0 Snap On Board has 1 general purpose user LED (D1) as shown in Figure 2-1. User can use this LED as an indication of any required output.

Clocks

This section describes the components used to set the USB 2.0 Snap on board clocking options.

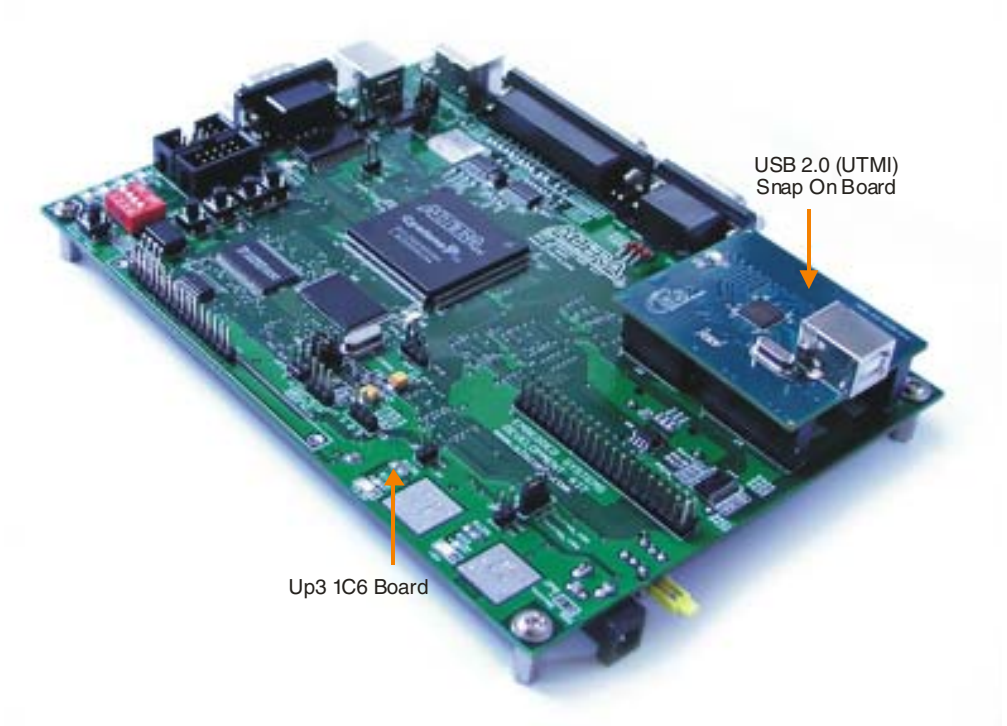
Crystal (Y1)

The USB 2.0 Snap On Board includes 24 MHz Crystal which is used to provide reference clock for PHY chip. Crystal clock input is on pin no 6 and crystal clock output is on pin 5 of PHY Chip.Figure 2-1. displays Crystal on the board.

3. Signal Mapping

The three (F) headers (JP2, JP3, JP4) on USB 2.0 Snap On board snaps on to three (M) SantaCruz headers (J2,J4,J3) of UP3 Education kit as shown in Figure 3-1.

Figure 3-1. Connection of USB 2.0 - UTMI Snap On Board with UP3 Education kit



Mapping PHY Pins with Core I/O

Table 3-1 shows the PHY Signals with Core I/O.

Table 3-1. Mapping PHY Signals with Core I/O

PHY Chip Signal	Header Pin #	Core Signals
CLK_OUT	JP4.13	phy_clk_pad_i
RESET	JP3.35	Reset
NSUSPEND	JP2.14	SuspendM_pad_o
DATABUS16_8	JP2.11	DataBus16_8
UNI_BIDI	JP2.13	UNI-BIDI
DATA0	JP3.3	Data[0]
DATA1	JP3.4	Data[1]
DATA2	JP3.5	Data[2]
DATA3	JP3.6	Data[3]
DATA4	JP3.7	Data[4]
DATA5	JP3.8	Data[5]
DATA6	JP3.9	Data[6]
DATA7	JP3.10	Data[7]
DATA8	JP3.11	Data[8]
DATA9	JP3.12	Data[9]
DATA10	JP3.13	Data[10]
DATA11	JP3.14	Data[11]
DATA12	JP3.15	Data[12]
DATA13	JP3.16	Data[13]
DATA14	JP3.17	Data[14]
DATA15	JP3.18	Data[15]
RXERROR	JP3.21	RxError_pad_i
RXACTIVE	JP3.23	RxActive_pad_i
RXVALID	JP3.25	RxValid_pad_i
LINESTATE0	JP2.12	LineState_pad_i [0]
LINESTATE1	JP2.14	LineState_pad_i [1]
OPMODE0	JP3.32	OpMode_pad_o [0]

Table 3-1. Mapping PHY Signals with Core I/O

PHY Chip Signal	Header Pin #	Core Signals
OPMODE1	JP3.29	OpMode_pad_o [1]
TERMSELECT	JP3.31	TermSel_pad_o
XCVERSELECT	JP3.33	XcvSelect_pad_o
TXVALID	JP3.37	TxValid_pad_o
TXREADY	JP3.36	TxReady_pad_i
VBUS_IN	JP3.39	usb_vbus_pad_i
VALIDH	JP3.27	-
NSUSPEND	JP3.28	SuspendM