Addition and Subtraction with signed - 2's Complement Data

The addition of two numbers in signed - 2's complement form consists of adding the nos with the sign bits treated the same as the other bits of the no. A carry - out of the sign - bit position is discarded.

Subtraction consists of first taking the 2's complement of the subtrahend and then adding it to the minuend.

When two nos of n digits each are added and that an overflow occurs when the sum occupies n+1 digits, we say by inspecting the last two carries An overflow can be detected when the two carries are applied to an XOR gate, the overflow is detected when the o/p of the gate is equal to 1.

The register configuration for the hardware implementation is shown below. This is the same configuration as for the sign bits are not seperated