Design Rules Verification Report

Filename : E:\undergrad\eee4022S-2017\NPSC\hardware\design\weekdays\Weekdays.PcbDoc

Warnings 0
Rule Violations 33

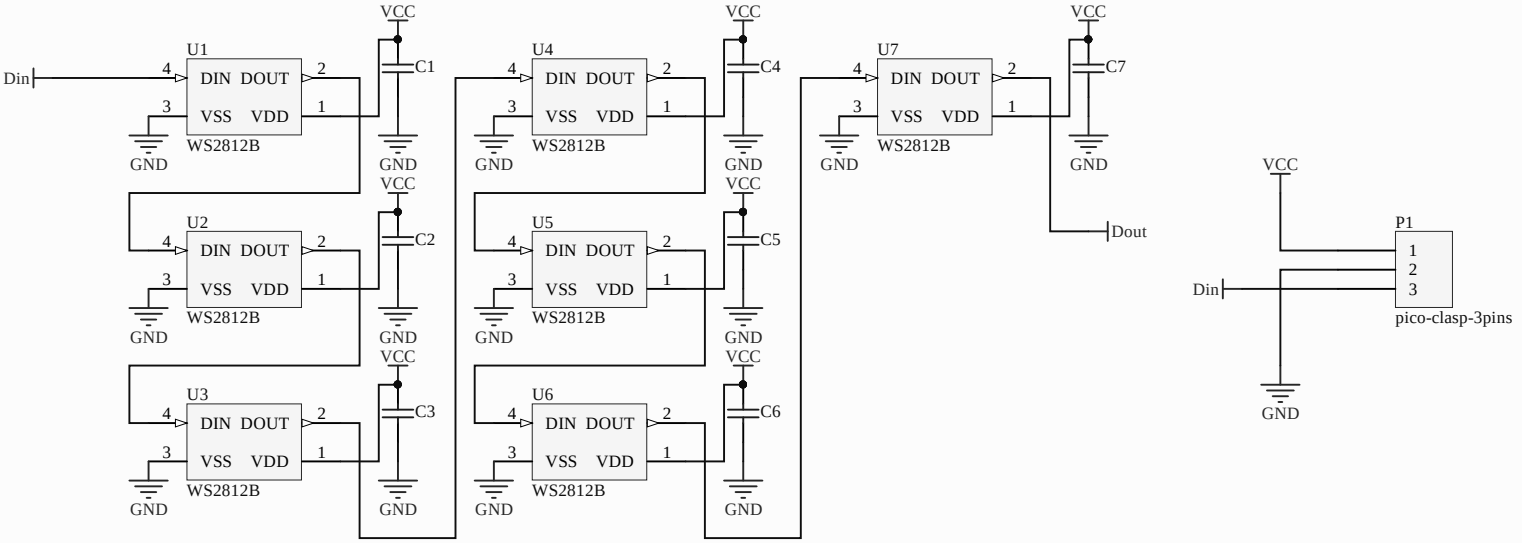
Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.5mm) (Max=3mm) (Preferred=1mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	2
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	31
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Room Weekday (Bounding Region = (35.3mm, 68.1mm, 151.3mm, 86.1mm) (InComponentClass('Weekday'))	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	33

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad P1-2(7.9mm,6.4mm) on Bottom Layer And Pad P1-1(7.9mm,5.4mm) on
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad P1-3(7.9mm,7.4mm) on Bottom Layer And Pad P1-2(7.9mm,6.4mm) on

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.247mm < 0.254mm) Between Track (2.2mm,3.9mm)(2.825mm,3.9mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.173mm < 0.254mm) Between Track (2.2mm,8.9mm)(2.8mm,8.9mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (9.225mm,8.55mm)(9.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (10.375mm,8.55mm)(10.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (Collision < 0.254mm) Between Text "DIN" (9mm,7mm) on Bottom Overlay And Pad C1-2(9.8mm,7.8mm) on
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (9.225mm,8.55mm)(9.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (10.375mm,8.55mm)(10.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (24.225mm,8.55mm)(24.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (25.375mm,8.55mm)(25.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (24.225mm,8.55mm)(24.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (25.375mm,8.55mm)(25.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (40.375mm,8.55mm)(40.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (39.225mm,8.55mm)(39.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (40.375mm,8.55mm)(40.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (39.225mm,8.55mm)(39.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (54.225mm,8.55mm)(54.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (55.375mm,8.55mm)(55.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (54.225mm,8.55mm)(54.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (55.375mm,8.55mm)(55.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (70.375mm,8.55mm)(70.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (69.225mm,8.55mm)(69.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (70.375mm,8.55mm)(70.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (69.225mm,8.55mm)(69.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (85.375mm,8.55mm)(85.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (84.225mm,8.55mm)(84.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (85.375mm,8.55mm)(85.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (84.225mm,8.55mm)(84.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (99.225mm,8.55mm)(99.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (100.375mm,8.55mm)(100.375mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (99.225mm,8.55mm)(99.225mm,8.65mm) on Bottom Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.175mm < 0.254mm) Between Track (100.375mm,8.55mm)(100.375mm,8.65mm) on Bottom Overlay And Pad

Comment	Description	Designator	Footprint	LibRef	Quantity
CAP 0.5pF 10V 0805(2012)	CAP 0.5pF 10V ±0.5pF 0805 (2012 Metric) Thickness 1mm SMD	C1, C2, C3, C4, C5, C6, C7	CAPC0805(2012)100_L	CMP-1036-00005-1	7
pico-clasp-3pins	3 pins pico clasp	P1	3 pins pico-clasp	pico-clasp-3	1
WS2812B	Intelligent Control LED Integrated Light Source, 3.5 to 5.3 V, -25 to 80 degC, 4-Pin SMD, RoHS, Bulk	U1, U2, U3, U4, U5, U6, U7	ADAI-WS2812B_V	CMP-1740-00005-1	7



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