



# An Integrated Optical Parallel Adder as a First Step towards Light Speed Data Processing

Tohru ISHIHARA<sup>†</sup>, Akihiko SHINYA<sup>‡</sup>, Koji INOUE<sup>§</sup>,  
Kengo NOZAKI<sup>‡</sup> and Masaya NOTOMI<sup>‡</sup>

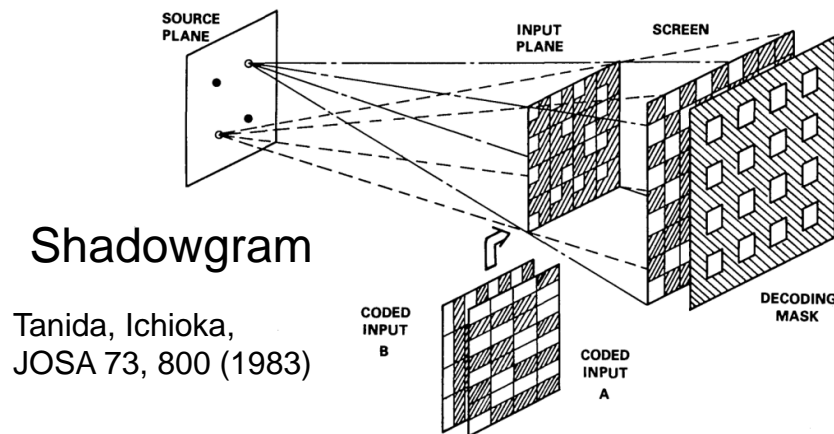
<sup>†</sup>Kyoto University, <sup>‡</sup>NTT Nanophotonics center, <sup>§</sup> Kyushu University

# History of Optical Computing

## ■ Opt. computers

Intensively studied in 1980's, but CMOS computers are much more superior to the optical computers

Based on optical filters

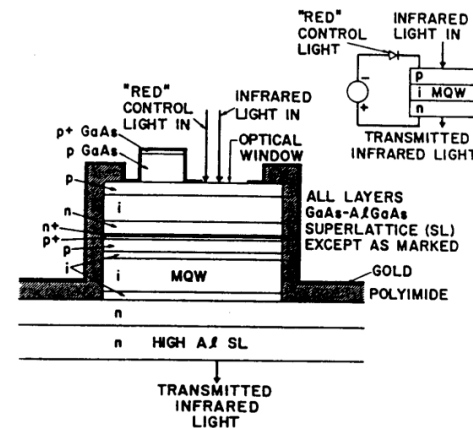


Shadowgram

Tanida, Ichioka,  
JOSA 73, 800 (1983)

Hard to miniaturize

Based on optical transistors



SEED  
(Bell Labs.)

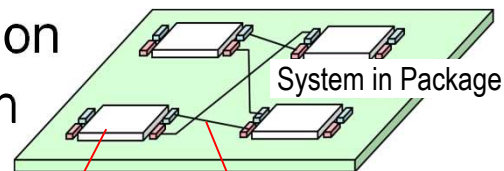
Miller et al.  
OQE 22, S61 (1990)

Lower performance than CMOS

## ■ Opt. interconnect

In 2000's, optical interconnects got into computers  
Intel, IBM, PETRA lead investigation (Si photonics)

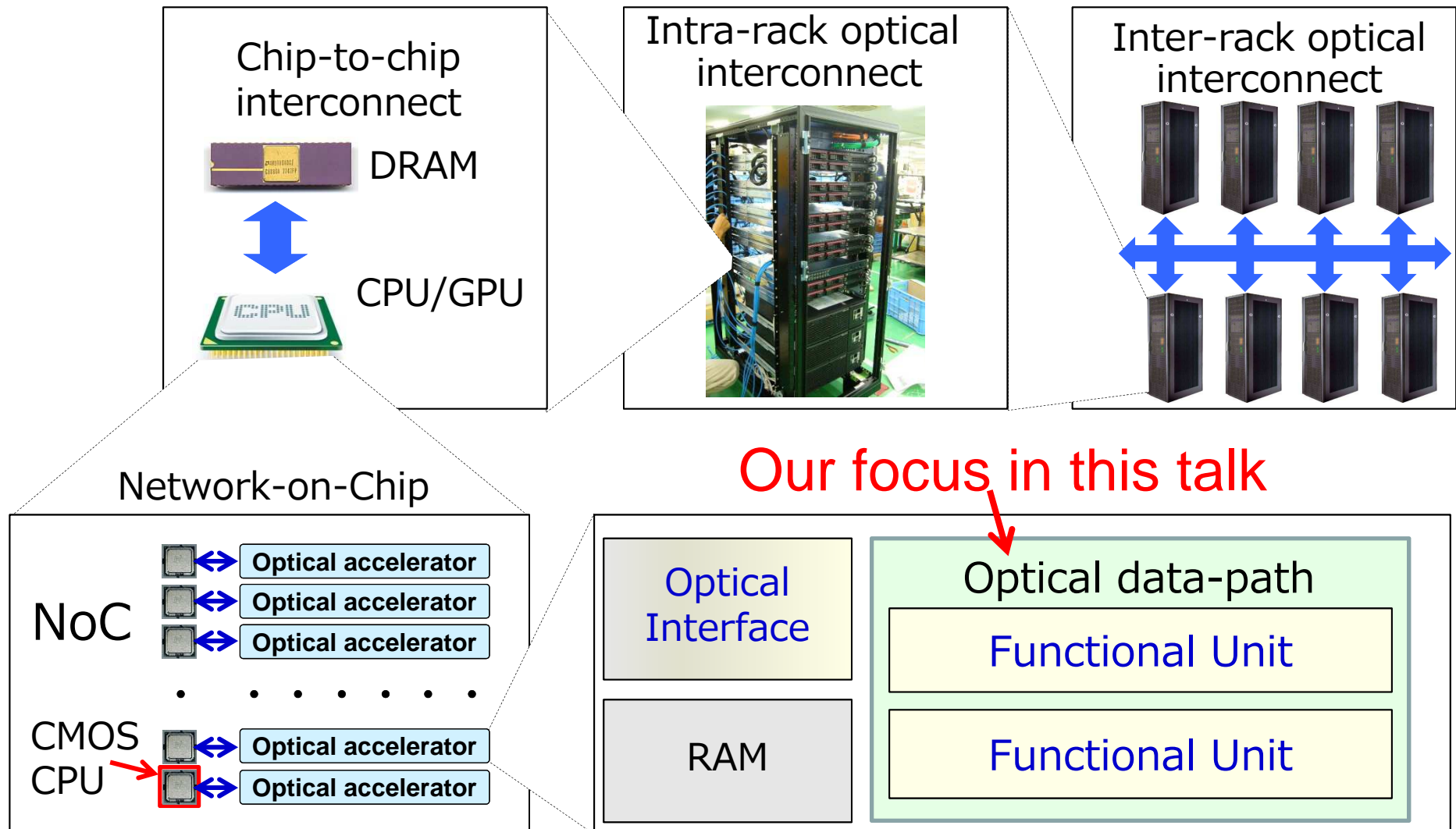
Electronics → computation  
Optics → communication



CPU Optical interconnect

Only for interconnect ?

# Beyond Optical Communication



# Basics of Optical Switches

## ■ Opt. gates

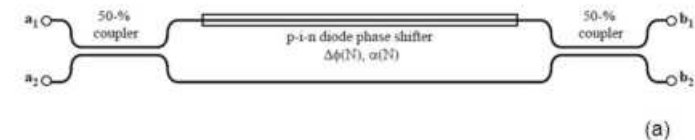
Speed of light in vacuum =  $3.00 \times 10^8$  m/s

If reflective index=3, speed =  $1.00 \times 10^8$  m/s

→ time for traveling 1 mm = 10 ps

E.g. Si MZI 2x2 crossbar switch

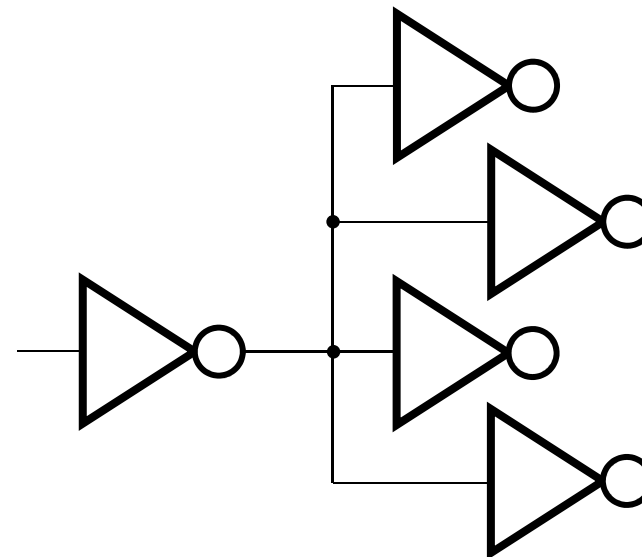
$L = 10$  mm, propagation delay = 100 ps



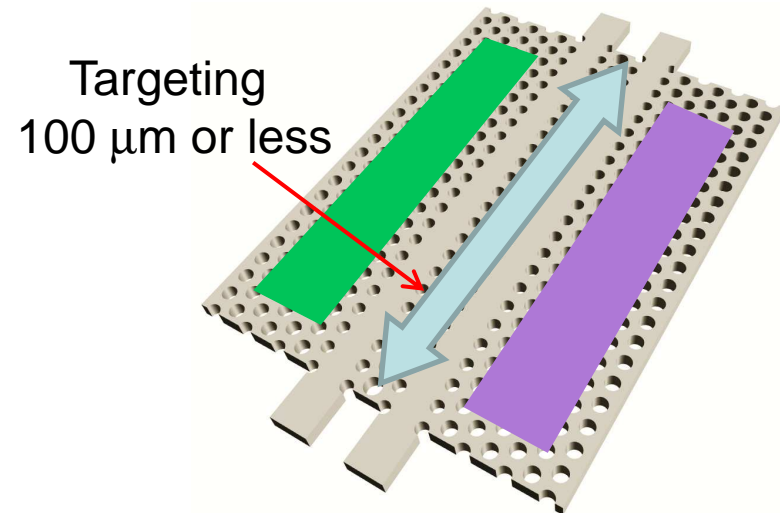
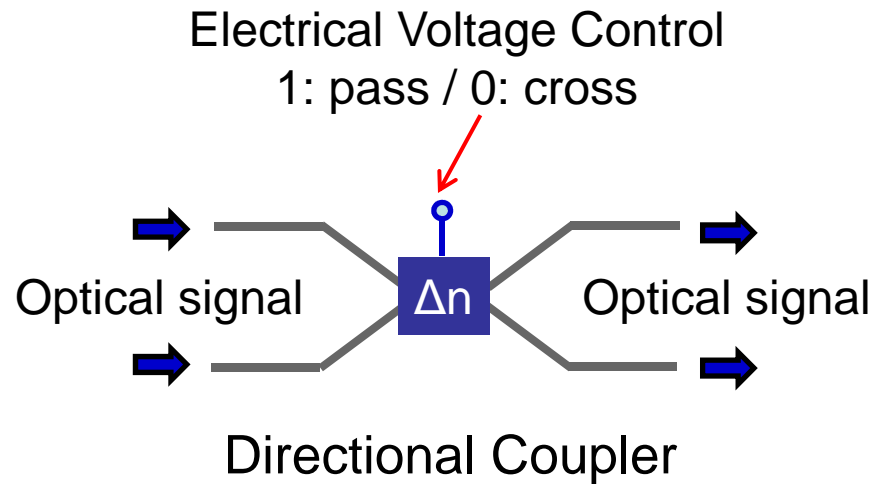
## ■ CMOS gates

E.g. Fan-out 4 inverter

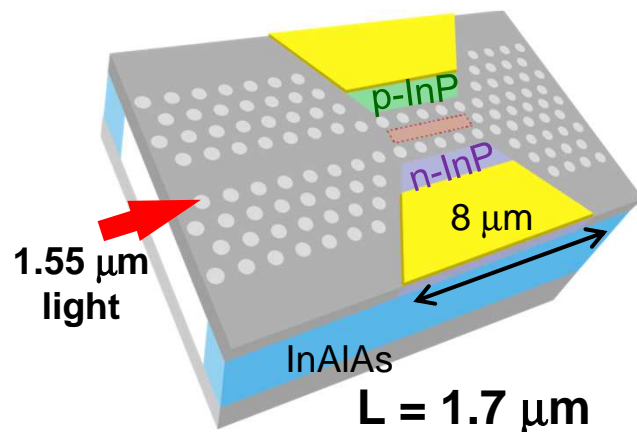
Propagation delay = 10 to 20 ps



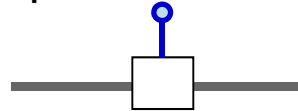
# Optical Pass Gate



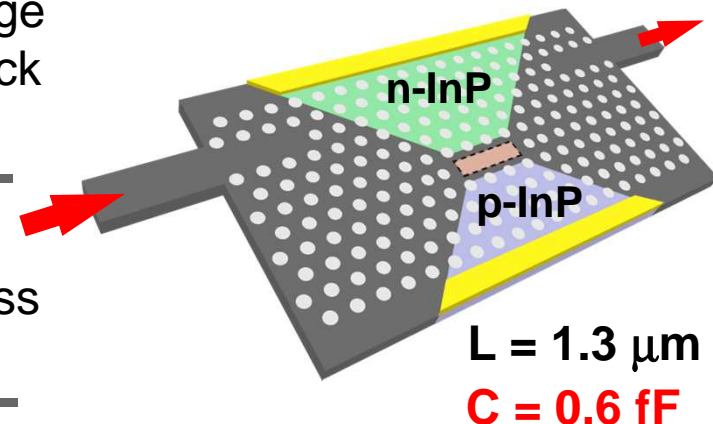
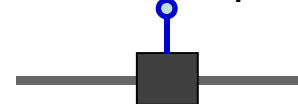
## Photo Detector



Electrical Voltage  
1: pass / 0: block



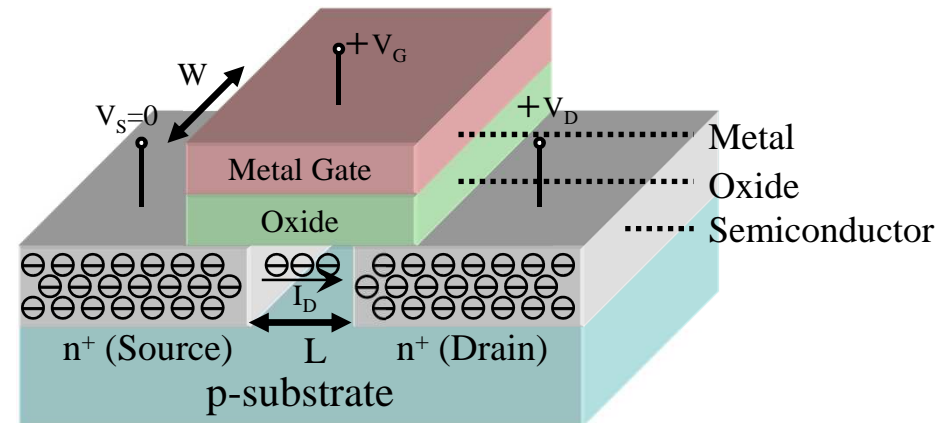
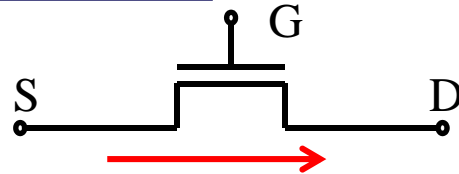
1: block / 0: pass



# Principle Optical Pass Gate

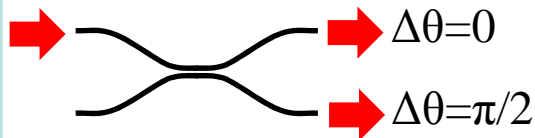
## ■ MOS Transistor

Controlled by gate voltage



## ■ Optical Switch

### Directional Coupler



Phase shifted  
by  $+\pi/2$  if  
crossed

### Phase shifter

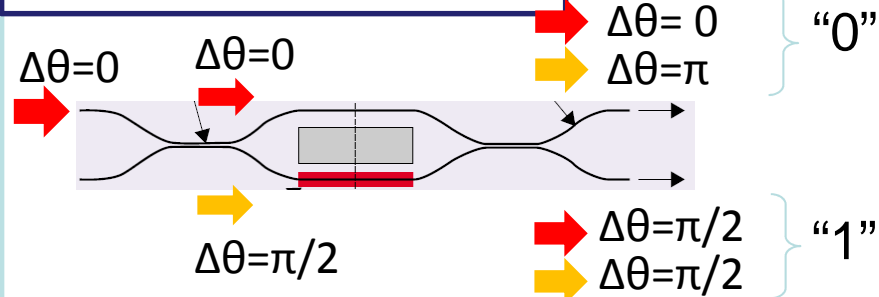
Voltage  $V_\pi$

If ON, phase shifted by  $\pi$

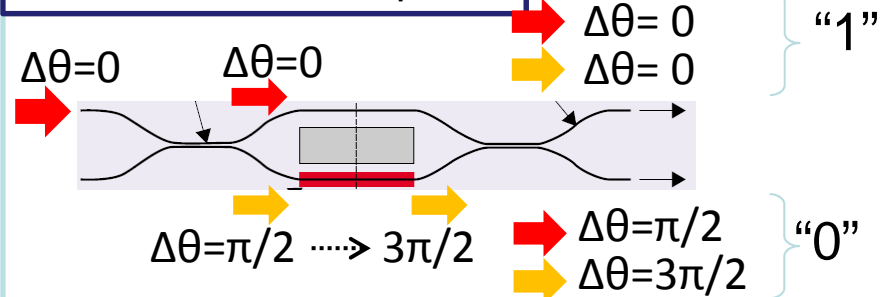


Electro-Optic Effect:  
Reflective index moves

### Phase shifter OFF (cross)



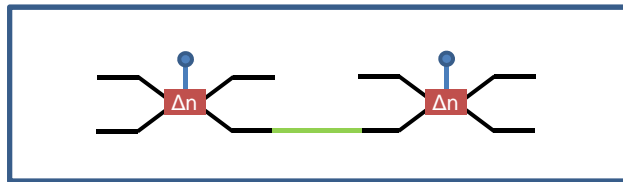
### Phase shifter ON (pass)



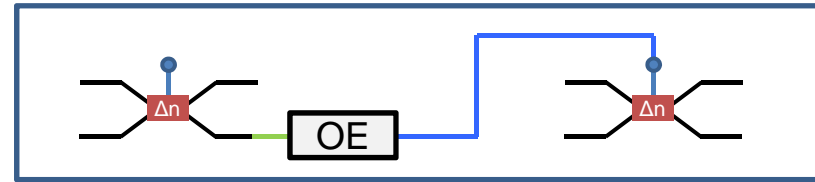
# Why Optical PG for Data Path?

- Good at data path operation
  - ✓ Light speed operation

Good at serial connection  
(light speed)

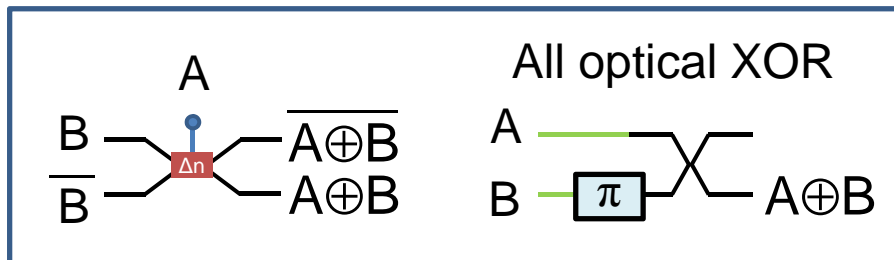


NOT good at cascade connection  
(OE & switching delay involved)

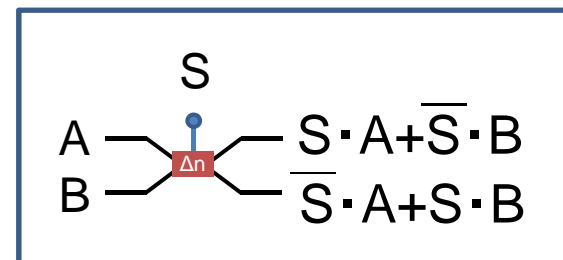


- ✓ Good at pass/cross propagations (XOR and MUX)

XOR

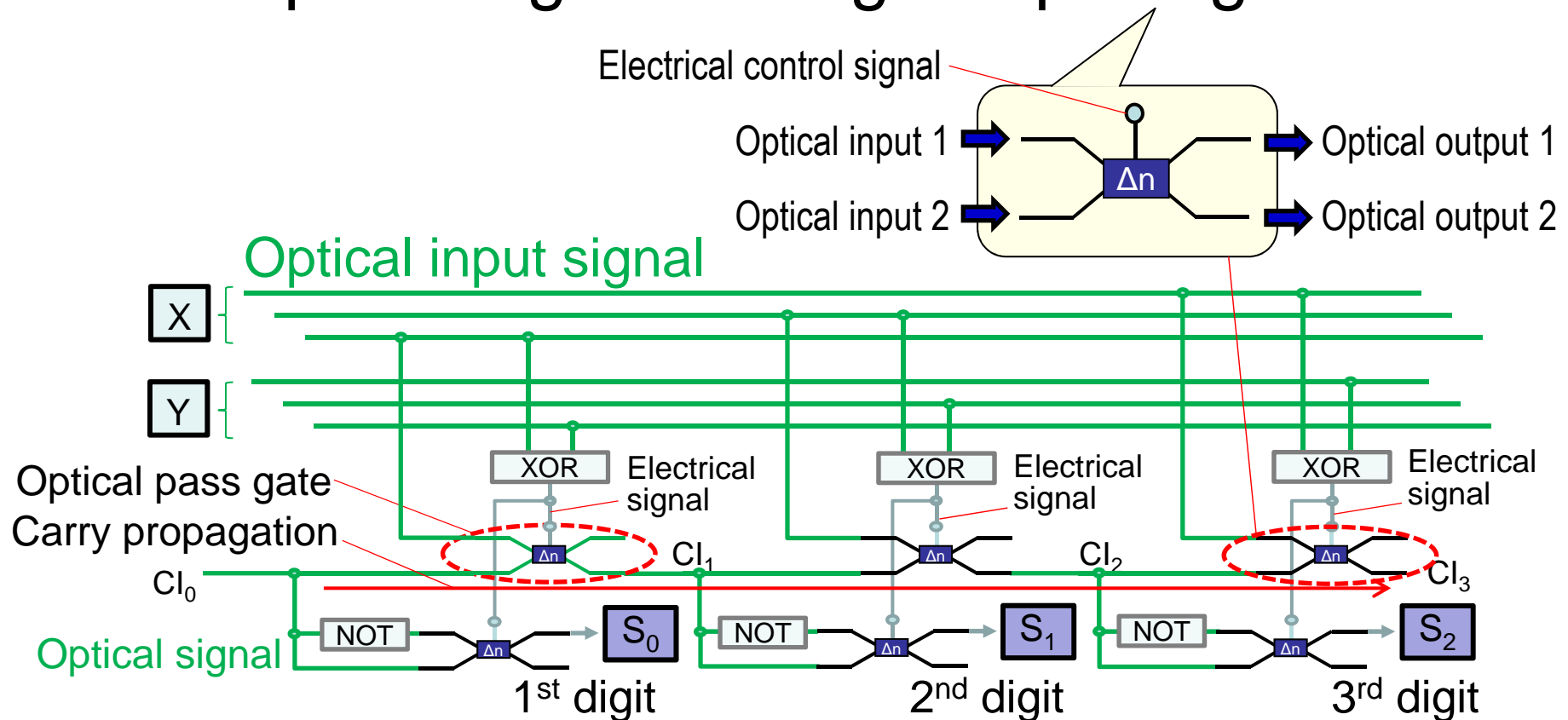


MUX



# Optical Data Processing

- Computation can be done by just passing the optical signal through a “pass gate”

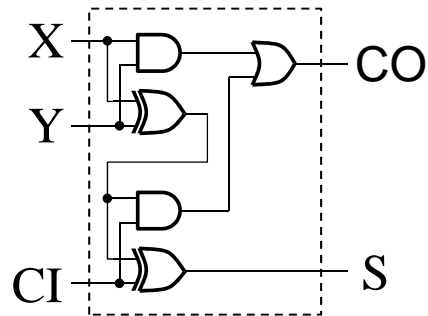




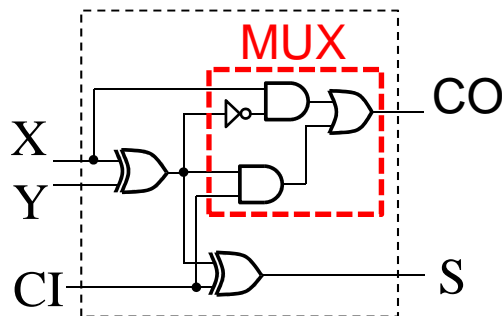
# Arithmetic Operation with OPG

- XOR/MUX-dominant data-path operation
  - ✓ Parallel Adder, Multiplier, and Barrel Shifter etc.

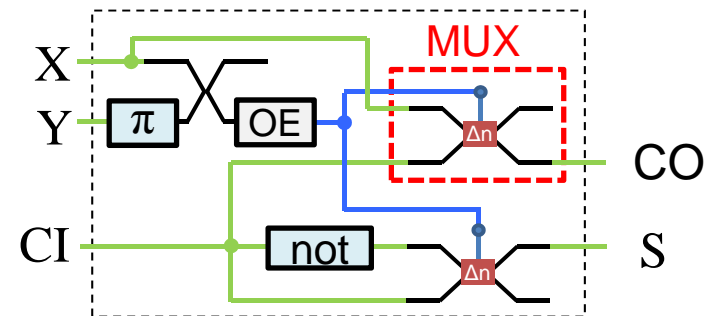
Full Adder (AOI logic)



Full Adder (modified)



Full Adder (OPG logic)



- ✓ Parallel adder as a first step
  - Can be constructed with serial connections only

# Optical Full Adder

Library Cells in  
OptiSPICE simulator  
(Optoelectronic  
circuit simulator)

1: through, 0:cross

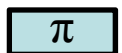
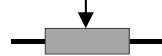


1: pass

0: pass

0: block

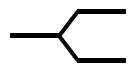
1: block



Phase shifter



OE conversion

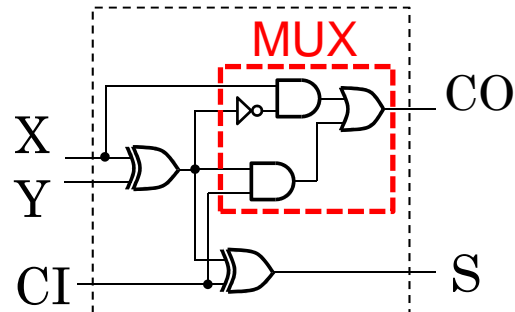


Y splitter

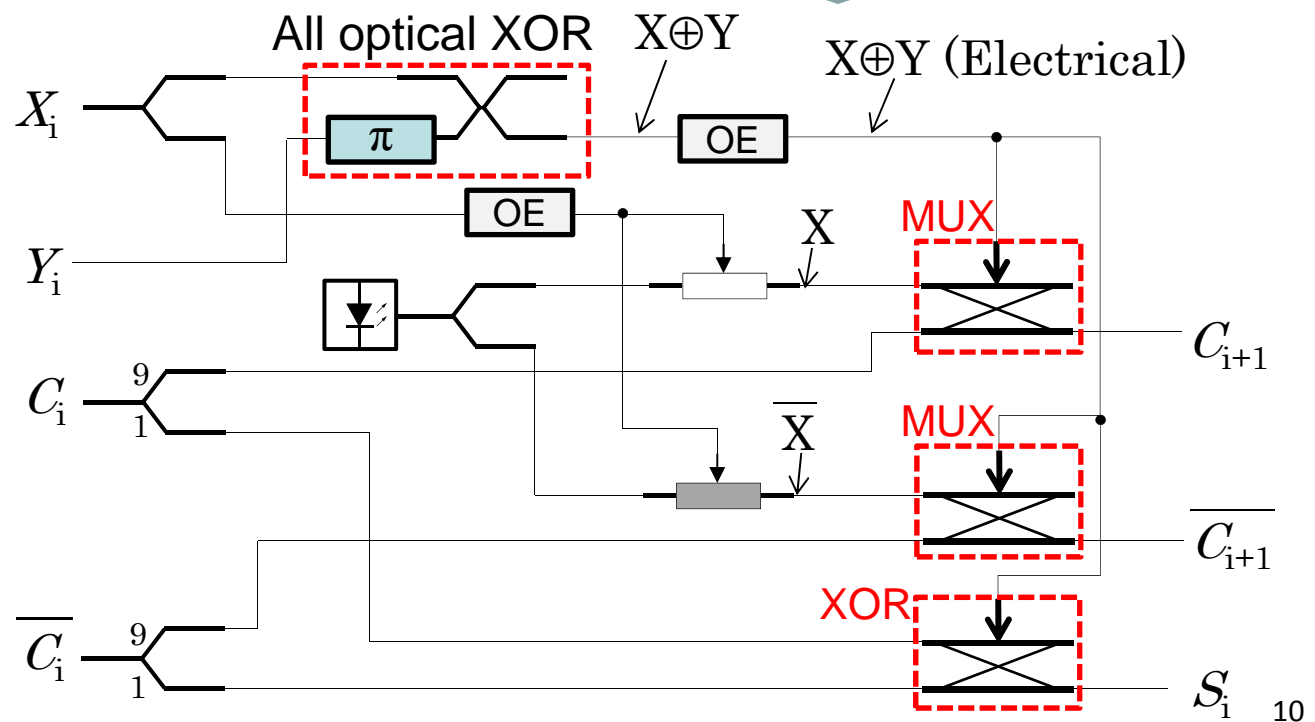
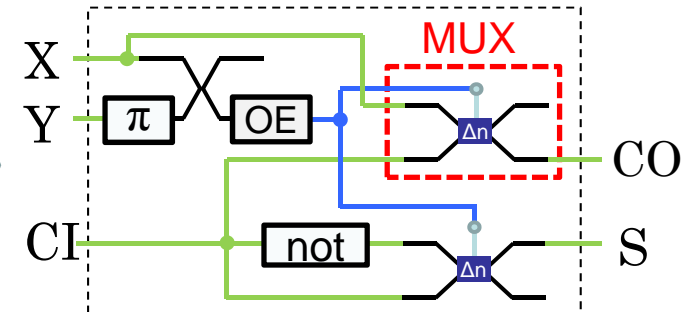


X coupler

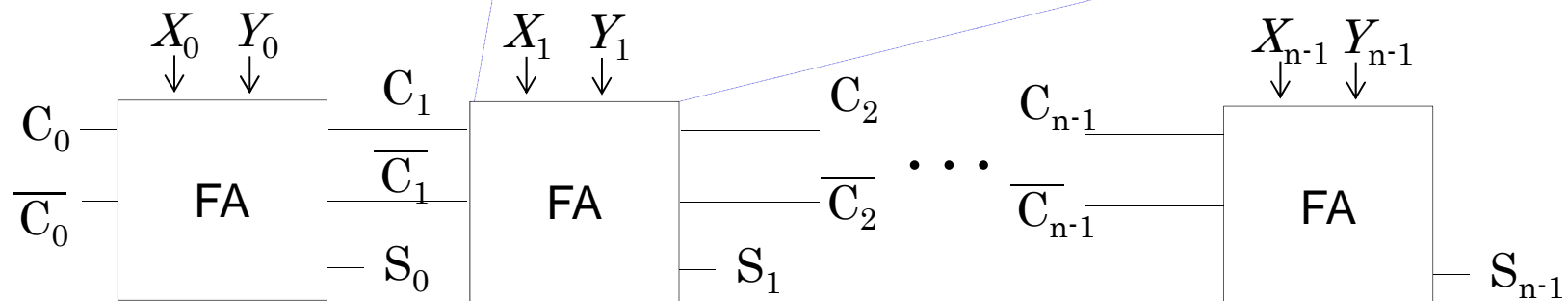
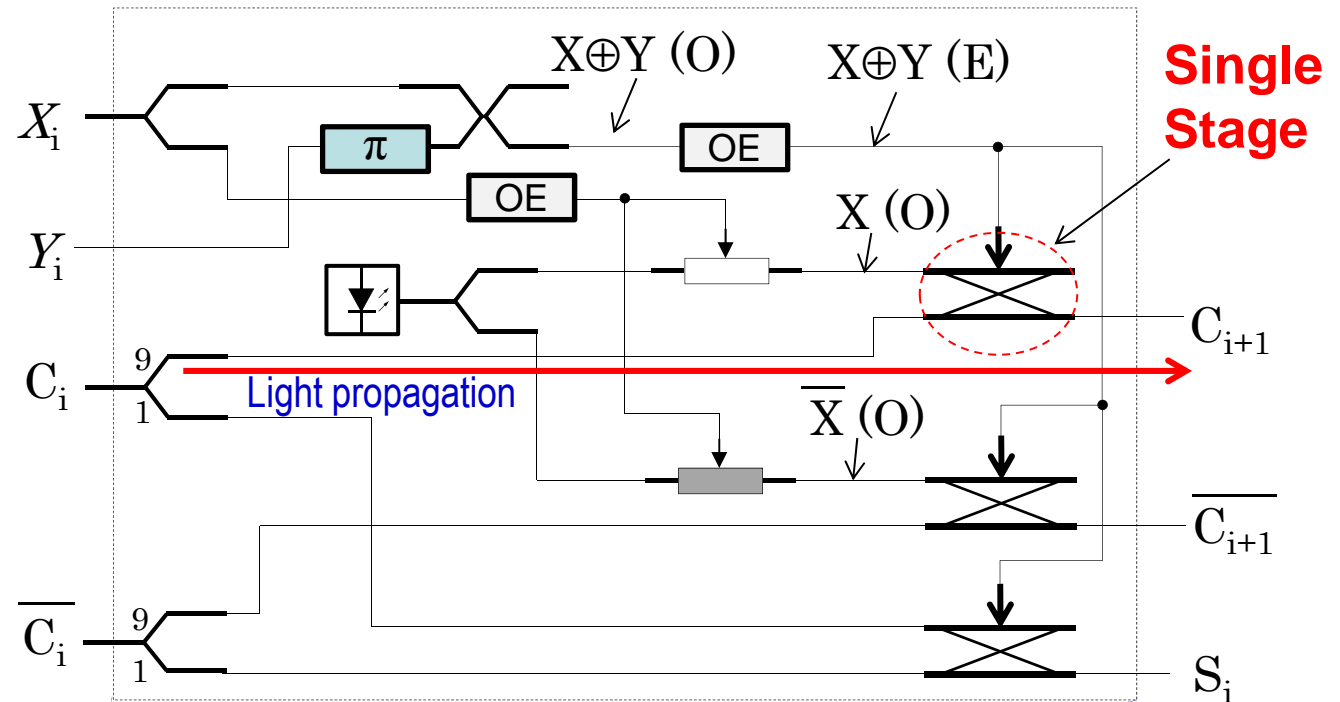
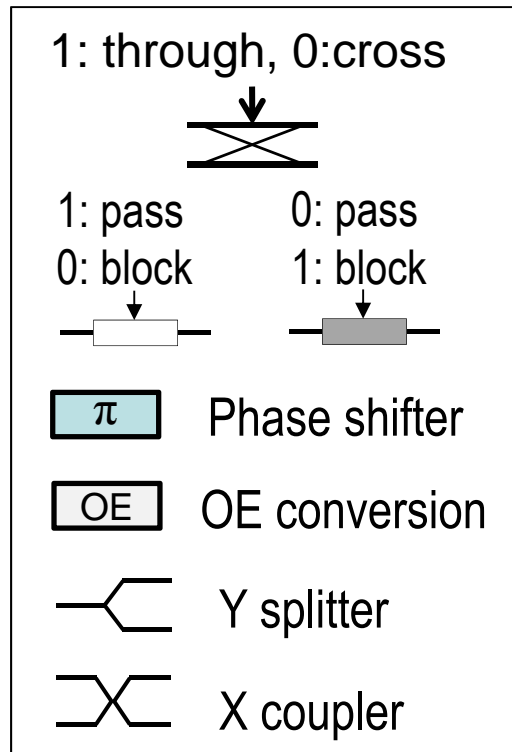
Full Adder (AOI logic)



Full Adder (OPG logic)

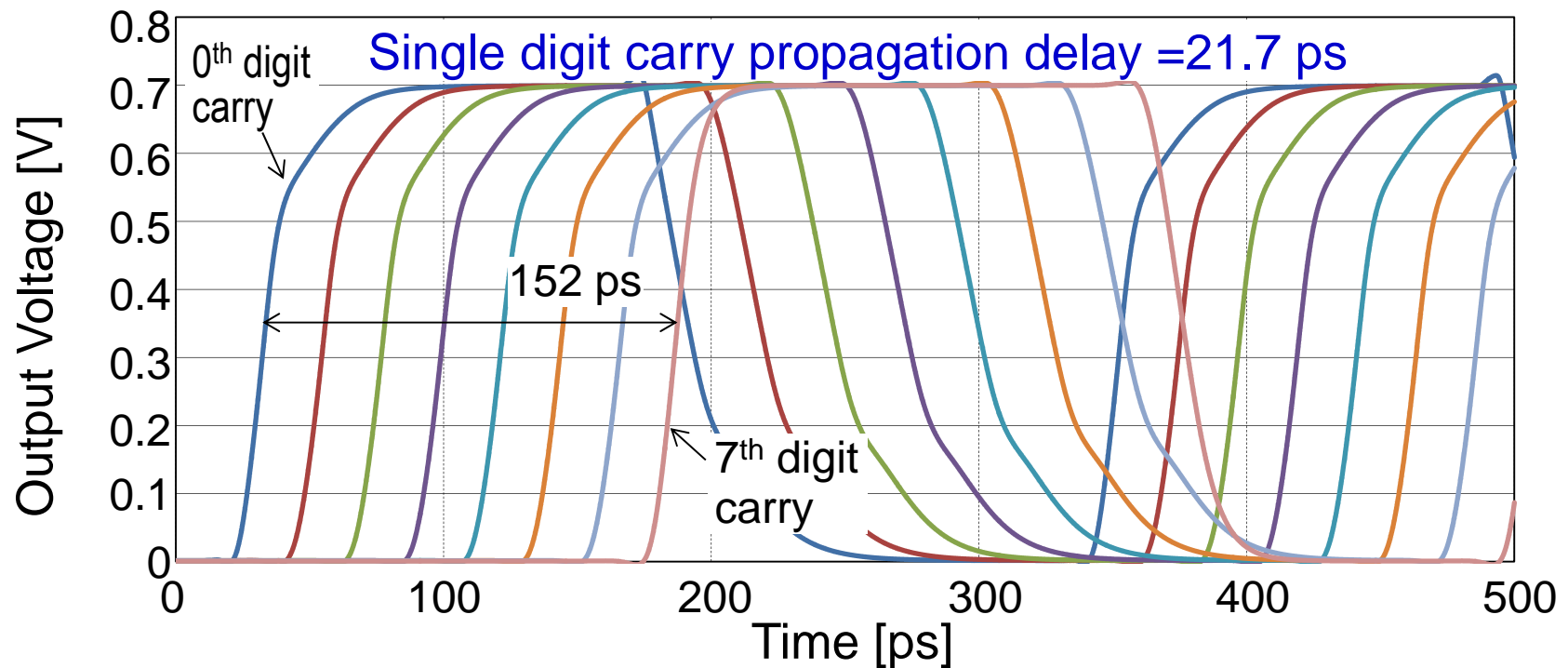
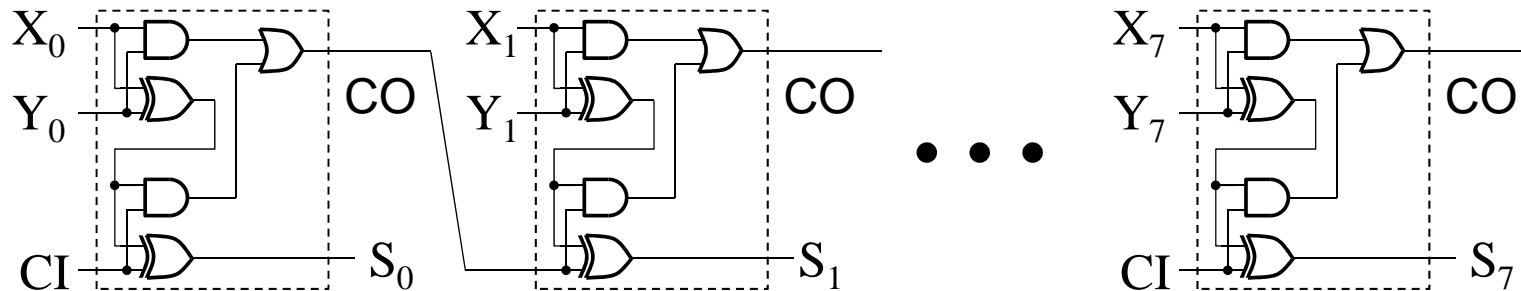


# Design and Evaluation: 8-bit Adder



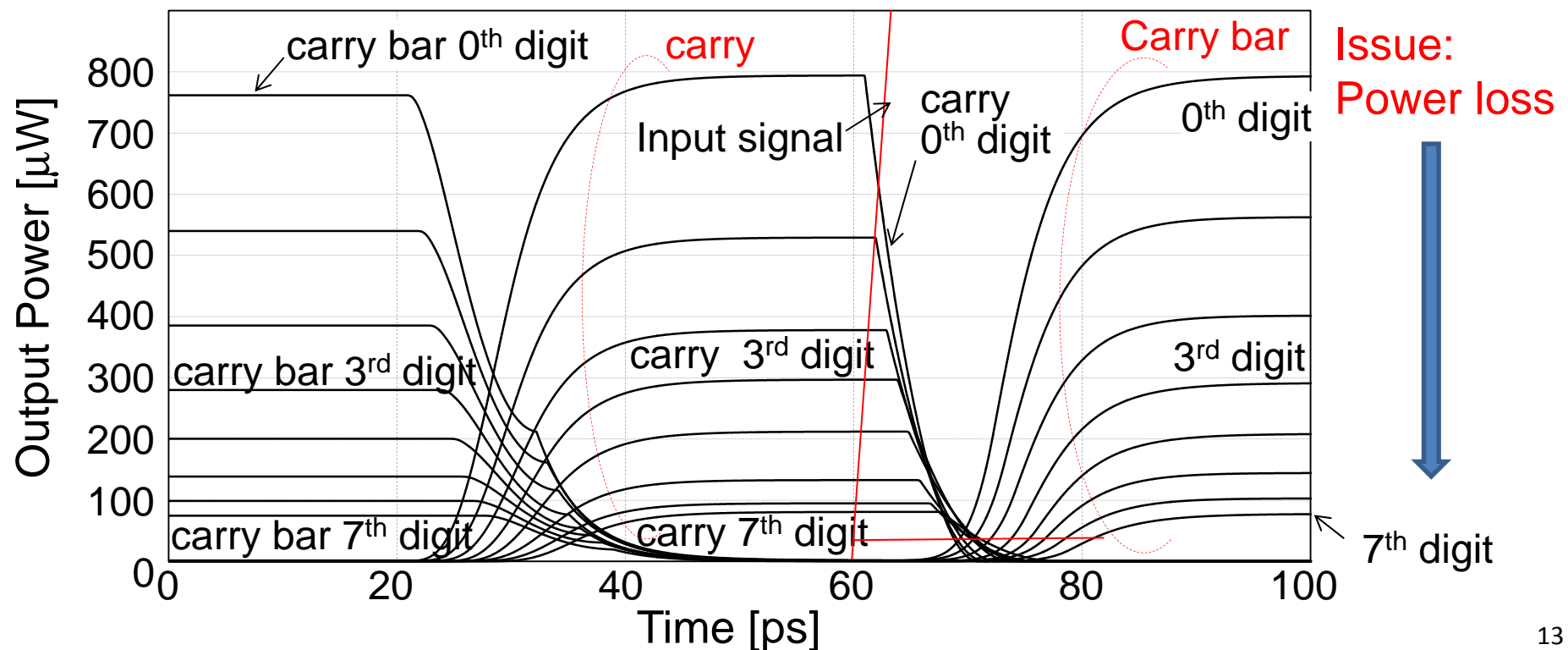
# 8-bit CMOS Adder as Comparison

16 nm High Performance CMOS Technology PTM



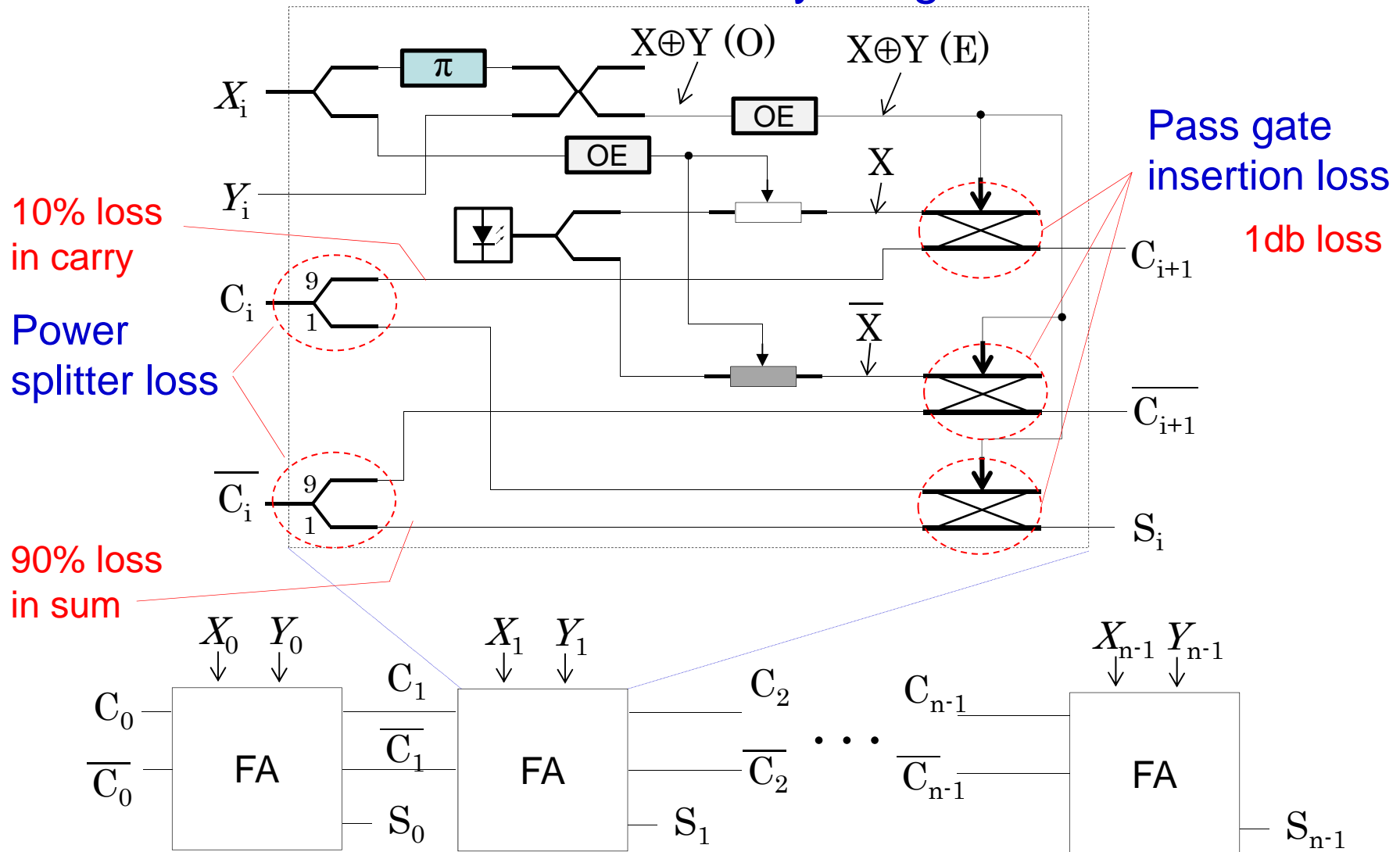
# Results of OptiSPICE Simulation

- Optoelectronic Circuit Simulator (HSPICE engine)
- Light-speed parallel adder operation confirmed
  - Per stage delay: ~1ps, Initial OE and switching delay: ~10ps
  - 8-bit CMOS adder with 16nm HP PTM: 174 ps



# Power Loss in Adder Operation

Power halves every 2 digits



# Related Work

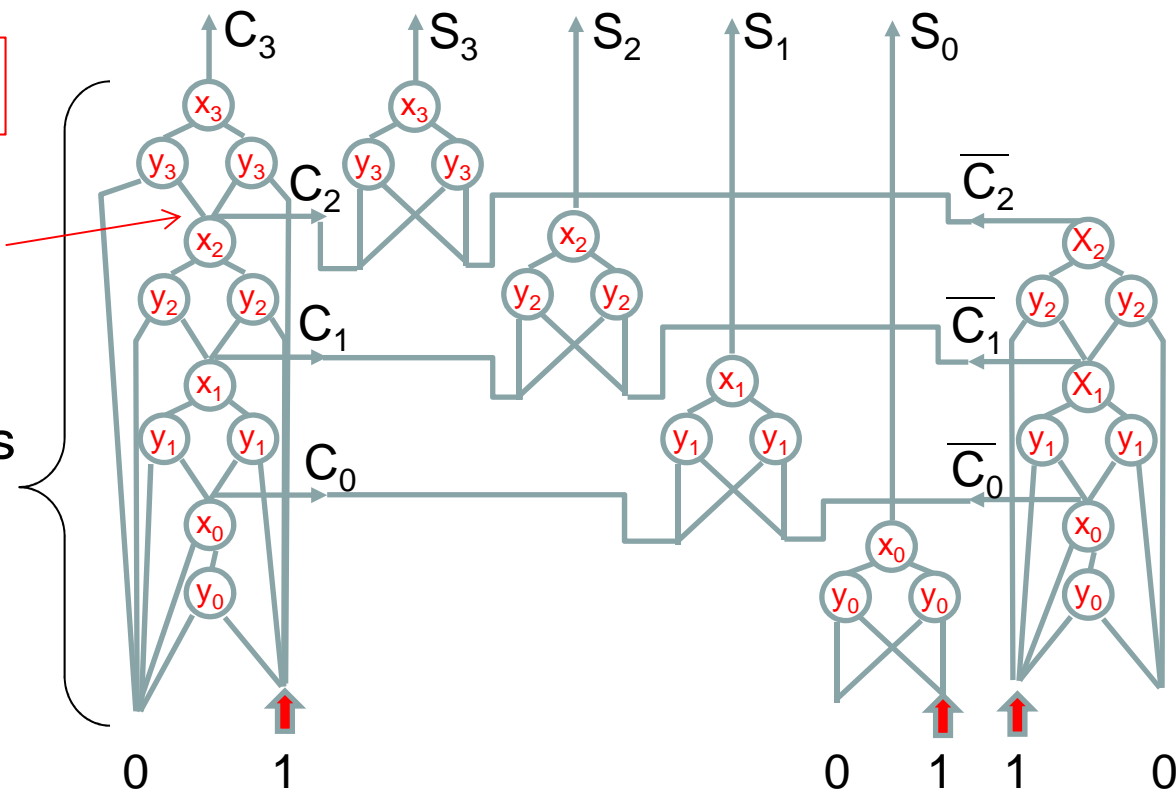
- Parallel adder based on shared BDD

T. Asai, Y. Amemiya, and M. Kosiba, "A Photonic-Crystal Logic Circuit Based on the Binary Decision Diagram," in *Proc. of IWPECS*, T4-14, March 2000.

72% loss per digit

Max fan-out = 4  
Large power loss

Serial connections  
= # digits x 2  
Large power loss



# Summary

- 8-bit parallel adder is designed with OPG
- Light-speed operation is confirmed
  - Per digit delay: OPG ~1 ps, CMOS 22 ps
  - 8-bit total delay: OPG ~17 ps, CMOS 174 ps
- Power loss is big issue to be resolved
  - Per digit power loss ~30%
- Future work
  - Extend it to more complicated functions