中国科学技术大学计算机学院
《计算机组成原理》报告

实验题目：运算器及其应用

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计算机实验教学中心制

【实验目的】

- 掌握算术逻辑单元（ALU）的功能
- 掌握数据通路和控制器的设计方法
- 掌握组合电路和时序电路，以及参数化和结构化的 Verilog 描述方法
- 了解查看电路性能和资源使用情况

【实验环境】

Vivado，fpgaol.ustc.edu.cn（FPGAOL）

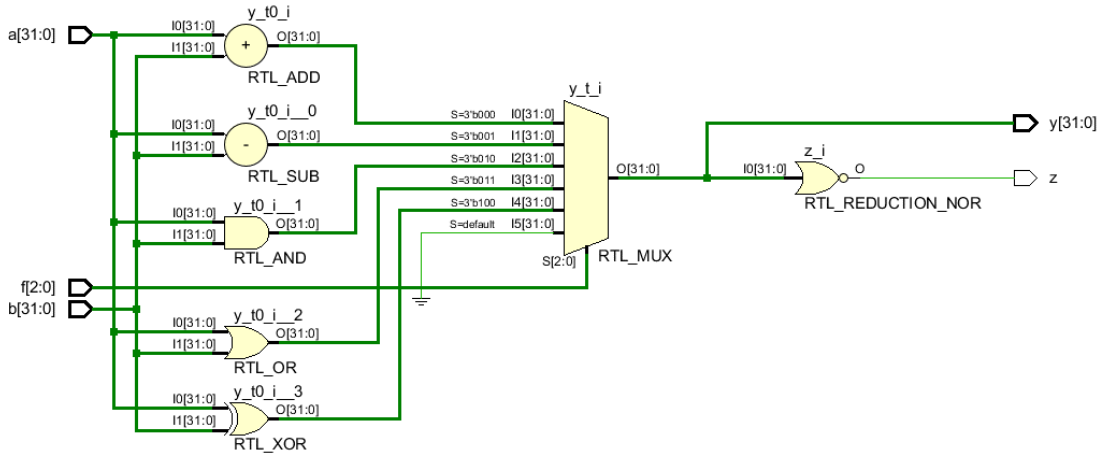
【实验过程】

题目一：32 位操作数 ALU

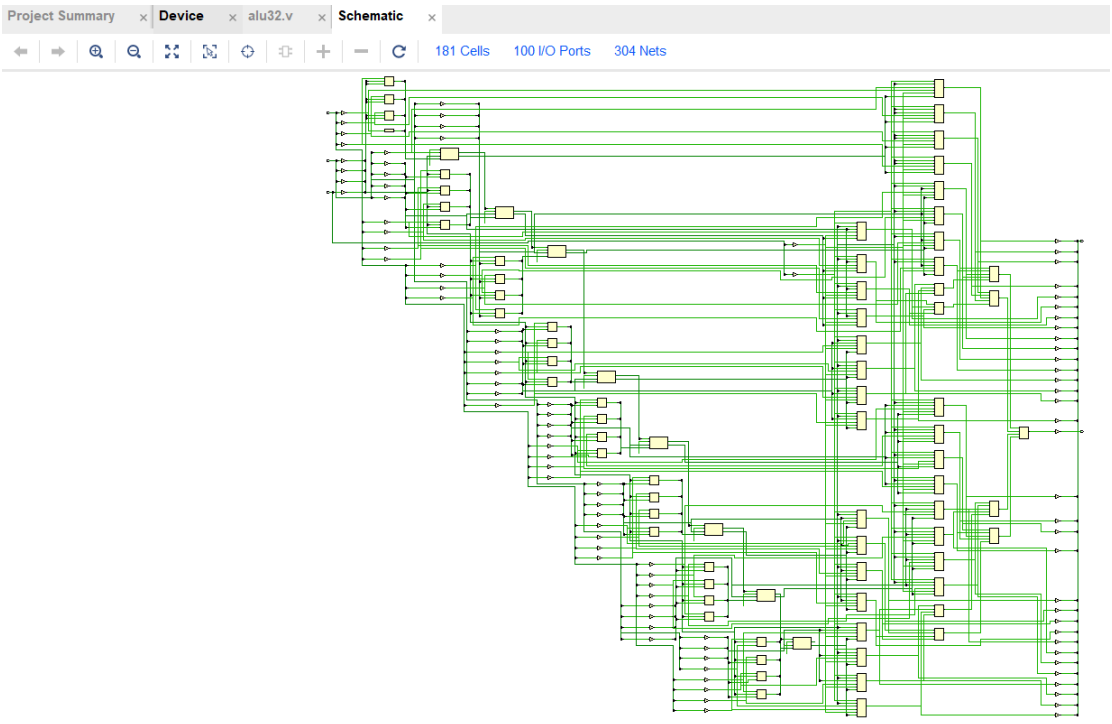
设计文件：

```
module alu32 #(parameter WIDTH = 32)(
input [WIDTH - 1:0] a,b,
input [2:0] f,
output [WIDTH - 1:0] y,
output z //0标志
    );
  reg [31:0] y_t;
  reg p_t;//进位/借位
  reg q_t;//溢出
  always@(*) begin
    case(f)
        3'b000:begin
                {p_t,y_t} = a+b;
                q_t = (a[31]&~b[31]&~y_t[31])|(~a[31]&~b[31]&y_t[31]);
            end         //加法
        3'b001:begin
                {p_t,y_t} = a-b;
                q_t = (a[31]&~b[31]&~y_t[31])|(~a[31]&b[31]&y_t[31]);
            end         //减法
        3'b010:y_t = a&b;   //与
        3'b011:y_t = a|b;    //或
        3'b100:y_t = a^b;   //异或
        default:y_t = 32'h0000_0000;
     endcase
     end
     assign z = ~|y_t;
     assign y = y_t;
endmodule
```

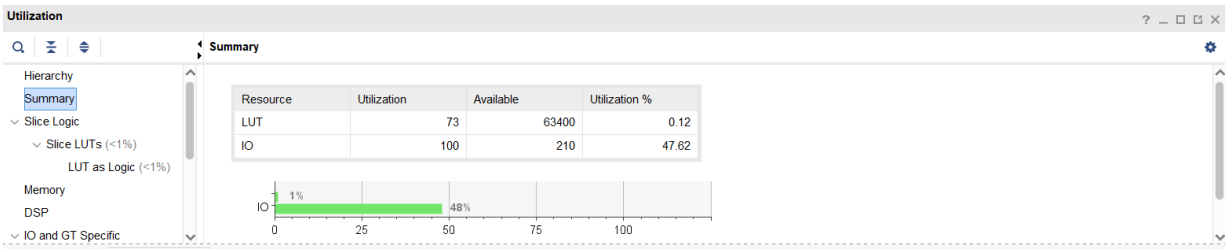
RTL：



综合电路图：

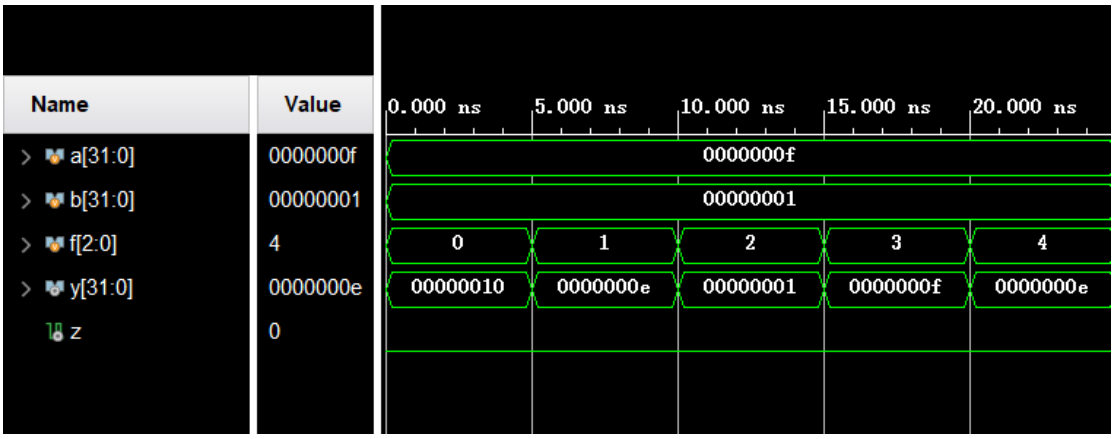


资源使用情况：



仿真：令 a=0000000f，b=00000001；f=000 为加法，001 为减法，010 为与，011 为或，100 为异或；代码与波形如下：

```
module sim1();
reg [31:0] a;
reg [31:0] b;
reg [2:0] f;
wire [31:0] y;
wire z;
alu32 aa(.a(a),.b(b),.f(f),.y(y),.z(z));
initial begin
    a=32'h0000_000f; #5 a=32'h0000_000f; #5 a=32'h0000_000f; #5
    a=32'h0000_000f; #5 a=32'h0000_000f; #5
    $finish;
end
initial begin
    b=32'h0000_0001; #5 b=32'h0000_0001; #5 b=32'h0000_0001; #5
    b=32'h0000_0001; #5 b=32'h0000_0001; #5
    $finish;
end
initial begin
    f=3'b000; #5 //加法
    f=3'b001; #5 //减法
    f=3'b010; #5 //与
    f=3'b011; #5 //或
    f=3'b100; #5 //异或
    $finish;
end
endmodule
```



题目二：6 位操作数 ALU

设计文件：

模块化寄存器：

```
module  register
#(parameter WIDTH = 32, RST_VALUE = 0)
(input  clk, rst, en,
input  [WIDTH-1 : 0]  d,
output reg  [WIDTH-1 : 0] q);
    always @(posedge clk, posedge rst)
        if (rst) q <= RST_VALUE;
            else  if (en)
                q <= d;
endmodule
```

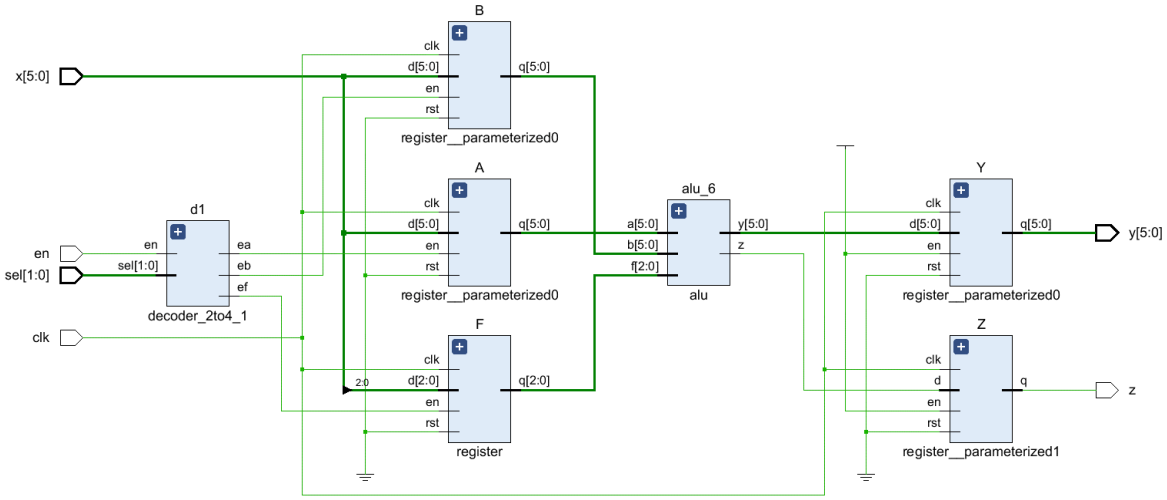
模块化译码器：

```
module decoder_2to4_1(
input en,
input [1:0] sel,
output  reg ef,ea,eb
    );
    always@(*) begin
        if(en==0) begin
            ef<=0;eb<=0;ea<=0;
        end
        else case(sel)
                2'b00: begin ef<=0;ea<=1;eb<=0; end
                2'b01: begin ef<=0;ea<=0;eb<=1; end
                2'b10: begin ef<=1;ea<=0;eb<=0; end
            endcase
        end
endmodule
```

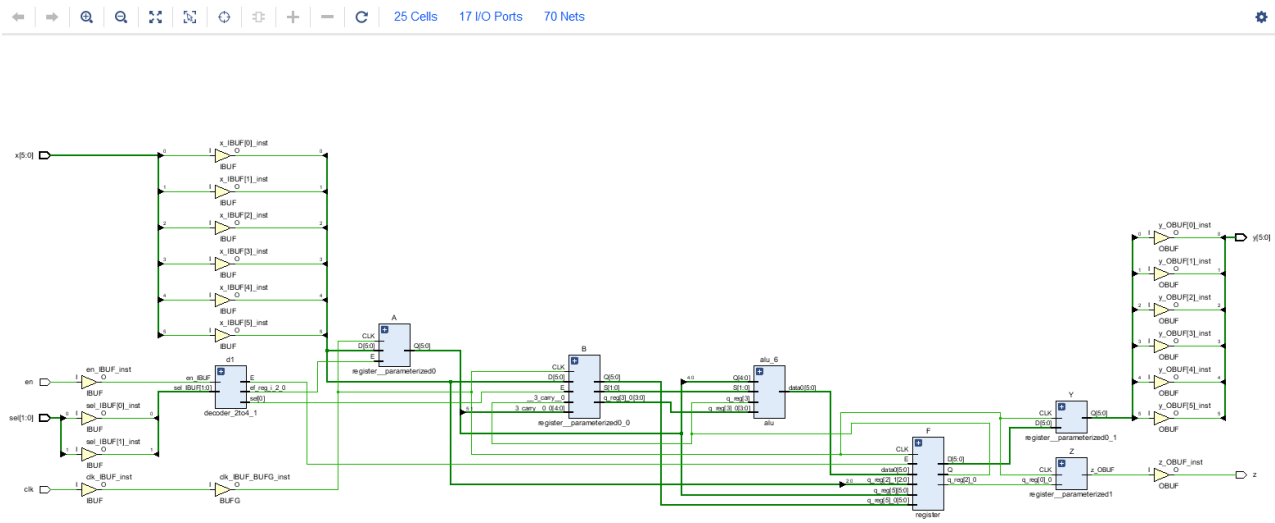
调用 32 位 ALU，译码器，寄存器得到 6 位 ALU 设计文件：

```
module alu6 (
    input clk,
    input  en,
    input  [1:0]sel,
    input  [5:0] x,
    output  [5:0] y,
    output  z
);
wire ef,ea,eb;
wire [5:0] m;
wire [5:0] a,b;
wire [2:0] f;
wire [5:0] y_in;
wire z_in;
assign m[5:0] = x [5:0];
decoder_2to4_1 d1(.en(en),.sel(sel[1:0]),.ef(ef),.ea(ea),.eb(eb));
register #(3,0) F(.clk(clk),.rst(0),.en(ef),.d(m[2:0]),.q(f[2:0]));
register #(6,0) A(.clk(clk),.rst(0),.en(ea),.d(m[5:0]),.q(a[5:0]));
register #(6,0) B(.clk(clk),.rst(0),.en(eb),.d(m[5:0]),.q(b[5:0]));
alu #(6) alu_6 (.a(a),.b(b),.f(f),.y(y_in),.z(z_in));
register #(6,0) Y(.clk(clk),.rst(0),.en(1),.d(y_in[5:0]),.q(y[5:0]));
register #(1,0) Z(.clk(clk),.rst(0),.en(1),.d(z_in),.q(z));
endmodule
```

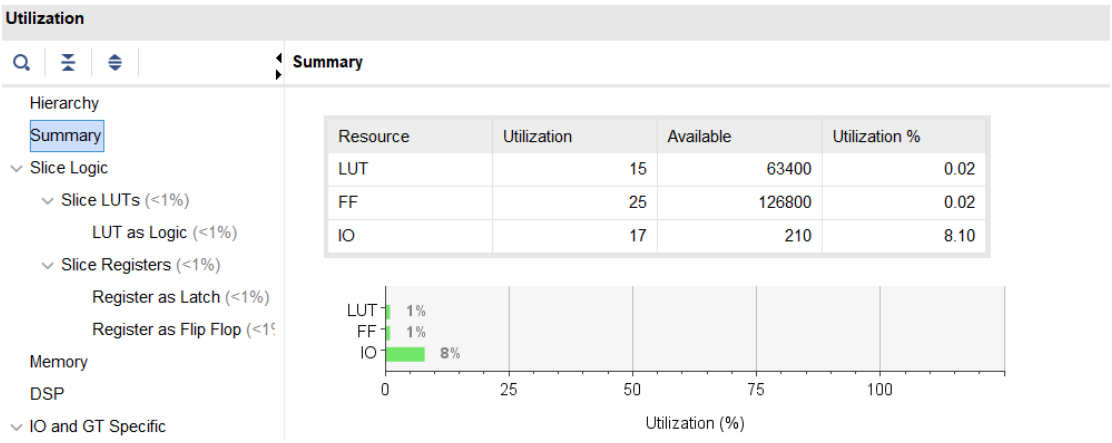
RTL：



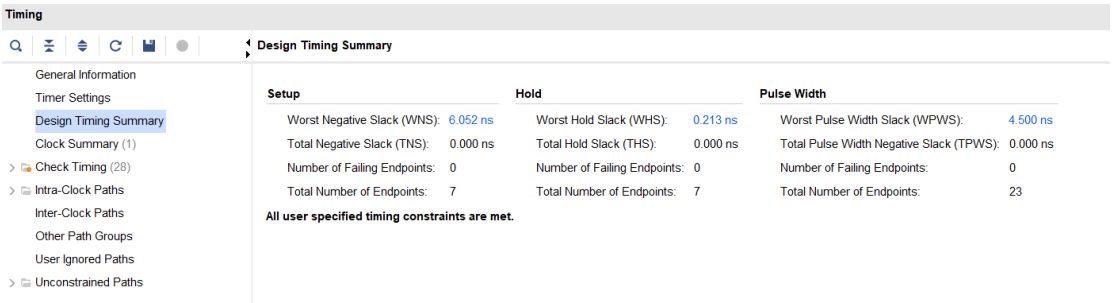
综合电路图：



资源使用情况：



时间性能报告：



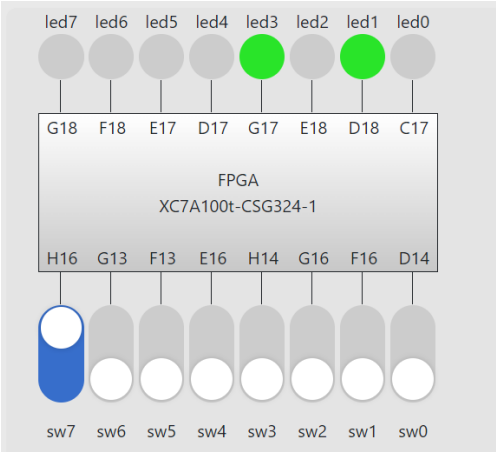
约束文件：

```
set_property -dict { PACKAGE_PIN E3   IOSTANDARD LVCMOS33 } [ get_ports { clk }];
create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports { clk }];

set_property -dict { PACKAGE_PIN B18   IOSTANDARD LVCMOS33 } [ get_ports { en }];

set_property -dict { PACKAGE_PIN C17   IOSTANDARD LVCMOS33 } [ get_ports { y[0] }];
set_property -dict { PACKAGE_PIN D18   IOSTANDARD LVCMOS33 } [ get_ports { y[1] }];
set_property -dict { PACKAGE_PIN E18   IOSTANDARD LVCMOS33 } [ get_ports { y[2] }];
set_property -dict { PACKAGE_PIN G17   IOSTANDARD LVCMOS33 } [ get_ports { y[3] }];
set_property -dict { PACKAGE_PIN D17   IOSTANDARD LVCMOS33 } [ get_ports { y[4] }];
set_property -dict { PACKAGE_PIN E17   IOSTANDARD LVCMOS33 } [ get_ports { y[5] }];
set_property -dict { PACKAGE_PIN G18   IOSTANDARD LVCMOS33 } [ get_ports { z }];

set_property -dict { PACKAGE_PIN D14   IOSTANDARD LVCMOS33 } [ get_ports { x[0] }];
set_property -dict { PACKAGE_PIN F16   IOSTANDARD LVCMOS33 } [ get_ports { x[1] }];
set_property -dict { PACKAGE_PIN G16   IOSTANDARD LVCMOS33 } [ get_ports { x[2] }];
set_property -dict { PACKAGE_PIN H14   IOSTANDARD LVCMOS33 } [ get_ports { x[3] }];
set_property -dict { PACKAGE_PIN E16   IOSTANDARD LVCMOS33 } [ get_ports { x[4] }];
set_property -dict { PACKAGE_PIN F13   IOSTANDARD LVCMOS33 } [ get_ports { x[5] }];
set_property -dict { PACKAGE_PIN G13   IOSTANDARD LVCMOS33 } [ get_ports { sel[0] }];
set_property -dict { PACKAGE_PIN H16   IOSTANDARD LVCMOS33 } [ get_ports { sel[1] }];
```

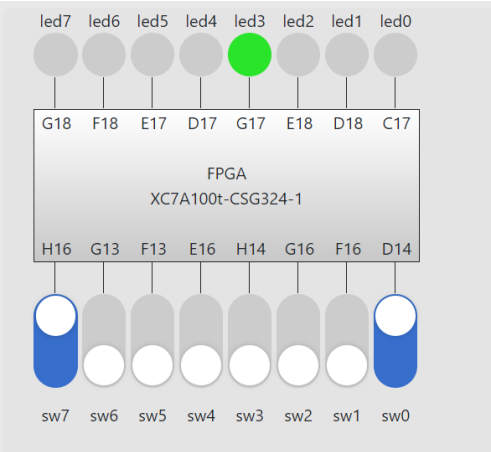
FPGA 情况：

输入 a=001001，b=000001,；

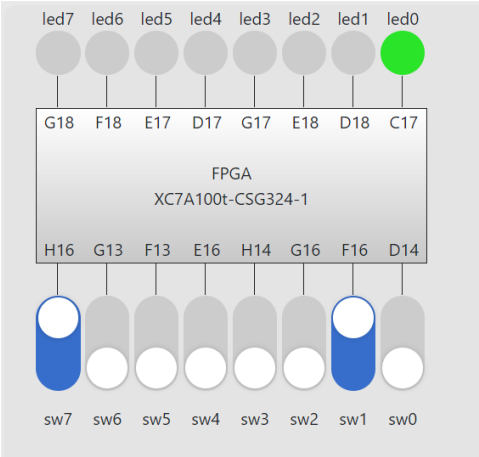
执行加、减、与、或、异或操作，结果应为：001010,0010000,000001,001001，001000 实际结果如下图所示：



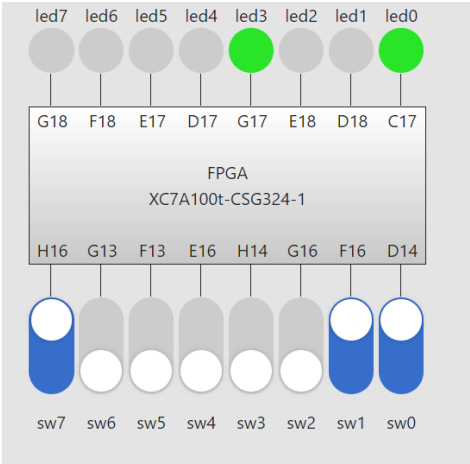
（加）



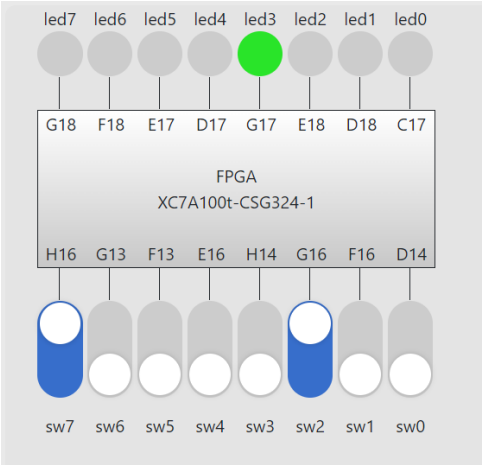
（减）



（与）



（或）



（异或）

完全符合预期。

题目三：FLS

设计文件：

取按键脉冲模块：

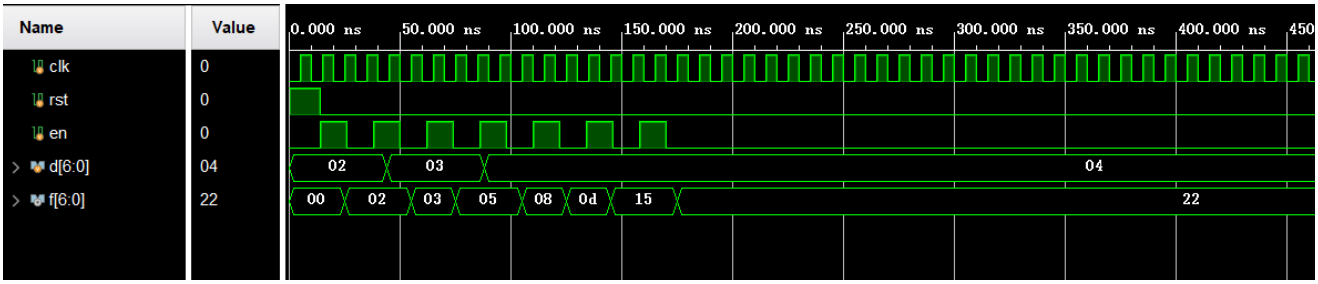
```
module pulse(
    input clk,
    input en,
    output en_pulse
    );
reg button_r1,button_r2;
always@(posedge clk) button_r1 <= en;
always@(posedge clk) button_r2 <= button_r1;
assign en_pulse = button_r1 & (~button_r2);
endmodule
```

源代码：

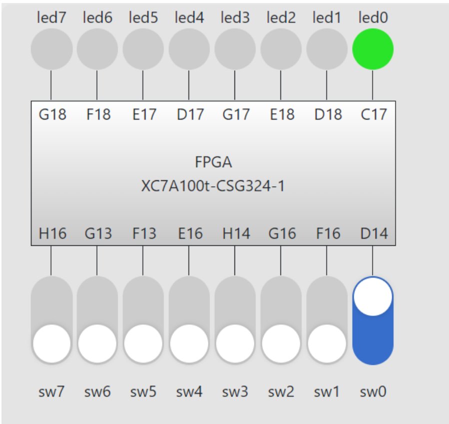
```
module  FLS (
    input  clk, rst, en,
    input  [6:0]  d,
    output reg [6:0]  f
);

parameter s0 = 2'b00;
parameter s1 = 2'b01;
parameter c_cal  = 2'b10;
reg [1:0] cs, ns;
reg [6:0] data_past, tmp;
wire en_pulse;
pulse en_edge(clk, en, en_pulse);   //取按键脉冲
initial begin
    cs = s0;
    ns = s1;
    data_past = 0;
    f = 0;
end
always @(*) begin
    case (cs)
        s0:
            ns = s1;
        s1, c_cal:
            ns = c_cal;
        default:
            ns = s0;

    endcase
end //有限状态机第一部分
always @(posedge clk or posedge rst) begin
    if (rst)
        cs <= s0;
    else if (en_pulse)
        cs <= ns;
end
always @(posedge clk or posedge rst) begin
    if (rst) begin
        data_past = 0;
        f = 0;
    end
    else if (en_pulse) begin
        case (cs)
            s0 : begin
                data_past <= f;
                f <= d;
            end
            s1 : begin
                data_past <= f;
                f <= d;
            end
            c_cal : begin
                tmp = data_past;
                data_past = f;
                f = tmp + f;

            end
            default: begin
                f <= 0;
                data_past <= 0;
            end
        endcase
    end
end

endmodule
```

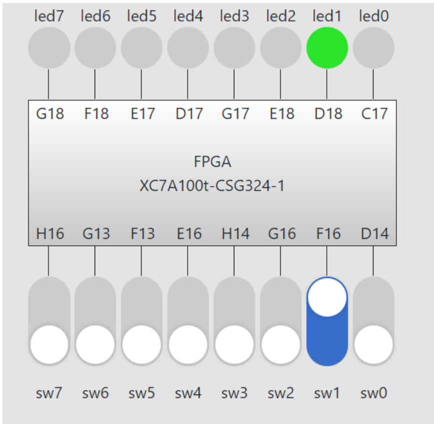
仿真文件及波形如下（结果符合预期）：

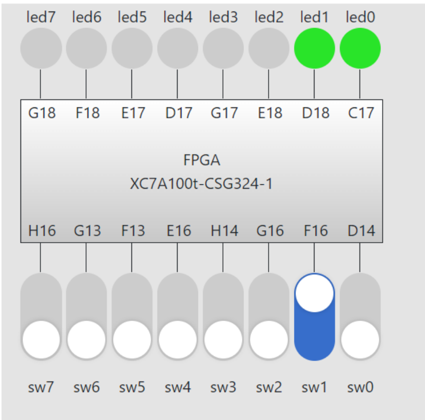
```
module sim1();
reg clk,rst,en;
reg [6:0] d;
wire [6:0] f;
FLS fls(.clk(clk),.rst(rst),.en(en),.d(d),.f(f));
initial clk = 0;
always #5 clk = ~clk;
initial begin
    rst = 1; #14
    rst = 0;
end
initial begin
    en = 0; #14 en = 1; #12 en = 0; #12 en = 1; #12 en = 0; #12 en = 1; #12 en = 0; #12 en = 1; #12 en = 0; #12 en = 1; #12 en = 0; #12 en = 1; #12 en = 0; #12 en = 1; #12 en = 0;
end
initial begin
    d<=7'b0000010; #44 d<=7'b0000011; #44 d<=7'b0000100;
end
endmodule
```

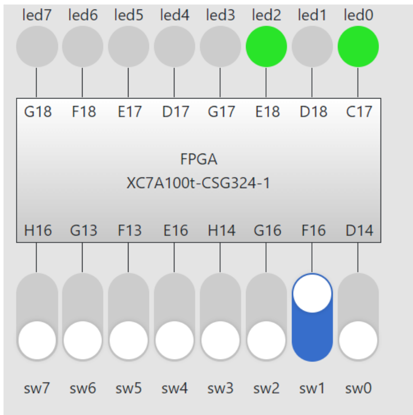


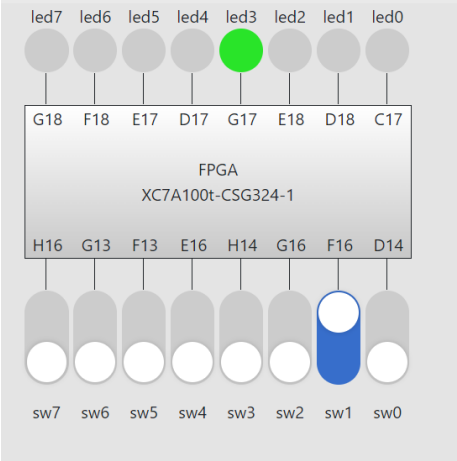
FPGA 情况：

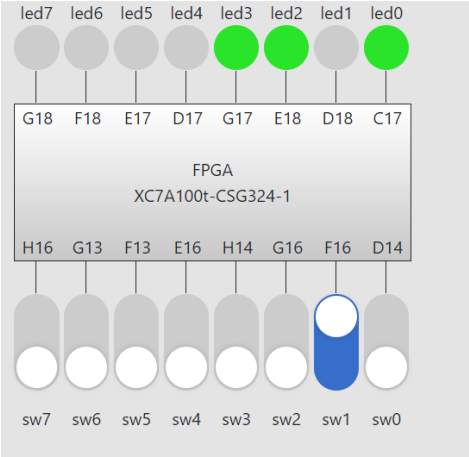






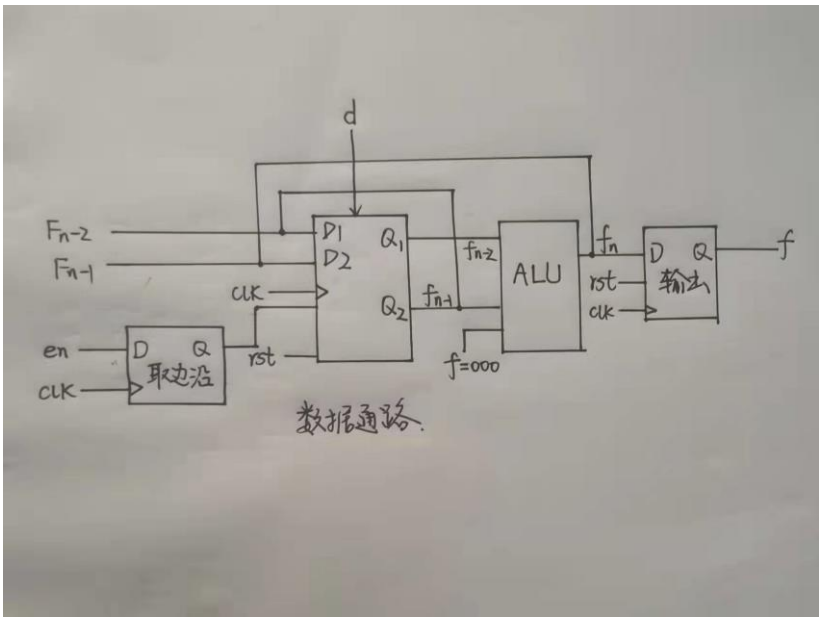






（与仿真波形及计算结果一致）

数据通路：



【总结与思考】

建议改进一下实验文档，有些地方交代的不够仔细，理解起来有很大困难。