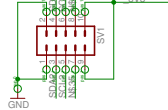
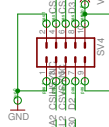
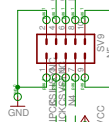
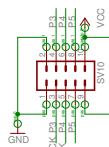
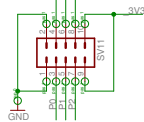
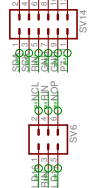
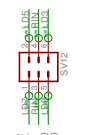
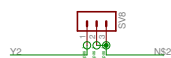
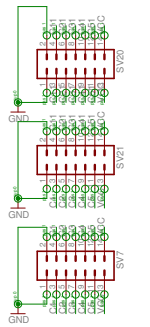


The figure consists of three schematic diagrams illustrating the test setup for the 128Kbit SRAM. The top diagram shows the input side with VIN connected to WIREPAD3,171,3 and WIREPAD3,171,3 connected to GND. The bottom diagram shows the output side with VCC connected to IP3 and CHR_IN, and GND connected to GND. The middle diagram shows the internal circuitry with VIN, GND, VOUT, and GNDOUT connections.

SV2

Pin	Signal
1	GND
2	5V
3	3V3
4	SD_A
5	SD_C
6	X1
7	V1
8	LD2
9	LD4
10	LD8
11	LD10
12	LD12
13	LD14
14	LD16
15	LD18
16	LD20
17	
18	
19	
20	
21	CHR_IN
22	GND
23	BAT
24	PWMONN
25	GND
26	X2
27	V2
28	LD3
29	LD5
30	LD7
31	LD9
32	LD11
33	LD13
34	LD15
35	LD17
36	LD19
37	
38	
39	
40	LD21

[illegible]

CHIP DIP LOGO 3x3 COPPER

CHIP DIP LOGO 3x3 COPPER

CHIP DIP LOGO 10x10 SILK