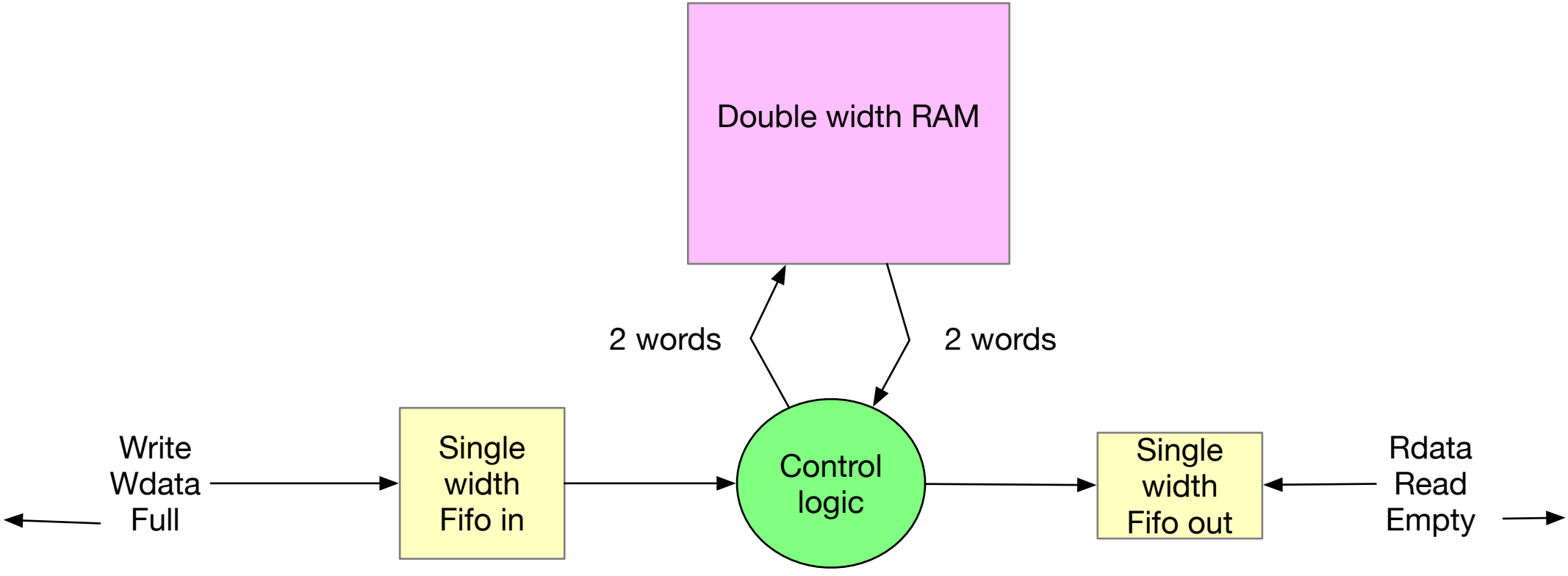
FULL RATE FIFO



Control logic steers data from inFifo to outfFifo, while outFifo is not full. When outFifo becomes full, the data is steered into the ram.
Because the ram is written with two datas in one clock, two entries can be read on the next clock. While there is data in a ram, it is read to outFifo on every clock the outFifo is not full.