Async fifo generator

Explain the principal

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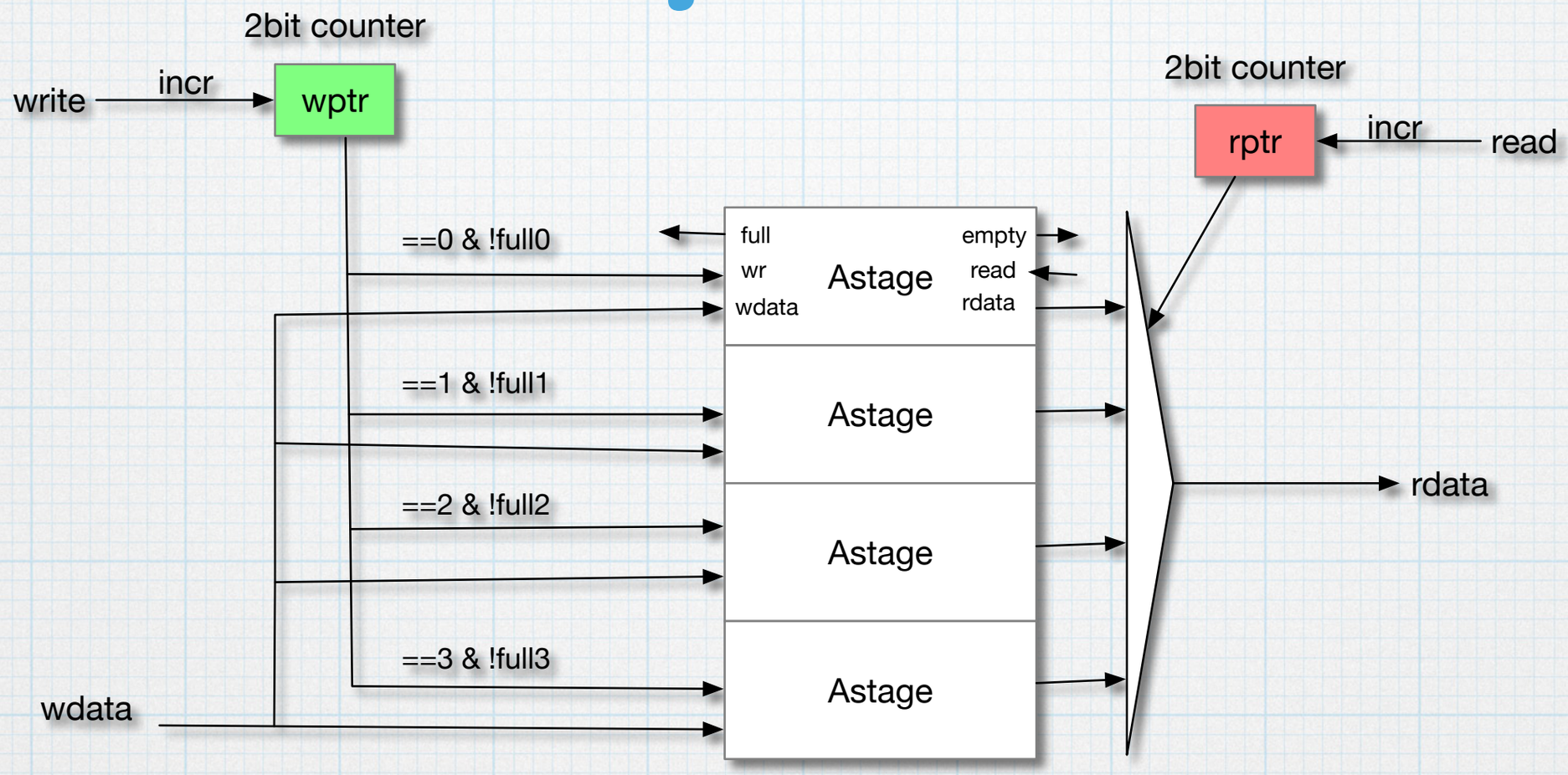
Overview

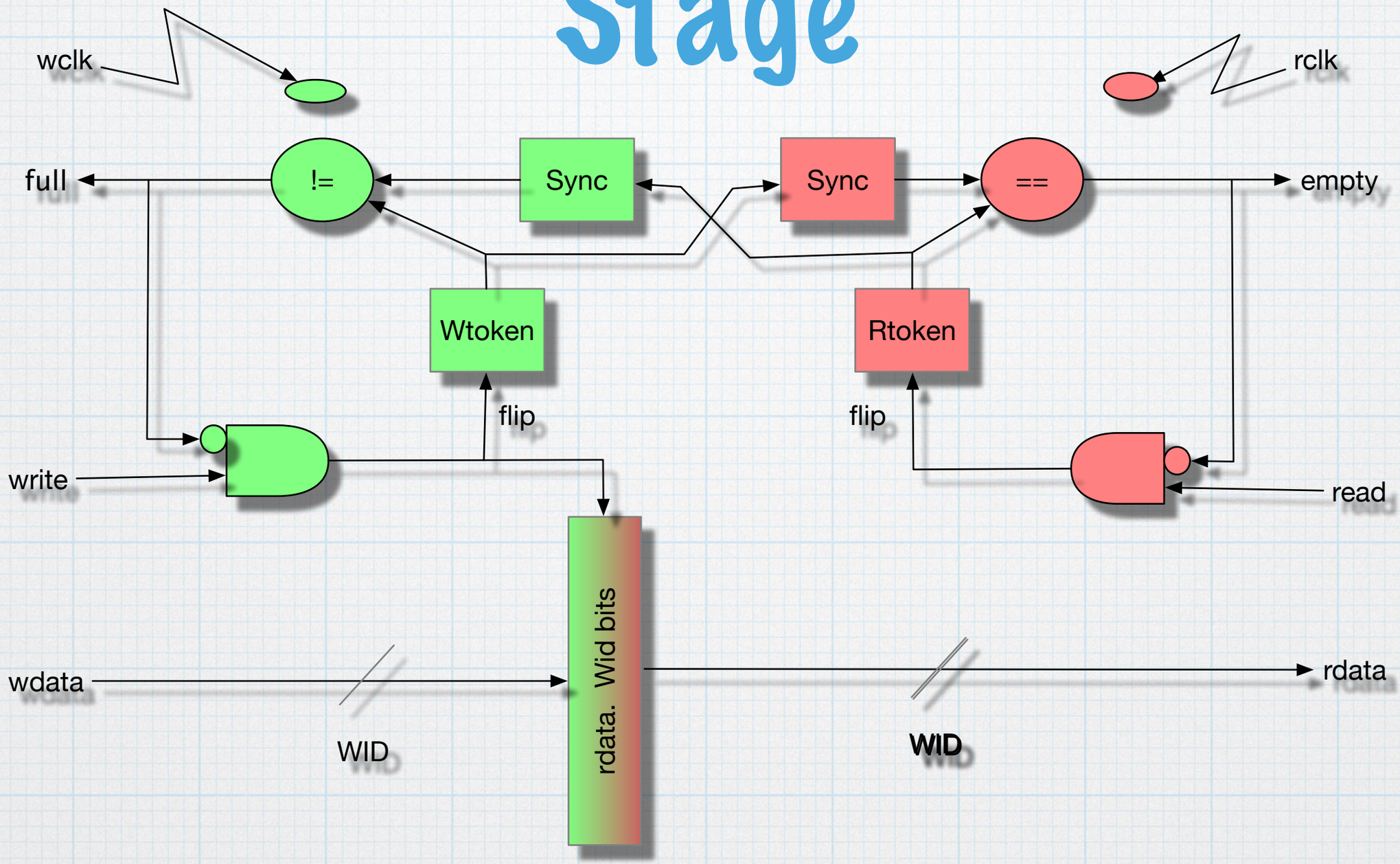
Asyncfifo has
write port on one clock
And
Read port on unrelated clock

Top level



Writes cause the write pointer to select next entry and write it if it is not full. Read pointer "chases" the wrote pointer and allows read only if the entry (stage) is not empty.
Pointers run in circles, ensuring there is not CDC problem, by delaying indications by synchronization delay.

Stage



Single stage has W flop and R flop. They flip values on read or write respectively. When they agree. - it means entry is empty. When they are different the entry has data. Their values are cross synchronized.

Chase

Rptr chases Wptr

Initial

	wtokens	rtokens	
!full	0	0	empty
!full	0	0	empty
!full	0	0	empty
!full	0	0	empty

1st write

	wtokens	rtokens	
!full	0	0	empty
!full	0	0	empty
!full	0	0	empty
full	1	0	!empty

2nd write

	wtokens	rtokens	
!full	0	0	empty
!full	0	0	empty
full	1	0	!empty
full	1	0	!empty

3rd write

	wtokens	rtokens	
!full	0	0	empty
full	1	0	!empty
full	1	0	!empty
full	1	0	!empty

1st read

	wtokens	rtokens	
!full	0	0	empty
full	1	0	!empty
full	1	0	!empty
!full	0	0	!empty

2nd read

	wtokens	rtokens	
!full	0	0	empty
full	1	0	!empty
!full	1	0	empty
!full	0	0	!empty