LAB A-06 (Week 7) Construction and Implementation of Flip-flops, Counters, and Shift Registers

Objectives

a. To get familiarity with the flip-flops, asynchronous counters, and shift registers by the construction of the circuit and studying the operation.

b. To design and construct the synchronous counter and verify the counting sequence.

Tasks

Questions to be discussed in the lab and to be submitted in the report:

1. a. Verify the function table for 7476 Dual Negative Edge Triggered JK Flip-flop

   b. Construct the following flip-flops using JK Flip-Flop andverify their truth tables

   - D (Data) Flip-Flop
   - T (Toggle) Flip-Flop

2. Design a 2-bit synchronous counter that can go through the following sequence in binary.

   1, 3, 2, 0 and repeat

   Use J-K Flip-flops for the design. Verify your design experimentally.

Questions to be submitted in the report:

3. Construct and explain the operation of the following ripple counters with positive edge triggered D Flip-flops.

   - 4 bit binary asynchronous UP counter
   - 4 bit binary asynchronous DOWN counter
   - Asynchronous BCD Counter
   - Asynchronous MOD-12 Counter
   - Ripple divide by 14 Counter

4. Design and Construct a parallel counter that has the following sequence.
   If the input (UP)/(DOWN)' = 1, it will count up, 000-010-100-110 and then recycle to 000
   If the input (UP)/(DOWN)' = 0, it will count down, 110-100-010-000 and then recycle to 110.
   Undesired states are don't care states.

   (i) Use T flip-flops for the design.
   (ii) Use D flip-flops for the design.

5. With the help of timing diagrams, state the number of pulses required to perform shifting of binary number 1001 using

   i. SISO shift register
   ii. SIPO shift register
   iii. PISO shift register
   iv. PIPO shift register
   v. Ring counter

Report Format

- Tutorial number and objectives
- Question 1
  - Problem Statement
  - Function table for JK Flip-flop,
  - Connection diagram for D Flip-flop using JK Flip-flop and truth table for D Flip-flop
  - Connection diagram for T Flip-flop using JK Flip-flop and truth table for T Flip-flop
- Question 2 and 4
  - Problem Statement
  - State Transition Diagram
  - Flip-flop Excitation Table
  - Circuit Excitation Table (State Table) showing present state, next state and Flip-flop inputs
  - Karnaugh maps for the simplification of Flip-flop inputs
  - Simplified Logical Expression for Flip-flop inputs
  - Construction diagram for the synchronous(parallel) counter using the simplified logic expressions
- Question 3 and 5
  - Problem Statement
  - Follow the instructions given in subdivisions of each question

Circuit Construction:

- Submit the constructed circuit (each question) via CircuitVerse, and label it according to question. Be self-explanatory.

Assessment:

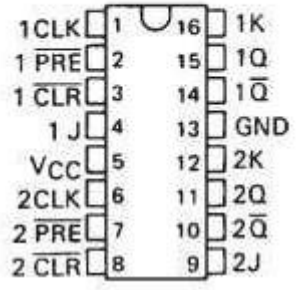
Total marks = 20/10=2%

Construction/Connections of the Circuit and Result during lab session= Tutor to pick one of the questions for students to do and submit via CircuitVerse = 10 marks,

Report =5 Questions × 2 marks = 10 marks

Pin Configurations:

SN5476, SN54LS76A . . . J PACKAGE
SN7476 . . . N PACKAGE
SN74LS76A . . . D OR N PACKAGE
(TOP VIEW)



'LS76A
FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

† This configuration is nonstable; that is, it will not persist when either preset or clear returns to its inactive (high) level.

TEXAS INSTRUMENTS
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