	A	B	C	D	E	F	G	H	I	J	K
1		A process		B process		C process		D process		Reschedule	
2	Clock tick	p_uspri	p_cpu	p_uspri	p_cpu	p_uspri	p_cpu	p_uspri	p_cpu	before	after
3	Starting point	60	0	60	0	60	0	60	0	A	A
4	1	60	1	60	0	60	0	60	0	A	A
5	50	60	50	60	0	60	0	60	0	A	A
6	99	60	99	60	0	60	0	60	0	A	A
7	100	73	50	60	0	60	0	60	0	A	B
8	101	73	50	60	1	60	0	60	0	B	B
9	150	73	50	60	50	60	0	60	0	B	B
10	199	73	50	60	99	60	0	60	0	B	B
11	200	73	25	73	50	60	0	60	0	B	C
12	201	73	25	73	50	60	1	60	0	C	C
13											
14											
15		A process		B process		C process		D process		Reschedule	
16	Clock tick	p_uspri	p_cpu	p_uspri	p_cpu	p_uspri	p_cpu	p_uspri	p_cpu	before	after
17	Starting point	60	0	60	0	60	0	60	0	A	A
18	1	60	1	60	0	60	0	60	0	A	A
19	10	60	10	60	0	60	0	60	0	A	A
20	11	60	10	60	1	60	0	60	0	A	B
21	20	60	10	60	10	60	0	60	0	B	B
22	21	60	10	60	10	60	1	60	0	B	B
23	30	60	10	60	10	60	10	60	0	B	C
24	31	60	10	60	10	60	10	60	1	C	C
25	40	60	10	60	10	60	10	60	10	C	C
26	41	60	11	60	10	60	10	60	10	C	D
27	50	60	20	60	10	60	10	60	10	D	D
28	51	60	20	60	11	60	10	60	10	D	D
29	60	60	20	60	20	60	10	60	10	D	A
30	61	60	20	60	20	60	11	60	10	A	A
31	70	60	20	60	20	60	20	60	10	A	A
32	71	60	20	60	20	60	20	60	11	A	B
33	80	60	20	60	20	60	20	60	20	B	B
34	81	60	21	60	20	60	20	60	20	B	B
35	90	60	30	60	20	60	20	60	20	B	C
36	91	60	30	60	21	60	20	60	20	C	C
37	100	64	15	64	15	60	10	60	10	C	C
38	101	64	15	64	15	60	11	60	10	C	D
39	110	64	15	64	15	60	20	60	10	D	D
40	111	64	15	64	15	60	20	60	11	D	D
41	120	64	15	64	15	60	20	60	20	D	A
42	121	64	16	64	15	60	20	60	20	A	A
43	130	64	25	64	15	60	20	60	20	A	A
44	131	64	25	64	16	60	20	60	20	A	B
45	140	64	25	64	25	60	20	60	20	B	B
46	141	64	25	64	25	60	21	60	20	B	B
47	150	64	25	64	25	60	30	60	20	B	C
48	151	64	25	64	25	60	30	60	21	C	C
49	160	64	25	64	25	60	30	60	30	C	C
50	161	64	26	64	25	60	30	60	30	C	D
51	170	64	35	64	25	60	30	60	30	D	D
52	171	64	35	64	26	60	30	60	30	D	D
53	180	64	35	64	35	60	30	60	30	D	A
54	181	64	35	64	35	60	31	60	30	A	A
55	190	64	35	64	35	60	40	60	30	A	A
56	191	64	35	64	5	60	40	60	31	A	C