GATE Question

January 31, 2024

1. The circuit shown in the figure below uses ideal positive edge-triggered synchronous $J-K$ flip flops with outputs X and Y. If the initial state of the output is $X = 0$ and $Y = 0$ just before the arrival of the first clock pulse, the state of the output just before the arrival of the second clock pulse is (GATE-IN2019,12)

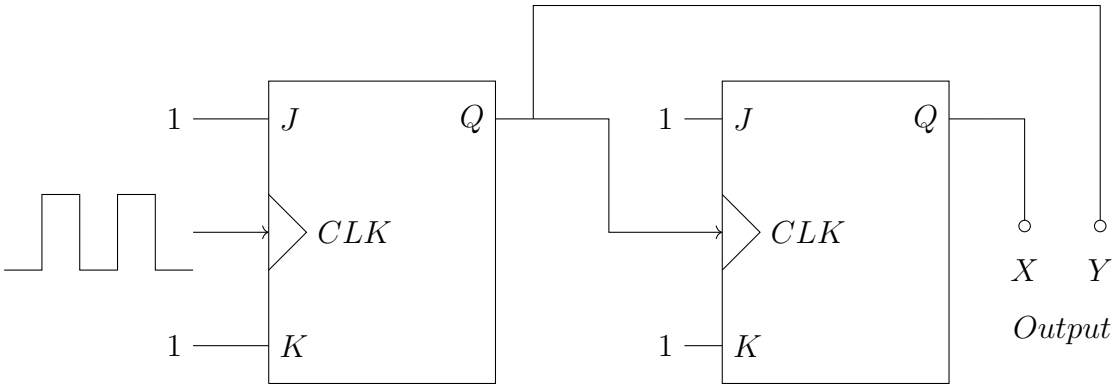

Figure 1: Ideal Positive Edge-triggered Synchronous J-K flip flops

(a) $X = 0, Y = 0$
(b) $X = 0, Y = 1$
(c) $X = 1, Y = 0$
(d) $X = 1, Y = 1$