

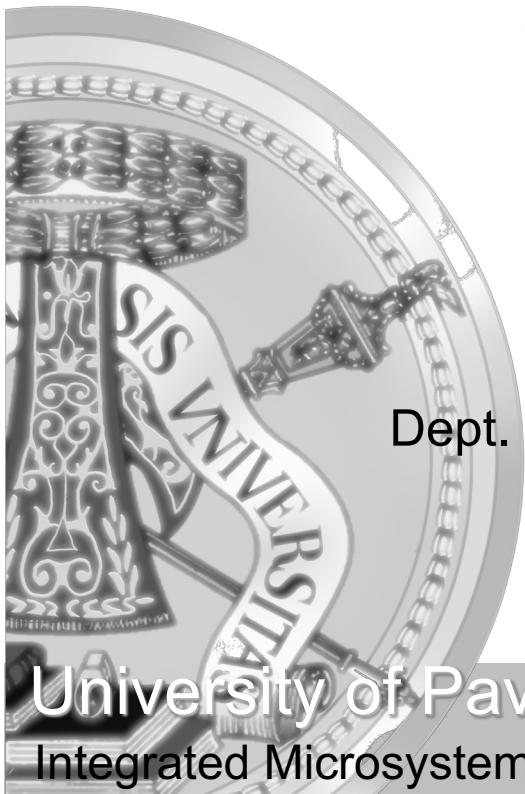


Introduction to the Course

Analog Integrated Circuits

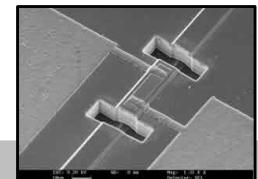
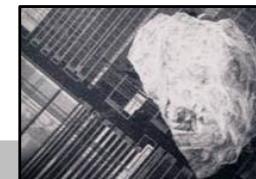
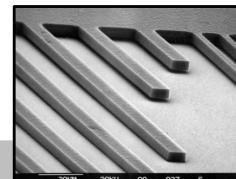
Edoardo Bonizzoni

Dept. of Electrical, Computer, and Biomedical Engineering



University of Pavia

Integrated Microsystems Laboratory

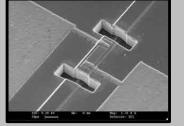
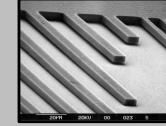


ABOUT MYSELF



Integrated MicroSystems (IMS) Laboratory
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Web-page: ims.unipv.it/~edoardo

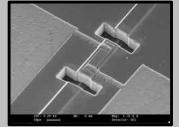
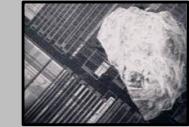
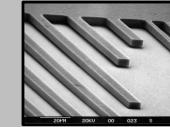
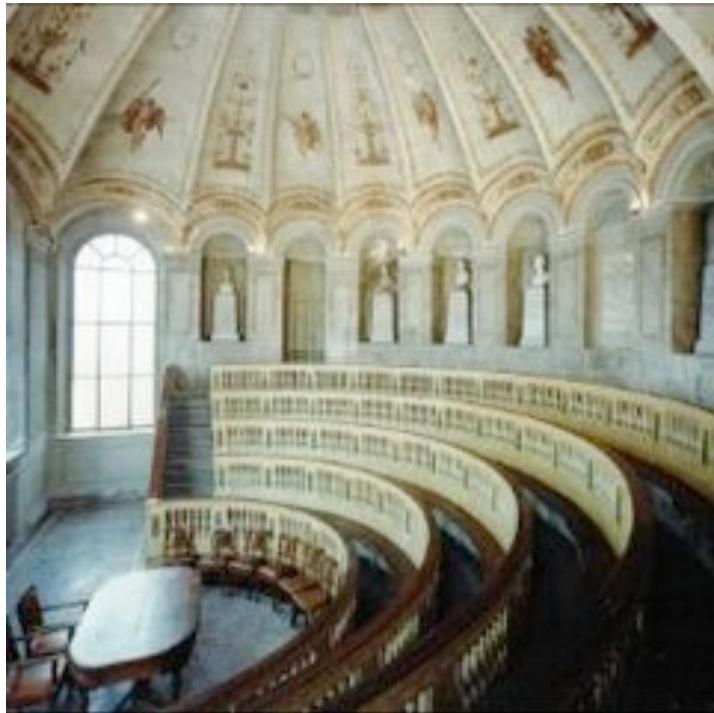
- ❖ Graduated (*summa cum laude*) in Electronics in 2002 (UP)
- ❖ Ph.D. in Electrical, Electronics, and Computer Science in 2006 (UP)
- ❖ Associate Professor
- ❖ Teaching: Elettronica I (undergrad program) and Analog Integrated Circuits (master program)
- ❖ Research interests: non-volatile memories, data converters, DC-DC converters, advanced analog circuits (voltage references, chopper amplifiers), magnetic sensors
- ❖ Author or co-author of 120+ publications in international journals or conference proceedings
- ❖ Associate Editor of IEEE Transactions on Circuits and Systems – I (previously AE of IEEE TCAS – II)

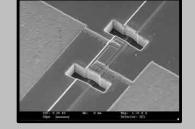
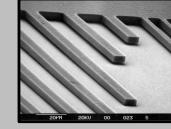


Year: 825 (theological and law school) 1361 (studium generale)

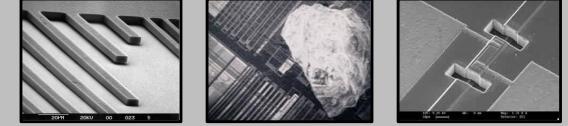
Famous Faculty: A. Volta, G. Cardano, C. Golgi, U. Foscolo







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la Provincia DOSSIER ECONOMIA PAVESE

ALTA TECNOLOGIA, LA SFIDA

di Sisto Capra

PAVIA. È un bacio che cresce in silenzio alle porte di Pavia. È quella che qualcuno chiama la Ticino Valley, successore italiana ed europea della celebre Silicon Valley calata nel cuore della terra dei mille microelettronica, informatica, ingegneria e chimica, cresciute in simbiosi con la facoltà di Ingegneria dell'Università.

Questa è la Pavia Valley rappresentata davvero una grande opportunità per Pavia e per l'intera provincia, portando i firmamenti delle città eccellenze, può darle un ruolo indebolito, può avviare un vero e proprio boom di nuovi impianti. Dalle scuole si neolaureati, attivare un interscambio di risorse umane con i laureati della ricerca e del sviluppo elettronico, informatico sparsi per il mondo, attirare nuove intelligenze a Pavia, incrementare le relazioni di altre aziende, con effetti moltiplicatori dagli esiti imprevedibili.



Cantoni



L'elettronica sta diventando un business importante per Pavia: le aziende la scelgono per la ricerca



Danese

hanno una elevata capacità di ricerca e producono molti risultati scientifici. I risultati di tali risultati in metodi produttivi, in attività industrialmente utilizzabili nella stessa città di Pavia. La trasformazione tra il sapere generato dalla ricerca e l'applicazione economicamente produttiva non è sempre facile, sono le iniziative e gli spin-off, cioè società generate da persone che si sono formate e hanno matrici scientifiche, ma anche dottorati di ricerca dell'Università, in particolare presso la facoltà di Ingegneria.

«È questo il nostro obiettivo», dice Giancarlo Malvestito, professore di strategia e politica aziendale al corso di laurea specialistica di Pavia. «Ci troviamo pensati più a fare impresa che a dare la caccia a finanziamenti. E fare impresa significa avere una visione, uso intelligente di risorse umane, capacità di creare occasione e sviluppo e tutto ciò che serve».



Pavia ha la sua Silicon Valley

*Dall'informatica alla microelettronica, 350 posti di lavoro
Viaggio nelle aziende che crescono intorno a Ingegneria*

denti e 80 collaboratori a progetto. Più di dieci docenti universitari collaborano alle attività di ricerca.

Altre aziende multinazionali hanno investito negli ultimi anni nei grandi complessi di impianti di produzione e ricerca sono stati implantati in Pavia da parte di Austria Microsystems, Acco, Renesas, Nissens, Stmicroelectronics, Virginie Cantoni, e recentemente Genzyme, Serono e Bifarmatika.

L'Università di Pavia ha saputo cogliere questa opportunità di crescita e di interesse di multinazionali della microelettronica, che hanno dato luogo a significative collaborazioni con l'ateneo: ne sono esempi STMicroelectronics, Marvell e Maxim. L'Università ha saputo, infatti, valutare e promuovere in grado di avviare iniziative di successo anche internazionali nel settore dell'industria e della ricerca, come Adipco Ariadne, SysNet e Funambol. Nell'ingegneria sismica e nella sismologia applicata Eucentre è diventato uno dei primi esempi di impegno mondiale per la ricerca e la formazione avanzata. Il laboratorio, insieme ai settecento studenti del Cnr, è dotato di impianti di simulazione unici in Europa e consente di effettuare analisi in scala fino ad ora effettuate solo in California. Richiama ricercatori da tutto il mondo e dà lavoro a 95 persone (15 dipen-

Il sapere diventa una significativa occasione: un successo internazionale di sviluppo

dopo la loro venuta in Italia. «La collaborazione che è iniziata da anni con l'Unione Industriali e con il Consorzio Pavia Export — spiega il presidente della facoltà di Ingegneria Virginie Cantoni — cresce costantemente. C'è un coinvolgimento diretto delle aziende nell'interno del Campus del Crayone. Ci sono iniziative particolari e progetti per il recupero di fondi nazionali. Il caso da cui ci ricaviamo è quello di Vigezzo, dove c'è un impianto di Vigezzo che produce solo l'ultimo esempio.

Si tratta della partecipazione ai progetti innovativi del ministero delle Ricerca e Sviluppo per il recupero di fondi nazionali. Il caso da cui ci ricaviamo è quello di Vigezzo, dove c'è un impianto di Vigezzo che produce solo l'ultimo esempio.

Ma in una provincia deindustrializzata la conoscenza giochi tutte le sue carte

di Antonella Zucchetta

I dibattiti sul tema del rapporto tra Università e territorio è oggi più utile che mai. Si moltiplicano i dibattiti sul tema e le prese di posizioni di tutti coloro che sono impegnati in un rapporto che già nel Medioevo era descritto come complesso, e talvolta problematico. Oggi abbondano le proposte di rinnovamento, di riqualificazione, con poco terzettato e produttivo, fra terzi territoriali, con poco terzettato avanzato e soluzioni concrete, che vedono la conoscenza e le risorse di istituzioni del settore pubblico e privato. Tuttavia restano a mia avviso due temi che meritano di essere affrontati: il primo è di poter fare chiarezza circa contenuti e prospettive del rapporto tra Università e sviluppo locale; il secondo è di poter fare chiarezza circa le realtà vicine, e dall'altro quando una azienda locale cerca personale qualificato fa-

la sua attività di formazione avanzata, cioè laureati e dotti di ricerca. Sono questi i punti più importanti perché la conoscenza è una economia dove è riconosciuto il ruolo crescente del capitale umano e del talento nella competitività. Se mancano soggetti capaci di «decodificare» al meglio queste conoscenze allora non solo la nostra provincia da un punto di vista economico, ma anche il territorio rientrante nel nostro territorio rientrante assunti di una azienda e la percentuale di occupazione assoluta di un territorio, per rendere le aziende più produttive e più innovative. Sono fatti di diverse parti, ma molto comuni, perché la principale arma competitiva per le aziende è rappresentata oggi dall'innovazione di prodotto e di servizio. Per questo l'Università può dare solo i risultati della sua attività di ricerca ma anche del-

(continua a pag. V)



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Analog Integrated Circuits
Edoardo Bonizzoni

The MOS Transistor

IMS LAB INDUSTRY ACTIVITIES



- ❖ Design of an high-resolution (20-b) ADC for audio applications (BCD 90 nm)
- ❖ Design of a wideband (40 MHz) ADC for car radio receivers (28 nm FDSOI)
- ❖ Design of an AFE for contactless temperature sensing (130 nm CMOS)



- ❖ Design of a high speed (2 GS/s) ADC for SERDES (7 nm FinFET)
- ❖ Design of a laser driver for HDD HAMR (BCD 90 nm)



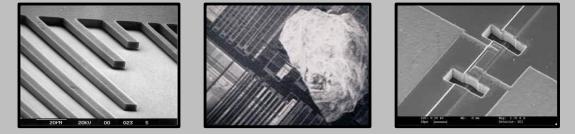
- ❖ Design of a high switching frequency DC-DC converter for automotive applications (130 nm CMOS)



- ❖ Design of an AFE for inductive position sensors in automotive pedal applications (180 nm CMOS)

- ❖ Design of an AFE for ultrasound based fingerprint sensors

IMS LAB ACADEMIC COOPERATIONS



STANFORD
UNIVERSITY

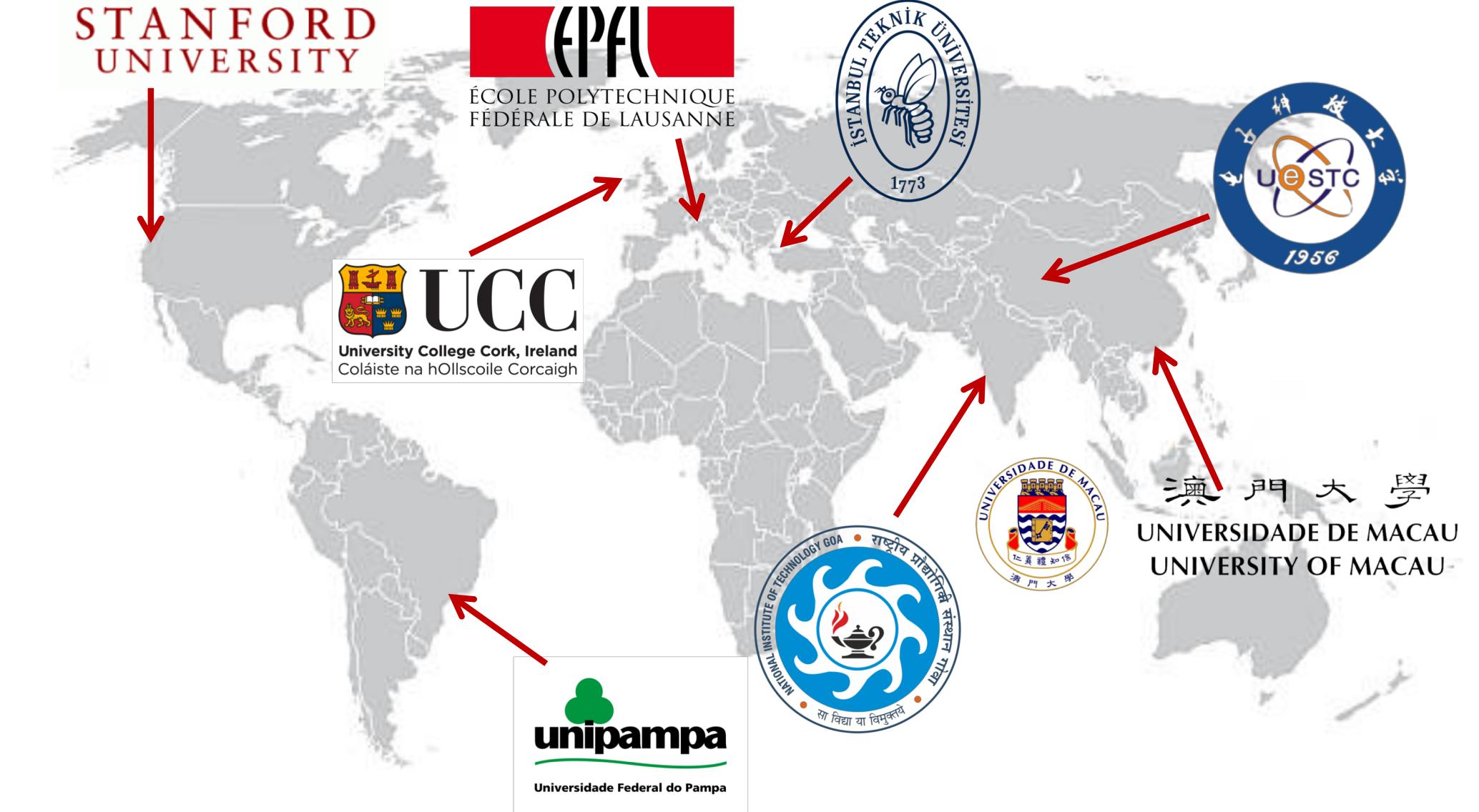


ÉCOLE POLYTECHNIQUE
FÉDÉRALE DE LAUSANNE

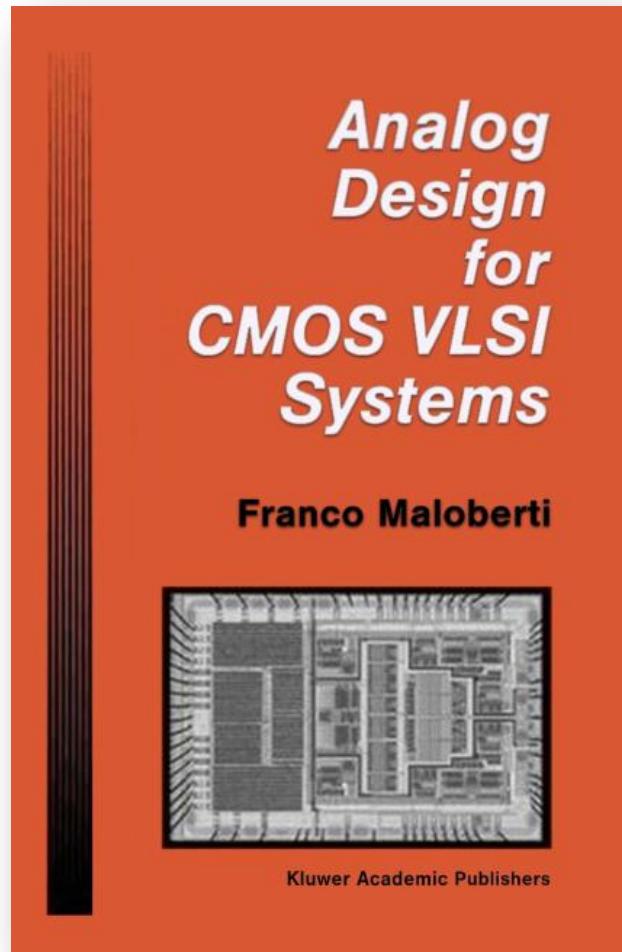


UCC

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Coláiste na hOllscoile Corcaigh



TEXT BOOK



Analog Integrated Circuits
Edoardo Bonizzoni

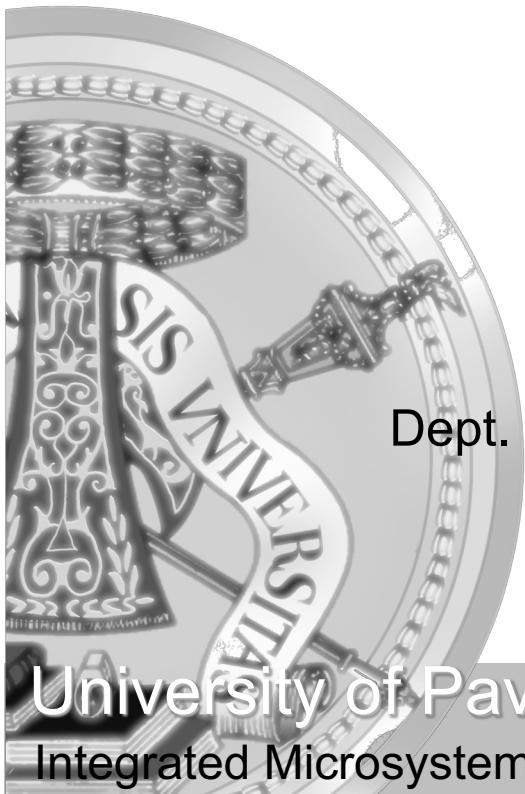


The MOS Transistor

Analog Integrated Circuits

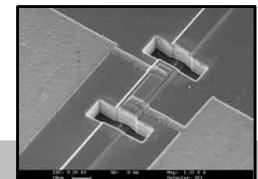
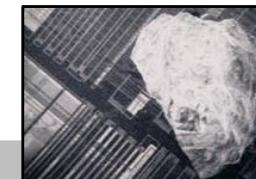
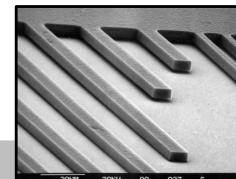
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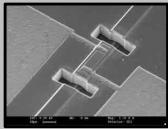
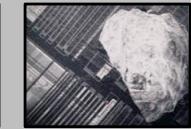
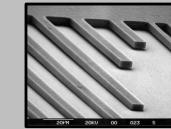
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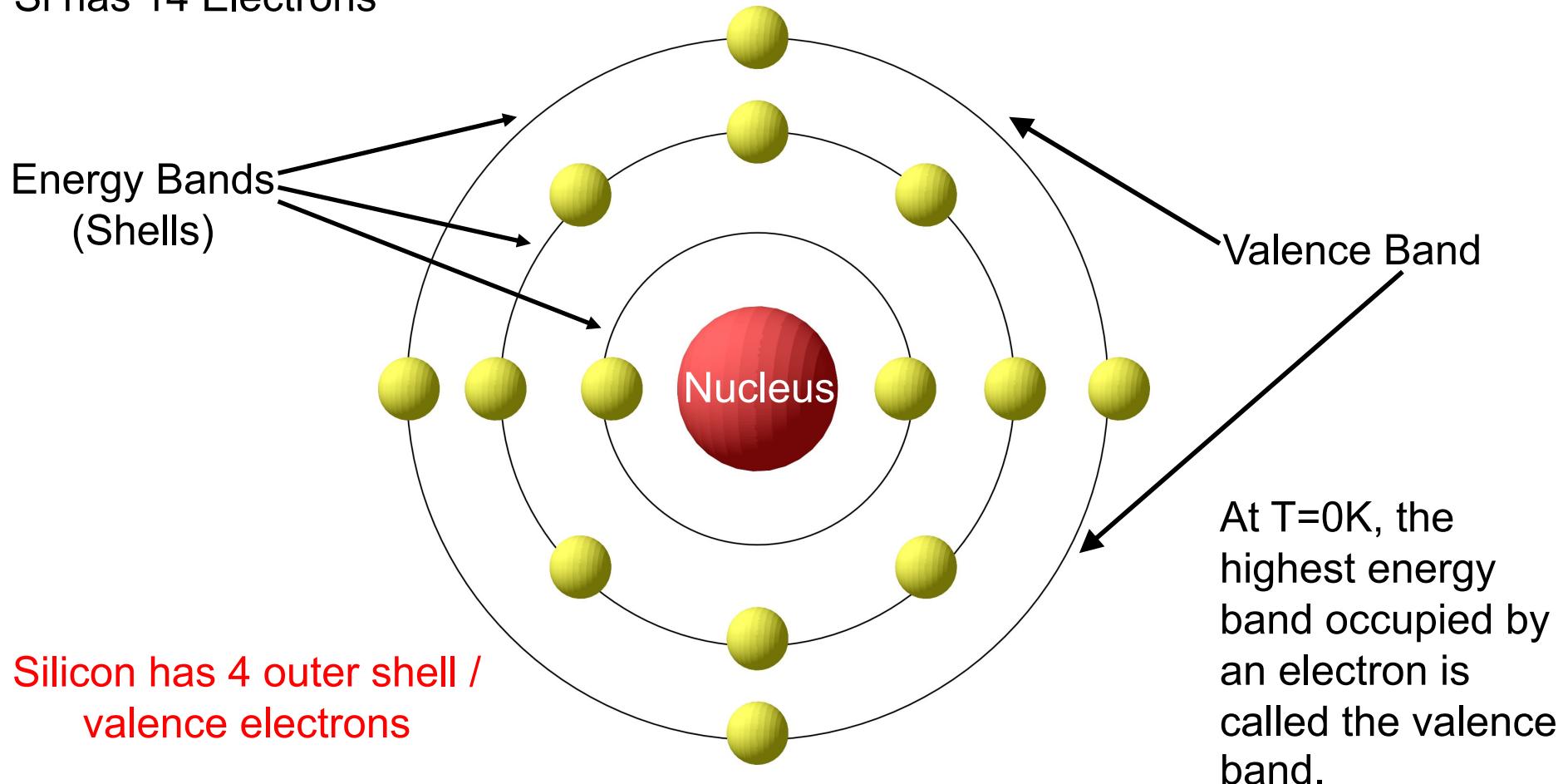
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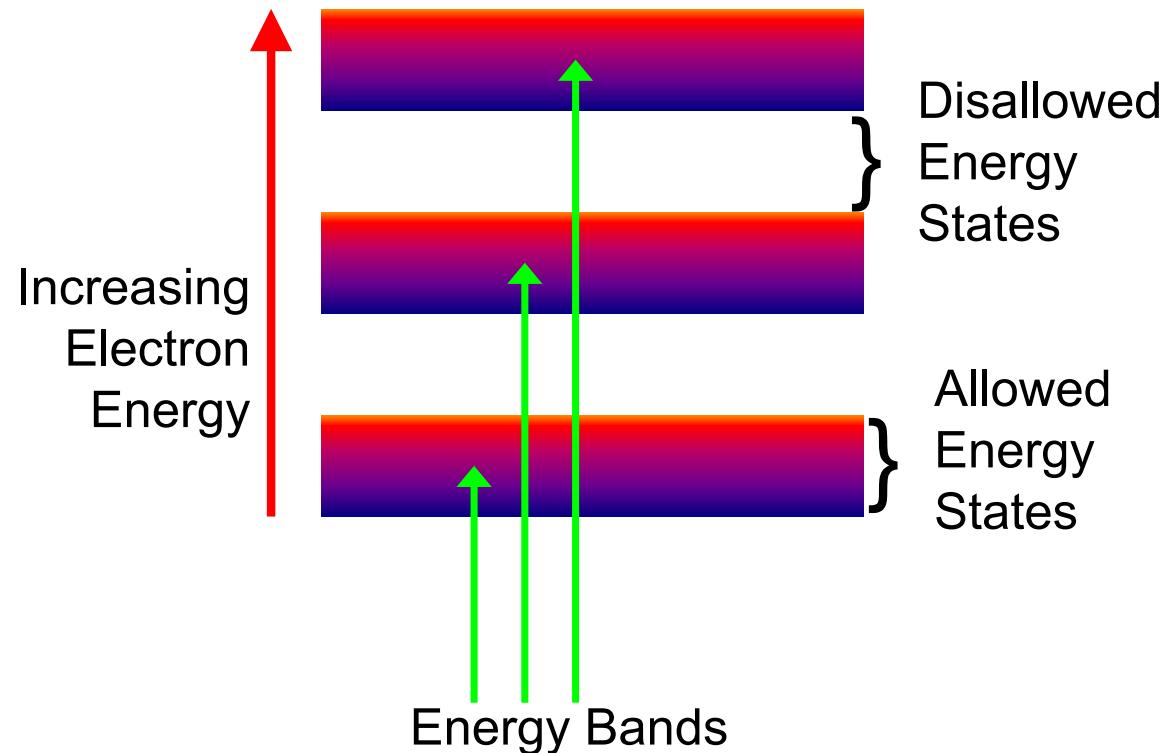
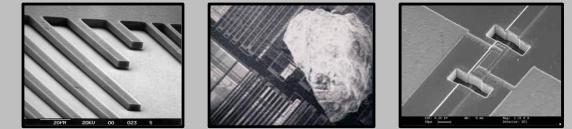


Silicon is the primary semiconductor used in VLSI systems

Si has 14 Electrons

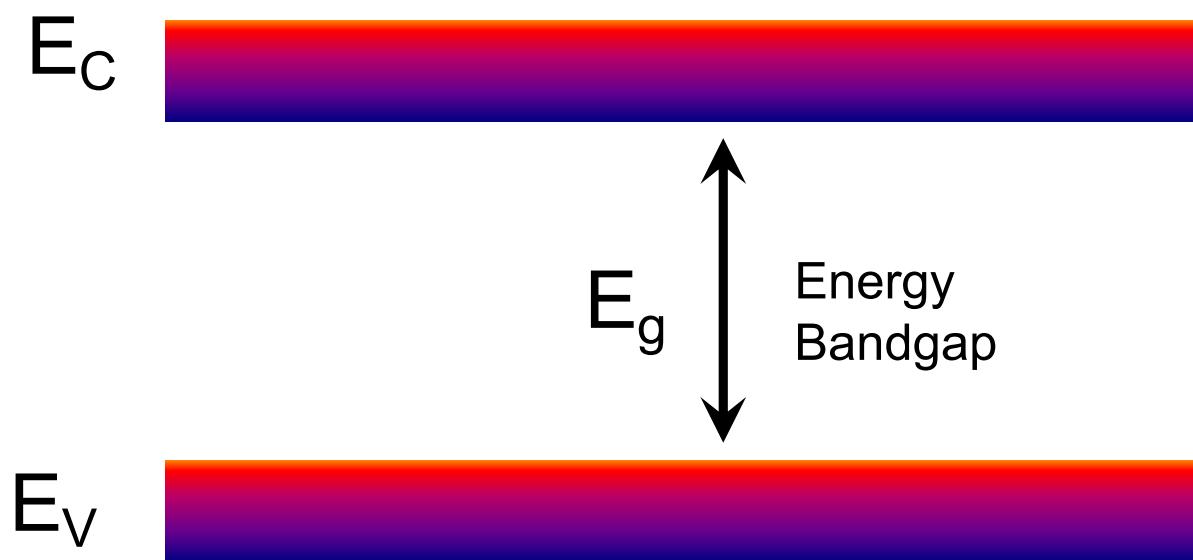
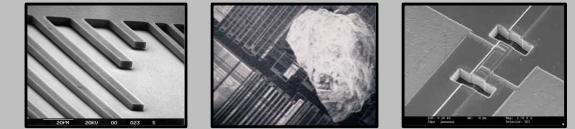


ENERGY BANDS



- ❖ Electrons try to occupy the lowest energy band possible
- ❖ Not every energy level is a legal state for an electron to occupy
- ❖ These legal states tend to arrange themselves in bands

ENERGY BANDS



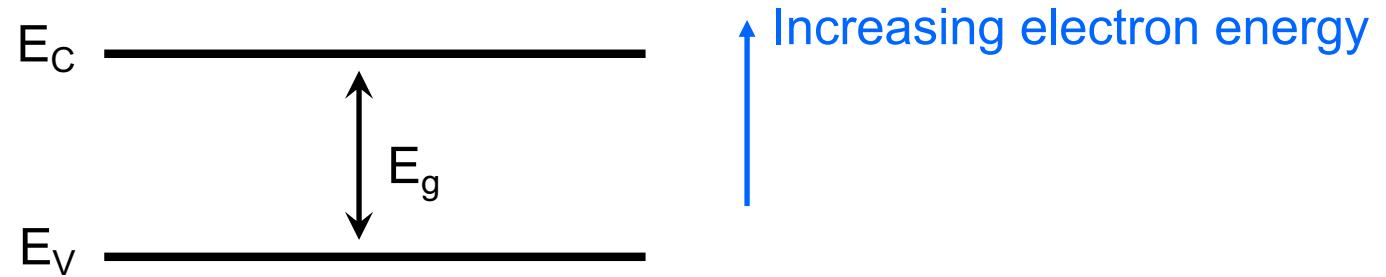
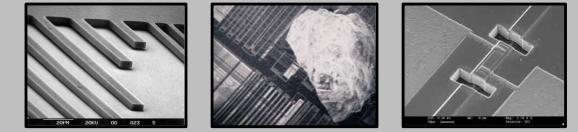
Conduction Band

First unfilled energy band at T=0K

Valence Band

Last filled energy band at T=0K

BAND DIAGRAM



Band Diagram Representation

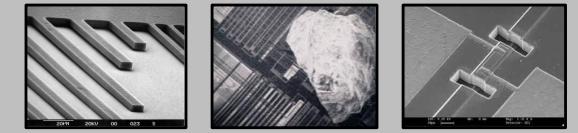
Energy plotted as a function of position

E_C → Conduction band
→ Lowest energy state for a free electron

E_V → Valence band
→ Highest energy state for filled outer shells

E_g → Band gap
→ Difference in energy levels between E_C and E_V
→ No electrons (e^-) in the bandgap (only above E_C or below E_V)
→ $E_g = 1.12\text{eV}$ in Silicon

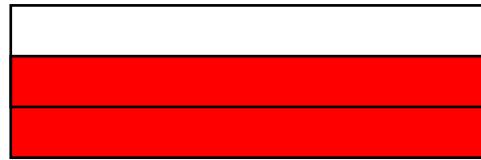
BAND DIAGRAM



Examples

Silver
Copper
Gold

Overlapping Bands



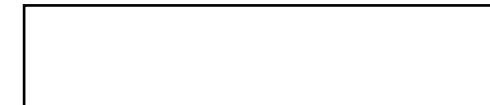
Conductor
Energy gap: none

Silicon
Si/Ge



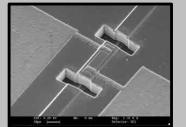
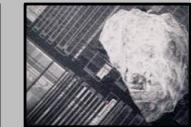
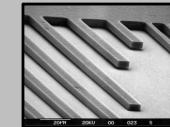
Semiconductor
Energy gap: 0.5 – 3 eV

SiO_2
Diamond

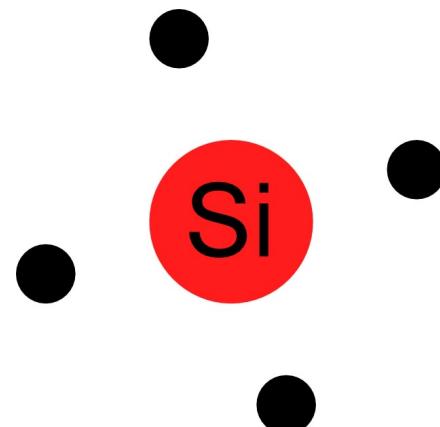


Insulator
Energy gap: >3 eV

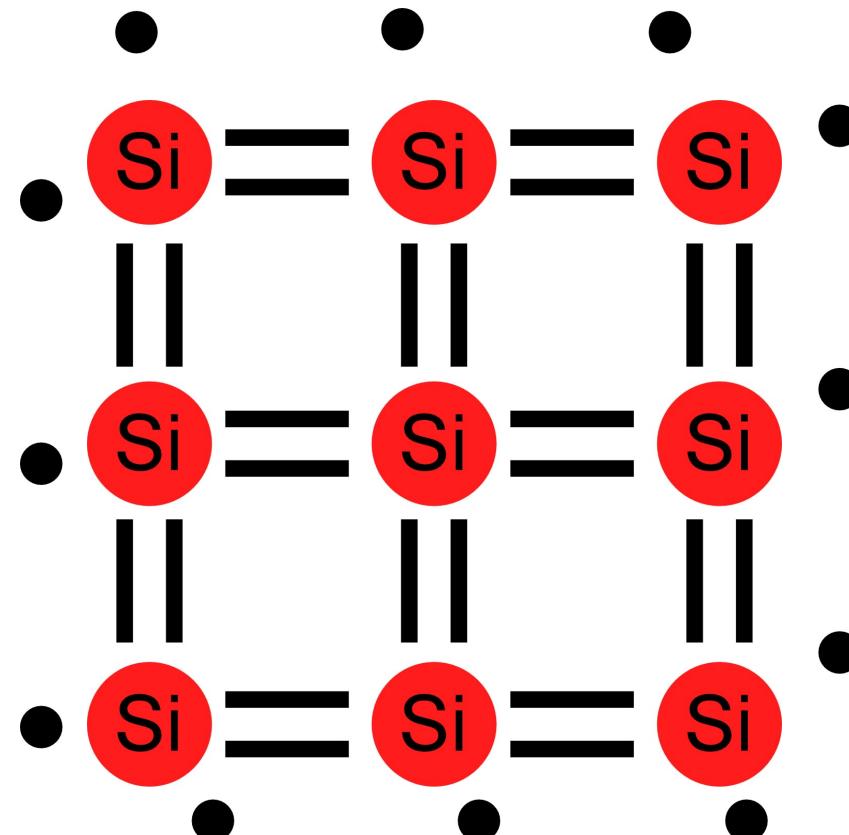
INTRINSIC SEMICONDUCTOR



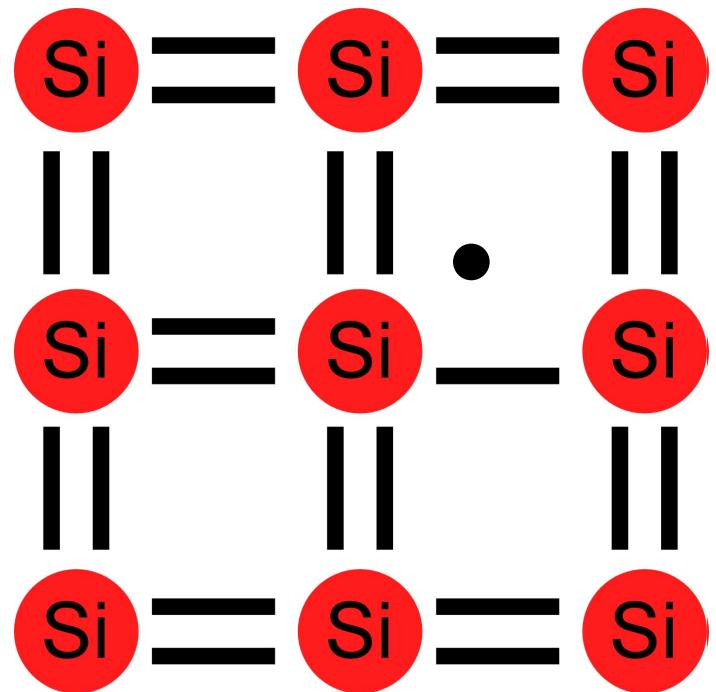
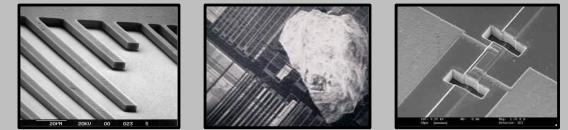
Silicon has 4 outer shell / valence electrons



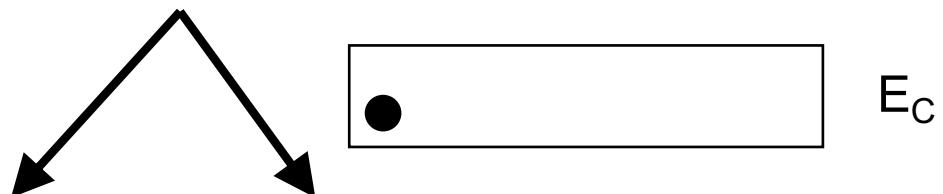
Forms into a lattice structure to share electrons



INTRINSIC SILICON

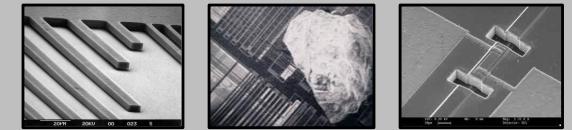


The valence band is full, and no electrons are free to move about



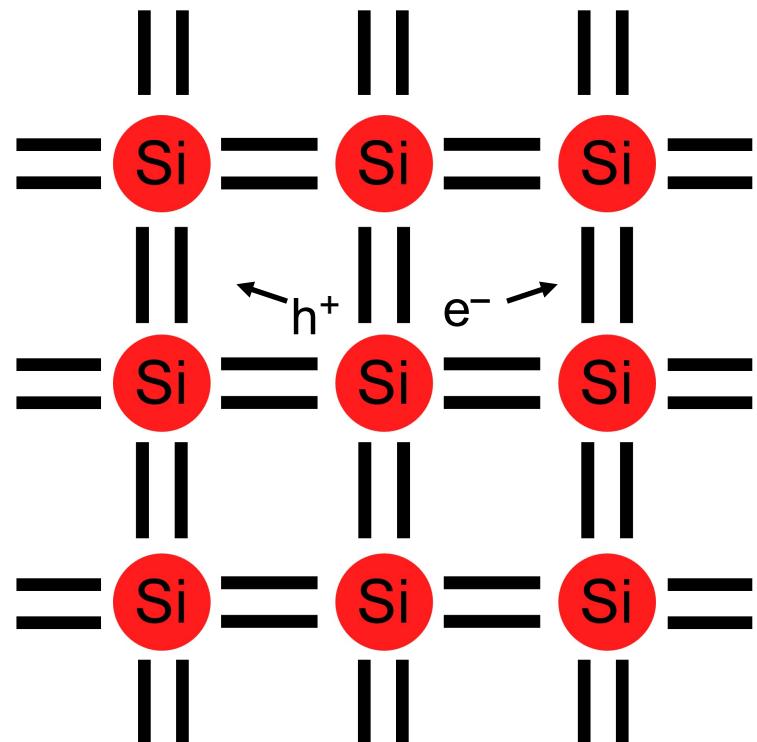
However, at temperatures above $T=0K$, thermal energy shakes an electron free

SEMICONDUCTOR PROPERTIES

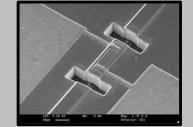
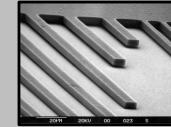


For $T > 0K$

Electron shaken free and can cause current to flow

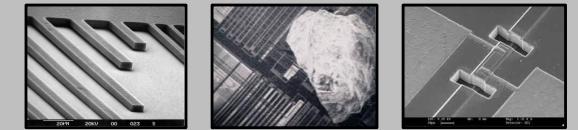


- ❖ Generation – Creation of an electron (e^-) and hole (h^+) pair
- ❖ h^+ is simply a missing electron, which leaves an excess positive charge (due to an extra proton)
- ❖ Recombination – if an e^- and an h^+ come in contact, they annihilate each other
- ❖ Electrons and holes are called “carriers” because they are charged particles – when they move, they carry current
- ❖ Therefore, semiconductors can conduct electricity for $T > 0K$... but not much current (at room temperature (300K), pure silicon has only 1 free electron per 3 trillion atoms)



- ❖ Doping – Adding impurities to the silicon crystal lattice to increase the number of carriers
- ❖ Add a small number of atoms to increase either the number of electrons or holes

PERIODIC TABLE



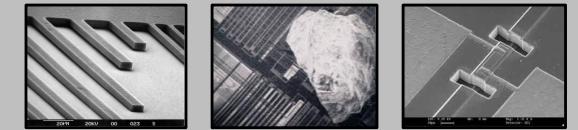
Column 3
Elements have 3 electrons in the Valence Shell

	IIIA	IVA	VA	VIA
	5 10.811 B Boron	6 12.01115 C Carbon	7 14.0067 N Nitrogen	8 15.9994 O Oxygen
IIB	13 26.9815 Al Aluminum	14 28.086 Si Silicon	15 30.9738 P Phosphorus	16 32.064 S Sulfur
30 65.37 Zn Zinc	31 69.72 Ga Gallium	32 72.59 Ge Germanium	33 74.922 As Arsenic	34 78.96 Se Selenium
48 112.40 Cd Cadmium	49 114.82 In Indium	50 118.69 Sn Tin	51 121.75 Sb Antimony	52 127.60 Te Tellurium
80 200.59 Hg Mercury	81 204.37 Tl Thallium	82 207.19 Pb Lead	83 208.980 Bi Bismuth	84 (210) Po Polonium

Column 4
Elements have 4 electrons in the Valence Shell

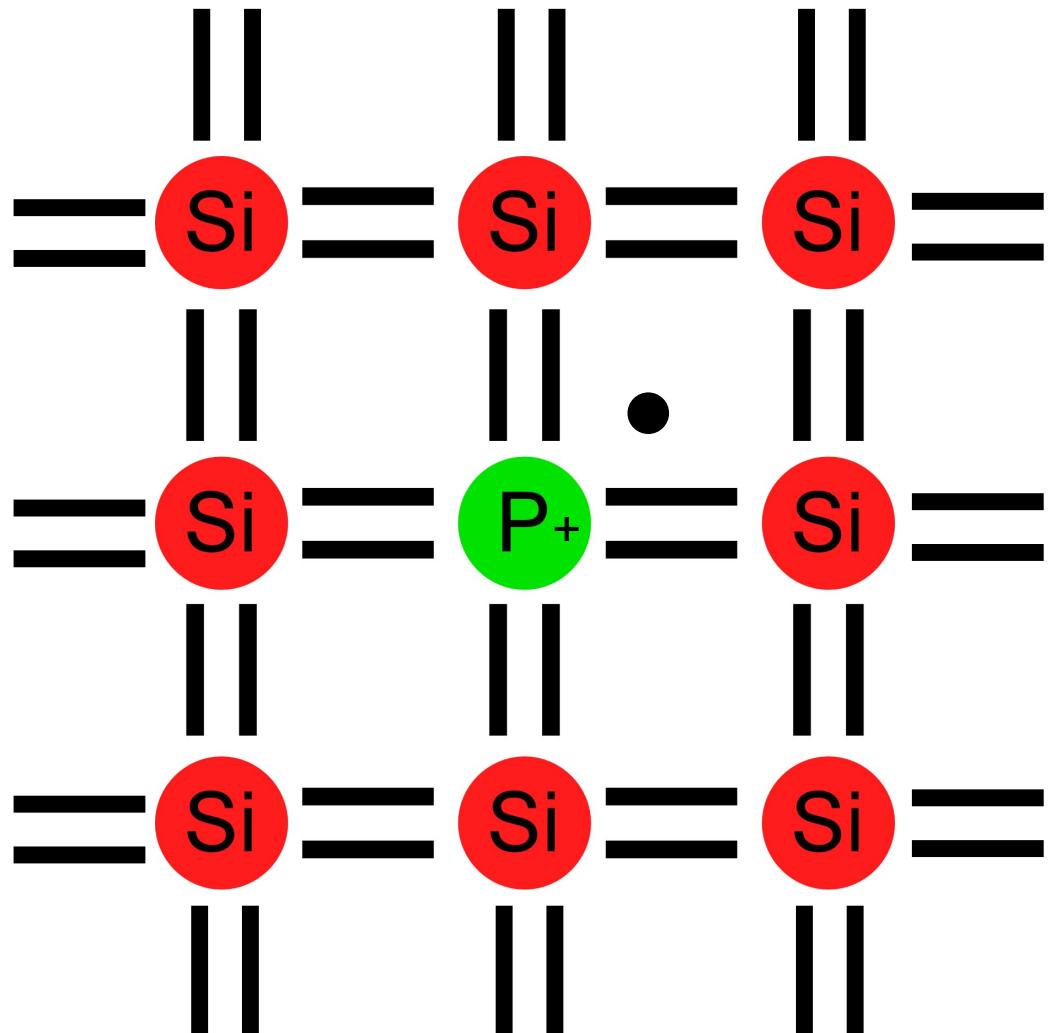
Column 5
Elements have 5 electrons in the Valence Shell

DONORS – nTYPE MATERIAL



Donors

- ❖ Add atoms with 5 valence-band electrons
- ❖ ex. Phosphorous (P)
- ❖ “Donates” an extra e^- that can freely travel around
- ❖ Leaves behind a positively charged nucleus (cannot move)
- ❖ Overall, the crystal is still electrically neutral
- ❖ Called “n-type” material (added negative carriers)
- ❖ N_D = the concentration of donor atoms [atoms/cm³ or cm⁻³]
 $\sim 10^{15}$ - 10^{20} cm⁻³
- ❖ e^- is free to move about the crystal (Mobility $\mu_n \approx 1350$ cm²/V)



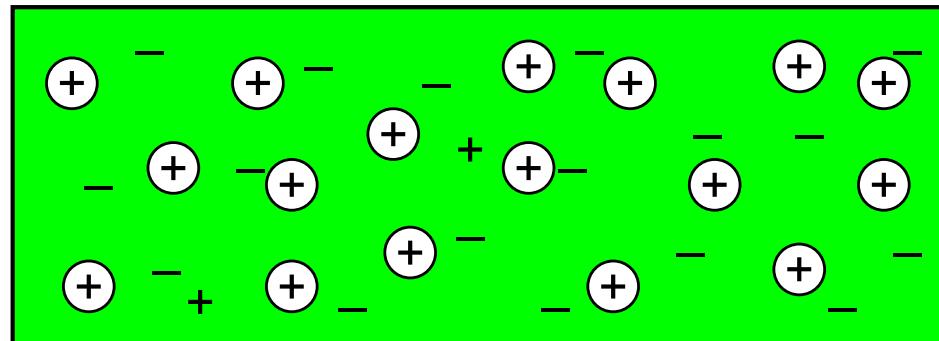
DONORS – nTYPE MATERIAL



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- ❖ Overall, the crystal is still electrically neutral
- ❖ Called “n-type” material (added negative carriers)
- ❖ N_D = the concentration of donor atoms [atoms/cm³ or cm⁻³]
 $\sim 10^{15}$ - 10^{20} cm⁻³
- ❖ e^- is free to move about the crystal
(Mobility $\mu_n \approx 1350$ cm²/V)

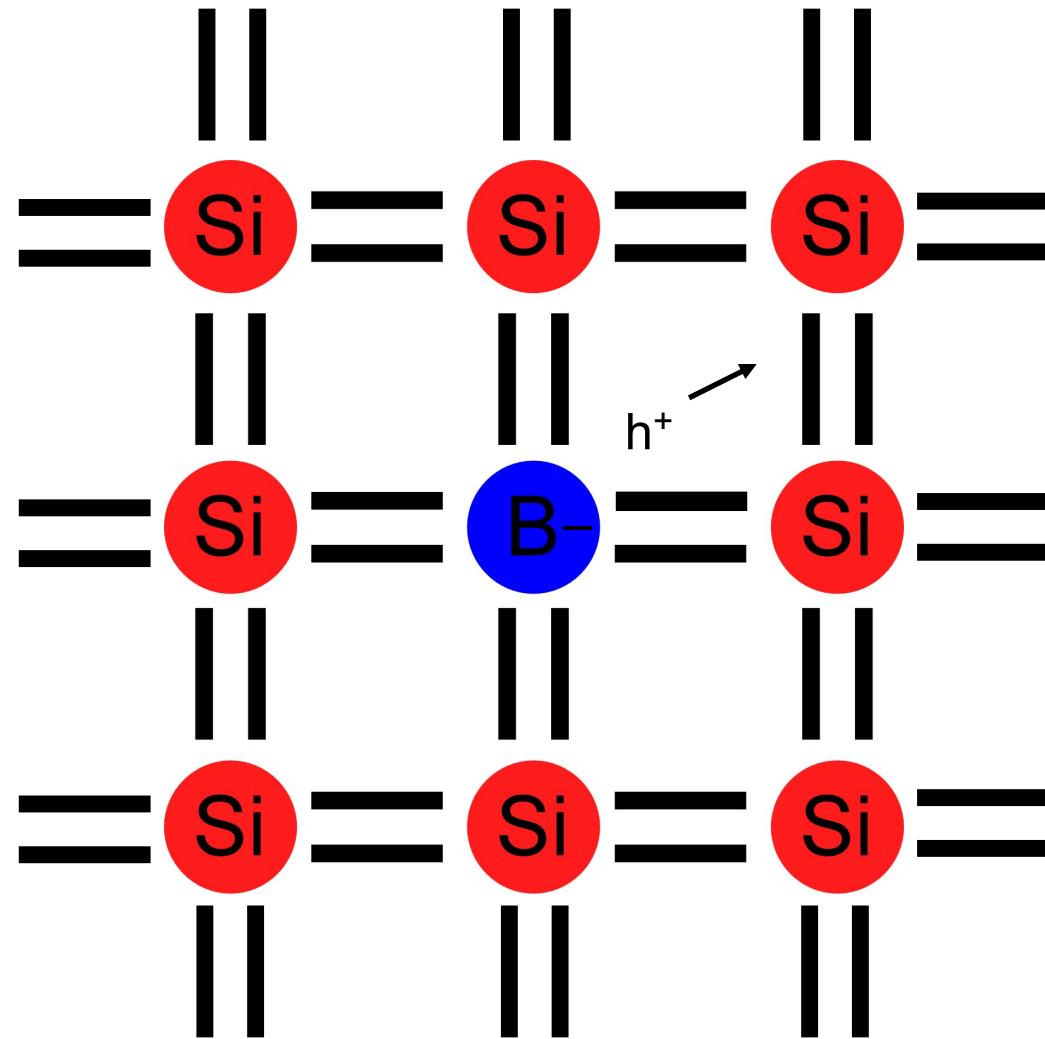
n-Type Material



Shorthand notation

- ⊕ Positively charged ion; immobile
- ⊖ Negatively charged e^- ; mobile;
Called “majority carrier”
- ⊕ Positively charged h^+ ; mobile;
Called “minority carrier”

ACCEPTORS – pTYPE MATERIAL



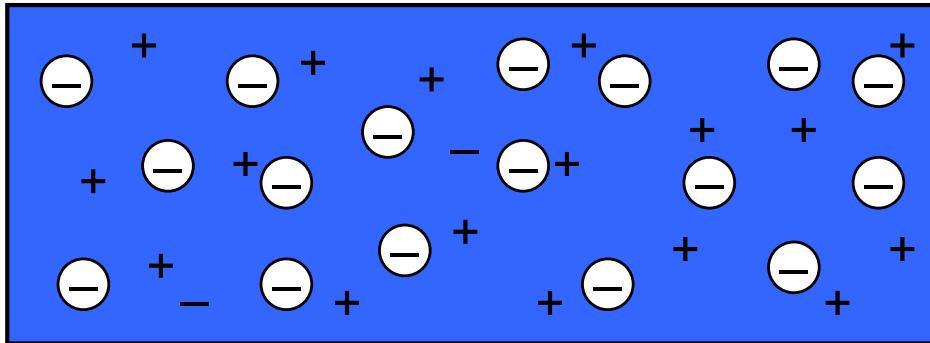
Acceptors

- ❖ Add atoms with only 3 valence-band electrons
- ❖ ex. Boron (B)
- ❖ “Accepts” e^- and provides extra h^+ to freely travel around
- ❖ Leaves behind a negatively charged nucleus (cannot move)
- ❖ Overall, the crystal is still electrically neutral
- ❖ Called “p-type” silicon (added positive carriers)
- ❖ N_A = the concentration of acceptor atoms [atoms/cm³ or cm⁻³]
- ❖ Movement of the hole requires breaking of a bond! (This is hard, so mobility is low, $\mu_p \approx 500\text{cm}^2/\text{V}$)

ACCEPTORS – pTYPE MATERIAL



p-Type Material



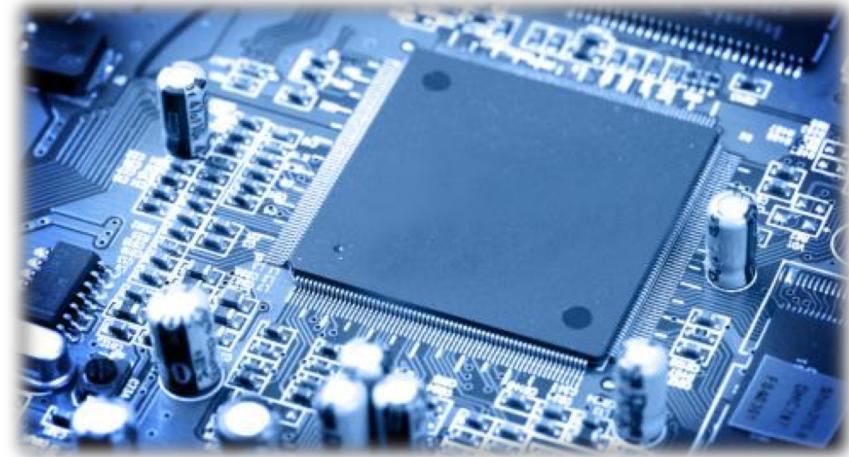
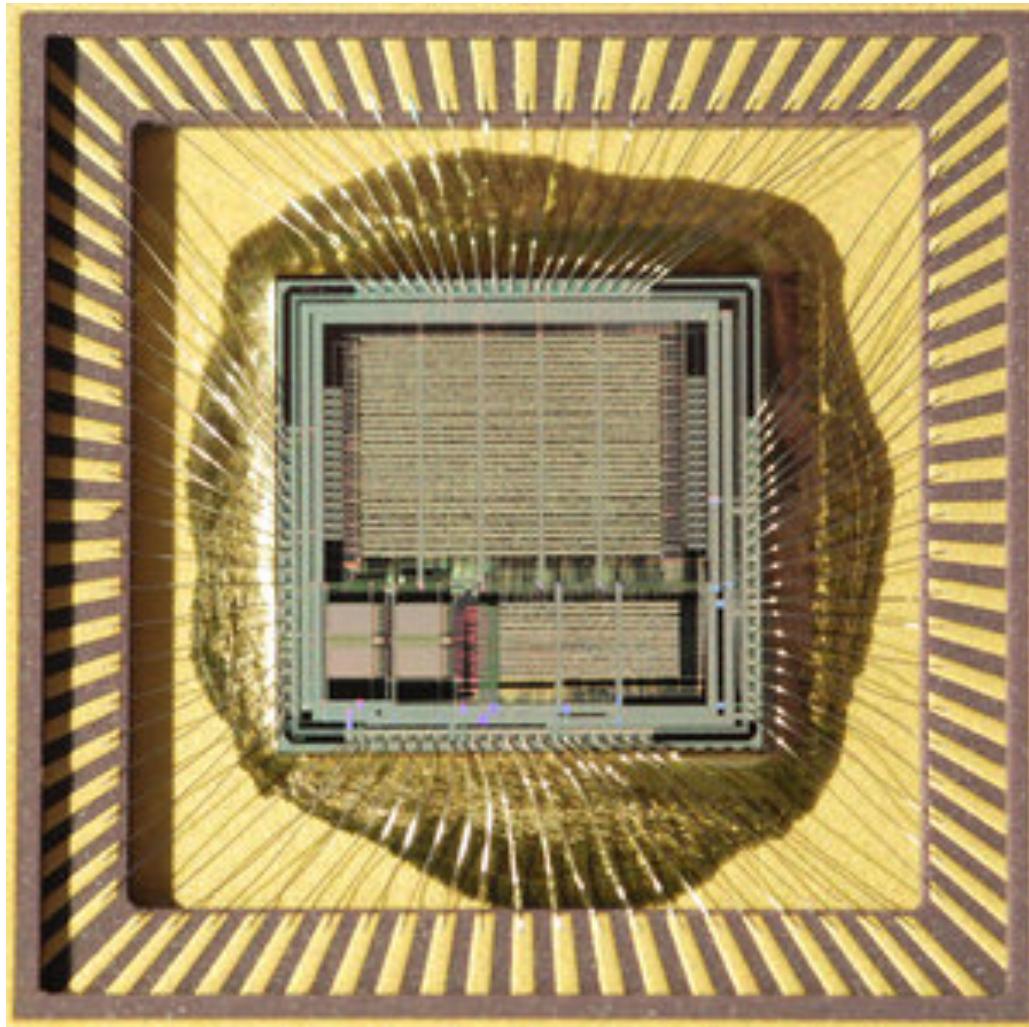
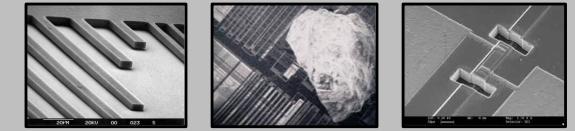
Shorthand notation

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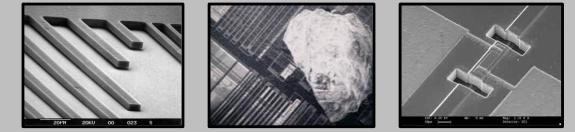
PROPERTIES OF MATERIALS



Important compounds used in microelectronics are:

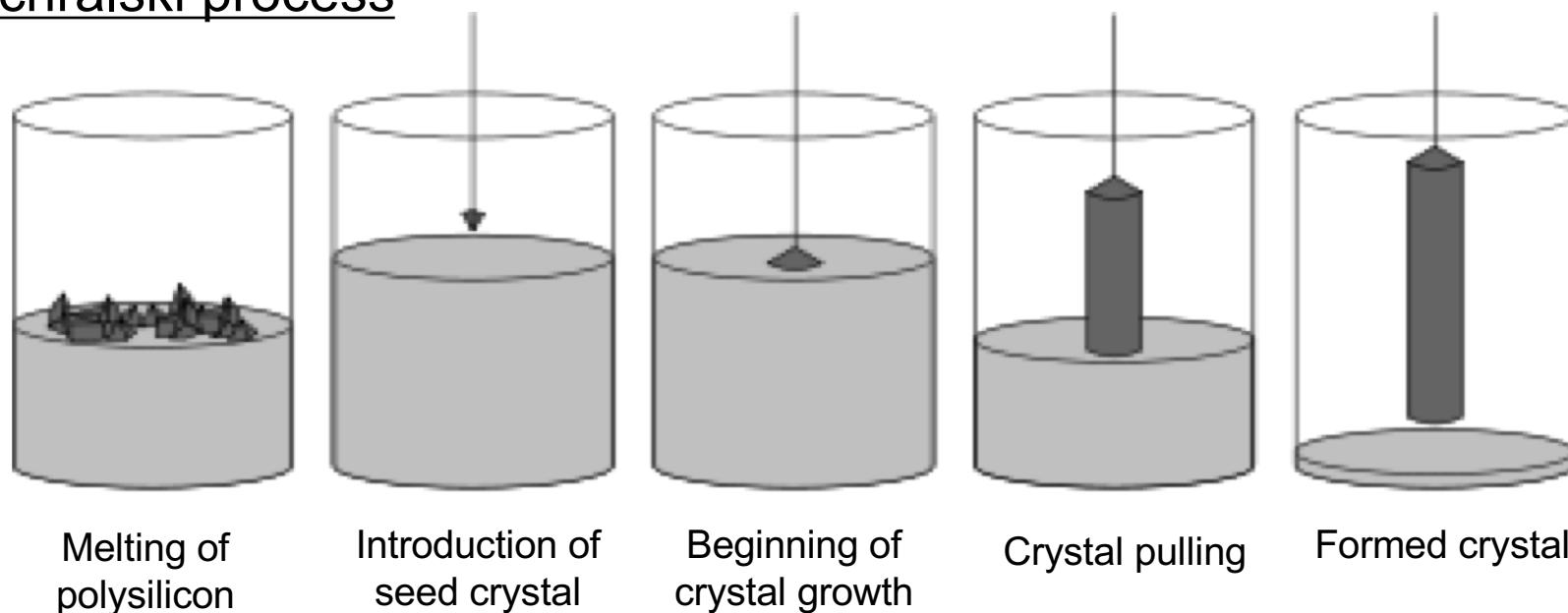
- ❖ Silicon dioxide
- ❖ Polysilicon
- ❖ Silicon nitride

MONOCRYSTAL SILICON

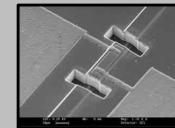
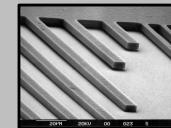


- ❖ The monocrystalline silicon used as bulk material is in the form of a thin (300-1000 μm) slice (generally referred to as *wafer*)
- ❖ The wafers are made by slicing a single crystal ingot whose diameter ranges from 4 to 12 inches
- ❖ This silicon is extremely pure (*electronic grade*) and it contains less than one part per billion of impurities

Czochralski process

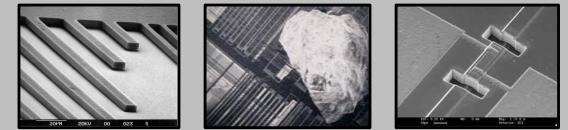


MONOCRYSTAL SILICON

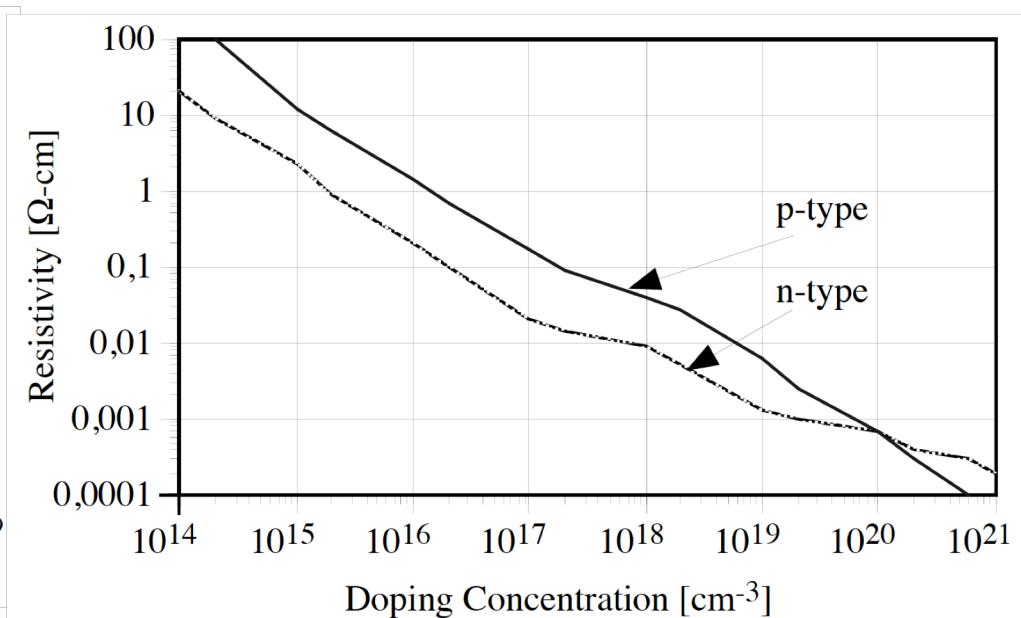
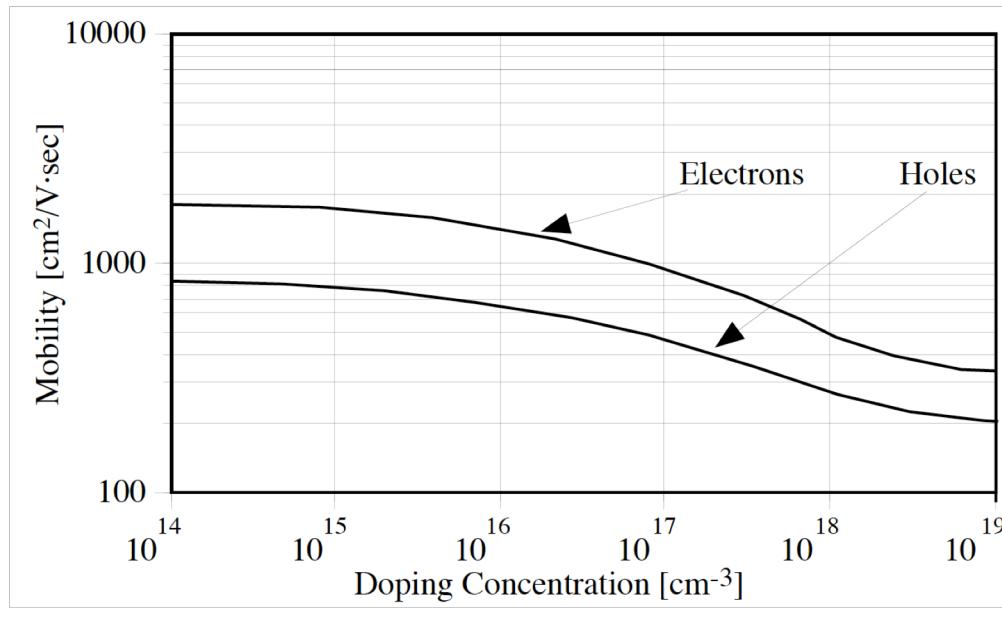


Property	Value	Dimension
Atomic density	$5 \cdot 10^{22}$	atoms/cm ³
Density	2.33	g/cm ³
Atomic weight	28.1	g/mole
Reticular constant	0.543	nm
Thermal Conductivity	1.41	$\Omega/\text{cm } ^\circ\text{C}$
Intrinsic resistivity (@ 300 °K)	$2.5 \cdot 10^5$	$\Omega\text{-cm}$
Relative dielectric constant, ϵ_r	11.9	-
Absolute dielectric constant, ϵ_0	$8.858 \cdot 10^{-14}$	F/cm

SILICON PROPERTIES



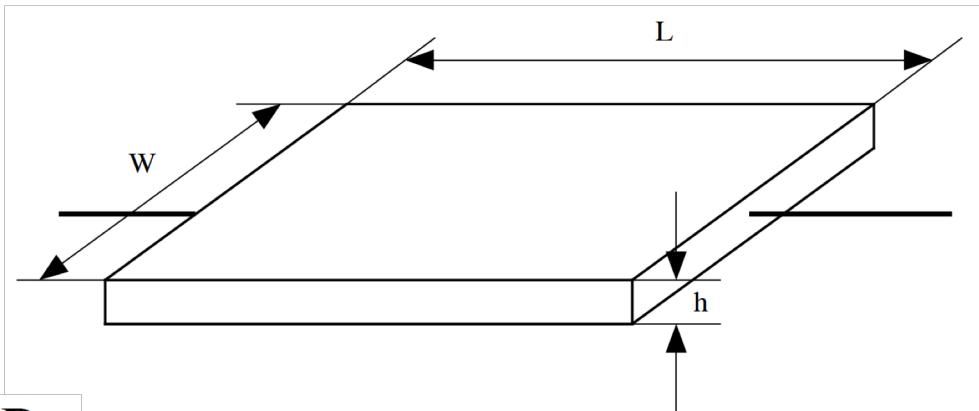
- ❖ Surface mobility of electrons and holes as a function of the doping (both n and p type) at room temperature (300 K)
- ❖ Resistivity of bulk silicon as a function of the doping (both n and p type)



LAYERS RESISTANCE



- ❖ Doped layers are used to obtain active devices – source and drain of MOS transistors – where minimum resistance is desired (to speed up the performance)
- ❖ Doped layers are used to create integrated resistors as well
- ❖ An estimation of the achieved resistance value is needed



$$R = \frac{\rho L}{A} = \frac{\rho L}{hW} = R_{\square} \frac{L}{W}$$

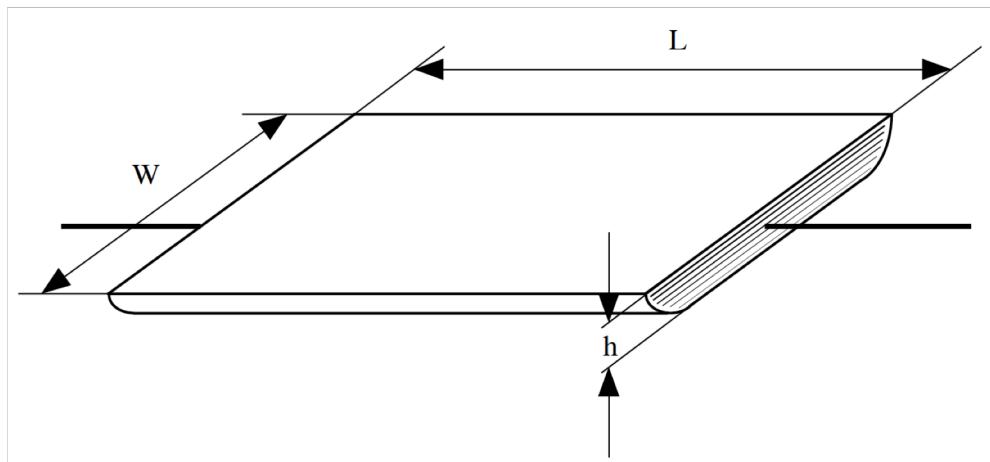
ρ is the electrical resistivity

R_{\square} : is the sheet resistance of the material (specific for each technology). It is called resistance per square and it is the resistance of a parallelepiped of material with $W/L=1$. It is measured in Ohm/square.

LAYERS RESISTANCE



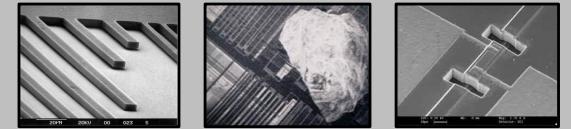
- ❖ In diffused layers, the resistivity is not constant, but it increases with depth
- ❖ For more realistic calculations, we have to describe the resistor as the parallel connection of infinitesimal elements (having the same width, for simplicity, even though it is an approximation)



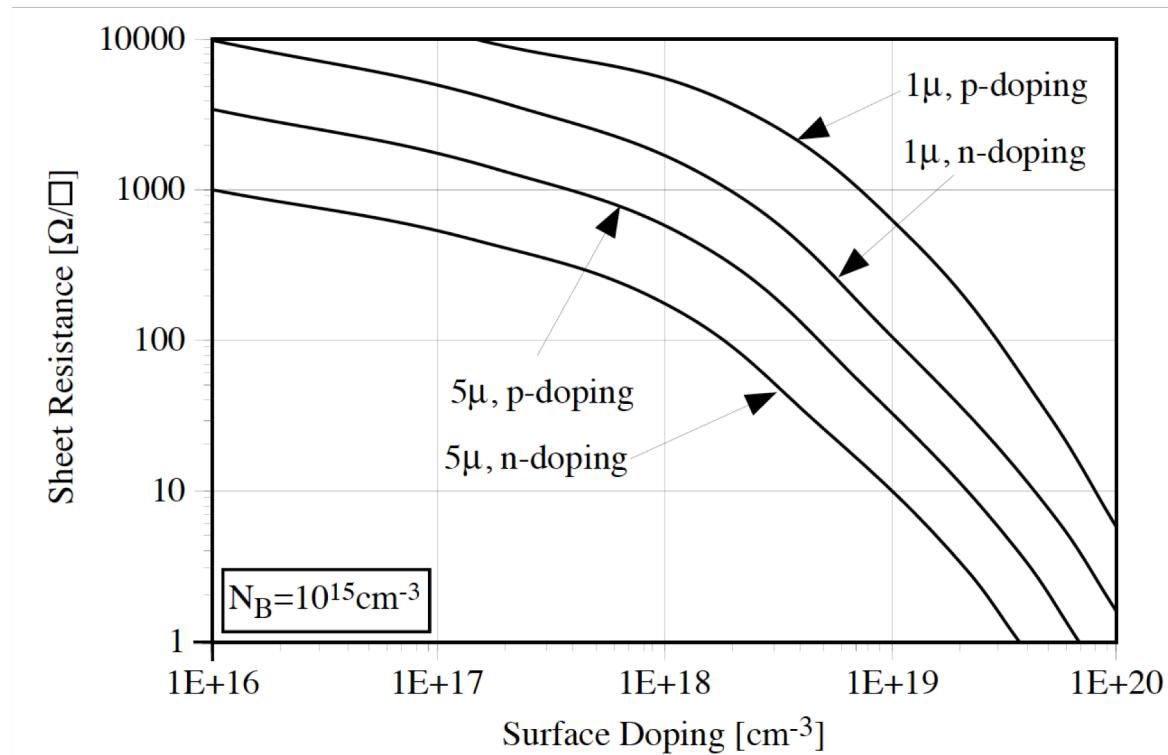
$$G = \frac{1}{R} = \int_0^h dG = \int_0^h \sigma(z) \frac{W}{L} dz = \frac{1}{R_{\square}} \frac{W}{L}$$

σ is the electrical conductivity

LAYERS RESISTANCE



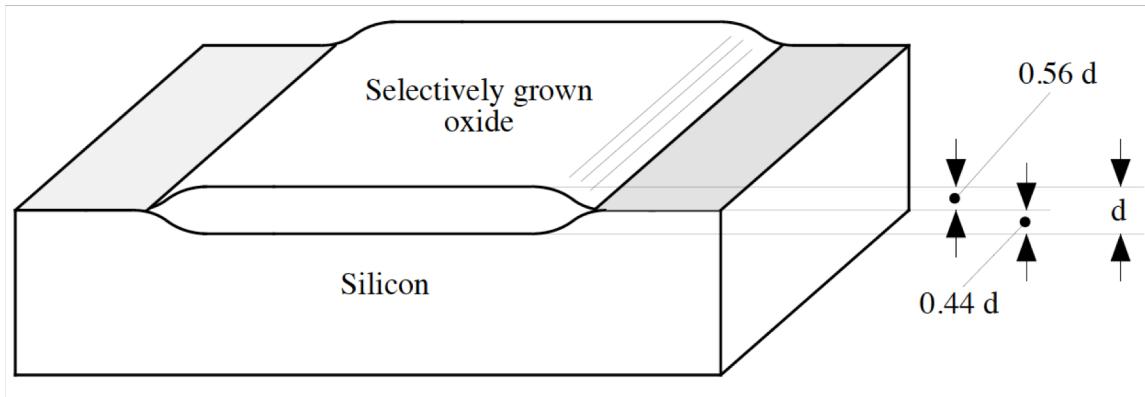
- ❖ Sheet resistance for a typical CMOS technology layer with two different thickness (1 μm and 5 μm) as a function of the surface doping. The substrate doping is 10^{15} cm^{-3} . Doping in the depth has a Gaussian profile.



SILICON DIOXIDE



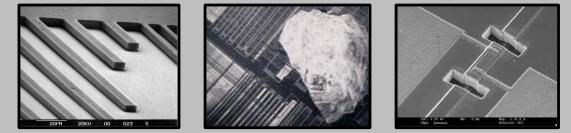
- ❖ Silicon dioxide is an excellent insulator and, in microelectronics, it is used or to make active devices or to ensure insulation.
- ❖ Silicon dioxide can be originated in two ways: it can be grown by thermal oxidation of silicon or by chemical vapor deposition (CVD).
- ❖ Thermal growth can be achieved in dry or wet (in presence of oxygen or water) conditions at a temperature that ranges from 800° C to 1100° C.
- ❖ The growth of SiO_2 determines a silicon consumption: if d is the thickness of the grown oxide, $0.44d$ of silicon is consumed.



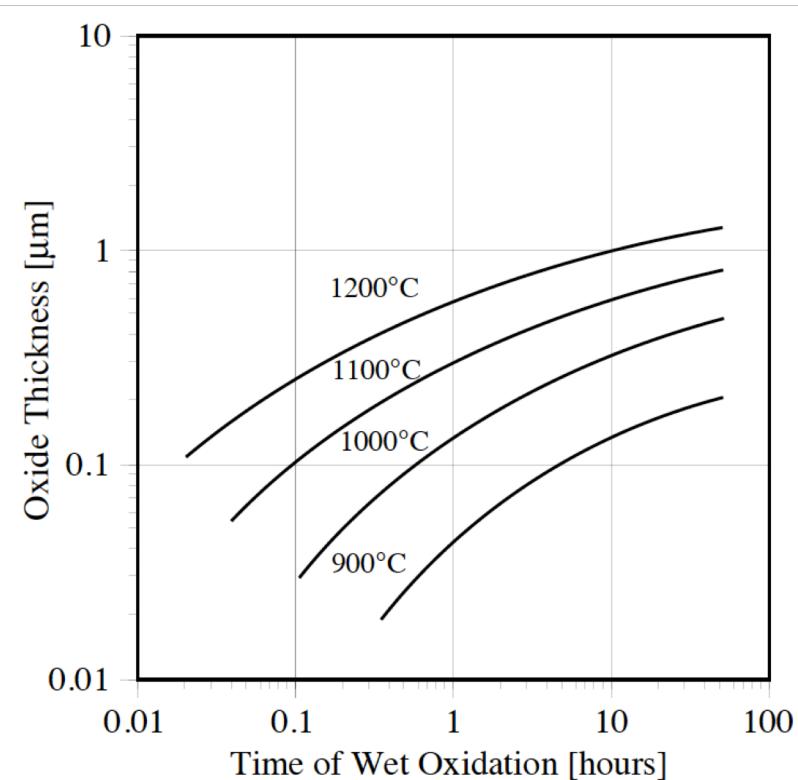
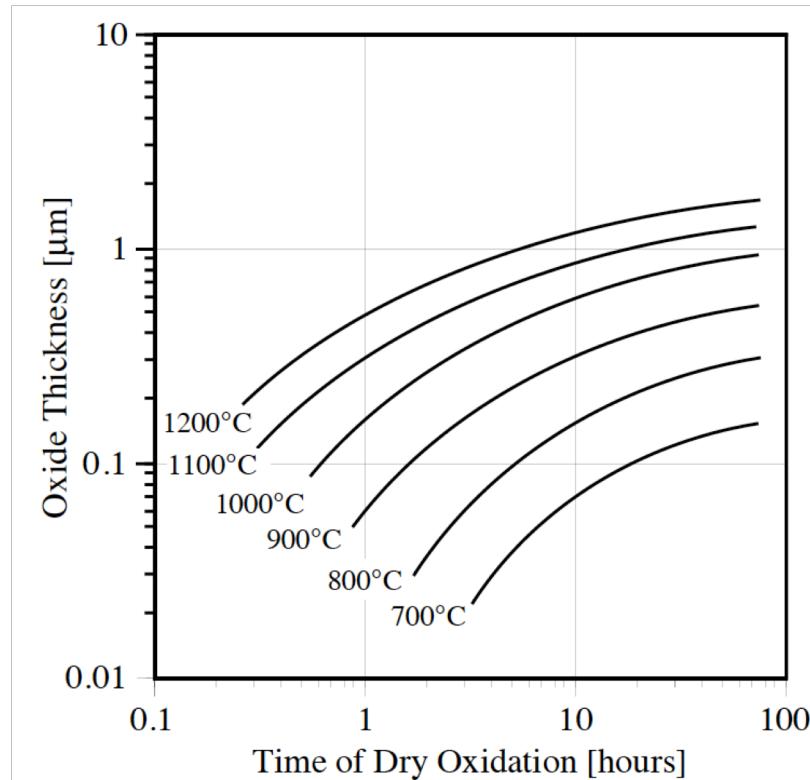
Reliability problems

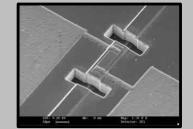
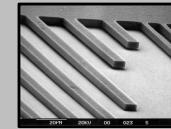
Non-flat surfaces: risk of micro-cracks when the layer thickness is lower than the surface curvature

SILICON DIOXIDE

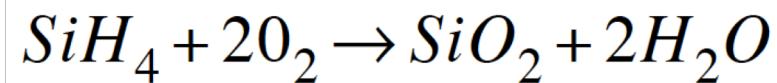


- ❖ Growth speed depends on the operating temperature of the reactor
- ❖ Wet oxidation growth speed is higher than the one in dry conditions
- ❖ The growth speed is not constant, but decreases as the oxide thickness increases



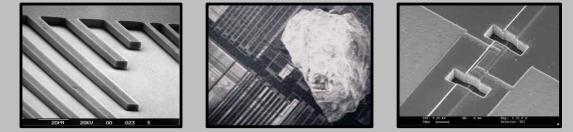


- ❖ Chemical vapor deposition (CVD):



- ❖ Operating temperature: from 300° C to 500° C.
- ❖ The reaction can take place at low pressure (LP-CVD) or at the atmospheric pressure (AP-CVD).
- ❖ CVD growth speed is higher (one order of magnitude) than that of thermal oxidation.
- ❖ Main advantage: the relatively low temperature operation. High temperature must be avoided after aluminum deposition. Low temperature operations preserve the doping profiles.
- ❖ CVD widely employed for surface protection.

SILICON DIOXIDE



Thickness of silicon dioxide depends on the specific fabrication step.
Typical figures:

- ❖ Gate of transistors: 5-15 nm
- ❖ Poly-metal insulation: 500 nm
- ❖ Field protection: 600 nm

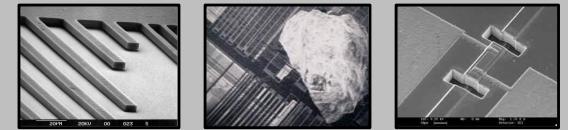
Property	Value	Dimension
Density	2.22	g/cm ³
Dielectric strength	2-8 10 ⁶	V/cm
Resistivity (@ 300 °K)	10 ¹⁵ - 10 ¹⁷	Ω cm
Relative dielectric constant	3.4 - 4.2	

POLYSILICON

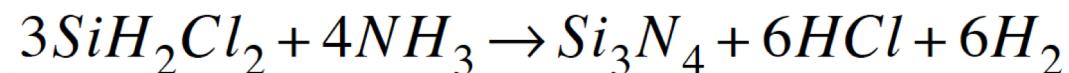
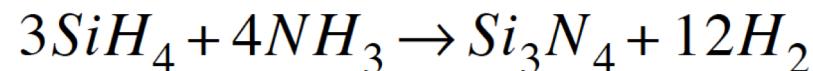


- ❖ Polysilicon is used to create MOS transistor gates, to make capacitor plates and for short interconnections
- ❖ Polysilicon is grown by pyrolytic decomposition of silane (SiH_4) at about 600° C
- ❖ The polycrystalline structure is made of monocrystal grains with a size in the range of $0.1\text{-}1 \mu\text{m}$
- ❖ The thickness of polysilicon layers ranges from 200 nm to 600 nm with a typical standard deviation of 2%
- ❖ The mobility is low because of the grain border resistance
- ❖ To have low sheet resistance, polysilicon must be strongly doped ($10^{20}\text{-}10^{21} \text{ cm}^{-3}$). The sheet resistance is on the order of 20-40 Ω/square
- ❖ Special technological steps (use of sandwich layers) can reduce the sheet resistance by a factor 10-20

SILICON NITRIDE

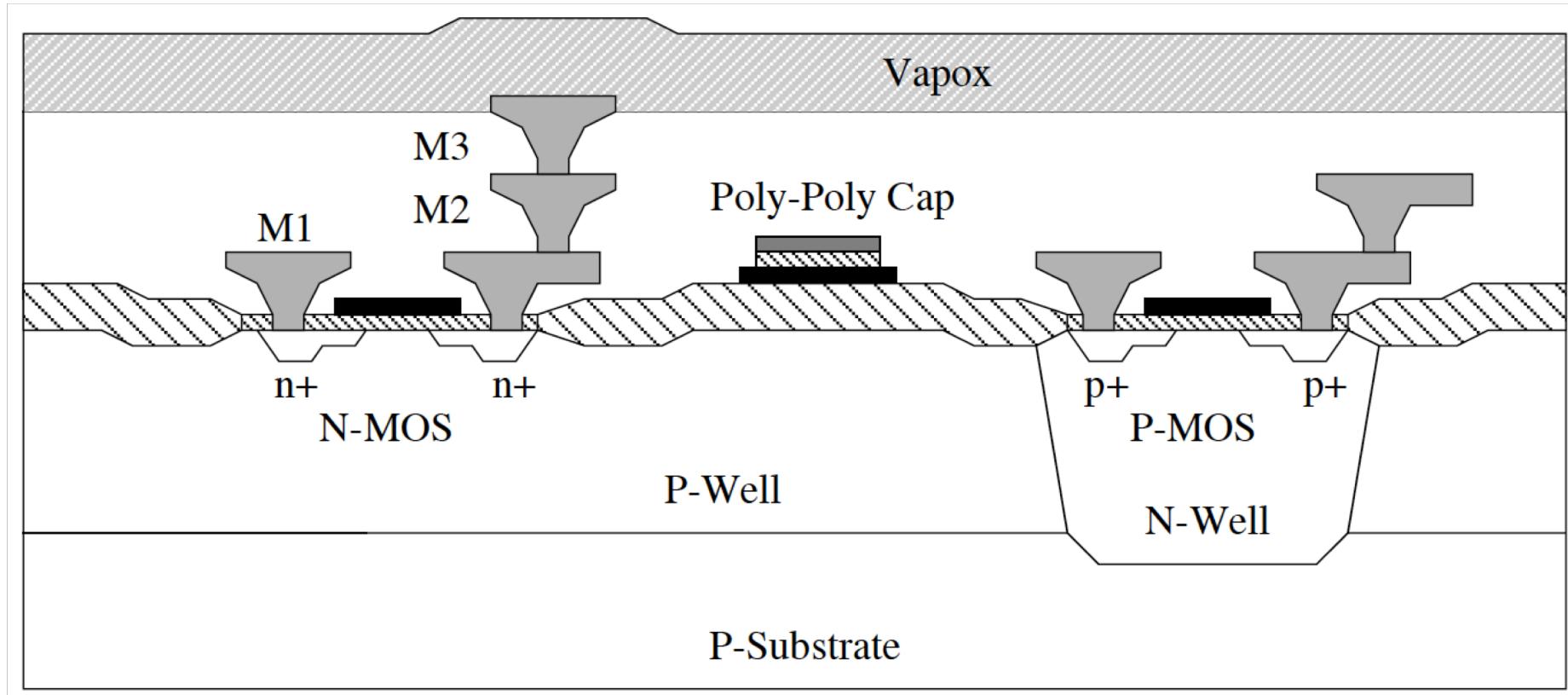
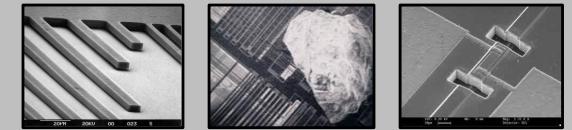


- ❖ Silicon nitride is mostly used to protect surfaces
- ❖ It is used in intermediate technological steps as well
- ❖ It is grown by decomposing silane or dichlorosilane and ammonia at 700-800 ° C



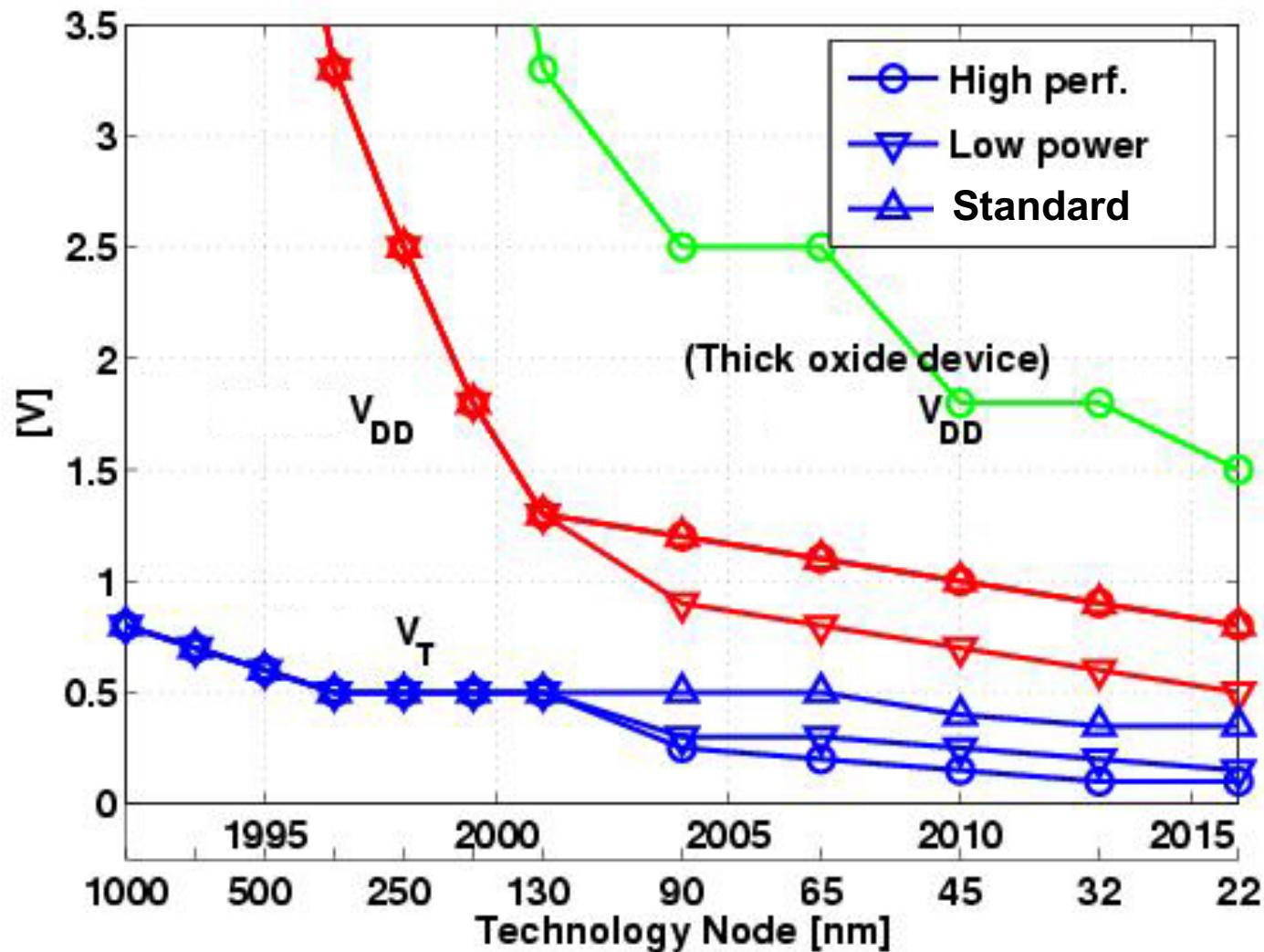
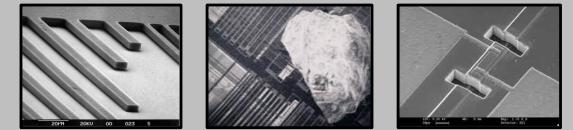
- ❖ The growth speed is excellent: 10-20 nm/minute
- ❖ Insulating properties optimal: the resistivity is 10^{14} - 10^{16} Ω/cm
- ❖ Dielectric strength: 5-10 MV/cm

CMOS TECHNOLOGY

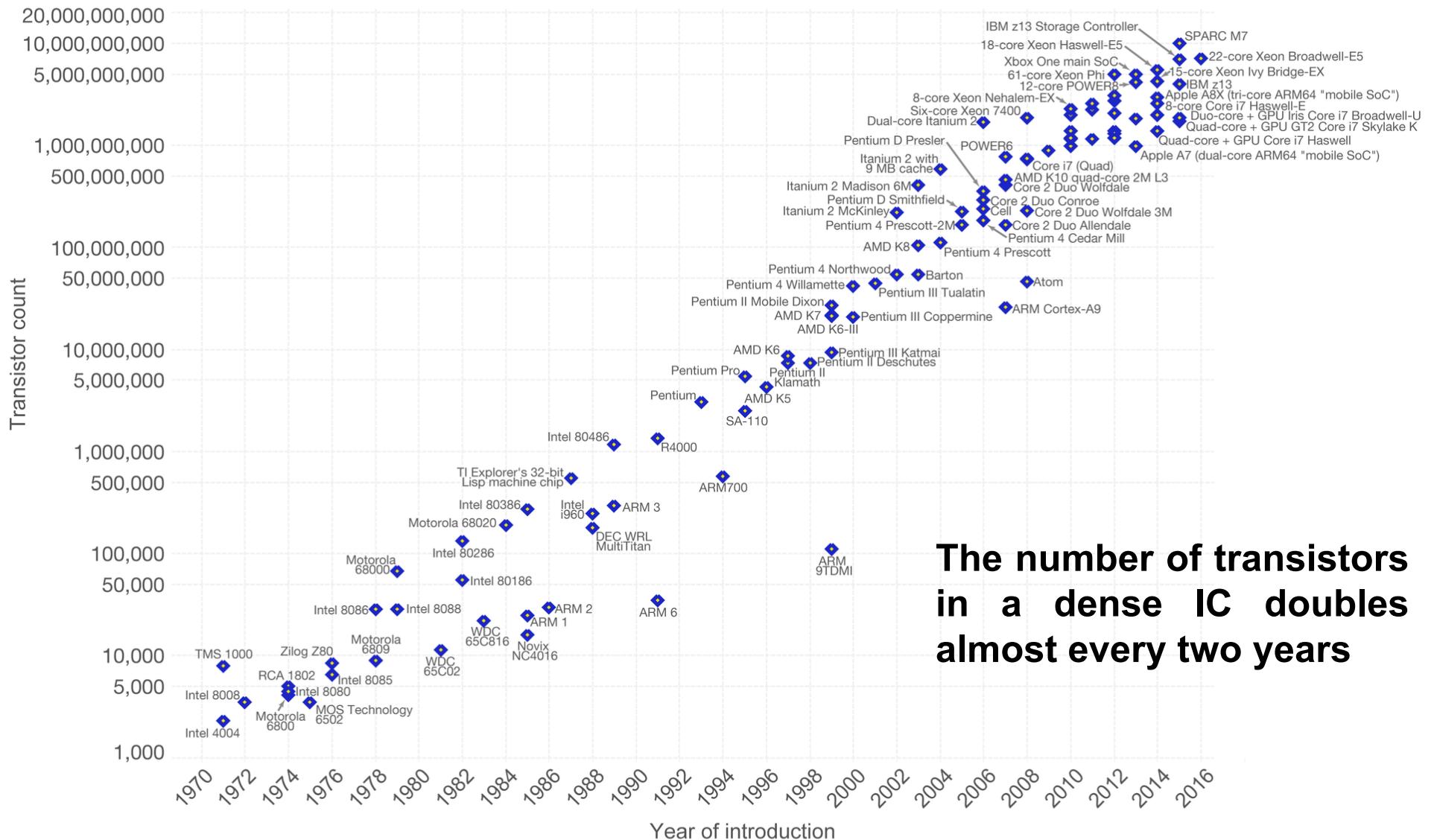
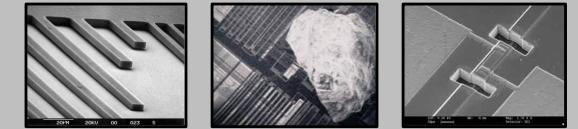


Cross section of a typical p-substrate CMOS process. Poly-to-poly caps are also shown.

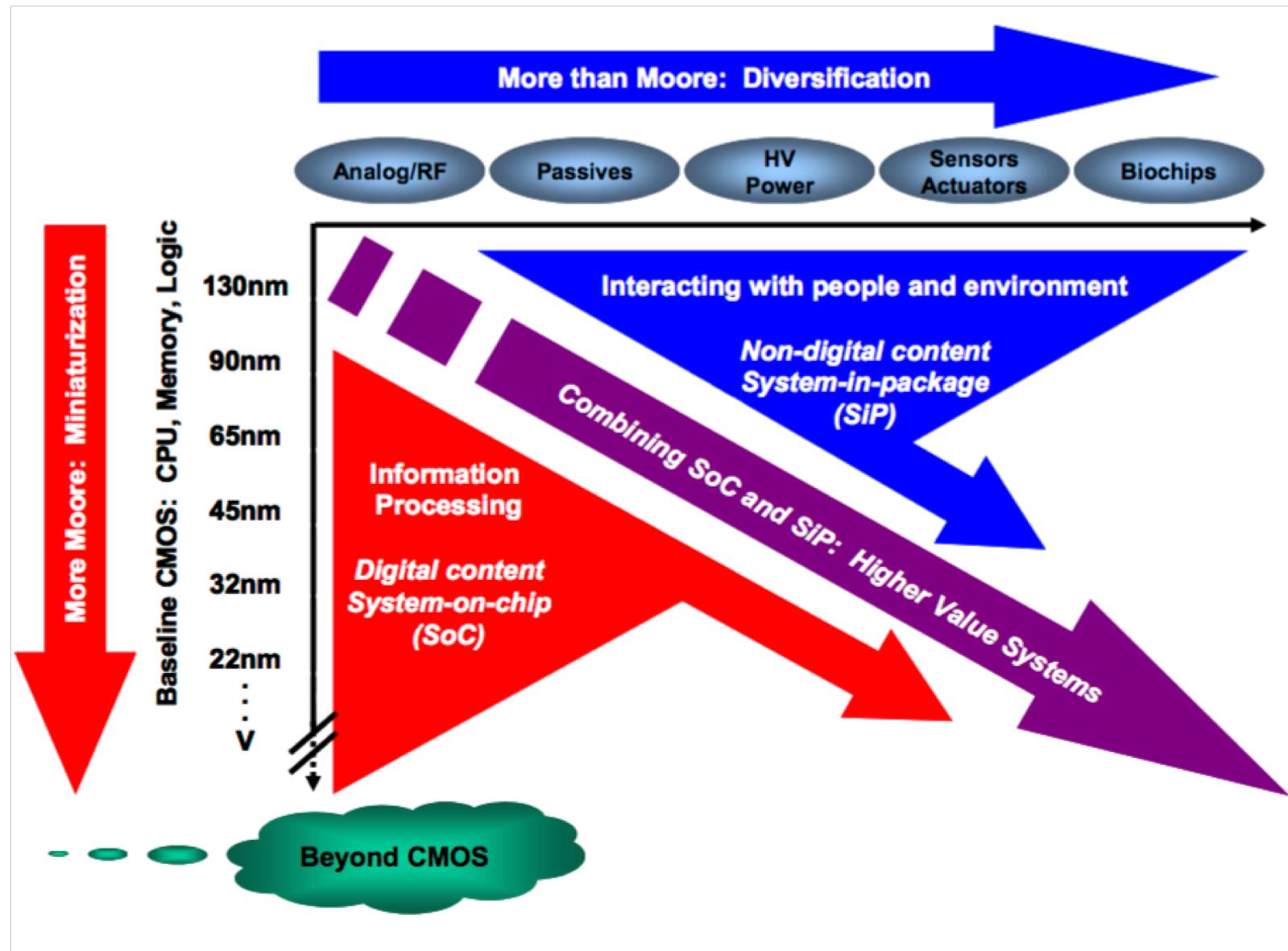
CMOS TECHNOLOGY



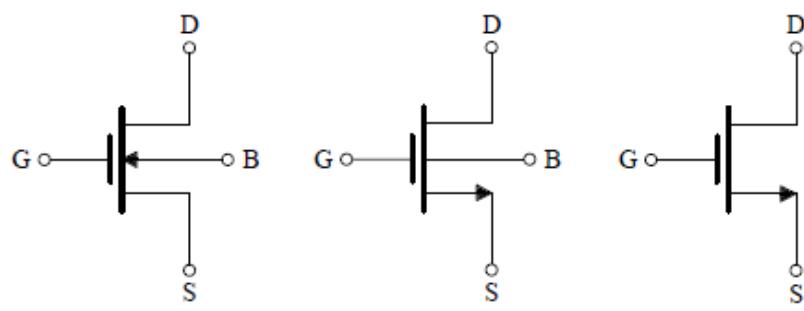
MOORE'S LAW



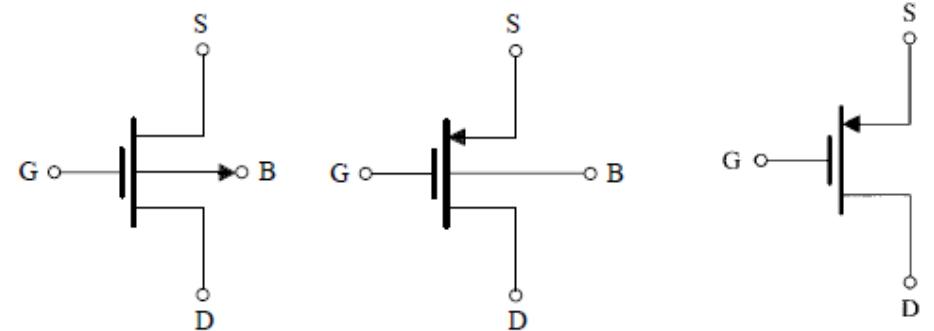
MOORE'S LAW and BEYOND



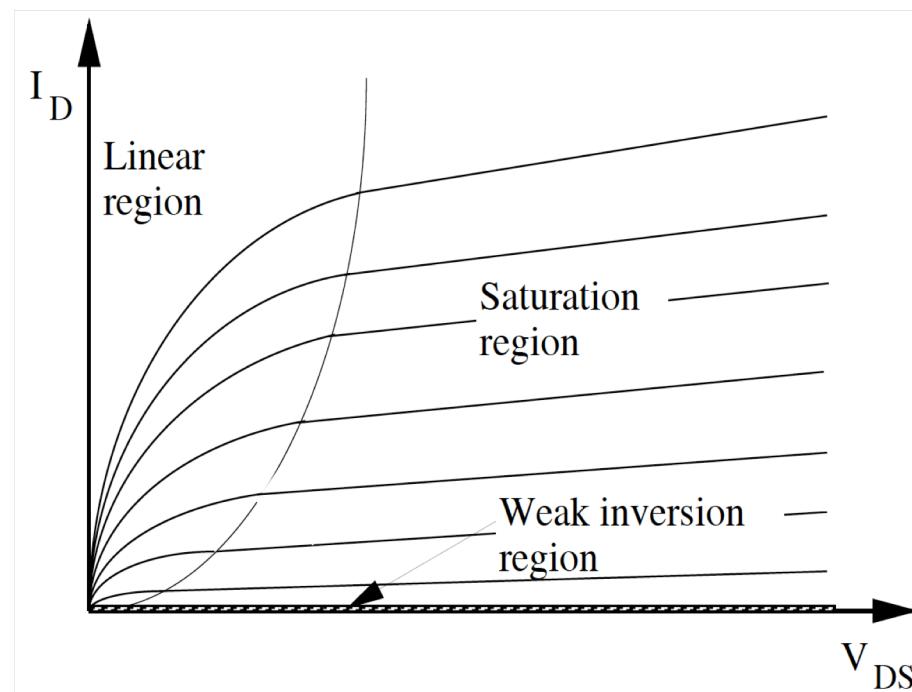
I-V CHARACTERISTICS



NMOS



PMOS



WEAK INVERSION REGION

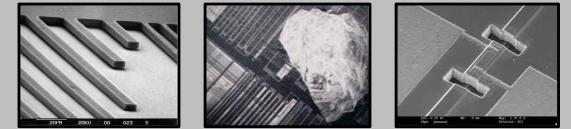


- ❖ $V_{GS} < V_{th}$
- ❖ The analytical study comes from the analysis of the band diagram. It denotes the presence of two back to back pn diodes in the source-channel-drain structure where the saturation current depends on the barrier height

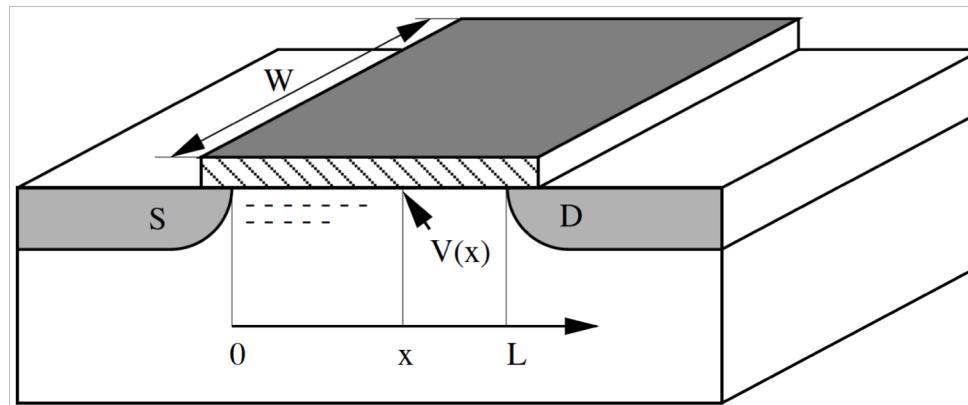
$$I_D = I_{D0} e^{qV_G/nkT} e^{-qV_B/nkT}$$

- ❖ A MOS transistor in weak inversion (sub-threshold) behaves like a bipolar transistor
- ❖ The I-V characteristic changes exponentially with variations of the control voltage, V_G (like in a bipolar transistor, disregarding n)
- ❖ n is technology dependent and ranges from 1 to 3

LINEAR (or TRIODE) REGION



- ❖ $V_{GS} > V_{th}$ and $V_{DS} < V_{GS} - V_{th}$



- ❖ When the V_{GS} exceeds V_{th} , the oxide-silicon interface is in strong inversion and the accumulation of mobile charges at the oxide-silicon interface forms the so called *inversion layer*
- ❖ For a generic position x , its charge per unity area is:

$$Q_{inv}(x) = C_{ox} \{ V_{GS} - V(x) - V_{Th}(x) \}$$

- ❖ $V(x)$ is the drop voltage from source to x

LINEAR (or TRIODE) REGION



- ❖ The resistance of an incremental element $x, x+dx$ in the channel is:

$$dR = \frac{dx}{\sigma A} = \frac{dx}{Q_{inv}(x)\mu W}$$

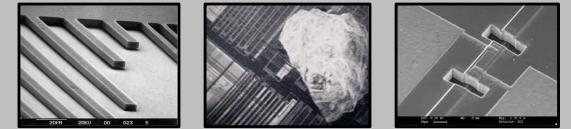
- ❖ The drop voltage across this element is:

$$dV = I_D dR = \frac{I_D dx}{C_{ox}[V_{GS} - V_{Th} - V(x)]\mu W}$$

- ❖ By integrating along the channel and neglecting the threshold voltage change along the channel due to the body effect, we get:

$$I_D = \mu C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_{Th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

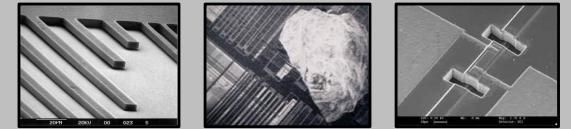
LINEAR (or TRIODE) REGION



$$I_D = \mu C_{ox} \left(\frac{W}{L} \right) \left[(V_{GS} - V_{Th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$$

- ❖ The drain current is larger with electrons acting as mobile carriers (the holes mobility is lower) and for thinner gate oxides
- ❖ The above expression represents a parabola in the I_D - V_{DS} plane with a maximum in $V_{DS} = V_{GS} - V_{th}$
- ❖ When using the above condition in the expression of Q_{inv} , the charge of the inverted layer at the drain ($x=L$, $V(L)=V_{DS}$) goes to 0. The above condition defines, hence, the limit of the triode region
- ❖ For small V_{DS} ($V_{GS} - V_{th} \gg V_{DS}$), the I-V curve approximates a straight line whose slope is proportional to V_{GS} . This feature is often used to achieve a voltage controlled resistor

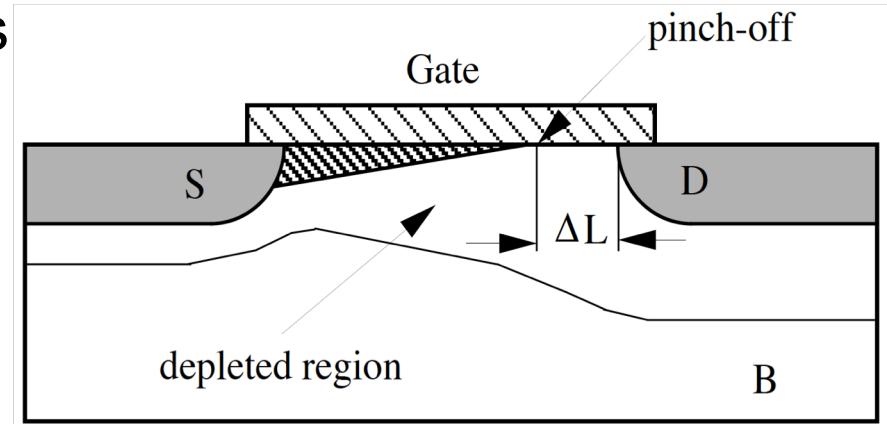
SATURATION REGION



- ❖ $V_{GS} > V_{th}$ and $V_{DS} > V_{GS} - V_{th}$
- ❖ As $V(x)$ increases, $Q_{inv}(x)$ decreases
- ❖ Its minimum is at the drain:

$$Q_{inv}(L) = C_{ox} (V_{GS} - V_{TH} - V_{DS})$$

- ❖ If $V_{DS} = V_{sat} = V_{GS} - V_{th}$, $Q_{inv}(L) = 0$
- ❖ The drain is in the pinch-off condition
- ❖ If $V_{DS} > V_{sat}$, the pinch-off point moves toward the source. The part of the V_{DS} exceeding V_{sat} drops along the depleted region, ΔL , extending from the pinch-off to the drain



$$\Delta L = \sqrt{\frac{2\epsilon}{qN_A}} (V_{DS} - V_{sat})$$

SATURATION REGION



- The structure can be assumed equivalent to a transistor with the pinch-off at the drain but with length reduced by ΔL . It results:

$$I_D = \frac{1}{2} \mu C_{ox} \frac{W}{L - \Delta L} (V_{GS} - V_{Th})^2 = \left(\frac{1}{2} \mu C_{ox} \frac{W}{L} V_{DS}^2 \right) \frac{L}{L - \Delta L}$$

$$\frac{L}{L - \Delta L} = \frac{1}{1 - \sqrt{\frac{2\epsilon}{qN_A L^2} (V_{DS} - V_{sat})}} \approx 1 + \sqrt{\frac{\epsilon}{qN_A L^2}} \sqrt{(V_{DS} - V_{sat})} \cong 1 + \lambda V_{DS}$$

- The above neglects V_{sat} with respect to V_{DS} and introduces a new parameter, the *channel length modulation parameter*

$$\lambda = \sqrt{\frac{\epsilon}{qN_A L^2}} \cong \frac{10^7}{L \sqrt{N_A}}$$

SATURATION REGION

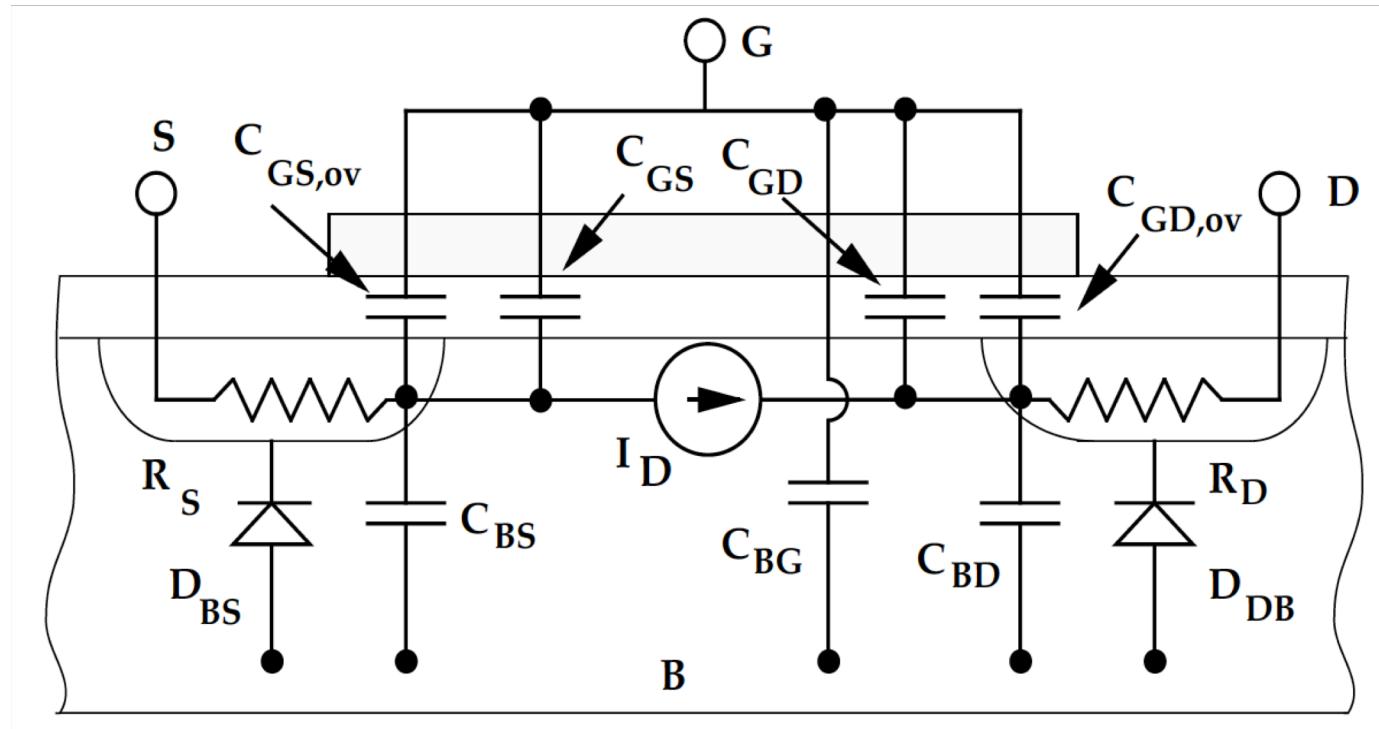
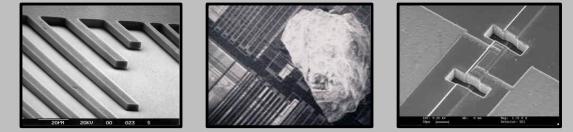


- ❖ Hence, in saturation, the drain current is:

$$I_D = \frac{1}{2} \mu C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{Th})^2 [1 + \lambda V_{DS}]$$

- ❖ Observe that the I-V characteristic derived for the triode region shows a zero slope at the boundary between triode and saturation region. The above equation gives a slope equal to lambda. This discontinuity in the derivatives arises from approximations.
- ❖ The product μC_{ox} (often represented by k_n or k_p) is called the *process transconductance parameter*. Its value depends on technology and on the type of charge carriers in the channel.

LARGE SIGNAL EQUIVALENT CIRCUIT



Non-linear

- ❖ Current source
- ❖ Diodes
- ❖ C_{GS} , C_{BG} , C_{GD} , C_{BS} , C_{BD}

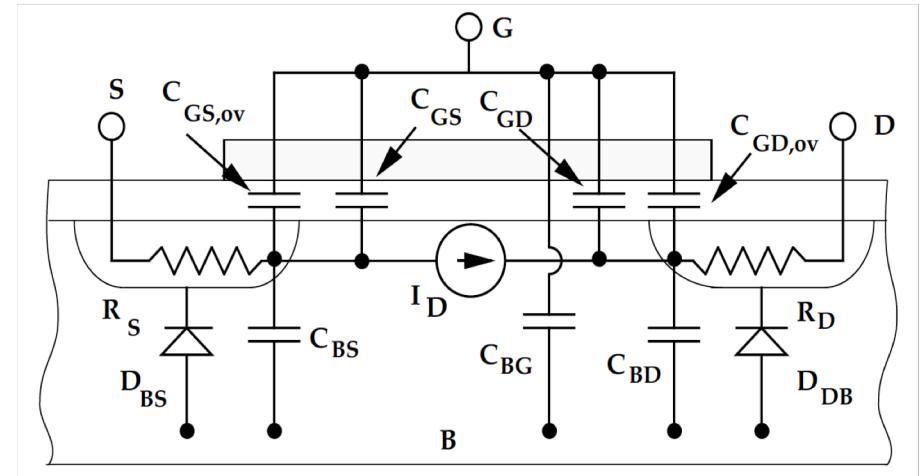
Linear (1st approximation)

- ❖ Resistors
- ❖ $C_{GS,ov}$, $C_{GD,ov}$

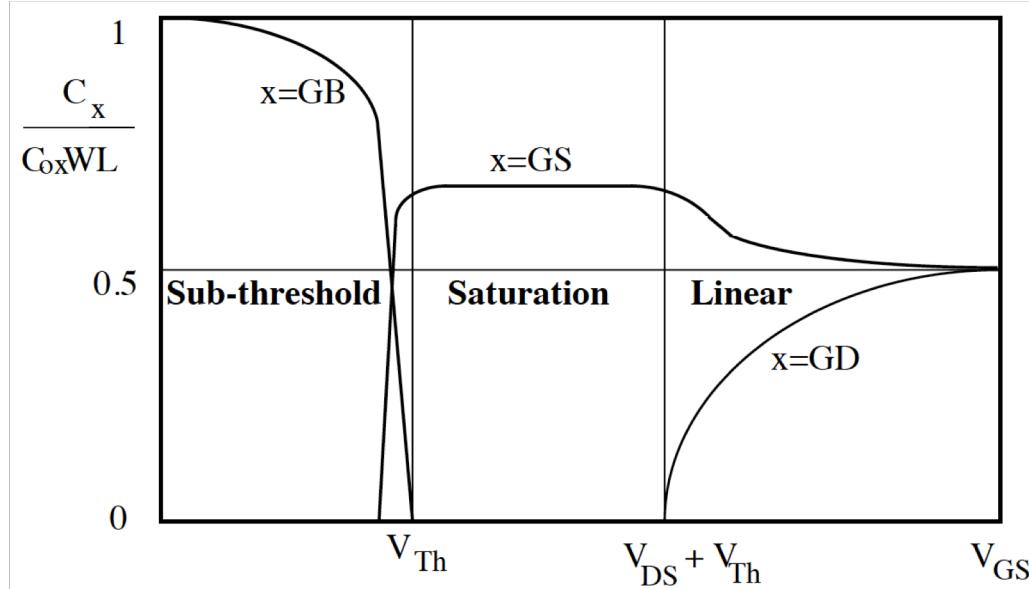
LARGE SIGNAL EQUIVALENT CIRCUIT



- ❖ $R_D \approx R_S \approx 10-50 \Omega$
- ❖ $C_{GS,ov} = C_{GD,ov} = Wx_{ov}C_{ox}$
- ❖ Diodes reversely biased. The reverse current is dominated by the generation-recombination term. The diodes parasitic caps are proportional to the area of the junction.
- ❖ C_{GS} , C_{GD} , C_{BG} account for the non-linear coupling between the gate and the other three terminals
- ❖ Meyer model empirically splits the gate capacitance $C_{ox}WL$ into varying amounts between the gate and the other terminals

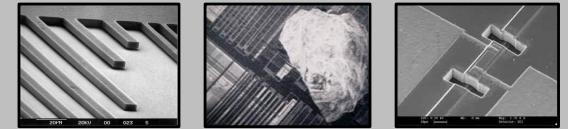


MEYER MODEL

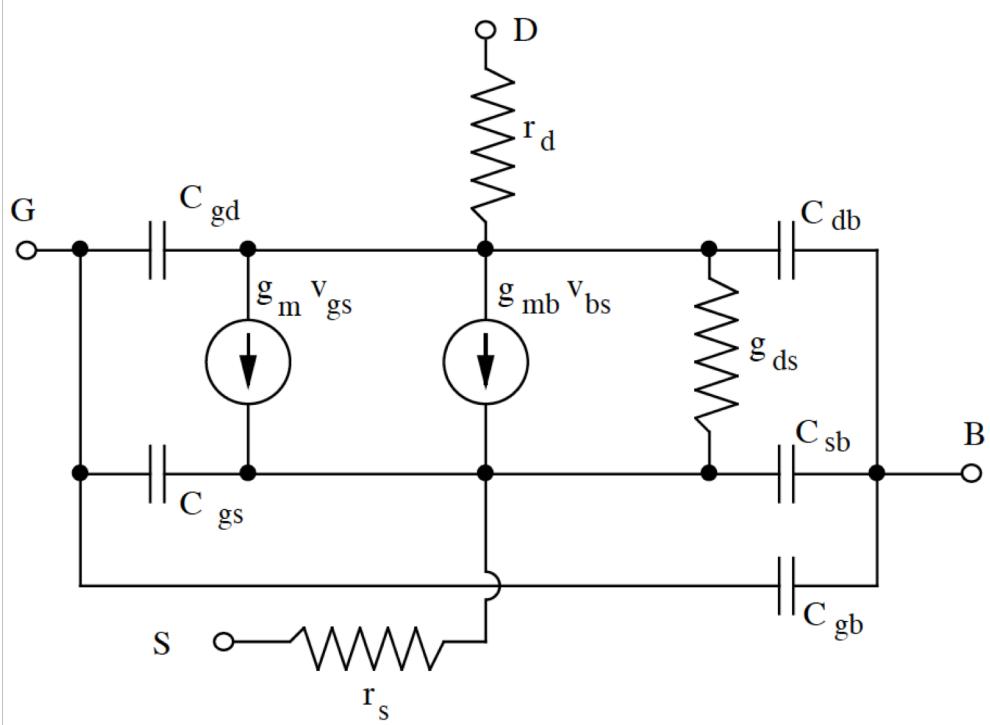


- ❖ In sub-threshold, the channel is not yet formed so that the coupling with source and drain is weak. C_{GB} dominates.
- ❖ In sat and triode the channel shields the substrate and C_{GB} effect vanishes.
- ❖ In triode, the channel is equivalent to a resistance: distributed RC network. Only two caps C_{GS} and C_{GD} are used. For large V_{GS} , they are almost equal.
- ❖ As V_{GS} decreases and reaches the saturation limit, the drain is no longer connected to the channel (C_{GD} goes to zero).
- ❖ In saturation, only C_{GS} is relevant.

SMALL SIGNAL EQUIVALENT CIRCUIT



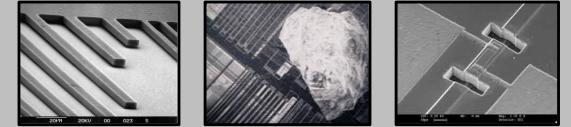
- ❖ The linearization of the large signal model leads to the small signal equivalent circuit.
- ❖ The voltage controlled current source generates three terms proportional to the small voltages v_{gs} , v_{ds} , and v_{bs}



$$i_d(v_{gs}, v_{ds}, v_{bs}) = \frac{\partial I_D}{\partial V_{GS}} v_{gs} + \frac{\partial I_D}{\partial V_{DS}} v_{ds} + \frac{\partial I_D}{\partial V_{BS}} v_{bs}$$

$$i_d = g_m v_{gs} + g_{ds} v_{ds} + g_{mb} v_{bs}$$

SMALL SIGNAL EQUIVALENT CIRCUIT

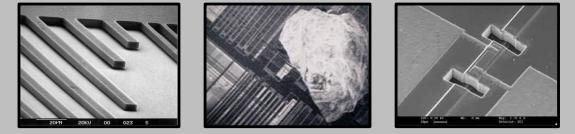


- ❖ g_m : transconductance
- ❖ g_{mb} : substrate transconductance
- ❖ g_{ds} : output conductance
- ❖ The above parameters are calculated from the I-V characteristics in the three regions of operation: weak inversion, linear region, saturation region

Weak inversion

$$g_m = -g_{mb} = \frac{I_D}{n \frac{kT}{q}}$$

$$g_{ds} = \lambda_{wi} I_D$$



Linear region

$$g_m = \mu C_{ox} \left(\frac{W}{L} \right) V_{DS}$$

$$g_{ds} = \mu C_{ox} \left(\frac{W}{L} \right) [V_{GS} - V_{Th} - V_{DS}]$$

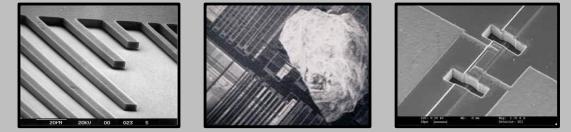
Saturation region

$$g_m = \mu C_{ox} \left(\frac{W}{L} \right) (V_{GS} - V_{Th}) = \frac{2I_D}{(V_{GS} - V_{Th})} = \sqrt{2\mu C_{ox} \left(\frac{W}{L} \right) I_D}$$

$$g_{ds} = \lambda I_D$$

Equations we used for triode and sat do not depend on V_{BS} . So, no expressions for g_{mb} : for that, more sophisticated models (simulators)

NOISE



- ❖ Noise accounts for unwanted and unpredictable voltage or current fluctuations in a network
- ❖ Noise is due to fundamental physical principles, but also to undesired coupling among parts of the same circuit
- ❖ Circuit noise is described by random voltage or current sources applied to given points of the network
- ❖ Each noise source is characterized by a given amplitude and a corresponding power spectrum (white or colored)
- ❖ For uncorrelated noise sources, their effects have to be combined quadratically
- ❖ In MOS transistors the two main noise effects are:
 - ❖ Thermal noise
 - ❖ Flicker noise

THERMAL NOISE

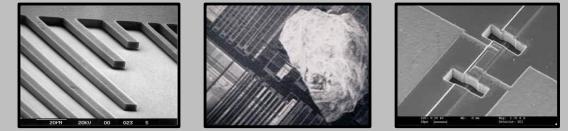


- ❖ It arises from carrier fluctuations in the channel because of a non-zero operating temperature
- ❖ It is representable with a voltage generator in series with the gate of the MOS transistor
- ❖ The spectrum of the voltage noise generator referred to the input is

$$S_{v_{n,th}^2} = \frac{8KT}{3g_m} \Delta f$$

- ❖ The spectrum is white and is inversely proportional to the transistor transconductance

FLICKER NOISE



- ❖ It arises from the mechanism of generation and recombination of carriers activated by localized energy levels in the forbidden gap
- ❖ These energy levels either represent localized impurities or they reflect the discontinuity of the band diagram at the MOS surface
- ❖ They are spread over a wide interval range
- ❖ The associated carriers mean lifetime is widely distributed
- ❖ It is representable with a voltage generator in series with the gate of the MOS transistor
- ❖ The spectrum of the voltage noise generator referred to the input is

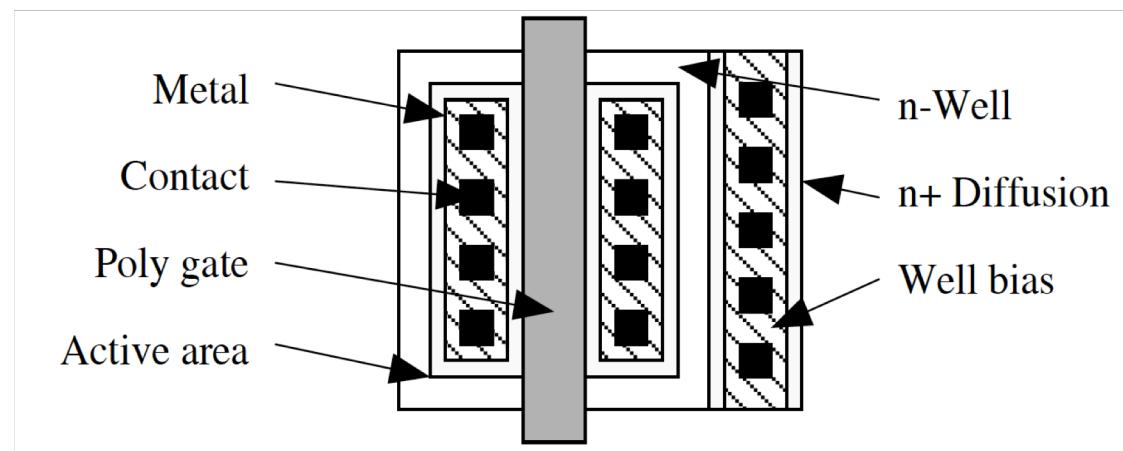
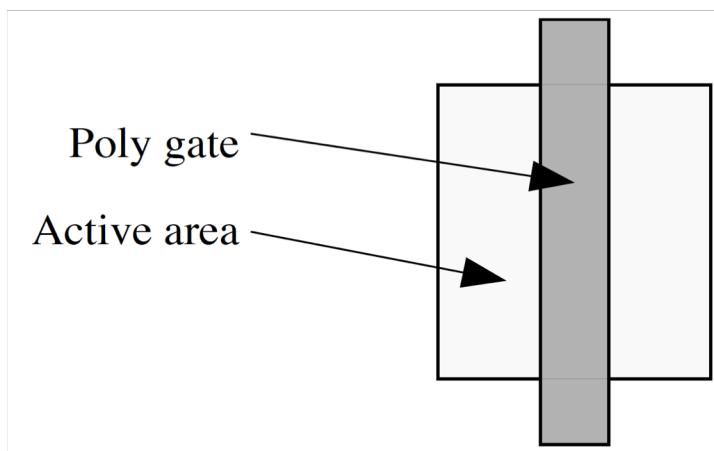
$$S_{V_{n,1/f}^2} = \frac{K_f}{\mu C_{ox} WL} \frac{\Delta f}{f^\alpha}$$

- ❖ Alpha is very close to 1. Colored spectrum

LAYOUT: THE BASICS



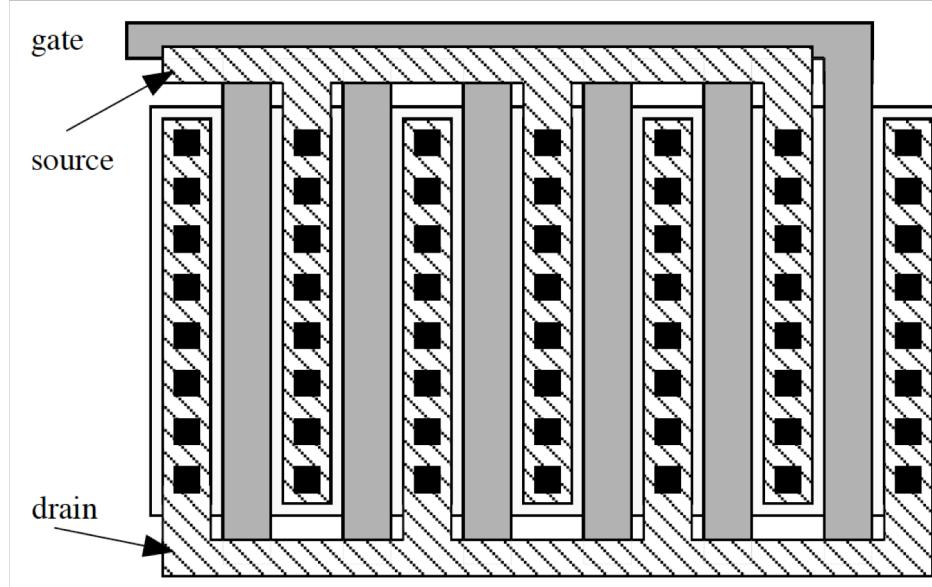
- ❖ A MOS transistor is basically the overlap of two rectangles: active area (not protected, to originate the source and the drain) and the polysilicon gate
- ❖ Keep the parasitic resistance at the source and the drain as low as possible
- ❖ Parasitic capacitances must be minimized
- ❖ Matching between paired elements is very important



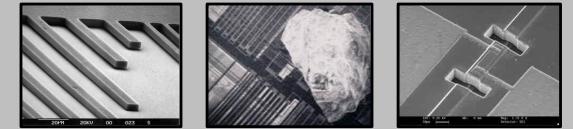
LAYOUT: THE BASICS



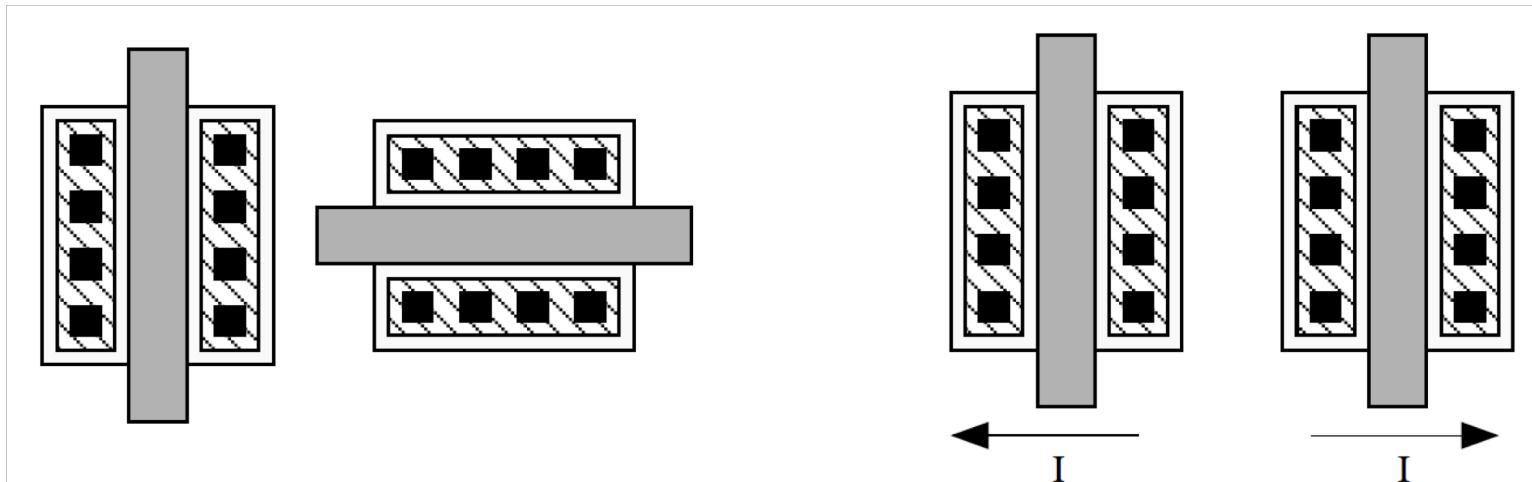
- ❖ Use multiple contacts. Many contacts placed close to each other make the surface of the metal connection smoother, preventing micro-cracks in the metal. Multiple contacts decreases the contact resistance.
- ❖ Splitting the transistor in a number of equal parts connected in parallel reduces the area of the transistor and its parasitic capacitances



LAYOUT: THE BASICS



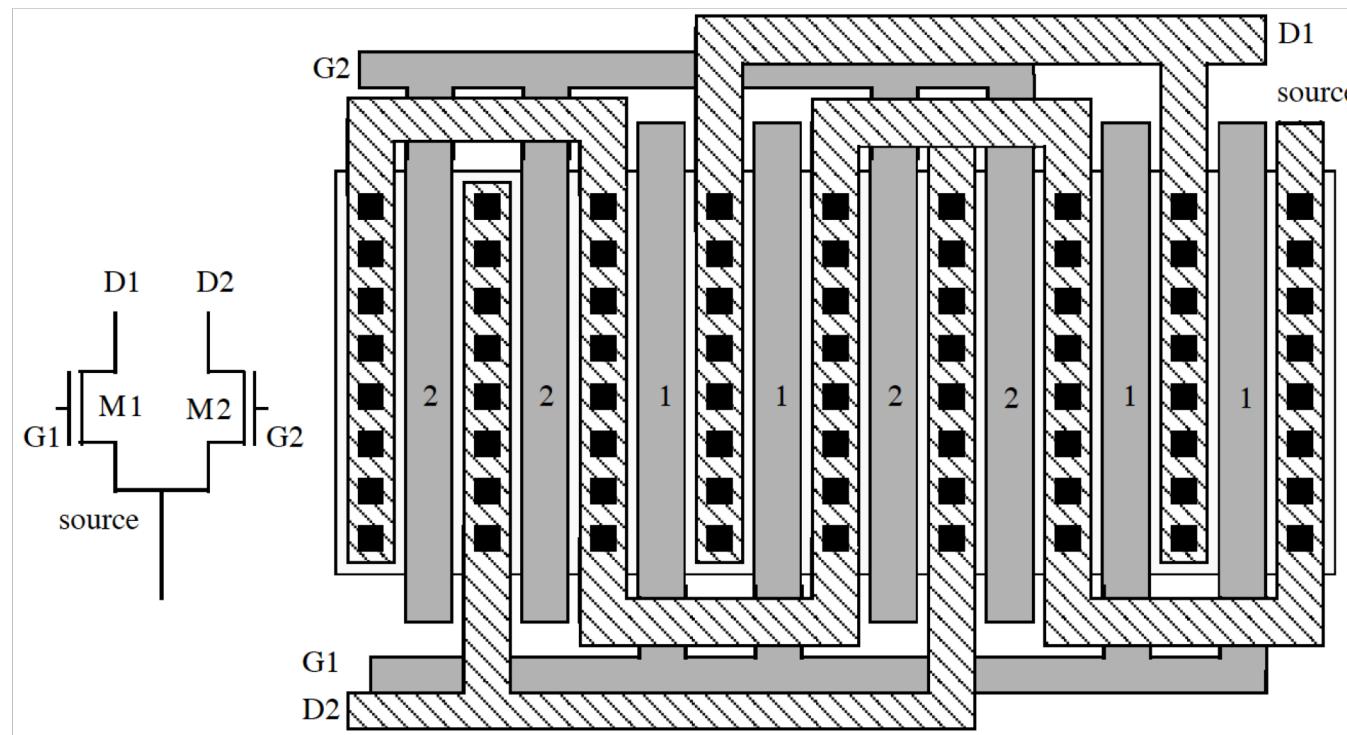
- ❖ Matching is very important when we design current mirrors and differential pairs. Bad matching produces high offset.
- ❖ Transistors with different orientation match badly
- ❖ Mismatch may occur if current flows in opposite directions
- ❖ Physical and technological parameters may change in points of the chip that are relatively far away



LAYOUT: THE BASICS



- ❖ Best method to achieve good matching is here shown
- ❖ Each transistor split into four equal parts (fingers) with a proper interleaving. For each pair of fingers of the same transistor, currents flow in the opposite directions



LAYOUT: THE BASICS



- ❖ Use poly connections only for the signal and never for the current because of the offset (high resistance)
- ❖ Minimize line lengths, especially for lines connecting high impedance nodes (if they are not the dominant node)
- ❖ Use matched structure. If necessary common centroid arrangement
- ❖ Respect symmetries (even respect power devices)
- ❖ Separate (or shield) the input from the output line (to avoid feedback) and separate (or shield) analog from digital signals
- ❖ Shielding of high impedance nodes avoids noise injection from the power supply and the substrate
- ❖ Use regular shapes