

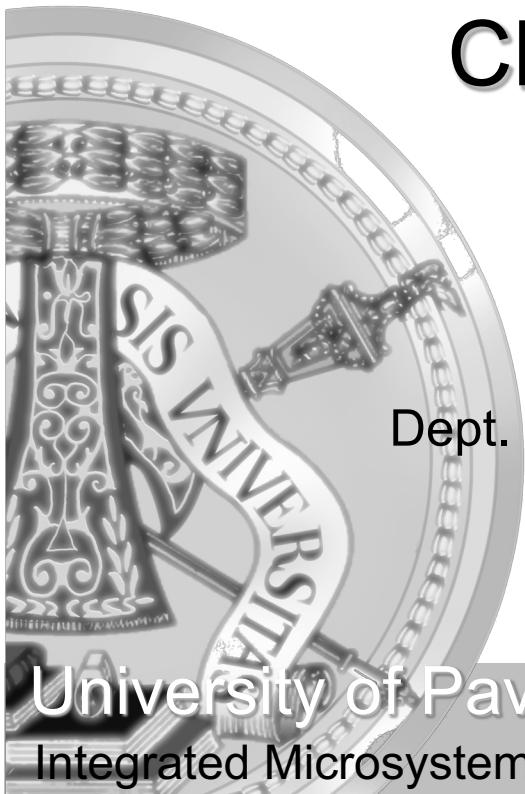


CMOS Operational Amplifiers

Analog Integrated Circuits

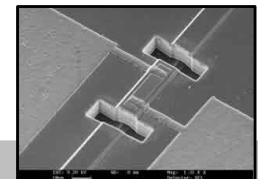
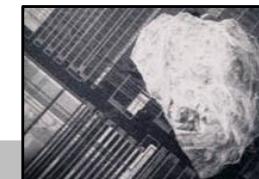
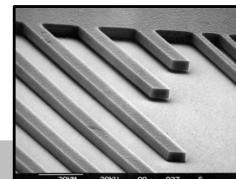
Edoardo Bonizzoni

Dept. of Electrical, Computer, and Biomedical Engineering

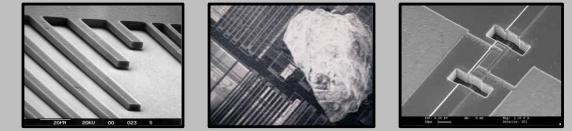


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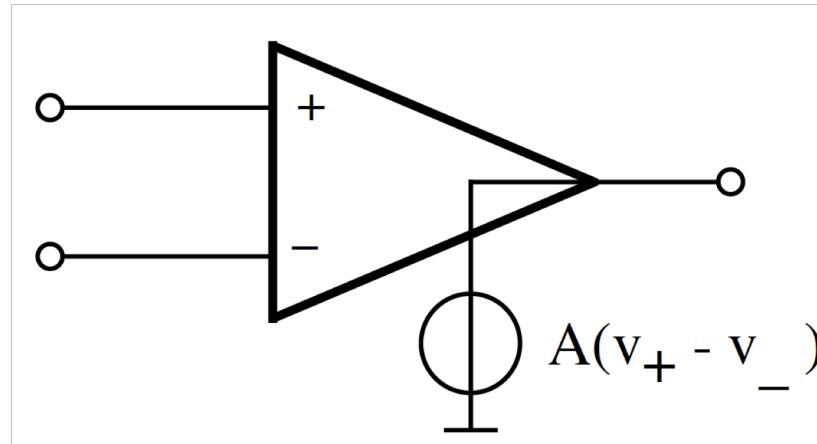
Integrated Microsystems Laboratory



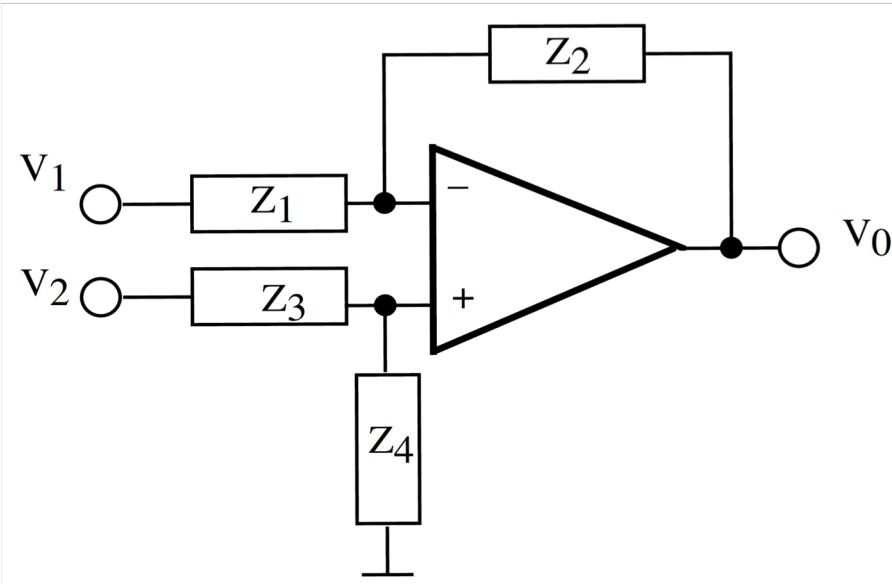
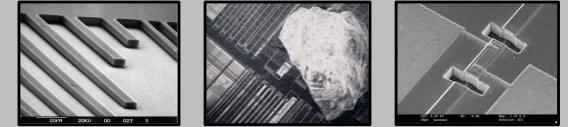
BASIC IDEA



- ❖ It generates at the output an amplified replica of the voltage across the input terminals.
- ❖ Ideally, the voltage gain is infinite, the input impedance infinite as well and the output impedance is zero.
- ❖ An ideal op-amp behaves like a voltage controlled voltage source (VCVS).
- ❖ The op-amp is never used as a stand-alone block, but always in feedback configuration.



FEEDBACK CONFIGURATION



$$V_0 = V_2 \frac{Z_4}{Z_3 + Z_4} \cdot \frac{Z_1 + Z_2}{Z_1} - V_1 \frac{Z_2}{Z_1}$$

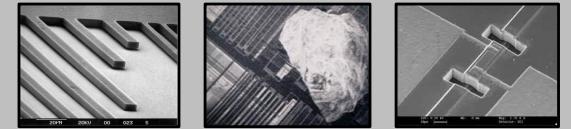
- ❖ If the op-amp gain, A , is not infinite, an error of the order of $1/A$ results.
- ❖ This error must be smaller or comparable with the other sources of errors, i.e. impedance matching. A gain on the order of 60 dB is normally enough for most of the applications.

INPUT AND OUTPUT IMPEDANCE

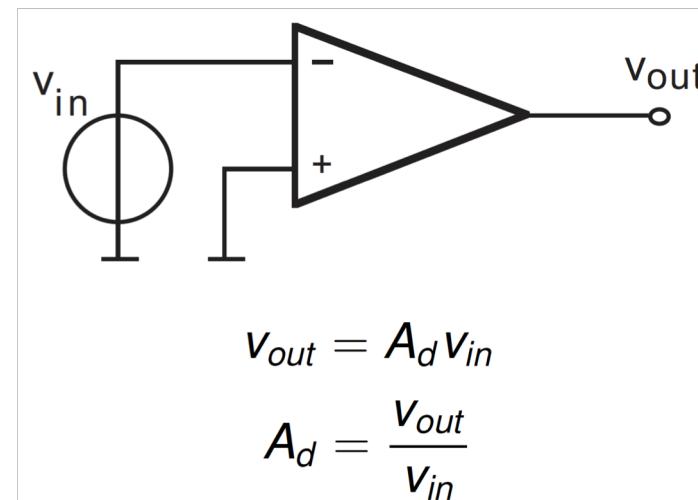
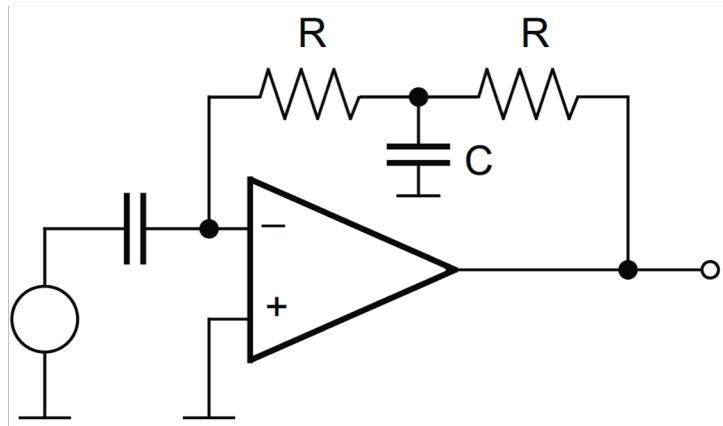


- ❖ The input impedance of a CMOS op-amp is normally not a problem since the input stage is realized by MOS transistors (the input terminals are gates). Large input impedance over wide frequency range is not an issue.
- ❖ Achieving low output impedance might be problematic.
- ❖ However, generally, integrated systems do not require strictly op-amp with low output impedance.
- ❖ In case, as often happens, the feedback element is a capacitor and the output load and the input are capacitors as well, possibly connected by switches, the output impedance is not a problem at all.

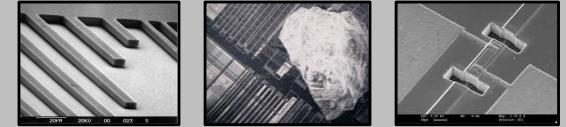
PERFORMANCE CHARACTERISTICS



- ❖ Actual operational amplifiers deviate from ideal behavior. The differences are described by the performance characteristics.
- ❖ Differential gain (A_d):
 - ❖ Open loop voltage gain as a function of the frequency measured with a small differential input signal. Typically, A_d ranges from 70 to 90 dB
 - ❖ For simulations, suitable large capacitor connects the small signal input to the amplifier. The T network in the feedback acts as unity gain configuration at low frequency and as an open circuit at high frequency. R and C are normally chosen very large (the T network loads the op-amp: use R larger than the output resistance of the op-amp itself)

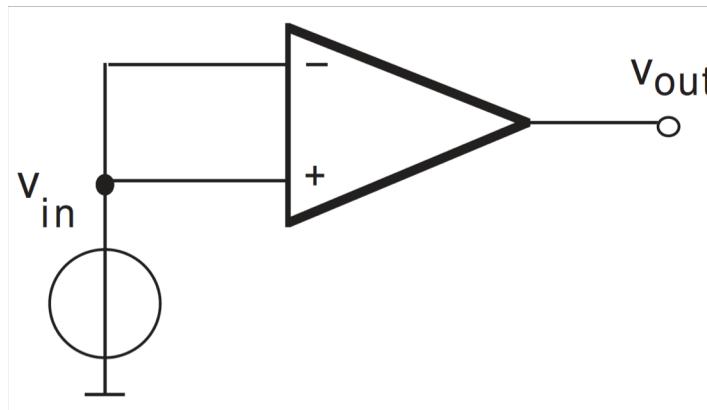


PERFORMANCE CHARACTERISTICS



❖ Common mode gain (A_{cm}):

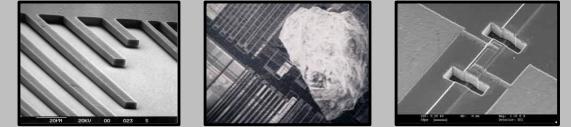
- ❖ Open loop voltage gain as a function of the frequency measured with a small signal applied to both input terminals.
- ❖ Ideally, an op-amp should amplify only the differential signals: a low common mode gain over a wide frequency range is desirable. A_{cm} typically ranges from 20 to 40 dB



❖ Common mode rejection ratio (CMRR):

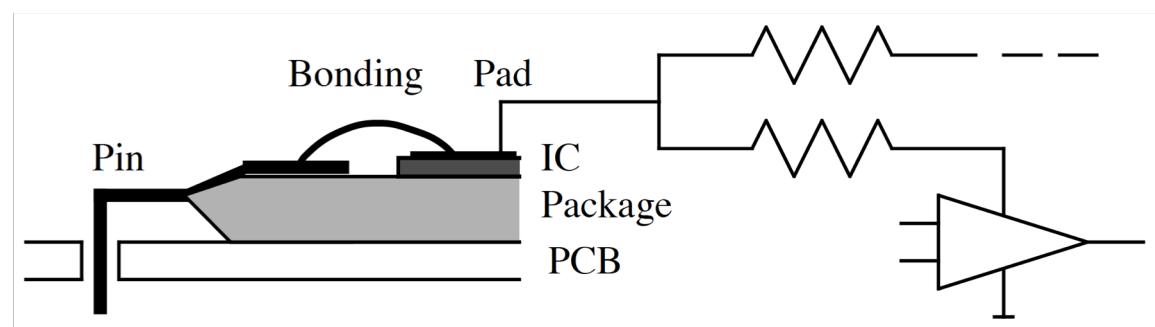
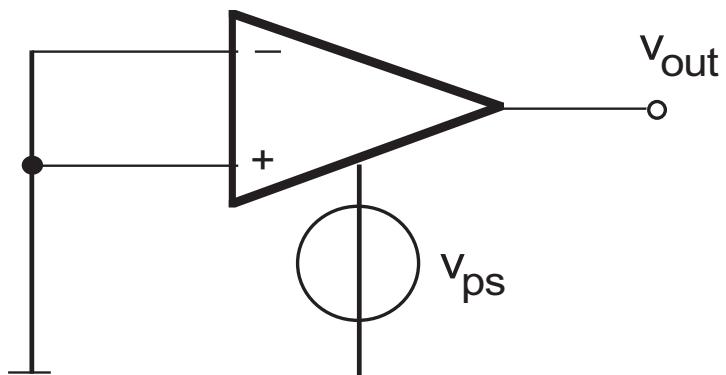
- ❖ It is the ratio between the differential and the common mode gain
- ❖ A high CMRR is an important feature for any op-amp
- ❖ Typically, CMRR ranges from 40 to 80 dB

PERFORMANCE CHARACTERISTICS

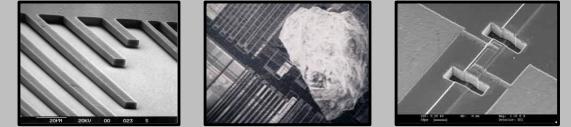


❖ Power supply rejection ratio (PSRR):

- ❖ If a small signal (V_{ps}) is applied in series with the positive (+) or negative (-) power supply, it is transferred to the output with a given gain A_{ps+} or A_{ps-}
- ❖ The ratios between the differential gain and the power supply gains define the two PSRRs ($PSRR_+$, $PSRR_-$)
- ❖ Typically, $PSRR = 90 \text{ dB (DC)}$, $PSRR = 60 \text{ dB (1 kHz)}$, $PSRR = 30 \text{ dB (100 kHz)}$
- ❖ It gives the ability of the op-amp to reject spur signals coming from the power supply

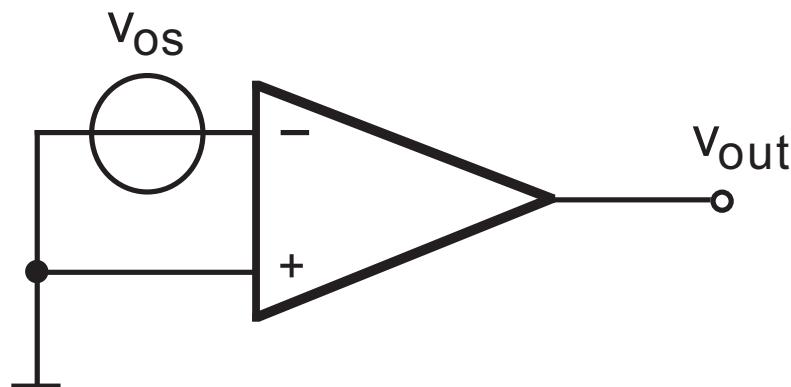


PERFORMANCE CHARACTERISTICS

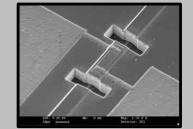
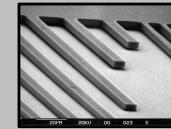


❖ Offset voltage (V_{os}):

- ❖ In a real operational amplifier, if the two input terminals are at the same voltage ($V_{in} = 0 \text{ V}$), V_{out} is not zero
- ❖ The input offset voltage, V_{os} , is the value of V_{in} which ensures $V_{out} = 0 \text{ V}$
- ❖ Typically, V_{os} ranges from 5 to 15 mV
- ❖ These values for a number of applications are not acceptable: sophisticated techniques (autozero, chopper) resolve the problem bringing to μV level the offset voltage



PERFORMANCE CHARACTERISTICS



❖ Input common mode range:

- ❖ It is the voltage range that can be used at the input without producing significant degradations in the op-amp performance
- ❖ A large input common mode range is important when the op-amp is used in the unity gain configuration. Since the input must follow the output, rail-to-rail operation at the input terminals is often required

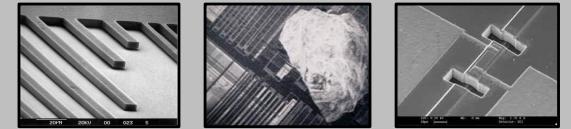
❖ Output voltage swing:

- ❖ Maximum swing at the output node that leads to a given amount of harmonic distortions
- ❖ Typically, the output swing ranges from 60% to 80% of $(V_{DD} - V_{SS})$

❖ Power consumption:

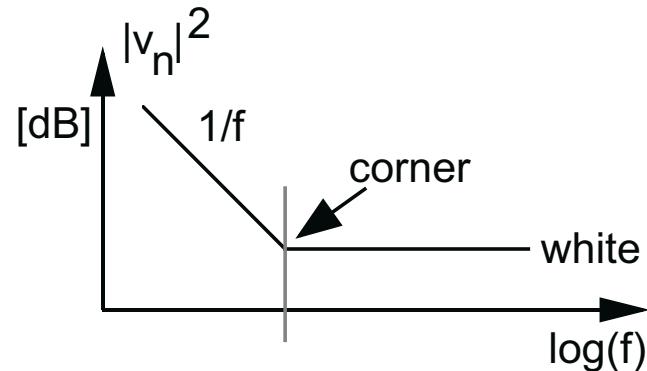
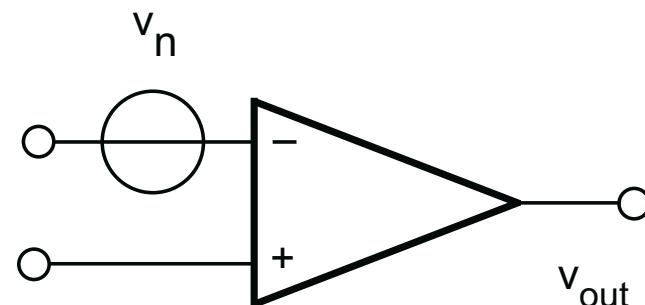
- ❖ Power consumed by the operational amplifier. Power consumption is often related to the amplifier bandwidth. Low-power operation is a very important quality factor for battery-operated systems: key design task is to have minimum power consumption for a given required speed

PERFORMANCE CHARACTERISTICS

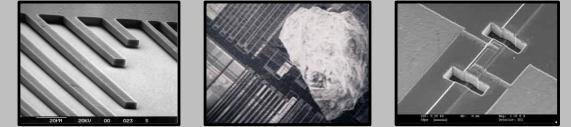


❖ Equivalent input noise:

- ❖ The noise performance can be described in terms of an equivalent voltage source, V_n , at the input of the operational amplifier. It accounts for the effect of all the MOS transistors of the network. As the noise spectrum of a single MOS transistor, it has a white and a $1/f$ term
- ❖ Typically, V_n ranges from 40 to 50 nV/ $\sqrt{\text{Hz}}$ at 1 kHz
- ❖ When this value of V_n is integrated over a wide band (1 MHz), the noise ranges from 10 to 50 μV_{RMS}

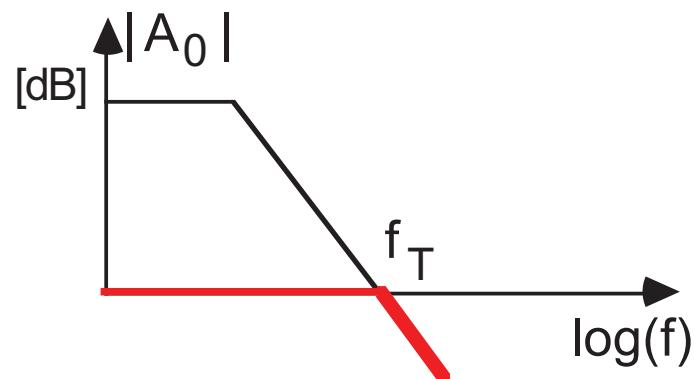
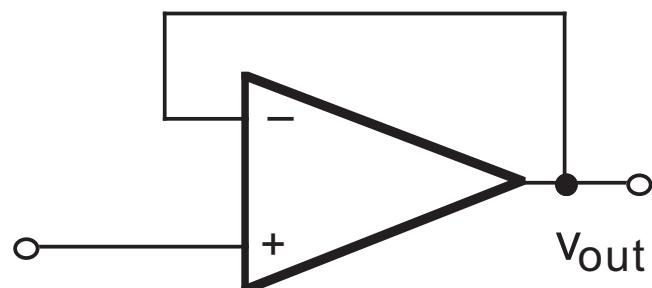


PERFORMANCE CHARACTERISTICS

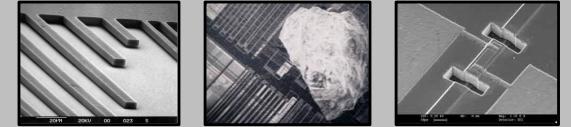


❖ Unity gain bandwidth (f_T):

- ❖ Frequency at which the open loop differential gain is one (0 dB)
- ❖ For stability requirements, one pole (at frequency f_1) has to be dominant. With a constant roll-off of 20 dB/decade, the unity gain bandwidth equals the product of the gain and bandwidth ($f_1 A_0$)
- ❖ f_T is also named gain-bandwidth product (GBW)
- ❖ Poles exceeding f_T are referred to as non-dominant poles
- ❖ f_T can be measured open loop or in unity gain configuration
- ❖ Typically, f_T ranges from 200 to 800 MHz

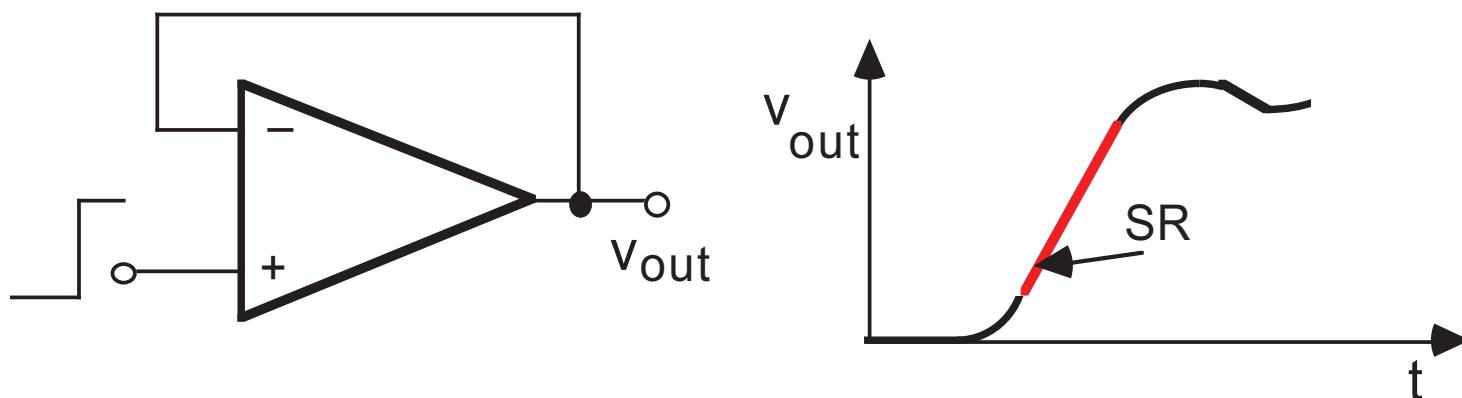


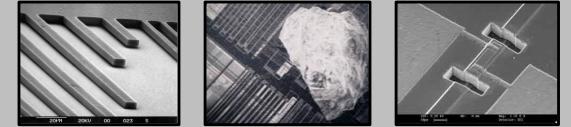
PERFORMANCE CHARACTERISTICS



❖ Slew rate (SR):

- ❖ It is the maximum slope of the output voltage for a step signal applied at the input
- ❖ Usually it is measured with the operational amplifier in unity gain closed loop conditions
- ❖ The positive slew rate can be different from the negative slew rate
- ❖ Typically, the SR ranges from 10 to 50 V/ μ s
- ❖ Micro-power circuits (in which the quiescent current is much lower) can show much lower figures



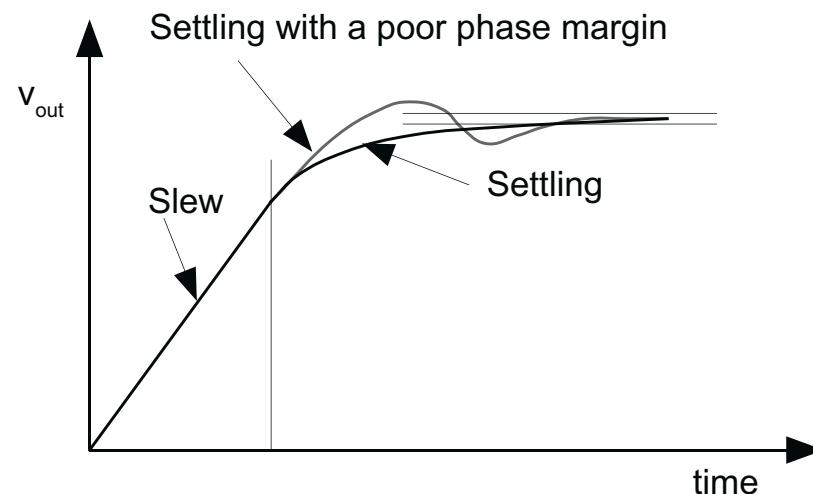


❖ Phase margin

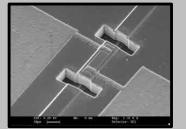
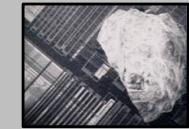
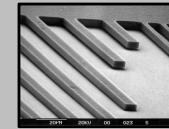
- ❖ It is the phase shift of the small signal differential gain measured at the unity gain frequency. A phase margin lower than 60° causes ringing in the output response

❖ Settling time:

- ❖ It is the time that the output voltage requires, under given operating conditions, to achieve the desired value with a given accuracy
- ❖ The settling time depends on the bandwidth, the slew rate, and the phase margin of the operational amplifier



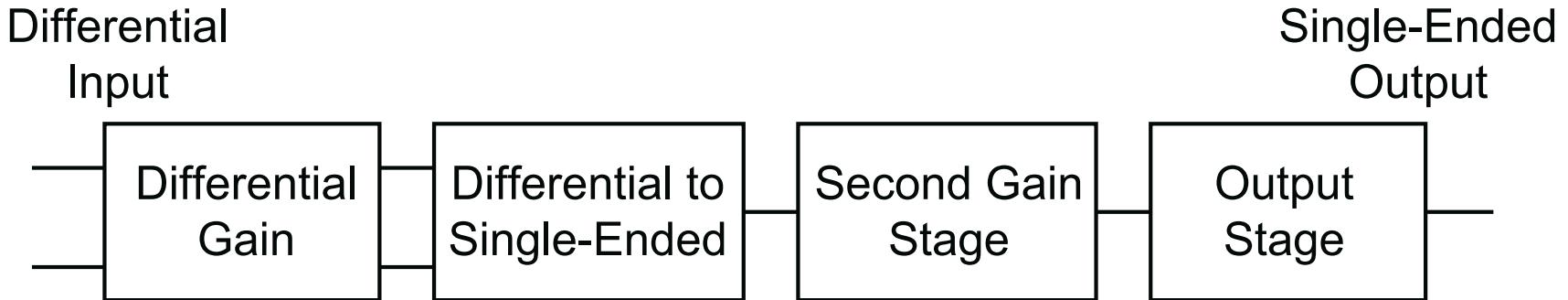
PERFORMANCE CHARACTERISTICS



- ❖ Typical performance of a 0.25- μm CMOS op-amp

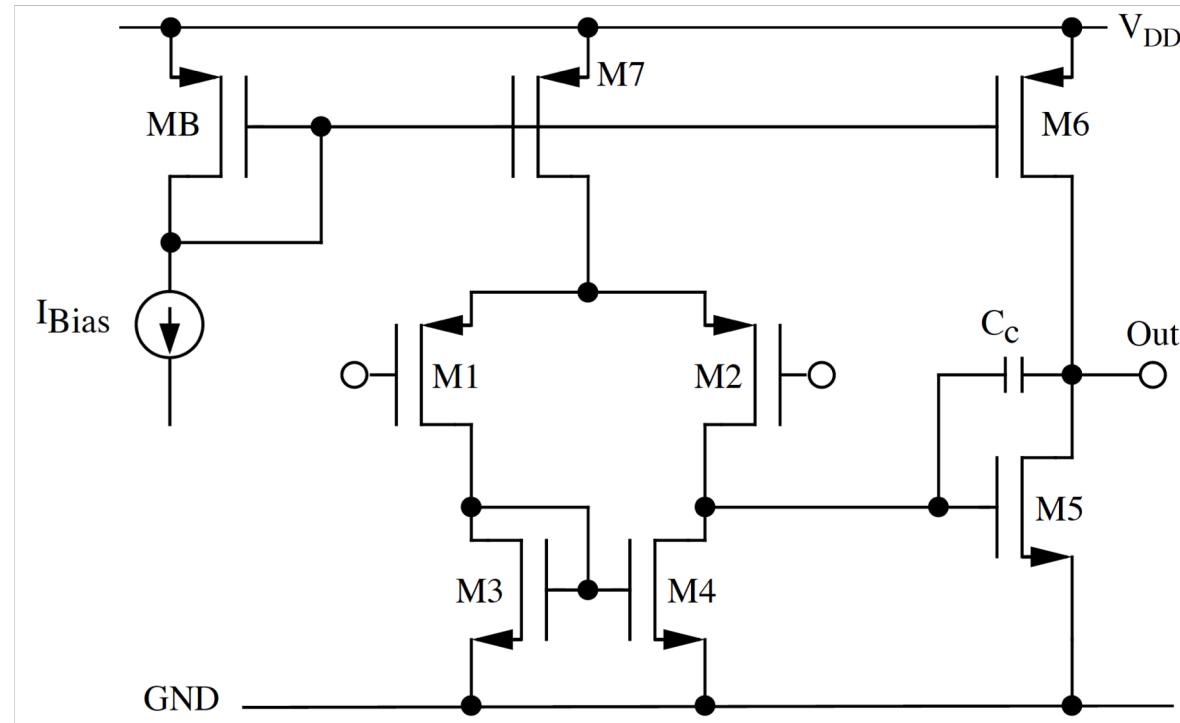
<i>Parameter</i>	<i>Value</i>	<i>Unit</i>
DC gain	80	dB
CMRR	40	dB
Offset	4 ÷ 6	mV
Gain-bandwidth product	100	MHz
Slew-rate	5	V/ μs
Settling time (1 V, $C_L = 4 \text{ pF}$)	300	ns
PSRR @ DC	90	dB
PSRR @ 1 kHz	60	dB
PSRR @ 100 kHz	30	dB
Input referred noise @ 1kHz	100	nV/ $\sqrt{\text{Hz}}$
Supply voltage	3.3	V
Input common-mode range	1.5	V
Output voltage swing	2.2	V _{pp}
Power consumption	1	mW

BASIC ARCHITECTURE



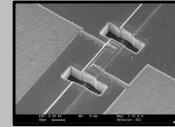
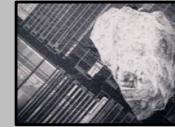
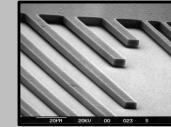
- ❖ High gain can be obtained by cascading (multi-stage operational amplifiers) or cascoding (single-stage operational amplifiers)
- ❖ Stability is required in unity gain closed loop conditions, when driving the maximum load, with adequate phase margin ($>60^\circ$)
- ❖ Use minimum number of gain stages to maximize the bandwidth
- ❖ Output stage is used to decrease the output impedance and is needed when driving resistive loads. When not needed the scheme is referred to as OTA

TWO STAGE AMPLIFIER



- ❖ Differential amplifier with differential to single ended transformation (M_3 - M_4) + inverter with active load
- ❖ Both stages controlled by the same reference current
- ❖ C_c (or more complicated network) for compensation

DIFFERENTIAL GAIN



- ❖ The gain is obtained by multiplying the gain of the two stages

$$\begin{aligned} A_v &= A_1 A_2 = \frac{g_{m1} g_{m5}}{(g_{ds2} + g_{ds4})(g_{ds5} + g_{ds6})} \\ &= \alpha \cdot \frac{\sqrt{\left(\frac{W}{L}\right)_1} \sqrt{\left(\frac{W}{L}\right)_5}}{\sqrt{I_7} \sqrt{I_6}} = \frac{\alpha}{I_{Bias}} \cdot \frac{\sqrt{\left(\frac{W}{L}\right)_1} \sqrt{\left(\frac{W}{L}\right)_5} \left(\frac{W}{L}\right)_B}{\sqrt{\left(\frac{W}{L}\right)_7} \sqrt{\left(\frac{W}{L}\right)_6}} \end{aligned}$$

- ❖ α is technology dependent (μ , C_{ox} , λ)
- ❖ All transistors are assumed to be in the saturation region
- ❖ At low frequency, the differential gain is inversely proportional to the bias current, I_{Bias}

COMMON MODE DC GAIN

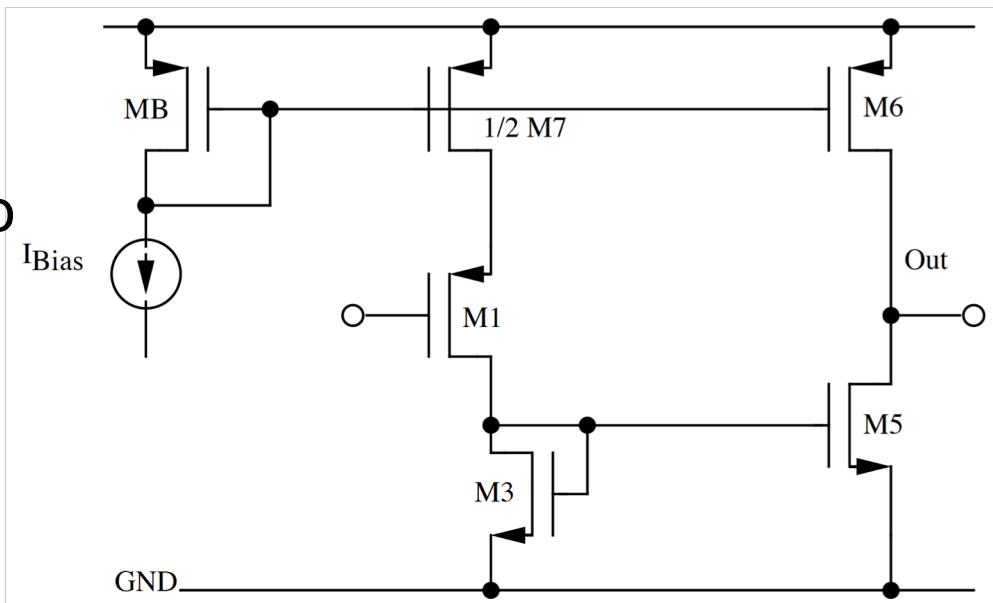


- ❖ Being the same signal applied to both input, the circuit becomes symmetrical and can be studied by considering only half circuit for the first stage
- ❖ The drain of $1/2 M_7$ follows the input. The signal current is $V_{in}/(2r_{ds7})$. It flows then into a diode connected transistor
- ❖ Common mode gain of the first stage is:

$$A_{CM,1} = -\frac{I}{2g_{m3}r_{ds7}}$$

- ❖ The total common mode gain is:

$$A_{CM} = \frac{g_{m5}}{2g_{m3}r_{ds7}(g_{ds5} + g_{ds6})}$$



$$CMRR = \frac{A_d}{A_{CM}} = \frac{2g_{m3}r_{ds7}g_{m1}}{(g_{ds2} + g_{ds4})}$$

OFFSET

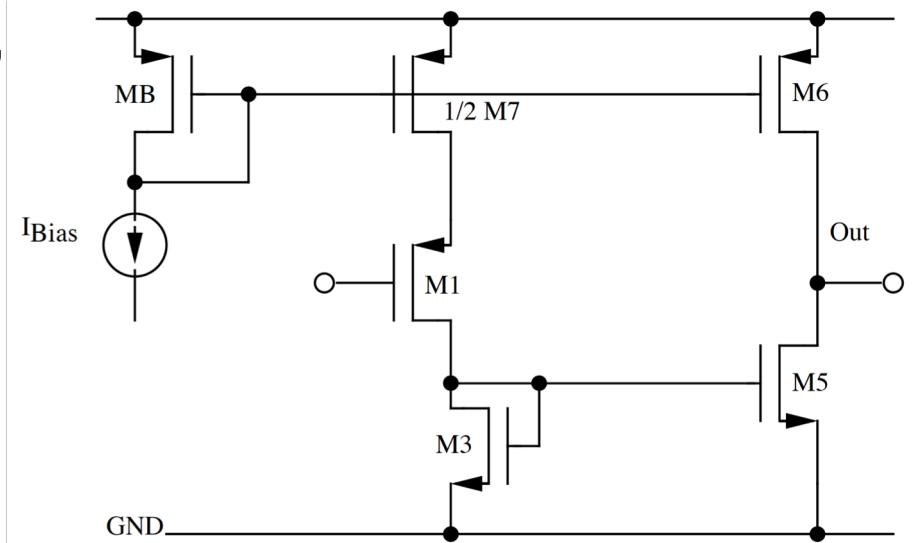


- ❖ The analog ground (V_{AG}) is commonly $V_{DD}/2$. For an ideal circuit, it is expected that a zero input signal (input terminals shorted) brings the output to V_{AG}
- ❖ Improper design or technological mismatch deviate the output from the expected value
- ❖ To bring the output to V_{AG} , it is necessary to apply a proper input signal that counterbalances the mismatch, the offset voltage
- ❖ Two additive contributions:
 - ❖ Systematic offset – It depends on the circuit design and can be compensated for by a proper and careful cell design
 - ❖ Random offset – It comes from random fluctuations of physical and technological parameters. It can be limited with a careful layout that minimizes the mismatch between critical components

SYSTEMATIC OFFSET



- ❖ Let's apply a zero differential input and let's suppose all transistors are in the saturation region
- ❖ Current in M_3 is the current in $1/2M_7$, which is a replica in first approximation of I_{Bias}
- ❖ Output stage made by two current generator: current of M_6 is sunk by M_5 . Since there is an high output impedance, the output reaches V_{AG} only if the two currents are equal



$$I_{Bias} \frac{(W/L)_6}{(W/L)_B} = \frac{I_{Bias}}{2} \cdot \frac{(W/L)_7}{(W/L)_B} \cdot \frac{(W/L)_5}{(W/L)_3}$$



$$(W/L)_3 \cdot (W/L)_6 = \frac{I}{2} \cdot (W/L)_7 \cdot (W/L)_5$$

SYSTEMATIC OFFSET

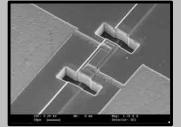
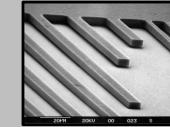


- ❖ Remember that the achieved condition does not consider mismatch in current mirrors. It means currents in the two transistors of the output branch will be slightly mismatched thus causing a residual offset
- ❖ Using the condition for zero systematic offset, the differential gain becomes:

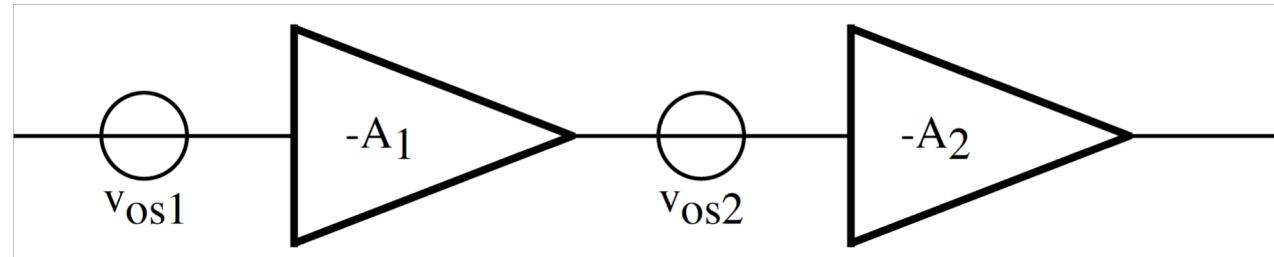
$$A_v = \frac{\alpha}{I_{Bias}} \cdot \frac{2\sqrt{(W/L)_1}\sqrt{(W/L)_3}}{(W/L)_7} (W/L)_B$$

- ❖ Note that if the designer takes care of the systematic offset, the DC gain can be no longer adjusted by operating over the second stage of the op-amp

RANDOM OFFSET



- ❖ The random offset is due to geometrical and process mismatches

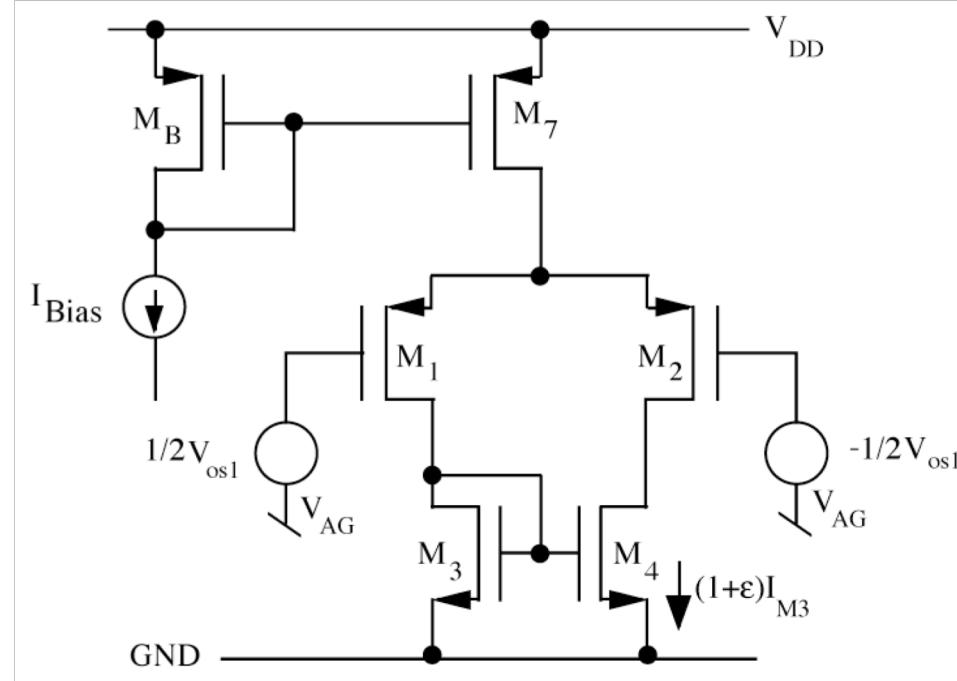


- ❖ When the offset of the second stage is referred at the input terminal, it has to be divided by the gain of the first stage. Since the two offsets are uncorrelated, it holds:

$$V_{os} = \sqrt{V_{os1}^2 + (V_{os2}/A_1)^2}$$

- ❖ Assuming that the two offset contributions have similar value, since A_1 is pretty large, the input stage practically determines the random offset

RANDOM OFFSET



- ❖ M_1-M_2 and M_3-M_4 are nominally equal. Let's assume that mismatch errors of M_1-M_2 are transferred to M_3-M_4 : ratio of the mirror is, hence, no more 1, but $1+\varepsilon$
- ❖ To make the current in M_4 equal to the one of M_2 it is necessary to unbalance the differential input (offset voltage)

RANDOM OFFSET



- ❖ Assuming that the offset is small, that the total current in the input pair is I_{Bias} , and being $g_{m1}=g_{m2}$:

$$\left(\frac{I_{Bias}}{2} - g_{m1,2} \frac{V_{os1}}{2} \right) (1 + \varepsilon) = \left(\frac{I_{Bias}}{2} + g_{m1,2} \frac{V_{os1}}{2} \right) \quad \rightarrow \quad V_{os1} \cong \frac{I_{1,2}}{g_{m1,2}} \varepsilon$$

$$\frac{I_{1,2}}{g_{m1,2}} = \frac{V_{GS} - V_{th}}{2} = 200 \div 300 \text{ mV in saturation}$$

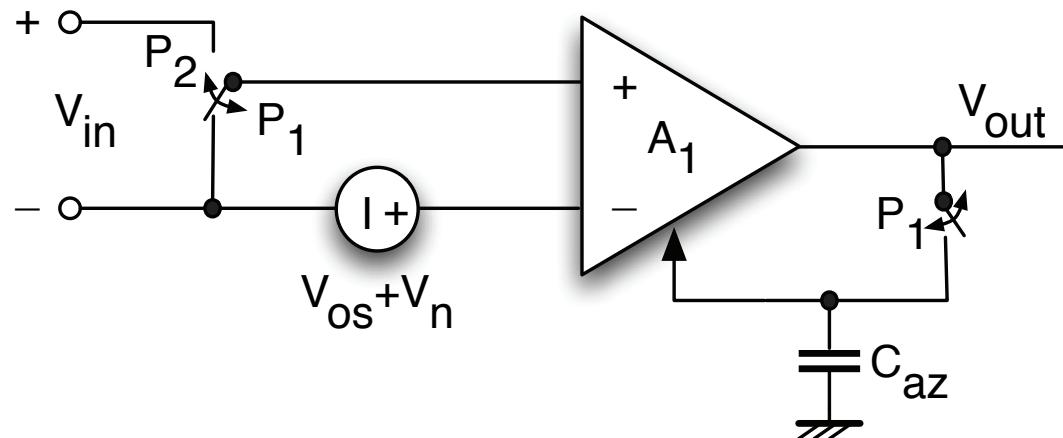
$$\frac{I_{1,2}}{g_{m1,2}} = nV_T = n \frac{kT}{q} \text{ in sub-threshold}$$

- ❖ Random offset is lower for input stages operating in sub-threshold
- ❖ ε is proportional to $1/\sqrt{WL}$: for low offset, large transistors are required

ADVANCED OFFSET CANCELLATION

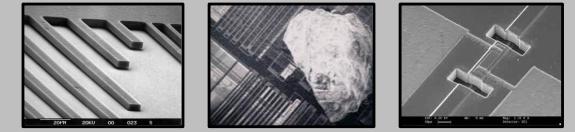


- ❖ Advanced technique to cancel out the offset (and 1/f noise): auto-zero

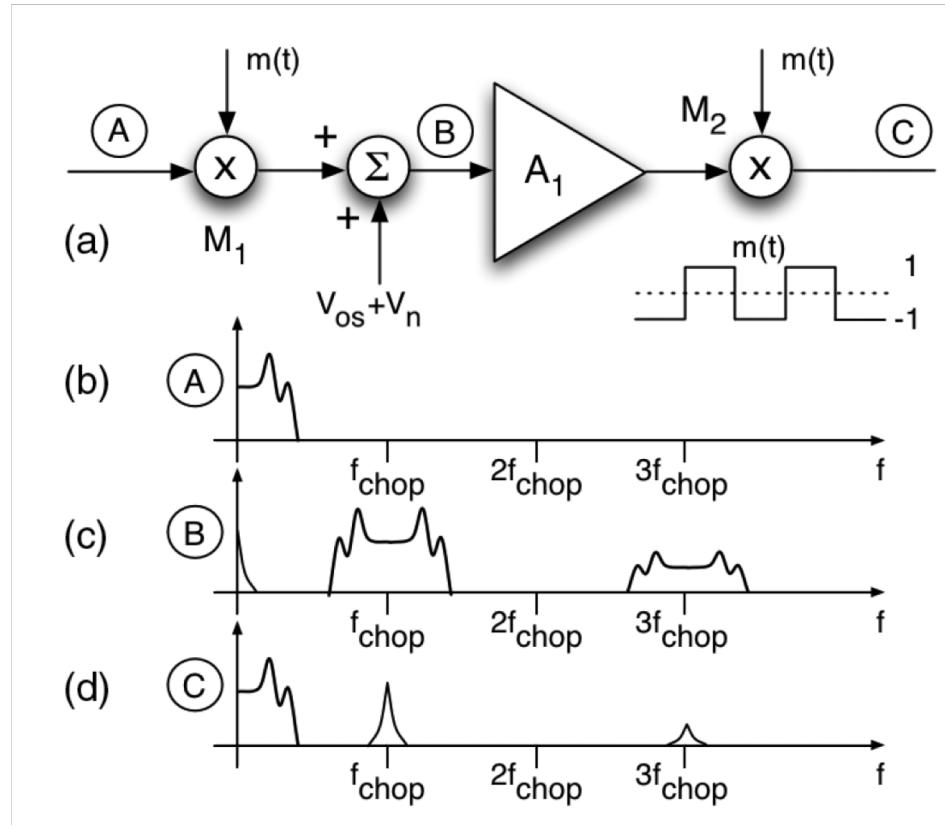


- ❖ Phase P1: offset and noise sampling phase: storing on C_{az} and offset nulling with proper control (current or voltage)
- ❖ Phase P2: offset free amplification phase
- ❖ 1/f noise high-pass filtered
- ❖ Limits: amplifier available during only one phase, large capacitors needed (low power operation is difficult)

ADVANCED OFFSET CANCELLATION

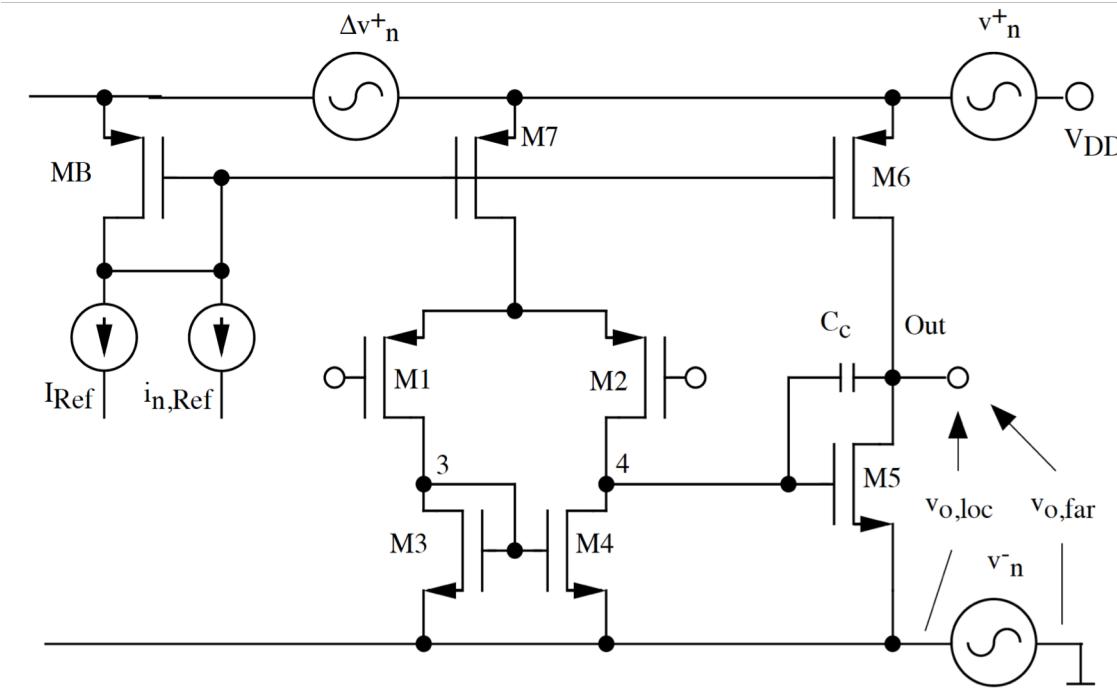
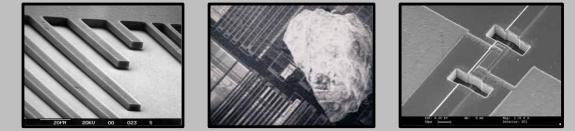


- ❖ Advanced technique to cancel out the offset (and 1/f noise): chopping stabilization



- ❖ Op-amp output affected by ripple. Depending on the applications, a remedy also for that is required

POWER SUPPLY REJECTION

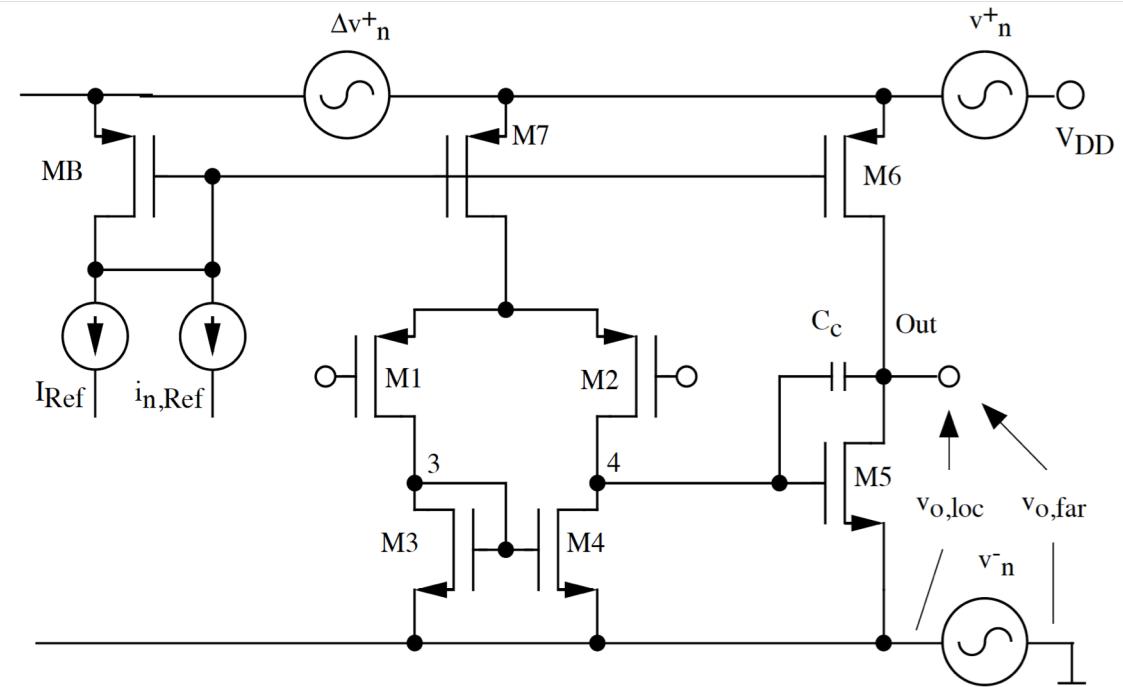


- ❖ Sources of transistors M_7 - M_6 and M_3 - M_4 - M_5 are physically close each others. By contrast, M_B can be located far from the amplifier: Δv^+_n and $i_{n,Ref}$ account for this
- ❖ Even the effect of spurs on the output node can be analyzed in two cases: local output or when the output signal is used far away from the op-amp

POWER SUPPLY REJECTION



Effect of Δv^+_n and $i_{n,Ref}$ at DC



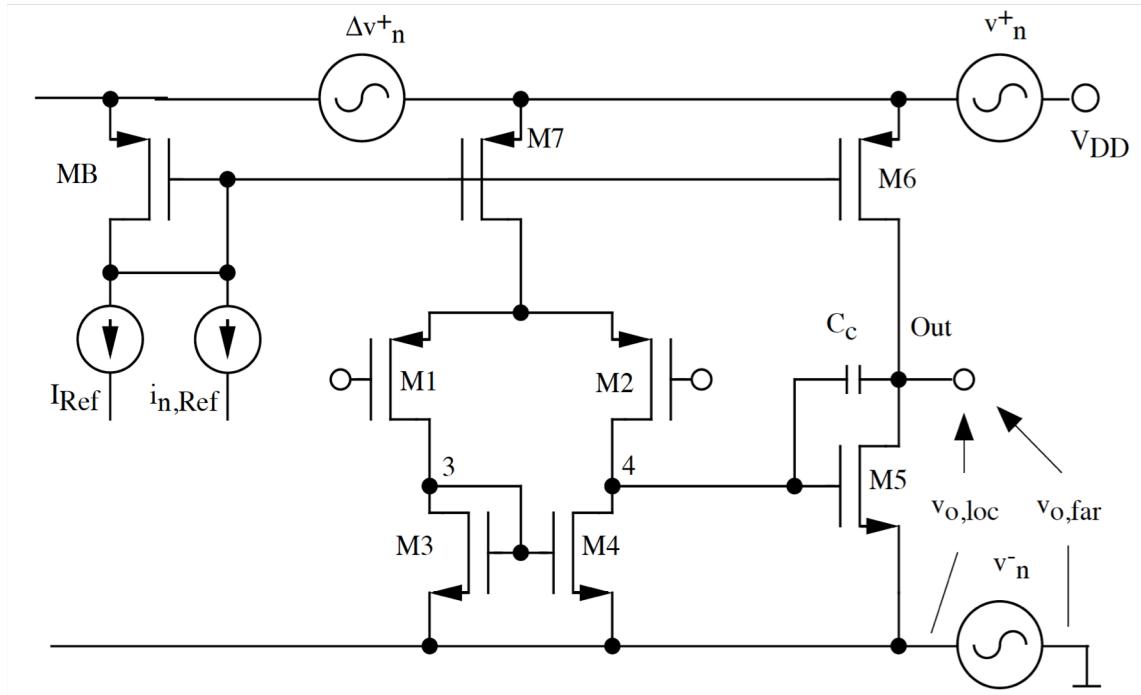
- ❖ Δv^+_n modifies the gate-to-source voltage originated by M_B , thus affecting the currents of M_7 and M_6 . The effect can be combined (in a quadratic way since they are uncorrelated) to the one of $i_{n,Ref}$
- ❖ Calculations lead to:

$$V_{out,I_n} = I_{n,Ref} \left[\frac{(W/L)_6}{(W/L)_B} - \frac{1}{2} \frac{(W/L)_5 (W/L)_7}{(W/L)_4 (W/L)_B} \right] \frac{1}{g_{ds6} + g_{ds5}}$$

POWER SUPPLY REJECTION



Effect of Δv^+_n and $i_{n,Ref}$ at DC

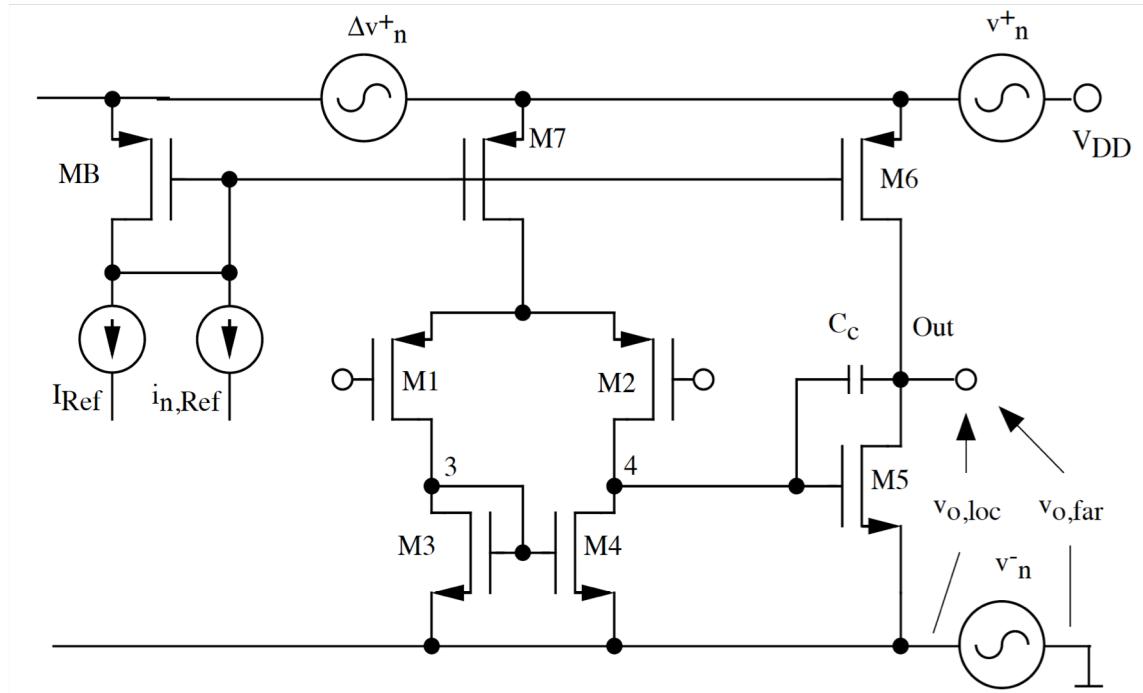


- ❖ The previous expression leads to zero noise at the output node if the condition to achieve zero systematic offset is satisfied
- ❖ Nulling the systematic offset also permits, hence, to reject the low frequency components of Δv^+_n and $i_{n,Ref}$

POWER SUPPLY REJECTION



Effect of Δv^+_n and $i_{n,Ref}$ at high frequency



- ❖ Capacitor C_c connects the gate and drain of M_5 . The contribution of the first stage vanishes and the second stage behavior fully controls the output voltage

$$V_{o,n} = i_{n,Ref} \frac{(W/L)_6}{(W/L)_B} \cdot \frac{I}{g_{m,5}}$$

POWER SUPPLY REJECTION



Effect of v_n^+ and v_n^- at DC

$$v_{out,n}^+ = -\frac{v_n^+}{2g_{m3}r_{ds7}} \frac{g_{m5}}{g_{ds5} + g_{ds6}} + \frac{g_{ds6}v_n^+}{g_{ds5} + g_{ds6}}$$

$$PSRR^+ = \frac{A_d v_n^+}{v_{out,n}^+} = \frac{2g_{m1}g_{m3}g_{m5}r_{ds7}}{(g_{ds2} + g_{ds4})(g_{m5} - 2g_{ds6}g_{m3}r_{ds7})}$$

$$v_{out,n}^- = \frac{v_n^-}{2g_{m3}r_{ds7}g_{m1,2}r_{ds1}} \frac{g_{m5}}{g_{ds5} + g_{ds6}} - \frac{g_{ds6}v_n^-}{g_{ds5} + g_{ds6}}$$

$$PSRR^- = \frac{A_d v_n^-}{v_{out,n}^-} = \frac{2g_{m1}^2 g_{m3} g_{m5} r_{ds1} r_{ds7}}{(g_{ds2} + g_{ds4})(g_{m5} - 2g_{ds6}g_{m1}g_{m3}r_{ds1}r_{ds7})}$$



Effect of v_n^+ and v_n^- at high frequency

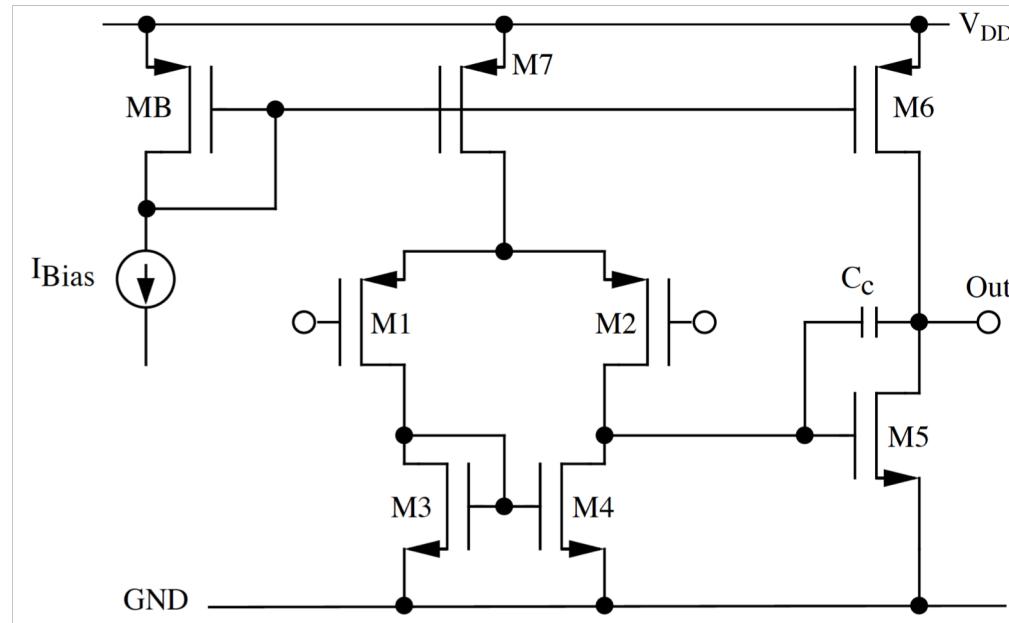
- ❖ Capacitor C_c connects the gate and drain of M_5 . Again, the contribution of the first stage vanishes
- ❖ The contribution of the second stage is given by the resistive divider between $1/g_{m5}$ and r_{ds6}

$$v_{out,n} = \frac{(v_n^+ - v_n^-)}{1 + g_{m5}r_{ds6}}$$

Contribution of external components

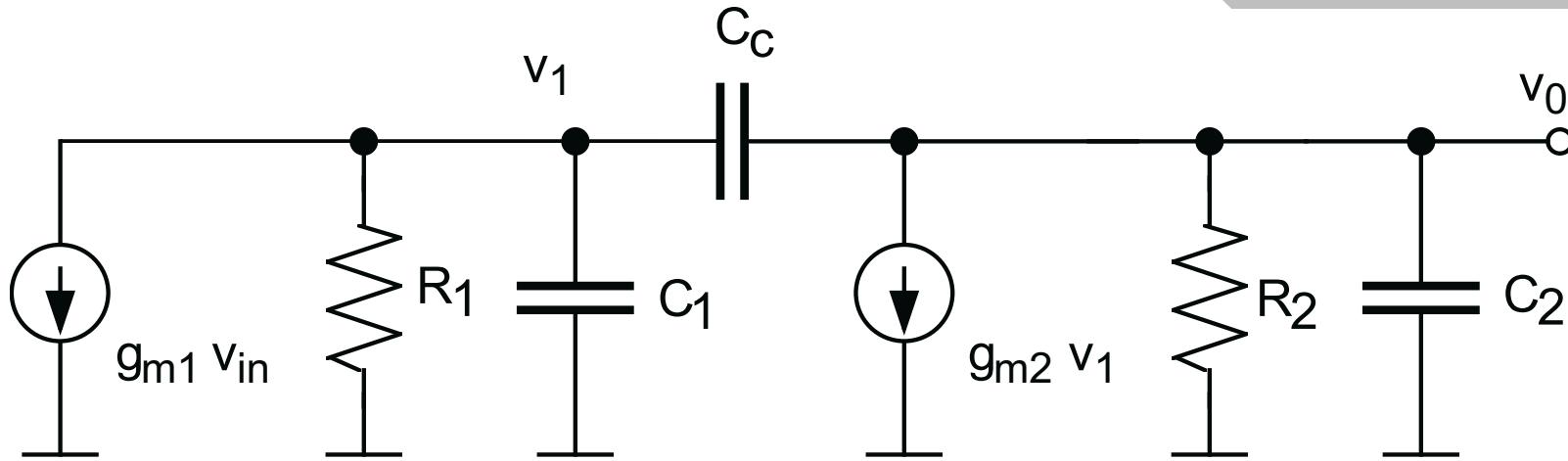
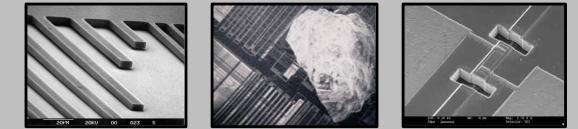
- ❖ In most of the cases, the PSRR at high frequency is determined by external parasitic capacitors and inductors

FREQUENCY RESPONSE



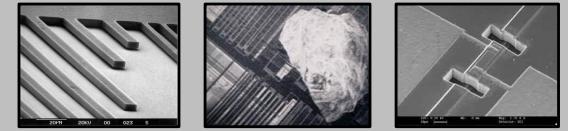
- ❖ A two stage scheme with poles in the same frequency range is unstable in closed loop and needs compensation
- ❖ A single pole system is always stable
- ❖ The strategy consists in approaching the single pole behavior by splitting the two poles apart

FREQUENCY RESPONSE



- ❖ Each stage is represented by a transconductance generator and the parallel connection of an output resistance and a load capacitance
- ❖ First stage: DC gain $A_{v1}=g_{m1}R_1$, pole p'_1 at angular frequency $1/R_1C_1$
- ❖ Second stage: $A_{v2}=g_{m2}R_2$, pole p'_2 at angular frequency $1/R_2C_2$
- ❖ R_1 and R_2 are the parallel connections of two r_{ds}
- ❖ C_1 and C_2 are the parallel connections of parasitic capacitances and eventual load capacitances

STABILITY



- ❖ The two time constants of the first and second stage are not significantly different: poles p'_1 and p'_2 are around the same frequency, leading to instability in closed loop configuration
- ❖ Compensation is required: Miller compensation with capacitor C_c connected between input and output of the second stage

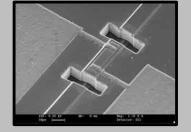
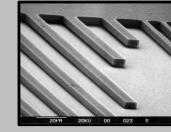
$$\begin{cases} v_1 \left(\frac{1}{R_1} + sC_1 \right) + (v_1 - v_0) sC_c + g_{m1} V_{in} = 0 \\ v_0 \left(\frac{1}{R_2} + sC_2 \right) + (v_0 - v_1) sC_c + g_{m2} V_1 = 0 \end{cases}$$

⇓

$$\frac{v_0}{V_{in}} \cong g_{m1} R_1 R_2 \frac{g_{m2} - sC_c}{1 + sR_1 R_2 g_{m2} C_c + s^2 R_1 R_2 [C_1 C_2 + (C_1 + C_2) C_c]}$$

- ❖ One zero and two poles

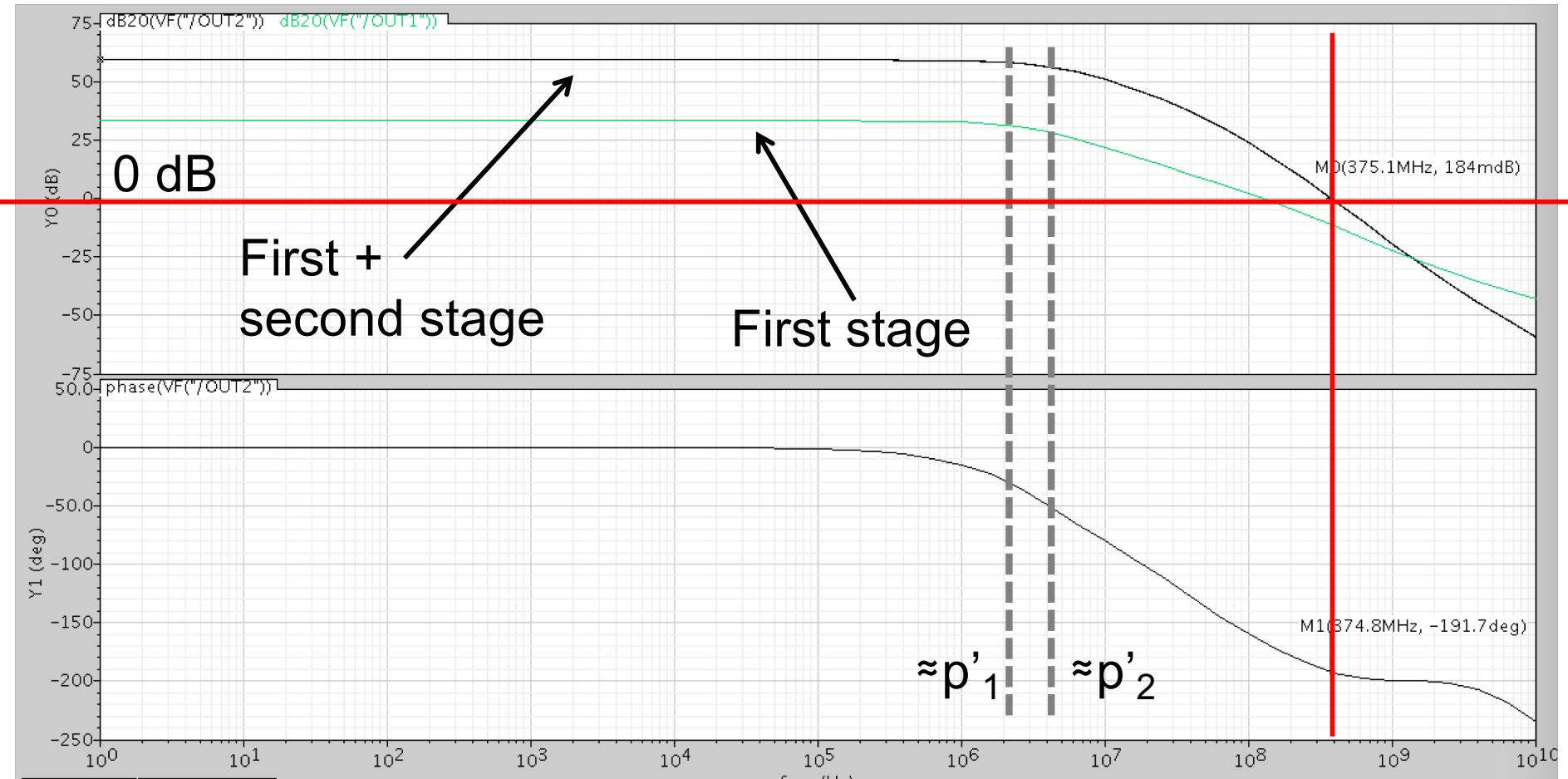
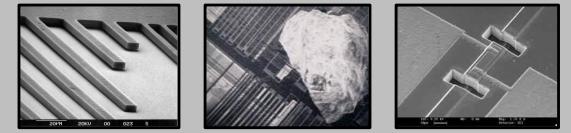
POLES AND ZEROS



$$p_1 \cong \frac{-1}{g_{m2} R_2 R_1 C_c}$$
$$p_2 \cong \frac{-g_{m2} C_c}{C_1 C_2 + (C_1 + C_2) C_c}$$
$$z = +\frac{g_{m2}}{C_c}$$

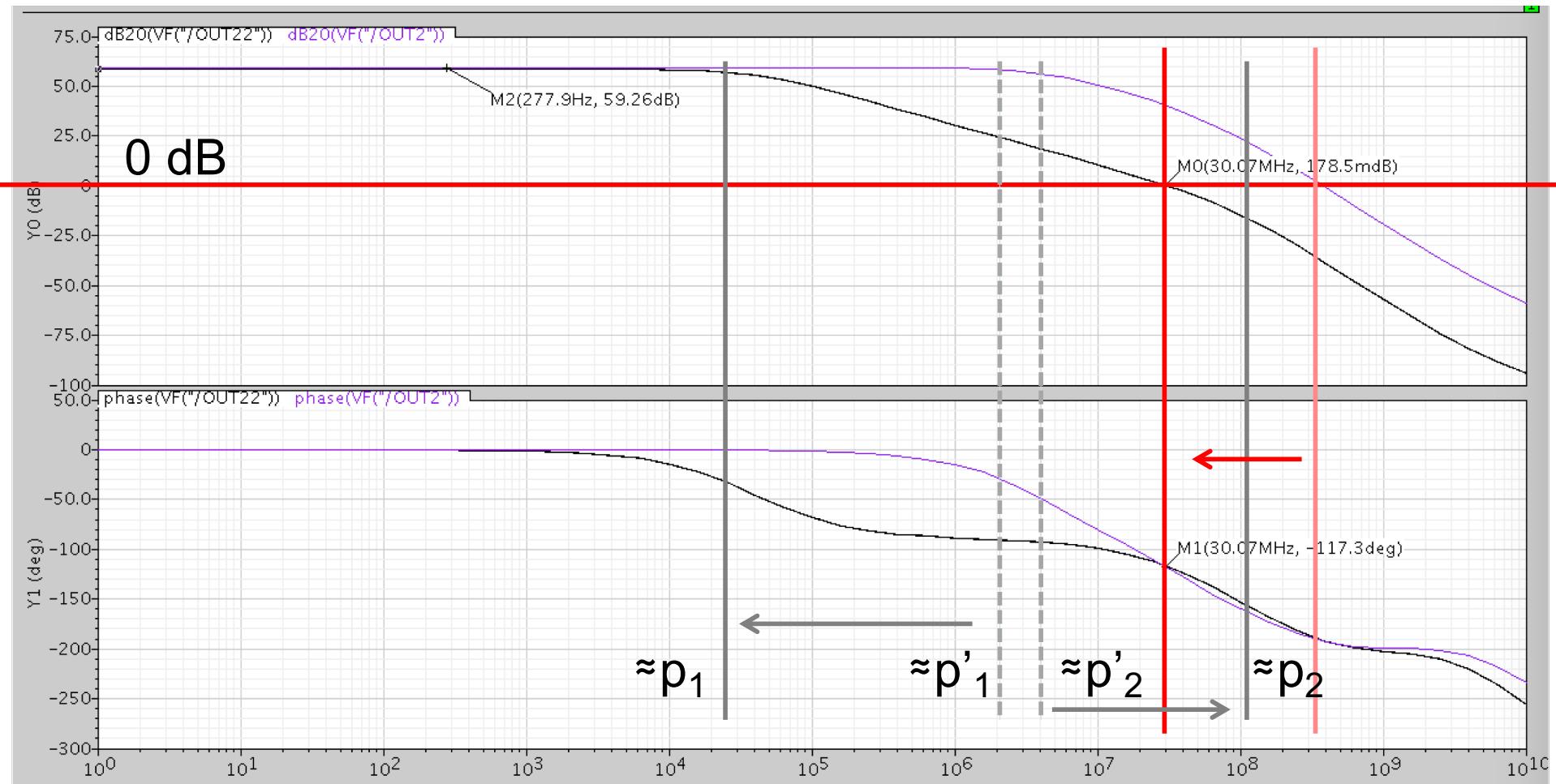
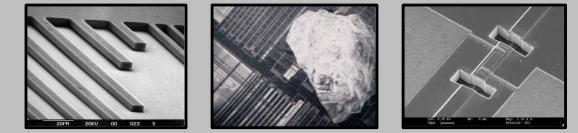
- ❖ Pole splitting: pole p'_1 is pushed at low frequency and becomes the so called *dominant pole* (p_1). Pole p'_2 is pushed at high frequency (p_2)
- ❖ The zero (z) is in the right half plane
- ❖ It produces a phase shift which is negative like the one caused by a pole
- ❖ It worsens the phase margin and creates a problem if the zero is located close to the unity gain frequency

POLE SPLITTING



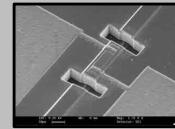
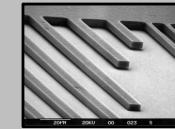
- ❖ Simulation with 0.18- μm CMOS technology

POLE SPLITTING



- ❖ Simulation with 0.18- μm CMOS technology

FREQUENCY RESPONSE



- ❖ Assuming the first pole (p_1) is dominant, multiplying it by the DC gain of the amplifier achieves the unity gain angular frequency

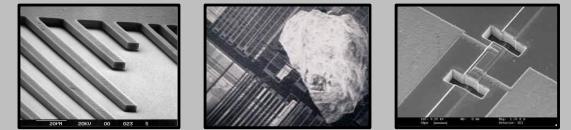
$$\omega_t = 2\pi f_t = A_v p_1 = g_{m1} R_1 g_{m2} R_2 \frac{1}{g_{m2} R_2 R_1 C_c} = \frac{g_{m1}}{C_c}$$

- ❖ The position of the zero (z, located in the right half plane) with respect to ω_t is:

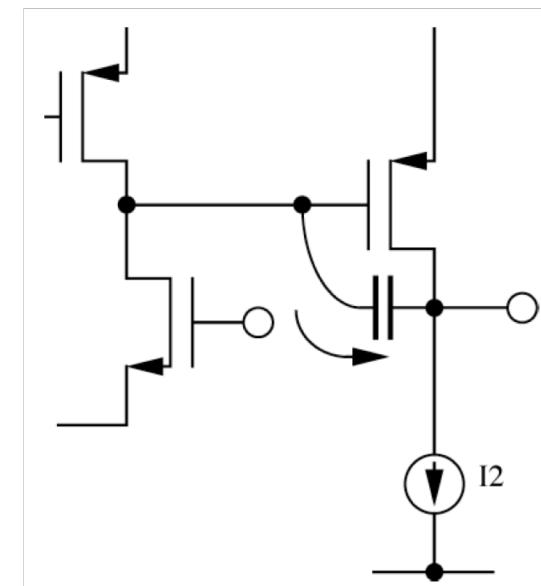
$$\frac{|z|}{\omega_t} = \frac{g_{m2}}{g_{m1}} \cong 1$$

- ❖ Unless g_{m2} is much larger than g_{m1} (not easy to realize in CMOS technology), the zero is located close to the expected ω_t , thus degrading the stability conditions
- ❖ It is needed to find out remedies to avoid the phase margin degradation

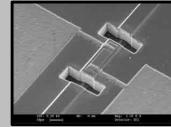
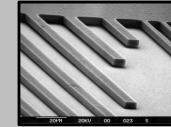
ZERO COMPENSATION



- ❖ The problem of the zero in the right half plane can be solved by three techniques:
 - Use of a unity-gain buffer
 - Use of the zero-nulling resistor
 - Use of a unity gain current amplifier
- ❖ The zero is due to signal feedforwarding to a point that is 180° out of phase



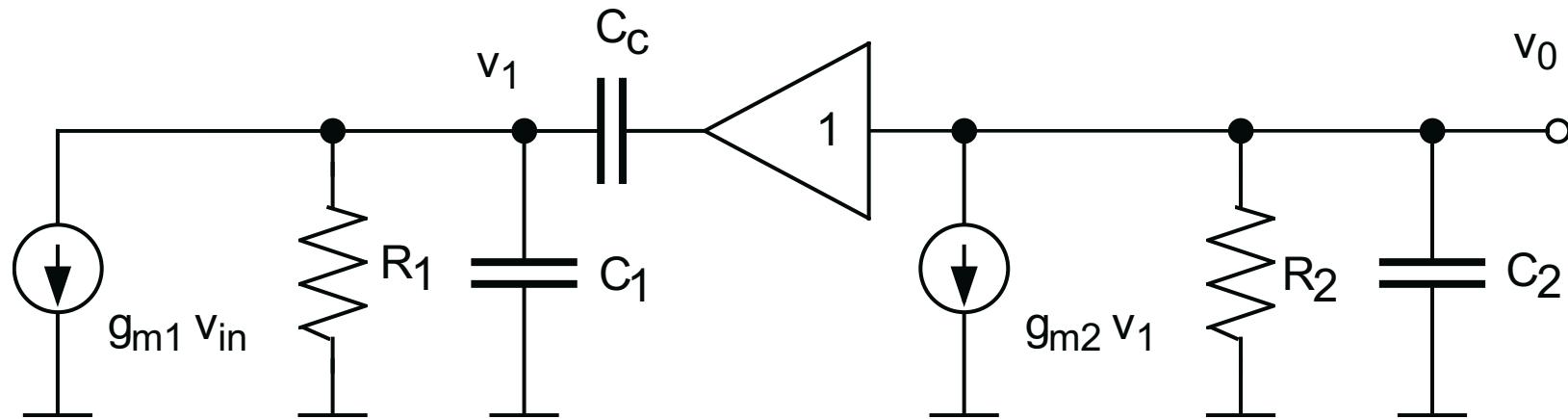
UNITY-GAIN BUFFER



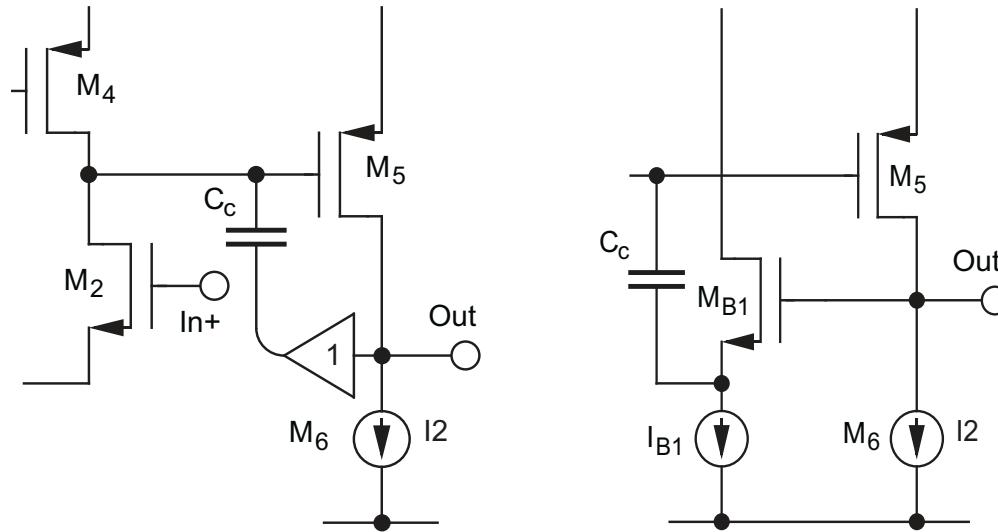
- The transfer function of a two stage amplifier with Miller compensation capacitor for pole splitting is:

$$\frac{v_0}{v_{in}} \cong g_{m1} R_1 R_2 \frac{g_{m2} - sC_c}{1 + sR_1 R_2 g_{m2} C_c + s^2 R_1 R_2 [C_1 C_2 + (C_1 + C_2) C_c]}$$

- The responsible of the zero is the term $-sC_c$. The use of a buffer in between the two stages eliminates the feedforward path due to C_c

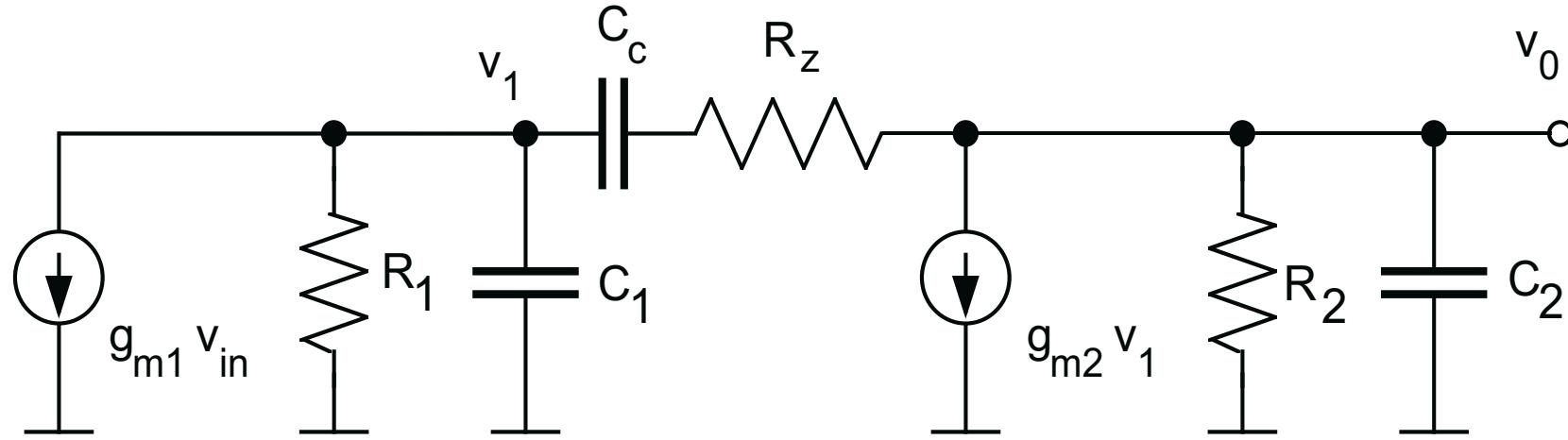


UNITY-GAIN BUFFER IMPLEMENTATION



- ❖ A source follower implements the buffer
- ❖ Output swing limitation. The output has to be at least $V_{th} + 2V_{sat}$ otherwise the current generator I_{B1} goes in triode
- ❖ At high frequency, the finite bandwidth of the follower matters. The result is that the zero is not eliminated but a doublet zero-pole (in the left half plane) appears (normally not too problematic)
- ❖ The scheme obviously increases the power consumption and the occupied area

ZERO-NULLING RESISTOR



❖ Capacitance C_c is replaced with an impedance:

$$\frac{1}{sC_c} \Rightarrow \frac{sC_c}{1 + sR_z C_c}$$

❖ The poles remain almost unchanged, while the zero becomes:

$$Z = \frac{1}{C_c \left(\frac{1}{g_{m2}} - R_z \right)}$$

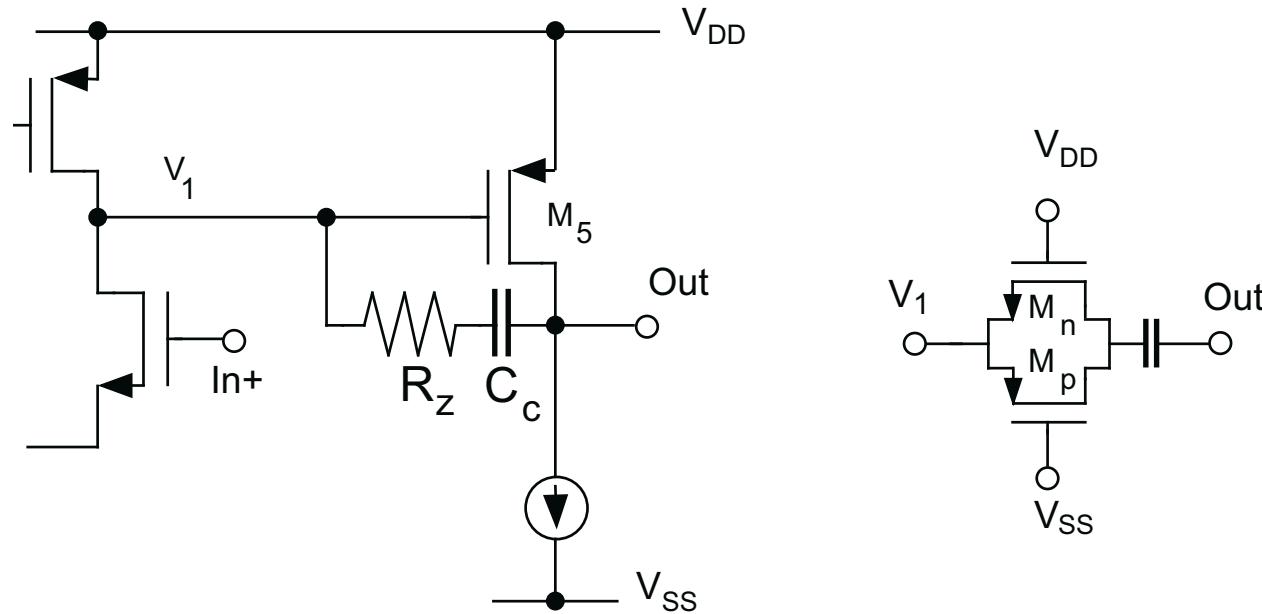
ZERO-NULLED RESISTOR VALUE



$$z = \frac{1}{C_c \left(\frac{1}{g_{m2}} - R_z \right)}$$

- ❖ Depending on the value of R_z , the zero location moves
- ❖ If $R_z > 1/g_{m2}$, the zero is located in the left half plane. This can be attractive in order to try to cancel a pole with a zero so as to enlarge the bandwidth (but be careful with the accuracy of resistors!)
- ❖ If $R_z = 1/g_{m2}$, the zero moves to infinity (zero nulled)
- ❖ If the zero is nulled, inaccuracies or process variations will eventually move the zero to around infinite in the positive or negative half plane but always adequately far away from the critical unity gain frequency
- ❖ The zero-nulling resistor can be implemented in polysilicon or any other available resistive layer or using CMOS transistors

ZERO-NULLING IMPLEMENTATION

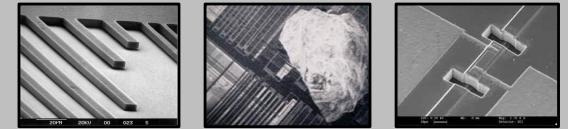


- ❖ DC currents is zero and MOS are in triode region

$$R_z = \frac{R_n R_p}{R_n + R_p}$$

$$\frac{1}{R_n} = k'_n \left(\frac{W}{L} \right)_n (V_{DD} - V_1 - V_{th,n}), \quad \frac{1}{R_p} = k'_p \left(\frac{W}{L} \right)_p (V_1 - V_{SS} - V_{th,p})$$

ZERO-NULLING IMPLEMENTATION

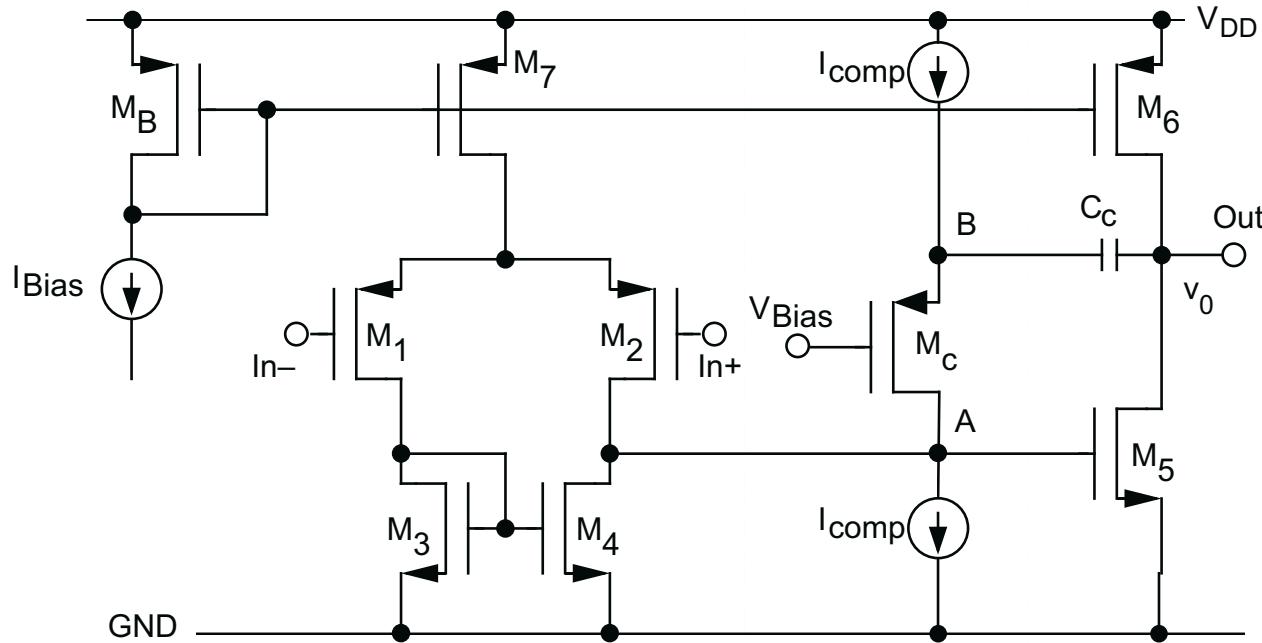


- ❖ From the electrical point of view, it does not matter if R_z is connected on the V_1 side or on V_{out} side
- ❖ The zero-nulling resistor is usually connected on the side of the compensation branch connected to V_1 , since the voltage swing of V_1 is A_2 times lower than the swing of V_{out}
- ❖ By designing $k'_n(W/L)_n = k'_p(W/L)_p$, R_z is almost independent from V_1

$$\frac{1}{R_z} = k'_n \left(\frac{W}{L} \right)_n (V_{DD} - V_{SS} - V_{th,n} - V_{th,p})$$

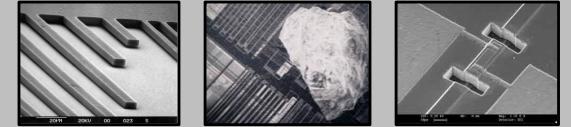
- ❖ Often, in practice, it is preferable to realize R_z with just one transistor of the same type as M_5 in order to guarantee that it operates properly in all the process corners

UNITY-GAIN CURRENT AMPLIFIER



- ❖ The feedforward path due to C_c can be interrupted using a unity-gain current amplifier
- ❖ Node A is a high-impedance node, while node B is a low-impedance one (almost ground for signal)
- ❖ The small signal current flowing in C_c is $i_c = v_o s C_c$, independent of the voltage at node A

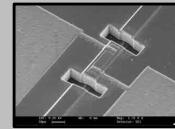
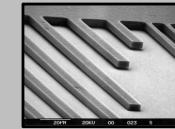
UNITY-GAIN CURRENT AMPLIFIER



$$\begin{cases} v_1 \left(\frac{1}{R_1} + sC_1 \right) - v_0 sC_c + g_{m1} V_{in} = 0 \\ v_0 \left(\frac{1}{R_2} + sC_2 \right) + v_0 sC_c + g_{m2} V_1 = 0 \end{cases}$$

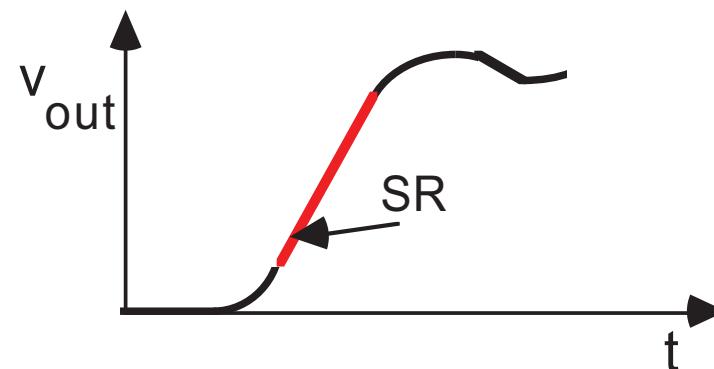
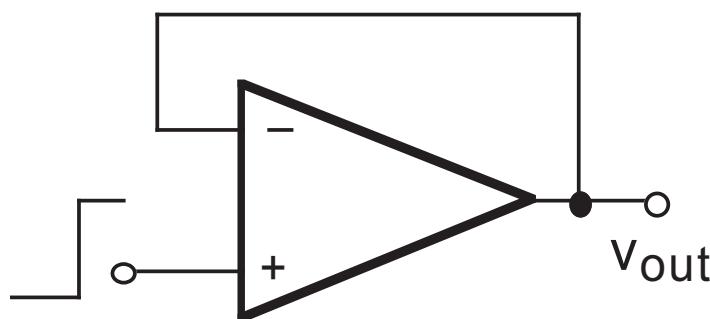
$$\frac{v_0}{v_{in}} \cong \frac{g_{m1}g_{m2}R_1R_2}{1 + sR_1R_2g_{m2}C_c + s^2R_1R_2(C_c + C_2)C_1}$$

- ❖ The two poles (p_1 and p_2) locations are almost unchanged and the zero disappears
- ❖ Care is needed while selecting the bias voltage for transistor M_c and while designing the two current sources

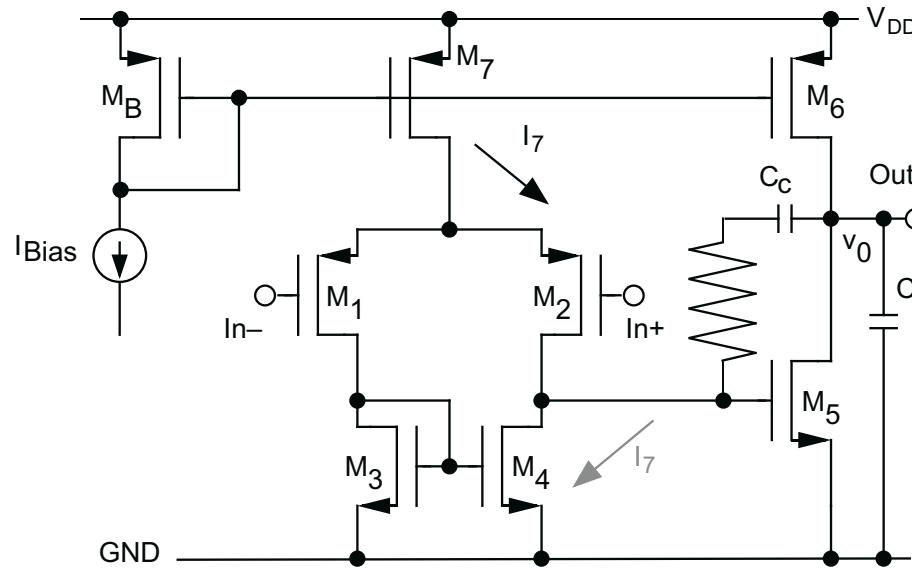


❖ Slew rate (SR):

- ❖ It is the maximum slope of the output voltage for a step signal applied at the input
- ❖ Usually it is measured with the operational amplifier in unity gain closed loop conditions
- ❖ The positive slew rate can be different from the negative slew rate
- ❖ Typically, the SR ranges from 10 to 50 V/ μ s
- ❖ Micro-power circuits (in which the quiescent current is much lower) can show much lower figures



SLEW-RATE



- ❖ A large signal at input causes complete unbalance of the input pair
- ❖ The current I_{Bias} completely flows through either M_1 or M_2
- ❖ The open loop gain drops and C_c and C_L need to be charged/discharged with the currents available in the first and second stage
- ❖ Since those currents are constant, the output voltage changes with constant slope (slew-rate)

SLEW-RATE



- ❖ In order to have symmetrical slew-rate ($SR_+ = SR_-$)

$$\frac{I_7}{C_c} = \frac{I_6}{C_c + C_L}$$

- ❖ The bias currents of the first and second stage are linked
- ❖ The slew-rate is also linked to f_t :

$$\omega_t = 2\pi f_t = \frac{g_{m1}}{C_c}$$

$$SR = \frac{I_7}{g_{m1}} \omega_t \cong (V_{GS1} - V_{th}) \omega_t$$

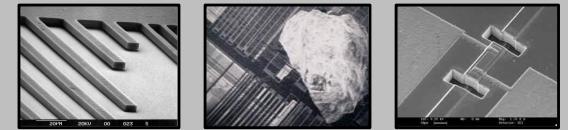
- ❖ With $(V_{GS} - V_{th}) = 300$ mV and $f_t = 20$ MHz, the slew rate becomes on the order of 40 V/ μ s

SINGLE-STAGE SCHEMES

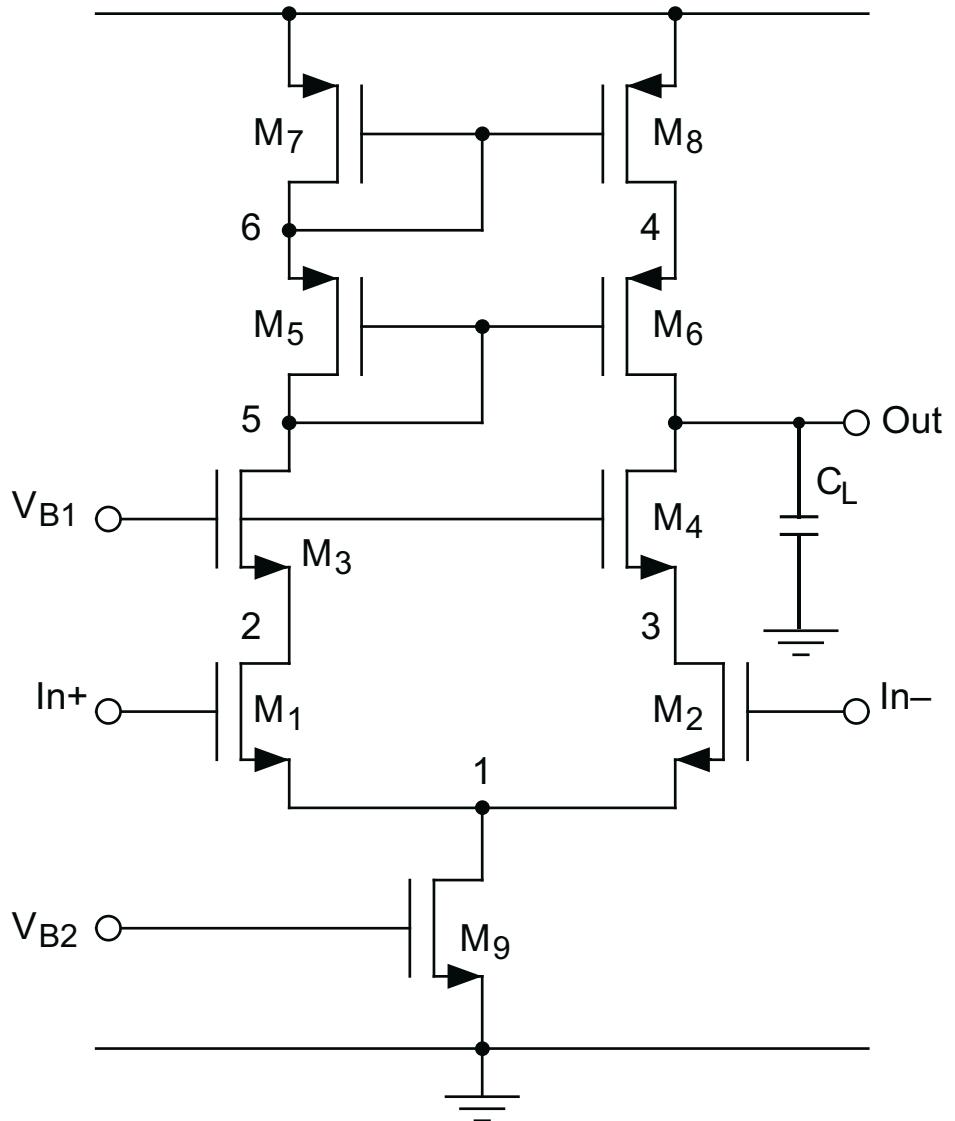


- ❖ Large gain is achieved by cascoding instead of cascading
- ❖ Having a single gain stage means that there is a single dominant pole at the output node (eventually compensated with C_L)
- ❖ At least four stacked transistors
- ❖ Different possible structures
 - ❖ Telescopic cascode
 - ❖ Mirrored cascode
 - ❖ Folded cascode
 - ❖ Regulated cascode

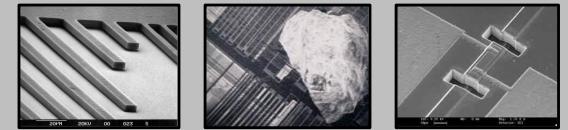
TELESCOPIC CASCODE



- ❖ The input differential pair injects the signal currents into a common gate stage
- ❖ Differential to single ended with a cascode current mirror
- ❖ 5 stacked transistors in a telescopic composition
- ❖ High small signal output resistance: parallel of two cascode configurations

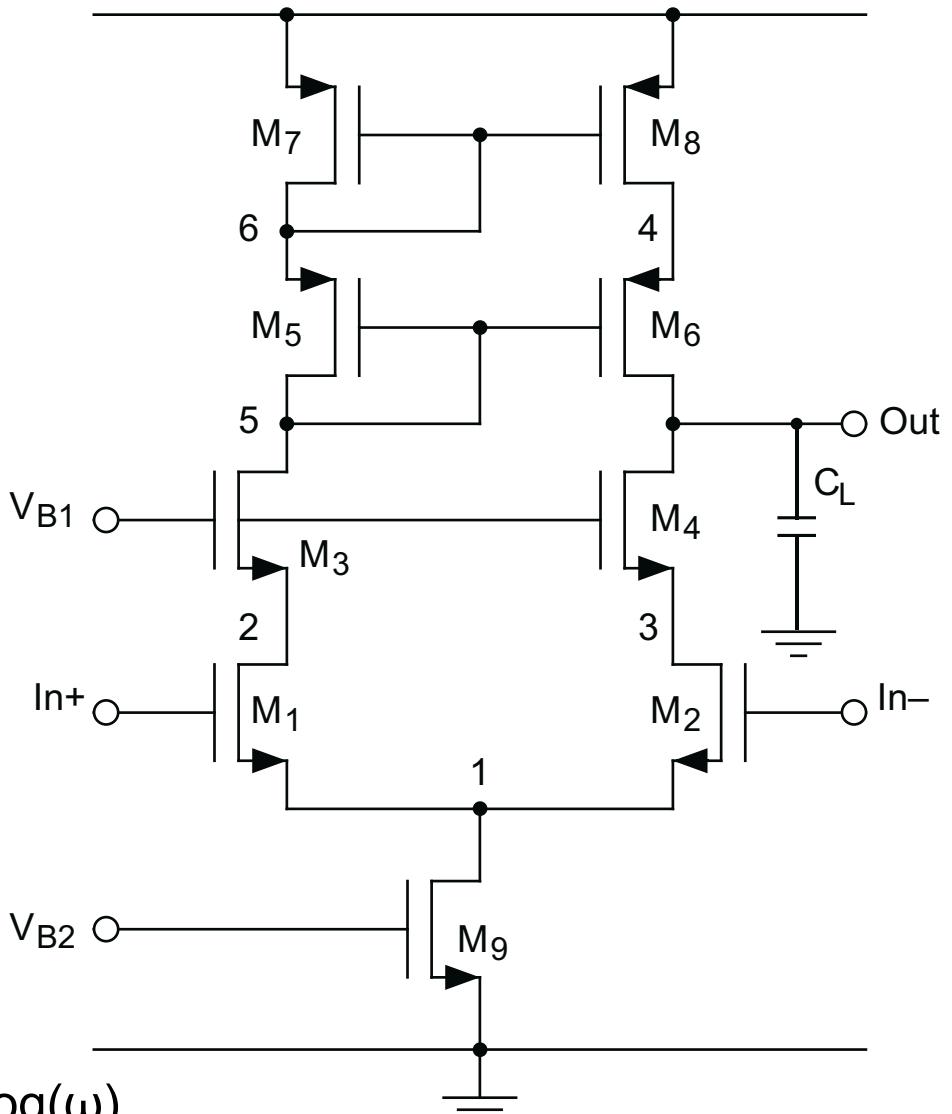
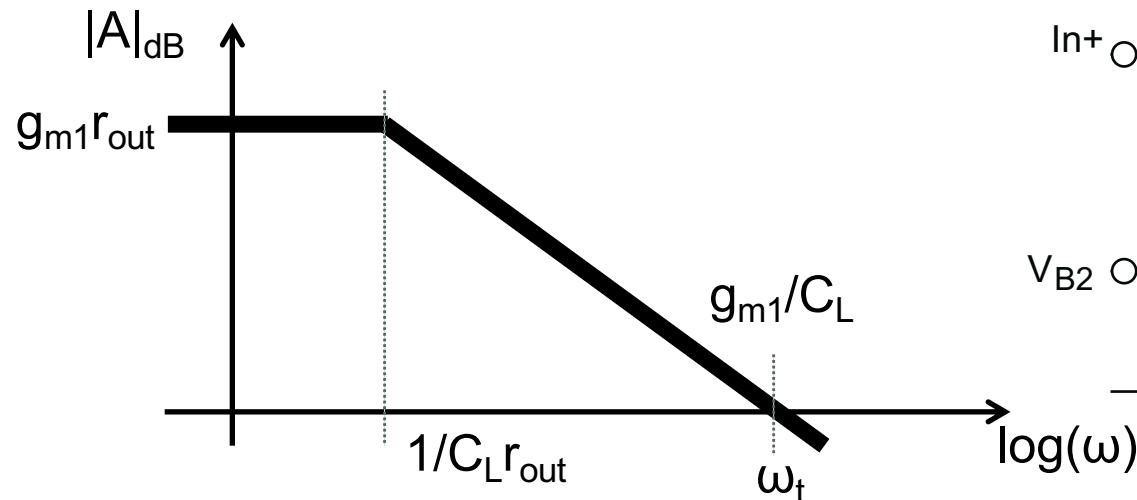


TELESCOPIC CASCODE

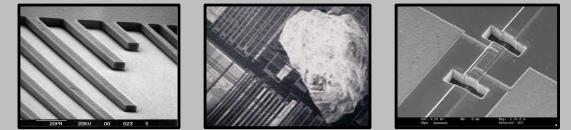


$$A_d = g_{m1,2} \frac{r_{ds8}g_{m6}r_{ds6}r_{ds2}g_{m4}r_{ds4}}{r_{ds8}g_{m6}r_{ds6} + r_{ds2}g_{m4}r_{ds4}}$$

- ❖ All low impedance nodes (will give non-dominant poles) except the output. 1 is an equivalent ground for differential signal, 2 and 3 are sources of transistors, 5 is coupled to 6 via a diode connected transistor



TELESCOPIC CASCODE



- The triode limit of M_6 establishes the maximum allowed output level

$$V_{out}|_{\max} = V_{DD} - V_{GS7} - V_{GS5} + V_{GS6} - V_{sat,6} \cong V_{DD} - V_{th,p} - 2V_{sat,p}$$

- Lower limit depends on triode of M_4 which depends on V_{B1}

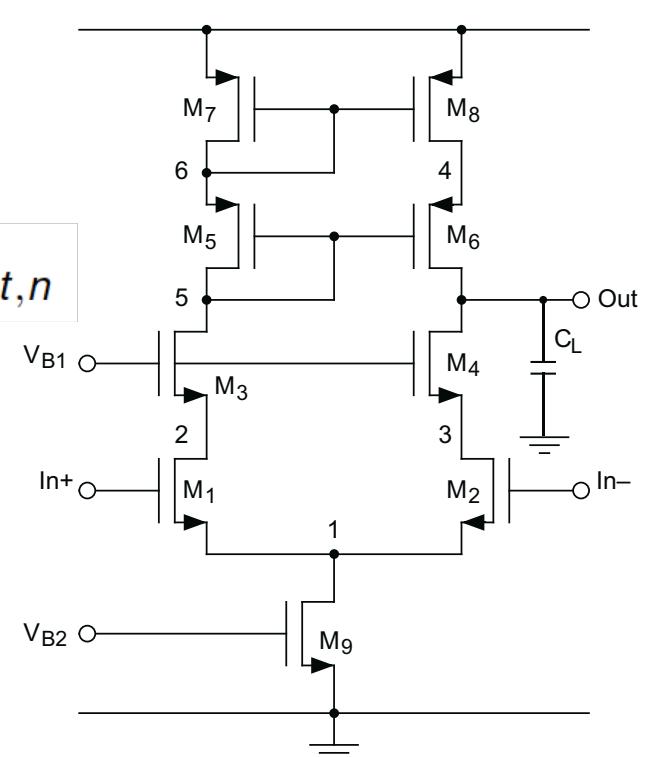
$$V_{out}|_{\min} = V_{B1} - V_{GS4} + V_{sat,4} \cong V_{B1} - V_{th,n}$$

- The value of V_{B1} affects the minimum level of the input common mode

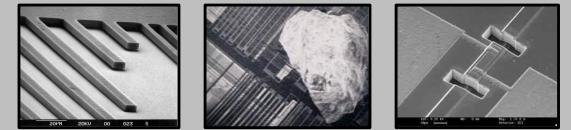
$$V_{in,cm} \leq V_{B1} - V_{GS3,4} - V_{sat,1,2} + V_{GS1,2} \cong V_{B1} - V_{sat,n}$$

- The input common mode has to keep M_9 in saturation

$$V_{in,cm} \geq V_{sat,9} + V_{GS1,2} \cong V_{th,n} + 2V_{sat,n}$$

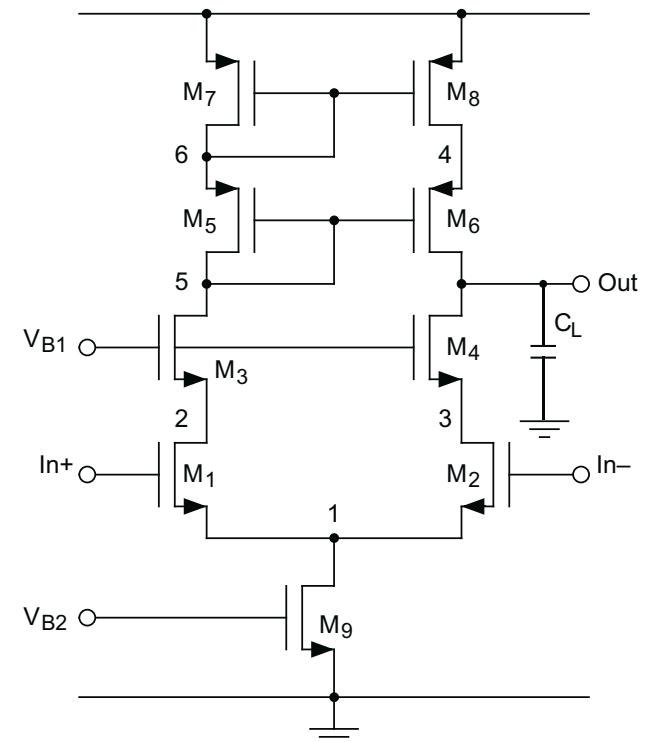


TELESCOPIC CASCODE

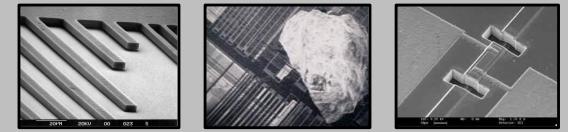


- ❖ The output common-mode voltage is different (higher) than the input common-mode voltage
- ❖ It is not possible to connect the telescopic cascode in unity gain closed-loop configuration
- ❖ The telescopic cascode uses only one bias current and, for a given bias voltage, the power is used at the best
- ❖ There is no systematic offset if $(W/L)_7 = (W/L)_8$ and $(W/L)_5 = (W/L)_6$
- ❖ Random offset as for the two-stage op-amp
- ❖ Slew-rate is symmetrical:

$$SR = SR_+ = SR_- = \frac{I_9}{C_L}$$

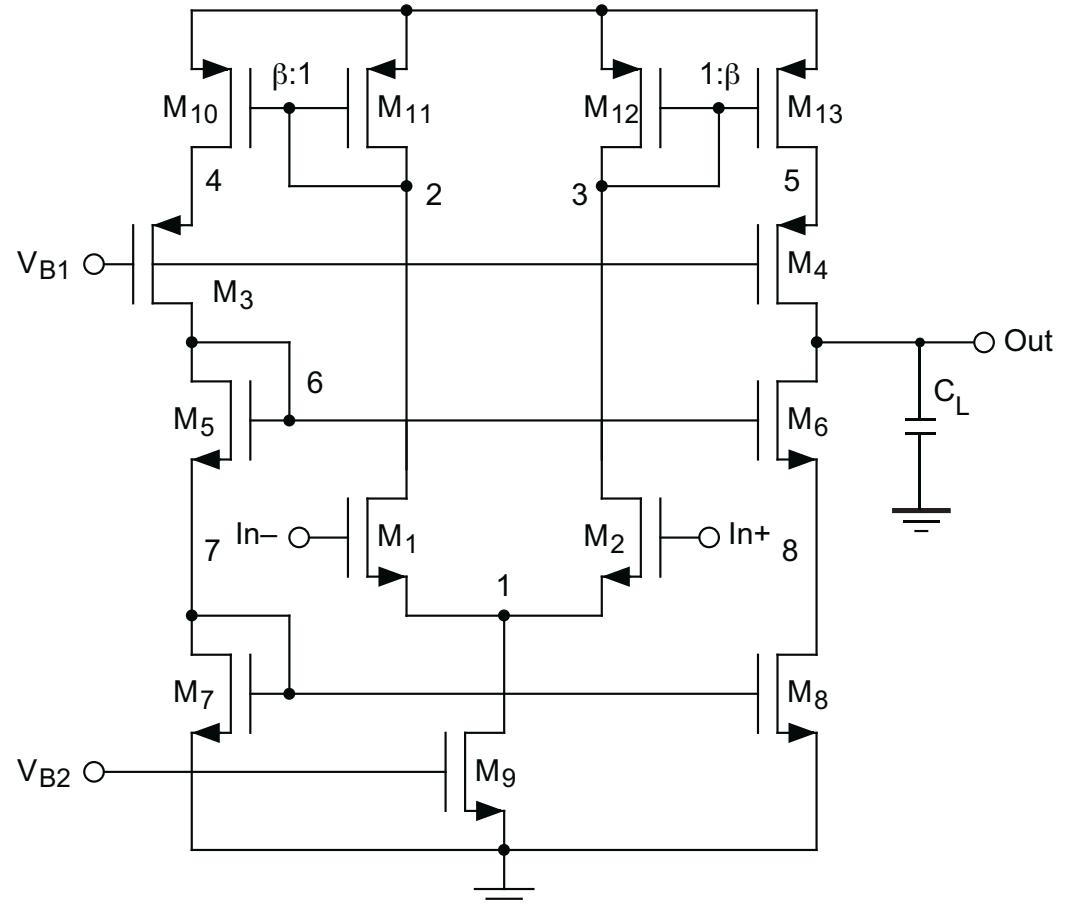


MIRRORED CASCODE

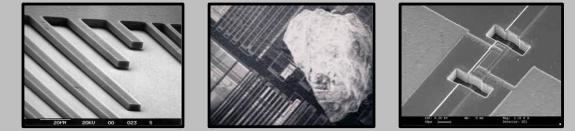


- ❖ This scheme relaxes the input common-mode range
- ❖ The signal currents generated by the input pair are mirrored by M_{11} - M_{10} and M_{12} - M_{13} (with a factor β) and delivered to a common gate stage
- ❖ The operation of the remaining part of the circuit is identical to the telescopic version

$$A_d = g_{m1,2}\beta \frac{r_{ds8}g_{m6}r_{ds6}r_{ds13}g_{m4}r_{ds4}}{r_{ds8}g_{m6}r_{ds6} + r_{ds13}g_{m4}r_{ds4}}$$



MIRRORED CASCODE



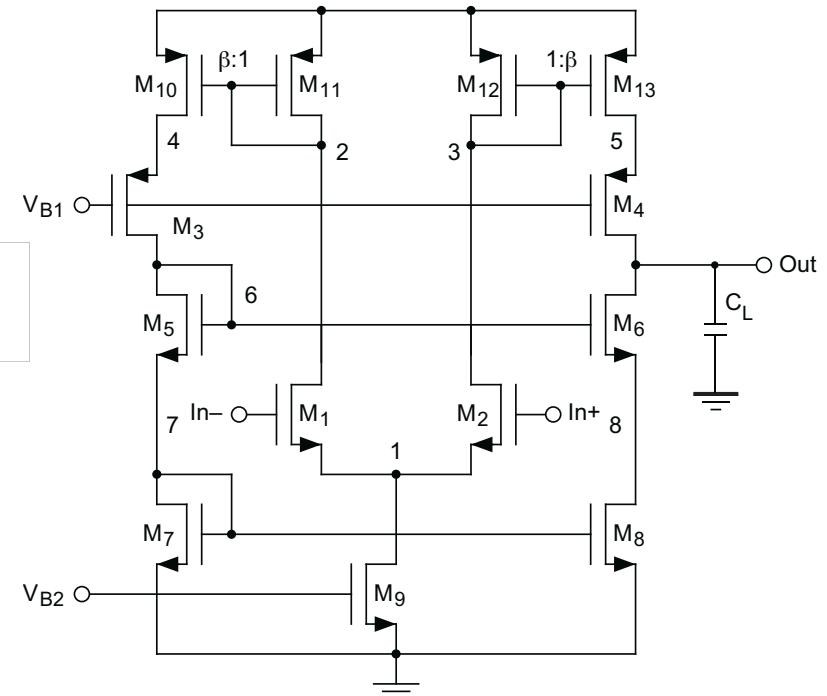
- ❖ The maximum input common mode value is

$$\begin{aligned} V_{in,cm} &\leq V_{DD} - V_{GS11,12} - V_{sat,1,2} + V_{GS1,2} \cong \\ &\cong V_{DD} + V_{th,n} - V_{th,p} - V_{sat,p} \end{aligned}$$

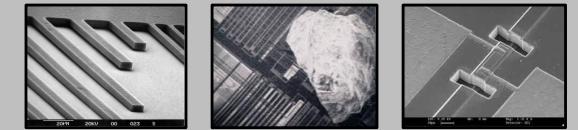
- ❖ If the two thresholds are comparable, the maximum input common mode can be very close to the supply
- ❖ The minimum value for the common mode input is determined by the triode limit of M_9

$$V_{in,cm} \geq V_{sat,9} + V_{GS1,2} \cong V_{th,n} + 2V_{sat,n}$$

- ❖ The input common mode range is pretty large



MIRRORED CASCODE



- The output range is limited by the conditions that bring M_4 and M_6 in triode. The saturation limit of M_4 depends on V_{B1} :

$$V_{B1|_{\max}} = V_{DD} - V_{sat,10,13} - V_{GS3,4} \cong V_{DD} - V_{th,p} - 2V_{sat,p}$$

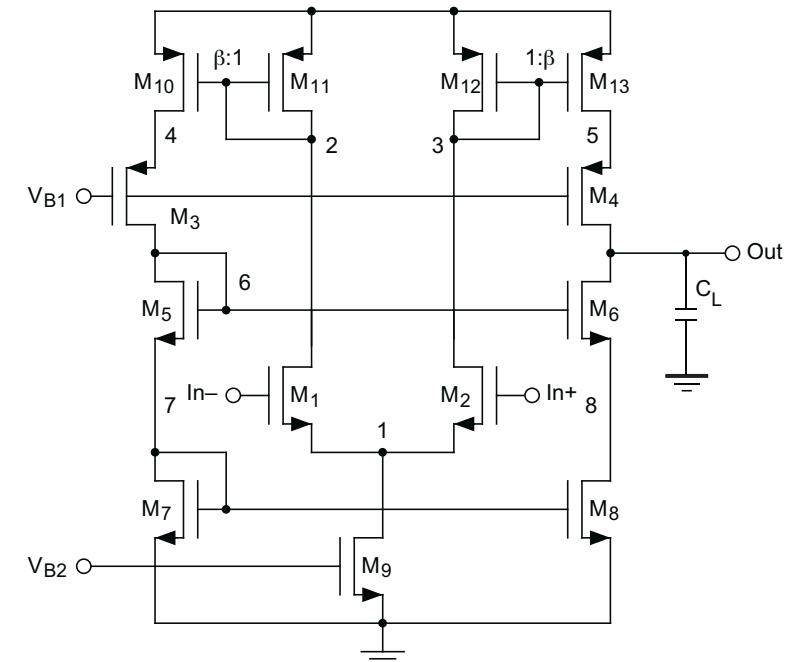
- With this condition, the maximum output voltage is:

$$V_{out|_{\max}} = V_{DD} - V_{sat,13} - V_{sat,4} \cong V_{DD} - 2V_{sat,p}$$

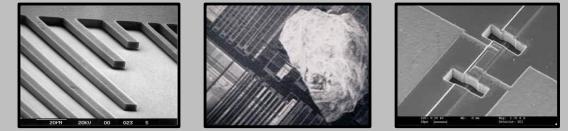
- The minimum output voltage value is:

$$V_{out|_{\min}} = V_{GS7} + V_{sat,6} \cong V_{th,n} + 2V_{sat,n}$$

- The output voltage swing is, hence, asymmetrical, but improved with respect to the telescopic scheme



MIRRORED CASCODE



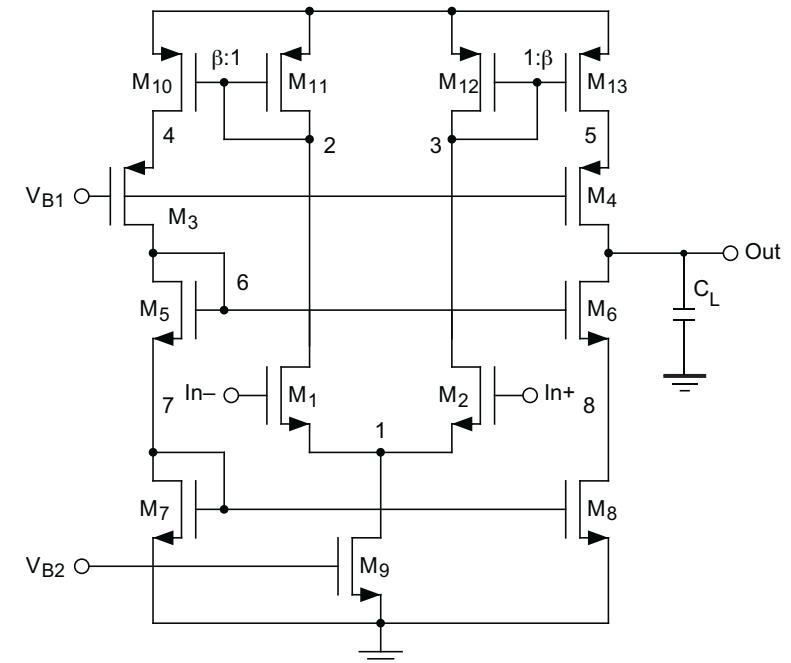
- The dominant pole is at the output node

$$p_1 = \frac{r_{ds8}g_{m6}r_{ds6} + r_{ds13}g_{m4}r_{ds4}}{C_L r_{ds8}g_{m6}r_{ds6}r_{ds13}g_{m4}r_{ds4}}$$

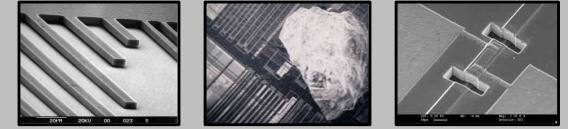
- Nodes 2, 3, 4, 5, 6, 7, and 8 introduce secondary (non-dominant) poles, which must be at frequency higher than f_t

$$\omega_t = 2\pi f_t = \frac{\beta g_{m1,2}}{C_L}$$

- Compared to the telescopic, this circuit has two additional non-dominant poles. This may degrade the phase margin to be compensated with a larger C_L (penalty in bandwidth and slew-rate)



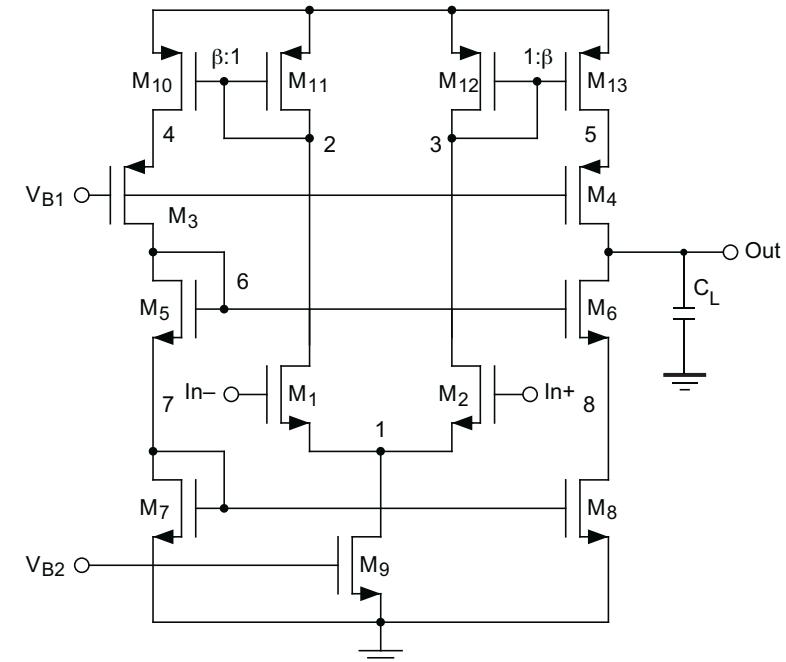
MIRRORED CASCODE



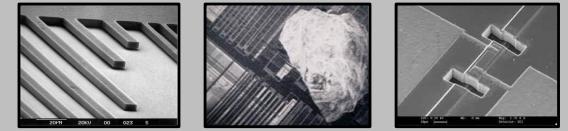
- ❖ There is no systematic offset if $(W/L)_7 = (W/L)_8$ and $(W/L)_5 = (W/L)_6$
- ❖ Random offset as for the two-stage op-amp
- ❖ Slew-rate is symmetrical:

$$SR = SR_+ = SR_- = \frac{\beta I_9}{C_L}$$

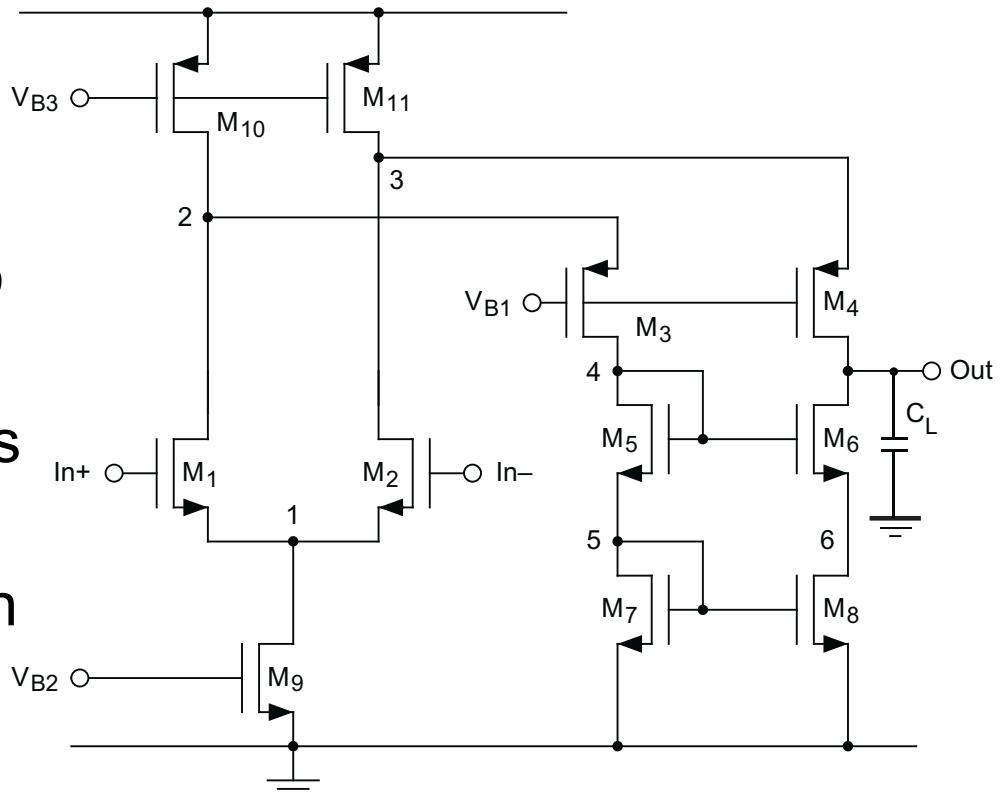
- ❖ Use of only 4 stacked transistors
- ❖ With respect to the telescopic scheme, the power consumption is increased



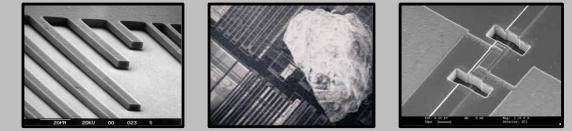
FOLDED CASCODE



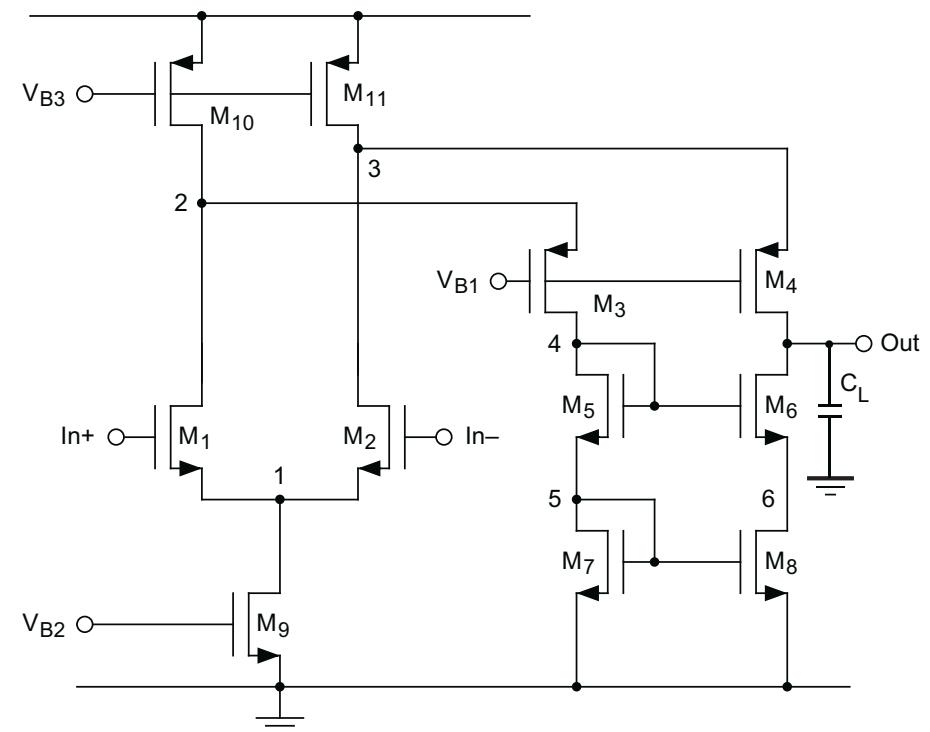
- ❖ The basic difference between mirrored and telescopic is the disconnection between the biasing of the input and output branch.
- ❖ The folded provides the same function by a direct transfer of the small signal currents from input to output
- ❖ The low impedance of the sources of M_3 and M_4 ensures the result
- ❖ Biasing of input and output branch does not affect each other: folded achieves the same benefit of mirrored for input and output common mode



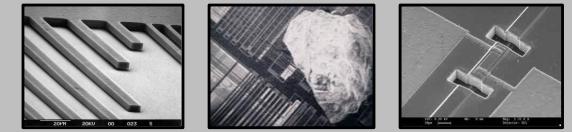
FOLDED CASCODE



- ❖ The resistance seen from the source of M_4 is the parallel connection of r_{ds2} and r_{ds11}
- ❖ The differential gain is achieved by replacing the pertinent term with the expression of that parallel connection
- ❖ Currents $I_{1,2}$ and $I_{7,8}$ are independent such as the differential gain can be optimized
- ❖ The constraints on input and output common mode swings are similar to what studied for the mirrored

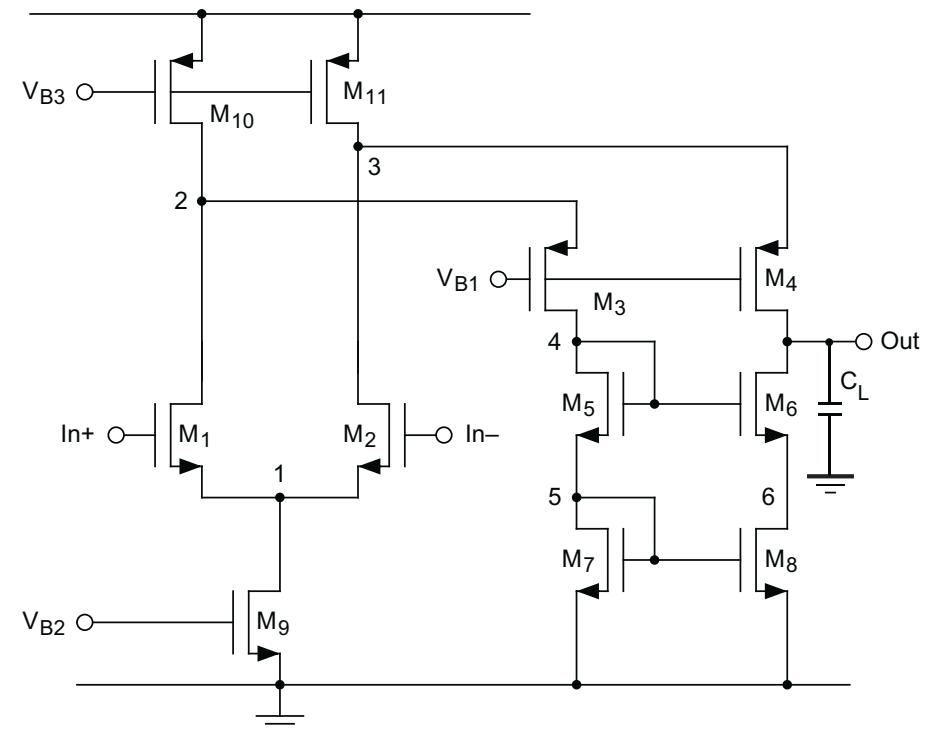


FOLDED CASCODE



- ❖ The downward swing can be improved by replacing the plain cascode current mirror with an high swing version like the high compliance cascode
- ❖ The folded cascode scheme requires additional bias currents, that, in turn, demand for extra bias generators (power and area)
- ❖ The gain-bandwidth product is:

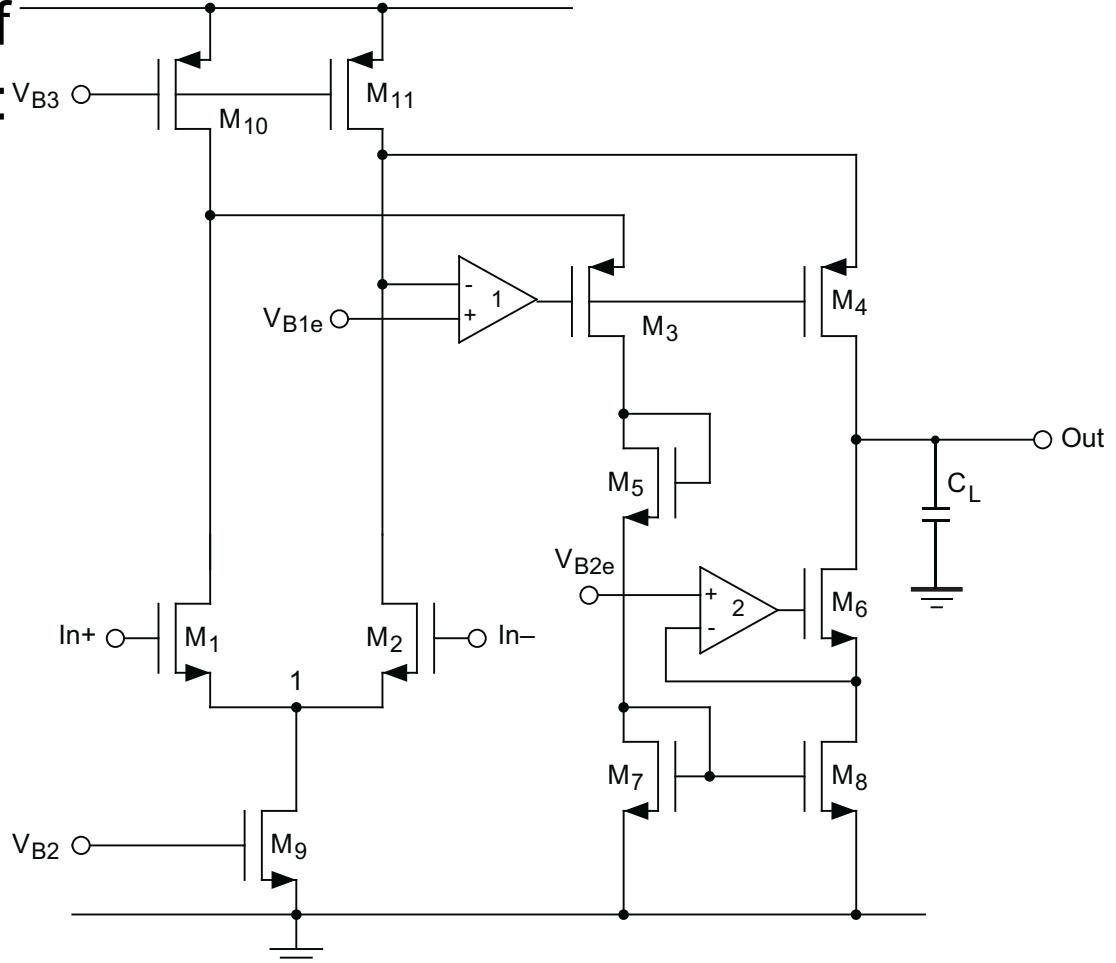
$$\omega_t = 2\pi f_t = \frac{g_{m1,2}}{C_L}$$



REGULATED FOLDED CASCODE



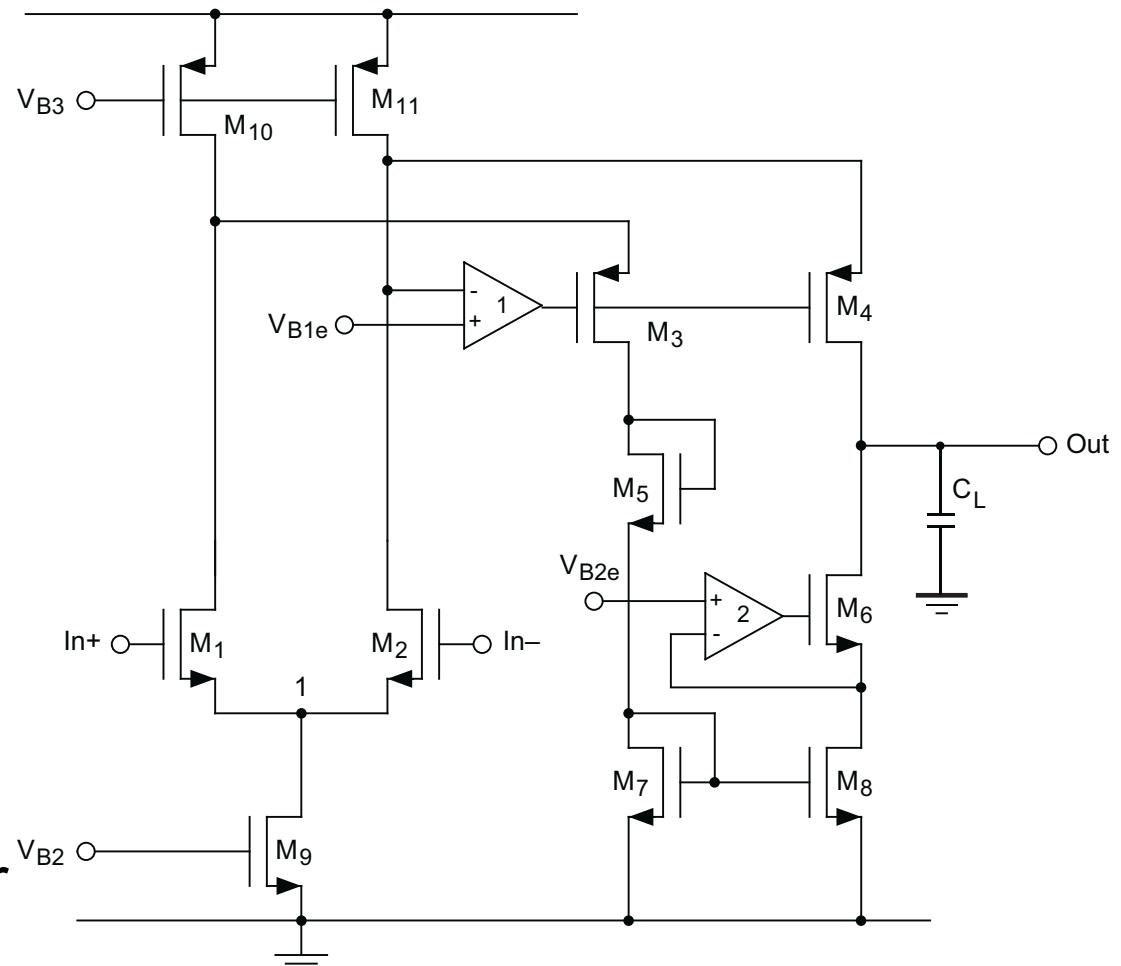
- ❖ The two auxiliary amplifiers boost the output resistance of the upper and lower cascode: result is a very very large output resistance (and so differential gain)
- ❖ Both stages control the source of the common gate stages (M_4 and M_6) to be constant
- ❖ V_{B1e} and V_{B2e} are the desired bias voltages
- ❖ M_5 in normal scheme biases the gate of M_6 . Here it provides just a drop voltage



REGULATED FOLDED CASCODE



- ❖ The frequency behavior of the circuit depends on the used gain stages and on their frequency performance
- ❖ To ensure stability, the unity gain frequencies of the gain stages must be higher than the unity gain frequency of the folded cascode
- ❖ The input common mode of the upper gain stage is close to V_{DD} (use n-channel input pair) and the one of the lower is close to ground (use p-channel input pair)



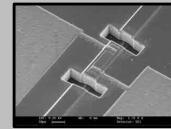
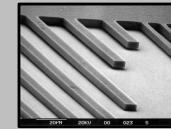
TWO STAGE Vs SINGLE STAGE



<i>Topology</i>	A_v
Two-stage	$g_m^2 r_{ds}^2 / 4$ [=]
Telescopic-cascode	$g_m^2 r_{ds}^2 / 2$ [=]
Folded-cascode	$g_m^2 r_{ds}^2 / 4$ [=]
Mirrored-cascode	$\beta g_m^2 r_{ds}^2 / 2$ [=]

<i>Topology</i>	f_t	SR
Two-stage	g_m / C_c [-]	$\min \left(\frac{I_{Bias,1}}{C_c}, \frac{I_{Bias,2}}{C_c + C_L} \right)$ [-]
Telescopic-cascode	g_m / C_L [+]	I_{Bias} / C_L [+]
Folded-cascode	g_m / C_L [+]	I_{Bias} / C_L [+]
Mirrored-cascode	$\beta g_m / C_L$ [+]	$\beta I_{Bias} / C_L$ [+]

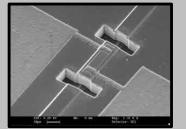
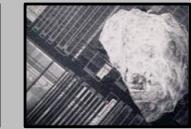
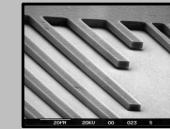
TWO STAGE Vs SINGLE STAGE



<i>Topology</i>	$V_{out} _{min}$	$V_{out} _{max}$
Two-stage	$V_{sat,n}$	[+]
Telescopic-cascode	$V_{B1} - V_{th,n}$	[−]
Folded-cascode	$V_{th,n} + 2V_{sat,n}$	[=]
Mirrored-cascode	$V_{th,n} + 2V_{sat,n}$	[=]

<i>Topology</i>	$V_{in,cm} _{min}$	$V_{in,cm} _{max}$
Two-stage	$V_{th,n} + 2V_{sat,n}$	[=] $V_{DD} + V_{th,n} +$ [=] $- V_{th,p} - V_{sat,p}$
Telescopic-cascode	$V_{th,n} + 2V_{sat,n}$	[=] $V_{B1} - V_{sat,n}$ [−]
Folded-cascode	$V_{th,n} + 2V_{sat,n}$	[=] $V_{DD} + V_{th,n} - V_{sat,p}$ [+]
Mirrored-cascode	$V_{th,n} + 2V_{sat,n}$	[=] $V_{DD} + V_{th,n} +$ [=] $- V_{th,p} - V_{sat,p}$

TWO STAGE Vs SINGLE STAGE



Advantages of two stage op-amps

- ❖ Maximum output signal swing (low-voltage operation)
- ❖ Minimum number of bias lines
- ❖ Reasonable gain also with resistive loads

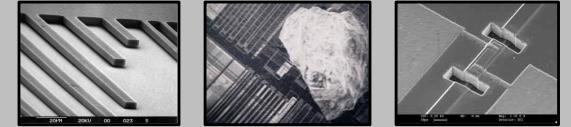
Advantages of single stage op-amps

- ❖ Compensation network not required
- ❖ Minimum power consumption for a given unity gain frequency

Op-amp choice

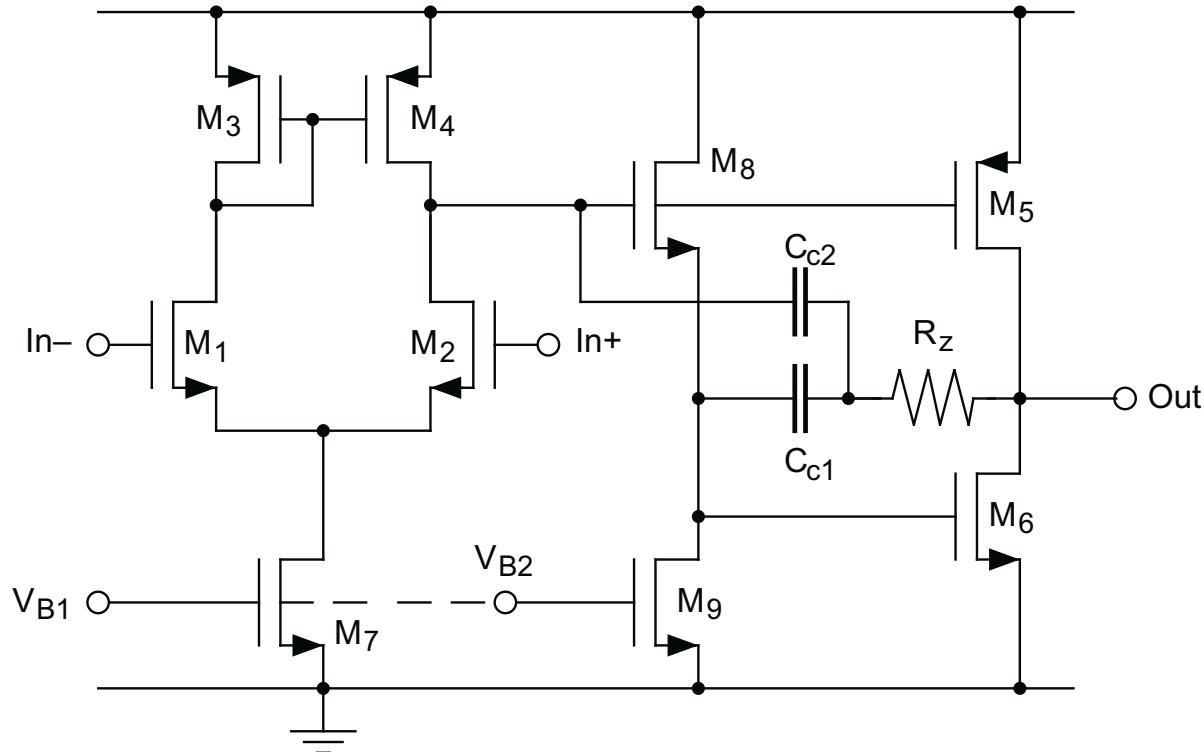
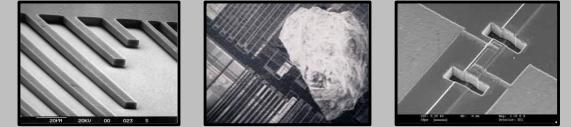
- ❖ If there are no particular requirements (like, for instance, low voltage operation), single or two stage op-amps achieve similar performance

CLASS AB OPERATIONAL AMPLIFIERS



- ❖ Class AB operational amplifiers are used to drive small resistive loads or large capacitive loads
- ❖ In CMOS integrated circuits, the load is generally capacitive
- ❖ Having large capacitive loads to be driven means imposing large slew-rate requirements
- ❖ In class AB operational amplifiers, the output current is larger than the quiescent bias current: in this way, the slew-rate is not limited by the bias current, as it was for the previously studied schemes
- ❖ Class AB operational amplifier topologies:
 - ❖ Two-stage class AB operational amplifier
 - ❖ Unfolded differential pair
 - ❖ Single-stage class AB operational amplifier

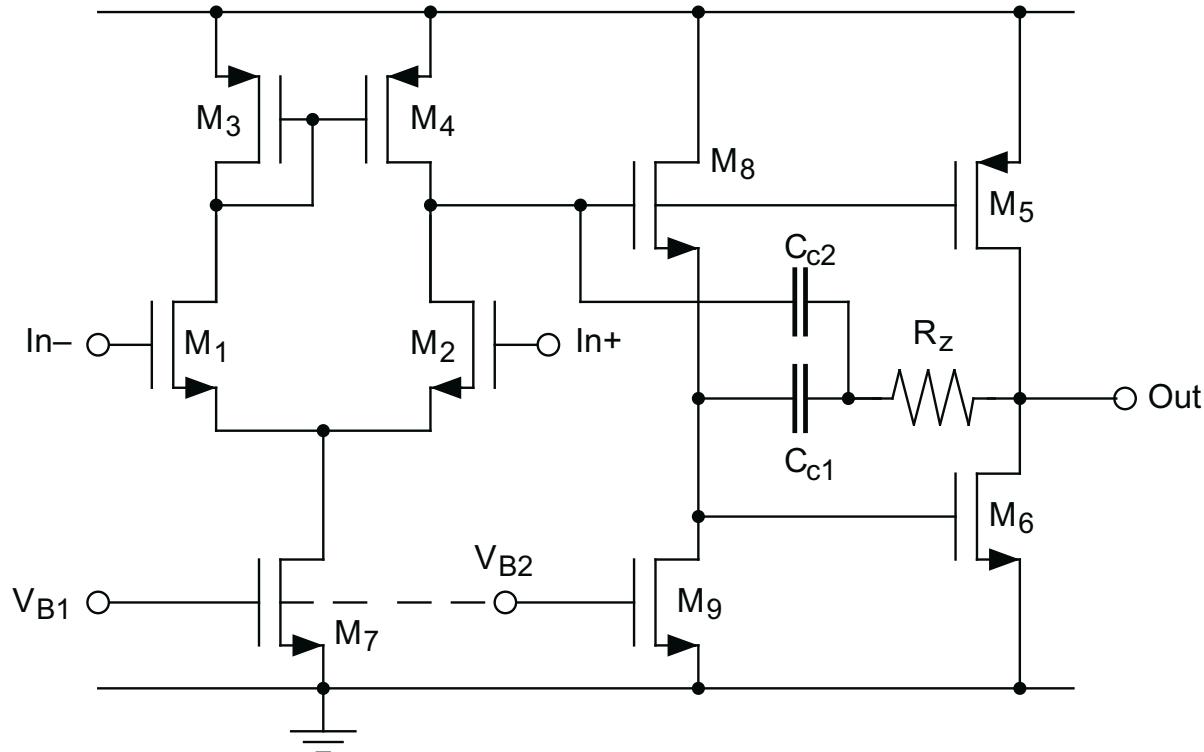
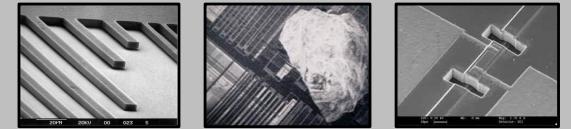
TWO-STAGE CLASS AB OP-AMP



- ❖ Transistor M_6 is no longer a fixed current source. Both M_5 and M_6 contribute to the transconductance of the second stage

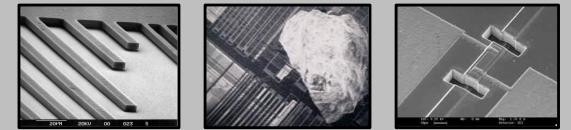
$$A_2 = \frac{g_{m5} + g_{m6}}{g_{ds5} + g_{ds6}}$$

TWO-STAGE CLASS AB OP-AMP



- ❖ C_{c1}-R_z ensure the compensation of the two-stage amplifier
- ❖ At high frequency, the pole introduced by M₈ and M₉ deteriorates the phase margin: capacitor C_{c2} avoids the problem

TWO-STAGE CLASS AB OP-AMP

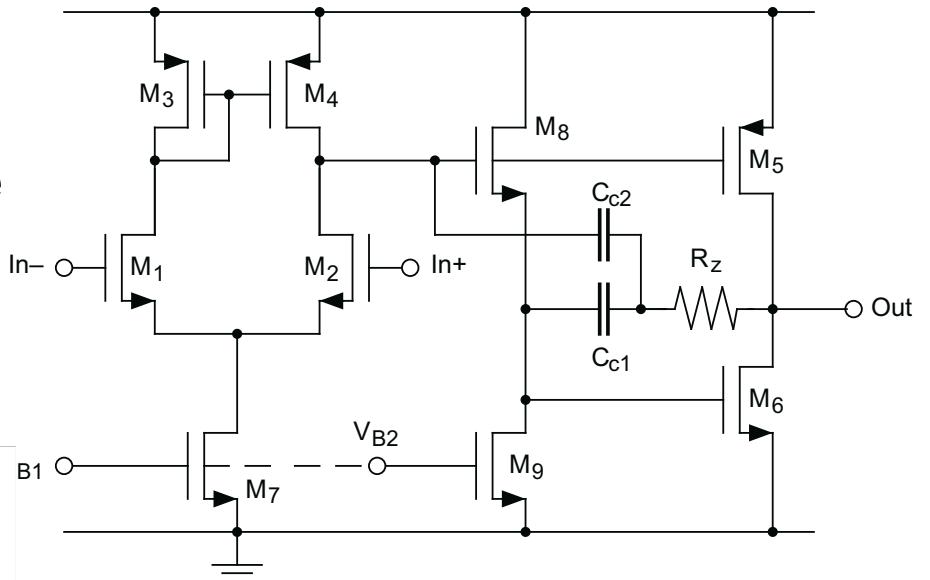


- ❖ A critical point is to control the quiescent current of the output stage $I_{5,6}$. It depends on transistor parameters and supply voltage:

$$V_{DD} = V_{GS6} + V_{GS8} + V_{GS5}$$

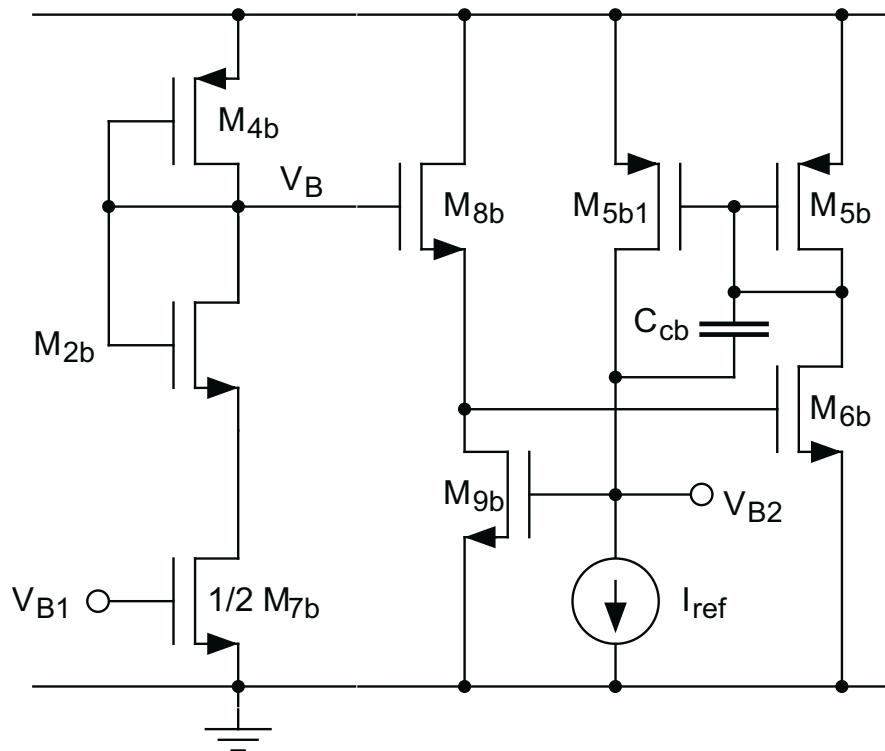
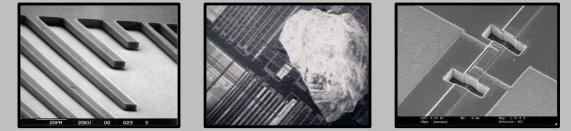
$$V_{DD} = V_{th,p} + 2V_{th,n} + \sqrt{\frac{2}{k'_n}} \left(\frac{L}{W} \right)_8 I_8 + \\ + \left[\sqrt{\frac{2}{k'_p}} \left(\frac{L}{W} \right)_5 + \sqrt{\frac{2}{k'_n}} \left(\frac{L}{W} \right)_6 \right] \sqrt{I_{5,6}}$$

$$\sqrt{I_{5,6}} = \frac{V_{DD} - V_{th,p} - 2V_{th,n} - \sqrt{\frac{2}{k'_n}} \left(\frac{L}{W} \right)_8 I_8}{\sqrt{\frac{2}{k'_p}} \left(\frac{L}{W} \right)_5 + \sqrt{\frac{2}{k'_n}} \left(\frac{L}{W} \right)_6}$$



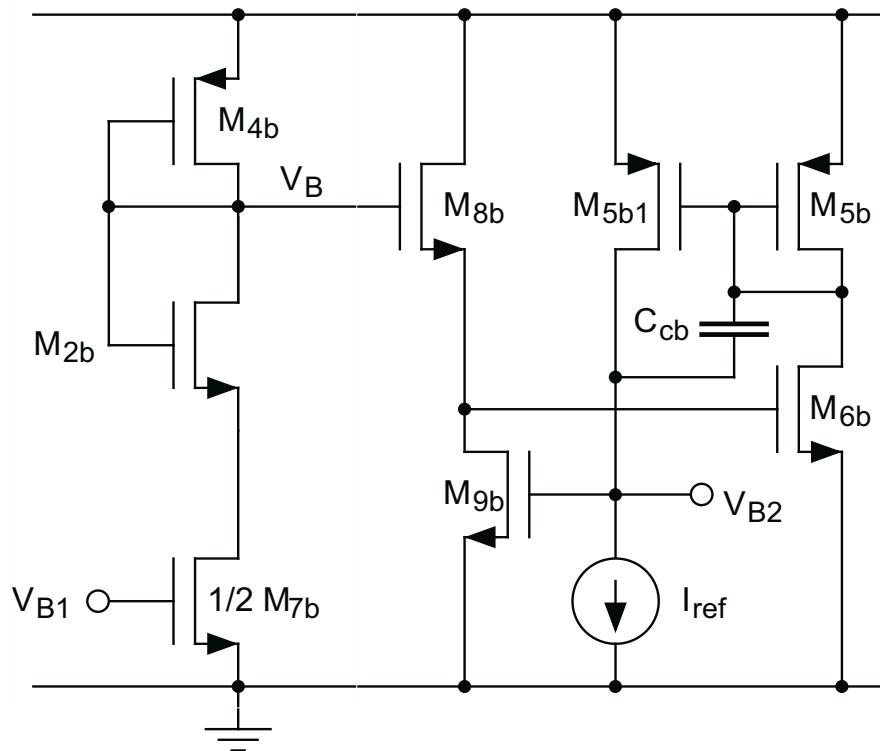
- ❖ Uncontrolled current mirror ($V_{B1}=V_{B2}$) causes current in M_6 to vary significantly with supply and thresholds
- ❖ It can be controlled by controlling the overdrive voltage of M_8

TWO-STAGE CLASS AB OP-AMP



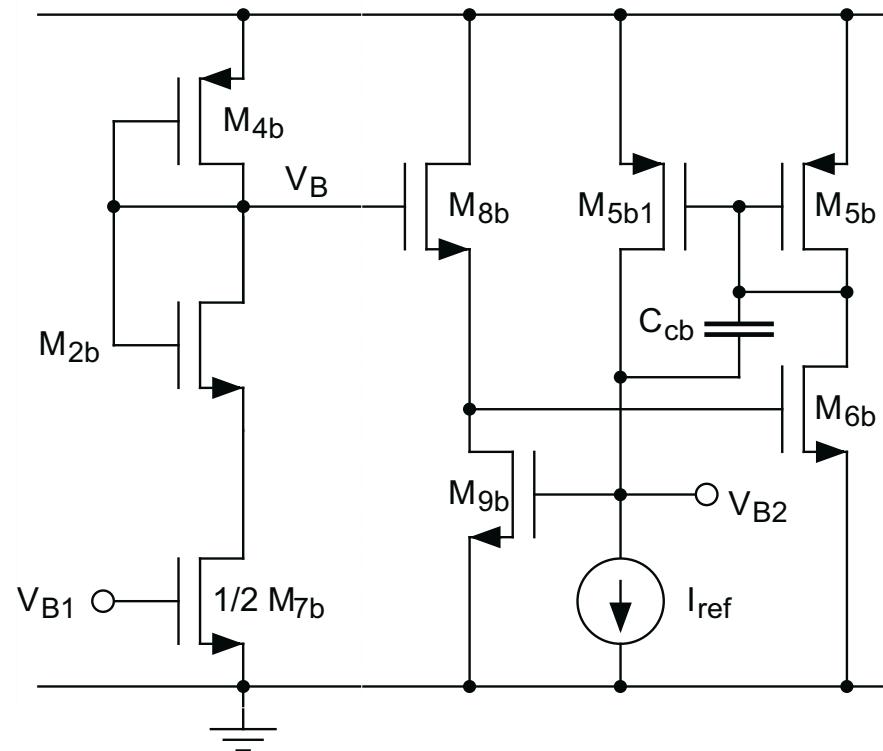
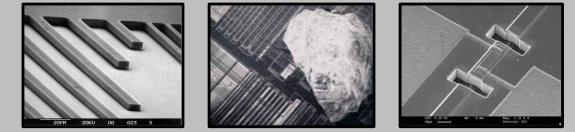
- ❖ Transistors M_{7b} , M_{2b} , and M_{4b} match half of the first stage, replicating at node V_B the voltage at the gate of M_8
- ❖ Voltage V_B is used to bias M_{8b} (a replica of M_8)

TWO-STAGE CLASS AB OP-AMP



- ❖ The current mirror M_{5b1} - M_{5b} copies the current of M_{6b} (replica of M_6) which is compared with the reference current I_{ref} , producing the voltage V_{B2} that will be used to control M_9
- ❖ The negative feedback loop ensures that $I_{6,b}$ (and, hence, $I_{5,6}$) is equal to I_{ref}

TWO-STAGE CLASS AB OP-AMP

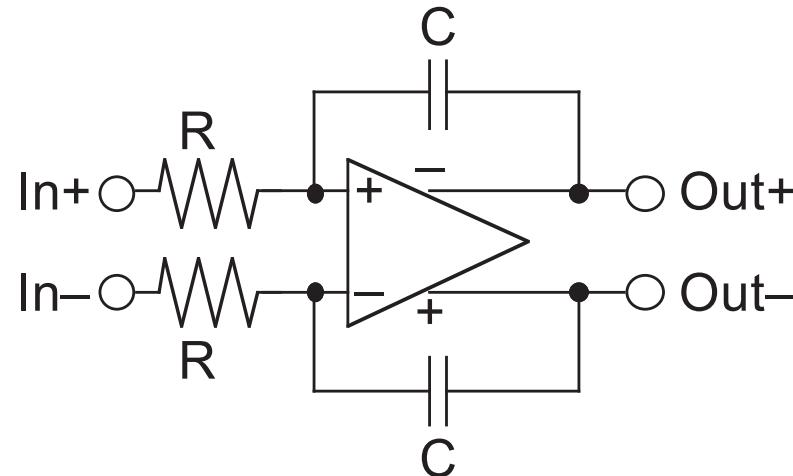
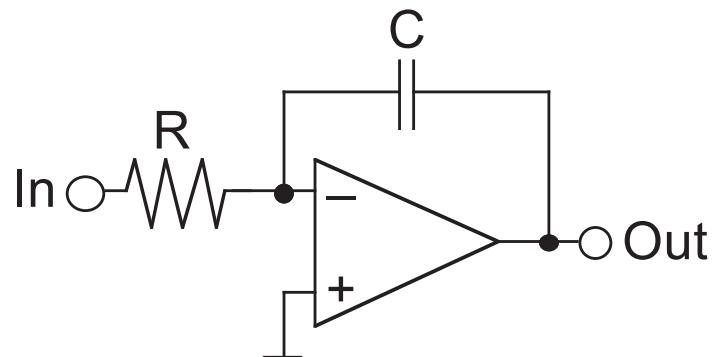


- ❖ There are three stages in the loop. To ensure the stability, a compensation capacitor C_{cb} is required
- ❖ Eventually, the currents in the replica circuit can be scaled to reduce the power consumption

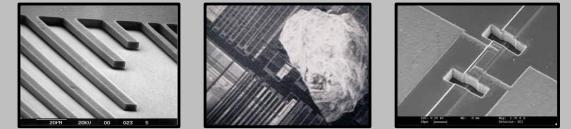
FULLY DIFFERENTIAL OP-AMPS: PROS



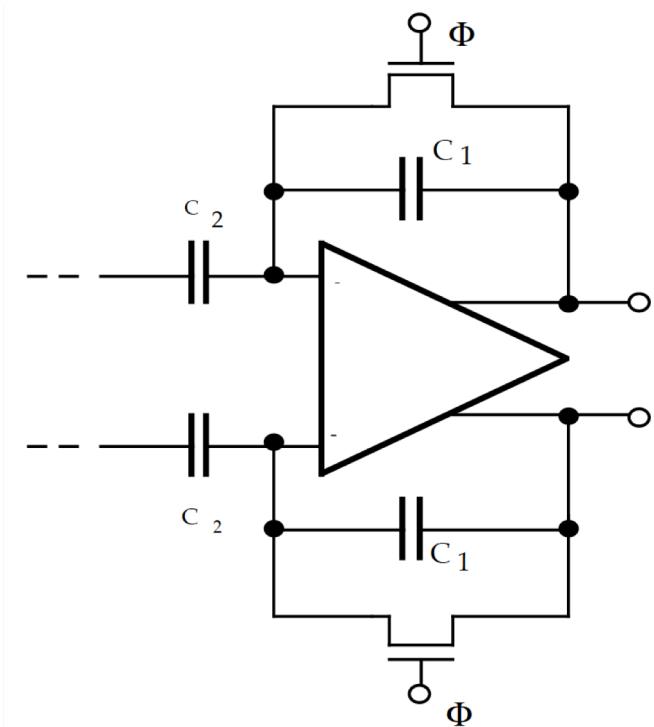
- ❖ A fully differential solution rejects all the common mode components that we have at the input
- ❖ Rejection of disturbances (treated as common mode signals)
- ❖ Better power supply rejection ratio (PSRR)
- ❖ Reduction of clock-feedthrough
- ❖ The output swing is doubled ($V_{max+} - V_{max-} = 2V_{max}$). Since the noise is unchanged, the dynamic range improves by 6 dB



FULLY DIFF for CLK FEEDTHROUGH



- ❖ Fully differential schemes elaborate the signal twice using two complementary paths. The advantage is that any common mode variation cancels the other and will not affect the result.
- ❖ Fully differential amplifiers are capable of providing two complementary outputs.
- ❖ Switching off the two transistors across C_1 produces an injection of charge in the two op-amp inputs. It is a common mode signal, rejected by the circuit operation.

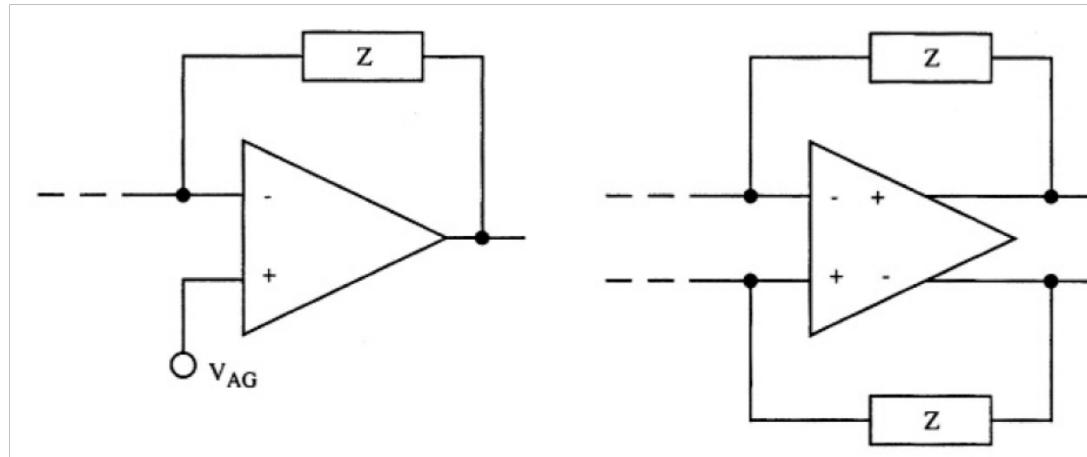


FULLY DIFFERENTIAL OP-AMPS: CONS



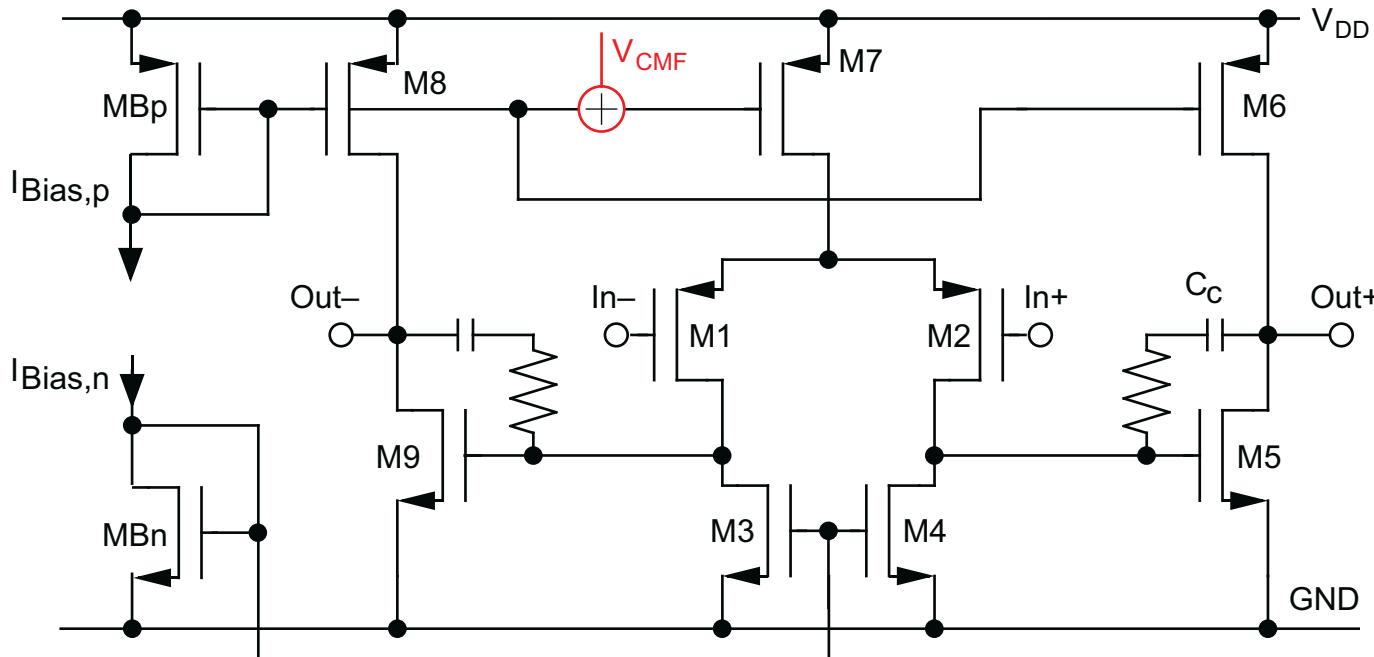
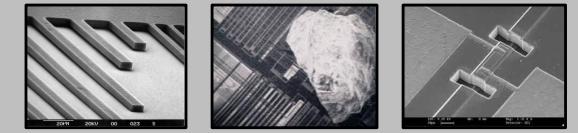
- ❖ Need of single-ended to double-ended and double-ended to single-ended converters
- ❖ Larger area (all passive components are required twice)
- ❖ Increase in the power consumption
- ❖ Need of larger number of bias lines
- ❖ The feedback around the op-amp controls the difference of the input terminal voltages and not their mean value. In turn, there is no control of the output common mode voltage
- ❖ Need of a common-mode feedback circuit

COMMON-MODE FEEDBACK



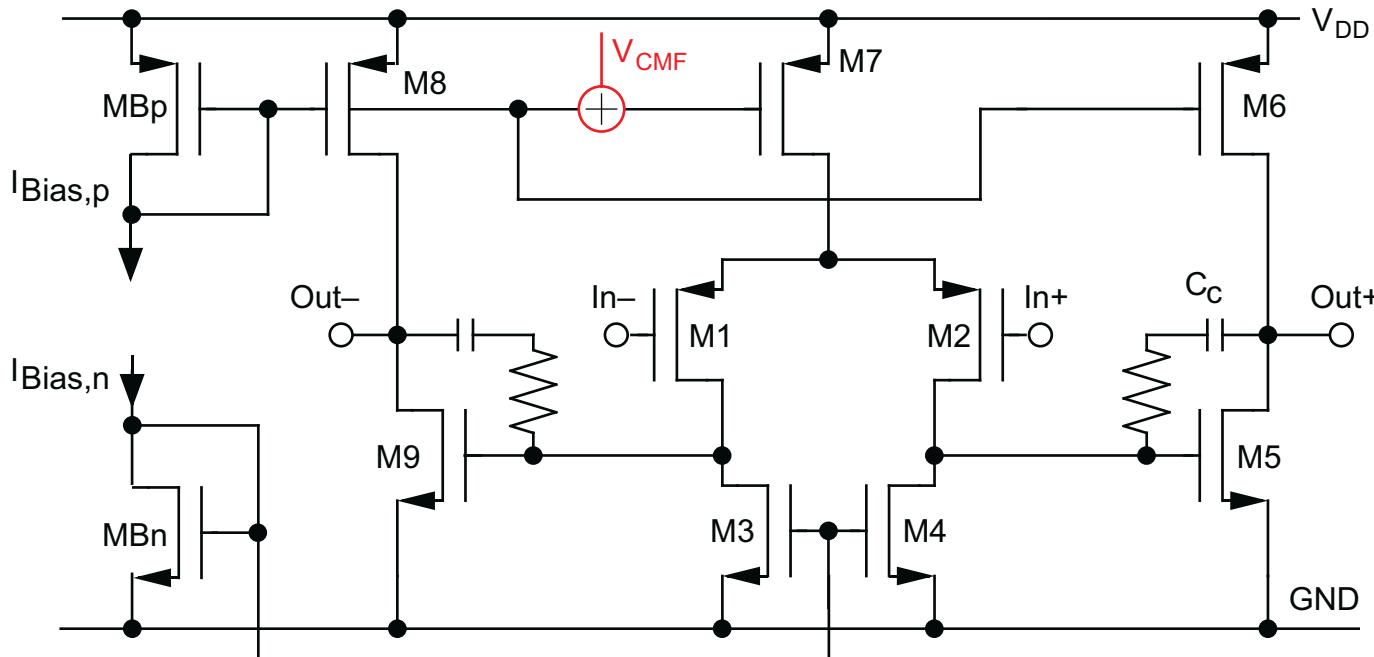
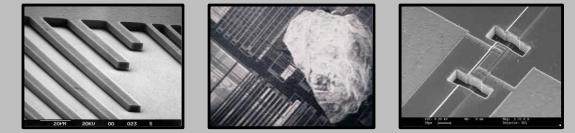
- ❖ SE circuit has the non-inverting terminal connected to V_{AG} . If the voltage gain is (very) high we have that the inverting terminal is virtually connected to the non-inverting one. In addition, the feedback links inverting terminal to output. The biasing of the non-inverting terminal fixes either the input and output common mode
- ❖ In fully diff scheme, there are no connection to V_{AG} . If the gain is high, the input differential input is small, but there is no condition determining the input and output common mode

TWO-STAGE FULLY DIFFERENTIAL OP-AMP



- ❖ The differential to single ended conversion achieved with M_4 diode connected has been removed. M_3 and M_4 work as an active load
- ❖ Two second stages with zero nulling compensation networks complete the scheme
- ❖ It requires one additional bias voltage for the gates of M_3 and M_4

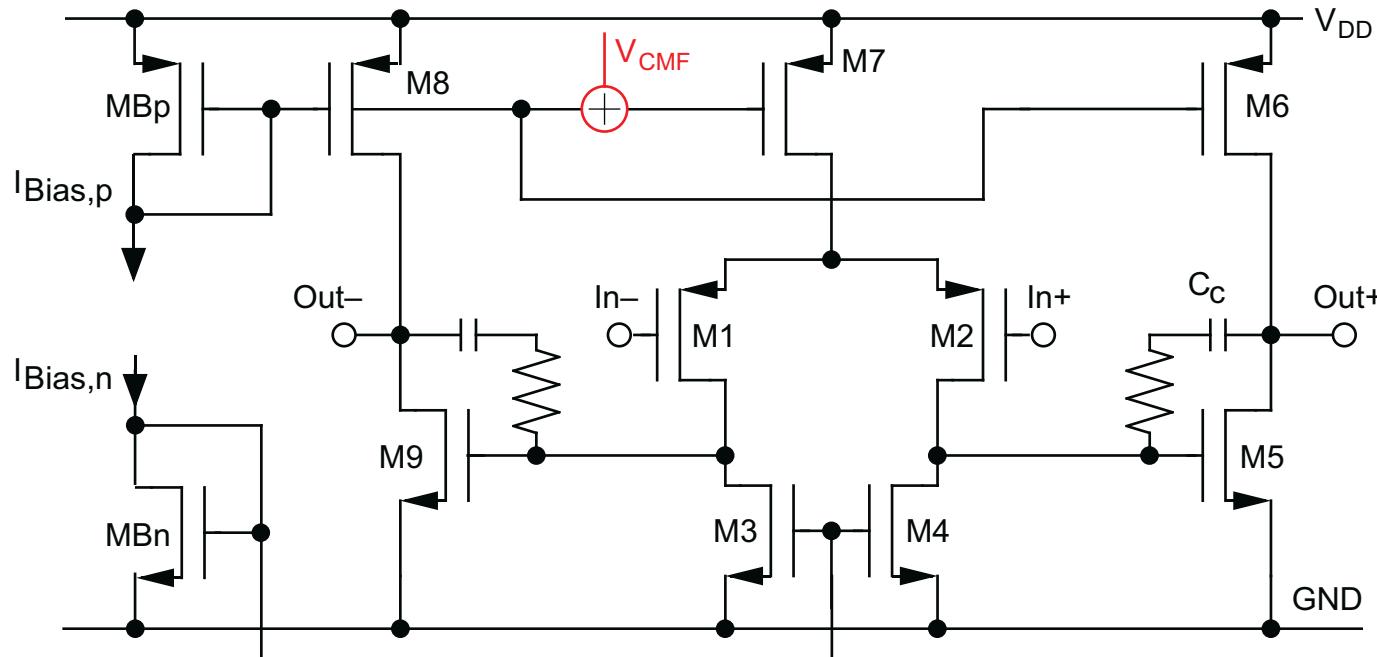
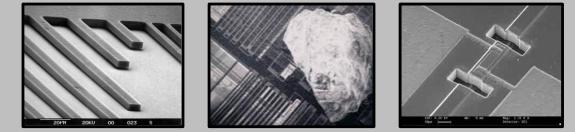
TWO-STAGE FULLY DIFFERENTIAL OP-AMP



$$A_1 = \frac{1}{2} \frac{g_{m1,2}}{g_{ds1,2} + g_{ds3,4}}, \quad A_2 = \frac{g_{m5,9}}{g_{ds5,9} + g_{ds6,8}}, \quad A_d = \frac{V_{out}^+ - V_{out}^-}{V_{in}^+ - V_{in}^-} = 2A_1A_2$$

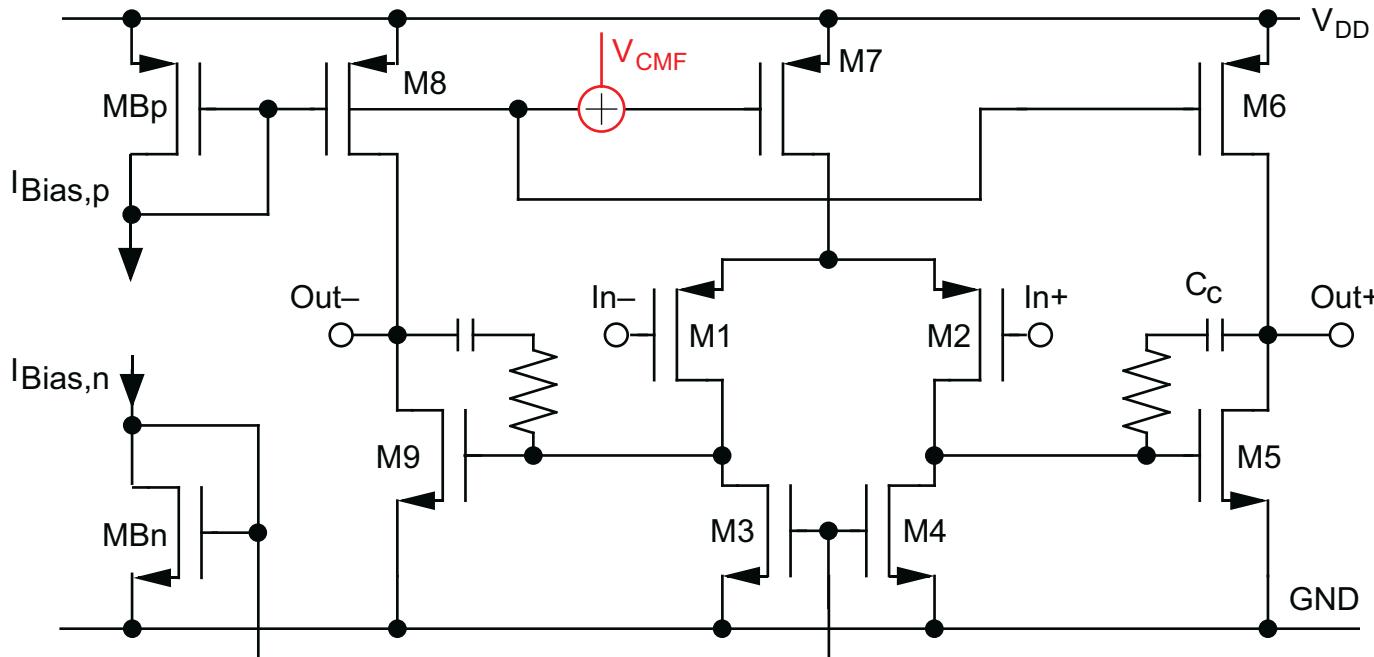
- ❖ A proper operation requires to balance quiescent currents in PMOS and NMOS. M_6 and M_8 need to match currents in M_5 and M_9 . Current in M_7 should match the sum of the currents in M_3 and M_4 .

TWO-STAGE FULLY DIFFERENTIAL OP-AMP



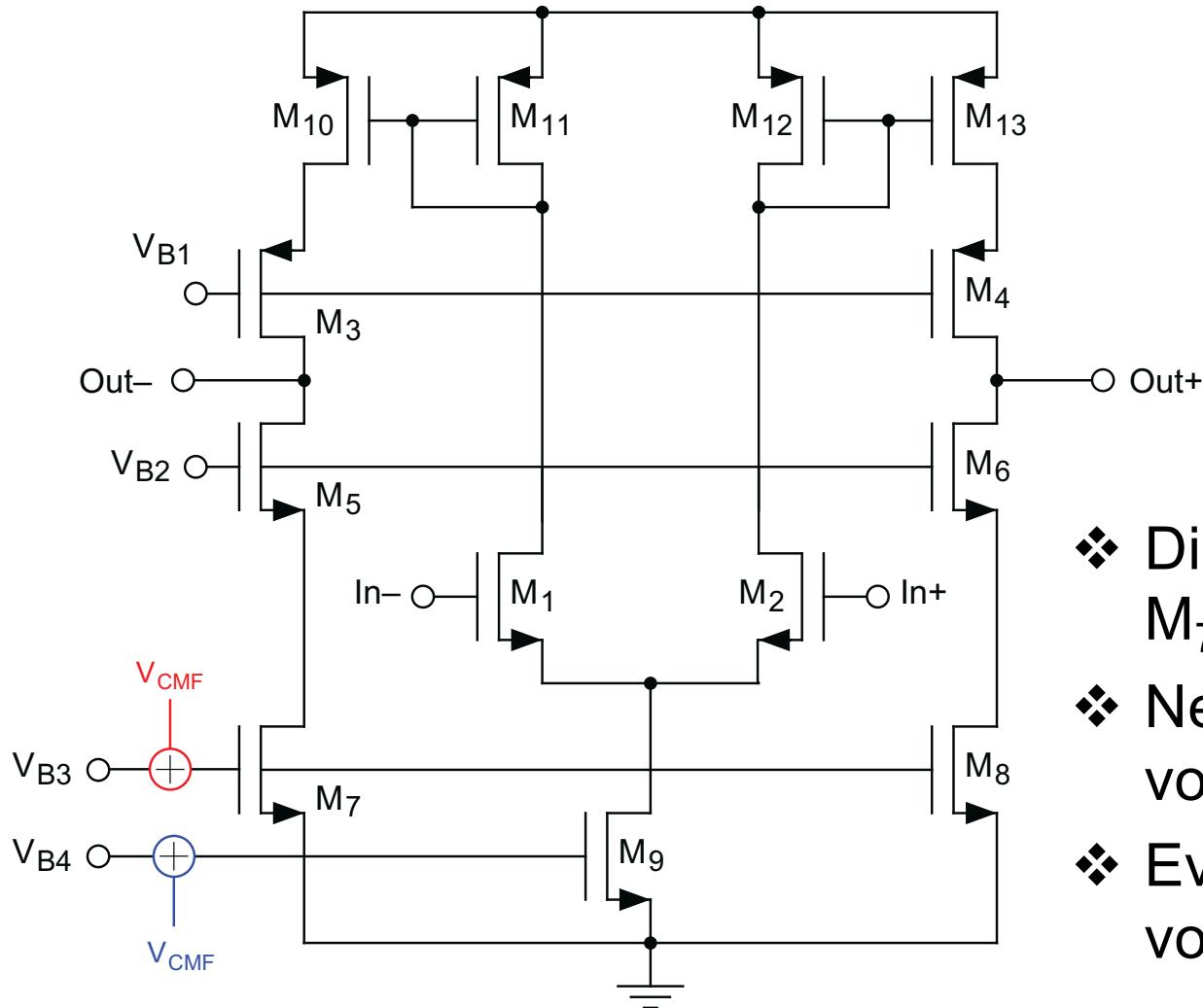
- ❖ Mismatches between current references and mirror factors prevent achieving this fitting
- ❖ Use *common mode feedback*: it detects the average value of the output voltages, compares it with a desired level and produces a control signal that, in feedback, regulates one of the currents that we want to match

TWO-STAGE FULLY DIFFERENTIAL OP-AMP



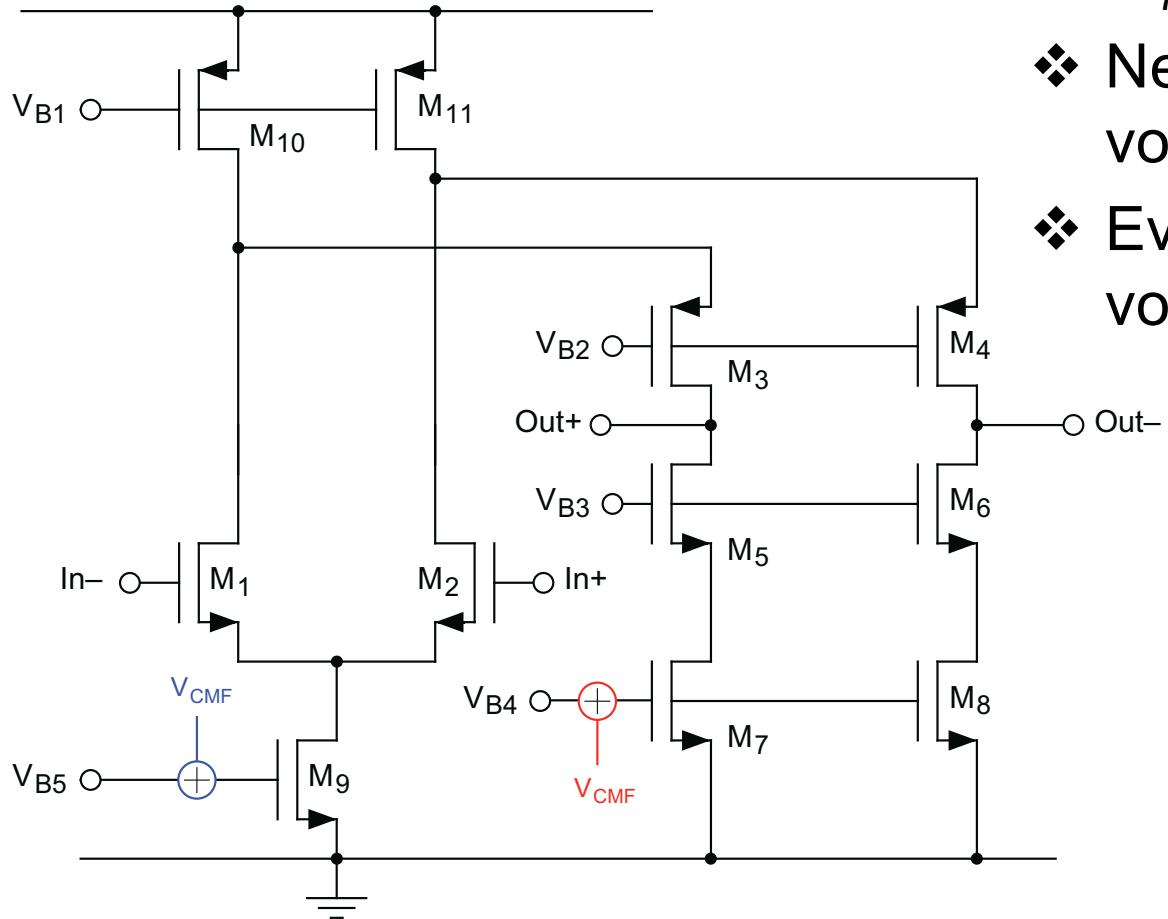
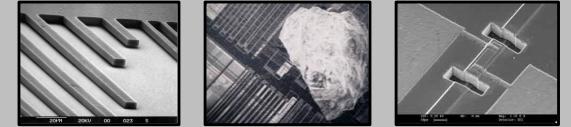
- ❖ Suppose that the current drained by M_8 and M_6 are lower than the ones in M_9 and M_5 . The common mode output voltage would drop and the circuit will not operate properly.
- ❖ V_{CMF} augments such as to diminish the overdrive of M_7 , reducing the current in the input stage. Drains of M_3 and M_4 diminish such as currents in M_5 and M_9 diminish till desired matching is achieved

MIRRORED CASCODE FULLY DIFF



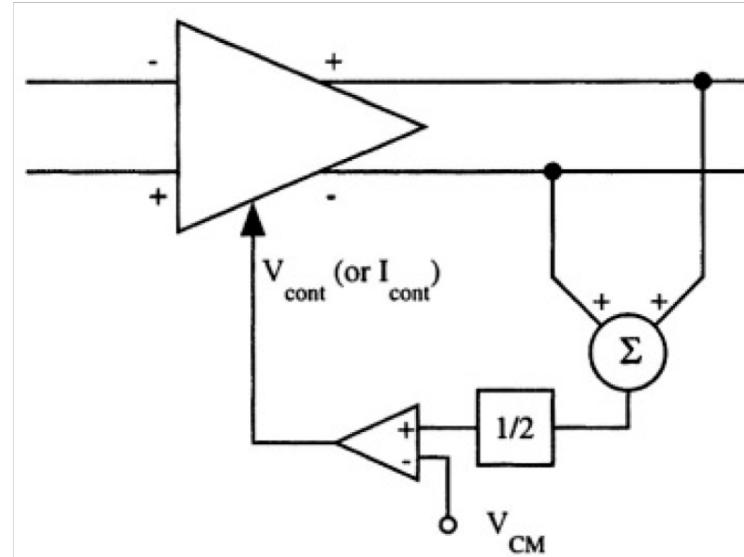
- ❖ Diode connection of M₅ and M₇ have been removed
- ❖ Need of additional bias voltages
- ❖ Eventually use the same voltage to bias M₇, M₈, and M₉

FOLDED CASCODE FULLY DIFF



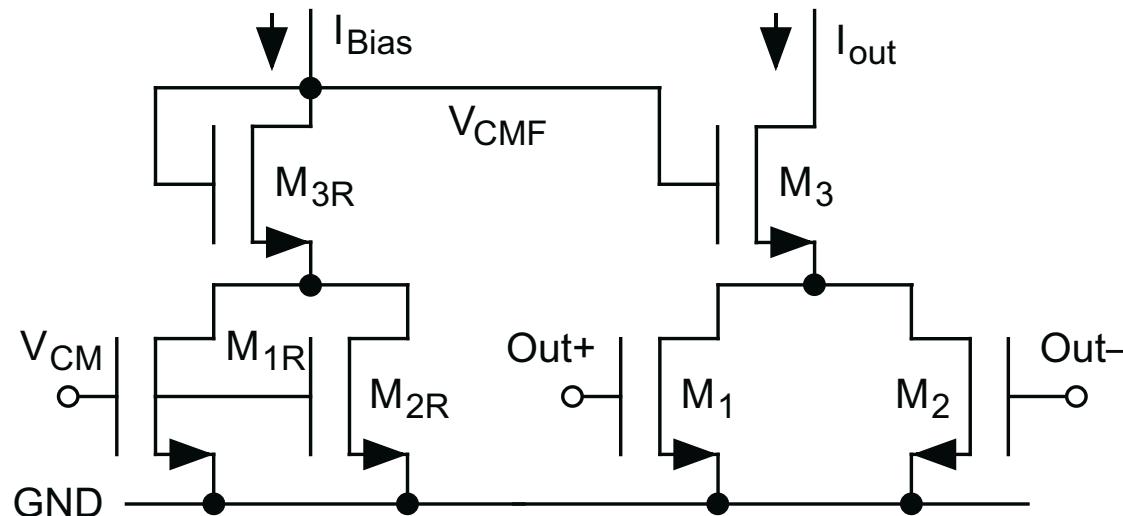
- ❖ Diode connection of M_5 and M_7 have been removed
 - ❖ Need of additional bias voltages
 - ❖ Eventually use the same voltage to bias M_7 , M_8 , and M_9

COMMON-MODE FEEDBACK



- ❖ The adder and the $1/2$ amplifier determine the common mode output
- ❖ The other block compares the result with the desired common mode level. The possible error (eventually amplified) controls in feedback a suitable node in the fully differential amplifier
- ❖ The common mode feedback can be continuous-time (CT) or switched-capacitor (SC)
- ❖ Stability of the common mode feedback needs to be verified

CT COMMON-MODE FEEDBACK



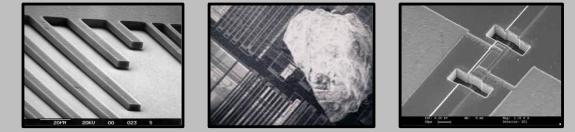
❖ M_1, M_2, M_{1R} , and M_{2R} are equal and operated in triode region

$$I_1 = \frac{1}{2} k' \left(\frac{W}{L} \right)_{1,2} \left[2 (V_{out}^+ - V_{th,1,2}) V_{DS1,2} - V_{DS1,2}^2 \right]$$

$$I_2 = \frac{1}{2} k' \left(\frac{W}{L} \right)_{1,2} \left[2 (V_{out}^- - V_{th,1,2}) V_{DS1,2} - V_{DS1,2}^2 \right]$$

$$I_{1R} = I_{2R} = \frac{1}{2} k' \left(\frac{W}{L} \right)_{1,2} \left[2 (V_{CM} - V_{th,1,2}) V_{DS1R,2R} - V_{DS1R,2R}^2 \right]$$

CT COMMON-MODE FEEDBACK



- ❖ Assuming $I_{Bias} \approx I_{out}$ and hence $V_{DS1,2} \approx V_{DS1R,2R} = V_{DS}$

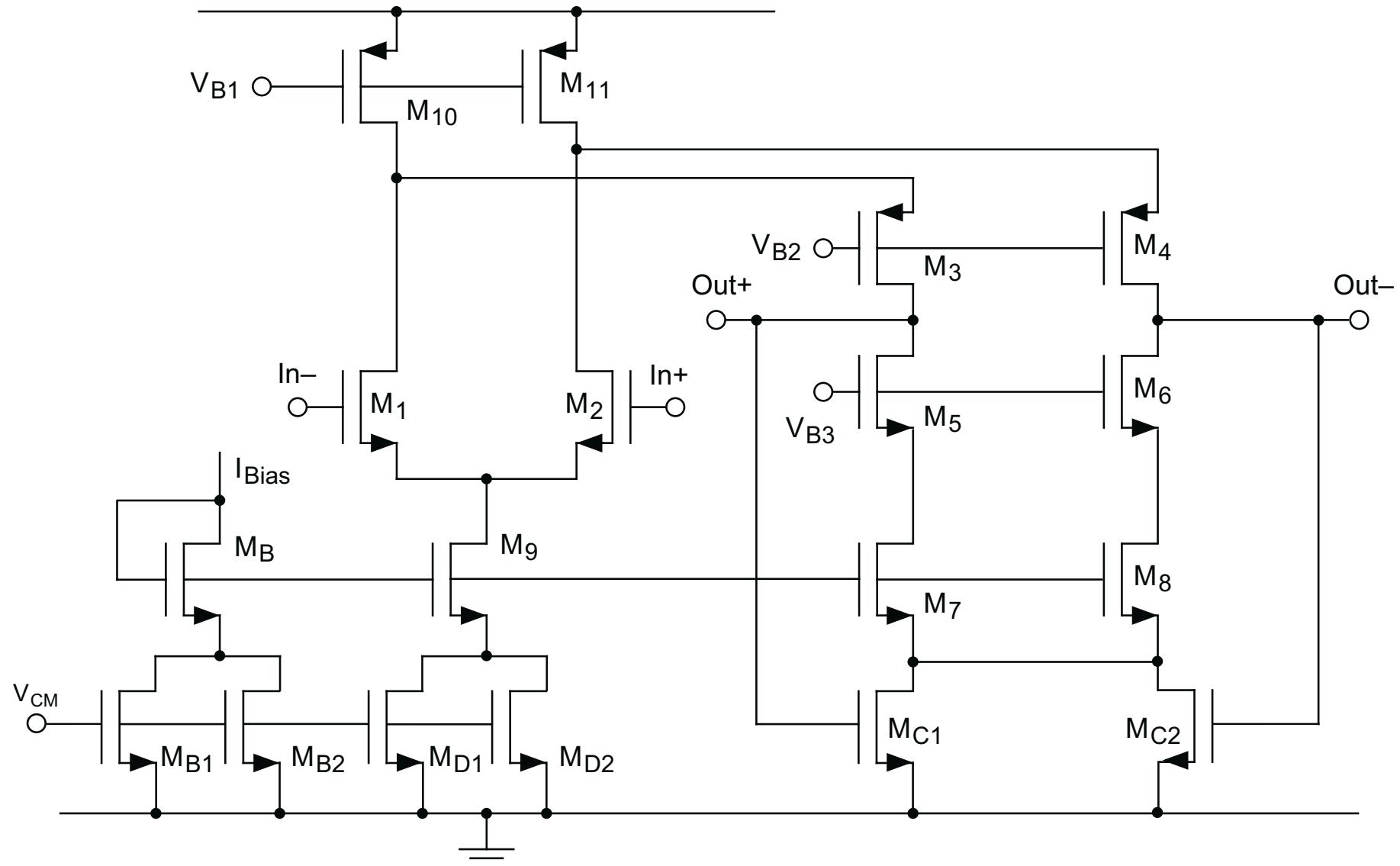
$$I_{out} = I_1 + I_2 = I_{Bias} + 2k' \left(\frac{W}{L} \right)_{1,2} V_{DS} \left(\frac{V_{out}^+ + V_{out}^-}{2} - V_{CM} \right)$$

- ❖ The achieved transconductance gain is:

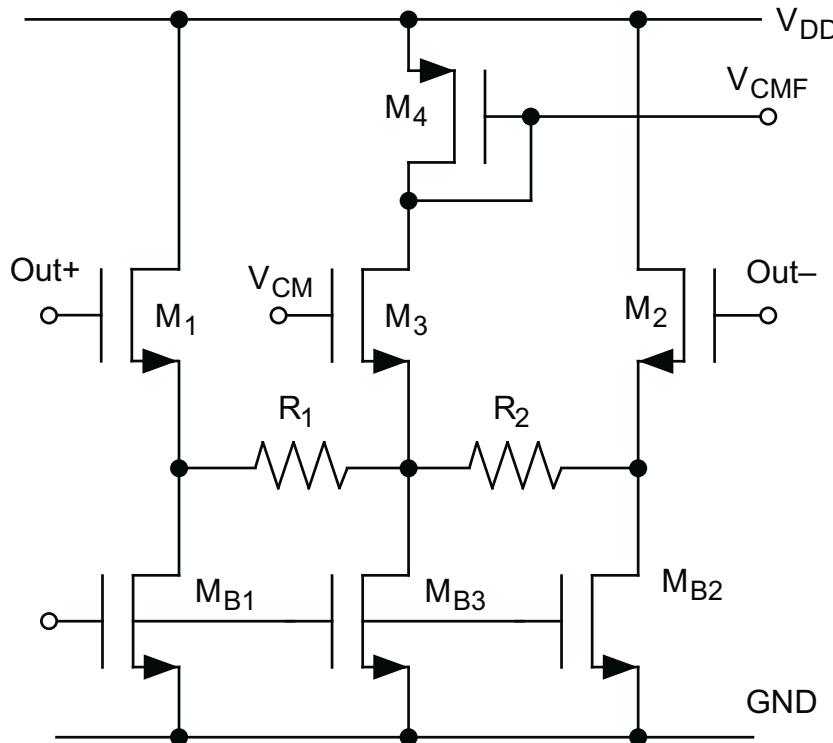
$$g_m = 2k' \left(\frac{W}{L} \right)_{1,2} V_{DS}$$

- ❖ Since M_1 , M_2 , M_{1R} , and M_{2R} are in the triode region, the loop gain of the common-mode feedback is low
- ❖ The comparison between V_{CM} and $(V_{out}^+ + V_{out}^-)/2$ is achieved by symmetry between $M_{1,2}$ and $M_{1R,2R}$. The circuit is not actually performing the difference $V_{CM} - (V_{out}^+ + V_{out}^-)/2$

FOLDED CASCODE with CT CMF

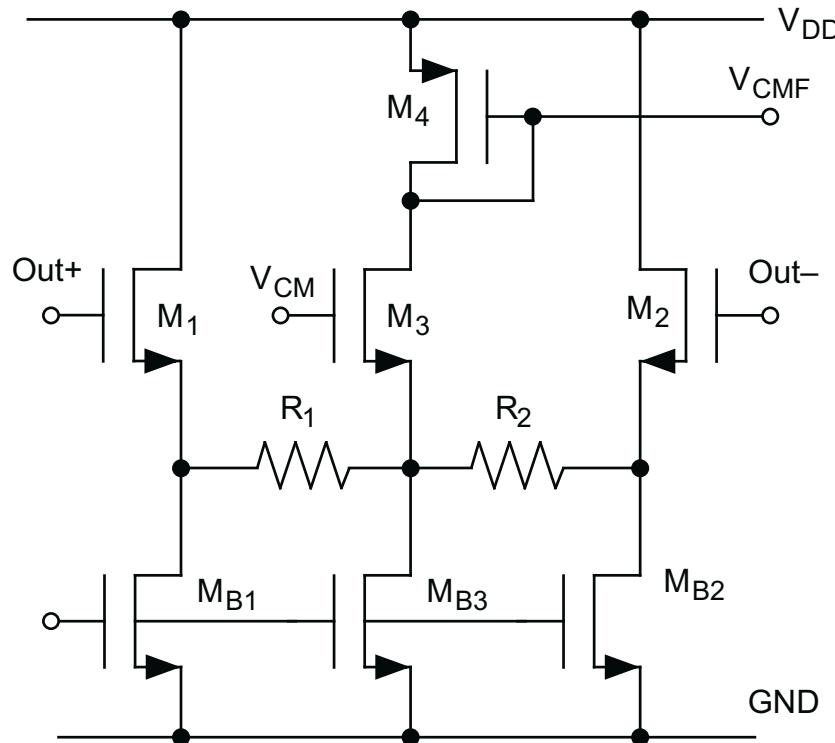


CT COMMON-MODE FEEDBACK



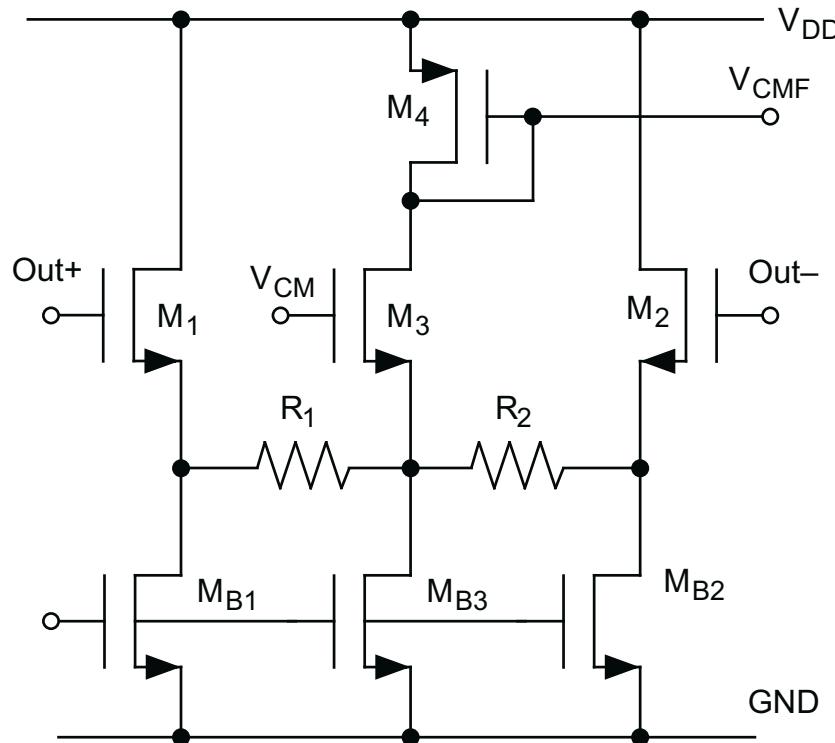
- ❖ Three source followers shift down the two outputs and the desired common mode voltage. R_1 and R_2 are equal. If the three gate voltages are equal, no current will flow on the resistors.

CT COMMON-MODE FEEDBACK



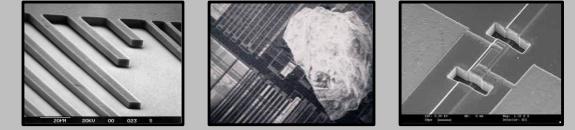
- An output common mode change (for example in the positive direction) causes two equal currents flowing out from the source of M₁ and M₂. These currents will cause a decrease of the current in M₃ (and M₄).

CT COMMON-MODE FEEDBACK

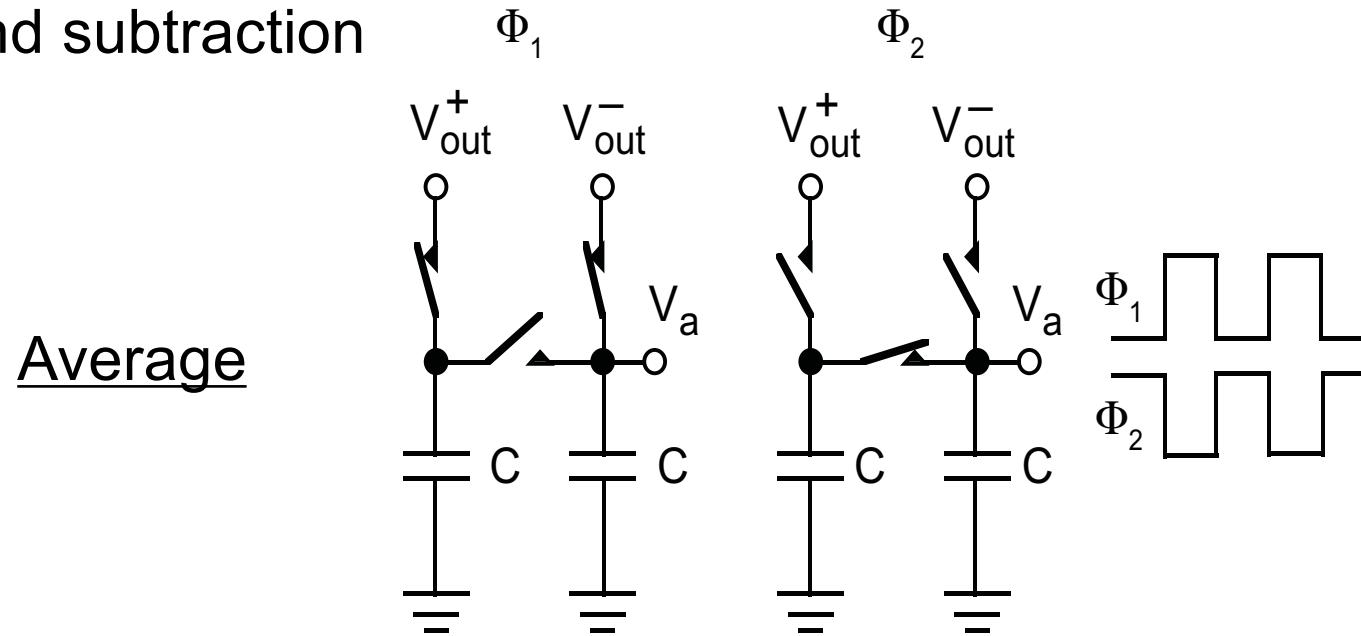


- ❖ A differential signal induces a balanced swing at the sources of M₁ and M₂. A current proportional to the differential signal flows from source of M₁ to source of M₂ without affecting the branch in the middle.

SC COMMON-MODE FEEDBACK

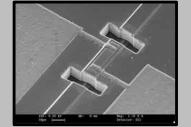
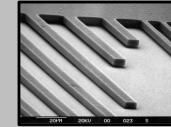


- ❖ With switches and capacitors it is possible to implement the two functions required by a common-mode feedback circuit: average and subtraction

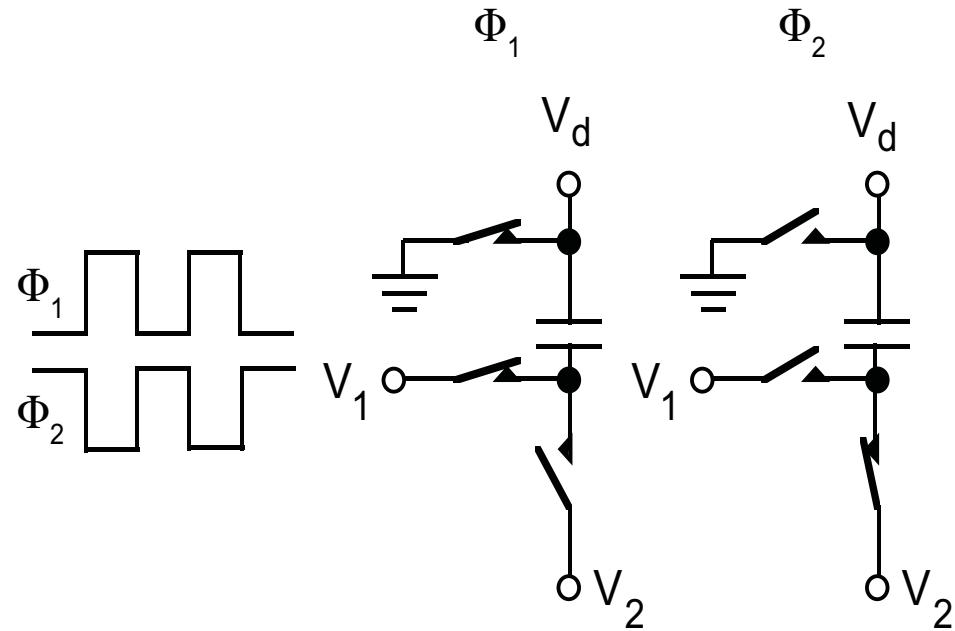


$\Phi_1 \rightarrow$ The two capacitors C are charged to V_{out}^+ and V_{out}^-
 $\Phi_2 \rightarrow$ The two capacitors C are connected in parallel

$$V_a = \frac{CV_{out}^+ + CV_{out}^-}{2C} = \frac{1}{2} (V_{out}^+ + V_{out}^-)$$



Subtraction

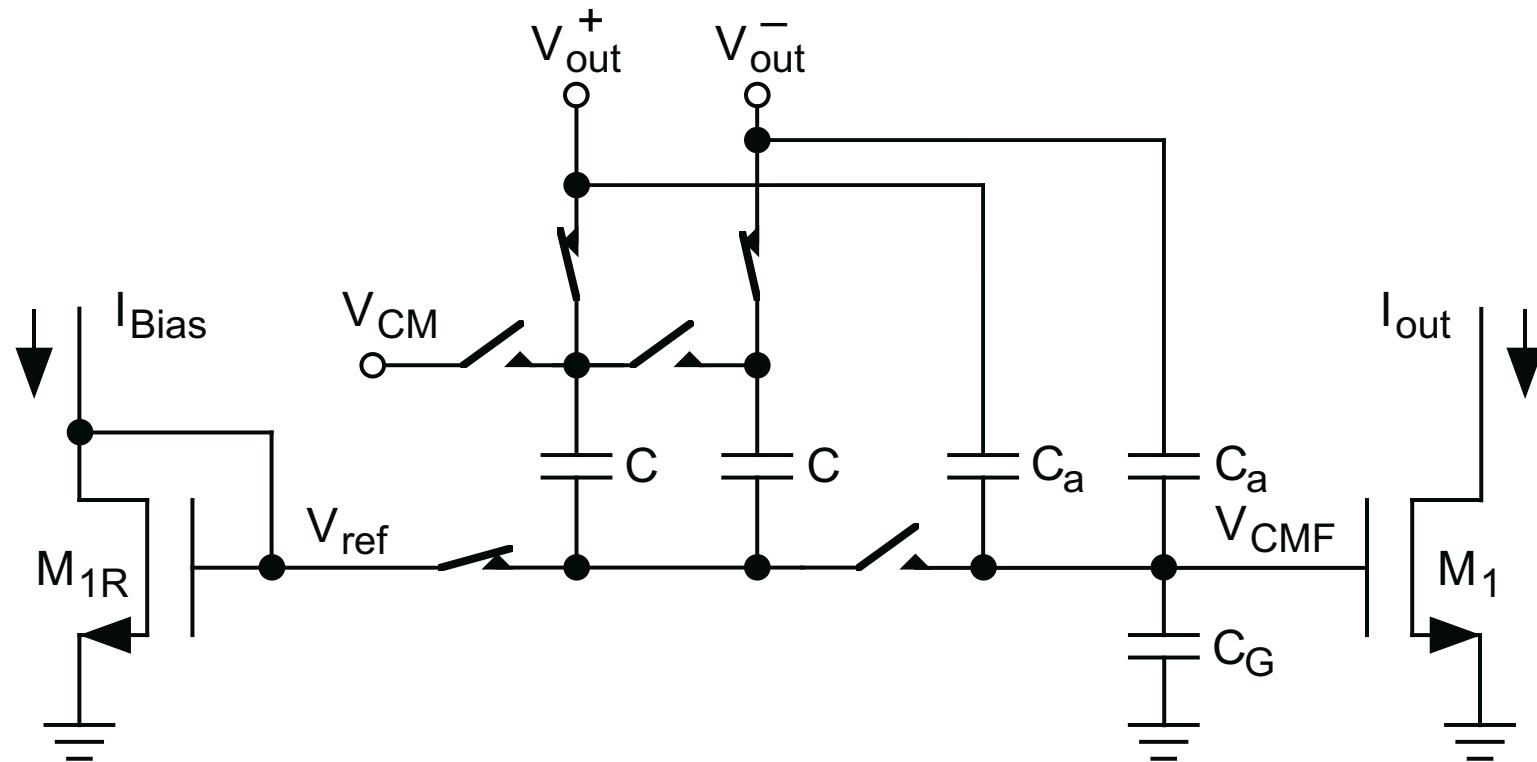


$\Phi_1 \rightarrow$ The capacitor is charged to V_1

$\Phi_2 \rightarrow V_2$ is connected to the capacitor

$$V_d = V_2 - V_1$$

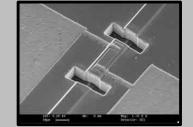
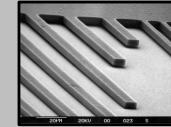
SC COMMON-MODE FEEDBACK



$\Phi_1 \rightarrow$ The two capacitors C are charged to $V_{out}^+ - V_{ref}$ and $V_{out}^- - V_{ref}$

$\Phi_2 \rightarrow$ The two capacitors C are connected in parallel between V_{CM} and V_{CMF}

SC COMMON-MODE FEEDBACK



If $(V_{out}^+ + V_{out}^-)/2 = V_{CM}$ then $V_{CMF} = V_{ref} \rightarrow I_{out} = I_{Bias}$

If $(V_{out}^+ + V_{out}^-)/2 > V_{CM}$ then $V_{CMF} < V_{ref} \rightarrow I_{out} < I_{Bias}$

If $(V_{out}^+ + V_{out}^-)/2 < V_{CM}$ then $V_{CMF} > V_{ref} \rightarrow I_{out} > I_{Bias}$

$$V_{CMF} = V_{ref} - \frac{V_{out}^+ + V_{out}^-}{2} + V_{CM}$$

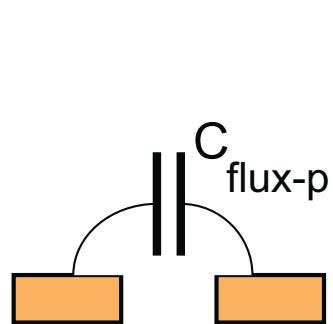
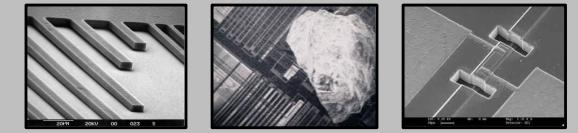
- ❖ The circuit behaves as a SC network whose function is equivalent to an RC low-pass filter
- ❖ The SC common-mode feedback is a sampled-data system. It is effective for frequencies up to half of the clock frequency. It does not react to instantaneous changes of the output voltage.
- ❖ Capacitors C_a , besides holding V_{CMF} , introduce a high-speed path for the common-mode feedback between the outputs and V_{CMF}

GENERAL LAYOUT GUIDELINES

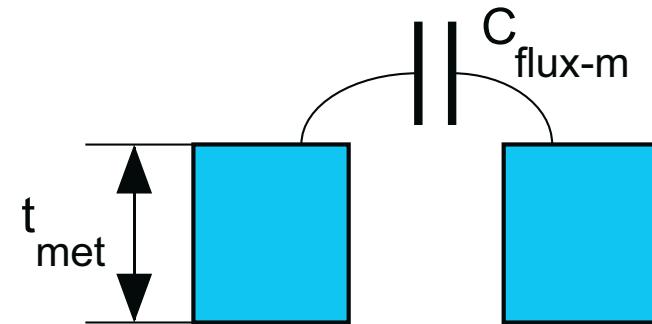


- ❖ Respect in the layout the symmetry of the circuits at the electrical level. This leads to low sensitivity to disturbances and matching of parasitics
- ❖ Ensure that transistors supposed to be equal or assumed to have a given aspect ratio match at the geometrical and technological level (use dummy devices if necessary)
- ❖ Minimize or match the parasitic voltage drops across interconnections
- ❖ Obtain balanced paths in signal interconnections
- ❖ Avoid (or minimize when unavoidable) capacitive couplings, especially when high-impedance nodes are involved
- ❖ Use interdigitated or, even better, common-centroid structures where matching is required
- ❖ Use always the same orientation for devices that have to be matched

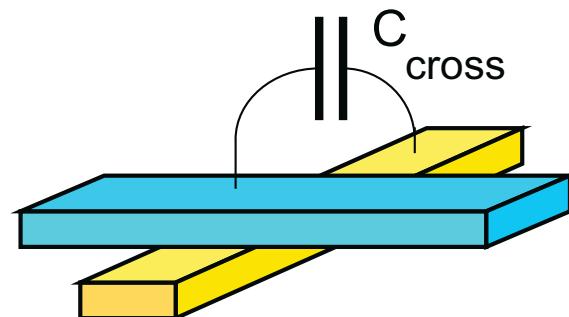
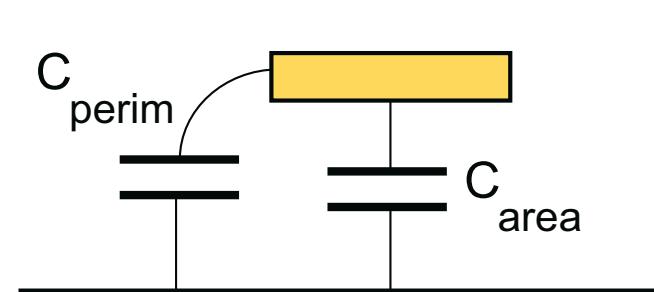
PARASITIC EFFECTS



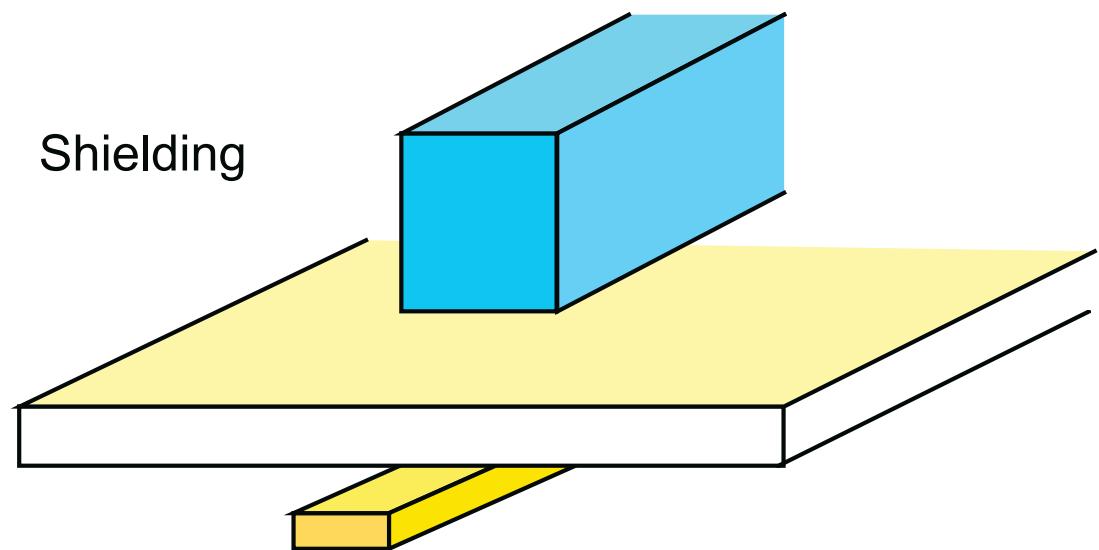
Poly-poly



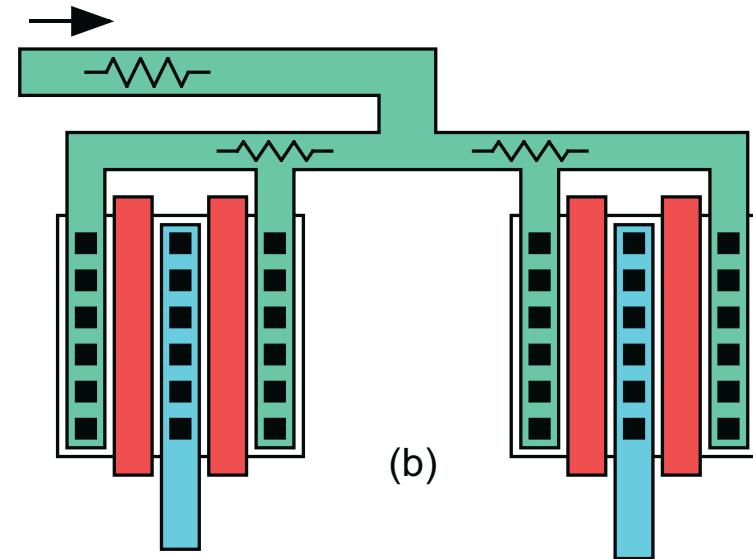
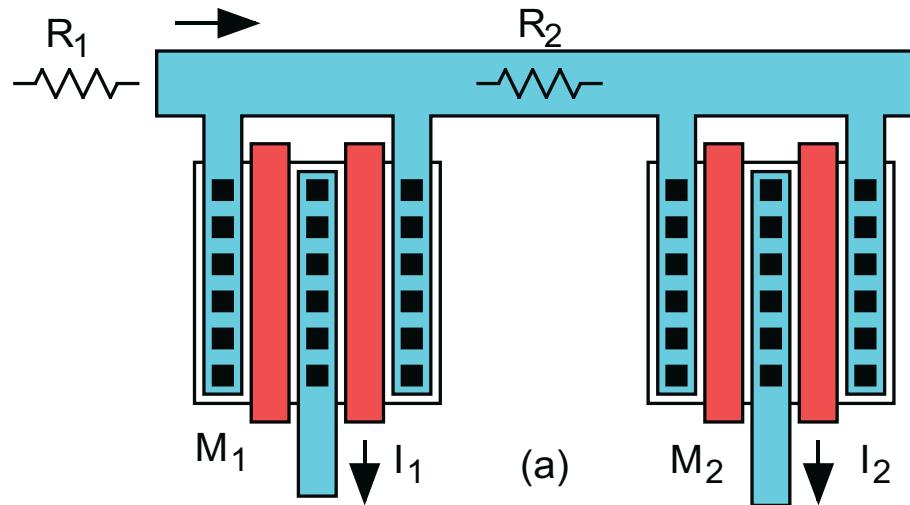
Metal-metal



Cross



INTERCONNECTIONS

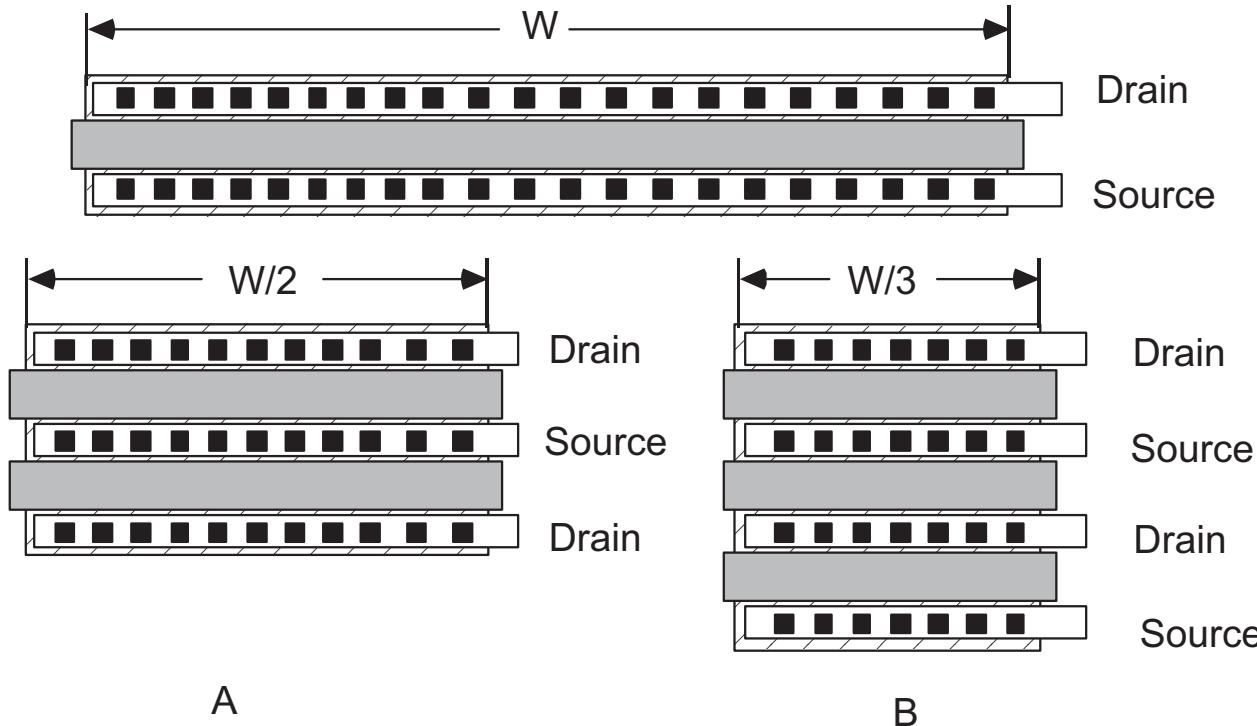


- ❖ With the layout (a) there is a voltage difference between the source of transistor M_1 and the source of transistor M_2 equal to $R_2 I_2$
- ❖ Even if transistors M_1 and M_2 are perfectly matched, there is a given current offset
- ❖ In layout (b), the currents are matched

LAYOUT HINTS



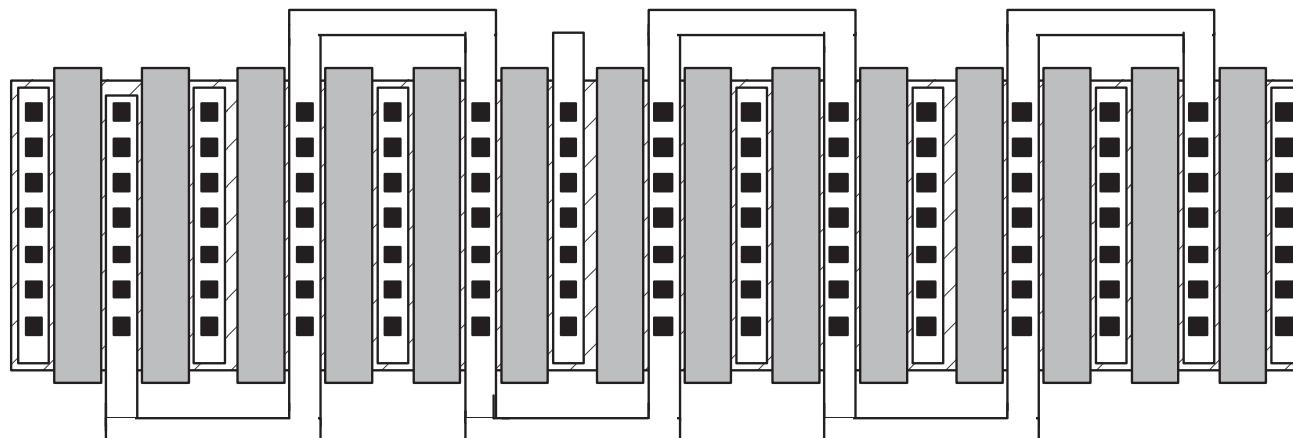
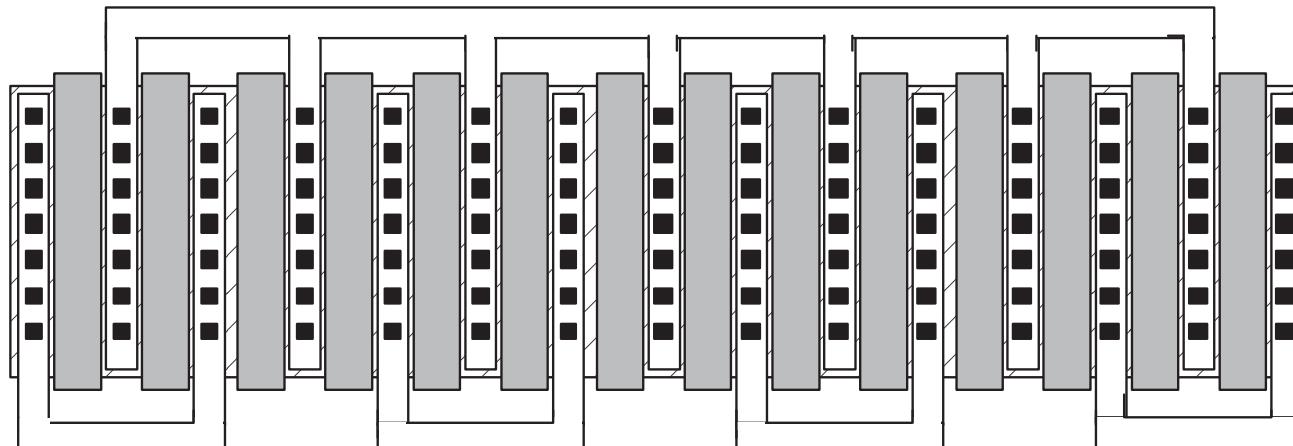
- ❖ The layout of a transistor can be realized as a single finger or with multiple fingers
- ❖ Parasitic capacitances change as a function of the number of fingers
- ❖ Use dummy structures at the edge of the stack to avoid threshold mismatch



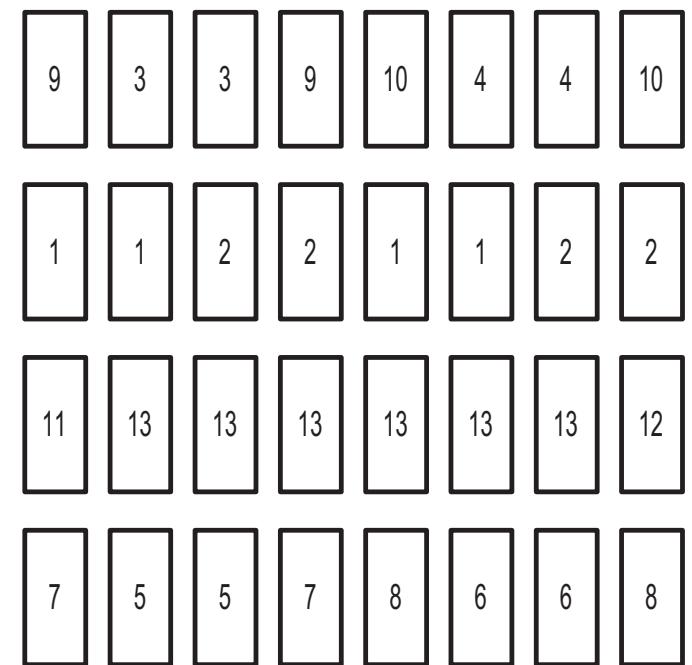
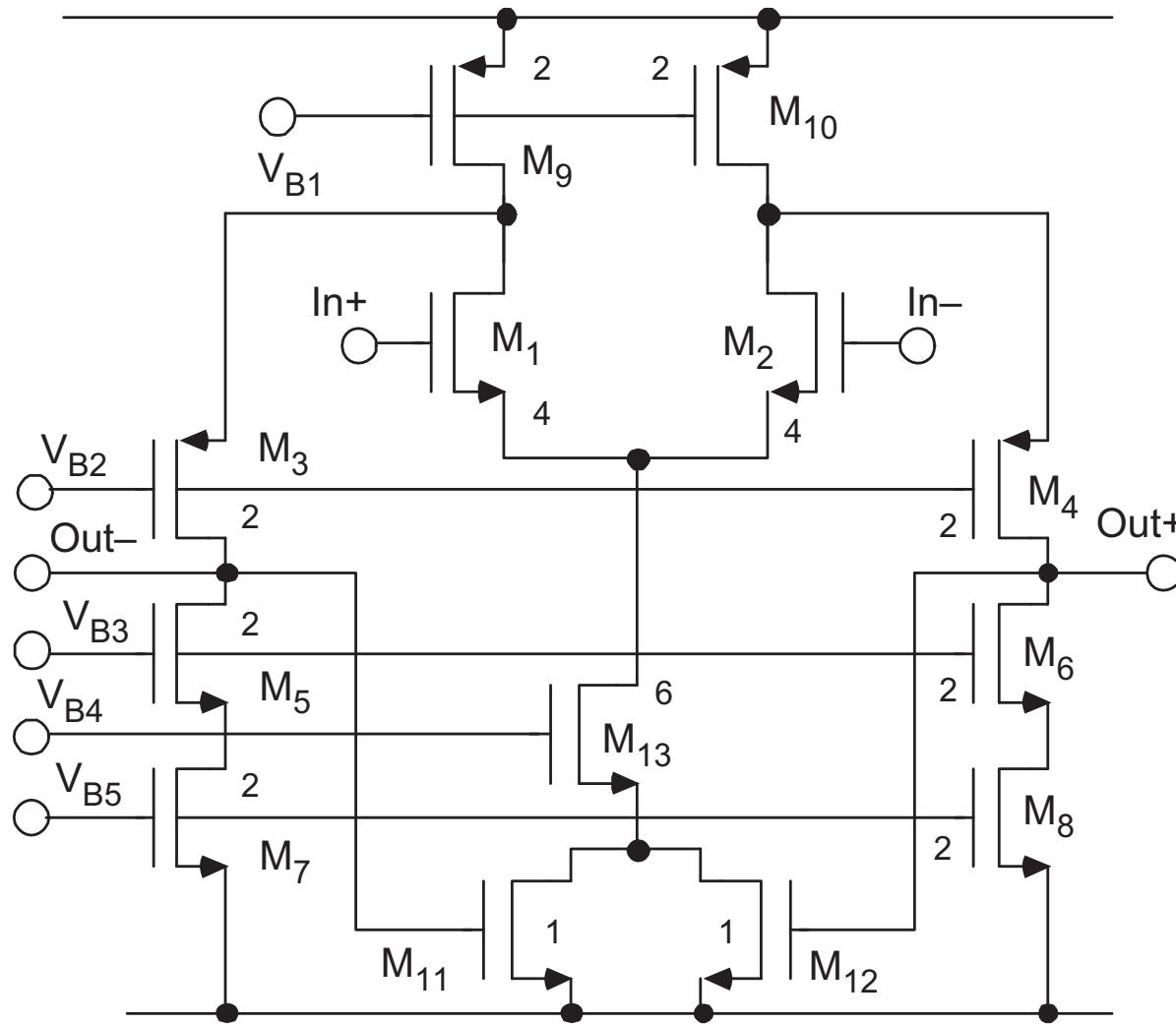
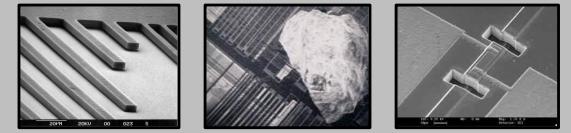
LAYOUT HINTS



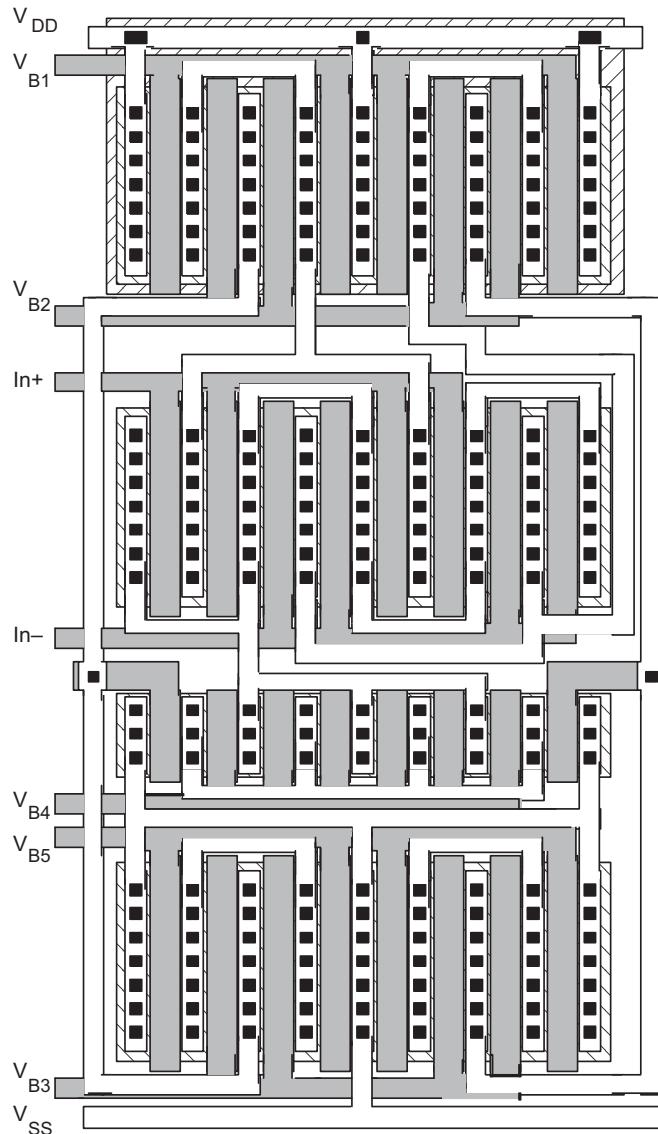
- ❖ For routing, use comb-like or snake-like connections (beware of current density in snake-like connections)



LAYOUT EXAMPLE



LAYOUT EXAMPLE



- ❖ Symmetry maintained
- ❖ Common-centroid differential pair
- ❖ Interdigitated current sources
- ❖ Layout oriented design
- ❖ Minimal parasitics
- ❖ Minimal interconnection length