

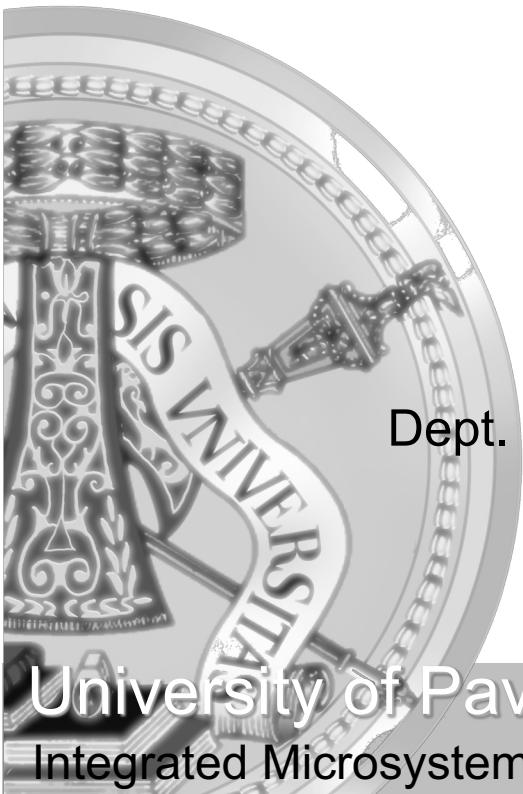


# Basic Building Blocks

Analog Integrated Circuits

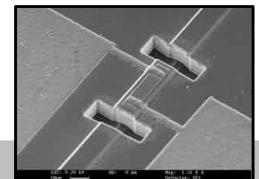
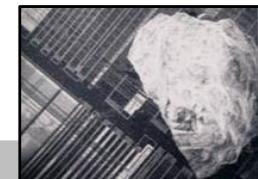
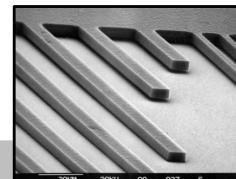
Edoardo Bonizzoni

Dept. of Electrical, Computer, and Biomedical Engineering

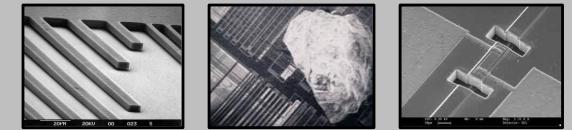


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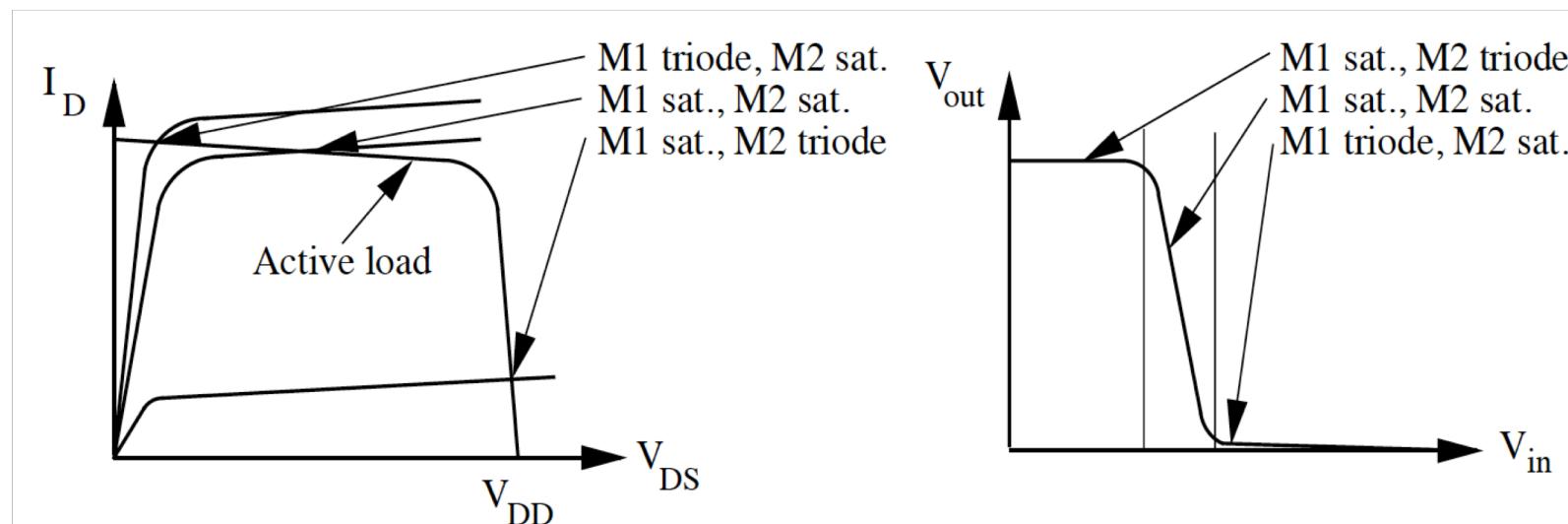
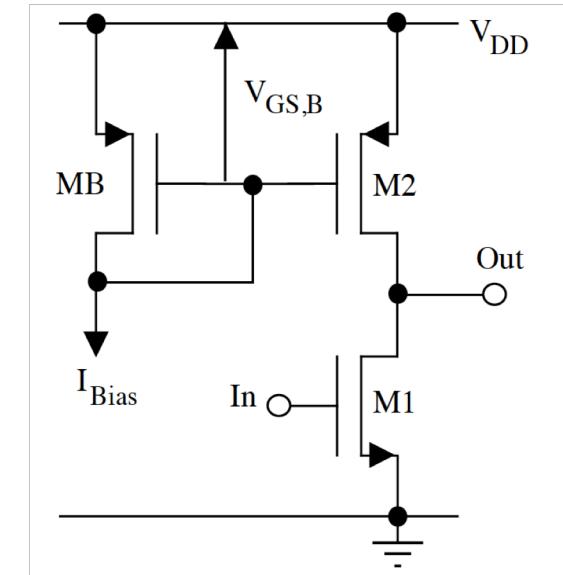
Integrated Microsystems Laboratory



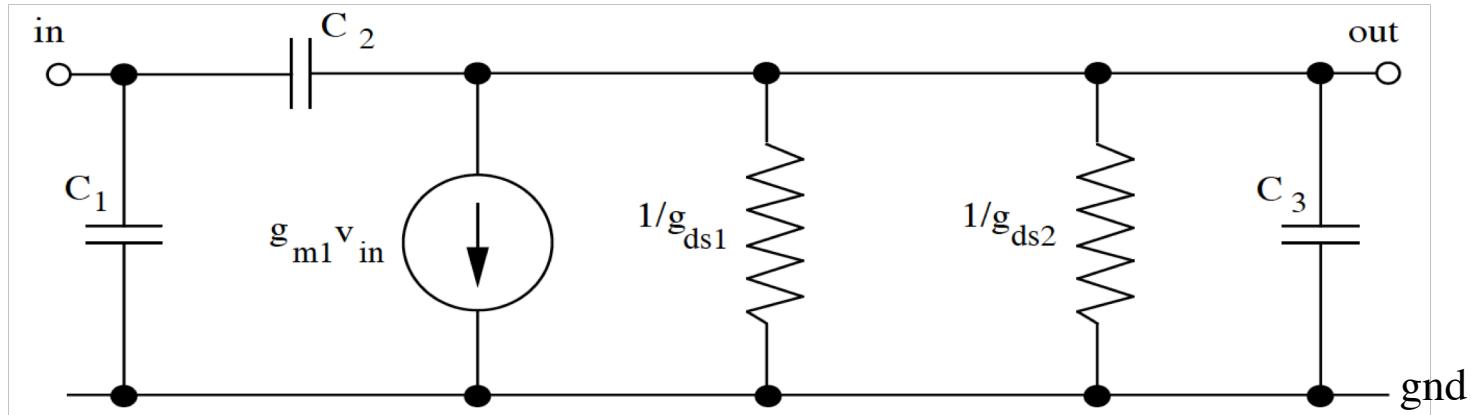
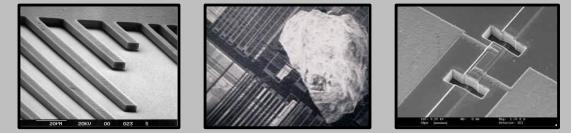
# INVERTER WITH ACTIVE LOAD



- ❖ It is the simplest gain stage. The input signal is applied to only one transistor while the other is biased to a determined voltage (its I-V curve is univocally defined). The DC gain is given by the slope of the transfer characteristic.



# SMALL SIGNAL ANALYSIS



$$C_1 = C_{gs1} + C_{gs1,ov}$$

$$C_2 = C_{gd1} + C_{gd1,ov}$$

$$C_3 = C_{db1} + C_{db2} + C_{gd2} + C_{gd2,ov} + C_L$$

❖ At low frequency, the small signal gain is:

$$A_v = \frac{V_{out}}{V_{in}} = \frac{-g_{m1}}{g_{ds1} + g_{ds2}}$$

# SMALL SIGNAL ANALYSIS



- ❖ Being both transistors in saturation:

$$g_m = \sqrt{2\mu C_{ox} \frac{W}{L} I_D}$$

$$g_{ds} = \lambda I_D$$

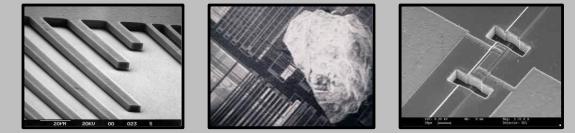
$$A_v = - \frac{\sqrt{2\mu_1 C_{ox} \left(\frac{W}{L}\right)_1}}{\sqrt{I_D} (\lambda_n + \lambda_p)}$$

- ❖ The DC gain increases as the square root of the bias current decreases.
- ❖ If the current is decreased to very low level, the input transistor enters the sub-threshold region.

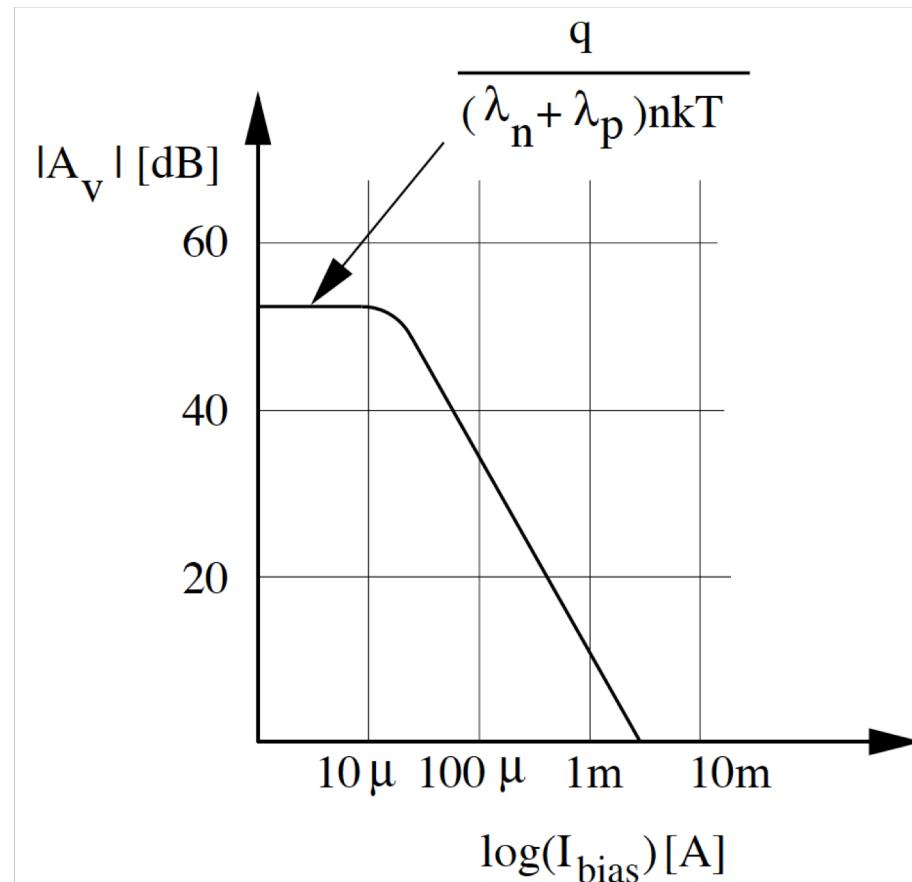
$$g_m = \frac{I_D}{n \frac{kT}{q}}$$

$$A_v = - \frac{1}{n \frac{kT}{q} (\lambda_n + \lambda_p)}$$

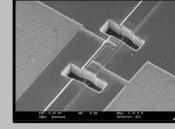
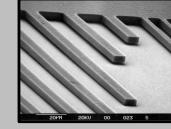
# SMALL SIGNAL ANALYSIS



- ❖ In sub-threshold, the DC gain becomes independent from the biasing current and, for typical CMOS technologies and at room temperature, it is around 50 dB.



# SMALL SIGNAL FREQUENCY RESPONSE

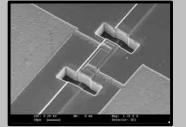
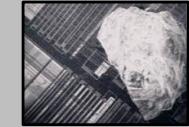
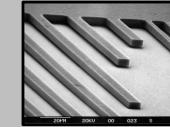


- ❖ Capacitance  $C_2$ , connected between the input and the output of the gain stage, can be decoupled using the Miller's theorem:  $C_2' = C_2(1 - A_v)$  loading the input and  $C_2'' = C_2(1 - 1/A_v)$  loading the output.
- ❖ If  $A_v$  is high enough, the output capacitance is  $C_2 + C_3$ . The output resistance is  $1/(g_{ds1} + g_{ds2})$ .
- ❖ The transfer function has one pole at the angular frequency:

$$\omega_p = \frac{g_{ds1} + g_{ds2}}{C_2 + C_3} = \frac{(\lambda_n + \lambda_p)I_D}{C_2 + C_3}$$

- ❖ The transfer function has also one zero at  $g_{m1}/C_2$ : it is in the right half plane and at much higher frequency than the pole.

# SMALL SIGNAL FREQUENCY RESPONSE



- ❖ An important parameter is the unity gain frequency  $f_T$  (or gain-bandwidth product), that is the frequency at which the gain becomes 0 dB.
- ❖ Neglecting the zero,  $f_T$  is:

$$f_T = \frac{1}{2\pi} \omega_p |A_v(0)| = \frac{1}{2\pi C_2 + C_3} \frac{g_{m1}}{C_2 + C_3} = \frac{1}{2\pi} \frac{\sqrt{2\mu_1 C_{ox} \left(\frac{W}{L}\right)}}{C_2 + C_3} \sqrt{I_D}$$

- ❖  $f_T$  increases as the square root of the bias current increases. This is the opposite of the previous recommendation derived for increasing the gain.
- ❖ Due to the Miller effect,  $C_{in} = C_1 + C_2(1 - A_v)$ .  $A_v$  can be as high as hundred or more. Even though  $C_2$  can be small (few fF), it becomes a non-negligible load for the stage driving the inverter.

# OUTPUT SWING



- ❖ Important feature is the output swing.
- ❖ Both transistors have to be kept in the saturation region.
- ❖ The drain-to-source voltages of the two transistors have to be larger than the respective overdrive voltage (or saturation voltage)  
 $V_{ov} = V_{sat} = V_{GS} - V_{th}$
- ❖ The output swing is, hence, limited as:

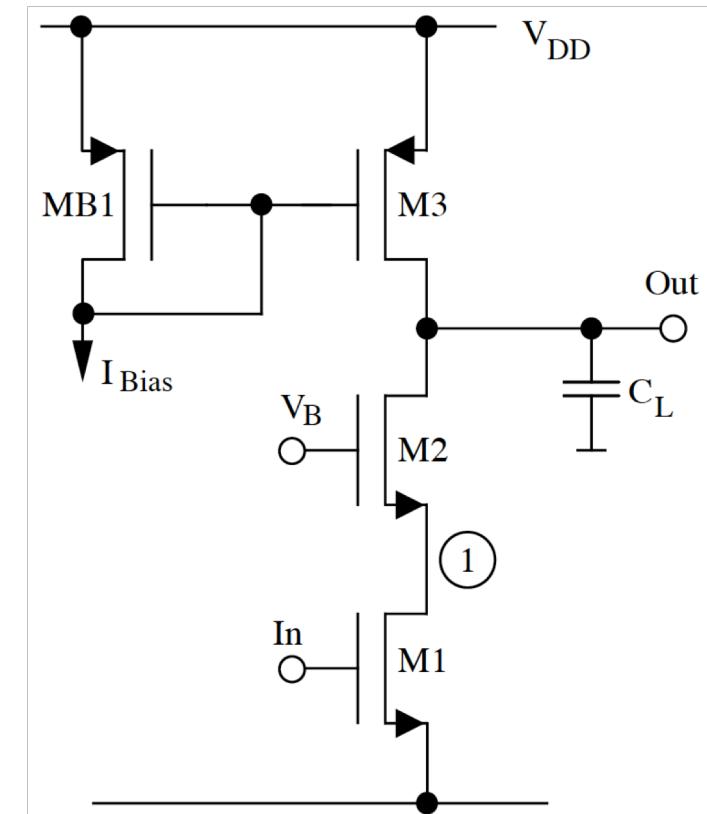
$$V_{sat,n} \leq V_{out} \leq V_{DD} - V_{sat,p}$$

- ❖ Since the saturation voltage is only few hundreds of mV, the output swing of an inverter with active load is one of the best that a designer can achieve with MOS technology.

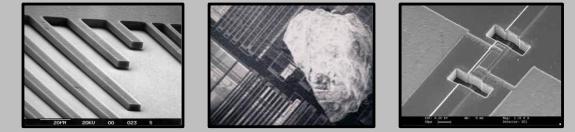
# CASCODE



- ❖ The cascode configuration is used to alleviate the problem related to the Miller amplification of the input-output parasitic capacitance of the inverter with active load stage.
- ❖ It is a cascade connection of a common source and a common gate stage.
- ❖ The extra node (1) decouples the input from the output.
- ❖ Miller effect exists on  $C_2 = C_{gd1} + C_{gd1,ov}$ .
- ❖ Target is to keep  $A_1$  (gain from input to node (1)) low and the gain from input to output high.



# CASCODE BIAS CONDITION

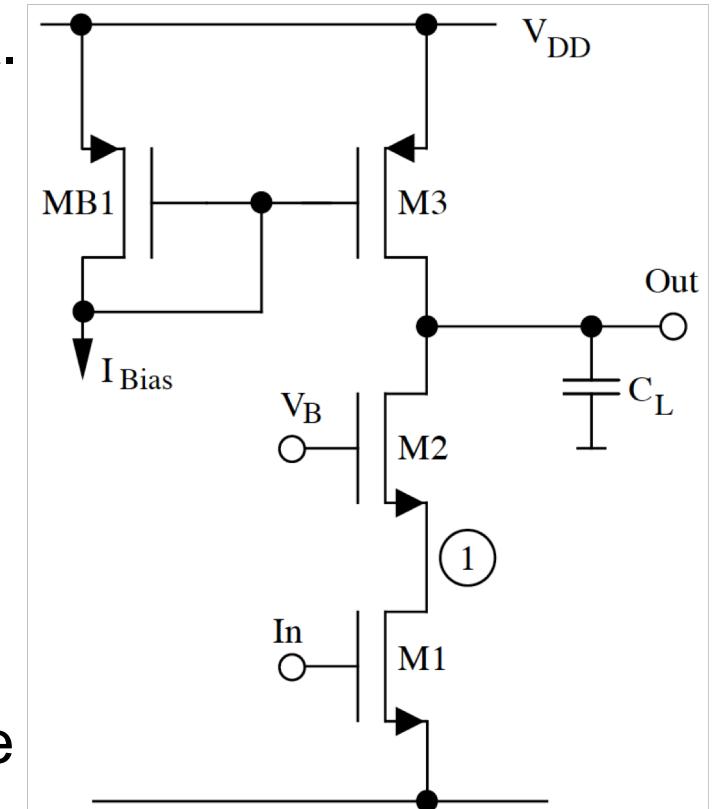


- ❖ All the transistors must work in saturation.
- ❖ For  $V_B$  there is an upper and a lower limit.
- ❖  $V_B$  cannot be too low in order to do not push  $M_1$  in triode region:

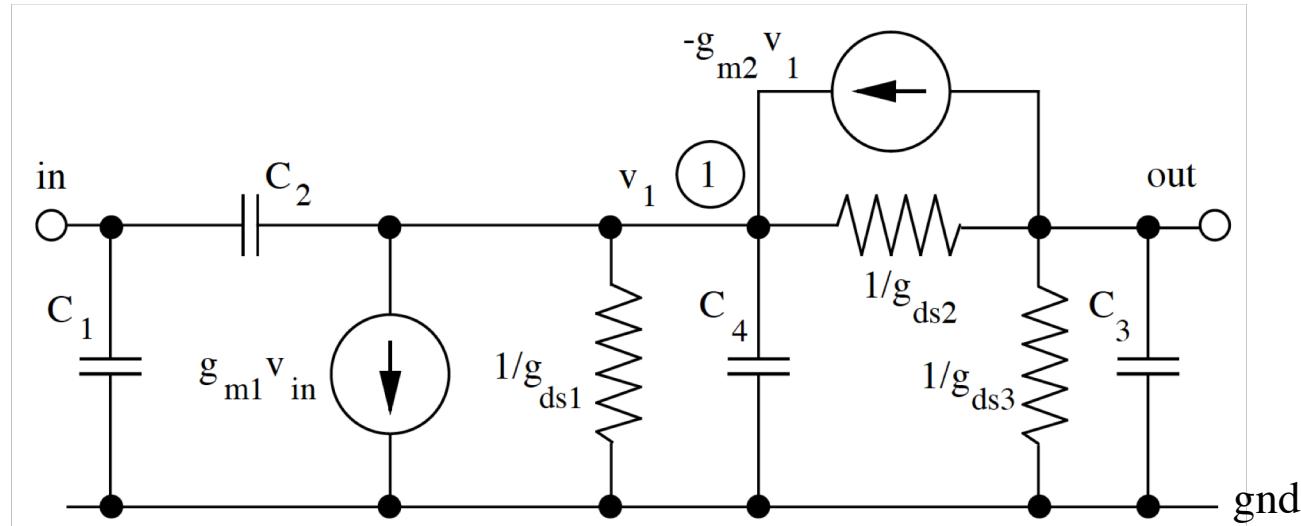
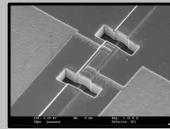
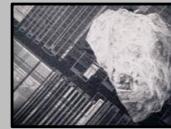
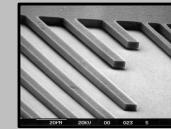
$$V_B > V_{sat,1} + V_{GS2} = V_{sat,1} + V_{Th,n} + V_{sat,2} = \\ = V_{Th,n} + \sqrt{\frac{I_1}{2\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} + \sqrt{\frac{I_1}{2\mu_n C_{ox} \left(\frac{W}{L}\right)_2}}$$

- ❖  $V_B$  cannot be too high in order to optimize the output swing:

$$V_B < V_{out,min} - V_{sat,2} + V_{GS2} = V_{out,min} + V_{Th,n}$$



# SMALL SIGNAL ANALYSIS



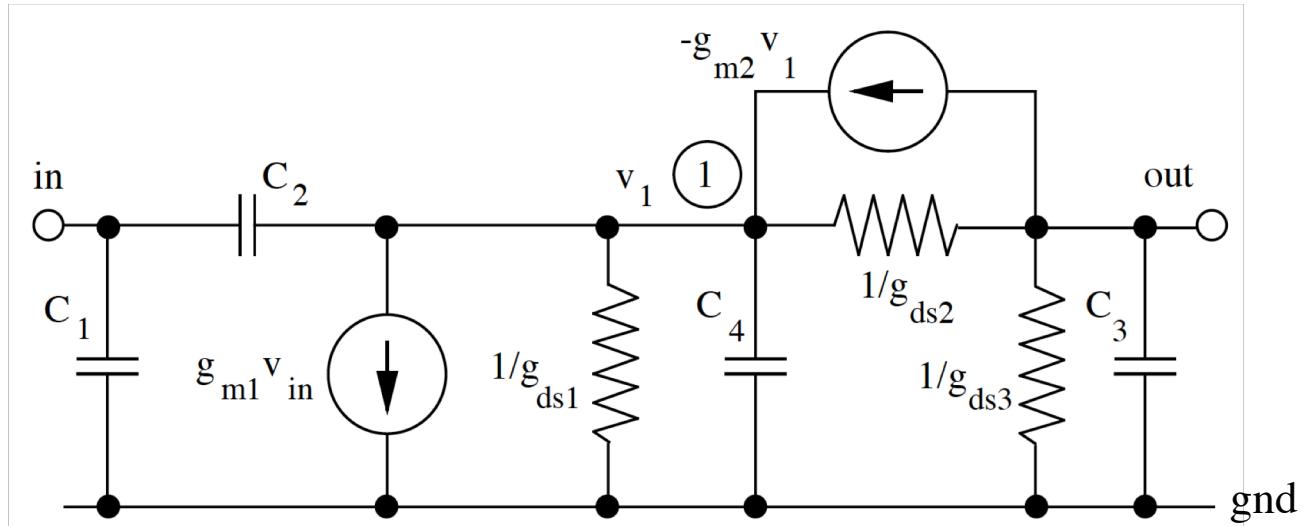
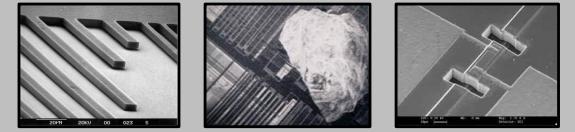
$$C_1 = C_{gs1} + C_{gs1,ov}$$

$$C_2 = C_{gd1} + C_{gd1,ov}$$

$$C_3 = C_{gd2} + C_{gd2,ov} + C_{gd3} + C_{gd3,ov} + C_{db2} + C_{db3} + C_L$$

$$C_4 = C_{gs2} + C_{gs2,ov} + C_{db1} + C_{sb2}$$

# SMALL SIGNAL ANALYSIS



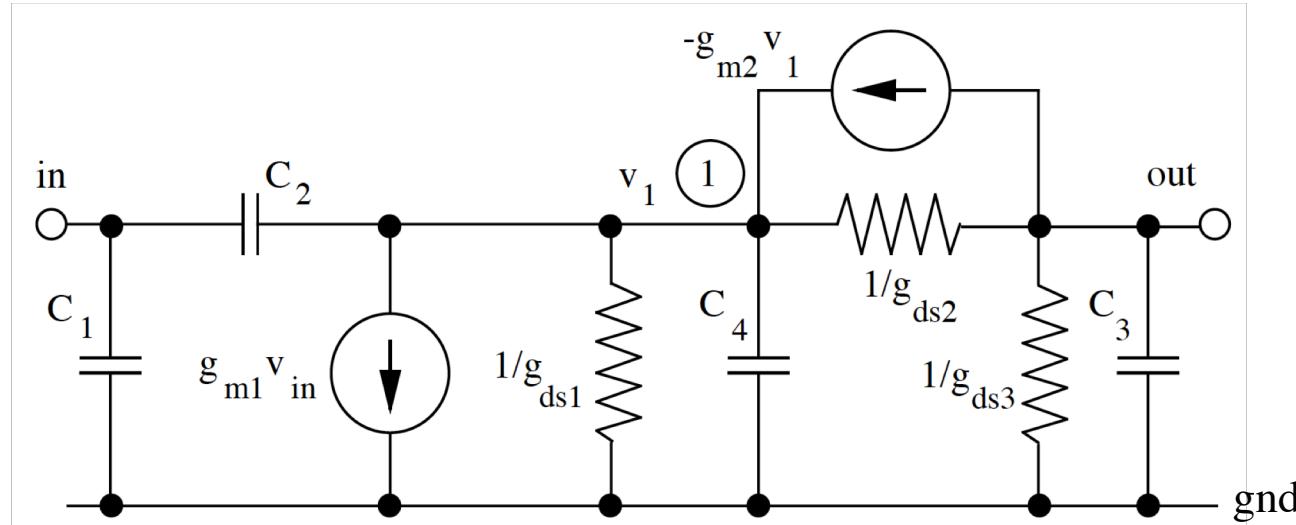
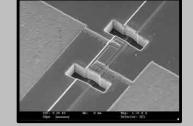
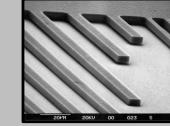
- ❖ At low frequency, neglecting  $g_{ds1}$  and  $g_{ds2}$ :

$$g_{m1}v_{in} = -g_{m2}v_I = -g_{ds3}v_0$$

$$A_v = \frac{v_0}{v_{in}} = -\frac{g_{m1}}{g_{ds3}}$$

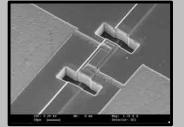
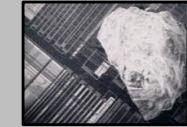
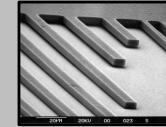
$$A_I = \frac{v_I}{v_{in}} = -\frac{g_{m1}}{g_{m2}}$$

# SMALL SIGNAL ANALYSIS



- ❖ Neglecting  $g_{ds1}$  and  $g_{ds2}$  means that the current  $g_{m1}v_{in}$  is fully transferred to the active load,  $1/g_{ds3}$ .
- ❖ It means, hence, assuming that the resistance looking into the drain of  $M_2$  is much larger than  $1/g_{ds3}$  and that the resistance looking into the source of  $M_2$  is negligible compared to  $1/g_{ds1}$ . (assumptions to be verified shortly)

# SMALL SIGNAL ANALYSIS



- ❖ Using the expressions for  $g_{m1}$  and  $g_{ds3}$ , the DC small signal gain turns out to be:

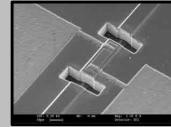
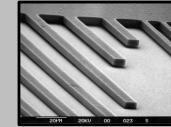
$$A_v = -\frac{\sqrt{2C_{ox}\mu_I \left(\frac{W}{L}\right)_I}}{\sqrt{I_D} \lambda_p}$$

- ❖ Similarly to the inverter with active load, it increases as the square root of the current increases.
- ❖ The gain from input to node (1) is for sure lower than  $A_v$  since it is the ratio between two transconductance:

$$A_I = -\sqrt{\frac{W_1}{L_1}} \sqrt{\frac{L_2}{W_2}}$$

- ❖ With transistors having a similar aspect ratio, the Miller amplification of  $C_2$  turns out to be a small number.

# SMALL SIGNAL FREQUENCY RESPONSE



- ❖ The circuit has three nodes: the input, the output, and node (1).
- ❖ For the input pole: if the circuit is driven by an ideal generator, there is no frequency limitation otherwise, with a finite input resistance  $R_{in}$ , the angular frequency of the input pole is  $1/[R_{in}(C_1+C_2(1-A_1))]$ .
- ❖ At the output node: the capacitance is  $C_3$  while the output impedance is  $1/g_{ds3}$  (neglecting the impedance seen at the drain of  $M_2$ , which is pretty large).

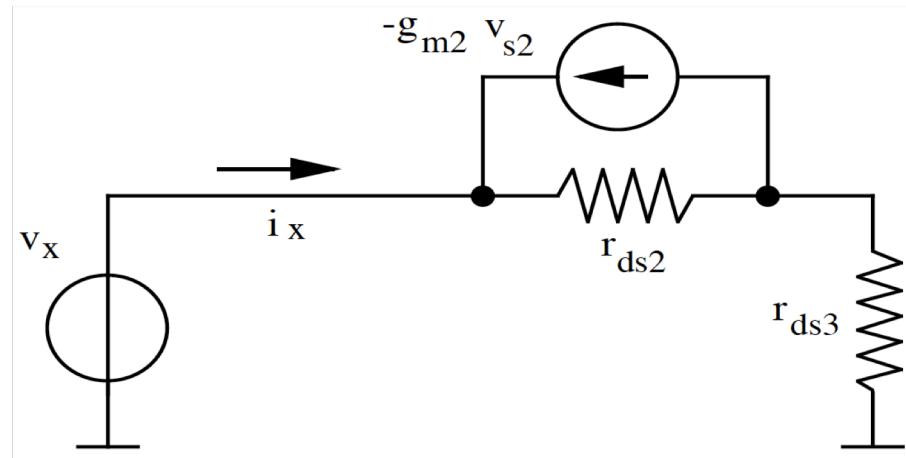
$$f_{p,out} = \frac{1}{2\pi} \cdot \frac{1}{\tau_{out}} = \frac{1}{2\pi} \cdot \frac{g_{ds3}}{C_3}$$

- ❖ At the node (1): the capacitance is  $C_4+C_2(1-1/A_1) \approx C_4+C_2$ .
- ❖ The impedance at node (1) has to be calculated.

# SMALL SIGNAL FREQUENCY RESPONSE



- ❖ Small signal equivalent circuit looking from the source of  $M_2$ . The equivalent resistance can be calculated by applying a test voltage  $V_x$  and estimating the current  $i_x$



$$v_x = r_{ds3}i_x + r_{ds2}(i_x - g_{m2}v_x)$$

$$r_{s2} = \frac{1}{g_{m2}} \left( 1 + \frac{r_{ds3}}{r_{ds2}} \right) = \frac{\zeta}{g_{m2}}$$

- ❖  $r_{ds3}$  is generally similar to  $r_{ds2}$  so that the impedance seen from the source of  $M_2$  is only few times the inverse of the transconductance of  $M_2$  (and for sure does not exceed  $r_{ds1}$ , one of the previous assumptions)

# SMALL SIGNAL FREQUENCY RESPONSE

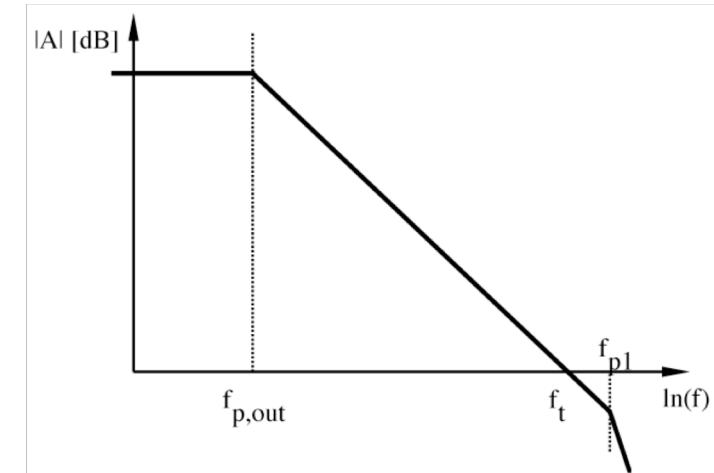


- ❖ The pole frequency associated to node (1) is hence (the cap is  $C_4 + C_2(1 + g_{m2}/g_{m1})$ ):

$$f_{p,1} = \frac{1}{2\pi} \cdot \frac{1}{\tau_1} = \frac{1}{2\pi} \cdot \frac{g_{m2}^2/\zeta}{g_{m1}(C_2 + C_4) + g_{m2}C_2}$$

- ❖ Since  $g_{m1}$  and  $g_{m2}$  are always larger than  $g_{ds3}$  and  $C_2$  and  $C_4$  are comparable or smaller than  $C_3$ , the dominant pole is the one at the output node.
- ❖ The unity gain frequency is:

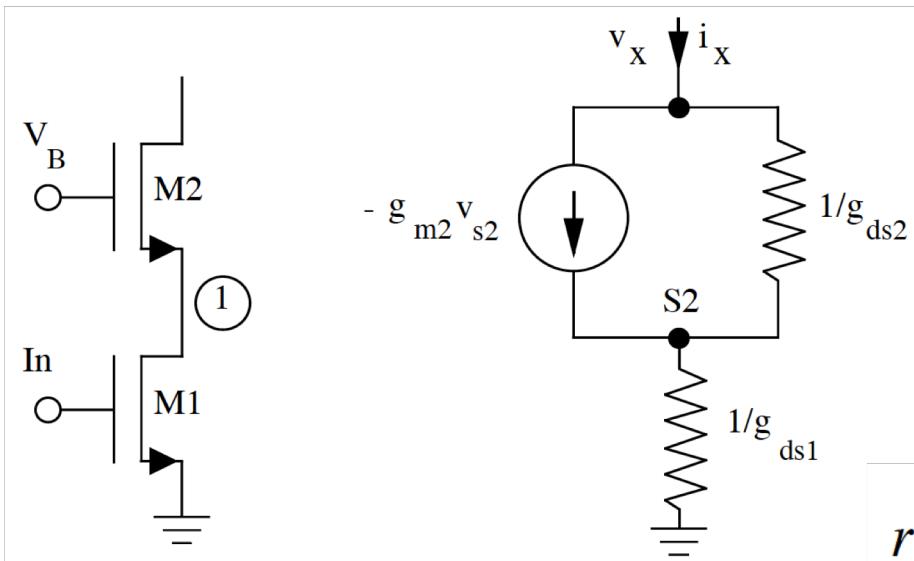
$$f_T = f_{p,dom}|A_v| = \frac{1}{2\pi} \frac{g_{m1}}{C_3}$$



# SMALL SIGNAL FREQUENCY RESPONSE



- ❖ Previous calculations assume that the impedance at the drain of M<sub>2</sub> is very large. Verification:



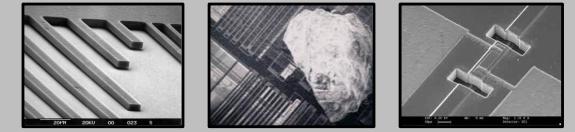
$$v_x = \frac{i_x}{g_{ds1}} + \frac{i_x + g_{m2}v_{s2}}{g_{ds2}}$$

$$v_{s2} = \frac{i_x}{g_{ds1}}$$

$$r_{d2} = \frac{v_x}{i_x} = r_{ds1} + r_{ds2} \left( 1 + \frac{g_{m2}}{g_{ds1}} \right) \cong r_{ds1} g_{m2} r_{ds2}$$

- ❖ Mnemonic rule: the output resistance of a cascode is given by the output resistance of the transistor with source grounded ( $r_{ds1}$ ) amplified by the gain of the other transistor ( $g_{m2}r_{ds2}$ )

# CASCODE WITH CASCODE LOAD

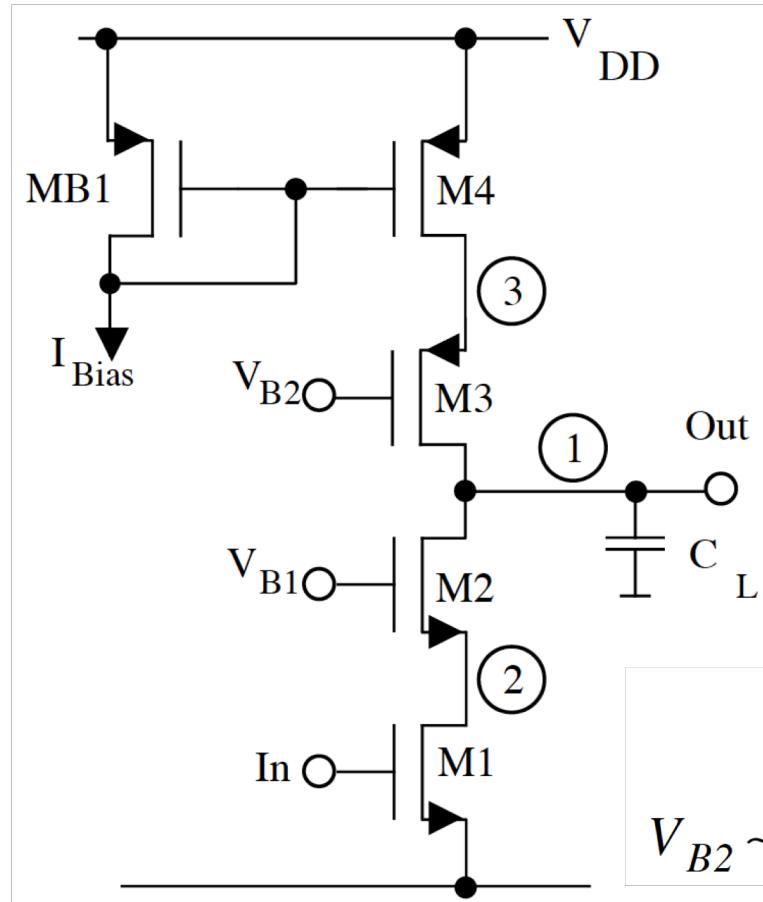


- ❖ The previous gain stages achieve their voltage gain because the signal current,  $g_m v_{in}$ , induced by the input transistor, flows into a relatively high output resistance ( $r_{ds}$  or a parallel of two  $r_{ds}$ ): these are referred to as *transconductance gain stages*.
- ❖ To further increase the gain there are two options: magnify the transconductance or increase the output resistance.
- ❖ The  $g_m$  can be increased by augmenting the bias current but augmenting the bias current at the same time depresses the output resistance by an extent which is larger than the achieved benefit.
- ❖ The  $g_m$  can be increased by using very large aspect ratio of the input transistor: however, aspect ratios higher than hundred is rarely used due to practical limits.
- ❖ Increasing the output resistance leads to better results.

# CASCODE WITH CASCODE LOAD



- The cascode with cascode load achieves a gain which is almost the square of what achieved by a simple inverter with active load.



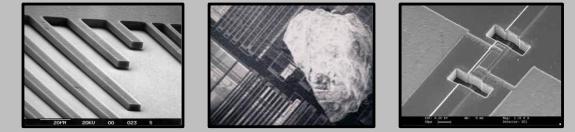
$$A_v = -g_m 1 \frac{(r_{ds1} g_{m2} r_{ds2})(r_{ds4} g_{m3} r_{ds3})}{r_{ds1} g_{m2} r_{ds2} + r_{ds4} g_{m3} r_{ds3}}$$

- The major limitation comes from the reduced output swing:

$$V_{B1} \sim V_{sat,1} + V_{GS2} + \Delta = V_{Th,n} + 2V_{sat} + \Delta$$

$$V_{B2} \sim V_{DD} - V_{sat,4} - V_{GS3} - \Delta = V_{DD} - V_{Th,p} - 2V_{sat} - \Delta$$

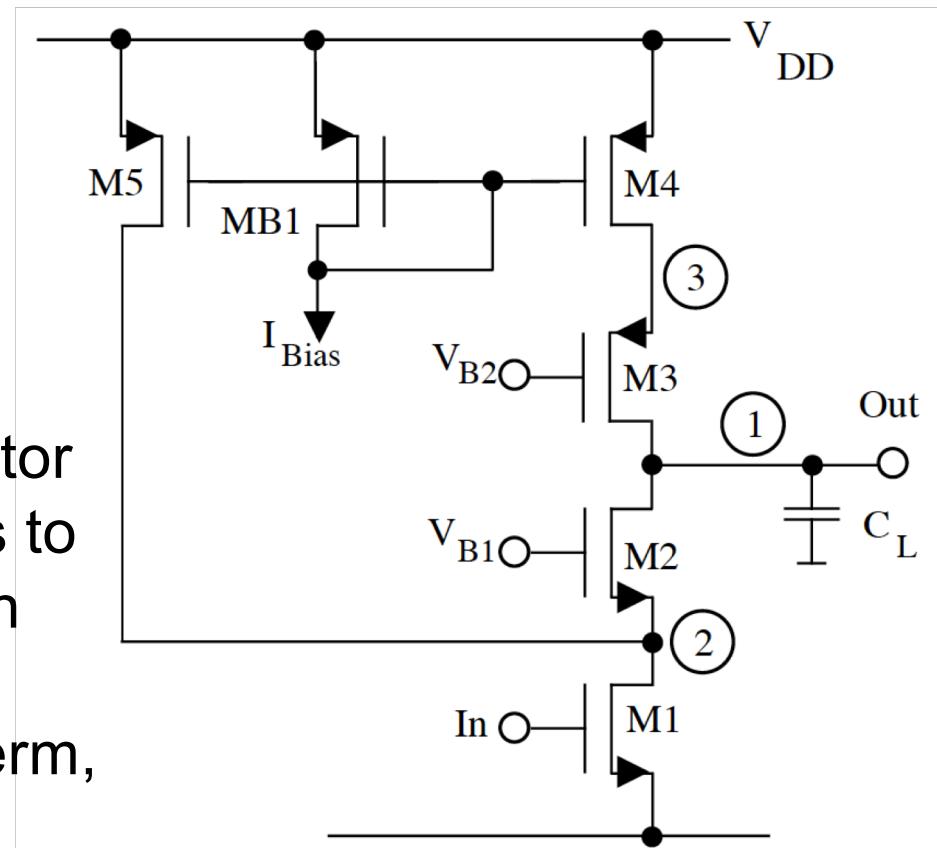
# CASCODE WITH CASCODE LOAD



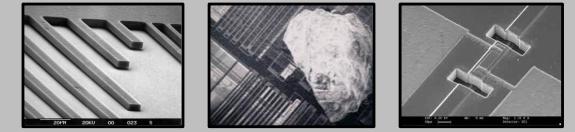
- ❖ The output resistance is the parallel effect of two cascodes and is dominated by the smaller one. If the smaller one is the one on the active load, the gain can be enhanced by increasing the input transistor bias current.
- ❖ The transconductance of  $M_1$  is increased by a factor:

$$\sqrt{\frac{I_4 + I_5}{I_4}}$$

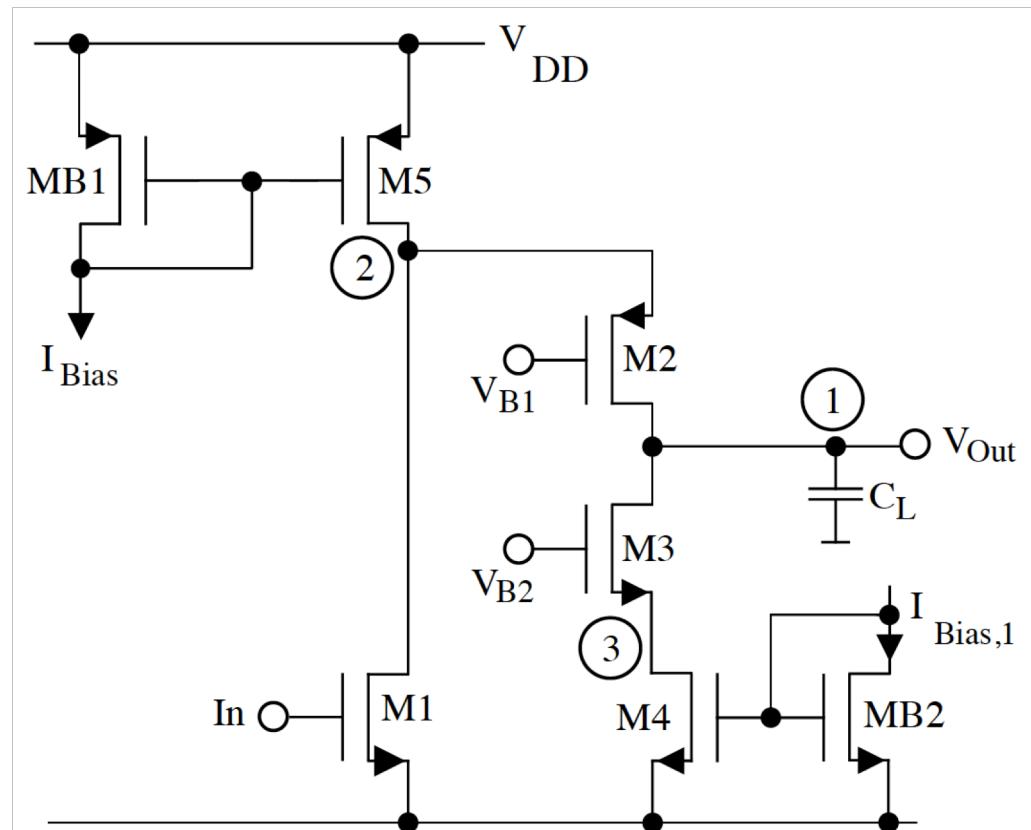
- ❖ The gain increases by the same factor because the signal current transfers to the output node. Resistance through  $M_2$  is lower: increased current in  $M_1$  reduces  $r_{ds1}$  and  $M_5$  adds another term,  $r_{ds5}$ , in parallel to  $r_{ds1}$ .



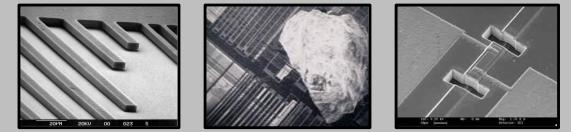
# CASCODE WITH CASCODE LOAD



- ❖ Folded cascode version: the current in the input transistor and in the output branch are separately controlled (this secures the possible DC gain improvement of the previous solution) and allows comfortably biasing the drain of  $M_1$ .
- ❖  $V_{B1}$  biases node (2) rather close to  $V_{DD}$  (instead, the previous solutions, to optimize the output swing, bias  $M_1$  at the border of the saturation, possibly affecting the transconductance gain  $g_{m1}$ ).
- ❖  $V_{B2}$  can be chosen to optimize the negative output swing.



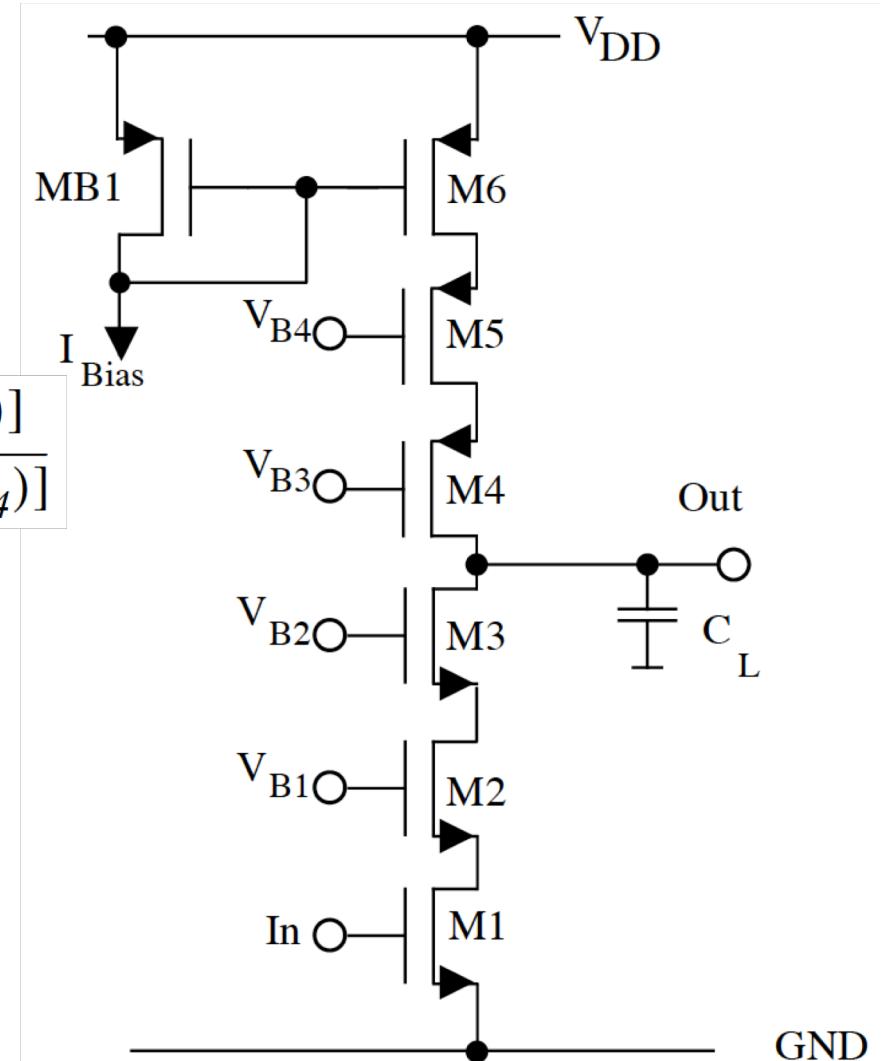
# GAIN ENHANCEMENT



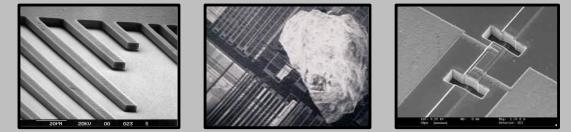
- ❖ For applications where extremely high gain (>80 dB) is crucial, use the double cascode scheme.
- ❖ The output resistance is:

$$R_{out} = \frac{[r_{d1}(g_{m2}r_{d2})(g_{m3}r_{d3})][r_{d6}(g_{m5}r_{d5})(g_{m4}r_{d4})]}{[r_{d1}(g_{m2}r_{d2})(g_{m3}r_{d4})] + [r_{d6}(g_{m5}r_{d5})(g_{m4}r_{d4})]}$$

- ❖ The voltage gain becomes proportional to the cube of  $g_m r_{ds}$ .
- ❖ Output swing further reduces by two  $V_{sat}$ .
- ❖ Generation of the bias voltages becomes tricky.

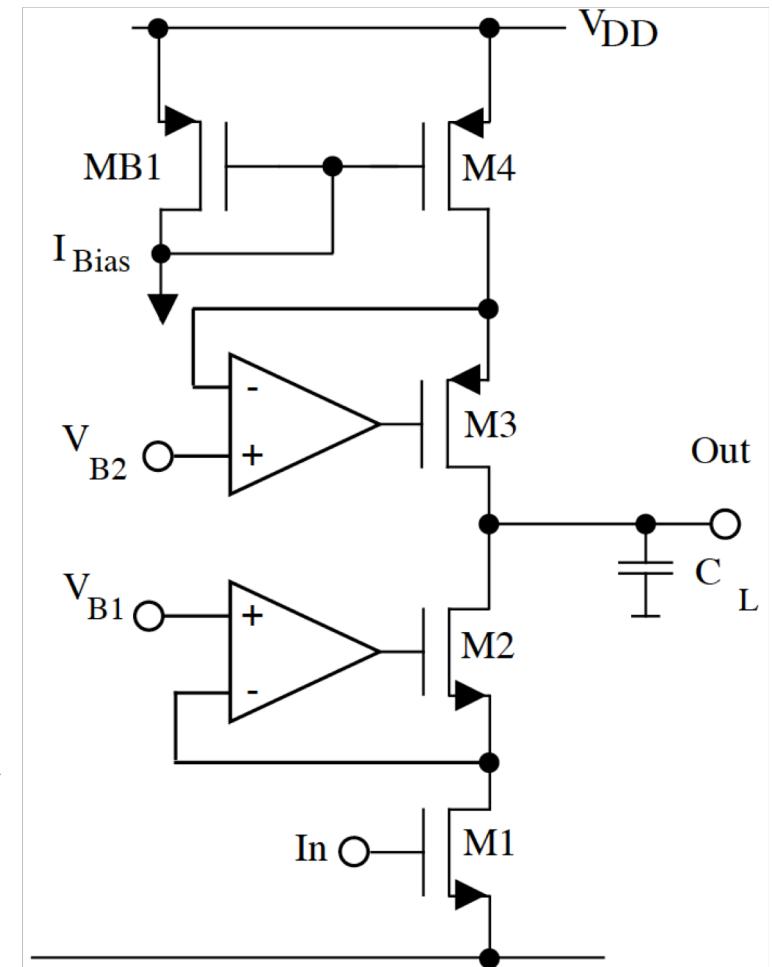


# GAIN ENHANCEMENT

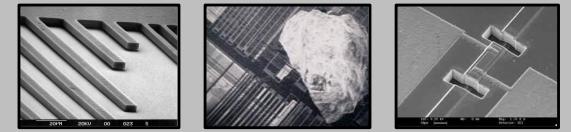


- ❖ Enhancement of the output resistance and output swing equivalent to cascode with cascode load scheme.
- ❖ Local feedbacks to keep constant the gate voltage of the common gate stages.
- ❖ If the source of  $M_2$  ( $M_3$ ) tries to change its value from what imposed by  $V_{B1}$  ( $V_{B2}$ ), the amplified difference is applied to the gate and the feedback loop stabilizes it.
- ❖ By using the same small signal equivalent circuit used for cascode scheme, replace  $g_{m2}$  with  $g_{m2}$  amplified by the op-amp gain

$$R_{out} = \frac{A_1 A_2 [r_{d1}(g_{m2} r_{d2})] [r_{d4}(g_{m3} r_{d3})]}{A_1 [r_{d1}(g_{m2} r_{d2})] + A_2 [r_{d4}(g_{m3} r_{d3})]}$$

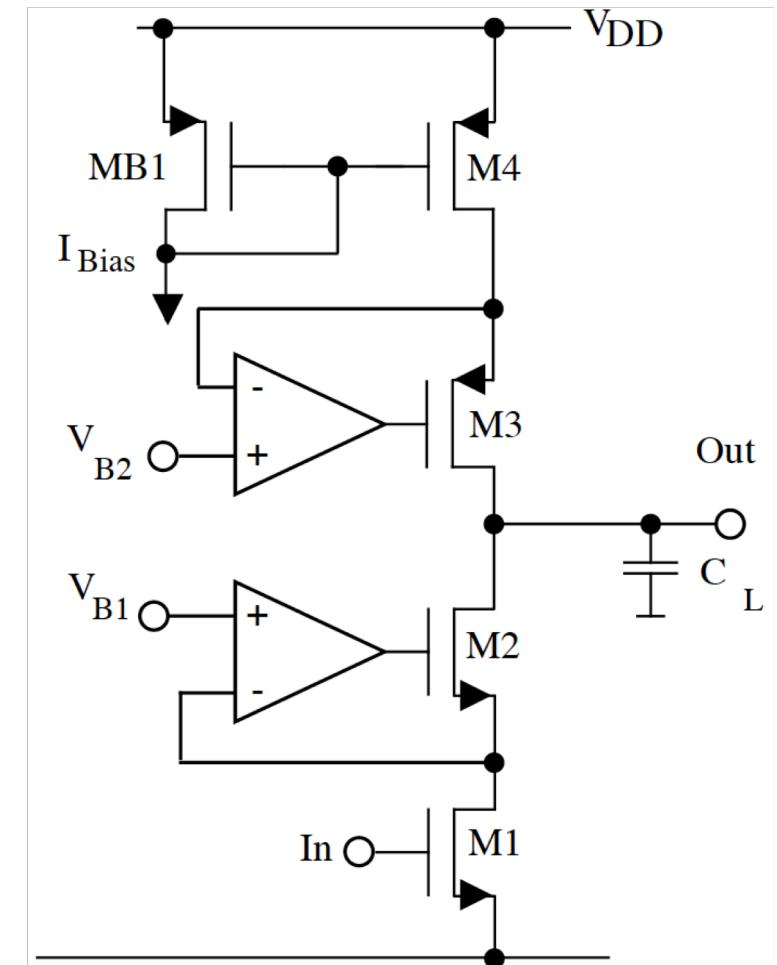


# GAIN ENHANCEMENT

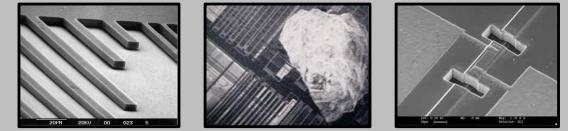


$$R_{out} = \frac{A_1 A_2 [r_{d1}(g_{m2} r_{d2})] [r_{d4}(g_{m3} r_{d3})]}{A_1 [r_{d1}(g_{m2} r_{d2})] + A_2 [r_{d4}(g_{m3} r_{d3})]}$$

- ❖ If  $A_1$  is similar to  $A_2$ , the output resistance and the gain is enhanced by a factor  $A_1$ .
- ❖ Same output swing of the cascode with cascode load
- ❖ Two additional gain amplifiers that means increased power consumption, silicon area, and stability issues
- ❖ The inputs of the two gain stages need to operate close to  $V_{DD}$  or to ground



# DIFFERENTIAL STAGE



- ❖ A differential pair is widely used as the input stage of op-amps.
- ❖  $(W/L)_1 = (W/L)_2$  and the transistors are matched.
- ❖ With both transistors in saturation:

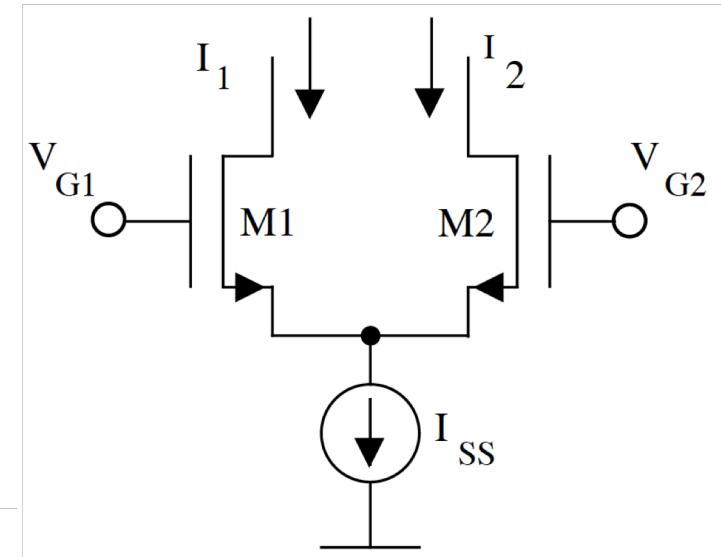
$$I_1 = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right)_1 (V_{GS1} - V_{Th})^2$$

$$I_2 = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right)_2 (V_{GS2} - V_{Th})^2$$

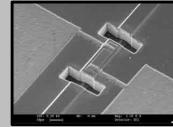
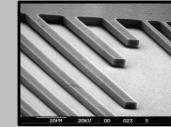
- ❖ The input signal can be expressed as:

$$V_{GS1} = V_{GS0} + \frac{V_{in}}{2}; \quad V_{GS2} = V_{GS0} - \frac{V_{in}}{2}$$

- ❖ It is a superposition of a common mode component and a differential signal.



# DIFFERENTIAL STAGE



- ❖ The output variable is the differential current:

$$\Delta I = I_1 - I_2 = \mu C_{ox} \left( \frac{W}{L} \right)_I V_{in} (V_{GS0} - V_{Th})$$

- ❖ By expressing the bias current as:

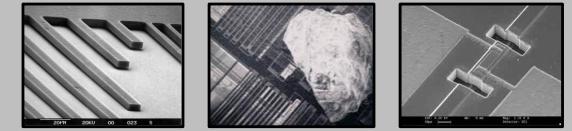
$$I_{SS} = I_1 + I_2 = \mu C_{ox} \left( \frac{W}{L} \right)_I (V_{GS0} - V_{Th})^2$$

- ❖ The differential current becomes:

$$\Delta I = V_{in} \sqrt{\mu C_{ox} \left( \frac{W}{L} \right)_I I_{SS}} = V_{in} g_m$$

- ❖ It is proportional to the input signal and to the square root of both the aspect ratio and the bias current.
- ❖ Like in the inverter with active load, the transconductance gain increase with the square root of the bias current.

# DIFFERENTIAL STAGE



- ❖ The main function of the differential stage is to amplify the differential signal,  $V_{in}$ , and to reject any common mode component,  $V_{G0}$ .
- ❖  $r_I$  represents the non-ideality of the current source.
- ❖ If a common mode signal,  $V_{CM}$ , is applied to the two inputs:

$$2g_m(v_{CM} - v_s) = v_s/r_I$$

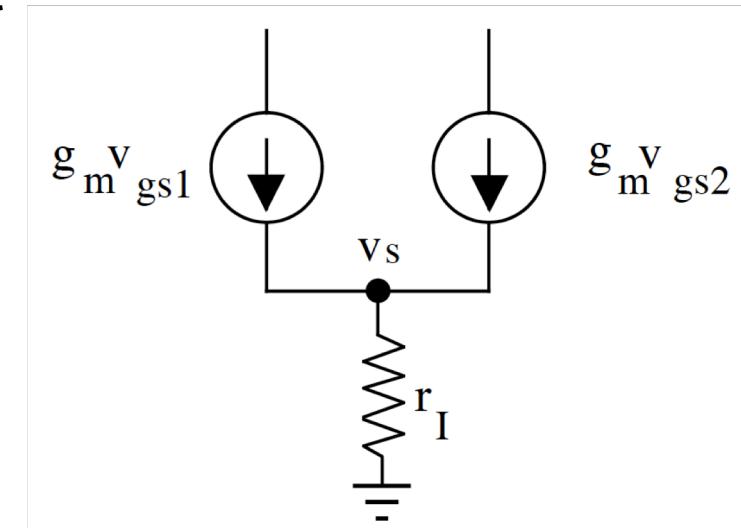
- ❖ The signal current flowing in the two output nodes is:

$$i_{CM} = \frac{g_m v_{CM}}{1 + 2g_m r_I}$$

- ❖ The common-mode rejection ratio is:

$$CMRR = \frac{i_d}{i_{CM}} \equiv 2g_m r_I$$

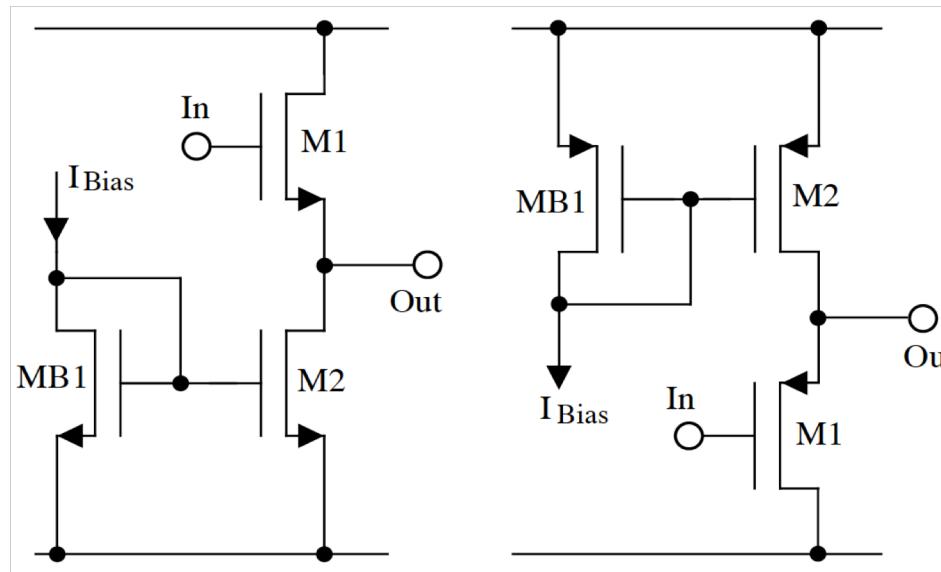
- ❖ To augment the CMRR, increase  $g_m$  or the equivalent resistance of the current source.



# SOURCE FOLLOWER

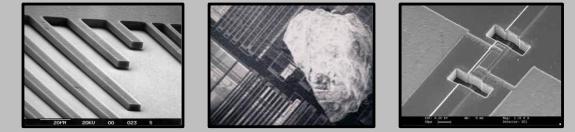


- ❖ Previous stages achieve high gain together with high output impedance. They are not suitable for driving low resistive or large capacitive loads.
- ❖ The source follower achieves low output impedance and level shifting



- ❖ The signal is replicated almost identically at the output with a DC difference which is equal to  $V_{GS1}$ .

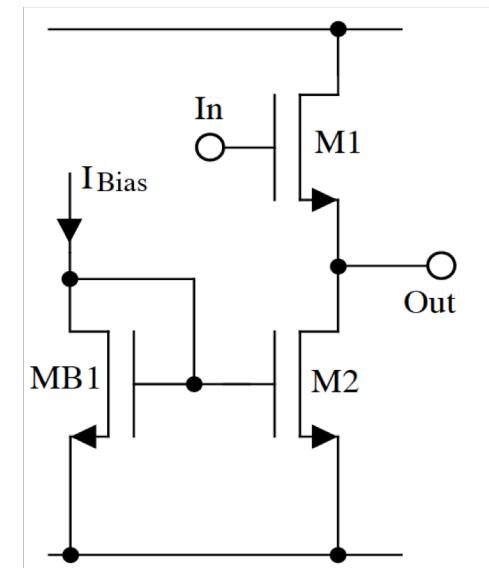
# SOURCE FOLLOWER



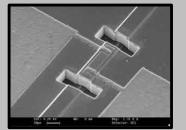
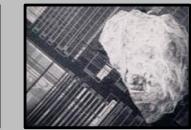
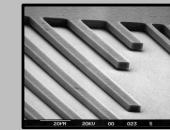
- ❖ All transistors are assumed to work in saturation.
- ❖ The output voltage is not allowed to reach ground (or  $V_{DD}$ ) and since the input cannot exceed  $V_{DD}$ , the output will be limited to one  $V_{GS}$  below  $V_{DD}$ .
- ❖ The output swing (for the n-channel case – similar considerations hold for the p-channel case) is:

$$V_{out,max} = V_{DD} - V_{GS1} = V_{DD} - V_{Th,n} - V_{sat,1}$$

$$V_{out,min} = V_{sat,2}$$



# SOURCE FOLLOWER

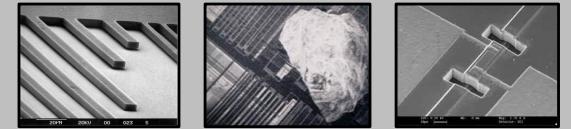


- ❖ The output DC shift is  $V_{GS1}$ . If  $M_2$  is in saturation and  $I_{M1}=I_{M2}$ :

$$V_{GS1} = V_{Th,1} + \sqrt{\frac{2I_2}{\mu C_{ox} \left(\frac{W}{L}\right)_1}}$$

- ❖ It is independent from the input and output voltage only if the threshold voltage remains constant.
- ❖ Body effect plays a critical role.
- ❖ If the source follower is used as a level shifter, the recommendation is to keep the  $V_{BS}$  of the input transistor equal to 0.

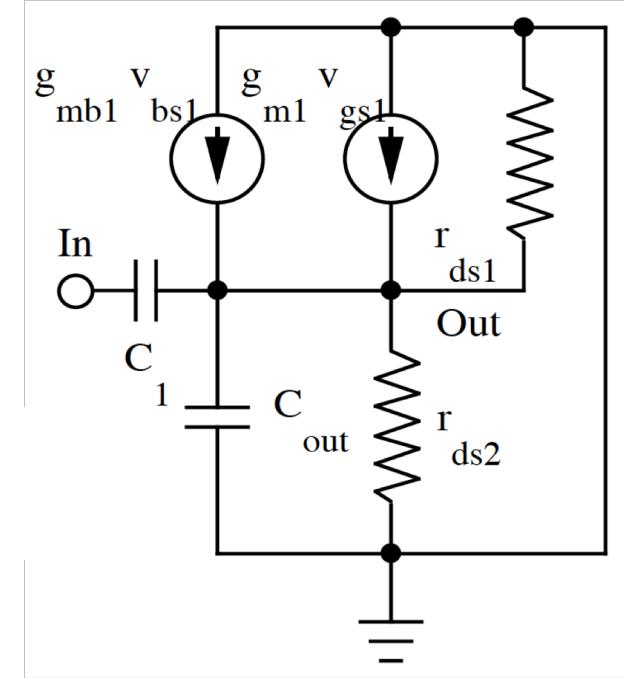
# SOURCE FOLLOWER – SMALL SIGNAL



- ❖ It includes the body effect element.
- ❖ Assuming the substrate connected to ground, at low frequency:

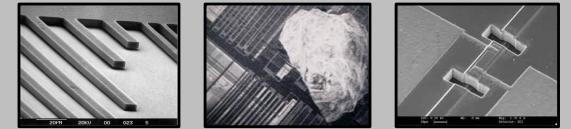
$$(g_{ds1} + g_{ds2})v_{out} + g_{mb1}v_{out} - g_{m1}v_{gs1} = 0$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{ds1} + g_{ds2} + g_{mb1}}$$



- ❖ If  $g_{m1}$  is larger compared to the other terms (as normally is), the voltage gain is very close to 1.
- ❖ When  $g_{mb1}$  has to be accounted for, the gain is lower than one since  $g_{mb1}$  can be as high as the 10% of  $g_{m1}$ .

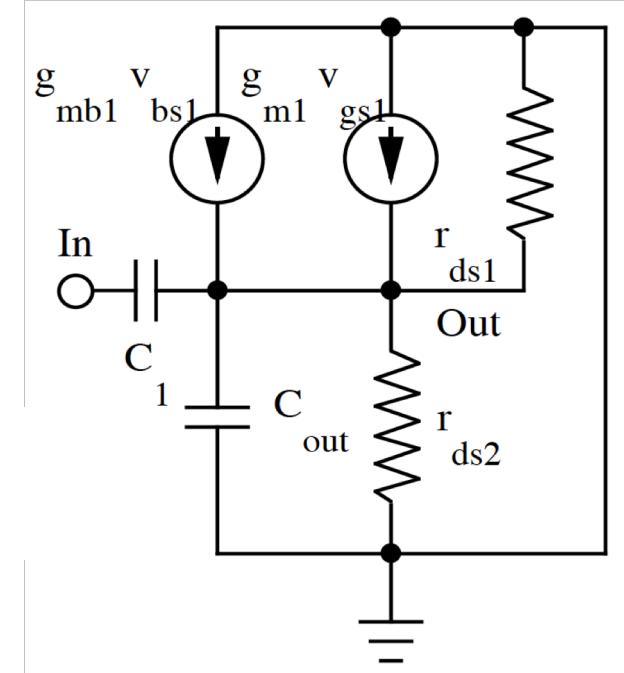
# SOURCE FOLLOWER – SMALL SIGNAL



- ❖ At high frequency, the transistor does not contribute at all and the output is just the input attenuated by the  $C_1/(C_1+C_{out})$ .
- ❖ For the computation of the output resistance, a test voltage generator,  $V_x$ , can be placed at the output node and the current it is providing,  $i_x$ , can be evaluated.

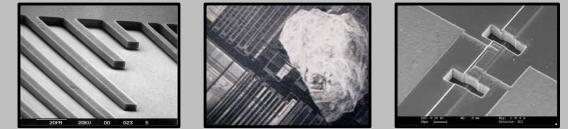
$$i_x = (g_{ds1} + g_{ds2} + g_{mb1} + g_{m1})v_x$$

$$R_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{mb1} + g_{m1}} \approx \frac{1}{g_{m1}}$$

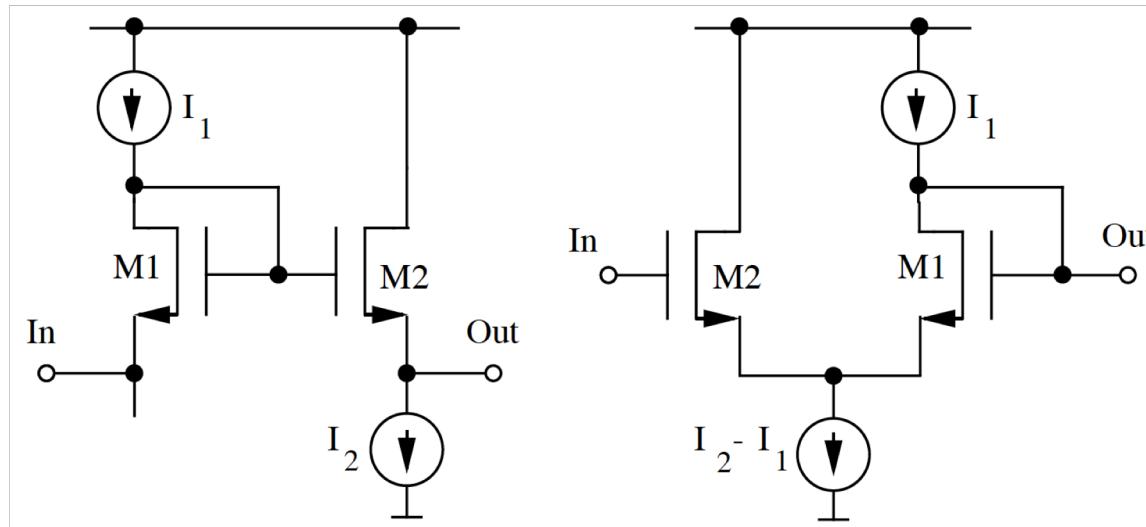


- ❖ The output resistance can be in the order of few kΩ.

# $V_{TH}$ INDEPENDENT LEVEL SHIFT

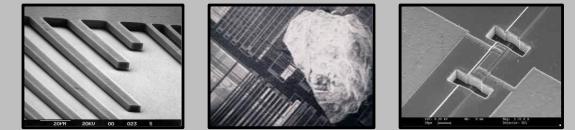


- ❖ The source follower generates a shift which is quite large and threshold-dependent.
- ❖ Many applications require small and threshold independent voltage shifts.

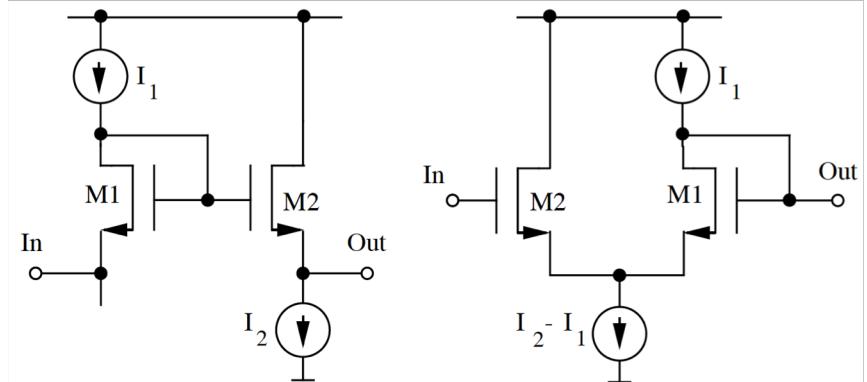


- ❖ Diode up + source follower down or viceversa.
- ❖ Complementary versions are available.

# $V_{TH}$ INDEPENDENT LEVEL SHIFT



- ❖ Both solutions achieve a shift  $\Delta V$  with a series of shift-up-down.
- ❖ By inspection of the circuits:



$$\Delta V = V_{Th,1} + \sqrt{\frac{2I_{D1}}{\mu C_{ox}\left(\frac{W}{L}\right)_1}} - V_{Th,2} - \sqrt{\frac{2I_{D2}}{\mu C_{ox}\left(\frac{W}{L}\right)_2}}$$

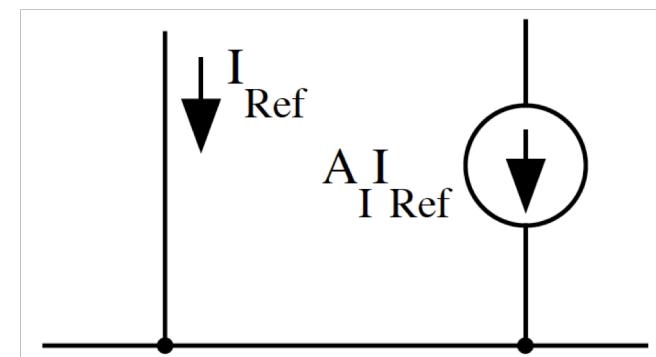
$$\Delta V = \frac{2}{\mu C_{ox}} \cdot \left\{ \sqrt{I_{D1}\left(\frac{W}{L}\right)_1} - \sqrt{I_{D2}\left(\frac{W}{L}\right)_2} \right\}$$

- ❖ The two shifts are achieved by the same kind of transistors, the thresholds will match and the  $\Delta V$  is given by the difference between two overdrives.
- ❖  $\Delta V$  can be tuned to the desired value with appropriate choice of transistors aspect ratios and bias currents.

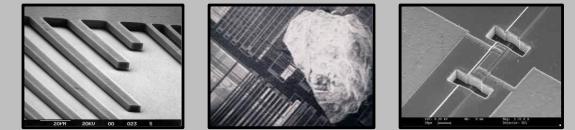
# CURRENT MIRRORS



- ❖ A current mirror generates a replica (attenuated or amplified, if necessary) of a given reference current.
- ❖ It behaves like a current controlled current source (CCCS) but with only positive gain factor and with finite output impedance, dynamic range and speed.
- ❖ The mostly used current mirrors are:
  - ❖ The simple current mirror
  - ❖ The Wilson current mirror
  - ❖ The improved Wilson current mirror
  - ❖ The cascode current mirror
  - ❖ The modified cascode current mirror
  - ❖ The high compliance current mirror

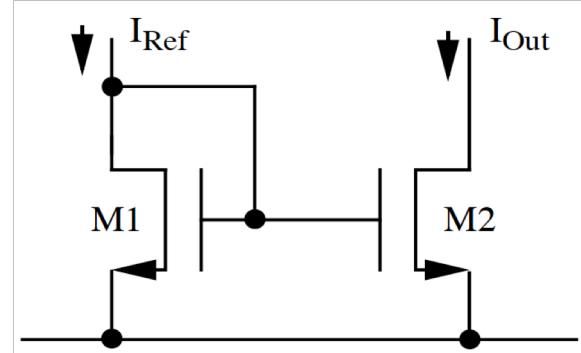


# SIMPLE CURRENT MIRROR (WIDLAR)



$$I_{Ref} = I_1 = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right)_1 (V_{GS1} - V_{Th})^2 (1 + \lambda V_{DS1})$$

$$I_{out} = \frac{\mu C_{ox}}{2} \left( \frac{W}{L} \right)_2 (V_{GS1} - V_{Th})^2 (1 + \lambda V_{DS2})$$



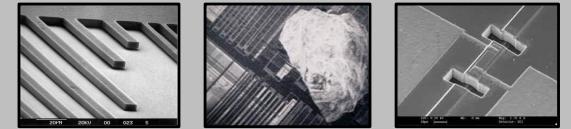
❖ By neglecting the term  $\lambda V_{DS1}$ :

$$I_{out} = I_{Ref} \frac{(W/L)_2}{(W/L)_1} (1 + \lambda V_{out})$$

$$r_{out} = \frac{1}{\lambda I_{out}}$$

- ❖ The output resistance (on the order of few hundreds of  $k\Omega$ ) is often not enough for a number of applications (more complicated structures achieve higher output resistance).
- ❖ Excellent output dynamic range (output can go down to the saturation voltage of  $M_2$ ).

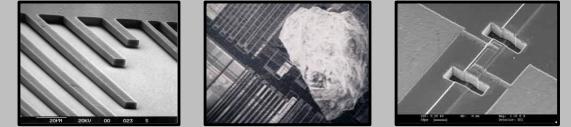
# CURRENT MIRROR ACCURACY



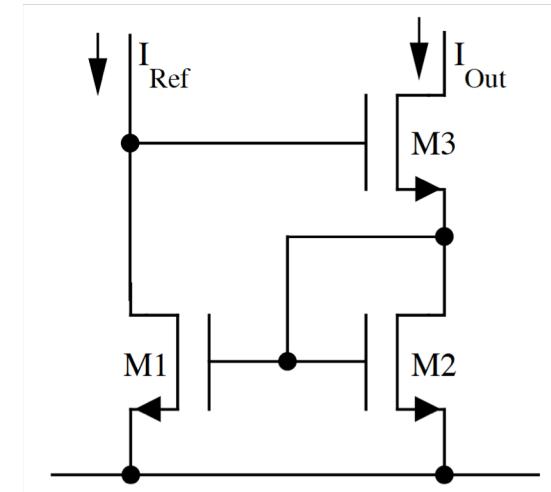
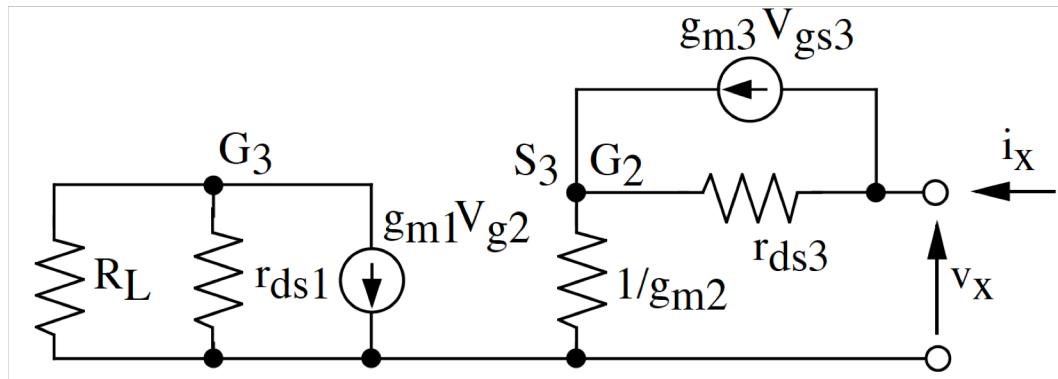
$$\left(\frac{\delta I_{out}}{I_{out}}\right)^2 = \left(\frac{\delta W}{W}\right)^2 + \left(\frac{\delta L}{L}\right)^2 + \left(\frac{\delta C_{ox}}{C_{ox}}\right)^2 + \left(\frac{\delta \mu}{\mu}\right)^2 + 2\left(\frac{\delta V_{Th}}{V_{GS} - V_{Th}}\right)^2 + 2\left(\frac{\delta V_{GS}}{V_{GS} - V_{Th}}\right)^2$$

- ❖ Inaccuracies come from:
  - ❖ Imperfect geometrical matching
  - ❖ Technological parameter mismatch
  - ❖ Parasitic resistances
- ❖ Inaccuracies in geometrical dimensions come from photolithographic processes and etching. Layout should take into account undercut and boundary dependent effects.
- ❖ Errors due to mobility and oxide thickness come from technology gradients along the surface of the chip. Use interdigitized or common centroid structures which minimize the distance among transistors.

# WILSON CURRENT MIRROR



- The relatively low output resistance of the simple current mirror can be increased by the Wilson scheme.



- $R_L$  represents the external load seen from the reference current connection.
- $r_T$  is the parallel of  $R_L$  and  $r_{ds1}$ .

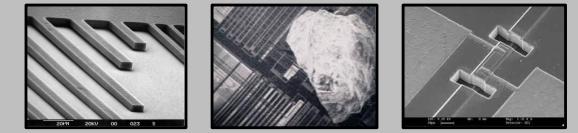
$$r_{out} = \frac{I}{g_{m2}} + r_{ds3} \left[ I + \frac{g_{m3}}{g_{m2}} (I + g_{m1} r_T) \right]$$

$$v_{g2} = v_{s3} = i_x / g_{m2}$$

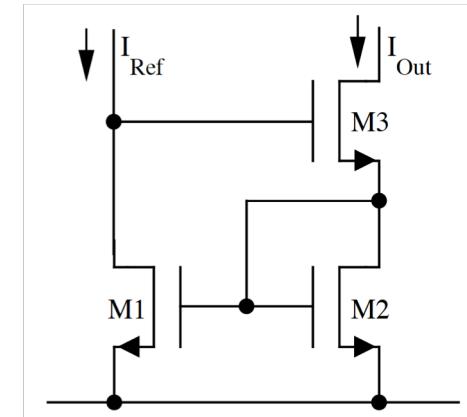
$$v_{g3} = -g_{m1} v_{g2} r_T$$

$$v_x = \frac{i_x}{g_{m2}} + (i_x - g_{m3} v_{gs3}) r_{ds3}$$

# WILSON CURRENT MIRROR



$$r_{out} = \frac{I}{g_{m2}} + r_{ds3} \left[ I + \frac{g_{m3}}{g_{m2}} (I + g_{m1}r_T) \right]$$



- ❖  $g_{m2}$  and  $g_{m3}$  have the same order of magnitude since  $M_2$  and  $M_3$  carry the same current.
- ❖ The output resistance is basically  $r_{ds3}$  amplified by the factor  $g_{m1}r_T$ . It is high if  $r_T$  is high, meaning  $R_L$  is high.
- ❖ This is normally met if the reference current comes from a current source.
- ❖ Main issue. The  $V_{DS}$  of  $M_1$  and  $M_2$  are systematically different:  $V_{DS1}=V_{GS3}+V_{DS2}$ . This imposes a systematic offset between reference and output current.

# IMPROVED WILSON CURRENT MIRROR



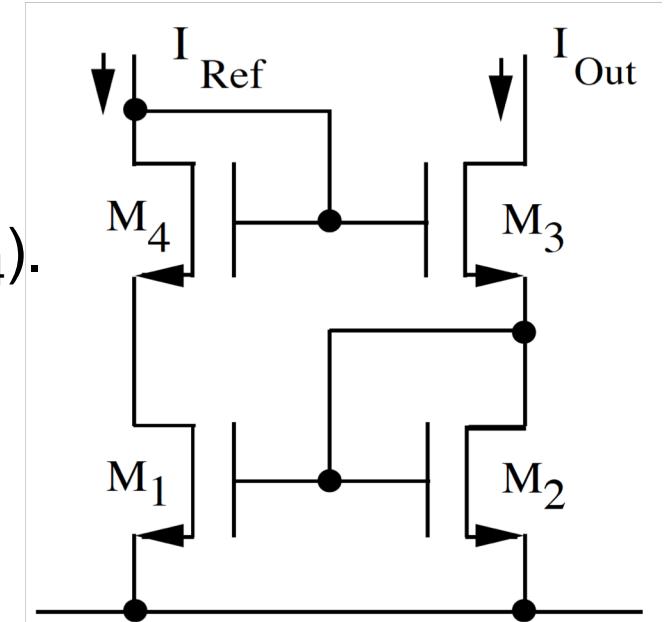
- The systematic current mismatch is compensated by this solution.  $M_4$  shifts down the gate voltage of  $M_3$  so that

$$V_{DS1} = V_{GS3} + V_{DS2} - V_{GS4}$$

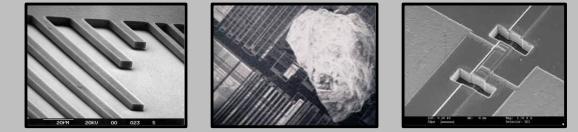
- If  $V_{GS3} = V_{GS4}$ , as reasonable if they are matched, current mismatch is overcome.
- $M_4$  adds a resistance  $1/g_{m4}$  in series with  $R_L$  ( $r_T' = r_{ds1} // (R_L + 1/g_{m4})$ ).
- Result is substantially unchanged ( $R_L \gg 1/g_{m4}$ ).

$$r_{out} \approx r_{ds3} \frac{g_{m3}}{g_{m2}} g_{m1} r_T \frac{R_L g_{m4}}{1 + R_L g_{m4}}$$

$$V_{out, min} = V_{GSI} + V_{sat, 3} = V_{Th, n} + V_{sat, 1} + V_{sat, 3}$$



# CASCODE CURRENT MIRROR



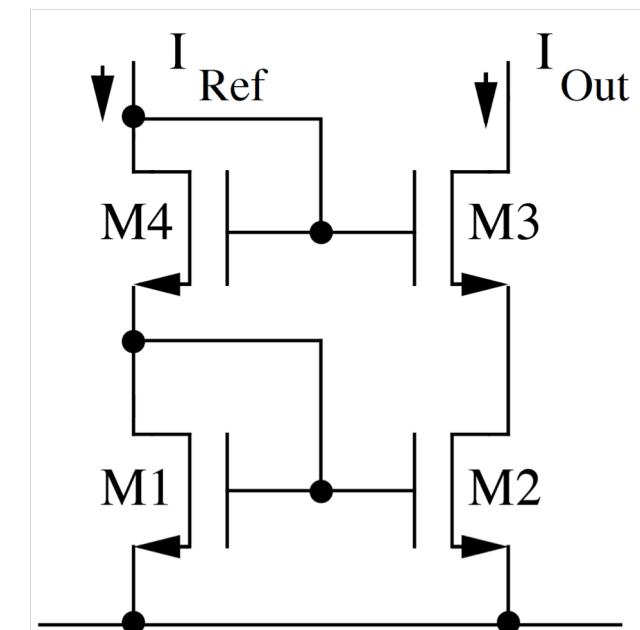
- ❖ Another way to improve the output resistance is to use the cascode arrangement. The  $V_{DS}$  of  $M_1$  and  $M_2$  are set equal (as in the improved Wilson case).
- ❖ The output resistance is obtained by studying the small signal equivalent circuit. However, from the known theory, it is given by the drain resistance of  $M_2$  multiplied by the gain of  $M_3$ :

$$r_{out} \approx r_{ds3} g_{m3} r_{ds2}$$

- ❖ The increase of the output impedance is paid by a reduction of the output swing:

$$V_{S3} = V_{GS1} + V_{GS4} - V_{GS3}$$

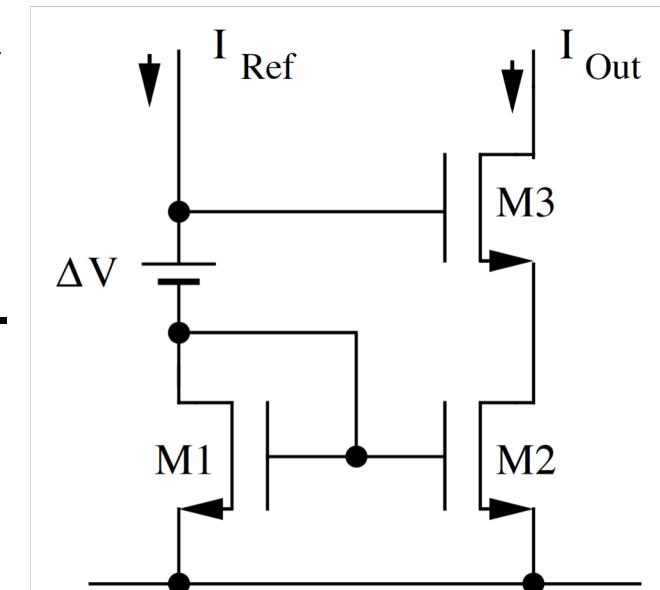
$$V_{out,min} = V_{S3} + V_{sat3} \approx V_{Th} + 2V_{sat}$$



# MODIFIED CASCODE CURRENT MIRROR



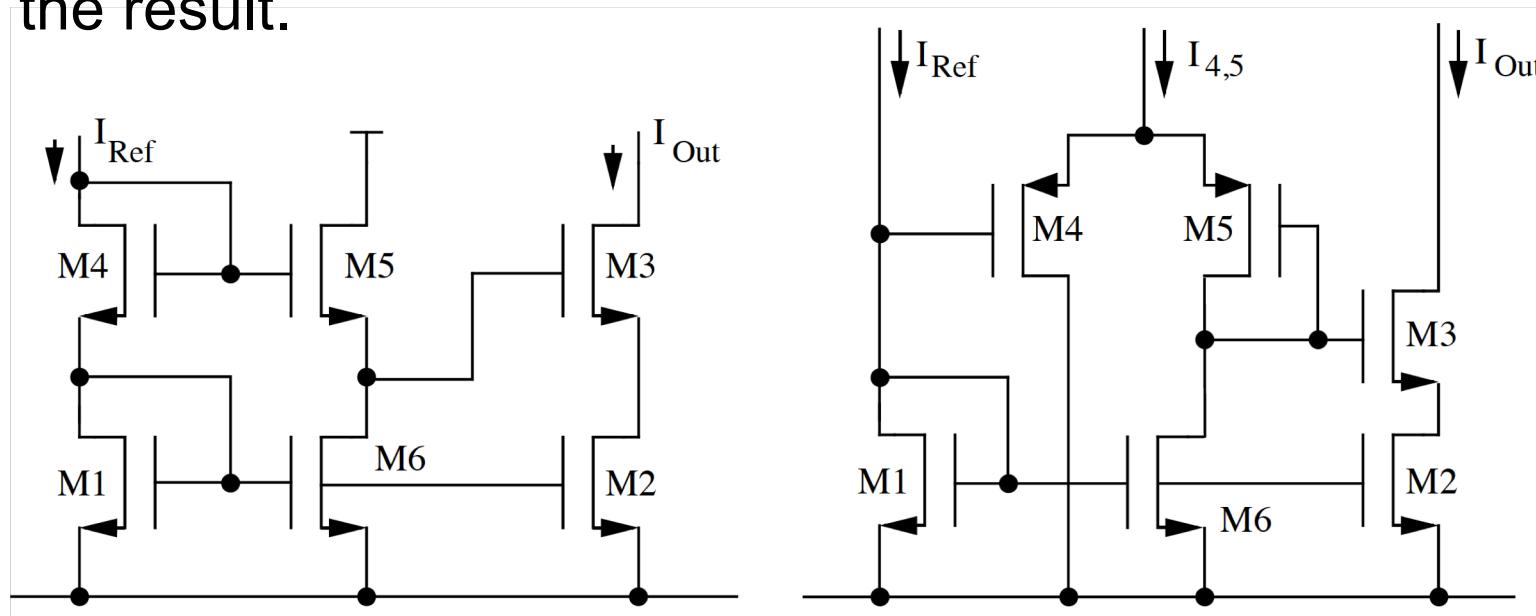
- ❖ Cascode current mirror secures high output impedance, reference and output current match, but low output swing.
- ❖ Often, for low voltage applications, output swing and output resistance are key factors and current matching can be sacrificed.
- ❖ The output resistance remains high if  $M_2$  and  $M_3$  work in saturation. The minimum value for  $V_{G3}$  is, hence,  $V_{sat,2} + V_{GS3}$ . This way the minimum output value is just  $2V_{sat}$ .
- ❖ It is required a level shift  $\Delta V = V_{GS3} + V_{sat,2} - V_{GS1}$ .
- ❖ The level shift needs to be threshold independent.



# MODIFIED CASCODE CURRENT MIRROR



- ❖ Both solutions use two additional transistors compared with the conventional cascode structure.
- ❖  $M_4$  in both scheme shifts up the gate voltage of  $M_1$  and  $M_5$  shifts down the result.

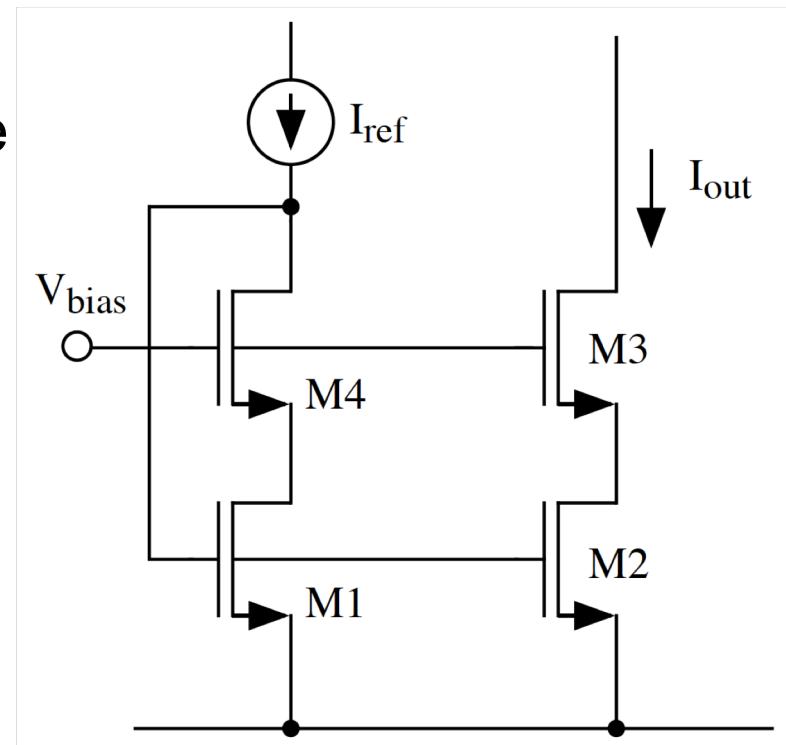


$$\Delta V = V_{GS4} - V_{GS5} = \sqrt{\frac{2I_4L_4}{\mu C_{ox}W_4}} - \sqrt{\frac{2I_5L_5}{\mu C_{ox}W_5}}$$

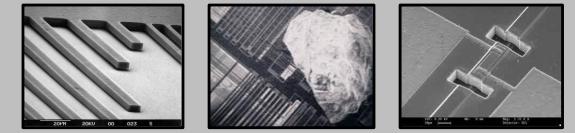
# HIGH COMPLIANCE CURRENT MIRROR



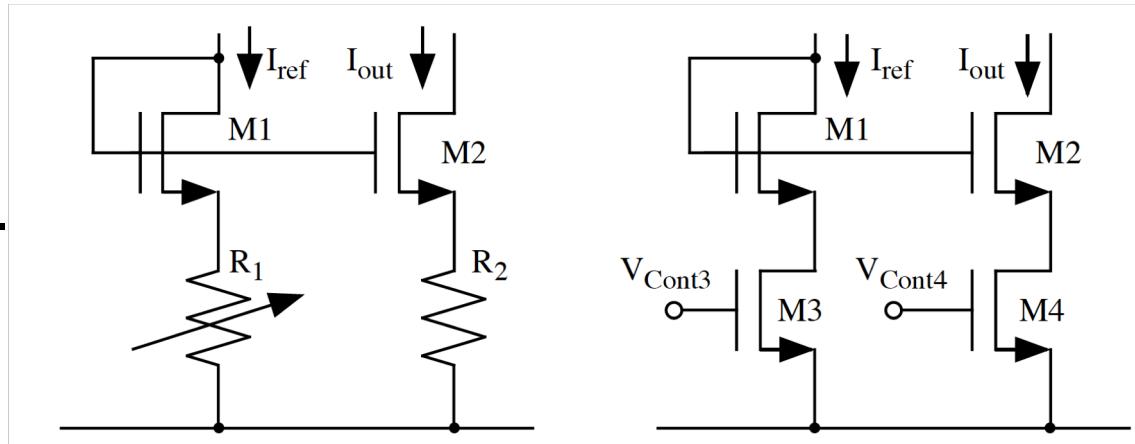
- ❖ High compliance scheme overcomes the current systematic mismatch of the previous solution.
- ❖  $V_{DS1}$  and  $V_{DS2}$  are controlled by the gate voltage of  $M_3$  and  $M_4$ .
- ❖ With  $M_1=M_2$  and  $M_3=M_4$ , systematic current matching achieved.
- ❖  $V_{bias}$  has to be selected such as all the transistors remain in saturation.



# ADJUSTABLE CURRENT MIRRORS



- ❖ In some applications, having an electrically adjustable mirror factor can be required.
- ❖ Use of source-degenerated current mirrors.



$$V_{G1} = R_1 I_{ref} + V_{Th,1} + \sqrt{\frac{2I_{ref}}{\mu C_{ox}}} \sqrt{\frac{L_1}{W_1}} = R_2 I_{out} + V_{Th,2} + \sqrt{\frac{2I_{out}}{\mu C_{ox}}} \sqrt{\frac{L_2}{W_2}}$$

$$R_1 I_{ref} + \sqrt{\frac{2I_{ref}}{\mu C_{ox}}} \sqrt{\frac{L_1}{W_1}} = R_2 I_{out} + \sqrt{\frac{2I_{out}}{\mu C_{ox}}} \sqrt{\frac{L_2}{W_2}}$$

- ❖ The ratio  $I_{out}/I_{ref}$  depends both on transistors aspect ratios and resistors value.
- ❖ Use  $M_3$  and  $M_4$  in triode and control their gate voltage.