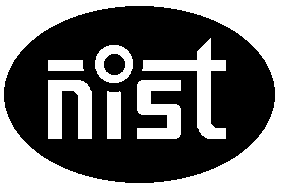
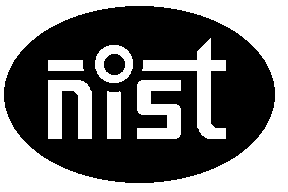
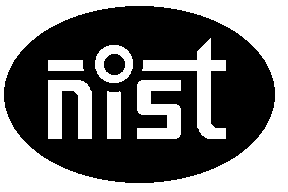
**LOW-POWER AND FAST FULL-ADDER BY EXPLORING NEW XOR AND XNOR GATES**

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**

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**1. INTRODUCTION:**

The use of handheld mobile devices has skyrocketed in recent years. These devices would use less power and operate at a high speed. Power consumption is a metric that can be designed for improved device efficiency when planning a system. A full adder is a fundamental block in many circuits that execute arithmetic operations. As a result, the performance of the full adder has an impact on the overall machine performance. As a consequence, improving the efficiency of the full adder will boost device performance. Many full adder circuits have been constructed using different logic types, each with its own set of advantages and drawbacks.

There are two types of prototypes that have been produced so far. There are two types of styles: static and dynamic. Static full adders have the advantage of high reliability and easy low power consumption. In contrast to static full adders, dynamic full adders need less chip area. One logic style favour’s one aspect of performance, and another logic style favour’s another aspect of performance.

CMOS, DPL, TGA, and TFA are some of the most popular logic design types. Hybrid-logic style refers to complete adders that use more than one logic style. These designs incorporate the characteristics of different logic types in order to boost maximum adder efficiency.

**2. OBJECTIVE OF PROJECT:**

The existing Full-Adder circuits uses more transistors or may have inadequate input values as a result factors like delay, power consumption affects the performance of the complete system.

So our objective is to design a new circuit that uses fewer transistors and adequate input values. As a result the circuits will have:

1. Low Power-Consumption
2. Less Delay
3. And more significantly less PDP

At the end we compared the results with the existing full-adder circuits and obtained some better outcomes.

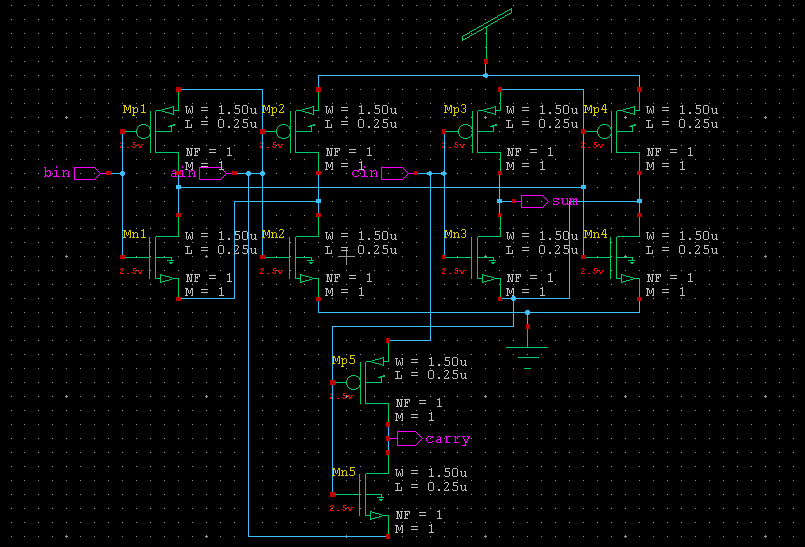
**3. REVIEW:**

Two full adder circuits using XOR and XNOR, have been proposed earlier. Those circuits were designed in order to have high speed and less power consumption. Each one of the circuits has its own advantage of speed and power consumption. Simulations are done in Tanner Tool in 250nm Technology. The performance of each full adder is analyzed by varying the supply voltage. From results, newly designed circuits are found to be better than the previous existing circuits.

Those Full-Adders uses 2 different circuits:

1. 4T and simultaneous XOR-XNOR circuits
2. NOT gates.
3. Multiplexers

10T and 22T Full Adder Circuits:



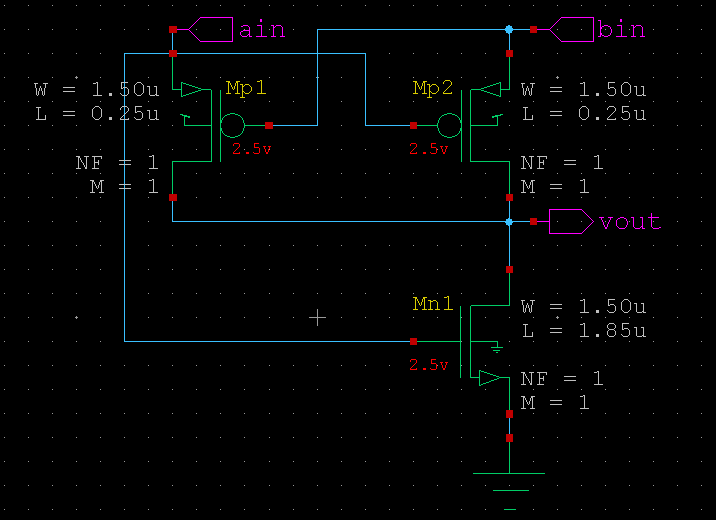
**Figure 1: 10T Full-ADDER**

**4. DATA COLLECTION AND PROCESSING:**

**4.1. DESIGNING:**

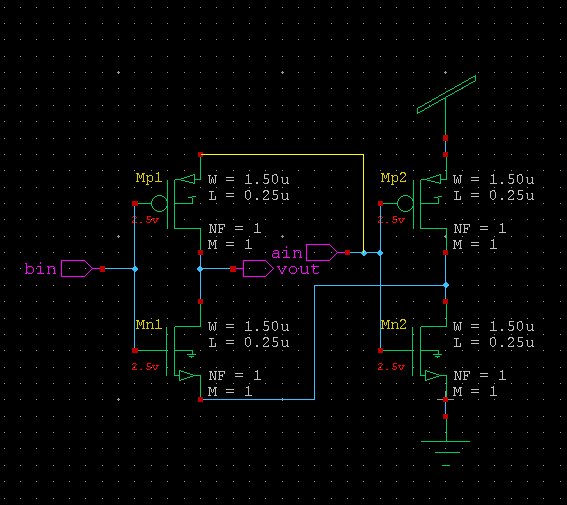
We have designed CMOS level logic gates with hybrid styles which have:

* + - * 1. **3-Transistors XOR gates**: This XOR is a 3 transistors circuit. It is not gate with a pass transistor.



**Figure 3: 3T-XOR**

* + - * 1. **4-Transistors XOR gates:** This is a not gate based XOR gate which has bin as input, ain as supply to pmos and output of ain as supply to nmos.



**Figure 4: 4T-XOR**

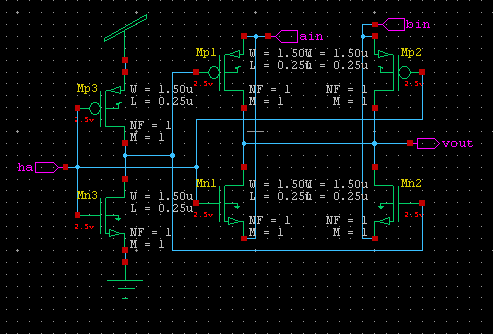
* + - * 1. Multiplexer: The multiplexer will be used for obtaining carry by using output of 3T-XOR gate as selector and ain, cin as supply.

Multiplexer (2) Equation (figure 4) = ̅̅S.a + S.c

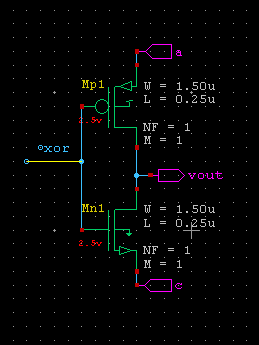
Considering S as output of XOR gate, the multiplexer equation becomes:

̅xor.a + xor.c = xnor.a + xor.c = a.b + xor.c ……… (1)

Here equation (1) is the equation for carry. In this way we calculated and designed for carry:



**Figure 5: 6T- Multiplexer**

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**Figure 6: 2T- multiplexer**

**4.2. ANALYSING:**

The designed circuits were analysed based on delay, PDP, W/L ratio, power consumption with previously existing circuits.

Few conditions are found very bizarre which have affected the output. For that reason we have changed the W/L ratio of the cmos. We choose those adequate values that provide us with the best possible results.

**NOTE:** The W/L ratio is the major parameter in the hand of the engineer to adjust the current in its transistor. This can be easily understood from the current equation of the MOS transistor in the saturation mode of operation:

**ID= (Kp W/2L) (VGS- Vtn)^2** , ... So it remains to increase W/L to increase the transistor current.

We have designed 8T Full-Adder with 3T XOR and 2T Multiplexer, 12T with 4T XOR and 2T Multiplexer and finally 14T with 4T XOR and 6T Multiplexer.

We have analysed the performance of full-adders by varying the input voltage from 5v to 3v by a factor of 0.5v.

**5. METHODOLOGY:**

We have designed CMOS level Full-Adder circuit with hybrid style which will have 3T-XOR, 4T-XOR gates, Multiplexers.

XNOR, XOR, AND and OR gates are often used in the construction of full adders. These gates uses more power in a full-adder. So the full-adder's power consumption can be minimised by reducing the transistors from those gates. Many other circuits, such as parity testing circuits and comparators, use the XOR or XNOR gate. This paper proposes high-speed and low-power XOR, XNOR using different hybrid styles.

And hence we tried to minimize these effects by changing the W/L ratio, minimizing the number of transistors and compared the power consumption, Delay, PDP, and Noise with previously existing circuits and we got better results compare the results of existing circuits.

We have designed a circuits which is having 12 transistors, 8 transistors and 14 transistors and few circuits which were from references.

Testing, Analysing and simulation of circuits is done in a Tanner tool in 250nm technology.

**6. PROCESS:**

## 8T Full Adder

We have used 3T XOR gates in 8T full adder (figure 7). 3T XOR is a combination of a CMOS inverter with a transistor. When input B=1, the output is the complement of the CMOS inverter and when B=0, the output acts an inverter. When A=1 and B=0, both PMOS and NMOS are switching on, because of the W/L ratio of PMOS threshold voltage is minimum comparative NMOS that the reason PMOS is conducted first & the output is same as the input A. As we got the output of 3T XOR gate, the output is connected to the first input of the second 3T XOR gate with C as the second input. By this we will get the sum from the output of the second 3T XOR gate.

Carry is obtained from the multiplexer. Here the input is connected with the output of AxorB. When AxorB=1, then carry=C and if AxorB=0, then carry=A.

## 12T Full Adder

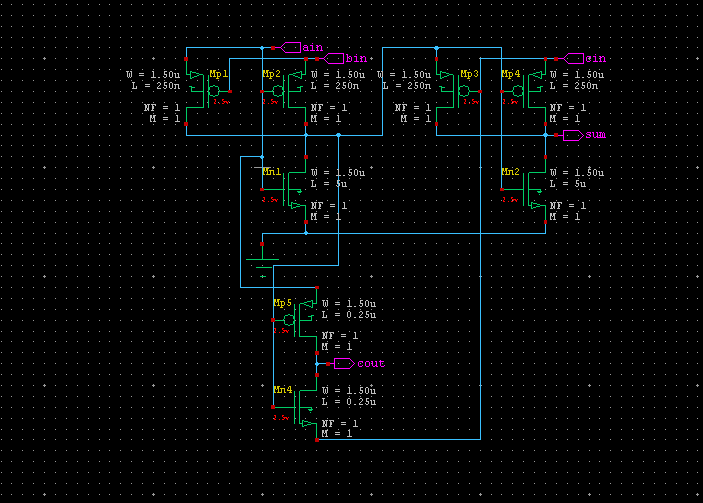
We have used 4T-XOR gate in 14T Full Adder circuit (figure 9). The 4T-XOR gate is two not gate based circuit. Bin is the input, ain is the supply for pmos and complement of ain is the supply for nmos. To obtain the complement of ain we have used another not gate.

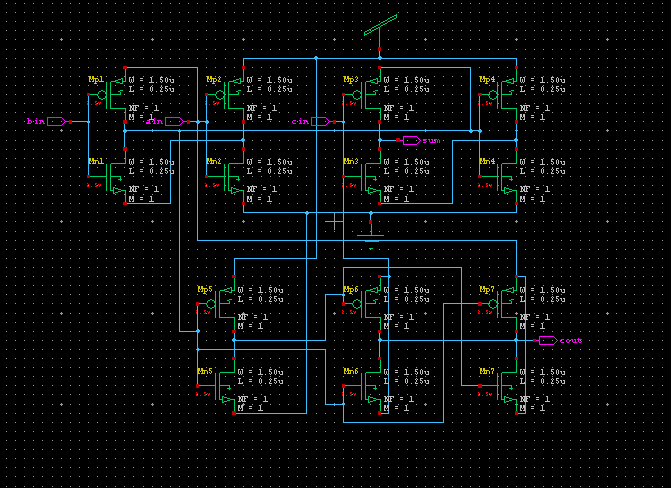
To obtain carry we have use a not gate based multiplexer by giving A input as supply to pmos, B as supply to nmos and XNOR as input.

## 14T Full Adder

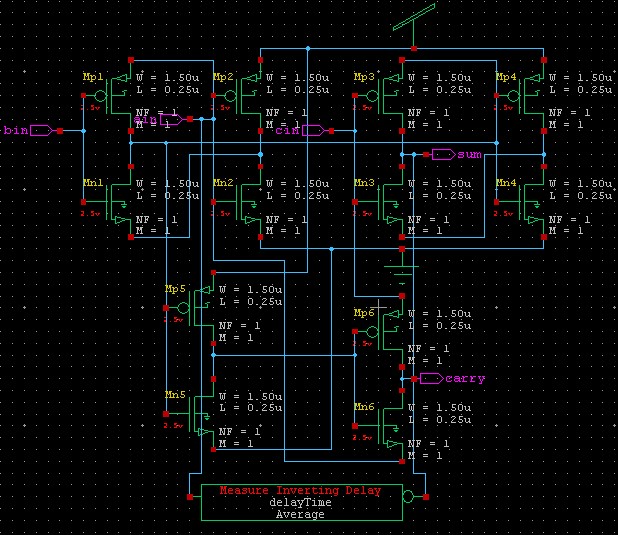
We have used 4T-XOR gate in 14T Full Adder circuit (figure 8). The 4T-XOR gate is two not gate based circuit. Bin is the input, ain is the supply for pmos and complement of ain is the supply for nmos. To obtain the complement of ain we have used another not gate. To obtain carry we use same operation as in 8T.

**7. FULL-ADDER CIRCUITS:**

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**Figure 7: 8T Full-Adder **

**Figure 8: 14T Full-Adder**

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**Figure 9: 12T Full-Adder**

**8. SIMULATION RESULTS:**

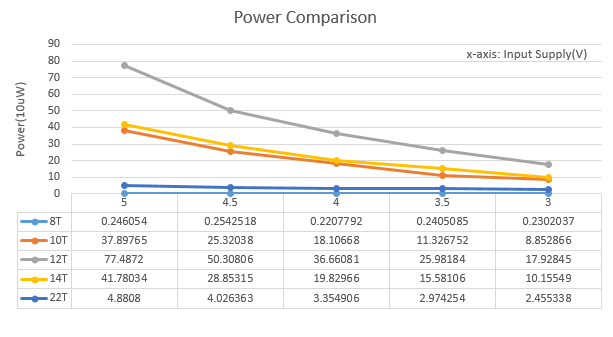
All simulations were done in Tanner tool in 250nm(16.3) technology. The power supply used for simulations was 5v. Below Table shows the simulation results of all full adders.

8T has minimum delay and PDP

**Table 1: Simulation results of all Full-Adders at 5V**

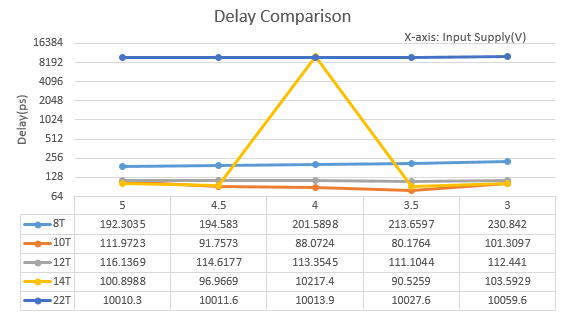
|  |  |  |  |
| --- | --- | --- | --- |
| **Circuits** | **Power**  **(W)** | **Delay**  **(s)** | **PDP**  **(fJ)** |
| 8T | 2.46e-006 | 192.3035p | 0.4731 |
| 12T | 7.74e-004 | 116.1369p | 89.89912 |
| 14T | 4.178e-004 | 100.8988p | 42.1558 |
| 10T | 3.789e-004 | 111.9723p | 42.4348 |
|  |  |  |  |

**9. COMPARISONS:**

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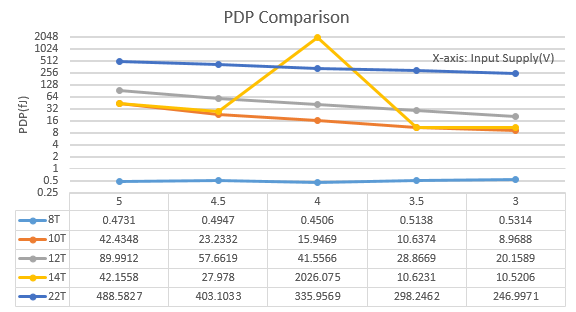
**Power comparisom of all the adders**

**Figure 10: Power Comparison**

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**Figure 11 ; DELAY COMPARISON**

**:Delay Comparison**

****

**FIG 12:PDPCOMPARISON**

**10. OUTCOMES:**

Technical Feasibility

1. Very less number of gates
2. Minimal Delay
3. Low Power Consumption
4. Low PDP
5. Better result than the previous existing circuits

Commercial Feasibility

1. Small in area
2. Easy to Design

**11. APPLICATIONS:**

* Basic building block of on-chip libraries.
* Configured according to designed complexity of arithmetic and numeric computations.
* In processors and other kind of computing devices, adders are used in the arithmetic logic units.
* Adders also used in the other parts of the processors, where they are used to calculate addresses, table indices, and similar operations.
* It is also used in DSP.
* Adders are used in graphical related applications, where there is very much need of complex computations, the GPU uses optimized ALU which is made up of full adders, other circuits as well.
* Basically, Full-Adder is used in designing ALU and this ALU is used for wide variety of applications from designing CPU to GPU.

**12. FUTURE TASKS:**

We will try to obtain maximum output voltage at the output and also try to minimize the PDP.

These factors will be obtain by varying W/L ratio and by varying input power supply.

**13. CONCLUSION:**

Due to the use of modern XOR-XNOR, multiplexer circuits the proposed full-adders have high speed and lower power consumption. From simulation results, the proposed full adders have low power consumption, less delay and best power delay product compared to existing circuits. The proposed full-adders works good at various VDD values from 3v – 5v. And even the full adders work reliably at most of the conditions given.

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