BTP – 1 PRESENTATION

DESIGN OF LOW NOISE AMPLIFIER (LNA)

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Agenda:

- What is LNA and What are it’s requirements ?
- Circuit Diagram
- Calculation of unknown parameters
- Simulation results
- Performance Summary
- Conclusion
- Further Scope

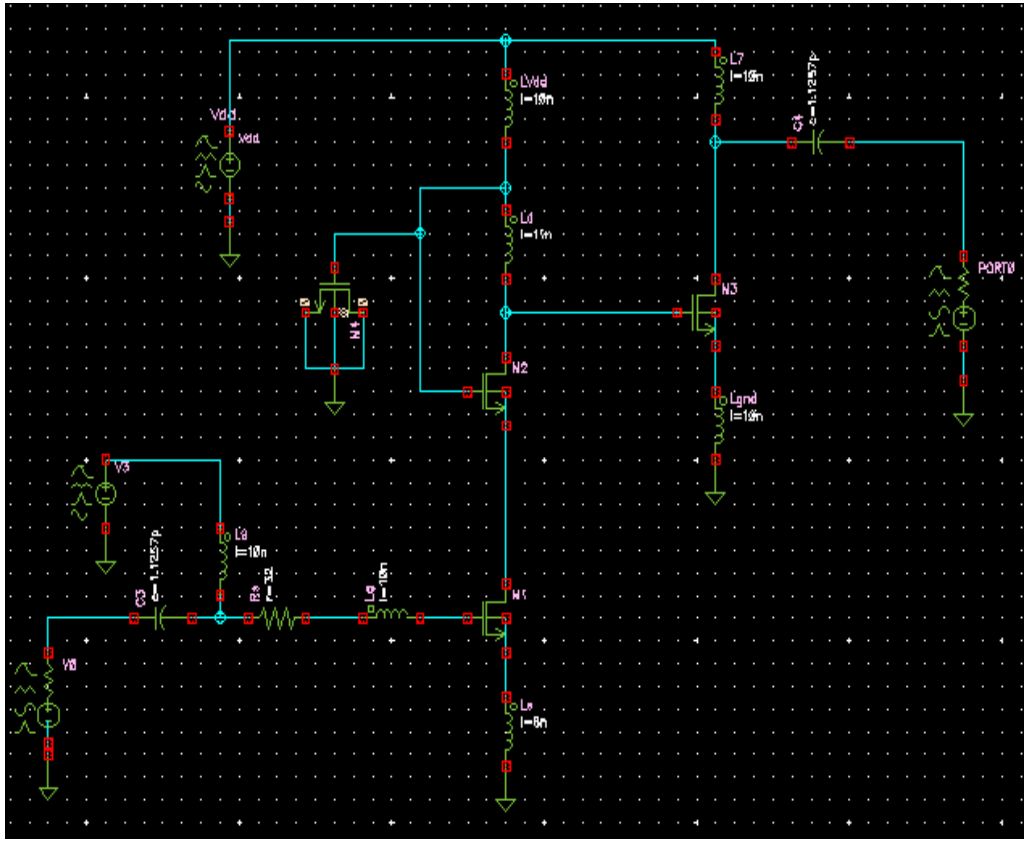
What are it’s Requirements ?

What is LNA ?

- A Low Noise Amplifier is a critical component in the Radio Frequency (RF) and microwave communication systems and responsible for **amplifying weak signals while minimizing the introduction of noise .**

- **Noise Figure:** The noise figure is given by total output noise power divided by noise power at output due to input source. Low NF is desirable because it indicates that device adds less noise to incoming signal. Typically NF < 2dB.
- **Gain:** A higher gain in an LNA allows it to detect and amplify weaker signals. Typically S21 > 15dB is good.
- **Input matching:** LNA is designed to have 50 Ohms resistive input impedance (since BPF operate with 50 Ohms) and 50 Ohms output impedance to drive the image-reject filter.
- **Linearity:** To maintain linear relation between input & output signals by prevention of intermodulation distortion & gain compression. IIP3 > -10dBm is good.

Circuit Diagram:



Schematic of Inductive Source Degenerated Low Noise Amplifier (in Cadence)

- The amplifier is 2-stage, cascoded architecture.
- M2, common-gate transistor, plays 2 important roles by increasing reverse isolation of the LNA: lowers LO leakage, improves stability of circuit by minimizing feedback from output to input.
- M3 serves as open drain output driver providing gain to overall LNA.
- Four of the inductors shown (Ls, L_gnd, L_vdd, L_out) are formed by bondwire inductances.
- Of these four, Ls is the only one whose specific value is significant in the operation of the amplifier, since it sets the input impedance of the LNA.
- L_vdd aids in supply filtering with M4, which acts as supply bypass capacitor.

Calculation of Unknown parameters:

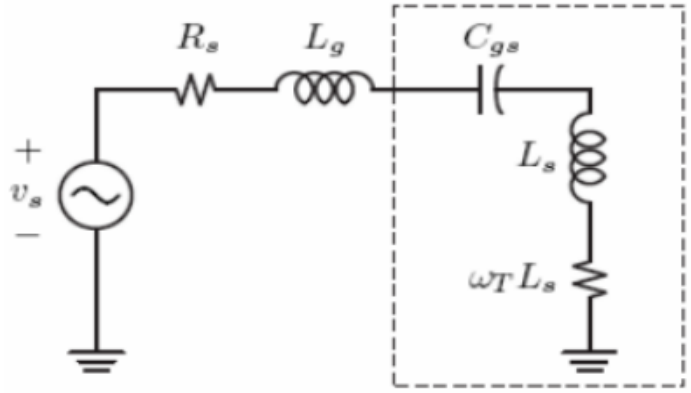
- The input impedance (Z_in):

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{m1}L_s}{C_{gs}}$$

- At resonance, impedance is purely real and proportional to Ls.

$$Z_{in}(jw_0) = R_s = \frac{g_{m1}}{C_{gs}}L_s = w_T L_s$$

$$(L_g + L_s)C_{gs} = \frac{1}{w_0^2}$$



Matching occurs when Z_in(jw0) = R_s.

- Gate inductance Lg is used to set resonance frequency once Ls is chosen to satisfy criterion of 50 – Ohms input impedance.
- The channel noise is white and the dominant noise contributor internal to the LNA is the channel current noise of the first MOS device.

- The noise factor (F) of LNA by neglecting correlation of the gate noise and drain current noise is:
- R_l (series inductor resistance), R_g (series gate resistance) have been neglected relative to the source resistance R_s.

$$F = 1 + \frac{R_l + R_g}{R_s} + \gamma g_{d0} R_s \left(\frac{w_0}{w_T}\right)^2$$

$$G_m = g_{m1} Q_{in} = \frac{g_{m1}}{w_0 C_{gs}(R_s + w_T L_s)} = \frac{w_T}{2 w_0 R_s}$$

γ is the coefficient of channel thermal noise.

- The noise factor (F) of LNA by Considering correlation of the gate noise and drain current noise is:
- The effect of induced gate noise is to modify the noise contribution of the device in proportion to χ.
- Therefore, the optimal noise figure (lowest NF) will be happened for a particular Q_L.
- Q_Lopt will be independent from the frequency of operation and around 4.5 while keeping power dissipation as constant.

$$F = 1 + \frac{R_l + R_g}{R_s} + \frac{\gamma \chi}{\alpha Q_L}\left(\frac{w_0}{w_T}\right)$$

$$\chi = 1 + 2|c| Q_L \sqrt{\frac{\delta \alpha^2}{5\gamma}} + \frac{\delta \alpha^2}{5\gamma}(1 + Q_L^2)$$

$$Q_L = Q_{Cgs} = \frac{1}{w_0 R_s C_{gs}}$$

δ is the coefficient of gate noise,
c is the correlation coefficient.

D.K. Shaeffer & T.H. Lee. A 1.5-v, 1.5-ghz cmos LNA. IEEE Journal of Solid-State Circuits, 32(5):745–759, 1997.

Choosing QL = 4.5

w0 = 1.5 GHz, Rs = 50 Ohms

$$Q_L = \frac{1}{w_0 R_s C_{gs}} \Rightarrow C_{gs} = \frac{1}{Q_L w_0 R_s} \Rightarrow C_{gs} = 0.4716pF$$

$$C_{gs} = \frac{2}{3} C_{ox} W L \Rightarrow W = \frac{3C_{gs}}{2C_{ox}L} \Rightarrow W = 460um$$

The drain current Id is assumed to be 10mA

$$I_d = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})^2$$

$$\Rightarrow V_{gs} = 0.6522V$$

$$g_m V_{gs} = \frac{i_d}{2} \Rightarrow g_m = \frac{i_d}{2V_{gs}} \Rightarrow g_m = 7.67mS$$

$$w_T = \frac{g_m}{C_{gs}} \Rightarrow w_T = 16.256GHz$$

$$L_s = \frac{R_s}{w_T} \Rightarrow L_s = 3.076nH$$

From the g_m and V_gs, the values of wT , Ls, Lg are calculated.

$$(L_g + L_s)C_{gs} = \frac{1}{w_0^2} \Rightarrow L_g = \frac{1}{w_0^2 C_{gs}} - L_s \Rightarrow L_g = 20.797nH$$

$$(C_{d2} + C_{gs3})L_d = \frac{1}{w_0^2}$$

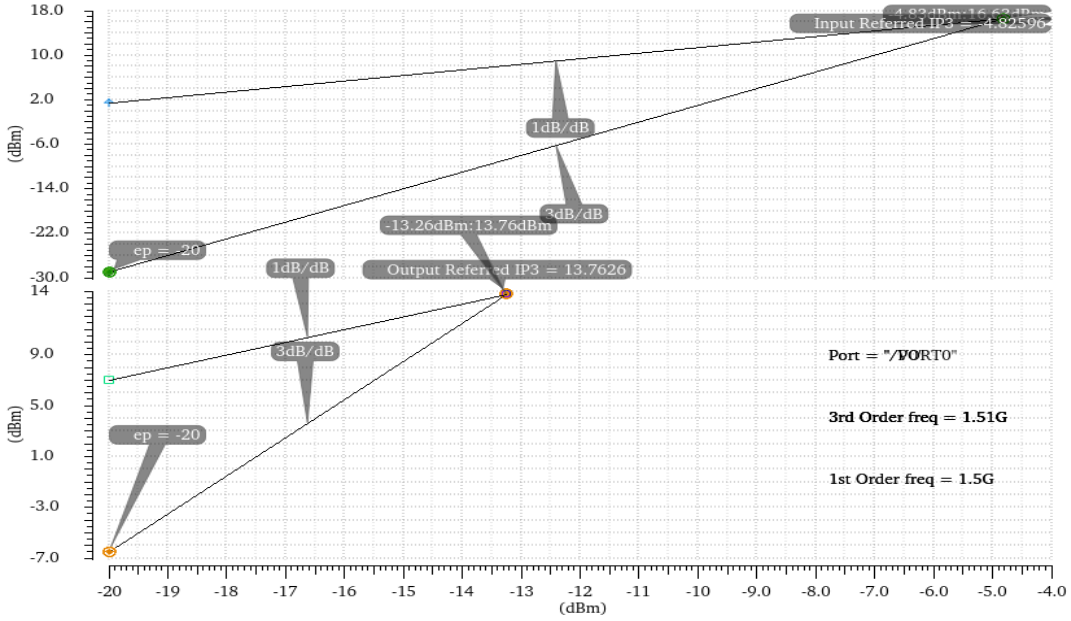
$$\Rightarrow (\frac{1}{2}C_{ox}W_2L + C_{gd0}W_2 + \frac{2}{3}C_{ox}W_3L)L_d = \frac{1}{w_0^2} \Rightarrow L_d = 11.9nH$$

Inductor Ld resonates with total capacitance at the drain of M2 including C_gs of M3.

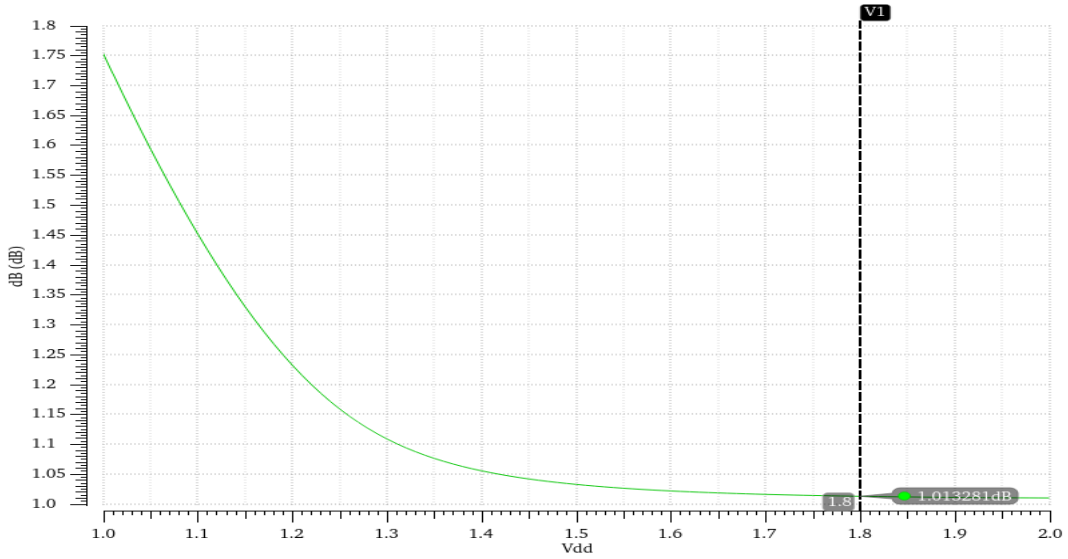
MOS Transistor (180nm) features

Parameter	Value
C_{ox}	8.57 fF/um^2
$\mu_n C_{ox}$	387 $\mu A/V^2$
L	0.18um
C_{gd0}	7.7e-10F/um
V_{th}	0.51V
γ	3
δ	0.01
$\|c\|$	0.395
α	0.75

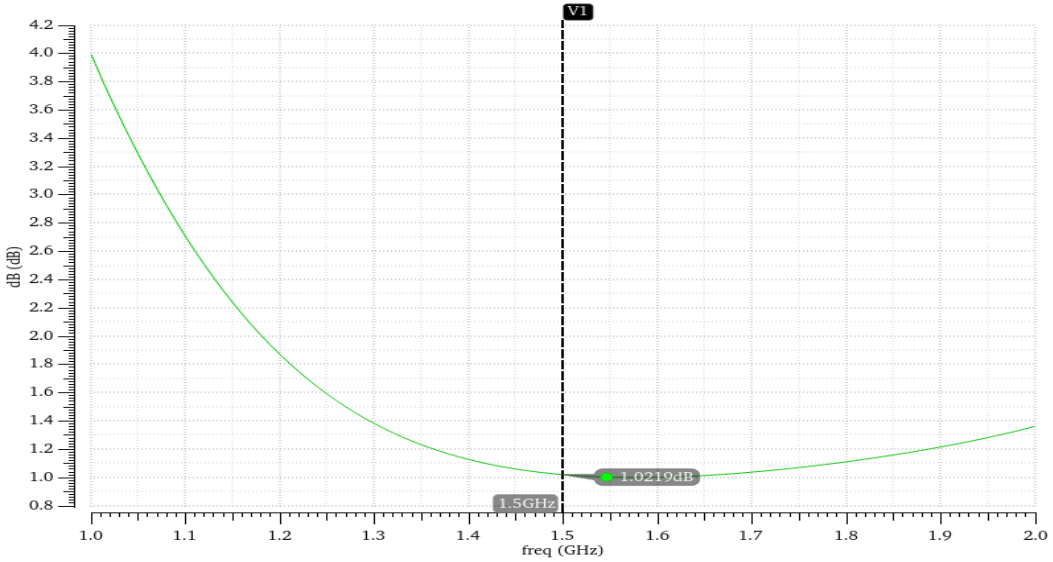
Simulation results:



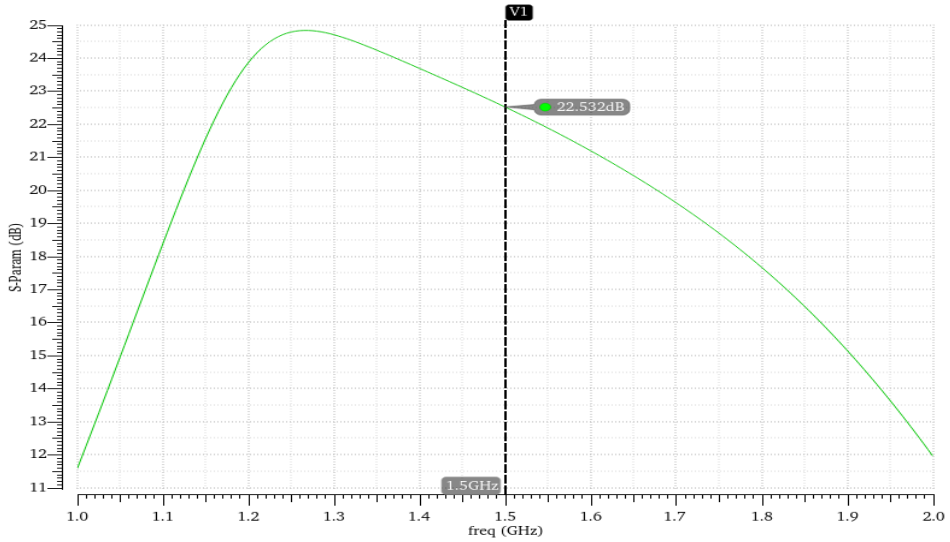
Input & Output IP3 points



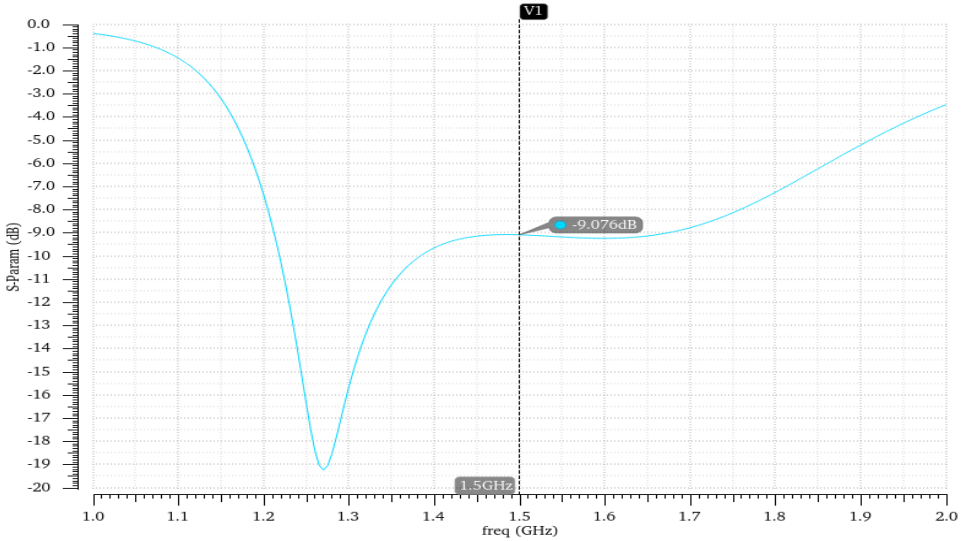
NF Vs Source Voltage



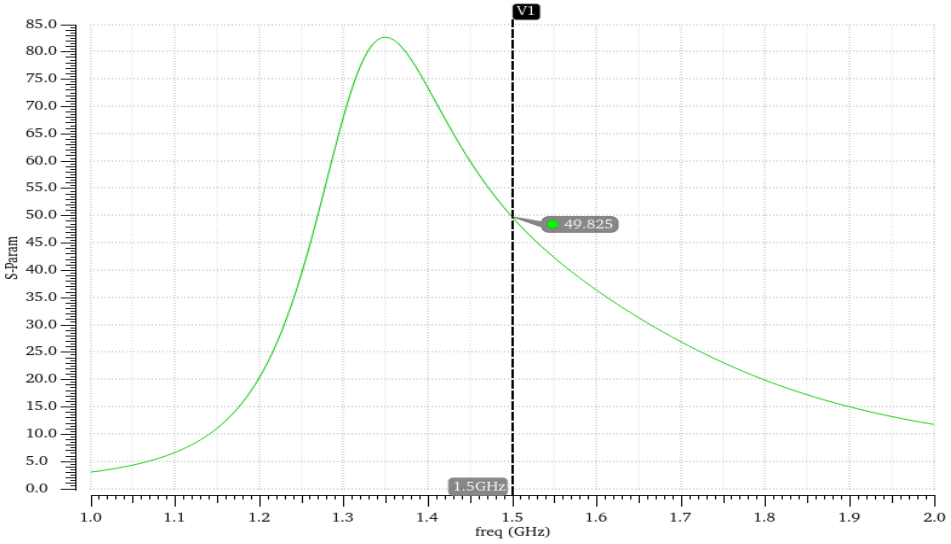
NF Vs Frequency



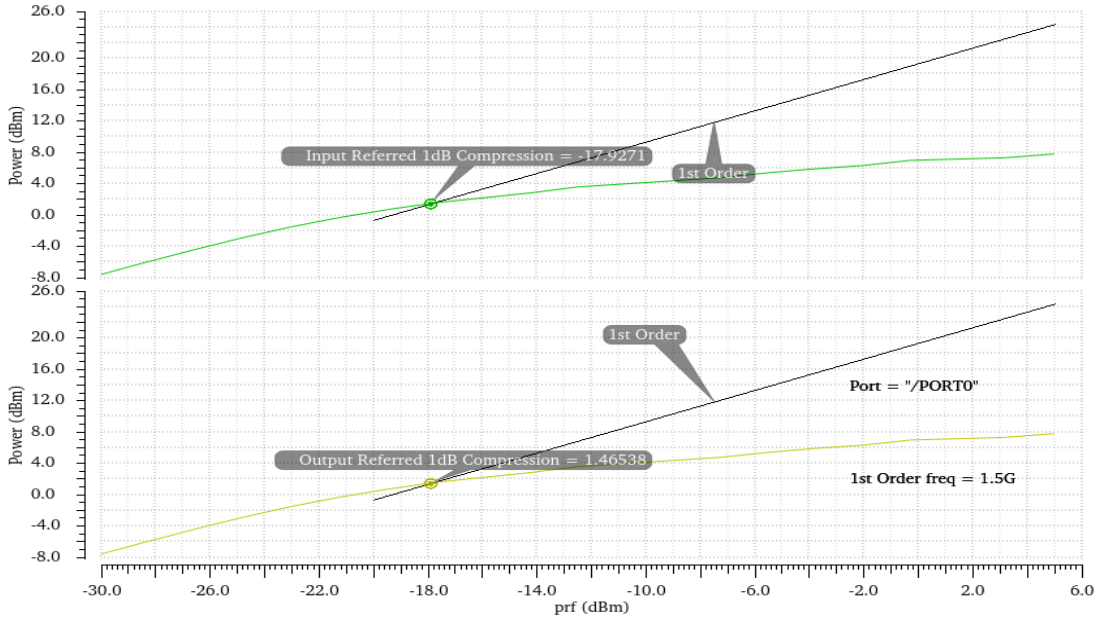
S21 Plot



S11 Plot



Re (Z_in) vs Frequency



Input & Output 1dB Compression points

Performance Summary:

Metric	Simulation result
Frequency	1.5GHz
NF	1.02dB
S21	22.53dB
S11	-9.07dB
IIP3	-4.826dBm
OIP3	13.763dBm
Re(Z_{in})	49.825 Ohms
Current	17.9mA
1dB Compression point (input)	-17.927dBm
1dB Compression point (output)	1.465dBm
Supply	1.8V

	Calculated Value	Simulated Value
M_1	$460\mu m/0.18\mu m$	$460\mu m/0.18\mu m$
M_2	$460\mu m/0.18\mu m$	$460\mu m/0.18\mu m$
M_3	$230\mu m/0.18\mu m$	$230\mu m/0.18\mu m$
L_g	20.797nH	10nH
L_s	3.076nH	8nH
L_d	11.9nH	11nH
I_d	10mA	17.9mA

Conclusion:

- A Inductive Source degenerated low noise amplifier in a 0.18 - um CMOS process have been demonstrated .
- The designed LNA demonstrates commendable performance characteristics, such as low noise figure of 1.02 dB, high gain of 22.53 dB. The design process involved careful trade-offs between various parameters, including gain and noise figure.
- Optimization techniques were employed to achieve the desired balance and meet the specifications outlined in the design requirements.
- Theoretical analysis of the amplifier architecture has demonstrated the fundamental role of induced gate noise, which is essential in defining the minimum noise figure.

Further scope:

- Having comprehensively explored the schematic design of the low noise amplifier (LNA), the next phase will focus on the crucial aspect of layout design and its impact since it serves as the bridge between theoretical electrical design and the physical realization of the circuit on a printed circuit board (PCB).
- Extending the design of Low Noise Amplifier to non-ideal inductors, checking the basic LNA requirements and working for the bandwidth extension.
- As technology continues to advance, future work could explore the application of more advanced technology nodes for further performance improvement.