BTP – 2 PRESENTATION

DESIGN OF GILBERT CELL (MIXER) AND LNA

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Agenda:

- What is Mixer and LNA, What are it’s requirements ?
- Circuit Diagram
- Calculation of unknown parameters
- Simulation results
- Performance Summary
- Conclusion
- Further Scope

What are it’s Requirements ?

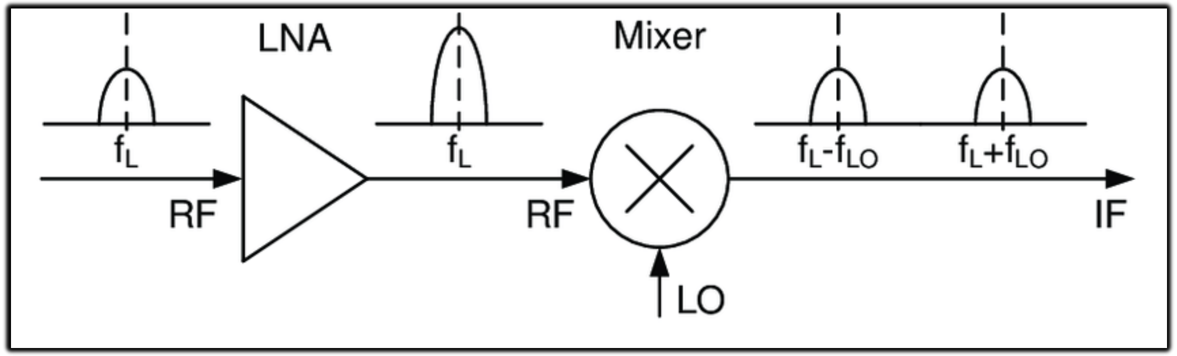
What is LNA ?

- A Low Noise Amplifier is a critical component in the Radio Frequency (RF) and microwave communication systems and responsible for **amplifying weak signals while minimizing the introduction of noise .**

- **Noise Figure:** The noise figure is given by total output noise power divided by noise power at output due to input source. Low NF is desirable because it indicates that device adds less noise to incoming signal. Typically NF < 2dB.
- **Gain:** A higher gain in an LNA allows it to detect and amplify weaker signals. Typically S21 > 15dB is good.
- **Linearity:** To maintain linear relation between input & output signals by prevention of intermodulation distortion & gain compression. IIP3 > 0dBm is good.

What is Mixer ?

- A Mixer is a critical component in the RF and microwave communication systems which is **responsible to convert the incoming signal (after it has been amplified by the LNA) to an intermediate frequency (IF).**



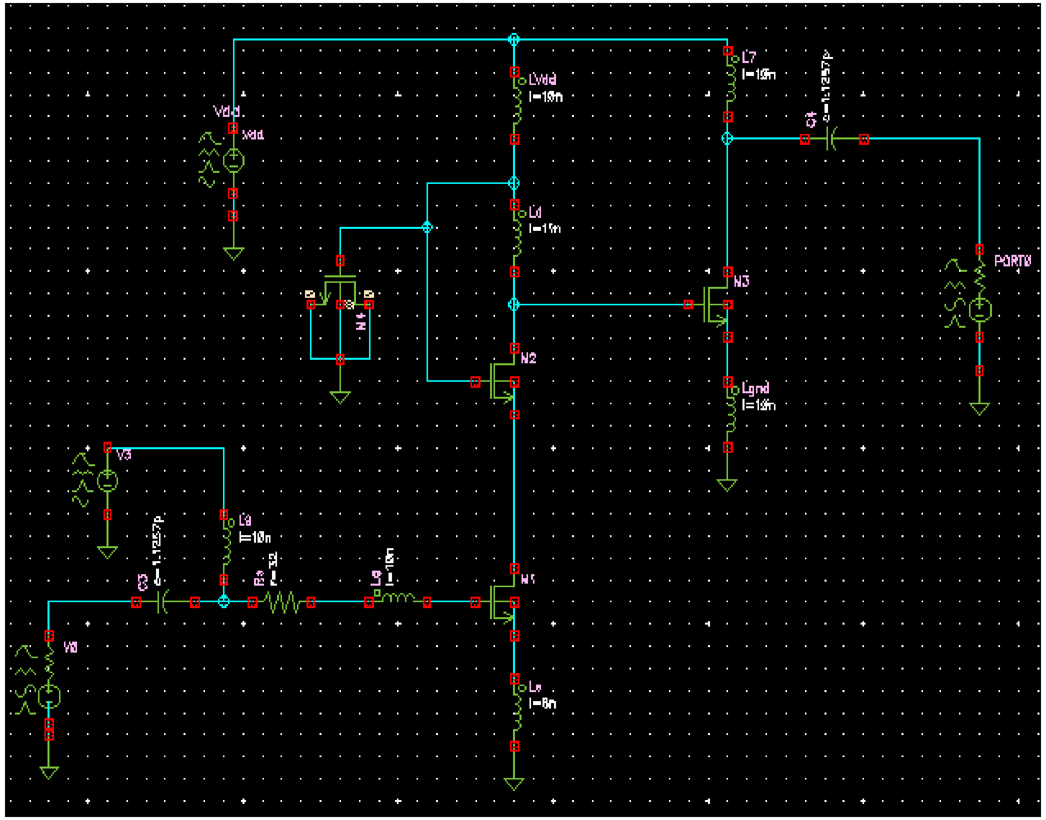
What are it's Requirements ?

- **Noise Figure:** From the specification of total noise figure of (LNA + Mixer), the NF of Mixer is estimated from NF of cascaded systems as:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + .. \frac{F_N - 1}{\pi_{n=1}^{N-1} G_n}$$

- **Conversion Gain:** Defined as ratio of the rms voltage of signal at IF frequency to the rms voltage of signal at RF frequency.
- **Linearity:** To maintain linear relation between input & output signals by prevention of intermodulation distortion & gain compression. IIP3 > 0dBm is good.

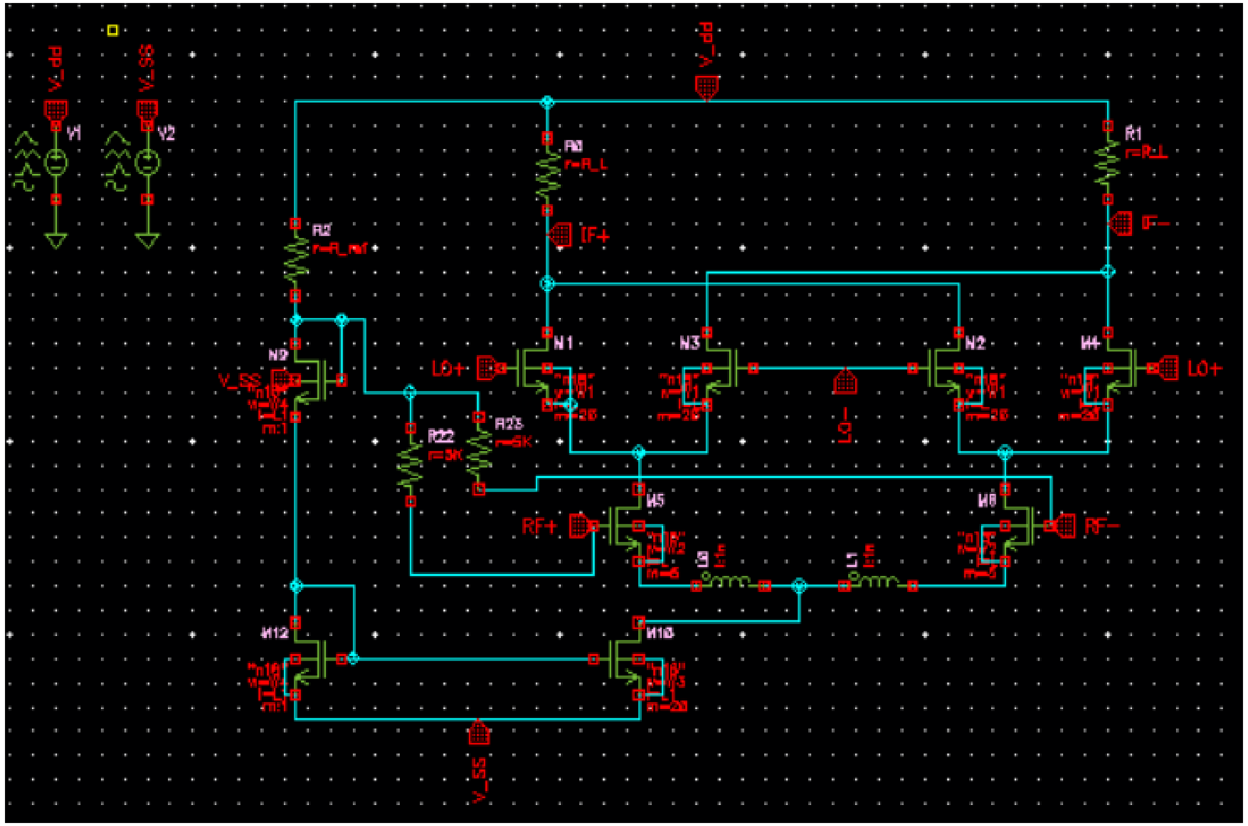
Circuit Diagram of LNA:



Schematic of Inductive Source Degenerated Low Noise Amplifier (in Cadence)

- The amplifier is 2-stage, cascoded architecture.
- **M2**, common-gate transistor, plays 2 important roles by increasing the reverse isolation of LNA: lowers LO leakage, improves the stability of circuit by minimizing the feedback from output to input.
- **M3** serves as open drain output driver providing gain to overall LNA.
- Out of 4 inductors, **Ls** is the only one whose specific value is significant in the operation of the amplifier, since it sets the input impedance of the LNA.
- **L_Vdd** aids in supply filtering with **M4**, which acts as supply bypass capacitor.

Circuit Diagram of Mixer:



Schematic of Gilbert Mixer Cell (in Cadence)

- The RF signal is applied to M5 and M6 which perform a voltage to current conversion.
- Performance can be improved by adding degeneration resistors or inductors, Inductor degeneration is usually preferred because it has no thermal noise to degrade Noise Figure.
- M1 to M4, multiplying the linear RF signal current from M5 and M6 with the LO signal applied across M1 to M4 which provide the switching function.
- The two load resistors form a current to voltage transformation giving differential output IF signals.

Calculation of Unknown parameters of Mixer:

Assuming current sink of 6mA to drive the mixer. So, 3mA of current is split between the differential pair.

RF Stage: The gain is proportional to the transconductance of the RF pairs. By knowing gm, the W can be calculated.

$$g_m = \frac{\pi(gain)}{2R_L} = 12.51mS$$

$$W_{5,6} = \frac{g_m^2 L}{K I_{DS}} = 13.7\mu m$$

LO Stage: For proper switching, V_gs needed to be just slightly larger than V_t and W to be large. Assuming V_t is 0.7V, V_gs was chosen to be 0.8V.

$$W_{1,2,3,4} = \frac{L I_{ds}}{K(V_{gs} - V_T)^2} = 316\mu m$$

A small current of 100µA was chosen for the reference current.

$$W_{10} = \frac{L I_{ss}}{K(V_{gs} - V_T)^2} = 316\mu m$$

From concept of current mirror, W of reference mosfet is calculated.

$$W_{12} = \frac{W_{10} I_{ref}}{I_{ss}} = 6\mu m$$

$$R_{ref} = \frac{3.3 - 0.810}{100\mu A} = 25KOhms$$

Calculation of Unknown parameters of LNA:

The input impedance (Z_in):

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{m1}L_s}{C_{gs}}$$

$$Z_{in}(jw_0) = R_s = \frac{g_{m1}}{C_{gs}}L_s = w_T L_s$$

$$(L_g + L_s)C_{gs} = \frac{1}{w_0^2}$$

At resonance, impedance is purely real and proportional to Ls.

The optimal noise figure (lowest NF) will be happened for a particular Q_L.

$$Q_L = \frac{1}{w_0 R_s C_{gs}} \Rightarrow C_{gs} = \frac{1}{Q_L w_0 R_s} \Rightarrow C_{gs} = 0.2947pF$$

The drain current I_d is assumed to be 10mA

$$C_{gs} = \tfrac{2}{3}C_{ox}WL \Rightarrow W = \frac{3C_{gs}}{2C_{ox}L} \Rightarrow W = 287um$$

$$I_d = \tfrac{1}{2}\mu_n C_{ox}\tfrac{W}{L}(V_{gs} - V_{th})^2 \Rightarrow V_{gs} = 0.6902V$$

$$g_m V_{gs} = \tfrac{i_d}{2} \Rightarrow g_m = \frac{i_d}{2V_{gs}} \Rightarrow g_m = 7.245mS$$

$$w_T = \frac{g_m}{C_{gs}} \Rightarrow w_T = 24.583GHz$$

$$L_s = \frac{R_s}{w_T} \Rightarrow L_s = 2.034nH$$

$$(L_g + L_s)C_{gs} = \frac{1}{w_0^2} \Rightarrow L_g = \frac{1}{w_0^2 C_{gs}} - L_s \Rightarrow L_g = 12.888nH$$

The total capacitance at the drain of M2, including the Cgs of M3, is in resonance with the inductor Ld.

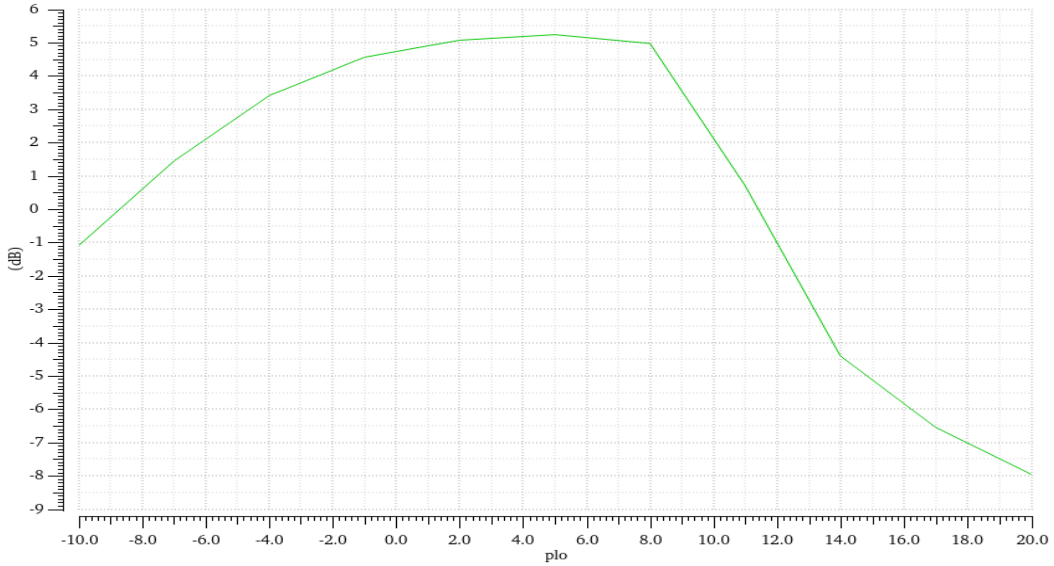
$$(C_{d2} + C_{gs3})L_d = \frac{1}{w_0^2}$$

$$\Rightarrow (\tfrac{1}{2}C_{ox}W_2L + C_{gd0}W_2 + \tfrac{2}{3}C_{ox}W_3L)L_d = \frac{1}{w_0^2} \Rightarrow L_d = 7.461nH$$

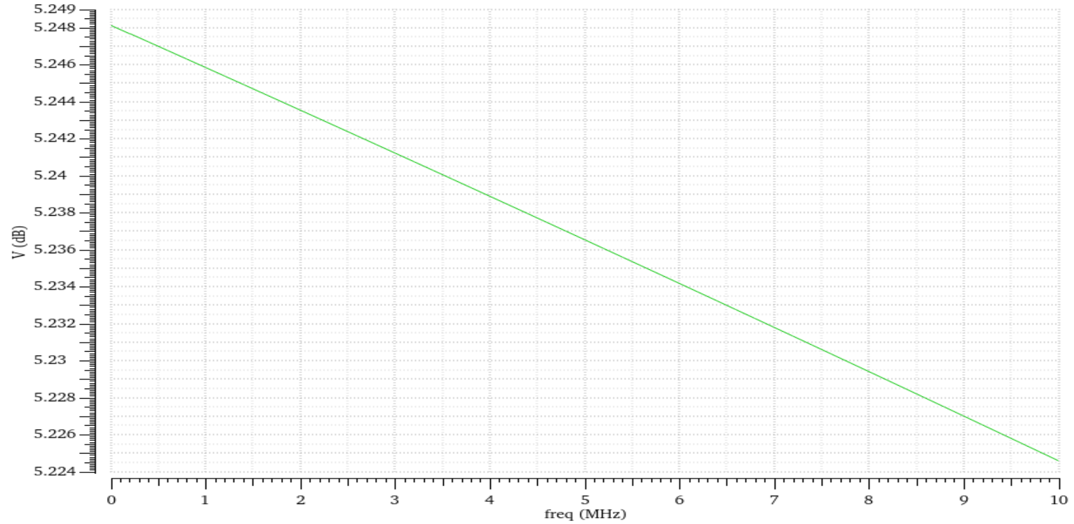
Simulation results of Mixer:

	Calculated Value	Simulated Value
$M_{1,4}$	$320\mu m/0.18\mu m$	$320\mu m/0.18\mu m$
$M_{2,3}$	$320\mu m/0.18\mu m$	$320\mu m/0.18\mu m$
$M_{5,6}$	$13.7\mu m/0.18\mu m$	$125\mu m/0.18\mu m$
M_{10}	$320\mu m/0.18\mu m$	$200\mu m/0.54\mu m$
$M_{9,12}$	$5.3\mu m/0.18\mu m$	$5\mu m/0.54\mu m$
R_L	267 Ohms	300 Ohms
R_{ref}	25K Ohms	15K Ohms
$R_{22,23}$	3K Ohms	5K Ohms

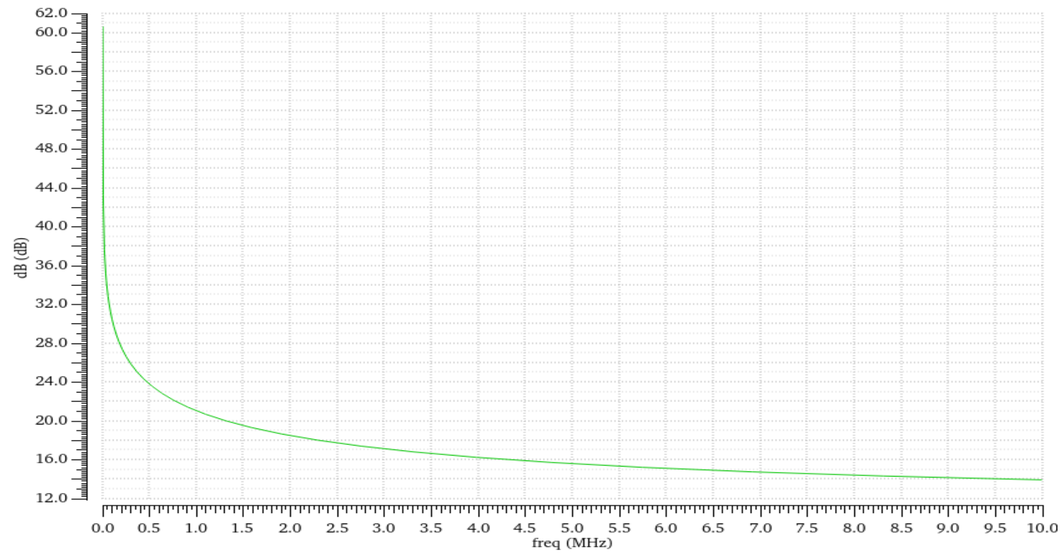
Calculated and Simulated Values of Mixer



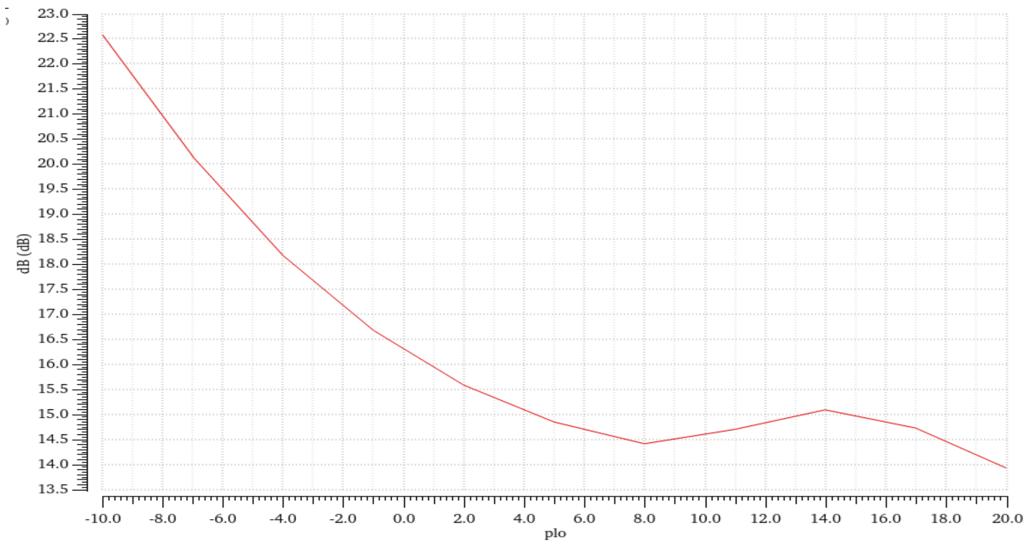
Conversion gain Vs LO Signal Power



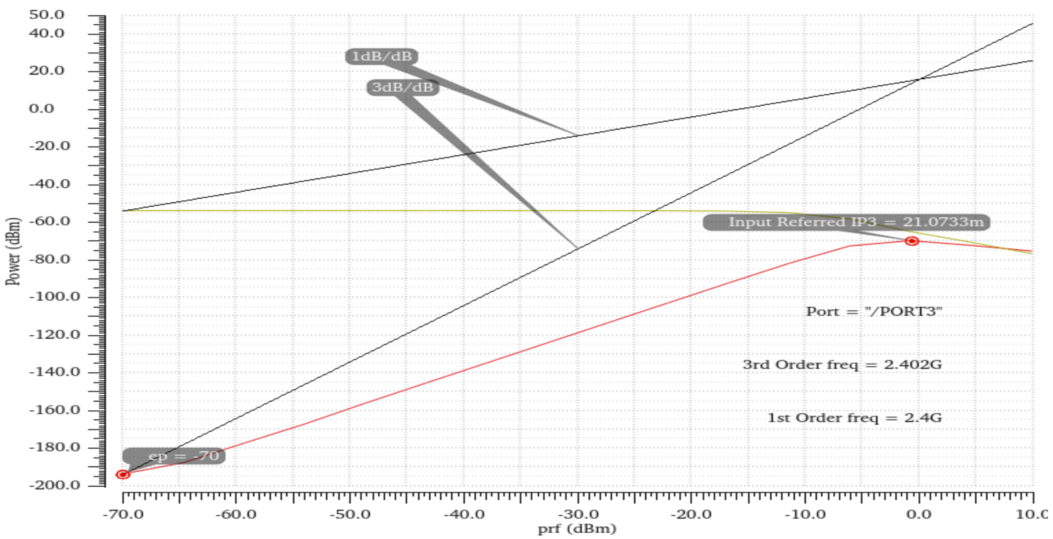
Conversion gain Vs RF frequency



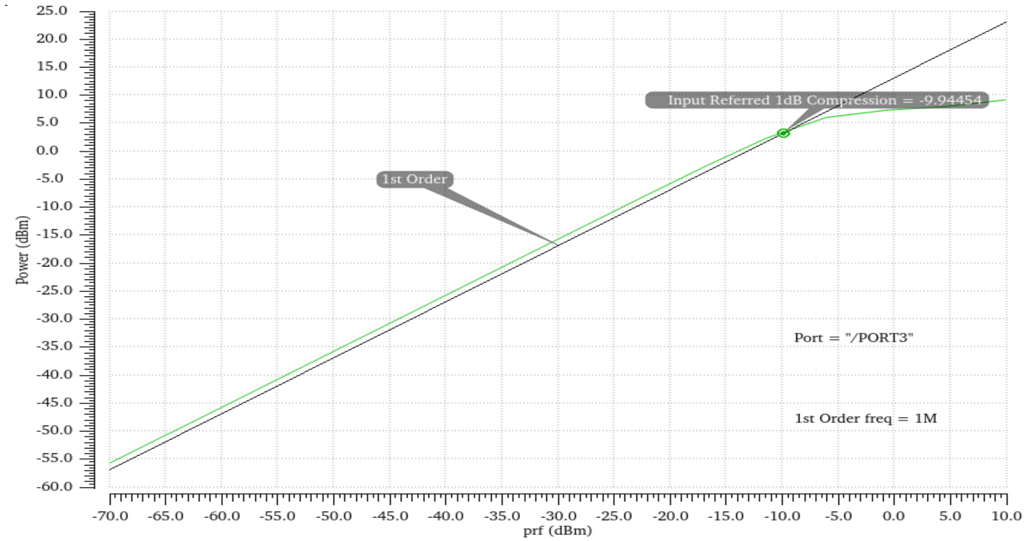
Noise Figure Vs frequency



Noise Figure Vs LO Signal Power

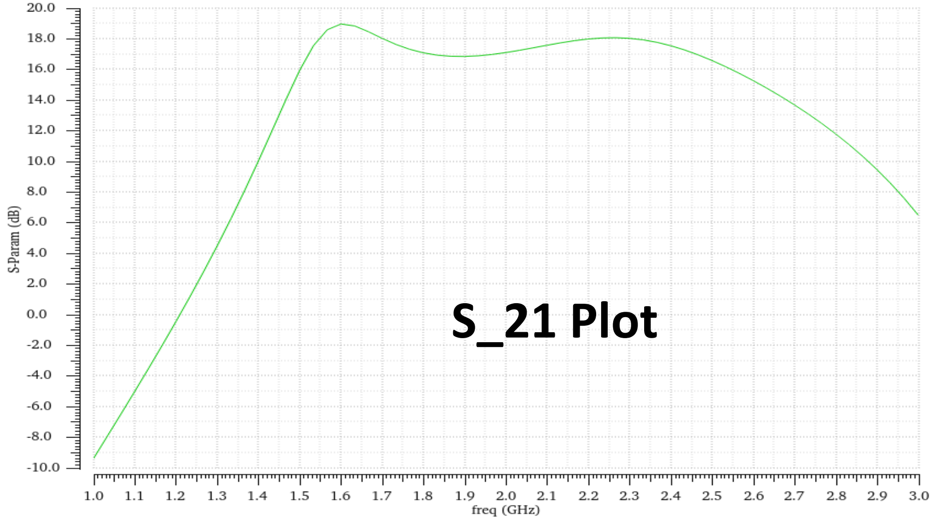


Input referred IP3 Point

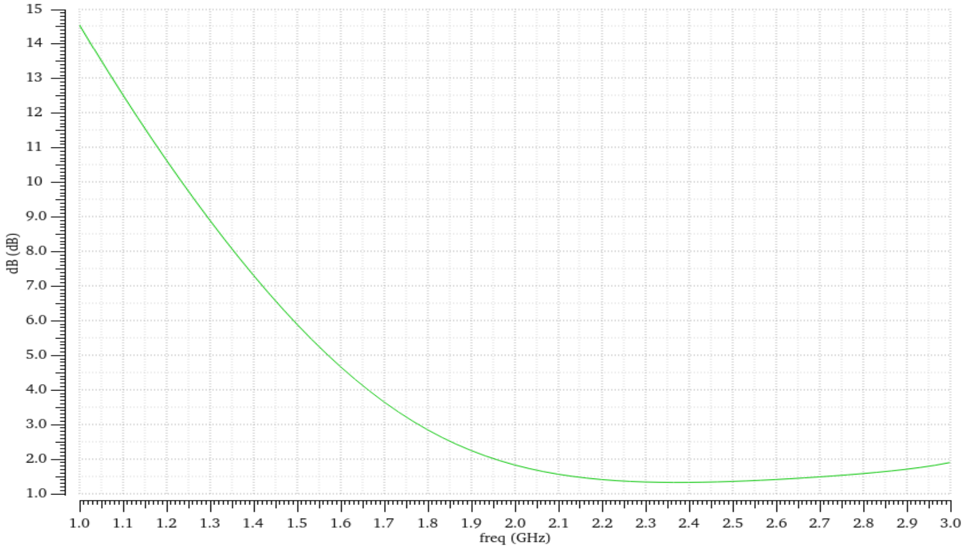


Input referred 1dB compression point

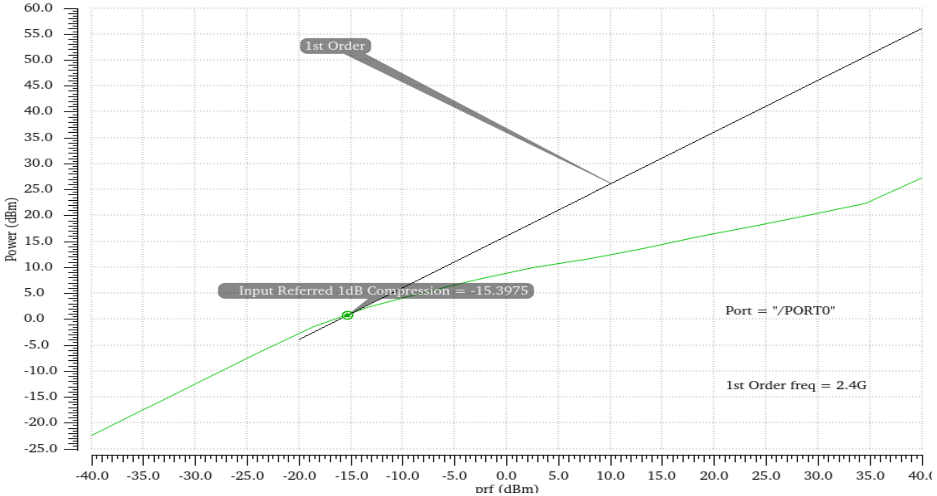
Simulation results of LNA:



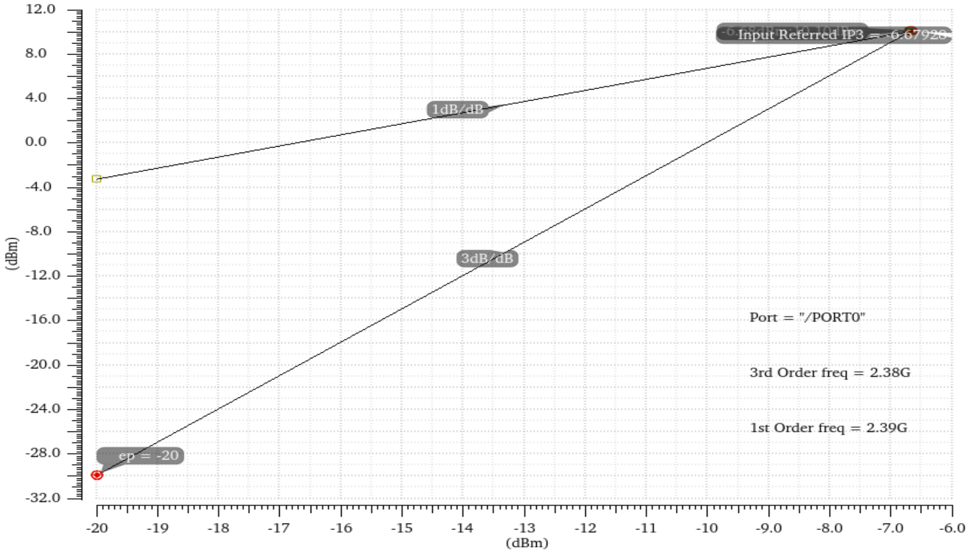
S_21 Plot



Noise Figure Vs Frequency



Input referred 1dB compression point



Input referred IP3 Point

Performance Summary:

Metric	[3]	[5]	[1]	This work
RF BW (GHz)	2.4 - 10.7	1 - 10	@2.4	1 - 7
IF BW (GHz)	@0.05	0.1 - 1	@0.15	0.01 - 0.5
CG (dB)	1.8 - 4.8	3 - 8	13.8	7 - 8
$P_{LO}(dBm)$	-5	0	NA	5
NF (dB)	NA	11.3 - 15	15.5	13 - 15
IIP3 (dBm)	4 - 6.9	-7 - -4	-2	0.021
CMOS Proces	$0.18\mu m$	$0.13\mu m$	$0.18\mu m$	$0.18\mu m$

Performance Summary of Mixer

	Calculated Value	Simulated Value
$M_{1,2}$	$287\mu m/0.18\mu m$	$280\mu m/0.18\mu m$
M_3	$143\mu m/0.18\mu m$	$140\mu m/0.18\mu m$
L_g	12.888nH	4nH
L_s	2.034nH	4nH
L_d	7.461nH	7nH

Calculated and Simulated Values of LNA

Metric	Simulation result
Frequency	2.4GHz
NF (dB)	1.42
S21 (dB)	17.9
1dB Compression point (dBm)	-15.397
IIP3 (dBm)	6.679

Performance Summary of LNA

Conclusion:

- A CMOS Gilbert cell Mixer has been demonstrated in standard 0.18 CMOS technology and simulated using spectre-RF simulator on Cadence.
- The proposed mixer also exhibits a measured IF bandwidth from 10 MHz to 500 MHz with a conversion gain variation less than 2 dB. The measured IP 1 dB, IIP3 and noise figure are better than -9 dBm, 0 dBm, and 15 dB throughout the entire RF band.
- The designed LNA exhibits a low noise figure of 1.42 dB, gain of 17.9 dB with the linearity parameter IIP3 of 6.67 dBm satisfying the LNA requirements.
- Optimization techniques were employed to achieve the desired balance and meet the specifications outlined in the design requirements.

Further scope:

- ❖ Having comprehensively explored the schematic design of the low noise amplifier (LNA) and the Gilbert Mixer Cell, the next phase will focus on the Merged Implementation on the LNA and Mixer.
- ❖ Along with the layout design and its impact since it serves as the bridge between theoretical electrical design and the physical realization of the circuit on a printed circuit board (PCB).
- ❖ As technology continues to advance, future work could explore the application of more advanced technology nodes for further performance improvement.
- ❖ Investigating into novel circuit topologies and design methodologies to enhance LNA and Mixer performance.