A thesis on Designing of Low Noise Amplifier (LNA)

Bachelor's Term Project-I (EC47003) report submitted to

Indian Institute of Technology Kharagpur

in partial fulfilment for the award of the degree of

Bachelor of Technology

in

Electronics and Electrical Communication Engineering

by

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(20EC10040)

Under the supervision of

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Indian Institute of Technology Kharagpur

Autumn Semester, 2023-24

November 25, 2023

DECLARATION

I certify that

(a) The work contained in this report has been done by me under the guidance of my supervisor.

(b) The work has not been submitted to any other Institute for any degree or diploma.

(c) I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.

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DEPARTMENT OF ELECTRONICS AND ELECTRICAL COMMUNICATION ENGINEERING

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KHARAGPUR - 721302, INDIA

CERTIFICATE

This is to certify that the project report entitled "**A thesis on Designing of Low Noise Amplifier (LNA)**" submitted by **Kondapalli Rajesh** (Roll No. 20EC10040) to Indian Institute of Technology Kharagpur towards partial fulfilment of requirements for the award of degree of Bachelor of Technology in Electronics and Electrical Communication Engineering is a record of bona fide work carried out by him under my supervision and guidance during Autumn Semester, 2023-24.

Date: November 25, 2023

Place: Kharagpur

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Abstract

Name of the student: **Kondapalli Rajesh** Roll No: **20EC10040**

Degree for which submitted: **Bachelor of Technology**

Department: **Department of Electronics and Electrical Communication Engineering**

Thesis title: **A thesis on Designing of Low Noise Amplifier (LNA)**

Thesis supervisor: **Professor Arijit De**

Month and year of thesis submission: **November 25, 2023**

The "Designing of Low-Noise Amplifier (LNA)" project aims to design, optimize an LNA with improved performance characteristics. A standard 180nm CMOS technology has been used to create a 1.5 GHz low noise amplifier (LNA). The amplifier has a noise figure of just 1.02 dB and a forward gain (S21) of 22.53 dB. The primary goal of this project is to design an LNA that minimizes the noise figure with an affective gain. This project encompasses several critical phases, including theoretical analysis, simulation. The initial phase involves a thorough review of LNA theory from the book [2], existing LNA designs and noise analysis. Simulation tools and software, such as Cadence is employed to design and optimize the LNA circuit. Parameters like noise figure and gain are carefully balanced to meet the specific requirements of the intended application.

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Chapter 1

Introduction

In the ever-evolving landscape of wireless communication systems and RF (Radio Frequency) electronics, the demand for high-performance and efficient devices is continually growing. Low-noise amplifiers, or LNAs, are essential components of radio receivers because they maximize signal amplification while reducing noise introduction and tend to dominate sensitivity. Numerous trade-offs involving noise figure (NF), gain, linearity, power dissipation, and impedance matching are involved in the design of the LNA. Attaining simultaneous noise and input matching (SNIM) at a particular power dissipation level is the primary objective of LNA design. A discussion of the design concepts, benefits, and drawbacks of several LNA design strategies based on noise parameter expressions may be found in [1].

The LNA can be designed for the the minimum Noise Figure of the specified technology at any given power dissipation in the Classical Noise Matching technique. Testing if modern CMOS is suitable for the challenge of low noise amplification at multi gigahertz frequencies is the first step towards accomplishing this aim. The excessive thermal noise displayed by submicron CMOS devices is one potential danger for low noise operation. It has been demonstrated in [3] that CMOS is a feasible media for building a GPS receiver, which needs to receive signals centered around 1.57542 GHz, despite this additional noise.

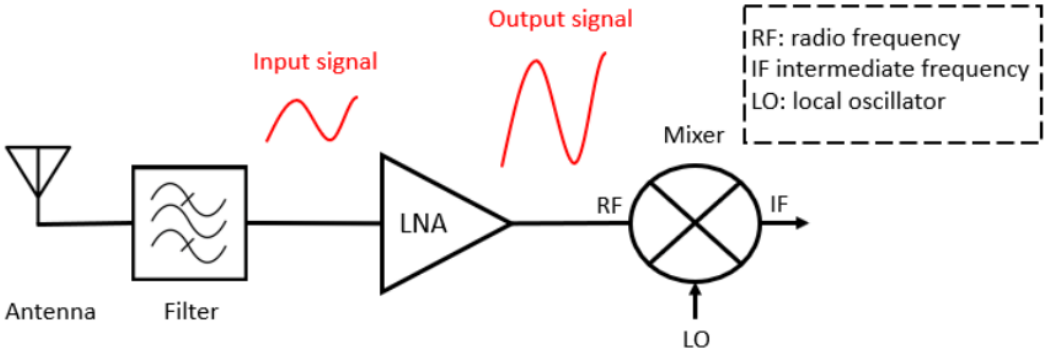

FIGURE 1: LNA in Front end Antenna

A Low-Noise Amplifier (LNA) is an essential part of an antenna system's front end, particularly in radio frequency (RF) and microwave communication systems. This project mainly explores the basic LNA requirements like Noise Figure, Gain, Linearity, Impedance Matching, Power supply of the inductive degenerated input matching topology. Analyzed and compared LNA architectures of Resistive termination, Common gate, Shunt feedback and Inductive degeneration input matching topologies.

Chapter 2

Literature Survey

LNA is designed to provide optimal input impedance Z_{opt} to the specified amplifier in order to achieve the lowest Noise Figure F_{min}. This is usually accomplished by adding a matching circuit between the amplifier's source and input. A good LNA should provide high gain while maintaining a low noise figure to ensure minimal signal degradation.

2.1 LNA Requirements

Noise Figure: It is defined as the relationship between a system's or device's input and output signal-to-noise ratio (SNR). Noise figure is typically expressed in decibels (dB). Lower noise figure is desirable because it indicates that the device adds less noise to the incoming signal. The formula for calculating the noise figure (NF) in dB is:

$$NF(in\ dB) = 10.log_{10}(F) \tag{1}$$

where, F is the noise factor

Gain: The measure of how much the LNA increases the signal's power or voltage. Gain is usually expressed in decibels (dB). A higher gain in an LNA allows it to detect and amplify weaker signals. LNAs have adjustable gain settings, allowing the user to control the level of amplification.

Linearity: Linearity refers to the ability of the LNA to maintain a linear relationship between the input and output signals by prevention

of intermodulation distortion and gain compression. Linearity is often measured using parameters such as the third-order intercept point (IP3) and third-order intermodulation (IM3).

Power Supply: LNAs typically require a stable and well regulated DC voltage supply. Many LNAs require a bias current or voltage to operate properly. Biasing may be accomplished through the power supply.

2.2 Input Matching Topologies

Impedance Matching: Since the LNA functions as a voltage amplifier, we can assume that its ideal input impedance is infinite. In order to achieve minimum NF, it might be necessary to apply a transformation network prior to the LNA, considering the noise perspective.

The resistive input impedance of the LNA is intended to be 50 ohms. This is due to the fact that the bandpass filter (as illustrated in 1) that comes after the antenna is typically made to be used in a variety of transceiver systems, necessitating the use of a standard termination impedance of 50 Ohms. The passband and stopband characteristics of the filter may show significant loss and ripples if the source and load impedances observed by the filter significantly deviate from 50 Ohms.

The LNA output impedance must also be equal to 50 Ohms so as to drive the image-reject filter (as shown in 1) with minimum loss and ripple. Impedance matching helps optimize the performance of the LNA by ensuring that the input and output impedances of the LNA match the impedance of the connected components and transmission lines, such as antennas, cables.

Some of the LNA input matching topologies are: resistive termination, common gate, resistive shunt feedback, inductive degenerated low noise amplifiers. Their configurations are shown below:

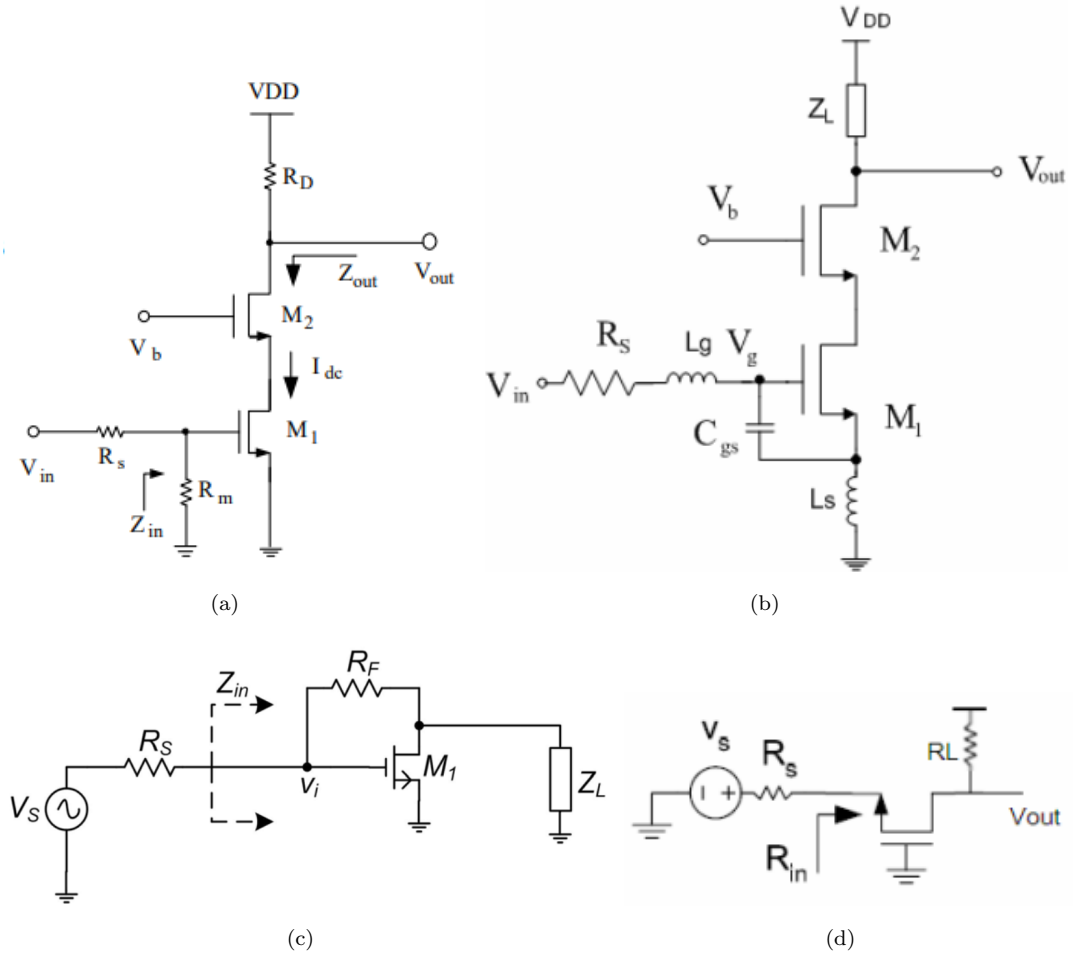

FIGURE 2: (a) Resistive Termination Topology (b) Inductive Degeneration Topology (c) Resistive Shunt Topology (d) Common Gate Topology

The Noise Figure, Gain, Input matching, Linearity, Power of the above four topologies are compared for the 180nm technology in the 1. As we are interested in Low Noise Figure, the Inductive Degenerated Topology has be chosen. All the required parameters in that topology have been calculated for the 180nm technology at 1.5GHz frequency range of operation. Compared the calculated and simulated values to get

low noise figure in the further sections. The Highlights and drawbacks for each topology also has been mentioned.

TABLE 1: Comparison of LNA architectures:

	Resistive Termination	**Common Gate**	**Shunt Feedback**	**Inductive Degeneration**
Noise Figure	>6 dB	3 to 5 dB	2.8 to 5 dB	1 to 2 dB
Gain (S21)	10 to 20 dB	10 to 20 dB	10 to 20 dB	15 to 25 dB
Input Matching	Easy	Easy	Easy	Complex
Linearity (IP3)	-10 to 10 dBm	-5 to 5 dBm	-5 to 5 dBm	-10 to 0 dBm
Power Dissipated	1 to 50 mW	5 mW	>15 mW	>10 mW
Highlight	Effortless Input Matching	Easy Input Matching	Broadband input matching	Good narrowband matching, small NF
Drawback	Large NF	Large NF	Stability	Large area

Chapter 3

Design of LNA

Achieving the lowest noise figure with appropriate power is the main objective in LNA design. At lower frequencies where loop gain requirements can be readily met, dual-feedback techniques are frequently employed. We have achieved a narrow-band 50Ω input impedance by utilizing input tuning in conjunction with inductive source degeneration. The schematic of the Inductive Source degenerated circuit (including off-chip elements) is shown in the 3. In order to investigate CMOS's capacity to provide low noise amplification at 1.5 GHz, we have integrated an LNA into a 180nm CMOS process.

3.1 Circuit Diagram

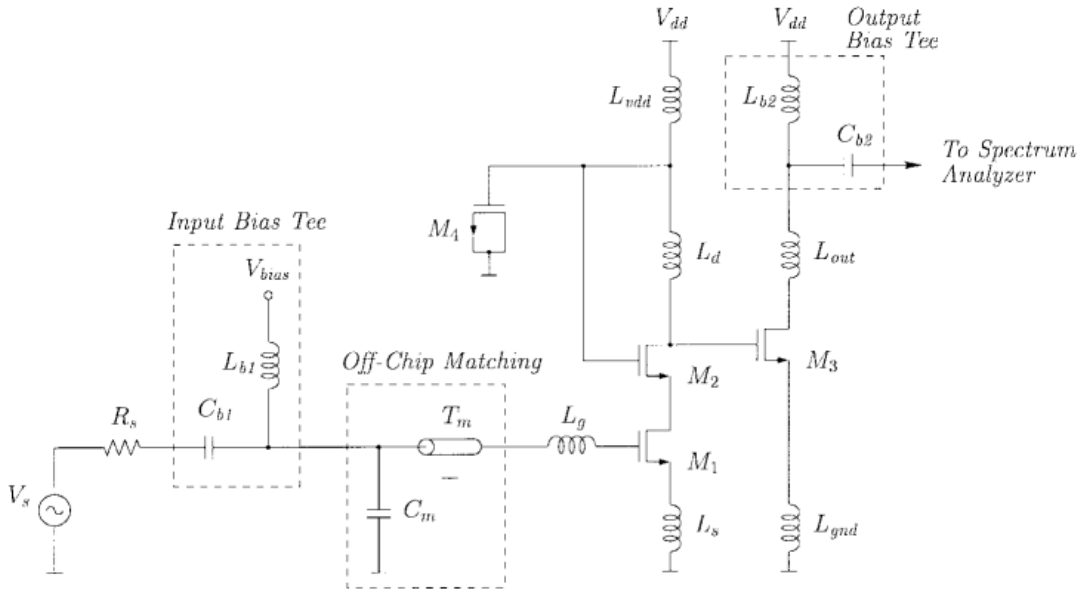

FIGURE 3: Schematic of LNA

The amplifier has a cascaded architecture with two stages. A spiral inductor L_d located on the chip adjusts the drain of M_2. The total capacitance at the drain of M_2, including the C_{gs} of M_3, is in resonance with this inductor. With a gate width that is half that of M_1, M_3 functions as an open drain output driver and adds some gain to the LNA as a whole. The common-gate transistor, or M_2, increases the LNA's reverse isolation to fulfill two crucial functions:
(1) It reduces the leakage of LO generated by the subsequent mixer.
(2) Reduces the feedback from the output to the input to increase the circuit's stability.

It is less likely that major errors will be introduced by ignoring the overlap capacitance C_{gd} when a cascoded first stage is used. Bondwire inductances form four of the shown inductors ($L_s, L_{gnd}, L_{vdd}, L_{out}$). Since it determines the LNA's input impedance, L_s is the only one of these four whose precise value affects how the amplifier functions.

Because L_{gnd}, L_{out} are undesired parasites, proper die bonding reduces their values. M_4, a supply bypass capacitor, helps L_{vdd} with supply filtering. For this purpose, a large inductance value is advantageous, so L_{vdd} is created from a relatively long bondwire.

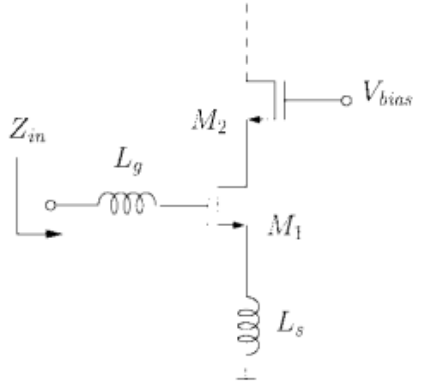

FIGURE 4: Common Source input stage

The input impedance is:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{m1}L_s}{C_{gs}} \tag{2}$$

Where, g_{m1} is the the device transconductance. The input circuit's series resonance occurs when the impedance is proportional to L_s and is entirely real. Considering the ideal case, matching occurs when $Z_{in}(jw_0) = R_s$. Therefore, $R_s = w_T L_s$, where $w_T = \frac{g_{m1}}{C_{gs}}$. The inductance of the gate L_g, after L_s is selected to meet the requirement of a 50 Ohms input impedance, is used to set the resonance frequency.

$$Z_{in}(jw_0) = R_s = \frac{g_{m1}}{C_{gs}}L_s = w_T L_s \tag{3}$$

$$(L_g + L_s)C_{gs} = \frac{1}{w_0^2} \tag{4}$$

In order to artificially lower w_T, a capacitor can be placed in a shunt with the C_{gs} if the value of L_s that was obtained above is too small. The equivalent input network from the source is:

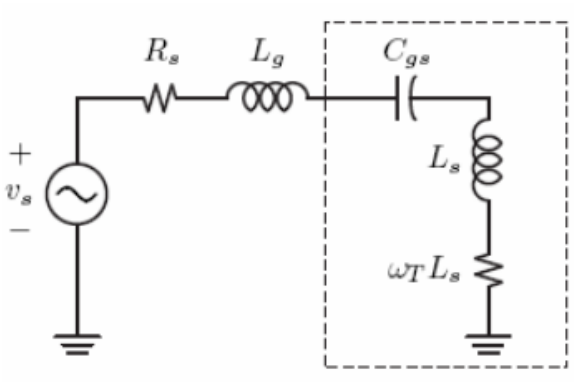

FIGURE 5: (a) Amplifier input (after ignoring Cgd)

The total input impedance must equal R_s at resonance. We experience a Q-boosting effect at resonance. Therefore, since V_{gs} is now growing Q times larger than the input signal, we must check for linearity.

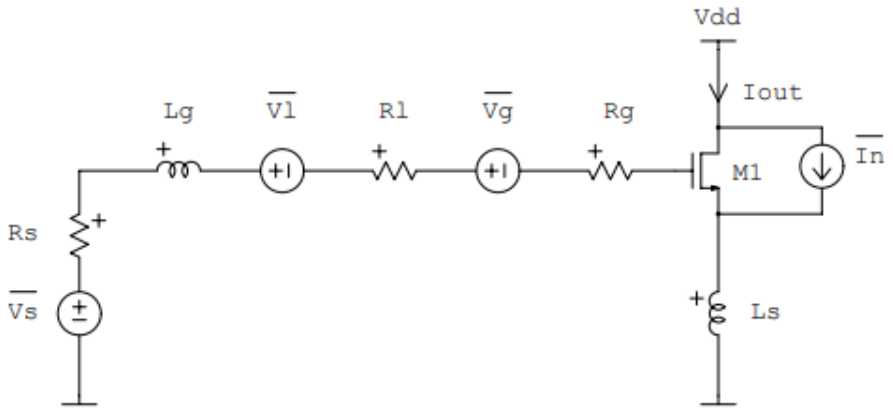

FIGURE 6: Equivalent circuit for noise calculation

The first MOS device's channel current noise is the main internal noise source of the LNA, contributing to the white channel noise. Let, Q_{in} be the effective Q (boosting effect) and G_m be the transconductance of the amplifier input circuit input stage which mean $V_{gs} = QV_s$.

The noise figure can be calculated by dividing the total output noise power by the input source-related noise power at the output.

By ignoring the relationship between drain current noise and gate noise, the noise factor (F) of the LNA is:

$$F = 1 + \frac{R_l + R_g}{R_s} + \gamma g_{d0} R_s (\frac{w_0}{w_T})^2 \tag{5}$$

$$G_m = g_{m1} Q_{in} = \frac{g_{m1}}{w_0 C_{gs}(R_s + w_T L_s)} = \frac{w_T}{2 w_0 R_s} \tag{6}$$

Where, γ is the coefficient of channel thermal noise, g_{d0} is the zero-bias drain conductance. R_g (series gate resistance) and R_l (series inductor resistance) has been disregarded relative to the source resistance R_s in this expression, which is valid at the series resonance w_0.

As long as the resonant frequency is kept constant, the transconductance of this circuit at resonance is independent of gm_1, the device

transconductance. As long as L_g is adjusted to maintain a fixed resonant frequency, adjusting the device's width will not affect the stage's transconductance.

Now that the relationship between drain current noise and gate noise is taken into account, the noise factor (F) becomes:

$$F = 1 + \frac{R_l + R_g}{R_s} + \frac{\gamma\chi}{\alpha Q_L}(\frac{w_0}{w_T}) \tag{7}$$

$$\chi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1 + Q_L^2) \tag{8}$$

$$Q_L = Q_{Cgs} = \frac{1}{w_0 R_s C_{gs}} \tag{9}$$

Where, δ is the coefficient of gate noise, c is the correlation coefficient, The device's noise contribution is altered in proportion to χ by the effects of induced gate noise.

Therefore, the optimal noise figure (lowest NF) will be happened for a particular Q_L.

The current divider indicates the noise component entering the source (for the drain noise analysis):

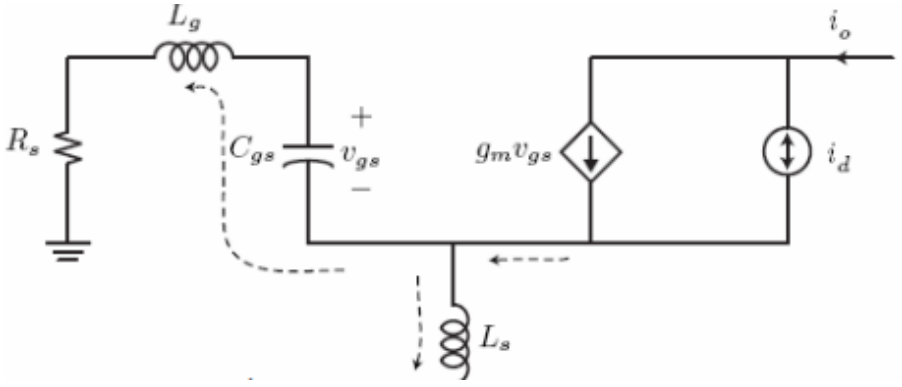

FIGURE 7: Small signal model for Drain noise analysis

$$V_{gs} = (g_m V_{gs} + i_d)(\frac{jwL_s}{jwL_s + \frac{1}{jwC_{gs}} + jwL_g + R_s})(\frac{1}{jwC_{gs}})$$

At Resonance,

$$V_{gs} = (g_m V_{gs} + i_d)(\frac{jwL_s}{R_s})(\frac{1}{jwC_{gs}})$$

$$g_m V_{gs} = \frac{i_d}{2} \tag{10}$$

3.2 Calculation of unknown parameters

F_{min} is not too sensitive to Q_L and changes by less than 0.1dB for Q_L between 3.5 and 5.5. If we try to optimize the noise figure while power dissipation is kept constant, then Q_{Lopt} will be independent from the frequency of operation and around 4.5.

TABLE 2: MOS transistor technology (180nm) features

Parameter	**Value**
C_{ox}	8.57 fF/um^2
$\mu_n C_{ox}$	387 $\mu A/V^2$
L	0.18um
C_{gd0}	7.7e-10F/um
V_{th}	0.51V
γ	3
δ	0.01
$\|c\|$	0.395
α	0.75

Choosing $Q_L = 4.5$. The value of C_gs can be obtained from the 9. Where, $w_0 = 1.5$ GHz, $R_s = 50$ Ohms and technology parameter values are taken from 2.

$$Q_L = \frac{1}{w_0 R_s C_{gs}} \Rightarrow C_{gs} = \frac{1}{Q_L w_0 R_s} \Rightarrow C_{gs} = 0.4716pF$$

$$C_{gs} = \frac{2}{3} C_{ox} W L \Rightarrow W = \frac{3C_{gs}}{2C_{ox}L} \Rightarrow W = 460um$$

From the available power budget, the drain current I_d is assumed to be 10mA.The value of V_{gs} can be calculated from 11, then the device transconductance g_m can be obtained from 10.

$$I_d = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{th})^2 \tag{11}$$

$$\Rightarrow V_{gs} = 0.6522V$$

$$g_m V_{gs} = \frac{i_d}{2} \Rightarrow g_m = \frac{i_d}{2V_{gs}} \Rightarrow g_m = 7.67mS$$

From the 3 and 4, the values of w_T, L_s, L_g are calculated.

$$w_T = \frac{g_m}{C_{gs}} \Rightarrow w_T = 16.256GHz$$

$$L_s = \frac{R_s}{w_T} \Rightarrow L_s = 3.076nH$$

$$(L_g + L_s)C_{gs} = \frac{1}{w_0^2} \Rightarrow L_g = \frac{1}{w_0^2 C_{gs}} - L_s \Rightarrow L_g = 20.797nH$$

The total capacitance at the drain of M_2, including the C_{gs} of M_3, is in resonance with the inductor L_d. Therefore,

$$(C_{d2} + C_{gs3})L_d = \frac{1}{w_0^2}$$

$$\Rightarrow (\frac{1}{2}C_{ox}W_2L + C_{gd0}W_2 + \frac{2}{3}C_{ox}W_3L)L_d = \frac{1}{w_0^2} \Rightarrow L_d = 11.9nH$$

In the input bias tree, the value of L_{b1}, C_{b1} are chosen such that:

$$L_{b1}C_{b1} = \frac{1}{w_0^2} \Rightarrow L_{b1} = 10nH, C_{b1} = 1.1257pF$$

Similarly in the output bias tree, the value of L_{b2}, C_{b2} are chosen such that:

$$L_{b2}C_{b2} = \frac{1}{w_0^2} \Rightarrow L_{b2} = 10nH, C_{b2} = 1.1257pF$$

Using above calculated values, Simulations are done and optimal simulated values are noted. The mentioned LNA requirements are plotted.

3.3 Simulation Results

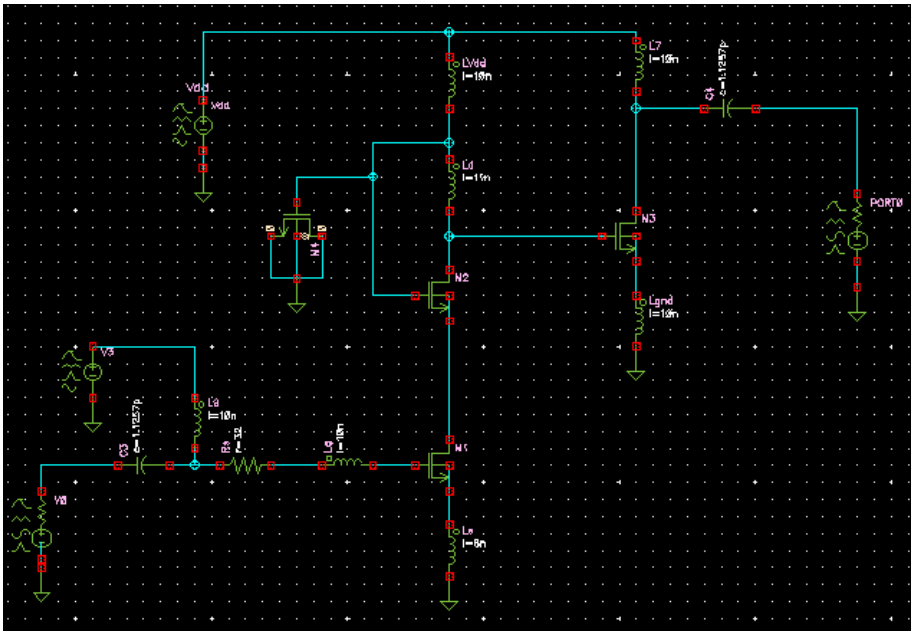

FIGURE 8: Circuit Diagram of Low Noise Amplifier (in Cadence environment)

The Noise Figure is plotted with respect to the frequency and source voltage. The Optimal source voltage, V_{dd} is 1.8V in 0.18μm technology.

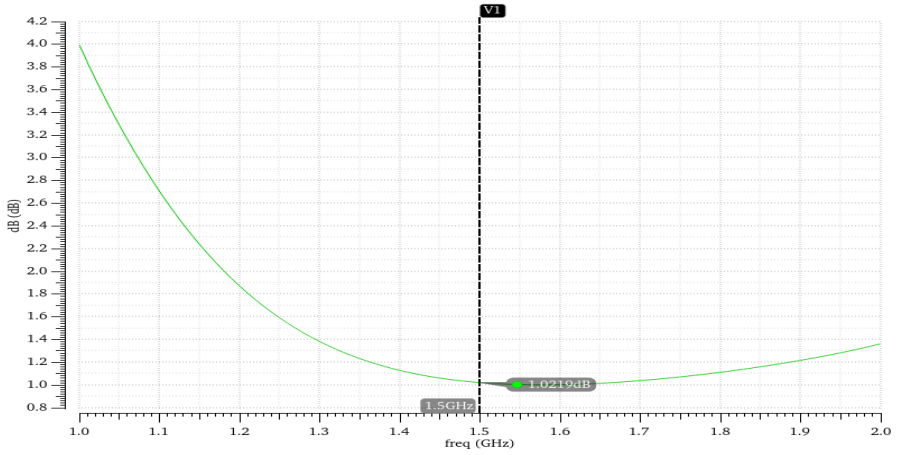

FIGURE 9: Noise Figure Vs Frequency

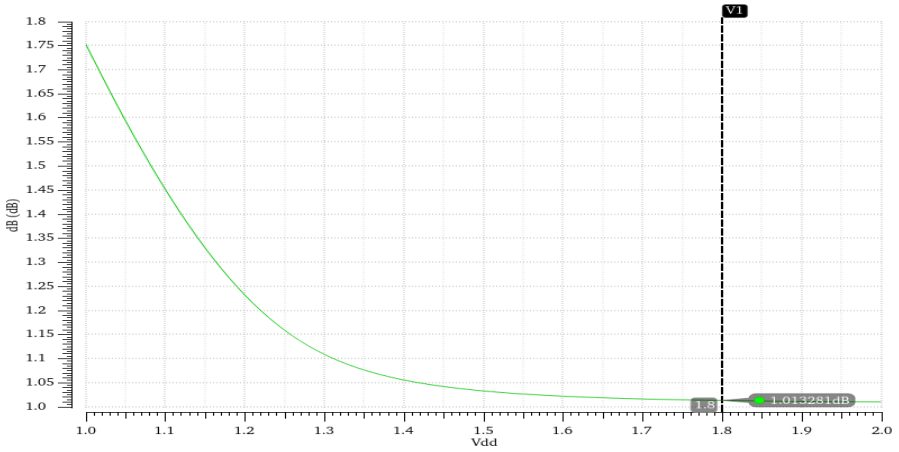

FIGURE 10: Noise Figure vs Source Voltage

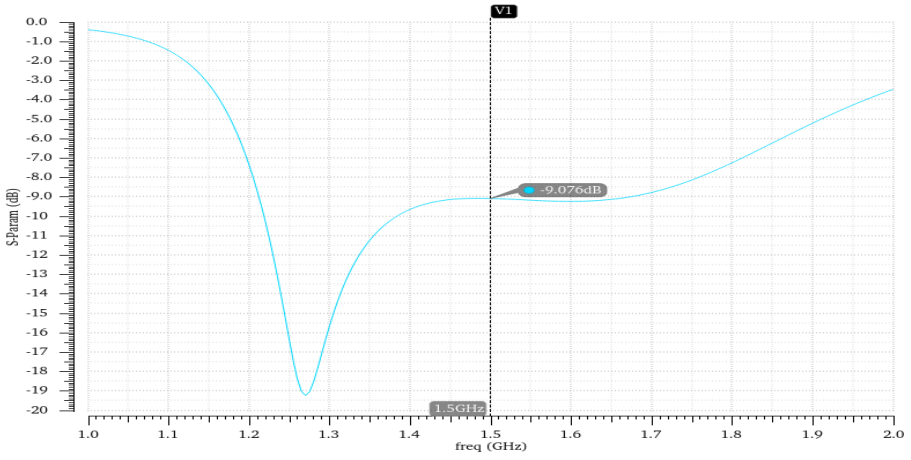

FIGURE 11: S_{11} Plot

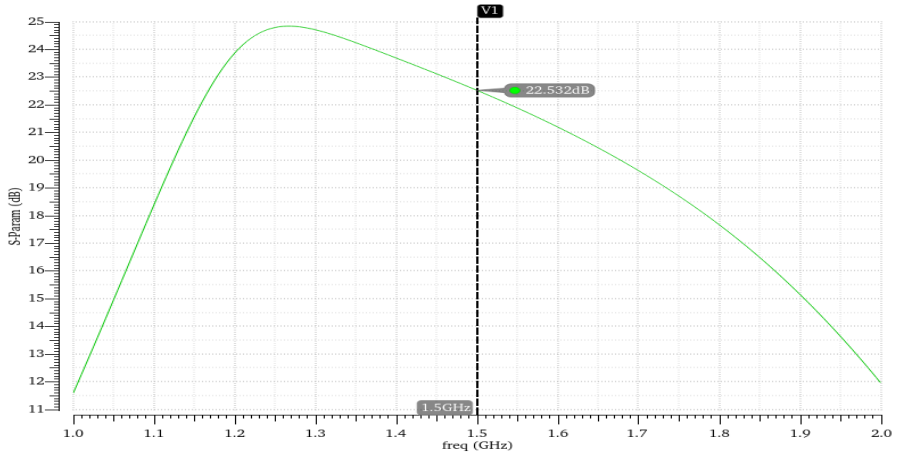

FIGURE 12: S_{21} Plot

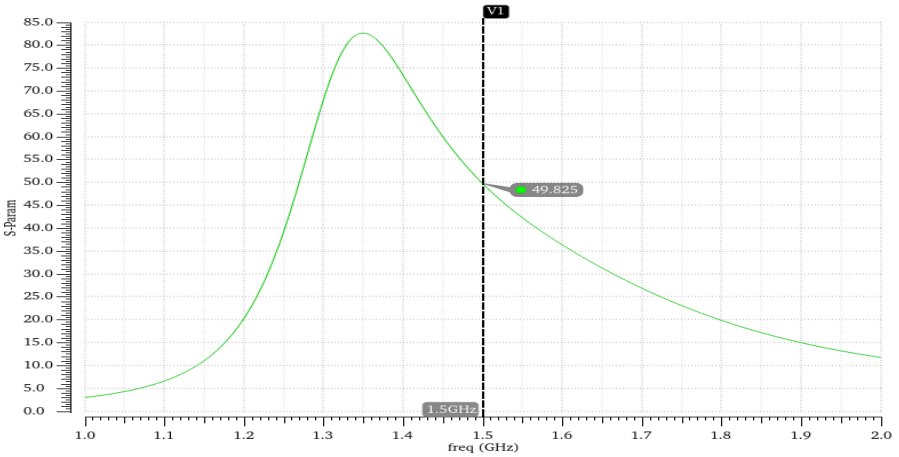

FIGURE 13: Re(Z_{in} Plot)

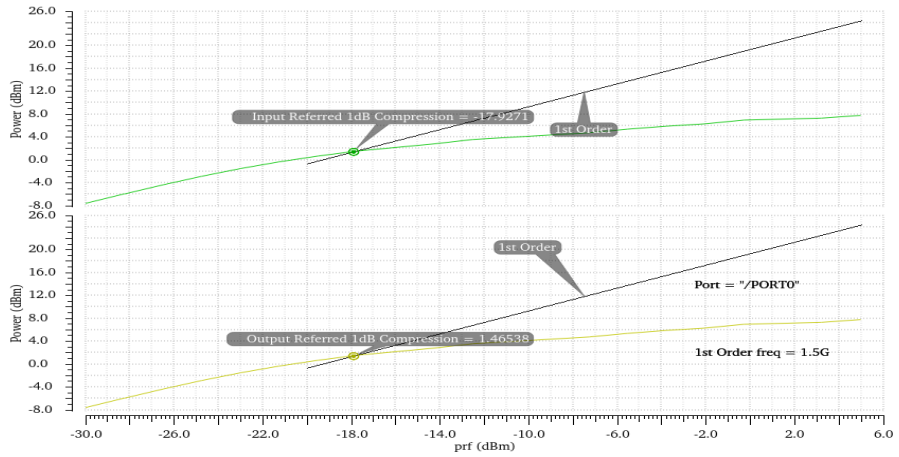

FIGURE 14: Input and Output referred 1dB Compression points

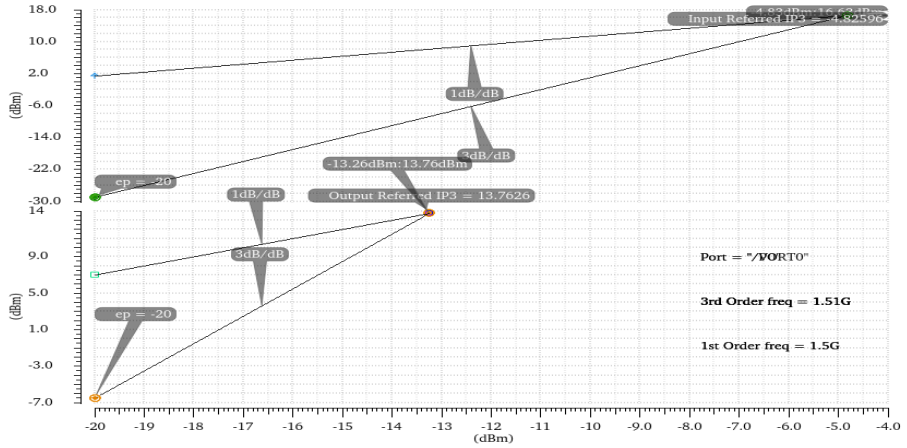

FIGURE 15: Input and Output referred IP3 points

TABLE 3: Calculated and Simulated Parameters

	Calculated Value	**Simulated Value**
M_1	$460\mu m/0.18\mu m$	$460\mu m/0.18\mu m$
M_2	$460\mu m/0.18\mu m$	$460\mu m/0.18\mu m$
M_3	$230\mu m/0.18\mu m$	$230\mu m/0.18\mu m$
L_g	20.797nH	10nH
L_s	3.076nH	8nH
L_d	11.9nH	11nH
I_d	10mA	17.9mA

The input and Output referred 1dB compression point is a measure of the input and output power level respectively at which the gain of a system drops by 1dB from its small-signal value.

The Input and Output Third-Order Intercept Point (IIP3 and OIP3) is a measure of the input and output power level respectively at which the third-order intermodulation distortion products reach the same power level as the desired signal.

TABLE 4: Performance Summary

Metric	**Simulation result**
Frequency	1.5GHz
NF	1.02dB
S21	22.53dB
S11	-9.07dB
IIP3	-4.826dBm
OIP3	13.763dBm
Re(Z_{in})	49.825 Ohms
Current	17.9mA
1dB Compression point (input)	-17.927dBm
1dB Compression point (output)	1.465dBm
Supply	1.8V

Chapter 4

Conclusion

We have successfully demonstrated a 0.18-um CMOS low noise amplifier. Excellent performance characteristics of the designed LNA include a low noise figure of 1.02 dB and a high gain of 22.53 dB. The design process involved careful trade-offs between various parameters, including gain and noise figure. Optimization techniques were employed to achieve the desired balance and meet the specifications outlined in the design requirements. Induced gate noise plays a fundamental role in defining the minimum noise figure, as theoretical analysis of the amplifier architecture has shown. The fact that this source of noise may dominate the amplifier's output noise in many real-world scenarios highlights the urgent need for better MOS noise models. We are confident that CMOS will be a strong contender for the preferred technology in wireless receiver designs in the future, based on this outcome. The digital VLSI industry is driving CMOS technology toward ever-smaller channel lengths, which will continue to enhance the performance of circuits like this one.

Chapter 5

Further Scope

Having comprehensively explored the schematic design of the low noise amplifier (LNA), the next phase will focus on the crucial aspect of layout design and its impact since it serves as the bridge between theoretical electrical design and the physical realization of the circuit on a printed circuit board (PCB). Extending the design of Low Noise Amplifier to non-ideal inductors, checking the basic LNA requirements and working for the bandwidth extension. As technology continues to advance, future work could explore the application of more advanced technology nodes for further performance improvement. Additionally, investigation into novel circuit topologies and design methodologies may provide opportunities to enhance LNA performance.

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