A thesis on Designing of Gilbert mixer

Bachelor's Term Project-II (EC47004) report submitted to

Indian Institute of Technology Kharagpur

in partial fulfilment for the award of the degree of

Bachelor of Technology

in

Electronics and Electrical Communication Engineering

by

Kondapalli Rajesh

(20EC10040)

Under the supervision of

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Indian Institute of Technology Kharagpur

Spring Semester, 2023-24

April 29, 2024

DECLARATION

I certify that

(a) The work contained in this report has been done by me under the guidance of my supervisor.

(b) The work has not been submitted to any other Institute for any degree or diploma.

(c) I have conformed to the norms and guidelines given in the Ethical Code of Conduct of the Institute.

(d) Whenever I have used materials (data, theoretical analysis, figures, and text) from other sources, I have given due credit to them by citing them in the text of the thesis and giving their details in the references. Further, I have taken permission from the copyright owners of the sources, whenever necessary.

Date: April 29, 2024 (Kondapalli Rajesh)

Place: Kharagpur (20EC10040)

DEPARTMENT OF ELECTRONICS AND ELECTRICAL COMMUNICATION ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY KHARAGPUR

KHARAGPUR - 721302, INDIA

CERTIFICATE

This is to certify that the project report entitled "**A thesis on Designing of Gilbert mixer**" submitted by **Kondapalli Rajesh** (Roll No. 20EC10040) to Indian Institute of Technology Kharagpur towards partial fulfilment of requirements for the award of degree of Bachelor of Technology in Electronics and Electrical Communication Engineering is a record of bona fide work carried out by him under my supervision and guidance during Spring Semester, 2023-24.

Date: April 29, 2024

Place: Kharagpur

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Abstract

Name of the student: **Kondapalli Rajesh** Roll No: **20EC10040**

Degree for which submitted: **Bachelor of Technology**

Department: **Department of Electronics and Electrical Communication Engineering**

Thesis title: **A thesis on Designing of Gilbert mixer**

Thesis supervisor: **Professor Arijit De**

Month and year of thesis submission: **April 29, 2024**

The "Design of an Gilbert cell mixer" project aims to design, optimize an mixer to improve the combined performance of the Low Noise Amplifier (LNA) and the Mixer. The design has been put into practice utilizing Cadence's spectre-RF simulator and standard TSMC-180nm CMOS technology has been used to implement mixer. The suggested mixer has RF and LO frequencies of 2.4GHz and 2.3GHz respectively, and an output frequency of 100MHz for the IF. This project encompasses several critical phases, including theoretical analysis, simulation. The initial phase involves review of theory and designing of LNA. The succeeding phases involves designing of mixer with review of theory and simulations for optimization of the circuit. Additionally Noise Figure, Conversion gain, linearity parameters are plotted in the cadence simulator as verification.

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Chapter 1

Introduction

Because of the potential low cost, low power, and system level integration, CMOS RF integrated circuits (RFIC) for wireless communication systems operating in the 2.4 GHz frequency range have attracted significantly more attention. One way to achieve low power and low cost is to minimize the number of off-chip components by integrating all necessary blocks in the receiver's front end as much as possible. Due to its relatively low noise, the heterodyne receiver architecture is the most popular RF architecture for wireless applications.

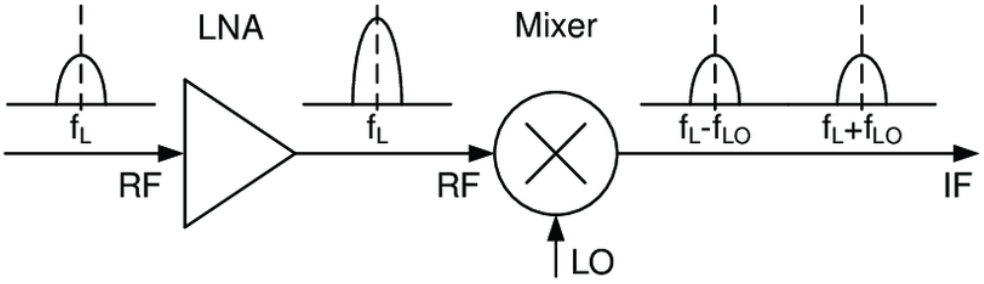

Figure 1: Block diagram of LNA-Mixer Interface

The low noise amplifier (LNA) and mixer are the most difficult components of the front-end receiver as shown in 1. The mixer translates an incoming RF signal to a lower frequency, called the intermediate frequency (IF).This mixing operation can be performed using switching property of MOS transistor. A Double Balanced Mixer, Gilbert Cell is used for implementation because they are less susceptible to noise compared to Single Balanced Mixer.

Chapter 2

Literature Survey

2.1 Mixer theory

In order to convert an incoming signal (after it has been amplified by the LNA) to an intermediate frequency (IF), mixers are used for frequency translation in which a local oscillator (LO) signal is multiplied on it. The block-level representation is shown in 1. The intermediate frequency can be either the difference between the two signal frequencies or the sum of the frequencies of the two input signals.

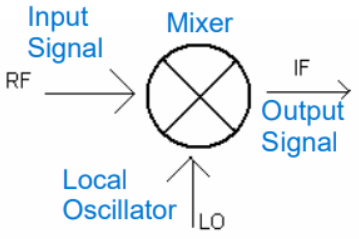

FIGURE 2: Block diagram of Mixer

Consider, the input signals as sinusoidal signals.

$$V_{RF}(t) = A_{RF} * \sin(2\pi f_{RF} t)$$

$$V_{LO}(t) = A_{LO} * \sin(2\pi f_{LO} t)$$

Multiplication of radio frequency signal and local oscillator frequency signal yields:

$$V_{IF}(t) = V_{RF}(t) * V_{LO}(t)$$

$$V_{IF}(t) = A_{RF} * A_{LO} * sin(2\pi f_{RF} t) * sin(2\pi f_{LO} t)$$

$$V_{IF}(t) = \frac{A_{RF} * A_{LO}}{2}(cos(2\pi(f_{RF} - f_{LO})t) - cos(2\pi(f_{RF} + f_{LO})t)) \quad (1)$$

According to the equation 1 mixing occurs and the wanted down converted intermediate frequency is obtained as:

$$V_{IF}(t) = \frac{A_{RF} * A_{LO}}{2}cos(2\pi(f_{RF} - f_{LO})t) = A_{IF} * cos(2\pi f_{IF}t) \quad (2)$$

This desired signal (eq 2) can be achieved by the combination of transistor in either single balanced or double balanced arrangement of mixer.

2.2 Mixer Requirements

Noise Figure: Noise figure (NF) measures how much the signal to noise ratio (SNR) of a signal degrades because of the added noise as it passes through the mixer. The NF of the mixer is defined as the total SNR at the RF frequency divided by the SNR at the IF frequency. Noise figure is typically expressed in decibels (dB).

Lower noise figure is desirable because it indicates that the device adds less noise to the incoming signal.

$$NF(in\ dB) = 10.log_{10}\frac{SNR_{in}}{SNR_{out}} \quad (3)$$

Noise Figure of Cascaded Systems: The total noise is the combined noise contribution of each stage divided by the total available gain between the stages. It is dependent on the gain of subsequent stages because noise becomes less important once the signal has been amplified. Therefore, the system noise figure (NF) is dominated by the noise performance of the first couple of stages of the system.

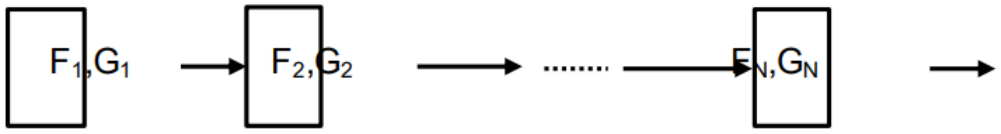

FIGURE 3: Cascaded Systems for Noise Figure Calculation

Consider F_i, G_i as Noise factor and gain of the stage i in the cascaded system shown in 3. Noise Factor of the system is:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + .. \frac{F_N - 1}{\pi_{n=1}^{N-1} G_n} \tag{4}$$

$$NoiseFigure(NF) = 10log(F)$$

Noise figure, for a mixer, considers only the noise associated with the IF frequency, according to the IEEE's NF definition for mixers, it assumes that there are no noise contribution at the image frequency $(2f_{LO} - f_{RF})$ due to mixing. There will be an Image Reject Filter preceding the mixer to remove the noise at the image frequency.

Conversion Gain: The voltage conversion gain of a mixer is defined as the rms voltage of the signal at the IF frequency divided by the rms voltage of the signal at the RF frequency. Gain is usually expressed in decibels (dB).

Linearity: Linearity refers to the ability of the Mixer to maintain a linear relationship between the input and output signals by prevention of intermodulation distortion and gain compression. Linearity is often measured using parameters such as 1dB compression point, third-order intercept point (IP3) and third-order Intermodulation (IM3). Usually expressed in the units of dBm.

1dB compression point: The measure of the power level at which the gain of a system drops by 1dB from its small-signal value.

Third-order intercept point (IP3): The measure of the power level at which the third-order intermodulation distortion products reach the same power level as the desired signal.

1-dB compression and the third order intercept point are related to each other. By knowing one, the other can be approximated. For a single tone input, the 1dB compression point is about 9.66dB below the intercept point.

2.3 Mixer topologies

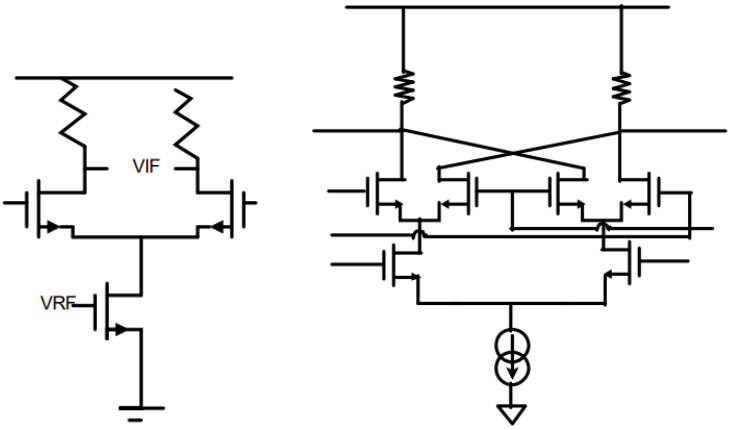

FIGURE 4: (a) Single Balanced Mixer (b) Double Balanced Mixer

Single Balanced Mixer: A mixer with a single-ended RF signal is called a single-balanced mixer which is shown in 4(a). This configuration is rarely used because it is more susceptible to noise in the LO signal. Its main drawback is the LO-IF feedthrough. That is, the LO signal could leak into the IF if the IF is not much lower than the LO

frequency. The low pass filter following the mixer may not properly suppress the LO signal without affecting the IF signal.

Double Balanced Mixer: Double Balanced Mixers are essentially two single-balanced circuits with the RF transistors connected in parallel and the switching pair in anti-parallel (shown in 4(b)). They are used to prevent the LO products from reaching the output. Therefore, the LO terms sum to zero and the RF signal doubled in the output. This configuration provides a high degree of LO-IF isolation easing filtering requirements at the output ([1]). Double Balanced mixers are less susceptible to noise than the single-balanced mixers because of the differential RF signal.

Chapter 3

Design of Mixer and LNA

3.1 Gilbert Cell Mixer

The Gilbert Cell has two pairs of transistors connected in parallel; this provides a double balanced mixer which attenuates the feed-through RF and LO components produced by the mixer. When two signals are mixed, the output will be the wanted frequency (the mixing) and the feed-through. Some of the feed-through is cancelled out due to a 180 degrees phase shift. The two transistors with RF terminals act as amplifier increasing the gain of the signal before mixing.

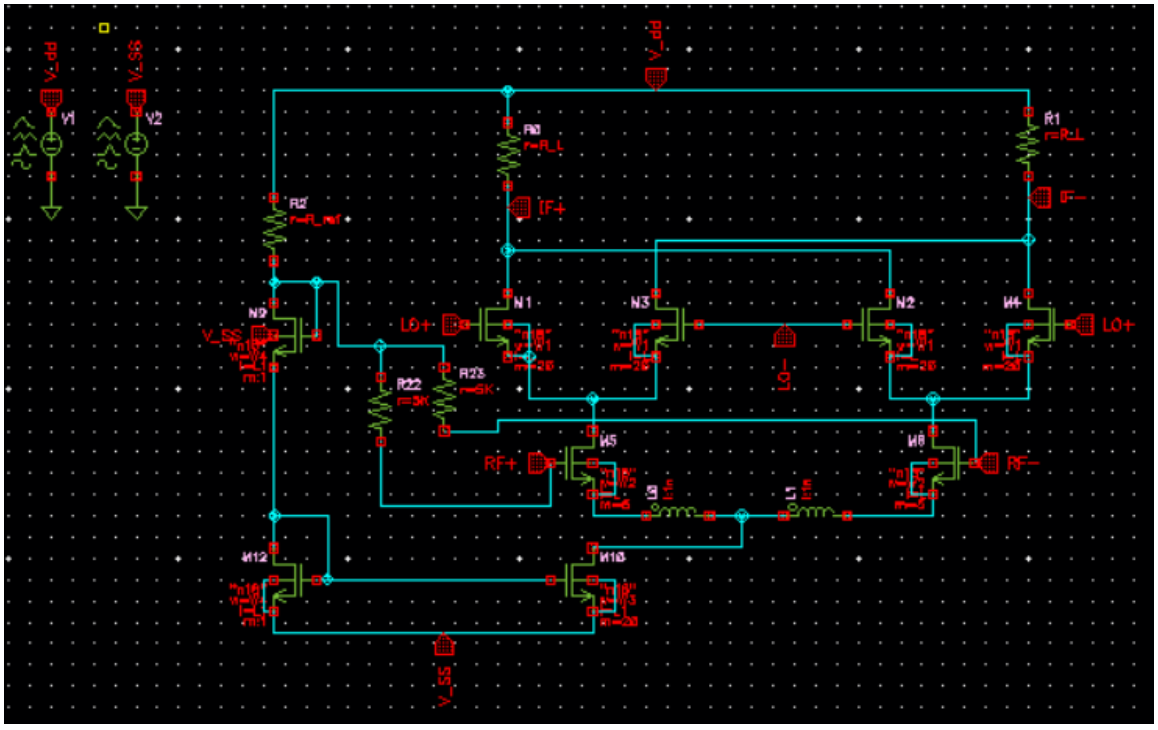

FIGURE 5: Schematic of Gilbert Mixer

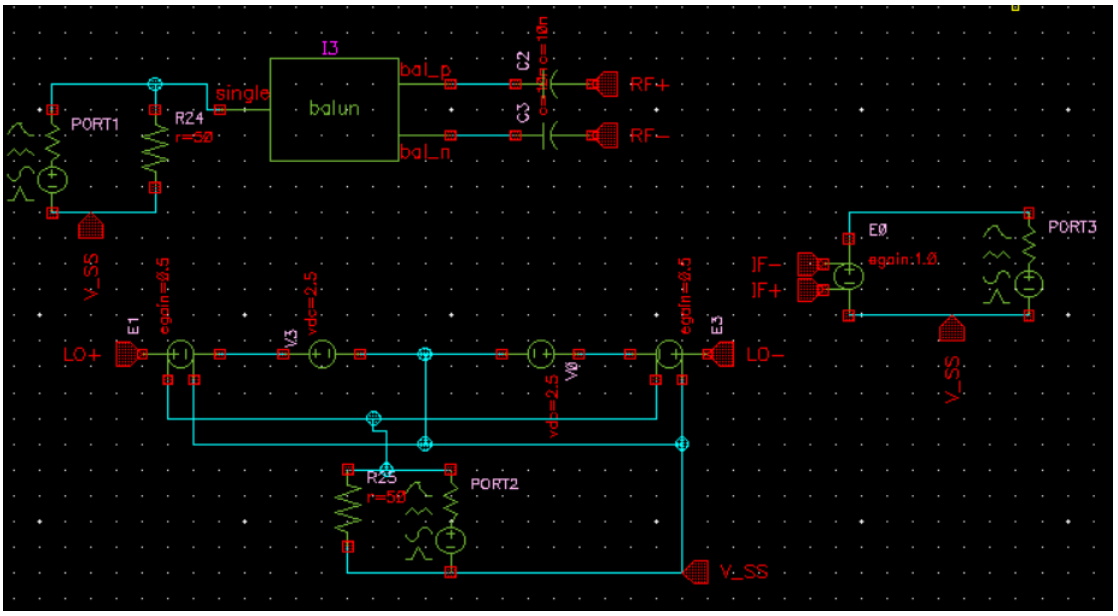

FIGURE 6: Test bench of Gilbert Mixer

The output is taken at the difference between IF- and If+ (shown in the 5 and 6). No input and output impedance matching are required for the mixer since the input comes from the image reject filter which is also on the same chip. A filter with high input impedance will be added at the output of the mixer to filter out the unwanted high frequency produced.

Mixer Operation: The RF signal is applied to the transistors M5 and M6 which perform a voltage to current conversion. Performance can be improved by adding degeneration resistors or inductors, on the source terminals of M5 and M6. Resistors are used when the size of the circuit needs to be minimized. Inductor degeneration is usually preferred because it has no thermal noise to degrade the noise figure. MOSFets M1 to M4 form a multiplication function, multiplying the linear RF signal current from M5 and M6 with the LO signal applied

across M1 to M4 which provide the switching function. M5 and M6 provide +/- RF current and M1 and M4 switch between them to provide the RF signal or the inverted RF signal to the left hand load. M3 and M4 switch between them for the right hand load. The two load resistors form a current to voltage transformation giving differential output IF signals.

3.2 Calculation of unknown parameters of Mixer

The parameters the model used in cadence, tsmc 180nm technology.

TABLE 1: MOS transistor technology (180nm) features

Parameter	**Value**
C_{ox}	8.57 fF/um^2
$\mu_n C_{ox}$	387 $\mu A/V^2$
L	0.18um
C_{gd0}	7.7e-10F/um
V_{th}	0.51V

A current sink of $I_{ss} = 6mA$ was chosen to drive the mixer. Therefore 3mA of current is split between the differential pair. To prevent compression at the IF, a voltage of 2.5V was decided on at the IF. From this decision, the load resistance can be calculated. $R_L = \frac{V_{DD}-V_D}{I} = 267Ohms$

RF stage: The gain is proportional to the transconductance of the RF pairs. By knowing g_m, the W can be calculated. Assuming the gain of 10dB.

$$g_m = \frac{\pi(gain)}{2R_L} = 12.51mS$$

$$W_{5,6} = \frac{g_m^2 L}{K I_{DS}} = 13.7\mu m$$

LO stage: For proper switching, Vgs needed to be just slightly larger than Vt and W to be large. Assuming Vt is 0.7V, Vgs was chosen to be 0.8V.

$$W_{1,2,3,4} = \frac{L I_{ds}}{K(V_{gs} - V_T)^2} = 316\mu m$$

A small current of $100\mu A$ was chosen for the reference current.

$$W_{10} = \frac{L I_{ss}}{K(V_{gs} - V_T)^2} = 316\mu m$$

From concept of current mirror, W of reference mosfet is calculated.

$$W_{12} = \frac{W_{10} I_{ref}}{I_{ss}} = 6\mu m$$

$$R_{ref} = \frac{3.3 - 0.810}{100\mu A} = 25KOhms$$

These parameters were used to setup the initial design of the mixer and modifications were later made to optimize the circuit.

3.3 Inductive Degenerated Low Noise Amplifier

The Noise Figure, Gain, Input matching, Linearity, Power of the four topologies (Resistive Termination Topology, Inductive Degeneration Topology, Resistive Shunt Topology, Common Gate Topology) are compared for the 180nm technology in the [2]. As we are interested in Low Noise Figure, the Inductive Degenerated Topology has be chosen.

The schematic of the Inductive Source degenerated circuit (including

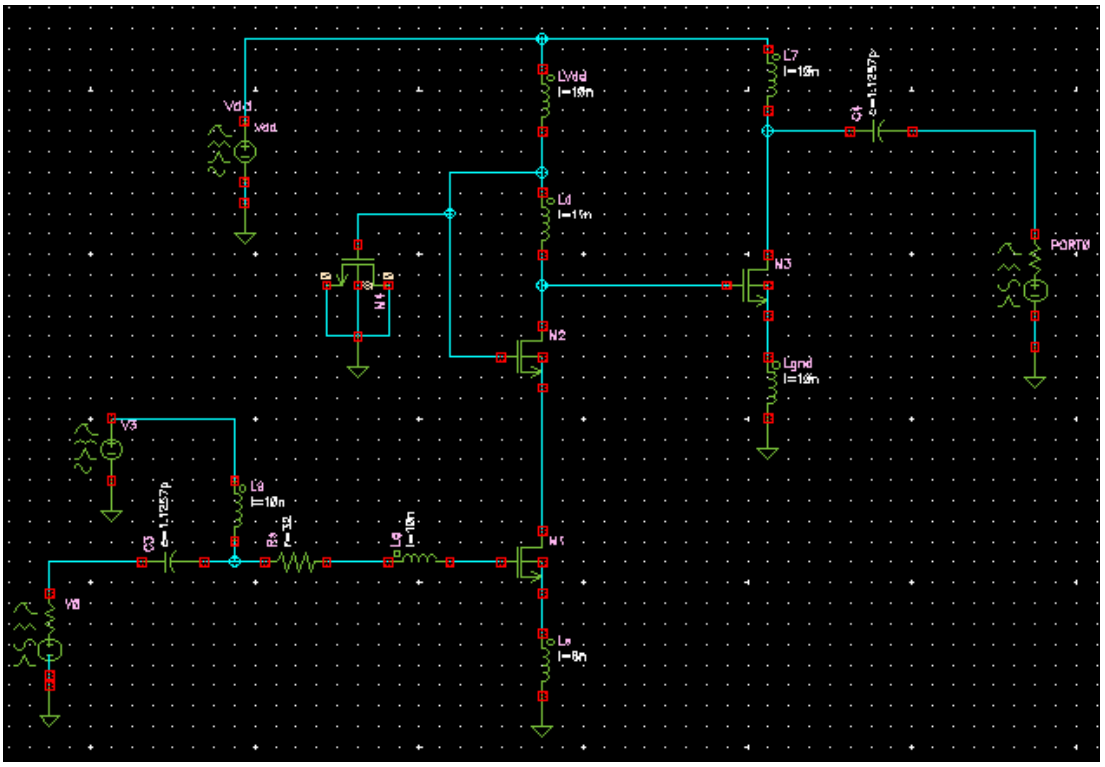

FIGURE 7: Schematic of Low Noise AMplifier

off-chip elements) is shown in the 7. In order to investigate CMOS's capacity to provide low noise amplification at 2.4 GHz, we have integrated an LNA into a 180nm CMOS process.

The amplifier has a cascaded architecture with two stages. A spiral inductor L_d located on the chip adjusts the drain of M2. The total capacitance at the drain of M2, including the C_{gs} of M3, is in resonance with this inductor. With a gate width that is half that of M1, M3 functions as an open drain output driver and adds some gain to the LNA as a whole. The values and parameters calculations are done from the refernece of [4].

3.4 Calculation of unknown parameters of LNA

The input impedance is:

$$Z_{in} = s(L_g + L_s) + \frac{1}{sC_{gs}} + \frac{g_{m1}L_s}{C_{gs}}$$

Where, g_{m1} is the the device transconductance. Considering the ideal case, matching occurs when $Z_{in}(jw_0) = R_s$. Therefore, $R_s = w_T L_s$, where $w_T = \frac{g_{m1}}{C_{gs}}$. The inductance of the gate L_g, after L_s is selected to meet the requirement of a 50 Ohms input impedance, is used to set the resonance frequency.

$$Z_{in}(jw_0) = R_s = \frac{g_{m1}}{C_{gs}}L_s = w_T L_s, (L_g + L_s)C_{gs} = \frac{1}{w_0^2}$$

The total input impedance must equal R_s at resonance. We experience a Q-boosting effect at resonance. Let, Q_{in} be the effective Q (boosting effect) and G_m be the transconductance of the amplifier input circuit input stage which mean $V_{gs} = QV_s$.

$$G_m = g_{m1}Q_{in} = \frac{g_{m1}}{w_0 C_{gs}(R_s + w_T L_s)} = \frac{w_T}{2w_0 R_s}$$

$$Q_L = Q_{Cgs} = \frac{1}{w_0 R_s C_{gs}}$$

Therefore, the optimal noise figure (lowest NF) will be happened for a particular Q_L. F_{min} is not too sensitive to Q_L and changes by less than 0.1dB for Q_L between 3.5 and 5.5. Choosing $Q_L = 4.5$. From the available power budget, the drain current I_d is assumed to be 10mA.

$$Q_L = \frac{1}{w_0 R_s C_{gs}} \Rightarrow C_{gs} = \frac{1}{Q_L w_0 R_s} \Rightarrow C_{gs} = 0.2947pF$$

$$C_{gs} = \frac{2}{3}C_{ox}WL \Rightarrow W = \frac{3C_{gs}}{2C_{ox}L} \Rightarrow W = 287um$$

$$I_d = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \Rightarrow V_{gs} = 0.6902V$$

$$g_m V_{gs} = \frac{i_d}{2} \Rightarrow g_m = \frac{i_d}{2V_{gs}} \Rightarrow g_m = 7.245mS$$

$$w_T = \frac{g_m}{C_{gs}} \Rightarrow w_T = 24.583GHz$$

$$L_s = \frac{R_s}{w_T} \Rightarrow L_s = 2.034nH$$

$$(L_g + L_s)C_{gs} = \frac{1}{w_0^2} \Rightarrow L_g = \frac{1}{w_0^2 C_{gs}} - L_s \Rightarrow L_g = 12.888nH$$

The total capacitance at the drain of M_2, including the C_{gs} of M_3, is in resonance with the inductor L_d. Therefore,

$$(C_{d2} + C_{gs3})L_d = \frac{1}{w_0^2}$$

$$\Rightarrow (\frac{1}{2}C_{ox}W_2L + C_{gd0}W_2 + \frac{2}{3}C_{ox}W_3L)L_d = \frac{1}{w_0^2} \Rightarrow L_d = 7.461nH$$

Using above calculated values, Simulations are done and optimal simulated values are noted.

Chapter 4

Simulation Results

4.1 Simulation results of Mixer

TABLE 2: Calculated and Simulated Parameters of Mixer

	Calculated Value	**Simulated Value**
$M_{1,4}$	$320\mu m/0.18\mu m$	$320\mu m/0.18\mu m$
$M_{2,3}$	$320\mu m/0.18\mu m$	$320\mu m/0.18\mu m$
$M_{5,6}$	$13.7\mu m/0.18\mu m$	$125\mu m/0.18\mu m$
M_{10}	$320\mu m/0.18\mu m$	$200\mu m/0.54\mu m$
$M_{9,12}$	$5.3\mu m/0.18\mu m$	$5\mu m/0.54\mu m$
R_L	267 Ohms	300 Ohms
R_{ref}	25K Ohms	15K Ohms
$R_{22,23}$	3K Ohms	5K Ohms

Mosfet naming from 5. Noise Figure, Conversion gain, S_{21}, 1dB compression point, IIP3, Power dissipation plots are shown:

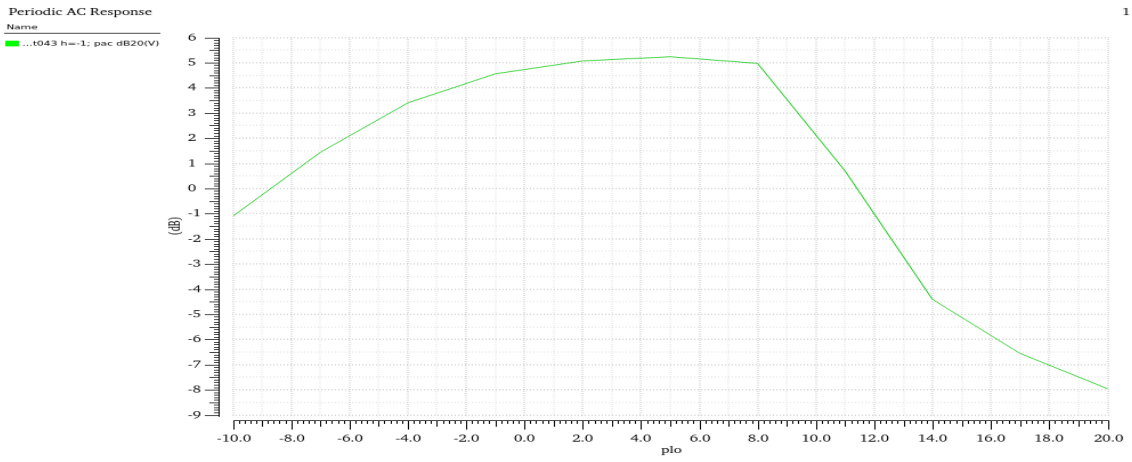

FIGURE 8: Conversion Gain Vs LO signal power

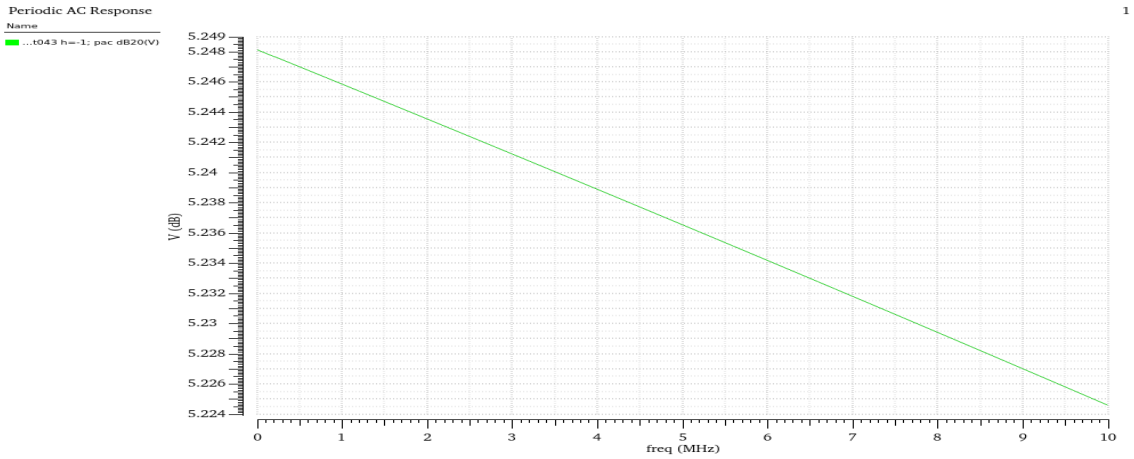

FIGURE 9: Conversion Gain Vs RF frequency

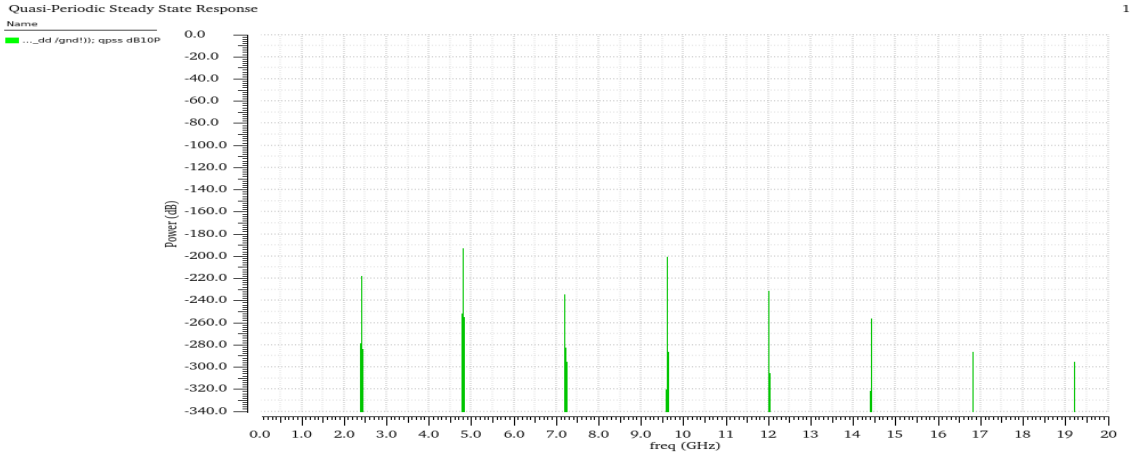

FIGURE 10: Power dissipation

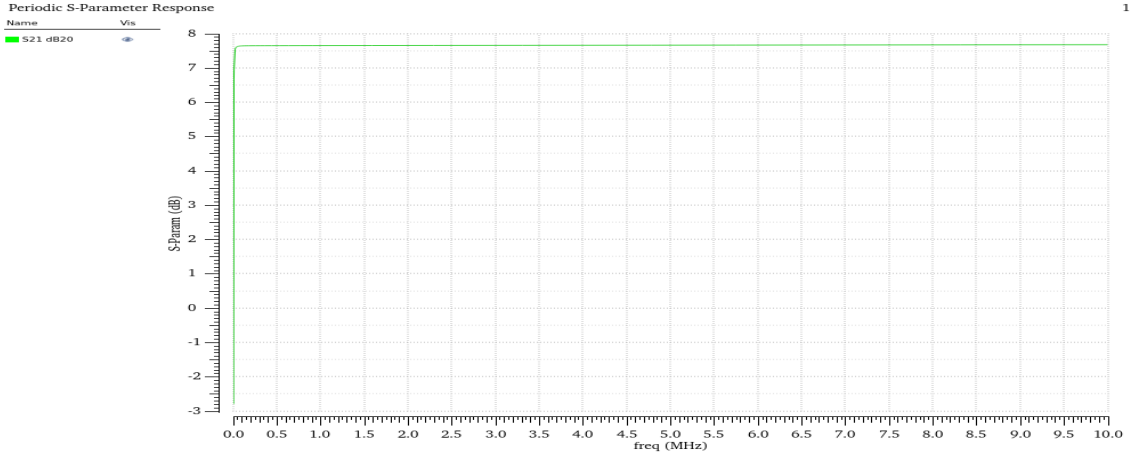

FIGURE 11: S_{21} Plot

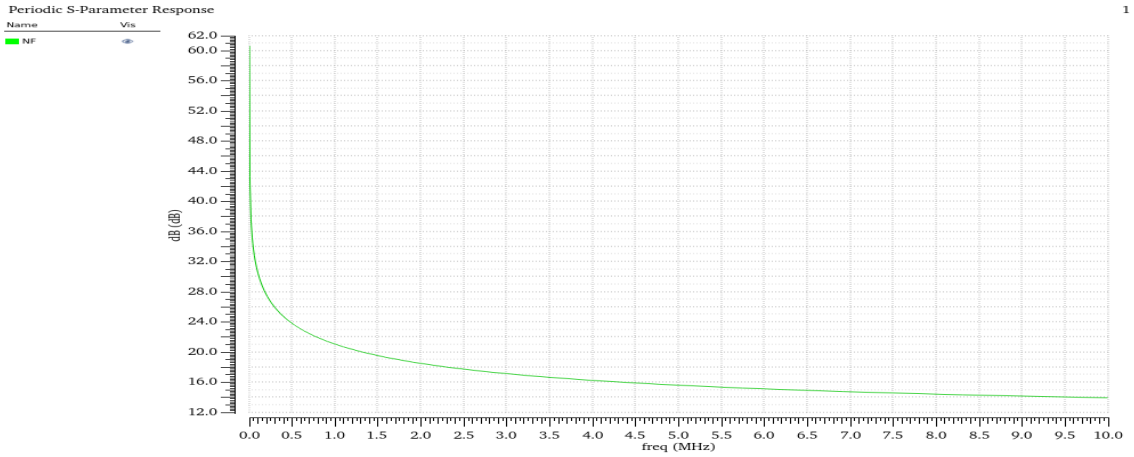

FIGURE 12: Noise Figure Vs Frequency

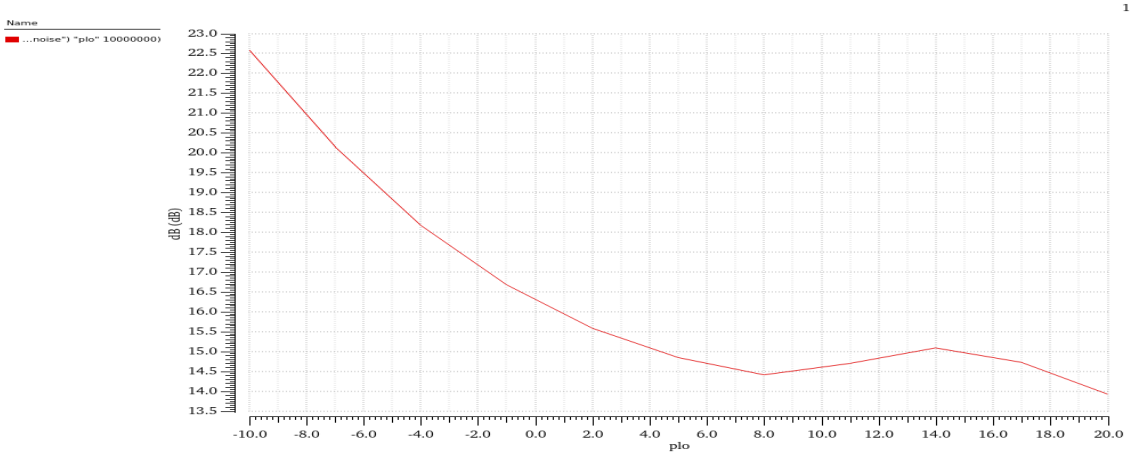

FIGURE 13: Noise Figure Vs LO Signal power

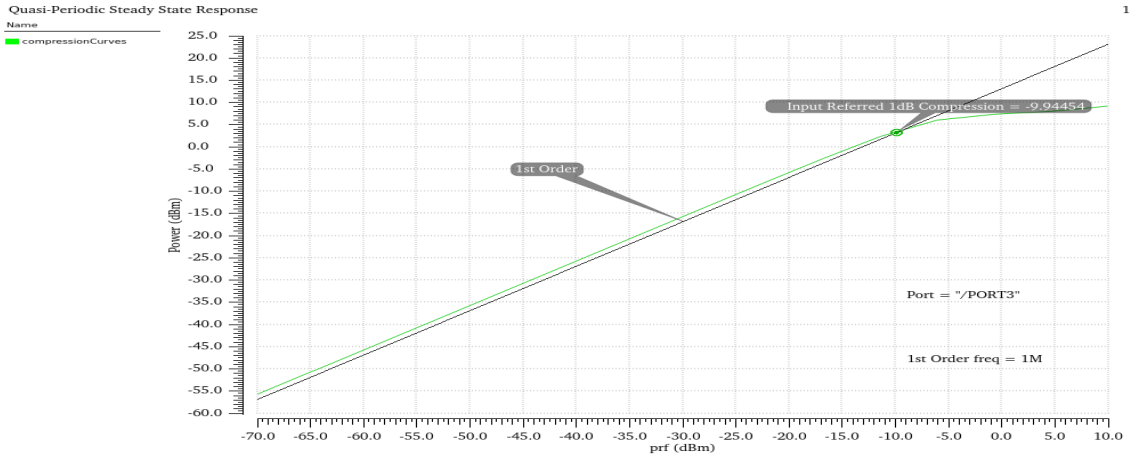

FIGURE 14: Input referred 1dB Compression points

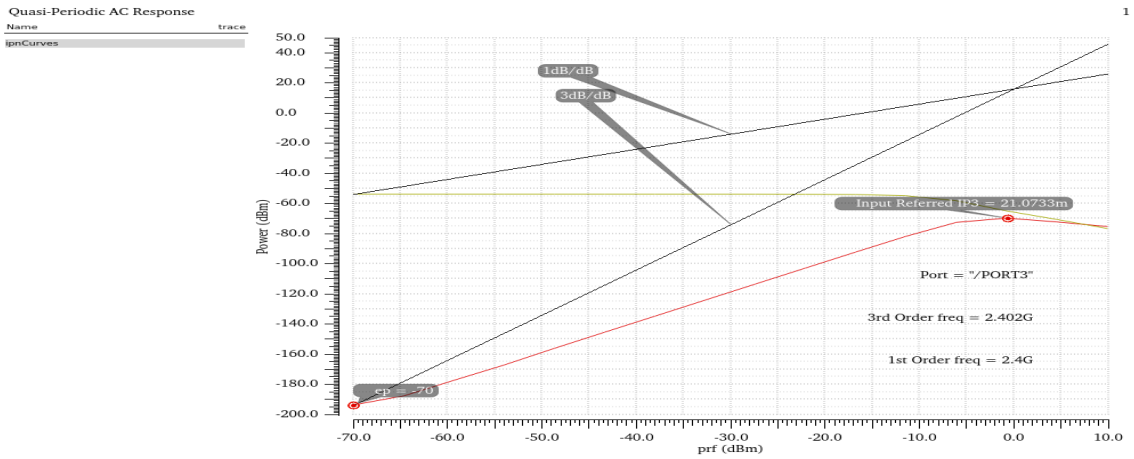

FIGURE 15: Input referred IP3 points

TABLE 3: Performance Summary of Mixer (Gilbert Cell)

Metric	[3]	[5]	[1]	**This work**
RF BW (GHz)	2.4 - 10.7	1 - 10	@2.4	1 - 7
IF BW (GHz)	@0.05	0.1 - 1	@0.15	0.01 - 0.5
CG (dB)	1.8 - 4.8	3 - 8	13.8	7 - 8
$P_{LO}(dBm)$	-5	0	NA	5
NF (dB)	NA	11.3 - 15	15.5	13 - 15
IIP3 (dBm)	4 - 6.9	-7 - -4	-2	0.021
CMOS Proces	$0.18\mu m$	$0.13\mu m$	$0.18\mu m$	$0.18\mu m$

4.2 Simulation results of LNA

TABLE 4: Calculated and Simulated Parameters of LNA

	Calculated Value	**Simulated Value**
$M_{1,2}$	$287\mu m/0.18\mu m$	$280\mu m/0.18\mu m$
M_3	$143\mu m/0.18\mu m$	$140\mu m/0.18\mu m$
L_g	12.888nH	4nH
L_s	2.034nH	4nH
L_d	7.461nH	7nH

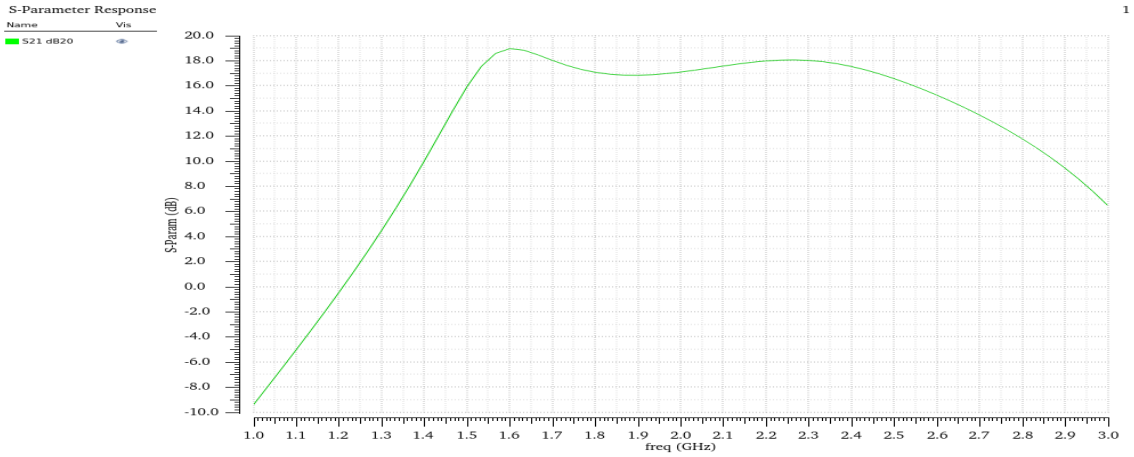

FIGURE 16: S_{21} Plot

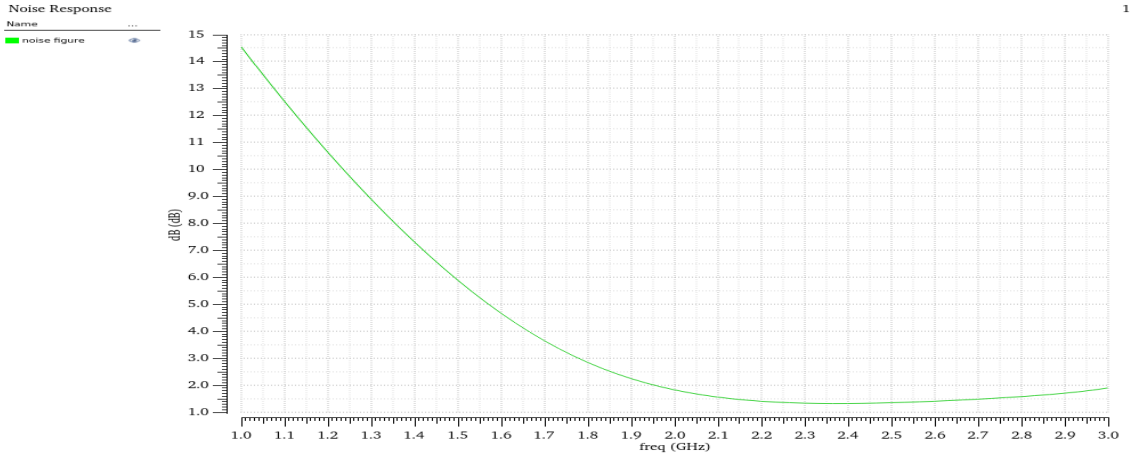

FIGURE 17: Noise Figure Vs Frequency

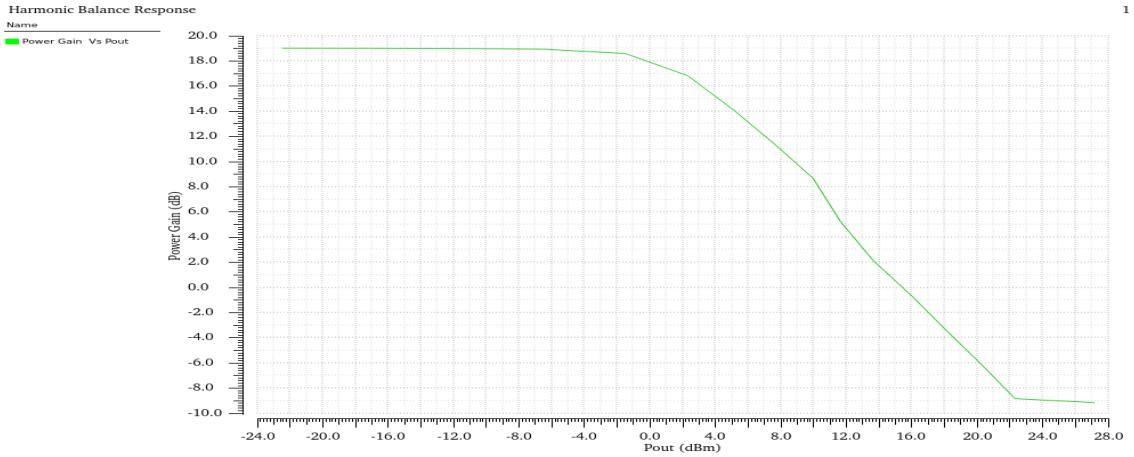

FIGURE 18: Power Gain Vs Output Power

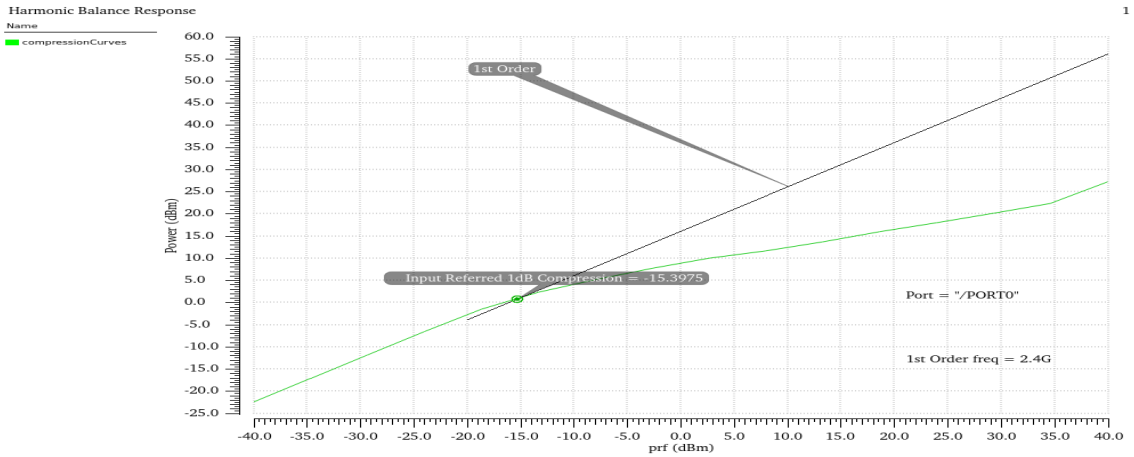

FIGURE 19: Input referred 1dB Compression point

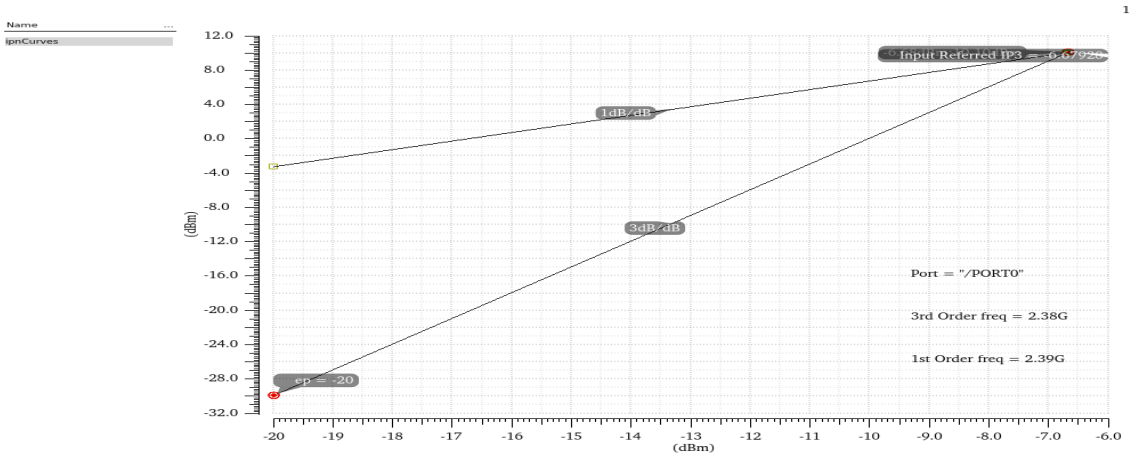

FIGURE 20: Input referred IP3 point

TABLE 5: Performance Summary of LNA

Metric	**Simulation result**
Frequency	2.4GHz
NF (dB)	1.42
S21 (dB)	17.9
1dB Compression point (dBm)	-15.397
IIP3 (dBm)	6.679

Chapter 5

Conclusion

A CMOS Gilbert cell Mixer has been demonstrated in standard 0.18 CMOS technology and simulated using spectre-RF simulator on Cadence. The mixer is operated at 1.8V power supply. By employing a common-gate RF stage with the cross-coupled complementary pair, a conversion gain of 7dB are measured over the RF band from 1 to 7 GHz. The proposed mixer also exhibits a measured IF bandwidth from 10 MHz to 500 MHz with a conversion gain variation less than 2 dB. The measured IP 1 dB, IIP3 and noise figure are better than -9 dBm, 0 dBm, and 15 dB throughout the entire RF band. All the requirements are fulfilled for the circuit as expected and they improved in performance. The measured parameters Mixer are appropriate for developing a RF Receiver Front End. The comparison between the simulated outputs to the reference outputs is shown in 3. The digital VLSI industry is driving CMOS technology toward ever-smaller channel lengths, which will continue to enhance the performance of circuits like this one.

Chapter 6

Further Scope

Having comprehensively explored the schematic design of the low noise amplifier (LNA) and the Gilbert Mixer Cell, the next phase will focus on the Merged Implementation on the LNA and Mixer along with the layout design and its impact since it serves as the bridge between theoretical electrical design and the physical realization of the circuit on a printed circuit board (PCB). As technology continues to advance, future work could explore the application of more advanced technology nodes for further performance improvement. Additionally, investigation into novel circuit topologies and design methodologies may provide opportunities to enhance LNA and Mixer performance.

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