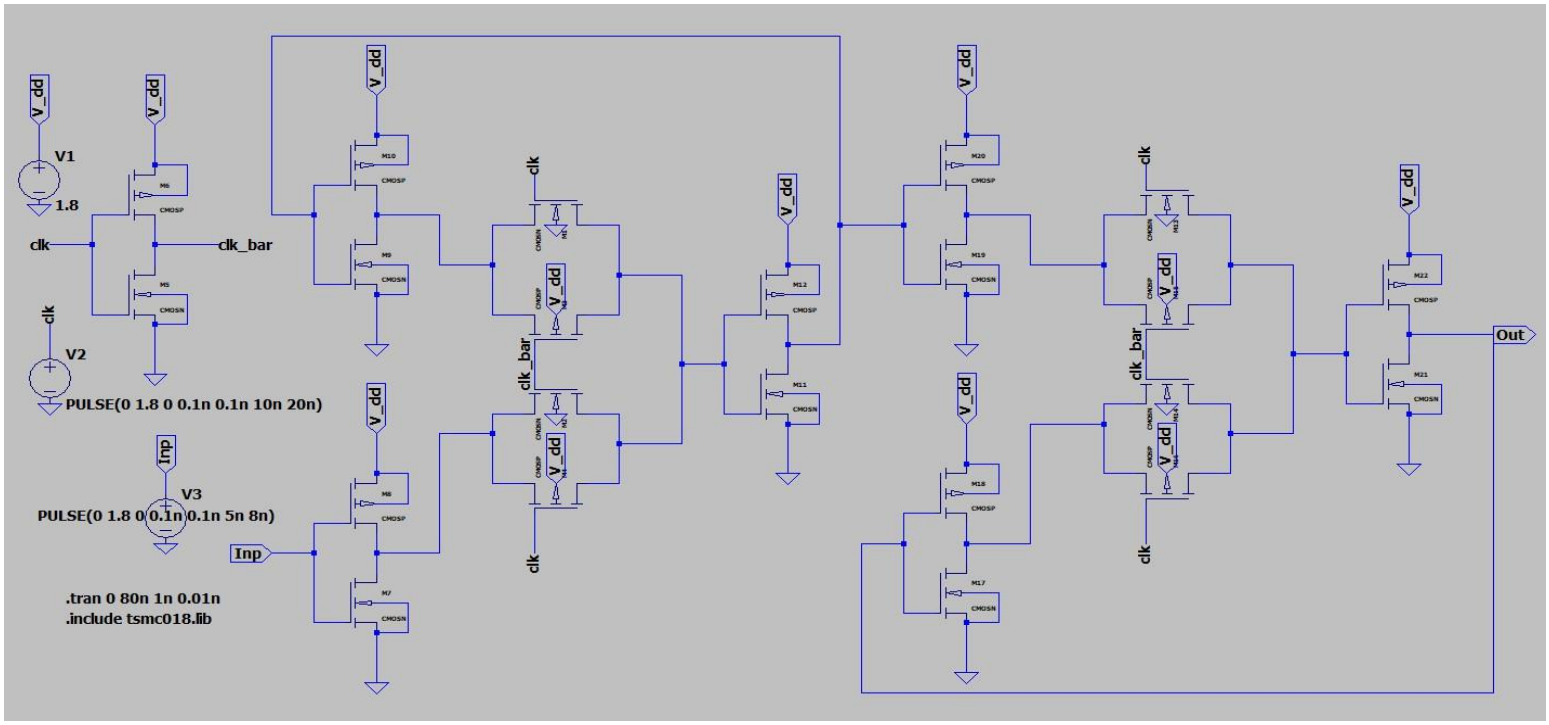
D – Flipflop Using Transmission Gate Logic

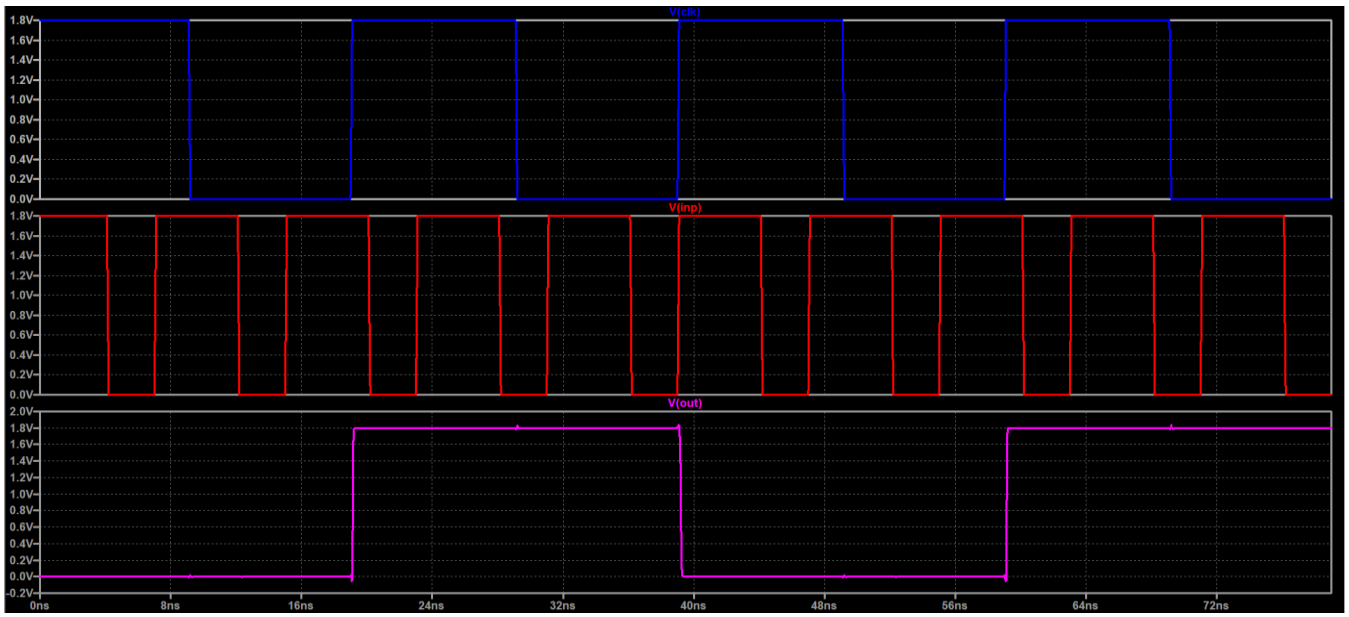
Objective:

- To implement D–Flipflop using Transmission Gate Logic

Circuit Diagram of implementation of D–Flipflop using Transmission Gate Logic:

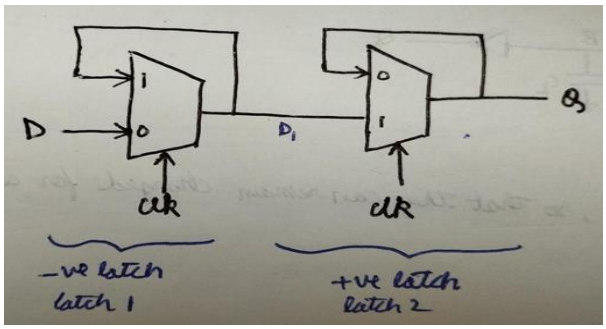


Simulation results:



Discussions:

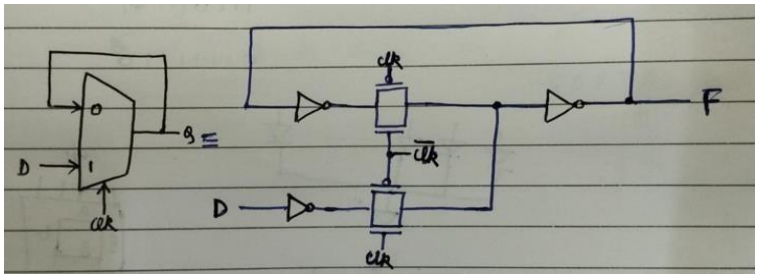
- The logic of the D-Flipflop is shown below–



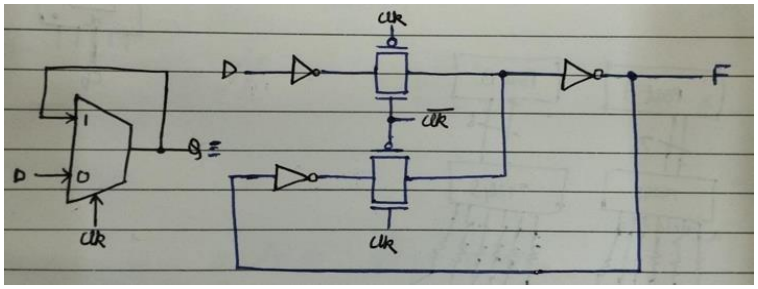
The circuit shown is a **Master-Slave D-Flipflop**, which consists of 2 D-Latches connected, the first one being a negative D-Latch, while the second one being a positive D-Latch.

- When **clk = 0**, the data input (D) of latch1, is passed to its output (D_1), while latch2 being a positive latch, cannot change its state and stores the last value, Q of the previous positive edge of the clock.
  When **clk = 1**, latch1 being a negative latch, cannot change its state and stores the last value of D just before the transition of the clk from 0→1, while latch1's output is passed to the output of latch2, which is the last value of D just before the transition of the clk from 0→1.
  The result is that the value of D at the positive edge of the clock is sampled and sent to Q. Thus, **the output can only change state when the clock makes a transition from Low to High**.

- The logic of the positive latch is shown below–



- The logic of the negative latch is shown below–



- Without the static CMOS inverters, the latch circuit can latch onto any value of input, which need not be only 0V or V_{DD}. We introduce static CMOS inverters in the circuit, thus using the **regenerative property** of CMOS inverters to make it a bistable circuit.

- We set the widths of the NMOS pass transistors to be **1 $\boldsymbol{\mu m}$** and PMOS pass transistors to be **2 $\boldsymbol{\mu m}$**. This is because resistance of a transistor between source and drain terminals is inversely proportional to the width of the transistor ($R_{eq} \propto \frac{1}{w}$). So, for the pass transistors to have lesser resistance, we increase their widths.

- The widths of the NMOS in the inverters are set to be **180nm** and those of PMOS are **1080nm**. These widths are used to get symmetric VTC curves for the inverters.