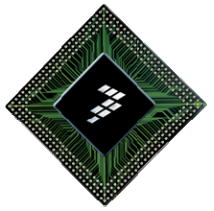
March 25, 2010

MPC8572E Rev. K Device Errata Update



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Disclaimer

This document is an attempt to release information about newly discovered errata in a timely manner. As such, please understand that all errata listed in this document are a work in progress and workarounds and dispositions may change as more information is learned.

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8572 Errata Update as of March 25, 2010

Rev. K errata document plus this updated errata addendum comprise all known errata on the 8572:

►New

- PCI-Ex 6: PCI Express Hot Reset event may cause data corruption

PCI-Ex 6: PCI Express Hot Reset event may cause data corruption

►**Description**

When the PCI Express controller is configured in EP Mode, if the controller detects an in-band Hot Reset event from its upstream device (either RC or Switch) before it finishes processing an inbound memory write TLP, the following may occur:

•TLP received right before the Hot Reset event may be discarded

•Data corruption may occur on the first inbound memory transaction received after the Hot Reset event.

Depending on the type of the first inbound memory transaction received after Hot Reset, data corruption may occur as below:

•If it is a memory write, the transaction may finish with data corruption at the target.

•If it is a memory read, the transaction may be decoded incorrectly and the return data might be incorrect.

PCI-Ex 6: PCI Express Hot Reset event may cause data corruption

►**Impact**

This only affects devices with PCI Express controller configured in EP Mode.

An inbound memory write TLP received by the PCI Express controller in EP Mode may be discarded, if a Hot Reset event is detected while the controller is still in the middle of moving the payload data of this memory write TLP from its receiver buffer toward the packet destination. As a consequence, data corruption may also occur on the first inbound memory transaction received right after this “inbound memory write followed immediately by a Hot Reset event” sequence.

Note that after the data corruption occurs, the system will return to normal operating condition.

If the first inbound transaction received is a configuration cycle, after the above mentioned “inbound memory write followed immediately by Hot Reset event” sequence, the configuration cycle will finish normally, with no error. Since a Hot Reset event resets all the configuration space registers in any PCI Express EP controller, per PCI Express base specification requirements, the upstream RC must re-configure all these registers after the Hot Reset event. Therefore, with the normal PCI Express programming model, there are always configuration cycles before the upstream device can send memory transactions to downstream EP controllers, which means the data corruption scenario after the Hot Reset event might not happen for most applications. However, the Memory Write TLP received immediately before the Hot Reset event might still be discarded. End product designers must check against their application programming model and determine the actual impact and appropriate workaround adoption.

The above described error will not occur in any of the following conditions:
•If the last inbound memory transaction received immediately before the Hot Reset event is a memory read, or,
•If the system (PCI Express controller) is idle in its inbound path when the Hot Reset event occurs.

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PCI-Ex 6: PCI Express Hot Reset event may cause data corruption

►**Workaround**

When possible, before issuing the Hot Reset, the upstream RC or Switch should quiesce the system first to ensure no inbound traffic is flowing into the Freescale PCI Express EP controller. This prevents the above mentioned "inbound memory write followed immediately by Hot Reset event" sequence from occurring. The exact requirement and action required to quiesce the system is dependent on system, application and software used. For example, some requirements may include, but not be limited to, using a software semaphore at the RC system side to stop the new memory requests targeting the downstream Freescale PCI Express EP controller from the RC system's software API layer or DMA controller.

Once such "quiescing system" actions have been finished, the RC system can send a configuration write cycle to clear the Memory Space bit in the Freescale PCI Express EP controller's Command Register, followed by a several micro-second delay to allow all previously received inbound memory writes to propagate through the EP controller. A Hot Reset command can then be applied.

If an "inbound memory write followed immediately by Hot Reset event" sequence cannot be avoided, do the following. Right after the Hot Reset event, the upstream RC can issue a dummy memory write followed by another write or read to the read-only PEX_IP_BLK_REV1 memory-mapped register in the downstream Freescale device with PCI Express controller configured in EP Mode. The RC can then re-transfer the last memory write TLP that occurred right before the Hot Reset event and resume other normal traffic.

►**Disposition**

No Plans to Fix.

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