

BGT70

Transceiver Chipset for E-band Backhaul
Applications from 71 to 76 GHz

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Target Specification

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Target Specification

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Previous Revision: Rev. 1.3

Page	Subjects (major changes since last revision)
all	Update target specification according to current measurement results
all	Add additional information about application
all	Updated specification
all	Updated block diagram

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1 **Product Features**

1.1 **Major Features of BGT70 Transceiver Chipset**

- BGT70 covers the frequency range from 71 to 76 GHz
- Fabricated with silicon-germanium (SiGe) Infineon process technology
- Housed in a **embedded Wafer Level Package (eWLB)** of Infineon technology
- BGT70 can be programmed via SPI interface to work either in transmit (Tx) or/and receive (Rx) mode
- Zero IF – differential I/Q interface – direct conversion architecture
- Differential RF transmit output signaling
- Differential RF receive input signaling
- Differential intermediate frequency I/Q signaling
- Peak detector at Modulator output on the transmit path
- Peak detector at PA output on the transmit path
- BITE (Built in test equipment) for EOL test in production at Infineon to verify RF performance
- SPI interface
- BIST (Build-In-Self-Test) for self-test and calibration in production at Infineon to verify RF performance
- Can be used in TDD or FDD systems



Product Name	Package	Marking
BGT70	PG-WFWLB-119-1	70Vxx

1.2 Applications

- E-Band 71 to 76 GHz FDD or TDD applications such as mmWave backhaul for mobile LTE basestations.

1.3 Description

The connection to the basestation was so far planned for lower data rates (few 100 MBit/s) and needs now increased capacity. To do so, the backhaul technology comes into place. A solution using wireless backhaul in the E-Band (71 to 76 GHz and 81 to 86 GHz) will open up more than 10 GHz frequency range. This enables datarates higher than 1 Gbit/s for video and data service, sufficient to support LTE/4G mobile communication. Infineon business approach will enable such Gbit service with the latest E-Band chipsets.

With Infineon's advanced SiGe (Silicon Germanium) technology with a transit frequency of 200 GHz, we can integrate all RF (Radio Frequency) building blocks, like Power Amplifier (PA), Low Noise Amplifier (LNA), Mixer, Programmable Gain Amplifier (PGA), Voltage Controlled Oscillator (VCO) and more into a single chip. This technology is proven and fully qualified for other Infineon Millimeter- and Microwave chipsets already.

Furthermore, Infineon is the leading company to house these single chipsets into a plastic embedded Wafer Level Package (eWLB) which can be processed in standard SMT flow. With the Infineon packaged chipsets, customer can reduce production cost and time-to-market significantly.

1.4 Block Diagram of BGT70 Transceiver Chipset

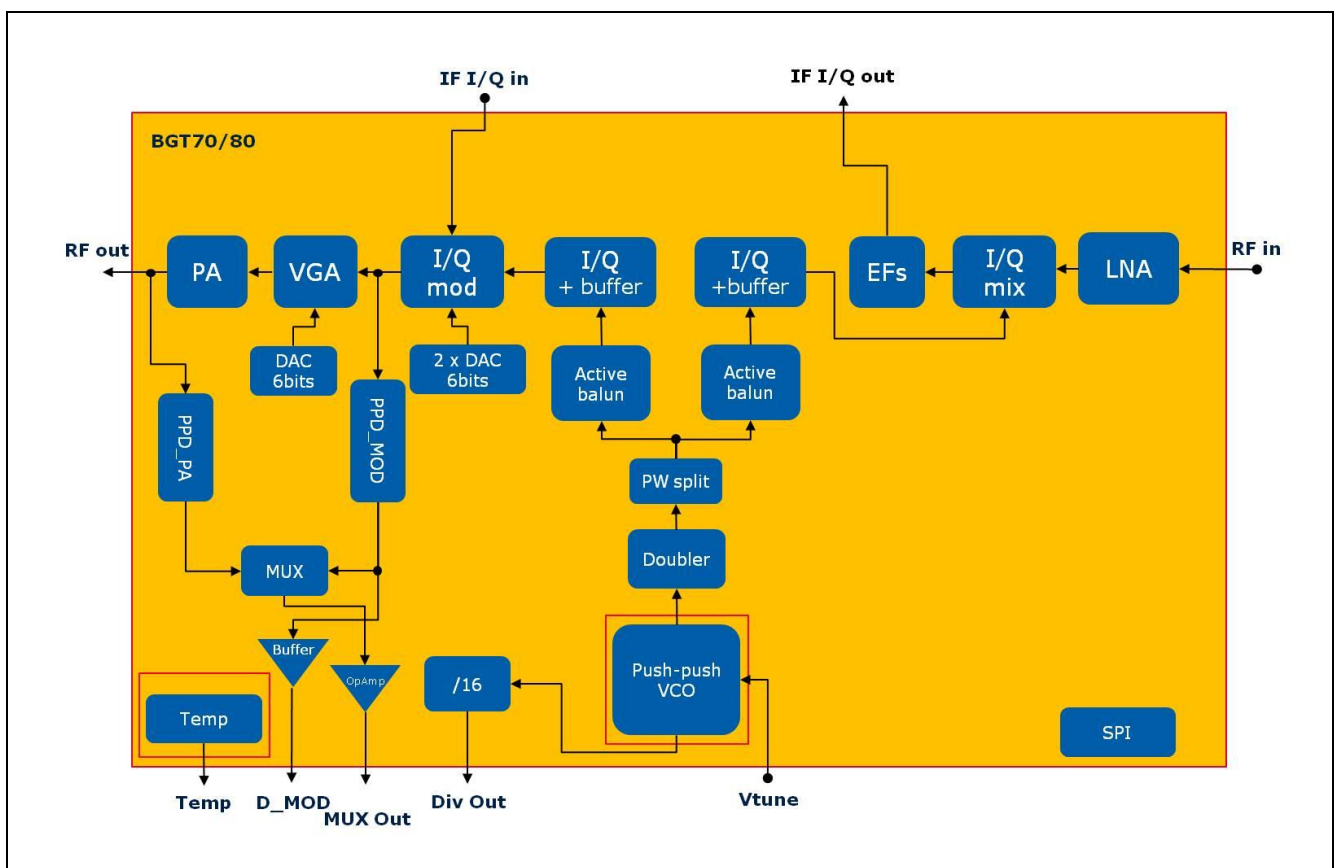


Figure 1 Block Diagram of BGT70 Transceiver Chipset

Pin Definition and Function

Figure 2 shows the bottom view of BGT70 package eWLB PG-WFWLB-119-1 with the pin number assignment. Their function of each pin is described in **Table 1** below.

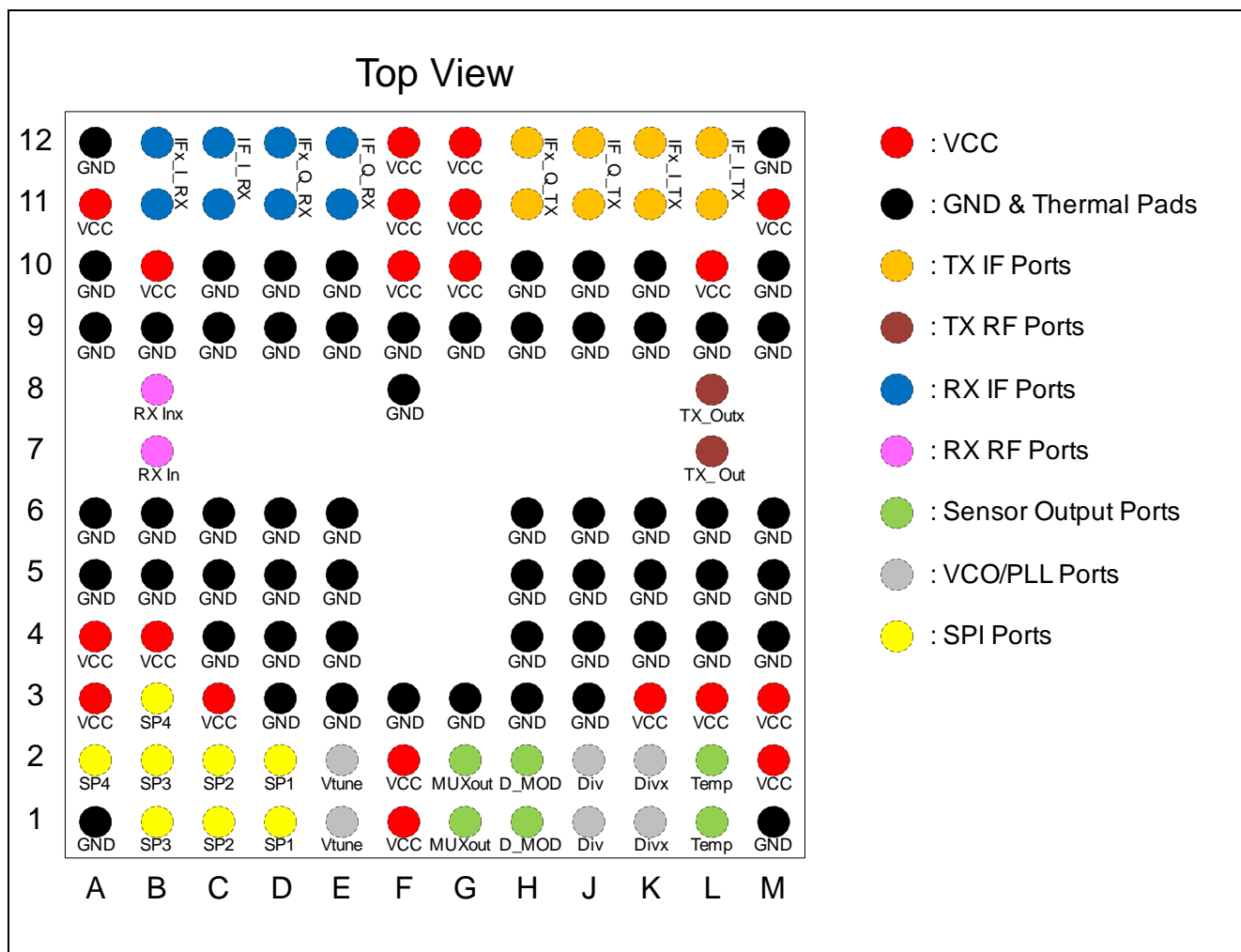


Figure 2 Pin Number Assignment of BGT70 package eWLB PG-WFWLB-119-1 (Top View)

Table 1 Pin Definition and Function

Pin No.	Name	Function
A3, A4, A11, B4, B10, C3, F10, F11, F12, G10, G11, G12, L10, M11	Vcc	DC supply for the transceiver chip – 3.3V
K3, L3, M2, M3	Vcc_Temp	Supply voltage for the temperature sensor – 3.3V
F1, F2	Vcc_VCO	Supply voltage for the VCO – 3.3V
E1, E2	Vtune	VCO tuning voltage

Table 1 Pin Definition and Function

[illegible]

Note: all pins described in the same line need to be connected on the PCB.

2 Target Specifications for BGT70 Chipset

Following tables show the target specification of Infineon's BGT70 transceiver chipset. The values are based on the measurement results of current BGT70 samples. All the values are subjected to change after the final qualification.

The reference for all specified data is the Infineon Application board defined in chapter 5.

2.1 General Specifications

Table 2 General Specifications

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Temperature Range	T	°C	-40		85	Chip backside temperature (measured with the on chip temperature sensor)
Package Rth (Chip to Board)	Rth	K/W		tbd		
ESD protection (HBM)	ESD _{HBM}	kV		1		All pins, DC, I/O, and RF
Frequency Range	F	GHz	71		76	
Voltage Supply	Vcc	V	3.135	3.300	3.465	
Current Consumption						
- IC powered on, TX off, RX off	ICoff	mA		310		@ max power
- TX on, Rx off	ICTX			460		
- TX off, RX on	ICRX			335		
- TX on, RX on	ICTRX			520		@ max power

2.2 Transmitter

Table 3 Target Specifications of Transmit Path

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Tx Output						
Output Signaling						differential
Output Referred P-1dB	OP-1dB _{TX}	dBm		12		differential in 100 Ω load This value includes already the 2dB loss of the eWLB package
Output Referred IP3	OIP3 _{TX}	dBm		22		
Saturated Power	P _{sat}	dBm		16		differential in 100 Ω load This value includes already the 2dB loss of the eWLB package
PA Control Step	P _{ctrls}	dB	0.5	1	2	6bits
PA Control Dynamic Range	P _{ctrl_d}	dB		20		
Tx Chain Gain	G _{TX}	dB		25		
LO feed-through Suppression	LO _s	dBc		25		before calibration
Image Rejection	IMR	dB		25		w/o feedback loop
Tx-Port Output Matching	S ₂₂	dB		-10		
Tx-Port Load Impedance	TX _{load}	Ω		100		differential
LO Generation						
VCO Tuning Voltage Range	V _{tune}	V	0		5.5 (6 opt.)	single tuning port

Table 3 Target Specifications of Transmit Path

Spec	Symbol	Unit	Value			Condition
Kvco	K _{VCO}	GHz/V	0.5		5	@ Tx output
Phase Noise						
@100kHz Offset	PN _{ssb100k}	dBc/Hz		-80		SSB
@1MHz Offset	PN _{ssb1M}	dBc/Hz		-100		SSB
@10MHz Offset	PN _{ssb10M}	dBc/Hz		-120		SSB
Divider Chain						
Output Signaling						differential
Divider Ratio	N _{DIV}			64		Referred to Tx output frequency
Divider Output Power	PDIV _{out}	dBm		-10		in 100 Ω differential load.
Divider Output Coupling on Board				AC		value to be specified
Divider Output Load Impedance	DIV _{load}	Ω		100		
IF Interface to TX Chain						
Input Signaling						differential
IF Bandwidth	IF _{BW}	MHz		500	1000	
IF Load Impedance	IF _{load}	Ω		50		differential
IF Coupling on Board				AC		value to be specified
Additional Features Spec.						
Output Power Vs PA Peak Detector Readout Relation	P _{out} PPD_PA (MUX Out)	dBm V	$P_{out} = t_1 * \ln\left(\frac{PPD_PA - y_0}{A_1}\right);$ $y_0 = 0.94755;$ $A_1 = 0.10191;$ $t_1 = 5.88103.$			

Table 3 Target Specifications of Transmit Path

Spec	Symbol	Unit	Value			Condition
PA Peak Detector Accuracy	PPD_PA _{acc}	dB	-2		+2	
Modulator Detector Bandwidth	D_MOD _{BW}	MHz		200		
Chip Backside Temperature (Temp) Vs Temperature Sensor Readout (Tsense) Relation	Temp Tsense	°C V	$Temp = \frac{Tsense - a}{b};$ $a = 1.36;$ $b = 0.005$			
Temperature Sensor Slope	Tsense_sl	mV/K		5		
Load Impedance for Tsense Output	Rsens _{load}	MΩ		1		

2.3 Receiver

Table 4 Target Specifications of Receive Path

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Rx Chain						
Input Signaling						differential
Conversion Gain	CG_{diff}	dB		20		differential in 400Ω load at IF Ports This value includes already the 2dB loss of the eWLB package
Double-Side-Band Noise Figure	NF _{dsb}	dB		8		This value includes already the 2dB loss of the eWLB package
Input Referred P-1dB	IP-1dB _{RX}	dBm	-15			
Input Referred IP3	IIP3 _{RX}	dBm	-5			
LO Residual Power at the RX Input	LO _{res}	dBm		-50		
RF-Port Input Matching	S ₁₁	dB		-10		
RF-Port Load Impedance	RF _{load}	Ω		100		differential
Rx Chain to IF Interface						
Output Signaling						differential
IF Bandwidth	IF _{BW}	MHz		500	1000	
IF Load Impedance	IF _{load}	Ω	400			differential
IF Coupling on Board				AC		value to be specified
I/Q Amplitude Imbalance	IQ _{AI}	dB		1		
I/Q Phase Imbalance	IQ _{PI}	deg		5		

3 Digital Control Interface

3.1 SPI (Serial Peripheral Interface)

The BGT70 is configured using a 4-wire SPI slave interface. The interface is always enabled and works autonomous; therefore no registers are required to control the SPI interface. It is used to configure the internal modules of the BGT70 chip via registers. The main tasks are to set the mode of operation of the Tx and/or Rx chain. Communication with an external micro controller is done via the four dedicated pins DATAOUT, DATA, CLK and ENABLE.

Note: SPI communication must be avoided during transmission/receiving to prevent a degradation of the system phase noise performance.

(Note: Detailed register map will follow)

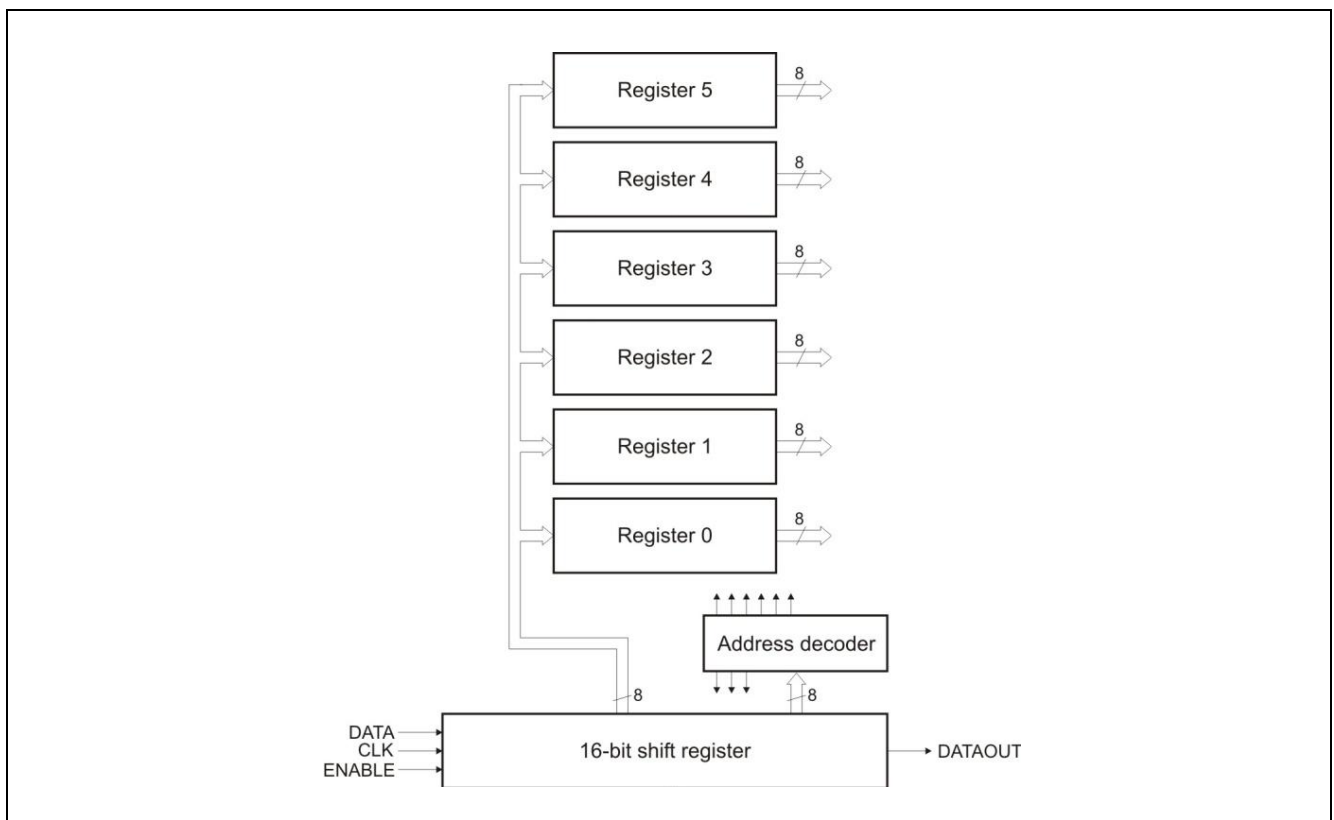


Figure 3 SPI Block Diagram

The SPI interface consists of a 16-bit shift register and six 8-bit registers (**Figure 3**). The interface is programmed by a 16-bit sequence consisting of a control (CMD)/address (ADDR) byte and a data byte (DATA). The transmitter circuit is configured by writing configuration data into the six 8-bit registers (Register 0 to Register 5).

3.2 Module Description

The SPI interface is programmed by a 16bit sequence consisting of two mode bits CMD, 6 address bits ADDR and 8 data bits DATA. This sequence is described in **Figure 4** and **Table 5**. The mode CMD is used to choose between read and write access.

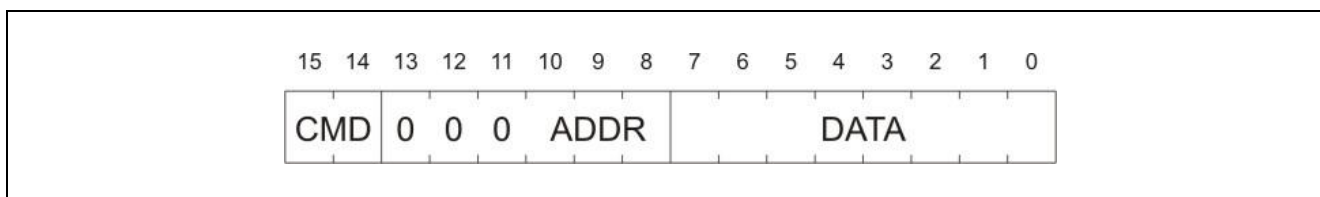


Figure 4 SPI Protocol

Table 5 SPI – Protocol Field Description

Field	Bit position	Description
CMD	15:14	Mode bit: 11 _B – write 10 _B – read 01 _B – not used 00 _B – not used
ADDR	13:11 10:8	000 _B – reserved Register address
DATA	7:0	Data

3.3 Timing

The signal ENABLE acts as chip select and is low-active. The transmission of the serial data provided to the serial data input DATA is started by a negative edge on the enable input ENABLE. Data at the serial input DATA is then read at the falling edge of the clock input CLK. The most significant bit (MSB) is read first (**Figure 5** and **Figure 6**).

The serial output DATAOUT is high impedance while ENABLE remains inactive (logic high). Output data is clocked out at the rising edge of the clock input CLK with the MSB first. The timing parameters specified in **Table 6** have to be considered.

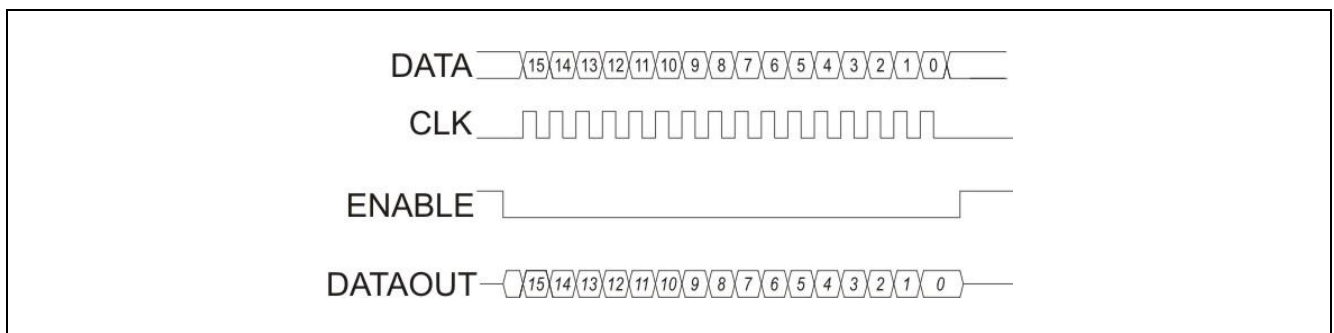


Figure 5 4-wire SPI Interface Transmission Scheme.

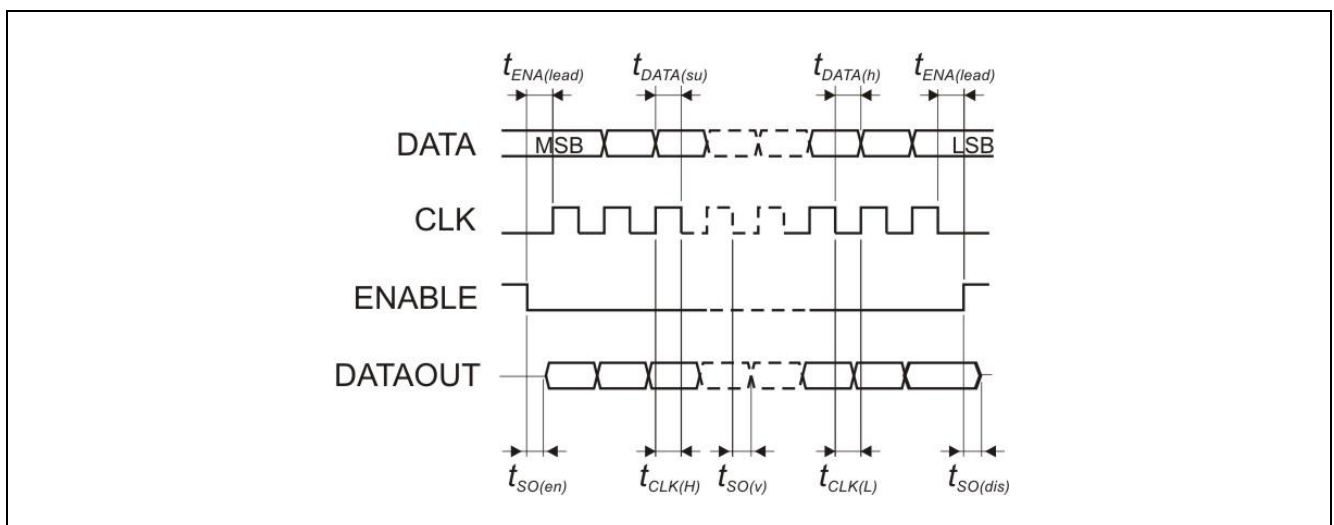


Figure 6 4-wire SPI interface timing diagram

Table 6 **Timing Characteristics**

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
Serial clock frequency	f_{CLK}			50	MHz
Serial clock high time	$t_{CLK(H)}$	10			ns
Serial clock low time	$t_{CLK(L)}$	10			ns
Enable lead time	$t_{ENA(lead)}$	20			ns
Enable select lag time	$t_{ENA(lag)}$	20			ns
Data setup time	$t_{DATA(su)}$	10			ns
Data hold time	$t_{DATA(h)}$	10			ns
Clock to serial output valid time	$t_{SO(v)}$			20	ns
Enable to serial output active time	$t_{SO(en)}$			100	ns
Enable to serial output high impedance time	$t_{SO(dis)}$			100	ns

3.4 Logic Levels

The digital inputs are designed to be compatible with standard CMOS / TTL levels (reported in **Table 7**). Unconnected input pins are at HIGH level. I/O interface is shown in **Figure 7** to **Figure 10**.

Table 7 **Logic levels for pins DATA, DATAOUT, CLK, and ENABLE**

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
LOW level / input (DATA, CLK, ENABLE)	$V_{IN(L)}$	0		0.8	V
HIGH level / input (DATA, CLK, ENABLE)	$V_{IN(H)}$	2.0		V_{CC}	V
Input current ($0V \leq V_{IN} \leq V_{CC}$)	I_{IN}	-150		150	μA
LOW level / output (DATAOUT)	$V_{OUT(L)}$	0		0.66	V
HIGH level / output (DATAOUT)	$V_{OUT(H)}$	$V_{CC} - 0.66$		V_{CC}	V
Output current (LOW)	$I_{OUT(L)}$	-1.5			mA
Output current (HIGH)	$I_{OUT(H)}$	1.5			mA

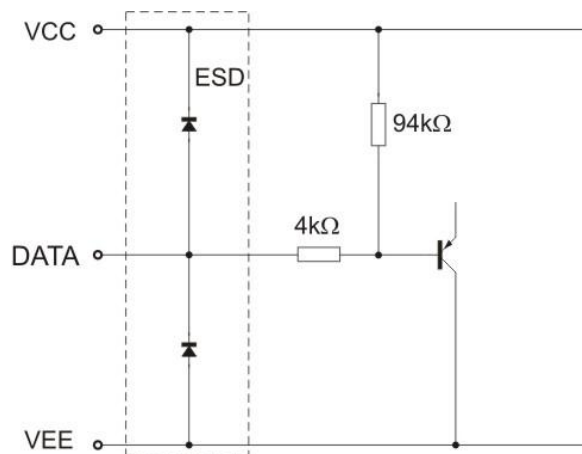


Figure 7 Data Input DATA

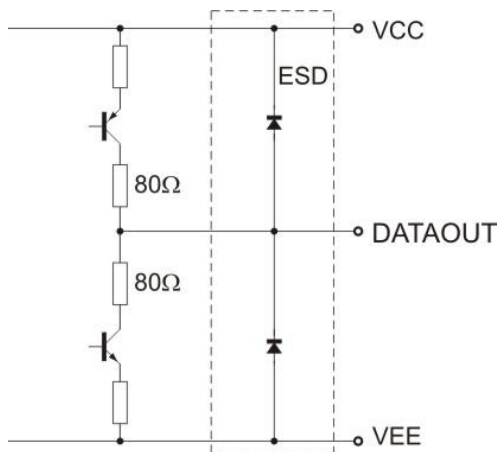


Figure 8 Data Output DATAOUT

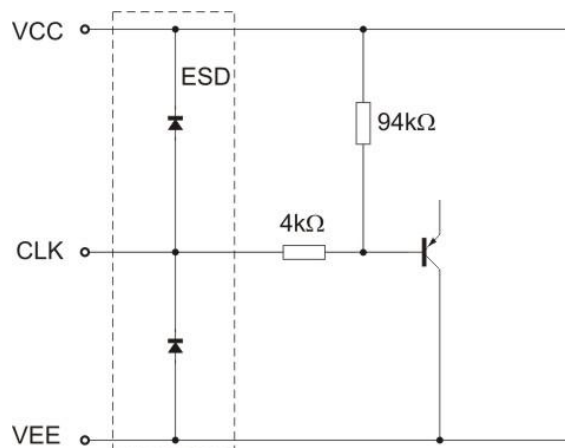


Figure 9 Clock Input CLK

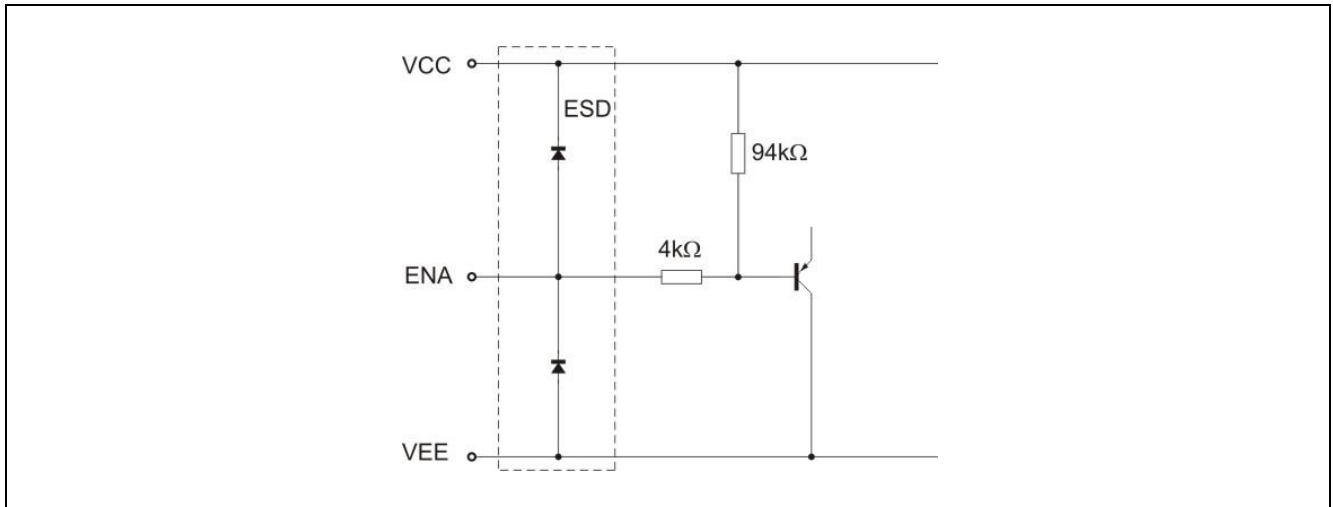


Figure 10 Enable Input ENABLE

3.5 Read Mode

Figure 11 shows a read command. The two most significant bits are set to 10_B to select the read mode, followed by three 0_Bs and three address bits (A2, A1 and A0) to select one of the six registers. The read sequence consists of two parts. In a first step, a read command is sent to the interface. The first most significant bit is set to 1_B followed by four bit set to 0_B, 10000_B, followed by three address bits (A2, A1 and A0) and eight data bits which may contain any arbitrary value. During the second part of the read sequence the selected 8-bit section is provided at DATAOUT. The command/address/data bits at DATA may contain any value.

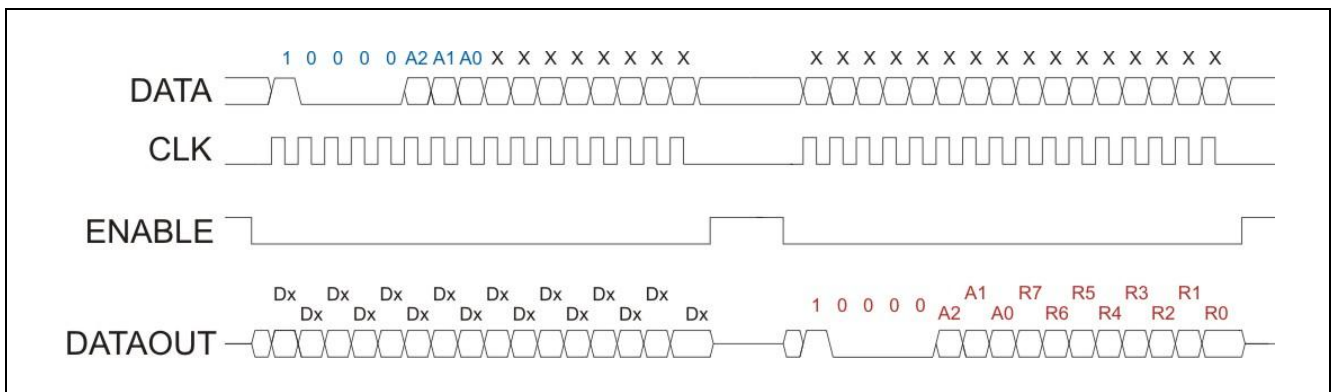


Figure 11 Read Mode Timing

3.6 Write Mode

Figure 12 shows a write command. The two most significant bits are 1_B to select the write mode, followed by three 0_Bs and three address bits (A2, A1 and A0) to select one of the six registers. The programming sequence is completed by eight data bits. While the 16-bit sequence consisting of command/address and data is read into the interface, 16 bits are shifted out at DATAOUT. The content of these bits depends on the previous command. The 16 bits at DATAOUT correspond to the previous command/address/data sequence.

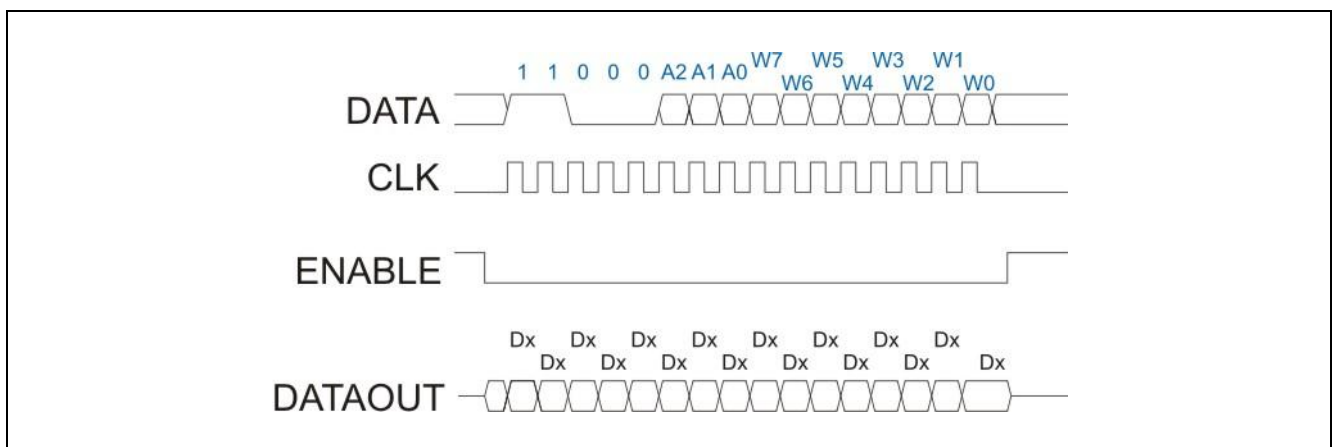


Figure 12 Write Mode Timing

4 Application Examples

4.1 E-Band Backhaul System with Frequency-Domain-Multiplexing (FDD)

In a FDD system, one BGT70 and one BGT80 chipsets are installed on each side of the link stations as shown in **Figure 13**. The two chips within one base station works in the TX or RX mode, respectively. For example, in the base station A, BGT70 is set to the receive mode (RX on / TX off) and BGT80 is set to the transmit mode (TX on / RX off). On the other hand, BGT70 is set to the transmit mode and BGT80 is set to the receive mode in the base station B.

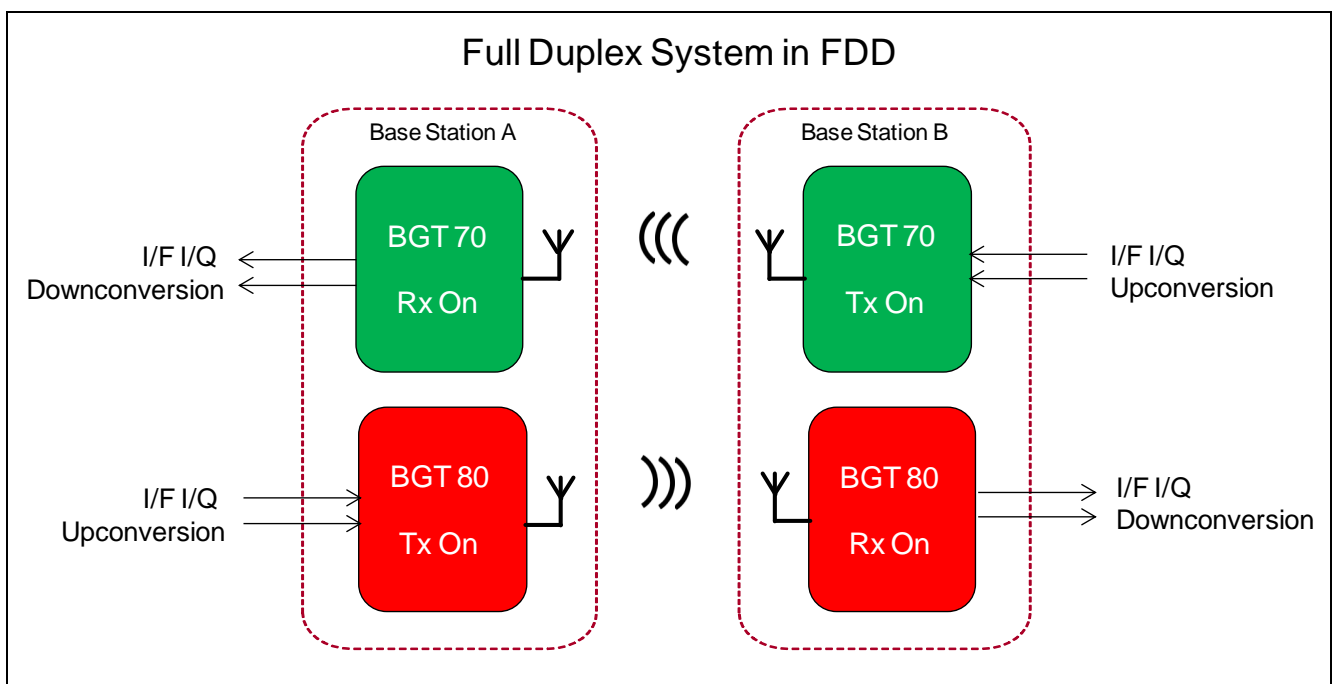


Figure 13 Application Example of BGT70 and BGT80 in a FDD System

4.2 E-Band Backhaul System with Time-Domain-Multiplexing (TDD)

In a TDD system, one BGT70 and one BGT80 chips are installed on each side of the link stations as shown in **Figure 14**. The two chips within one base station can work in the TX and RX mode independently. The two base stations need to be aligned to set one side to the transmit mode (TX on / RX off) and the other side to the receive mode (RX on / TX off) for the lower E-band (71 to 76 GHz) and for the higher E-Band (81 to 86 GHz) separately.

Because both the TX and RX modes on each chip are used in the application, discrete diplexer needs to be used to between the TX, RX ports and the antenna.

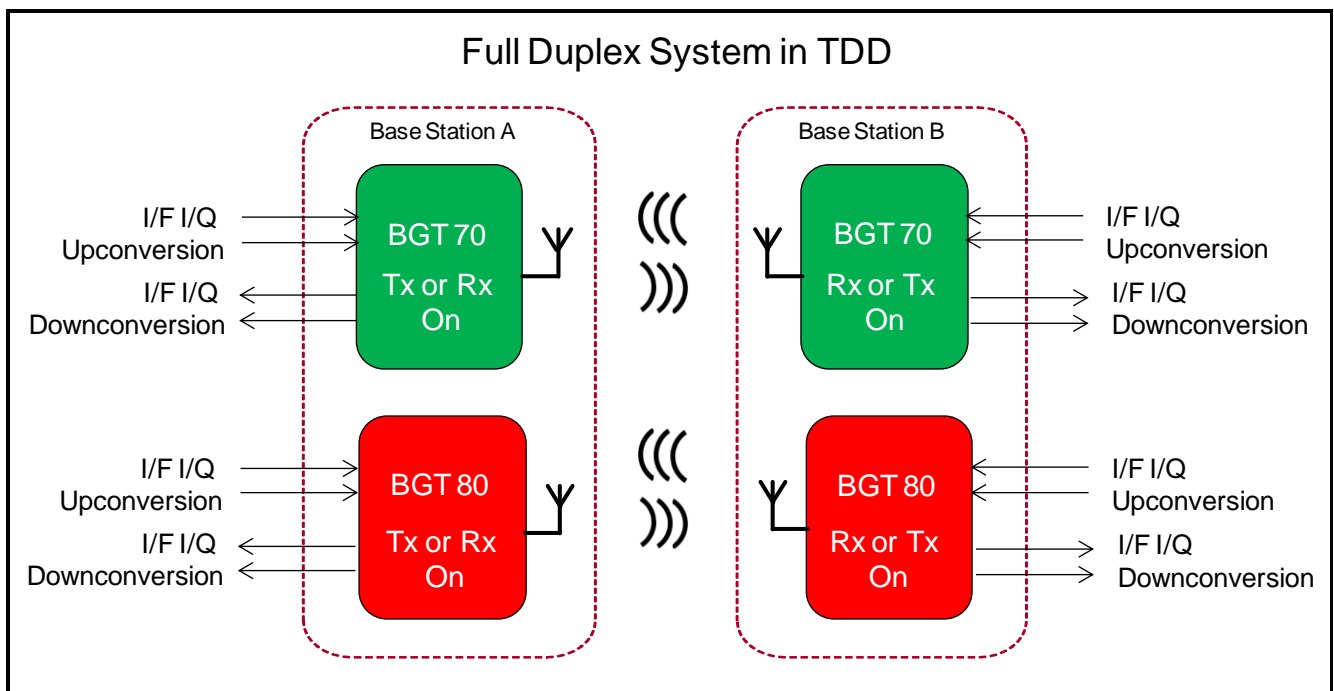


Figure 14 Application Example of BGT70 and BGT80 in a TDD System

5 Application Information

5.1 Application Diagram and Schematic

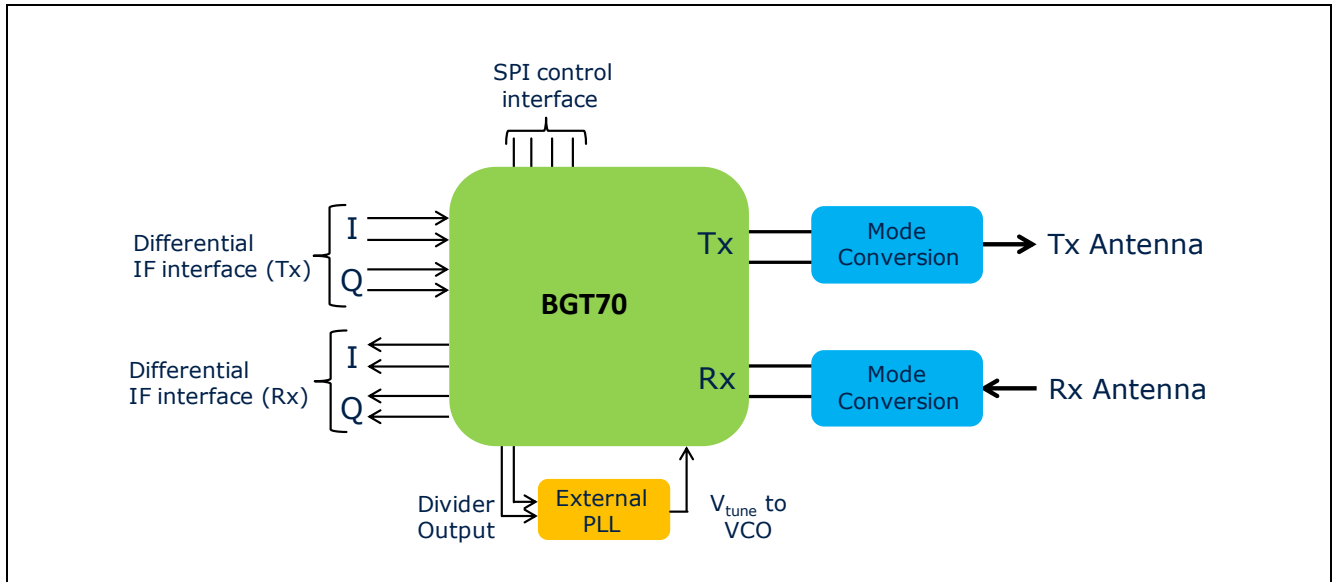


Figure 15 Application Diagram of BGT70

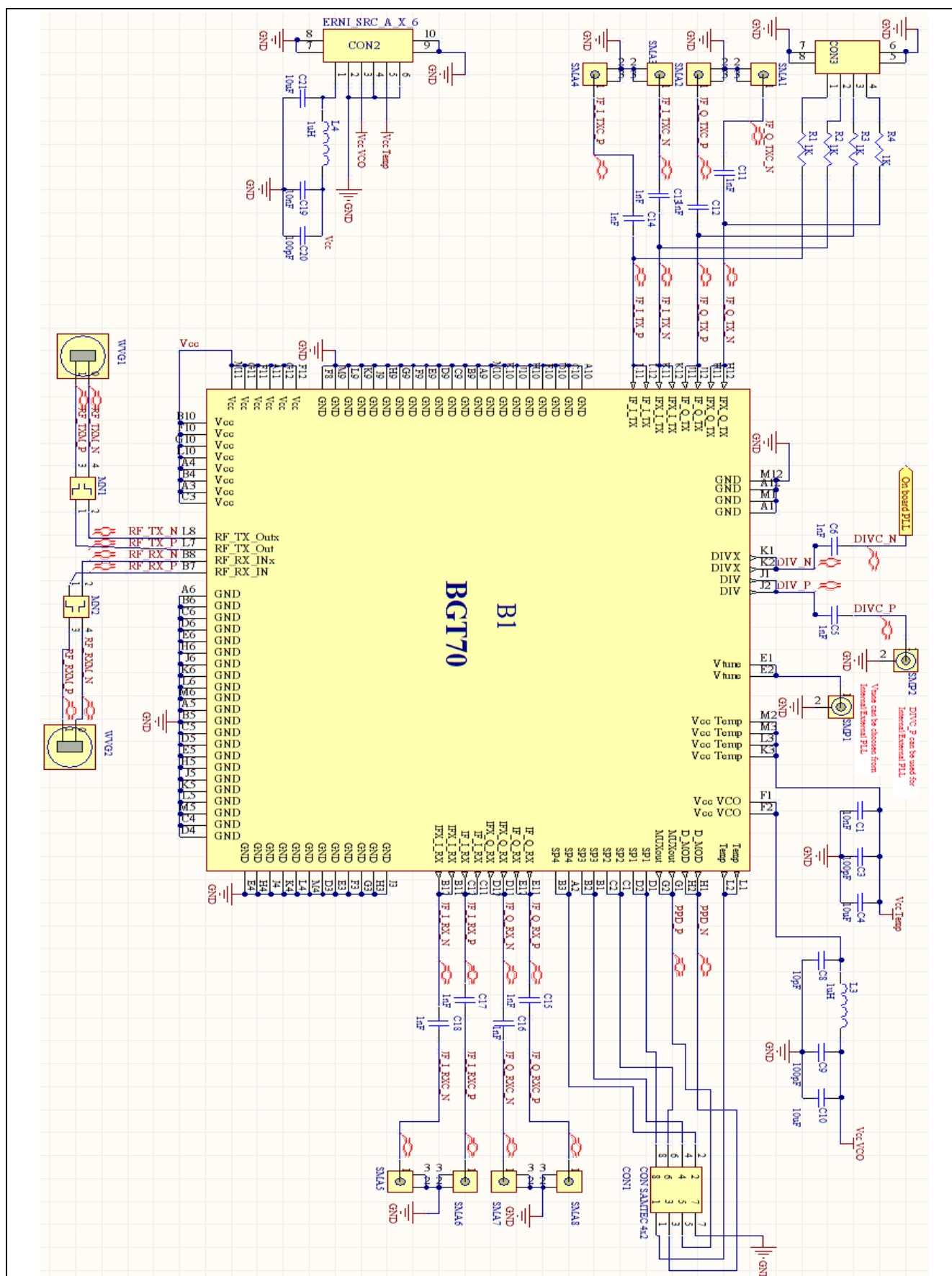


Figure 16 Schematic of BGT70 Application Circuit

5.2 Bill-of-Materials

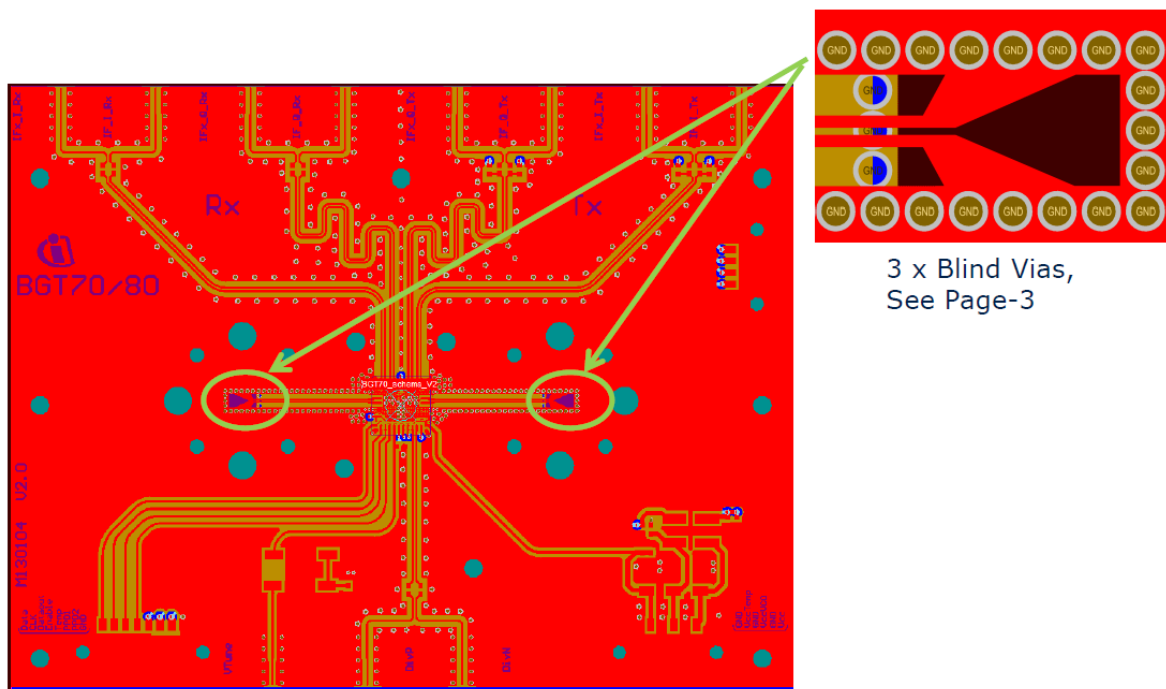
Table 8 shows the layout of the application board BGT70 version 2.2.

Table 8 Bill-of-Materials

Symbol	Value	Unit	Package	Manufacturer	Comment
B1	BGT70	-	eWLB	Infineon	RF transceiver chip
C1	10	nF	0402	Murata	RF bypass
C3, C9, C20	100	pF	0402	Murata	RF bypass
C4, C10, C21	10	uF	1206	AVX	DC filtering
C5, C6, C11, C12, C13, C14, C15, C16, C17, C18	1	nF	0402	Murata	DC block
C7, C8	10	pF	0402	Murata	RF bypass
L3, L4	1	uH	1210	Murata	DC filtering
CON1	8-Pin SRC	-	MiniBridge	ERNI	SPI & other readout functions
CON2	6-Pin SRC	-	MiniBridge	ERNI	DC supply
SMA1, SMA2	SMA connector	-	SMA	Johnson	IF Tx-Q differential interface
SMA3, SMA4	SMA connector	-	SMA	Johnson	IF Tx-I differential interface
SMA5, SMA6	SMA connector	-	SMA	Johnson	IF Rx-Q differential interface
SMA7, SMA8	SMA connector	-	SMA	Johnson	IF Rx-I differential interface
SMP2	Mini SMP connector	-	Mini SMP	Rosenberger	VCO Divider differential interface
SMP1	Mini SMP connector	-	Mini SMP	Rosenberger	Vtune (VCO Tuning voltage interface)
L1, L2	n.u.	-	-	-	Not used
R1, R2, R3, R4	n.u.	-	-	-	Not used
C2	n.u.	-	-	-	Not used
CON3	n.u.	-	-	-	Not used
MSWG_Tx, MSWG_Rx	WR12 Waveguide	-	-	-	RF transmission and reception interface
PLL	External PCB	-	-	Analog Devices	External using ADF4158

5.3 Application Board

Figure 17 shows the top view of the layout of the application board BGT70. **Figure 21** shows the top view picture of BGT70 after assembly. IF interface can be connected via the SMA ports (upper side). On-Board mode conversion circuits (differential <-> single mode) are implemented for the RF TX and RX ports. The TX port is on the middle right side and RX port on the middle left side. They can be connected with WR-12 waveguides. Down left side are the controls and sense pins while the DC supply pins are on the bottom right corner.



- Top Overlay → Yes
- Top Solder Resist → Yes
- Bottom Solder Resist → No
- NiAu plating
- Thick plating for Vias
- Drill size
 - 1.6 mm drill with 1.7 mm
 - 1.65 mm drill with 1.75 mm
 - 2.1 mm drill with 2.15 mm
 - 3.0 mm drill with 3.1 mm

BGT70 Application Board Version 2.2

Figure 17 Top view of the Application Board BGT70

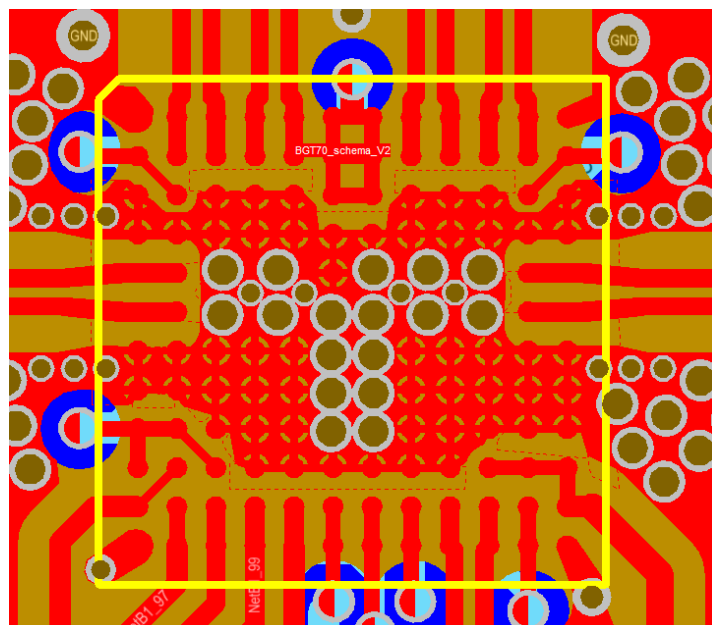


Figure 18 Zoom-in Picture of of the center area of Application Board BGT70. Landing pads and through thermal vias in the center.

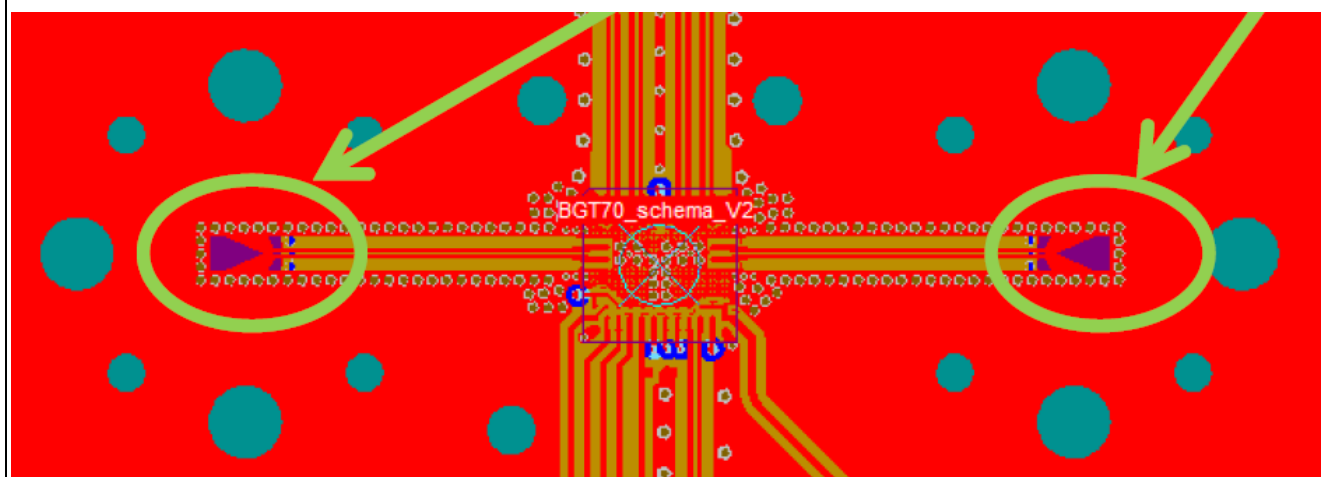


Figure 19 Zoom-in Picture of Transition Area of Application Board BGT70

Figure 20 shows the side view of the PCB layers. It consists of:

- 130 μm thick Rogers RO3003 material: as dielectrics for the RF transmission lines
- Rogers RO3003 material is recommended for these applications because of its excellent high frequency characteristics
- 400 μm thick FR4 material: as carrier of PCB for mechanical stability. Two cavities in the FR4 layer are shaped as transition from the RF microstrip lines on top metal layer to the waveguides with WR-12 flanges at the backside for TX and RX

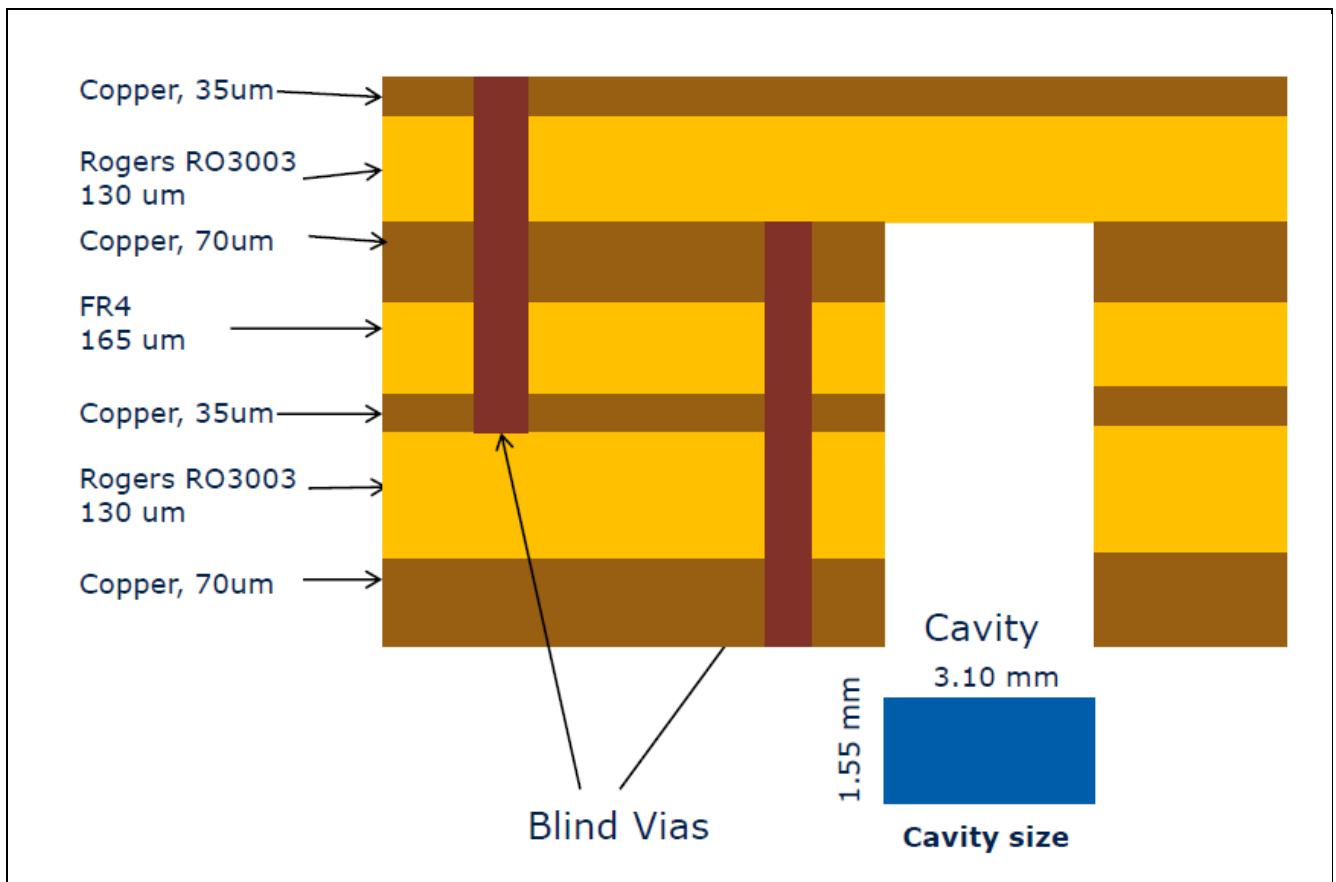


Figure 20 Cross Section of BGT70 Application Board

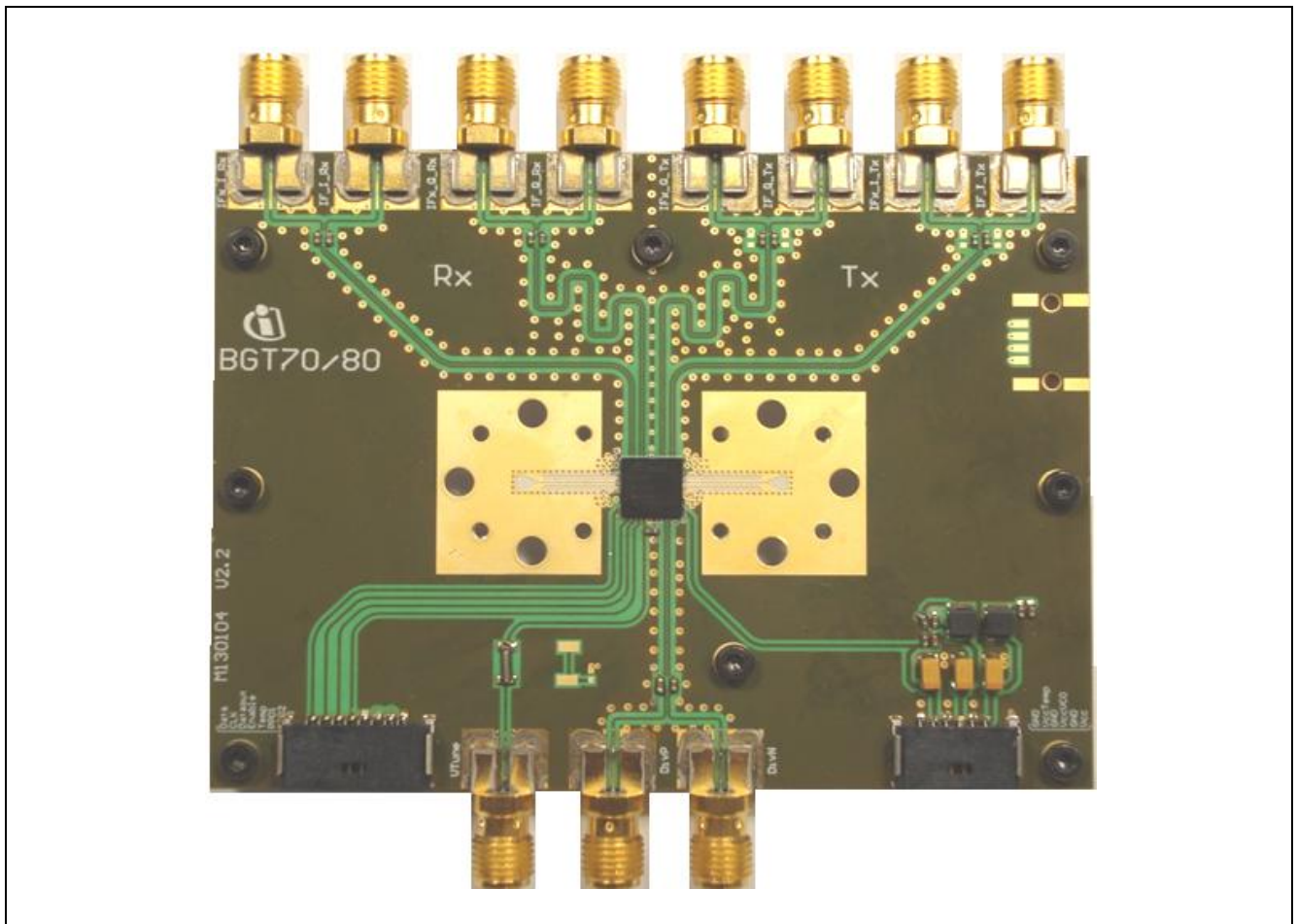


Figure 21 Picture of Application Board for BGT70 after Assembly

Table 9 Control Interface Description of BGT70 Application Board

Pin	Function	Description
Flat connector 1 (CON1)		
CLK	SPI clock	50 MHz
Data	SPI Data sequence (Control Board → Device)	See SPI description
Dataout	SPI Data sequence (Device → Control Board)	See SPI description
Enable	Chip Select	See SPI description
Temp	Temperature Sensor Output	DC Voltage
D_MOD	Modulator detector output	RF signal
MUXout	MUX output (PPD_PA or PPD_MOD DC level output)	DC Voltage
GND	Ground	Ground
Flat Connector 2 (CON2)		
VccTemp	DC Supply for Temperature Sensor	3.3V
VccVCO	DC Supply for VCO	3.3V
Vcc	DC Supply for RF Transmitter/Receiver Chain	3.3V
GND	Ground	Ground

Note: VccTemp, VccVCO & Vcc can all be connected together to one single 3.3V DC supply.

6 Package

The BGT70 chipset is in eWLB type package PG-WFWLB-119-1 with bump balls of diameter of 300 μm and height of 150 μm . **Figure 22** shows the BGT70 package.

Figure 23 shows the physical dimension of it. The package size is 6.0 x 6.0 x 0.8 mm³ with pitch of 500 μm .

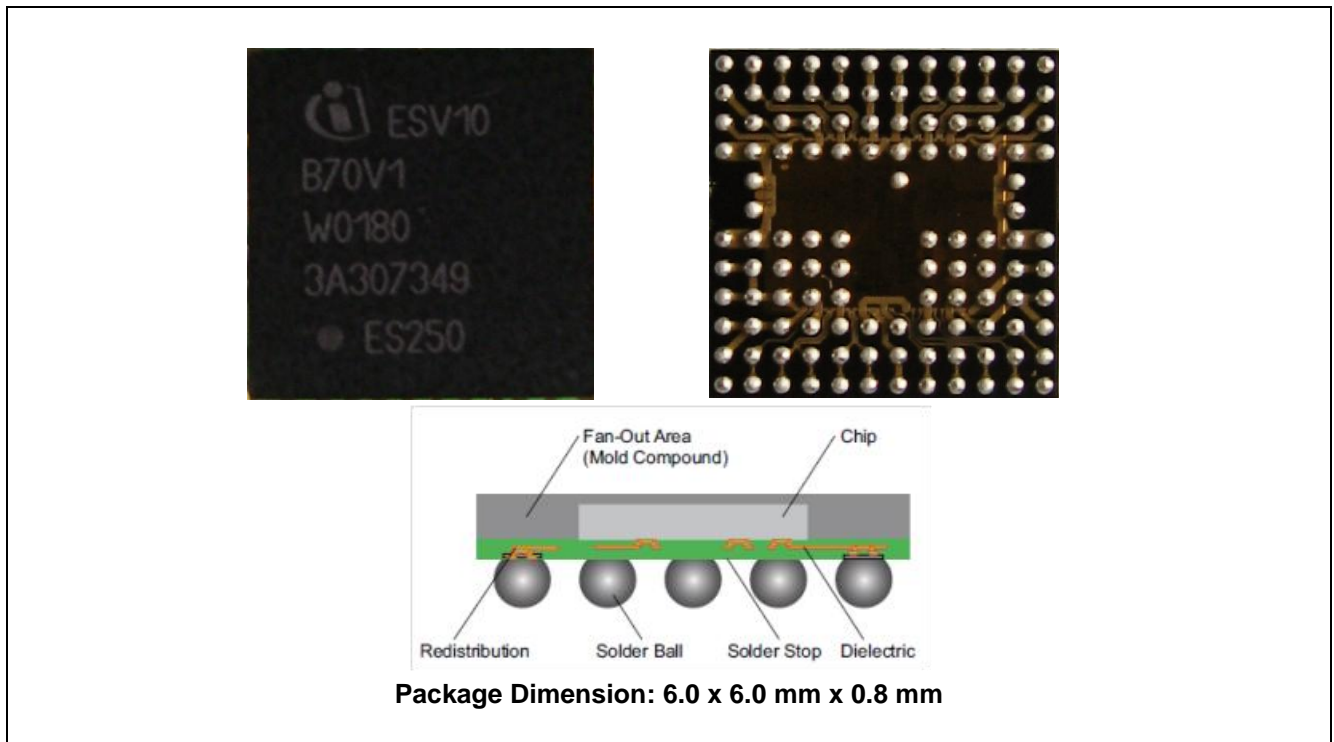


Figure 22 Top View (left), Bottom View (right) and Side View of BGT70 in eWLB Package

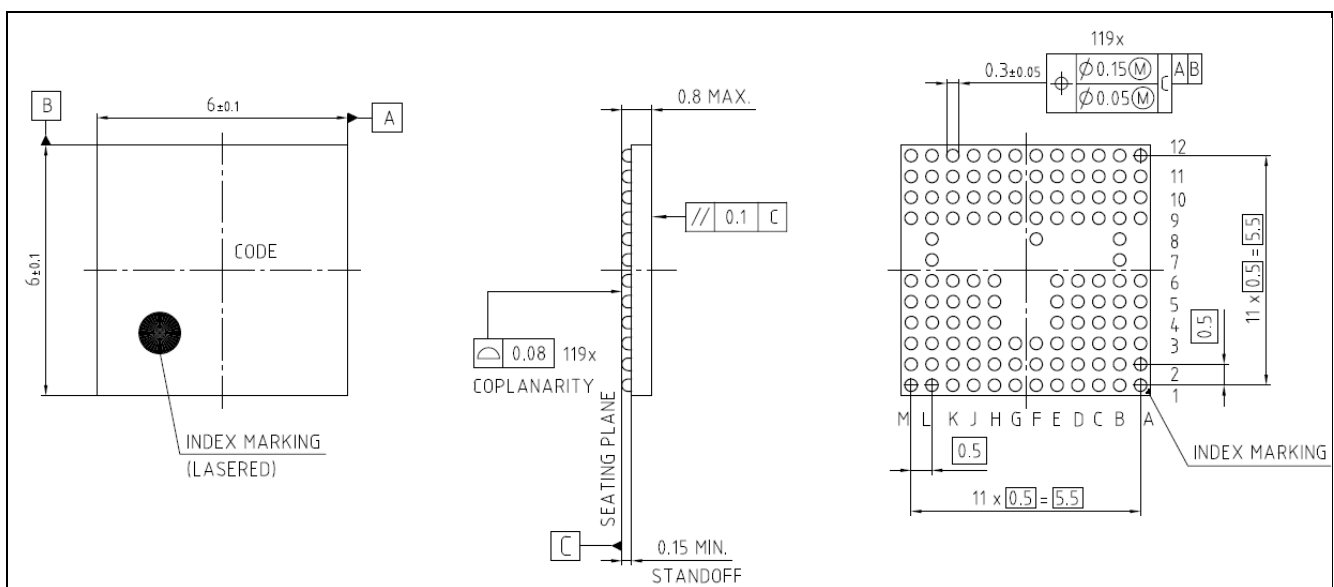
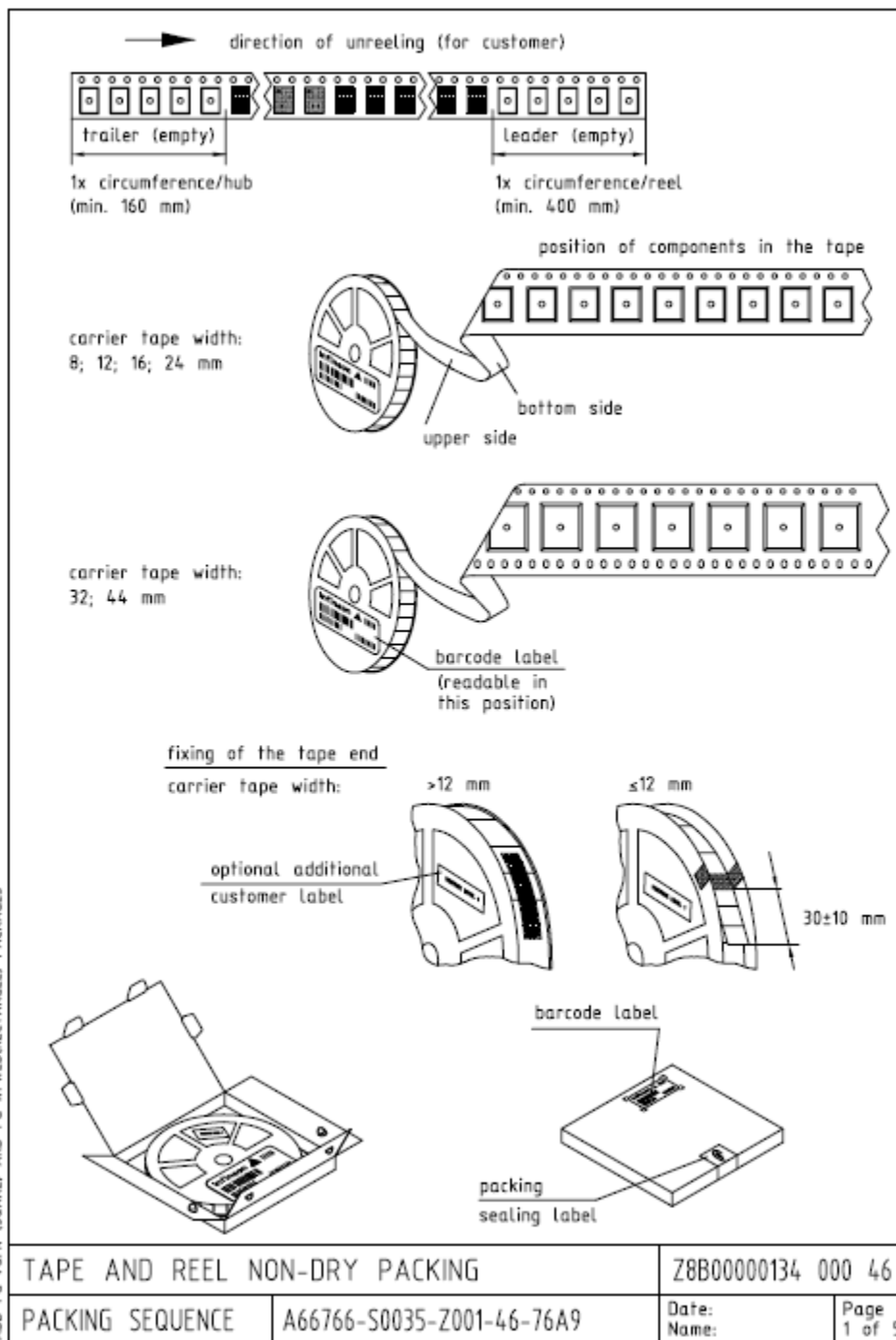


Figure 23 Dimension of eWLB Package PG-WFWLB-119-1 for BGT70 (left: top view; center: side view; right: bottom view)

Tape and reel information:

- Solder balls at bottom side, marking at top side
- 3000 pcs per reel



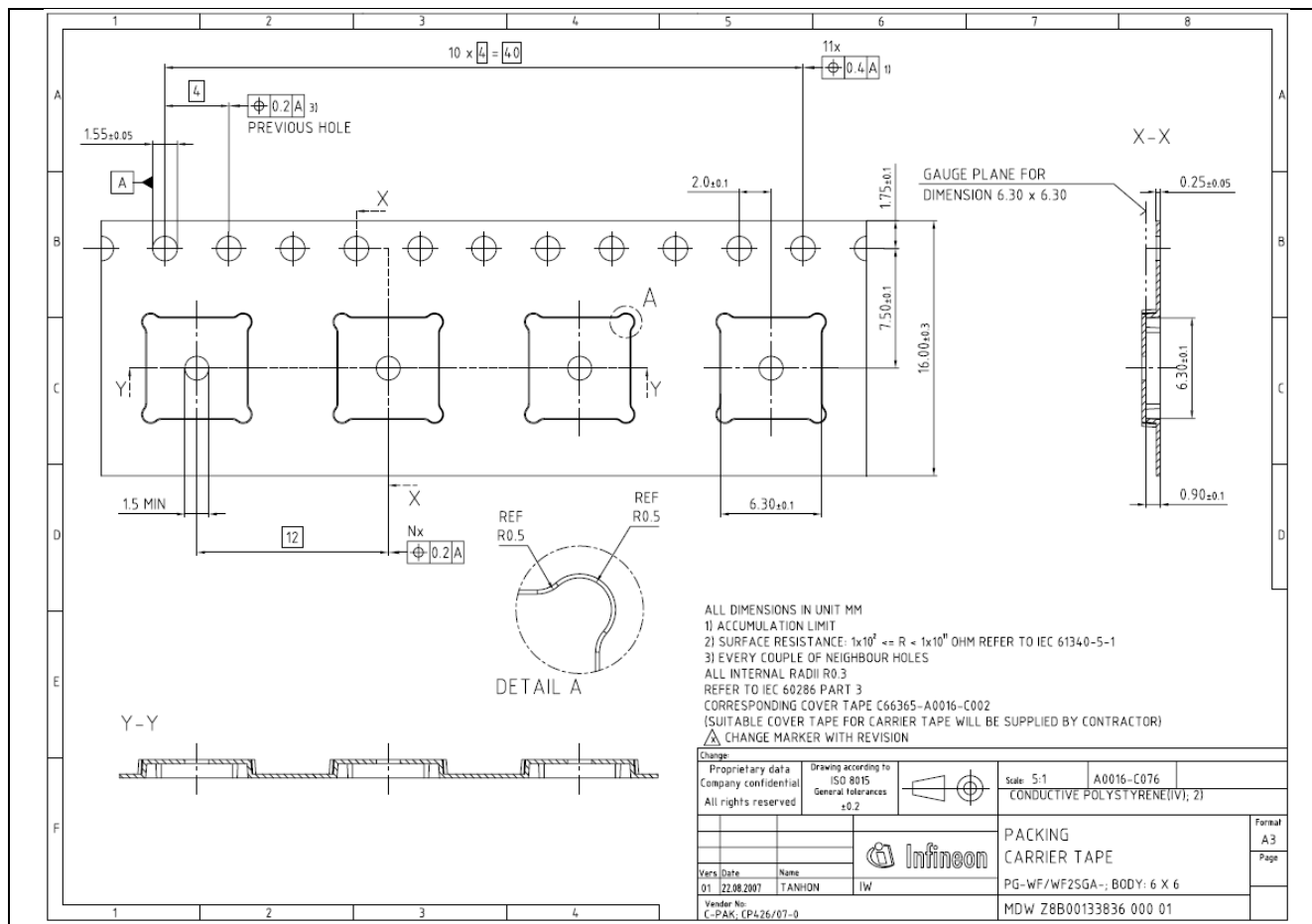


Figure 24 Tape and Reel Information of BGT80 in eWLB Package

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