# Cyclone<sup>®</sup> III EP3C40 Device Pin-Out PT-FP3C40-1 3

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Bank Number	VREFB Group		Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
31		VCCD_PLL3			1	F5	F6	J9										
31	VREFB1N0				2	E5	F5	H9										+
31 31	VREFB1N0 VREFB1N0	IO	DIFFIO_L1p		3	E4 B2	G6 G4	J8 D3	-	DQ1L	DQ1L		_					Adj.
31	VREFB1N0		DIFFIO_L1p			B1	G3	C2		DQTL	DQTL				DQ2L	DQ1L	DQ1L	Adj.
31	VREFB1N0		DII TIO_EIII		4		00	OZ.							DQZE	DQTE	DQTE	, ruj.
31	VREFB1N0				5													1
31	VREFB1N0							M9										1
31	VREFB1N0		DIFFIO_L2p				B2	D2				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Sep.
31	VREFB1N0	Ю	DIFFIO_L2n				B1	D1				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Sep.
B1	VREFB1N0		VREFB1N0		6	C2	G5	H7										
31	VREFB1N0		DIFFIO_L3p					E5										Adj.
31	VREFB1N0		DIFFIO_L3n			C1	ļ	E4		DQ1L	DQ1L							Adj.
B1	VREFB1N0		DIFFIO_L4p	nRESET		C3	E4	G6				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Adj.
31	VREFB1N0		DIFFIO_L4n		<u> </u>		E3	G5 H4				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Adj.
B1 B1	VREFB1N0 VREFB1N0		DIFFIO_L5p DIFFIO_L5n				1	H4 H3	-				_					Adj. Adj.
B1	VREFB1N0		DIFFIO_L6p					J5										Sep.
B1	VREFB1N0		Dil 1 10_Lop		7		1	00										оер.
B1	VREFB1N0		DIFFIO_L6n	1	Ĺ		<b>†</b>	G7	1	1	1	1	1		1		1	Sep.
B1	VREFB1N0			1	8		1	T .	1	İ	İ	1	1		İ	İ	İ	1
							1	1	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	DQS2L/CQ3L,	1
B1	******	Ю	DIFFIO_L7p		9	D3	C2	E3	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	CDPCLK0	Sep.
B1	VREFB1N1				10													
B1	VREFB1N1		DIFFIO_L7n				C1	F3				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Sep.
B1		GND			11													
B1		Ю	DIFFIO_L8p			D2	D2	F5		DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Adj.
B1	VREFB1N1	10	DIFFIO_L8n	DATA1, ASDO	12	D1	D1	F4										Adj.
B1			VREFB1N1		13	F3	H7	L5	1			500	2011	804	0.00	2011	2011	
B1 B1	VREFB1N1 VREFB1N1		DIFFIO_L9p DIFFIO L9n		<u> </u>		H6 J6	G4 G3				DQ2L DQ2L	DQ1L DQ1L	DQ1L DQ1L	DQ2L	DQ1L	DQ1L	Adj. Adj.
B1	VREFB1N1		DIFFIO_L9II DIFFIO_L10p	FLASH_nCE, nCSO	14	E2	E2	E2				DQZL	DQTL	DQTL				Adj.
B1	VREFB1N1		DIFFIO_L10p	FLASH_IICE, IICSO	14	E1	E1	J6		DQ1L	DQ1L		DQ1L	DQ1L				Adj.
B1	VREFB1N1		DIFFIO_L11p					E1		DQTE	DQTE		DQTE	DQIL		DQ1L	DQ1L	Adj.
B1	VREFB1N1		DIFFIO L11n					J7								54.2	54.2	Adj.
B1	VREFB1N1		DIFFIO_L12p				F2	F2				DM2L	DM1L0/BWS#1L0	DM1L0/BWS#1L0	DM2L	DM1L0/BWS#1L0	DM1L0/BWS#1L0	
B1	VREFB1N1		DIFFIO_L12n				F1	F1				DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	Sep.
B1	VREFB1N1	Ю	DIFFIO_L13p					K4										Adj.
B1	VREFB1N1		DIFFIO_L13n					K3										Adj.
B1	VREFB1N1		DIFFIO_L14p				H8	K7										Adj.
B1	VREFB1N1		DIFFIO_L14n				J8	L6										Adj.
B1	VREFB1N1		DIFFIO_L15p					L8										Adj.
B1	VREFB1N2		DIFFIO_L15n					L7										Adj.
B1	VREFB1N2		DIFFIO_L16p				1	M8	1									Adj.
B1 B1	VREFB1N2 VREFB1N2		DIFFIO_L16n		15		1	M7	-				_					Adj.
<u>В1</u>		IO	DIFFIO_L17p		15		1	L4										Sep.
B1	VREFB1N2		DIFFIO_L17p		16		1	L4										зер.
B1		IO	DIFFIO_L17n	<u> </u>	10		1	L3	<b>†</b>	1		<u> </u>	<del>                                     </del>		1	1	1	Sep.
B1		10	DIFFIO_L18p	1			<b>†</b>	H6	1	1	1	1	1		1		1	Adj.
B1	VREFB1N2		DIFFIO_L18n				J5	H5		ĺ						İ	İ	Adj.
B1	VREFB1N2		DIFFIO_L19p					J4		1	<u> </u>				<u> </u>		1	Adj.
B1	VREFB1N2	Ю	DIFFIO_L19n					J3							DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N2			nSTATUS	17	G5	K6	M6										
B1	VREFB1N2		VREFB1N2		18	H6	H5	N8										
B1	VREFB1N2			ļ	19		ļ	ļ	ļ	ļ	ļ	1	<del>                                     </del>		ļ	ļ	ļ	<u> </u>
B1	VREFB1N2		DIFFIO_L20p		<u> </u>	G2	L8	G2		DQ1L	DQ1L				DQ0L	DQ1L	DQ1L	Sep.
B1	VREFB1N2			<b></b>	20		<u> </u>	<u> </u>	ļ	L	L	+	+		<b> </b>	ļ	ļ	<del>_</del>
B1	VREFB1N2		DIFFIO_L20n	1	<u> </u>	G1	K8	G1	1	DQ1L	DQ1L	+	+		1	1	1	Sep.
B1	VREFB1N2		DIFFIO_L21p	<del> </del>	-	-	J7	M3	<del>                                     </del>	1	<del>                                     </del>	+	+	-	DON	DOM	DOM	Adj.
B1	VREFB1N2		DIFFIO_L21n DIFFIO_L22p	-	<u> </u>	1	K7	K1	-	-	-	+	+	-	DQ0L	DQ1L	DQ1L	Adj.
B1 B1	VREFB1N2 VREFB1N2		DIFFIO_L22p DIFFIO_L22n	1			<del>                                     </del>	N4 N3	<del>                                     </del>	1	<del> </del>	+	+	1	1	1	1	Adj. Adj.
вт В1	VREFB1N2 VREFB1N3		DIFFIO_LZZII	<del> </del>	<del>                                     </del>		<del>                                     </del>	M4	<del>                                     </del>	<del> </del>	<del>                                     </del>	+	1		<del> </del>	1	1	Auj.
	.11.61.01143			<u> </u>			1	101-7	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	DQS0L/CQ1L,	<b>†</b>
B1	VREFB1N3	Ю		1	21	H2	J4	K2	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	DPCLK0	



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Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18	DQS for X32/X36	res (2), (3)
Number		Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	in F780	in F780	NOTES
			(0)															(4), (5), (6)
																		( ), (-), (-)
	VDEED 4110		DIEEIO LOO		-	ļ						500	2011	2011				+
B1	VREFB1N3		DIFFIO_L23p				H2	L2				DQ0L	DQ1L	DQ1L				Adj.
B1	VREFB1N3	10	DIFFIO_L23n			1	H1	L1				DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N3	10	VREFB1N3		22	H1	J3	M5									ļ	<del></del>
B1	VREFB1N3	10	DIFFIO_L24p				J2	M2				DQ0L	DQ1L	DQ1L				Adj.
B1	VREFB1N3	Ю	DIFFIO_L24n				J1	M1				DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N3	10	DIFFIO_L25p					P2										Adj.
B1	VREFB1N3	10	DIFFIO_L25n					P1							DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N3		_	DCLK	23	H4	K2	P3									1	1
B1	VREFB1N3	10		DATA0	24	НЗ	K1	N7									1	1
B1	VREFB1N3			nCONFIG	25		K5	P4										+
B1	VREFB1N3			TDI	26	J6	L5	P7										1
D1	VREFB1N3	TCK		TCK	27	J1	L2	P5									<del>                                     </del>	+
D1																	<del>                                     </del>	+
B1	VREFB1N3	TMS		TMS	28	J2	L1	P8									ļ	<del></del>
B1	VREFB1N3	TDO		TDO	29	J5	L4	P6									<b>↓</b>	
B1	VREFB1N3	nCE		nCE	30	K6	L3	R8										
B1	VREFB1N3	CLK0	DIFFCLK_0p		31	F2	G2	J2										
B1	VREFB1N3	CLK1	DIFFCLK_0n		32	F1	G1	J1										
B2	VREFB2N0	CLK2	DIFFCLK_1p		33	N2	T2	Y2										
B2	VREFB2N0	CLK3	DIFFCLK_1n		34	N1	T1	Y1										1
B2	VREFB2N0	IO	DIFFIO_L26p		T .	K2	L6	R2		DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	Sep.
B2	VREFB2N0	VCCIO2	5.1 1 10_L20p		35	114		1.72		D-04.1L		2 40L	241L		S SKOL		DAIL	Эср.
B2			DIEEIO 1 20°		30	V 1	M6	R1	-	DO1	DO1	DON	DO11	DO1	-	DO1	DOU	Con
	VREFB2N0		DIFFIO_L26n		00	K1	IVIO	rx i	-	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	-	DQ1L	DQ1L	Sep.
B2	VREFB2N0				36	1		ļ									ļ	
B2	VREFB2N0	10	DIFFIO_L27p				M2	U3				DQ0L	DQ1L	DQ1L	DM0L	DM1L1/BWS#1L1	DM1L1/BWS#1L1	
B2	VREFB2N0	10	DIFFIO_L27n				M1	U2					DQ1L	DQ1L				Adj.
B2	VREFB2N0	10	DIFFIO_L28p		37	K5	M4	R3	DQ1L	DQ1L	DQ1L	DM0L	DM1L1/BWS#1L1	DM1L1/BWS#1L1	DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0	10	DIFFIO_L28n		38	L5	M3	R6	DQ1L	DM1L/BWS#1L	DM1L0/BWS#1L0	DQ1L	DQ3L	DQ1L				Adj.
B2	VREFB2N0	IO	DIFFIO_L29p				N2	R4				DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0	10	DIFFIO_L29n				N1	R7				DQ1L	DQ3L	DQ1L				Adj.
B2	VREFB2N0	10	DIFFIO L30p		1			T4				54.2	5 402	DQIL	DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0	10	DIFFIO L30n		1		17	T3							DQTL	DQJL	DQTL	Adj.
		-			00												<del> </del>	Auj.
B2	VREFB2N0	10	VREFB2N0		39	L6	M5	T8									<b>↓</b>	
B2	VREFB2N0	10	DIFFIO_L31p					U4									ļ	Adj.
B2	VREFB2N0	10	DIFFIO_L31n					R5							DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0	VCCINT			40													
B2	VREFB2N0	10	DIFFIO_L32p		41	L2	P2	U1	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	Sep.
B2	VREFB2N0	GND			42													
B2	VREFB2N0	IO	DIFFIO_L32n			L1	P1	V4		DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	Sep.
B2	VREFB2N0	IO.	DIFFIO_L33p			14	R2	V3		DQ3L	DQ1L	DQ1L	DQ3L	DQ1L				Adj.
B2	VREFB2N0	10	DIFFIO_L33n		43	1.3	R1	V2	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0 VREFB2N1	.0	DIFFIO_E33II		43	LJ	N5	V2 V9	DQTL	DQ3L	DQTL	DQ1L	DQ3L DQ3L	DQ1L DQ1L	DQTL	DQ3L	DQTL	Auj.
DZ.	VREFBZINI	10			1	1	CVI	V9									<del> </del>	+
		l						1	DQS1L/CQ1L#,	DQS1L/CQ1L#,	DQS1L/CQ1L#,	DQS1L/CQ1L#,	DQS1L/CQ1L#,	DQS1L/CQ1L#,	DQS1L/CQ1L#,	DQS1L/CQ1L#,	DQS1L/CQ1L#,	
B2	VREFB2N1		DIFFIO_L34p		44	M2	P4	AB2	DPCLK1	DPCLK1	DPCLK1	DPCLK1	DPCLK1	DPCLK1	DPCLK1	DPCLK1	DPCLK1	Adj.
B2	VREFB2N1		DIFFIO_L34n		45	M1	P3	AB1	DQ1L			DQ1L	DQ3L	DQ1L			ļ	Adj.
B2	VREFB2N1				1		<u> </u>	V1							DQ1L	DQ3L	DQ1L	<u> </u>
B2	VREFB2N1	Ю	DIFFIO_L35p		<u> </u>	L	U2	W2		L	L	DM1L/BWS#1L	DM3L0/BWS#3L0	DM1L2/BWS#1L2	DQ1L	DQ3L	DQ1L	Sep.
B2	VREFB2N1	10	DIFFIO_L35n				U1	W1				DQ3L	DQ3L	DQ1L	DM1L/BWS#1L	DM3L0/BWS#3L0	DM1L2/BWS#1L2	
B2	VREFB2N1	Ю	DIFFIO_L36p					W3										Adj.
B2	VREFB2N1	10	DIFFIO_L36n				1	W4										Adj.
B2	VREFB2N1	10	DIFFIO L37p		1		1	V6	1			1	1		1	1	<del>                                     </del>	Adj.
D2 D2	VREFB2N1 VREFB2N1	10	DIFFIO_L37p		1		1	U5	-	-		-	<del> </del>	1	-	1	+	Adj.
D2		-		-	1	<u> </u>	1/0		-			DON	DON	DOM	-		<del> </del>	
B2	VREFB2N1	10	DIFFIO_L38p		1		V2	Y5	1			DQ3L	DQ3L	DQ1L	1	1	<del></del>	Adj.
B2	VREFB2N1		DIFFIO_L38n		1	<u> </u>	V1	Y6				DQ3L	DQ3L	DQ1L				Adj.
B2	VREFB2N1	Ю	DIFFIO_L39p					V5									<b></b>	Adj.
B2	VREFB2N1	IO	DIFFIO_L39n					U6							DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N1	Ю	DIFFIO_L40p		$\perp$			AA7										Adj.
B2	VREFB2N1	Ю	DIFFIO L40n					AA6										Adj.
B2	VREFB2N1	10	VREFB2N1	Ì	46	МЗ	P5	T7			İ						1	1
B2	VREFB2N1	10	DIFFIO_L41p		1	IVIO	N6	AA8				DQ3L	DQ3L	DQ1L				Adj.
				1	1	1		Y7				DUSL	DUJJL	DQTL	1		<del>                                     </del>	
B2	VREFB2N1		DIFFIO_L41n			1	M7	Y /	1	-		1	1		1	<b> </b>	<del></del>	Adj.
B2	VREFB2N1		<u> </u>		47		<u> </u>	L	1			1	1		L		<del></del>	<del> </del>
B2	VREFB2N1		DIFFIO_L42p				M8	Y4					ļ	ļ	DQ3L	DQ3L	DQ1L	Sep.
Inc	VREFB2N1				48		<u> </u>											
B2			DIEELO LAO			1	N8	Y3		I	I	1	1	1	1			Sep.
B2 B2	VREFB2N2	10	DIFFIO_L42n	<u> </u>														оор.
B2 B2 B2	VREFB2N2 VREFB2N2	10 10	DIFFIO_L42n DIFFIO_L43p				110	T9										Adj.



Bank		Pin Name /	Optional	Configuration	Q240	F324	F484 /					DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in		DQS for X16/X18	DQS for X32/X36	PKG
Number	Group	Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	in F780	in F780	NOTES (4), (5), (6)
																		(4), (3), (0)
B2	VREFB2N2	10	DIFFIO_L44p		49	P2	W2	W8	DQ1L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L				Adj.
B2		10	DIFFIO_L44n			P1	W1	AC1	54.2	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N2	IO	DIFFIO L45p			R2	Y2	V7		DQ3L	DQ1L	DQ3L	DQ3L	DQ1L				Adj.
B2	VREFB2N2	10	DIFFIO_L45n				Y1	AC3				DQ3L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N2	10	DIFFIO_L46p					AD2							DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N2	10	DIFFIO_L46n					AD1										Adj.
B2	VREFB2N2	10	DIFFIO_L47p					AB3							DQ3L	DQ3L	DQ1L	Sep.
B2		10	DIFFIO_L47n			<u> </u>		AA4							DQ3L	DQ3L	DQ1L	Sep.
B2		10	DIEELO I 40			-		W9										<del> </del>
B2		10	DIFFIO_L48p					AB7					-				-	Adj.
B2 B2	VREFB2N2 VREFB2N2	10	DIFFIO_L48n VREFB2N2		50	R1	Т3	AC7 V8										Adj.
B2	VREFB2N2 VREFB2N2	10	DIFFIO L49p		50	KI	N7	Vo AE1										Adj.
B2		IO	DIFFIO_L49n				P7	AE2							DQ3L	DQ3L	DQ1L	Adj.
B2		10	DIFFIO_L50p				AA2	AA5							DOOL	DQUL	DQTE	Adj.
B2	VREFB2N2	10	DIFFIO_L50n				AA1	AF2				DQ3L	DQ3L	DQ1L	DM3L/BWS#3L	DM3L1/BWS#3L1	DM1L3/BWS#1L3	
B2	VREFB2N3	10	DIFFIO_L51p					AB6										Adj.
B2	VREFB2N3	10	DIFFIO_L51n					AB5										Adj.
B2	VREFB2N3							AA3										1
B2	VREFB2N3		RUP1		51	T2	V4	U7	DQ1L				ļ	1		1	ļ	<b></b>
B2		10	RDN1		52	T1	V3	U8	DQ1L					ļ		ļ		<u> </u>
B2			DIFFIO_L52p		-	Т3	P6	AC4		DQ3L	DQ1L							Sep.
B2 B2		VCCINT	DIFFIO LEO-		53	R3		400		DON	DO41		-				-	0
B2 B2	VREFB2N3 VREFB2N3	.0	DIFFIO_L52n		54	R3		AD3		DQ3L	DQ1L							Sep.
B2	VREFB2N3 VREFB2N3	GND			54		T5	AD4				DM3L/BWS#3L	DM3L1/BWS#3L1	DM1L3/BWS#1L3				+
D2	VICEI DZING	10					13	AD4	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	DQS3L/CQ3L#,	+
B2	VREFB2N3	10			55	M5	T4	AE3	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	CDPCLK1	
B2	VREFB2N3	IO	VREFB2N3		56	R5	R5	AB4										
B2	VREFB2N3				57	R4	R6	AB8	DQ1L	DM3L/BWS#3L	DM1L1/BWS#1L1							
B2	VREFB2N3	10	DIFFIO_L53p				R7	AC5										Adj.
B2		10	DIFFIO_L53n				T7	AD5										Adj.
B2	VREFB2N3		DIFFIO_L54p			-		AE4										Adj.
B2		10	DIFFIO_L54n		-	<u> </u>		AF3										Adj.
B2	VREFB2N3				58	N5	T6	Y8					-				-	
B2 B2	VREFB2N3 VREFB2N3				59 60	P5 P4	U5 U6	AA9 Y9										+
B3	VREFB3N3				61	P4	06	19										+
B3	VREFB3N3		DIFFIO_B1p		0.	U1	V6	AC11										Res.
B3	VREFB3N3		51.10_5.p		62			7.011										1100.
В3	VREFB3N3		DIFFIO_B1n			V1	V5	AD11				DM3B/BWS#3B	DM3B1/BWS#3B1	DM5B3/BWS#5B3				Res.
B3	VREFB3N3	Ю	DIFFIO_B2p					AD12										Res.
B3		Ю	DIFFIO_B2n					AE6							DM1B			Res.
B3	VREFB3N3	10	DIFFIO_B3p				U7	AF4							DQ1B			Res.
B3	VREFB3N3	10	DIFFIO_B3n		<u> </u>	<u> </u>	U8	AB12						ļ		ļ		Res.
B3		10	VREFB3N3		63	T4	Y4	Y10				DOOD	DOOD	DOED	1	1	<del>                                     </del>	Des
B3 B3	VREFB3N3 VREFB3N3	IO VCCINIT	DIFFIO_B4p		64	1	Y3	AG4				DQ3B	DQ3B	DQ5B	1	<del>                                     </del>	<b>_</b>	Res.
B3	VREFB3N3 VREFB3N3		DIFFIO_B4n		04	1	1	AG3					<del> </del>	+	DQ1B	+	<del> </del>	Res.
B3		GND	DII I'IO_D4II		65	1	1	703							ם עום			1169.
B3		IO	DIFFIO_B5p		50	<b>1</b>	<b>†</b>	AE7					1	1		1	1	Res.
B3	VREFB3N3				66		1	† <del></del>				İ	İ				İ	1
B3		10	DIFFIO_B5n					AE8										Res.
B3	VREFB3N3	GND			67													
								1		DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	DQS1B/CQ1B#,	
B3	VREFB3N3	10	DIFFIO_B6p		68	P6	Y6	AD7	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	CDPCLK2	Res.
B3	VREFB3N3	10	DIFFIO_B6n		60	112	440	Y12					-	<del>                                     </del>	1	<del>                                     </del>	<b>_</b>	Res.
B3 B3	TITLE BOILE	10	PLL1_CLKOUTp PLL1_CLKOUTn		69 70	U2 V2	AA3 AB3	AE5 AF5	<b> </b>				-	1	1	1	-	+
B3	VREFB3N2 VREFB3N2		DIFFIO_B7p		70	٧∠	W6	AH3				DQ3B	DQ3B	DQ5B	DQ1B	+	<del> </del>	Res.
B3	VREFB3N2 VREFB3N2		DIFFIO_B/P		71	<del>                                     </del>	VVO	AHS				D C O D	מעאם	סמאס	ם עום	1	<del>                                     </del>	1165.
B3	VREFB3N2		DIFFIO_B7n		ř -	1	V7	W10										Res.
B3	VREFB3N2		0_5///		72	1	i i	1					1				1	150.
B3		10				<u> </u>	AA4	AF6				DQ3B	DQ3B	DQ5B	DQ1B			1
B3		10	VREFB3N2		73	T6	AB4	AA12										
B3	VREFB3N2	10	DIFFIO_B8p				AA5	AC12				DQ3B	DQ3B	DQ5B				Res.



Function	DIFFIO_B8n DIFFIO_B9p DIFFIO_B9n DIFFIO_B10p DIFFIO_B11p DIFFIO_B11n DIFFIO_B11p DIFFIO_B12p DIFFIO_B12p DIFFIO_B13p DIFFIO_B13n DIFFIO_B14p DIFFIO_B14p DIFFIO_B15p DIFFIO_B15p DIFFIO_B15p DIFFIO_B15p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B18p DIFFIO_B18p	Configuration Function	74 75 76 77 78 79	P7 U3 U3 U4	U484  AB5  T8  T9  W7  Y7  U9  V8  W8  AA7  AB7  Y8  T110  T111  V9  V10	AH4 AC10 AD8 AG6 AB13 AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11		PQS3B/CQ3B#,	F324	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQS for X16/X18 in F484/U484  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B	DQ1B DQ1B DQ1B DQ1B		in F780	Res. Res. Res. Res. Res. Res. Res. Res.
N2   IO N1   IO N1   IO	DIFFIO B8n DIFFIO B9p DIFFIO B9n DIFFIO B10p DIFFIO B10n DIFFIO B11p DIFFIO B11p DIFFIO B11p DIFFIO B12p  DIFFIO B12p  DIFFIO B13n  DIFFIO B13n  DIFFIO B14p DIFFIO B14p DIFFIO B15p DIFFIO B15p DIFFIO B15p DIFFIO B16p DIFFIO B16p  DIFFIO B16p DIFFIO B16p DIFFIO B17p DIFFIO B17p DIFFIO B17p DIFFIO B17p DIFFIO B18p DIFFIO B18p		76 77 78	U3 V3	T8 T9 W7 V7 U9 V8 W8 AA7 AB7 Y8 T10 T11 V9	AC10 AD8 AG6 AB13 AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ1B DQ1B DQ1B DM3B/BWS#3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DM5B3/BWS#5B3 DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2   IO N1   IO N1   IO	DIFFIO_B9p DIFFIO_B9n DIFFIO_B9n DIFFIO_B10p DIFFIO_B10p DIFFIO_B11p DIFFIO_B11p DIFFIO_B12p DIFFIO_B12p DIFFIO_B13p DIFFIO_B13p DIFFIO_B13p DIFFIO_B14p DIFFIO_B14p DIFFIO_B15p DIFFIO_B15p DIFFIO_B15p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B18p DIFFIO_B18p		76 77 78	U3 V3	T8 T9 W7 Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AC10 AD8 AG6 AB13 AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ1B DQ1B DQ1B DM3B/BWS#3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DM5B3/BWS#5B3 DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2   IO N1   IO N1   IO	DIFFIO_B9p DIFFIO_B9n DIFFIO_B9n DIFFIO_B10p DIFFIO_B10p DIFFIO_B11p DIFFIO_B11p DIFFIO_B12p DIFFIO_B12p DIFFIO_B13p DIFFIO_B13p DIFFIO_B13p DIFFIO_B14p DIFFIO_B14p DIFFIO_B15p DIFFIO_B15p DIFFIO_B15p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B18p DIFFIO_B18p		76 77 78	U3 V3	T8 T9 W7 Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AC10 AD8 AG6 AB13 AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ1B DQ1B DQ1B DM3B/BWS#3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DM5B3/BWS#5B3 DQ5B DQ5B DQ5B DQ5B DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2   IO N1   IO N1   IO	DIFFIO_B9p DIFFIO_B9n DIFFIO_B9n DIFFIO_B10p DIFFIO_B10p DIFFIO_B11p DIFFIO_B11p DIFFIO_B12p DIFFIO_B12p DIFFIO_B13p DIFFIO_B13p DIFFIO_B13p DIFFIO_B14p DIFFIO_B14p DIFFIO_B15p DIFFIO_B15p DIFFIO_B15p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B18p DIFFIO_B18p		76 77 78	U3 V3	T8 T9 W7 Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AC10 AD8 AG6 AB13 AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ1B DQ1B DQ1B DM3B/BWS#3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DM5B3/BWS#5B3 DQ5B DQ5B DQ5B DQ5B DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2 IO N1 IO N1 IO	DIFFIO_B9n DIFFIO_B10p DIFFIO_B11p DIFFIO_B11p DIFFIO_B11p DIFFIO_B12p DIFFIO_B12p DIFFIO_B12n DIFFIO_B13p DIFFIO_B13n DIFFIO_B14p DIFFIO_B14p DIFFIO_B15p DIFFIO_B15p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B18p DIFFIO_B18p		76 77 78	U3 V3	T9 W7 Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AD8 AG6 AB13 AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ1B  DQ1B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DM5B3/BWS#5B3 DQ5B DQ5B DQ5B DQ5B DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N1 IO	DIFFIO_B10p DIFFIO_B10n DIFFIO_B10n DIFFIO_B11p DIFFIO_B11p DIFFIO_B12p  DIFFIO_B12p  DIFFIO_B13p DIFFIO_B13n  DIFFIO_B13n  DIFFIO_B14p DIFFIO_B14p DIFFIO_B15p DIFFIO_B15p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B16p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B18p DIFFIO_B18p		76 77 78	U3 V3	T9 W7 Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AG6 AB13 AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ1B  DQ1B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DM5B3/BWS#5B3 DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N2 VCCINT N2 IO N2 IO N2 IO N1 IO	DIFFIO B10n DIFFIO B11p DIFFIO B11p DIFFIO B11p DIFFIO B12p DIFFIO B12p DIFFIO B12p DIFFIO B13p DIFFIO B13p DIFFIO B13n DIFFIO B14p DIFFIO B14p DIFFIO B15p DIFFIO B15p DIFFIO B16p DIFFIO B16p DIFFIO B16p DIFFIO B17p DIFFIO B17p DIFFIO B17p DIFFIO B17p DIFFIO B18p DIFFIO B18p		76 77 78	U3 V3	T9 W7 Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AB13 AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ1B  DM3B/BWS#3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ5B  DQ5B  DQ5B  DQ5B  DQ5B  DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2 IO N2 IO N2 IO N2 IO N2 IO N2 VCCINT N2 IO N2 GND N2 IO N2 IO N2 IO N1 IO	DIFFIO B11p DIFFIO B11p DIFFIO B12n  DIFFIO B12n  DIFFIO B13p DIFFIO B13n  DIFFIO B14p DIFFIO B14p DIFFIO B15p DIFFIO B15p DIFFIO B16p  DIFFIO B16p  DIFFIO B16p  DIFFIO B17p DIFFIO B17p DIFFIO B17p DIFFIO B17p DIFFIO B18p DIFFIO B18p		76 77 78	U3 V3	T9 W7 Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AH6 AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DM3B/BWS#3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ5B  DQ5B  DQ5B  DQ5B  DQ5B  DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2 IO N2 IO N2 IO N2 VCCINT N2 IO N2 GND N2 GND N2 IO N2 IO N1 IO	DIFFIO_B11n DIFFIO_B12p  DIFFIO_B12p  DIFFIO_B13p DIFFIO_B13n  DIFFIO_B14p DIFFIO_B14n  DIFFIO_B15p DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B18p DIFFIO_B18p		76 77 78	U3 V3	T9 W7 Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AA13 AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DM3B/BWS#3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ5B  DQ5B  DQ5B  DQ5B  DQ5B  DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2 IO N2 VCCINT N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N1 IO	DIFFIO_B11n DIFFIO_B12p  DIFFIO_B12p  DIFFIO_B13p DIFFIO_B13n  DIFFIO_B14p DIFFIO_B14n  DIFFIO_B15p DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B17p DIFFIO_B18p DIFFIO_B18p		76 77 78	U3 V3	W7  Y7  U9  V8  W8  AA7  AB7  Y8  T10  T11  V9	AB9 AD10 AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ5B  DQ5B  DQ5B  DQ5B  DQ5B  DQ5B	Res. Res. Res. Res. Res. Res. Res. Res.
N2 IO N2 VCCINT N2 IO N2 IO N2 IO N2 IO N2 IO N2 IO N1 IO	DIFFIO_B12p  DIFFIO_B12n  DIFFIO_B13p  DIFFIO_B13n  DIFFIO_B14p  DIFFIO_B14p  DIFFIO_B15p  DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B17p  DIFFIO_B17p  DIFFIO_B17p  DIFFIO_B18p  DIFFIO_B18p  DIFFIO_B18p		76 77 78	U3 V3	Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AD10  AG7  Y13  AH7  AC8  AA10  Y14  AG8  Y15  AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ5B  DQ5B  DQ5B  DQ5B  DQ5B  DQ5B	Res. Res. Res. Res. Res. Res.
N2 VCCINT N2 IO N2 GND N2 IO N2 IO N2 IO N2 IO N1 IO	DIFFIO_B12n  DIFFIO_B13p  DIFFIO_B13n  DIFFIO_B14p  DIFFIO_B14n  DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B17p  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		76 77 78	U3 V3	Y7 U9 V8 W8 AA7 AB7 Y8 T10 T111 V9	AD10  AG7  Y13  AH7  AC8  AA10  Y14  AG8  Y15  AB11				DQ3B DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ3B  DQ3B  DQ3B  DQ3B  DQ3B	DQ5B  DQ5B  DQ5B  DQ5B  DQ5B  DQ5B	Res. Res. Res. Res. Res. Res.
N2   IO   N2   GND   N2   GND   N2   IO   N2   IO   N2   IO   N2   IO   N1	DIFFIO_B12n  DIFFIO_B13p  DIFFIO_B13n  DIFFIO_B14p  DIFFIO_B14n  DIFFIO_B15p  DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B17p  DIFFIO_B17p  DIFFIO_B17p  DIFFIO_B17p  DIFFIO_B18p  DIFFIO_B18p		76 77 78	U3 V3	U9 V8 W8 AA7 AB7 Y8 T10 T11	AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B DQ3B DQ3B	DQ3B DQ3B DQ3B DQ3B	DQ5B DQ5B DQ5B DQ5B	Res. Res. Res. Res. Res.
N2 GND N2 IO N2 IO N2 IO N2 IO N1 IO	DIFFIO_B13p DIFFIO_B13n  DIFFIO_B14p DIFFIO_B14n  DIFFIO_B15p DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B17p DIFFIO_B17n DIFFIO_B17n DIFFIO_B18p DIFFIO_B18n		76 77 78	U3 V3	U9 V8 W8 AA7 AB7 Y8 T10 T11	AG7 Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B DQ3B DQ3B	DQ3B DQ3B DQ3B DQ3B	DQ5B DQ5B DQ5B DQ5B	Res. Res. Res. Res. Res.
N2 IO N2 IO N2 IO N2 IO N1 IO	DIFFIO_B13n  DIFFIO_B14p  DIFFIO_B15p  DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16n  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		76 77 78	U3 V3	V8 W8 AA7 AB7 Y8 T10 T11 V9	Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B DQ3B	DQ3B DQ3B DQ3B	DQ5B DQ5B DQ5B	Res. Res. Res.
N2 IO N2 IO N2 IO N1 IO	DIFFIO_B13n  DIFFIO_B14p  DIFFIO_B15p  DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16n  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		77 78 79	U3 V3	V8 W8 AA7 AB7 Y8 T10 T11 V9	Y13 AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DQ3B DM5B/BWS#5B DQ5B	DQ3B DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DQ5B DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B DQ3B	DQ3B DQ3B DQ3B	DQ5B DQ5B DQ5B	Res. Res. Res.
N2 IO N1 IO	DIFFIO_B14p DIFFIO_B15p DIFFIO_B15n VREFB3N1  DIFFIO_B16p DIFFIO_B16n DIFFIO_B17p DIFFIO_B17p DIFFIO_B17n DIFFIO_B18p DIFFIO_B18n		77 78 79	U3 V3	W8 AA7 AB7 Y8 T10 T11 V9	AH7 AC8 AA10 Y14 AG8 Y15 AB11				DQ3B DM5B/BWS#5B DQ5B	DQ3B DM3B0/BWS#3B0 DQ3B	DQ5B DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B	DQ3B DQ3B	DQ5B DQ5B	Res. Res.
N1 IO N1 IO	DIFFIO_B14n  DIFFIO_B15p  DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16n  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		77 78 79	U3 V3	AA7 AB7 Y8 T10 T11 V9	AC8 AA10 Y14 AG8 Y15 AB11				DM5B/BWS#5B DQ5B	DM3B0/BWS#3B0 DQ3B	DM5B2/BWS#5B2 DQ5B	DQ3B DQ3B	DQ3B DQ3B	DQ5B DQ5B	Res.
N1 IO N1 IO	DIFFIO_B14n  DIFFIO_B15p  DIFFIO_B15n  VREFB3N1  DIFFIO_B16p  DIFFIO_B16n  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		77 78 79	U3 V3	AB7 Y8 T10 T11 V9	AA10 Y14 AG8 Y15 AB11				DQ5B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B	Res.
N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 VCCIO3 N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B15p DIFFIO_B15n VREFB3N1  DIFFIO_B16p  DIFFIO_B16n DIFFIO_B17p DIFFIO_B17n DIFFIO_B18p DIFFIO_B18n		77 78 79	U3 V3	Y8 T10 T11 V9	Y14 AG8 Y15 AB11										Res.
N1 IO N1 IO N1 IO N1 VCCIO3 N1 IO N1 GND N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B16n  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		77 78 79	U3 V3	T10 T11 V9	AG8 Y15 AB11				DQ5B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B	
N1 IO N1 IO N1 VCCIO3 N1 IO N1 GND N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B16n  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		77 78 79	U3 V3	T11 V9	Y15 AB11							DQ3B	DQ3B	DQ5B	
N1 IO N1 IO N1 VCCIO3 N1 IO N1 GND N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B16p  DIFFIO_B16p  DIFFIO_B16n  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		77 78 79	U3 V3	T11 V9	Y15 AB11										
N1 IO N1 VCCIO3 N1 IO N1 GND N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B16n DIFFIO_B17p DIFFIO_B17n DIFFIO_B18p DIFFIO_B18p DIFFIO_B18p		77 78 79	U3 V3	V9	AB11										
N1 VCCIO3  N1 IO  N1 GND  N1 IO  N1 IO  N1 IO  N1 IO  N1 IO  N1 IO  N1 IO  N1 IO  N1 IO	DIFFIO_B16n DIFFIO_B17p DIFFIO_B17n DIFFIO_B18p DIFFIO_B18p		77 78 79	U3 V3							1	<del>                                     </del>				
N1 IO N1 GND N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B16p  DIFFIO_B16n  DIFFIO_B17p  DIFFIO_B17n  DIFFIO_B18p  DIFFIO_B18p		78 79	V3	V10	AE10						1				1
N1 GND N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B16n DIFFIO_B17p DIFFIO_B17n DIFFIO_B18p DIFFIO_B18n		79	V3	V10	AE10			DOCOD/COOP#	DOC2D/0000#	DO03D/003D#	D063D/000D#	DOCAD/COAD/	DOCAD/COAD#	DOCAD/COAD#	+
N1 GND N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B16n DIFFIO_B17p DIFFIO_B17n DIFFIO_B18p DIFFIO_B18n		79	V3	VIU	AE 10	DICLINZ	DDCI K3	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,	DQS3B/CQ3B#,		DQS3B/CQ3B#,	Boo
N1 IO N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B17p DIFFIO_B17n DIFFIO_B18p DIFFIO_B18n				1		1	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2	DPCLK2	Res.
N1 IO N1 IO N1 IO N1 IO N1 IO	DIFFIO_B17p DIFFIO_B17n DIFFIO_B18p DIFFIO_B18n		00			1										
N1 IO N1 IO N1 IO N1 IO	DIFFIO_B17n DIFFIO_B18p DIFFIO_B18n		00	ш	1	AH8		DM3B/BWS#3B	DM5B1/BWS#5B1				DQ3B	DQ3B	DQ5B	Res.
N1 IO N1 IO N1 IO	DIFFIO_B18p DIFFIO_B18n		00			AF7		DQ3B	DQ5B				DQ3B	DQ3B	DQ5B	Res.
N1 IO N1 IO	DIFFIO_B18n		0U	V4	U10	AH10	DM5B/BWS#5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B				Res.
N1 IO N1 IO			81	U5	AA8	AF9	DQ5B			DQ5B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B	Res.
N1 IO		1	82	V5	AB8	AH12	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B				Res.
	DIFFIO_B19p					AF8							DM5B/BWS#5B	DM3B0/BWS#3B0	DM5R2/RWS#5R2	Res.
	DIFFIO_B19n					AF12							DIVIODIDIVO#OD	DIVIODO/DVVO#ODO	DIVIODE/DVVO#ODE	Res.
N1 IO	DIFFIO_B20p		-	<u> </u>		AE9						<u> </u>	DQ5B	DQ3B	DQ5B	Res.
				1									DQSB	DQ3B	DQSB	
N1 IO	DIFFIO_B20n			<u> </u>		AF13										Res.
N1 IO	DIFFIO_B21p			R8	AA9	AF10		DQ3B	DQ5B	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B	Res.
							DQS5B/CQ5B#,	DQS5B/CQ5B#,	DQS5B/CQ5B#,	DQS5B/CQ5B#,	DQS5B/CQ5B#,	DQS5B/CQ5B#,	DQS5B/CQ5B#,	DQS5B/CQ5B#,	DQS5B/CQ5B#,	
N1 IO			83				DPCLK3	DPCLK3	DPCLK3	DPCLK3	DPCLK3	DPCLK3	DPCLK3	DPCLK3	DPCLK3	Res.
N0 IO	VREFB3N0		84	P8	U11											
N0 IO	DIFFIO_B22p					AG10							DQ5B	DQ3B	DQ5B	Res.
N0 IO	DIFFIO B22n					AE12							DQ5B	DQ3B	DQ5B	Res.
																Res.
			85			<u> </u>										
			00	DΩ		AC11		DO3B	DOED				DOEB	DO3B	DOEB	Res.
	DII 1 10_D23II		96	1 3		AGTI		DQSB	DQSB			<u> </u>	DQSB	DQJD	DQJD	ixes.
	DIEEIO DOI		00					D.O.O.D.	noen.				D.O.E.D.	B 0 0 B	0.050	
												-	DQ5B	DQ3B		Res.
			-	νб	1		1	DQ3B	DM2R			1				Res.
				<u> </u>	ļ							<b>.</b>	DQ5B	DQ3B	DQ5B	Res.
				<u> </u>				ļ					ļ			Res.
N0 IO	DIFFIO_B26p										DQ3B	DQ5B	DQ5B	DQ3B	DQ5B	Res.
N0 IO	DIFFIO_B26n				Y10	AD14		DQ3B	DQ5B	DQ5B	DQ3B	DQ5B				Res.
N0 IO	DIFFIO_B27p		87	U8	AA10	AE14	DQ5B	DQ3B	DQ5B	DM4B	DM5B1/BWS#5B1	DM5B1/BWS#5B1				Res.
N0 IO			88	V8	AB10	AF14	DQ5B				DQ5B					Res.
								1				1	İ			
												<b>†</b>		1		<del>                                     </del>
							1	1				<del> </del>	1	1		-
							-					<b>_</b>		-		+
													l			ᡶ
N3 IO			93					DQ5B	DQ5B							Res.
N3 IO			94				DQ5B	ļ					DM4B	DM5B1/BWS#5B1	DM5B1/BWS#5B1	Res.
N3 IO	DIFFIO_B29p			U12	AA14	AD15		DQ5B	DQ5B	DQ4B	DQ5B	DQ5B				Res.
N3 IO	DIFFIO_B29n				AB14	AE15				DQ4B	DQ5B	DQ5B		DQ5B	DQ5B	Res.
N3 IO						AA16										
N3 IO	VREFB4N3		95	V12	V12			İ			İ	İ	İ			1
				<u> </u>	1		1	1				†	DO4B	DO5B	DO5B	Res.
			96	<del>                                     </del>	<del>                                     </del>	711 10		<del> </del>				<del>                                     </del>	DQ-10	D 400	D 04 0 D	1100.
			30	<u> </u>	<del>                                     </del>	1017	-					<b>_</b>	DO 4B	DOED	DOED	Dee
	DIFFIO_B30n			<b>├</b>	1	AG1/	1	1				1	DQ4B	D/Q2R	DG2R	Res.
NR KAND	1	1	97	<b>-</b>	<u> </u>	1						L				Res.
	10	10   IO   VREFB3NO     10   IO   DIFFIO B22p     10   IO   DIFFIO B22p     10   IO   DIFFIO B22p     10   IO   DIFFIO B23n     10   IO   DIFFIO B23n     10   IO   DIFFIO B23n     10   IO   DIFFIO B23n     10   IO   DIFFIO B24p     10   IO   DIFFIO B24p     10   IO   DIFFIO B25n     10   IO   DIFFIO B25n     10   IO   DIFFIO B25n     10   IO   DIFFIO B25n     10   IO   DIFFIO B25n     10   IO   DIFFIO B25n     10   DIFFIO B25n     10   DIFFIO B25n     10   DIFFIO B25n     10   DIFFIO B25n     10   DIFFIO B27n     10   CLK15   DIFFCLK 6p     11   DIFFIO B25n     12   DIFFIO B25n     13   CLK12   DIFFCLK 7p     13   IO   DIFFIO B25n     14   DIFFIO B25n     15   DIFFIO B25n     16   DIFFIO B25n     17   DIFFIO B25n     18   IO   DIFFIO B25n     19   DIFFIO B25n     10   DIFFIO B25n     11   DIFFIO B25n     12   DIFFIO B25n     13   IO   DIFFIO B30n     14   IO   DIFFIO B30n     15   DIFFIO B30n     16   DIFFIO B30n     17   DIFFIO B30n     18   DIFFIO B30n     10   DIFFIO B30n     1	10	10   IO	10   IO	10   IO	10   IO	11   O	11   IO	11   O	11   O	11   O	11   O	11   O	11   O	11   DO   DIFFIO B216   83   T8   A89   AF11   DPCLK3



B4         VRE           B4         VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB		Function(s)  DIFFIO_B31n DIFFIO_B32p DIFFIO_B32p DIFFIO_B33p DIFFIO_B33p DIFFIO_B34p DIFFIO_B34n DIFFIO_B34n DIFFIO_B35p DIFFIO_B35p DIFFIO_B35p DIFFIO_B35n	Function	98 99 100 101 102 103 104	P11 U14 V14 U15	W13 Y13 AA15 AB15 U12 AA16 AB16	W16 AF16 AF17 AB16 AE16 AE17 AG18	DQ5B DQ5BBCQ5B, DPCLK4 DQ5B	DQ5B DQ5B/DQ54B/CQ5B, DPCLK4 DQ5B DQ5B DQ5B	DQ5B DQ54B/CQ5B, DPCLK4 DQ5B DQ5B	DQ4B DQ4B DQ5B/CQ5B, DPCLK4 DQ4B DQ4B DQ4B	DQS for X16/X18 in F484/U484  DQ5B  DQS4B/CQ5B, DPCLK4  DQ5B  DQ5B  DQ5B	P484/U484  DQ5B  DQ5B/PCLK4  DQ5B  DQ5B  DQ5B  DQ5B	DQ4B DQ54B/CQ5B, DPCLK4 DQ4B DQ4B	DQ5B DQ54B/CQ5B, DPCLK4 DQ5B DQ5B	DQ5B DQ54B/CQ5B, DPCLK4 DQ5B DQ5B	NOTES (4), (5), (6) Res. Res. Res. Res. Res.
B4         VRE           B4         VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB	IO IO IO IO IO IO IO VCCINT IO GND IO VCCIO4 IO IO IO IO IO IO IO IO IO IO IO IO IO	DIFFIO_B32p DIFFIO_B32n DIFFIO_B33p DIFFIO_B33n DIFFIO_B34p DIFFIO_B34n DIFFIO_B35p DIFFIO_B35p DIFFIO_B35n DIFFIO_B35n		99 100 101 102 103 104	V13 P10 P11 U14 V14 U15	Y13 AA15 AB15 U12	AF16 AF17 AB16 AE16 AE17 AG18 AH18	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ4B DQ4B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ4B	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B	Res. Res. Res. Res. Res. Res.
B4         VRE           B4         VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB	IO IO IO IO IO IO IO VCCINT IO GND IO VCCIO4 IO IO IO IO IO IO IO IO IO IO IO IO IO	DIFFIO_B32p DIFFIO_B32n DIFFIO_B33p DIFFIO_B33n DIFFIO_B34p DIFFIO_B34n DIFFIO_B35p DIFFIO_B35p DIFFIO_B35n DIFFIO_B35n		99 100 101 102 103 104	V13 P10 P11 U14 V14 U15	Y13 AA15 AB15 U12	AF16 AF17 AB16 AE16 AE17 AG18 AH18	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ4B DQ4B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ4B	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B	Res. Res. Res.
B4         VRE           B4         VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB	IO IO IO IO IO IO IO VCCINT IO GND IO VCCIO4 IO IO IO IO IO IO IO IO IO IO IO IO IO	DIFFIO_B32p DIFFIO_B32n DIFFIO_B33p DIFFIO_B33n DIFFIO_B34p DIFFIO_B34n DIFFIO_B35p DIFFIO_B35p DIFFIO_B35n DIFFIO_B35n		99 100 101 102 103 104	V13 P10 P11 U14 V14 U15	Y13 AA15 AB15 U12	AF16 AF17 AB16 AE16 AE17 AG18 AH18	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ4B DQ4B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ4B	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B	Res. Res. Res.
B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB	IO IO IO IO VCCINT IO GND IO VCCIO4 IO GND IO IO IO IO IO IO IO IO IO IO IO IO IO	DIFFIO_B32n DIFFIO_B33p DIFFIO_B33n DIFFIO_B34p DIFFIO_B34n DIFFIO_B35p DIFFIO_B35p DIFFIO_B35p DIFFIO_B35p		99 100 101 102 103 104	V13 P10 P11 U14 V14 U15	Y13 AA15 AB15 U12	AF17 AB16 AE16 AE17 AG18	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ4B DQ4B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B DQ5B	DQS4B/CQ5B, DPCLK4 DQ4B	DQS4B/CQ5B, DPCLK4 DQ5B	DQS4B/CQ5B, DPCLK4 DQ5B	Res. Res.
B4         VRE           B4         VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB4N3   EFB	IO IO IO IO IO IO IO IO IO IO IO IO IO I	DIFFIO_B33p DIFFIO_B33n DIFFIO_B34p DIFFIO_B34n DIFFIO_B35p DIFFIO_B35n DIFFIO_B35n		100 101 102 103 104	P10 P11 U14 V14 U15	AA15 AB15 U12 AA16	AB16 AE16 AE17 AG18 AH18	DQ5B	DQ5B DQ5B	DQ5B	DQ4B DQ4B	DQ5B DQ5B	DQ5B DQ5B	DQ4B	DQ5B	DQ5B	Res. Res.
B4         VRE           B4         VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB	IO IO IO VCCINT IO GND IO VCCIO4 IO GND IO IO IO IO IO IO IO IO IO IO IO IO IO	DIFFIO_B33n DIFFIO_B34p DIFFIO_B34n DIFFIO_B35p DIFFIO_B35n DIFFIO_B36p		101 102 103 104	P11 U14 V14 U15	AB15 U12 AA16	AE16 AE17 AG18 AH18		DQ5B	DQ5B	DQ4B	DQ5B	DQ5B				Res.
B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE B4 VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB4N3   EFB	VCCINT IO GND IO VCCIO4 IO GND IO IO IO IO IO IO IO IO IO IO IO IO IO	DIFFIO_B34p  DIFFIO_B35p  DIFFIO_B35n  DIFFIO_B36p		101 102 103 104	U14 V14 U15	U12 AA16	AE17 AG18 AH18							DQ4B	DQ5B	DQ5B	
B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE	EFB4N3   EFB4N3   EFB4N3   EFB4N2   EFB	VCCINT IO GND IO VCCIO4 IO GND IO IO IO IO IO IO IO IO IO IO IO IO IO	DIFFIO_B35p  DIFFIO_B35n  DIFFIO_B36p		101 102 103 104	V14 U15	AA16	AG18 AH18				DQ4B	DG9B	DQ5B	DQ4B	DG9R	DQ5B	Res.
B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE	EFB4N3   I   EFB4N2	IO GND IO VCCIO4 IO GND IO	DIFFIO_B35p DIFFIO_B35n DIFFIO_B36p		102 103 104	U15		AH18	DQ5B	DQ5B	DQ5B							
B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE	EFB4N3 ( EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2   EFB4N2	GND IO VCCIO4 IO GND IO IO	DIFFIO_B35p DIFFIO_B35n DIFFIO_B36p		103 104	U15		AH18	DQ5B						DQ4B	DQ5B	DQ5B	Res.
B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE	EFB4N2   EFB	VCCIO4 IO GND IO	DIFFIO_B35n DIFFIO_B36p		104				DQ5B						54.5	2402	5405	1100.
B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE	EFB4N2   EFB	IO GND IO IO	DIFFIO_B36p			V15	AB16		1			DM2B	DM5B0/BWS#5B0	DM5B0/BWS#5B0	DQ4B	DQ5B	DQ5B	Res.
B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE           B4         VRE	EFB4N2   EFB	GND IO IO	DIFFIO_B36p		105	V15	AB16		<b></b>									
<ul><li>B4 VRE</li><li>B4 VRE</li><li>B4 VRE</li><li>B4 VRE</li></ul>	EFB4N2   I EFB4N2   I EFB4N2   I EFB4N2   I EFB4N2   I	10 10			105			AH19		DQ5B	DQ5B	DQ2B	DQ5B	DQ5B	DM2B	DM5B0/BWS#5B0	DM5B0/BWS#5B0	Res.
B4 VRE B4 VRE B4 VRE	EFB4N2 I EFB4N2 I EFB4N2 I EFB4N2 I EFB4N2 I	10			1		T12	AD17				<del>                                     </del>			DOOD	DOED	DOED	Res.
B4 VRE	EFB4N2 I EFB4N2 I EFB4N2 I EFB4N2 I	10	DII 1 10_DOOII			R11	T13	AF18		DQ5B	DQ5B	1			DQ2B	DQ5B	DQ5B	Res.
B4 VRE	EFB4N2 I EFB4N2 I EFB4N2 I					1111	110	711 10	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	DQS2B/CQ3B,	1103.
	EFB4N2 I	10			106	P12	V13	AE18	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	DPCLK5	
B4 VRE	EFB4N2	10	VREFB4N2		107	T11	W14	Y17										
		10	DIFFIO_B37p	ļ	<b> </b>	1		AG21		ļ		<b>_</b>	ļ	ļ	DQ2B	DQ5B	DQ5B	Res.
		10	DIFFIO_B37n DIFFIO_B38p					AC17 AH21				<del>                                     </del>			DOOD	DQ5B	DOED	Res.
	EFB4N2 I	.0	DIFFIO_B38p		+		U13	AG22							DQ2B DQ2B	DQ5B DQ5B	DQ5B DQ5B	Res.
		10	DIFFIO_B39p				V14	AH22				DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B	Res.
		10	DIFFIO_B39n				U14	AG19										Res.
B4 VRE	EFB4N2	10	DIFFIO_B40p				U15	AH23							DQ2B	DQ5B	DQ5B	Res.
		VCCINT			108													
		10	DIFFIO_B40n				V15	AE19				DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B	Res.
		GND	DIEEIO DAA-		109			4504				1			DOOD	DOED	DOED	Dec
		10 10	DIFFIO_B41p DIFFIO_B41n		+		W15	AF24 AF19				DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B	Res.
		10	DIFFIO_B411				T14	AF25				DQZD	DQUB	DQSB	DM0B	DQ5B	DQ5B	Res.
		10	DIFFIO_B42n				T15	AF20				DQ2B	DQ5B	DQ5B	DQ0B	2402	5 405	Res.
B4 VRE	EFB4N1	10					AB18	AD18				DQ2B	DQ5B	DQ5B	DQ0B			1
		10	DIFFIO_B43p				AA17	Y19										Res.
		10	DIFFIO_B43n				AB17	AE21				<b>.</b>			DQ0B			Res.
		10	VREFB4N1		110	U16	AA18	AC18										
	EFB4N1 I	IO	DIFFIO_B44p DIFFIO_B44n			V16		AB18 AA19		DQ5B	DQ5B							Res.
	EFB4N1 I	.0	DIFFIO_B44II			V 10		AD19		DQSB	DQSB							Res.
		10	DIFFIO_B45n					AE20										Res.
		10	DIFFIO_B46p					AC19										Res.
		10	DIFFIO_B46n					AB19										Res.
	_, _ ,, ,	10	RUP2		111		AA19	AA17										_
	EFB4N1	10	RDN2		112	T14	AB19	AB17				1						4
	EFB4N1 I	10	DIFFIO_B47p	1	1	U17		AD21 AF21	<del> </del>		1	1	1	1	1	1		Res.
		10	DIFFIO_B47p	<del> </del>	1	V17	1	AE25	<b> </b>	<del> </del>	<b> </b>	<del>                                     </del>	1	<del> </del>	DQ0B			Res.
		10	DIFFIO_B48p			,	W17	AC21				DQ2B	DQ5B	DQ5B	5405			Res.
									DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	DQS0B/CQ1B,	1
	EFB4N0 I	10	DIFFIO_B48n	ļ	113	R13	Y17	AF26	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	CDPCLK3	Res.
	EFB4N0 I	10	DIFFIO_B49p	1	<del> </del>	<u> </u>	AA20	AG25	<del>                                     </del>	1	<del>                                     </del>	DOSB	DQ5B	DQ5B	DOOD	<del>                                     </del>		Res.
	EFB4N0 I	10	DIFFIO_B49n VREFB4N0	1	114	P13	AB20 V16	AH25 AB20	<del> </del>		1	DQ2B	DQ5B	DQ5B	DQ0B	1		Res.
		10	DIFFIO_B50p	<del> </del>	114	r 13	U16	AG23	<del>                                     </del>	+	<del>                                     </del>	+	<del> </del>	<del> </del>	<del>                                     </del>	<del>                                     </del>		Res.
		VCCINT		1	115			. 1020	1	1	1			1	1	1		
	EFB4N0	10	DIFFIO_B50n	<u> </u>			U17	AF22			<u> </u>	1		<u> </u>	DQ0B			Res.
B4 VRE	EFB4N0	GND			116													
	EFB4N0	10	DIFFIO_B51p	ļ				AE24	ļ		ļ	ļ	ļ	ļ	DQ0B	ļ		Res.
		10	DIFFIO_B51n		<del> </del>		L	AG26				-	ļ		DQ0B			Res.
	EFB4N0	10	PLL4_CLKOUTp PLL4_CLKOUTn	1	117 118		T16	AE23 AF23	<del>                                     </del>	1	<del>                                     </del>	+	<del> </del>	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>		+
		10 10	DIFFIO_B52p	<del> </del>	118	V18	R16 R14	AF23 AD22	<del>                                     </del>	1	<del> </del>	1	<del> </del>	<del> </del>	1	<del>                                     </del>		Res.
		VCCINT	Dil I IO_DUZP	<del> </del>	119	<del>                                     </del>	17.17	AD22	<b> </b>	<del> </del>	<b> </b>	<del>                                     </del>	1	<del> </del>	<del> </del>			1100.
		10	DIFFIO_B52n		T		R15	AE22				1	1					Res.
	EFB4N0	GND			120													



Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18	DQS for X32/X36	PKG
Number	Group	Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	in F780	in F780	NOTES
																		(4), (5), (6)
B4	VREFB4N0		DIFFIO_B53p					AB21										Res.
B4	VREFB4N0		DIFFIO_B53n					AC22										Res.
B4	VREFB4N0							AH26										
B5		VCCD_PLL4				P15	V17	Y20										
B5		GNDA4				P14	V18	AA20										
B5 B5		VCCA4 IO	DIFFIO_R56n		123	N14	U18 AA22	Y21 AA21										A ali
B5			DIFFIO_R56p				AA21	AB22				DM3D/DM6#3D	DM3R1/BWS#3R1	DM1D2/DM/C#1D2				Adj. Adj.
B5	VREFB5N3		DIFFIO_K30p		124		AAZI	ADZZ				DIVISION BWS#3K	DIVISION I/BWS#3K I	DIVITES/BWS#TRS				Auj.
B5		IO	DIFFIO_R55n		124			AB24							DM3R/RWS#3R	DM3R1/RWS#3R1	DM1R3/BWS#1R3	Sen
B5	VREFB5N3		DII 1 10_100II		125			7 (DZ-7							DIVIDITORION	DINOITHBWOHOITH	DWTTO/DWO#TTO	оср.
B5			DIFFIO_R55p			N15		AC24		DM3R/BWS#3R	DM1R1/BWS#1R1							Sep.
B5	VREFB5N3	10	RUP3		126	T16	T17	AA22	DQ1R	DQ3R	DQ1R							
B5	VREFB5N3	10	RDN3				T18	AB23	DQ1R									
B5	VREFB5N3							AD25										
									DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	DQS3R/CQ3R#,	
B5	VREFB5N3				128	T18	W20	AF27	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	CDPCLK4	ļ
B5	VREFB5N3				129		<u> </u>						ļ	ļ			ļ	
B5	VREFB5N3		DIFFIO_R54n			T17	ļ	AE26		DQ3R	DQ1R							Sep.
B5		GND			130	<u> </u>	ļ											L
B5			DIFFIO_R54p		407		<b> </b>	AE27	5045				<b> </b>	<b> </b>	1		<b>.</b>	Sep.
B5	VREFB5N3	10	DIFFIO_R53n		131		<b> </b>	Y22	DQ1R				ļ	ļ			ļ	Adj.
B5	VREFB5N3		DIFFIO_R53p		132	D40	W/4C	AD24	DQ1R				-	-			<b>_</b>	Adj.
B5 B5		10	VREFB5N3		133	R18	W19	AA24 AC25										Can
B5		10	DIFFIO_R52n DIFFIO_R52p					AD26							DOSD	DOSD	DO4D	Sep.
B5	VREFB5N3		DIFFIO_R52p		134		Y22	AE28	DQ1R			DQ3R	DQ3R	DQ1R	DQ3R DQ3R	DQ3R DQ3R	DQ1R DQ1R	Sep. Adj.
B5			DIFFIO_R51II		135		Y21	AA23	DQ1R DQ1R			DQSK	DQSK	DQIK	DQ3K	DQSK	DQIK	Adj.
B5		10	DIFFIO_R50n		155		U20	AD28	DQIIV			DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	.0	DIFFIO_R50p				U19	Y23				DQUIT	DOIN	DQIIV	Daoit	DOON	DQIII	Adj.
B5	VREFB5N2		DIFFIO_R49n				W22	AD27				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R	Adj.
B5			DIFFIO R49p				W21	AC26				DQ3R	DQ3R	DQ1R				Adj.
B5	VREFB5N2		DIFFIO_R48n					Y24							DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	IO	DIFFIO_R48p					W22										Adj.
B5		10	DIFFIO_R47n					AC28							DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	10	DIFFIO_R47p					W21										Adj.
B5	VREFB5N2		DIFFIO_R46n				P15	AC27							DQ3R	DQ3R	DQ1R	Sep.
B5	VREFB5N2				136													
B5	VREFB5N2		DIFFIO_R46p		137		P16	AB26	DQ1R						DQ3R	DQ3R	DQ1R	Sep.
B5		GND			138													ļ
B5	VREFB5N2							V26										
B5		IO	VREFB5N2		139	R17	R17	U24										
B5		10	DIEELO DAS				P17	V22				D 0 0 D	D.00D	0040	0.000	D.O.O.D.	0040	
B5		10	DIFFIO_R45n			-	V22	AA26				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R	Adj.
B5 B5	VREFB5N2 VREFB5N2		DIFFIO_R45p		140	<u> </u>	V21	U26				DQ3R	DQ3R	DQ1R			-	Adj.
B5	VREFB5N2 VREFB5N2		DIFFIO_R44n	1	140		R20	AB28				DQ3R	DQ3R	DQ1R	DM1D/RW/S#1D	DW3DU/BW6#3DU	DM1R2/BWS#1R2	Son
B5	VREFB5N2 VREFB5N2		DII-LIO_K44II	1	141		1720	ADZ0				אפאמ	העטת	שואט	NI #6WaVIII	ONC#CANDING#9K0	DIVITAZIBWO#1KZ	оер.
B5	VREFB5N2		DIFFIO R44p		171		<b>†</b>	AB27					<b>H</b>	<b>H</b>	DQ1R	DQ3R	DQ1R	Sep.
B5			DIFFIO_R44p				U22	V21				DQ3R	DQ3R	DQ1R	23111	23011		Adj.
B5		10	DIFFIO R43p				U21	Y26				DQ3R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R	Adj.
B5		10	DIFFIO_R42n			P18	R18	U20		DQ3R	DQ1R							Adj.
B5		10	DIFFIO_R42p				R19	W26		DQ3R	DQ1R	DM1R/BWS#1R	DM3R0/BWS#3R0	DM1R2/BWS#1R2	DQ1R	DQ3R	DQ1R	Adj.
B5		10	DIFFIO_R41n					W27							DQ1R	DQ3R	DQ1R	Sep.
B5	VREFB5N1	10	DIFFIO_R41p					W28							DQ1R	DQ3R	DQ1R	Sep.
B5	VREFB5N1	10	DIFFIO_R40n					AB25										Adj.
B5		10	DIFFIO_R40p				N16	V28							DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N1		DIFFIO_R39n				R22	AA25				DQ1R	DQ3R	DQ1R				Adj.
B5	VIII. DOIL!	10	DIFFIO_R39p				R21	V27				DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N1		VREFB5N1		142	N16	P20	U23										
B5	VREFB5N1						ļ	W25					ļ	ļ			ļ	ļ
B5	VREFB5N1		DIFFIO_R38n			M14		V25		DQ3R	DQ1R	DQ1R	DQ3R		DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N1		DIFFIO_R38p			L13	P21	R22		DQ3R	DQ1R	DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N1		DIFFIO_R37n				<u> </u>	V24										Sep.
B5	VREFB5N1	Ю	DIFFIO_R37p					U27					l	l			l	Sep.



Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18	DQS for X32/X36	PKG
Number	Group	Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	in F780	in F780	NOTES
										-								(4), (5), (6)
																		( ), (-), (-)
-	VDEEDEN 4		DIEELO DOS					1.00		D00D	DO 4 D	BO 4B	2002	2012				
B5	VREFB5N1	10	DIFFIO_R36n			L15	N20	V23		DQ3R	DQ1R	DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N1	10	DIFFIO_R36p			L14	N19	U28		DQ3R	DQ1R				DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N1	10	DIFFIO_R35n					Y25										Adj.
B5	VREFB5N1	10	DIFFIO_R35p					T26										Adj.
B5	VREFB5N0	10	DIFFIO_R34n					W20										Adj.
B5	VREFB5N0	IO	DIFFIO_R34p					U22										Adj.
B5		10	DIFFIO_R33n			M17	N17	V20		DQ3R	DQ1R							Adj.
50	VIIIEI BOIIO		5o			1		***	DQS1R/CQ1R#.		DQS1R/CQ1R#,	DOC4D/CO4D#	DOC4D/CO4D#	DOC4D/CO4D#	DQS1R/CQ1R#.	DOC4D/CO4D#	DQS1R/CQ1R#.	, .c.j.
B5	VREFB5N0	10	DIEEIO Daam		143	1.46	N18	T25		DQS1R/CQ1R#,		DQS1R/CQ1R#,	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6		DQS1R/CQ1R#,		Adi.
		10	DIFFIO_R33p	557.05					DPCLK6	DPCLK6	DPCLK6	DPCLK6	DPCLKO	DPCLK6	DPCLK6	DPCLK6	DPCLK6	-,
B5	VI LLI DOI TO	Ю	DIFFIO_R32n	DEV_OE	144	M18	N22	T22										Adj.
B5		Ю	DIFFIO_R32p	DEV_CLRn	145	L17	N21	T21										Adj.
B5		Ю	DIFFIO_R31n				M22	R26				DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N0	IO	DIFFIO_R31p				M21	R25				DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N0	10	DIFFIO_R30n				M20	R28				DQ1R	DQ3R	DQ1R	DM0R	DM1R1/BWS#1R1	DM1R1/BWS#1R1	Adj.
B5	VREFB5N0	10	DIFFIO_R30p				M19	U25				DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N0	IO	VREFB5N0		146	L18	M16	R24										1
B5				1	1	<u> </u>		R27	1	1	1	†	1	1	1	DQ1R	DQ1R	1
B5	VREFB5N0				147	1	1								1			+
		IO	DIEEIO DOO	+	147	V10	1	Daa		DM1D/DMC#15	DM4D0/DM/C#4D0	<del> </del>	+	<b>†</b>	+	<del> </del>	1	Con
B5			DIFFIO_R29n			K18		R23		DINI 1K/BW5#1R	DM1R0/BWS#1R0	<del>                                     </del>	<b></b>	<b> </b>	<del> </del>	<del>                                     </del>		Sep.
B5		GND			148		<u> </u>						ļ		ļ			<del>_</del>
B5	VREFB5N0	Ю	DIFFIO_R29p			K17		R21		DQ1R	DQ1R							Sep.
B5	VREFB5N0	Ю						P21										
B5	VREFB5N0	CLK7	DIFFCLK_3n		149	N18	T22	Y28										
B5	VREFB5N0	CLK6	DIFFCLK_3p		150	N17	T21	Y27										1
B6	VREFB6N3	CLK5	DIFFCLK_2n		151	F18	G22	J28										1
B6	VREFB6N3	CLK4	DIFFCLK_2p		152	F17	G21	J27										+
B6	VREFB6N3	CONF DONE	Bii i GEI(_Ep	CONF DONE	153	K14		P24										1
B6				CON _DONE	154	17.1-4	IVI IO	1 24										+
		VCCIO6					<u> </u>											
B6		MSEL0		MSEL0	155	K13	M17	N22										
B6	VREFB6N3	GND			156	1												
B6		MSEL1		MSEL1	157	J18	L18	P23										
B6	VREFB6N3	MSEL2		MSEL2	158	J17	L17	M22										
B6	VREFB6N3	MSEL3		MSEL3 (1)		J14	K20	P22										
B6	VREFB6N3	10	DIFFIO_R28n					K25										Adj.
B6	VREFB6N3	IO	DIFFIO R28p			H17		M24		DQ1R	DQ1R							Adj.
B6		10	DIFFIO_R27n	INIT_DONE	159	G18	L22	P26		DQIII	DQIIC							Adj.
B6			DIFFIO R27p	CRC ERROR	160	G17		P25								-		Adj.
		10		CRC_ERROR	100	GII	LZI											
B6		10	DIFFIO_R26n		<u> </u>	<u> </u>		H26										Adj.
B6	VI LI DONO	10	DIFFIO_R26p					L25										Adj.
B6	VREFB6N3	10	VREFB6N3		161	J13	K19	N21										
B6	VREFB6N3	10	DIFFIO_R25n					N25										Adj.
B6	VREFB6N3	10	DIFFIO_R25p					G24										Adj.
B6	VREFB6N3	IO	DIFFIO R24n	nCEO	162	E18	K22	P28										Sep.
B6		VCCINT		1	163	<u> </u>			1	1	1	†	1	1	1	†	1	1.77
B6		IO	DIFFIO_R24p	CLKUSR	164	E17	K21	P27							1			Sep.
		.0	Dil 1 10_R24p	OLIVOON		L1/	1141	. 21	1	1	1	<del> </del>	1	1	1	<del> </del>	1	эер.
B6	VREFB6N3	GND	1	1	165	<u> </u>	1		D00000/0045	D000D/0045	DOCCODIO CAD	D000D(004E	D000D/004D	DOGGD/OO4D	D0000000045	DOCODIOCAE	D000D/004E	+
D.C.	VREFB6N3	l.o	DIEEIO BOO-		160	1140	122	NOC	DQS0R/CQ1R,	DQS0R/CQ1R,	DQS0R/CQ1R,	DQS0R/CQ1R,	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R,	DQS0R/CQ1R,	DQS0R/CQ1R,	A 41:
B6		IU	DIFFIO_R23n		166	H16	J22	N26	DPCLK7	DPCLK7	DPCLK7	DPCLK7			DPCLK7	DPCLK7	DPCLK7	Adj.
B6		Ю	DIFFIO_R23p				J21	L22	ļ	ļ	ļ	DM0R	DM1R1/BWS#1R1	DM1R1/BWS#1R1	ļ	ļ	ļ	Adj.
B6		Ю	DIFFIO_R22n				H22	M28				DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R	Sep.
B6	VREFB6N2	10	DIFFIO_R22p				H21	M23				DQ0R	DQ1R	DQ1R				Sep.
B6		IO						M27							DQ0R	DQ1R	DQ1R	T
B6	VREFB6N2		DIFFIO_R21n	Ì				L20				İ	Ì	Ì		T		Adj.
B6	VREFB6N2		DIFFIO_R21p		1	1	1	M26							DQ0R	DQ1R	DQ1R	Adj.
B6		10			1		V17		1	1		t	1	1	DQUIT	Dalik	DQ IIV	
	VREFB6N2	10	DIFFIO_R20n	<b> </b>	1	-	K17	K22	-	-		DOOD	DOAD	DOAD	<del> </del>	<del>                                     </del>		Adj.
B6	VREFB6N2	10	DIFFIO_R20p	1	l		K18	L23		ļ		DQ0R	DQ1R	DQ1R	ļ	<del>                                     </del>	1	Adj.
B6		VCCINT	<b></b>		167	<u> </u>	<b></b>					<b></b>			ļ	<b></b>		4
B6	VREFB6N2	Ю			1			J26										1
B6	VREFB6N2	GND			168	$\mathbb{L}^{\top}$	$\bot$											
B6		IO	DIFFIO_R19n					H25										Adj.
B6	VREFB6N2	IO	DIFFIO R19p					K21	İ	İ		İ	Ì	Ì	İ	İ		Adi.
B6	VREFB6N2	10	VREFB6N2		169	H18	J18	M25				t	<b> </b>	<b>†</b>	<b>†</b>	<b>†</b>		, ruj.
					109	П10			1	1	1	DOOD	DO4D	DO4D	1	<del>                                     </del>	1	A ali
B6	VREFB6N2	10	DIFFIO_R18n		<u> </u>	1	F22	J23	1	1		DQ0R	DQ1R	DQ1R	D 0 0 D	2012	0010	Adj.
B6		10	DIFFIO_R18p		<u> </u>	<u> </u>	F21	L28				DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R	Adj.
B6		10	DIFFIO_R17n					L27							DQ0R	DQ1R	DQ1R	Sep.
B6	VREFB6N2	10	DIFFIO_R17p		L	L		L24		L		L			DQ0R	DQ1R	DQ1R	Sep.



Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18	DQS for X32/X36	PKG
Number	Group	Function	Function(s)	Function			U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	in F780	in F780	NOTES
	o.oup		1 411041011(0)				0.0.			. 02 .								(4), (5), (6
																		(4), (5), (
36	VREFB6N2	Ю	DIFFIO_R16n					E25										Adj.
36	VREFB6N2	Ю	DIFFIO_R16p					K28							DQ0R	DQ1R	DQ1R	Adj.
36	VREFB6N2	IO	DIFFIO_R15n					F24										Adj.
B6	VREFB6N1	10	DIFFIO_R15p					K27							DQ0R	DQ1R	DQ1R	Adj.
B6	VREFB6N1	IO	DIFFIO R14n				1	J24										Adj.
De .	VREFB6N1	10	DIFFIO R14p			1		L26							DMOD	DM4D0/DW6#4D0	DM4DO/DM6#4D0	
56		.0			_	1									DM2R	DIVITRU/BWS#TRU	DM1R0/BWS#1R0	
B6	VREFB6N1	IO	DIFFIO_R13n				H20	H23				DQ0R	DQ1R	DQ1R				Adj.
B6	VREFB6N1	IO	DIFFIO_R13p				H19	J25				DQ0R	DQ1R	DQ1R		DQ1R	DQ1R	Adj.
B6	VREFB6N1	VCCIO6			170													
36	VREFB6N1	IO	DIFFIO R12n	nWE	171	D18	E22	G28	DQ1R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Sep.
36	VREFB6N1	GND			172													
B6	VREFB6N1	10	DIFFIO_R12p	nOE	172	D17	E21	G27		DQ1R	DQ1R		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Co.
50		10		IIUE		ווע	EZI			DQIR	DQIR		DQIR	DQIR	DQZR	DQIR	DQIR	Sep.
B6	VREFB6N1	IO	DIFFIO_R11n					H22										Adj.
36	VREFB6N1	10	DIFFIO_R11p					H24										Adj.
B6	VREFB6N1	IO	VREFB6N1		173	H15	H18	M21										
36	VREFB6N1	10	DIFFIO_R10n				J17	G25										Adj.
B6	VREFB6N1	IO	DIFFIO R10p		1	1	H16	K26	İ			İ			DQ2R	DQ1R	DQ1R	Adj.
B6	VREFB6N1	IO	DIFFIO_R9n					G26				DM2R	DM1R0/BWS#1R0	DM1R0/BWS#1R0	Duzit	DQ	DQ.II.	
				+		+	D22		1	-	-	DIVIZIT			-	1		Adj.
B6	VREFB6N1	10	DIFFIO_R9p	+		1	D21	G23	ļ	ļ.,		<b>!</b>	DQ1R	DQ1R	ļ	ļ .		Adj.
B6	VREFB6N1	IO	DIFFIO_R8n	nAVD		H14	F20	F28		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Sep.
36	VREFB6N1	10	DIFFIO_R8p		1	H13	F19	F27		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R				Sep.
B6	VREFB6N1	IO	DIFFIO_R7n	PADD23		G14	G18	E28		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Adj.
B6	VREFB6N1	io	DIFFIO_R7p	<del> </del>	-	1	H17	G22	1	T	T	<del> </del> -	† <del>* * * * * * * * * * * * * * * * * * *</del>	T	T	† <del></del>	1	Adj.
20	VREFB6N1	10	DIFFIO_R/p		-	1		E27				DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	
36		Ю			_	1	C22								DQZR	DQTR	DQTR	Adj.
36	VREFB6N0	Ю	DIFFIO_R6p				C21	H21				DQ2R	DQ1R	DQ1R				Adj.
B6	VREFB6N0	IO						F26							DQ2R	DQ1R	DQ1R	
36	VREFB6N0	VCCINT			174													
36	VREFB6N0	Ю	DIFFIO_R5n	PADD22		C18	B22	D28		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R				Sep.
B6	VREFB6N0	GND	Bii i io_rtoii	1710022	175	0.0		520		DQC	54	DQLIT	DQt	54				
	VREFB6N0	GIND	DIEEIO DE-	PADD21	173	047	D04	D07		DO4D	DO4D	DOOD	DOAD	DO4D	DOOD	DO4D	DOAD	
B6	VKEFB6NU	Ю	DIFFIO_R5p	PADD21	_	C17	B21	D27		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Sep.
									DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	DQS2R/CQ3R,	
B6	VREFB6N0	Ю	DIFFIO_R4n	PADD20	176	B18	C20	C27	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	CDPCLK5	Adj.
B6	VREFB6N0	IO	DIFFIO_R4p					F25										Adj.
B6	VREFB6N0	IO	VREFB6N0		177	B17	D20	J22										
B6	VREFB6N0	10	DIFFIO R3n			D.,,	520	E26										Adj.
		10			_	-		E24										
B6	VREFB6N0	Ю	DIFFIO_R3p			1												Adj.
B6	VREFB6N0	Ю	DIFFIO_R2n				F17	D25				DQ2R	DQ1R	DQ1R				Sep.
B6	VREFB6N0	IO	DIFFIO_R2p				G17	D24										Sep.
B6	VREFB6N0	10	DIFFIO_R1n					D26										Adj.
B6	VREFB6N0	IO	DIFFIO R1p					C26										Adj.
B6	VREFB6N0	VCCA2	Dil 110_1(1)		178	F14	F18	J21										, ruj.
50																		
36	VREFB6N0	GNDA2			179	F15	E18	H20										
36	VREFB6N0	VCCD_PLL2			180	E15	E17	J20										
37	VREFB7N0	VCCINT			181													
37	VREFB7N0	Ю						G21										
37	VREFB7N0	GND	1		182	1	1	1								1		+
27		IO	DIEEIO TEO	+	102	+	<b>†</b>	Pac	<b>†</b>	<b> </b>	<b>†</b>	<u> </u>	1	<b>†</b>	DOOT	<del> </del>		Poc
o/	VREFB7N0	.0	DIFFIO_T52n	+		1	<del>                                     </del>	B26	<del>                                     </del>	1	<del> </del>	<del>                                     </del>	+	<del> </del>	DQ0T	<del>                                     </del>	<del>                                     </del>	Res.
37	VREFB7N0	10	DIFFIO_T52p		_	1	<u> </u>	D22	ļ	ļ	ļ			ļ	DQ0T	ļ		Res.
37	VREFB7N0	IO	DIFFIO_T51n				F16	E22							DQ0T			Res.
37	VREFB7N0	10	DIFFIO_T51p			1	E16	J19	1			DQ2T	DQ5T	DQ5T		1		Res.
37	VREFB7N0	Ю	DIFFIO_T50n				F15	A26				DQ2T	DQ5T	DQ5T	DQ0T			Res.
37		10	DIFFIO_T50p	1	-	1	G16	G20	1	1	1	† <del></del> -	† <del></del> -	T	T	1	1	Res.
77			5/11/10_100p	+	+	+	510	B25	1	1	1	1	+	1	DQ0T	1		1100.
٥/	VREFB7N0		1	+		<del>                                     </del>	<u> </u>		1	ļ	1	<b>!</b>	1	1	וטטטו	1	ļ	+
37	VREFB7N0	Ю	DIFFIO_T49n			C16	G15	G19	ļ		ļ		ļ	ļ		ļ		Res.
	I	1			1	1	1		DQS0T/CQ1T,	DQS0T/CQ1T,	DQS0T/CQ1T,	DQS0T/CQ1T,	DQS0T/CQ1T,	DQS0T/CQ1T,	DQS0T/CQ1T,	DQS0T/CQ1T,	DQS0T/CQ1T,	
37	VREFB7N0	10	DIFFIO_T49p		183	D16	F14	A25	CDPCLK6	CDPCLK6	CDPCLK6	CDPCLK6	CDPCLK6	CDPCLK6	CDPCLK6	CDPCLK6	CDPCLK6	Res.
37	VREFB7N0	IO	DIFFIO_T48n				H15	F21							DQ0T			Res.
37	VREFB7N0	IO	DIFFIO T48p		1	A18	H14	C25	1	DQ5T	DQ5T	İ		Ì	DQ0T	1		Res.
37	VREFB7N0		VREFB7N0	+	184	A17	D17	F22	<del>                                     </del>	2401	2401	<del>                                     </del>	+	<u> </u>	23(01	<del>                                     </del>	<del> </del>	1103.
			VKCFB/INU	+	104	AII	ווע		<b> </b>	-	<b> </b>	<b>_</b>	+	<b> </b>	B 0 0 T	<del>                                     </del>		+
37	VREFB7N0		ļ			1	<u> </u>	A23	ļ		ļ		ļ	ļ	DQ0T	ļ		
37	VREFB7N0	IO	DIFFIO_T47n	1			C19	H19		ļ		DQ2T	DQ5T	DQ5T	ļ			Res.
37	VREFB7N0	IO	DIFFIO_T47p				D19	B23				DQ2T	DQ5T	DQ5T	DM0T			Res.
37	VREFB7N0	IO	PLL2_CLKOUTn		185	C14	A20	C23				İ	İ					1
B7	VREFB7N1	10	PLL2_CLKOUTp	+	186	D14	B20	D23	<b>†</b>		<b>†</b>	<b>†</b>	+	<b>†</b>	<u> </u>	<b>†</b>		+
) i		.0		+	100	14 טו	DZU		<del> </del>	<del>                                     </del>	<del>                                     </del>	<del>                                     </del>	+	<del>                                     </del>	DOOT	DOST	DOST	-
	VREFB7N1	IO	DIFFIO_T46n	I		1	<u> </u>	C24 E21	ļ	ļ	ļ	DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1		DIFFIO_T46p				C17											Res.

Version 1.3 Notes (2), (3)

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Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18	DQS for X32/X36	es (2), (3)
Number	Group	Function	Function(s)	Function	4240	. 524	U484		Q240	F324	F324	F484/U484	F484/U484	F484/U484	F780	in F780	in F780	NOTES
Number	Group	runction	runction(s)	Function			0464		Q240	F324	F324	F404/U404	F404/U404	F404/U404	F/0U	III F 700	III F/00	
																		(4), (5), (6)
D.7	VREFB7N1	IO	RUP4		187	E14	B19	F19	+									+
ь/		,,,																
B7	VREFB7N1	10	RDN4		188	E13	A19	E19										
B7	VREFB7N1	IO						C22							DQ2T	DQ5T	DQ5T	
R7	VREFB7N1	IO	DIFFIO_T45n				A18	D21				DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T	Res.
D7				DADDO	+	E42			+	DOST	DOST	DQLI	DQUI	DQUI	DQLI	DQUI	Daoi	
В/	VREFB7N1	IO	DIFFIO_T45p	PADD0	1	E12	B18	B22		DQ5T	DQ5T							Res.
B7	VREFB7N1	10	VREFB7N1		189	D12	D15	F18										
B7	VREFB7N1	IO	DIFFIO T44n				E15	C21				DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	IO	DIFFIO_T44p		1	1	G14	D19										Res.
					<del> </del>	-	G 14											
B7	VREFB7N1	IO	DIFFIO_T43n					A22							DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	10	DIFFIO_T43p					A21							DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	VCCINT			190													
					130	1							-					_
B7	VREFB7N1	IO	DIFFIO_T42n				G13	B21							DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	GND			191													
R7	VREFB7N1	IO	DIFFIO_T42p					E18							DQ2T	DQ5T	DQ5T	Res.
B7			DII 1 10_142p	1	192	1	1	L10					+		DQLI	DQUI	DQUI	1100.
В/	VREFB7N1				192													
B7	VREFB7N1	10	DIFFIO_T41n	PADD1		A16	A17	C18				DQ2T	DQ5T	DQ5T		DQ5T	DQ5T	Res.
B7	VREFB7N2	GND			193											I		
R7	VREFB7N2	10	DIFFIO_T41p	PADD2	194	B16	B17	D18	DQ5T	DQ5T	DQ5T	Ì	DQ5T	DQ5T	Ì	1		Res.
D/				FAUUZ	194	010			ופטע	ופאת	ונטע	D110T			D1107	D. 1570 (5:	D14870/0:	
B7	VREFB7N2	10	DIFFIO_T40n	ļ	1	1	A16	C20	ļ		1	DM2T	DM5T0/BWS#5T0	DM5T0/BWS#5T0	DM2T	DM5T0/BWS#5T0	DM5T0/BWS#5T0	
B7	VREFB7N2	IO	DIFFIO T40p		1	1	B16	H17				DQ4T	DQ5T	DQ5T				Res.
B7	VREFB7N2	10	VREFB7N2	1	195	C12	C15	G17	1	1	1	1		1	Ì	1		1
0.0				<del>                                     </del>	190	012	010		+	<del></del>	<del>                                     </del>	1	+	<del>                                     </del>	DO 17	DOST	DO ST	-
B7	VREFB7N2	Ю	DIFFIO_T39n	ļ		1	<u> </u>	D20	1	1	1		1	1	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N2	IO	DIFFIO_T39p					C19							DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N2	IO	DIFFIO_T38n	PADD3	196	A15	E14	C17		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
57				17,880		7110	L 1-T		DOST	DQUI	DQUI	DQTI	Daei	DQUI	DQTI	DQUI	DQUI	
В/	VREFB7N2	Ю	DIFFIO_T38p		197			G18	DQ5T									Res.
B7	VREFB7N2	IO						H15										
B7	VREFB7N2	VCCINT			198													
B7	VREFB7N2	IO	DIFFIO_T37n		100	1	1	F17										Res.
			DIFFIO_13/11		<del> </del>	-		F17										Res.
B7	VREFB7N2	GND			199													
									DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	DQS2T/CQ3T,	
B7	VREFB7N2	IO	DIFFIO T37p	PADD4	200	B15	F13	D17	DPCLK8	DPCLK8	DPCLK8	DPCLK8	DPCLK8	DPCLK8	DPCLK8	DPCLK8	DPCLK8	Res.
B7	VREFB7N2	IO	DIFFIO_T36n	PADD5	201	A14	A15	A19	DQ5T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	IO	DIFFIO_T36p	PADD6	202	B14	B15	B19	DQ5T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	IO	DIFFIO_T35n	PADD7		A13	C13	A18										Res.
B7	VREFB7N3	IO	DIFFIO T35p	PADD8			D13	B18		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
				17,880	1	D10	D10			DQUI	DQUI	DQTI	Daei	DQUI				
B7	VREFB7N3	Ю	DIFFIO_T34n					E17							DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	IO	DIFFIO_T34p					J16										Res.
B7	VREFB7N3	IO	DIFFIO_T33n					J17										Res.
B7	VREFB7N3	10	DIFFIO T33p		1	1		H16										Res.
ы					1	1	<del>                                     </del>						+					
B7	VREFB7N3	10	DIFFIO_T32n					G16										Res.
B7	VREFB7N3	IO	DIFFIO T32p					F15										Res.
R7	VREFB7N3	IO	VREFB7N3		203	E11	E13	G15										
D7		.0		DADDO	200				1	DOST	DOST	DOAT	DOST	DOST	DOAT	DOST	DOST	Dee
B7	VREFB7N3		DIFFIO_T31n	PADD9	-	A12	A14	C16	<b>+</b>	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	VCCINT	<u> </u>		204	<u> </u>		<u></u>	<u> </u>				<u> </u>					<u> </u>
B7	VREFB7N3	IO	DIFFIO T31p	PADD10		B12	B14	D16				DQ4T	DQ5T	DQ5T		I		Res.
B7	VREFB7N3	GND			205	1			Ì	1	†		1	1	Ì	†		
D7			DIEEIO TOO	1	200	+	<del>                                     </del>		1	+	t	1	+	t	1	<del> </del>	1	D
R/	VREFB7N3	Ю	DIFFIO_T30n		1	1	ļ	H14				ļ			ļ	<b></b>		Res.
B7	VREFB7N3	IO	DIFFIO_T30p	<u> </u>	<u> </u>	<u>L</u>	<u> </u>	K15	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	<u> </u>	Res.
B7	VREFB7N3	IO	DIFFIO_T29n	PADD11		A11	A13	A17		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T		DQ5T	DQ5T	Res.
 D7					206	<del>/ ` · · ·</del>		· · · ·	1			- ~			1			
D/	VREFB7N3	vCCIU/	+	<b> </b>	206	1	-	<b>!</b>	1				<del> </del>	L	L	L		1
	l	1	1	1	1	1	1	1	DQS4T/CQ5T,	DQS4T/CQ5T,	DQS4T/CQ5T,	DQS4T/CQ5T,	DQS4T/CQ5T,	DQS4T/CQ5T,	DQS4T/CQ5T,	DQS4T/CQ5T,	DQS4T/CQ5T,	1
B7	VREFB7N3	IO	DIFFIO_T29p	PADD12	207	B11	B13	B17	DPCLK9	DPCLK9	DPCLK9	DPCLK9	DPCLK9	DPCLK9	DPCLK9	DPCLK9	DPCLK9	Res.
B7		GND			208	1		1	Ì	1	†	İ	1	†	Ì	†		İ
 D7			DIEEIO TOO-	<del> </del>		+	<del>                                     </del>	E45	1	<del>                                     </del>	<del>                                     </del>		†	<del>                                     </del>	DMAT	DMET4/DWO4ET	DMETA/DWO4ET	Dee
R/	VREFB7N3	Ю	DIFFIO_T28n			1		E15		L	<b></b>	ļ	<b></b>	<b></b>	DM4T	DM511/BWS#5T1	DM5T1/BWS#5T1	
B7	VREFB7N3	10	DIFFIO_T28p			<u> </u>	E12	J14			<u> </u>	<u> </u>	DQ5T	DQ5T	<u> </u>	<u></u>		Res.
B7	VREFB7N3	IO	DIFFIO_T27n	PADD13		C10	E11	C15		DM5T/BWS#5T	DM5T0/BWS#5T0					I		Res.
	VREFB7N3	10	DIFFIO_T27p	PADD14	1	D10		D15	1			DM4T	DM5T1/RM/C#ET4	DM5T1/BWS#5T1	DQ5T	DQ3T	DQ5T	
R7				1 AUU 14	1				+	<del>                                     </del>	<del>                                     </del>	DIVI4 I	LIC#CANGALICIAN	רונ#פועם/וונואים	ונשטו	ונטטו	ונטטו	Res.
B7	VREFB7N3	CLK8	DIFFCLK_5n		209	A10	A12	A15										1
B7 B7		CLK9	DIFFCLK 5p		210	B10	B12	B15								I		
B7 B7 B7	VREFB7N3	CLN9		1	211	A9	A11	A14	1	1	1	Ì	1	1	Ì	1		1
B7 B7	VREFB7N3		IDIEECI V 45				ALI.			<del>                                     </del>	<del>                                     </del>	1	+	<del>                                     </del>	ļ			+
B7 B7 B8	VREFB7N3 VREFB8N0	CLK10	DIFFCLK_4n			_	D 4 4											
B7	VREFB7N3 VREFB8N0 VREFB8N0		DIFFCLK_4p		212	B9	B11	B14										<u> </u>
B7 B7 B8	VREFB7N3 VREFB8N0	CLK10				_	B11 D10	B14 C13				DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	Res.
B7 B7 B8 B8 B8	VREFB7N3 VREFB8N0 VREFB8N0 VREFB8N0	CLK10 CLK11 IO	DIFFCLK_4p DIFFIO_T26n			_	D10	C13				DQ5T	DQ3T	DQ5T				Res.
B7 B7 B8	VREFB7N3 VREFB8N0 VREFB8N0 VREFB8N0 VREFB8N0	CLK10 CLK11	DIFFCLK_4p DIFFIO_T26n DIFFIO_T26p			_	D10 E10	C13 D13							DQ5T	DQ3T	DQ5T	Res.
B7 B7 B8 B8 B8	VREFB7N3 VREFB8N0 VREFB8N0 VREFB8N0 VREFB8N0 VREFB8N0	CLK10 CLK11 IO	DIFFCLK_4p DIFFIO_T26n DIFFIO_T26p DIFFIO_T25n			B9	D10 E10 A10	C13 D13 C14				DQ5T DQ5T	DQ3T DQ3T	DQ5T DQ5T				Res. Res.
B7 B7 B8 B8 B8	VREFB7N3 VREFB8N0 VREFB8N0 VREFB8N0 VREFB8N0	CLK10 CLK11 IO	DIFFCLK_4p DIFFIO_T26n DIFFIO_T26p	PADD15		_	D10 E10	C13 D13							DQ5T	DQ3T	DQ5T	Res.



Bank Number		Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484		DQS for X8/X9 in Q240		DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B8	VREFB8N0	VCCION			213													+
		VCCIO							DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	DQS5T/CQ5T#,	+
B8 B8	VREFB8N0 VREFB8N0	IO GND	DIFFIO_T24p	PADD17	214 215	D9	B9	D12	DPCLK10	DPCLK10	DPCLK10	DPCLK10	DPCLK10	DPCLK10	DPCLK10	DPCLK10	DPCLK10	Res.
B8		IO	DIFFIO_T23n		210			A12							DQ5T	DQ3T	DQ5T	Res.
B8	VREFB8N0	10	DIFFIO_T23p					B12										Res.
B8	VREFB8N0	10	VREFB8N0		216	E9	C10	G14	0.057									
B8 B8	VREFB8N0 VREFB8N0	10	DIFFIO_T22n DIFFIO_T22p		217		G11	K13 F14	DQ5T			ļ						Res.
B8		10	DIFFIO_122p					E14							DQ5T	DQ3T	DQ5T	Res.
B8		10	DIFFIO_T21n					H12										Res.
B8		10	DIFFIO_T21p					J12										Res.
B8 B8		10 10	DIFFIO_T20n DIFFIO_T20p	DATA2 DATA3	218 219	A8 B8	A8 B8	A11 B11	DQ5T	DQ3T	DQ5T	DQ5T DQ5T	DQ3T DQ3T	DQ5T DQ5T	DQ5T DQ5T	DQ3T DQ3T	DQ5T DQ5T	Res.
B8	VREFB8N1		DIFFIO_T19n	PADD18	210		A7	A10	DQST	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DQSI	DQSI	DQJI	Res.
B8	VREFB8N1				220													
B8	VREFB8N1		DIFFIO_T19p	DATA4	221	B7	B7	B10	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DM5T/BWS#5T	DM3T0/BWS#3T0	DM5T2/BWS#5T2	Res.
B8 B8	VREFB8N1 VREFB8N1	GND IO	DIFFIO_T18n	PADD19	222	A6	A6	G13		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	<del>                                     </del>	-	1	Pac
B8	VREFB8N1	10	DIFFIO_118h	DATA15	1	B6	B6	H13		D431	ומאו	DQ5T DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N1	Ю	DIFFIO_T17n			Ė		B8										Res.
B8	VREFB8N1	10	DIFFIO_T17p					C10							DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N1		) (DEEDONIA		000	07	F0	D11										+
B8	VREFB8N1	Ю	VREFB8N1		223	C7	E9	F11	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	DQS3T/CQ3T#,	+
В8	VREFB8N1	Ю	DIFFIO_T16n	DATA14	224	A5	C8	E12	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	DPCLK11	Res.
B8	VREFB8N1		DIFFIO_T16p	DATA13		B5	C7	F12				DM5T/BWS#5T	DM3T0/BWS#3T0	DM5T2/BWS#5T2				Res.
B8		10	DIFFIO_T15n					D10							DQ3T	DQ3T	DQ5T	Res.
B8 B8	VREFB8N1 VREFB8N1	10	DIFFIO_T15p DIFFIO_T14n				H11	F10 E11							DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N1		DIFFIO_T14II				H10	E8							DQSI	DQST	DQSI	Res.
B8	VREFB8N1		DIFFIO_T13n					E10										Res.
B8	VREFB8N2		DIFFIO_T13p					E7										Res.
B8 B8	VREFB8N2 VREFB8N2	10 10	DIFFIO_T12n DIFFIO_T12p					A7 G10							DQ3T	DQ3T	DQ5T	Res.
B8		10	DIFFIO_T11n					G11										Res.
B8	VREFB8N2	VCCIO8	_		225													
B8	VREFB8N2		DIFFIO_T11p	DATA5	226	C5	A5	B7	DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8 B8		GND IO	DIFFIO_T10n		227			B3										Res.
в В8	VREFB8N2		DIFFIO_I IUII		228			ьз				-						Res.
B8		10	DIFFIO_T10p		LLU			J10										Res.
B8		GND			229													
B8	VREFB8N2	10	DIFFIO_T9n					F8 F7										Res.
B8 B8	VREFB8N2 VREFB8N2	IO IO	DIFFIO_T9p VREFB8N2	<del>                                     </del>	230	D7	B5	F7 G12						<del> </del>	<del>                                     </del>		1	Res.
B8	VREFB8N2		DIFFIO_T8n				G10	A6									1	Res.
B8	VREFB8N2		DIFFIO_T8p	DATA6	231	E8	F10	B6	DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N2		DIFFIO_T7n	DATA7	232	A4	C6	C11	DM5T/BWS#5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8 B8		10	DIFFIO_T7p	<del>                                     </del>	<del>                                     </del>		D7	H10 G8						<del> </del>	<del>                                     </del>		1	Res.
B8		10	DIFFIO_T6n	1	<del>                                     </del>		A4	C9				DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N2	VCCINT			233													
B8	VREFB8N3		DIFFIO_T6p	DATA8		B4	B4	D9				DQ3T	DQ3T	DQ5T			ļ	Res.
B8 B8		GND IO	DIFFIO_T5n	DATA9	234	E7	F8	A8		DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DM3T/RWS#3T	DM3T1/RWS#3T1	DM5T3/BWS#5T3	Res.
B8	VREFB8N3	10	DIFFIO_T5p	DITINO	<del>                                     </del>		G8	C8		5401	D001	D001	D401	D401	DQ1T	DINIOT ITOWO#311	DINIOTOROVO#013	Res.
B8	VREFB8N3	10						D8							DQ1T			
B8	VIILE DOING	10	DIFFIO_T4n	DATA10		A3	A3	C7		DM3T/BWS#3T	DM5T1/BWS#5T1	DQ3T	DQ3T	DQ5T	DQ1T			Res.
B8 B8	VREFB8N3	10	DIFFIO_T4p VREFB8N3	DATA11	235	B3 E6	B3	D7 G9				DQ3T	DQ3T	DQ5T	<del>                                     </del>			Res.
B8	VREFB8N3 VREFB8N3	10	VKEFDONS	<del>                                     </del>	233	<u></u>	D6 E7	G9 D6						<del> </del>	DQ1T		+	+
B8	VREFB8N3		DIFFIO_T3n	1			C3	A4				DQ3T	DQ3T	DQ5T	DQ1T			Res.
B8	VREFB8N3		DIFFIO_T3p	DATA12	236	D5	C4	B4	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	Res.

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Bank	VREFB	Pin Name /	Optional	Configuration	Q240	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X8/X9 in	DQS for X16/X18 in	DQS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18	DQS for X32/X36	PKG
Number			Function(s)	Function			U484			F324	F324	F484/U484	F484/U484			in F780	in F780	NOTES
										-	-							(4), (5), (6)
																		( - ), ( - ), ( - )
B8	VREFB8N3				237													
B8	VREFB8N3		DIFFIO_T2n					A3							DQ1T			Res.
B8	VREFB8N3	GND			238													
B8		Ю	DIFFIO_T2p					C6							DQ1T			Res.
B8	VREFB8N3	10	DIFFIO_T1n				F7	H8				DM3T/BWS#3T	DM3T1/BWS#3T1	DM5T3/BWS#5T3				Res.
B8	VREFB8N3	10	DIFFIO_T1p				G7	C4							DQ1T			Res.
B8	VREFB8N3		_				F9	D4							DM1T			
B8	VREFB8N3		PLL3 CLKOUTn		239	A1	E6	C5							J			+
B8	VREFB8N3		PLL3_CLKOUTp		240	A2	E5	D5			<u> </u>						-	+
			PLL3_CLKOUTP		240	AZ												
B8	VREFB8N3				1		G9	C3										
		VCCINT					J11	K9										
		VCCINT				G8	J12	K11										
		VCCINT				G10	L14	L16										
		VCCINT				G11	M14	K17										
		VCCINT				G12	P11	K19										
		VCCINT				H7	P12	L10										-
		VCCINT			1		L9	L12										+
		VCCINT	<b>†</b>	<b>†</b>	<del>                                     </del>	J7	M9	L14	t		<b>†</b>	t	<b> </b>				<b>†</b>	+
			<del> </del>	-	+				<del>                                     </del>		<del>                                     </del>	<del>                                     </del>	1	-		-	<del>                                     </del>	+
	<del>                                     </del>	VCCINT	<del>                                     </del>	<del>                                     </del>	1	J12	J13	L18	<del>                                     </del>		<del>                                     </del>	<del>                                     </del>					<del>                                     </del>	+
		VCCINT	L		<b></b>	K7	J14	N20	L		L	L					L	<del>  </del>
		VCCINT			1	K12	K14	M11										ļ
		VCCINT				L7	J10	M13										
		VCCINT			1	L12	K9	M15										
		VCCINT				M7	N9	M17										
		VCCINT				M8	P9	M19										-
		VCCINT			1		P10	N10										+
		VCCINT	-		+	M11	P13	N12			<u> </u>						<u> </u>	+
			-	-	1			N1Z			-	-					-	+
		VCCINT			1	M12	P14	N14										
		VCCINT				F10		N16										
		VCCINT					J16	N18										
		VCCINT				F6	K15	P9										
		VCCINT				F8	L16	P11										
		VCCINT				G13		P13										
		VCCINT					R12	P15										-
		VCCINT				N11	R10	P17										+
		VCCINT			+		R8	P19			+							+
	-				1													+
		VCCINT			1	N7	H9	R10										
		VCCINT			1	N9	G12	R12										
		VCCINT						R14										
		VCCINT						R16										
		VCCINT						R18										
		VCCINT						R20										T
		VCCINT						T11										1
	1	VCCINT	†	†			1	T13	†	1	†	†	1	1	1		†	1
	<b>-</b>	VCCINT			1		1	T15										+
	<del>                                     </del>		<del>                                     </del>	+	1	1	1	T17	<del>                                     </del>	1	+	<del>                                     </del>	}	1	1	-	<del>                                     </del>	+
		VCCINT	<del>                                     </del>	1	1	-	1		1	ļ	1	1		1	l		<b>.</b>	+
		VCCINT			1	-	<u> </u>	T19	<b></b>									
		VCCINT			1		<u> </u>	U10										
		VCCINT						U12										
		VCCINT						U14										
		VCCINT						U16										
		VCCINT						U18										1
	1	VCCINT	<del> </del>	<del> </del>	1		1	V11	<del> </del>	<b> </b>	<del> </del>	<del> </del>	1	1	1		<del> </del>	<del>1</del>
	1	VCCINT	<b>†</b>	<b>†</b>	<del>                                     </del>		<del>                                     </del>	V15	t	<b> </b>	<b>†</b>	t	<b> </b>				<b>†</b>	+
			<del> </del>	-	+	$\vdash$	<del>                                     </del>		<del>                                     </del>		<del> </del>	<del>                                     </del>	1	-		-	<del>                                     </del>	+
	1	VCCINT	<del>                                     </del>	1	1	-	1	V17	1	ļ	1	1		1	l		1	+
		VCCINT	<b></b>		1	<u> </u>	ļ	V19	<b></b>		L	<b></b>					<b></b>	4
		VCCINT					<u> </u>	V13										
		VCCINT			<u> </u>		<u></u>	W12										
		VCCINT						W14										
		VCCINT						W18										1
		VCCIO1	1			F4	D4	B1	1		1	1					1	<b>†</b>
	<b>-</b>	VCCIO1			1	G4	F4	H1										+
	<del>                                     </del>		<del>                                     </del>	+	1	J4			<del>                                     </del>	1	+	<del>                                     </del>	}	1	1	-	<del>                                     </del>	+
	-	VCCIO1	<del>                                     </del>	<del>                                     </del>	1	J4	K4	K5	<del>                                     </del>	-	<del>                                     </del>	<del>                                     </del>	<b> </b>	1	-		<del>                                     </del>	+
		VCCIO1	L		<u> </u>	-	H4	K8	L		L	L					L	<del>  </del>
	1	VCCIO1		L	<u> </u>		<u></u>	N1	<u> </u>		<u> </u>	<u> </u>	<u> </u>			<u></u>	<u> </u>	1

Version 1.3

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	NOTES
																		(4), (5), (6)
		1/00/04						NE										
		VCCIO1 VCCIO2				K4	N4	N5 AA1										+
		VCCIO2					U4	AG1										+
		VCCIO2					W4	T1										1
		VCCIO2					R4	T5										
		VCCIO2						W7										
		VCCIO2						W5										
		VCCIO3				R6	AB2	AA11										
		VCCIO3					W5	AD6										
		VCCIO3				R9	W9 W11	AD9 AD13										+
		VCCIO3					AA6	AH2										
		VCCIO3					7010	AH5										+
		VCCIO3						AH9										
		VCCIO3						AH13										1
		VCCIO3						AB10										
		VCCIO4					AB21	AA18										
		VCCIO4	1		<u> </u>	R12		AD16										<del>                                     </del>
<b>—</b>		VCCIO4 VCCIO4	<b> </b>		<del>                                     </del>	R14	W16 W18	AD20 AD23										+
		VCCIO4 VCCIO4	<u> </u>		<del>                                     </del>		Y14	AH16										+
		VCCIO4	1		l			AH20										+
		VCCIO4	1		1			AH24				İ						1
		VCCIO4						AH27										
		VCCIO4						Y16										
		VCCIO5				K15		AA28										
		VCCIO5				M15		AG28										
		VCCIO5				R15		T24										4
		VCCIO5 VCCIO5					T19	T28 U21										+
		VCCIO5						W24										+
		VCCIO6				F16	E19	B28										+
		VCCIO6				G15		H28										
		VCCIO6				J15		K24										
		VCCIO6					J20	L21										
		VCCIO6						N24										
		VCCIO6				D44	404	N28										4
		VCCIO7 VCCIO7				D11 D13	A21	A16 A20										+
		VCCIO7				D15		A24										+
		VCCIO7				D10	D16	A27										+
		VCCIO7					D18	E16										
		VCCIO7						E20										
		VCCIO7						E23										
		VCCIO7	<u> </u>		<u> </u>			H18										1
		VCCIO7	1		<u> </u>	D.4	40	J15										+
		VCCIO8	1				A2	A2										
-		VCCIO8 VCCIO8	1		<del>                                     </del>		D5 D9	A5 A9										+
		VCCIO8	1		<b>†</b>	20	D11	A13										
		VCCIO8	1		1		E8	E6										1
		VCCIO8			L			E9										
		VCCIO8						E13										
		VCCIO8						H11										
		VCCIO8	1		<u> </u>			J13										
		GND			<del>                                     </del>	G9	L10	K10										+
		GND GND	1			H9 H8	L11 M10	K12 K14										+
		GND	1				M11	K14 K18										+
		GND			<b>†</b>	J9	L12	K20										<b>†</b>
		GND	İ				L13	L11										1
		GND					M12	L15										
		GND					M13	L17										
		GND			<u> </u>	J11		L19										<u> </u>
	l	GND			1	K11	K11	L9	1	1		J	]		l	<u> </u>		1

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Bank Number	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
	GND						M10										+
	GND GND				K9 K8	K12 K13	M12 M14										+
	GND				L8	N13	M16										+
	GND				L9	N10	M18										+
	GND				L10	K10	N11										
	GND				M10	J9	N13										
	GND					F12	N15										
	GND				F11	H12	N17										
	GND GND				F13 F7	H13 J15	N19										
	GND	1			F7	K16	P10 P12										+
	GND				G6	L15	P14										+
	GND	1				N15	P16										1
	GND					R13	P18										
	GND					R11	P20										
	GND	1			N6	R9	R11									ļ	1
	GND	-			N8	P8	R13		ļ						ļ	-	<u> </u>
	GND GND	1		1		1	R15 R17	-								-	+
	GND	+		1		1	R17	1	1		1		<del> </del>	<del> </del>		+	+
<b>-</b>	GND	+	1	<del>                                     </del>		+	R19	<del> </del>	<b>†</b>		+		<del> </del>	<del>                                     </del>	<b>†</b>	+	+
	GND	1		1		1	T10	1	1		1		1	1	1	1	†
	GND						T12										1
	GND						T14										
	GND						T16										
	GND						T18										
	GND						U11										
	GND GND						U13 U15										+
	GND	1					U17										+
	GND						U19										
	GND						V10										1
	GND						V12										
	GND						V14										
	GND	<u> </u>					V18										
	GND						W11										
	GND GND						W15 W17										+
	GND	1					W19										+
	GND				C15	A1	AA2										+
	GND					C5	AA27										1
	GND					C9	AC6										
	GND	1			C8	C11	AC9				1					1	1
	GND				C6	C12	AC13										1
	GND	1			C4	C14	AC16							ļ		1	+
<b> </b>	GND GND	+	1		E3 G3	C16 A22	AC20 AC23	<del>                                     </del>	<del> </del>		<del>                                     </del>	-	<del>                                     </del>	<del>                                     </del>	<del> </del>	+	+
<del>                                     </del>	GND	1	1		J3	E20	AC23 AF1	1	1		1		<del> </del>	<del>                                     </del>	1	1	+
<b> </b>	GND	<del>                                     </del>			лз К3	G20	AF28	<del> </del>	<b>†</b>		<del> </del>		<del> </del>	<b> </b>	<u> </u>	<del> </del>	†
	GND	1			N3	L20	AG2	1	1		1		1	1	1	1	†
	GND				P3	P19	AG5										1
	GND				T5	V20	AG9										
	GND	ļ			T7	Y20	AG13	ļ			1		ļ	ļ		1	ļ
	GND	<b>_</b>	-		T9	AB22	AG16		<b></b>		<b></b>		ļ		ļ		<del>                                     </del>
	GND	+			T10	Y18	AG20	1	1		1		<del>                                     </del>	<del>                                     </del>	1	+	+
	GND GND	+	+	-		Y16 Y12	AG24 AG27	-	<b>+</b>		-		-	-	<b> </b>	+	+
	GND	1	1	1		Y12 Y11	B2	1	1		1		<del> </del>	<del>                                     </del>	1	1	+
	GND	1				Y9	B5	+			+		<b>+</b>	<b>+</b>		+	+
	GND	1				Y5	B9	1	1		1		1	1	1	1	†
	GND					AB1	B13										1
	GND				G16	N3	B16										
	GND				E16	U3	B20										
	GND	1				W3	B24						1	1			



Bank	VREFB	Pin Name /	Ontional	Configuration	Q24n	F324	F484 /	F780	DQS for X8/X9 in	DQS for X8/X9 in	DOS for X16/X18 in	DQS for X8/X9 in	DOS for X16/X18 in	DOS for X32/X36 in	DQS for X8/X9 in	DQS for X16/X18	DOS for X32/Y36	IPKG
Number		Function	Function(s)	Function	Q240	. 324	11484	1.750	O240	F324	F324	F484/11484	DQS for X16/X18 in F484/U484	F484/11484	F780	in F780	in F780	NOTES
Number	Group	unction	i unction(s)	i unction			0404		Q240	1 324	1 324	1 404/0404	1 404/0404	1 404/0404	1700		111 700	(4), (5), (6)
																		( .), (0), (0)
	1	OND					D0	D07				-						+
	1	GND					D3	B27				-						
		GND			-		F3	C1										
	1	GND					K3	C28				-						
		GND			-		H3 R3	F6 F9										+
	1	GND										-						+
		GND			-		AB6	F13										+
		GND			-		Y15	F16										+
		GND					T20	F20										4
		GND			-		J19	F23										+
		GND					C18	H2										
		GND					D8	H27										
		GND						J11										
		GND					<u> </u>	J18										
		GND						K6										
		GND						K16										
		GND						K23										
		GND						L13										
		GND						M20										
		GND						N2										
		GND						N6										
		GND						N9										
		GND						N23										
		GND						N27										
		GND						T2										
		GND						T6										
		GND						T20										
		GND						T23										
		GND						T27										
		GND						U9										
		GND						V16										
		GND						W6										
		GND						W13										
		GND						W23										
		GND						Y11										
		GND						Y18										

## Notes:

- (1) Q240 in the EP3C40 device does not have the MSEL[3] pin and does not support the Active Parallel (AP) configuration mode.
  (2) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
- (3) If dedicated CLK pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the core logic.
- (4) "Adj." in PKG NOTE denotes the dedicated differential output drivers with p and n pins located adjacent to each other.
- (5) "Sep." in PKG NOTE denotes the dedicated differential output drivers with p and n pins not located adjacent to each other.
- (6) "Res." in PKG NOTE denotes differential output drivers that require external resistor network.



Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
		is the responsibility of the designer to apply simulation results to the design to verify p	
Prior provides these guidennes only a	o recommendations. It	Supply and Reference Pins	Topor device functionality.
			All VCCINT pins must be connected to 1.2V supply. Decoupling depends on the design decoupling
VCCINT	Power	These are internal logic array voltage supply pins.	requirements of the specific board. See Note (8)
		These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage	
		level. VCCIO supplies power to the input and output buffers for all I/O standards. VCCIO powers up the JTAG pins (TCK, TMS, TDI and TDO) and the following configuration pins: nCONFIG, DCLK,	
VCCIO[18]	Power	DATA[15.0], nCE, nCEO, nWE, nRESET, nOE, FLASH_nCE, nCSO and CLKUSR.	Decoupling depends on the design decoupling requirements of the specific board. See <i>Note</i> (8)
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.	All GND pins should be connected to the board GND plane.
		Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then	If VREF pins are not used, the designer should connect them to either the VCCIO in the bank in which the pin
		these pins are used as the voltage-referenced pins for the bank. If voltage-referenced I/O standards	resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note
VREFB[18]N[03] (Note 2)	1/0	are not used in the bank, the VREF pins are available as user I/O pins.	(8)
			The designer must connect these pins to 2.5V, even if the PLL is not used. These pins must be powered up
VCCA[14] (Note 3)	Power	Supply (analog) voltage for PLLs[14] and other analog circuits in the device.	and powered down at the same time. Connect VCCA[14] pins together. VCCA supply to the chip should be isolated. See <i>Note(9)</i> for details. See <i>Note(10)</i> for recommended decoupling.
VOCA[1+] (Note 3)	rowei	Supply (analog) voltage for 1 ELS[14] and other analog circuits in the device.	The designer must connect these pins to 1.2V, even if the PLL is not used.Connect VCCD PLL[14] pins
1			together. VCCD_PLL supply to the chip should be isolated. See <i>Note(9)</i> for details. See <i>Note (11)</i> for
VCCD_PLL[14] (Note 3)	Power	Supply (digital) voltage for PLLs[14].	recommended decoupling.
		Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5 and 7. The external precision	
		resistor Rup must be connected to the designated RUP pin within the same bank. If not required, this	When the device does not use this dedicated input for the external precision resistor or as an I/O, the pin can
RUP[14]	I/O, Input	pin is a regular I/O pin.	be connected to VCCIO of the bank in which the RUP pin resides or GND.
		Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5 and 7. The external precision resistor Rdn must be connected to the designated RDN pin within the same bank. If not required, this	When the device does not use this dedicated input for the external precision resistor or as an I/O, it is
RDN[14]	I/O, Input	pin is a regular I/O pin.	recommended that the pin be connected to GND.
GNDA[14] (Note 3)	Ground	Ground for PLL[14]. You can connect these pins to GND plane on the board.	The designer should connect these pins to an isolated analog ground plane on the board.
NC	No Connect	Do not drive signals into these pins.	Do not connect these pins to any signal.
	<del>.</del>	Dedicated Configuration/JTAG Pins	•
		Dedicated configuration clock pin. In PS and PP configuration modes, DCLK is used to clock	DCLK should not be left floating. In JTAG configuration and schemes that use an external host, designer should
DCLK	Input (PS, FPP) Output (AS, AP)	configuration data from an external source into the Cyclone III device. In AS and AP modes, DCLK is an output from the Cyclone III device that provides timing for the configuration interface.	drive it high or low, whichever is more convenient on the board. In AS and AP mode, the DCLK has an internal pull-up resistor(typically $25-k\Omega$ ) that is always active.
DCLK	Output (AS, AP)		pull-up resistor(typically 25-k12) that is always active.
		Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active.	
		After AS configuration, DATA0 is a dedicated input pin with optional user control. After PS or PP	
	Input (PS, FPP, AS)	configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the Dual-	If you are using a serial configuration device in AS configuration mode, you must connect a 25- Ω series resistor
	Bidirectional open drain	Purpose Pin settings. After AP configuration, DATA0 is a dedicated bidirectional pin with optional user	at the near end of the serial configuration device for the DATA[0]. If DATA[0] is not used, it should be driven
DATA0	(AP)	control.	high or low, whichever is more convenient on the board.
		Configuration input nine that get the Cyclene III device configuration scheme. These nine must be	These pins are internally connected to $5-k\Omega$ resistor to GND. Do not leave these pins floating. When these pins
		Configuration input pins that set the Cyclone III device configuration scheme. These pins must be hardwired to VCCA or GND. Some of the smaller devices or package options do not support the AP	are unused connect them to GND. Depending on the configuration scheme used, these pins should be tied to VCCA or GND. Refer to Chapter 10 of Cyclone III Handbook: Configuring Cyclone III Devices. If only JTAG
MSEL[30]	Input	flash programming and do not have the MSEL[3] pin.	configuration is used, then connect these pins to GND.
	7	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next
nCE	Input	device is disabled.	device in the chain. In single device configuration and JTAG programming, nCE is tied low.
		Dedicated configuration control input. Pulling this pin low during user mode causes the FPGA to lose	
		its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high	If you are using PS configuration scheme with a download cable, connect this pin through a 10-k Ω resistor to
nCONFIG	Input	level will initiate reconfiguration. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.	VCCA. For other configuration schemes, if this pin is not used, this pin must be connected directly or through a 10-kΩ resistor to VCCIO.
IICONFIG	Прис	Circuity.	10-K12 TESISION TO VICCIO.
		This is a dedicated configuration status pin. As a status output, the CONF DONE pin drives low	
		before and during configuration. Once all configuration data is received without error and the	
	Bidirectional	initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after	This pin is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-k Ω pull-up
CONF_DONE	(open-drain)	all data is received. Then the device initializes and enters user mode.	resistor.
		This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-	
	Bidirectional	up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low	
nSTATUS	(open-drain)	by an external source during configuration or initialization.	This pin is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-k $\Omega$ pull-up resistor.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.	Connect this pin to a $1+k\Omega$ resistor to GND.
	<u> </u>		When interfacing with 2.5V/3.0V/3.3V configuration voltage standards, connect this pin through a 1-k $\Omega$ resistor
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.	to VCCA. Otherwise, connect this pin through a 1-k $\Omega$ resistor to VCCIO. See <i>Note</i> (4).
	l		When interfacing with 2.5V/3.0V/3.3V configuration voltage standards, connect this pin through a 1-k $\Omega$ resistor
TDI TDO	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.	to VCCA. Otherwise, connect this pin through a 1-k Ω resistor to VCCIO. See <i>Note</i> (4).
טטו	Output	Dedicated JTAG output pin.  Clock and PLL Pins	The JTAG circuitry can be disabled by leaving TDO unconnected.
CLK[0,2,4,6,9,11,13,15], DIFFCLK_[07]p		Dedicated global clock input pins that can also be used for the positive terminal inputs for differential	1
(Note 5)	Clock, Input	global clock input or user input pins.	Connect unused pins to GND. See Note (12).
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	T		Note (1) Version 1.5
Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
CLK[1,3,5,7,8,10,12,14], DIFFCLK_[07]n	ord Function)	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential	Connection Guidelines
(Note 5)	Clock, Input	global clock input or user input pins.	Connect unused pins to GND. See Note (12).
		I/O pins that be used as two single-ended clock output pins or one differential clock output pair. These	
PLL[14]_CLKOUT[p,n] (Note 3)	I/O, Output	pins can only use the differential I/O standard if it is being fed by a PLL output.	Connect unused pins to GND. See Note (12).
		Optional/Dual-Purpose Configuration Pins	T
nCEO	I/O, Output	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds a subsequent device's nCE pin and must be pulled high to VCCIO by an external $10-k\Omega$ pull-up resistor. During single device configuration and for the last device in multi-device configuration, this pin can be left floating or used as a user I/O after configuration.
		This pin functions as FLASH_nCE in AP mode, and nCSO in AS mode. This pin has an internal pull-up resistor that is always active.	
		nCSO: Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device.	Manual Civilian Control of Control of Civilian
FLASH_nCE, nCSO	I/O, Output	FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash.	When not programming the device in AS mode, nCSO is not used. Similarly, FLASH_nCE is not used when not programming the device in AP mode. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
		This pin functions as DATA1 in PS, FPP, and AP modes, and as ASDO in AS mode.	
		DATA1: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[70] or DATA[150] respectively. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings.  After AP configuration, DATA1 is a dedicated bidirectional pin with optional user control.	
DATA1, ASDO	Input (FPP) Output (AS) Bidirectional open-drain (AP)	ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.	When not programming the device in AS or AP mode, this pin is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
DATA[72]	Input (FPP) Bidirectional open-drain (AP)	Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[70] or DATA[150] respectively.  In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.  After FPP configuration, DATA[72] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.  After AP configuration, DATA[72] are dedicated bidirectional pins with optional user control.	When not programming the device in AP mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to leave these pins unconnected.
DATA[158]	Bidirectional open-drain (AP)	Data inputs. Btye-wide or word-wide configuration data is presented to the target device on DATA[15.0]. In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After AP configuration, DATA[15.8] are dedicated bidirectional pins with optional user control.	When not programming the device in AP mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to leave these pins unconnected.
PADD[230]	I/O, Output (AP)	24-bit address bus from the Cyclone III device to the parallel flash in AP mode.	When not programming the device in AP mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to leave these pins unconnected.
nRESET	I/O, Output (AP)	Active-low reset output. Driving the nRESET pin low resets the parallel flash.	When not programming the device in AP mode, nRESET is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nAVD	I/O, Output (AP)	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[230] address bus.	When not programming the device in AP mode, nRESET is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nOE	I/O, Output (AP)	Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[150] and RDY).	When not programming the device in AP mode, nOE is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nWE	I/O, Output (AP)	Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[15.0] bus is valid.	When not programming the device in AP mode, nWE is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
CRC ERROR	I/O, Output	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled. This pin can be set in Quartus ® II software to support open-drain output.	If open drain feature is used, connect this pin to VCCIO of Bank 1 through a 10-k $\Omega$ resistor. When the output fo CRC_ERROR is not used and this pin is not used as an I/O then it is recommended to leave the pin unconnected.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations.	When the input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to VCCIO or GND



Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
DEV_OE	I/O (when option off),	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.	
INIT_DONE		This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.	Connect this pin to a 10-k $\Omega$ resistor to VCCIO.
CLKUSR		Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to GND.
		Dual-Purpose Differential and External Memory Interface Pin	S
DIFFIO_[L,R,T,B][061][n,p] (Note 6)	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).
DQS[05][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCL K[011] ( <i>Note 7</i> )		signals such as clocks, asynchronous clears, presets, and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).
DQS[05][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPC LK[07] (Note 7)		Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before being driven into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).
DQ[05][L,R,T,B] (Note 7)	I/O, DQ	Optional data signal for use in external memory interfaces.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).
		The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).

### Notes

- (1) This pin connection guideline is created based on the largest Cyclone III device (EP3C120F780).
- (2) EP3C5 and EP3C10 only have VREFB[1..8]N0.
- (3) EP3C5 and EP3C10 only have PLL(1 & 2). EP3C16 and other larger densities have PLL (1,2,3 & 4).
- (4) You must follow specific requirements when interfacing Cyclone III devices with 2.5V/3.0V/3.3V configuration voltage standards. All I/O inputs must maintain a maximum AC voltage of 4.1V. Refer to Configuration and JTAG Pin I/O Requirements of Chapter 10 in Cyclone III Handbook: Configuring Cyclone III Devices.
- (5) The number of dedicated global clocks for each device density is different. EP3C5 and EP3C10 support four dedicated clock pins on the left and right sides of the device, that can drive a total of 10 global clock networks. EP3C16 and other larger densities support four dedicated clock pins on each side of the device that can drive a total of 20 global clock networks.
- (6) The differential TX/RX channels for each device density and package is different. Please refer to the Cyclone III Handbook Chapter 8: High-Speed Differential Interfaces in Cyclone III Devices.
- (7) For details on the DQ and DQS bus modes support in different device densities, refer to the Cyclone III Handbook Chapter 9: External Memory Interfaces in Cyclone III Devices.
- (8) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling.
- (9) Use a power island for VCCA and VCCD\_PLL. PLL power supply may originate from another plane on the board but must be isolated using a ferrite bead or other equivalent methods. If using a ferrite bead, choose an 0402 package with low DC resistance, higher current rating than the maximum steady state current for the supply it is connected to (VCCA or VCCD\_PLL) and high impedance at 100MHz.
- (10) Decouple VCCA power island with a parallel combination of 1x47uF, 1x4.7uF, 1x0.1uF, 1x0.022uF, 1x0.01uF, 1x0.0047uF, 2x0.022uF, 1x0.001uF. Use 0402 package for 0.1uF and smaller capacitors for lower mounting inductance. Place 0.1uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20mV ripple voltage was used in the analysis for VCCA decoupling. Refer to the figure on "VCCA&VCCD Decoupling" worksheet for decoupling capacitor placement guidelines. The figure on "VCCA&VCCD Decoupling" worksheet depicts symbolic representation of decoupling scheme and not the exact layout.
- (11) Decouple VCCD\_PLL power island with a parallel combination of 1x470uF(low ESR Tantalum), 1x4.7uF, 5x0.1uF, 2x0.01uF, 1x0.0047uF, 1x0.0022uF. Use 0402 package for 0.1uF and smaller capacitors for lower mounting inductance. Place 0.1uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on itter, a 20mV ripple voltage was used in the analysis for VCCD\_PLL decoupling.Refer to the figure on "VCCA&VCCD\_Decoupling" worksheet for decoupling capacitor placement quidelines.

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Pin Information for the Cyclone® III EP3C40 Device

Note (1) Version 1.3

Pin Name

Pin Type (1st, 2nd, and 3rd Function)

Pin Description

Connection Guidelines

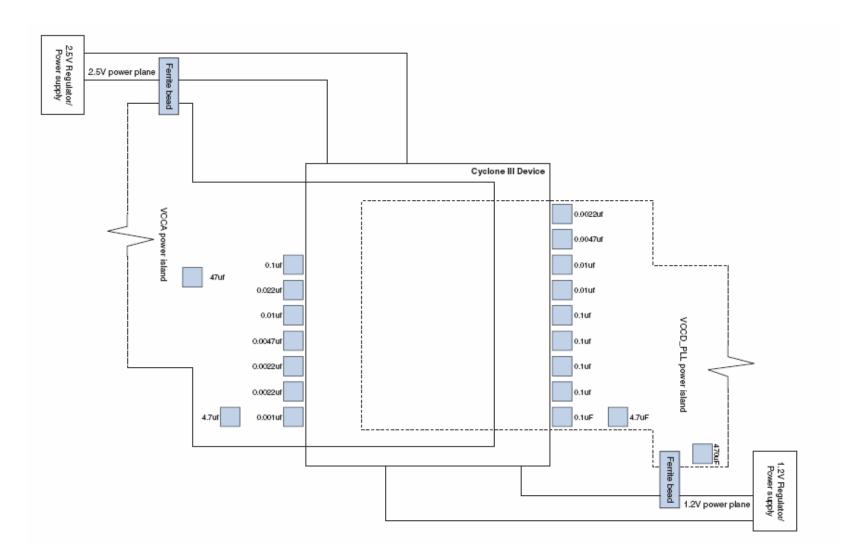
The figure on "VCCA&VCCD Decoupling" worksheet depicts symbolic representation of decoupling scheme and not the exact layout.

(12) The unused pins must be connected as specified in the Quartus II software settings. The default Quartus II setting for unused pins is 'As inputs tri-stated with weak pull-up resistors'. To change the setting, go to 'Assignments', then 'Device'. Click on 'Device & Pin options' dialog box and go to 'Unused Pins' tab. You may choose the desired setting from the 'Reserve all unused pins' drop down list.

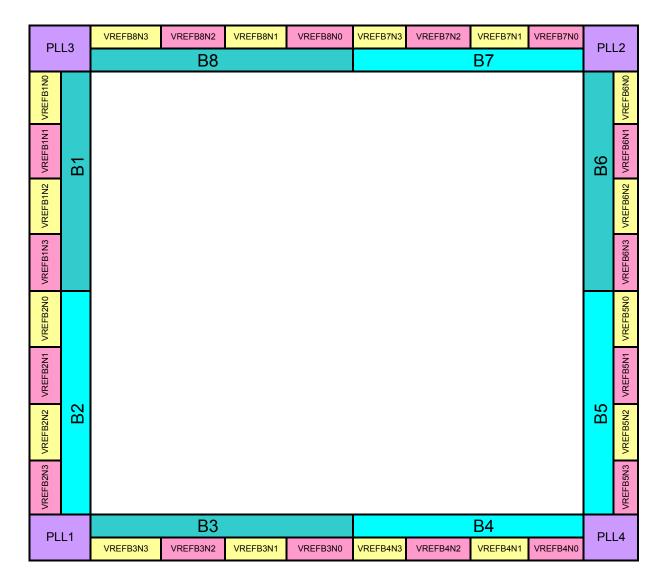
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# Pin Information for the Cyclone® III EP3C40 Device Version 1.3







## Notes:

- 1. This is a top view of the silicon die.
- 2. This is only a pictorial representation to get an idea of placement on the device. Refer to the pin list and the Quartus<sup>®</sup> II software for exact locations.



# Pin Information for the Cyclone<sup>®</sup> III EP3C40 Device Version 1.3

Version Number	Date	Changes Made
1.0	9/7/2007	Initial release.
1.1	1/4/2008	Updated Note(2) in Pin List.
		■ Updated pin function for CRC_ERROR pin.
		■ Updated DQ/DQS support for UBGA package.
		■ Updated pin function for PLL[14]_CLKOUT[p,n] pin.
		■ Remove RDY from pin list and pin definitions.
		■ Incorporated pin connection guideline into Pin Definitions worksheet.
1.2	5/23/2008	■ Incorporated VCCA and VCCD Decoupling recommendations.
1.3		