REFERENCE DESIGN

PCIE SINGLE LANE 1000/100/10 BASE-T

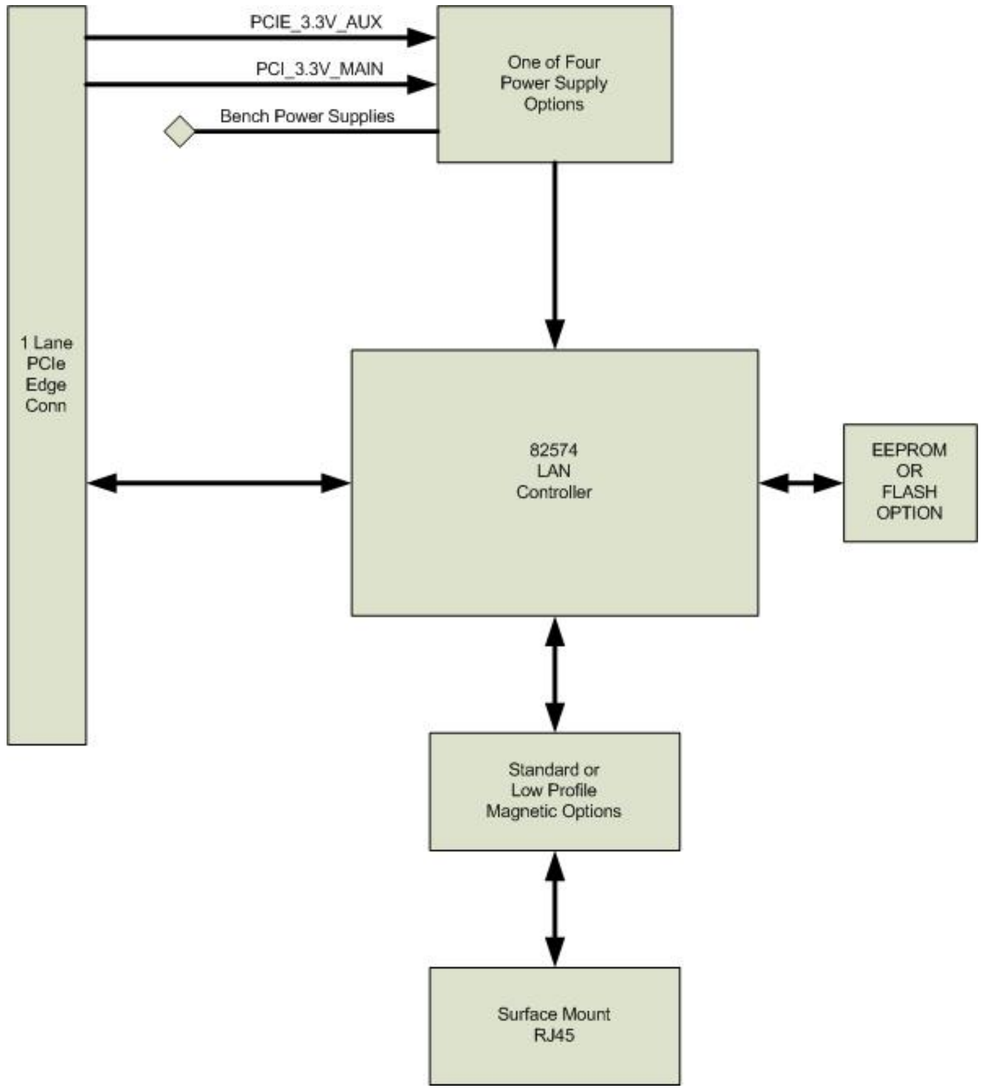
INTEL 82574 ETHERNET CONTROLER

INTEL

LAN ACCESS DIVISION
2111 N.E. 25th AVENUE
HILLSBORO, OR 97124

TITLE	SIZE	CODE	DOCUMENT NUMBER	REV	DATE	SHEET
82574 REFERENCE DESIGN				2.1	08-04-2008	1

FUNCTIONAL BLOCK DIAGRAM

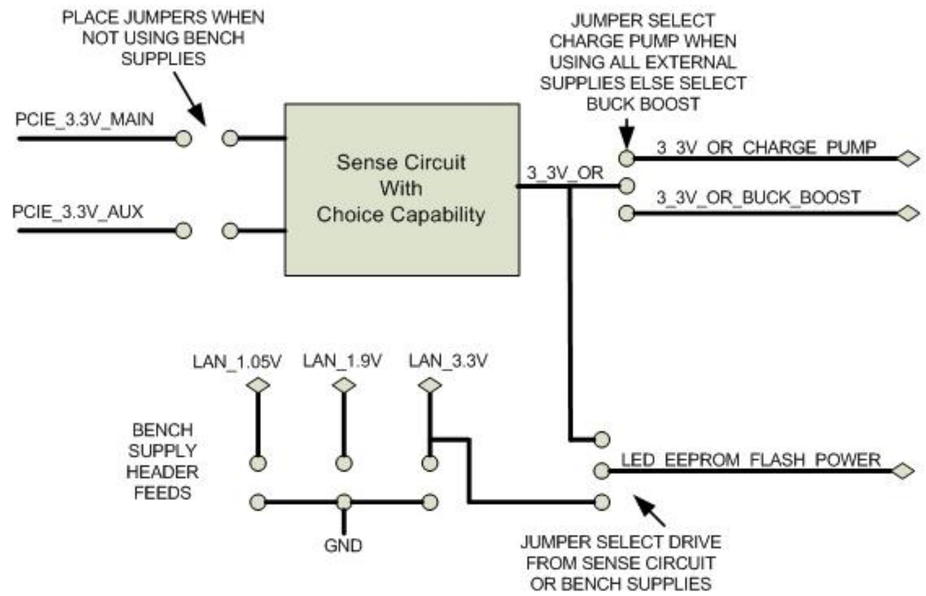


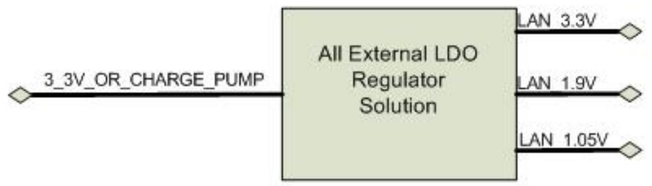
INTEL

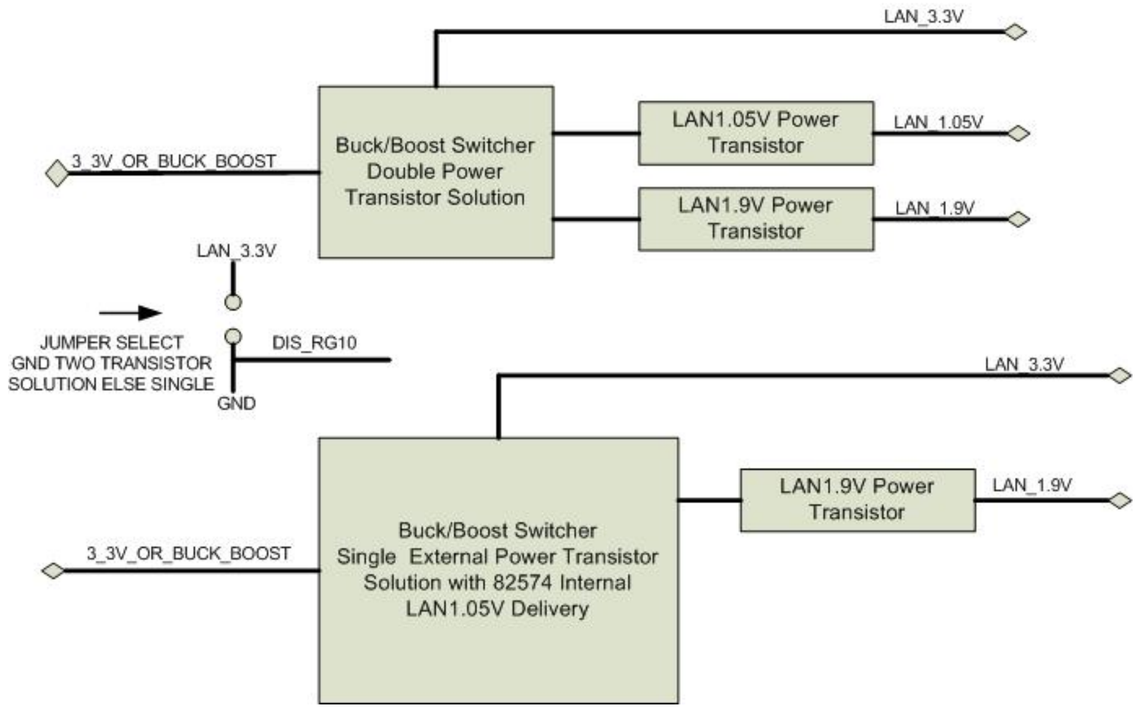
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 2

POWER BLOCK DIAGRAM

JUMPER_TABLE ON_SHEET_08







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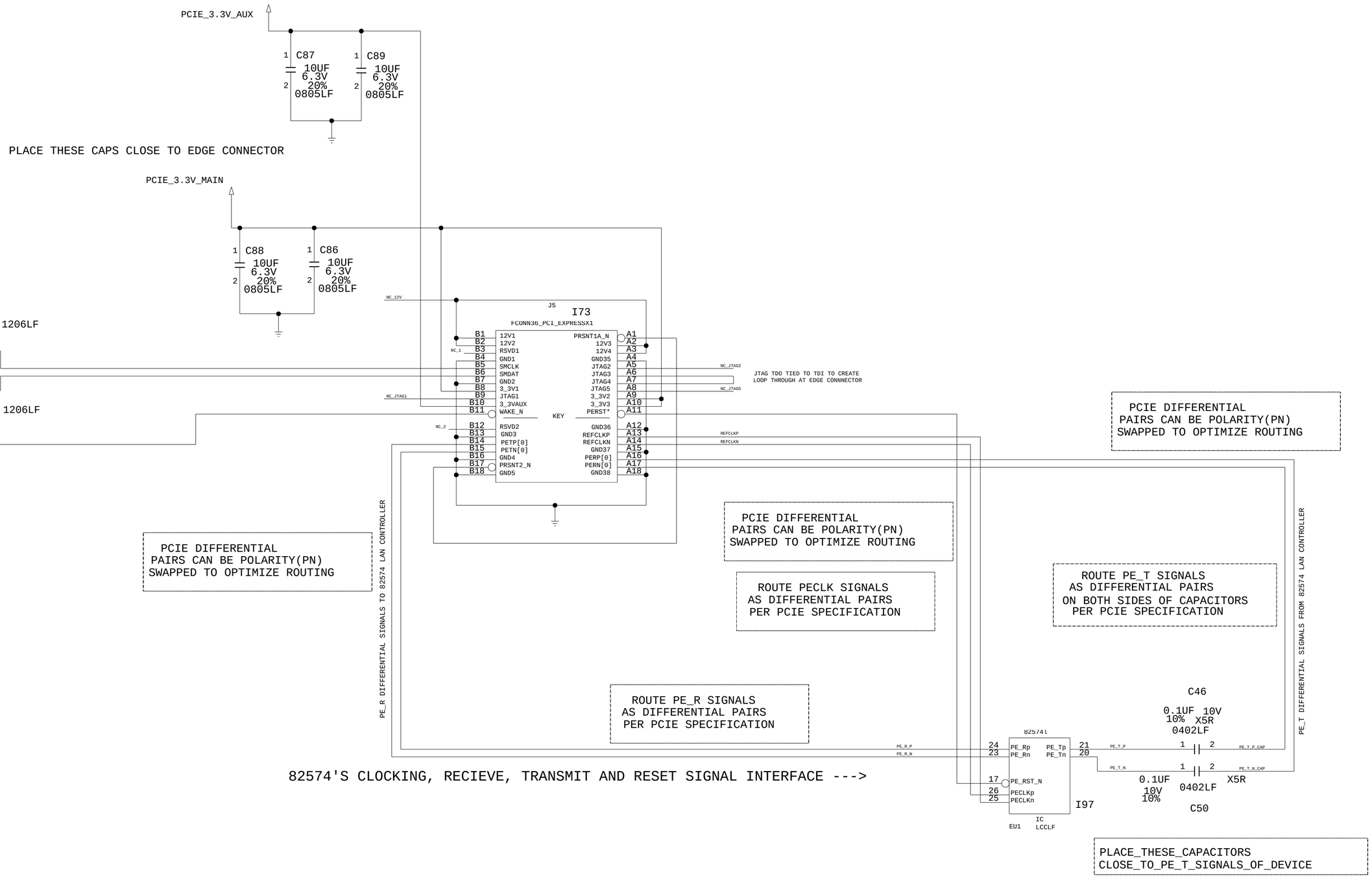
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 3

PCIE X1 LANE EDGE CONNECTOR WITH 82574'S CLOCKING, RECV, XMIT AND RESET SIGNAL INTERFACE



82574'S CLOCKING, RECIEVE, TRANSMIT AND RESET SIGNAL INTERFACE --->

INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 4

82574'S NC_SI AND MULIPLEXED TEST SIGNAL INTERFACE

LAN_3.3V

I73 THLF CONN J6 1 2

PLACE_JUMPER_PULL
HIGH_ENABLES_TEST_MODE

R27 1K 5% 1/10W CHIP 0603LF

I3

LAN_3.3V

R21 1K 5% 1/10W CHIP 0603LF

HIGH_SELECTS EEPROM

R16 DNP 0 1% 1/2W CHIP 1206LF

J21 CONN CONN3 1 2 3

LOW_SELECTS FLASH

R17 DNP 1% 0 1/2W CHIP 1206LF

R19 1K 1/10W CHIP 5% 0603LF

I51

LAN_3.3V

R201 5% 10K 1/10W CHIP 0603LF

R200 5% 10K 1/10W CHIP 0603LF

R12 5% 1K 1/10W CHIP 0603LF

I7

EU1 82574L

29	TEST_EN	
	PE_WAKE_N/JTAG_TDO	16
39	AUX_PWR/JTAG_TCK	
38	NVMT/JTAG_TMS	
40	JTAG_TDI	
2	NC_SI_CLK_IN	
3	NC_SI_CRS_DV	
6	NC_SI_RXD0	NC_SI_TXD0 9
5	NC_SI_RXD1	NC_SI_TXD1 8
7	NC_SI_TX_EN	

IC LCCLF

R205 0603LF 5% 33 1/10W CHIP

R202 5% 10K 1/10W CHIP 0603LF

R203 5% 10K 1/10W CHIP 0603LF

R204 5% 10K 1/10W CHIP 0603LF

I96

RESISTORS ON THE NC-SI INTERFACE PROTECT THE DEVICE
FROM NOISE AND SHOULD BE USED EVEN WHEN
NC-SI IS NOT USED

<----- 82574'S NC_SI INTERFACE, MULTIPLEXED TEST INTERFACE SIGNALS

LAN_3.3V

R49 5% 10K 1/10W CHIP 0603LF

R48 5% 10K 1/10W CHIP 0603LF

DNP

IMPLEMENTED IN HOST

LAN_3.3V

R11 10K 5% 1/10W CHIP 0603LF

PE_WAKE_N OUT 4D8<

J22 CONN CONN16

I77

NC_SI_RXD0
NC_SI_RXD1
NC_SI_CRS_DV
NC_SI_TXD0
NC_SI_TXD1
NC_SI_TX_EN
NC_SI_CLK_IN

R53 0 5% 1/16W CHIP 0603LF

I8

ROUTE THE NC_SI SIGNALS WITH A TRACE IMPEDIANCE
OF 50 OHMS PLUS 20% MINUS 10%
TRACE LENGTH OF 8 INCHES MAXIMUM

AUX_POWER SUPPORTED WHEN_PULLED_HIGH
TEST_NOT_ENABLED

LAN_3.3V

R13 10K 5% 1/10W CHIP 0603LF

J7 1 2 3 4 5

C10 0.1UF 16V 10% X7R 0603LF

C11 0.1UF 16V 10% X7R 0603LF

C12 0.1UF 16V 10% X7R 0603LF

C13 0.1UF 16V 10% X7R 0603LF

DNP POPULATE AS NEEDED
PLACE THESE CAPS CLOSE TO CONNECTOR

I24

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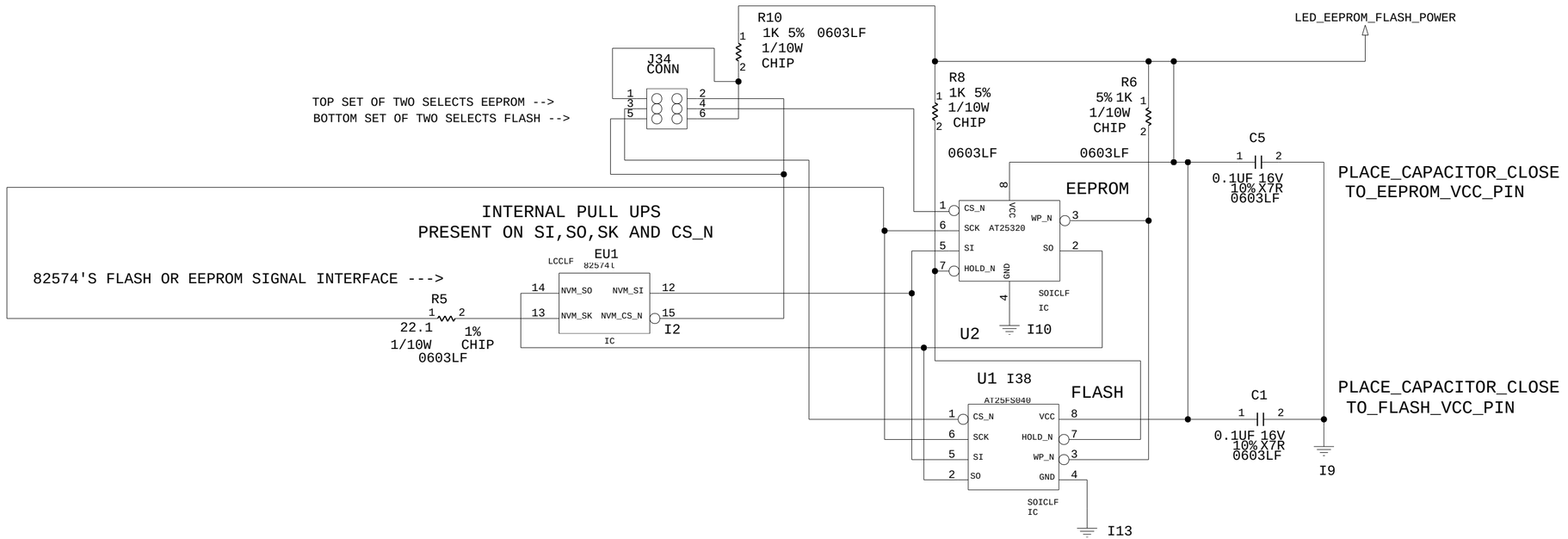
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 5

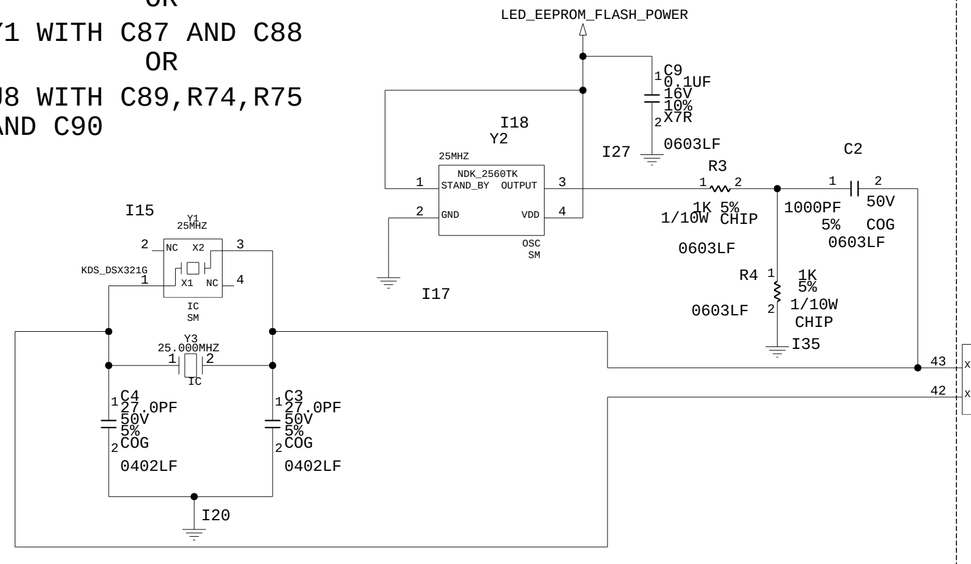
82574'S FLASH, EEPROM, XTAL AND LED SIGNAL INTERFACE



IMPORTANT!!

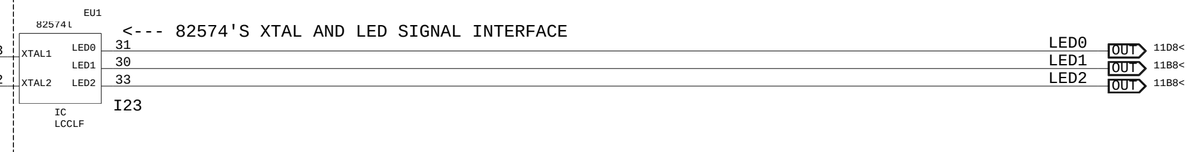
POPULATE ONLY ONE
OF THESE COMPONENT BLOCKS

Y2 WITH C87 AND C88
OR
Y1 WITH C87 AND C88
OR
U8 WITH C89,R74,R75
AND C90



PLACE R74,R75 AND C90 CLOSE
U8 MINIMIZING STUB LENGTHS
WHEN UNPOPULATED

PLACE C89 CLOSE TO U8'S VDD



INTEL LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 6

82574'S MDI,SMBUS,POWER AND REGULATION SIGNAL INTERFACE

ROUTE ALL MDI SIGNAL PAIRS ON ALL PAGES AS DIFFERENTIAL PAIRS
82574 HAS INTERNAL MDI TERMINATION; EXTERNAL TERMINATION MUST NOT BE USED

I2
EU1
82574L

MDI_PLUS(0) 58
MDI_MINUS(0) 57
MDI_PLUS(1) 55
MDI_MINUS(1) 54
MDI_PLUS(2) 53
MDI_MINUS(2) 52
MDI_PLUS(3) 50
MDI_MINUS(3) 49
RSET 48
SMB_DAT 36
SMB_CLK 34
SMB_ALRT_N 35
ATEST_P 45
ATEST_N 46
GND_PAD 65
IC LCCLF

<--- 82574'S MDI,SMBUS SIGNAL INTERFACE

PLACE THIS JUMPER CLOSE TO THE 82574

R23 4.99K 1% 1/10W CHIP 0603LF
I57

J24 THLF CONN
I136

LAN_3.3V
SM_BUS_CONNECTOR
R28 10K 5% 1/10W CHIP 0603LF
R25 10K 5% 1/10W CHIP 0603LF
J26 CONN3
R32 10K 5% 1/10W CHIP 0603LF
SMB_DAT
SMB_CLK

PLACE_0.1UF_CAPACITORS_CLOSE_TO_PIN_OF_DEVICE
PLACE_10.0UF_CAPACITOR_CLOSE_TO_POWER_PLANE_NEAR_DEVICE
LAN_1.05V
C15 10UF 6.3V 20% 0805LF
C64 C23 C45 C62 C37 C54 C22 0.1UF 16V 10% X7R 0603LF
I120

PLACE_0.1UF_CAPACITORS_CLOSE_TO_PIN_OF_DEVICE
PLACE_10.0UF_CAPACITOR_CLOSE_TO_POWER_PLANE_NEAR_DEVICE
LAN_3.3V
C60 10UF 6.3V 20% 0805LF
C30 C61 C63 0.1UF 16V 10% X7R 0603LF
I119

CTRL10 OUT 9B8<
CTRL19 OUT 9C8<

PLACE_JUMPER_PULL_HIGH
ENABLES_THE_82574L
PULL_DOWN_TO_DISABLE

I32
EU1
82574L

DEV_OFF_N 28
DIS_REG10 59
AVDD3p3/VDD3p3 1
VDD3p3 10
VDD3p3 32
VDD1p0 4 11 18 27 37 41 60
GND_PAD 65
CTRL10 62
CTRL19 64
AVDD1p9 22 44 47 51 56 61 63
VDD1p9 19
IC LCCLF
I5

<--- 82574'S POWER AND REGULATION SIGNAL INTERFACE

LAN_1.9V
R9 0 1% CHIP 1/2W 1206LF
I135
J25 THLF CONN
C16 10UF 6.3V 20% 0805LF
C48 C52 C39 C21 C20 C31 C43 0.1UF 16V 10% X7R 0603LF
I108

PLACE_0.1UF_CAPACITORS_CLOSE_TO_PIN_OF_DEVICE
PLACE_10.0UF_CAPACITOR_CLOSE_TO_POWER_PLANE_NEAR_DEVICE

C7 0.1UF 16V 10% X7R 0603LF
I138

LAN_3.3V
R20 1K 5% 1/10W CHIP 0603LF
I134 THLF CONN J23
I12

LAN_3.3V
I133 THLF CONN J20
R46 1K 5% 1/10W CHIP 0603LF
I20

PLACE_JUMPER_PULL_HIGH
DISABLES_INTERNAL_1_0V_REGULATOR
CTRL1_0_SIGNAL_ACTIVE
NO_JUMPER_CTRL1_0_INACTIVE
ENABLES_INTERNAL_1_0V_REGULATOR

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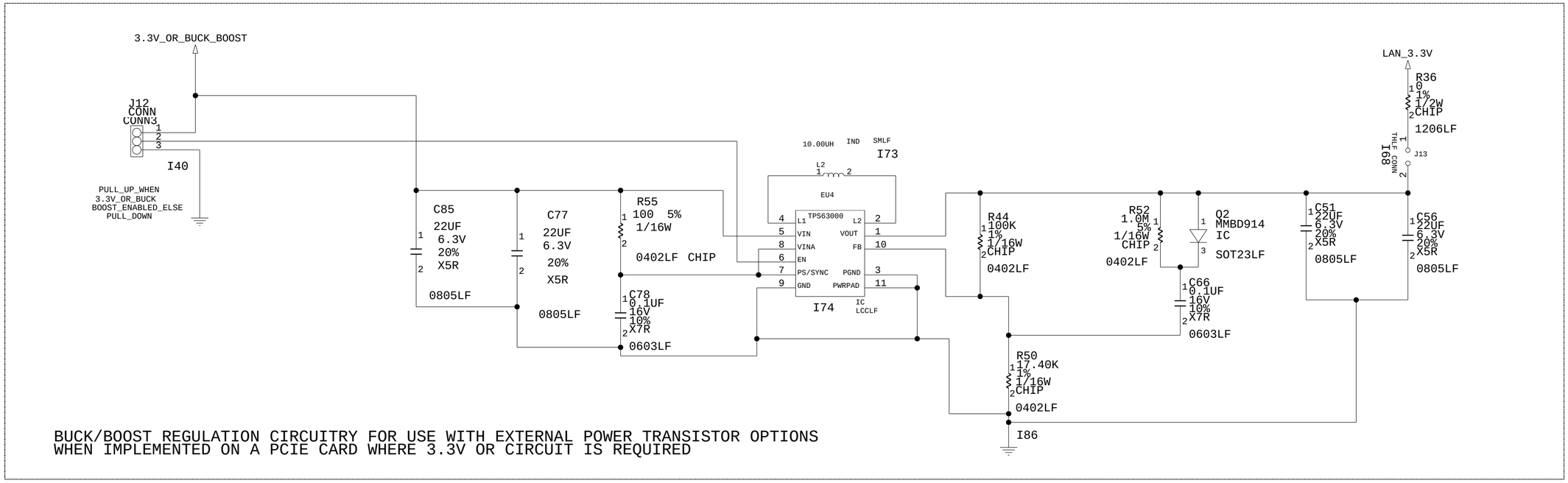
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 7

JUMPER TABLE
SET_JUMPERS_AS_LISTED_BELOW_TO_GENERATE DESIRED_CONFIGURATION

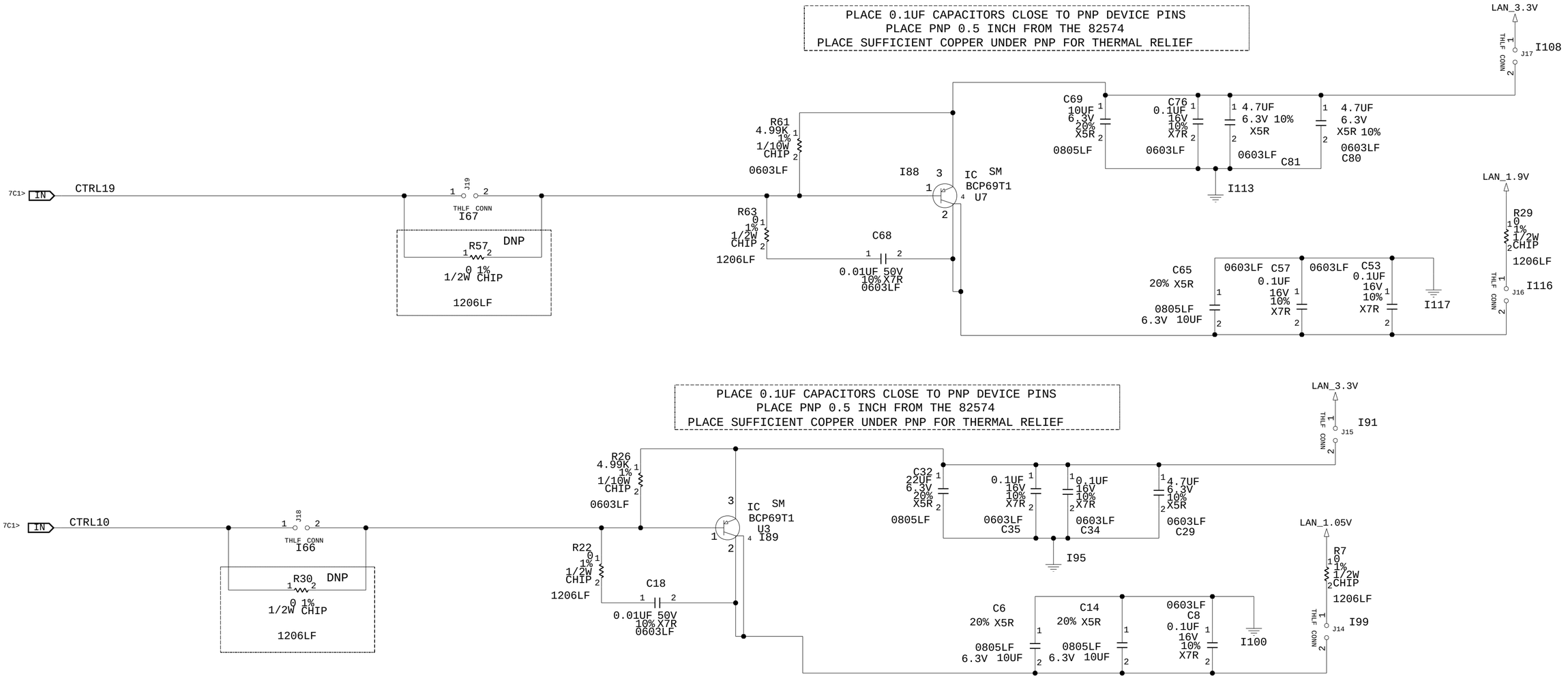
Jumper Number	Function	To Use Bench supplies	To Use Fully External LDO Supplies	To Use 2 External Power Transistors	To Use 1 External and 1 Internal Power Transistor
J1, 2 pin	PCIE_3.3V_MAIN	-	1-2	1-2	1-2
J2, 2 pin	PCIE_3.3V_AUX	-	1-2	1-2	1-2
J3, 3 pin	3.3V Charge Pump OR 3.3V Buck/Boost	-	1-2 (Select Charge Pump)	2-3 (Select Buck/Boost)	2-3 (Select Buck/Boost)
J4, 3 pin	LED_EEPROM_FLASH_POWER	1-2 (Select LAN_3.3V)	2-3 (Select 3_3V_OR)	2-3 (Select 3_3V_OR)	2-3 (Select 3_3V_OR)
J5	PCIe Connector	-	-	-	-
J6, 2 pin	TEST_EN	-	-	-	-
J7, 5 pin	JTAG	-	-	-	-
J8, 3 pin	CHARGE PUMP ENABLE	2-3 (Select GND)	1-2 (Select HIGH)	2-3 (Select GND)	2-3 (Select GND)
J9, 2 pin	3.3V CHARGE PUMP OUT	-	1-2	-	-
J10, 2 pin	1.9V LDO OUT	-	1-2	-	-
J11, 2 pin	1.05V LDO OUT	-	1-2	-	-
J12, 3 pin	BUCK/BOOST ENABLE	2-3 (Select GND)	2-3 (Select GND)	1-2 (Select HIGH)	1-2 (Select HIGH)
J13, 2 pin	BUCK/BOOST OUT	-	-	1-2	1-2
J14, 2 pin	1.05V PNP OUT	-	-	1-2	-
J15, 2 pin	1.05V PNP IN	-	-	1-2	-
J16, 2 pin	1.9V PNP OUT	-	-	1-2	1-2
J17, 2 pin	1.9V PNP IN	-	-	1-2	1-2
J18, 2 pin	CTRL10	-	-	1-2	-
J19, 2 pin	CTRL19	-	-	1-2	1-2
J20, 2 pin	DIS_REG10	1-2	1-2	1-2	-
J21, 3 pin	NVMT	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH	1-2=EEPROM 2-3=FLASH
J22, 16 pin	NC_SI	-	-	-	-
J23, 2 pin	DEV_OFF_N	-	-	-	-
J24, 2 pin	ATEST	-	-	-	-
J25, 2 pin	VDD1p9	-	-	-	-
J26, 3 pin	SMBUS	-	-	-	-
J27, 4 pin	3.3V Bench Feed	3.3V Bench Feed	-	-	-
J28, 4 pin	1.9V Bench Feed	1.9V Bench Feed	-	-	-
J29, 4 pin	1.05V Bench Feed	1.05V Bench Feed	-	-	-
J30, 3 pin	Center Tap Feed	-	-	-	-
J34, 6 pin	NVM Chip Select	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH	1-3, 2-4=EEPROM 3-5, 4-6=FLASH

82574'S 2 EXTERNAL OR 1 EXTERNAL POWER TRANSISTOR OPTIONS



BUCK/BOOST REGULATION CIRCUITRY FOR USE WITH EXTERNAL POWER TRANSISTOR OPTIONS
WHEN IMPLEMENTED ON A PCIE CARD WHERE 3.3V OR CIRCUIT IS REQUIRED

PLACE 0.1UF CAPACITORS CLOSE TO PNP DEVICE PINS
PLACE PNP 0.5 INCH FROM THE 82574
PLACE SUFFICIENT COPPER UNDER PNP FOR THERMAL RELIEF



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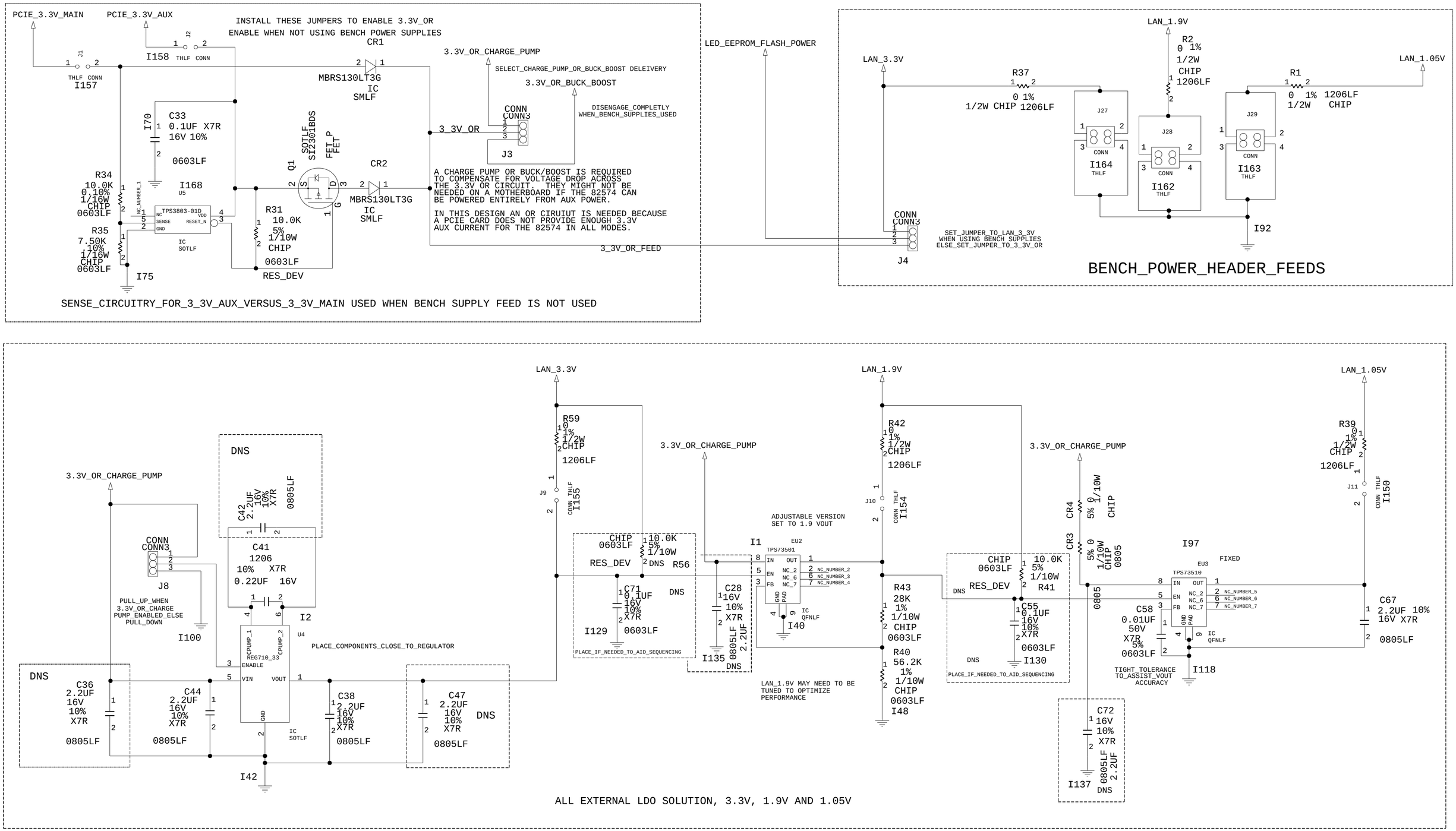
LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 9

82574'S BENCH OR ALL EXTERNAL LDO POWER SUPPLY OPTIONS



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LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 10

LAN PORT W/MAGNETIC OPTION

CENTER TAP POWER

IF MDI TRACES ARE LONGER THAN 4"
OR A LAN SWITCH IS USED:
AN ADDITIONAL POWER SUPPLY TO
BOOST THE CENTER TAP VOLTAGE
MAY BE REQUIRED

LAN_1.9V
R15 0 1% 1/2W CHIP 1206LF
J30 CONN CONN3
I294
C70 0.01UF 10% 25V 0402LF
C49 0.01UF 10% 25V 0402LF
C59 0.01UF 10% 25V 0402LF
C40 0.01UF 10% 25V 0402LF
I11

11D3<> 11C3<> BI CENTER_TAP_RIGHT_0
11D3<> 11C3<> BI CENTER_TAP_RIGHT_1
11D3<> 11C3<> BI CENTER_TAP_RIGHT_2
11D3<> 11C3<> BI CENTER_TAP_RIGHT_3

RES_DEV R33 75 5% 1/8W CHIP 0805LF
RES_DEV R38 75 5% 1/8W CHIP 0805LF
RES_DEV R45 75 5% 1/8W CHIP 0805LF
RES_DEV R51 75 5% 1/8W CHIP 0805LF

C74 1500PF 2000V 1808LF 10% X7R
C19 10UF 20% 6.3V 0805LF
C26 1000PF 50V 10% X7R 0603LF
C75 10UF 20% 6.3V 0805LF
C83 1000PF 50V 10% X7R 0603LF
I70
I54
DNP

TWO OPTIONS FOR MAGNETIC MODULES ON TOP OF EACH OTHER

STANDARD PROFILE MAGNETIC OPTION

L1

11F8<> 11C5<> 7E8<> BI MDI_PLUS(0)
11E8<> 11C5<> 7E8<> BI MDI_MINUS(0)
11E8<> 11C5<> 7E8<> BI MDI_PLUS(1)
11E8<> 11C5<> 7E8<> BI MDI_MINUS(1)
11E8<> 11C5<> 7E8<> BI MDI_PLUS(2)
11E8<> 11C5<> 7E8<> BI MDI_MINUS(2)
11E8<> 11C5<> 7E8<> BI MDI_PLUS(3)
11E8<> 11C5<> 7E8<> BI MDI_MINUS(3)

CENTER_TAP_RIGHT_0 BI 11C3<> 11F4<>
RJ_MDI_PLUS(0) BI 11B4<> 11C3<> 11F4<>
RJ_MDI_MINUS(0) BI 11B4<> 11C3<> 11F4<>
CENTER_TAP_RIGHT_1 BI 11C3<> 11F4<>
RJ_MDI_PLUS(1) BI 11B4<> 11C3<> 11F4<>
RJ_MDI_MINUS(1) BI 11B4<> 11C3<> 11F4<>
CENTER_TAP_RIGHT_2 BI 11C3<> 11F4<>
RJ_MDI_PLUS(2) BI 11B4<> 11C3<> 11F4<>
RJ_MDI_MINUS(2) BI 11B4<> 11C3<> 11E4<>
CENTER_TAP_RIGHT_3 BI 11C3<> 11F4<>
RJ_MDI_PLUS(3) BI 11B4<> 11C3<> 11E4<>
RJ_MDI_MINUS(3) BI 11B4<> 11C3<> 11E4<>

I245 XFMR IC

LOW PROFILE MAGNETIC OPTION

I242 U6

11F8<> 11D5<> 7E8<> BI MDI_PLUS(0)
11E8<> 11D5<> 7E8<> BI MDI_MINUS(0)
11E8<> 11D5<> 7E8<> BI MDI_PLUS(1)
11E8<> 11D5<> 7E8<> BI MDI_MINUS(1)
11E8<> 11D5<> 7E8<> BI MDI_PLUS(2)
11E8<> 11D5<> 7E8<> BI MDI_MINUS(2)
11E8<> 11D5<> 7E8<> BI MDI_PLUS(3)
11E8<> 11D5<> 7E8<> BI MDI_MINUS(3)

CENTER_TAP_RIGHT_0 BI 11D3<> 11F4<>
RJ_MDI_PLUS(0) BI 11B4<> 11D3<> 11F4<>
RJ_MDI_MINUS(0) BI 11B4<> 11D3<> 11F4<>
CENTER_TAP_RIGHT_1 BI 11D3<> 11F4<>
RJ_MDI_PLUS(1) BI 11B4<> 11D3<> 11F4<>
RJ_MDI_MINUS(1) BI 11B4<> 11D3<> 11F4<>
CENTER_TAP_RIGHT_2 BI 11D3<> 11F4<>
RJ_MDI_PLUS(2) BI 11B4<> 11D3<> 11F4<>
RJ_MDI_MINUS(2) BI 11B4<> 11D3<> 11E4<>
CENTER_TAP_RIGHT_3 BI 11D3<> 11F4<>
RJ_MDI_PLUS(3) BI 11B4<> 11D3<> 11E4<>
RJ_MDI_MINUS(3) BI 11B4<> 11D3<> 11E4<>

6B1> IN LED1
POPULATE ONE, NOT BOTH
CHOOSE TO SINK OR SOURCE
LED_EEPROM_FLASH_POWER
R18 330 5% 1/10W CHIP 0603LF
R14 DNP 0 5% 1/16W CHIP 0603LF
I213
R24 160 1/16W 5% 0402LF
SINGLE_LED_CATHODE OUT 11B4<
OUT 11B2<
SINGLE_LED_ANODE
C24 C25 C17 C27 0.1UF 10% 16V 0603LF
I61
I66

6B1> IN LED0
R62 160 1/16W 5% 0402LF
DUAL_LED_TOP OUT 11A4<
6B1> IN LED2
R54 160 1/16W 5% 0402LF
DUAL_LED_BOTTOM OUT 11A4<
C79 C84 C73 C82 0.1UF 10% 16V 0603LF
I47
I55

DS1 IC YELLOW
11C6> IN SINGLE_LED_CATHODE
SINGLE_LED_ANODE IN 11C6>

I292 J32 IO1 IO2 TH CONN

11F4<> 11D3<> 11C3<> BI RJ_MDI_PLUS(0)
11F4<> 11D3<> 11C3<> BI RJ_MDI_MINUS(0)
11F4<> 11D3<> 11C3<> BI RJ_MDI_PLUS(1)
11F4<> 11D3<> 11C3<> BI RJ_MDI_PLUS(2)
11E4<> 11D3<> 11C3<> BI RJ_MDI_PLUS(3)
11E4<> 11D3<> 11C3<> BI RJ_MDI_MINUS(3)
11E4<> 11D3<> 11C3<> BI RJ_MDI_MINUS(2)
11F4<> 11D3<> 11C3<> BI RJ_MDI_MINUS(1)

J31 SCONN8_623377023
PR1+ PR2+ PR1- PR3+ PR4+ PR4- PR3- PR2- SHIELD2 SHIELD1
CONN SM
I244
I220

DS2 IC GREEN/YELLOW
11B6> IN DUAL_LED_TOP
11B6> IN DUAL_LED_BOTTOM

LED_EEPROM_FLASH_POWER
R60 330 5% 1/10W CHIP 0603LF
R58 DNP 0 5% 1/16W CHIP 0603LF
I226

INTEL

LAN ACCESS DIVISION 2111 N.E. 25th AVENUE HILLSBORO, OR 97124	TITLE 82574 REFERENCE DESIGN	SIZE	CODE	DOCUMENT NUMBER	REV 2.1	DATE 08-04-2008	SHEET 11