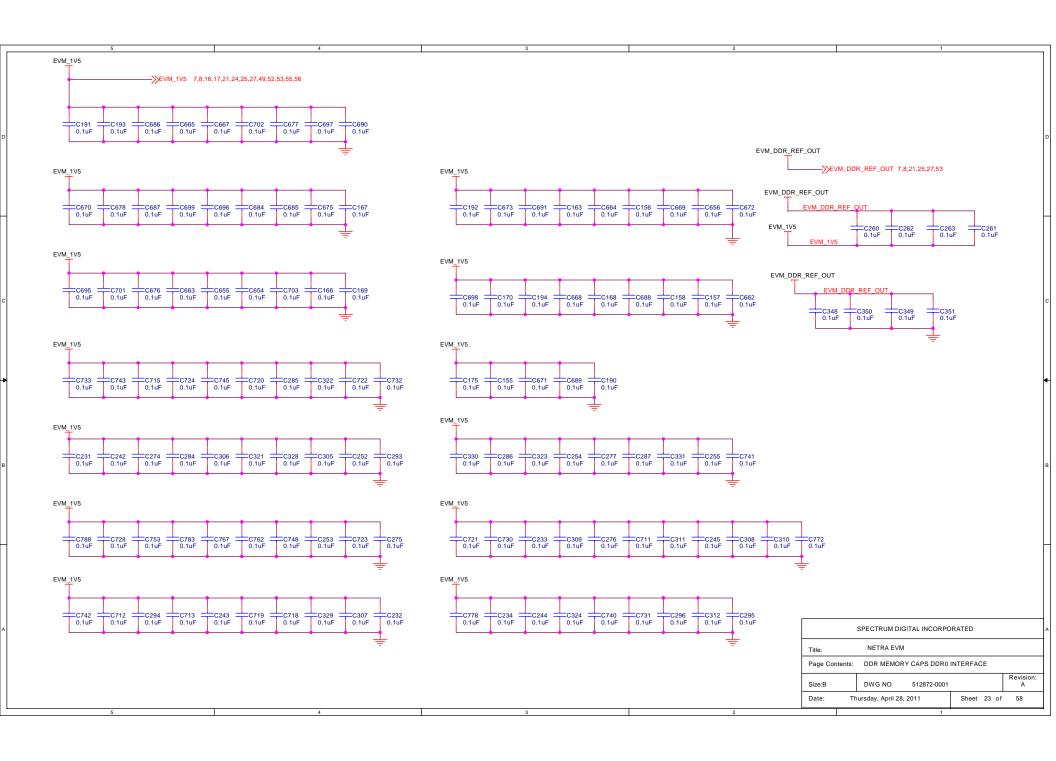
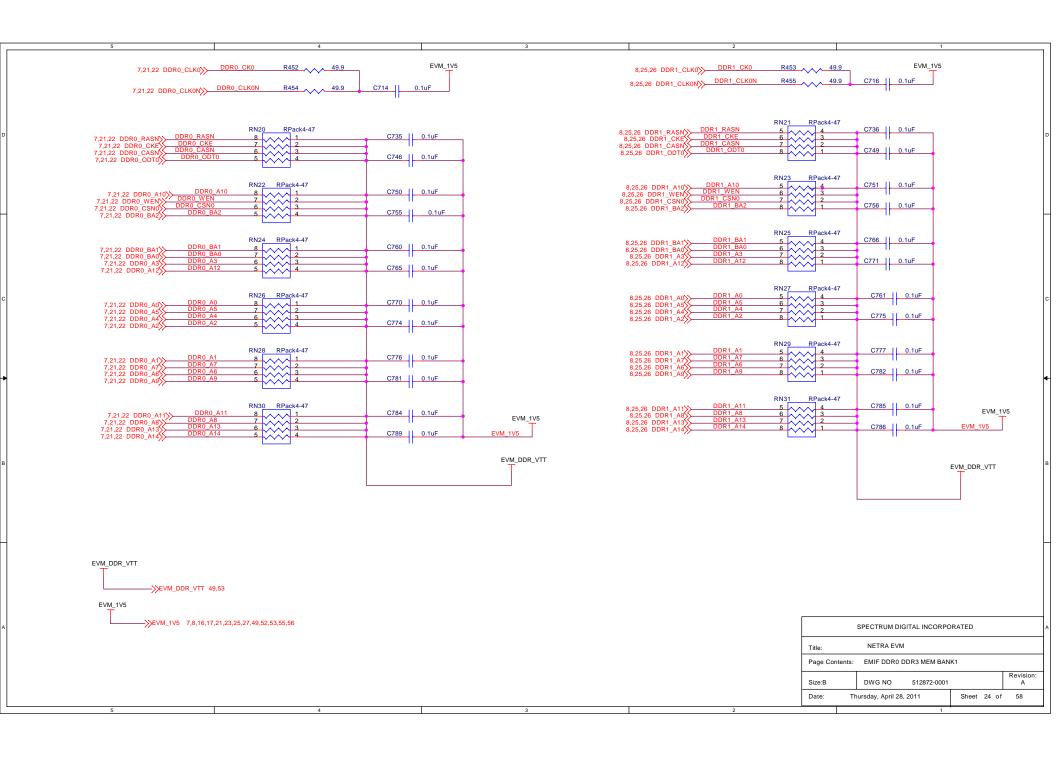
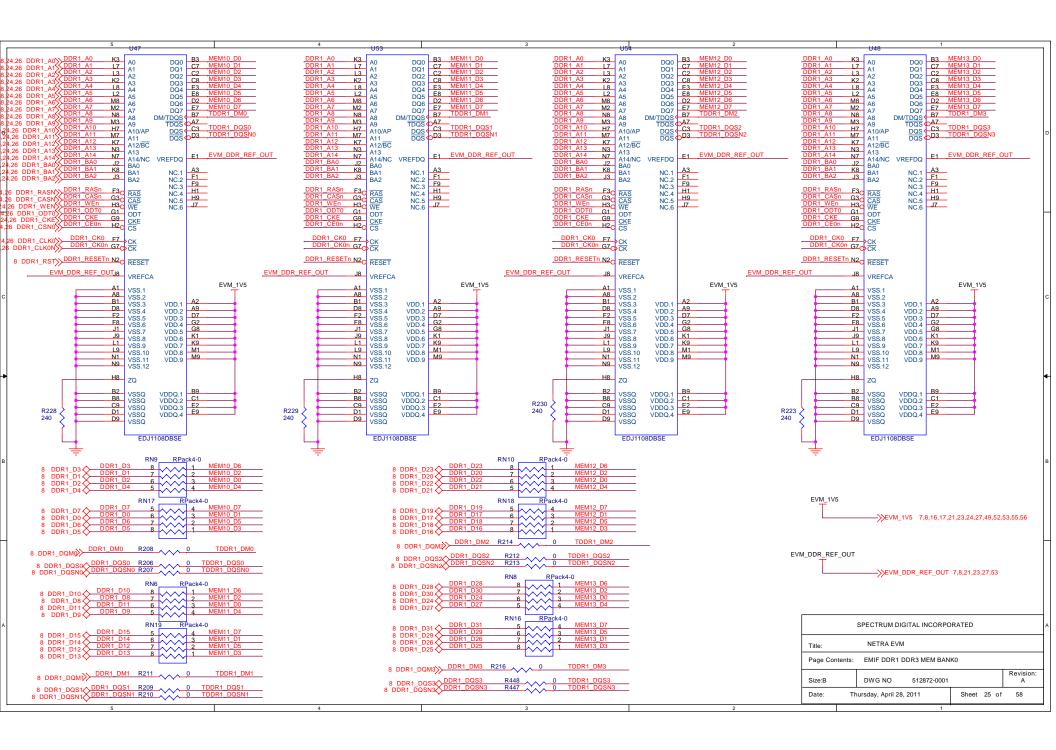


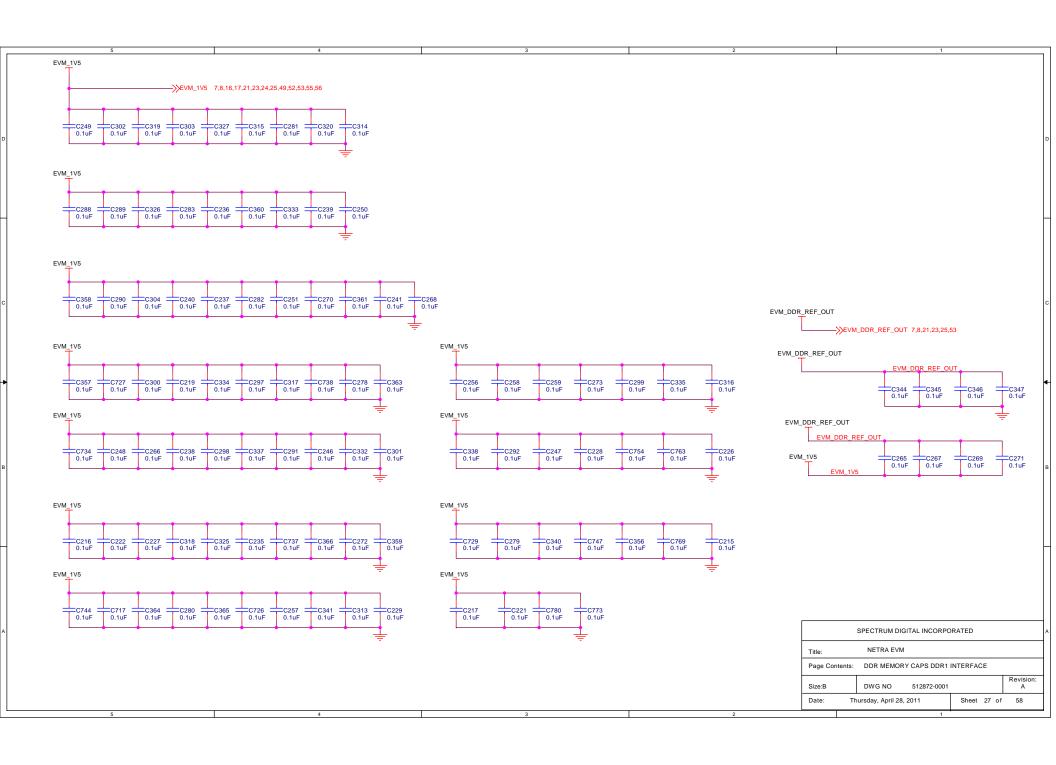
This section is an outline of vias labeled as Testpoints in the schematic. This allows us to determine pwb line lengths for memory to memory and CPU to memory it is purely a visibility tool no actual "component" is used the vias are just replaced with a via that is labeled a test point DATA D24-D31 MEMORY DATA D16-D23 MEMORY DATA D8-D15 MEMORY DATA D0-D7 MEMORY _1_O TPMD15 DDR0 A0 ____ TPM15 _1___ TPMB15 1_0 TPMC15 7,21,24 DDR0_A0>> _1_O TPMC19 _1_O TPMD19 _1_O TPMB19 _1_O TPM19 DDR0 A1 7,21,24 DDR0_A1>> 1_O TPMB18 1_O TPMC18 _1_O TPMD18 DDR0 A2 1_0 TPM18 7,21,24 DDR0_A2>> DDR0_A3 __1__0 TPM13 _1_O TPMB13 _1_O TPMC13 _1_0 TPMD13 7,21,24 DDR0_A3>> _1_0 TPM17 _1_O TPMB17 DDR0_A4 1_0 TPMC17 _1_O TPMD17 7,21,24 DDR0_A4>> _1_O TPMD16 _1_O TPM16 _1_O TPMC16 DDR0_A5 ______TPMB16 7,21,24 DDR0_A5>> _1_O TPMB21 ____O TPMD21 _1_0 TPM21 _1_O TPMC21 DDR0_A6 7,21,24 DDR0_A6>> _1_0 TPMB20 _1_O TPMD20 _1_O TPMC20 DDR0_A7 7,21,24 DDR0_A7>> _1_O TPMD24 _1_0 TPM24 _1___ TPMB24 _1_O TPMC24 7,21,24 DDR0_A8>> _1_0 TPM22 _1_O TPMB22 _1_O TPMC22 ___O TPMD22 DDR0_A9 7,21,24 DDR0_A9>> 10 TPM7 1_0 TPMB7 1_0 TPMC7 _1_O TPMD7 7,21,24 DDR0_A10>> _1_O TPM23 _1_O TPMB23 _1_O TPMC23 _1_O TPMD23 DDR0_A11 7,21,24 DDR0_A11>> _1_O TPM14 _1_O TPMB14 _1_O TPMC14 ___O TPMD14 DDR0 A12 7,21,24 DDR0_A12>> 1_0 TPMB25 _1_O TPMD25 _1_O TPMC25 DDR0 A13 1 TPM25 7,21,24 DDR0_A13 DDR0_A14 _1_O TPM26 _1_O TPMB26 _1_O TPMC26 7,21,24 DDR0_A14>> DDR0_BA0 _1_O TPMB11 _1_O TPMC11 ____O TPMD11 ______TPM11 7,21,24 DDR0_BA0>> DDR0_BA1 _1__O TPM12 1_O TPMB12 1_O TPMC12 _1_0 TPMD12 7,21,24 DDR0_BA1>> ______ TPMD10 DDR0_BA2 1 TPMB10 1_0 TPM10 1_0 TPMC10 7,21,24 DDR0_BA2>> 1 TPMB2 _1_O TPMD2 _1_O TPM2 _1_O TPMC2 DDR0_RAS 7,21,24 DDR0_RASN>> _1_O TPM6 _1_O TPMB6 _1_O TPMC6 _1_O TPMD6 7,21,24 DDR0_CASN>> _1_O TPMD8 1_0 TPM8 _1_O TPMB8 _1_O TPMC8 DDR0_WEn 7,21,24 DDR0_WEN>> 10 TPM5 1_0 TPMB5 _1_O TPMC5 10 TPMD5 7,21,24 DDR0_ODT0>> 1_0 TPMB4 _1_O TPMD4 1_O TPM4 DDR0_CKE 1_0 TPMC4 7,21,24 DDR0_CKE>> _1_O TPM9 _1_O TPMB9 _1_O TPMC9 _1_O TPMD9 DDR0_CE0 7,21,24 DDR0_CSN0>> DDR0 CK0 _1_O TPM1 _1_O TPMB1 _1_O TPMC1 1_O TPMD1 7,21,24 DDR0_CLK0>> _1_O TPMB3 ____O TPMD3 DDR0_CK0 1_O TPM3 1_O TPMC3 7,21,24 DDR0_CLK0N>> SPECTRUM DIGITAL INCORPORATED NETRA EVM Page Contents: DDR0 ADDRESS CONTROL TEST POINTS FOR ROUTING Revision DWG NO 512872-0001 Thursday, April 28, 2011 Sheet 22 of 58

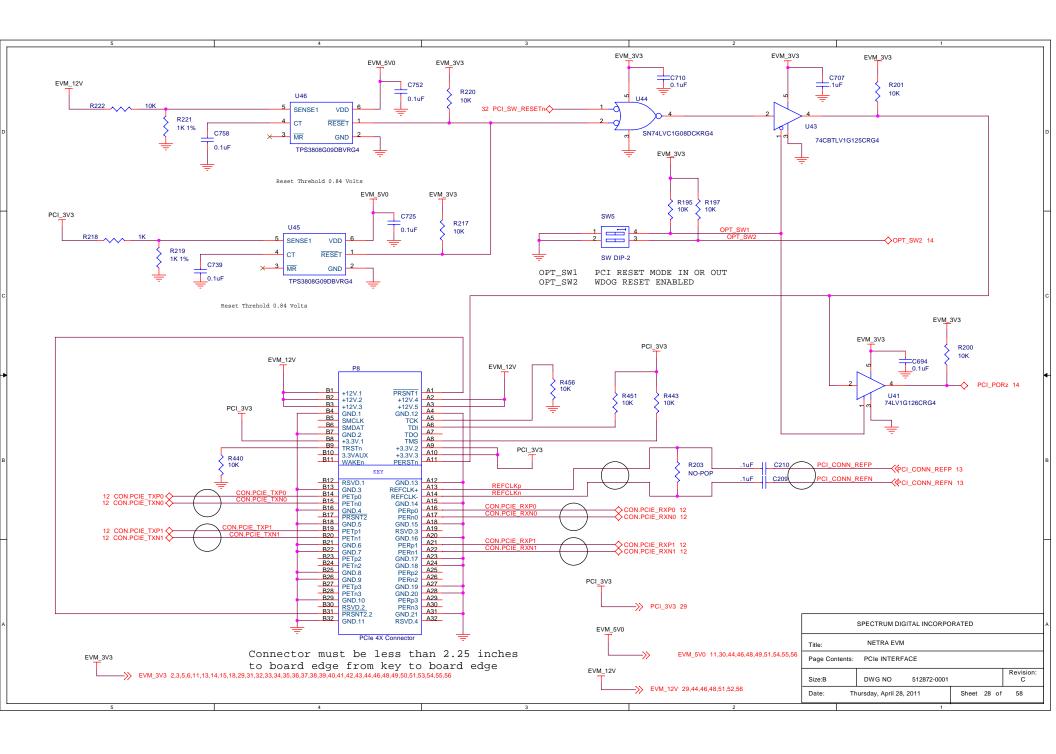


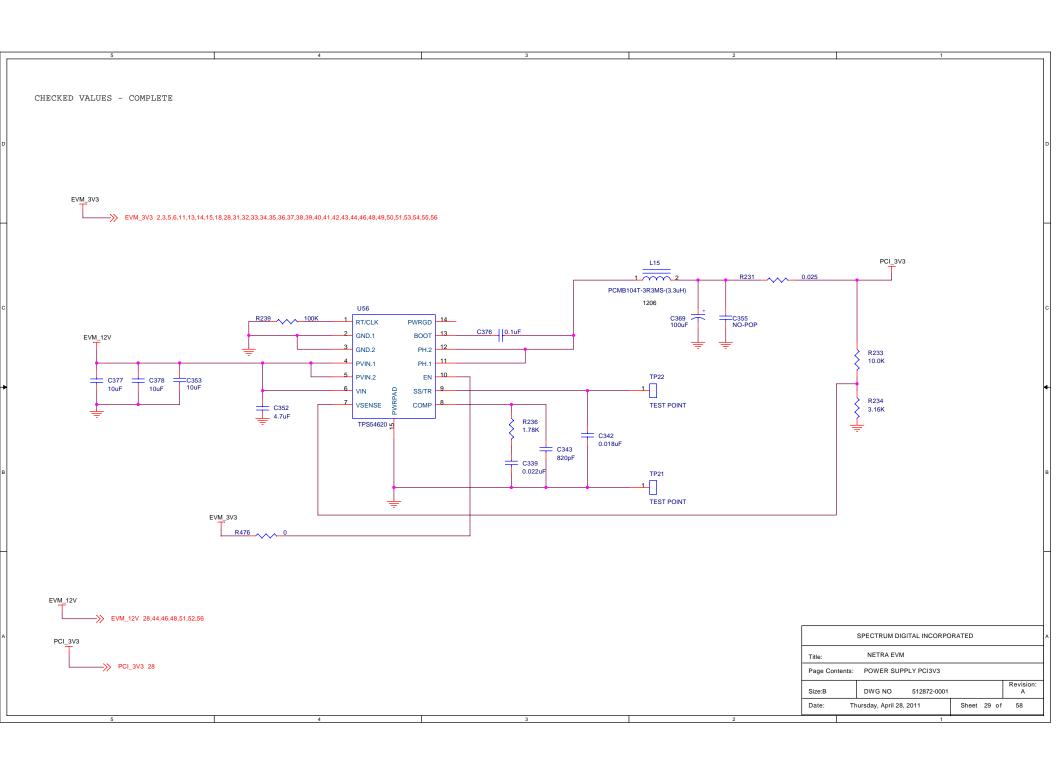


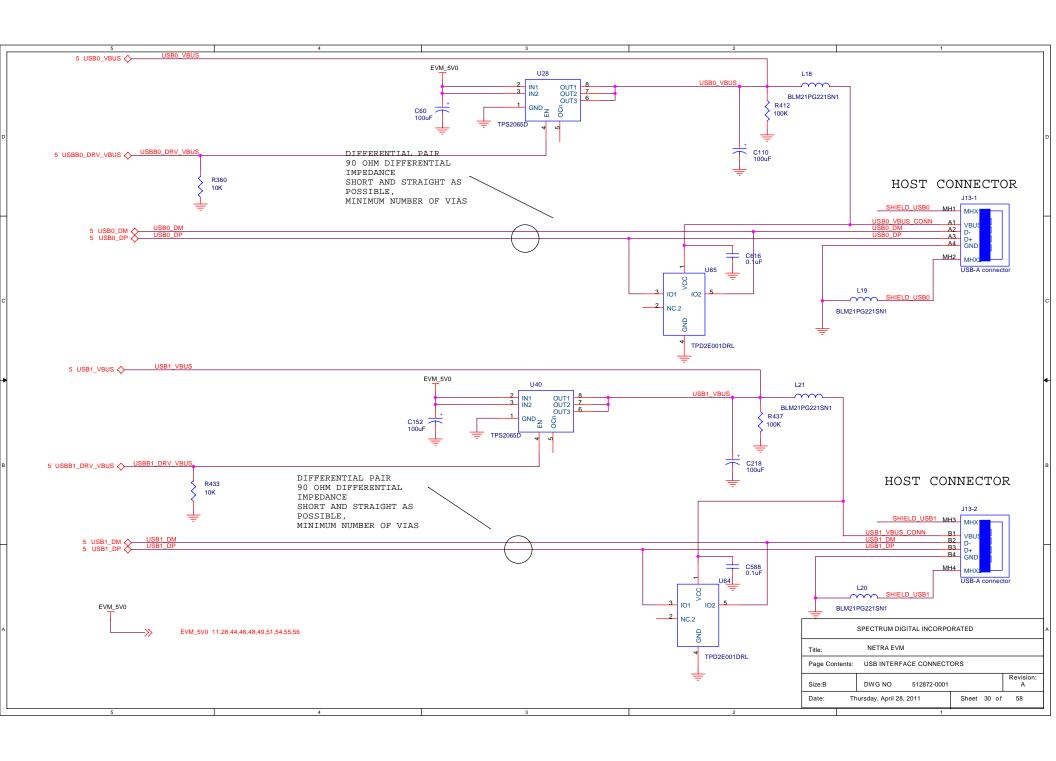


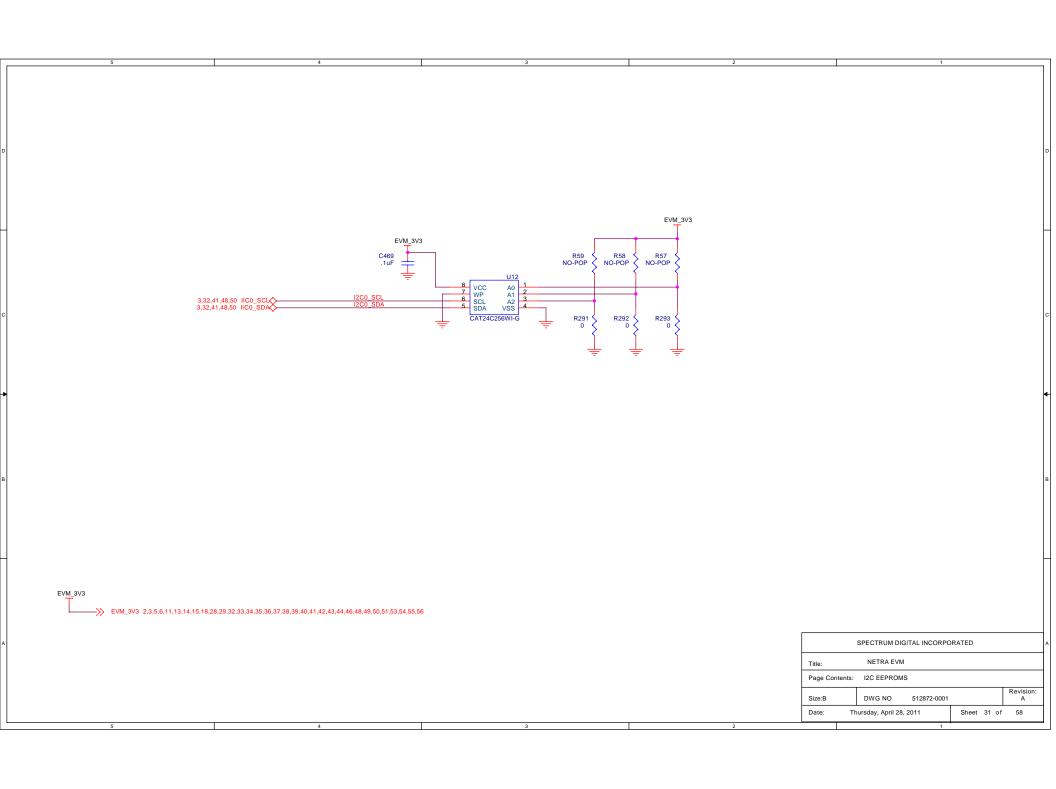
This section is an outline of vias labeled as Testpoints in the schematic. This allows us to determine pwb line lengths for memory to memory and CPU to memory it is purely a visibility tool no actual "component" is used the vias are just replaced with a via that is labeled a test point DATA D24-D31 MEMORY DATA D16-D23 MEMORY DATA D8-D15 MEMORY DATA D0-D7 MEMORY _1__O TP2MB15 _1___0 TP2MD15 DDR1 A0 _____ TP2M15 ______TP2MC15 8,24,25 DDR1_A0>> _1__O TP2MB19 _1_O TP2MC19 _1__O TP2MD19 _1_0 TP2M19 DDR1 A1 8,24,25 DDR1_A1>> 1_O TP2MB18 _1_O TP2MD18 DDR1 A2 1_0 TP2M18 1 ___ TP2MC18 8,24,25 DDR1_A2>> DDR1_A3 _1_O TP2M13 _1__O TP2MB13 _1_O TP2MC13 _1__0 TP2MD13 8,24,25 DDR1_A3>> _1_O TP2M17 _1___ TP2MB17 _1_O TP2MC17 _1_O TP2MD17 8,24,25 DDR1_A4>> _1_O TP2MD16 _1_O TP2MB16 1_0 TP2MC16 DDR1_A5 _1___ TP2M16 8,24,25 DDR1_A5>> _1_O TP2M21 _1_O TP2MB21 _1_O TP2MC21 _1_O TP2MD21 DDR1_A6 8,24,25 DDR1_A6>> _1_O TP2MB20 _1_O TP2MC20 _1_O TP2MD20 _1_0 TP2M20 DDR1_A7 8,24,25 DDR1_A7>> _1_O TP2MD24 _1_O TP2M24 _1__O TP2MB24 _1_O TP2MC24 8,24,25 DDR1_A8>> _1_O TP2M22 _1_O TP2MB22 _1_O TP2MC22 _1_O TP2MD22 DDR1_A9 8,24,25 DDR1_A9>> 1_0 TP2MB7 _1_O TP2MC7 _1_O TP2MD7 _1_O TP2M7 8,24,25 DDR1_A10>> _1_O TP2M23 _1_O TP2MB23 _1_O TP2MC23 _1_O TP2MD23 DDR1_A11 8,24,25 DDR1_A11>> _1_O TP2M14 _1_O TP2MB14 _1_O TP2MC14 DDR1 A12 8,24,25 DDR1_A12>> _1_O TP2M25 _1__O TP2MB25 _1_O TP2MC25 _1_O TP2MD25 DDR1 A13 8,24,25 DDR1_A13>> _1_O TP2MD26 _1_O TP2M26 _1__O TP2MB26 _1_O TP2MC26 DDR1_A14 8,24,25 DDR1_A14>> DDR1_BA0 1 O TP2M11 _1__O TP2MB11 _1_O TP2MC11 _1___0 TP2MD11 8,24,25 DDR1_BA0>> DDR1_BA1 _1__O TP2M12 1 TP2MB12 1 O TP2MC12 _1__O TP2MD12 8,24,25 DDR1_BA1>> _1_O TP2MD10 DDR1_BA2 1_0 TP2M10 1 TP2MB10 ______TP2MC10 8,24,25 DDR1_BA2>> _1_O TP2MD2 _1_O TP2MB2 DDR1_RAS 1_O TP2MC2 8,24,25 DDR1_RASN>> _1_O TP2MC6 _1_O TP2MD6 1_0 TP2M6 1_O TP2MB6 8,24,25 DDR1_CASN>> _1_O TP2M8 _1_O TP2MB8 _1_O TP2MD8 DDR1_WEn _1_O TP2MC8 8,24,25 DDR1_WEN>> _1_0 TP2M5 _1_O TP2MB5 _1_O TP2MC5 _1_O TP2MD5 8,24,25 DDR1_ODT0>> _1_O TP2MB4 _1_O TP2MD4 DDR1_CKE 1_0 TP2M4 1_O TP2MC4 8,24,25 DDR1_CKE>> _1____ TP2M9 _1_O TP2MB9 _1_O TP2MC9 _1_O TP2MD9 DDR1_CE0 8,24,25 DDR1_CSN0>> _1_O TP2MB1 DDR1 CK0 _1_O TP2M1 _1_O TP2MC1 _____TP2MD1 8,24,25 DDR1_CLK0>> _1_O TP2M3 DDR1_CK0 1_O TP2MB3 1 O TP2MC3 ___O TP2MD3 8,24,25 DDR1_CLK0N>> SPECTRUM DIGITAL INCORPORATED NETRA EVM Page Contents: DDR1 ADDRESS CONTROL TEST POINTS FOR ROUTING Revision DWG NO 512872-0001 Thursday, April 28, 2011 Sheet 26 of 58

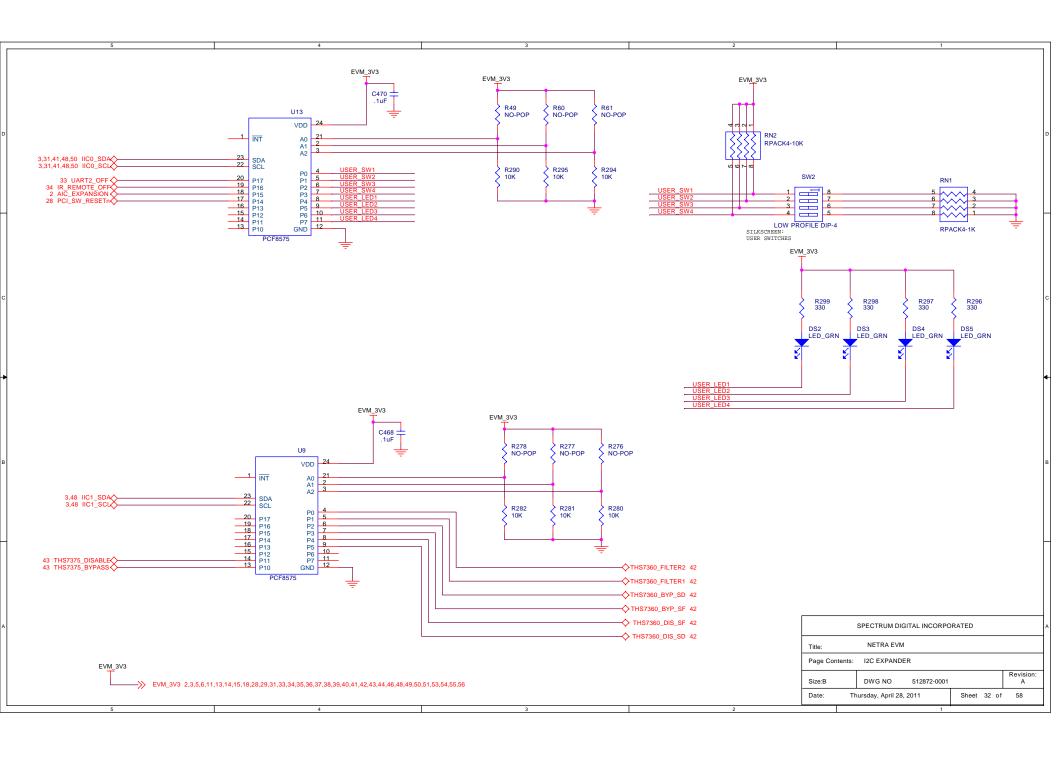


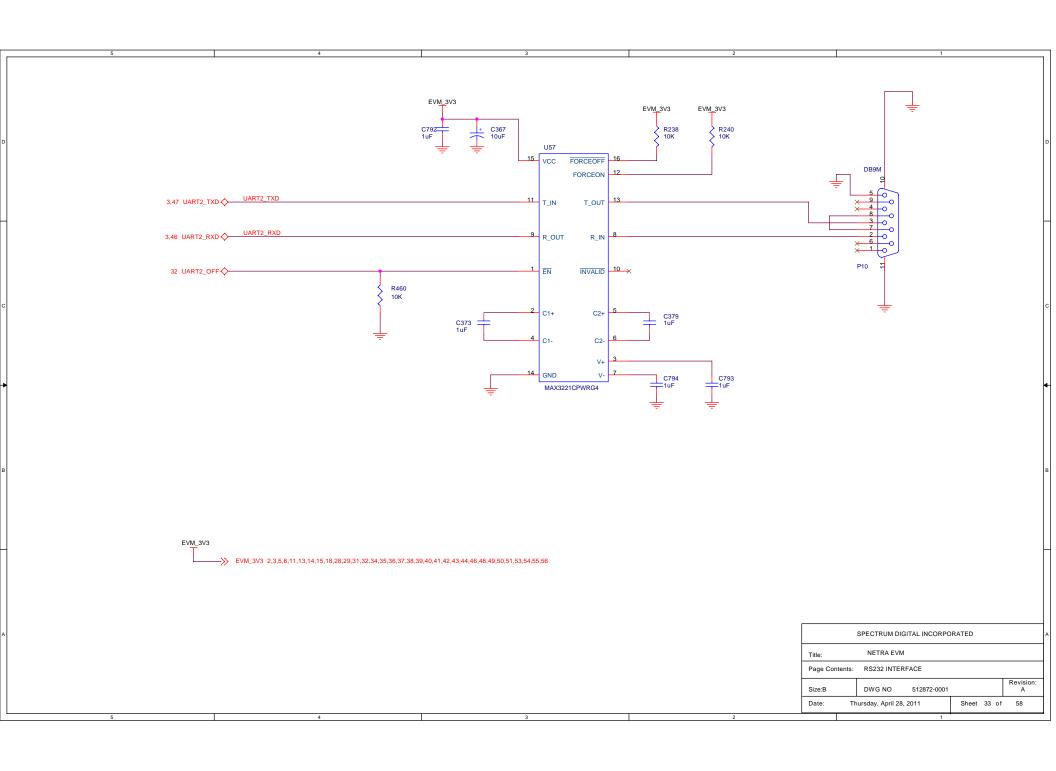


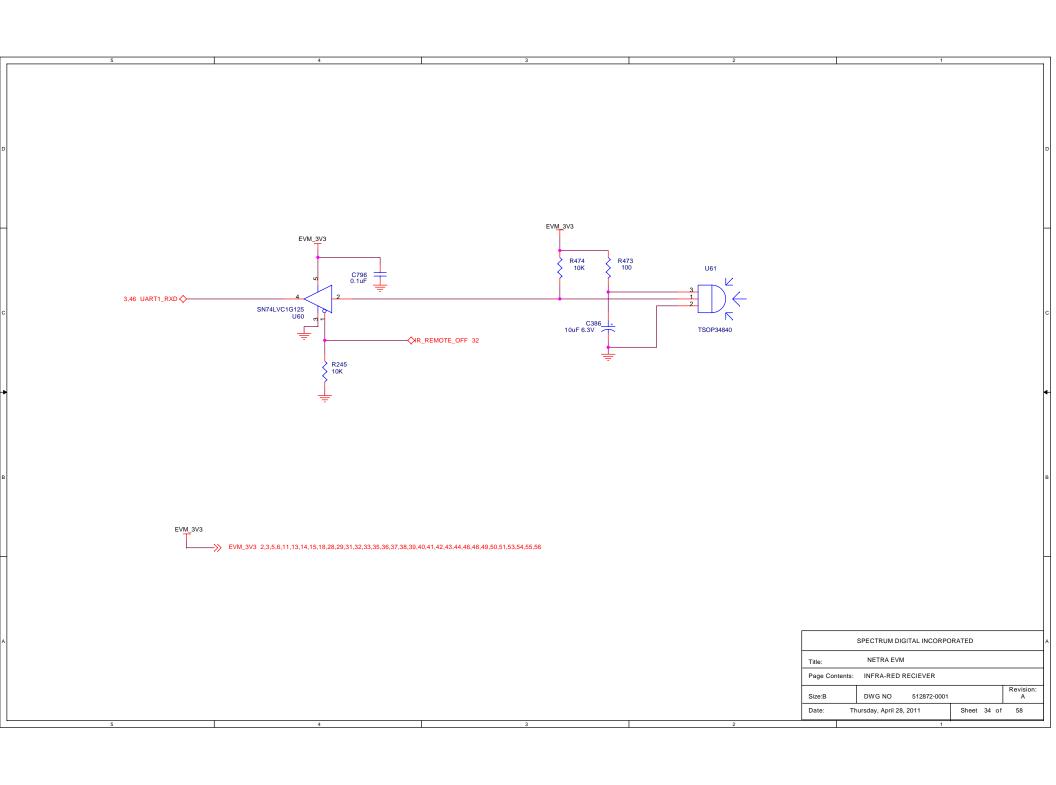


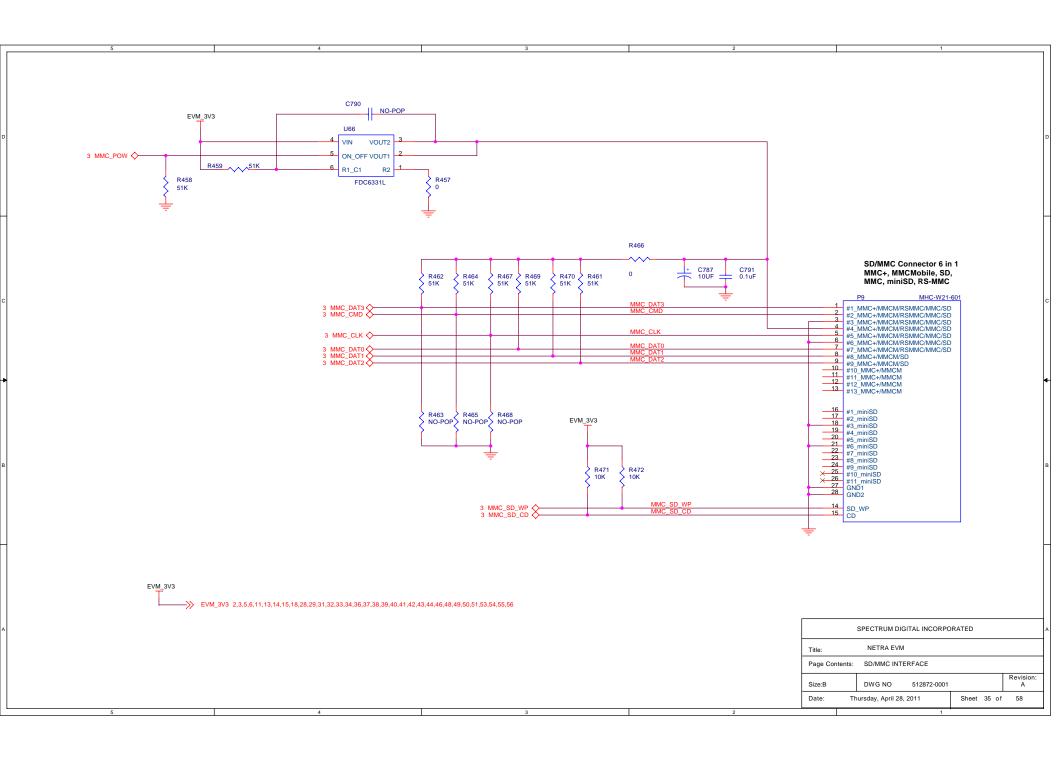


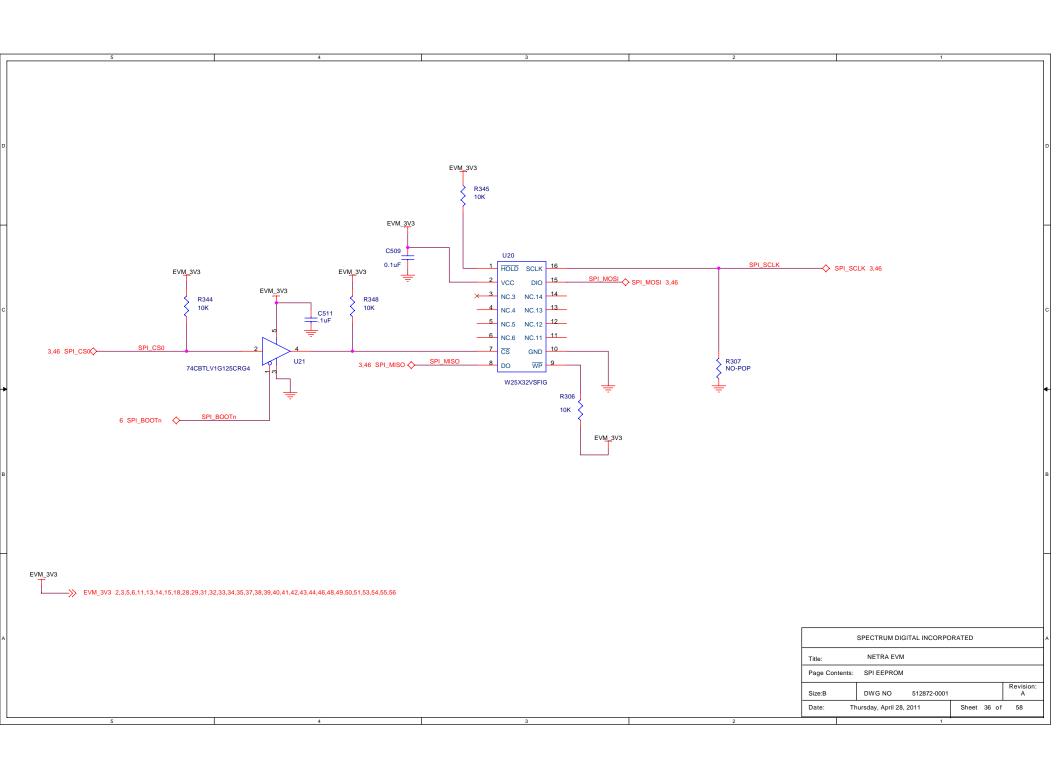


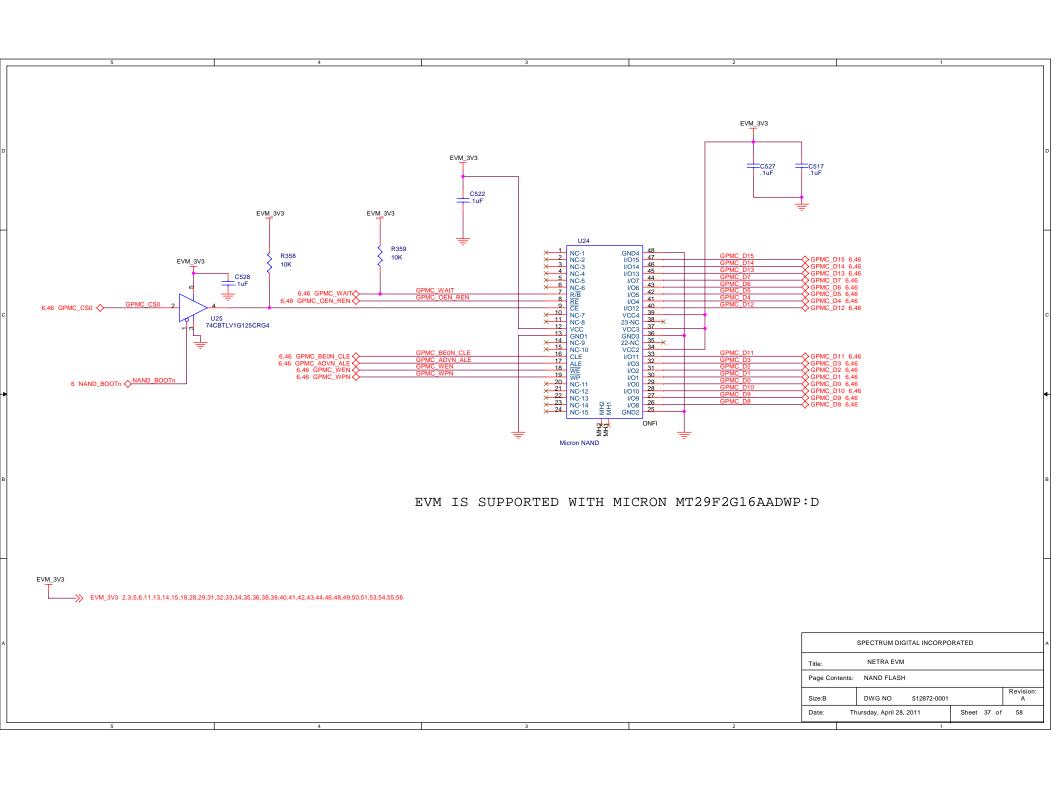


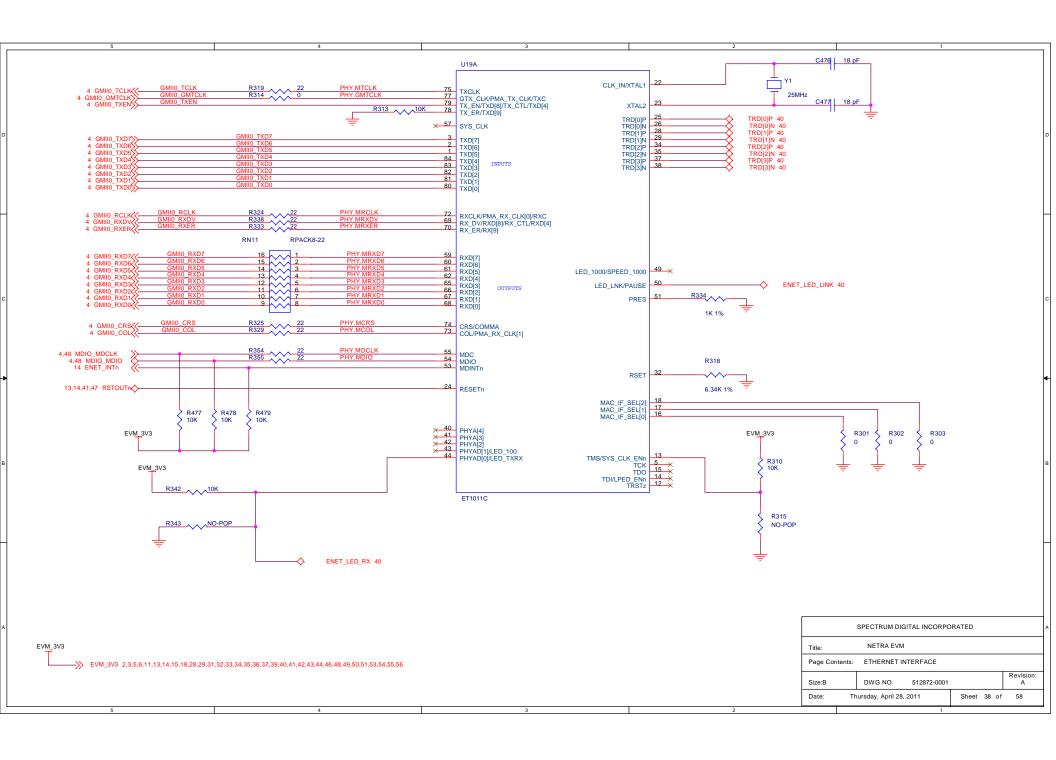


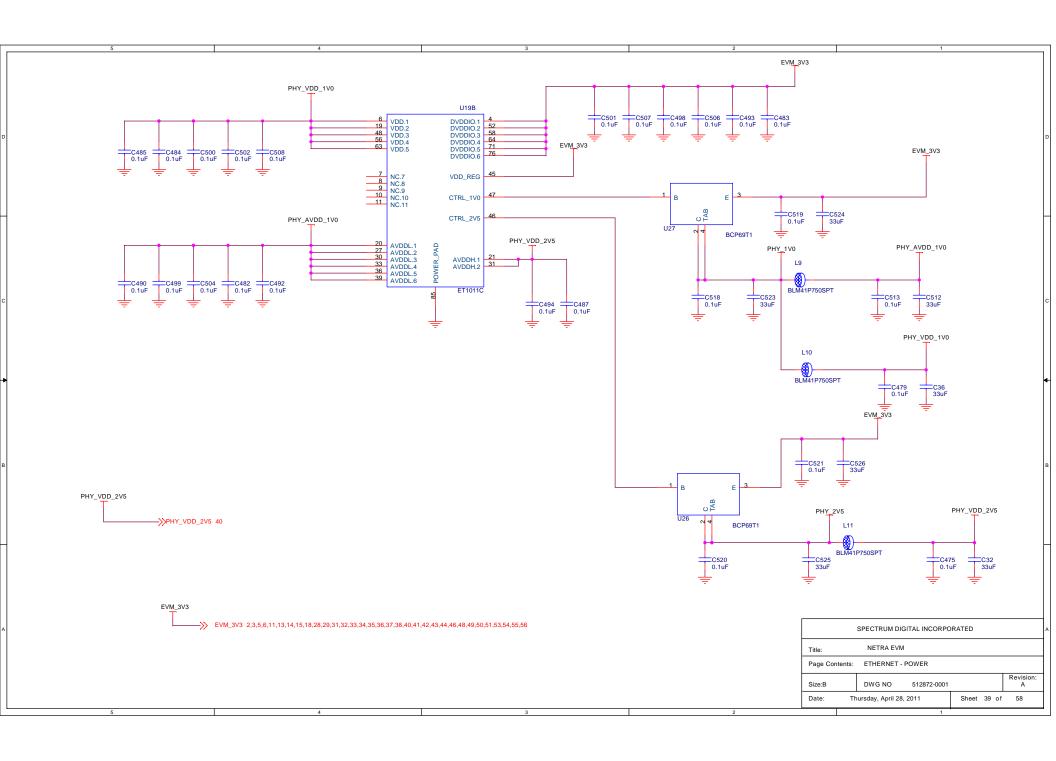


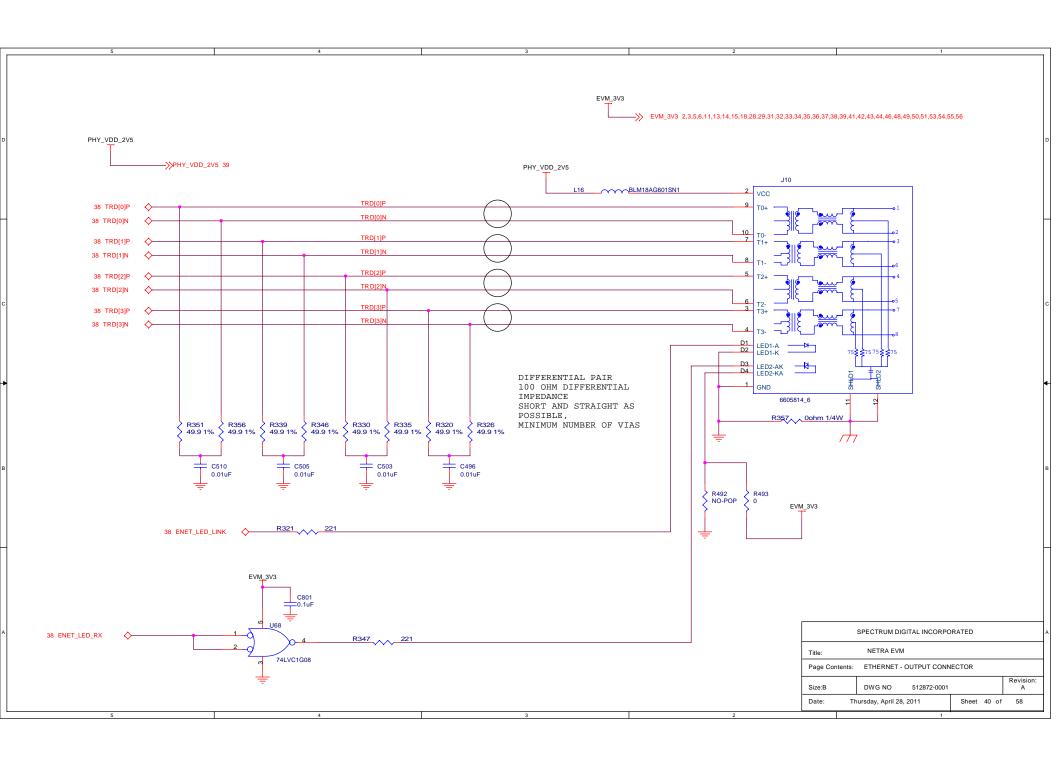


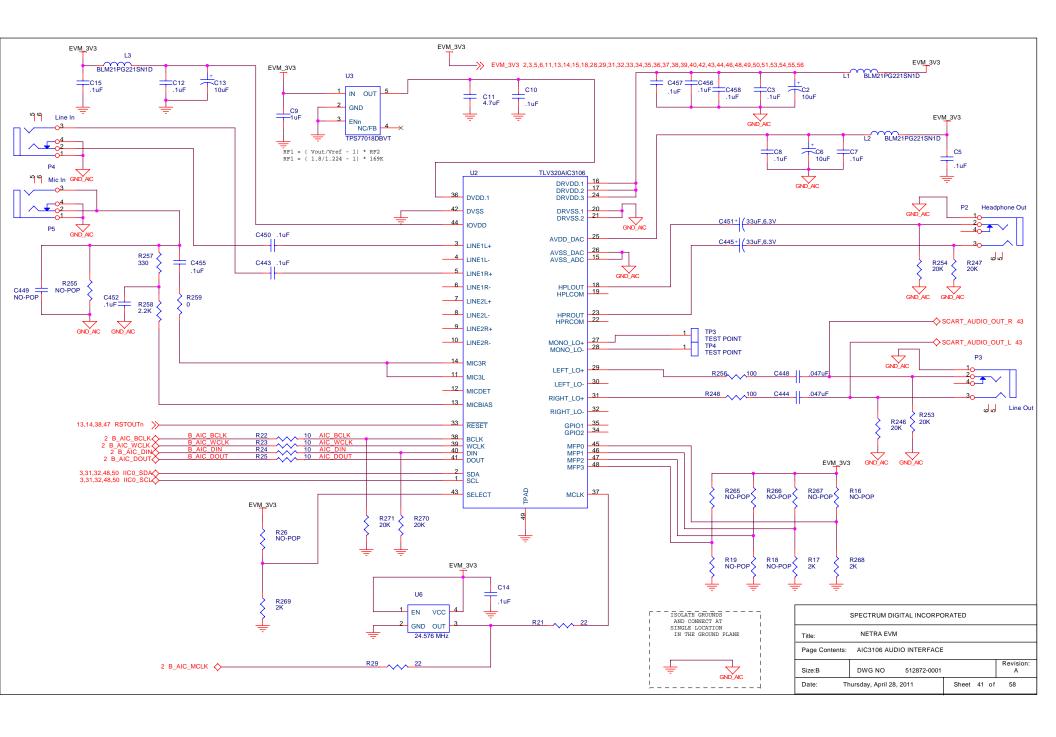


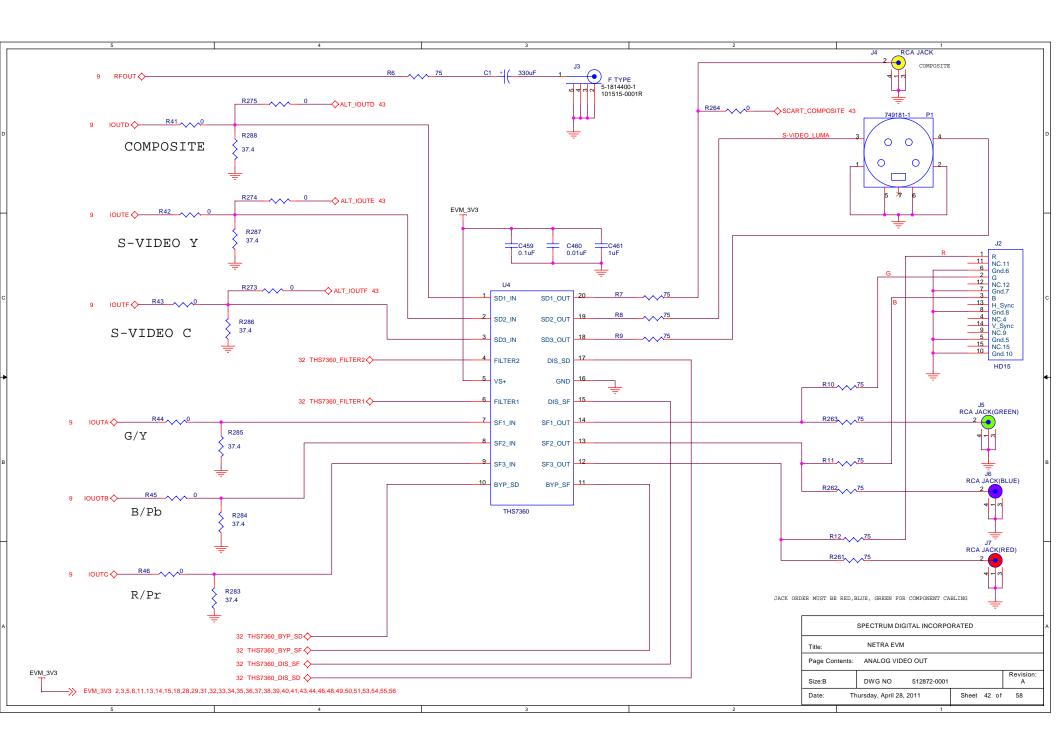


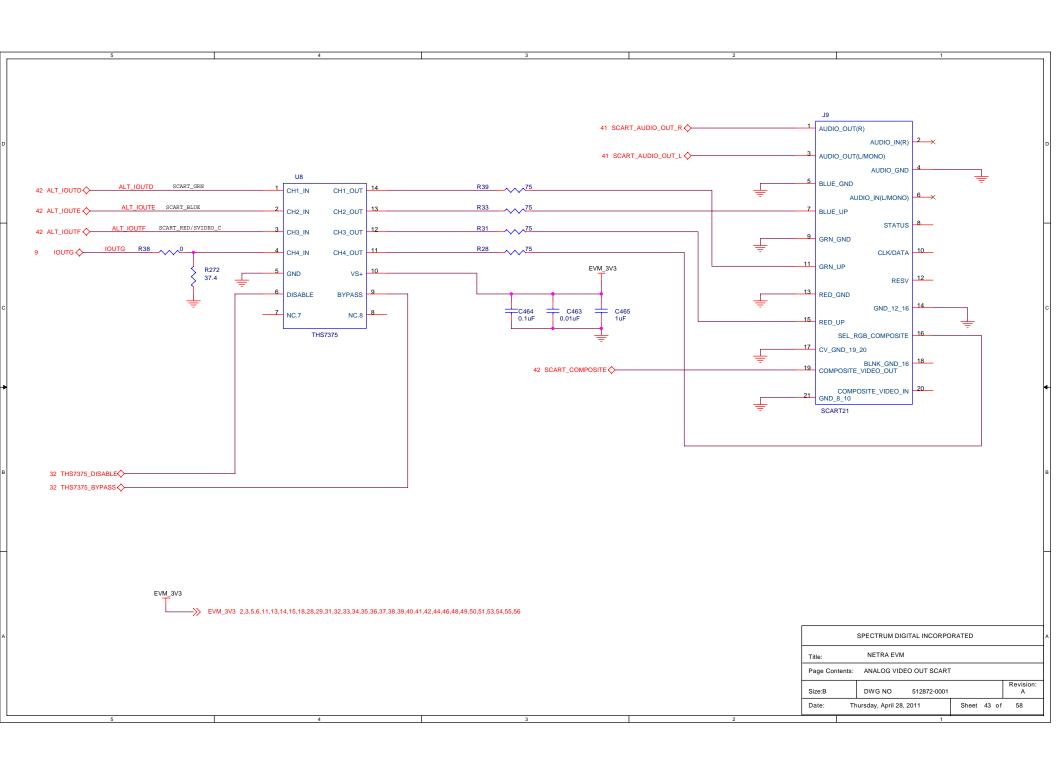


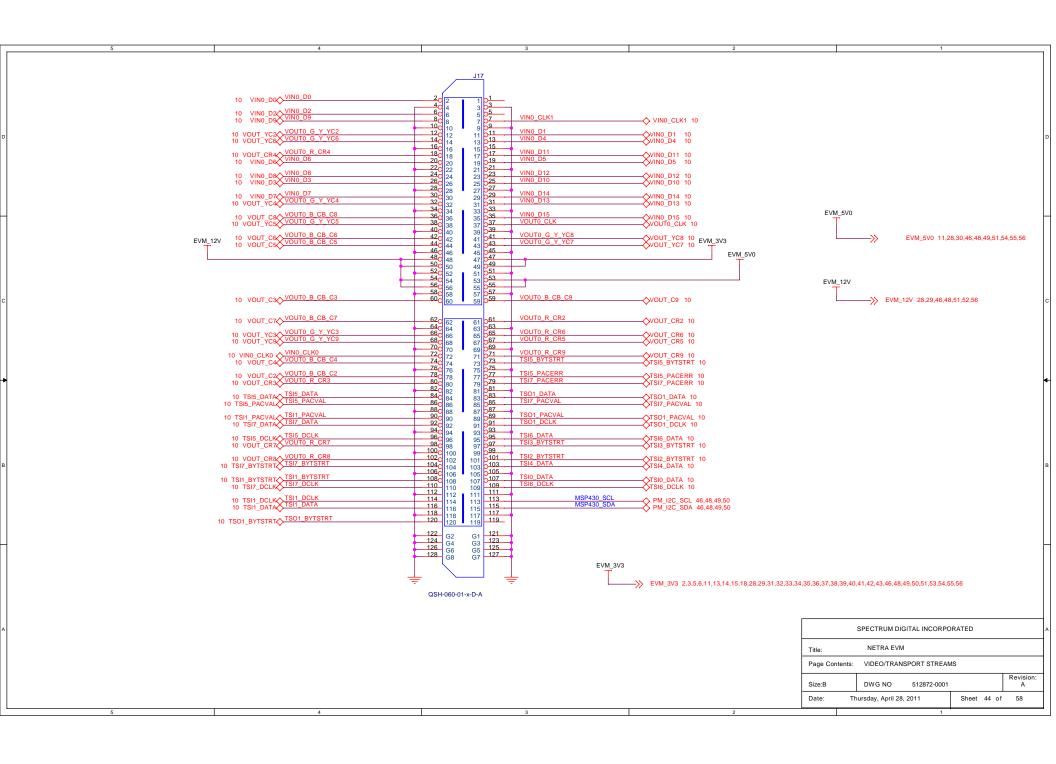


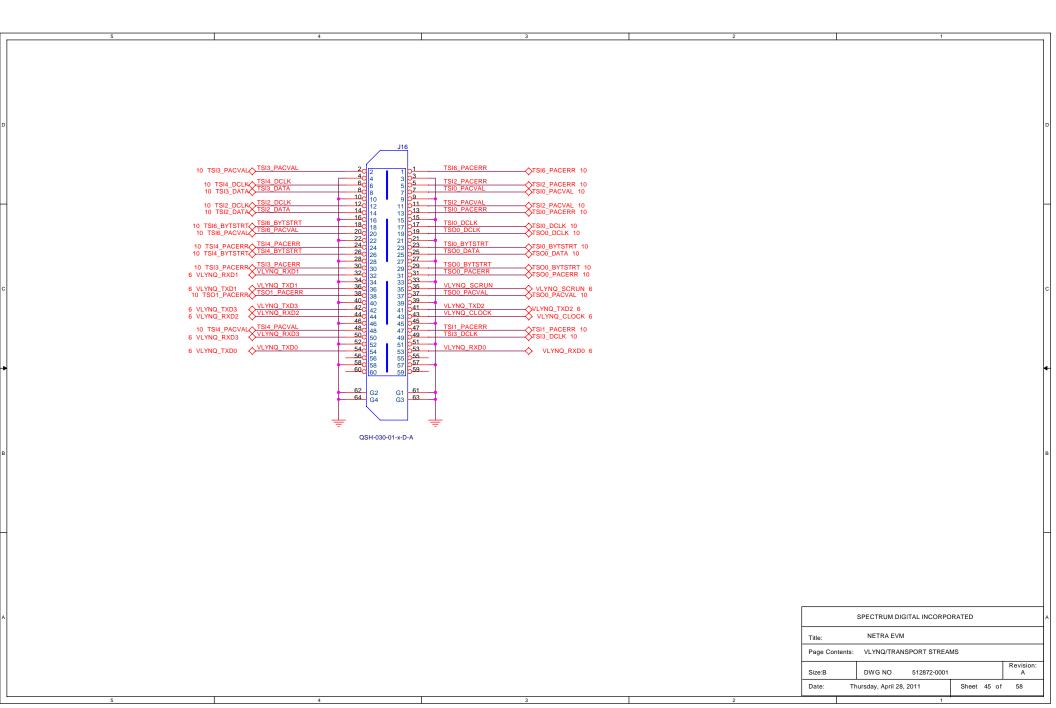


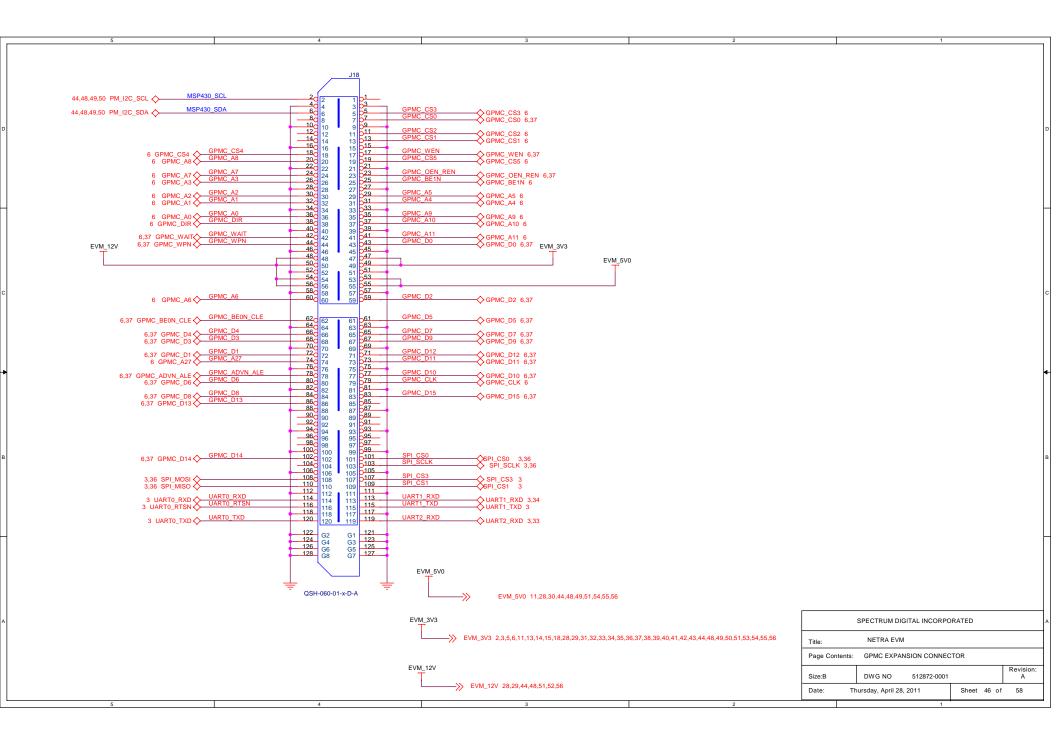


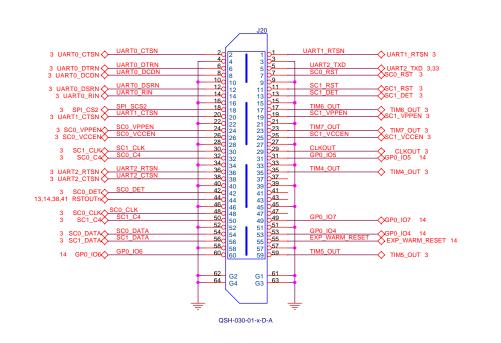




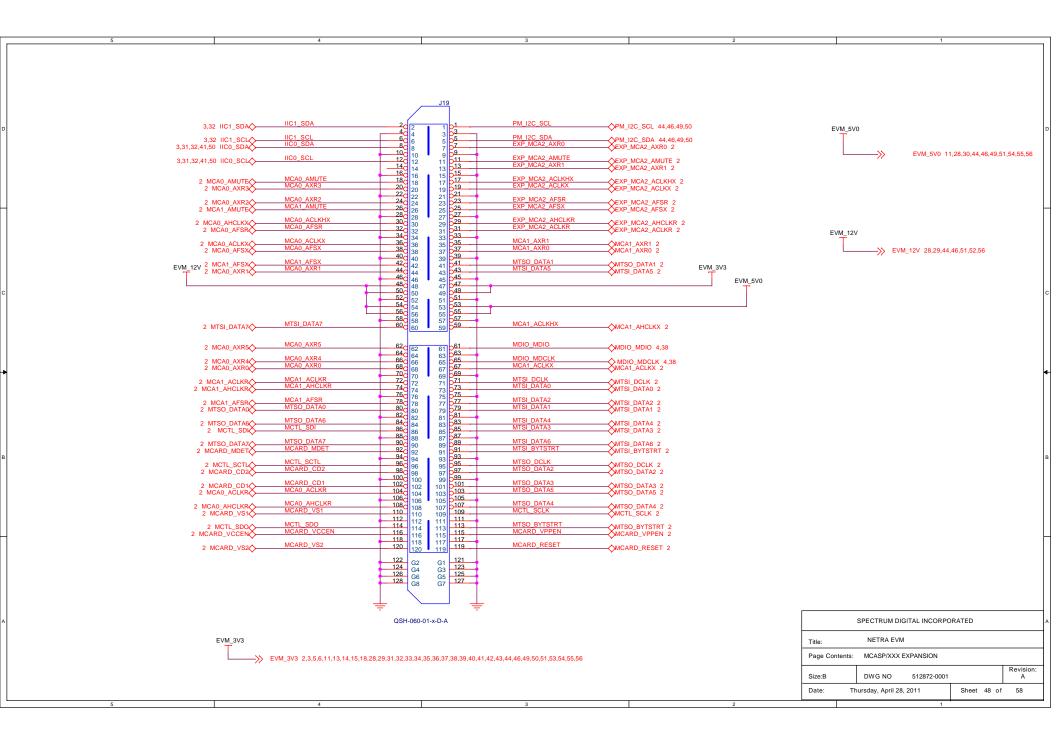


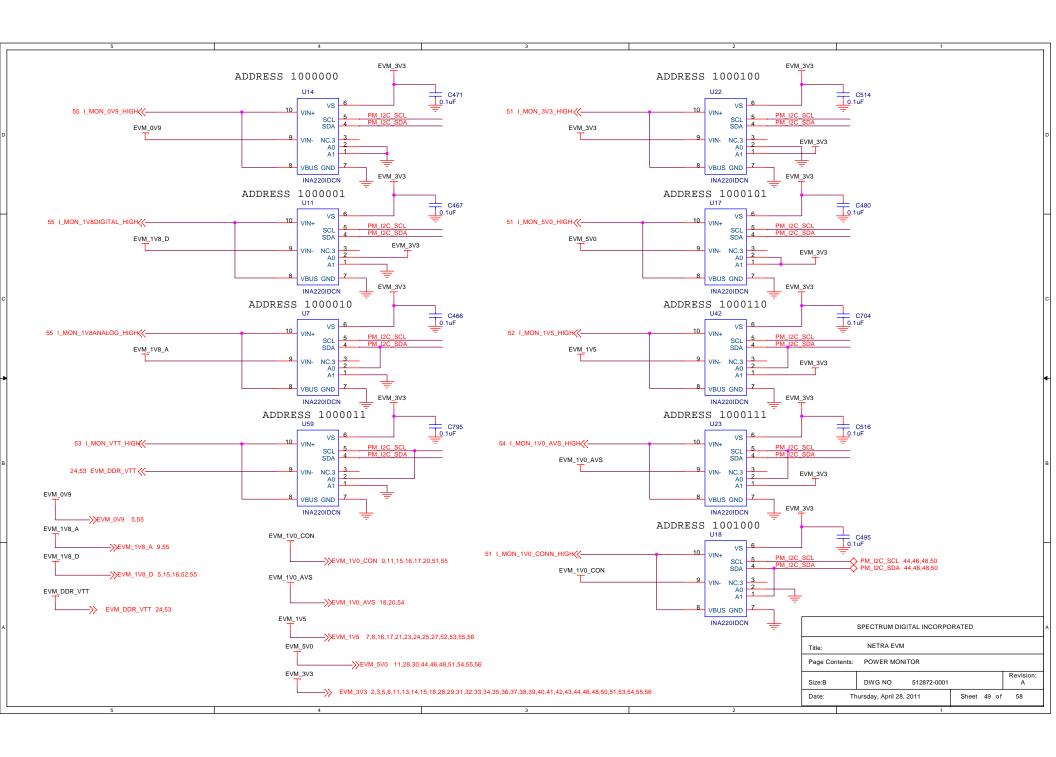


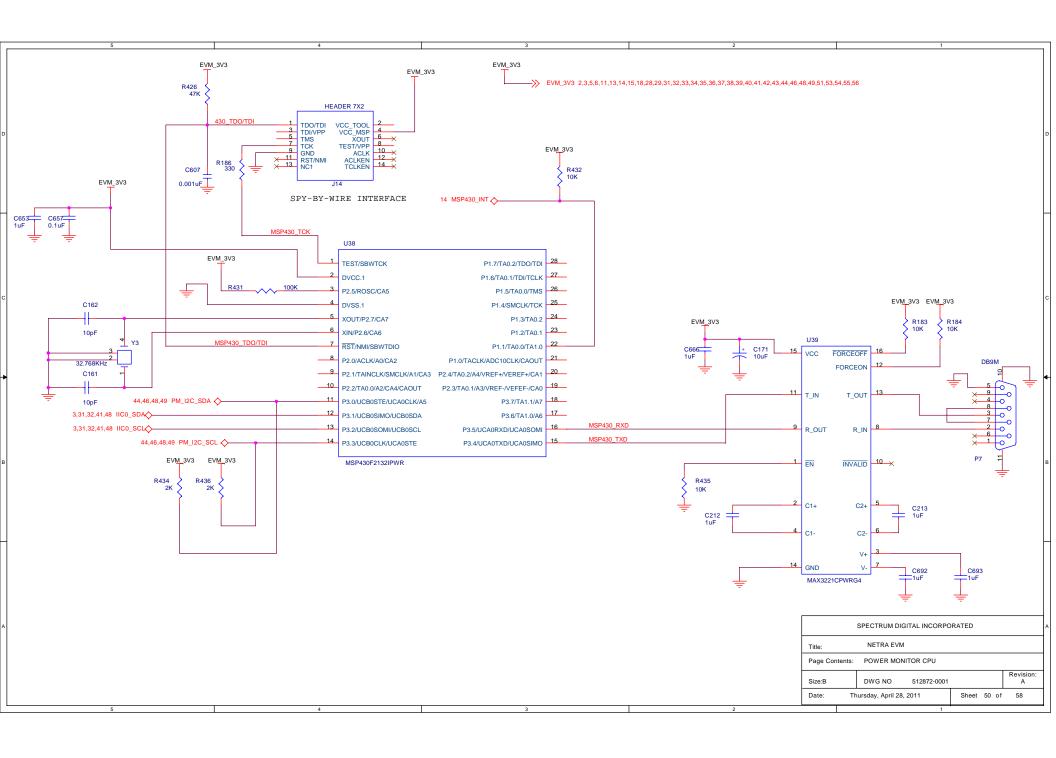


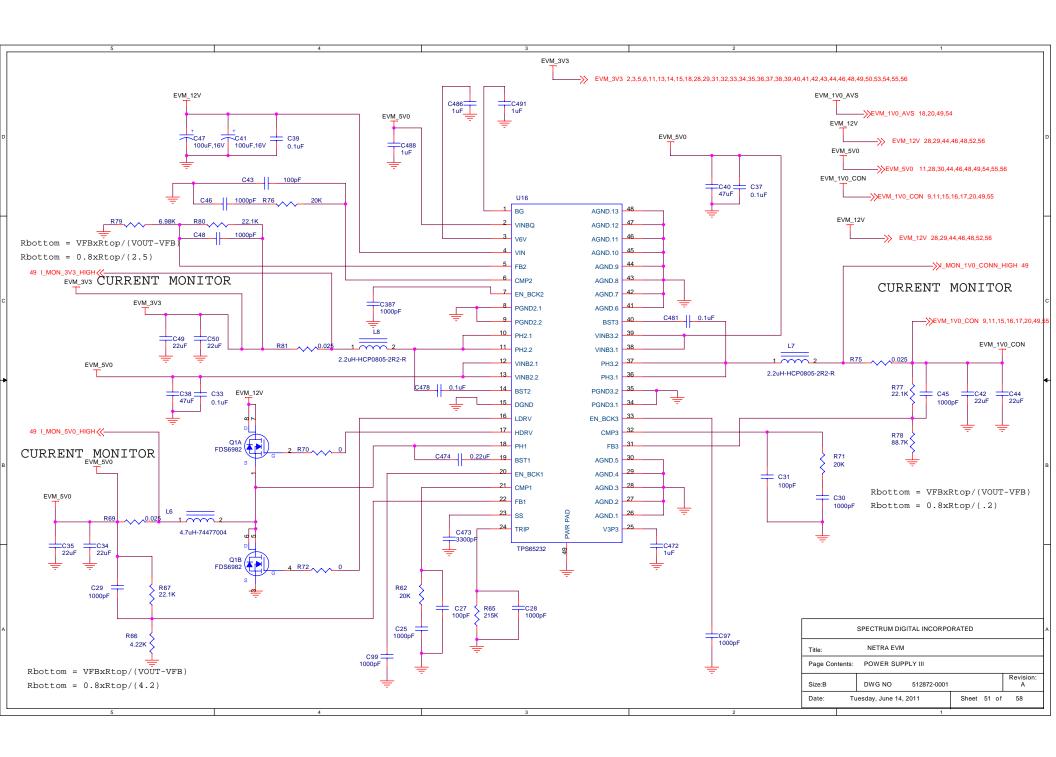


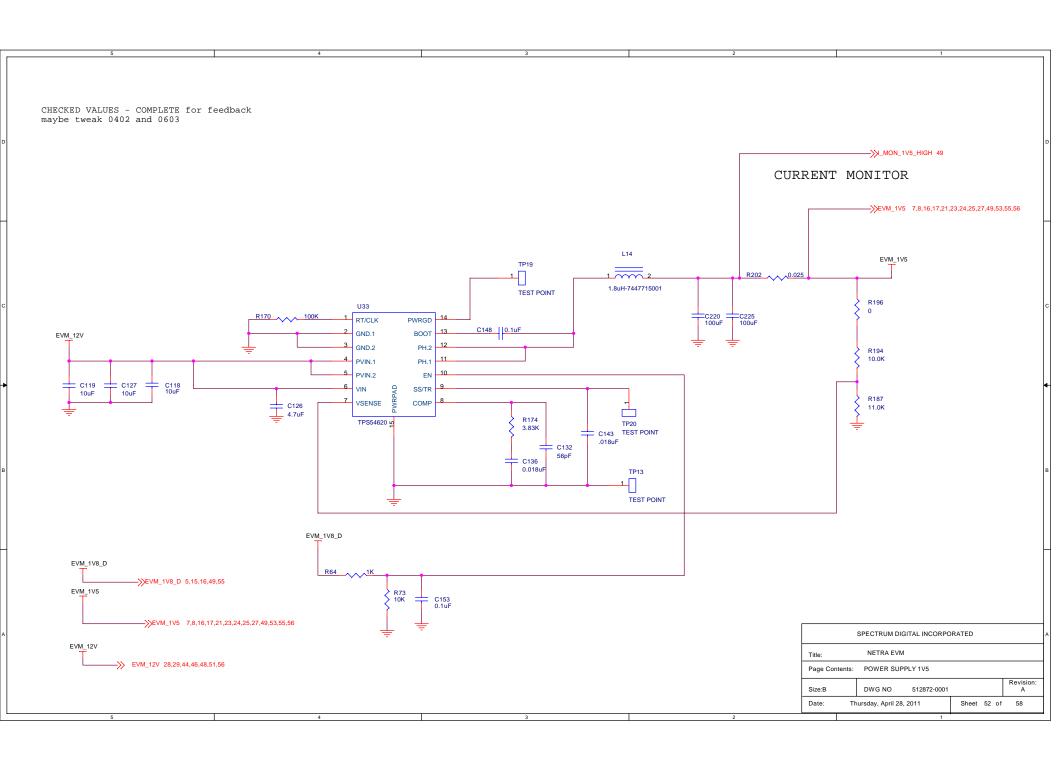
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Title:	NETRA EVM			
Page Contents: SERIAL I/O EXPANSION CONNECTOR				
Size:B	DWG NO 512872-0001		Revision: A	
Date: Th	ursday, April 28, 2011	Sheet 47 of	58	

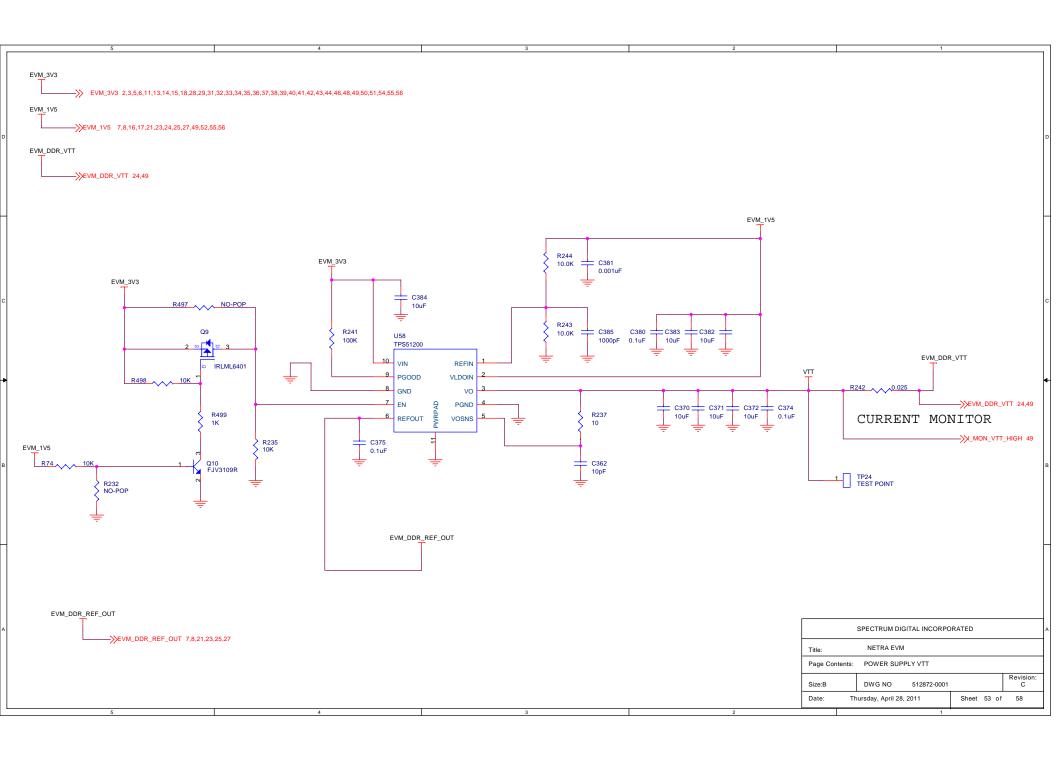


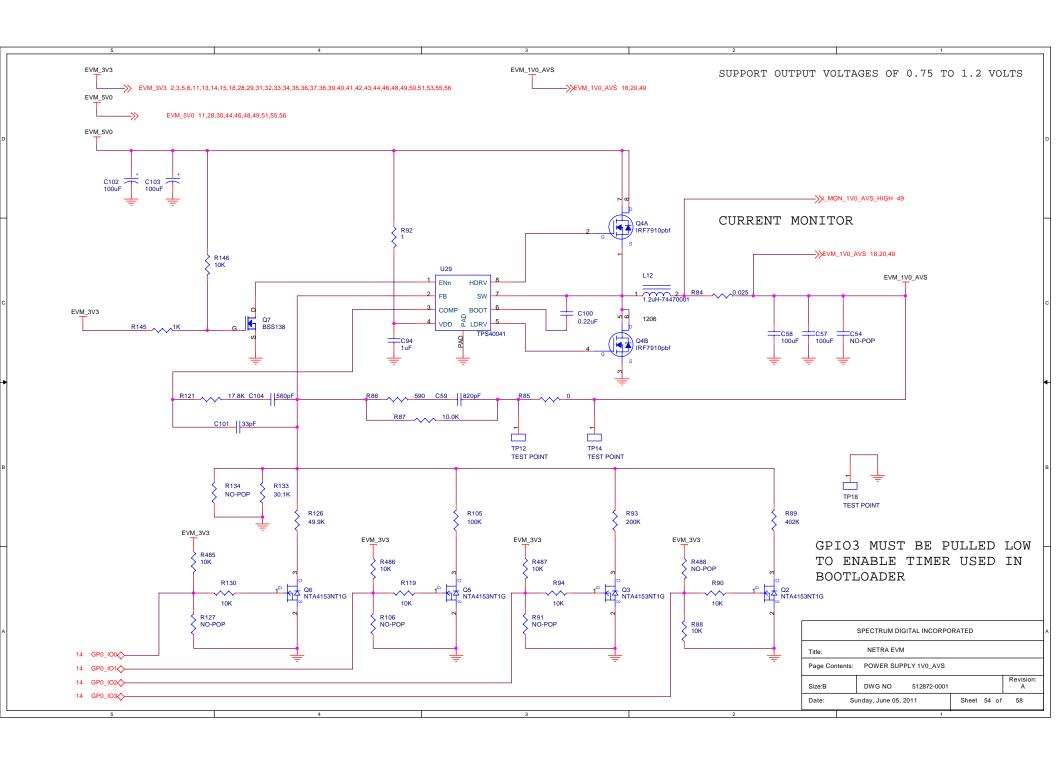


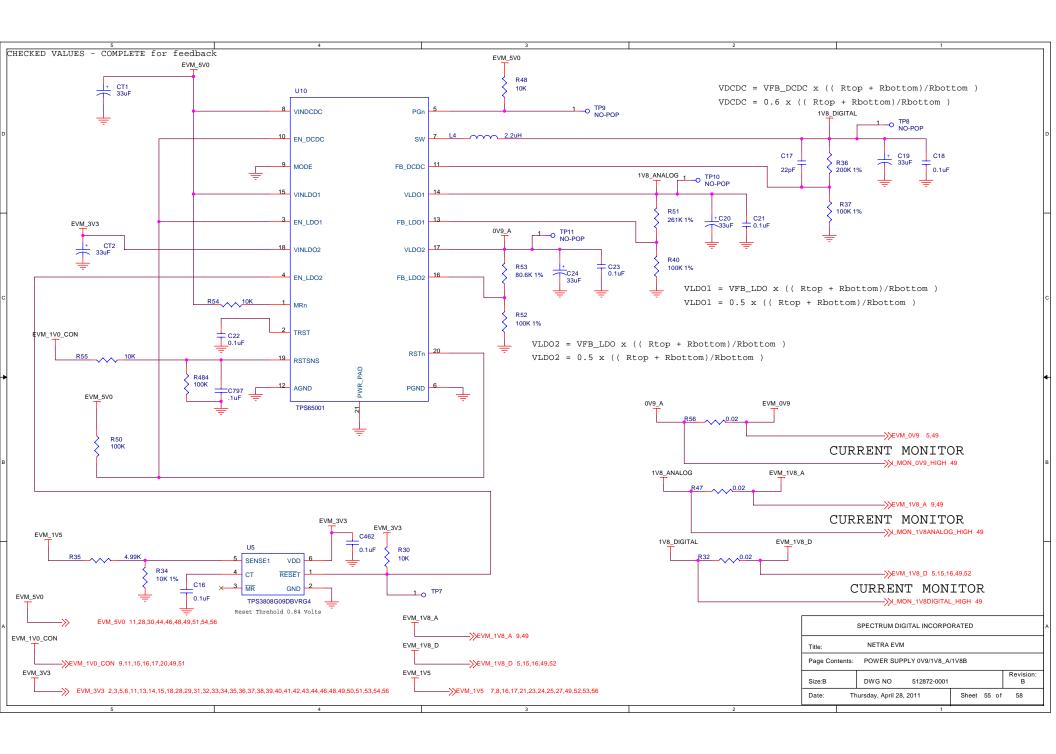


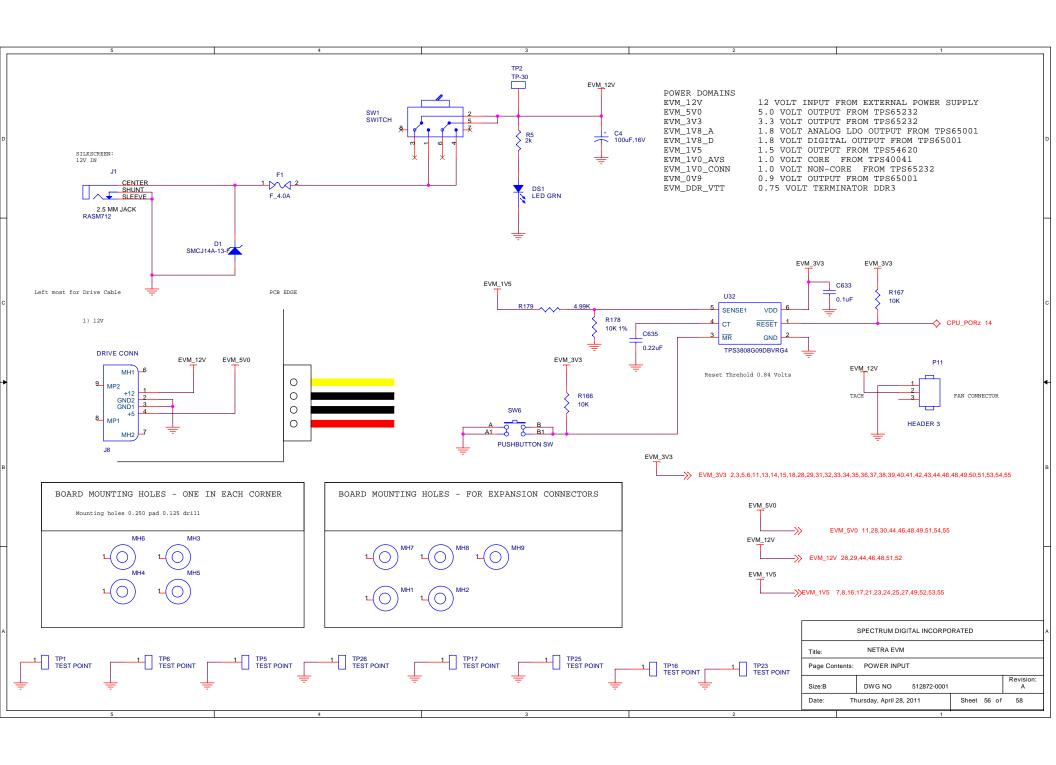


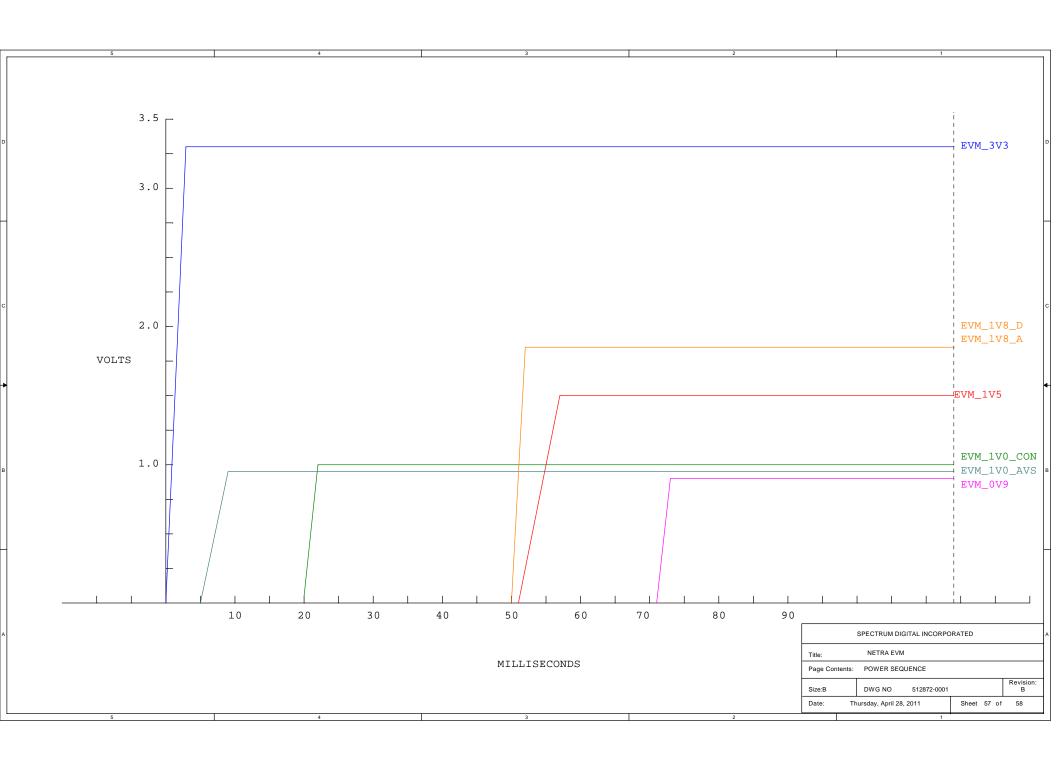












REVISION A - ASSY 512870

BUILT ON PWB 512871 REVISION A
BUILT ON LOGIC 512872 REVISION A

ENGINEERING UNITS ONLY

REVISION B - ASSY 512870

BUILT ON PWB 512871 REVISION B
BUILT ON LOGIC 512872 REVISION B

UPDATED POWER SEQUENCING FROM REVISION A

REVISION C - ASSY 512870

BUILT ON PWB 512871 REVISION B

BUILT ON LOGIC 512872 REVISION B

INCREASED C635 TO .22uF FOR LONGER POWER ON RESET FIXED USB ISSUE

CHANGED R218 TO 1K TO FIX PCI RESET

REMOVED R232 AND CHANGED R74 TO 0 , TO HELP RAISE VT ENABLE VOLTAGE (STILL A BIT OUT OF SPEC, WILL FIX IN NEXT BOARD REVISION)

REVISION D - ASSY 512870

BUILT ON PWB 512871 REVISION B

BUILT ON LOGIC 512872 REVISION B

CHANGED AVS CIRCUITRY AND CPU HAS AVS ENABLED

REVISION E - ASSY 512870

BUILT ON PWB 512871 REVISION C

BUILT ON LOGIC 512872 REVISION C

UPDATED CAPS AROUND TPS65232 TO HELP WITH OVERVOLTAGE ON SWITCH OUTPUTS OF THE PART LAYOUT IMPROVEMENT UPDATED VTT ENABLE TO RAISE ENABLE VOLTAGE PAST 1.7V MIN

SPECTRUM DIGITAL INCORPORATED				
Title:	NETRA EVM			
Page Contents:	REVISION HISTORY			
Size:B	DWG NO 512872-0001		Revision: C	
Date: Tuesday, June 14, 2011		Sheet 58 of	58	