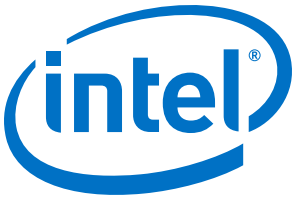

Intel® Arria® 10 GX/GT Device Errata and Design Recommendations

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Contents

ES-1057 | 2017.12.20

Intel® Arria® 10 GX/GT Device Errata and Design Recommendations

This errata sheet provides information about known device issues affecting Intel® Arria® 10 GX/GT devices. It also offers design recommendations you should follow when using Intel Arria 10 GX/GT devices.

Design Recommendations for Intel Arria 10 GX/GT Devices

The following section describes recommendations you should follow when using Intel Arria 10 GX/GT devices.

Intel Arria 10 GX/GT Device Lifetime Guidance

The table below describes the Intel Arria 10 GX/GT product family lifetime guidance corresponding to VGA gain settings.

Table 1. Lifetime Guidance

VGA Gain Setting	Device Lifetime Guidance for Continuous Operation (1)	
	100°C T_J (Years)	90°C T_J (Years)
0	11.4	11.4
1	11.4	11.4
2	11.4	11.4
3	11.4	11.4
4	11.4	11.4
5	9.3	11.4
6	6.9	11.4
7	5.4	11.4

Design Recommendation

If you are using VGA gain settings of 5, 6, or 7 and require an 11.4-year lifetime, Intel recommends either one of the following guidelines:

- Change the VGA gain setting to 4, and re-tune the link, or
- Limit the junction temperature T_J to 90°C.

(1) Device lifetime recommendation calculation assumes the device is configured and the transceiver is always powered up (24 x 7 x 365).

Device Errata for Intel Arria 10 GX/GT Devices

The table below lists specific device issues and affected Intel Arria 10 GX/GT devices.

Table 2. Device Issues

Issue	Affected Devices	Planned Fix
Automatic Lane Polarity Inversion for PCIe Hard IP on page 5	All Intel Arria 10 devices	No planned fix
High VCCBAT Current when VCC is Powered Down on page 5	All Intel Arria 10 devices	No planned fix

Automatic Lane Polarity Inversion for PCIe Hard IP

For Intel Arria 10 PCIe Hard IP open systems where you do not control both ends of the PCIe link, Intel does not guarantee automatic lane polarity inversion with the Gen1x1 configuration, Configuration via Protocol (CvP), or Autonomous Hard IP mode. The link may not train successfully, or it may train to a smaller width than expected. There is no planned workaround or fix.

For all other configurations, refer to the following workaround.

Workaround

Refer to the Knowledge Database for details to workaround this issue.

Status

Affects: All Intel Arria 10 devices.

Status: No planned silicon fix.

Related Links

Knowledge Database

High V_{CCBAT} Current when V_{CC} is Powered Down

If you power off V_{CC} when V_{CCBAT} remains powered on, V_{CCBAT} may draw higher current than expected.

If you use the battery to maintain volatile security keys when the system is not powered up, V_{CCBAT} current could be up to 120 µA, resulting in shortened battery life.

Workaround

Contact your battery provider to evaluate the impact to the retention period of the battery used on your board.

There is no impact if you connect the V_{CCBAT} to the on-board power rail.

Status

Affects: All Intel Arria 10 devices

Status: No planned silicon fix.

Document Revision History

Date	Version	Changes
December 2017	2017.12.20	Made the following change: • Added the High V_{CCBAT} current erratum.
July 2017	2017.07.28	Initial release