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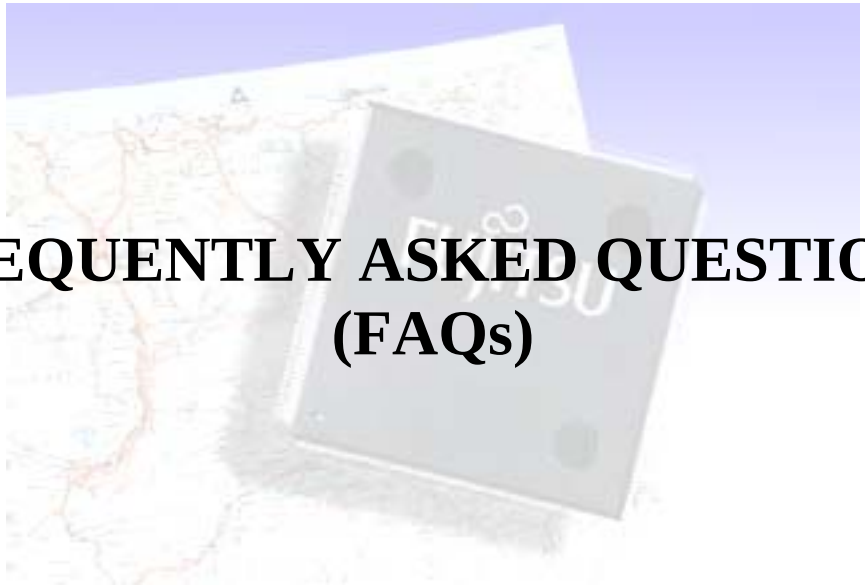
FUJITSU GDCs



FREQUENTLY ASKED QUESTIONS (FAQs)

FUJITSU MICROELECTRONICS AMERICA Inc.

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Revision History

Date	Version	Page Count	Change
July 17, 2007	1.4	59	Added more Q&As
May 30, 2007	1.3	54	Added more Q&As
Sep 29, 2006	1.1	50	Corrected Errors and Revised for formatting
Aug 28, 2006	1.0	50	Initial Draft

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1. Fujitsu GDC Overview-FAQs

1.1. What are the target applications for Fujitsu's GDCs?

A: They are mainly designed for automotive-navigation and entertainment applications. However, the GDCs are equally suitable for industrial, medical, gaming, and other embedded applications.

1.2. Do Fujitsu GDCs support alpha blending?

A: Yes, alpha blending is supported on several levels.

- Layers can be set to a uniform transparency level.
- All devices support one alpha plane layer that allows the transparency to be set at the pixel level. MB86297 enables four layers to be designated as alpha planes.
- BitBlt with alpha blending is supported in hardware.
- Primitive drawing can also be done with alpha blending

1.3. Do Fujitsu GDCs support BitBlt (bit block transfers)?

A: Yes, both textures and video can be BitBlt'd.

1.4. Do Fujitsu GDCs support layers?

A: Yes. Up to four layers in MB86290, MB86292 and MB86291, up to six layers in MB86293/4/5 and MB86276, and up to eight layers in MB86297.

1.5. Does any Fujitsu GDC have a PCI bus?

A: Yes, MB86296 and MB86297 feature PCI as the host interface.

1.6. Are Fujitsu GDCs automotive grade?

A: Yes, Fujitsu GDCs meet the automotive cabin temperature range of -40 to +85C for operation and -60 to +125 for storage.

1.7. Can the Fujitsu GDCs be used in under-the-hood (automotive) or military applications?

A: No. A cabin temperature (automotive) range for -40 to +85C is the maximum operating range.

1.8. Do Fujitsu GDCs support Phong shading?

A: No, only flat and Gouraud shading are supported.

1.9. Do the GDCs support anti-aliasing?

A: Yes, they support anti-aliasing for line primitive.

1.10. Can the GDC's external memory interface be connected to a 1.8V memory?

A: No, the interface can only be connected with a memory that supports 3.3V level signals. MB86297 has a 2.5V memory interface (for DDR SDRAM) in contrast with all the other GDCs.

1.11. Do any of the GDCs support gamma correction functions for video input or output?

A: No, that capability is not supported. The probability is very small that an application using one of the GDCs would use that function.

1.12. Do Fujitsu GDCs support direct and color palette modes?

A: Yes, the GDCs support both these modes.

1.13. Do Fujitsu's GDCs support video capture? If so, what is the required video format?

A: Yes, the GDCs support video inputs in RGB and ITU-656 formats.

1.14. What screen resolutions do Fujitsu GDCs support?

A: It varies by the type of GDC. The highest display resolution supported is 1280 x 1024, by MB86297.

1.15. What video output format do the GDCs provide?

A: Fujitsu GDCs output graphics in analog and digital RGB formats, depending on the type of product.

1.16. What type of memory interface do the GDCs have?

A: Currently, the GDCs have a dedicated interface for external graphics memory. Since, this interface is the bottleneck for data traffic in the system, having a dedicated memory interface boosts the graphics efficiency.

1.17. What CPU core does Jade include?

A: It includes AMR926EJ-S CPU core.

1.18. What type of GDC core does Jade include?

A: It includes a GDC core that is based on Coral-PA (MB86296), but has various enhancements to it (two channel video input, two channel video output etc.).

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2. Alpha Blending

2.1. How are the different color-depths from active layers processed internally for layer- and alpha-plane blending?

A: All pixels from the different color spaces (8bit/pixel palette, 16bit/pixel, 24bit/pixel and 16bit YUV) will be converted to RGB888 before any further operation. During this conversion, the lower two bits of the 8bit palette values (from the RGB666 values) will always be set to 00. The three lower bits of the 16bit/pixel (RGB555) values will be set to 000 if the color value is also zero; otherwise they will be set to 111. The YUV values from the video input will be converted to RGB888 using a YUV->RGB conversion matrix. Then the available RGB888 values will be displayed (in a priority order) or blended together with the other layer values. At the output stage, an RGB888 value is available that can be used to drive a display directly or that can be converted to analog using a DAC.

2.2. How are the alpha-blending values calculated?

A: If alpha-blending is enabled for a particular layer, all pixel colors are calculated according to the formula:
C = C1 * A + (1-A) * C2
where,

C is the resulting pixel color
C1 is the 1st layer color
C2 is the 2nd layer color
A is the blending coefficient A=alphavalue/255

Thus,
Alpha=0 -> A=0 -> C = C2
Alpha=255 -> A=1 -> C = C1
Alpha=128 -> A=0.5 -> C=0.5*C1 + 0.5*C2

Note that there are two possibilities:
1.) All alpha-values for one layer can be constant (layer blending mode).
2.) Each pixel can have a different alpha-value (alpha map mode).

2.3. Can MB86297 output the alpha-blending value for each pixel to the video output interface?

A: It is possible if the alpha map layer is being used for layering alpha blending. The alpha-map layer is assigned to one of the two video output interfaces in dual display.

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3. Anti-Aliasing

3.1. Is it possible for all primitives to draw with an anti-alias effect?

A: The anti-alias effect can be used only on lines. If you want to draw a triangle or polygon using anti-aliasing, please draw the objects first, then draw lines along the perimeter with anti-aliasing enabled.

3.2. What kind of anti-aliasing does the GDC use? Are there different modes other than "on" and "off"? There is no description in the specifications.

A: There is just one mode available for anti-aliasing. The GDC uses an unweighted-area sampling algorithm to perform anti-aliasing.

3.3. Does the GDC automatically perform anti-aliasing along the edges of filled primitive areas?

A: No. Area edges must be overdrawn (outlined) with lines to make them anti-aliased.

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4. BLT

4.1. Is it possible to specify the transparent color (not copied color) by BltCopy?

A. It is possible by setting the transparent color to the TColor register in DrawBase + 0x280.

4.2. The area rendered by the Blt command and by the triangle command is different.

A: By default, the algorithm of the triangle and polygon does not render one pixel of the right and bottom edge. We call this algorithm the "Top Left Rule." It reduces the possibility of rendering an edge twice. By using this algorithm, you can render alpha-blending objects correctly.

The algorithm for line and Blt render all the pixels. If you'd like to draw the entire area, you can use the "Non Top Left Rule" command by setting the TL-bit of GMDR2 register. However, the performance of the "Top Left Rule" command is better than the performance of the "Non Top Left Rule" command.

4.3. I tried to copy a 50x50 pixel rectangle with the BltCopyAlt command, but it did not work correctly.

A: The memory width (stride) of the logic frame has to be in 64-bit units. Consequently, the horizontal pixel volume must be of the following sizes:
16bit/pixel mode: 4 multiples (4n pixel)
8bit/pixel mode: 8 multiples (8n pixel)

4.4. The clipping setting does not work with the BltCopyAlt command.

A: The drawing clipping function is not supported in the BltCopyAlt command. Please copy only the required area.

4.5. Note about stride specified in BltCopyAltAlpha operation:

In BltCopyAltAlpha operation, the strides specified should be in 8bytes unit, i.e. the width of source and alpha map should be divisible by 4 (2 bytes per pixel divided by 8 byte unit).

4.6. Does the AlphaBLT operation (XGdcBltCopyAltAlpha) use the alpha bit of the pixel color?

A: No.

4.7. Is AlphaBLT operation supported in 8bpp color mode?

A: No, because the blending operation can result in color values that are not present in the Color LookUp Table (CLUT). Therefore, the operation is not supported to avoid complexity.

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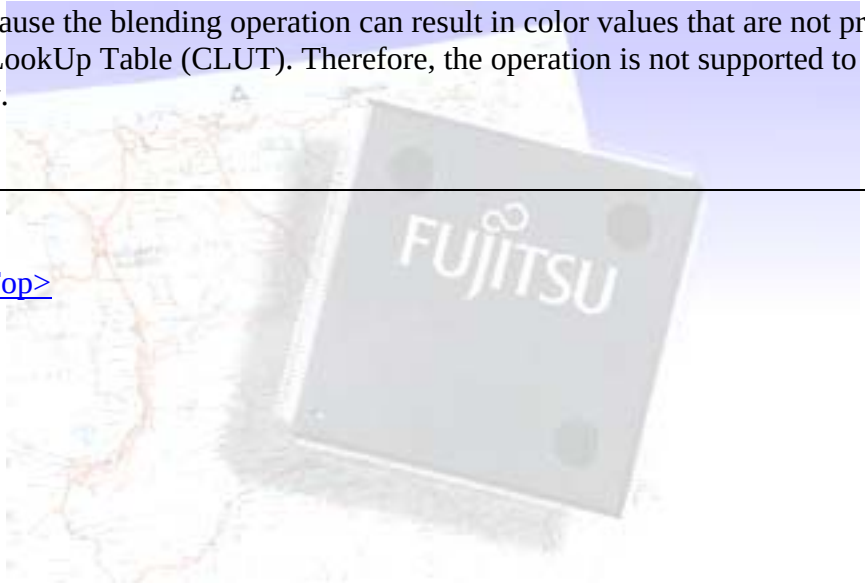

5. Shading & Lighting

5.1. Does the GDC provide any lighting source support or just flat and Gouraud shading?

A: Other than MB86297, the GDCs do not support lighting function.

5.2. I can't draw a line with Gouraud shading.

A: The line command does not support shading effect.

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6. Rendering Texture Maps

6.1. Is it possible to render texture mapping and anti-aliasing in the 8bit/pix mode?

A. Texture mapping and anti-aliasing are supported only in 16bit/pix mode. The complete list of special effects NOT supported in 8bit/pix mode are:

- Anti-aliasing
- Texture mapping
- Rendered alpha blending (The 8bit product will support display alpha blending.)

6.2. The manual of MB86295 says that texturing in 24bit/pixel mode works. Is MB86295 really able to render a 24bit/pixel texture into a 24bit/pixel layer? Or is Coral P only able to render a 24bit/pixel texture into a 16bit/pixel layer?

A: MB86295 devices do not support texture mapping in 24-bit/pixel. Page 91, section 10.4.2, Texture Color is wrong. We will revise it.

MB86293, 4, 5, 6, all support only 8-bit and 16-bit/pixel texture mapping. The reason for this mistake is that this family's ES (the first evaluation chip) supported 24bit/pixel rendering and texture mapping, but this function was removed later.

Note that this applies to MB86276 as well.

6.3. Is it possible to draw stencil texture mapping in 8bit/pixel mode (indirect color mode)?

A: It's impossible to draw stencil texture mapping in 8bit/pixel mode, because there is no way to set the stencil bit in texture data. Please use the 16bit/pixel color mode or transparent color.

6.4. If we have one or two textures that don't change and therefore want to save bus transmission bandwidth, is there a "texture cache" or "graphics local memory" that can be used for this, rather than host system memory as assumed in the PC architecture?

A: There is no permanent memory to store texture and other content permanently. Such content has to be loaded into the SDRAM.

6.5. Are any static-image bit-map-type files such as TIFF, GIFF, .BMP, .JPG or .PNG internally decoded by MB86295? If so, which types are supported?

A: No, MB86295 or other GDCs do not support such formats in hardware. They have to be supported in software by the CPU.

6.6. Where does the coordinate (0, 0) of a texture map align in the texture space?

A: It aligns with the start of the texture map.

6.7. Back face culling

A:

Back Face Culling should be enabled only while drawing one of the triangle primitives. It should not be used with point, line and polygon.

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7. Display Controller

7.1. What should DCLKI be connected to when not in use?

A: Please connect it to V_{cc} or V_{dd}.

7.2. Please show an example of display parameter setting.

A: Please refer to the following table. These are only sample values and the actual setting may be different depending on the display panel's timing specification.

Sample Display Setting

"SC" is the SC bit of DCM0 register. The divisor for 400.06MHz, for calculating the Pixel Frequency, can be calculated by the expression: "2*SC + 2."

Resolution	SC	HTP	HSP	HDP	HSW	VTR	VSP	VDP	VSW
320×200	29	423	350	319	30	262	224	199	2
320×240	29	423	350	319	30	262	244	239	2
360×200	26	470	389	359	34	262	224	199	2
400×200	23	529	435	399	38	262	224	199	2
480×200	19	635	520	479	46	262	224	199	2
640×400i	14	847	700	639	62	262	224	199	2
640×480	7	799	655	639	95	524	489	479	1
640×480i	14	847	700	639	62	262	242	239	2
720x480	6	859	735	719	109	524	505	479	1
720x480i	13	850	722	719	54	262	242	228	1
854×480	5	1061	874	853	125	524	489	479	1
800×600	4	1055	839	799	127	632	600	599	3
1024×768	2	1388	1047	1023	135	805	770	767	5

Note:

- "i" stands for "interlace"
- For interlace video output, the pixel frequency is reduced to half, vertical display timing is reduced to half, and the SYNC bits in the DCM register should be set to 10 or 11.
- If SYNC bits are set to 10, the logical and display frame height should be half of that used in progressive mode. If they are 11, this is not required.

- Pixel Frequency = 400.96MHz / (HTP * VTR * Vertical Scanning Frequency)
- Vertical Scanning Frequency is typically 60Hz for progressive video in the US
- Horizontal Scanning Frequency = VTR * Vertical Scanning Frequency

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7.3. What range of frequencies is guaranteed for the CLK pin?

A: We guarantee the CLK frequency from the standard value to -1% of it.

7.4. Is it ok to use a crystal oscillator that has +/- 100ppm tolerance?

A: Yes, it is ok

7.5. What setting is recommended for the external sync mode?

A: We recommend the following:

- Set both the horizontal (htp) and vertical (vtp) period small.
- To avoid synchronizing the period twice, set the periods small.
- Set HSW to 255 (the maximum size). The display controller waits for a sync pulse in hsw period.

7.6. Does the composite synchronous signal (CSYNC) add an equalizing pulse?

A: It is possible to enable this using "the EEQ bit of the DCM register." Please refer to the specification manual.

7.7. The picture is not displayed correctly.

A7. Check the width of the logical frame. The width must be assigned in 64byte units.

Example:

A horizontal width is 800 pixels in 8bit/pixel mode. 800(pix) x 1(byte)/64=12.5 =>13 (Round up) 13x64=832 (Width of logical frame size). So you have to allocate the horizontal width as 832.

A horizontal width is 800 pixels in 16bit/pixel mode. Therefore, 800(pix) x 2(byte)/64=25, there is no need to round up. And, the width is determined as 25 x 64= 800. So you have to allocate the horizontal width as 800.

Note: By the way, in case of BltCopyAltAlpha operation, the strides specified should be in 8 bytes unit, i.e. the width of source and alpha map should be divisible by 4 (2 bytes per pixel divided by 8 byte unit).

Note: Also refer to this FAQ (Question 10.10).

7.8. How many layers can be used simultaneously with MB86295 without video capture?

A: Coral bandwidth estimation:
Conditions:
Display: Resolution=800 x 480, Dot clock= 33.3MHz,
All layers (windows) have 800 x 480 sizes.
Graphic Memory: Clock= 133MHz, Memory data width= 64bit,
Memory model = SDRAM
Bus Traffic: No video capture, constant drawing operations

Simulation results:
1. 16BPP:0 layers and 8BPP:6 layers => OK
2. 16BPP:1 layers and 8BPP:5 layers => OK
3. 16BPP:2 layers and 8BPP:4 layers => OK
4. 16BPP:3 layers and 8BPP:3 layers => OK
5. 16BPP:4 layers and 8BPP:2 layers => NG
6. 16BPP:5 layers and 8BPP:1 layers => NG
7. 16BPP:6 layers and 8BPP:0 layers => NG

The above values are purely measured from the evaluation board.

The number of layers is limited by the following factors:
- Resolution and speed of dot clock

- Graphics memory bus width (64bit or 32bit)
- Number of display layers and overlapped area
- Color mode of a layer
- Display starting position of a layer
- Bank interleave (Place the each layers frame buffer to different bank)

7.9. How many layers can be used with MB86295 with video capture enabled?

A: It is as follows:

- Resolution: 800x480
- Geometry clock frequency: 166MHz
- Other clock frequency: 133MHz
- Pixel clock: 33.4MHz – (register setting: 0x0b00)
- (Capture-layer-L1) + (16bpp-layer - L0, L2, L3) x 3 + (8bpp-layer-L5, Alpha-plane) x 1

The following conditions are possible to use in the 32-bit bus width with "drawing."
- (Capture-layer) + (16bpp-layer) x 2 + (8bpp-layer) x 1
- (Capture-layer) + (16bpp-layer) x 3

Please also refer to the application note on Coral's display performance.

7.10. The sync registers appear to support higher resolutions than XGA (1024x768). Why is XGA stated as the upper limit? (MB86276 and MB86297 support higher resolutions than XGA)

A: The reason is that GDC's internal clock system is designed to generate only a maximum pixel clock (mentioned in the specification) that can drive XGA display. External synchronization mode will be required to if resolutions higher than XGA are required.

7.11. How many pixels per clock tick can the output interface support?

A: MB86293 (and all other GDCs) can only output one pixel per clock. Glue logic is required if multiple pixels per clock are required.

7.12. What sort of "windowing" or "partition support" does the GDC provide that might be useful for critical-versus-non-critical flight information protection and separation? It is unclear if /how Coral

controls partitioning (protection) of each window to ensure that the information that's supposed to be in one window doesn't get written into another window.

A: GDC has two modes: window and compatibility mode. There is support for up to six or eight layers, which can be independent and resized. Please refer to the specification manual. The partitioning between successive frames is guaranteed by properly assigning memory to the respective layer frames.

7.13. HSYNC/VSYNC default output mode

A:

All GDCs initialize the HSYNC and VSYNC pins as inputs so there is no conflict if the external synchronization mode is used. That is the reason those signals have to be pulled up externally.

7.14. Comment: Display enable signal

After MB86291/2, all the GDCs have unmultiplexed display enable and CSYNC signals on the video-output interface.

7.15. What display timing and other settings are required to convert GDC's video output to NTSC/PAL (interlaced) using an external TV encode?

A:

Only the following settings need to be changed for this purpose:

1. Pixel clock should be reduced to half for that resolution.
2. The SYNC bits of DCM0 register should be set for either Interlace or Interlace Video mode.
3. The vertical display timing settings should remain the same but the horizontal settings should be halved.

As an example, video timing settings for 640x480 progressive and 640x480 interlace are mentioned below:

640×480	7	799	655	639	95	524	489	479	1
640×480i	14	847	700	639	62	262	242	239	2

7.16. Why doesn't the GDC display timing correspond to the indicated values in the timing registers?

A: The start point for HSP has a latency of 14 clocks.

7.17. How many pixels per clock tick can the output interface support?

A: The GDCs can only output one pixel per clock. Glue logic is required if multiple pixels per clock are required.

7.18. When running with external syncs, do HSP, HSW, VSW and VSP need to be programmed?

A: Yes, they have to be programmed.

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8. Video Capture or Input

8.1. There is a noise when the capture function is used.

A: This may be the result of a limitation in the graphics memory bus bandwidth.
The factors affecting graphics memory band width in general are as follows:

- Resolution (Frequency of doc clock).
- Using video capture or not.
- Number of layer and color mode (16 bit/pix or 8 bit/pix) and window size.
- Type of graphics memory (SDRAM or FCRAM). FCRAM provides better performance.
- Width of the graphics memory data bus.
- Frequency of the memory clock.
- Layer overlap in the memory

8.2. How do I read data captured in graphics memory? Is it possible to use captured data as texture data?

A: The beginning address of the latest captured picture can be acquired from the CBOA (Capture Base Address+0x14) register. Please note that MB86294 does not support video texture.

8.3. Is it possible to have simultaneous up-/downscaling with MB86295?

A: In principle, up- and downscaling does work if an odd value is set to CIHSTR. But the first few pixels (nine pixels) are not captured. So the CIHSTR value plus nine pixels are not captured.

Note: MB86295 was not designed for simultaneous up- and downscaling. The Cb data and Cr data are exchanged when up- and downscaling is selected. The reason for the Cb and Cr swap is a different latency between up- and downscaling. If the CIHSTR register is set to an odd value, it will overcome this problem with the restrictions mentioned above. This will be corrected in Coral PA. The first few pixels of each line at each frame are missing. Therefore, it seems like the frame is shifted to the left. This phenomenon occurs only at the combination of up- and downscaling (e.g., horizontal upscaling and vertical downscaling).

(TA: -40 to +85 deg C, VDDL: 1.65 to 1.95V, VDDH: 3.0 to 3.3V)

Not all the pixels are captured as explained, but the capturing and displaying process is stable. The WEAVE mode cannot be used in vertical upscaling mode. So if vertical downscaling and horizontal upscaling are selected, the WEAVE mode can be used. But there is the same restriction as in the BOB mode. (The first few pixels are not captured.)

8.4. What should I do with the unused YUV input pins?

A: If you are not using video capture, you have to set these signals to "High" or "Low." However, in the case of MB86294 and 5, the video-capture signals are multiplexed with the graphics memory bus. Therefore, please connect to the "high" or "low" level by the pull-up/down resistor. In case of MB86291, the video-capture signals are not multiplexed with the memory bus. Therefore please connect to "VDD" or "GND" directly.

Additional information: If unused video-input pins are left open, it is the same as for all CMOS devices. Leaving pins open can destroy the pad cells by static electricity, latch-up, or from direct tunneling current.

8.5. Does MB86295 provide any capability to lock to an external sync sources for primary vertical sync and horizontal pixel output? If so, what are the limitations on range, if any, of this sync rate? Is this software programmable?

A: Yes. Please refer to the AC specification of the video interface signals on page 303 of the specification manual.

8.6. What technique is used to reconstruct the decimated chroma information for 4:2:2 video inputs?

A: If you are referring to RGB-to-YCbCr conversion, please refer to page 76 of the specification manual.

8.7. What is the pin assignment for the RGB888 (multiplexed) video input of MB8695? In the manual only the direct RGB666 video input is explained.

A: The pin assignment is shown in the following table:

Direct	Multiplex
GI [5] GI [4] GI [3] GI [2] GI [1] GI [0]	GI [7] GI [6] GI [5] GI [4] GI [3] GI [2]
IBI [5] IBI [4] IBI [3] IBI [2] IBI [1] IBI [0]	RB [7] RB [6] RB [5] RB [4] RB [3] RB [2]
IRI [5] IRI [4] IRI [3] IRI [2] IRI [1] IRI [0]	RB [1] RB [0] GI [1] GI [0] COLSEL

8.8. What are the maximum limits on the video input size?

A:

- ITU-R BT.656 input: The limits are as specified in the standard specification. Basically, the maximum size is 720 x 486 (525/60; NTSC) or 720 x 576 (625/50; PAL).
- RGB input:
  - RGBCLK = 80 MHz
  - RGBVEN = 4096 (Max V. size)
  - RGBHEN = 840 (Max H. size. This is due to the limitation of the line buffer size in the video capture module.)

8.9. What is the new function of the CBM register in MB86295?

A: CBM register (Address: Capture Base+0x010)
Bit-0, CBST (Capture Burst) bit

Select the burst length for writing the captured data to the graphics memory. This function is used when saturation has occurred.

CBST=0 Default (4 words burst)
CBST=1 Long Burst (8 words burst)

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9. Memory (including interface)

9.1. Can you show a sample circuit diagram for connecting the GDC and graphics memory?

A: Please refer to the circuit diagram of the evaluation boards. Our recommendation circuit is should only be consider a sample as may not take into account every design consideration.

Note: The serial resistor is for reducing ringing noise. Other resistors are for adjusting the timing. Actually, the resisters are not mounted on the evaluation board, but these wires are printed to adjust the timing. The GDC was designed so that it can connect directly to memory. However, the clock frequency is fast, so one should consider "impedance matching," "noise cut," etc., when designing the PCB. We recommend simulating by using IBIS data to take care of these factors.

9.2. How should the bank address pins of the SDRAM be connected to MB86296 or any other GDC's memory interface?

A: They can be connected to the MSBs of the memory address bus. For example, in the case of Micron's MT48LC8M32B2 - 2 Meg x 32 x 4 banks, the BA0 and BA1 can be connected to A12 and A13 respectively.

9.3. What memory can be connected to MB86296? How is it connected?

A: The memory controller of MB86296 supports a simple connection to SD/FCRAM by setting MMR (Memory Mode Register). If there are N(=11 to 13) address pins in SD/FCRAM, connect the SD/FCRAM address (A[n]) pin to Coral's memory address (MA[n]) pin and the SD/FCRAM bank pin to Coral's next address (MA[N]) pin. Then set MMR by the number and type of memory.

The following is the connection table between the MB86296 pin and SD/FCRAM pin.

64M bit SDRAM (x16 bit)		64M bit SDRAM (x32 bit)	
Coral	SDRAM	Coral	SDRAM
MA[11:0] MA12 MA13	A[11:0] BA0 BA1	MA[10:0] MA11 MA12	A[10:0] BA0 BA1
128M bit SDRAM (x16 bit)		128M bit SDRAM (x32 bit)	
Coral	SDRAM	Coral	SDRAM
MA[11:0] MA12 MA13	A[11:0] BA0 BA1	MA[11:0] MA12 MA13	A[11:0] BA0 BA1
128M bit SDRAM (x16 bit)		128M bit SDRAM (x32 bit)	
SDRAM	Coral	SDRAM	Coral
MA[12:0] MA13 MA14	A[12:0] BA0 BA1	MA[10:0] MA11	A[10:0] BA

9.4. Does Coral provide any kind of memory error detection?

A: No, it does not.

9.5. Is the frame buffer cleared automatically when swapping buffers or is a command needed?

A: The frame buffer has to be cleared manually by using the BLT command with any drawing color. If the color used is transparent, you will be able to see the content of the layers that lies below the cleared one.

9.6. Since the accompanying graphics memory array can be very large, does the GDC provide any kind of hardware accelerated memory test that can be activated by software on the memory array?

A: No.

9.7. Coral only appears to have 15 memory address lines, yet the spec says it can address 64M of memory. How does this work?

A: It works by using the MRAS and MCAS pins.

9.8. Is the graphics memory a unified structure or distinct for the various types needed? What are the maximum supported allocations for frame buffer, textures and stencils, and how are they "controlled" when setting up the chip?

A: The memory is a unified structure and the software must keep track of the memory assignments for display lists, textures, bitmaps, frame buffer, etc. Please also refer to the graphics memory chapter of the GDC's specification manual.

9.9. MB86297's DDR-SDRAM has only been characterized for memories up to 256Mbit.

A: Beyond that, it might be possible to use that particular memory part. However, Fujitsu cannot confirm or guarantee the operation.

9.10. What is the function of the LOOP input and output signals on MB86297's DDR SDRAM interface?

A: They are related to the DLL (Digital PLL) used in the memory controller block to adjust clock phase.

9.11. Does Coral provide any kind of memory error detection?

A: No, it does not.

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10. Drawing Engine

10.1. Do the GDCs support concave polygons?

A. Yes, they do. The concavity is controlled while specifying the vertices.

10.2. Is it possible to draw a broken bold line perpendicularly along the direction of a line?

A: In MB86296, it is possible to draw the beginning and end points and pattern perpendicularly along the direction of a line. In the previous generation products, the method was to draw the lines perpendicularly along the direction of the x- or y-axis.

10.3. Can the GDC generate rounded end points for lines or only square?

A: No specific functionality is implemented to generate rounded end points for (thick) lines. However, it might be accomplished using polygons.

10.4. The specification uses the terms "line edging," "border primitive" and "shadow primitive" in reference to line drawing (pages 233, 234 and others). Can you define each of these terms, explain if they are unique entities, and describe what controls (shadow width or color, for example) over them are available?

A: For an explanation of body and shadow primitive and edging, please refer to sections 10.7 and 10.8 of the specification manual.

10.5. Please explain border primitive.

A: The edging line is drawn by the combination of body and border primitives; these rendering attributions are set by the MDR1 and MDR1B register. Please refer to "1.12.2.1: Shadowing Line drawing" and "1.12.2.2: Edging Line Drawing" in the application note.

10.6. What is a "non-top-left applicable primitive"? This is referenced for both line and polygon drawings.

A: Basically the rendering algorithm of triangle and polygon in the GDC is the "top-left algorithm." But Coral has both "top-left" and "non-top-left" algorithms. Please refer to the "1.13: Triangle Drawing" in the application note.

10.7. What are the differences between high-speed and regular line and triangle drawing? Is there an equation for the estimated speed improvement between the methods?

A: High speed implies a faster execution of the same algorithm, i.e. the algorithm of a high-speed line and regular commands is the same. The two commands are differentiated by their relative utilization of the CPU and the GDC. The drawing is divided into three stages: Transform, Set-Up, and Render.

MB86296 has three types of drawing commands.

- *Geometry Command*: Coral performs **Transformation**, **Set-Up** and **Rendering** and the CPU has to simply send the commands.
- *Set-Up Command*: Coral performs **Set-Up** and **Rendering** and the CPU has to calculate **Transformations**.
- *Rendering Command*: Coral performs **Rendering** only, so the CPU has to calculate **Transformations** and **Set-up**.

Notes: Number 2 and 3 refer to MB86290 (an earlier-generation Fujitsu GDC) compatible commands. (MB86290 does not have a geometry processor. MB86296 is equipped with a geometry engine so these modes are probably not useful unless you are migrating up from an MB86290 device and do not want to make extensive code changes.)

The high-speed line is described in number 2 above (Set-Up" command).

In terms of execution time, “1” is the fastest and “3” is the slowest. Therefore, the high-speed line corresponds to categories 1 or 2, whereas the regular line corresponds to category 3.

10.8. The interrupt list indicates a drawing command error. Where is there a list of possible causes?

A: You will have to inspect your code manually for errors.

10.9. What is the restriction on logical and drawing frame width?

A: The frame width should be 64-bytes aligned (meaning that the width should be a multiple of that value). The logical and drawing frame widths should be divisible by 16 if the resolution is 24 bpp, by 32 (2 bytes pp / 64) for 16bpp, and by 64 aligned for 8bpp color depth.

10.10. What are other restrictions on the boundaries of data types?

A: The horizontal size of the display original address must be in 64-bytes units. Basically the display frame and drawing frame is the same. And, regarding the BLT commands, the XRES, source stride, destination stride, must be in 8-bytes units.

10.11. Does the order of vertices/coordinates matter in polygon drawing?

A: As long as it does not make the sides intersect, it does not matter what the order is.

10.12. What operations use the alpha bit (MSB) of the pixel color?

A: Only layer blending and texture blending use this bit.

10.13. GDC vertex data format for MB86296 (Coral-PA).

A:

Geo Engine: Float, Fixed Point, and Integer
Rendering Engine: Fixed Point and Integer

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11. Host Interface (and other non-memory signals)

11.1. Does MB86296 use a 5V or 3.3V PCI interface?

A: It uses 3.3V only PCI interface.

11.2. How can the pins of the PCI bus be put in tri-state mode?

A: The following conditions are required in order for each pin to be in High level, Low level, and High Impedance (Tri-State).

AD0..31, CBE0..3, PAR, FRM, IRDY
- Hi level: When Coral operates as PCI master read/write burst.
- Low level: When Coral operates as PCI master read/write burst.
- Hiz: Under reset or after reset.

TRDY, STOP, DSEL
- Hi level: When Coral operates as PCI slave read/write.
- Low level: When Coral operates as PCI slave read/write.
- Hiz: Under reset or after reset.

REQ
- Hi level: After reset.
- Low level: When Coral operates as PCI master read/write burst.
- Hiz: Under reset.

PERR
- Hi level: When Coral operates as PCI slave read/write.
- Low level: When Coral operates as PCI slave read/write and parity error occurs in the data phase.
- Hiz: Under reset or after reset.

SERR (open drain)
- Low level: When Coral operates as PCI slave read/write and parity error occurs in the address phase.
- Hiz: Under reset or after reset.

XINT
- Low level: When interrupt occurs.
- Hiz: Under reset or after reset.

11.3. What is the effect of a reset (XRST, Firm RESET) on to the pin voltage levels?

A: The various pins have the following levels after reset.

AD0-31	HiZ
CBE0-3	HiZ
PAR	HiZ
FRM	HiZ
TRDY	HiZ
IRD	HiZ
STOP	HiZ
DSEL	HiZ
PERR	HiZ
REQ	Hi level
SERR	HiZ
XINT	HiZ

11.4. What happens if MB86296 does not get a bus grant after it issues a REQ demand?

A: If MB86296 does not get a bus grant after it issues a REQ demand, Coral continues waiting for the bus grant. In the meantime, it is possible to access Coral as a PCI slave.

11.5. Coral PA 66MHz operation – bus speed comparison in MB per sec

A:

	Coral P(33MHz)	PA(33MHz)	PA(66MHz)
slave write	28.0	89.2	83.2
slave read	27.5	54.1	70.8
slave write BCU	26.8	62.6	66.5
slave read BCU	30.5	33.6	41.2
master read BCU	29.2	29.2	40.6
master write BCU	28.2	28.2	36.5

11.6. Note: When the 16-bit-wide host bus is used, MB86276's memory address space reduces to 16 Mbytes.

11.7. Will MB86296's or any other GDC's I^2C Master interface conflict with other Master devices present on the same I^2C bus?

A: The following measures take care of any such conflicts:

1. Synchronization of SCL line: If two I^2C devices become master at the same time, each device senses the state of the SCL line and adjusts this line's timing automatically in accordance with that of the device becoming Master the last.
2. Arbitration: If two I^2C Master devices start sending data at the same time, the arbitration mechanism in I^2C makes sure that no conflict occurs.
3. If an I^2C Master is not driving the bus then it is similar to that device not being present at all. There will not be any problem with other I^2C Masters communicating on the same bus.

11.8. Is there a recommendation from Fujitsu regarding the bypass capacitors for the GDC's power supply pins?

A: There is no such specific recommendation from Fujitsu. The values and configurations of these bypass capacitors used in the Fujitsu evaluation boards may be treated as a reference.

11.9. What are the general recommendations for GDC's parallel host interface?

A:

- If BCLKI = 100MHz, internal PLL output should not be used by setting CKM=H.
- BS mode is always recommended.
- When using a non-BS mode, a slower clock (66MHz or so) and ample wait states (3) should be used.
- 66MHz BCLKI is also recommended in BS mode.

11.10. What is the difference between SH3, SH4, and V83x modes?

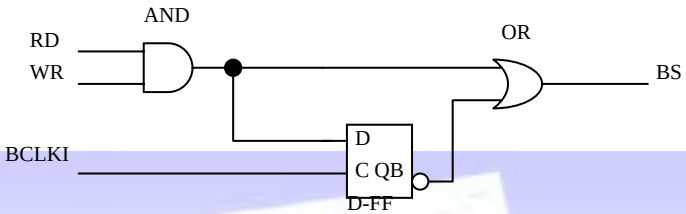
A: It is given as follows. Note that this applied to the 32-bit non-PCI legacy modes in the GDCs.

1. SH4 Mode:
    - CPU access:
        - Write (8,16,32 bit)
        - Read (32 bit only)
    - Memory Map Area: 64MB
    - XRDY pin:
        - low level: ready
        - high level: wait
    - DMA:
        - Single or Dual address DMA
        - 1 or 8-long double word transfer
2. SH3 Mode:
    - CPU
        - Write (8,16,32 bit)
        - Read (32 bit only)
    - Memory Map Area: 64MB
    - XRDY pin:
        - low level: wait
        - high level: ready
    - DMA:
        - Dual address DMA
        - 1-long double word transfer
3. V83x Mode:
    - CPU access:
        - Write (8,16,32 bit)
        - Read (8,16,32 bit)
        - A24 pin works as XWR (write enable)
        - XWE [3:0] pins work as byte enables
    - Memory Map Area: 16MB
    - XRDY pin:
        - low level: ready
        - high level: wait
    - DMA:
        - Dual address DMA
        - DTACK pin works as XTC (DMA transfer end signal).
        - DRAK pin works as DMAAK (DMA acknowledge signal)
        - 1-long double word transfer

11.11. How should the XBS signal be treated in the no-BS signal mode?

A: It should be pulled high. It is always recommended to use the BS (Bus Start) mode, even if glue logic is needed to generate it.

Note that the BS signal can be generated using a glue logic such as shown below.



11.12. Is it ok to have more wait states than required for the SRAM type host interface?

A: Yes, but only in the Normally Ready Mode. For the Normally Not Ready Mode, the exact number of states, as mentioned in the GDC specification, should be used. For details of the various host interface modes, please refer the GDC specification document.

11.13. Can CS be held for multiple read/write accesses?

A: Yes.

11.14. How does the BS signal relate to the RD and WE signals going low?

A: The RD (or OE) and WE signals must be asserted 1 clock cycle (this is fixed) after BS. (Please see the attached word document for explanation). You should make sure that the setup and hold times are according to the GDC's AC spec.

11.15. Is RD or WE signal expected to be low before the rising clock after BS is asserted low?

A: The sampling of RD (OE) and WE signals is done at the rising BCLK after BS.

11.16. When does a cycle start the falling edge or rising edge of BS?

A: BS is sampled at the rising BCLK with CS asserted (held low). This means that BS is valid when CS is low. Therefore, the bus cycle starts at that point in time.

11.17. What is the minimum and maximum amount of time that the BS signal is asserted low?

A: The amount of time BS is asserted low is approximately one clock cycle. The setup and hold times for the BS signal are as specified in the data sheet.

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12. Development Tools

12.1. What are the various evaluation board part numbers?

A: The part numbers are: MB86296 (MB86296EB01), MB86297 (MB86297EB01), and MB86276 (CREMSON-STARTERKIT-LIME).

12.2. What is the composition of the boards?

A: MB86296 and MB86297 evaluation boards are PCI adapter cards. These boards can be used on a Windows (2000 for Coral PA and XP for MB86297) PC with Visual C++. MB86276 has a standalone board that connects to a Fujitsu MCU board.

12.3. What kind of OS is used on the PC for controlling the PCI boards?

A. Windows NT/2000 is the OS for which the GDC Library has been ported to for evaluation and development.

12.4. Do you have a reference design (example schematic) and any PCB layout guides?

A: Yes, they are available in the form of schematics for the evaluation boards (MB86295EB01 and MB86296EB01). Specific PCB design guidelines are available for MB86297. Please contact your Fujitsu support person.

12.5. Are any simulation models available?

A: IBIS model is available. BSDL model is available for MB86297.

12.6. Comment: Please be aware of the following regarding Lime Starterkit:

- A [25:2] on the CPU connector of the board is mapped to A [23:0] of MB86276. Therefore, when connecting a CPU board with Lime Starterkit, connect A2 of the CPU's address bus with A2 of that of the Starterkit's connector.

- You might need to pull up CS2 in order to connect the Lime Starterkit with a CPU board different from the one provided by Fujitsu.

12.7. The MB86297 evaluation board does not seem to follow the PCB design guideline document.

A: That is correct. In any case, please follow the recommendations of the PCB design guideline.

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13. Display List

13.1. Does the GDC provide any kind of “end-of-display-list” processing indication? If so, how and when does it occur (after receipt of the final command, when the pipeline is empty, when the final pixel rendering is complete, etc.)?

A: Yes, by observing the bit-1 of the IST register. Please refer to the GDC manual for details.

13.2. Does the GDC provide any kind of error detection of the display list commands or internal register access? If so, what kind of error event or “program counter” capture type of information is recoverable for debug purposes of the location and type of fault?

A: Yes, the GDC provides that information through the registers: 1-IST, 2-GCTR (doesn’t exist in MB86276), 3-CTR. Please refer to the GDC specification manual for information about these registers.

13.3. For command or address errors, is there any way to determine which command in a list or what invalid address respectively caused the error?

A: No, you have to check your code.

13.4. What is the maximum number of nested display lists (similar to subroutine depth) that the GDC can handle?

A: The display list is not nested.

13.5. Is there a “display list cache” or “graphics local memory” that can be used for storing short, reusable, unchanging display lists rather than the host system memory as assumed in the PC architecture?

A: The display list has to be loaded each time into the display list memory (external SDRAM) after the power is turned off. There is no internal cache or permanent memory available for such use.

13.6. Can the GDC store a display list permanently?

A: No, it cannot. The CPU has to arrange for permanent storage of the display list.

13.7. Is the BltDraw or Bitmap data transferred directly from CPU memory to the graphics memory or through the display list FIFO?

A: This data is transferred through the display list FIFO after it becomes a part of the display list. It is possible to write the data from host memory directly to the drawing frame in graphics memory. However, this approach requires the application to ensure that the operation is synchronized with other graphic function calls from the application.

13.8. How deep is the Display List FIFO in the GDCs?

A: Carmine has a 64 step deep FIFO. All the other GDCs have a 32 step deep FIFO.

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14. Interrupts and Errors & Messages

14.1. What does “Internal Bus/FIFO timeout” mean? Can this event, or any other detected fault, be made to activate a GPIO without host processor interaction?

A: It means that an unexpected delay can occur while accessing GDC’s internal bus. This is indicated through the interrupts reported by the IST and TCS registers. The IOM register can be set up to report this error through the GPIO. However, the processor has to interact and set up the IOM register. “Internal Bus/FIFO timeout” is for our internal debugging use only. Therefore, this section has been removed from the latest document.

14.2. What types of command errors generate the CERR interrupt?

A: It is generated by errors that occur while the display list commands are executed; e.g., if an incorrect command code is specified while making the display list.

14.3. What types of sync errors generate the SYNCERR interrupt?

A: It is generated when there is a lack of synchronization of the external video sync signals (VSYNC and HSYNC). This is when DCLKI is used instead of the dot clock generated by the internal PLL.

14.4. The interrupt list indicates a drawing command error. Is there a list of causes of this error?

A: You have to inspect your code manually for errors.

14.5. Can the software generate both a “hard” and “soft” reset of the part?

A: Yes.

14.6. Note: Enable interrupts, IMASK register:

A: The description in the hardware manual is wrong.

The correct information is IMASK

- 1: Not mask
- 0: mask

Set the bit to 1 to enable the according interrupt. By calling the function "GdcGeoSetInterruptMask," the parameter is set to the IMASK register (e.g., enable command interrupt GdcGeoSetInterruptMask (0x2)).

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15. Clock Related

15.1. DCLKO Duty-Cycle :

A: A duty of the DCLKO signal made by an internal PLL output depends on the setting of the SC bit in the DCM/DCEM register. If you set the scale value to the SC bit of DCM register, the duty of the DCLKO signal is always 50%. If you set the scale value to the SC bit of the DCEM register, it is dependent on the scale value. If the frequency division rate is an even number, the duty is 50%. If it is odd number, the pulse ratio of L:H is (n+1):n.

(Example)
1)SC bit of DCEM = 12 (Frequency division rate = 1/13)
L:H of DCLKO => 7:6

1)SC bit of DCEM = 36 (Frequency division rate = 1/37)
L:H of DCLKO => 19:18

Note:
The following values are not considered PLL jitter.
Regarding PLL jitter, please refer to the hardware manual.
If you need an exact 50% duty-dot clock, please input the clock from the DCLKI pin.

15.2. Regarding the internal PLL, I need to use a PLL frequency of 398MHz to get the correct display timings. According to the GDC specification, it is possible to use a 14.22MHz oscillator (allowed range for CLKSEL= 01 is 14.177...14.32MHz). The question is: will the PLL generate 14.22MHz * 28 = 398.16MHz internally or will the PLL output 400.909MHz anyway in this mode?

A: The PLL generates 398.16MHz when 14.22MHz. Please do take into consideration the duty of DCLKO.

15.3. DCLKO Jitter

Aa: 1. If the Clock comes from the internal PLL:
Although it depends on the stability of the supplied power for the PLL, the reference values are as follow.
PLL jitter * ((PLL clock dividing value)^(1/2))

Ab: If the Clock is given via DCLKI:
If DCLKI does not include jitter, DCLKO also does not include jitter. These specs assume that the ideal input clock is given.

15.4. What is the time relation (delay) between DCLKI and DCLKO in the external display clock mode?

A: This delay time is not controlled as a spec; it is different with each product series. We show them as reference values. For MB86295, the max=11.1ns and the min=5.4ns.

15.5. After changing the geometry engine COT clock frequency for the device, is a stabilization period required to maintain proper operation? Can it be changed while drawing?

A: Please refer to section 3.1 of MB86296 specification. This applies to other GDCs as well. The stabilization period is 200usec. No, it cannot be changed while drawing.

15.6. What is the level of the clock input pin (CLKIN) of the GDC?

A: The CLKIN pin has a 3.3V level. On the evaluation board, the CLKIN pin is connected to the 74LVC04APW. This chip is a 3V device, but it is also possible to use a 5V swing.

15.7. What range of frequency is guaranteed for the CLK pin?

A: We guarantee CLK frequency from standard value to minus 1%.

15.8. What setting is recommended for the external sync mode?

A: We recommend the following:

- Set both the horizontal (htp) and vertical (vtp) periods to small or little.
- To avoid synchronizing to twice the period, set the periods to small.
- Set hsw to 255 (max size).
- The display controller waits a sync pulse in hsw period.
- To make synchronization easier, set hsw to 255 (max size).

15.9. Is it possible to use a standard crystal, instead of non-standard oscillator (as the Evaluation Boards use), with the GDCs?

A: No, the GDCs do not support standard crystals.

15.10. Is it possible to use CLK values other than those listed in the GDC specification manual?

A: No, only the values listed in the specification manual (14.31818MHz etc.) may be used. The tolerance level is the specified value to -1% of it.

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16. Package

16.1. What is the package type?

A: The various package types used are.

MB86291	QFP208
MB86292	QFP256
MB86293	QFP256
MB86294	QFP256 / BGA256
MB86295	BGA256
MB86296	BGA256
MB86276	BGA256
MB86297	TEBGA543

16.2. In addition to the normally specified external package dimensional parameters for MB86295, we need the package-related information listed below.

A: This GDC is basically a “lead-free package,” so the parts number is “MB86295SPB-GS-BND-E1.” The comments are based on “E1” (lead-free package). Other GDCs from Fujitsu are also lead free.

The following relate to the MB86295.

16.3. Substrate type and material (ceramic, laminate, FR-4, etc.)

A: FR-4

16.4. Dimensions of internal cavity, die, and relation to solder ball arrays.

A: Sn-Ag-Cu Ball

16.5. Any field moisture sensitivity data available or HAST data.

A: It is available upon request.

16.6. Thermal parameters (Tj max, theta junction-to-case, etc.)

A: Theta j-a = 22.5deg/W(0m), Theta j-c = 2.43deg/W

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17. Power Consumption & Thermal Characterstics

17.1. What are MB86293's temperature characteristics?

A:

- Thermal resistance junction – package: 16 degC/W
- Maximum junction temperature: 117 degC
- Maximum power dissipation
  Typical (measurement eva-board, Host I/F: 33MHz, GE: 166MHz, OT: 133MHz)
  1.8V: 480mA
  3.3V: 50mA
- Maximum (Host I/F up to 100MHz)
  1.8V: 960mA
  3.3V: 200mA

17.2. What voltages do MB86296 use, what tolerance is required, and what levels of current are needed for them?

A: 1.8V (core) +/- 7%, 3.3V +/- 10%. The current consumption is 500mA for 1.8V and 100mA for 3.3V. The typical conditions for the current consumption are Geo Engine Clock: 166MHz and Rendering Engine Clock: 133MHz.

17.3. What is MB86276's current consumption value?

A: MB86276's typical current consumption is 1.8V: 170mA and 3.3V: 50mA. As a reference for designing the PCB, Fujitsu recommends maximum current consumption as 1.8V: 500mA and 3.3V:100mA.

For other GDCs' current consumption number, please see the GDC Feature Matrix on FMA's GDC web site.

17.4. What is MB86297's power consumption?

A:

Minimum power consumption of Carmine is 350mW. It is under the condition when all internal clocks are stopped (the clocks that can be stopped using software).

The following results are worst-case power consumption. The data is measure using Fujitsu's Evaluation Board.

Conditions:

Ta = 27oC
Power Supply Voltages = 1.3V, 2.7V, 3.3V
Capture0= Camera (NTSC)
Capture1= Play Station (NTSC)
Display0= 8 layer (L0=image, L1=cap0, L2-L7= image & flip), SVGA
Display1= 8layer (L0=image, L1=cap1, L2-L7= image & flip), SVGA
Draw Operation= Geometry alpha texture repetition of depth test draw

Power consumption= 2.233W

17.5. What is the junction temperature figure of MB86295?

A: The thermal resistance of MB86295 (BGA) is:

- Theta j-a = 22.5 degree/W
- Theta j-c = 2.43 degree/W

Then you can calculate the junction temperature like the example below.

- Tj (Junction temp)= P * Theta j-a + Ta
- Tc (Package surface temp)= Tj - Theta j-c * P

P: Power consumption (W)
Ta: Ambient temperature (Deg)

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18. Miscellaneous FAQs

18.1. What is the initialization or bring-up routine of the GDC?

A: We recommend the following sequence:

- Set the CCF (change of clock frequency) register
- Wait for a time equivalent to 100 bus cycles
- Issue a software reset
- Wait for a time equivalent to 100 bus cycles
- Set MMR (Memory Mode Register)

Note: Before accessing the graphic memory, please set the MMR register. Fujitsu can provide a sample program, which doesn't use the graphics driver. Please refer to the manual and application note about the details of each register.

18.2. Do the GDCs support the IEEE 1149.1 boundary scan?

A: The GDCs don't support boundary scan. The new devices, Carmine and Jade, do support JTAG scan.

18.3. How should unused I2C pins in the GDCs be treated?

A: Unused I2C pins (SDA, SCL) must be pulled up.

18.4. Does the GDC provide any kind of internal test (Built In Self Test) that can be activated by software or is automatically performed after a reset that verifies the chip is operational? How long does it take to run?

A: GDCs don't have internal test (BIST) functions.

18.5. If the GDC graphics pipeline were to "lock up," is there a way to detect this? If a lockup occurs, does the frame buffer memory refresh continue? Does the frame buffer pixel output to display continue?

A: The lockup is detected by checking the IST and TCS registers. In such a case, the frame buffer is not updated. However, the display refresh continues.

18.6. What is a "miller register" or is this just a typo?

A: It's actually a typo: Miller = mirror

18.7. Does the chip have any kind of identification register or signature that can be accessed by software to identify it from other things on the bus?

A: Yes, please check the CID register, a host interface register. Most of our GDCs have it.

18.8. What will happen if the chip is powered up at -55 C and held in reset with the clock(s) operating? Will the chip operate properly if the reset is released when the chip is warmed to -40 C? Will the chip draw increased power during this period of time?

A: The chip should operate properly. Please refer to the thermal parameters. We don't have any data regarding the time to heat up.

18.9. What is the purpose of the pins TEST, DACT, MST, XSM, SMCK and XTST?

A: They are for Fujitsu's internal use only. Please provide them with 3.3V input (pull-up).

18.10. Does the GDC provide any error detection of display list commands or internal register access?

A: Yes, this information is available through the IST, GCTR and CTR registers.

18.11. Unused pin treatment in general

A:

- input pins: Pull down
- output pins: Leave open
- input/output pins: Pull up or pull down depending on the active level.

The greater the resistance value, the better it is. Fujitsu does not recommend any specific resistance value.

18.12. Is there any signal sequencing requirement while powering-off the GDC?

A: No, there is no such requirement. The only precaution is to make sure that VDDH alone is not kept turned on for more than a few seconds.

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