Using the Dual Cast™ Feature on PEX 86xx Gen 2 PCI Express Switches

Application Note

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Website: www.plxtech.com
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Introduction

This application note describes the functions and programming of the Dual Cast feature available on PLX PEX86xx series Gen 2 PCI Express switches. A typical system configuration and register programming example is also provided.

The Dual Cast feature, in short, allows programs to write the same data to two different destinations at the same time. Whenever posted memory write TLPs entering the switch through a designated port, called the Dual Cast Source Port, are addressed to designated regions of memory, called Dual Cast BARs, the switch automatically generates a copy of the original TLP, called the Dual Cast Copy TLP, replacing the original TLP's address with one that is mapped to an egress port designated as the Dual Cast Destination Port.

When an incoming TLP is copied in this fashion, both the original TLP and Dual Cast copy TLP are queued at their respective egress ports at the same time, effectively doubling the egress rate of the switch for the same rate of ingress.

1. Dual Cast System Model

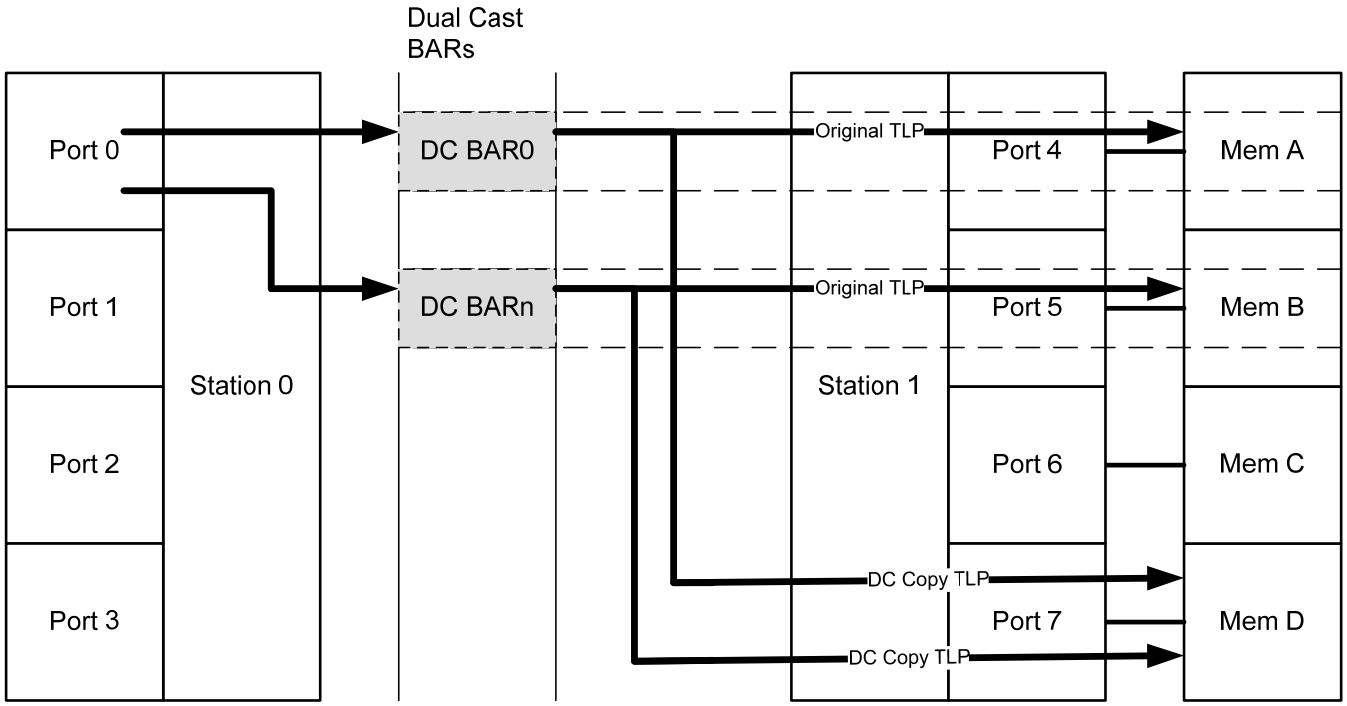

Figure 1. Typical Dual Cast System Model

Dual Cast functions are illustrated in Figure 1. This figure illustrates a port/station configuration available in the PEX 8648 or PEX 8633, but the concept extends to all devices in the PEX 86xx family. In this figure, the designated Dual Cast Source port is Port 0. Only memory write TLPs that enter the switch through this port (or alternately, any port of a designated station) will be subject to dualcasting. Dual Cast control registers allow the programmer to define up to eight separate regions of memory, called Dual Cast BARs, over which Dual Casting will be applied. If a memory write TLPs enters the switch through the designated Dual Cast Source Station/Port, AND its header address falls within an active Dual Cast BAR, then the switch

automatically generates a Dual Cast Copy TLP, replacing the original TLP's header address with a new address mapped to the designated Dual Cast Destination port, in this case Port 7.

Dual Cast BARs can be mapped to any egress port of the switch. In other words, original memory write TLPs that are being copied can exit the switch on any egress port, as they would normally. However, Dual Cast Copy TLPs, regardless of which Dual Cast BAR generates them, must all exit the switch through the designated Dual Cast Destination port.

The Dual Cast Destination port can also be configured as NT (non-transparent). See section 4 for additional programming requirements.

2. Dual Cast Control Registers

This section describes each of the Dual Cast control registers. There are eight sets of identical registers, used to describe each of the eight Dual Cast BARs, and one single register that is used to specify Dual Cast Source and Destination ports. These registers are described in detail in the following subsections. See the data book for a register address table.

2.1 DualCastLowBAR0-7[31:0], DualCastHighBAR0-7[31:0]

These registers are used to define the 64-bit physical base address of each of the Dual Cast BAR address windows, numbered 0-7.

DualCastLowBAR*n* contains the low 32-bits of the base address of Dual Cast BAR window *n*. Only the upper 12 bits (31:20) of this register are used to specify address. Bits 19:0 of this register are not de-coded, and are hard-wired with the value 0x00.000c. Thus, Dual Cast BARs will be naturally aligned on 1MB boundaries. Since 1MB boundary is also a 4K boundary, any memory write TLP that falls within the Dual Cast BAR's address range will be guaranteed never to exceed the top of the DC BAR*n* range

DualCastHighBAR*n* contains the upper 32-bits of the base address for Dual Cast BAR window *n.* For base addresses in the lower 4 GB or for all 32-bit systems, this register should be cleared to 0h (default).

2.2 DualCastLowBARSetup0-7[31:0], DualCastHighBARSetup0-7[31:0]

These register pairs form a 64-bit value used to define the size of the Dual Cast BAR window, which increases in powers of 2 in size starting from 1 MByte. The size of the address window is determined by the number of 1s bits set, starting from bit 63 down to bit 20. For each bit that is 1, the copy TLP's header address bit will be replaced by the corresponding address bit in the DualCastLow/HighBARTranslation0-7 registers. This is illustrated in Figure 2 below.

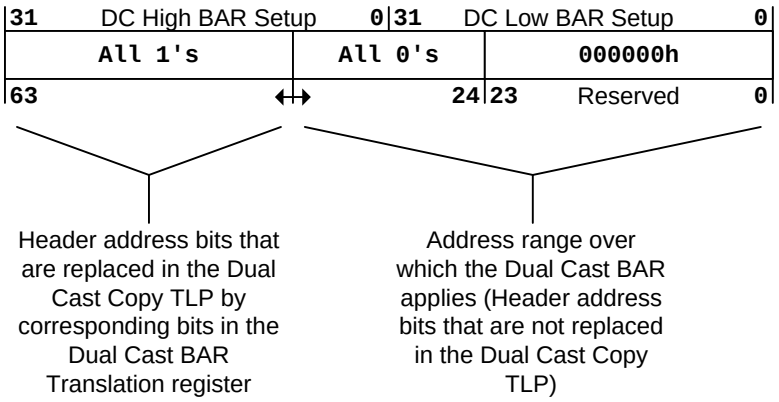

Figure 2. DualCastHigh/LowBARnSetup Register Example

If bits 63:20 are all '1', the source window size is 1MB. If bits 63:21 are '1', and bit 20 is zero, the window size is 2 MB. When DualCastHighBAR*n*Setup[31] = 0, the corresponding Dual Cast BAR is disabled. Table 1 lists some example DualCastLow/HighBARnSetup register values and corresponding DC BAR address window sizes selected.

Table 1 . Dual Cast BARn Setup Register Address Window Sizing Examples

DualCastHighBAR*n*Setup[31:0]	DualCastLowBAR*n*Setup[31:20]	DC BAR*n* Window Size
0000.0000	XXX	Disabled (default)
FFFF.FFFF	FFF	1 MB
FFFF.FFFF	FFE	2 MB
FFFF.FFFF	000	4 GB
FFFF.FFFE	000	8 GB

Restrictions:

1. Dual Cast BAR address windows must not overlap one another
2. Dual Cast Source address windows 0-7 can be mapped to any station or port (including upstream and NT ports), but only write TLPs that enter the switch via the designated Dual Cast Source Station/Port are subject to dual casting (see 2.4 below).
3. Both the original forwarded TLP ***AND*** the Dual Cast copy TLP must be acknowledged on their respective egress ports before the original incoming TLP will be retired.

2.3 DualCastLowBARTranslation0-7[31:0], DualCastHighBARTranslation0-7[31:0]

These registers specify the destination address of the Dual Cast Copy TLP for their corresponding Dual Cast BARs. When a Dual Cast Copy TLP is formed, the original TLPs header address bits will be replaced with corresponding address bits from these registers.

Restrictions:

1. Dual Cast BAR Translation addresses must be mapped to the Dual Cast Destination port as specified in the Dual Cast Source Destination Port register (see 2.4 below). While the original TLPs that are copied can be mapped to any port of the switch, copied TLPs from all of the Dual Cast BARs must be mapped to the Dual Cast Destination port.
2. Dual Cast BAR Translation Address plus Dual Cast BAR window size must never exceed the address range mapped to the Dual Cast Destination port.

2.4 DualCastSourceDestinationPort[31:0]

This register is used to specify the Dual Cast Source Station/Port and the Dual Cast Destination Port. Bit definitions for this register are given in Table 2.

Table 2. DualCastSourceDestinationPort Register Definition

Register Bits	Function
1:0	**Dual Cast Source Port #** Specifies the ingress Port # on which Dual Cast BARs are applied (valid only when DualCastSourceDestinationPort[8]=1).
3:2	**Dual Cast Source Station #** Specifies the ingress Station # on which Dual Cast BARs are applied.
7:4	**Dual Cast Destination Port #** Specifies the egress port number to which Dual Cast BAR Translation addresses are mapped and to which Dual Cast Copy TLPs will be queued.
8	**Dual Cast Source Port Enable** When set, dual casting applies only to write TLPs entering the switch by way of the Dual Cast Source Port # specified in bits 3:0 above. When clear, dual casting applies to write TLPs entering any port on the Dual Cast Source Station # specified in bits 3:2 above. In that case, bits 1:0 above are don't care.
31:9	**Reserved (zero)**

Note: Elsewhere in PEX 86xx documentation, ports are numbered using 4-bit values 0000b, 0001b, and so on. In this register, Dual Cast Source ports are numbered on a per-station basis. For example, what is referred to as port 7 elsewhere in the documentation is described in this register as station 01b, port 11b.

3. Dual Cast Programming Example

In this example, we consider a PEX 8624 switch configured as x8, x8, x8, with port 0 being the upstream port (connected to Root Complex), and ports 5 and 8 configured as transparent downstream ports. Port 5 maps to a block of physical memory at base address 0xAAA00000 (32-bit addressing). Port 8 maps to a block of memory at base address 0xBBB00000.

For this example, the switch must be programmed such that write TLPs entering Port 0 and addressed to port 5 (in the range 0xAAA00000-AAAFFFFF) are dual cast (copied) to the memory mapped to port 8, starting at address 0xBBB00000.

3.1 Register Programming Steps

Step 1. Program DualCastBAR0 with the base address of the memory on Port 5.

DualCastLowBAR0[31:0] = 0xAAA0.000C (note: [19:0] are hard-wired to 0x0000C)

DC High BAR0[31:0] = 0x0000.0000

Step 2. Program DualCastBAR0Setup to specify the size of the DC BAR window (1 MByte).

DualCastLowBAR0Setup[31:0] = 0xFFF0.0000 (note: [19:0] are hard-wired to 0x00000)

DualCastHighBAR0Setup[31:0] = 0xFFFF.FFFF

Step 3. Program DualCastBAR0Translation registers with the address of the memory on port 8.

DualCastLowBAR0Translation[31:0] = 0xBBB0.0000 (note: [19:0] are hard-wired to 0x00000)

DualCastHighBAR0Translation[31:0] = 0x0000.0000

Step 4. Program the DualCastSourceDestinationPort register bits as follows:

DualCastSourceDestinationPort[3:0] = 00.00b (Dual Cast Source Station/Port = 0)

DualCastSourceDestinationPort[7:4] = 1000b (Dual Cast Destination Port = 8)

DualCastSourceDestinationPort[8] = 1b (Dual Cast on Station 0, Port 0 only)

OR

DualCastSourceDestinationPort[8] = 0b (Dual Cast on Station 0, Ports 0-3)

At this point, all write TLPs entering the switch by way of port 0 having addresses in the range 0xAAA00000-AAAFFFFF will be copied to memory at base address 0xBBB0.0000. To verify that dual casting is enabled, try clearing memory at address 0xBBB0.0000, then write a non-zero pattern to memory at address 0xAAA0.0000. A read of memory at 0xBBB0.0000 should now show what was written at address 0xAAA0.0000.

4. Dual Cast to a Non-Transparent Destination Port

When the Dual Cast Destination port is configured as non-transparent (NT), the Dual Cast copy TLPs do not use the same address translation mechanism as do original 'unicast' TLPs that are routed to that port. Where a unicast TLP uses the address translation mechanism in the NT port (NT BAR), Dual Cast Copy TLPs are sent directly to the NT port's egress queue. Therefore, in applications where the Dual Cast Destination port is NT, the Dual Cast High/Low BAR*n* Translation registers must be loaded with the physical base address of the destination memory in the NT address domain.