# N-Channel 20-V (D-S) MOSFET

| PRODUCT SUMMARY | | | |
|---|---|---|---|
| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A)[a] | $Q_g$ (Typ.) |
| 20 | 0.0048 at $V_{GS}$ = 10 V | 35 | 12.7 nC |
| | 0.0063 at $V_{GS}$ = 4.5 V | 35 | |

## FEATURES

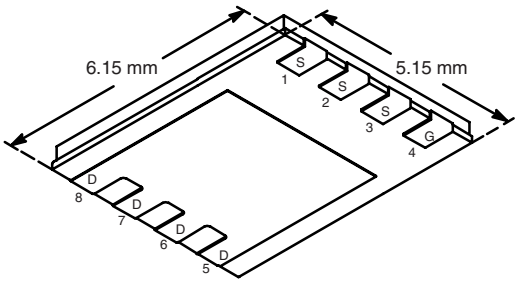
- **Halogen-free**
- TrenchFET® Power MOSFET
- 100 % $R_g$ Tested
- 100 % UIS Tested

RoHS COMPLIANT

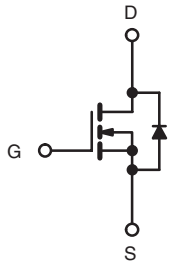
## APPLICATIONS

- DC/DC Converter
  - Notebook
  - POL

**PowerPAK® SO-8**




Bottom View




N-Channel MOSFET

**Ordering Information:** SiR410DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

| ABSOLUTE MAXIMUM RATINGS $T_A$ = 25 °C, unless otherwise noted | | | | |
|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Limit** | **Unit** |
| Drain-Source Voltage | | $V_{DS}$ | 20 | V |
| Gate-Source Voltage | | $V_{GS}$ | ± 20 | |
| Continuous Drain Current ($T_J$ = 150 °C) | $T_C$ = 25 °C | $I_D$ | 35[a] | A |
| | $T_C$ = 70 °C | | 35[a] | |
| | $T_A$ = 25 °C | | 23[b, c] | |
| | $T_A$ = 70 °C | | 18.6[b, c] | |
| Pulsed Drain Current | | $I_{DM}$ | 60 | |
| Avalanche Current | L = 0.1 mH | $I_{AS}$ | 35 | |
| Avalanche Energy | | $E_{AS}$ | 61 | mJ |
| Continuous Source-Drain Diode Current | $T_C$ = 25 °C | $I_S$ | 30 | A |
| | $T_A$ = 25 °C | | 3.5[b, c] | |
| Maximum Power Dissipation | $T_C$ = 25 °C | $P_D$ | 36 | W |
| | $T_C$ = 70 °C | | 23 | |
| | $T_A$ = 25 °C | | 4.2[b, c] | |
| | $T_A$ = 70 °C | | 2.7[b, c] | |
| Operating Junction and Storage Temperature Range | | $T_J$, $T_{stg}$ | - 55 to 150 | °C |
| Soldering Recommendations (Peak Temperature)[d, e] | | | 260 | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **Typical** | **Maximum** | **Unit** |
| Maximum Junction-to-Ambient[b, f] | t ≤ 10 s | $R_{thJA}$ | 25 | 30 | °C/W |
| Maximum Junction-to-Case (Drain) | Steady State | $R_{thJC}$ | 2.9 | 3.5 | |

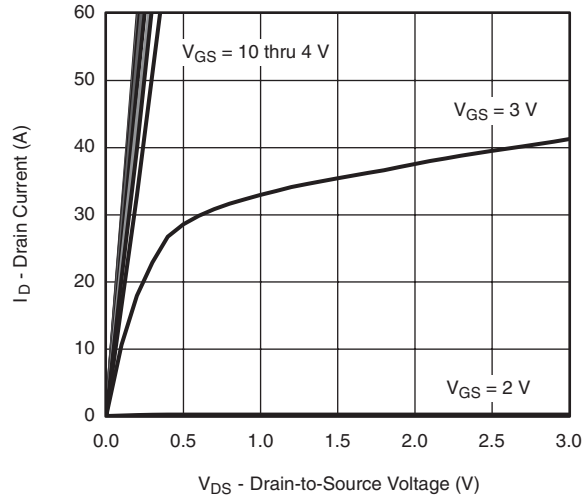
Notes:
a. Package Limited.
b. Surface Mounted on 1" x 1" FR4 board.
c. t = 10 s.
d. See Solder Profile (*http://www.vishay.com/ppg?73257*). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
f. Maximum under Steady State conditions is 70 °C/W.

| **SPECIFICATIONS** $T_J$ = 25 °C, unless otherwise noted | | | | | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Test Conditions** | **Min.** | **Typ.** | **Max.** | **Unit** |
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $V_{DS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 20 | | | V |
| $V_{DS}$ Temperature Coefficient | $\Delta V_{DS}/T_J$ | $I_D$ = 250 µA | | 19 | | mV/°C |
| $V_{GS(th)}$ Temperature Coefficient | $\Delta V_{GS(th)}/T_J$ | | | - 5.3 | | |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$ , $I_D$ = 250 µA | 1.2 | | 2.5 | V |
| Gate-Source Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 20 V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | | | 1 | µA |
| | | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V, $T_J$ = 55 °C | | | 5 | |
| On-State Drain Current[a] | $I_{D(on)}$ | $V_{DS} \geq$ 5 V, $V_{GS}$ = 10 V | 40 | | | A |
| Drain-Source On-State Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 20 A | | 0.004 | 0.0048 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 19.4 A | | 0.005 | 0.0063 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 20 A | | 70 | | S |
| **Dynamic[b]** | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | | 1600 | | pF |
| Output Capacitance | $C_{oss}$ | | | 500 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | 200 | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $I_D$ = 20 A | | 27 | 41 | nC |
| | | $V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 19 A | | 16.7 | 25 | |
| Gate-Source Charge | $Q_{gs}$ | | | 4.5 | | |
| Gate-Drain Charge | $Q_{gd}$ | | | 3.5 | | |
| Gate Resistance | $R_g$ | f = 1 MHz | | 1.3 | 2.6 | Ω |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V, $R_L$ = 1 Ω<br>$I_D \cong$ 10 A, $V_{GEN}$ = 4.5 V, $R_g$ = 1 Ω | | 25 | 40 | ns |
| Rise Time | $t_r$ | | | 15 | 25 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 30 | 45 | |
| Fall Time | $t_f$ | | | 15 | 25 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V, $R_L$ = 1 Ω<br>$I_D \cong$ 10 A, $V_{GEN}$ = 10 V, $R_g$ = 1 Ω | | 12 | 20 | |
| Rise Time | $t_r$ | | | 10 | 15 | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | 25 | 40 | |
| Fall Time | $t_f$ | | | 10 | 15 | |
| **Drain-Source Body Diode Characteristics** | | | | | | |
| Continuous Source-Drain Diode Current | $I_S$ | $T_C$ = 25 °C | | | 35 | A |
| Pulse Diode Forward Current | $I_{SM}$ | | | | 60 | |
| Body Diode Voltage | $V_{SD}$ | $I_S$ = 10 A, $V_{GS}$ = 0 V | | 0.8 | 1.2 | V |
| Body Diode Reverse Recovery Time | $t_{rr}$ | $I_F$ = 10 A, dI/dt = 100 A/µs, $T_J$ = 25 °C | | 30 | 45 | ns |
| Body Diode Reverse Recovery Charge | $Q_{rr}$ | | | 21 | 35 | nC |
| Reverse Recovery Fall Time | $t_a$ | | | 17 | | ns |
| Reverse Recovery Rise Time | $t_b$ | | | 13 | | |

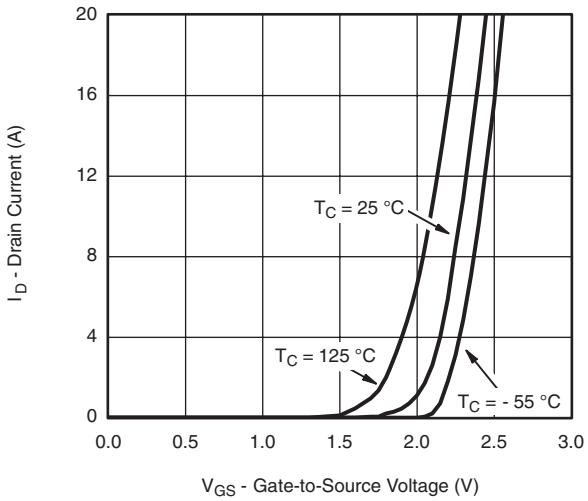
Notes:
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

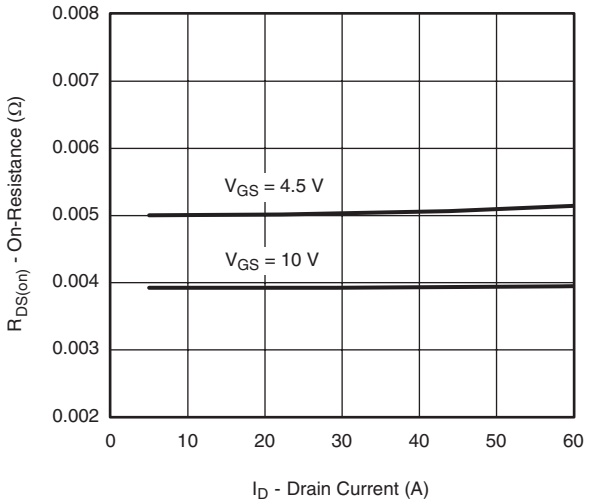
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



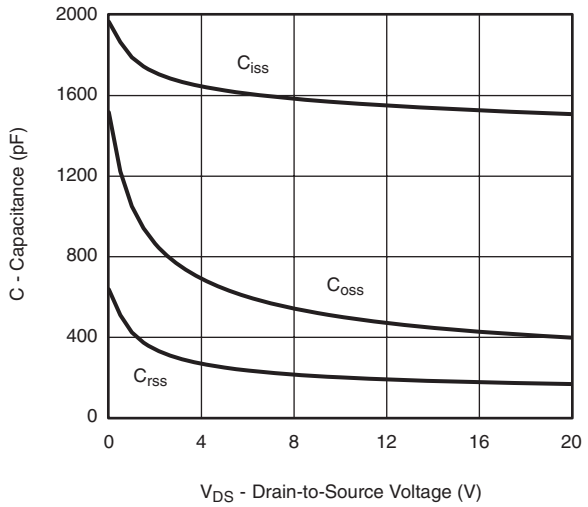

**Output Characteristics**



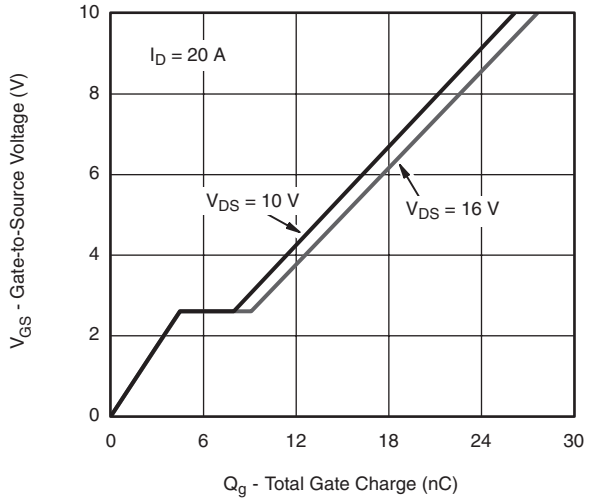

**Transfer Characteristics**



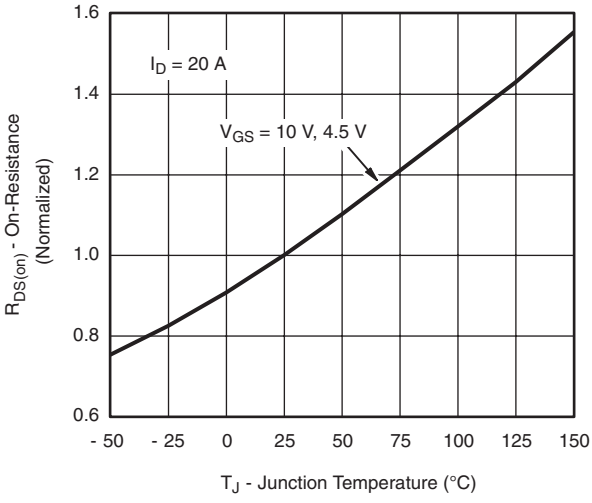

**On-Resistance vs. Drain Current and Gate Voltage**




**Capacitance**

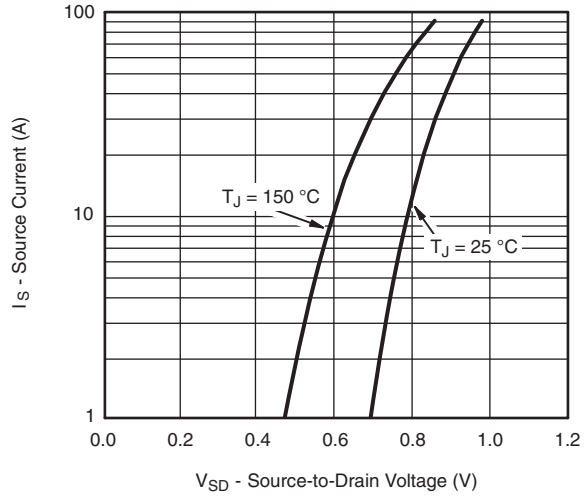



**Gate Charge**

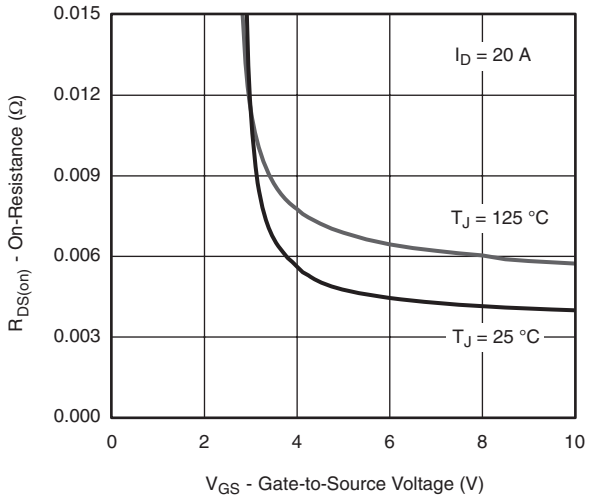



**On-Resistance vs. Junction Temperature**

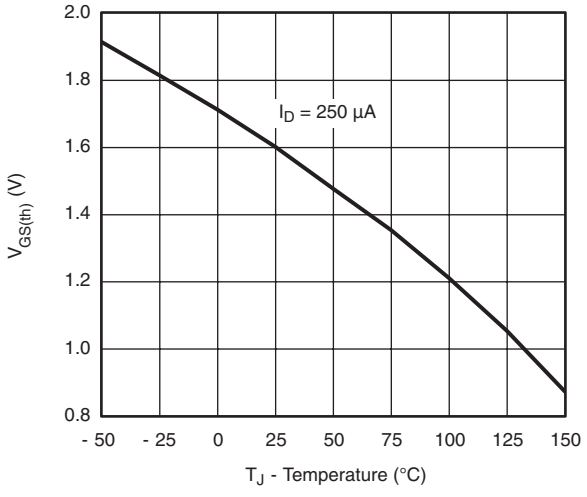
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



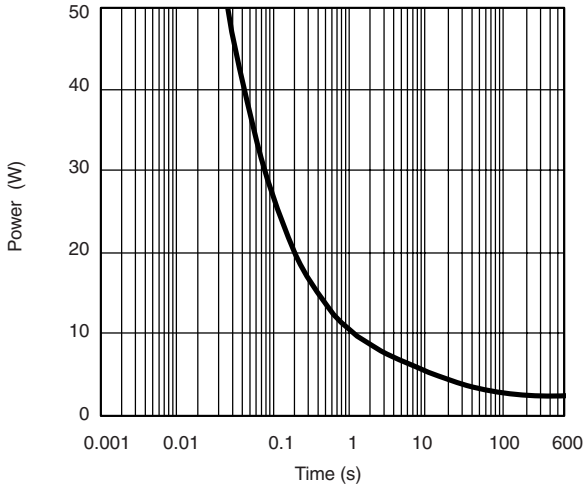

**Source-Drain Diode Forward Voltage**



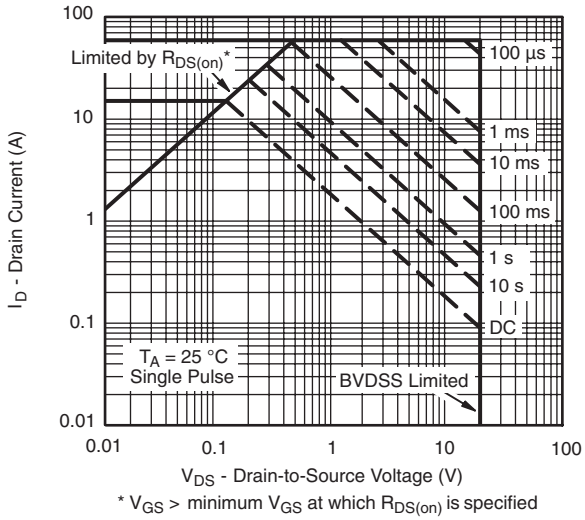

**On-Resistance vs. Gate-to-Source Voltage**




**Threshold Voltage**



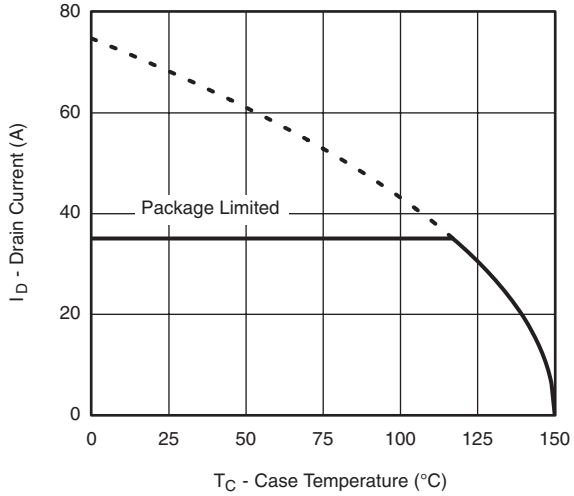

**Single Pulse Power (Junction-to-Ambient)**



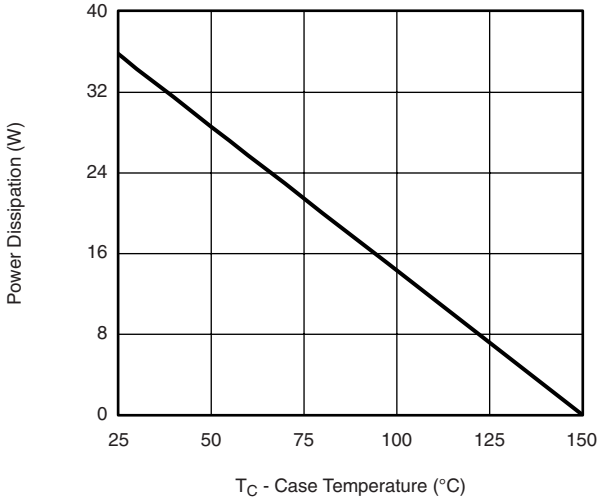

* $V_{GS}$ > minimum $V_{GS}$ at which $R_{DS(on)}$ is specified

**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



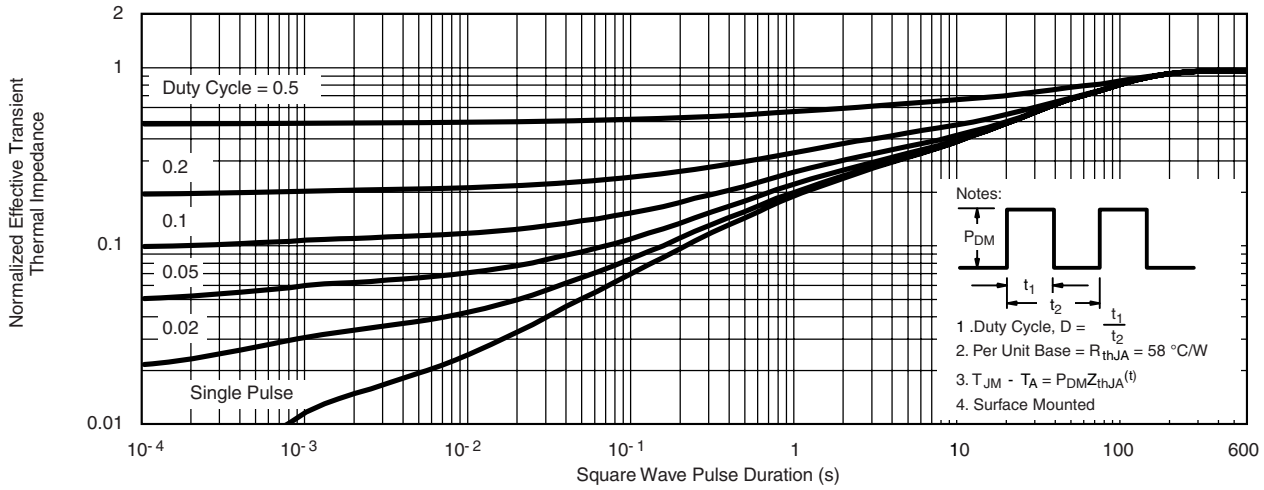

**Current Derating***



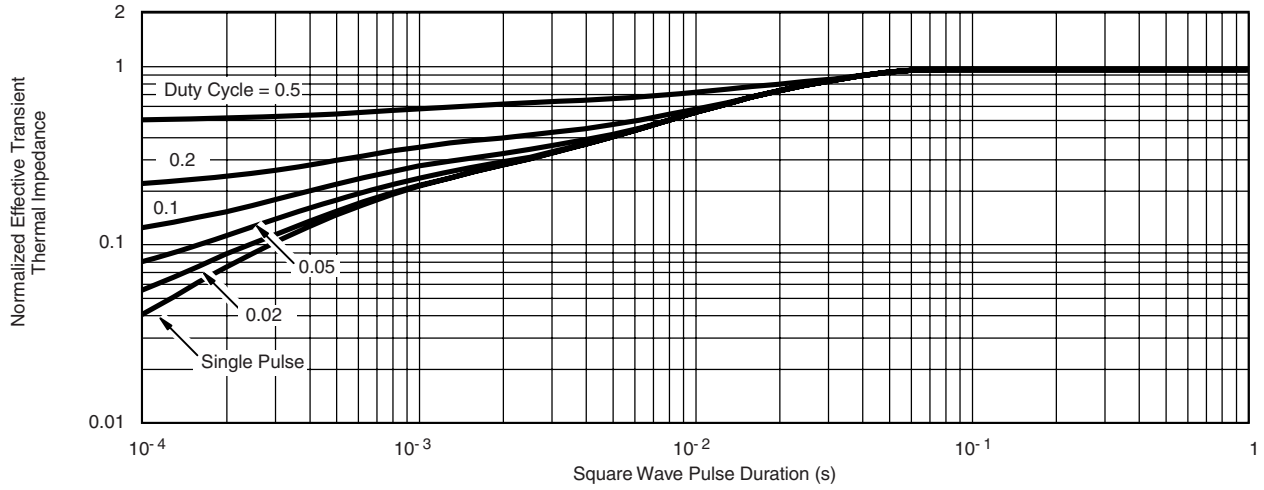

**Power Derating**

* The power dissipation $P_D$ is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



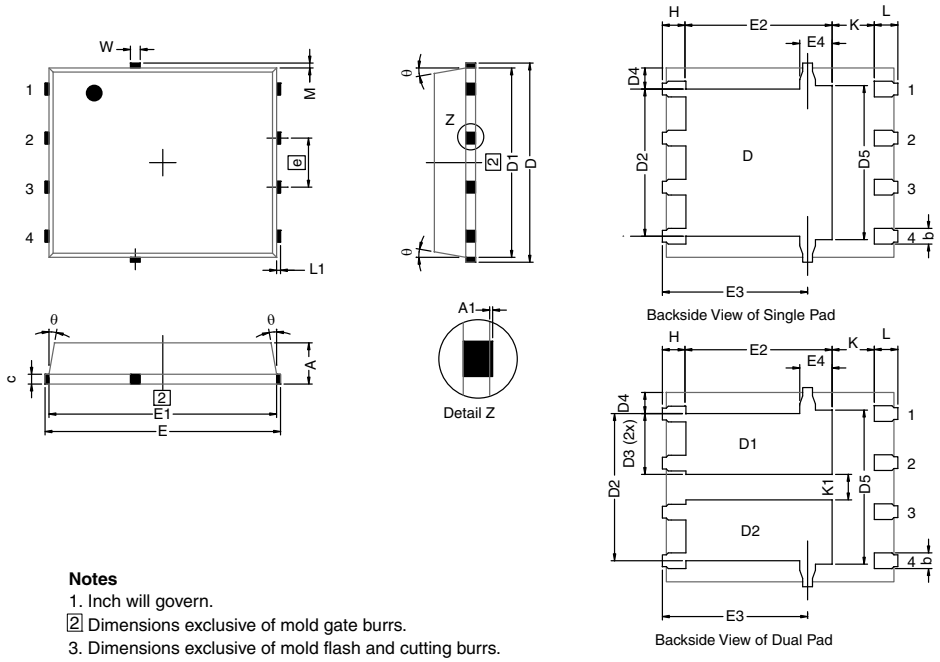

**Normalized Thermal Transient Impedance, Junction-to-Ambient**




**Normalized Thermal Transient Impedance, Junction-to-Case**

*Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?68997.*

# PowerPAK® SO-8, (Single/Dual)




**Notes**

1. Inch will govern.
2. Dimensions exclusive of mold gate burrs.
3. Dimensions exclusive of mold flash and cutting burrs.

| DIM. | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.97 | 1.04 | 1.12 | 0.038 | 0.041 | 0.044 |
| A1 | | - | 0.05 | 0 | - | 0.002 |
| b | 0.33 | 0.41 | 0.51 | 0.013 | 0.016 | 0.020 |
| c | 0.23 | 0.28 | 0.33 | 0.009 | 0.011 | 0.013 |
| D | 5.05 | 5.15 | 5.26 | 0.199 | 0.203 | 0.207 |
| D1 | 4.80 | 4.90 | 5.00 | 0.189 | 0.193 | 0.197 |
| D2 | 3.56 | 3.76 | 3.91 | 0.140 | 0.148 | 0.154 |
| D3 | 1.32 | 1.50 | 1.68 | 0.052 | 0.059 | 0.066 |
| D4 | | 0.57 typ. | | | 0.0225 typ. | |
| D5 | | 3.98 typ. | | | 0.157 typ. | |
| E | 6.05 | 6.15 | 6.25 | 0.238 | 0.242 | 0.246 |
| E1 | 5.79 | 5.89 | 5.99 | 0.228 | 0.232 | 0.236 |
| E2 (for AL product) | 3.30 | 3.48 | 3.66 | 0.130 | 0.137 | 0.144 |
| E2 (for other product) | 3.48 | 3.66 | 3.84 | 0.137 | 0.144 | 0.151 |
| E3 | 3.68 | 3.78 | 3.91 | 0.145 | 0.149 | 0.154 |
| E4 (for AL product) | | 0.58 typ. | | | 0.023 typ. | |
| E4 (for other product) | | 0.75 typ. | | | 0.030 typ. | |
| e | | 1.27 BSC | | | 0.050 BSC | |
| K (for AL product) | | 1.45 typ. | | | 0.057 typ. | |
| K (for other product) | | 1.27 typ. | | | 0.050 typ. | |
| K1 | 0.56 | - | - | 0.022 | - | - |
| H | 0.51 | 0.61 | 0.71 | 0.020 | 0.024 | 0.028 |
| L | 0.51 | 0.61 | 0.71 | 0.020 | 0.024 | 0.028 |
| L1 | 0.06 | 0.13 | 0.20 | 0.002 | 0.005 | 0.008 |
| θ | 0° | - | 12° | 0° | - | 12° |
| W | 0.15 | 0.25 | 0.36 | 0.006 | 0.010 | 0.014 |
| M | | 0.125 typ. | | | 0.005 typ. | |
| ECN: C13-0702-Rev. K, 20-May-13<br>DWG: 5881 | | | | | | |

# PowerPAK® SO-8 Mounting and Thermal Considerations

**by Wharton McDaniel**

MOSFETs for switching applications are now available with die on resistances around 1 mΩ and with the capability to handle 85 A. While these die capabilities represent a major advance over what was available just a few years ago, it is important for power MOSFET packaging technology to keep pace. It should be obvious that degradation of a high performance die by the package is undesirable. PowerPAK is a new package technology that addresses these issues. In this application note, PowerPAK's construction is described. Following this mounting information is presented including land patterns and soldering profiles for maximum reliability. Finally, thermal and electrical performance is discussed.

## THE PowerPAK PACKAGE

The PowerPAK package was developed around the SO-8 package (figure 1). The PowerPAK SO-8 utilizes the same footprint and the same pin-outs as the standard SO-8. This allows PowerPAK to be substituted directly for a standard SO-8 package. Being a leadless package, PowerPAK SO-8 utilizes the entire SO-8 footprint, freeing space normally occupied by the leads, and thus allowing it to hold a larger die than a standard SO-8. In fact, this larger die is slightly larger than a full sized DPAK die. The bottom of the die attach pad is exposed for the purpose of providing a direct, low resistance thermal path to the substrate the device is mounted on. Finally, the package height is lower than the standard SO-8, making it an excellent choice for applications with space constraints.

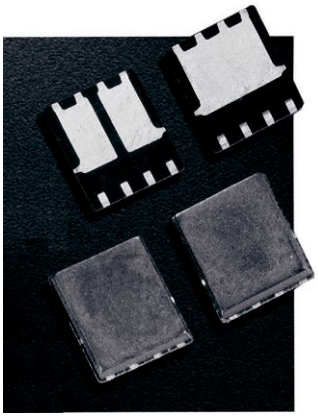
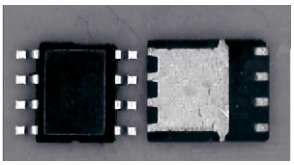


Fig. 1 PowerPAK 1212 Devices

## PowerPAK SO-8 SINGLE MOUNTING

The PowerPAK single is simple to use. The pin arrangement (drain, source, gate pins) and the pin dimensions are the same as standard SO-8 devices (see figure 2). Therefore, the PowerPAK connection pads match directly to those of the SO-8. The only difference is the extended drain connection area. To take immediate advantage of the PowerPAK SO-8 single devices, they can be mounted to existing SO-8 land patterns.



Standard SO-8 PowerPAK SO-8

Fig. 2

The minimum land pattern recommended to take full advantage of the PowerPAK thermal performance see Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*. Click on the PowerPAK SO-8 single in the index of this document.

In this figure, the drain land pattern is given to make full contact to the drain pad on the PowerPAK package.

This land pattern can be extended to the left, right, and top of the drawn pattern. This extension will serve to increase the heat dissipation by decreasing the thermal resistance from the foot of the PowerPAK to the PC board and therefore to the ambient. Note that increasing the drain land area beyond a certain point will yield little decrease in foot-to-board and foot-to-ambient thermal resistance. Under specific conditions of board configuration, copper weight and layer stack, experiments have found that more than about 0.25 $in^2$ to 0.5 $in^2$ of additional copper (in addition to the drain land) will yield little improvement in thermal performance.

APPLICATION NOTE

# PowerPAK® SO-8 Mounting and Thermal Considerations

## PowerPAK SO-8 DUAL

The pin arrangement (drain, source, gate pins) and the pin dimensions of the PowerPAK SO-8 dual are the same as standard SO-8 dual devices. Therefore, the PowerPAK device connection pads match directly to those of the SO-8. As in the single-channel package, the only exception is the extended drain connection area. Manufacturers can likewise take immediate advantage of the PowerPAK SO-8 dual devices by mounting them to existing SO-8 dual land patterns.

To take the advantage of the dual PowerPAK SO-8's thermal performance, the minimum recommended land pattern can be found in Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*. Click on the PowerPAK 1212-8 dual in the index of this document.

The gap between the two drain pads is 24 mils. This matches the spacing of the two drain pads on the PowerPAK SO-8 dual package.

## REFLOW SOLDERING

Vishay Siliconix surface-mount packages meet solder reflow reliability requirements. Devices are subjected to solder reflow as a test preconditioning and are then reliability-tested using temperature cycle, bias humidity, HAST, or pressure pot. The solder reflow temperature profile used, and the temperatures and time duration, are shown in figures 3 and 4.

For the lead (Pb)-free solder profile, see www.vishay.com/doc?73257.

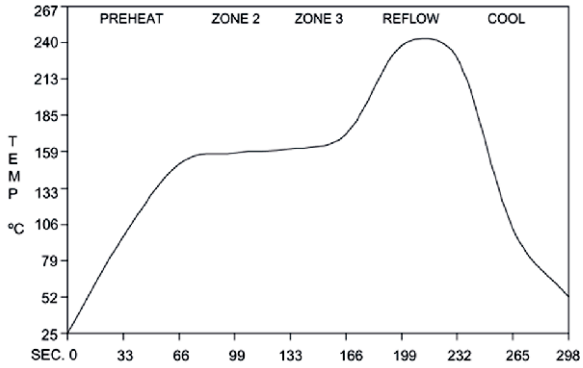



Fig. 3 Solder Reflow Temperature Profile

| | |
|---|---|
| Ramp-Up Rate | + 3 °C /s max. |
| Temperature at 150 - 200 °C | 120 s max. |
| Temperature Above 217 °C | 60 - 150 s |
| Maximum Temperature | 255 + 5/- 0 °C |
| Time at Maximum Temperature | 30 s |
| Ramp-Down Rate | + 6 °C/s max. |

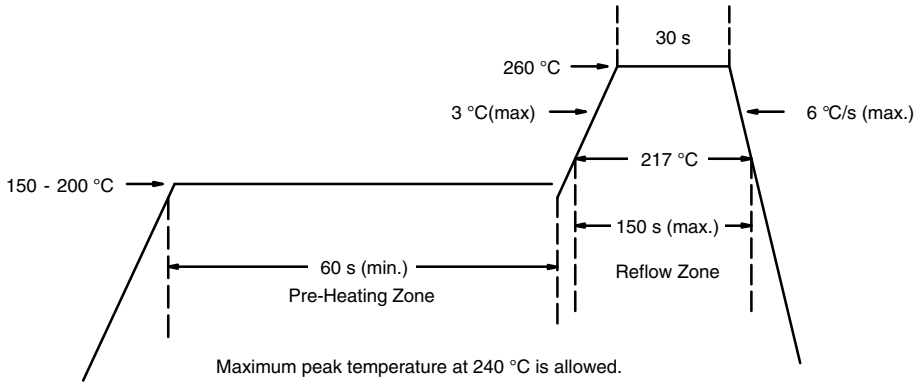



Fig. 4 Solder Reflow Temperatures and Time Durations

APPLICATION NOTE

# PowerPAK® SO-8 Mounting and Thermal Considerations

## THERMAL PERFORMANCE

### Introduction

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, $R_{thJC}$, or the junction-to-foot thermal resistance, $R_{thJF}$ This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only, in other words, independent of the properties of the object to which the device is mounted. Table 1 shows a comparison of the DPAK, PowerPAK SO-8, and standard SO-8. The PowerPAK has thermal performance equivalent to the DPAK, while having an order of magnitude better thermal performance over the SO-8.

**TABLE 1 - DPAK AND POWERPAK SO-8 EQUIVALENT STEADY STATE PERFORMANCE**

| | DPAK | PowerPAK SO-8 | Standard SO-8 |
|---|---|---|---|
| Thermal Resistance $R_{thJC}$ | 1.2 °C/W | 1 °C/W | 16 °C/W |

### Thermal Performance on Standard SO-8 Pad Pattern

Because of the common footprint, a PowerPAK SO-8 can be mounted on an existing standard SO-8 pad pattern. The question then arises as to the thermal performance of the PowerPAK device under these conditions. A characterization was made comparing a standard SO-8 and a PowerPAK device on a board with a trough cut out underneath the PowerPAK drain pad. This configuration restricted the heat flow to the SO-8 land pads. The results are shown in figure 5.

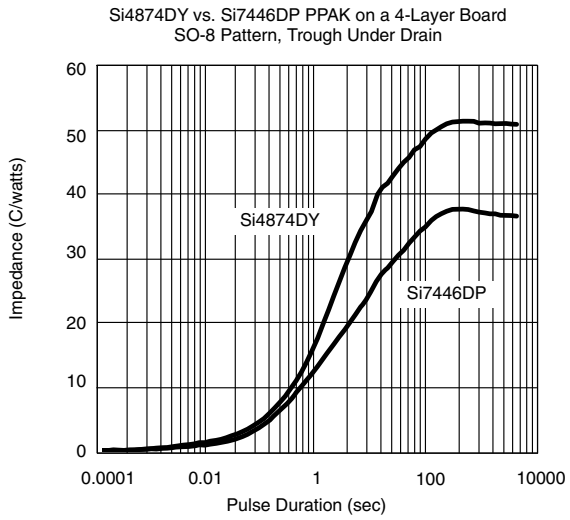



Fig. 5 PowerPAK SO-8 and Standard SO-0 Land Pad Thermal Path

Because of the presence of the trough, this result suggests a minimum performance improvement of 10 °C/W by using a PowerPAK SO-8 in a standard SO-8 PC board mount.

The only concern when mounting a PowerPAK on a standard SO-8 pad pattern is that there should be no traces running between the body of the MOSFET. Where the standard SO-8 body is spaced away from the pc board, allowing traces to run underneath, the PowerPAK sits directly on the pc board.

### Thermal Performance - Spreading Copper

Designers may add additional copper, spreading copper, to the drain pad to aid in conducting heat from a device. It is helpful to have some information about the thermal performance for a given area of spreading copper.

Figure 6 shows the thermal resistance of a PowerPAK SO-8 device mounted on a 2-in. 2-in., four-layer FR-4 PC board. The two internal layers and the backside layer are solid copper. The internal layers were chosen as solid copper to model the large power and ground planes common in many applications. The top layer was cut back to a smaller area and at each step junction-to-ambient thermal resistance measurements were taken. The results indicate that an area above 0.3 to 0.4 square inches of spreading copper gives no additional thermal performance improvement. A subsequent experiment was run where the copper on the back-side was reduced, first to 50 % in stripes to mimic circuit traces, and then totally removed. No significant effect was observed.

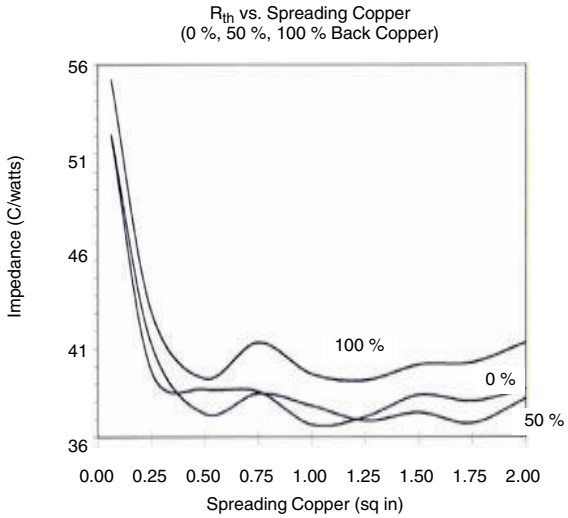



Fig. 6 Spreading Copper Junction-to-Ambient Performance

APPLICATION NOTE

# PowerPAK® SO-8 Mounting and Thermal Considerations

## SYSTEM AND ELECTRICAL IMPACT OF PowerPAK SO-8

In any design, one must take into account the change in MOSFET $R_{DS(on)}$ with temperature (figure 7).

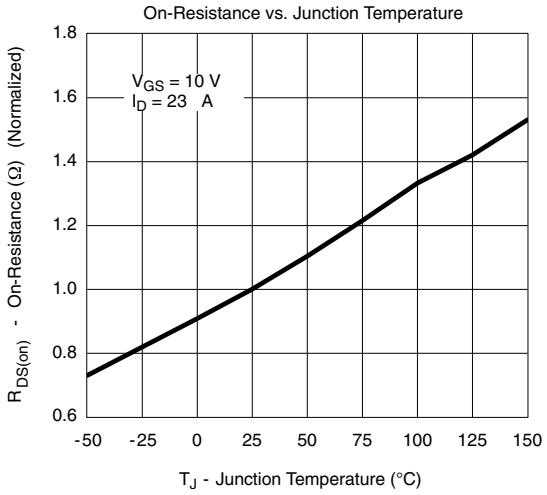



Fig. 7 MOSFET $R_{DS(on)}$ vs. Temperature

A MOSFET generates internal heat due to the current passing through the channel. This self-heating raises the junction temperature of the device above that of the PC board to which it is mounted, causing increased power dissipation in the device. A major source of this problem lies in the large values of the junction-to-foot thermal resistance of the SO-8 package.

PowerPAK SO-8 minimizes the junction-to-board thermal resistance to where the MOSFET die temperature is very close to the temperature of the PC board. Consider two devices mounted on a PC board heated to 105 °C by other components on the board (figure 8).

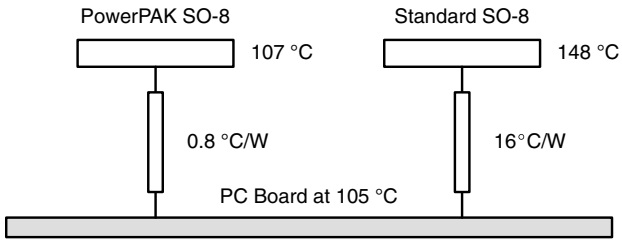



Fig. 8 Temperature of Devices on a PC Board

Suppose each device is dissipating 2.7 W. Using the junction-to-foot thermal resistance characteristics of the PowerPAK SO-8 and the standard SO-8, the die temperature is determined to be 107 °C for the PowerPAK (and for DPAK) and 148 °C for the standard SO-8. This is a 2 °C rise above the board temperature for the PowerPAK and a 43 °C rise for the standard SO-8. Referring to figure 7, a 2 °C difference has minimal effect on $R_{DS(on)}$ whereas a 43 °C difference has a significant effect on $R_{DS(on)}$.

Minimizing the thermal rise above the board temperature by using PowerPAK has not only eased the thermal design but it has allowed the device to run cooler, keep $r_{DS(on)}$ low, and permits the device to handle more current than the same MOSFET die in the standard SO-8 package.

## CONCLUSIONS

PowerPAK SO-8 has been shown to have the same thermal performance as the DPAK package while having the same footprint as the standard SO-8 package. The PowerPAK SO-8 can hold larger die approximately equal in size to the maximum that the DPAK can accommodate implying no sacrifice in performance because of package limitations.

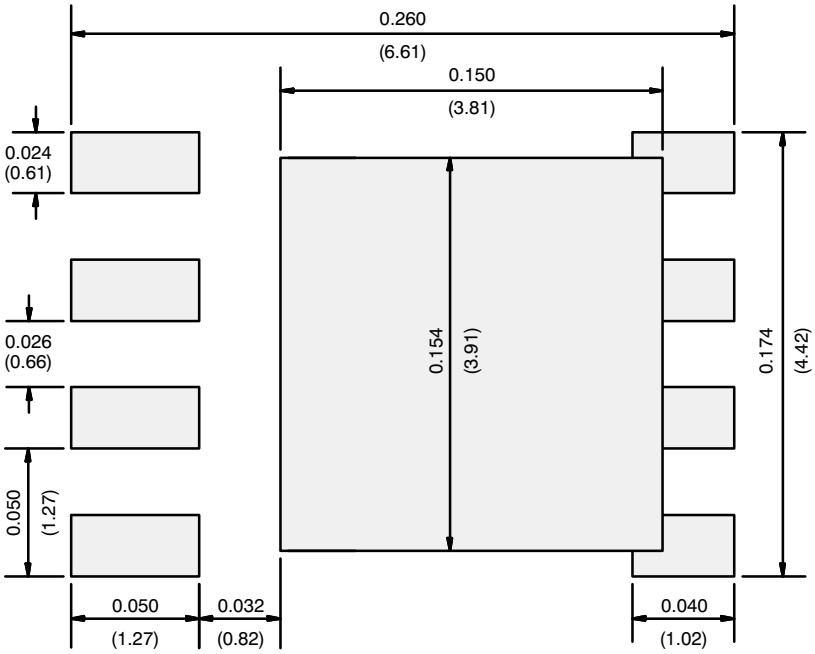
Recommended PowerPAK SO-8 land patterns are provided to aid in PC board layout for designs using this new package.

Thermal considerations have indicated that significant advantages can be gained by using PowerPAK SO-8 devices in designs where the PC board was laid out for the standard SO-8. Applications experimental data gave thermal performance data showing minimum and typical thermal performance in a SO-8 environment, plus information on the optimum thermal performance obtainable including spreading copper. This further emphasized the DPAK equivalency.

PowerPAK SO-8 therefore has the desired small size characteristics of the SO-8 combined with the attractive thermal characteristics of the DPAK package.

APPLICATION NOTE

## RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single




Recommended Minimum Pads
Dimensions in Inches/(mm)

Return to Index

# Useful Web Links

### COMPARE MOSFET PACKAGES

www.vishay.com/mosfets/tapereel-package-list/

### FEATURED MOSFET FAMILIES

www.vishay.com/landingpage/tradeshows/powermanagement/2011/mosfets.html

### CHECK DISTRIBUTOR STOCK

www.vishay.com/search?query=&type=inv&search-inventory-submit.x=41&search-inventory-submit.y=13

### SAMPLES

www.vishay.com/how/samples/

### SALES CONTACTS

www.vishay.com/company/contacts/

**PCNS** (if applicable)

www.vishay.com/how/pcn/

www.vishay.com/quality/pcn-search/

### APPLICATION NOTES

www.vishay.com/mosfets/related/#appnot

### ON-LINE LITERATURE

www.vishay.com/how/onlineliterature/online-libraries/

### THERMAL SIMULATION

www.vishay.com/mosfets/thermasim/

See Application Note AN832 (www.vishay.com/doc?69510) for the ThermaSim User Guide.

### RELIABILITY INFORMATION

www.vishay.com/doc?70863

### SPICE MODELS

Available spice models are located on the specific device's web product page. See Application Note AN838 (www.vishay.com/doc?65038) for tips downloading, preparing and using them.

# Devices:

# PowerPAK® SO-8, PowerPAK SO-8L
# PowerPAK 1212-8, PowerPAK 1212-8S, PowerPAK 1212-8W
# PowerPAIR® 6 x 3.7, PowerPAIR 6 x 5, PowerPAIR 3 x 3

Single and Dual


| | | |
|---|---|---|
| 7401 | = | Example Base Part Number or marking code [a] |
| | = | Siliconix Logo |
| LL | = | Lot Code |
| | = | ESD Symbol |
| ● | = | Pin 1 Indicator |
| T | = | Assembly Factory Code |
| Y | = | Year Code |
| W | = | Week Code |
| F | = | Wafer Fab Code |

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

**Note**

a. These digits will be a code, if indicated on the datasheet. Otherwise, the digits will be the base number like indicated in the example.

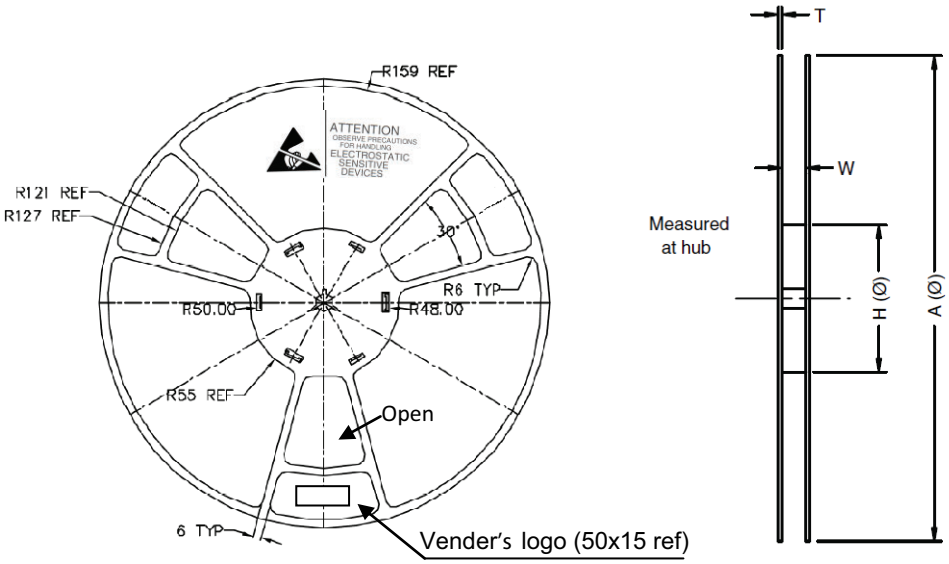
| ENVIRONMENTAL AND PACKAGE TESTING DATA FOR PowerPAK® SO-8 SOLDER PROCESS | | | | | |
|---|---|---|---|---|---|
| **STRESS** | **SAMPLE SIZE** | **DEVICE HR./CYC** | **CONDITION** | **TOTAL FAILS** | **FAIL PERCENTAGE** |
| BOND INT | 400 | 200 000 | 200 °C + N2 | 0 | 0 |
| HAST | 2956 | 295 600 | 130 °C, 85 % RH | 0 | 0 |
| Pressure Pot | 3332 | 319 872 | 121°, 15 PSIG | 0 | 0 |
| Solder DUNK | 1217 | 3651 | 260 °C, 10 s | 0 | 0 |
| Solderability | 165 | 1320 | 883 M2003 | 0 | 0 |
| Temp. Cycle | 5500 | 2 625 300 | -55 °C to 150 °C | 0 | 0 |

| N-CHANNEL ACCELERATED OPERATING LIFE TEST RESULT | |
|---|---|
| Sample Size | 232 395 |
| Equivalent Device Hours | 28 904 254 900 |
| Failure Rate in FIT | 1.073 |

Failure Rate in FIT is calculated according to JEDEC Standard JESD85, *Methods for Calculating Failure Rates in Units of FITs*, based on accelerated high temperature operating life test results by using an apparent activation energy of 0.7 eV. The junction temperature of the device at use is assumed to be 55 °C. A constant failure rate distribution is assumed. The upper confidence bound of the failure rate is 60 %.

# Reel

**330 mm Reel** (Lock Reel)



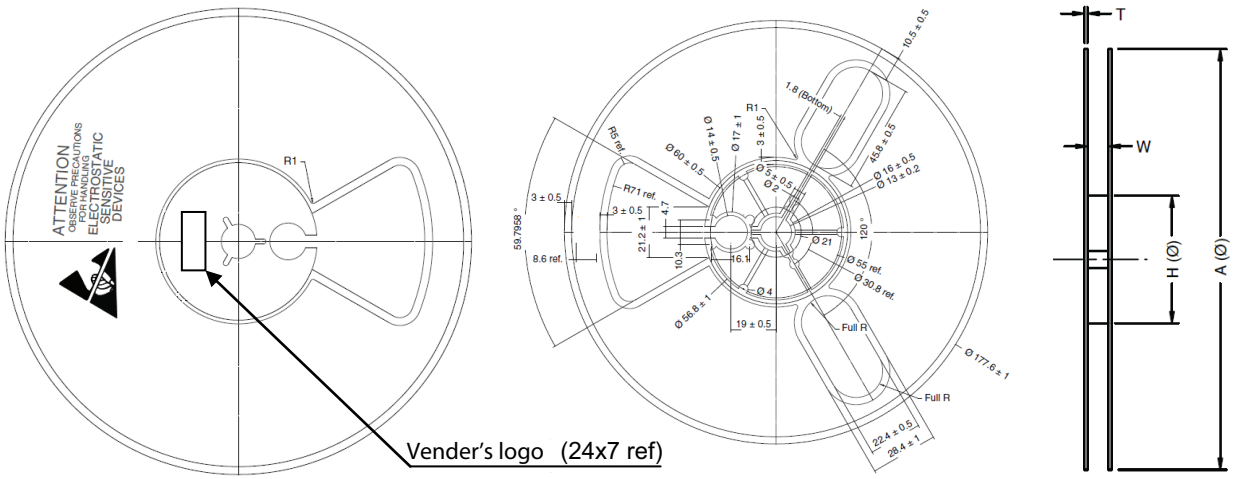

Note:

1. Material: Antistatic or conductor plastic
2. All dimensions in mm
3. ESD-surface resistivity-$10^4$ to $10^{11}$ Ω/sq
4. Color: Black

| VER | APPLICATION | | A | W | TAPE WIDTH | H | T |
|---|---|---|---|---|---|---|---|
| - 1 | SOIC-14/16<br>TO-251 (Short Lead)<br>TO-252/TO-252 (Reverse Lead)<br>PLCC-20<br>TSSOP-8/14/16/20/28<br>SSOP-24<br>SOIC-16 (W) | PowerPAK MLF 9 x 9<br>PowerPAK MLP 6 x 6<br>MLF 8 x 8<br>PowerPAK 8 x 8L<br>PowerPAK 8 x 8<br>MLP77 | 330 ± 2 | 16.4 +2.0 -0 | 16 | 100 ± 1 | 2.5 ± 0.5 |
| - 2 | SOIC-8 (N), SOIC-8 (N) epad<br>MSOP-8/10<br>PowerPAK® SO-8<br>PowerPAK 1212<br>PowerPAK 1212-8W<br>MICRO FOOT®<br>MLP33-5, MLP33-8, MLP33-10<br>QFN (4 x 4)/(3 x 3)/DFN-10 (3 x 3)/<br>MLP44-16L<br>MLP65-18/20L | PolarPAK®<br>MLP55<br>PowerPAIR® 6 x 5<br>PowerPAIR 6 x 3 J<br>PowerPAIR SO-8L<br>PolarPAK1215<br>PowerPAIR 6 x 3.7<br>PowerPAK SO-8L<br>MLP4.5 x 3.5-22L | 330 ± 2 | 12.4 +2.0 -0 | 12 | 100 ± 1 | 2.5 ± 0.5 |
| - 4 | SOT-23/143<br>SC70<br>MICRO FOOT | TSOP-6, 1206-8 ChipFET<br>PowerPAK SC70,<br>PowerPAK SC75 | 330 ± 2 | 8.4 +1.5 -0 | 8.4 | 100 ± 1 | 2.5 ± 0.5 |
| - 5 | SOIC-20W/24W<br>$D^2PAK$<br>SSOP-28<br>QSOP-36 | PowerPAK MLF 10 x 10 | 330 ± 2 | 24.4 +2.0 -0 | 24 | 100 ± 1 | 2.5 ± 0.5 |
| - 8 | KGD | | 330 ± 2 | 16.4 +2.0 -0 | 16 | 130 ± 1 | 2.5 ± 0.5 |

**178 mm Reel** (Complete Reel)

Front Back Side




Note:

1. Material: Antistatic or conductor plastic
2. All dimensions in mm
3. ESD-surface resistivity-$10^4$ to $10^{11}$ Ω/sq
4. Color: Black

| VER | APPLICATION | | A | W | TAPE WIDTH | H | T |
|---|---|---|---|---|---|---|---|
| - 3 | SOT-23/143<br>TSOP-5/6/SC70JW-8L<br>1206-8 ChipFET®<br>SC70/SC75A/SC89<br>MICRO FOOT<br>SC-89 (SOT-666)<br>SOT23-5, 6<br>KGD<br>WCSP<br>PowerPAK 0806 | PowerPAK SC70<br>PowerPAK SC75<br>MiniQFN<br>PowerPAK MLP22-5<br>PowerPAK ChipFET<br>PowerPAK SC75-6L (PIC)<br>PowerPAK TSC75-6L (PIC)<br>TDFN4 1.2 x 1.6,<br>TDFN8 2 x 2<br>Thin PowerPAK SC-70<br>Thin PowerPAK SC-75 | 178 ± 2 | 8.4 +1.5 -0 | 8.4 | 62 ± 2 | 1.5 ± 0.5 |
| - 7 | MICRO FOOT<br>PowerPAK 2 x 5 | KGD | 178 ± 2 | 12.4 +2.0 -0 | 12 | 55 ± 2 | 1.6 ± 0.25 |

ECN: C15-0680-Rev. BR, 15-Jun-15
DWG: 93-5211-X

# N-Channel 20 V (D-S) MOSFET

## DESCRIPTION

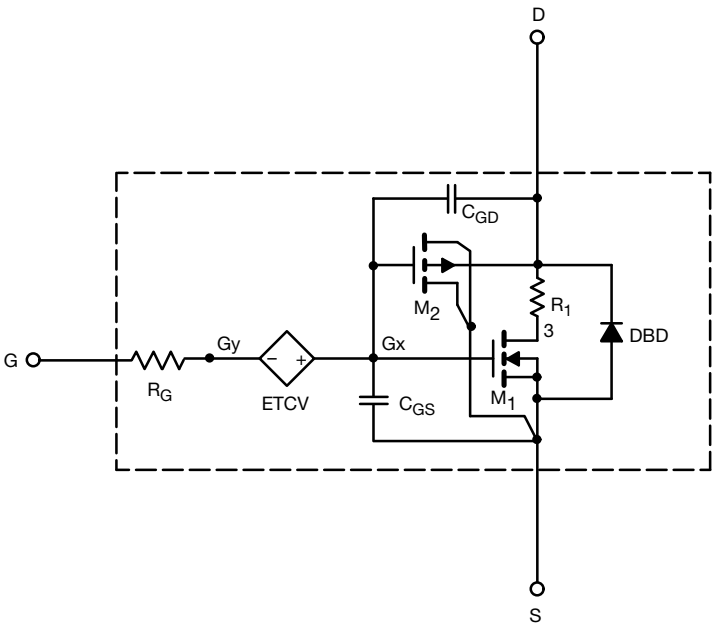
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the - 55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched $C_{gd}$ model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

## CHARACTERISTICS

- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the - 55 °C to + 125 °C Temperature Range
- Model the Gate Charge

## SUBCIRCUIT MODEL SCHEMATIC




**Note**

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.

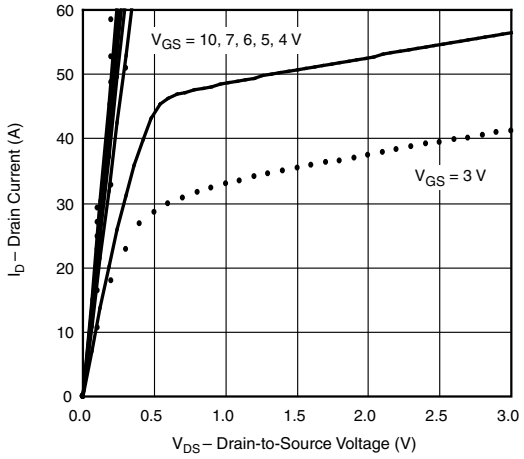
| **SPECIFICATIONS** ($T_J$ = 25 °C, unless otherwise noted) | | | | | |
|---|---|---|---|---|---|
| **PARAMETER** | **SYMBOL** | **TEST CONDITIONS** | **SIMULATED DATA** | **MEASURED DATA** | **UNIT** |
| **Static** | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1.5 | - | V |
| Drain-Source On-State Resistance[a] | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 20 A | 0.004 | 0.004 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 19.4 A | 0.005 | 0.005 | |
| Forward Transconductance[a] | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 20 A | 80 | 70 | S |
| Diode Forward Voltage | $V_{SD}$ | $I_S$ = 10 A | 0.79 | 0.80 | V |
| **Dynamic[b]** | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1 MHz | 1560 | 1600 | pF |
| Output Capacitance | $C_{oss}$ | | 503 | 500 | |
| Reverse Transfer Capacitance | $C_{rss}$ | | 200 | 200 | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 10 V, $I_D$ = 20 A | 25 | 27 | nC |
| | | $V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 20 A | 13 | 16.7 | |
| Gate-Source Charge | $Q_{gs}$ | | 4.5 | 4.5 | |
| Gate-Drain Charge | $Q_{gd}$ | | 3.5 | 3.5 | |

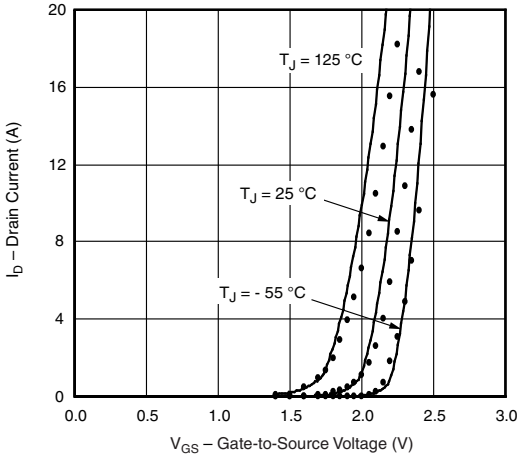
**Notes**

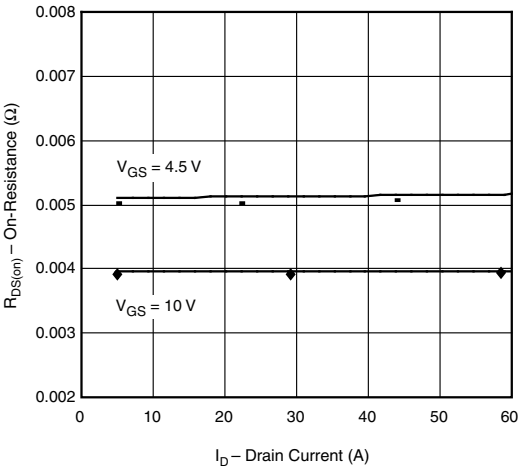
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

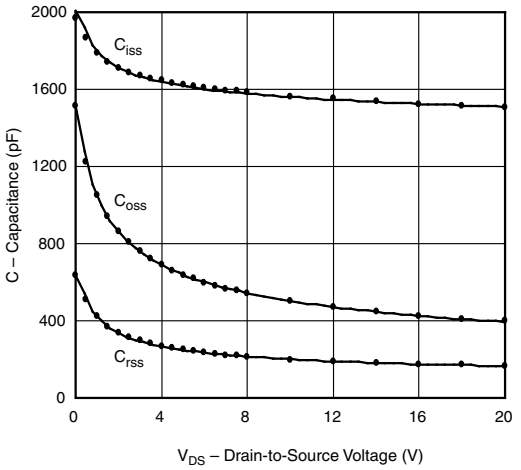
b. Guaranteed by design, not subject to production testing.

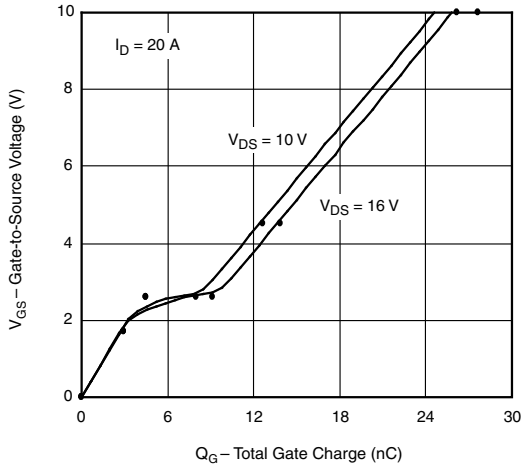
## COMPARISON OF MODEL WITH MEASURED DATA ($T_J$ = 25 °C, unless otherwise noted)

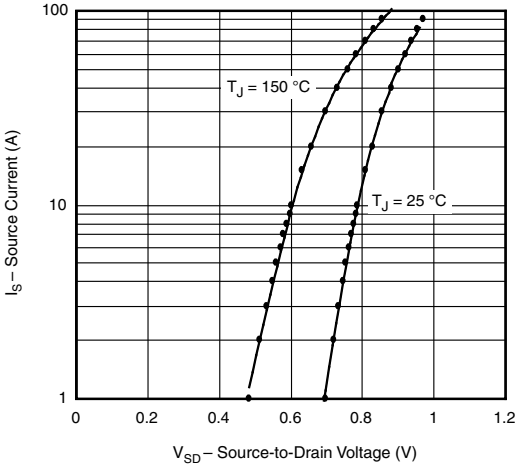


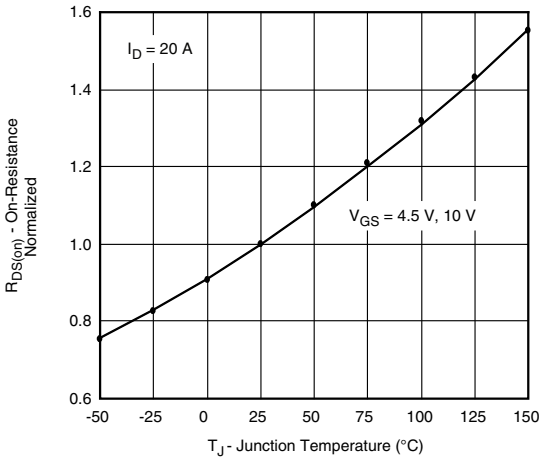



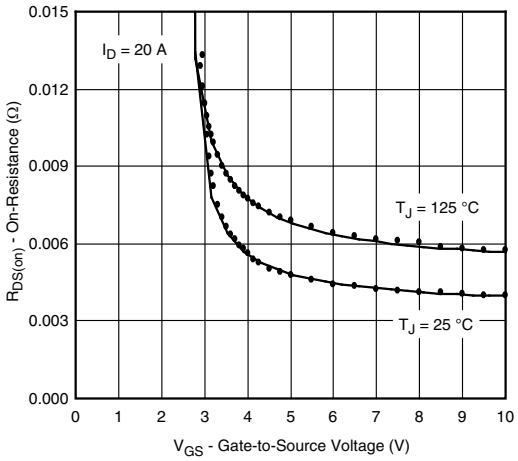




**Note**

- Dots and squares represent measured data.

**COMPARISON OF MODEL WITH MEASURED DATA** ($T_J$ = 25 °C, unless otherwise noted)




**Note**

- Dots and squares represent measured data.

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**Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.**

**Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.**

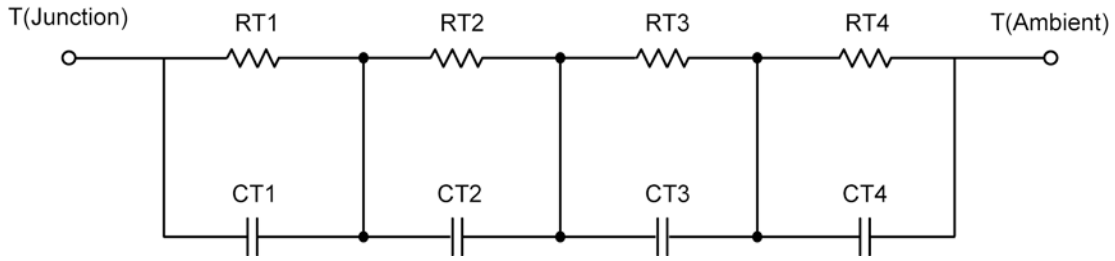
# R-C Thermal Model Parameters

## DESCRIPTION

The parametric values in the R-C thermal model have been derived using curve-fitting techniques. R-C values for the electrical circuit in the Foster/Tank and Cauer/Filter configurations are included. When implemented in P-Spice, these values have matching characteristic curves to the single-pulse transient thermal impedance curves for the MOSFET.

These RC values can be used in the P-SPICE simulation to evaluate the thermal behavior of the MOSFET junction temperature under a defined power profile. These techniques are described in Application Note AN609, "Thermal Simulation of Power MOSFETs on the P-Spice Platform."

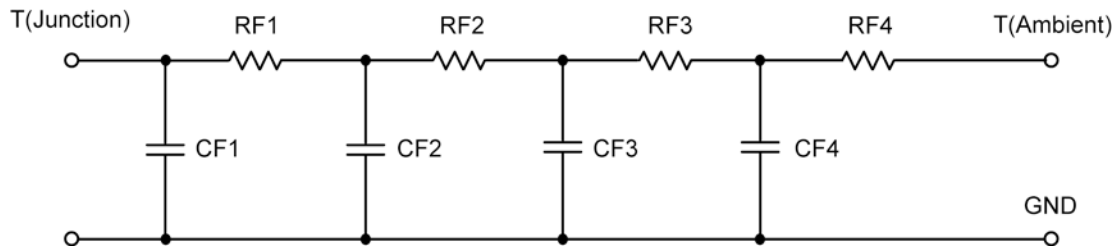
## R-C THERMAL MODEL FOR TANK CONFIGURATION




| R-C VALUES FOR TANK CONFIGURATION | | | |
|---|---|---|---|
| **Thermal Resistance (°C/W)** | | | |
| **Junction to** | **Ambient** | **Case** | **Foot** |
| RT1 | 1.9921 | 546.0005 m | N/A |
| RT2 | 12.7242 | 284.8987 m | N/A |
| RT3 | 10.4306 | 492.2008 m | N/A |
| RT4 | 44.8531 | 2.1769 | N/A |
| **Thermal Capacitance (Joules/°C)** | | | |
| **Junction to** | **Ambient** | **Case** | **Foot** |
| CT1 | 1.4947 m | 600.9468 u | N/A |
| CT2 | 506.3593 m | 30.2059 m | N/A |
| CT3 | 38.2285 m | 9.4434 m | N/A |
| CT4 | 1.6532 | 9.4063 m | N/A |

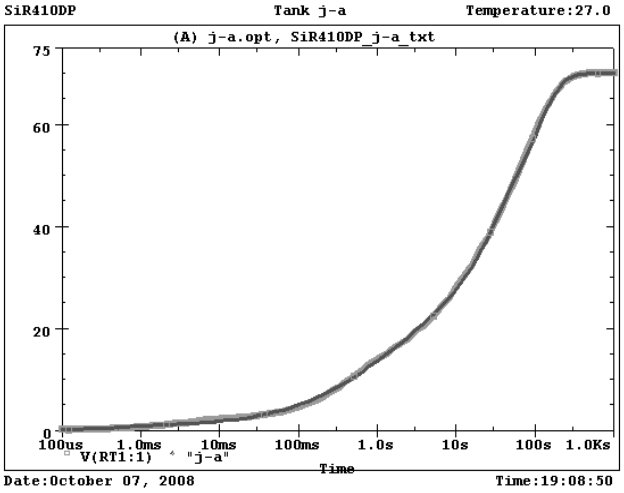
*This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.*

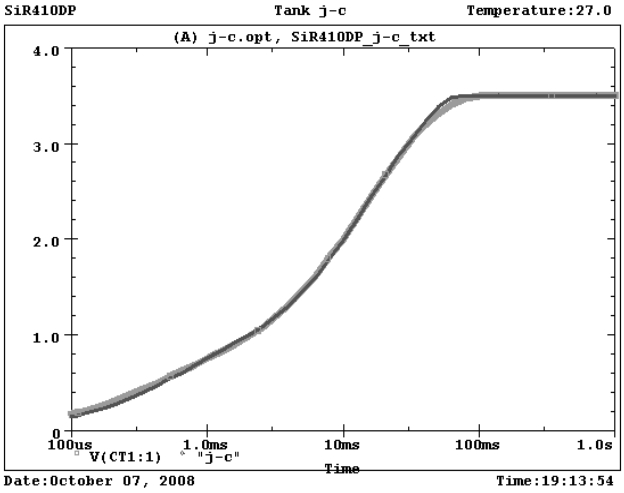
## R-C THERMAL MODEL FOR FILTER CONFIGURATION

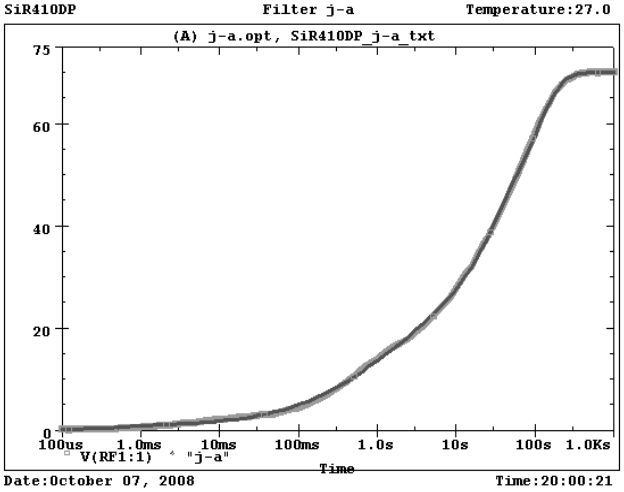


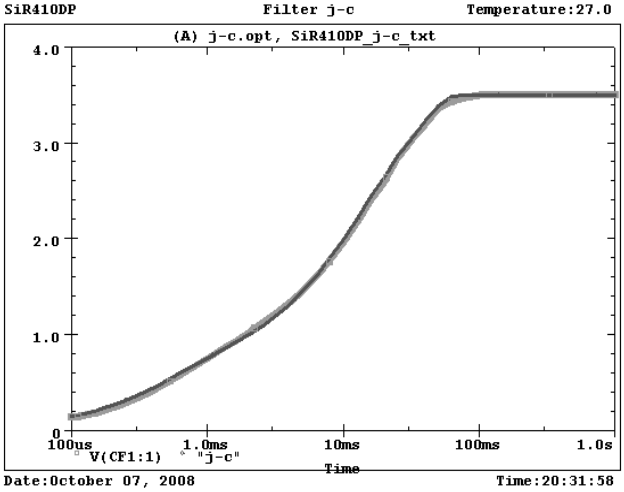

| R-C VALUES FOR FILTER CONFIGURATION | | | |
|---|---|---|---|
| **Thermal Resistance (°C/W)** | | | |
| **Junction to** | **Ambient** | **Case** | **Foot** |
| RF1 | 2.2098 | 956.0920 m | N/A |
| RF2 | 13.0792 | 1.3571 | N/A |
| RF3 | 21.1865 | 649.5091 m | N/A |
| RF4 | 33.5245 | 537.2989 m | N/A |
| **Thermal Capacitance (Joules/°C)** | | | |
| **Junction to** | **Ambient** | **Case** | **Foot** |
| CF1 | 1.7629 m | 737.3986 u | N/A |
| CF2 | 35.3857 m | 5.4126 m | N/A |
| CF3 | 458.6534 m | 2.7800 m | N/A |
| CF4 | 1.6882 | 1.1187 m | N/A |

**Note**
NA indicates not applicable

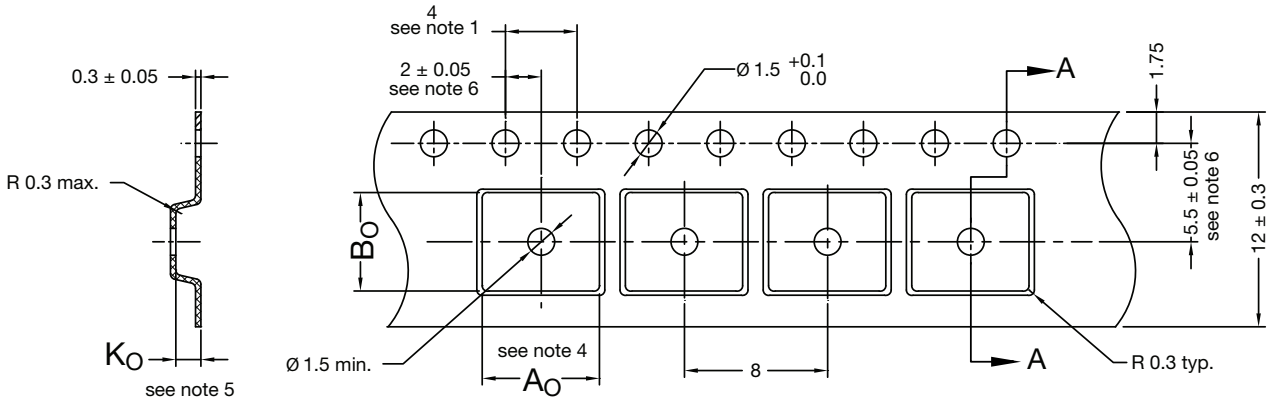

SiR410DP
Tank j-a
Temperature:27.0
(A) j-a.opt, SiR410DP_j-a_txt
75
60
40
20
0
100us
1.0ms
10ms
100ms
1.0s
10s
100s
1.0Ks
V(RT1:1)
"j-a"
Time
Date:October 07, 2008
Time:19:08:50


SiR410DP
Tank j-c
Temperature:27.0
(A) j-c.opt, SiR410DP_j-c_txt
4.0
3.0
2.0
1.0
0
100us
1.0ms
10ms
100ms
1.0s
V(CT1:1)
"j-c"
Time
Date:October 07, 2008
Time:19:13:54


SiR410DP
Filter j-a
Temperature:27.0
(A) j-a.opt, SiR410DP_j-a_txt
75
60
40
20
0
100us
1.0ms
10ms
100ms
1.0s
10s
100s
1.0Ks
V(RF1:1)
"j-a"
Time
Date:October 07, 2008
Time:20:00:21


SiR410DP
Filter j-c
Temperature:27.0
(A) j-c.opt, SiR410DP_j-c_txt
4.0
3.0
2.0
1.0
0
100us
1.0ms
10ms
100ms
1.0s
V(CF1:1)
"j-c"
Time
Date:October 07, 2008
Time:20:31:58

# PowerPAK® SOIC-8




Section A-A

$A_O$ = 6.5 mm ± 0.1 mm
$B_O$ = 5.5 mm ± 0.1 mm
$K_O$ = 1.4 mm ± 0.1 mm

**Notes**

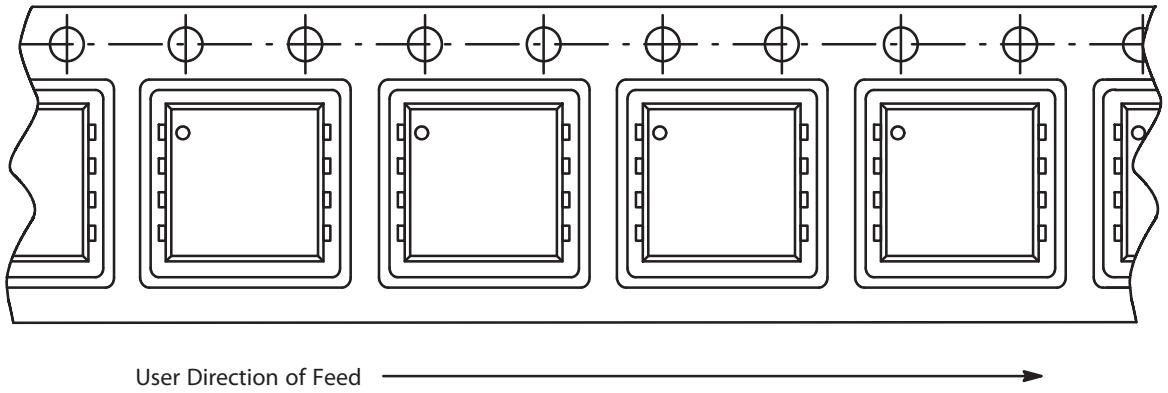
(1) 10 sprocket hole pitch cumulative tolerance ± 0.2 mm.
(2) Camber not to exceed 1 mm in 100 mm, also not to exceed 1.5 cm in 1 m actually.
(3) Material: Black conductive or black static dissipative.
(4) For advantek carrier tape, $A_O$ and $B_O$ are calculate on a plane at a distance "R" above the bottom of the pocket.
(5) $K_O$ measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
(6) It should be measured from:
  a. sprocket hole to pocket center
  and
  b. sprocket hole to pocket hole
(7) All sizes in mm unless specified.
(8) Tolerances will be ± 0.1 mm unless specified.
(9) Vishay part number must be labeled at all reels of carrier tape.
(10) Surface resistivity: $10^4$ to $10^{11}$ Ω.

| QUANTITY PER REEL | |
|---|---|
| T1 | 3000 |

ECN: C15-0525-Rev. F, 08-Jun-15
DWG: 90-2378-1

# Device Orientation
# PowerPAK® 1212-8, PowerPAK 1212-8S, PowerPAK 1212-8W
# PowerPAK SO-8

| DEVICE ORIENTATION | |
|---|---|
| **PACKAGE** | **METHOD** |
| PowerPAK 1212-8 | T1 |
| PowerPAK 1212-8S | T1 |
| PowerPAK 1212-8W | T1 |
| PowerPAK SO-8 | T1 |




Revision control of this drawing is maintained through Document Control, Pack Specification-PACK-0007-14

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