Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
1A		TDI		TDI			J20	B32						
1A		TMS		TMS			G23	A33						
1A		TRST		TRST			D26	C32						
1A		TCK		TCK			D25	B34						
1A		TDO		TDO			E25	B33						
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	H23	K24						
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	H22	L24						
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	D28	D29						
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D27	C28						
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G25	L23	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G24	M23	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B28	E29	DQSn1L	DQ1L	DQ1L	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C28	D28	DQS1L	DQ1L/CQn1L	DQ1L	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	F26	J26	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	F25	K25	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	E28	C30	DQSn2L	DQSn1L/DQ1L	DQ1L	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	E27	C29	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	H25	K27	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	H24	K26	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	G27	F29	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	G26	F28	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	K24	P24	DQ3L	DQ2L	DQ1L	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	K23	P23	DQ3L	DQ2L	DQ1L	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	F28	G29	DQSn3L	DQ2L	DQSn1L/DQ1L	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G28	G28	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K22	J25	DQ3L	DQ2L	DQ1L	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K21	H24	DQ3L	DQ2L	DQ1L	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J26	H27	DQSn4L	DQSn2L/DQ2L	DQ1L	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J25	G26	DQS4L	DQS2L/CQ2L	DQ1L	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	L21	J27	DQ4L	DQ2L	DQ1L	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	L20	H26	DQ4L	DQ2L	DQ1L	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	H28	G27	DQ4L	DQ2L	DQ1L	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	H27	F26	DQ4L	DQ2L	DQ1L	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	L23	M24						
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L22	N23						
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	K26	J30						
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	K25	H29						
1C	VREFB1CN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	L24	N26						
1C	VREFB1CN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	M23	N25						
1C	VREFB1CN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	L26	J29	DQSn5L			DQSn5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	L25	J28	DQS5L			DQS5L		
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L10n	DIFFOUT_L19n	N21	N27	DQ5L			DQ5L		
1C	VREFB1CN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	N20	M26	DQ5L			DQ5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	J28	L27	DQ5L			DQ5L		
1C	VREFB1CN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	K28	L26	DQ5L			DQ5L		
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L11n	DIFFOUT_L21n	N23	P26	DQ6L	DQ5L		DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L11p	DIFFOUT_L21p	N22	R25	DQ6L	DQ5L		DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L11n	DIFFOUT_L22n	L28	K30	DQSn6L	DQ5L		DQSn6L	DQ5L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L11p	DIFFOUT_L22p	K27	L30	DQS6L	DQ5L/CQn5L		DQS6L	DQ5L/CQn5L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L12n	DIFFOUT_L23n	P21	U25	DQ6L	DQ5L		DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L12p	DIFFOUT_L23p	P20	T24	DQ6L	DQ5L		DQ6L	DQ5L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L12n	DIFFOUT_L24n	M26	K29	DQSn7L	DQSn5L/DQ5L		DQSn7L	DQSn5L/DQ5L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L12p	DIFFOUT_L24p	M25	K28	DQS7L	DQS5L/CQ5L		DQS7L	DQS5L/CQ5L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L13n	DIFFOUT_L25n	N25	R24	DQ7L	DQ5L		DQ7L	DQ5L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L13p	DIFFOUT_L25p	N24	R23	DQ7L	DQ5L		DQ7L	DQ5L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L13n	DIFFOUT_L26n	M28	M30	DQ7L	DQ5L		DQ7L	DQ5L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L13p	DIFFOUT_L26p	L27	L29	DQ7L	DQ5L		DQ7L	DQ5L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L14n	DIFFOUT_L27n	P26	M29						
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L14p	DIFFOUT_L27p	P25	M28						
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L14n	DIFFOUT_L28n	N28	T26						
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L14p	DIFFOUT_L28p	N27	U26						
1C	VREFB1CN0	CLK1n	CLK1n				P28	N29						
1C	VREFB1CN0	CLK1p	CLK1p				P27	N28						
2C	VREFB2CN0	CLK3p	CLK3p				T28	AA28						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
2C	VREFB2CN0	CLK3n	CLK3n				R28	AA29						
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L15p	DIFFOUT_L29p	T27	AC29						
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L15n	DIFFOUT_L29n	U28	AB29						
2C	VREFB2CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L30p	R25	W24						
2C	VREFB2CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L30n	R26	V25						
2C	VREFB2CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L31p	T25	AB27	DQ8L	DQ10L		DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L31n	U26	AC28	DQ8L	DQ10L		DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L32p	R20	AA26	DQ8L	DQ10L		DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L32n	T21	AA27	DQ8L	DQ10L		DQ8L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L33p	U27	AD26	DQS8L	DQS10L/CQ10L		DQS8L	DQS10L/CQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L33n	V28	AE27	DQSn8L	DQSn10L/DQ10L		DQSn8L	DQSn10L/DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L34p	T22	Y22	DQ9L	DQ10L		DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L34n	T23	W23	DQ9L	DQ10L		DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L35p	U25	AC26	DQS9L	DQ10L/CQn10L		DQS9L	DQ10L/CQn10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L35n	V26	AD27	DQSn9L	DQ10L		DQSn9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L36p	T20	Y23	DQ9L	DQ10L		DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L36n	U21	Y24	DQ9L	DQ10L		DQ9L	DQ10L	
2C	VREFB2CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L37p	W27	AF28	DQ10L			DQ10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L37n	W28	AE29	DQ10L			DQ10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L38p	U23	AC25	DQ10L			DQ10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L38n	U24	AB26	DQ10L			DQ10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L39p	V25	AE28	DQS10L			DQS10L		
2C	VREFB2CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L39n	W26	AD29	DQSn10L			DQSn10L		
2C	VREFB2CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L40p	V22	AA24						
2C	VREFB2CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L40n	V23	Y25						
2A	VREFB2AN0	IO			DIFFIO_RX_L21p	DIFFOUT_L41p	Y27	AG29						
2A	VREFB2AN0	IO			DIFFIO_RX_L21n	DIFFOUT_L41n	Y28	AF29						
2A	VREFB2AN0	IO			DIFFIO_TX_L21p	DIFFOUT_L42p	W24	AE23						
2A	VREFB2AN0	IO			DIFFIO_TX_L21n	DIFFOUT_L42n	W25	AD24						
2A	VREFB2AN0	IO			DIFFIO_RX_L22p	DIFFOUT_L43p	AB28	AJ26	DQ11L	DQ13L	DQ14L	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L22n	DIFFOUT_L43n	AA28	AK27	DQ11L	DQ13L	DQ14L	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L22p	DIFFOUT_L44p	W22	AG24	DQ11L	DQ13L	DQ14L	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L22n	DIFFOUT_L44n	W23	AF25	DQ11L	DQ13L	DQ14L	DQ11L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L23p	DIFFOUT_L45p	AB27	AH26	DQS11L	DQS13L/CQ13L	DQ14L	DQS11L	DQS13L/CQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L23n	DIFFOUT_L45n	AC28	AJ27	DQSn11L	DQSn13L/DQ13L	DQ14L	DQSn11L	DQSn13L/DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L23p	DIFFOUT_L46p	V20	AG23	DQ12L	DQ13L	DQ14L	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L23n	DIFFOUT_L46n	W21	AF24	DQ12L	DQ13L	DQ14L	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AC27	AH28	DQS12L	DQ13L/CQn13L	DQS14L/CQ14L	DQS12L	DQ13L/CQn13L	DQS14L/CQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AD28	AH29	DQSn12L	DQ13L	DQSn14L/DQ14L	DQSn12L	DQ13L	DQSn14L/DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	Y25	AF26	DQ12L	DQ13L	DQ14L	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	Y26	AF27	DQ12L	DQ13L	DQ14L	DQ12L	DQ13L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AA25	AJ28	DQ13L	DQ14L	DQ14L	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AA26	AJ29	DQ13L	DQ14L	DQ14L	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AB25	AG26	DQ13L	DQ14L	DQ14L	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AC26	AG27	DQ13L	DQ14L	DQ14L	DQ13L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AE27	AM29	DQS13L	DQS14L/CQ14L	DQ14L/CQn14L	DQS13L	DQS14L/CQ14L	DQ14L/CQn14L
2A	VREFB2AN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AE28	AM30	DQSn13L	DQSn14L/DQ14L	DQ14L	DQSn13L	DQSn14L/DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	Y23	AF23	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	Y24	AE24	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AF27	AM28	DQS14L	DQ14L/CQn14L	DQ14L	DQS14L	DQ14L/CQn14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AF28	AL29	DQSn14L	DQ14L	DQ14L	DQSn14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	AB23	AB23	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	AB24	AA23	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L	DQ14L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L28p	DIFFOUT_L55p	AH27	AL28						
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L28n	DIFFOUT_L55n	AG28	AK29						
2A	VREFB2AN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AC25	AD23						
2A	VREFB2AN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AD26	AC24						
		nCONFIG		nCONFIG			AA22	AM34						
		nSTATUS		nSTATUS			AC23	AM33						
		CONF_DONE		CONF_DONE			AC24	AL32						
		PORSEL		PORSEL			W20	AN33						
		nCE		nCE			Y21	AN34						
3A	VREFB3AN0	IO				DIFFOUT_B1n	AB21	AP31	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AC21	AP29	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AD22	AP30	DQSn1B	DQ1B	DQ1B	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AC22	AN30	DQS1B	DQ1B/CQn1B	DQ1B	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AA20	AN29	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AB20	AP28	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE23	AP27	DQSn2B	DQSn1B/DQ1B	DQ1B	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD23	AN27	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AE24	AM26	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AE25	AP25	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AG23	AP26	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AF24	AN26	DQ2B	DQ1B	DQ1B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AF25	AL26	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AF26	AL27	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH25	AM25	DQSn3B	DQ2B	DQSn1B/DQ1B	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AG25	AL25	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AG26	AJ25	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AH26	AH25	DQ3B	DQ2B	DQ1B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AH24	AK23	DQSn4B	DQSn2B/DQ2B	DQ1B	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AH23	AJ23	DQS4B	DQS2B/CQ2B	DQ1B	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AG22	AH24	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AH22	AH23	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AF22	AL24	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AE22	AK24	DQ4B	DQ2B	DQ1B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AH20	AL22	DQ5B	DQ3B		DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AH21	AJ21	DQ5B	DQ3B		DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AF21	AM23	DQSn5B	DQ3B		DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AE21	AL23	DQS5B	DQ3B/CQn3B		DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AG19	AH22	DQ5B	DQ3B		DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AG20	AJ22	DQ5B	DQ3B		DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AF19	AP24	DQSn6B	DQSn3B/DQ3B		DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AE20	AN24	DQS6B	DQS3B/CQ3B		DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AD19	AM22	DQ6B	DQ3B		DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AC19	AP22	DQ6B	DQ3B		DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AE19	AP23	DQ6B	DQ3B		DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AD20	AN23	DQ6B	DQ3B		DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AA19	AH20						
3A	VREFB3AN0	IO				DIFFOUT_B19p	AB18	AF20						
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	Y18	AG21						
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	Y17	AF21						
3C	VREFB3CN0	IO				DIFFOUT_B21n	AA17	AN21	DQ7B	DQ7B		DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B21p	AA16	AP21	DQ7B	DQ7B		DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AC18	AL21	DQSn7B	DQ7B		DQSn7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AB17	AK21	DQS7B	DQ7B/CQn7B		DQS7B	DQ7B/CQn7B	
3C	VREFB3CN0	IO				DIFFOUT_B23n	Y15	AM21	DQ7B	DQ7B		DQ7B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B23p	Y16	AM20	DQ7B	DQ7B		DQ7B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AH19	AL20	DQSn8B	DQSn7B/DQ7B		DQSn8B	DQSn7B/DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AH18	AK20	DQS8B	DQS7B/CQ7B		DQS8B	DQS7B/CQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25n	AE17	AJ20	DQ8B	DQ7B		DQ8B	DQ7B	
3C	VREFB3CN0	IO				DIFFOUT_B25p	AG17	AJ19	DQ8B	DQ7B		DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AF18	AM19	DQ8B	DQ7B		DQ8B	DQ7B	
3C	VREFB3CN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AE18	AL19	DQ8B	DQ7B		DQ8B	DQ7B	
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B27n	AD17	AC18						
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B27p	AD16	AD18						
3C	VREFB3CN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AF16	AF19						
3C	VREFB3CN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AE16	AE19						
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B29n	AC16	AF18						
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B29p	AB15	AE18						
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B15n	DIFFOUT_B30n	AF15	AM18						
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B15p	DIFFOUT_B30p	AE15	AL18						
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B31n	AH17	AP20						
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B31p	AG16	AN20						
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B16n	DIFFOUT_B32n	AH16	AP18						
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B16p	DIFFOUT_B32p	AH15	AN18						
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B17p	DIFFOUT_B33p	AG14	AN15						
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B17n	DIFFOUT_B33n	AH14	AP15						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B34p	AH12	AN17						
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B34n	AH13	AP17						
4C	VREFB4CN0	IO			DIFFIO_RX_B18p	DIFFOUT_B35p	AF14	AE17						
4C	VREFB4CN0	IO			DIFFIO_RX_B18n	DIFFOUT_B35n	AG13	AF17						
4C	VREFB4CN0	IO				DIFFOUT_B36p	Y13	AH16	DQ9B			DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B36n	Y14	AJ15	DQ9B			DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19p	DIFFOUT_B37p	AA13	AE16	DQS9B			DQS9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B19n	DIFFOUT_B37n	AA14	AF16	DQSn9B			DQSn9B		
4C	VREFB4CN0	IO				DIFFOUT_B38p	AB12	AD17	DQ9B			DQ9B		
4C	VREFB4CN0	IO				DIFFOUT_B38n	AB11	AK17	DQ9B			DQ9B		
4C	VREFB4CN0	IO			DIFFIO_RX_B20p	DIFFOUT_B39p	AD13	AL16	DQ10B	DQ11B		DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B20n	DIFFOUT_B39n	AE12	AM16	DQ10B	DQ11B		DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40p	AE13	AM17	DQ10B	DQ11B		DQ10B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B40n	AE14	AL17	DQ10B	DQ11B		DQ10B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21p	DIFFOUT_B41p	AC12	AK15	DQS10B	DQS11B/CQ11B		DQS10B	DQS11B/CQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B21n	DIFFOUT_B41n	AD11	AL15	DQSn10B	DQSn11B/DQ11B		DQSn10B	DQSn11B/DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42p	AF12	AM14	DQ11B	DQ11B		DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B42n	AH11	AM15	DQ11B	DQ11B		DQ11B	DQ11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22p	DIFFOUT_B43p	AE11	AK14	DQS11B	DQ11B/CQn11B		DQS11B	DQ11B/CQn11B	
4C	VREFB4CN0	IO			DIFFIO_RX_B22n	DIFFOUT_B43n	AF11	AL14	DQSn11B	DQ11B		DQSn11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44p	AH10	AN14	DQ11B	DQ11B		DQ11B	DQ11B	
4C	VREFB4CN0	IO				DIFFOUT_B44n	AG11	AP14	DQ11B	DQ11B		DQ11B	DQ11B	
4A	VREFB4AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B45p	Y12	AE15						
4A	VREFB4AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B45n	AA11	AF15						
4A	VREFB4AN0	IO				DIFFOUT_B46p	Y10	AF14						
4A	VREFB4AN0	IO				DIFFOUT_B46n	Y11	AG15						
4A	VREFB4AN0	IO			DIFFIO_RX_B24p	DIFFOUT_B47p	AC10	AN12	DQ12B	DQ15B		DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B24n	DIFFOUT_B47n	AD10	AP12	DQ12B	DQ15B		DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48p	AB9	AM13	DQ12B	DQ15B		DQ12B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B48n	AB10	AP13	DQ12B	DQ15B		DQ12B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25p	DIFFOUT_B49p	AE9	AN11	DQS12B	DQS15B/CQ15B		DQS12B	DQS15B/CQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B25n	DIFFOUT_B49n	AE10	AP11	DQSn12B	DQSn15B/DQ15B		DQSn12B	DQSn15B/DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50p	AF10	AJ12	DQ13B	DQ15B		DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B50n	AF9	AL13	DQ13B	DQ15B		DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26p	DIFFOUT_B51p	AG8	AL11	DQS13B	DQ15B/CQn15B		DQS13B	DQ15B/CQn15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B26n	DIFFOUT_B51n	AH8	AM11	DQSn13B	DQ15B		DQSn13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52p	AH9	AK12	DQ13B	DQ15B		DQ13B	DQ15B	
4A	VREFB4AN0	IO				DIFFOUT_B52n	AG10	AL12	DQ13B	DQ15B		DQ13B	DQ15B	
4A	VREFB4AN0	IO			DIFFIO_RX_B27p	DIFFOUT_B53p	AG7	AH13	DQ14B	DQ16B	DQ17B	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B27n	DIFFOUT_B53n	AH6	AJ13	DQ14B	DQ16B	DQ17B	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54p	AH5	AH11	DQ14B	DQ16B	DQ17B	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B54n	AH7	AH12	DQ14B	DQ16B	DQ17B	DQ14B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28p	DIFFOUT_B55p	AF6	AH14	DQS14B	DQS16B/CQ16B	DQ17B	DQS14B	DQS16B/CQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B28n	DIFFOUT_B55n	AG5	AJ14	DQSn14B	DQSn16B/DQ16B	DQ17B	DQSn14B	DQSn16B/DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56p	AE7	AJ10	DQ15B	DQ16B	DQ17B	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B56n	AE8	AK11	DQ15B	DQ16B	DQ17B	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29p	DIFFOUT_B57p	AE6	AL10	DQS15B	DQ16B/CQn16B	DQS17B/CQ17B	DQS15B	DQ16B/CQn16B	DQS17B/CQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B29n	DIFFOUT_B57n	AF7	AM10	DQSn15B	DQ16B	DQSn17B/DQ17B	DQSn15B	DQ16B	DQSn17B/DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58p	AD7	AL9	DQ15B	DQ16B	DQ17B	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B58n	AD8	AL8	DQ15B	DQ16B	DQ17B	DQ15B	DQ16B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30p	DIFFOUT_B59p	AG4	AN9	DQ16B	DQ17B	DQ17B	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B30n	DIFFOUT_B59n	AH4	AP9	DQ16B	DQ17B	DQ17B	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60p	AF3	AM8	DQ16B	DQ17B	DQ17B	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B60n	AF4	AP10	DQ16B	DQ17B	DQ17B	DQ16B	DQ17B	DQ17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31p	DIFFOUT_B61p	AH2	AN8	DQS16B	DQS17B/CQ17B	DQ17B/CQn17B	DQS16B	DQS17B/CQ17B	DQ17B/CQn17B
4A	VREFB4AN0	IO			DIFFIO_RX_B31n	DIFFOUT_B61n	AH3	AP8	DQSn16B	DQSn17B/DQ17B	DQ17B	DQSn16B	DQSn17B/DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62p	AC6	AN6	DQ17B	DQ17B	DQ17B	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B62n	AC8	AP7	DQ17B	DQ17B	DQ17B	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B32p	DIFFOUT_B63p	AA8	AN5	DQS17B	DQ17B/CQn17B	DQ17B	DQS17B	DQ17B/CQn17B	DQ17B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B32n	DIFFOUT_B63n	AB7	AP5	DQSn17B	DQ17B	DQ17B	DQSn17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64p	Y9	AP4	DQ17B	DQ17B	DQ17B	DQ17B	DQ17B	DQ17B
4A	VREFB4AN0	IO				DIFFOUT_B64n	AA10	AP6	DQ17B	DQ17B	DQ17B	DQ17B	DQ17B	DQ17B
		nIO_PULLUP		nIO_PULLUP			Y8	AN2						
		nCEO		nCEO			W6	AL3						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		DCLK		DCLK			Y6	AM3						
		nCSO		nCSO			W7	AM2						
		ASDO		ASDO			Y7	AM1						
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n		AC11						
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p		AC12						
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n		AL6						
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p		AM7						
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n		AB12				DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p		AA12				DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n		AM5				DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p		AM6				DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n		AF11				DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p		AE12				DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n		AL5				DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p		AK6				DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n		AE8				DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p		AF9				DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n		AH7				DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p		AJ8				DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n		AE9				DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p		AE10				DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n		AJ6				DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p		AJ7				DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n		AG12				DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p		AF12				DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n		AH8				DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p		AJ9				DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n		AF10				DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p		AG11				DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n		AL7				DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p		AK8				DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n		AD11						
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p		AD12						
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n		AG8						
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p		AG9						
5C	VREFB5CN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n		AB10						
5C	VREFB5CN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p		AB11						
5C	VREFB5CN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n		AE6				DQSn5R		
5C	VREFB5CN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p		AF7				DQS5R		
5C	VREFB5CN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n		AB9				DQ5R		
5C	VREFB5CN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p		AC10				DQ5R		
5C	VREFB5CN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n		AG6				DQ5R		
5C	VREFB5CN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p		AF6				DQ5R		
5C	VREFB5CN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n		Y10				DQ6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p		AA11				DQ6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n		AD6				DQSn6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p		AE7				DQS6R	DQ5R/CQn5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n		Y12				DQ6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p		W12				DQ6R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n		AD8				DQSn7R	DQSn5R/DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p		AD9				DQS7R	DQS5R/CQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n		AA8				DQ7R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p		AA9				DQ7R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n		AC7				DQ7R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p		AB8				DQ7R	DQ5R	
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n		V10						
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p		W11						
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R14n	DIFFOUT_R28n		AC6						
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R14p	DIFFOUT_R28p		AB6						
5C	VREFB5CN0	CLK8n	CLK8n					AA6						
5C	VREFB5CN0	CLK8p	CLK8p					AA7						
6C	VREFB6CN0	CLK10p	CLK10p					N7						
6C	VREFB6CN0	CLK10n	CLK10n					N6						
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R15p	DIFFOUT_R29p		M6						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R15n	DIFFOUT_R29n		M5						
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R15p	DIFFOUT_R30p		T9						
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R15n	DIFFOUT_R30n		U9						
6C	VREFB6CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R31p		M7				DQ8R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R31n		L6				DQ8R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R32p		R11				DQ8R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R32n		R10				DQ8R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R33p		J5				DQS8R	DQS10R/CQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R33n		K5				DQSn8R	DQSn10R/DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R34p		T11				DQ9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R34n		U10				DQ9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R35p		K6				DQS9R	DQ10R/CQn10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R35n		L5				DQSn9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R36p		R13				DQ9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R36n		R12				DQ9R	DQ10R	
6C	VREFB6CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R37p		L9				DQ10R		
6C	VREFB6CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R37n		M8				DQ10R		
6C	VREFB6CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R38p		N9				DQ10R		
6C	VREFB6CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R38n		N8				DQ10R		
6C	VREFB6CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R39p		L8				DQS10R		
6C	VREFB6CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R39n		K7				DQSn10R		
6C	VREFB6CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R40p		N10						
6C	VREFB6CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R40n		P9						
6A	VREFB6AN0	IO			DIFFIO_RX_R21p	DIFFOUT_R41p		J7						
6A	VREFB6AN0	IO			DIFFIO_RX_R21n	DIFFOUT_R41n		H6						
6A	VREFB6AN0	IO			DIFFIO_TX_R21p	DIFFOUT_R42p		L11						
6A	VREFB6AN0	IO			DIFFIO_TX_R21n	DIFFOUT_R42n		M10						
6A	VREFB6AN0	IO			DIFFIO_RX_R22p	DIFFOUT_R43p		F9				DQ11R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R22n	DIFFOUT_R43n		G8				DQ11R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R22p	DIFFOUT_R44p		H9				DQ11R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R22n	DIFFOUT_R44n		J8				DQ11R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R45p		G9				DQS11R	DQS13R/CQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R45n		H8				DQSn11R	DQSn13R/DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R23p	DIFFOUT_R46p		H11				DQ12R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R23n	DIFFOUT_R46n		J10				DQ12R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p		G7				DQS12R	DQ13R/CQn13R	DQS14R/CQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n		G6				DQSn12R	DQ13R	DQSn14R/DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p		P12				DQ12R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n		P11				DQ12R	DQ13R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p		F7				DQ13R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n		F6				DQ13R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p		J9				DQ13R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n		K8				DQ13R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p		C6				DQS13R	DQS14R/CQ14R	DQ14R/CQn14R
6A	VREFB6AN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n		C5				DQSn13R	DQSn14R/DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p		K11				DQ14R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n		K10				DQ14R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p		D7				DQS14R	DQ14R/CQn14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n		E6				DQSn14R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p		M12				DQ14R	DQ14R	DQ14R
6A	VREFB6AN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n		M11				DQ14R	DQ14R	DQ14R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R28p	DIFFOUT_R55p		C7						
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R28n	DIFFOUT_R55n		D6						
6A	VREFB6AN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p		N12						
6A	VREFB6AN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n		N11						
		MSEL2		MSEL2			J7	B1						
		MSEL1		MSEL1			J9	C3						
		MSEL0		MSEL0			K9	B2						
7A	VREFB7AN0	IO				DIFFOUT_T1n	F7	A6	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	G8	A4	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	E7	A5	DQSn1T	DQ1T	DQ1T	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	F8	B5	DQS1T	DQ1T/CQn1T	DQ1T	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	G9	A7	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	H9	B6	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T	DQ1T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	D6	A8	DQSn2T	DQSn1T/DQ1T	DQ1T	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	E6	B8	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	D5	A10	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	F6	C9	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	C4	A9	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	C5	B9	DQ2T	DQ1T	DQ1T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	A2	E8	DQ3T	DQ2T	DQ1T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	B3	D8	DQ3T	DQ2T	DQ1T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	A3	C10	DQSn3T	DQ2T	DQSn1T/DQ1T	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	B4	D10	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	A5	F10	DQ3T	DQ2T	DQ1T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	A4	D9	DQ3T	DQ2T	DQ1T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A6	G12	DQSn4T	DQSn2T/DQ2T	DQ1T	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	B6	H12	DQS4T	DQS2T/CQ2T	DQ1T	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	C7	F13	DQ4T	DQ2T	DQ1T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	D7	G13	DQ4T	DQ2T	DQ1T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A7	F11	DQ4T	DQ2T	DQ1T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B7	G11	DQ4T	DQ2T	DQ1T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	B9	C12	DQ5T	DQ3T		DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	A8	D12	DQ5T	DQ3T		DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	D11	DQSn5T	DQ3T		DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	E11	DQS5T	DQ3T/CQn3T		DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	B10	D13	DQ5T	DQ3T		DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	A9	E12	DQ5T	DQ3T		DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	D10	A11	DQSn6T	DQSn3T/DQ3T		DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	E9	B11	DQS6T	DQS3T/CQ3T		DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	F10	A13	DQ6T	DQ3T		DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	E10	C13	DQ6T	DQ3T		DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	C10	A12	DQ6T	DQ3T		DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	D9	B12	DQ6T	DQ3T		DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	H10	F14						
7A	VREFB7AN0	IO				DIFFOUT_T19p	G11	H14						
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	J11	H15						
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	J12	J15						
7C	VREFB7CN0	IO				DIFFOUT_T21n	A11	A14	DQ7T	DQ7T		DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T21p	A10	B14	DQ7T	DQ7T		DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	C11	D14	DQSn7T	DQ7T		DQSn7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	D11	E14	DQS7T	DQ7T/CQn7T		DQS7T	DQ7T/CQn7T	
7C	VREFB7CN0	IO				DIFFOUT_T23n	B12	C15	DQ7T	DQ7T		DQ7T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T23p	D12	C14	DQ7T	DQ7T		DQ7T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	E12	D15	DQSn8T	DQSn7T/DQ7T		DQSn8T	DQSn7T/DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	F11	E15	DQS8T	DQS7T/CQ7T		DQS8T	DQS7T/CQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25n	F13	D17	DQ8T	DQ7T		DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T25p	E13	C17	DQ8T	DQ7T		DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	C13	C16	DQ8T	DQ7T		DQ8T	DQ7T	
7C	VREFB7CN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	D13	D16	DQ8T	DQ7T		DQ8T	DQ7T	
7C	VREFB7CN0	IO				DIFFOUT_T27n	H12	E17	DQ9T			DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T27p	G12	L17	DQ9T			DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	G14	J16	DQSn9T			DQSn9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	H13	K16	DQS9T			DQS9T		
7C	VREFB7CN0	IO				DIFFOUT_T29n	J14	F15	DQ9T			DQ9T		
7C	VREFB7CN0	IO				DIFFOUT_T29p	J13	G16	DQ9T			DQ9T		
7C	VREFB7CN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C14	J17						
7C	VREFB7CN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D14	K17						
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T31n	A14	A17						
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T31p	B13	B17						
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T16n	DIFFOUT_T32n	A12	A15						
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T16p	DIFFOUT_T32p	A13	B15						
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T17p	DIFFOUT_T33p	B15	B18						
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T17n	DIFFOUT_T33n	A15	A18						
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T34p	B16	B20						
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T34n	A16	A20						
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T18p	DIFFOUT_T35p	D15	D18						
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T18n	DIFFOUT_T35n	C15	C18						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T36p	J15	K18						
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T36n	H15	J18						
8C	VREFB8CN0	IO			DIFFIO_RX_T19p	DIFFOUT_T37p	E16	K19						
8C	VREFB8CN0	IO			DIFFIO_RX_T19n	DIFFOUT_T37n	D16	J19						
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T38p	J16	L18						
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T38n	H16	M18						
8C	VREFB8CN0	IO			DIFFIO_RX_T20p	DIFFOUT_T39p	A19	D19	DQ10T	DQ11T		DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T20n	DIFFOUT_T39n	A18	C19	DQ10T	DQ11T		DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40p	A17	F19	DQ10T	DQ11T		DQ10T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T40n	B18	F20	DQ10T	DQ11T		DQ10T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21p	DIFFOUT_T41p	C18	E20	DQS10T	DQS11T/CQ11T		DQS10T	DQS11T/CQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T21n	DIFFOUT_T41n	C17	D20	DQSn10T	DQSn11T/DQ11T		DQSn10T	DQSn11T/DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42p	G17	C20	DQ11T	DQ11T		DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T42n	D17	C21	DQ11T	DQ11T		DQ11T	DQ11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22p	DIFFOUT_T43p	F17	E21	DQS11T	DQ11T/CQn11T		DQS11T	DQ11T/CQn11T	
8C	VREFB8CN0	IO			DIFFIO_RX_T22n	DIFFOUT_T43n	E18	D21	DQSn11T	DQ11T		DQSn11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44p	D18	A21	DQ11T	DQ11T		DQ11T	DQ11T	
8C	VREFB8CN0	IO				DIFFOUT_T44n	F18	B21	DQ11T	DQ11T		DQ11T	DQ11T	
8A	VREFB8AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T45p	J17	J21						
8A	VREFB8AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T45n	H18	H21						
8A	VREFB8AN0	IO				DIFFOUT_T46p	H19	J20						
8A	VREFB8AN0	IO				DIFFOUT_T46n	J18	G20						
8A	VREFB8AN0	IO			DIFFIO_RX_T24p	DIFFOUT_T47p	C19	B23	DQ12T	DQ15T		DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T24n	DIFFOUT_T47n	B19	A23	DQ12T	DQ15T		DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48p	A20	A22	DQ12T	DQ15T		DQ12T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T48n	A21	C22	DQ12T	DQ15T		DQ12T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T49p	C20	B24	DQS12T	DQS15T/CQ15T		DQS12T	DQS15T/CQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T49n	B21	A24	DQSn12T	DQSn15T/DQ15T		DQSn12T	DQSn15T/DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50p	F19	F22	DQ13T	DQ15T		DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T50n	G19	G22	DQ13T	DQ15T		DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26p	DIFFOUT_T51p	E19	D23	DQS13T	DQ15T/CQn15T		DQS13T	DQ15T/CQn15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T26n	DIFFOUT_T51n	D19	C23	DQSn13T	DQ15T		DQSn13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52p	D20	F21	DQ13T	DQ15T		DQ13T	DQ15T	
8A	VREFB8AN0	IO				DIFFOUT_T52n	F20	D22	DQ13T	DQ15T		DQ13T	DQ15T	
8A	VREFB8AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T53p	D21	E24	DQ14T	DQ16T	DQ17T	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T53n	C21	D24	DQ14T	DQ16T	DQ17T	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54p	A22	G23	DQ14T	DQ16T	DQ17T	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T54n	A23	G24	DQ14T	DQ16T	DQ17T	DQ14T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28p	DIFFOUT_T55p	C22	F23	DQS14T	DQS16T/CQ16T	DQ17T	DQS14T	DQS16T/CQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T28n	DIFFOUT_T55n	B22	E23	DQSn14T	DQSn16T/DQ16T	DQ17T	DQSn14T	DQSn16T/DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56p	H21	G25	DQ15T	DQ16T	DQ17T	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T56n	E21	F25	DQ15T	DQ16T	DQ17T	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T57p	E22	D25	DQS15T	DQ16T/CQn16T	DQS17T/CQ17T	DQS15T	DQ16T/CQn16T	DQS17T/CQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T57n	D22	C25	DQSn15T	DQ16T	DQSn17T/DQ17T	DQSn15T	DQ16T	DQSn17T/DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58p	G21	D27	DQ15T	DQ16T	DQ17T	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T58n	F21	D26	DQ15T	DQ16T	DQ17T	DQ15T	DQ16T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30p	DIFFOUT_T59p	B24	B26	DQ16T	DQ17T	DQ17T	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T30n	DIFFOUT_T59n	A24	A26	DQ16T	DQ17T	DQ17T	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60p	D24	A25	DQ16T	DQ17T	DQ17T	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T60n	C25	C26	DQ16T	DQ17T	DQ17T	DQ16T	DQ17T	DQ17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T61p	D23	B27	DQS16T	DQS17T/CQ17T	DQ17T/CQn17T	DQS16T	DQS17T/CQ17T	DQ17T/CQn17T
8A	VREFB8AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T61n	C24	A27	DQSn16T	DQSn17T/DQ17T	DQ17T	DQSn16T	DQSn17T/DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62p	A26	A28	DQ17T	DQ17T	DQ17T	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T62n	C26	B29	DQ17T	DQ17T	DQ17T	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T32p	DIFFOUT_T63p	B25	B30	DQS17T	DQ17T/CQn17T	DQ17T	DQS17T	DQ17T/CQn17T	DQ17T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T32n	DIFFOUT_T63n	A25	A30	DQSn17T	DQ17T	DQ17T	DQSn17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64p	A27	A29	DQ17T	DQ17T	DQ17T	DQ17T	DQ17T	DQ17T
8A	VREFB8AN0	IO				DIFFOUT_T64n	B27	A31	DQ17T	DQ17T	DQ17T	DQ17T	DQ17T	DQ17T
QL1		GXB_TX_L7n						E32						
QL1		GXB_TX_L7p						E31						
QL1		GXB_RX_L7n						F34						
QL1		GXB_RX_L7p						F33						
QL1		GXB_TX_L6n						G32						
QL1		GXB_TX_L6p						G31						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
QL1		GXB_RX_L6n						H34						
QL1		GXB_RX_L6p						H33						
QL1		GXB_CMUTX_L3n						J32						
QL1		GXB_CMUTX_L3p						J31						
QL1		REFCLK_L3n, GXB_CMURX_L3n						K34						
QL1		REFCLK_L3p, GXB_CMURX_L3p						K33						
QL1		GXB_CMUTX_L2n						L32						
QL1		GXB_CMUTX_L2p						L31						
QL1		REFCLK_L2n, GXB_CMURX_L2n						M34						
QL1		REFCLK_L2p, GXB_CMURX_L2p						M33						
QL1		GXB_TX_L5n						N32						
QL1		GXB_TX_L5p						N31						
QL1		GXB_RX_L5n						P34						
QL1		GXB_RX_L5p						P33						
QL1		GXB_TX_L4n						R32						
QL1		GXB_TX_L4p						R31						
QL1		GXB_RX_L4n						T34						
QL1		GXB_RX_L4p						T33						
QL0		GXB_TX_L3n						U32						
QL0		GXB_TX_L3p						U31						
QL0		GXB_RX_L3n						V34						
QL0		GXB_RX_L3p						V33						
QL0		GXB_TX_L2n						W32						
QL0		GXB_TX_L2p						W31						
QL0		GXB_RX_L2n						Y34						
QL0		GXB_RX_L2p						Y33						
QL0		GXB_CMUTX_L1n						AA32						
QL0		GXB_CMUTX_L1p						AA31						
QL0		REFCLK_L1n, GXB_CMURX_L1n						AB34						
QL0		REFCLK_L1p, GXB_CMURX_L1p						AB33						
QL0		GXB_CMUTX_L0n						AC32						
QL0		GXB_CMUTX_L0p						AC31						
QL0		REFCLK_L0n, GXB_CMURX_L0n						AD34						
QL0		REFCLK_L0p, GXB_CMURX_L0p						AD33						
QL0		GXB_TX_L1n						AE32						
QL0		GXB_TX_L1p						AE31						
QL0		GXB_RX_L1n						AF34						
QL0		GXB_RX_L1p						AF33						
QL0		GXB_TX_L0n						AG32						
QL0		GXB_TX_L0p						AG31						
QL0		GXB_RX_L0n						AH34						
QL0		GXB_RX_L0p						AH33						
QR0		GXB_RX_R0p					AD2	AH2						
QR0		GXB_RX_R0n					AD1	AH1						
QR0		GXB_TX_R0p					AC4	AG4						
QR0		GXB_TX_R0n					AC3	AG3						
QR0		GXB_RX_R1p					AB2	AF2						
QR0		GXB_RX_R1n					AB1	AF1						
QR0		GXB_TX_R1p					AA4	AE4						
QR0		GXB_TX_R1n					AA3	AE3						
QR0		REFCLK_R0p, GXB_CMURX_R0p					Y2	AD2						
QR0		REFCLK_R0n, GXB_CMURX_R0n					Y1	AD1						
QR0		GXB_CMUTX_R0p						AC4						
QR0		GXB_CMUTX_R0n						AC3						
QR0		REFCLK_R1p, GXB_CMURX_R1p					W4	AB2						
QR0		REFCLK_R1n, GXB_CMURX_R1n					W3	AB1						
QR0		GXB_CMUTX_R1p						AA4						
QR0		GXB_CMUTX_R1n						AA3						
QR0		GXB_RX_R2p					V2	Y2						
QR0		GXB_RX_R2n					V1	Y1						
QR0		GXB_TX_R2p					U4	W4						
QR0		GXB_TX_R2n					U3	W3						
QR0		GXB_RX_R3p					T2	V2						
QR0		GXB_RX_R3n					T1	V1						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
QR0		GXB_TX_R3p					R4	U4						
QR0		GXB_TX_R3n					R3	U3						
QR1		GXB_RX_R4p					P2	T2						
QR1		GXB_RX_R4n					P1	T1						
QR1		GXB_TX_R4p					N4	R4						
QR1		GXB_TX_R4n					N3	R3						
QR1		GXB_RX_R5p					M2	P2						
QR1		GXB_RX_R5n					M1	P1						
QR1		GXB_TX_R5p					L4	N4						
QR1		GXB_TX_R5n					L3	N3						
QR1		REFCLK_R2p, GXB_CMURX_R2p					K2	M2						
QR1		REFCLK_R2n, GXB_CMURX_R2n					K1	M1						
QR1		GXB_CMUTX_R2p						L4						
QR1		GXB_CMUTX_R2n						L3						
QR1		REFCLK_R3p, GXB_CMURX_R3p					J4	K2						
QR1		REFCLK_R3n, GXB_CMURX_R3n					J3	K1						
QR1		GXB_CMUTX_R3p						J4						
QR1		GXB_CMUTX_R3n						J3						
QR1		GXB_RX_R6p					H2	H2						
QR1		GXB_RX_R6n					H1	H1						
QR1		GXB_TX_R6p					G4	G4						
QR1		GXB_TX_R6n					G3	G3						
QR1		GXB_RX_R7p					F2	F2						
QR1		GXB_RX_R7n					F1	F1						
QR1		GXB_TX_R7p					E4	E4						
QR1		GXB_TX_R7n					E3	E3						
		GND					W8	AN1						
		GND					P15	U18						
		GND					AG3	E7						
		GND					AG6	AN4						
		GND					AG9	AN7						
		GND					AG12	AN10						
		GND					AG15	AN13						
		GND					AG18	AN16						
		GND					AG21	AN19						
		GND					AG24	AN22						
		GND					AG27	AN25						
		GND					AD6	AN28						
		GND					AD9	AN31						
		GND					AD12	AK4						
		GND					AD15	AK7						
		GND					AD18	AK10						
		GND					AD21	AK13						
		GND					AD24	AK16						
		GND					AD27	AK19						
		GND					AA6	AK22						
		GND					AA9	AK25						
		GND					AA12	AK28						
		GND					AA15	AK31						
		GND					AA18	AG7						
		GND					AA21	AG10						
		GND					AA24	AG13						
		GND					AA27	AG16						
		GND					W12	AG19						
		GND					W14	AG22						
		GND					W16	AG25						
		GND					W18	AG28						
		GND					W19	AD7						
		GND					V9	AD10						
		GND					V11	AD13						
		GND					V13	AD16						
		GND					V15	AD19						
		GND					V17	AD22						
		GND					V19	AD25						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					V21	AD28						
		GND					V24	AB7						
		GND					V27	AB13						
		GND					U12	AB15						
		GND					U14	AB17						
		GND					U16	AB19						
		GND					U18	AB21						
		GND					T11	AB28						
		GND					T13	AA10						
		GND					T15	AA14						
		GND					T17	AA16						
		GND					T19	AA18						
		GND					R12	AA20						
		GND					R16	AA22						
		GND					R18	AA25						
		GND					R21	Y13						
		GND					R24	Y15						
		GND					R27	Y17						
		GND					P11	Y19						
		GND					P13	Y21						
		GND					P17	W10						
		GND					P19	W14						
		GND					N12	W16						
		GND					N14	W18						
		GND					N16	W20						
		GND					N18	W22						
		GND					M11	W25						
		GND					M13	V13						
		GND					M15	V15						
		GND					M17	V19						
		GND					M19	V21						
		GND					M21	U14						
		GND					M24	U16						
		GND					M27	U20						
		GND					L8	U22						
		GND					L12	T10						
		GND					L14	T13						
		GND					L16	T15						
		GND					L18	T17						
		GND					K11	T19						
		GND					K13	T21						
		GND					K15	T25						
		GND					K17	R14						
		GND					K19	R16						
		GND					J21	R18						
		GND					J24	R20						
		GND					J27	R22						
		GND					H5	P10						
		GND					H8	P13						
		GND					H11	P15						
		GND					H14	P17						
		GND					H17	P19						
		GND					H20	P21						
		GND					F24	P25						
		GND					F27	N14						
		GND					E5	N16						
		GND					E8	N18						
		GND					E11	N20						
		GND					E14	N22						
		GND					E17	L7						
		GND					E20	L10						
		GND					E23	L13						
		GND					C27	L16						
		GND					B2	L19						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					B5	L22						
		GND					B8	L25						
		GND					B11	L28						
		GND					B14	H7						
		GND					B17	H10						
		GND					B20	H13						
		GND					B23	H16						
		GND					B26	H19						
		GND					C2	H22						
		GND					C1	H25						
		GND					D4	H28						
		GND					D3	E10						
		GND					D2	E13						
		GND					E2	E16						
		GND					E1	E19						
		GND					F4	E22						
		GND					F3	E25						
		GND					G2	E28						
		GND					G1	B4						
		GND					H4	B7						
		GND					H3	B10						
		GND					J2	B13						
		GND					J1	B16						
		GND					K4	B19						
		GND					K3	B22						
		GND					L5	B25						
		GND					L2	B28						
		GND					L1	B31						
		GND					M6	C34						
		GND					M4	C33						
		GND					M3	D33						
		GND					N7	D32						
		GND					N5	D31						
		GND					N2	D30						
		GND					N1	E34						
		GND					P8	E33						
		GND					P6	E30						
		GND					P4	F32						
		GND					P3	F31						
		GND					R7	F30						
		GND					R5	G34						
		GND					R2	G33						
		GND					R1	G30						
		GND					T8	H32						
		GND					T6	H31						
		GND					T4	AL33						
		GND					T3	AL34						
		GND					U5	AK30						
		GND					U2	AK33						
		GND					U1	AJ30						
		GND					V6	AJ33						
		GND					V4	AJ34						
		GND					V3	AH30						
		GND					W2	AH31						
		GND					W1	AH32						
		GND					Y4	AG30						
		GND					Y3	AG33						
		GND					AA2	AG34						
		GND					AA1	AF30						
		GND					AB4	AF31						
		GND					AB3	AF32						
		GND					AC2	AE30						
		GND					AC1	AE33						
		GND					AD4	AE34						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					AD3	AD30						
		GND					AE2	AD31						
		GND					AE1	AD32						
		GND					AF2	AC33						
		GND					AG2	AC34						
		GND					AG1	AB30						
		GND						AB31						
		GND						AB32						
		GND						AA33						
		GND						AA34						
		GND						Y28						
		GND						Y29						
		GND						Y30						
		GND						Y31						
		GND						Y32						
		GND						W33						
		GND						W34						
		GND						V27						
		GND						V29						
		GND						V30						
		GND						V31						
		GND						V32						
		GND						U28						
		GND						U29						
		GND						U33						
		GND						U34						
		GND						T30						
		GND						T31						
		GND						T32						
		GND						R27						
		GND						R29						
		GND						R33						
		GND						R34						
		GND						P27						
		GND						P28						
		GND						P29						
		GND						P30						
		GND						P31						
		GND						P32						
		GND						N33						
		GND						N34						
		GND						M31						
		GND						M32						
		GND						L33						
		GND						L34						
		GND						K31						
		GND						K32						
		GND						J33						
		GND						J34						
		GND						H30						
		GND						C2						
		GND						C1						
		GND						D5						
		GND						D4						
		GND						D3						
		GND						D2						
		GND						AL1						
		GND						E5						
		GND						E2						
		GND						E1						
		GND						F5						
		GND						F4						
		GND						F3						
		GND						G5						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND						G2						
		GND						G1						
		GND						H5						
		GND						P5						
		GND						AL2						
		GND						AK2						
		GND						AK5						
		GND						AJ1						
		GND						AJ2						
		GND						AJ5						
		GND						AH3						
		GND						AH4						
		GND						AH5						
		GND						AG1						
		GND						AG2						
		GND						AG5						
		GND						AF3						
		GND						AF4						
		GND						AF5						
		GND						AE1						
		GND						AE2						
		GND						AE5						
		GND						AD3						
		GND						AD4						
		GND						AD5						
		GND						AC1						
		GND						AC2						
		GND						AB3						
		GND						AB4						
		GND						AB5						
		GND						AA1						
		GND						AA2						
		GND						Y3						
		GND						Y4						
		GND						Y5						
		GND						Y6						
		GND						Y7						
		GND						W1						
		GND						W2						
		GND						V3						
		GND						V4						
		GND						V5						
		GND						V6						
		GND						V8						
		GND						U1						
		GND						U2						
		GND						U6						
		GND						U7						
		GND						T3						
		GND						T4						
		GND						T5						
		GND						R1						
		GND						R2						
		GND						R6						
		GND						R8						
		GND						P3						
		GND						P4						
		GND						P6						
		GND						P7						
		GND						P8						
		GND						N1						
		GND						N2						
		GND						M3						
		GND						M4						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND						L1						
		GND						L2						
		GND						K3						
		GND						K4						
		GND						J1						
		GND						J2						
		GND						H3						
		GND						H4						
		VCC					P14	U17						
		VCC					V12	AA15						
		VCC					V14	AA17						
		VCC					V16	AA19						
		VCC					V18	AA21						
		VCC					U11	Y14						
		VCC					U13	Y16						
		VCC					U15	Y18						
		VCC					U17	Y20						
		VCC					T12	W15						
		VCC					T14	W17						
		VCC					T16	W19						
		VCC					T18	W21						
		VCC					R11	V14						
		VCC					R13	V16						
		VCC					R15	V18						
		VCC					R17	V20						
		VCC					P12	U15						
		VCC					P16	U19						
		VCC					P18	U21						
		VCC					N11	T14						
		VCC					N13	T16						
		VCC					N15	T18						
		VCC					N17	T20						
		VCC					M12	R15						
		VCC					M14	R17						
		VCC					M16	R19						
		VCC					M18	R21						
		VCC					L11	P14						
		VCC					L13	P16						
		VCC					L15	P18						
		VCC					L17	P20						
		VCC					U7	Y27						
		VCC					U8	W27						
		VCC					M7	U27						
		VCC					M8	T27						
		VCC						Y8						
		VCC						W8						
		VCC						U8						
		VCC						T8						
		VCCPT					R22	V23						
		VCCPT					P22	U23						
		VCCPT					AB14	AH17						
		VCCPT					R10	V12						
		VCCPT					P10	U12						
		VCCPT					G15	G17						
		DNU					R14	V17						
		VCCPGM					Y20	AK26						
		VCCPGM					W9	AH10						
		TEMPDIODEn					H7	A3						
		TEMPDIODEp					G6	B3						
		VCC_CLKIN3C					AD14	AJ18						
		VCC_CLKIN4C					AC13	AG17						
		VCC_CLKIN7C					F14	H17						
		VCC_CLKIN8C					F16	F18						
		VCCBAT					H6	E9						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		VCCA_PLL_B1					AC14	AH18						
		VCCA_PLL_L2					R23	U24						
		VCCA_PLL_R2						V11						
		VCCA_PLL_T1					E15	G18						
		VCCD_PLL_B1					AC15	AG18						
		VCCD_PLL_L2					P23	V24						
		VCCD_PLL_R2						U11						
		VCCD_PLL_T1					F15	H18						
		VCCIO1A					J23	N24						
		VCCIO1A					H26	J24						
		VCCIO1A					E26	F27						
		VCCIO1C					P24	T23						
		VCCIO1C					N26	M27						
		VCCIO2A					AD25	AH27						
		VCCIO2A					AB26	AE26						
		VCCIO2A					AA23	AC23						
		VCCIO2C					T24	AC27						
		VCCIO2C					T26	AB24						
		VCCIO3A					AF20	AM24						
		VCCIO3A					AF23	AM27						
		VCCIO3A					AC20	AJ24						
		VCCIO3A					Y19	AH21						
		VCCIO3C					AF17	AP19						
		VCCIO3C					AC17	AK18						
		VCCIO4A					AF5	AM9						
		VCCIO4A					AF8	AM12						
		VCCIO4A					AC7	AJ11						
		VCCIO4A					AC9	AH15						
		VCCIO4C					AF13	AP16						
		VCCIO4C					AC11	AJ17						
		VCCIO5A						AH6						
		VCCIO5A						AH9						
		VCCIO5A						AE11						
		VCCIO5C						AC8						
		VCCIO5C						Y11						
		VCCIO6A						J6						
		VCCIO6A						J11						
		VCCIO6A						F8						
		VCCIO6C						T12						
		VCCIO6C						M9						
		VCCIO7A					J10	G15						
		VCCIO7A					F9	F12						
		VCCIO7A					C6	C8						
		VCCIO7A					C9	C11						
		VCCIO7C					F12	F17						
		VCCIO7C					C12	A16						
		VCCIO8A					J19	G21						
		VCCIO8A					F22	F24						
		VCCIO8A					E24	C24						
		VCCIO8A					C23	C27						
		VCCIO8C					G18	E18						
		VCCIO8C					C16	A19						
		VCCPD1A					L19	P22						
		VCCPD1C					N19	T22						
		VCCPD2A					U19	AB22						
		VCCPD2C					R19	V22						
		VCCPD3A					W17	AB20						
		VCCPD3C					W15	AB18						
		VCCPD4A					W11	AB14						
		VCCPD4C					W13	AB16						
		VCCPD5A						AA13						
		VCCPD5C						W13						
		VCCPD6A						N13						
		VCCPD6C						U13						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		VCCPD7A					K12	N15						
		VCCPD7C					K14	N17						
		VCCPD8A					K18	N21						
		VCCPD8C					K16	N19						
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				J22	M25						
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				M22	R26						
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				Y22	AE25						
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				U22	AB25						
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB19	AG20						
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AB16	AH19						
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB8	AG14						
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AB13	AJ16						
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0					AF8						
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0					AC9						
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0					K9						
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0					R9						
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G10	G14						
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G13	F16						
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G20	H20						
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G16	G19						
		NC					F23	A32						
		NC					AE26	AP33						
		NC					AB6	AP2						
		NC					J8	A2						
		NC					AE4	AJ31						
		NC					AE3	AJ32						
		NC					AE5	AJ3						
		NC					AD5	AJ4						
		NC					AC5	AP3						
		NC					AB5	AP32						
		NC					AA5	AN3						
		NC					Y5	AN32						
		NC					W5	AM4						
		NC					W10	AM31						
		NC					V7	AM32						
		NC					V8	AL4						
		NC					V10	AL30						
		NC					U9	AL31						
		NC					U10	AK3						
		NC					U20	AK32						
		NC					T9	AF13						
		NC					T10	AE13						
		NC					N10	AE14						
		NC					M9	AE20						
		NC					M10	AE21						
		NC					M20	AE22						
		NC					L7	AD14						
		NC					L9	AD15						
		NC					L10	AD20						
		NC					K5	AD21						
		NC					K6	AC13						
		NC					K7	AC14						
		NC					K8	AC15						
		NC					K10	AC16						
		NC					K20	AC17						
		NC					J5	AC19						
		NC					J6	AC20						
		NC					G5	AC21						
		NC					F5	AC22						
		NC					C3	M13						
		NC					B1	M14						
		NC						M15						
		NC						M16						
		NC						M17						

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	F1152	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		NC						M19						
		NC						M20						
		NC						M21						
		NC						M22						
		NC						L12						
		NC						L14						
		NC						L15						
		NC						L20						
		NC						L21						
		NC						K12						
		NC						K13						
		NC						K14						
		NC						K15						
		NC						K20						
		NC						K21						
		NC						K22						
		NC						K23						
		NC						J12						
		NC						J13						
		NC						J14						
		NC						J23						
		NC						H23						
		NC						E26						
		NC						E27						
		NC						C4						
		NC						C31						
		VCCAUX					G22	J22						
		VCCAUX					AB22	AF22						
		VCCAUX					AA7	AK9						
		VCCAUX					G7	G10						
		VCCA_L						U30						
		VCCA_L						AC30						
		VCCA_R					N6	AC5						
		VCCA_R					T5	U5						
		VCCH_GXBL0						W29						
		VCCH_GXBL1						T29						
		VCCH_GXBR0					V5	W6						
		VCCH_GXBR1					L6	T6						
		VCCL_GXBL0						V28						
		VCCL_GXBL0						W28						
		VCCL_GXBL1						R28						
		VCCL_GXBL1						T28						
		VCCL_GXBR0					R8	V7						
		VCCL_GXBR0					T7	W7						
		VCCL_GXBR1					N8	T7						
		VCCL_GXBR1					P7	R7						
		VCCR_R					M5	W5						
		VCCR_R					R6	N5						
		VCCR_L						N30						
		VCCR_L						W30						
		VCCT_R					P5	R5						
		VCCT_R					U6	AA5						
		VCCT_L						R30						
		VCCT_L						AA30						
		VCCHIP_R					N9	V9						
		VCCHIP_R					P9	W9						
		VCCHIP_R					R9	Y9						
		VCCHIP_L						V26						
		VCCHIP_L						W26						
		VCCHIP_L						Y26						
		RREF_L0						AK34						
		RREF_L1						D34						
		RREF_R0					AF1	AK1						
		RREF_R1					D1	D1						

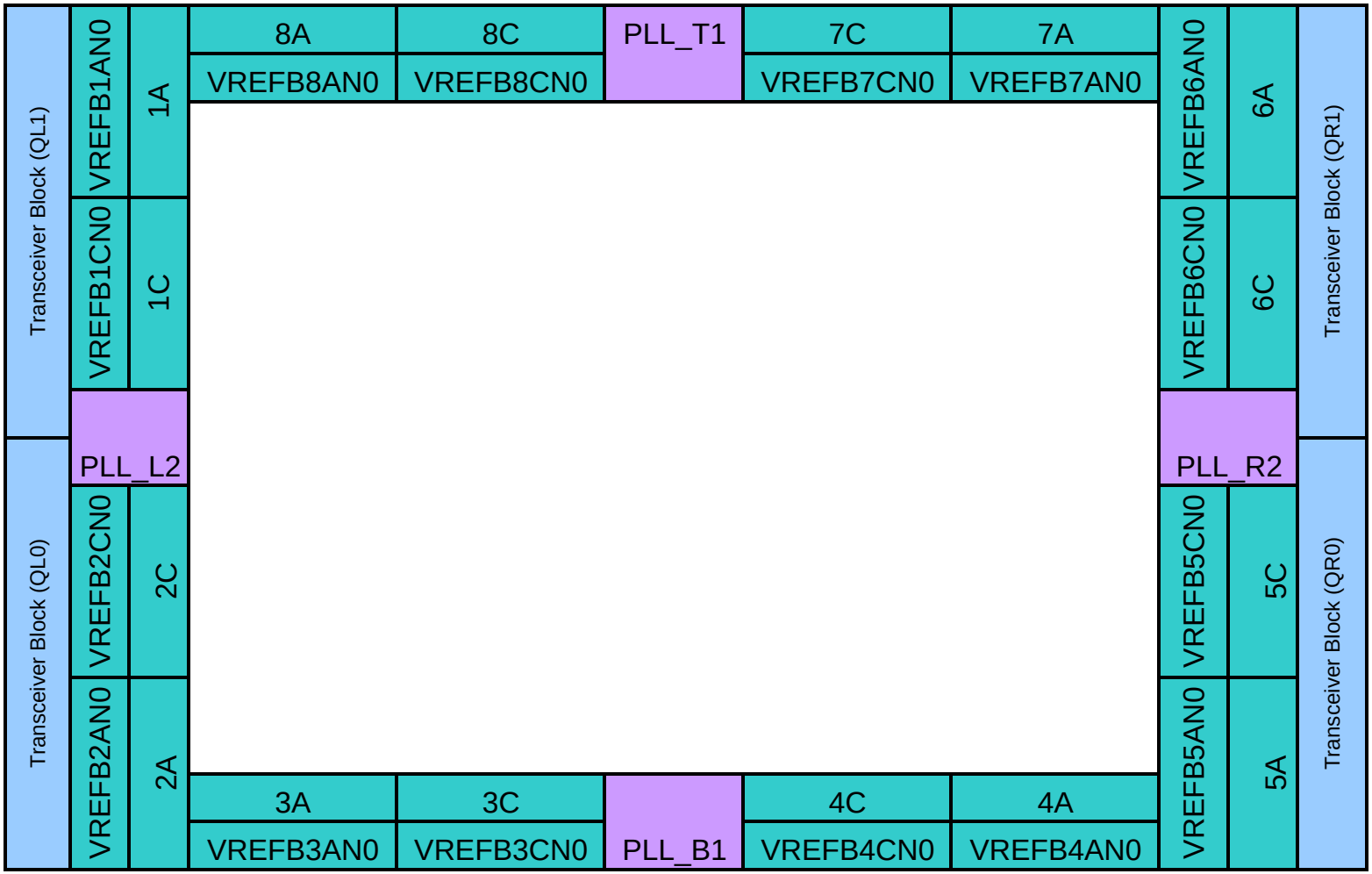
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[0:7], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.
MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
	Optional/Dual-Purpose Configuration Pins	
CRC_ERROR (Note 6)	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
DEV_CLRn (Note 6)	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE (Note 6)	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0 (Note 6)	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[1:7] (Note 6)	I/O, Input	Dual-purpose configuration input data pins. The DATA[1:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
INIT_DONE (Note 6)	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR (Note 6)	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[1:38][T,B], DQS[1:34][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:38][T,B], DQ[1:34][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VCCPT	Power	Power supply for the programmable power technology.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in datasheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), HSTL(12,15,18),SSTL(15,18,2),3.0V PCI/PCI-X I/O as well as LVTTL 3.3V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2V, 1.5V, 1.8V, 2.5V, 3.3V), 3.0V PCI/PCI-X and LVTTL 3.3V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREFB[1:8][A,C]N0, VREFB[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
Transceiver (I/O Banks) Pins		
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p (Note 3)	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n (Note 3)	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p (Note 3)	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n (Note 3)	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]p GXB_CMURX_[L,R][0:7]p (Note 4 and 5)	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n GXB_CMURX_[L,R][0:7]n (Note 4 and 5)	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p (Note 5) GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

1. This pin definition is prepared based on the EP4SGX530.
2. Some of the pull-up /pull-down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
Refer to the Configuring Stratix IV GX Devices chapter in the Stratix IV GX Device Handbook for more information.
3. Transceiver signals GXB_RX[0:15] and GXB_TX[0:15] are device specific.
4. Dual purpose CMU Receiver channels. Can be used either as reference clock or CMU receiver channels in devices with 5th and 6th channels.
5. Only available in package with 5th and 6th channels.
6. These dual purpose configuration pins can only be used as configuration pins but not regular I/O in F780 of EP4SGX360 and EP4SGX290.
7. Refer to Pin Connections Guidelines and datasheet for the recommended operating voltage.



Note:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Pin Information for the Stratix® IV GX EP4SGX70 Device
Version 1.3

Version Number	Date	Changes Made
1.0	9/30/2008	Initial release.
1.1	12/30/2008	Updated VCCBAT from 2.5 V to 3.0 V.
1.2	6/9/2009	Added F1152 package and removed recommended operating voltage in pin definition.
1.3	12/3/2009	Added bank number for JTAG pins.
		Grouped nCSO, ASDO, and DCLK into dedicated configuration/JTAG pins in Pin Definitions.