Stratix® II GX Device Family Pin Connection Guidelines
PCG-01001-3.1

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification.
The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Pin Name	Pin Type (1st, 2nd, 3rd Function)	Pin Description	Connection Guidelines
		Supply and Reference Pins	
VCCINT	Power	1.2-V internal logic array voltage supply pins. VCCINT also supplies power on column dedicated clock input pins for HSTL, SSTL, and all differential IO standards.	All VCCINT pins require a 1.2-V supply. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
VCCIO[1..4,7,8]	Power	I/O supply voltage pins for banks 1-4, 7, and 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for row differential standards and all single-ended I/O standards with the exception of HSTL and SSTL on column dedicated clock input pins, which are powered by VCCINT.	Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
VCCPD[1..4,7,8]	Power	Dedicated power pins. This 3.3-V supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR.	The VCCPD pins require 3.3 V and must ramp up from 0 V to 3.3 V within 100 ms to ensure successful configuration. For Secure Configuration, this needs to power up to 3.7 V for no longer than 1 minute (on VCCPD[8] only). TDO buffer is powered by VCCIO, not VCCPD. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
GND	Ground	Device ground pins.	All GND pins should be connected to the board GND plane.
VREFB[1..4,7,8]N[4..0]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for that bank. All of the VREF pins within a bank are shorted together.	If VREF pins are not used, you should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p, and PLL5_FBn/OUT2n.	This pin should be connected to the voltage level of the target device that PLL5 in bank 9 is driving. Refer to the data sheet for the absolute maximum voltage rating on this pin. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p, and PLL6_FBn/OUT2n.	This pin should be connected to the voltage level of the target device that PLL6 in bank 10 is driving. Refer to the data sheet for the absolute maximum voltage rating on this pin. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
VCC_PLL11_OUT (Note 6)	Power	External clock output VCCIO power for PLL11 clock outputs PLL11_OUT[1..0]p, PLL11_OUT[1..0]n, PLL11_FBp/OUT2p, and PLL11_FBn/OUT2n.	This pin should be connected to the voltage level of the target device that PLL11 in bank 11 is driving. Refer to the data sheet for the absolute maximum voltage rating on this pin. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.

Pin Name	Pin Type (1st, 2nd, 3rd Function)	Pin Description	Connection Guidelines
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VCC_PLL12_OUT (Note 6)	Power	External clock output VCCIO power for PLL12 clock outputs PLL12_OUT[1..0]p, PLL12_OUT[1..0]n, PLL12_FBp/OUT2p, and PLL12_FBn/OUT2n.	This pin should be connected to the voltage level of the target device that PLL12 in bank 12 is driving. Refer to the data sheet for the absolute maximum voltage rating on this pin. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
VCCA_PLL[1,2,5..8,11,12] (Note 4)	Power	1.2-V analog power for PLLs[1,2,5..8,11,12].	You are required to connect these pins to 1.2 V, even if the PLL is not used. Use an isolated linear supply. Power on the PLLs operating at the same frequency should be decoupled. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
VCCD_PLL[1,2,5..8,11,12] (Note 4)	Power	1.2-V digital power for PLLs[1,2,5..8,11,12].	You are required to connect these pins to 1.2 V, even if the PLL is not used. Power on the PLLs operating at the same frequency should be decoupled. Decoupling depends on the design decoupling requirements of the specific board. See Note 8.
GNDA_PLL[1,2,5..8,11,12] (Note 4)	Ground	Analog ground for PLLs[1,2,5..8,11,12].	You should connect these pins to an isolated analog ground plane on the board.
NC	No Connect	No Connect	Generally, do not drive signals into these pins. In some cases, NC pins need to be connected to VCCINT or GND for successful device migration. For more information, refer to http://www.altera.com/support/kdb/solutions/rd03132006_933.html
RUP4	I/O, Input	Reference pin for calibrated OCT for banks 3 and 4 when those I/O banks have the same VCCIO level. If I/O banks 3 and 4 have different VCCIO levels, only bank 4 can use calibrated OCT. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.	When using calibrated OCT, connect RUP to VCCIO4 via a 25-Ω or 50-Ω precision resistor. If it is not used for calibrated OCT or as an I/O pin, Altera recommends that the pin be connected to VCCIO4.
RDN4	I/O, Input	Reference pin for calibrated OCT for banks 3 and 4 when those I/O banks have the same VCCIO level. If I/O banks 3 and 4 have different VCCIO levels, only bank 4 can use calibrated OCT. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.	When using calibrated OCT, connect RDN to GND via a 25-Ω or 50-Ω precision resistor. If this pin is not used for calibrated OCT or as an I/O pin, Altera recommends that the pin be connected to GND.
RUP7	I/O, Input	Reference pin for calibrated OCT for banks 7 and 8 when those I/O banks have the same VCCIO level. If I/O banks 7 and 8 have different VCCIO levels, only bank 7 can use calibrated OCT. The external precision resistor Rup must be connected to the designated RUP pin within bank 7. If not required, this pin is a regular I/O pin.	When using calibrated OCT, connect RUP to VCCIO7 via a 25-Ω or 50-Ω precision resistor. If it is not used for calibrated OCT or as an I/O pin, Altera recommends that the pin be connected to VCCIO7.

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RDN7	I/O, Input	Reference pin for calibrated OCT for banks 7 and 8 when those I/O banks have the same VCCIO level. If I/O banks 7 and 8 have different VCCIO levels, only bank 7 can use calibrated OCT. The external precision resistor Rdn must be connected to the designated RDN pin within bank 7. If not required, this pin is a regular I/O pin.	When using calibrated OCT, connect RDN to GND via a 25-Ω or 50-Ω precision resistor. If this pin is not used for calibrated OCT or as an I/O pin, Altera recommends that the pin be connected to GND.
		Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO, ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns it on.	The nIO-PULLUP can be tied directly to VCCPD, use a 1-kΩ pull-up resistor, or tied directly to GND, depending on how the device is used. Refer to the Description column.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input), DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory.	The VCCSEL input buffer is powered by VCCPD and must be hardwired to VCCPD in order to enable the 1.8-V/1.5-V input buffers for configuration. VCCSEL tied to GND will enable a 3.3-V/2.5-V POR trip point, which may be above 1.8 V. Refer to the Description column.
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the Stratix II GX device.	If the temperature-sensing diode is not used, connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the Stratix II GX device.	If the temperature-sensing diode is not used, connect this pin to GND.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Stratix II GX device. In AS mode, DCLK is an output from the Stratix II GX device that provides timing for the configuration interface.	In PPA mode, DCLK should be tied to VCC to prevent this pin from floating.
MSEL[3..0]	Input	Configuration input pins that set the Stratix II GX device configuration scheme.	These pins are internally connected through a 5-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused, connect them to GND. Depending on the configuration scheme used, these pins should be tied directly to VCCPD or GND. Refer to the *Configuring Stratix II and Stratix II GX Devices* chapter in volume 1 of the *Configuration Handbook*. If only JTAG configuration is used, connect these pins to ground.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single-device configuration and JTAG programming, nCE should be connected to GND.

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Pin Name	**Pin Type (1st, 2nd, 3rd Function)**	**Pin Description**	**Connection Guidelines**
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the nINIT_CONF pin of the configuration device. If this pin is not used, it requires a connection directly or through a resistor to VCCPD.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration Done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	Pull high to VCCIO via an external 10-kΩ resistor, unless internal pull-up resistors on the enhanced configuration device are used. When using EPC2 devices, external 10-kΩ pull-up resistors must be used.
nCEO	Output	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds the nCE pin of a subsequent device. During single-device configuration, this pin is left floating. For recommendations on how to connect nCEO in a chain with multiple voltages across the devices in the chain, refer to the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.	Pull high to VCCIO via a 10-kΩ resistor, unless internal pull-up resistors on the enhanced configuration device are used. When using EPC2 devices, external 10-kΩ pull-up resistors must be used.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5-V, 1.8-V, 2.5-V, 3.3-V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms.	The PORSEL pin should be tied directly to VCCPD or GND.
Optional/Dual-Purpose Configuration Pins			
nCSO	I/O, Output	Output control signal from the Stratix II GX FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode, nCSO is not used. Also, when this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
ASDO	I/O, Output	Control signal from the Stratix II GX FPGA to the serial configuration device in AS mode used to read out configuration data.	When not programming the device in AS mode, ASDO is not used. Also, when this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	When the dedicated output for CRC_ERROR is not used and this pin is not used as an I/O, Altera recommends that you leave the pin unconnected.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.	When the dedicated input DEV_CLR is not used and this pin is not used as an I/O, Altera recommends that you tie this pin to VCCPD or ground.

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Pin Name	Pin Type (1st, 2nd, 3rd Function)	Pin Description	Connection Guidelines
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O, Altera recommends that you tie this pin to VCCPD or ground.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.	When the dedicated input for DATA0 is not used and it is not used as an I/O, Altera recommends that you leave this pin unconnected
DATA[6..1]	I/O, Input	Dual-purpose configuration input data pins. The DATA[6..1] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	When the dedicated inputs for DATA[6..1] are not used and these pins are not used as an I/O, Altera recommends that you leave these pins unconnected.
DATA7	I/O, Bidirectional	In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the nRS signal has been strobed low.	When the dedicated input for DATA7 is not used and it is not used as an I/O, Altera recommends that you leave this pin unconnected
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	Connect this pin to a 10-kΩ resistor to VCCIO3.
nCS, CS	I/O, Input	These are chip-select inputs that enable the Stratix II GX device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active-high enable, use the CS pin and drive the nCS pin low. If a design requires an active-low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.	When the dedicated inputs for nCS, CS are not used and these pins are not used as an I/O, Altera recommends that you leave these pins unconnected.
nRS	I/O, Input	Read strobe input pin. A low input directs the device to drive the RDYnBSY signal on the DATA7 pin. In non-PPA schemes, it functions as a user I/O during configuration, which means it is tri-stated. This pin can be used as a user I/O pin after configuration.	If the nRS pin is not used in PPA mode, it should be tied to VCCIO8.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.	If the device is not being programmed in PPA mode and the pin is not being used, Altera recommends that you connect the nWS pin to the power bank this pin resides in.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O, Altera recommends that you connect this pin to ground.

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Pin Name	Pin Type (1st, 2nd, 3rd Function)	Pin Description	Connection Guidelines
RDYnBSY	I/O, Output	Ready, not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.	If the device is not being programmed in PPA mode and the pin is not being used as an I/O, Altera recommends that you leave the RDYnBSY pin unconnected.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the memory (either flash or enhanced configuration device) when using a remote system update mode. When not using remote update or local update configuration modes, these pins are user I/O pins.	If the PGM[2..0] pins are not used as page select output and these pins are not used as I/O, Altera recommends that you leave these pins unconnected.
RUnLU	I/O, Input	Input that selects between remote update and local update. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects remote update and a logic low selects local update. When not using remote update or local update configuration mode, this pin is available as general-purpose user I/O pin.	If the RUnLU pin is not used as a local or remote configuration input and the pin is not used as an I/O, Altera recommends that you leave this pin unconnected.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.	Connect TCK to the correct JTAG interface signal. To disable JTAG circuitry, connect TCK to GND via a 1-kΩ resistor.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.	Connect TMS to the correct JTAG interface signal. To disable JTAG circuitry, connect TMS to VCCPD via a 10-kΩ resistor.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.	Connect TDI to the correct JTAG interface signal. To disable JTAG circuitry, connect TDI to VCCPD via a 10-kΩ resistor.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.	Connect TDO to the correct JTAG interface signal. To disable JTAG circuitry, leave TDO unconnected.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Connect TRST to VCCPD if JTAG circuitry is used. To disable JTAG circuitry, connect TRST to GND.
Clock and PLL Pins			
CLK[1,3]p	Clock, Input	Dedicated clock input pins 1 and 3 that can also be used for data inputs. These clock pins do not support differential OCT.	Connect unused pins to the VCCIO of the bank which the pin resides in.
CLK[1,3]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. These clock pins do not support differential OCT.	Connect unused pins to GND.
CLK[2,0]p/DIFFIO_RX_C[1,0]p (Note 5)	I/O, Clock	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels. These clock pins support differential OCT.	Connect unused pins to GND.
CLK[2,0]n/DIFFIO_RX_C[1,0]n (Note 5)	I/O, Clock	These pins can be used as I/O pins, the negative clock input pins for differential clock input, or the negative data pins of differential receiver channels.	Connect unused pins to GND.
CLK[4-7,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. These clock pins do not support differential OCT.	Connect unused pins to GND.
CLK[4-7,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. These clock pins do not support differential OCT.	Connect unused pins to GND.

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Pin Name	Pin Type (1st, 2nd, 3rd Function)	Pin Description	Connection Guidelines
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs.	If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs, including the counters, to their default state. If VCCSEL = 0, you must drive the PLL_ENA with a 3.3-V/2.5-V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8 V or 1.5 V to enable the PLLs.
FPLL[8..7]CLKp (Note 6)	Clock, Input	Dedicated positive clock inputs for fast PLLs (PLLs 7 and 8), which can also be used for data inputs. These pins do not support differential OCT.	Connect unused pins to the VCCIO which the pin resides in.
FPLL[8..7]CLKn (Note 6)	Clock, Input	Dedicated negative clock inputs associated with the FPLL[7,8]CLKp pins, which can also be used for data inputs. These pins do not support differential OCT.	Connect unused pins to GND.
PLL5_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL5. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL5).	When these pins are not used, they may be left floating.
PLL5_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL5. If the clock outputs are single-ended, each pair of pins (i.e. PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in-phase or 180° out-of-phase.	When these pins are not used, they may be left floating.
PLL6_OUT[1,0]p	Output	Optional positive external clock outputs [1,0] from enhanced PLL6. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL6).	When these pins are not used, they may be left floating.
PLL6_OUT[1,0]n	Output	Optional negative external clock outputs [1,0] from enhanced PLL6. If the clock outputs are single-ended, each pair of pins (i.e. PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180° out of phase.	When these pins are not used, they may be left floating.
PLL11_OUT[1,0]p (Note 4, 6)	Output	Optional positive external clock outputs [1,0] from enhanced PLL11. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL11).	When these pins are not used, they may be left floating.
PLL11_OUT[1,0]n (Note 4, 6)	Output	Optional negative external clock outputs [1,0] from enhanced PLL11. If the clock outputs are single-ended, each pair of pins (i.e. PLL11_OUT0p and PLL11_OUT0n are considered one pair) can be either in phase or 180° out of phase.	When these pins are not used, they may be left floating.
PLL12_OUT[1,0]p (Note 4, 6)	Output	Optional positive external clock outputs [1,0] from enhanced PLL12. These pins can be differential (two output pin pairs) or single-ended (four clock outputs from PLL12).	When these pins are not used, they may be left floating.
PLL12_OUT[1,0]n (Note 4, 6)	Output	Optional negative external clock outputs [1,0] from enhanced PLL12. If the clock outputs are single-ended, each pair of pins (i.e. PLL12_OUT0p and PLL12_OUT0n are considered one pair) can be either in phase or 180° out of phase.	When these pins are not used, they may be left floating.
PLL[6..5]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins, or external clock outputs for PLL[6,5]. These pins do not support differential OCT.	Connect unused pins to GND.

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PLL[6..5]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[6,5]_FBp, or negative terminal clock output pins for differential clock output. These pins do not support differential OCT.	Connect unused pins to GND.
PLL[12..11]_FBp/OUT2p (Note 4, 6)	I/O, Input, Output	These pins can be used as I/O pins, positive external feedback input pins, or positive external clock outputs for PLL[12..11]. These pins do not support differential OCT.	Connect unused pins to GND.
PLL[12..11]_FBn/OUT2n (Note 4, 6)	I/O, Input, Output	These pins can be used as I/O pins, negative external feedback input PLL[12..11]_FBp, or negative external clock output pins for differential clock output. These pins do not support differential OCT.	Connect unused pins to GND.
Dual-Purpose Differential and External Memory Interface Pins			
DIFFIO_RX[76..1]p (Note 5)	I/O, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these IO pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND.
DIFFIO_RX[76..1]n (Note 5)	I/O, Input	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these IO pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND.
DIFFIO_TX[77..0]p (Note 5)	I/O, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these IO pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND.
DIFFIO_TX[77..0]n (Note 5)	I/O, Output	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS-compatible signals. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these IO pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND.
DQS[17..0][T,B] (Note 7)	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	When these IO pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND.
DQSn[17..0][T,B]	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry.	When these IO pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND.

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Pin Name	Pin Type (1st, 2nd, 3rd Function)	Pin Description	Connection Guidelines
DQ[17..0][T,B][3..0] (Note 7)	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	When these IO pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND.
DQVLD[8..0][T,B]	DQVLD	Optional data valid signal for use in external memory interfacing.	When these IO pins are not used, they can be tied to the VCCIO of the bank that they reside in or GND.
Transceiver (I/O Banks) Pins			
VCCP	Power	GX bank [17..13] PCS power. This power is connected to 1.2 V.	Connect VCCP to an isolated 1.2-V linear regulator. These pins need to be isolated from noisy digital voltage planes. Decoupling depends on the design decoupling requirements of the specific board design. See Note 8.
VCCR	Power	GX bank [17..13] receiver analog power. This power is connected to 1.2 V.	Connect VCCR to a 1.2-V linear regulator. These pins may be tied to the same 1.2-V plane as VCCT_B[] and/or VCCL_B[]. However, for the best jitter performance at high data rates, this plane should be isolated from all other power supplies. Decoupling depends on the design decoupling requirements of the specific board design. See Note 8.
VCCT_B[17..13] (Note 3)	Power	GX bank [17..13] transmitter analog power. This power is connected to 1.2 V.	Connect VCCT_B[] to a 1.2-V linear regulator. These pins may be tied to the same 1.2-V plane as VCCR and/or VCCL_B[]. However, for the best jitter performance at high data rates, this plane should be isolated from all other power supplies. Decoupling depends on the design decoupling requirements of the specific board design. See Note 8.
VCCA	Power	GX bank [17..13] analog power. This power is connected to 3.3 V.	Connect VCCA to a 3.3-V linear regulator. Decoupling depends on the design decoupling requirements of the specific board design. See Note 8.
VCCH_B[17..13] (Note 3)	Power	GX bank [17..13] Transmitter driver analog power. This power is connected to 1.2 V or 1.5 V. Supply 1.2 V for 3.125 Gbps max data rate, and for lower power. Supply 1.5 V for higher data rates in single or double width modes.	Connect VCCH_B[] to a 1.2-V or 1.5-V linear regulator. Decoupling depends on the design decoupling requirements of the specific board design. See Note 8.
VCCL_B[17..13] (Note 3)	Power	GX bank [17..13] VCO analog power and general transceiver clock circuitry. This power is connected to 1.2 V.	Connect VCCL_B[] to a 1.2-V linear regulator. These pins may be tied to the same 1.2-V plane as VCCT_B[] and/or VCCR. However, for the best jitter performance at high data rates, this plane should be isolated from all other power supplies. Decoupling depends on the design decoupling requirements of the specific board design. See Note 8.

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Pin Name	Pin Type (1st, 2nd, 3rd Function)	Pin Description	Connection Guidelines
GXB_RX[19..0]p (Note 2)	I, Input	High speed positive differential receiver channels.	These pins may be AC-coupled or DC-coupled when used (see Note 9 and Note 10). Connect all unused GXB_RXp pins to the VCCR 1.2-V plane either individually through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible.
GXB_RX[19..0]n (Note 2)	I, Input	High speed negative differential receiver channels.	These pins may be AC-coupled or DC-coupled when used (see Note 9 and Note 10). Connect all unused GXB_RXn pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible.
GXB_TX[19..0]p (Note 2)	O, Output	High speed positive differential transmitter channel.	Connect all unused GXB_TXp pins to the VCCT_B[] or VCCR (if tied together w/ VCCT_B[]) 1.2-V plane either individually through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible.
GXB_TX[19..0]n (Note 2)	O, Output	High speed negative differential transmitter channels.	Connect all unused GXB_TXn pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible.
REFCLK[0,1]_B[17..13]p (Note 3)	I, Input	High speed differential I/O reference clock positive.	These pins should be AC-coupled when used (see Note 11). Connect all unused REFCLK[0,1]_B[]p pins to the VCCT_B[] or VCCR (if tied together w/ VCCT_B[]) 1.2-V plane either individually through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible.
REFCLK[0,1]_B[17..13]n (Note 3)	I, Input	High speed differential I/O reference clock negative.	These pins should be AC-coupled when used (see Note 11). Connect all unused REFCLK[0,1]_B[]n pins either individually to GND through a 10-kΩ resistor or tie all unused pins together through a single 10-kΩ resistor. Ensure that the trace from the pins to the resistor(s) is as short as possible.
RREFB[17..13] (Note 3)	I, Input	Reference resistor for GX side banks.	These pins should be connected to a 2-kΩ ±1% resistor to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Notes:
(1) These pin connection guidelines are created based on the largest Stratix II GX device, EP2SGX130GF1508.

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Pin Name	Pin Type (1st, 2nd, 3rd Function)	Pin Description	Connection Guidelines

(2) Transceiver signals GXB_RX[19..0] and GXB_TX[19..0] are device-specific.
   EP2SGX30C and EP2SGX60C each contains 4 transceivers: GXB_RX[3..0] and GXB_TX[3..0].
   EP2SGX30D and EP2SGX60D each contains 8 transceivers: GXB_RX[7..0] and GXB_TX[7..0].
   EP2SGX60E and EP2SGX90E each contains 12 transceivers: GXB_RX[11..0] and GXB_TX[11..0].
   EP2SGX90F contains 16 transceivers: GXB_RX[15..0] and GXB_TX[15..0].
   EP2SGX130G contains 20 transceivers: GXB_RX[19..0] and GXB_TX[19..0].

(3) Pins VCCT_B[17..13], VCCH_B[17..13], REFCLK[0,1]_B[17..13], RREFB[17..13], and VCCL_B[17..13] refer to the bank number of the transceiver.
   EP2SGX30C and EP2SGX60C each consists of 4 transceivers in Bank 13.
   EP2SGX30D and EP2SGX60D each consists of 8 transceivers in Banks 13 and 14.
   EP2SGX60E and EP2SGX90E each consists of 12 transceivers in Banks 13, 14, and 15.
   EP2SGX90F consists of 16 transceivers in Banks 13, 14, 15, and 16.
   EP2SGX130G consists of 20 transceivers in Banks 13, 14, 15, 16, and 17.

(4) EP2SGX30 and EP2SGX60C/D only have PLL(1, 2, 5 and 6). EP2SGX60E, EP2SGX90 and EP2SGX130 have PLL(1,2, 5, 6, 7, 8, 11, and 12).

(5) The differential TX/RX count for each device and package is different.
   EP2SGX30, EP2SGX60C and EP2SGX60D each consists of 29 transmit and 29 receive differential I/O pins.
   EP2SGX60E consists of 42 transmit and 40 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
   EP2SGX90E consists of 45 transmit and 45 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
   EP2SGX90F consists of 59 transmit and 57 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]).
   EP2SGX130G consists of 71 transmit and 71 receive differential I/O, and 2 clock/receive differential I/O pins, (CLK[2,0]/DIFFIO_RX_C[1,0]). The transmit bus numbers 15-17, and 64-68 are not used. Also, the receive bus numbers 15-17, 64 and 65 are not unused.

(6) EP2SGX30 does not have the following signals: FPLL[8..7]CLK, PLL11_OUT[1,0], PLL12_OUT[1,0], PLL[12..11]_FBp/OUT2, VCC_PLL11_OUT, and VCC_PLL12_OUT.
   EP2SGX60C/D does not have the following signals: FPLL[8..7]CLK, PLL11_OUT[1]p/n, PLL11_OUT[0]p, PLL12_OUT[1]p/n, PLL12_OUT[0]n, PLL[11]_FBp/OUT2p/n,
   PLL[12]_FBp/OUT2p, VCC_PLL11_OUT, and VCC_PLL12_OUT.
   The EP2SGX60CF780 and EP2SGX60DF780 only have 4 PLLs.
   Although the following pin names use PLL labels, they are only I/O pins and should not be construed as PLL pins.
   For these devices, only the power source is as indicated below.
   a. PLL11_OUTn (C17 in the GX60F780) - uses Bank 3 power supply, VCCIO3.
   b. PLL12_FBn/OUT2n (AE16 in the GX60F780) - uses Bank 8 power supply, VCCIO8.
   c. PLL12_OUT0p (AF16 in the GX60F780) - uses Bank 8 power supply, VCCIO8.

(7) EP2SGX30C, EP2SGX30D, EP2SGX60C, and EP2SGX60D support either (18, x4), (8, x8/x9), or (4, x16/x18) DQ and DQS bus modes.
   EP2SGX60E, EP2SGX90D, EP2SGX90F, and EP2SGX130G support either (36, x4), (18, x8/x9), or (8, x16/x18) DQ and DQS bus modes.

(8) Capacitance values for the power supply should be selected after considering the amount of power they need to supply over the frequency of operation of the particular circuit
   being decoupled. The target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device/supply. The power
   plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series
   Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency
   decoupling.

(9) Refer to the *DC Coupling* section of the Stratix II GX Transceiver Architecture Overview chapter in volume 2 of the Stratix II GX Device Handbook.

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(10) For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.

(11) In PCI Express configuration, DC-coupling is allowed on REFCLK if the selected REFCLK I/O standard is HCSL (High-Speed Current Steering Logic).

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Revision History		
Rev	**Description of Changes**	**Date**
3.0	Initial release.	6/29/2007
3.1	Updated RX and TX coupling information in lines 96 - 99. Updated lines 6-7, 18-22, 30, 32, 34, 53-56, 59-61, 63-64, 66-67, 76-79. Added Note 9.	11/6/2007