



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					G4				
GXB_L1		REFCLK1Lp					F5				
XB_L1		GXB_TX_L4n					E1				
XB_L1		GXB_TX_L4p					E2				
XB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
XB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
XB_L1		GXB_TX_L3n					J1				
XB_L1		GXB_TX_L3p					J2				
XB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2				
XB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1				
XB_L0		GXB_TX_L2n					N1				
XB_L0		GXB_TX_L2p					N2				
XB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2				
XB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1				
XB_L0		GXB_TX_L1n					U1				
XB_L0		GXB_TX_L1p					U2				
XB_L0		GXB_RX_L1p,GXB_REFCLK_L1p GXB_RX_L1n,GXB_REFCLK_L1n					W2 W1				
XB_L0											
XB_L0		GXB_TX_L0n					Y3				
XB_L0	 	GXB_TX_L0p		1		1	Y4 AA2			 	+
XB_L0	-	GXB_RX_L0p,GXB_REFCLK_L0p GXB_RX_L0n,GXB_REFCLK_L0n	 	-						 	+
XB_L0	 			1		1	AA1			 	+
XB_L0	 	REFCLK0Lp		1		1	V4			 	+
XB_L0	 	REFCLK0Ln		TDO		1	U4			 	+
A A	 	TDO nCSO		TDO		1	V3 AB6			 	+
				DATA4			R4				
A		TMS		TMS							
A A		AS_DATA3		DATA3			AA5				
		TCK		TCK			V5				
A		AS_DATA2		DATA2			T5				
A		TDI		TDI			P5				
A		AS_DATA1		DATA1			W5				
A		DCLK		DCLK			M5				
A		AS_DATA0,ASDO		DATA0			AB4				
A	TITLE DOTTING	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B			
A	VREFB3AN0	10		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7	2012			
A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N6	DQ1B			
A		IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B			
A	TITLE DOTTING	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M6	DQSn1B			
A		IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B			
A		IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	M7	DQS1B			
A	TITLE DOTTING	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	R6	2012			-
A	TITLE DOTTE	10		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R7	DQ1B			
A		10		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	L7	DQ1B			
A		IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T7	DQ1B			
A	TITLE DOTTING	10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	L8	DQ1B			
A		IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8				
Α		10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B	1	ļ	+
Α	TITLE DOTTING	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9	2012	1	ļ	+
Α	TITLE DOTTE	10	İ	1	DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B	1	GND	CNID
В					DIEELO EV SSS	DIFFOLIT DOO-			1		GND
		10			DIFFIO_TX_B33n	DIFFOUT_B33n	V8	DOED.			
В	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	N8	DQ5B		B_A_15	
B B	VREFB3BN0 VREFB3BN0	IO IO			DIFFIO_RX_B34n DIFFIO_TX_B33p	DIFFOUT_B34n DIFFOUT_B33p	N8 W8	DQ5B		B_A_15 B_WE#	
B B	VREFB3BN0 VREFB3BN0 VREFB3BN0	10 10 10			DIFFIO_RX_B34n DIFFIO_TX_B33p DIFFIO_RX_B34p	DIFFOUT_B34n DIFFOUT_B33p DIFFOUT_B34p	N8 W8 M8	DQ5B DQ5B		B_A_15 B_WE# B_A_14	D 00# :
B B B	VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0	10 10 10 10			DIFFIO_RX_B34n DIFFIO_TX_B33p DIFFIO_RX_B34p DIFFIO_RX_B35n	DIFFOUT_B34n DIFFOUT_B33p DIFFOUT_B34p DIFFOUT_B35n	N8 W8 M8 N9	DQ5B DQ5B DQSn5B		B_A_15 B_WE# B_A_14 B_CS#_1	B_CS#_1
B B B B	VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0	10 10 10 10			DIFFIO_RX_B34n DIFFIO_TX_B33p DIFFIO_RX_B34p DIFFIO_RX_B35n DIFFIO_TX_B36n	DIFFOUT_B34n DIFFOUT_B33p DIFFOUT_B34p DIFFOUT_B35n DIFFOUT_B36n	N8 W8 M8 N9 AA7	DQ5B DQ5B DQSn5B DQ5B		B_A_15 B_WE# B_A_14 B_CS#_1 B_A_13	
3 3 3 3 3	VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0	10 10 10 10 10 10			DIFFIO RX B34n DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B35n DIFFIO TX B36n DIFFIO RX B35p	DIFFOUT B34n DIFFOUT B339 DIFFOUT B34p DIFFOUT B35n DIFFOUT B36n DIFFOUT B35p	N8 W8 M8 N9 AA7 N10	DQ5B DQ5B DQSn5B		B A 15 B WE# B A 14 B CS# 1 B A 13 B CS# 0	B_CS#_1 B_CS#_0
B B B B B B B	VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0	IO IO IO IO IO IO			DIFFIO RX B34n DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B35n DIFFIO TX B36n DIFFIO RX B35p DIFFIO_TX_B36p	DIFFOUT_B33p DIFFOUT_B33p DIFFOUT_B34p DIFFOUT_B35n DIFFOUT_B36n DIFFOUT_B36n DIFFOUT_B35p DIFFOUT_B36p	N8 W8 M8 N9 AA7 N10 AB7	DQ5B DQ5B DQSn5B DQ5B DQS5B		B_A_15 B_WE# B_A_14 B_CS#_1 B_CS#_0 B_A_12	
3 3 3 3 3 3 3 3	VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0	10 10 10 10 10 10 10			DIFFIO_RX_B34n DIFFIO_TX_B33p DIFFIO_RX_B34p DIFFIO_RX_B35n DIFFIO_TX_B36n DIFFIO_RX_B35p DIFFIO_TX_B36p DIFFIO_TX_B36p DIFFIO_TX_B36p	DIFFOUT_B34n DIFFOUT_B33p DIFFOUT_B35p DIFFOUT_B35n DIFFOUT_B36n DIFFOUT_B35p DIFFOUT_B35p DIFFOUT_B35p DIFFOUT_B37n	N8 W8 M8 N9 AA7 N10 AB7 Y7	DQ5B DQ5B DQSn5B DQ5B DQ5B DQ5B		B A 15 B WE# B A 14 B CS# 1 B A 13 B A 13 B CS# 0 B A 12 B A 11	B_CS#_0
B B B B B B B B B B B B B B B B B B B	VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0	10 10 10 10 10 10 10 10 10			DIFFIO_RX_B34n DIFFIO_TX_B33p DIFFIO_RX_B34p DIFFIO_RX_B35n DIFFIO_TX_B36n DIFFIO_TX_B36p DIFFIO_TX_B36p DIFFIO_TX_B37n DIFFIO_TX_B38n	DIFFOUT B34n DIFFOUT B33p DIFFOUT B34p DIFFOUT B35n DIFFOUT B35n DIFFOUT B35n DIFFOUT B36p DIFFOUT B36p DIFFOUT B37n DIFFOUT B38n	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8	DQ5B DQ5B DQSn5B DQ5B DQS5B DQ5B DQ5B DQ5B		B_A_15 B_WE# B_A_14 B_CS#_1 B_CS#_0 B_A_12 B_A_11 B_A_9	
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0 VREFB3BN0	IO I			DIFFIO RX B34n DIFFIO TX B33p DIFFIO RX B35n DIFFIO RX B35n DIFFIO TX B36n DIFFIO TX B36n DIFFIO TX B36p DIFFIO TX B37n DIFFIO RX B38n DIFFIO TX B38n DIFFIO TX B38n	DIFFOUT B34n DIFFOUT B33p DIFFOUT B34p DIFFOUT B35n DIFFOUT B36n DIFFOUT B36n DIFFOUT B36p DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8	DQ5B DQ5B DQ5nB DQ5nB DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		B_A_15 B_WE# B_A_14 B_CS#_1 B_A_13 B_CS#_0 B_A_12 B_A_11 B_A_9 B_A_10	B_CS#_0 B_CA_9
B B B B B B B B B B B B B B B B B B B	VREFB3BNO	IO I			DIFFIO RX B34n DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B35n DIFFIO TX B36n DIFFIO TX B36n DIFFIO TX B36n DIFFIO TX B37n DIFFIO RX B38n DIFFIO RX B38n DIFFIO TX B37n DIFFIO TX B37p DIFFIO RX B38p	DIFFOUT B34n DIFFOUT B33p DIFFOUT B33p DIFFOUT B35n DIFFOUT B35n DIFFOUT B36n DIFFOUT B36p DIFFOUT B37n DIFFOUT B37n DIFFOUT B38n	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8 W7	DQ5B DQ5B DQSn5B DQ5B DQS5B DQ5B DQ5B DQ5B		B_A_15 B_WE# B_A_14 B_CS#_1 B_CS#_0 B_A_12 B_A_11 B_A_9	B_CS#_0
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3BNO	10 10 10 10 10 10 10 10 10 10 10	CLKOn,FPLL_BL_FBn		DIFFIO RX B34n DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B35n DIFFIO RX B35n DIFFIO TX B36n DIFFIO TX B36n DIFFIO TX B36n DIFFIO TX B36n DIFFIO TX B37n DIFFIO TX B37n DIFFIO TX B37n DIFFIO TX B37n DIFFIO RX B38n DIFFIO RX B38p DIFFIO RX B38p	DIFFOUT B34n DIFFOUT B33p DIFFOUT B33p DIFFOUT B35n DIFFOUT B35n DIFFOUT B35n DIFFOUT B36p DIFFOUT B37n DIFFOUT B37n DIFFOUT B37p	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8 W7 V9	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		B A 15 B WE# B A 14 B CS# 1 B A 13 B CS# 0 B A 13 B A 13 B A 12 B A 11 B A 9 B A 9 B A 9	B_CS#_0 B_CA_9
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO VREFB3BNO	IO I			DIFFIO RX B34n DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B35n DIFFIO TX B36n DIFFIO TX B36n DIFFIO TX B36p DIFFIO TX B37n DIFFIO TX B37n DIFFIO TX B37n DIFFIO TX B37n DIFFIO RX B38n DIFFIO RX B38p DIFFIO RX B38p DIFFIO RX B38p DIFFIO RX B38p	DIFFOUT B34n DIFFOUT B33p DIFFOUT B33p DIFFOUT B34p DIFFOUT B35n DIFFOUT B36n DIFFOUT B36n DIFFOUT B36p DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n DIFFOUT B38n DIFFOUT B38p DIFFOUT B38p DIFFOUT B38p DIFFOUT B38p DIFFOUT B38p	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8 W7 V9 R9 AB8	DQ5B DQ5B DQ5nB DQ5nB DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		B_A_15 B_WE# B_A_14 B_CS#_1 B_A_13 B_CS#_0 B_A_12 B_A_11 B_A_9 B_A_10	B_CS#_0 B_CA_9
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3BNO	10	CLK0p,FPLL_BL_FBn CLK0p,FPLL_BL_FBp		DIFFIO RX B34h DIFFIO TX B33p DIFFIO TX B34p DIFFIO RX B34p DIFFIO RX B35n DIFFIO TX B36n DIFFIO TX B36p DIFFIO TX B36p DIFFIO TX B36p DIFFIO TX B37n	DIFFOUT B34n DIFFOUT B33p DIFFOUT B33p DIFFOUT B35n DIFFOUT B35n DIFFOUT B35n DIFFOUT B35n DIFFOUT B36p DIFFOUT B37n DIFFOUT B38n DIFFOUT B37n DIFFOUT B38n DIFFOUT B38n DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8 W7 V9 R9 AB8	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		B A 15 B WE# B A 14 B CS# 1 B A 13 B A 13 B A 12 B A 12 B A 11 B A 9 B A 11 B A 8 B A 8	B_CS#_0 B_CA_9
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3BNO	IO I			DIFFIO RX B34n DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B35n DIFFIO RX B35n DIFFIO TX B36n DIFFIO TX B35n DIFFIO TX B37n DIFFIO TX B40n DIFFIO TX B40n DIFFIO TX B40p	DIFFOUT B34n DIFFOUT B33p DIFFOUT B33p DIFFOUT B35p DIFFOUT B35n DIFFOUT B35n DIFFOUT B36p DIFFOUT B37n DIFFOUT B38n DIFFOUT B37p DIFFOUT B38p DIFFOUT B38p DIFFOUT B39p DIFFOUT B39p DIFFOUT B39n DIFFOUT B40n DIFFOUT B40p	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8 W7 V9 R9 AB8 P9	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		B A 15 B WE# B A 14 B CS# 1 B A 13 B CS# 0 B A 12 B A 11 B A 12 B A 11 B A 9 B A 9 B A 10 B A 8 B A 8 B A 8	B_CS#_0 B_CA_9 B_CA_8
B B B B B B B B B B B B B B B B B B B	VREFB3BNO	IO I			DIFFIO RX B34h DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B34p DIFFIO RX B35p DIFFIO TX B36p DIFFIO TX B36p DIFFIO TX B36p DIFFIO TX B37p DIFFIO RX B38p DIFFIO RX B38p DIFFIO RX B38p DIFFIO RX B39p DIFFIO RX B39p DIFFIO RX B39p DIFFIO RX B39p DIFFIO TX B40p DIFFIO TX B40p DIFFIO TX B40p	DIFFOUT B34n DIFFOUT B33p DIFFOUT B33p DIFFOUT B35n DIFFOUT B36n DIFFOUT B36n DIFFOUT B36p DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n DIFFOUT B38n DIFFOUT B38n DIFFOUT B38n DIFFOUT B39n DIFFOUT B39n DIFFOUT B39n DIFFOUT B39n DIFFOUT B40n DIFFOUT B40n DIFFOUT B40n DIFFOUT B40n DIFFOUT B40n DIFFOUT B40n	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8 W7 V9 R9 AB8 P9 AA8 Y10	DQ5B DQ5B DQ5AB DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5		B_A 15 B_WE# B_A.14 B_CS#,1 B_A.13 B_A.12 B_A.12 B_A.12 B_A.10 B_A.8 B_A.8 B_RAS# B_RAS#	B_CS#_0 B_CA_9
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3BNO	10 10 10 10 10 10 10 10 10 10 10 10 10 1			DIFFIO RX B34h DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B35h DIFFIO TX B36h DIFFIO TX B36h DIFFIO TX B36p DIFFIO TX B36p DIFFIO TX B37h DIFFIO TX B39h DIFFIO TX B40h DIFFIO TX B40h DIFFIO TX B40h DIFFIO TX B49h	DIFFOUT B34n DIFFOUT B33p DIFFOUT B33p DIFFOUT B35n DIFFOUT B35n DIFFOUT B35n DIFFOUT B35n DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n DIFFOUT B37p DIFFOUT B37p DIFFOUT B39n DIFFOUT B39n DIFFOUT B39n DIFFOUT B39n DIFFOUT B39n	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8 W7 V9 R89 AA8 P9 AA8 Y10 AA9	DQSB DQSB DQSnSB DQSSB DQSSB DQSSB DQSB DQSB DQSB DQSB		B A 15 B WE# B A 14 B CS# 1 B A 13 B CS# 0 B A 13 B A 13 B A 12 B A 11 B A 9 B A 11 B A 9 B A 10 B A 8 B A 8	B_CS#_0 B_CA_9 B_CA_8
3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3 3	VREFB3BNO	IO I			DIFFIO RX B34h DIFFIO TX B33p DIFFIO RX B34p DIFFIO RX B34p DIFFIO RX B35p DIFFIO TX B36p DIFFIO TX B36p DIFFIO TX B36p DIFFIO TX B37p DIFFIO RX B38p DIFFIO RX B38p DIFFIO RX B38p DIFFIO RX B39p DIFFIO RX B39p DIFFIO RX B39p DIFFIO RX B39p DIFFIO TX B40p DIFFIO TX B40p DIFFIO TX B40p	DIFFOUT B34n DIFFOUT B33p DIFFOUT B33p DIFFOUT B35n DIFFOUT B36n DIFFOUT B36n DIFFOUT B36p DIFFOUT B37n DIFFOUT B37n DIFFOUT B37n DIFFOUT B38n DIFFOUT B38n DIFFOUT B38n DIFFOUT B39n DIFFOUT B39n DIFFOUT B39n DIFFOUT B39n DIFFOUT B40n DIFFOUT B40n DIFFOUT B40n DIFFOUT B40n DIFFOUT B40n DIFFOUT B40n	N8 W8 M8 N9 AA7 N10 AB7 Y7 U8 W7 V9 R9 AB8 P9 AA8 Y10	DQ5B DQ5B DQ5AB DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5		B_A 15 B_WE# B_A.14 B_CS#,1 B_A.13 B_A.12 B_A.12 B_A.12 B_A.10 B_A.8 B_A.8 B_RAS# B_RAS#	B_CS#_0 B_CA_9 B_CA_8

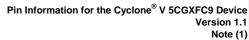


											Note (1
Bank Number		Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0				DIFFIO_TX_B44n	DIFFOUT_B44n	W11	DQ6B		B_A_7	B_CA_7
BB	VREFB3BN0				DIFFIO_RX_B43p	DIFFOUT_B43p	M10	DQS6B		B_CK	B_CK
3B	VREFB3BN0				DIFFIO_TX_B44p	DIFFOUT_B44p	Y11			B_A_6	B_CA_6
BB	TITEL BOBITO	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B45n	DIFFOUT_B45n	AB10	DQ6B		B_A_3	B_CA_3
BB		10			DIFFIO_RX_B46n	DIFFOUT_B46n	U10	DQ6B		B_A_5	B_CA_5
3B	VREFB3BN0	•	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AB11	DQ6B		B_A_2	B_CA_2
3B	TITEL BOBITO	10	0114		DIFFIO_RX_B46p	DIFFOUT_B46p	U11	DQ6B	+	B_A_4	B_CA_4
3B 3B	VREFB3BN0 VREFB3BN0	10	CLK1n		DIFFIO_RX_B47n DIFFIO_TX_B48n	DIFFOUT_B47n DIFFOUT B48n	T10 R11	DQ6B	1	B_A_1	B_CA_1
3B	VREFB3BN0		CLK1p		DIFFIO_IX_B46II	DIFFOUT_B47p	R10	DQ6B		D_A_I	B_CA_I
3B	VREFB3BN0		CERTP		DIFFIO_TX_B48p	DIFFOUT B48p	P12	DQ6B	+	B A 0	B CA 0
1A		10	RZQ_0		DIFFIO TX B49n	DIFFOUT B49n	AA13	DQ0B		B_A_0	B_CA_0
4A	VREFB4AN0		1124_0		DIFFIO RX B50n	DIFFOUT B50n	W12	DQ7B		B_DQ_0	B_DQ_0
4A	VREFB4AN0				DIFFIO_TX_B49p	DIFFOUT B49p	AB13	DQ7B		B DQ 2	B DQ 2
4A	VREFB4AN0				DIFFIO_RX_B50p	DIFFOUT_B50p	Y12	DQ7B		B_DQ_1	B DQ 1
4A	VREFB4AN0				DIFFIO RX B51n	DIFFOUT B51n	U12	DQSn7B		B DQS# 0	B DQS# 0
4A	VREFB4AN0	IO			DIFFIO TX B52n	DIFFOUT B52n	R12	DQ7B		B DQ 3	B DQ 3
4A	VREFB4AN0	10			DIFFIO_RX_B51p	DIFFOUT_B51p	T12	DQS7B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	T13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AB15	DQ7B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	10			DIFFIO_RX_B54n	DIFFOUT_B54n	W13	DQ7B		B_DQ_4	B_DQ_4
4A	VREFB4AN0				DIFFIO_TX_B53p	DIFFOUT_B53p	AB16	DQ7B		B_DQ_6	B_DQ_6
4A	VREFB4AN0				DIFFIO_RX_B54p	DIFFOUT_B54p	V13	DQ7B		B_DQ_5	B_DQ_5
4A	VREFB4AN0		CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	T14				
4A	VREFB4AN0			ļ	DIFFIO_TX_B56n	DIFFOUT_B56n	AB18	DQ7B		B_DQ_7	B_DQ_7
4A	VREFB4AN0		CLK2p		DIFFIO_RX_B55p	DIFFOUT_B55p	U13				
4A	VREFB4AN0				DIFFIO_TX_B56p	DIFFOUT_B56p	AA18	DQ7B		B_DM_0	B_DM_0
4A	VREFB4AN0				DIFFIO_TX_B57n	DIFFOUT_B57n	AA19			GND	GND
4A	VREFB4AN0				DIFFIO_RX_B58n	DIFFOUT_B58n	Y14	DQ8B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0				DIFFIO_TX_B57p	DIFFOUT_B57p	Y19	DQ8B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0				DIFFIO_RX_B58p	DIFFOUT_B58p	W14	DQ8B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0				DIFFIO_RX_B59n	DIFFOUT_B59n	P14	DQSn8B	DQ1B	B_DQS#_1	B_DQS#_1
4A 4A	VREFB4AN0				DIFFIO_TX_B60n	DIFFOUT_B60n	AA20	DQ8B	DQ1B	B_DQ_11	B_DQ_11
	VREFB4AN0				DIFFIO_RX_B59p	DIFFOUT_B59p	R14	DQS8B	DQ1B	B_DQS_1	B_DQS_1
4A 4A	VREFB4AN0 VREFB4AN0				DIFFIO_TX_B60p DIFFIO_TX_B61n	DIFFOUT_B60p DIFFOUT_B61n	Y20	DQ8B	DQ1B	B_CKE_1 B_CKE_0	B_CKE_1 B_CKE_0
4A	VREFB4AN0				DIFFIO_IX_B62n	DIFFOUT_B62n	AA15 U15	DQ8B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0				DIFFIO_RX_B62II	DIFFOUT_B62II	Y15	DQ8B	DQ1B	B_DQ_12 B_DQ_14	B_DQ_12 B_DQ_14
4A 4A	VREFB4AN0				DIFFIO_TX_B61p	DIFFOUT B62p	V15	DQ8B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0		CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	R15	DQ0B	DQIB	B_DQ_13	
4A	VREFB4AN0		CERON		DIFFIO_TX_B64n	DIFFOUT_B64n	AB20	DQ8B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0		CLK3p		DIFFIO RX B63p	DIFFOUT B63p	T15	2402	54.5	5_540	5_540
4A	VREFB4AN0		OL TOP		DIFFIO_TX_B64p	DIFFOUT_B64p	AB21	DQ8B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0				DIFFIO_TX_B65n	DIFFOUT_B65n	AB22	2402	54.5	GND	GND
4A	VREFB4AN0				DIFFIO_RX_B66n	DIFFOUT_B66n	Y16	DQ9B	DQ1B	B_DQ_16	B_DQ_16
4A		10			DIFFIO_TX_B65p	DIFFOUT_B65p	AA22	DQ9B	DQ1B	B_DQ_18	B_DQ_18
4A		10			DIFFIO_RX_B66p	DIFFOUT_B66p	Y17	DQ9B	DQ1B	B_DQ_17	B DQ 17
4A	VREFB4AN0	10			DIFFIO_RX_B67n	DIFFOUT_B67n	U16	DQSn9B	DQSn1B	B_DQS#_2	B_DQS#_2
4A		IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AA17	DQ9B	DQ1B	B_DQ_19	B_DQ_19
4A		10			DIFFIO_RX_B67p	DIFFOUT_B67p	U17	DQS9B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AB17			B_RESET#	B_RESET#
1A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	Y22	DQ9B	DQ1B	GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B70n	DIFFOUT_B70n	V18	DQ9B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	10			DIFFIO_TX_B69p	DIFFOUT_B69p	Y21	DQ9B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	W18	DQ9B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	W16			GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B72n	DIFFOUT_B72n	W21	DQ9B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	W17			GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B72p	DIFFOUT_B72p	W22	DQ9B	DQ1B	B_DM_2	B_DM_2
5A	VREFB5AN0	10	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R		+	
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20	L		+	
bA .	VREFB5AN0	IIU		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R	1	+	+
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19	2012	1	+	+
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R		+	
DA .	VREFB5AN0	IO IO	<u> </u>	O.D. CONEDONE	DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R	 	+	+
5A	VREFB5AN0	10	<u> </u>	CvP_CONFDONE	DIFFIO_TX_R3n DIFFIO_RX_R4n	DIFFOUT_R3n	T20	DQ1R	 	+	+
DA EA	VREFB5ANO	IO.	<u> </u>	DEV OF		DIFFOUT_R4n	T18	DQ1R	 	+	+
)M	VREFB5AN0 VREFB5AN0	10	 	DEV_OE	DIFFIO_TX_R5p DIFFIO_RX_R6p	DIFFOUT_R5p DIFFOUT_R6p	T22 R16	DQS1R	 	+	+
)A	VREFB5AN0 VREFB5AN0	10	 	DEV_CLRn	DIFFIO_RX_R6p DIFFIO_TX_R5n	DIFFOUT_R6p DIFFOUT_R5n	R16 R22	DQS1R DQ1R	 	+	+
5A 5A		IO IO		nPERSTL1	DIFFIO_IX_R5n	DIFFOUT_R5n DIFFOUT_R6n	R22	DQ1R DQSn1R	1	+	+
)M	NVELBOAM0	IU	1	HEEKOILI	DILLIO_KY_K0U	טוררטט ו_אטוו	K17	DUSTIK	1	1	1





											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
5A	VREFB5AN0	Ю			DIFFIO TX R7p	DIFFOUT R7p	R20	DQ1R		DDING/DDINZ (Z)	LI DDICE
5A	VREFB5AN0	10			DIFFIO_RX_R8p	DIFFOUT_R8p	R19	DQ1R			
5A	VREFB5AN0	10			DIFFIO_TX_R7n	DIFFOUT_R7n	R21				
5A	VREFB5AN0				DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R			
5B	VREFB5BN0				DIFFIO_RX_R25p	DIFFOUT_R25p	P16	2012			
5B 5B	VREFB5BN0 VREFB5BN0				DIFFIO_TX_R26p DIFFIO_RX_R25n	DIFFOUT_R26p DIFFOUT_R25n	P21 N16	DQ4R			_
5B	VREFB5BN0 VREFB5BN0				DIFFIO_RX_R25n DIFFIO_TX_R26n	DIFFOUT_R25n DIFFOUT_R26n	P22	DQ4R			
5B	VREFB5BN0				DIFFIO_RX_R27p	DIFFOUT_R27p	N20	DQ4R			
5B	VREFB5BN0				DIFFIO TX R28p	DIFFOUT R28p	M22	DQ4R			
5B	VREFB5BN0				DIFFIO RX R27n	DIFFOUT_R27n	N21	DQ4R			
5B	VREFB5BN0				DIFFIO_TX_R28n	DIFFOUT_R28n	L22	DQ4R			
5B	VREFB5BN0	10			DIFFIO_RX_R29p	DIFFOUT_R29p	P18	DQS4R			
5B	VREFB5BN0				DIFFIO_TX_R30p	DIFFOUT_R30p	K22				
5B	VREFB5BN0				DIFFIO_RX_R29n	DIFFOUT_R29n	N18	DQSn4R			
5B	VREFB5BN0				DIFFIO_TX_R30n	DIFFOUT_R30n	J22	DQ4R			
5B	VREFB5BN0				DIFFIO_RX_R31p	DIFFOUT_R31p	M21	DQ4R			
5B 5B	VREFB5BN0				DIFFIO_TX_R32p	DIFFOUT_R32p	F22	DQ4R			_
SB	VREFB5BN0 VREFB5BN0				DIFFIO_RX_R31n DIFFIO_TX_R32n	DIFFOUT_R31n DIFFOUT_R32n	M20 E22	DQ4R		1	+
5B		10	CLK7p,FPLL_BR_FBp		DIFFIO_TX_R32II	DIFFOUT_R33p	M16	 	+	+	+
iB		10	OCTO P. 1 CC_OIT_1 DP		DIFFIO_TX_R34p	DIFFOUT_R34p	E21	DQ5R		1	
5B		10	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	M17		1	1	1
5B		10			DIFFIO_TX_R34n	DIFFOUT_R34n	D22	DQ5R	1	1	1
5B	VREFB5BN0	10			DIFFIO_RX_R35p	DIFFOUT_R35p	L19	DQ5R			
5B		10			DIFFIO_TX_R36p	DIFFOUT_R36p	K21	DQ5R			
5B	VREFB5BN0	10			DIFFIO_RX_R35n	DIFFOUT_R35n	L20	DQ5R			
5B		10			DIFFIO_TX_R36n	DIFFOUT_R36n	J21	DQ5R			
5B	TILLIBOBITO	10			DIFFIO_RX_R37p	DIFFOUT_R37p	L15	DQS5R			
5B		10			DIFFIO_TX_R38p	DIFFOUT_R38p	G22				
5B	TILL BOBIG	10			DIFFIO_RX_R37n	DIFFOUT_R37n	K15	DQSn5R			
SB	VREFB5BN0	10			DIFFIO_TX_R38n	DIFFOUT_R38n	G21	DQ5R			
5B 5B		10			DIFFIO_RX_R39p DIFFIO_TX_R40p	DIFFOUT_R39p DIFFOUT_R40p	L18 G20	DQ5R DQ5R			
5B		10			DIFFIO_TX_R40p DIFFIO_RX_R39n	DIFFOUT_R39n	K19	DQ5R DQ5R			_
5B		10			DIFFIO_RX_R39II	DIFFOUT R40n	H21	DQSK			
5B		10	CLK6p		DIFFIO RX R41p	DIFFOUT R41p	L17				
5B	VREFB5BN0	10	oerop		DIFFIO_TX_R42p	DIFFOUT_R42p	E20	DQ6R			
5B	VREFB5BN0	10	CLK6n		DIFFIO RX R41n	DIFFOUT R41n	K17	Daoit			
5B	VREFB5BN0	Ю			DIFFIO TX R42n	DIFFOUT R42n	F20	DQ6R			
5B	VREFB5BN0	10			DIFFIO_RX_R43p	DIFFOUT_R43p	H20	DQ6R			
5B	VREFB5BN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	G18	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	H19	DQ6R			
5B	VREFB5BN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	G17	DQ6R			
5B	VREFB5BN0	10			DIFFIO_RX_R45p	DIFFOUT_R45p	K16	DQS6R			
SB	VREFB5BN0				DIFFIO_TX_R46p	DIFFOUT_R46p	F19	000.00			
SB	VREFB5BN0				DIFFIO_RX_R45n	DIFFOUT_R45n	J16	DQSn6R			
SB SB	VREFB5BN0 VREFB5BN0				DIFFIO_TX_R46n DIFFIO_RX_R47p	DIFFOUT_R46n DIFFOUT_R47p	F18 J17	DQ6R			
SB	VREFB5BN0 VREFB5BN0				DIFFIO_RX_R47p DIFFIO_TX_R48p	DIFFOUT_R47p DIFFOUT_R48p	J17 J19	DQ6R DQ6R		1	1
SB	VREFB5BN0				DIFFIO_TX_R46p DIFFIO_RX_R47n	DIFFOUT_R47n	J18	DQ6R		+	+
5B	VREFB5BN0				DIFFIO TX R48n	DIFFOUT R48n	H18			1	
	05,10	GND					F17	Ì		1	1
7A	VREFB7AN0				DIFFIO_RX_T25p	DIFFOUT_T25p	H16			GND	GND
7A	VREFB7AN0				DIFFIO_TX_T26p	DIFFOUT_T26p	C21	DQ4T	DQ1T	T_DM_2	T_DM_2
7A	VREFB7AN0		-		DIFFIO_RX_T25n	DIFFOUT_T25n	G16			GND	GND
7A	VREFB7AN0				DIFFIO_TX_T26n	DIFFOUT_T26n	C20	DQ4T	DQ1T	T_DQ_23	T_DQ_23
7A	VREFB7AN0				DIFFIO_RX_T27p	DIFFOUT_T27p	D18	DQ4T	DQ1T	T_DQ_21	T_DQ_21
7A	VREFB7AN0				DIFFIO_TX_T28p	DIFFOUT_T28p	B20	DQ4T	DQ1T	T_DQ_22	T_DQ_22
7A	VREFB7AN0				DIFFIO_RX_T27n	DIFFOUT_T27n	E17	DQ4T	DQ1T	T_DQ_20	T_DQ_20
7A 7A	VREFB7AN0				DIFFIO_TX_T28n	DIFFOUT_T28n	B21	DQ4T	DQ1T	GND T DOO 0	GND T DOC 0
7A 7A	VREFB7AN0 VREFB7AN0				DIFFIO_RX_T29p DIFFIO_TX_T30p	DIFFOUT_T29p DIFFOUT_T30p	G15 B22	DQS4T	DQS1T	T_DQS_2 T_RESET#	T_DQS_2 T_RESET#
7A	VREFB7AN0 VREFB7AN0				DIFFIO_TX_T30p DIFFIO_RX_T29n	DIFFOUT_T29n	G14	DQSn4T	DQSn1T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0				DIFFIO_TX_T30n	DIFFOUT_T30n	A22	DQ3H41 DQ4T	DQ3IITI DQ1T	T_DQ3#_2 T_DQ_19	T_DQ3#_2 T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	E16	DQ4T	DQ1T	T_DQ_19	T_DQ_17
7A		10			DIFFIO_TX_T32p	DIFFOUT_T32p	A20	DQ4T	DQ1T	T_DQ_18	T_DQ_18
'A	VREFB7AN0				DIFFIO_RX_T31n	DIFFOUT_T31n	D17	DQ4T	DQ1T	T_DQ_16	T_DQ_16
7A		10			DIFFIO_TX_T32n	DIFFOUT_T32n	A19	<u> </u>		GND	GND
7A		10	CLK11p		DIFFIO_RX_T33p	DIFFOUT_T33p	G13				
7A	VREFB7AN0				DIFFIO TX T34p	DIFFOUT_T34p	C19	DQ5T	DQ1T	T_DM_1	T_DM_1





Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0		CLK11n		DIFFIO_RX_T33n	DIFFOUT_T33n	F14				
7A	VREFB7AN0				DIFFIO_TX_T34n	DIFFOUT_T34n	C18	DQ5T	DQ1T	T_DQ_15	T_DQ_15
7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T35p DIFFIO_TX_T36p	DIFFOUT_T35p DIFFOUT_T36p	C16 B16	DQ5T DQ5T	DQ1T DQ1T	T_DQ_13 T_DQ_14	T_DQ_13 T_DQ_14
7A 7A		10			DIFFIO_IX_I36p DIFFIO_RX_T35n	DIFFOUT_136p DIFFOUT_T35n	C15	DQ5T	DQ1T	T_DQ_14	T_DQ_14 T_DQ_12
7A		IO			DIFFIO_TX_T36n	DIFFOUT_T36n	B15	DQ5T	DQ1T	T_CKE_0	T_CKE_0
7A		10			DIFFIO_RX_T37p	DIFFOUT_T37p	G12	DQS5T	DQ1T	T_DQS_1	T_DQS_1
7A	VREFB7AN0				DIFFIO_TX_T38p	DIFFOUT_T38p	A18			T_CKE_1	T_CKE_1
7A	VREFB7AN0				DIFFIO_RX_T37n	DIFFOUT_T37n	H12	DQSn5T	DQ1T	T_DQS#_1	T_DQS#_1
7A		IO IO			DIFFIO_TX_T38n DIFFIO_RX_T39p	DIFFOUT_T38n DIFFOUT_T39p	A17 F15	DQ5T DQ5T	DQ1T DQ1T	T_DQ_11 T_DQ_9	T_DQ_11 T_DQ_9
7A		10			DIFFIO_RX_139p DIFFIO_TX_T40p	DIFFOUT_T40p	B18	DQ5T	DQ1T	T_DQ_9	T_DQ_9
7A		10			DIFFIO RX T39n	DIFFOUT_T39n	E14	DQ5T	DQ1T	T_DQ_8	T DQ 8
7A	VREFB7AN0	10			DIFFIO_TX_T40n	DIFFOUT_T40n	B17			GND	GND
7A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T41p	DIFFOUT_T41p	H10				
7A	VREFB7AN0	10	12		DIFFIO_TX_T42p	DIFFOUT_T42p	A15	DQ6T		T_DM_0	T_DM_0
7A	VREFB7AN0 VREFB7AN0		CLK10n		DIFFIO_RX_T41n DIFFIO_TX_T42n	DIFFOUT_T41n DIFFOUT_T42n	G11 A14	DOCT	+	T DO 7	T DO 7
7A 7Δ	VREFB7AN0 VREFB7AN0	10			DIFFIO_IX_I42n DIFFIO_RX_T43p	DIFFOUT_142h DIFFOUT_T43p	D13	DQ6T DQ6T	+	T_DQ_7 T_DQ_5	T_DQ_7 T_DQ_5
7A	VREFB7AN0	10			DIFFIO_TX_T44p	DIFFOUT_T44p	C14	DQ6T	+	T_DQ_6	T_DQ_6
7A	VREFB7AN0	10			DIFFIO_RX_T43n	DIFFOUT_T43n	C13	DQ6T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	10			DIFFIO_TX_T44n	DIFFOUT_T44n	D14	DQ6T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	10			DIFFIO_RX_T45p	DIFFOUT_T45p	H9	DQS6T		T_DQS_0	T_DQS_0
7A 7A	VREFB7AN0	10		1	DIFFIO_TX_T46p	DIFFOUT_T46p	A13	D00-07	+	T_ODT_0	T_ODT_0
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T45n DIFFIO_TX_T46n	DIFFOUT_T45n DIFFOUT_T46n	G8 B13	DQSn6T DQ6T		T_DQS#_0 T_DQ_3	T_DQS#_0 T_DQ_3
7A	VREFB7AN0	10			DIFFIO_TX_T46II	DIFFOUT_T47p	E12	DQ6T	+	T_DQ_1	T_DQ_1
7A	VREFB7AN0	10			DIFFIO_TX_T48p	DIFFOUT T48p	B12	DQ6T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	10			DIFFIO_RX_T47n	DIFFOUT_T47n	F12	DQ6T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	10	RZQ_2		DIFFIO_TX_T48n	DIFFOUT_T48n	A12				
8A	VREFB8AN0	10	CLK9p		DIFFIO_RX_T49p	DIFFOUT_T49p	G10				
8A	VREFB8AN0	10	OLIVA		DIFFIO_TX_T50p	DIFFOUT_T50p	C11	DQ7T		T_A_0	T_CA_0
8A 8A	VREFB8AN0 VREFB8AN0	10	CLK9n		DIFFIO_RX_T49n DIFFIO_TX_T50n	DIFFOUT_T49n DIFFOUT_T50n	F10 B11	DQ7T		T A 1	T_CA_1
8A	VREFB8AN0	10			DIFFIO_RX_T51p	DIFFOUT_T51p	D11	DQ7T		T.A.4	T_CA_1
8A	VREFB8AN0	10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	A8	DQ7T		T_A_2	T_CA_2
8A	VREFB8AN0	10	·		DIFFIO_RX_T51n	DIFFOUT_T51n	E11	DQ7T		T_A_5	T_CA_5
8A	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	A7	DQ7T		T_A_3	T_CA_3
8A	VREFB8AN0	10			DIFFIO_RX_T53p	DIFFOUT_T53p	J9	DQS7T		T_CK	T_CK
8A 9 A	VREFB8AN0 VREFB8AN0	10			DIFFIO_TX_T54p DIFFIO_RX_T53n	DIFFOUT_T54p DIFFOUT_T53n	F8 J8	DQSn7T		T_A_6 T_CK#	T_CA_6 T_CK#
8A	VREFB8AN0	10			DIFFIO TX T54n	DIFFOUT T54n	F7	DQ3II/ I		T A 7	T CA 7
8A	VREFB8AN0	10			DIFFIO RX T55p	DIFFOUT T55p	C10	DQ7T		T_BA_1	1_0/
8A	VREFB8AN0	10			DIFFIO_TX_T56p	DIFFOUT_T56p	C6	DQ7T		T_BA_0	
8A	VREFB8AN0	10			DIFFIO_RX_T55n	DIFFOUT_T55n	C9	DQ7T		T_BA_2	
8A	VREFB8AN0	10	OLIVA EDILL TI ED		DIFFIO_TX_T56n	DIFFOUT_T56n	D7			GND	GND
8A	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	K7	DOOT	+	T 040#	
8A	VREFB8AN0 VREFB8AN0	10	CLK8n,FPLL TL FBn	<u> </u>	DIFFIO_TX_T58p DIFFIO_RX_T57n	DIFFOUT_T58p DIFFOUT_T57n	A10	DQ8T	+	T_CAS#	+
8A	VREFB8AN0	10	and the state of t	1	DIFFIO_TX_T58n	DIFFOUT_T58n	A9	DQ8T	1	T_RAS#	1
8A	VREFB8AN0	Ю			DIFFIO_RX_T59p	DIFFOUT_T59p	D9	DQ8T		T_A_8	T_CA_8
8A	VREFB8AN0	10			DIFFIO_TX_T60p	DIFFOUT_T60p	B6	DQ8T		T_A_10	
8A	VREFB8AN0	10			DIFFIO_RX_T59n	DIFFOUT_T59n	D8	DQ8T		T_A_9	T_CA_9
8A		10		 	DIFFIO_TX_T60n	DIFFOUT_T60n	B5	DQ8T	+	T_A_11	T 00# 0
8A	VREFB8AN0 VREFB8AN0	10		1	DIFFIO_RX_T61p DIFFIO_TX_T62p	DIFFOUT_T61p DIFFOUT_T62p	H8 C8	DQS8T	+	T_CS#_0 T_A_12	T_CS#_0
8A		10		1	DIFFIO_TX_T62p	DIFFOUT_162p DIFFOUT_T61n	G7	DQSn8T	1	T_K_12	T_CS#_1
8A		10			DIFFIO_TX_T62n	DIFFOUT_T62n	B8	DQ8T		T_A_13	
8A	VREFB8AN0	10			DIFFIO_RX_T63p	DIFFOUT_T63p	H6	DQ8T		T_A_14	
8A	VREFB8AN0	10			DIFFIO_TX_T64p	DIFFOUT_T64p	E6	DQ8T		T_WE#	
8A	VREFB8AN0	10			DIFFIO_RX_T63n	DIFFOUT_T63n	G6	DQ8T	-	T_A_15	OND
A8 Δ	VREFB8AN0	IO MSEL0		MSEL0	DIFFIO_TX_T64n	DIFFOUT_T64n	F7 L6	1	+	GND	GND
9A		CONF_DONE		CONF_DONE		 	J6	1	+	†	+
9A		MSEL1		MSEL1		1	K6	1			+
9A		nSTATUS		nSTATUS			G5				
9A		nCE		nCE			H5				
9A		MSEL2		MSEL2		1	A2 E5				+
								•			
9A		MSEL3 nCONFIG		MSEL3 nCONFIG			A4				+





										Note (1)
Bank Number	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
	GND					F3				
	GND					M9				
	GND					V22				
	GND					L3				
	GND					N11				
	GND					W20				
	GND					F11				
	GND					C3				
	GND					Y8				
	GND					K14				
	GND			-		D1		-		
	GND			-		K8		-		
	GND GND					V2 C7				-
	GND					A5				-
	GND					B2				+
	GND					M14				+
	GND			<u> </u>		M4		-		+
	GND			<u> </u>		G9		-		+
	GND			 		D2		 		+
	GND	 	+	 		L5		† 	1	+
	GND	<u> </u>			<u> </u>	J5		 		†
	GND					K1				
	GND					F1				
	GND					C22				+
	GND					AB1				1
	GND					L16				+
	GND					C4				1
	GND					H2				1
	GND					H1				1
	GND					J13				1
	GND					AB2				
	GND					E4				
	GND					AB19				1
	GND					D5				
	GND					J20				
	GND					V17				
	GND					A11				
	GND					U5				
	GND					G3				
	GND					H14				
	GND					T11				1
	GND					M2				1
	GND					J15				1
	GND					D10				
	GND					J3				
	GND					L13				
	GND					F6				
	GND					H4				
	GND					U9				
	GND					N7				
	GND					U19				
	GND					N15				
	GND					K12				ļ
	GND					AA11				
	GND					K2				
	GND					E3				ļ
	GND					P10				
	GND					A21				ļ
	GND					F2				
	GND			ļ		M1		ļ		ļ
	GND			ļ		P1		ļ		
	GND					K10				<u> </u>
	GND					Y5				<u> </u>
	GND					D20				1
	GND					B14				
	GND					Y2				
	GND					T2				
	GND					K4				
	GND					P4				
	GND	İ	1	1	1	C17	l	1	1	1





											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					M12				1
		GND					N22				
		GND					Y1				
		GND					N13				
		GND					W4				
		GND					AA3				
		GND					B1				
		GND					U14				
		GND					R3				
		GND					AA16				
		GND					T1				
		GND					AA4				
		GND					H3				
		GND			-		V1			-	+
		GND					F21				
		GND		+			N5 M19				+
		GND GND					W19 U3				
		GND					J11				
		GND			-	-	J11 Y13			-	+
		GND GND			 		F13			 	+
		GND GND		1	 	 	P2		1	 	+
		GND			 	 	N3		1	+	+
		GND			 	 	N3 R13		1	+	+
		GND GND		1	 	1	L11		1	†	+
		GND					W3			+	+
		GND					F16			+	+
		VCC					M13			+	+
		VCC			<u> </u>		K13			-	+
		VCC					J10			+	+
		VCC					M11			+	+
		VCC					P13				+
		VCC			<u> </u>		H15			-	+
		VCC					M15			+	+
		VCC			<u> </u>		N14			-	+
		VCC		†			L12				+
		VCC			<u> </u>		J12			-	+
		VCC					H13				+
		VCC					L10				+
		VCC					K9				+
		VCC					P11				+
		VCC					P15				+
		VCC					N12				+
		VCC					H11				+
		VCC					J14				+
		VCC					L14				†
		VCC					K11				1
		DNU					B3				1
		DNU					B4				1
		DNU					AB3				
		DNU					V11				
		DNU					D21				
		DNU					E10				
		VCCPGM					Y6				
		VCCPGM					U20				
		VCCPGM					B7				
		VCCBAT					A3				
		VCCIO3A					AA6				
		VCCIO3A					T6				
		VCCIO3B					R8				
		VCCIO3B					AB9				
		VCCIO3B					W10				
		VCCIO3B					V7				
		VCCIO4A					Y18				
		VCCIO4A					W15				
		VCCIO4A					T16				
		VCCIO4A					V12				
		VCCIO4A					AB14				
		VCCIO4A					AA21				
		VCCIO5A VCCIO5A					T21 R18				



Pin Information for the Cyclone® V 5CGXFC9 Device Version 1.1 Note (1)

Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin	HMC Pin
Number	VKLF	riii Name/runcuon	Optional Function(s)	Configuration Function	Channel	Emulated EVD3 Output Channel	0404	DQ3 IOI X0	DQ3 IOI X IO	Assignment for	Assignment for
										DDR3/DDR2 (2)	LPDDR2
		VCCIO5B					G19				
		VCCIO5B					N17				
		VCCIO5B					P20				_
		VCCIO5B					K18				_
		VCCIO5B				ļ	L21				
		VCCIO5B				ļ	H22				
		VCCIO7A				ļ	H17				
		VCCIO7A				ļ	C12				
		VCCIO7A					D15				
		VCCIO7A				ļ	B19				
		VCCIO7A				ļ	A16				
		VCCIO7A					E18				
		VCCIO8A					E8				
		VCCIO8A					A6				
		VCCIO8A					H7				
		VCCIO8A					B9				
		VCCPD3A					V6				
		VCCPD3B4A					V14				
		VCCPD3B4A				1	V10		1		
		VCCPD3B4A					W9				
		VCCPD3B4A					V16				
		VCCPD5A					P17				
		VCCPD5B		1			N19				1
		VCCPD5B		1			M18				1
		VCCPD7A8A		1			E9				1
		VCCPD7A8A		1			F13				1
		VCCPD7A8A					F9				+
		VCCPD7A8A					E15				+
3A	VREFB3AN0	VREFB3AN0					W6				+
3B	VREFB3BN0	VREFB3BN0		+		+	AB12				+
4A	VREFB4AN0	VREFB4AN0		+		+	AA14				+
5A	VREFB5AN0	VREFB5AN0		+		+	V21				+
5B	VREFB5BN0	VREFB5BN0		+		+	K20				+
7A	VREFB7AN0	VREFB7AN0		1		+	D16				+
8A	VREFB8AN0	VREFB8AN0		1		+	B10				+
OM	VKEFBOAINU	NC		1		+	C2				+
		NC					C2 C1			-	+
		NC NC					D4			-	+
										-	+
		NC VCCH_GXBL		+	+	+	D3 T3	-	†	+	+
		VCCH_GXBL VCCH_GXBL		+	+	+	M3	-	†	+	+
				+	+	+	P3	-	†	+	+
		VCCL_GXBL		+	-	+		+	1	+	+
		VCCL_GXBL		+	+	+	K3		 	-	+
		RREF_TL		1	ļ	1	A1		ļ	1	+
		VCCA_FPLL		+	+	+	T4		 	-	+
		VCCA_FPLL		1	ļ	1	F4		ļ	1	+
		VCCA_FPLL				1	U18		ļ		
		VCCA_FPLL				1	E19		ļ		
		VCC_AUX				1	D19		ļ		
		VCC_AUX				4	AA12				
		VCC_AUX				4	W19				
		VCC_AUX		1			D6				
		VCC_AUX		1			D12				
		VCC_AUX					AB5				
		VCCE_GXBL				1	N4				
		VCCE_GXBL					L4				
		VCCE_GXBL					J4		<u> </u>		
		VCCE_GXBL					K5				

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for	HMC Pin Assignment for
01/0 14		DEED IN								DDR3/DDR2 (2), (3)	LPDDR2 (3)
GXB_L1 GXB_L1	1	REFCLK1Ln REFCLK1Lp				+	F5 G4				
XB_L1		GXB_TX_L5n					D3		1	1	
XB_L1		GXB_TX_L5p					D4				-
XB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2				
XB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1				
XB_L1		GXB_TX_L4n					E1				
XB_L1		GXB_TX_L4p					E2				
XB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
SXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
XB_L1		GXB_TX_L3n					J1				
XB_L1		GXB_TX_L3p					J2				
XB_L1 XB_L1		GXB_RX_L3p,GXB_REFCLK_L3p			-		L2		-	+	
XB_L1 XB_L0		GXB_RX_L3n,GXB_REFCLK_L3n GXB_TX_L2n					L1				-
XB_L0 XB_L0		GXB_TX_L2n GXB_TX_L2p			+		N1 N2		+	+	
XB_L0		GXB_TX_L2p GXB_RX_L2p,GXB_REFCLK_L2p					R2				-
XB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1				
XB_L0		GXB_TX_L1n					U1		+		-
XB_L0	1	GXB_TX_L1p		1	 	<u> </u>	U2		 	 	†
XB_L0	1	GXB_RX_L1p,GXB_REFCLK_L1p		İ	1		W2	Ì	1	1	1
XB_L0	İ	GXB_RX_L1n,GXB_REFCLK_L1n		İ	İ		W1	Ì	İ	İ	1
XB_L0	i e	GXB_TX_L0n					Y3				
XB_L0	1	GXB_TX_L0p					Y4				
XB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2				
XB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1				
XB_L0		REFCLK0Lp					V4				
XB_L0		REFCLK0Ln					U4				
4		TDO		TDO			M5				
4		nCSO		DATA4			R4			ļ	
١		TMS		TMS			P5				
<u> </u>		AS_DATA3		DATA3	-		T4		-	+	
A A		TCK AS_DATA2		TCK DATA2	-		V5 AA5		-	+	
A		TDI		TDI			W5				
A		AS_DATA1		DATA1	+		AB3		+	+	
A		DCLK		DCLK	+		V3		+	+	
Α		AS_DATA0,ASDO		DATA0			AB4				
Α	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT B1n	R6	DQ1B	+		-
A	VREFB3AN0	10		DATA5	DIFFIO TX B2n	DIFFOUT B2n	U7	54.5		1	
A	VREFB3AN0	10		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B		1	
A	VREFB3AN0	IO		DATA7	DIFFIO TX B2p	DIFFOUT B2p	U8	DQ1B			
A	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B		ĺ	
Ą	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B		ĺ	
Ą	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N6	DQS1B			
A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W9				
A	VREFB3AN0	10		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	T7	DQ1B			
4	VREFB3AN0	10		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B			
١	VREFB3AN0	10		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B	_	_	
4	VREFB3AN0	10		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B	+	+	1
1	VREFB3AN0	10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6	DOAD	+	+	
1	VREFB3AN0 VREFB3AN0	10		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7 M7	DQ1B	 	 	
^	VREFB3AN0 VREFB3AN0	10	+	PR_ERROR	DIFFIO_RX_B7p DIFFIO_TX_B8p	DIFFOUT_B7p DIFFOUT_B8p	M7 P7	DQ1B	+	+	
3	VREFB3AN0 VREFB3BN0	IO IO	 	1	DIFFIO_TX_B33n	DIFFOUT_B33n	AB6	מומ	†	GND	GND
3	VREFB3BN0	10		1	DIFFIO_TX_B33II	DIFFOUT B34n	V9	DQ2B	+	B_A_15	OND
3	VREFB3BN0	10		İ	DIFFIO_TX_B33p	DIFFOUT_B33p	AB5	DQ2B	1	B_WE#	1
3	VREFB3BN0	IO			DIFFIO RX B34p	DIFFOUT_B34p	V10	DQ2B	1	B A 14	
3	VREFB3BN0	IO			DIFFIO RX B35n	DIFFOUT_B35n	P8	DQSn2B		B_CS#_1	B_CS#_1
3	VREFB3BN0	10			DIFFIO_TX_B36n	DIFFOUT_B36n	AA7	DQ2B		B_A_13	
3	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	N8	DQS2B		B_CS#_0	B_CS#_0
3	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AB7			B_A_12	
3	VREFB3BN0	10			DIFFIO_TX_B37n	DIFFOUT_B37n	AA8	DQ2B		B_A_11	
3	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	T9	DQ2B		B_A_9	B_CA_9
3	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AB8	DQ2B		B_A_10	
3	VREFB3BN0	10			DIFFIO_RX_B38p	DIFFOUT_B38p	U10	DQ2B	1	B_A_8	B_CA_8
В		10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	M8		1	1	
3	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AA10	DQ2B		B_RAS#	
3	VREFB3BN0		CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p	DIFFOUT_B39p	M9	L	_	 	_
В	VREFB3BN0			ļ	DIFFIO_TX_B40p	DIFFOUT_B40p	AA9	DQ2B	+	B_CAS#	
BB	VREFB3BN0	IO		1	DIFFIO_TX_B41n	DIFFOUT_B41n	Y10			GND	GND



											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2), (3)	HMC Pin Assignment for LPDDR2 (3)
3B	VREFB3BN0				DIFFIO_RX_B42n	DIFFOUT_B42n	T10	DQ3B		B_BA_2	
В	VREFB3BN0	-			DIFFIO_TX_B41p	DIFFOUT_B41p	Y9	DQ3B		B_BA_0	
В		10			DIFFIO_RX_B42p	DIFFOUT_B42p	R9	DQ3B		B_BA_1	<u> </u>
B	VREFB3BN0				DIFFIO_RX_B43n	DIFFOUT_B43n	U11	DQSn3B		B_CK#	B_CK#
BB BB	VREFB3BN0 VREFB3BN0				DIFFIO_TX_B44n DIFFIO_RX_B43p	DIFFOUT_B44n DIFFOUT_B43p	R12 U12	DQ3B DQS3B	-	B_A_7 B_CK	B_CA_7 B_CK
BB	VREFB3BN0				DIFFIO_RX_B43p	DIFFOUT_B43p DIFFOUT_B44p	P12	DQSSB		B A 6	B_CA_6
BB	VREFB3BN0		FPLL BL CLKOUT1,FPLL BL CLKOUTn		DIFFIO_TX_B45n	DIFFOUT B45n	AB10	DQ3B		B A 3	B CA 3
3B	VREFB3BN0				DIFFIO RX B46n	DIFFOUT B46n	R10	DQ3B		B A 5	B CA 5
3B	VREFB3BN0	10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AB11	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0				DIFFIO_RX_B46p	DIFFOUT_B46p	R11	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0		CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	P9				
3B	VREFB3BN0				DIFFIO_TX_B48n	DIFFOUT_B48n	Y11	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0		CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	N9	0000			2.01.0
3B 4A	VREFB3BN0 VREFB4AN0	10	RZQ_0		DIFFIO_TX_B48p DIFFIO_TX_B49n	DIFFOUT_B48p DIFFOUT_B49n	AA12 AB13	DQ3B	-	B_A_0	B_CA_0
4A 4A	VREFB4AN0		RZQ_U		DIFFIO_IX_B49fi DIFFIO_RX_B50n	DIFFOUT_B49h DIFFOUT_B50h	V13	DQ4B		B_DQ_0	B_DQ_0
4A		10			DIFFIO TX B49p	DIFFOUT_B49p	AB12	DQ4B	1	B_DQ_0 B_DQ_2	B DQ 2
4A	VREFB4AN0	10			DIFFIO_RX_B50p	DIFFOUT_B50p	U13	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0				DIFFIO_RX_B51n	DIFFOUT_B51n	T12	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VICEIDAMINO	10			DIFFIO_TX_B52n	DIFFOUT_B52n	AA14	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0				DIFFIO_RX_B51p	DIFFOUT_B51p	T13	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	10			DIFFIO_TX_B52p	DIFFOUT_B52p	AA13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	10			DIFFIO_TX_B53n	DIFFOUT_B53n	AB15	DQ4B	-	B_ODT_1	B_ODT_1
4A	VREFB4AN0				DIFFIO_RX_B54n	DIFFOUT_B54n	Y14	DQ4B		B_DQ_4	B_DQ_4
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B53p DIFFIO_RX_B54p	DIFFOUT_B53p	AA15	DQ4B DQ4B		B_DQ_6 B_DQ_5	B_DQ_6 B DQ 5
1A	VREFB4AN0 VREFB4AN0	10	CLK2n		DIFFIO_RX_B54p DIFFIO_RX_B55n	DIFFOUT_B54p DIFFOUT_B55n	Y15 V14	DQ4B	-	B_DQ_5	B_DQ_5
4A 4A	VREFB4AN0 VREFB4AN0		CLKZN		DIFFIO_RX_B55fi	DIFFOUT_B55n DIFFOUT_B56n	AB17	DQ4B		B DQ 7	B DQ 7
4A	VREFB4AN0	In	CLK2p		DIFFIO_RX_B55p	DIFFOUT B55p	V15	DQ4B		B_DQ_r	B_DQ_1
4A	VREFB4AN0	10	OLALP		DIFFIO_TX_B56p	DIFFOUT_B56p	AB18	DQ4B		B DM 0	B DM 0
4A	VREFB4AN0				DIFFIO_TX_B57n	DIFFOUT_B57n	AB20	54.5		GND	GND
4A	VREFB4AN0				DIFFIO_RX_B58n	DIFFOUT_B58n	Y16	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AB21	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	10			DIFFIO_RX_B58p	DIFFOUT_B58p	Y17	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0				DIFFIO_RX_B59n	DIFFOUT_B59n	T14	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0				DIFFIO_TX_B60n	DIFFOUT_B60n	AA17	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	10			DIFFIO_RX_B59p	DIFFOUT_B59p	U15	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A 4A	VREFB4AN0	10			DIFFIO_TX_B60p	DIFFOUT_B60p	AA18	0.050	2012	B_CKE_1	B_CKE_1
4A 4A		10			DIFFIO_TX_B61n DIFFIO_RX_B62n	DIFFOUT_B61n DIFFOUT_B62n	AA19 V20	DQ5B DQ5B	DQ1B DQ1B	B_CKE_0 B_DQ_12	B_CKE_0 B_DQ_12
4A 4A	VREFB4AN0	10			DIFFIO_TX_B61p	DIFFOUT_B62II DIFFOUT_B61p	AA20	DQ5B	DQ1B	B_DQ_12 B_DQ_14	B_DQ_12 B_DQ_14
4A 4A	VREFB4AN0	lio			DIFFIO_TX_B61p	DIFFOUT B62p	W19	DQ5B DQ5B	DQ1B DQ1B	B_DQ_14	B_DQ_14 B_DQ_13
4A		10	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	V16	DQSD	DQID		D_DQ_10
4A	VREFB4AN0	10			DIFFIO_TX_B64n	DIFFOUT B64n	AB22	DQ5B	DQ1B	B DQ 15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO RX B63p	DIFFOUT B63p	W16				
4A	VREFB4AN0	10			DIFFIO_TX_B64p	DIFFOUT_B64p	AA22	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	Y22			GND	GND
1A	VREFB4AN0	10			DIFFIO_RX_B66n	DIFFOUT_B66n	Y20	DQ6B	DQ1B	B_DQ_16	B_DQ_16
1A	VREFB4AN0	10			DIFFIO_TX_B65p	DIFFOUT_B65p	W22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IIO			DIFFIO_RX_B66p	DIFFOUT_B66p	Y19	DQ6B	DQ1B	B_DQ_17	B_DQ_17
IA 1A	VREFB4ANO	IO IO			DIFFIO_RX_B67n	DIFFOUT Been	P14	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A 4A		lio		+	DIFFIO_TX_B68n DIFFIO_RX_B67p	DIFFOUT_B68n DIFFOUT_B67p	Y21 R14	DQ6B DQS6B	DQ1B DQS1B	B_DQ_19 B_DQS_2	B_DQ_19 B_DQS_2
<i>1</i> Δ	VREFB4AN0 VREFB4AN0	IIO		1	DIFFIO_RX_B67p DIFFIO_TX_B68p	DIFFOUT_B67p DIFFOUT_B68p	W21	DUSOD	סופאת	B_DQS_2 B_RESET#	B_DQS_2 B_RESET#
4A	VREFB4AN0 VREFB4AN0	lio		+	DIFFIO_TX_B68p	DIFFOUT_B68p DIFFOUT_B69n	U22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0				DIFFIO RX B70n	DIFFOUT_B70n	V19	DQ6B	DQ1B DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0			İ	DIFFIO_TX_B69p	DIFFOUT B69p	V21	DQ6B	DQ1B	B DQ 22	B DQ 22
4A	VREFB4AN0				DIFFIO_RX_B70p	DIFFOUT_B70p	V18	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	10			DIFFIO_RX_B71n	DIFFOUT_B71n	U16			GND	GND
1A	VREFB4AN0				DIFFIO_TX_B72n	DIFFOUT_B72n	U21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0				DIFFIO_RX_B71p	DIFFOUT_B71p	U17			GND	GND
4A	VREFB4AN0				DIFFIO_TX_B72p	DIFFOUT_B72p	U20	DQ6B	DQ1B	B_DM_2	B_DM_2
5A	VREFB5AN0		RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	T19	DQ1R	ļ	\bot	
	VREFB5AN0			INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	T18	2012		+	+
5A						DIFFOUT_R1n	T20	DQ1R	1	1	1
5A 5A	VREFB5AN0			PR_REQUEST	DIFFIO_TX_R1n						+
5A 5A 5A	VREFB5AN0 VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	T17				
5A 5A 5A 5A	VREFB5AN0 VREFB5AN0 VREFB5AN0	IO IO			DIFFIO_RX_R2n DIFFIO_TX_R3p	DIFFOUT_R2n DIFFOUT_R3p	T17 T22	DQ1R			
5A 5A	VREFB5AN0 VREFB5AN0 VREFB5AN0 VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	T17				





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Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2), (3)	HMC Pin Assignment for LPDDR2 (3)
5A	VREFB5AN0	10		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21			DDI(G/DDI(E (E), (G)	LI DDILE (0)
iA	VREFB5AN0			nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	P22	DQ1R			
A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
A	VREFB5AN0	10			DIFFIO_TX_R7p	DIFFOUT_R7p	P19	DQ1R			
iA	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	P16	DQ1R			ļ
iA	VREFB5AN0	10			DIFFIO_TX_R7n	DIFFOUT_R7n	P18				
iA iB	VREFB5AN0 VREFB5BN0	10	CLK6p		DIFFIO_RX_R8n	DIFFOUT_R8n	P17 N16	DQ1R	+		
B B	VREFB5BN0	10	СЕКОР		DIFFIO_RX_R41p DIFFIO_TX_R42p	DIFFOUT_R41p DIFFOUT_R42p	N20	DQ2R	+	+	+
SR.	VREFB5BN0 VREFB5BN0	10	CLK6n		DIFFIO_IX_R42p	DIFFOUT_R42p DIFFOUT_R41n	M16	DQZR		+	-
SR.	VREFB5BN0	in .	CEROII	+	DIFFIO_TX_R42n	DIFFOUT R42n	N21	DQ2R		+	
5B	VREFB5BN0	IO			DIFFIO RX R43p	DIFFOUT R43p	N19	DQ2R		+	
5B	VREFB5BN0	10	FPLL BR CLKOUTO,FPLL BR CLKOUTp,FPLL BR FB		DIFFIO TX R44p	DIFFOUT R44p	M22	DQ2R		+	
iB.	VREFB5BN0	10			DIFFIO_RX_R43n	DIFFOUT_R43n	M18	DQ2R		1	
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	L22	DQ2R			
iΒ	VREFB5BN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	K17	DQS2R			
5B	VREFB5BN0				DIFFIO_TX_R46p	DIFFOUT_R46p	M20				
5B	VREFB5BN0				DIFFIO_RX_R45n	DIFFOUT_R45n	L17	DQSn2R			ļ
5B	VREFB5BN0				DIFFIO_TX_R46n	DIFFOUT_R46n	M21	DQ2R	1		
5B	VREFB5BN0				DIFFIO_RX_R47p	DIFFOUT_R47p	L19	DQ2R	1		↓
5B	VREFB5BN0			+	DIFFIO_TX_R48p	DIFFOUT_R48p	K21	DQ2R	1	+	
5B	VREFB5BN0				DIFFIO_RX_R47n	DIFFOUT_R47n	L18	DQ2R	+		
5B 7A	VREFB5BN0	GND		+	DIFFIO_TX_R48n	DIFFOUT_R48n	K22 F17		+	+	+
7A	VREFB7AN0				DIFFIO_RX_T9p	DIFFOUT_T9p	H21		+	GND	GND
7A	VREFB7AN0				DIFFIO_TX_T10p	DIFFOUT_T10p	E21	DQ1T	+	T DM 4	T_DM_4
7A		10			DIFFIO_RX_T9n	DIFFOUT_T9n	G21	DQTT		GND	GND
7A		10			DIFFIO_TX_T10n	DIFFOUT T10n	D21	DQ1T		T DQ 39	T DQ 39
7A		IO			DIFFIO_RX_T11p	DIFFOUT_T11p	E19	DQ1T		T_DQ_37	T_DQ_37
7A		IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C20	DQ1T		T_DQ_38	T_DQ_38
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	D19	DQ1T		T_DQ_36	T_DQ_36
7A		IO			DIFFIO_TX_T12n	DIFFOUT_T12n	B20	DQ1T		GND	GND
7A		10			DIFFIO_RX_T13p	DIFFOUT_T13p	J21	DQS1T		T_DQS_4	T_DQS_4
7A		IO			DIFFIO_TX_T14p	DIFFOUT_T14p	B18			GND	GND
7A		10			DIFFIO_RX_T13n	DIFFOUT_T13n	J22	DQSn1T		T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	B17	DQ1T		T_DQ_35	T_DQ_35
7A	VREFB7AN0	10			DIFFIO_RX_T15p	DIFFOUT_T15p	C21	DQ1T		T_DQ_33	T_DQ_33
7A	VREFB7AN0				DIFFIO_TX_T16p	DIFFOUT_T16p	G22	DQ1T		T_DQ_34	T_DQ_34
7A 7A	VREFB7AN0 VREFB7AN0				DIFFIO_RX_T15n DIFFIO_TX_T16n	DIFFOUT_T15n	B21 F22	DQ1T	+	T_DQ_32	T_DQ_32
7A 7A	VREFB7AN0				DIFFIO_TX_T16n DIFFIO_RX_T25p	DIFFOUT_T16n DIFFOUT_T25p	K20		+	GND GND	GND GND
7A	VREFB7AN0				DIFFIO_RX_125p DIFFIO_TX_T26p	DIFFOUT_T26p	B16	DQ2T	DQ1T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO .		+	DIFFIO RX T25n	DIFFOUT T25n	K19	DQZI	DQTT	GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT T26n	C16	DQ2T	DQ1T	T DQ 23	T DQ 23
7A	VREFB7AN0				DIFFIO_RX_T27p	DIFFOUT_T27p	D17	DQ2T	DQ1T	T DQ 21	T DQ 21
7A	VREFB7AN0				DIFFIO_TX_T28p	DIFFOUT_T28p	G17	DQ2T	DQ1T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	10			DIFFIO_RX_T27n	DIFFOUT_T27n	E16	DQ2T	DQ1T	T_DQ_20	T_DQ_20
7A	VREFB7AN0				DIFFIO_TX_T28n	DIFFOUT_T28n	G16	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0				DIFFIO_RX_T29p	DIFFOUT_T29p	G18	DQS2T	DQS1T	T_DQS_2	T_DQS_2
'A	VREFB7AN0				DIFFIO_TX_T30p	DIFFOUT_T30p	J19		1	T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	H18	DQSn2T	DQSn1T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IIO		+	DIFFIO_TX_T30n	DIFFOUT_T30n	J18	DQ2T	DQ1T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO IO		1	DIFFIO_RX_T31p	DIFFOUT_T31p	E15	DQ2T	DQ1T	T_DQ_17	T_DQ_17
7A 7A	VREFB7AN0 VREFB7AN0	10		+	DIFFIO_TX_T32p DIFFIO_RX_T31n	DIFFOUT_T32p DIFFOUT_T31n	A15 F15	DQ2T DQ2T	DQ1T DQ1T	T_DQ_18 T_DQ_16	T_DQ_18 T_DQ_16
7A 7A	VREFB7AN0 VREFB7AN0	IO			DIFFIO_RX_131n DIFFIO_TX_T32n	DIFFOUT_T31n DIFFOUT_T32n	A14	DQ21	DQTI	GND	GND
7A	VREFB7AN0	IO	CLK11p	+	DIFFIO_IX_I32n DIFFIO_RX_T33p	DIFFOUT_T33p	H16	1	1	CIND	SIND
7A	VREFB7AN0	IO		1	DIFFIO_TX_T34p	DIFFOUT T34p	J17	DQ3T	DQ1T	T DM 1	T DM 1
7A	VREFB7AN0	10	CLK11n		DIFFIO RX T33n	DIFFOUT T33n	H15				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	K16	DQ3T	DQ1T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	10			DIFFIO_RX_T35p	DIFFOUT_T35p	C15	DQ3T	DQ1T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	G15	DQ3T	DQ1T	T_DQ_14	T_DQ_14
7A		IO			DIFFIO_RX_T35n	DIFFOUT_T35n	B15	DQ3T	DQ1T	T_DQ_12	T_DQ_12
7A		IO			DIFFIO_TX_T36n	DIFFOUT_T36n	F14	DQ3T	DQ1T	T_CKE_0	T_CKE_0
7A	VREFB7AN0				DIFFIO_RX_T37p	DIFFOUT_T37p	H14	DQS3T	DQ1T	T_DQS_1	T_DQS_1
7A	VREFB7AN0				DIFFIO_TX_T38p	DIFFOUT_T38p	B13		<u> </u>	T_CKE_1	T_CKE_1
7A	VREFB7AN0				DIFFIO_RX_T37n DIFFIO_TX_T38n	DIFFOUT_T37n	J13	DQSn3T	DQ1T	T_DQS#_1	T_DQS#_1
			•			DIFFOUT_T38n	A13	DQ3T	DQ1T	T DQ 11	T DQ 11
7A 7A	VREFB7AN0 VREFB7AN0			1	DIFFIO_TX_T39p	DIFFOUT_T39p	E14	DQ3T	DQ1T	T DQ 9	T_DQ_11





Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for	HMC Pin Assignment for
										DDR3/DDR2 (2), (3)	LPDDR2 (3)
7A		10			DIFFIO_RX_T39n	DIFFOUT_T39n	F13	DQ3T	DQ1T	T_DQ_8	T_DQ_8
7A	VREFB7AN0				DIFFIO_TX_T40n	DIFFOUT_T40n	H10			GND	GND
7A		10	CLK10p	+	DIFFIO_RX_T41p	DIFFOUT_T41p	H13				
7A		10	0.1440		DIFFIO_TX_T42p	DIFFOUT_T42p	G11	DQ4T		T_DM_0	T_DM_0
7A		10	CLK10n		DIFFIO_RX_T41n	DIFFOUT_T41n	G13	DOAT		T DO 7	T DO 7
7A 7A		10		+	DIFFIO_TX_T42n	DIFFOUT_T42n	F12	DQ4T	_	T_DQ_7	T_DQ_7
7A 7A	VREFB7AN0	10			DIFFIO_RX_T43p	DIFFOUT_T43p	D13	DQ4T		T_DQ_5	T_DQ_5
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T44p DIFFIO_RX_T43n	DIFFOUT_T44p	B12 C13	DQ4T DQ4T		T_DQ_6	T_DQ_6
7A 7Δ		10		+	DIFFIO_RX_143n DIFFIO_TX_T44n	DIFFOUT_T43n DIFFOUT_T44n	A12	DQ4T	_	T_DQ_4	T_DQ_4 T_ODT_1
7A 7A		10					H11			T_ODT_1	
7A		10		+	DIFFIO_RX_T45p DIFFIO_TX_T46p	DIFFOUT_T45p DIFFOUT_T46p	H11	DQS4T		T_DQS_0 T_ODT_0	T_DQS_0 T_ODT_0
7A				+	DIFFIO_TX_146p DIFFIO_RX_T45n	DIFFOUT_146p DIFFOUT_T45n	G12	DQSn4T			T_DQS#_0
7A		10		+	DIFFIO_RX_145fi	DIFFOUT T46n				T_DQS#_0	T_DQS#_0 T_DQ_3
7A		10		+			K9	DQ4T		T_DQ_3	
7A		10		+	DIFFIO_RX_T47p	DIFFOUT_T47p	D12	DQ4T		T_DQ_1	T_DQ_1
/A		10			DIFFIO_TX_T48p	DIFFOUT_T48p	C11	DQ4T		T_DQ_2	T_DQ_2
7A		10	070.0	+	DIFFIO_RX_T47n	DIFFOUT_T47n	E12	DQ4T	_	T_DQ_0	T_DQ_0
7A	VREFB7AN0		RZQ_2		DIFFIO_TX_T48n	DIFFOUT_T48n	B11				
ŏΑ		10	CLK9p	+	DIFFIO_RX_T49p	DIFFOUT_T49p	G10	DOST	-	T A O	T 04 0
ŏΑ		10	0.140	+	DIFFIO_TX_T50p	DIFFOUT_T50p	L7	DQ5T	-	T_A_0	T_CA_0
8A		10	CLK9n	+	DIFFIO_RX_T49n	DIFFOUT_T49n	F10	DOST	-		T 01 1
8A		10		+	DIFFIO_TX_T50n	DIFFOUT_T50n	K7	DQ5T	+	T_A_1	T_CA_1
8A		10		+	DIFFIO_RX_T51p	DIFFOUT_T51p	J7	DQ5T	+	T_A_4	T_CA_4
8A		10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	H8	DQ5T		T_A_2	T_CA_2
8A	VREFB8AN0	10		+	DIFFIO_RX_T51n	DIFFOUT_T51n	J8	DQ5T	+	T_A_5	T_CA_5
8A	VREFB8AN0	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	G8	DQ5T		T_A_3	T_CA_3
8A	VREFB8AN0	10			DIFFIO_RX_T53p	DIFFOUT_T53p	J9	DQS5T		T_CK	T_CK
8A	VREFB8AN0	10			DIFFIO_TX_T54p	DIFFOUT_T54p	A10			T_A_6	T_CA_6
8A	VREFB8AN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	H9	DQSn5T		T_CK#	T_CK#
8A	VREFB8AN0	10			DIFFIO_TX_T54n	DIFFOUT_T54n	A9	DQ5T		T_A_7	T_CA_7
8A	VREFB8AN0	10			DIFFIO_RX_T55p	DIFFOUT_T55p	B10	DQ5T		T_BA_1	
8A	VREFB8AN0	10			DIFFIO_TX_T56p	DIFFOUT_T56p	A5	DQ5T		T_BA_0	
8A	VREFB8AN0	10			DIFFIO_RX_T55n	DIFFOUT_T55n	C9	DQ5T		T_BA_2	
8A	VREFB8AN0	10			DIFFIO_TX_T56n	DIFFOUT_T56n	B5			GND	GND
8A	VREFB8AN0	10	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	E10				
8A	VREFB8AN0	10			DIFFIO_TX_T58p	DIFFOUT_T58p	B6	DQ6T		T_CAS#	
8A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T57n	DIFFOUT_T57n	F9				
8A	VREFB8AN0	10			DIFFIO_TX_T58n	DIFFOUT_T58n	B7	DQ6T		T_RAS#	
8A	TITLE DOTTE	10			DIFFIO_RX_T59p	DIFFOUT_T59p	A8	DQ6T		T_A_8	T_CA_8
8A		10			DIFFIO_TX_T60p	DIFFOUT_T60p	C6	DQ6T		T_A_10	
8A	VREFB8AN0	10			DIFFIO_RX_T59n	DIFFOUT_T59n	A7	DQ6T		T_A_9	T_CA_9
8A	VREFB8AN0	10			DIFFIO_TX_T60n	DIFFOUT_T60n	D6	DQ6T		T_A_11	
8A	VREFB8AN0	10			DIFFIO_RX_T61p	DIFFOUT_T61p	E9	DQS6T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	10			DIFFIO_TX_T62p	DIFFOUT_T62p	D7			T_A_12	
8A	VREFB8AN0	10			DIFFIO_RX_T61n	DIFFOUT_T61n	D9	DQSn6T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	10		1	DIFFIO_TX_T62n	DIFFOUT_T62n	C8	DQ6T		T_A_13	
8A		10		1	DIFFIO_RX_T63p	DIFFOUT_T63p	G6	DQ6T		T_A_14	
8A		10		1	DIFFIO_TX_T64p	DIFFOUT_T64p	F7	DQ6T		T_WE#	
8A		10		1	DIFFIO_RX_T63n	DIFFOUT_T63n	H6	DQ6T		T_A_15	
8A	VREFB8AN0	10		1	DIFFIO_TX_T64n	DIFFOUT_T64n	E7	ļ		GND	GND
9A		MSEL0		MSEL0			L6	1			
9A		CONF_DONE		CONF_DONE			K6	1			
9A		MSEL1		MSEL1			J6	ļ			
9A		nSTATUS		nSTATUS			H5	1			
9A		nCE		nCE			G5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			E5				
9A		nCONFIG		nCONFIG			A4				
9A		MSEL4		MSEL4			F3				
9A		GND		1			C5	1			
		GND					J20				
		GND					L21				
		GND					N22				
		GND					T21				
		GND				1	Y18				
		GND					AB14				
		GND					V12				
		GND					AA6				
I		GND					V7				
		GND					U5				
		GND			T .		AA4	1	1	- I	





											Note (1
Bank Number		Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2), (3)	HMC Pin Assignment for LPDDR2 (3)
		GND					Y5				
		GND					U3				
		GND					R3				
		GND					P4				
		GND					P2				
		GND					N5				
		GND					L3				
		GND					M4				
		GND					L5				
		GND		†			K2				
		GND		<u> </u>			J3				
	1	GND		1	+		K4			+	
		GND					H2				
		GND		ł			H3				
				+							
		GND					J5				
		GND					G3				
		GND					H4				
		GND					F2				
	1	GND			ļ		B1			ļ	1
		GND					E3				
		GND					AB19				
		GND					AB9				
		GND					AB2				
		GND					AB1				
		GND					AA11				
		GND					AA3				
		GND					Y2				
		GND					Y1				
		GND					W4				<u> </u>
		GND					W3				
	1	GND		1	+		V22			+	
		GND					V22				-
		GND		+			V17				
		GND					V2				
		GND					V1				
		GND					U9				
		GND					T16				
		GND					T2				
		GND					T1				
		GND					R13				
		GND					P10				
		GND					P1				
		GND					N17				
		GND					N15				
		GND					N13				
		GND					N11				
		GND					N7				
		GND			İ		N3			İ	
	1	GND			†		M14		1	†	
	1	GND		1	†		M12		1	†	t
	1	GND			†		M10		1	†	
	1	GND		+	 	†	M2		 	 	
	1	GND	1	1	 	 	M2 M1		1	 	
	1	GND	 	}	+	 	M1 L15		1	+	
	 	CND			-	 	L10		1	-	
	1	GND					L13		ļ		
	.	GND					L11				
	!	GND					K14				
	ļ	GND			Ļ	ļ	K12			Ļ	
	1	GND			ļ		K10			ļ	1
		GND					K8				
		GND					K1				
		GND					J15				
		GND					H22				
		GND					H12				
		GND			1		H7			1	
	1	GND		1	†		H1		1	†	†
	1	GND	†		†	†	G19			†	
	1	GND	1	1	†	 	G19 G9		1	†	
	 				-	 			1	-	
	 	GND				-	F16				
	1	GND					F6		ļ		
		GND GND		1			F1 E13			-	-





											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2), (3)	HMC Pin Assignment for LPDDR2 (3)
		GND					E4				
		GND					D20				
		GND					D10				
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C17				
		GND					C4				
		GND					C3				
		GND					B14				
		GND					B9				
		GND					B2				
		GND					A21				
		GND					A11				
		VCC					P15	-			
		VCC					P13				
		VCC					P11				
		VCC					N14				
	-	VCC		1	1	1	N12	1	1	1	
	1	VCC		1	1	1	N10	+	}	1	
	1	VCC		1	1	1	M15	+	}	1	
	1	VCC		1			M13	1	ļ	1	
	1	VCC		1			M11	1	ļ	1	
-	1	VCC		1			L16	1	ļ	1	
		VCC					L14				
		VCC					L12				
		VCC					L10				
		VCC					K15				
		VCC					K13				
		VCC					K11				
		VCC					J16				
		VCC					J14				
		VCC					J12				
		VCC					J10				
		DNU					B3				
		DNU					B4				
		DNU					Y6				
		DNU					V11	-			
		DNU					E17	-			
		DNU					L9	-			
		VCCPGM		-			V8				
		VCCPGM		-			R19 F8				
		VCCPGM		-							
		VCCBAT					A3				
	-	VCCIO3A VCCIO3A		+		 	T6 Y8	 	1	-	
	1	VCCIO3A VCCIO3B	 	1	1	1	78 R8	 	1	1	+
	-			+		 	Y13	 	1	-	
	1	VCCIO3B VCCIO3B				1	W10	 	+	1	+
	1	VCCIO3B VCCIO3B	1	1		1	T11	t	†		-
	1	VCCIO3B VCCIO4A	 	1	1	1	U19	 	1	1	+
	1	VCCIO4A VCCIO4A		+		1	AA21	 	†		
	1	VCCIO4A VCCIO4A		+		1	AA16	 	†		
		VCCIO4A VCCIO4A				1	W20				
	1	VCCIO4A VCCIO4A		†	 	†	W15	† 	†	 	
	1	VCCIO4A VCCIO4A		+		1	W15 U14	 	†		
	1	VCCIO4A VCCIO5A		†	 	†	P20	† 	†	 	
	1	VCCIOSA VCCIOSA	 	1	1	1	R18	 	1	1	+
	1	VCCIO5A VCCIO5B		+		1	M19	 	†		
	1	VCCIO5B VCCIO5B		†	 	†	K18	† 	†	 	
		VCCIO7A				1	B19				
	1	VCCIO7A VCCIO7A		†	 	†	H17	† 	†	 	
	1	VCCIO7A VCCIO7A		†	 	†	G14	† 	†	 	
	1	VCCIO7A VCCIO7A		+		1	F21	 	†		
	 	VCCIO7A VCCIO7A		1		+	F11	—	†	-	
	1	VCCIO7A VCCIO7A				1	F11 E18	 	+	1	+
	1	VCCIO7A VCCIO7A		+		1	D15	 	†		
	1	VCCIO7A VCCIO7A	 	1	1	1	C22	 	1	1	+
	 	VCCIO7A VCCIO7A		1		+	C12	—	†	-	
 	1	VCCIO7A VCCIO7A	 	1	1	1	A16	 	1	1	
	1	VCCIO7A VCCIO8A	1	1		1	A16	t	†		-
	1	VOCIOOA	I.	ı	1	I.	MD	l	l	I	



Pin Information for the Cyclone® V 5CGXFC9 Device Version 1.1 Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2), (3)	HMC Pin Assignment for LPDDR2 (3)
		VCCIO8A					G7				
		VCCIO8A					E8				
		VCCIO8A					C7				
		VCCPD3A					W6				
		VCCPD3B4A					W12				
		VCCPD3B4A				İ	W17				
		VCCPD3B4A				İ	W14				
		VCCPD3B4A				İ	W11				
		VCCPD5A				İ	P21				
		VCCPD5B					M17				
		VCCPD5B					N18				
		VCCPD7A8A					D8				
		VCCPD7A8A		+		1	E11				
		VCCPD7A8A					D16				
		VCCPD7A8A					D16				
		VCCPD7A8A VCCPD7A8A		+	1		C10	+	+		
3A	VDEEDOANS			+		+	Y7	-	+	+	-
	VREFB3AN0	VREFB3AN0		+	-	+		-	+	+	
3B	VREFB3BN0	VREFB3BN0		+	-	+	Y12	-	+	+	
4A	VREFB4AN0	VREFB4AN0				+	AB16	1	+		
5A	VREFB5AN0	VREFB5AN0					R20				
5B	VREFB5BN0	VREFB5BN0					L20				
7A	VREFB7AN0	VREFB7AN0					C14				
8A	VREFB8AN0	VREFB8AN0					B8				
		NC					H20				
		NC					G20				
		NC					F20				
		NC					F19				
		NC					F18				
		NC					E22				
		NC				İ	E20				
		NC				İ	D22				
		NC					C19				
		NC					C18				
		NC					B22				
		NC NC					A22				
		NC NC					A20				
		NC NC		+		1	A19				
		NC NC		-		1	A18				
		NC NC		-		1	A17				
		VCCH_GXBL					M3		+		t
					-		T3	+	+		
		VCCH_GXBL			-		K3	+	+		
		VCCL_GXBL		+	-	+		-	+	+	
		VCCL_GXBL				-	P3	1	+		1
		RREF_TL				-	A1	1	+		1
		VCCA_FPLL				+	T5	1	+		
		VCCA_FPLL				+	F4	1	+		
		VCCA_FPLL					U18		1		ļ
		VCCA_FPLL					H19		1		ļ
		VCC_AUX					E6		1		ļ
		VCC_AUX					D11				
		VCC_AUX					W18				
		VCC_AUX					W13				
		VCC_AUX					W7				
		VCC_AUX					D18				
		VCCE_GXBL					J4				
		VCCE_GXBL					N4		1		1
		VCCE_GXBL	1				L4		1		İ
		VCCE GXBL		_			K5				

(1) For more information about pin definition and pin connection guidelines, refer to the

Cyclone V Device Family Pin Connection Guidelines.

(2) RESET pin is only applicable for DDR3 device.
(3) This package supports only a 24-bit HMC using T_DQ_[0..23] pins. The T_DQ_[32..39] pins cannot be used for HMC.



						Note (
Bank lumber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
SXB_L2		GXB_TX_L8n					C3				
SXB_L2		GXB_TX_L8p					C4				
SXB_L2		GXB_RX_L8p,GXB_REFCLK_L8p					D2				
SXB_L2		GXB_RX_L8n,GXB_REFCLK_L8n					D1				
XB_L2		GXB_TX_L7n					E3				
XB_L2		GXB_TX_L7p					E4				
XB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					F2 F1				
XB_L2 XB_L2		GXB_RX_L7n,GXB_REFCLK_L7n GXB_TX_L6n					F1 G3				
XB_L2 XB_L2		GXB_TX_L6p				+	G3 G4				
XB_L2		GXB_RX_L6p,GXB_REFCLK_L6p					H2				
XB_L2		GXB RX L6n,GXB REFCLK L6n					H1				
XB_L2		REFCLK2Lp					M6				
XB_L2		REFCLK2Ln					1.5				
XB_L1		REFCLK1Ln					P6				
XB_L1		REFCLK1Lp					N7				
XB_L1		GXB_TX_L5n					K1				
XB_L1		GXB_TX_L5p					K2				
KB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					M2				
(B_L1		GXB_RX_L5n,GXB_REFCLK_L5n					M1				
(B_L1		GXB_TX_L4n					P1				
(B_L1		GXB_TX_L4p		ļ	ļ		P2	ļ	ļ	1	ļ
(B_L1		GXB_RX_L4p,GXB_REFCLK_L4p		ļ		ļ	T2	ļ			
(B_L1	-	GXB_RX_L4n,GXB_REFCLK_L4n		!	ļ	1	T1	ļ		ļ	!
KB_L1	-	GXB_TX_L3n		 	1	1	W3	1	1	1	1
KB_L1 KB_L1		GXB_TX_L3p		1	 		W4	 	-	<u> </u>	
(B_L1 (B_L1	-	GXB_RX_L3p,GXB_REFCLK_L3p GXB_RX_L3n,GXB_REFCLK_L3n		+		1	V2 V1	 	 	1	
(B_L0 (B_L0		GXB_TX_L2n GXB_TX_L2p					AA3 AA4				
(B_L0		GXB_TX_L2p GXB_RX_L2p,GXB_REFCLK_L2p					Y2				
(B_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y1				
(B_L0		GXB_TX_L1n					AC3				
(B_L0		GXB_TX_L1p					AC4				
(B L0		GXB_RX_L1p,GXB_REFCLK_L1p					AB2				
(B_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB1				
(B_L0		GXB_TX_L0n					AE3				
(B_L0		GXB_TX_L0p					AE4				
XB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD2				
KB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD1				
KB_L0		REFCLK0Lp					V6				
(B_L0		REFCLK0Ln					W6				
		TDO		TDO			V7				
		nCSO		DATA4			Y6				
		TMS		TMS			R6				
		AS_DATA3		DATA3			U6				
		TCK AS_DATA2		TCK DATA2			Y5 AB5				
		TDI		TDI			T6				
		AS DATA1		DATA1			AD5				
		DCLK		DCLK		1	N8	1	 		1
		AS_DATA0,ASDO		DATA0			AF5				
		10		DATA6	DIFFIO RX B1n	DIFFOUT_B1n	T7	DQ1B			
	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7	1	İ		İ
	VREFB3AN0			DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	T8	DQ1B			İ
	VREFB3AN0	10		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V8	DQ1B			
	VREFB3AN0	10		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	W8	DQSn1B			
	VREFB3AN0			DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB6	DQ1B			
	VREFB3AN0	10		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	Y9	DQS1B			
	VREFB3AN0	10		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA6				
	VREFB3AN0	10		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R10	DQ1B	ļ	1	ļ
	VREFB3AN0	10		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AA7	DQ1B			
	VREFB3AN0			CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	R9	DQ1B		ļ	!
		IO .	1	DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B	-	ļ	
	VREFB3AN0			PR_DONE	DIFFIO_RX_B7n DIFFIO_TX_B8n	DIFFOUT_B7n	R8	DOAD	-	<u> </u>	
	VREFB3ANO	10		PR_READY		DIFFOUT_B8n	AD6	DQ1B		-	
	VREFB3AN0 VREFB3AN0			PR_ERROR	DIFFIO_RX_B7p DIFFIO_TX_B8p	DIFFOUT_B7p DIFFOUT_B8p	P8 AD7	DQ1B	—	-	1
		IO IO	1	 	DIFFIO_TX_B8p DIFFIO_TX_B33n	DIFFOUT_B33n	U9	שואעום	 	GND	GND
	VREFB3BN0 VREFB3BN0		1	 	DIFFIO_IX_B33n DIFFIO_RX_B34n	DIFFOUT_B33n DIFFOUT_B34n	V11	DQ2B	† 	B_A_15	OIND
	VREFB3BN0		1	 	DIFFIO_KX_B34II	DIFFOUT_B33p	T9	DQ2B		B_A_IS B WE#	1
	VREFB3BN0	10	1	 	DIFFIO_TX_B33p	DIFFOUT_B33p	W11	DQ2B DQ2B		B_A_14	1
	VREFB3BN0	10		<u> </u>	DIFFIO_RX_B34p	DIFFOUT_B35n	T11	DQSn2B	<u> </u>	B_CS#_1	B CS# 1
	VREFB3BN0	10		<u> </u>	DIFFIO_TX_B36n	DIFFOUT_B36n	AC10	DQ3H2B	<u> </u>	B_A_13	5_00#_1
	VREFB3BN0	10		1	DIFFIO_RX_B35p	DIFFOUT_B35p	R11	DQS2B	†	B_CS#_0	B_CS#_0
		10		1	DIFFIO TX B36p	DIFFOUT_B36p	AB10	1	1	B_A_12	
3	VREFB3BN0	10		1	DIFFIO_TX_B37n	DIFFOUT_B37n	AC8	DQ2B	1	B_A_11	
	VREFB3BN0			†	DIFFIO_RX_B38n	DIFFOUT B38n	AB11	DQ2B		B_A_9	B CA 9



											Note (1
Bank Number		Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	10			DIFFIO_TX_B37p	DIFFOUT_B37p	AC9	DQ2B		B_A_10	
3B	VREFB3BN0	10			DIFFIO_RX_B38p	DIFFOUT_B38p	AB12	DQ2B		B_A_8	B_CA_8
3B	VREFB3BN0	10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	T12				
3B	VREFB3BN0	10			DIFFIO_TX_B40n	DIFFOUT_B40n	Y10	DQ2B		B_RAS#	
3B	VREFB3BN0	10	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p	DIFFOUT_B39p	T13	2002			
3B	VREFB3BN0	10			DIFFIO_TX_B40p	DIFFOUT_B40p	W10	DQ2B		B_CAS#	OND
3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_IX_B41n DIFFIO_RX_B42n	DIFFOUT_B41n DIFFOUT_B42n	V9 AE8	DQ3B		GND B BA 2	GND
3B 3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_RX_B42h DIFFIO_TX_B41p	DIFFOUT_B42n DIFFOUT_B41p	V10	DQ3B DQ3B		B_BA_2 B_BA_0	
3D 3D	VREFB3BN0	9			DIFFIO_TX_B41p	DIFFOUT_B41p	AD8	DQ3B DQ3B		B BA 1	+
3D 3D	VREFB3BN0	0			DIFFIO_RX_B43n	DIFFOUT_B43n	P10	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	10			DIFFIO_TX_B44n	DIFFOUT_B44n	AF9	DQ3B3B		B_A_7	B_CA_7
3B		10			DIFFIO_RX_B43p	DIFFOUT_B43p	N10	DQS3B		B_CK	B_CK
3B	VREFB3BN0	10			DIFFIO_TX_B44p	DIFFOUT_B44p	AE9	Dacob		B A 6	B CA 6
3B	VREFB3BN0		FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO TX B45n	DIFFOUT_B45n	AF8	DQ3B		B_A_3	B CA 3
3B	VREFB3BN0	10			DIFFIO RX B46n	DIFFOUT B46n	U11	DQ3B		B A 5	B CA 5
3B	VREFB3BN0	Ю	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AF7	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO RX B46p	DIFFOUT_B46p	U10	DQ3B		B A 4	B CA 4
3B	VREFB3BN0	Ю	CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	P12				
3B	VREFB3BN0	Ю			DIFFIO_TX_B48n	DIFFOUT_B48n	AF6	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	Ю	CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	P11				
3B	VREFB3BN0				DIFFIO_TX_B48p	DIFFOUT_B48p	AE6	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	Ю	RZQ_0		DIFFIO_TX_B49n	DIFFOUT_B49n	AE11				
4A	VREFB4AN0	Ю			DIFFIO_RX_B50n	DIFFOUT_B50n	AA14	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	Ю			DIFFIO_TX_B49p	DIFFOUT_B49p	AD11	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	10			DIFFIO_RX_B50p	DIFFOUT_B50p	Y14	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	10			DIFFIO_RX_B51n	DIFFOUT_B51n	W13	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0				DIFFIO_TX_B52n	DIFFOUT_B52n	AD12	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	10			DIFFIO_RX_B51p	DIFFOUT_B51p	V13	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	10			DIFFIO_TX_B52p	DIFFOUT_B52p	AD13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	10			DIFFIO_TX_B53n	DIFFOUT_B53n	AE10	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	10			DIFFIO_RX_B54n	DIFFOUT_B54n	Y13	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0				DIFFIO_TX_B53p	DIFFOUT_B53p	AD10	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	10			DIFFIO_RX_B54p	DIFFOUT_B54p	W12	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	10	CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	V12				
4A	VREFB4AN0	10			DIFFIO_TX_B56n	DIFFOUT_B56n	AF12	DQ4B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	10	CLK2p		DIFFIO_RX_B55p	DIFFOUT_B55p	U12				
4A	VREFB4AN0	10			DIFFIO_TX_B56p	DIFFOUT_B56p	AF11	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	10			DIFFIO_TX_B57n	DIFFOUT_B57n	AC13		2012	GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B58n	DIFFOUT_B58n	AC15	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A 4A	VREFB4AN0 VREFB4AN0				DIFFIO_TX_B57p	DIFFOUT_B57p	AC14 AB15	DQ5B DQ5B	DQ1B DQ1B	B_DQ_10 B_DQ_9	B_DQ_10
., .	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B58p DIFFIO_RX_B59n	DIFFOUT_B58p DIFFOUT_B59n	V14	DQ5B DQSn5B	DQ1B DQ1B	B_DQ_9 B_DQS#_1	B_DQ_9 B_DQS#_1
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B59n DIFFIO_TX_B60n	DIFFOUT_B59n DIFFOUT_B60n	V14 AF13	DQ5B5B	DQ1B DQ1B	B_DQS#_1 B_DQ_11	B_DQS#_1 B_DQ_11
4A	VREFB4AN0				DIFFIO_TX_B6001	DIFFOUT_B59p	U14	DQS5B	DQ1B	B DQS 1	B DQS 1
4A 4A	VREFB4AN0	0			DIFFIO_RX_B59p	DIFFOUT_B60p	AE13	DQSSB	DQIB	B_CKE_1	B_DQS_1 B_CKE_1
4A		10			DIFFIO_TX_B61n	DIFFOUT_B61n	AF14	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	2			DIFFIO_TX_B6111	DIFFOUT B62n	AB16	DQ5B DQ5B	DQ1B	B DQ 12	B DQ 12
4A	VREFB4AN0				DIFFIO_TX_B61p	DIFFOUT_B61p	AE14	DQ5B	DQ1B	B_DQ_12	B_DQ_14
4A	VREFB4AN0				DIFFIO_RX_B62p	DIFFOUT_B62p	AA16	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	10	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	Y16	DQSD	DQID	D_DQ_10	
4A	VREFB4AN0	i0	OLIVOIT		DIFFIO_TX_B64n	DIFFOUT_B64n	AF18	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VRFFB4AN0		CLK3p		DIFFIO_RX_B63p	DIFFOUT_B63p	Y15	Daob	Daile	D_DQ_10	D_50_10
4A	VREFB4AN0	Ю		1	DIFFIO_TX_B64p	DIFFOUT_B64p	AE18	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	Ю			DIFFIO_TX_B65n	DIFFOUT_B65n	AD18	1		GND	GND
4A	VREFB4AN0				DIFFIO_RX_B66n	DIFFOUT_B66n	AD16	DQ6B	DQ1B	B_DQ_16	B DQ 16
4A	VREFB4AN0	Ю			DIFFIO_TX_B65p	DIFFOUT_B65p	AC18	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	Ю			DIFFIO_RX_B66p	DIFFOUT_B66p	AD17	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	10			DIFFIO RX B67n	DIFFOUT_B67n	W15	DQSn6B	DQSn1B	B DQS# 2	B DQS# 2
4A	VREFB4AN0	Ю			DIFFIO_TX_B68n	DIFFOUT_B68n	AF19	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0				DIFFIO_RX_B67p	DIFFOUT_B67p	V15	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	Ю			DIFFIO_TX_B68p	DIFFOUT_B68p	AE19			B_RESET#	B_RESET#
4A	VREFB4AN0	10			DIFFIO_TX_B69n	DIFFOUT_B69n	AF22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	Ю			DIFFIO_RX_B70n	DIFFOUT_B70n	AC17	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	10			DIFFIO_TX_B69p	DIFFOUT_B69p	AF21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0				DIFFIO_RX_B70p	DIFFOUT_B70p	AB17	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	10			DIFFIO_RX_B71n	DIFFOUT_B71n	U17			GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B72n	DIFFOUT_B72n	AE21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	10			DIFFIO_RX_B71p	DIFFOUT_B71p	T17			GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B72p	DIFFOUT_B72p	AE20	DQ6B	DQ1B	B_DM_2	B_DM_2
4A	VREFB4AN0			<u> </u>	DIFFIO_TX_B73n	DIFFOUT_B73n	AD20	1		GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B74n	DIFFOUT_B74n	AE15	DQ7B	DQ2B	B_DQ_24	B_DQ_24
4A	VREFB4AN0	10			DIFFIO_TX_B73p	DIFFOUT_B73p	AC20	DQ7B	DQ2B	B_DQ_26	B_DQ_26
4A	VREFB4AN0	10	1		DIFFIO_RX_B74p	DIFFOUT_B74p	AE16	DQ7B	DQ2B	B_DQ_25	B_DQ_25
4A	VREFB4AN0		1		DIFFIO_RX_B75n	DIFFOUT_B75n	W17	DQSn7B	DQ2B	B_DQS#_3	B_DQS#_3
4A	VREFB4AN0				DIFFIO_TX_B76n	DIFFOUT_B76n	AD21	DQ7B	DQ2B	B_DQ_27	B_DQ_27
4A	VREFB4AN0		1		DIFFIO_RX_B75p	DIFFOUT_B75p	W16	DQS7B	DQ2B	B_DQS_3	B_DQS_3
4A	VREFB4AN0	10			DIFFIO_TX_B76p	DIFFOUT_B76p	AD22	1		GND	GND



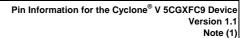
											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	Ю			DIFFIO_TX_B77n	DIFFOUT_B77n	AE23	DQ7B	DQ2B	GND	GND
4A	VREFB4AN0	Ю			DIFFIO_RX_B78n	DIFFOUT_B78n	AF16	DQ7B	DQ2B	B_DQ_28	B_DQ_28
4A	VREFB4AN0	Ю			DIFFIO_TX_B77p	DIFFOUT_B77p	AD23	DQ7B	DQ2B	B_DQ_30	B_DQ_30
4A		Ю			DIFFIO_RX_B78p	DIFFOUT_B78p	AF17	DQ7B	DQ2B	B_DQ_29	B_DQ_29
4A	VREFB4AN0	10			DIFFIO_RX_B79n	DIFFOUT_B79n	U16			GND	GND
4A	VICEIDINATO	10			DIFFIO_TX_B80n	DIFFOUT_B80n	AF23	DQ7B	DQ2B	B_DQ_31	B_DQ_31
4A	VREFB4AN0	10			DIFFIO_RX_B79p	DIFFOUT_B79p	U15		ļ	GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B80p	DIFFOUT_B80p	AE24	DQ7B	DQ2B	B_DM_3	B_DM_3
4A	VREFB4AN0	10			DIFFIO_TX_B81n	DIFFOUT_B81n	AF24			GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B82n	DIFFOUT_B82n	AA18	DQ8B	DQ2B	B_DQ_32	B_DQ_32
4A 4A	VREFB4AN0 VREFB4AN0				DIFFIO_TX_B81p DIFFIO_RX_B82p	DIFFOUT_B81p DIFFOUT_B82p	AE25 Y18	DQ8B DQ8B	DQ2B DQ2B	B_DQ_34 B_DQ_33	B_DQ_34 B_DQ_33
4A 4A	VREFB4AN0				DIFFIO_RX_B83n	DIFFOUT_B83n	V17	DQSn8B	DQSn2B	B_DQ_33 B_DQS#_4	B_DQ_33 B_DQS#_4
4A		10			DIFFIO_TX_B84n	DIFFOUT B84n	AE26	DQ8B	DQ3H2B	B_DQ3#_4 B DQ 35	B_DQ3#_4 B_DQ_35
4A	VREFB4AN0	10			DIFFIO_RX_B83p	DIFFOUT_B83p	V18	DQS8B	DQS2B	B DQS 4	B DQS 4
4A		10			DIFFIO_TX_B84p	DIFFOUT_B84p	AD26	DQOOD	DQOZD	GND	GND
4A		10			DIFFIO TX B85n	DIFFOUT B85n	AC19	DQ8B	DQ2B	GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B86n	DIFFOUT_B86n	Y19	DQ8B	DQ2B	B DQ 36	B DQ 36
4A		Ю			DIFFIO_TX_B85p	DIFFOUT_B85p	AB19	DQ8B	DQ2B	B_DQ_38	B_DQ_38
4A	VREFB4AN0	Ю			DIFFIO RX B86p	DIFFOUT_B86p	Y20	DQ8B	DQ2B	B DQ 37	B DQ 37
4A	VREFB4AN0	Ю			DIFFIO_RX_B87n	DIFFOUT_B87n	W18			GND	GND
4A		Ю			DIFFIO_TX_B88n	DIFFOUT_B88n	AA21	DQ8B	DQ2B	B_DQ_39	B_DQ_39
4A	VREFB4AN0				DIFFIO_RX_B87p	DIFFOUT_B87p	V19			GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B88p	DIFFOUT_B88p	AB22	DQ8B	DQ2B	B_DM_4	B_DM_4
5A		10	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AC22	DQ1R			
5A		10		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	U19	ļ		+	
5A	VREFB5AN0			PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AC23	DQ1R	ļ		
5A	VREFB5AN0			CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V20				
5A	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AA22	DQ1R			
5A	VREFB5AN0	10		O. D. CONEDONE	DIFFIO_RX_R4p	DIFFOUT_R4p	W20	DQ1R	-	+	
5A 5A	VREFB5AN0 VREFB5AN0	10		CvP_CONFDONE	DIFFIO_TX_R3n DIFFIO_RX_R4n	DIFFOUT_R3n DIFFOUT_R4n	AA23 W21	DQ1R DQ1R		+	+
5A	VREFB5AN0			DEV OF	DIFFIO_RX_R4II	DIFFOUT_R5p	AC24	DQIK		+	+
5A	VREFB5AN0			nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	V22	DQS1R		+	
5A		10		DEV CLRn	DIFFIO TX R5n	DIFFOUT R5n	AB24	DQ1R		+	+
5A	VREFB5AN0	10		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	U22	DQSn1R		+	+
5A		10		III EIGHEI	DIFFIO TX R7p	DIFFOUT R7p	Y23	DQ1R		+	+
5A	VREFB5AN0	Ю			DIFFIO RX R8p	DIFFOUT_R8p	T19	DQ1R			-
5A	VREFB5AN0				DIFFIO_TX_R7n	DIFFOUT_R7n	Y24			1	1
5A	VREFB5AN0	Ю			DIFFIO_RX_R8n	DIFFOUT_R8n	U20	DQ1R		T	
5B	VREFB5BN0	Ю	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R33p	DIFFOUT_R33p	T21				
5B	VIKEI DODING	Ю			DIFFIO_TX_R34p	DIFFOUT_R34p	V23	DQ2R			
5B	VREFB5BN0	Ю	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	T22				
5B	VREFB5BN0				DIFFIO_TX_R34n	DIFFOUT_R34n	V24	DQ2R			
5B		10			DIFFIO_RX_R35p	DIFFOUT_R35p	T23	DQ2R			
5B	VREFB5BN0	10			DIFFIO_TX_R36p	DIFFOUT_R36p	AA24	DQ2R			
5B	VREFB5BN0				DIFFIO_RX_R35n	DIFFOUT_R35n	T24	DQ2R			
5B	VIKEI DODING	10			DIFFIO_TX_R36n	DIFFOUT_R36n	AB25	DQ2R			
5B	VREFB5BN0				DIFFIO_RX_R37p	DIFFOUT_R37p	R23	DQS2R			
5B 5B	VREFB5BN0 VREFB5BN0	10		-	DIFFIO_TX_R38p DIFFIO_RX_R37n	DIFFOUT_R38p DIFFOUT_R37n	AD25 P23	DQSn2R	+	+	+
		0								+	+
5B 5B	VREFB5BN0 VREFB5BN0	0		†	DIFFIO_TX_R38n DIFFIO_RX_R39p	DIFFOUT_R38n DIFFOUT_R39p	AC25 R24	DQ2R DQ2R	1	+	+
5B		10	1		DIFFIO_RX_R39p	DIFFOUT_R40p	U24	DQ2R DQ2R	1	+	+
5B		10		†	DIFFIO_TX_R40p	DIFFOUT R39n	R25	DQ2R DQ2R	1	1	1
5B	VREFB5BN0	Ю			DIFFIO_TX_R40n	DIFFOUT_R40n	V25	1		1	1
5B		Ю	CLK6p		DIFFIO_RX_R41p	DIFFOUT_R41p	R20	İ	1	1	1
5B		Ю			DIFFIO_TX_R42p	DIFFOUT_R42p	AB26	DQ3R	İ	1	1
5B	VREFB5BN0	Ю	CLK6n	<u> </u>	DIFFIO_RX_R41n	DIFFOUT_R41n	P20		<u> </u>	1	
5B	VREFB5BN0				DIFFIO_TX_R42n	DIFFOUT_R42n	AA26	DQ3R			
5B	VREFB5BN0	Ю			DIFFIO_RX_R43p	DIFFOUT_R43p	T26	DQ3R			
5B	VREFB5BN0	Ю	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	Y25	DQ3R			
5B	VREFB5BN0	10			DIFFIO_RX_R43n	DIFFOUT_R43n	R26	DQ3R			
5B	VREFB5BN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn	ļ	DIFFIO_TX_R44n	DIFFOUT_R44n	Y26	DQ3R		+	
5B	VREFB5BN0	10			DIFFIO_RX_R45p	DIFFOUT_R45p	P21	DQS3R			
5B	VREFB5BN0	IO .		ļ	DIFFIO_TX_R46p	DIFFOUT_R46p	W25		_	 	
5B	VREFB5BN0	10	ļ		DIFFIO_RX_R45n	DIFFOUT_R45n	P22	DQSn3R	1	+	+
5B	VIKEI DODING	10		ļ	DIFFIO_TX_R46n	DIFFOUT_R46n	W26	DQ3R	1	+	+
5B		10		_	DIFFIO_RX_R47p	DIFFOUT_R47p	N25	DQ3R	 	+	+
5B	VREFB5BN0 VRFFB5BN0	10		 	DIFFIO_TX_R48p DIFFIO_RX_R47n	DIFFOUT_R48p DIFFOUT_R47n	U25 P26	DQ3R DQ3R	 	+	+
5B 5B	VREFB5BN0 VREFB5BN0	10		-				DUSK	 	+	+
		10	CLK5p	†	DIFFIO_TX_R48n DIFFIO_RX_R49p	DIFFOUT_R48n DIFFOUT_R49p	U26 N20	†	1	+	+
	AKELBRAM)	10	OEROP	+	DIFFIO_RX_R49p DIFFIO_TX_R50p	DIFFOUT_R49p DIFFOUT_R50p	J25	DQ4R	1	+	+
6A	VPEEDGANG					DILL OUT LYOUR	JZJ	D/GHV	1	1	
6A	VREFB6ANO	10	CI K5n			DIFFOLIT R49n	M21			1	
6A 6A	VREFB6AN0	10 10	CLK5n		DIFFIO_RX_R49n	DIFFOUT_R49n	M21	DO4R			
6A	VREFB6AN0	10 10 10	CLK5n			DIFFOUT_R49n DIFFOUT_R50n DIFFOUT_R51p	M21 J26 N24	DQ4R DQ4R			



											Note (
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
6A	VREFB6AN0	Ю			DIFFIO_RX_R51n	DIFFOUT_R51n	M24	DQ4R		DDI(G/DDI(E (E)	- LI DDIKE
βA	VREFB6AN0	Ю	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R52n	DIFFOUT_R52n	G26	DQ4R			
iA	VREFB6AN0	Ю			DIFFIO_RX_R53p	DIFFOUT_R53p	N23	DQS4R			
A	VREFB6AN0	Ю			DIFFIO_TX_R54p	DIFFOUT_R54p	G25				
A	VREFB6AN0	Ю			DIFFIO_RX_R53n	DIFFOUT_R53n	M22	DQSn4R			
A	VREFB6AN0				DIFFIO_TX_R54n	DIFFOUT_R54n	H25	DQ4R			
A	VREFB6AN0				DIFFIO_RX_R55p	DIFFOUT_R55p	M25	DQ4R			
iA	VREFB6AN0				DIFFIO_TX_R56p	DIFFOUT_R56p	D26	DQ4R			
SA .	VREFB6AN0	Ю			DIFFIO_RX_R55n	DIFFOUT_R55n	M26	DQ4R			
A	VREFB6AN0	Ю			DIFFIO_TX_R56n	DIFFOUT_R56n	E26				
A	VREFB6AN0	10	CLK4p,FPLL_TR_FBp		DIFFIO_RX_R57p	DIFFOUT_R57p	K25				
A	VREFB6AN0	10			DIFFIO_TX_R58p	DIFFOUT_R58p	E24	DQ5R			
4	VREFB6AN0		CLK4n,FPLL_TR_FBn		DIFFIO_RX_R57n	DIFFOUT_R57n	K26				
A	VREFB6AN0	10			DIFFIO_TX_R58n	DIFFOUT_R58n	E25	DQ5R			
4	VREFB6AN0	10			DIFFIO_RX_R59p	DIFFOUT_R59p	K24	DQ5R			
١	VREFB6AN0				DIFFIO_TX_R60p	DIFFOUT_R60p	F24	DQ5R			
4	VREFB6AN0				DIFFIO_RX_R59n	DIFFOUT_R59n	K23	DQ5R			
4	VREFB6AN0				DIFFIO_TX_R60n	DIFFOUT_R60n	G24	DQ5R			
4	VREFB6AN0	Ю			DIFFIO_RX_R61p	DIFFOUT_R61p	L23	DQS5R			
4	VREFB6AN0	Ю			DIFFIO_TX_R62p	DIFFOUT_R62p	H23				
4	VREFB6AN0				DIFFIO_RX_R61n	DIFFOUT_R61n	L24	DQSn5R			
١	VREFB6AN0			1	DIFFIO_TX_R62n	DIFFOUT_R62n	H24	DQ5R	1		
	VREFB6AN0			1	DIFFIO_RX_R63p	DIFFOUT_R63p	H22	DQ5R	1		
١	VREFB6AN0	10			DIFFIO_TX_R64p	DIFFOUT_R64p	F23	DQ5R			
١	VREFB6AN0	10		1	DIFFIO_RX_R63n	DIFFOUT_R63n	J23	DQ5R	1		
	VREFB6AN0	Ю			DIFFIO_TX_R64n	DIFFOUT_R64n	G22				
1	VREFB6AN0				DIFFIO_RX_R73p	DIFFOUT_R73p	L22				
١	VREFB6AN0				DIFFIO_TX_R74p	DIFFOUT_R74p	B25	DQ6R			
١	VREFB6AN0	Ю			DIFFIO_RX_R73n	DIFFOUT_R73n	K21				
١	VREFB6AN0	Ю			DIFFIO_TX_R74n	DIFFOUT_R74n	B26	DQ6R			
	VREFB6AN0				DIFFIO_RX_R75p	DIFFOUT_R75p	H19	DQ6R			
	VREFB6AN0	Ю			DIFFIO_TX_R76p	DIFFOUT_R76p	D25	DQ6R			
	VREFB6AN0	0			DIFFIO_RX_R75n	DIFFOUT_R75n	H20	DQ6R			
	VREFB6AN0				DIFFIO_TX_R76n	DIFFOUT_R76n	C25	DQ6R			
	VREFB6AN0	10			DIFFIO_RX_R77p	DIFFOUT_R77p	J20	DQS6R			
ı	VREFB6AN0	10			DIFFIO_TX_R78p	DIFFOUT_R78p	D22				
ı	VREFB6AN0	10			DIFFIO_RX_R77n	DIFFOUT_R77n	J21	DQSn6R			
ı	VREFB6AN0	10			DIFFIO_TX_R78n	DIFFOUT_R78n	E23	DQ6R			
4	VREFB6AN0	10			DIFFIO_RX_R79p	DIFFOUT_R79p	G20	DQ6R			
١	VREFB6AN0	10			DIFFIO_TX_R80p	DIFFOUT_R80p	E21	DQ6R			
ı	VREFB6AN0	10			DIFFIO_RX_R79n	DIFFOUT_R79n	F21	DQ6R			
١	VREFB6AN0	10			DIFFIO_TX_R80n	DIFFOUT_R80n	F22				
		GND					D23				
ı	VREFB7AN0	10			DIFFIO_RX_T9p	DIFFOUT_T9p	H15			GND	GND
	VREFB7AN0	Ю			DIFFIO_TX_T10p	DIFFOUT_T10p	C23	DQ1T	DQ1T	T_DM_4	T_DM_4
	VREFB7AN0	10			DIFFIO_RX_T9n	DIFFOUT_T9n	J16			GND	GND
	VREFB7AN0	Ю			DIFFIO_TX_T10n	DIFFOUT_T10n	C22	DQ1T	DQ1T	T_DQ_39	T_DQ_39
	VREFB7AN0	10			DIFFIO_RX_T11p	DIFFOUT_T11p	B24	DQ1T	DQ1T	T_DQ_37	T_DQ_37
	VREFB7AN0	Ю			DIFFIO_TX_T12p	DIFFOUT_T12p	A23	DQ1T	DQ1T	T_DQ_38	T_DQ_38
	VREFB7AN0	Ю			DIFFIO_RX_T11n	DIFFOUT_T11n	A24	DQ1T	DQ1T	T_DQ_36	T_DQ_36
	VREFB7AN0	10			DIFFIO_TX_T12n	DIFFOUT_T12n	A22	DQ1T	DQ1T	GND	GND
	VREFB7AN0	Ю			DIFFIO_RX_T13p	DIFFOUT_T13p	H18	DQS1T	DQS1T	T_DQS_4	T_DQS_4
	VREFB7AN0	Ю			DIFFIO_TX_T14p	DIFFOUT_T14p	B22			GND	GND
	VREFB7AN0	Ю			DIFFIO_RX_T13n	DIFFOUT_T13n	H17	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
	VREFB7AN0				DIFFIO_TX_T14n	DIFFOUT_T14n	A21	DQ1T	DQ1T	T_DQ_35	T_DQ_35
	VREFB7AN0	Ю			DIFFIO_RX_T15p	DIFFOUT_T15p	D21	DQ1T	DQ1T	T_DQ_33	T_DQ_33
	VREFB7AN0	Ю			DIFFIO_TX_T16p	DIFFOUT_T16p	B21	DQ1T	DQ1T	T_DQ_34	T_DQ_34
	VREFB7AN0				DIFFIO_RX_T15n	DIFFOUT_T15n	D20	DQ1T	DQ1T	T_DQ_32	T_DQ_32
	VREFB7AN0	Ю			DIFFIO_TX_T16n	DIFFOUT_T16n	B20			GND	GND
	VREFB7AN0				DIFFIO_RX_T17p	DIFFOUT_T17p	G16			GND	GND
	VREFB7AN0	Ю			DIFFIO_TX_T18p	DIFFOUT_T18p	C20	DQ2T	DQ1T	T_DM_3	T_DM_3
	VREFB7AN0	Ю			DIFFIO RX T17n	DIFFOUT_T17n	G17			GND	GND
	VREFB7AN0				DIFFIO_TX_T18n	DIFFOUT_T18n	B19	DQ2T	DQ1T	T_DQ_31	T_DQ_31
	VREFB7AN0	Ю			DIFFIO RX T19p	DIFFOUT_T19p	E20	DQ2T	DQ1T	T_DQ_29	T DQ 29
	VREFB7AN0				DIFFIO_TX_T20p	DIFFOUT_T20p	C19	DQ2T	DQ1T	T_DQ_30	T_DQ_30
	VREFB7AN0	Ю			DIFFIO_RX_T19n	DIFFOUT_T19n	E19	DQ2T	DQ1T	T_DQ_28	T_DQ_28
	VREFB7AN0	Ю			DIFFIO_TX_T20n	DIFFOUT_T20n	C18	DQ2T	DQ1T	GND	GND
	VREFB7AN0				DIFFIO_RX_T21p	DIFFOUT_T21p	J12	DQS2T	DQ1T	T_DQS_3	T_DQS_3
	VREFB7AN0			1	DIFFIO_TX_T22p	DIFFOUT_T22p	A19		1	GND	GND
	VREFB7AN0			İ	DIFFIO_RX_T21n	DIFFOUT_T21n	J11	DQSn2T	DQ1T	T_DQS#_3	T_DQS#_3
	VREFB7AN0		<u> </u>	1	DIFFIO_KX_12111	DIFFOUT T22n	A18	DQ3TZT	DQ1T	T DQ 27	T DQ 27
	VREFB7AN0	10		1	DIFFIO_TX_T22II	DIFFOUT_T23p	D18	DQ2T	DQ1T	T_DQ_25	T_DQ_25
	VREFB7AN0	10		†	DIFFIO_TX_T24p	DIFFOUT_T24p	A17	DQ2T	DQ1T	T_DQ_26	T_DQ_26
	VREFB7AN0 VREFB7AN0	0	 	1	DIFFIO_TX_T24p	DIFFOUT_T23n	D17	DQ2T	DQ1T DQ1T	T_DQ_26	T_DQ_26
	VREFB7AN0	0	<u> </u>	+	DIFFIO_TX_T24n	DIFFOUT_T24n	A16	DUZI	DQII	GND	GND
	I A LY EL DI WIND			+			H14	+	+		GND
<u> </u>	V/DEED74NA										
A A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T25p DIFFIO_TX_T26p	DIFFOUT_T25p DIFFOUT_T26p	H14 C17	DQ3T	DQ2T	GND T_DM_2	T_DM_2



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	10			DIFFIO_TX_T26n	DIFFOUT_T26n	B17	DQ3T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	10			DIFFIO_RX_T27p	DIFFOUT_T27p	E18	DQ3T	DQ2T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	10			DIFFIO_TX_T28p	DIFFOUT_T28p	A14	DQ3T	DQ2T	T_DQ_22	T_DQ_22
7A		10			DIFFIO_RX_T27n	DIFFOUT_T27n	F18	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	10			DIFFIO_TX_T28n	DIFFOUT_T28n	B14	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0				DIFFIO_RX_T29p	DIFFOUT_T29p	L12	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0				DIFFIO_TX_T30p	DIFFOUT_T30p	B15	DOG 47		T_RESET#	T_RESET#
7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_RX_T29n DIFFIO_TX_T30n	DIFFOUT_T29n DIFFOUT_T30n	K11 C15	DQSn3T DQ3T	DQSn2T DQ2T	T_DQS#_2 T_DQ_19	T_DQS#_2 T_DQ_19
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T30h DIFFIO_RX_T31p	DIFFOUT_T30h DIFFOUT_T31p	C15	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A 7A	VREFB7AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	A8	DQ3T	DQ2T	T_DQ_18	T_DQ_17
7A	VREFB7AN0				DIFFIO_TX_T32p	DIFFOUT_T31n	D15	DQ3T	DQ2T	T_DQ_16	T_DQ_16
7A	VREFB7AN0				DIFFIO_TX_T32n	DIFFOUT_T32n	A9	DQSI	DQZI	GND	GND
7A		10	CLK11p		DIFFIO_RX_T33p	DIFFOUT T33p	G15			ONE	0.15
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	C9	DQ4T	DQ2T	T_DM_1	T_DM_1
7A	VREFB7AN0	10	CLK11n		DIFFIO_RX_T33n	DIFFOUT_T33n	G14				
7A	VREFB7AN0	10			DIFFIO_TX_T34n	DIFFOUT_T34n	B9	DQ4T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	Ю			DIFFIO_RX_T35p	DIFFOUT_T35p	E16	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	10			DIFFIO_TX_T36p	DIFFOUT_T36p	D10	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	10			DIFFIO_RX_T35n	DIFFOUT_T35n	D16	DQ4T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	10			DIFFIO_TX_T36n	DIFFOUT_T36n	C10	DQ4T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0			ļ	DIFFIO_RX_T37p	DIFFOUT_T37p	N12	DQS4T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0			1	DIFFIO_TX_T38p	DIFFOUT_T38p	B10	DOG: 4T	DOOT	T_CKE_1	T_CKE_1
7A	VREFB7AN0			1	DIFFIO_RX_T37n	DIFFOUT_T37n	M12	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
7A 7A		IO IO		-	DIFFIO_TX_T38n	DIFFOUT_T38n	A11	DQ4T	DQ2T	T_DQ_11	T_DQ_11
7A 7A	VREFB7AN0 VREFB7AN0	.0	 	+	DIFFIO_RX_T39p DIFFIO_TX_T40p	DIFFOUT_T39p DIFFOUT_T40p	F16 E10	DQ4T DQ4T	DQ2T DQ2T	T_DQ_9 T_DQ_10	T_DQ_9 T_DQ_10
7A 7A	VREFB7AN0 VRFFB7AN0				DIFFIO_TX_T40p	DIFFOUT T39n	E10	DQ4T	DQ2T	T DQ 8	T_DQ_10
7A	VREFB7AN0				DIFFIO_TX_T40n	DIFFOUT_T40n	E13	DQ41	DQZI	GND	GND
7A	VREFB7AN0	10	CLK10p		DIFFIO_RX_T41p	DIFFOUT_T401	H12			GIND	GIND
7A	VREFB7AN0	10	DERTOP		DIFFIO_TX_T42p	DIFFOUT_T42p	B12	DQ5T		T_DM_0	T_DM_0
7A		10	CLK10n		DIFFIO_RX_T41n	DIFFOUT_T41n	G11	Dao.		1_50	
7A	VREFB7AN0	10			DIFFIO_TX_T42n	DIFFOUT_T42n	A13	DQ5T		T_DQ_7	T_DQ_7
7A	VREFB7AN0				DIFFIO_RX_T43p	DIFFOUT_T43p	G12	DQ5T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	Ю			DIFFIO_TX_T44p	DIFFOUT_T44p	A12	DQ5T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	Ю			DIFFIO_RX_T43n	DIFFOUT_T43n	F12	DQ5T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	Ю			DIFFIO_TX_T44n	DIFFOUT_T44n	B11	DQ5T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	10			DIFFIO_RX_T45p	DIFFOUT_T45p	M11	DQS5T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	10			DIFFIO_TX_T46p	DIFFOUT_T46p	C13			T_ODT_0	T_ODT_0
7A		10			DIFFIO_RX_T45n	DIFFOUT_T45n	L11	DQSn5T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	10			DIFFIO_TX_T46n	DIFFOUT_T46n	C12	DQ5T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	10			DIFFIO_RX_T47p	DIFFOUT_T47p	E13	DQ5T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	10			DIFFIO_TX_T48p	DIFFOUT_T48p	D11	DQ5T		T_DQ_2	T_DQ_2
7A	VREFB7AN0 VREFB7AN0		R7O 2		DIFFIO_RX_T47n DIFFIO_TX_T48n	DIFFOUT_T47n DIFFOUT_T48n	D13	DQ5T		T_DQ_0	T_DQ_0
7A		10						-			
8A 8A	VREFB8AN0 VREFB8AN0	10	CLK9p		DIFFIO_RX_T49p DIFFIO_TX_T50p	DIFFOUT_T49p DIFFOUT_T50p	N9 A5	DQ6T	-	T_A_0	T_CA_0
8A		10	CLK9n		DIFFIO_TX_T50p	DIFFOUT_T49n	M10	DQ61		1_A_0	I_CA_U
8A	VREFB8AN0	.0	CERSII		DIFFIO_RX_149II	DIFFOUT_T50n	B6	DQ6T		T_A_1	T_CA_1
8A		10			DIFFIO_RX_T51p	DIFFOUT_T51p	H8	DQ6T		T A 4	T CA 4
8A	VREFB8AN0	10	FPLL TL CLKOUT0,FPLL TL CLKOUTp,FPLL TL FB		DIFFIO_TX_T52p	DIFFOUT_T52p	A7	DQ6T		T_A_2	T_CA_2
8A		10			DIFFIO_RX_T51n	DIFFOUT_T51n	H9	DQ6T		T_A_5	T_CA_5
8A	VREFB8AN0	Ю	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	B7	DQ6T		T_A_3	T_CA_3
8A		10			DIFFIO_RX_T53p	DIFFOUT_T53p	M9	DQS6T		T_CK	T_CK
8A	VREFB8AN0	Ю			DIFFIO_TX_T54p	DIFFOUT_T54p	D6			T_A_6	T_CA_6
8A	VREFB8AN0	Ю			DIFFIO_RX_T53n	DIFFOUT_T53n	L9	DQSn6T		T_CK#	T_CK#
8A	VICEI DOMINO	Ю			DIFFIO_TX_T54n	DIFFOUT_T54n	E6	DQ6T		T_A_7	T_CA_7
8A	VREFB8AN0				DIFFIO_RX_T55p	DIFFOUT_T55p	H10	DQ6T		T_BA_1	_
8A	VREFB8AN0				DIFFIO_TX_T56p	DIFFOUT_T56p	D7	DQ6T		T_BA_0	
8A	VREFB8AN0	10			DIFFIO_RX_T55n	DIFFOUT_T55n	G10	DQ6T		T_BA_2	
8A	VREFB8AN0	10			DIFFIO_TX_T56n	DIFFOUT_T56n	C7			GND	GND
8A		10	CLK8p,FPLL_TL_FBp	ļ	DIFFIO_RX_T57p	DIFFOUT_T57p	L8		+	T 010"	
8A	VICEI DOMINO	10	CLKOn EDIT TI EDN	1	DIFFIO_TX_T58p	DIFFOUT_T58p	F6	DQ7T	+	T_CAS#	+
8A 8A	VREFB8AN0	10	CLK8n,FPLL_TL_FBn	 	DIFFIO_RX_T57n	DIFFOUT_T57n	K9	DOZT	+	T DAC#	+
8A 8A	VREFB8AN0 VREFB8AN0	IO IO	 	+	DIFFIO_TX_T58n DIFFIO_RX_T59p	DIFFOUT_T58n DIFFOUT_T59p	G6 K8	DQ7T DQ7T	+	T_RAS# T A 8	T_CA_8
8A	VREFB8AN0 VREFB8AN0	10			DIFFIO_RX_159p DIFFIO_TX_T60p	DIFFOUT_159p DIFFOUT_T60p	G7	DQ7T	1	T_A_10	1_UA_0
8A 8A		10			DIFFIO_TX_T60P	DIFFOUT_160P	J8	DQ/T	1	T_A_10	T CA 9
8A	VREFB8AN0 VREFB8AN0	.0		 	DIFFIO_RX_159n	DIFFOUT_159h DIFFOUT_T60n	J8 F7	DQ7T	+	T_A_9	1_UA_9
8A	VREFB8AN0		<u> </u>	<u> </u>	DIFFIO_TX_T61p	DIFFOUT_T61p	K10	DQS7T	+	T_CS#_0	T_CS#_0
8A		IO		1	DIFFIO_TX_T62p	DIFFOUT_T62p	H7	24011	1	T_A_12	00#_0
8A	VREFB8AN0	IO		1	DIFFIO_TX_T62p	DIFFOUT T61n	J10	DQSn7T	1	T_CS#_1	T_CS#_1
8A		10		1	DIFFIO_TX_T62n	DIFFOUT_T62n	J7	DQ7T		T_A_13	T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	L7	DQ7T		T_A_14	1
8A	VREFB8AN0	Ю			DIFFIO_TX_T64p	DIFFOUT_T64p	D8	DQ7T		T_WE#	1
8A		10			DIFFIO_RX_T63n	DIFFOUT_T63n	K6	DQ7T		T_A_15	1
8A		IO			DIFFIO_TX_T64n	DIFFOUT_T64n	E9			GND	GND
9A		MSEL0		MSEL0	_		M7				



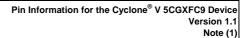


											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
9A		CONF_DONE		CONF_DONE			A6			DDI(3)DDI(E (2)	LIDDINZ
9A		MSEL1		MSEL1			L6				
9A		nSTATUS		nSTATUS			B5				
9A		nCE		nCE			D5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			K5				
9A		nCONFIG		nCONFIG			F5				
9A		MSEL4		MSEL4			J5				
9A		GND					H5				
		GND		İ			E7				
		GND					G5				
		GND					C11				
		GND					D14				
		GND					E17				
		GND		İ			F20				
		GND					G23				
		GND					L25				
		GND					N21				
		GND					P24				
		GND					P19				
		GND					T20				
		GND			1		U23	1	1	1	1
		GND		†	†		Y22	1	1	†	t
		GND		†	†		AA15	1	1	†	t
		GND		†	†		AE17	1	1	†	t
		GND		<u> </u>	<u> </u>		AD14	1	1	<u> </u>	f
		GND					M8				†
		GND	 	 	t		A25			t	F
		GND	 	 	t		D24			t	F
		GND	 	 	t		H26			t	F
		GND		†			V26				
		GND		†			AA25				
		GND					AC26				
		GND		+	+		AF25			+	
		GND		+	+		K22			+	
		GND GND					AD24 C21				
		GND					L20				
		GND					K19 M19				
		GND									
		GND					W19				
		GND GND					AC21				
							AF20				
		GND					B18 L18				
		GND					K17				
		GND					K17				
		GND GND					J18 N18				
		GND					M17				
		GND		 	 		R18			 	
		GND		 	 		P17			 	
		GND		 	 		AB18	-	-	 	
		GND		 	 		A15	-	-	 	
		GND		 	 		H16	-	-	 	
		GND		 	 		L16			 	
		GND		1	 		L14	 	 	 	
		GND		 	 		K15			 	
		GND		 	 		J14			 	
		GND		1	 		N16	 	 	 	
		GND		1	 		N14	 	 	 	
		GND		_	-		M15	ļ	ļ	-	
		GND	ļ		-		T15	ļ	ļ	-	
		GND		_	-		R16	ļ	ļ	-	
		GND		_	-		R14	ļ	ļ	-	
		GND	ļ		-		P15	ļ	ļ	-	
		GND					V16				
		GND	ļ				G13				
		GND	ļ				K13				
		GND		ļ	ļ		K12			ļ	
		GND					M13				
		GND		ļ	Ļ		R12			Ļ	
		GND		ļ	ļ		P13			ļ	
		GND		ļ	ļ		U13			ļ	1
		GND		ļ	Ļ		Y12			Ļ	
		GND		ļ	Ļ		F10			Ļ	
		GND		ļ	ļ		L10			ļ	
		GND		ļ			J9				
		GND	1				N11				



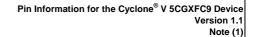


										Note (1)
Bank Number		Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel		DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
	GND					T10				
	GND					P9				
	GND					W9				
	GND					AC11				
	GND GND					AF10 B8				
	GND					H6				
	GND					N6				
	GND					R7				
	GND					P7				
	GND					AB8				
	GND					AE7				
	GND					C5				
	GND					B4				
	GND					F4				
	GND					E5				
	GND					D4				
	GND					H4				
	GND					L4				
	GND					J4				
	GND			-		N4	-			
	GND		1	 		M5	 	1	1	
 	GND	 	+	 	1	T5 R4	 	-	-	-
	GND GND		+	 		P5	 	1	1	
	GND					V5				
	GND		†	-	İ	V5 V4	 			
	GND					U4				
	GND					AA5				
	GND					Y4				
	GND					W5				
	GND					AC5				
	GND					AB4				
	GND					AF4				
	GND					AE5				
	GND					AD4				
	GND					C2				
	GND					C1				
	GND					B3				
	GND					B2				
	GND			-		F3 E2				
	GND GND					E2				
	GND					D3				
	GND					H3				
	GND					G2				
	GND					G2 G1				
	GND					L2				
	GND					L1				
	GND					K3				
	GND					J2				
	GND					J1				
	GND					N2				
	GND					N1				
	GND			ļ		M3				
	GND					T3				
	GND		ļ	-		R2		ļ		
	GND			-		R1	-			
	GND			-		P3	-			
 	GND GND	 	+	 	1	V3	 	-	-	-
	GND		+	—		U2 U1	—	-	-	-
	GND		 	† 	1	AA2	† 	1	1	
	GND	<u> </u>	-	t	 	AA2 AA1	t			
	GND		†	-	İ	Y3	 			
	GND		1	†		W2	†		1	
	GND			1		W1	1			
	GND			İ		AC2	İ			
	GND					AC1				
	GND					AB3				
	GND					AF3				
	GND					AF2				
	GND					AE2				
	GND					AE1				
	GND					AD3				
	VCC					J19				
	VCC					L19			ļ	
	VCC					K20				L





											Note (1)
3ank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCC					N19			DDITO, DDITE (2)	
		VCC					M20				
		VCC					R19				
		VCC					L17				
		VCC					K18				
		VCC					J17				
		VCC					N17				<u> </u>
		VCC		†			M18				
		VCC		†			T18				
		VCC		†			R17				
		VCC		+	+		P18				
				-							
		VCC					L15				
		VCC					K16				
		VCC					K14				
		VCC					J15				
		VCC					N15				
		VCC					M16				
		VCC					M14				
		VCC					T16				
		VCC					T14				
		VCC		ļ	ļ		R15]			1
		VCC					P16				
		VCC					P14				
		VCC					L13				
		VCC					J13				
		VCC	<u> </u>				N13				
		VCC					R13				
		DNU					A4				
		DNU					A3				
		DNU		İ			AB7				
		DNU		İ			AA12				
		DNU					C24				
		DNU					F14				
		VCCPGM					AA9				
		VCCPGM					W22				
		VCCPGM					F8				<u> </u>
		VCCBAT					E8				<u> </u>
		VCCIO3A					Y7				<u> </u>
		VCCIO3A VCCIO3A		†			AC6				
		VCCIO3A VCCIO3B		†			V11				
		VCCIO3B VCCIO3B		+	+		AA10				
		VCCIO3B		-			AD9				
		VCCIO3B					U8				
		VCCIO3B									
		VCCIO4A VCCIO4A					U18 AE22				
		VCCIO4A					AA20				
		VCCIO4A					AD19				
		VCCIO4A					Y17				
		VCCIO4A					W14				
		VCCIO4A					AC16				
		VCCIO4A	1	ļ	Ļ		AF15				
		VCCIO4A					AB13				
		VCCIO4A					AE12				
		VCCIO5A					V21				
		VCCIO5A					AB23				
		VCCIO5B	<u> </u>				N26				
		VCCIO5B	<u> </u>				T25				
		VCCIO5B					W24				
		VCCIO5B					R22				
		VCCIO6A					C26				
		VCCIO6A					F25				
		VCCIO6A		İ	İ		J24				
		VCCIO6A		Ì	İ		E22				
		VCCIO6A		1	1		M23				t
		VCCIO6A			1		H21		1		
		VCCIO7A					B23	1		1	
		VCCIO7A					A20				
		VCCIO7A VCCIO7A	<u> </u>	 	 		D19	1			
		VCCIO7A VCCIO7A		 	 		G18				
		VCCIO7A VCCIO7A		 	 		C16	1	1	1	+
		VCCIO7A VCCIO7A		 	 		F15		1	1	
		VCCIO7A VCCIO7A		 	 		B13		1	1	
			+	-	-		D13	 		-	
		VCCIO7A		 	 		E12	-		1	
		VCCIO7A		 	 		A10				
		VCCIO7A	ļ	+	1		H11	ļ	ļ	1	+
		VCCIO8A			-		C6	-	ļ	ļ	
		VCCIO8A					D9				
		VCCIO8A		l .	1		G8				





lank lumber			Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCIO8A					K7				
		VCCPD3A					AB9				
		VCCPD3B4A					AA17				
		VCCPD3B4A					AA11				
		VCCPD3B4A					AA19				
		VCCPD3B4A					AB21				
		VCCPD3B4A					AA13				
		VCCPD5A					U21				
		VCCPD5B					N22				
		VCCPD5B					R21				
		VCCPD6A					J22				
		VCCPD6A					L21				
		VCCPD7A8A					F19				
		VCCPD7A8A					F17				
		VCCPD7A8A					F13				
		VCCPD7A8A					F11				
		VCCPD7A8A					F9				
1	VREFB3AN0	VREFB3AN0					AC7				
3	VREFB3BN0	VREFB3BN0					AC12				
1	VREFB4AN0	VREFB4AN0					AD15				
١	VREFB5AN0	VREFB5AN0					W23				
3	VREFB5BN0	VREFB5BN0					P25				
		VREFB6AN0					L26				
A	VREFB7AN0	VREFB7AN0					B16				
\		VREFB8AN0					C8				
		VCCH_GXBL					R3				
		VCCH_GXBL					T4				
		VCCH_GXBL					L3				
		VCCL GXBL					J3				
		VCCL GXBL					N3				
		VCCL GXBL					U3				
		RREF_TL					B1				
		VCCA FPLL					W7				
		VCCA_FPLL					J6			İ	İ
		VCCA_FPLL					Y21			İ	İ
		VCCA_FPLL					G21			İ	İ
		VCC_AUX					G9			İ	İ
		VCC_AUX					E14			İ	İ
		VCC_AUX					G19			İ	İ
		VCC_AUX					AB20		İ		İ
		VCC_AUX					AB14			İ	İ
		VCC_AUX					AA8			İ	İ
		VCCE_GXBL					U5				
		VCCE_GXBL					K4				
		VCCE_GXBL					N5			1	1
		VCCE_GXBL					M4			1	1
		VCCE_GXBL		1			R5	i		1	1
		VCCE_GXBL				1	P4	†	1	1	1

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the
<u>Cyclone V Device Family Pin Connection Guidelines</u>,

(2) RESET pin is only applicable for DDR3 device.

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											Note (1		
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2		
GXB_L3		REFCLK3Ln					L7						
SXB_L3		REFCLK3Lp					K8						
SXB_L3		GXB_TX_L11n					D3						
SXB_L3		GXB_TX_L11p					D4						
SXB_L3		GXB_RX_L11p,GXB_REFCLK_L11p					E2						
GXB_L3		GXB_RX_L11n,GXB_REFCLK_L11n					E1						
GXB_L3		GXB_TX_L10n					F3						
SXB_L3		GXB_TX_L10p					F4						
GXB_L3 GXB_L3		GXB_RX_L10p,GXB_REFCLK_L10p		-			G2 G1				+		
SXB_L3		GXB_RX_L10n,GXB_REFCLK_L10n GXB_TX_L9n					H3						
SXB_L3		GXB_TX_L9n GXB_TX_L9p					H3 H4						
SXB_L3		GXB_RX_L9p,GXB_REFCLK_L9p		1			J2						
GXB_L3		GXB_RX_L9n,GXB_REFCLK_L9n		+			J1						
SXB_L3		GXB_TX_L8n					K3						
GXB_L2		GXB_TX_L8p					K4						
GXB_L2		GXB_RX_L8p,GXB_REFCLK_L8p					L2						
SXB L2		GXB_RX_L8n,GXB_REFCLK_L8n		1			L1						
GXB_L2		GXB_TX_L7n		1			M3						
GXB_L2		GXB_TX_L7p					M4						
GXB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					N2						
GXB_L2		GXB_RX_L7n,GXB_REFCLK_L7n					N1						
GXB_L2		GXB_TX_L6n				-	P3						
GXB_L2		GXB_TX_L6p		1			P4						
GXB_L2		GXB_RX_L6p,GXB_REFCLK_L6p					R2						
SXB_L2		GXB_RX_L6n,GXB_REFCLK_L6n					R1		ļ				
SXB_L2		REFCLK2Lp					P8						
GXB_L2		REFCLK2Ln					N7						
GXB_L1		REFCLK1Ln		-			R7 R8				+		
GXB_L1 GXB_L1		REFCLK1Lp GXB_TX_L5n		-			T3						
SXB_L1		GXB_TX_L5n GXB_TX_L5p					T4						
SXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p		1			U2						
SXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n		+			U1						
GXB_L1		GXB_TX_L4n					V3						
GXB_L1		GXB_TX_L4p					V4						
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p		1			W2						
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n		1			W1						
GXB_L1		GXB_TX_L3n					Y3						
GXB_L1		GXB_TX_L3p					Y4						
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					AA2						
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					AA1						
SXB_L0		GXB_TX_L2n					AB3						
GXB_L0		GXB_TX_L2p					AB4						
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AC2						
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AC1						
GXB_L0		GXB_TX_L1n					AD3						
SXB_L0		GXB_TX_L1p		-			AD4				+		
SXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p		-			AE2				+		
GXB_L0 GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n GXB_TX_L0n					AE1 AF3						
SXB_L0		GXB_TX_L0p		1			AF4						
SXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p		1		<u> </u>	AG2		†	+	+		
SXB LO	1	GXB_RX_L0n,GXB_REFCLK_L0n		†	<u> </u>		AG2 AG1	<u> </u>	†				
SXB_L0		REFCLK0Lp			1		W8		1				
SXB_L0		REFCLK0Ln		İ	1		W7	1	1				
BA .		TDO		TDO			W9		Ì				
BA		nCSO		DATA4			AA7		l				
BA		TMS		TMS			V7						
BA		AS_DATA3		DATA3			AB7						
3A		TCK		TCK			AC7						
BA		AS_DATA2		DATA2			AE7						
BA		TDI		TDI			U7		ļ	1	1		
BA		AS_DATA1		DATA1			AE5		ļ				
BA		DCLK		DCLK			T7		ļ				
BA		AS_DATA0,ASDO		DATA0		DIFFOUR D	AG5	2012	ļ				
BA	VICEI DOMINO	10		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	U12	DQ1B	 	1	1		
BA .	VREFB3AN0			DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AA10	DOID	 		1		
BA BA		10		DATA8 DATA7	DIFFIO_RX_B1p DIFFIO_TX_B2p	DIFFOUT_B1p	U11	DQ1B	 	+	+		
BA BA		10	+			DIFFOUT_B2p	Y10	DQ1B DQSn1B	1	+	+		
BA BA	VREFB3AN0 VREFB3AN0	10	+	DATA10 DATA9	DIFFIO_RX_B3n DIFFIO_TX_B4n	DIFFOUT_B3n DIFFOUT_B4n	Y11 AD9	DQSn1B DQ1B	1	+	+		
BA	VREFB3AN0 VREFB3AN0			DATA12	DIFFIO_IX_B4n DIFFIO_RX_B3p	DIFFOUT_B3p	AA11	DQ1B DQS1B	†	-	-		
BA BA	VREFB3AN0 VREFB3AN0		<u>†</u>	DATA12 DATA11	DIFFIO_RX_B3p DIFFIO_TX_B4p	DIFFOUT_B3p DIFFOUT_B4p	AA11 AC9	סופאת	1	+	+		
BA	VREFB3AN0 VREFB3AN0	10	1	DATA11 DATA14	DIFFIO_TX_B4p	DIFFOUT_B5n	R10	DQ1B	 	1	1		
BA		10		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	W10	DQ1B	†	+	+		
BA		10		CLKUSR	DIFFIO_TX_B6II	DIFFOUT_B5p	T11	DQ1B	1	1	1		
BA .	VREFB3AN0		†	DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V9	DQ1B	†	+	+		
	20,0		1		Dop				1				



											Note
ank umber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for	HMC Pin Assignment fo
	VREFB3AN0	10		PR_DONE	DIFFIO RX B7n	DIFFOUT_B7n	V10			DDR3/DDR2 (2)	LPDDR2
	VREFB3AN0			PR READY	DIFFIO TX B8n	DIFFOUT B8n	AF6	DQ1B			+
	VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	V11	54.5			+
	VREFB3AN0	Ю			DIFFIO_TX_B8p	DIFFOUT_B8p	AF7	DQ1B			
	VREFB3AN0	Ю			DIFFIO_TX_B9n	DIFFOUT_B9n	AB9				1
	VREFB3AN0	Ю			DIFFIO_RX_B10n	DIFFOUT_B10n	AH6	DQ2B			
	VREFB3AN0	Ю			DIFFIO_TX_B9p	DIFFOUT_B9p	AA9	DQ2B			
	VREFB3AN0	Ю			DIFFIO_RX_B10p	DIFFOUT_B10p	AG6	DQ2B			
	VREFB3AN0	Ю			DIFFIO_RX_B11n	DIFFOUT_B11n	U8	DQSn2B			
	VREFB3AN0				DIFFIO_TX_B12n	DIFFOUT_B12n	AG8	DQ2B			
	VREFB3AN0				DIFFIO_RX_B11p	DIFFOUT_B11p	T9	DQS2B			
	VREFB3AN0	10			DIFFIO_TX_B12p	DIFFOUT_B12p	AF8				
	VREFB3AN0	10			DIFFIO_TX_B13n	DIFFOUT_B13n	AB8	DQ2B			
	VREFB3AN0				DIFFIO_RX_B14n	DIFFOUT_B14n	AH5	DQ2B	_		
	VILLI DOMINO	10			DIFFIO_TX_B13p	DIFFOUT_B13p	AA8	DQ2B			
	VREFB3AN0	10		+	DIFFIO_RX_B14p	DIFFOUT_B14p	AH4	DQ2B			
	VREFB3AN0 VREFB3AN0	10		-	DIFFIO_RX_B15n DIFFIO_TX_B16n	DIFFOUT_B15n DIFFOUT_B16n	U9 AH7	DQ2B	+	+	
	VREFB3AN0 VREFB3AN0	.0		-	DIFFIO_TX_B16n DIFFIO_RX_B15p	DIFFOUT_B15p	T10	DQZB	+	+	
	VREFB3AN0			+	DIFFIO_TX_B16p	DIFFOUT B16p	AG7	DQ2B			
	VILLI DOMINO	10	 	†	DIFFIO_TX_B16p	DIFFOUT_B16p DIFFOUT_B25n	AF10	DUZD	+	+	+
	VREFB3BN0			+	DIFFIO_TX_B25II	DIFFOUT_B26n	AD13	DQ3B	DQ1B	+	+
	VREFB3BN0	IO		+	DIFFIO_TX_B25p	DIFFOUT B25p	AE10	DQ3B	DQ1B	1	+
	VREFB3BN0	Ю		1	DIFFIO_TX_B25p	DIFFOUT_B26p	AD12	DQ3B	DQ1B	1	1
	VREFB3BN0	Ю			DIFFIO_RX_B27n	DIFFOUT_B27n	W12	DQSn3B	DQ1B		1
	VREFB3BN0	Ю			DIFFIO_TX_B28n	DIFFOUT_B28n	AJ2	DQ3B	DQ1B		1
	VREFB3BN0	Ю		İ	DIFFIO_RX_B27p	DIFFOUT_B27p	V12	DQS3B	DQ1B	1	1
	VREFB3BN0	Ю	İ	1	DIFFIO_TX_B28p	DIFFOUT_B28p	AJ1	1	1		1
	VREFB3BN0	Ю		1	DIFFIO_TX_B29n	DIFFOUT_B29n	AK3	DQ3B	DQ1B		1
	VREFB3BN0	Ю			DIFFIO_RX_B30n	DIFFOUT_B30n	AE13	DQ3B	DQ1B		
	VREFB3BN0	Ю			DIFFIO_TX_B29p	DIFFOUT_B29p	AJ3	DQ3B	DQ1B		
	VREFB3BN0	Ю			DIFFIO_RX_B30p	DIFFOUT_B30p	AE12	DQ3B	DQ1B		
	VREFB3BN0				DIFFIO RX B31n	DIFFOUT_B31n	AB13				
	VREFB3BN0	Ю			DIFFIO_TX_B32n	DIFFOUT_B32n	AJ5	DQ3B	DQ1B		
	VREFB3BN0	Ю			DIFFIO_RX_B31p	DIFFOUT_B31p	AB12				
	VREFB3BN0	Ю			DIFFIO_TX_B32p	DIFFOUT_B32p	AJ4	DQ3B	DQ1B		
	VREFB3BN0	10			DIFFIO_TX_B33n	DIFFOUT_B33n	AK6			GND	GND
	VREFB3BN0	10			DIFFIO_RX_B34n	DIFFOUT_B34n	AG12	DQ4B	DQ1B	B_A_15	
	VREFB3BN0	Ю			DIFFIO_TX_B33p	DIFFOUT_B33p	AK5	DQ4B	DQ1B	B_WE#	
	VREFB3BN0	0			DIFFIO_RX_B34p	DIFFOUT_B34p	AF13	DQ4B	DQ1B	B_A_14	
	VILLI DODING	Ю			DIFFIO_RX_B35n	DIFFOUT_B35n	AA13	DQSn4B	DQSn1B	B_CS#_1	B_CS#_1
	VREFB3BN0	Ю			DIFFIO_TX_B36n	DIFFOUT_B36n	AK7	DQ4B	DQ1B	B_A_13	
	VREFB3BN0	Ю			DIFFIO_RX_B35p	DIFFOUT_B35p	Y12	DQS4B	DQS1B	B_CS#_0	B_CS#_0
	VREFB3BN0	10			DIFFIO_TX_B36p	DIFFOUT_B36p	AJ7			B_A_12	
	VREFB3BN0	10			DIFFIO_TX_B37n	DIFFOUT_B37n	AK8	DQ4B	DQ1B	B_A_11	
	VILLI BOBITO	10			DIFFIO_RX_B38n	DIFFOUT_B38n	AG11	DQ4B	DQ1B	B_A_9	B_CA_9
	VREFB3BN0	10			DIFFIO_TX_B37p	DIFFOUT_B37p	AJ8	DQ4B	DQ1B	B_A_10	
	VREFB3BN0	10			DIFFIO_RX_B38p	DIFFOUT_B38p	AF11	DQ4B	DQ1B	B_A_8	B_CA_8
	VREFB3BN0	10	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	AC14				
	VREFB3BN0				DIFFIO_TX_B40n	DIFFOUT_B40n	AG9	DQ4B	DQ1B	B_RAS#	
	VREFB3BN0		CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p	DIFFOUT_B39p	AB14	0.010	0.010		
	VREFB3BN0			+	DIFFIO_TX_B40p	DIFFOUT_B40p	AF9	DQ4B	DQ1B	B_CAS#	OND
	VREFB3BN0 VREFB3BN0			+	DIFFIO_TX_B41n DIFFIO_RX_B42n	DIFFOUT_B41n DIFFOUT_B42n	AJ9 AJ10	DQ5B	+	GND B BA 2	GND
	VREFB3BN0 VREFB3BN0			+			AJ10 AH9	DQ5B DQ5B	+		+
	VREFB3BN0 VREFB3BN0	2		+	DIFFIO_TX_B41p DIFFIO_RX_B42p	DIFFOUT_B41p DIFFOUT_B42p	AH10	DQ5B DQ5B	+	B_BA_0 B_BA_1	+
	VREFB3BN0 VREFB3BN0	0	1	+	DIFFIO_RX_B42p	DIFFOUT_B42p DIFFOUT_B43n	AA14	DQ5B DQSn5B	+	B_BA_1 B_CK#	B_CK#
	VREFB3BN0	10	 	+	DIFFIO_TX_B44n	DIFFOUT_B44n	AK11	DQ5B	+	B_A_7	B_CA_7
	VREFB3BN0	10		+	DIFFIO_TX_B44II	DIFFOUT B43p	Y13	DQS5B	+	B CK	B CK
	VREFB3BN0	IO		†	DIFFIO_TX_B44p	DIFFOUT_B43p	AK10	24000	†	B A 6	B CA 6
	VREFB3BN0	Ю	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO TX B45n	DIFFOUT B45n	AH12	DQ5B	1	B A 3	B CA 3
	VREFB3BN0				DIFFIO_RX_B46n	DIFFOUT_B46n	AG14	DQ5B	1	B_A_5	B CA 5
	VREFB3BN0		FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AH11	DQ5B	1	B_A_2	B_CA_2
	VREFB3BN0			1	DIFFIO_RX_B46p	DIFFOUT_B46p	AG13	DQ5B	1	B A 4	B CA 4
	VREFB3BN0	Ю	CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	AA15				
	VREFB3BN0	Ю			DIFFIO_TX_B48n	DIFFOUT_B48n	AK12	DQ5B	İ	B_A_1	B_CA_1
	VREFB3BN0	Ю	CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	Y15				T
	VREFB3BN0	Ю			DIFFIO_TX_B48p	DIFFOUT_B48p	AJ12	DQ5B		B_A_0	B_CA_0
	VREFB4AN0		RZQ_0		DIFFIO_TX_B49n	DIFFOUT_B49n	AK13		İ		
	VREFB4AN0	Ю			DIFFIO_RX_B50n	DIFFOUT_B50n	AF15	DQ6B		B_DQ_0	B_DQ_0
		Ю			DIFFIO_TX_B49p	DIFFOUT_B49p	AJ14	DQ6B		B_DQ_2	B_DQ_2
	VREFB4AN0	Ю			DIFFIO_RX_B50p	DIFFOUT_B50p	AE16	DQ6B		B_DQ_1	B_DQ_1
	VREFB4AN0	Ю			DIFFIO_RX_B51n	DIFFOUT_B51n	AA16	DQSn6B		B_DQS#_0	B_DQS#_0
	VREFB4AN0				DIFFIO_TX_B52n	DIFFOUT_B52n	AH15	DQ6B		B_DQ_3	B_DQ_3
	VREFB4AN0	Ю			DIFFIO_RX_B51p	DIFFOUT_B51p	Y16	DQS6B		B_DQS_0	B_DQS_0
		10			DIFFIO_TX_B52p	DIFFOUT_B52p	AH14			B_ODT_0	B_ODT_0
_		10			DIFFIO_TX_B53n	DIFFOUT_B53n	AK15	DQ6B		B_ODT_1	B_ODT_1
	VREFB4AN0	Ю			DIFFIO_RX_B54n	DIFFOUT_B54n	AE17	DQ6B		B_DQ_4	B_DQ_4



											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	10			DIFFIO_TX_B53p	DIFFOUT_B53p	AJ15	DQ6B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	10			DIFFIO_RX_B54p	DIFFOUT_B54p	AD17	DQ6B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	AC15				
4A	VREFB4AN0	Ю			DIFFIO_TX_B56n	DIFFOUT_B56n	AF14	DQ6B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	Ю	CLK2p		DIFFIO_RX_B55p	DIFFOUT_B55p	AB16				
4A	VREFB4AN0				DIFFIO_TX_B56p	DIFFOUT_B56p	AE15	DQ6B		B_DM_0	B_DM_0
4A	VREFB4AN0				DIFFIO_TX_B57n	DIFFOUT_B57n	AH17			GND	GND
4A 4A	VREFB4AN0 VRFFB4AN0				DIFFIO_RX_B58n DIFFIO_TX_B57n	DIFFOUT_B58n DIFFOUT_B57p	AK17 AG17	DQ7B DQ7B	DQ2B DQ2B	B_DQ_8 B_DQ_10	B_DQ_8 B_DQ_10
4A 4A	VREFB4AN0 VRFFB4AN0	10			DIFFIO_TX_B57p DIFFIO_RX_B58p	DIFFOUT_B57p DIFFOUT_B58p	AK16	DQ7B DQ7B	DQ2B DQ2B	B_DQ_10 B_DQ_9	B_DQ_10 B_DQ_9
4A 4A	VREFB4AN0	10			DIFFIO_RX_B59n	DIFFOUT_B59n	Y18	DQ7B DQSn7B	DQ2B	B_DQS#_1	B_DQ_9 B_DQS#_1
4A	VREFB4AN0	IO .			DIFFIO_TX_B60n	DIFFOUT_B60n	AJ18	DQ3II/B DQ7B	DQ2B	B_DQ_11	B_DQ3#_1
4A	VREFB4AN0	IO.			DIFFIO_RX_B59p	DIFFOUT_B59p	Y17	DQS7B	DQ2B	B_DQS_1	B_DQS_1
4A	VRFFB4AN0				DIFFIO TX B60p	DIFFOUT_B60p	A.J17	540.5	DQLD	B CKF 1	B CKF 1
4A	VREFB4AN0	10			DIFFIO_TX_B61n	DIFFOUT_B61n	AK18	DQ7B	DQ2B	B CKE 0	B CKE 0
4A	VREFB4AN0	Ю			DIFFIO_RX_B62n	DIFFOUT_B62n	AG16	DQ7B	DQ2B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AJ19	DQ7B	DQ2B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AF16	DQ7B	DQ2B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	AB18				
4A	VREFB4AN0	Ю			DIFFIO_TX_B64n	DIFFOUT_B64n	AH20	DQ7B	DQ2B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	10	CLK3p		DIFFIO_RX_B63p	DIFFOUT_B63p	AB17	ļ	L	1	
4A	VREFB4AN0				DIFFIO_TX_B64p	DIFFOUT_B64p	AH19	DQ7B	DQ2B	B_DM_1	B_DM_1
4A	VREFB4AN0				DIFFIO_TX_B65n	DIFFOUT_B65n	AK20	DOOD	DOOD	GND D. DO. 40	GND D. DO. 40
4A	VREFB4AN0	IO IO		-	DIFFIO_RX_B66n	DIFFOUT_B66n	AE18	DQ8B	DQ2B	B_DQ_16	B_DQ_16
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_TX_B65p DIFFIO_RX_B66p	DIFFOUT_B65p DIFFOUT_B66p	AJ20 AD18	DQ8B DQ8B	DQ2B DQ2B	B_DQ_18 B_DQ_17	B_DQ_18 B_DQ_17
4A 4A	VREFB4AN0 VRFFB4AN0	10			DIFFIO_RX_B66p	DIFFOUT B66p	AA20	DQ8B DQSn8B	DQ2B DQSn2B	B_DQ_17 B_DQS#_2	B_DQ_17 B_DQS#_2
4A 4A	VREFB4AN0 VRFFB4AN0				DIFFIO_RX_B67n DIFFIO_TX_B68n	DIFFOUT_B68n	AK22	DQSR8B DQ8B	DQSn2B DQ2B	B_DQS#_2 B_DQ_19	B_DQS#_2 B_DQ_19
4A 4A	VREFB4AN0				DIFFIO_TX_B67p	DIFFOUT_B66fp	Y20	DQ88B	DQS2B	B_DQS_2	B_DQ_19 B_DQS_2
4A	VREFB4AN0	IO .			DIFFIO_TX_B68p	DIFFOUT_B68p	AK21	DQS0B	DQ32B	B_RESET#	B_BQS_2 B_RESET#
4A	VREFB4AN0	10			DIFFIO_TX_B69n	DIFFOUT_B69n	AJ22	DQ8B	DQ2B	GND	GND
4A	VREFB4AN0	10			DIFFIO_RX_B70n	DIFFOUT_B70n	AF19	DQ8B	DQ2B	B DQ 20	B DQ 20
4A	VREFB4AN0	10			DIFFIO_TX_B69p	DIFFOUT_B69p	AH21	DQ8B	DQ2B	B DQ 22	B DQ 22
4A	VREFB4AN0	Ю			DIFFIO_RX_B70p	DIFFOUT_B70p	AF18	DQ8B	DQ2B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	Ю			DIFFIO_RX_B71n	DIFFOUT_B71n	AA19			GND	GND
4A	VREFB4AN0	Ю			DIFFIO_TX_B72n	DIFFOUT_B72n	AK23	DQ8B	DQ2B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AA18			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AJ23	DQ8B	DQ2B	B_DM_2	B_DM_2
4A	VREFB4AN0				DIFFIO_TX_B73n	DIFFOUT_B73n	AJ24			GND	GND
4A	VREFB4AN0	Ю			DIFFIO_RX_B74n	DIFFOUT_B74n	AG19	DQ9B	DQ3B	B_DQ_24	B_DQ_24
4A	VREFB4AN0	10			DIFFIO_TX_B73p	DIFFOUT_B73p	AH24	DQ9B	DQ3B	B_DQ_26	B_DQ_26
4A	VREFB4AN0	10			DIFFIO_RX_B74p	DIFFOUT_B74p	AG18	DQ9B	DQ3B	B_DQ_25	B_DQ_25
4A	VREFB4AN0	10			DIFFIO_RX_B75n	DIFFOUT_B75n	AC19	DQSn9B	DQ3B	B_DQS#_3	B_DQS#_3
4A	VREFB4AN0 VRFFB4AN0				DIFFIO_TX_B76n DIFFIO_RX_B75n	DIFFOUT_B76n DIFFOUT_B75p	AK25 AB19	DQ9B	DQ3B	B_DQ_27	B_DQ_27
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B75p DIFFIO_TX_B76p			DQS9B	DQ3B	B_DQS_3	B_DQS_3
4A 4A		io			DIFFIO_TX_B76p DIFFIO_TX_B77n	DIFFOUT_B76p DIFFOUT_B77n	AJ25 AH25	DQ9B	DQ3B	GND GND	GND GND
4A 4A	VREFB4AN0	10			DIFFIO_TX_B78n	DIFFOUT_B78n	AE20	DQ9B DQ9B	DQ3B	B DQ 28	B DQ 28
4A	VREFB4AN0	IO .			DIFFIO_TX_B77p	DIFFOUT_B77p	AG24	DQ9B	DQ3B	B_DQ_28	B_DQ_28
44	VREFR4ANO	IO.			DIFFIO_RX_B78p	DIFFOUT B78p	AD19	DQ9B	DQ3B	B DQ 29	B DQ 29
4A	VREFB4AN0	10			DIFFIO_RX_B79n	DIFFOUT_B79n	AB21	5405	DGOD	GND	GND
4A	VREFB4AN0	Ю			DIFFIO_TX_B80n	DIFFOUT_B80n	AK26	DQ9B	DQ3B	B_DQ_31	B_DQ_31
4A	VREFB4AN0	Ю			DIFFIO_RX_B79p	DIFFOUT_B79p	AA21		1	GND	GND
4A	VREFB4AN0	Ю			DIFFIO_TX_B80p	DIFFOUT_B80p	AJ27	DQ9B	DQ3B	B_DM_3	B_DM_3
4A	VREFB4AN0				DIFFIO_TX_B81n	DIFFOUT_B81n	AK28			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B82n	DIFFOUT_B82n	AG21	DQ10B	DQ3B	B_DQ_32	B_DQ_32
4A	VREFB4AN0	10			DIFFIO_TX_B81p	DIFFOUT_B81p	AK27	DQ10B	DQ3B	B_DQ_34	B_DQ_34
4A	VREFB4AN0				DIFFIO_RX_B82p	DIFFOUT_B82p	AF20	DQ10B	DQ3B	B_DQ_33	B_DQ_33
4A	VREFB4AN0				DIFFIO_RX_B83n	DIFFOUT_B83n	AD20	DQSn10B	DQSn3B	B_DQS#_4	B_DQS#_4
4A	VREFB4AN0	Ю			DIFFIO_TX_B84n	DIFFOUT_B84n	AH26	DQ10B	DQ3B	B_DQ_35	B_DQ_35
4A	VREFB4AN0	IO .			DIFFIO_RX_B83p	DIFFOUT_B83p	AC21	DQS10B	DQS3B	B_DQS_4	B_DQS_4
1A	VREFB4AN0	IO .			DIFFIO_TX_B84p	DIFFOUT_B84p	AG26			GND	GND
1A	VREFB4AN0	IO			DIFFIO_TX_B85n	DIFFOUT_B85n	AF23	DQ10B	DQ3B	GND	GND
1A 1A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B86n	DIFFOUT_B86n	AG22	DQ10B	DQ3B	B_DQ_36	B_DQ_36
1A 1A	VREFB4AN0 VREFB4AN0	10	 		DIFFIO_TX_B85p DIFFIO_RX_B86p	DIFFOUT_B85p DIFFOUT_B86p	AE22 AF21	DQ10B DQ10B	DQ3B DQ3B	B_DQ_38 B_DQ_37	B_DQ_38 B_DQ_37
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B86p DIFFIO_RX_B87n	DIFFOUT_B86p DIFFOUT_B87n	AC22	DQTUB	DUSD	GND	GND
IA	VREFB4AN0 VREFB4AN0				DIFFIO_RX_B87n DIFFIO_TX_B88n	DIFFOUT_B88n	AH22	DQ10B	DQ3B	B_DQ_39	B_DQ_39
4A	VREFB4AN0	IO .	<u> </u>		DIFFIO_TX_Booti	DIFFOUT_B887p	AB22	DQ10B	DGOD	GND	GND
4A	VREFB4AN0	10			DIFFIO_TX_B88p	DIFFOUT_B88p	AG23	DQ10B	DQ3B	B DM 4	B DM 4
5A	VREFB5AN0		RZQ 1		DIFFIO TX R1p	DIFFOUT R1p	AD23	DQ1R			1-2
5A	VREFB5AN0			INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	W22		1		1
5A	VREFB5AN0			PR REQUEST	DIFFIO TX R1n	DIFFOUT_R1n	AC24	DQ1R	1		1
5A	VREFB5AN0	Ю		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	Y21	1	İ		1
5A	VREFB5AN0	10		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AD24	DQ1R	1		1
5A	VREFB5AN0	10			DIFFIO_RX_R4p	DIFFOUT_R4p	Y25	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AD25	DQ1R			
					DIFFIO RX R4n	DIFFOUT R4n	Y26	DQ1R			



										_	Note
ank umber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for
	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AB26			DDR3/DDR2 (2)	LPDDR2
	VREFB5AN0			nPERSTL0	DIFFIO RX R6p	DIFFOUT_R6p	Y23	DQS1R			+
	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AA26	DQ1R			
	VREFB5AN0	10		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	W24	DQSn1R			
	VREFB5AN0	Ю			DIFFIO_TX_R7p	DIFFOUT_R7p	AC26	DQ1R			
	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	Y22	DQ1R			
	VREFB5AN0	Ю			DIFFIO_TX_R7n	DIFFOUT_R7n	AC27				
	VREFB5AN0	Ю			DIFFIO_RX_R8n	DIFFOUT_R8n	AA23	DQ1R			
	VREFB5AN0	Ю			DIFFIO_RX_R17p	DIFFOUT_R17p	AA24				
	VREFB5AN0	Ю			DIFFIO_TX_R18p	DIFFOUT_R18p	AE23	DQ2R			
	VREFB5AN0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	AA25				
	VREFB5AN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	AF24	DQ2R			
	VREFB5AN0	10			DIFFIO_RX_R19p	DIFFOUT_R19p	AE27	DQ2R			
	VREFB5AN0	IO			DIFFIO_TX_R20p	DIFFOUT_R20p	AE25	DQ2R			
	VIKEI DOMINO	Ю			DIFFIO_RX_R19n	DIFFOUT_R19n	AD27	DQ2R			
	VREFB5AN0	IO			DIFFIO_TX_R20n	DIFFOUT_R20n	AE26	DQ2R			
	VREFB5AN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	V21	DQS2R			
	VREFB5AN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	AF25				
	VREFB5AN0				DIFFIO_RX_R21n	DIFFOUT_R21n	V22	DQSn2R			
	VREFB5AN0	10			DIFFIO_TX_R22n	DIFFOUT_R22n	AF26	DQ2R			
	VREFB5AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	Y27	DQ2R			
	VREFB5AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	AH27	DQ2R			
	VREFB5AN0	Ю			DIFFIO_RX_R23n	DIFFOUT_R23n	W27	DQ2R	1		
	VREFB5AN0	Ю			DIFFIO_TX_R24n	DIFFOUT_R24n	AG27		1		
	VREFB5BN0	Ю			DIFFIO_RX_R25p	DIFFOUT_R25p	V24		1		
	VREFB5BN0	Ю			DIFFIO_TX_R26p	DIFFOUT_R26p	AJ28	DQ3R	DQ1R		
	VREFB5BN0				DIFFIO_RX_R25n	DIFFOUT_R25n	V25		1		
	VREFB5BN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	AJ29	DQ3R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_RX_R27p	DIFFOUT_R27p	AA28	DQ3R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_TX_R28p	DIFFOUT_R28p	AH29	DQ3R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_RX_R27n	DIFFOUT_R27n	Y28	DQ3R	DQ1R		
	VREFB5BN0				DIFFIO_TX_R28n	DIFFOUT_R28n	AG29	DQ3R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_RX_R29p	DIFFOUT_R29p	V26	DQS3R	DQS1R		
	VREFB5BN0	Ю			DIFFIO_TX_R30p	DIFFOUT_R30p	AJ30				
	VREFB5BN0	Ю			DIFFIO_RX_R29n	DIFFOUT_R29n	U26	DQSn3R	DQSn1R		
	VREFB5BN0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	AH30	DQ3R	DQ1R		
	VREFB5BN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	AE30	DQ3R	DQ1R		
	VREFB5BN0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	AG28	DQ3R	DQ1R		
	VREFB5BN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	AD30	DQ3R	DQ1R		
	VICEI DODINO	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	AF28				
	VREFB5BN0	Ю	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R33p	DIFFOUT_R33p	U21				
	VREFB5BN0	Ю			DIFFIO_TX_R34p	DIFFOUT_R34p	AF29	DQ4R	DQ1R		
	VREFB5BN0	Ю	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	U22				
	VREFB5BN0	Ю			DIFFIO_TX_R34n	DIFFOUT_R34n	AF30	DQ4R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_RX_R35p	DIFFOUT_R35p	V27	DQ4R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_TX_R36p	DIFFOUT_R36p	AE28	DQ4R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_RX_R35n	DIFFOUT_R35n	W28	DQ4R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_TX_R36n	DIFFOUT_R36n	AD28	DQ4R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_RX_R37p	DIFFOUT_R37p	U27	DQS4R	DQ1R		
	VREFB5BN0				DIFFIO_TX_R38p	DIFFOUT_R38p	AD29				
	VREFB5BN0	Ю			DIFFIO_RX_R37n	DIFFOUT_R37n	U28	DQSn4R	DQ1R		
	VREFB5BN0	Ю			DIFFIO_TX_R38n	DIFFOUT_R38n	AC29	DQ4R	DQ1R		
	VREFB5BN0			1	DIFFIO_RX_R39p	DIFFOUT_R39p	AA29	DQ4R	DQ1R		
	VREFB5BN0				DIFFIO_TX_R40p	DIFFOUT_R40p	AB27	DQ4R	DQ1R		
	VREFB5BN0				DIFFIO_RX_R39n	DIFFOUT_R39n	AA30	DQ4R	DQ1R		
	VREFB5BN0	10			DIFFIO_TX_R40n	DIFFOUT_R40n	AB28	<u> </u>	ļ		
	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R41p	DIFFOUT_R41p	U23				
	VREFB5BN0		<u> </u>		DIFFIO_TX_R42p	DIFFOUT_R42p	AB29	DQ5R	ļ		
	VREFB5BN0	10	CLK6n		DIFFIO_RX_R41n	DIFFOUT_R41n	T24		_		
	VREFB5BN0	IO	ļ		DIFFIO_TX_R42n	DIFFOUT_R42n	AC30	DQ5R	_		
	VREFB5BN0				DIFFIO_RX_R43p	DIFFOUT_R43p	T28	DQ5R	ļ		
		10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	Y30	DQ5R	_		
	VREFB5BN0		<u> </u>		DIFFIO_RX_R43n	DIFFOUT_R43n	T29	DQ5R	_		
	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	W30	DQ5R	_	-	
	VREFB5BN0	IO	ļ		DIFFIO_RX_R45p	DIFFOUT_R45p	T25	DQS5R	_	-	
	VREFB5BN0	IIO	1	1	DIFFIO_TX_R46p	DIFFOUT_R46p	V29	200	1	1	+
	VREFB5BN0	IIO	1	1	DIFFIO_RX_R45n	DIFFOUT_R45n	R26	DQSn5R	1	1	+
	VREFB5BN0		ļ		DIFFIO_TX_R46n	DIFFOUT_R46n	W29	DQ5R	_	-	
	VREFB5BN0	IO	ļ		DIFFIO_RX_R47p	DIFFOUT_R47p	T30	DQ5R	_		
	VREFB5BN0	IO	ļ		DIFFIO_TX_R48p	DIFFOUT_R48p	U29	DQ5R	_	-	
	VREFB5BN0		ļ		DIFFIO_RX_R47n	DIFFOUT_R47n	R30	DQ5R	_	-	
	VIKEI DODING	10	1		DIFFIO_TX_R48n	DIFFOUT_R48n	V30		_		
	VREFB6AN0		CLK5p		DIFFIO_RX_R49p	DIFFOUT_R49p	T23		_		
	VREFB6AN0	IO	1		DIFFIO_TX_R50p	DIFFOUT_R50p	P28	DQ6R	_		+
	VREFB6AN0	IO	CLK5n		DIFFIO_RX_R49n	DIFFOUT_R49n	R23		_		+
	VREFB6AN0	10	ļ		DIFFIO_TX_R50n	DIFFOUT_R50n	N29	DQ6R			+
	VREFB6AN0	Ю		1	DIFFIO_RX_R51p	DIFFOUT_R51p	P29	DQ6R		1	
	VREFB6AN0	10	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R52p	DIFFOUT_R52p	M29	DQ6R			



											Note
lank lumber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
	VREFB6AN0	10			DIFFIO_RX_R51n	DIFFOUT_R51n	P30	DQ6R			
	VREFB6AN0	10	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R52n	DIFFOUT_R52n	N30	DQ6R			
	VREFB6AN0	10			DIFFIO_RX_R53p	DIFFOUT_R53p	P25	DQS6R			
	VREFB6AN0	10			DIFFIO_TX_R54p	DIFFOUT_R54p	L28				
	VREFB6AN0	10			DIFFIO_RX_R53n	DIFFOUT_R53n	R25	DQSn6R			
	VREFB6AN0	10			DIFFIO_TX_R54n	DIFFOUT_R54n	K28	DQ6R			
		10			DIFFIO_RX_R55p	DIFFOUT_R55p	R27	DQ6R			
	VREFB6AN0	10			DIFFIO_TX_R56p	DIFFOUT_R56p	M27	DQ6R			-
	VREFB6AN0				DIFFIO_RX_R55n DIFFIO_TX_R56n	DIFFOUT_R55n	R28 M28	DQ6R			-
	VREFB6AN0	10	OLIVA- EDIL TO ED-	-		DIFFOUT_R56n					
	VREFB6AN0	10	CLK4p,FPLL_TR_FBp	-	DIFFIO_RX_R57p	DIFFOUT_R57p	P22	DOTE	DQ2R		
	VREFB6AN0 VREFB6AN0	10	CLK4n,FPLL_TR_FBn		DIFFIO_TX_R58p DIFFIO_RX_R57n	DIFFOUT_R58p DIFFOUT_R57n	K25 P23	DQ7R	DQ2R		
	VREFB6AN0	10	CER4II,FPEE_IR_FBII		DIFFIO_TX_R58n	DIFFOUT_R58n	K26	DQ7R	DQ2R		1
	VREFB6AN0				DIFFIO_RX_R59p	DIFFOUT R59p	N26	DQ7R	DQ2R		
	VREFB6AN0	10			DIFFIO_TX_R60p	DIFFOUT_R60p	L29	DQ7R	DQ2R		
	VREFB6AN0	10			DIFFIO_RX_R59n	DIFFOUT_R59n	N27	DQ7R	DQ2R		
	VREFB6AN0	10			DIFFIO_TX_R60n	DIFFOUT_R60n	L30	DQ7R	DQ2R		
	VREFB6AN0	10			DIFFIO_RX_R61p	DIFFOUT_R61p	N24	DQS7R	DQS2R		
	VREFB6AN0				DIFFIO_TX_R62p	DIFFOUT_R62p	K30	- 40111	- 40211		
	VREFB6AN0	10			DIFFIO_RX_R61n	DIFFOUT_R61n	N25	DQSn7R	DQSn2R		
	VREFB6AN0	IO			DIFFIO_TX_R62n	DIFFOUT_R62n	J30	DQ7R	DQ2R		
	VREFB6AN0	Ю			DIFFIO_RX_R63p	DIFFOUT_R63p	L25	DQ7R	DQ2R		1
	VREFB6AN0	Ю			DIFFIO_TX_R64p	DIFFOUT_R64p	G27	DQ7R	DQ2R		
	VREFB6AN0	IO			DIFFIO_RX_R63n	DIFFOUT_R63n	L26	DQ7R	DQ2R		
	VREFB6AN0	Ю			DIFFIO_TX_R64n	DIFFOUT_R64n	G28			1	
	VREFB6AN0	Ю			DIFFIO_RX_R65p	DIFFOUT_R65p	R21			1	
	VREFB6AN0				DIFFIO_TX_R66p	DIFFOUT_R66p	J28	DQ8R	DQ2R		
	VREFB6AN0	Ю			DIFFIO_RX_R65n	DIFFOUT_R65n	R22				
	VREFB6AN0	Ю			DIFFIO_TX_R66n	DIFFOUT_R66n	J29	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_RX_R67p	DIFFOUT_R67p	K27	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_TX_R68p	DIFFOUT_R68p	H29	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_RX_R67n	DIFFOUT_R67n	J27	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_TX_R68n	DIFFOUT_R68n	H30	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_RX_R69p	DIFFOUT_R69p	N22	DQS8R	DQ2R		
	VREFB6AN0	10			DIFFIO_TX_R70p	DIFFOUT_R70p	H27				
	VREFB6AN0				DIFFIO_RX_R69n	DIFFOUT_R69n	M23	DQSn8R	DQ2R		
	VREFB6AN0				DIFFIO_TX_R70n	DIFFOUT_R70n	G26	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_RX_R71p	DIFFOUT_R71p	F25	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_TX_R72p	DIFFOUT_R72p	F30	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_RX_R71n	DIFFOUT_R71n	F26	DQ8R	DQ2R		
	VREFB6AN0	10			DIFFIO_TX_R72n	DIFFOUT_R72n	E30				
	VREFB6AN0	10			DIFFIO_RX_R73p	DIFFOUT_R73p	R20				
	VICE DOTTIO	10			DIFFIO_TX_R74p	DIFFOUT_R74p	G29	DQ9R	DQ3R		
	VREFB6AN0	10			DIFFIO_RX_R73n	DIFFOUT_R73n	T21				
	VREFB6AN0 VREFB6AN0	10		-	DIFFIO_TX_R74n DIFFIO_RX_R75p	DIFFOUT_R74n DIFFOUT_R75p	F29 L23	DQ9R DQ9R	DQ3R DQ3R		
	VREFB6AN0 VREFB6AN0			-	DIFFIO_RX_R75p DIFFIO_TX_R76p	DIFFOUT_R75p DIFFOUT_R76p		DQ9R DQ9R	DQ3R DQ3R		
	VREFB6AN0				DIFFIO_TX_R76p	DIFFOUT_R75n	D30	DQ9R DQ9R			
	VREFB6AN0	10			DIFFIO_TX_R76n	DIFFOUT_R76n	L24 C30	DQ9R	DQ3R DQ3R		
	VREFB6AN0	10			DIFFIO_RX_R77p	DIFFOUT_R77p	N21	DQS9R	DQS3R		
	VREFB6AN0	10			DIFFIO_KX_K77p	DIFFOUT R78p	F28	DQSSK	DQSSK		
	VREFB6AN0	10			DIFFIO_RX_R77n	DIFFOUT_R77n	M22	DQSn9R	DQSn3R		
	VREFB6AN0				DIFFIO_TX_R78n	DIFFOUT R78n	E28	DQ9R	DQ3R		
	VREFB6AN0	10			DIFFIO_RX_R79p	DIFFOUT_R79p	K21	DQ9R	DQ3R		1
	VREFB6AN0	IO			DIFFIO_TX_R80p	DIFFOUT_R80p	C29	DQ9R	DQ3R		1
		IO			DIFFIO_RX_R79n	DIFFOUT_R79n	K22	DQ9R	DQ3R		1
	VREFB6AN0	Ю			DIFFIO_TX_R80n	DIFFOUT_R80n	B29				
	VREFB6AN0				DIFFIO_RX_R81p	DIFFOUT_R81p	M21		İ		
	VREFB6AN0	Ю			DIFFIO_TX_R82p	DIFFOUT_R82p	B28	DQ10R	DQ3R		
	VREFB6AN0	Ю			DIFFIO_RX_R81n	DIFFOUT_R81n	L21				
	VREFB6AN0	Ю			DIFFIO_TX_R82n	DIFFOUT_R82n	A29	DQ10R	DQ3R		
	VREFB6AN0				DIFFIO_RX_R83p	DIFFOUT_R83p	H25	DQ10R	DQ3R		
	VREFB6AN0	10			DIFFIO_TX_R84p	DIFFOUT_R84p	D28	DQ10R	DQ3R		
	VREFB6AN0	10			DIFFIO_RX_R83n	DIFFOUT_R83n	H26	DQ10R	DQ3R		
	VREFB6AN0	IO			DIFFIO_TX_R84n	DIFFOUT_R84n	D29	DQ10R	DQ3R		1
	VREFB6AN0	IO			DIFFIO_RX_R85p	DIFFOUT_R85p	P20	DQS10R	DQ3R		1
	VREFB6AN0				DIFFIO_TX_R86p	DIFFOUT_R86p	E27	1			
	VREFB6AN0	10			DIFFIO_RX_R85n	DIFFOUT_R85n	N20	DQSn10R	DQ3R		1
	VREFB6AN0	10			DIFFIO_TX_R86n	DIFFOUT_R86n	D27	DQ10R	DQ3R		
	VREFB6AN0	10			DIFFIO_RX_R87p	DIFFOUT_R87p	J22	DQ10R	DQ3R		1
	VREFB6AN0	10			DIFFIO_TX_R88p	DIFFOUT_R88p	H24	DQ10R	DQ3R		_
	VREFB6AN0				DIFFIO_RX_R87n	DIFFOUT_R87n	J23	DQ10R	DQ3R		
	VREFB6AN0				DIFFIO_TX_R88n	DIFFOUT_R88n	J25				
	l	GND				 	G24			4	
	VREFB7AN0				DIFFIO_RX_T9p	DIFFOUT_T9p	H21	1	DQ1T	GND	GND T_DM_4
	VREFB7AN0				DIFFIO_TX_T10p	DIFFOUT_T10p	E26	DQ1T		T_DM_4	



											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	E25	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO RX T11p	DIFFOUT T11p	G22	DQ1T	DQ1T	T DO 37	T DQ 37
7A	VREFB7AN0	io In			DIFFIO_TX_T12p	DIFFOUT_T12p	C27	DQ1T	DQ1T	T_DQ_38	T_DQ_38
'A	VREFB7AN0	10			DIFFIO_RX_T11n	DIFFOUT_T11n	G23	DQ1T	DQ1T	T_DQ_36	T_DQ_36
'A	VREFB7AN0	10			DIFFIO_TX_T12n	DIFFOUT_T12n	C26	DQ1T	DQ1T	GND	GND
A	VREFB7AN0	0			DIFFIO_RX_T13p	DIFFOUT_T13p	L20	DQS1T	DQS1T	T_DQS_4	T_DQS_4
Ά.	VREFB7AN0	0			DIFFIO_KX_T13p	DIFFOUT_T13p	B27	DQSTI	DQSTI	GND	GND
Α	VREFB7AN0	10			DIFFIO_TX_T14p	DIFFOUT_T13n	L19	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
Α		10									
^	VREFB7AN0	10			DIFFIO_TX_T14n	DIFFOUT_T14n	A28	DQ1T	DQ1T	T_DQ_35	T_DQ_35
Ά	VREFB7AN0	10			DIFFIO_RX_T15p	DIFFOUT_T15p	E22	DQ1T	DQ1T	T_DQ_33	T_DQ_33
Ά	VREFB7AN0	10			DIFFIO_TX_T16p	DIFFOUT_T16p	B26	DQ1T	DQ1T	T_DQ_34	T_DQ_34
Ά	VREFB7AN0	10			DIFFIO_RX_T15n	DIFFOUT_T15n	E21	DQ1T	DQ1T	T_DQ_32	T_DQ_32
'A	VICEI DITTIO	10			DIFFIO_TX_T16n	DIFFOUT_T16n	A26			GND	GND
'A	VREFB7AN0				DIFFIO_RX_T17p	DIFFOUT_T17p	J20			GND	GND
Ά	VREFB7AN0	10			DIFFIO_TX_T18p	DIFFOUT_T18p	D25	DQ2T	DQ1T	T_DM_3	T_DM_3
Ά	VREFB7AN0	0			DIFFIO_RX_T17n	DIFFOUT_T17n	H20			GND	GND
'A	VREFB7AN0	10			DIFFIO_TX_T18n	DIFFOUT_T18n	C25	DQ2T	DQ1T	T_DQ_31	T_DQ_31
Ά	VREFB7AN0	Ю			DIFFIO RX T19p	DIFFOUT T19p	C21	DQ2T	DQ1T	T DQ 29	T DQ 29
A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	D23	DQ2T	DQ1T	T_DQ_30	T_DQ_30
Α.	VREFB7AN0	10			DIFFIO_RX_T19n	DIFFOUT_T19n	C20	DQ2T	DQ1T	T_DQ_28	T_DQ_28
Δ.	VREFB7AN0	io.			DIFFIO TX T20n	DIFFOUT T20n	C22	DQ2T	DQ1T	GND.	GND
'Δ	VREFB7AN0	10	 	1	DIFFIO_TX_T2011	DIFFOUT_T21p	K20	DQS2T	DQ1T	T_DQS_3	T_DQS_3
A A	VREFB7AN0		 	1				DUGGET	DQII	GND	GND
		10	 	-	DIFFIO_TX_T22p	DIFFOUT_T22p	E23	DOC=2T	DOAT		
'A	VREFB7AN0	10	 	-	DIFFIO_RX_T21n	DIFFOUT_T21n	J19	DQSn2T	DQ1T	T_DQS#_3	T_DQS#_3
A	VREFB7AN0			1	DIFFIO_TX_T22n	DIFFOUT_T22n	D22	DQ2T	DQ1T	T_DQ_27	T_DQ_27
Ά	VREFB7AN0	10		ļ	DIFFIO_RX_T23p	DIFFOUT_T23p	D20	DQ2T	DQ1T	T_DQ_25	T_DQ_25
Ά	VREFB7AN0	10		<u> </u>	DIFFIO_TX_T24p	DIFFOUT_T24p	A25	DQ2T	DQ1T	T_DQ_26	T_DQ_26
Α	VREFB7AN0				DIFFIO_RX_T23n	DIFFOUT_T23n	C19	DQ2T	DQ1T	T_DQ_24	T_DQ_24
Ά	VREFB7AN0	10			DIFFIO_TX_T24n	DIFFOUT_T24n	A24			GND	GND
Α	VREFB7AN0	10			DIFFIO_RX_T25p	DIFFOUT_T25p	F20			GND	GND
A	VREFB7AN0	Ю			DIFFIO_TX_T26p	DIFFOUT_T26p	C24	DQ3T	DQ2T	T_DM_2	T_DM_2
A	VREFB7AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	E20			GND	GND
A	VREFB7AN0	10			DIFFIO_TX_T26n	DIFFOUT_T26n	B24	DQ3T	DQ2T	T_DQ_23	T_DQ_23
A	VREFB7AN0				DIFFIO_RX_T27p	DIFFOUT_T27p	F19	DQ3T	DQ2T	T_DQ_21	T_DQ_21
^	VREFB7AN0	9			DIFFIO_TX_T28p	DIFFOUT_T28p	B23	DQ3T	DQ2T	T_DQ_21	T_DQ_21
7.A		10									
A	VREFB7AN0	10			DIFFIO_RX_T27n	DIFFOUT_T27n	E18	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0				DIFFIO_TX_T28n	DIFFOUT_T28n	A23	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0				DIFFIO_RX_T29p	DIFFOUT_T29p	L18	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0				DIFFIO_TX_T30p	DIFFOUT_T30p	B22			T_RESET#	T_RESET#
7A	VREFB7AN0				DIFFIO_RX_T29n	DIFFOUT_T29n	K18	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0				DIFFIO_TX_T30n	DIFFOUT_T30n	B21	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	10			DIFFIO_RX_T31p	DIFFOUT_T31p	D19	DQ3T	DQ2T	T_DQ_17	T_DQ_17
'A	VREFB7AN0	10			DIFFIO_TX_T32p	DIFFOUT_T32p	A21	DQ3T	DQ2T	T_DQ_18	T_DQ_18
Ά	VREFB7AN0	0			DIFFIO_RX_T31n	DIFFOUT_T31n	D18	DQ3T	DQ2T	T_DQ_16	T_DQ_16
Ά	VREFB7AN0	Ю			DIFFIO_TX_T32n	DIFFOUT_T32n	A20			GND	GND
Ά	VREFB7AN0	Ю	CLK11p		DIFFIO_RX_T33p	DIFFOUT_T33p	H19				
Ά		IO			DIFFIO_TX_T34p	DIFFOUT_T34p	B19	DQ4T	DQ2T	T_DM_1	T_DM_1
Ά		IO	CLK11n		DIFFIO RX T33n	DIFFOUT T33n	J18				
Ά	VREFB7AN0	10			DIFFIO_TX_T34n	DIFFOUT_T34n	A19	DQ4T	DQ2T	T_DQ_15	T_DQ_15
A	VREFB7AN0			1	DIFFIO_RX_T35p	DIFFOUT T35p	G18	DQ4T	DQ2T	T_DQ_13	T_DQ_13
'A	VREFB7AN0	10			DIFFIO_TX_T36p	DIFFOUT T36p	B18	DQ4T	DQ2T	T DQ 14	T_DQ_13
Λ	VREFB7AN0	2	 		DIFFIO_TX_T35n	DIFFOUT_T35n	F18	DQ4T	DQ2T	T_DQ_14	T_DQ_12
Ά.	VREFB7AN0 VREFB7AN0		 	-	DIFFIO_RX_135n DIFFIO_TX_T36n		F18 A18	DQ41 DQ4T	DQ2T	T_CKE_0	
A		10	 	-		DIFFOUT_T36n					T_CKE_0
•	VREFB7AN0	IU		<u> </u>	DIFFIO_RX_T37p	DIFFOUT_T37p	K16	DQS4T	DQ2T	T_DQS_1	T_DQS_1
Ά	VREFB7AN0			!	DIFFIO_TX_T38p	DIFFOUT_T38p	D14	200 12		T_CKE_1	T_CKE_1
A	VREFB7AN0	10		ļ	DIFFIO_RX_T37n	DIFFOUT_T37n	L16	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
A	VREFB7AN0	10		<u> </u>	DIFFIO_TX_T38n	DIFFOUT_T38n	C14	DQ4T	DQ2T	T_DQ_11	T_DQ_11
Α	VREFB7AN0	10		<u> </u>	DIFFIO_RX_T39p	DIFFOUT_T39p	C17	DQ4T	DQ2T	T_DQ_9	T_DQ_9
A	VREFB7AN0	Ю			DIFFIO_TX_T40p	DIFFOUT_T40p	A16	DQ4T	DQ2T	T_DQ_10	T_DQ_10
Α	VREFB7AN0				DIFFIO_RX_T39n	DIFFOUT_T39n	B17	DQ4T	DQ2T	T_DQ_8	T_DQ_8
A	VREFB7AN0	10			DIFFIO_TX_T40n	DIFFOUT_T40n	A15			GND	GND
A	VREFB7AN0	Ю	CLK10p		DIFFIO_RX_T41p	DIFFOUT_T41p	H17				
A	VREFB7AN0	Ю			DIFFIO_TX_T42p	DIFFOUT_T42p	B14	DQ5T		T_DM_0	T_DM_0
A	VREFB7AN0	Ю	CLK10n		DIFFIO RX T41n	DIFFOUT_T41n	G17	1			1
A	VREFB7AN0	10			DIFFIO_TX_T42n	DIFFOUT_T42n	A14	DQ5T		T_DQ_7	T_DQ_7
Α	VREFB7AN0	10			DIFFIO_RX_T43p	DIFFOUT_T43p	E17	DQ5T	1	T_DQ_5	T_DQ_5
Α		10	 	1	DIFFIO_KX_143p	DIFFOUT T44p	D12	DQ5T	 	T DQ 6	T DQ 6
Λ.	VREFB7AN0	9	 		DIFFIO_TX_T44p		D12		1	T_DQ_6	T_DQ_6
Α		10	 	-		DIFFOUT_T43n		DQ5T	 		
, ,	VREFB7AN0			<u> </u>	DIFFIO_TX_T44n	DIFFOUT_T44n	C12	DQ5T	 	T_ODT_1	T_ODT_1
A	VREFB7AN0			ļ	DIFFIO_RX_T45p	DIFFOUT_T45p	K17	DQS5T	ļ	T_DQS_0	T_DQS_0
4	VREFB7AN0				DIFFIO_TX_T46p	DIFFOUT_T46p	B13			T_ODT_0	T_ODT_0
A	VREFB7AN0	10		<u> </u>	DIFFIO_RX_T45n	DIFFOUT_T45n	J17	DQSn5T	ļ	T_DQS#_0	T_DQS#_0
	VREFB7AN0	Ю			DIFFIO_TX_T46n	DIFFOUT_T46n	A13	DQ5T		T_DQ_3	T_DQ_3
4	VIDEEDZANIO	10			DIFFIO_RX_T47p	DIFFOUT_T47p	C16	DQ5T	L	T_DQ_1	T_DQ_1
A A	VREFB7AN0										
'A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T48p	DIFFOUT_T48p	C11	DQ5T		T_DQ_2	T_DQ_2
A A		IO IO			DIFFIO_TX_T48p DIFFIO_RX_T47n						
7A 7A 7A 7A	VREFB7AN0	Ю	RZQ_2			DIFFOUT_T48p DIFFOUT_T47n DIFFOUT_T48n	C11 C15 B12	DQ5T DQ5T		T_DQ_2 T_DQ_0	T_DQ_2 T_DQ_0



											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
ВА	VREFB8AN0	Ю			DIFFIO_TX_T50p	DIFFOUT_T50p	B11	DQ6T		T A 0	T_CA_0
8A	VREFB8AN0	10	CLK9n		DIFFIO_RX_T49n	DIFFOUT_T49n	K15				
8A	VREFB8AN0	10			DIFFIO_TX_T50n	DIFFOUT_T50n	A11	DQ6T		T_A_1	T_CA_1
BA	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	F16	DQ6T		T_A_4	T_CA_4
3A	VREFB8AN0	Ю	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	F9	DQ6T		T_A_2	T_CA_2
3A	VREFB8AN0				DIFFIO_RX_T51n	DIFFOUT_T51n	E16	DQ6T		T_A_5	T_CA_5
3A	VREFB8AN0		FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	E10	DQ6T		T_A_3	T_CA_3
BA	VREFB8AN0				DIFFIO_RX_T53p	DIFFOUT_T53p	M9	DQS6T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	D9			T_A_6	T_CA_6
8A 8A	VREFB8AN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	M8	DQSn6T		T_CK#	T_CK#
8A 8A	VREFB8AN0 VREFB8AN0	10			DIFFIO_TX_T54n DIFFIO_RX_T55p	DIFFOUT_T54n DIFFOUT_T55p	C10 F15	DQ6T DQ6T		T_A_7 T_BA_1	T_CA_7
8A	VREFB8AN0	10			DIFFIO_RX_T56p	DIFFOUT_T56p	A10	DQ6T		T_BA_0	+
8A	VREFB8AN0				DIFFIO_TX_T55p	DIFFOUT T55n	F15	DQ6T		T_BA_2	+
84	VREFB8AN0	IO.			DIFFIO_TX_T56n	DIFFOUT_T56n	A9	DQUI		GND	GND
8A	VREFB8AN0	IO.	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	L14			CIND	OND
8A	VREFB8AN0		oerop, i ee_re_r op		DIFFIO TX T58p	DIFFOUT T58p	C9	DQ7T		T CAS#	+
8A	VREFB8AN0		CLK8n,FPLL_TL_FBn		DIFFIO_RX_T57n	DIFFOUT_T57n	L13				
8A	VREFB8AN0				DIFFIO_TX_T58n	DIFFOUT T58n	B8	DQ7T		T_RAS#	
8A	VREFB8AN0	Ю			DIFFIO_RX_T59p	DIFFOUT_T59p	E12	DQ7T		T_A_8	T_CA_8
8A	VREFB8AN0	Ю			DIFFIO_TX_T60p	DIFFOUT_T60p	B7	DQ7T		T_A_10	
8A	VREFB8AN0	Ю			DIFFIO_RX_T59n	DIFFOUT_T59n	D13	DQ7T		T_A_9	T_CA_9
8A	VREFB8AN0				DIFFIO_TX_T60n	DIFFOUT_T60n	A8	DQ7T		T_A_11	
8A	VREFB8AN0	Ю			DIFFIO_RX_T61p	DIFFOUT_T61p	J15	DQS7T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	Ю			DIFFIO_TX_T62p	DIFFOUT_T62p	B6			T_A_12	
8A	VREFB8AN0	10		ļ	DIFFIO_RX_T61n	DIFFOUT_T61n	H15	DQSn7T		T_CS#_1	T_CS#_1
8A	VREFB8AN0				DIFFIO_TX_T62n	DIFFOUT_T62n	A6	DQ7T		T_A_13	
8A	VREFB8AN0				DIFFIO_RX_T63p	DIFFOUT_T63p	E11	DQ7T		T_A_14	
8A	VREFB8AN0	10			DIFFIO_TX_T64p	DIFFOUT_T64p	C7	DQ7T		T_WE#	_
8A	VREFB8AN0	10			DIFFIO_RX_T63n	DIFFOUT_T63n	D10	DQ7T		T_A_15	
8A	VREFB8AN0				DIFFIO_TX_T64n	DIFFOUT_T64n	C6			GND	GND
8A	VREFB8AN0				DIFFIO_RX_T65p	DIFFOUT_T65p	L10				
8A	VREFB8AN0				DIFFIO_TX_T66p	DIFFOUT_T66p	F13	DQ8T			
8A 8A	VREFB8AN0 VREFB8AN0				DIFFIO_RX_T65n DIFFIO_TX_T66n	DIFFOUT_T65n DIFFOUT_T66n	L9 E13	DQ8T			+
8A	VREFB8AN0 VREFB8AN0	10			DIFFIO_TX_T65n DIFFIO_RX_T67p	DIFFOUT_T66n DIFFOUT_T67p	G14	DQ8T			+
8A 8A	VREFB8AN0 VREFB8AN0	10			DIFFIO_RX_T68p	DIFFOUT_167p DIFFOUT_168p	A5	DQ81 DQ8T			+
8A	VREFB8AN0	10			DIFFIO_TX_T66p	DIFFOUT_168p DIFFOUT_T67n	F14	DQ8T			+
8A	VREFB8AN0	10			DIFFIO_RX_T68n	DIFFOUT_T68n	A4	DQ8T			+
8A		IO .			DIFFIO_TX_T68II	DIFFOUT T69p	J14	DQS8T			+
84	VREFB8AN0	IO .			DIFFIO_TX_T70p	DIFFOUT_T70p	J7	DQ361			+
88	VREFB8AN0	IO.			DIFFIO_RX_T69n	DIFFOUT_T69n	H14	DQSn8T			+
8A	VREFB8AN0	10			DIFFIO_TX_T70n	DIFFOUT_T70n	H7	DQ8T			+
8A	VREFB8AN0	10			DIFFIO_RX_T71p	DIFFOUT_T71p	L11	DQ8T			
8A	VREFB8AN0				DIFFIO_TX_T72p	DIFFOUT_T72p	J9	DQ8T			1
8A	VREFB8AN0	Ю			DIFFIO_RX_T71n	DIFFOUT_T71n	K11	DQ8T			
8A	VREFB8AN0	Ю			DIFFIO_TX_T72n	DIFFOUT_T72n	H9				
8A	VREFB8AN0				DIFFIO_RX_T73p	DIFFOUT_T73p	P12				
8A	VREFB8AN0				DIFFIO_TX_T74p	DIFFOUT_T74p	G9	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	N12				
8A	VREFB8AN0	Ю			DIFFIO_TX_T74n	DIFFOUT_T74n	F8	DQ9T	DQ3T		
8A	VREFB8AN0	10			DIFFIO_RX_T75p	DIFFOUT_T75p	H12	DQ9T	DQ3T		
8A	VREFB8AN0	IO		!	DIFFIO_TX_T76p	DIFFOUT_T76p	E8	DQ9T	DQ3T	-	4
8A	VREFB8ANO		ļ	 	DIFFIO_RX_T75n	DIFFOUT_T75n	G12	DQ9T	DQ3T	-	+
8A	VIVEI DOMINO	10		 	DIFFIO_TX_T76n	DIFFOUT_T76n	D8	DQ9T	DQ3T	+	+
8A 8A	VREFB8ANO	10		 	DIFFIO_RX_T77p	DIFFOUT_T77p	K13	DQS9T	DQS3T	+	+
8A 8A	VREFB8AN0 VREFB8AN0	10		+	DIFFIO_TX_T78p DIFFIO_RX_T77n	DIFFOUT_T78p	J13	DQSn9T	DQSn3T	+	+
8A 8A	VREFB8AN0 VREFB8AN0			†	DIFFIO_RX_17/h DIFFIO_TX_T78n	DIFFOUT_17/h DIFFOUT_T78n	A2	DQSn91 DQ9T	DQSn31 DQ3T	1	+
8A	VREFB8AN0		1	 	DIFFIO_TX_T78II DIFFIO_RX_T79p	DIFFOUT T79p	P10	DQ9T	DQ3T	1	+
8A	VREFB8AN0	in .	 	†	DIFFIO_KX_179p DIFFIO_TX_T80p	DIFFOUT_T80p	D7	DQ9T	DQ3T	1	+
8A	VREFB8AN0	IO .			DIFFIO_RX_T79n	DIFFOUT_T79n	N11	DQ9T	DQ3T		+
BA	VREFB8AN0	10		1	DIFFIO_KX_17911	DIFFOUT T80n	D6		,0,0,1	1	1
8A	VREFB8AN0	10		1	DIFFIO_RX_T81p	DIFFOUT_T81p	R12	1	1	1	1
8A	VREFB8AN0	Ю	İ		DIFFIO_TX_T82p	DIFFOUT_T82p	E7	DQ10T	DQ3T		1
8A	VREFB8AN0	10		1	DIFFIO_RX_T81n	DIFFOUT_T81n	R11			1	1
8A	VREFB8AN0	Ю			DIFFIO_TX_T82n	DIFFOUT_T82n	E6	DQ10T	DQ3T		
8A	VREFB8AN0				DIFFIO_RX_T83p	DIFFOUT_T83p	K12	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	K10	DQ10T	DQ3T		1
8A	VREFB8AN0				DIFFIO_RX_T83n	DIFFOUT_T83n	J12	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T84n	DIFFOUT_T84n	J10	DQ10T	DQ3T		
8A	VREFB8AN0	10			DIFFIO_RX_T85p	DIFFOUT_T85p	N10	DQS10T	DQ3T		
8A	VREFB8AN0	Ю			DIFFIO_TX_T86p	DIFFOUT_T86p	G6				
8A	VREFB8AN0	Ю			DIFFIO_RX_T85n	DIFFOUT_T85n	N9	DQSn10T	DQ3T		
8A	VREFB8AN0	Ю			DIFFIO_TX_T86n	DIFFOUT_T86n	F6	DQ10T	DQ3T		
8A	VREFB8AN0	Ю			DIFFIO_RX_T87p	DIFFOUT_T87p	M12	DQ10T	DQ3T		
84	VREFB8AN0	10		1	DIFFIO_TX_T88p	DIFFOUT_T88p	G8	DQ10T	DQ3T		
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											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
BA	VREFB8AN0	Ю			DIFFIO_TX_T88n	DIFFOUT_T88n	G7			DOTTO, DOTTE (E)	TEI DEILE
9A		MSEL0		MSEL0		_	T8				1
9A		CONF_DONE		CONF_DONE			L8				
9A		MSEL1		MSEL1			P9				
9A		nSTATUS		nSTATUS			K7				
A.		nCE		nCE			H6				
A.		MSEL2		MSEL2			G5				
9A		MSEL3		MSEL3			P7				
9A		nCONFIG		nCONFIG			C5				
9A		MSEL4		MSEL4			M7				
ΙA		GND					E5				
		GND					F22				
		GND					AK2				
		GND					AK14				
		GND					AK24				
		GND					AK29				
		GND					AJ6				
		GND					AJ11				
		GND					AJ21				
		GND					AH1				
		GND					AH2				
		GND					AH3				
		GND					AH8				
		GND					AH18				
		GND					AH28				1
		GND					AG3				
		GND					AG4				
		GND					AG15				
		GND		İ			AG25				1
		GND		İ			AF1				1
		GND					AF2				1
		GND					AF5				1
		GND					AF12				+
		GND					AF22				1
		GND					AE3				+
		GND					AE4				+
		GND					AE6				+
		GND		1			AE9				+
		GND		1			AE19				+
	1	GND		1	+		AE19 AE29		+		+
	1	GND		1	+		AD1		+		+
		GND		1			AD2				+
	1	GND		1	+		AD5		+		+
		GND		1	+		AD7		+		+
		GND					AD7 AD16				+
											+
		GND					AD26				+
		GND					AC3				
		GND					AC4				
		GND					AC6				
	1	GND		 	 		AC13	 	 	1	+
	!	GND			-	 	AC23	1	-	ļ	+
	!	GND		 	1	 	AB1	1	1	ļ	+
		GND			-	 	AB2	1	-	ļ	+
	!	GND			-	 	AB5	1	-	ļ	+
	1	GND		 	 		AB10	 	 	1	+
	!	GND			-	 	AB20	1	-	ļ	+
		GND	ļ	!	-	 	AB30	1	-	ļ	+
		GND				ļ	AA3	ļ			
		GND				 	AA4	ļ		ļ	
	ļ	GND		ļ		1	AA6	ļ	L		1
		GND					AA17				1
	ļ	GND		1	1		AA27	1	1		1
		GND					Y1	1			1
		GND		<u> </u>			Y2	1			1
		GND					Y5				1
		GND					Y7				
		GND					Y14				
		GND				1	Y24				
		GND					W3				
		GND					W4				
		GND					W6				
		GND					W11				
		GND					W13				1
		GND		İ	1	İ	W15	Ì	İ		1
	İ	GND			†		W17		1		1
	İ	GND			†		W19		1		1
	1	GND			1		W21	1	1	Ì	1
		GND	1	1	 	1	V1	t		1	+





											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					V2			DDR3/DDR2 (2)	LPDDR2
		GND					V5				
		GND					V8				
		GND					V14				
		GND					V16				ļ
		GND GND		+			V18 V20				ł
		GND					V20 V23				
		GND					V28				
		GND					U3				
		GND					U4				
		GND					U6				ļ
		GND GND		+			U13 U15				ł
		GND					U17				
		GND					U19				
		GND					U25				
		GND					T1				
		GND					T2				ļ
		GND GND					T5 T12	-	-	_	
		GND		1	1		T14	1	1	 	1
		GND					T16			1	
		GND					T18				
		GND					T20				
		GND					T22				
		GND GND					R3				ļ
		GND		+			R4 R6				
		GND					R9				
		GND					R13				
		GND					R15				
		GND					R17				
		GND					R19				
		GND					R29 P1				
		GND GND		+			P1 P2				
		GND					P5				
		GND					P11				
		GND					P14				
		GND					P16				
		GND					P18				
		GND					P26 N3				-
		GND GND					N4				
		GND					N6				
		GND					N8				
		GND					N13				
		GND					N15				
		GND GND					N17 N19				
		GND					N23			-	
		GND		1	1		M1			1	
		GND					M2				
		GND					M5				
		GND					M10	ļ			
		GND					M14 M16	-	-		+
		GND GND		1			M16 M18	1	1	 	1
		GND		1	1		M20	1	1	 	
		GND		İ	İ		M30			İ	
		GND					L3				
		GND					L4				
		GND		1			L6	ļ	ļ		
		GND GND					L17 L27	-	-	_	
		GND		1	1		K1	1	1	 	1
		GND					K2			1	
		GND		<u> </u>			K5				
		GND					K9				
		GND		1			K14				L
		GND					K24			1	
		GND GND					J3	-	-	_	
		GND		+		1	J4 J6	1		†	
		GND GND		İ			J11			İ	
		GND					J21				
		GND		-			H1				





											Note (
Bank lumber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					H2				
		GND					H5				
		GND					H8				
		GND					H11				
		GND					H18				
		GND					H28				
		GND					G3				
		GND					G4				
		GND					G15				
		GND		1			G25				
		GND		1			F1				
		GND		†			F2				
		GND		 			F5				
		GND		†			F12				
		GND		+		1	E3				
		GND		+			E4				-
											
		GND					E9 E19				
		GND		ļ							
	1	GND		1	 		E29	 	 	 	
	!	GND		ļ	ļ		D1	-	ļ	ļ	
	ļ	GND	ļ	ļ	ļ		D2	ļ			
		GND					D5				↓
	!	GND	ļ		ļ		D16	ļ			
	ļ	GND			ļ		D26				ļ
		GND			ļ		C2				ļ
		GND					C3				L
		GND			1		C4				1
		GND					C13				
		GND					C23				
		GND					B1				
		GND					B2				
		GND					B10				
		GND					B20				
		GND		1			B30				
		GND					A12				
		GND					A17				
		GND					A27				
		vcc					M15				
		vcc		1			W14				
		VCC					W16				
		vcc					W18				
		VCC		†			W20				
		VCC		 			V13				
		VCC		†			V15				
		VCC		+		1	V17				
	1	VCC		+			V17 V19				
		VCC		+			U14				-
		VCC		+			U14 U16				-
		VCC									
		VCC					U18				
	1	VCC		1	 		U20	 	 	 	
		VCC					T13				
		vcc					T15				
	ļ	VCC	ļ	ļ	ļ	ļ	T17	ļ			
		vcc	ļ		ļ		T19	ļ			
		VCC			ļ		R14				ļ
		VCC			ļ		R16				ļ
		VCC					R18				<u> </u>
		VCC					P13				<u> </u>
		VCC					P15				
		VCC					P17				
		VCC					P19				
		VCC					N14				
		VCC VCC					N16				
		VCC					N18				
		VCC					M13				
		vcc					M17				
		VCC		Ì	1		M19				
		DNU			İ		B4				
	1	DNU		İ	1		B3				†
	1	DNU		1	1	1	AD8	1			†
	1	DNU		 	†		AD14				
	1	DNU	1	1	1	1	F24	1	1	1	
	 	DNU		1	 		F24	 			
	 	DNU		1	 	1	D15	-		ļ	
	1	VCCPGM		-	 		AC11			-	
	1	VCCPGM	1	1	1		AB24	ļ	ļ	ļ	
	!	VCCPGM		ļ	ļ		F10	-	ļ	ļ	
	ļ	VCCBAT		ļ	ļ	1	H10				
	1	VCCIO3A		1	l	1	U10	l			





											Note (1)
Bank lumber		Pin Name/Function	Optional Function(s)		Dedicated Tx/Rx Channel	Emulated LVDS Output Channel		DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCIO3A					AD11				
		VCCIO3A					AC8				
		VCCIO3A					Y9			ļ	
		VCCIO3B					AA12		ļ	ļ	
		VCCIO3B	<u> </u>	<u> </u>			AK4		ļ	ļ	
		VCCIO3B		<u> </u>			AK9		ļ	ļ	
		VCCIO3B		<u> </u>			AH13		ļ	ļ	
		VCCIO3B VCCIO3B		_			AG10 AE14		ļ	ļ	
				+			AE14 AK19		 	 	
	1	VCCIO4A VCCIO4A	-	+			AK19 AJ16	 		 	-
		VCCIO4A VCCIO4A	 	 			AJ16 AJ26		 	 	
		VCCIO4A VCCIO4A	 	 			AJZ6 AH23		 	 	
	1	VCCIO4A		 			AG20	 	 	 	<u> </u>
		VCCIO4A	1	†			AF17		1		
		VCCIO4A	1	†			AD21		1		
		VCCIO4A		1			AC18				
		VCCIO4A		1			AB15				
	1	VCCIO4A		1			Y19				
		VCCIO5A					AF27				
		VCCIO5A					AE24				
		VCCIO5A					AB25				
		VCCIO5A					AA22				
		VCCIO5B					AG30			<u> </u>	
		VCCIO5B		ļ	ļ		AC28	<u> </u>	<u> </u>	<u> </u>	
		VCCIO5B					Y29			 	
		VCCIO5B	<u> </u>	<u> </u>			W26		ļ	ļ	
		VCCIO5B	<u> </u>	<u> </u>			U30		ļ	ļ	
		VCCIO5B		<u> </u>			T27		ļ	ļ	
		VCCIO6A		<u> </u>			R24		ļ	ļ	
		VCCIO6A		<u> </u>			P21		ļ	ļ	
		VCCIO6A		_			N28		ļ	ļ	
		VCCIO6A		_			M25		ļ	ļ	
		VCCIO6A VCCIO6A		+			L22 K29		 	 	
				+					 	 	
		VCCIO6A VCCIO6A		+			J26		 	 	
		VCCIO6A VCCIO6A	-	 			G30 F27	 		 	
		VCCIO6A VCCIO6A	+	+			C28	 	 	 	
		VCCIO7A	 	 			K19		 	 	
		VCCIO7A		 			H23		 	 	
	1	VCCIO7A		 			G20	 	 	 	<u> </u>
		VCCIO7A	1	†			F17		1		
		VCCIO7A		1			E24				
	1	VCCIO7A		1			D21				
		VCCIO7A					C18				
		VCCIO7A					B15				
		VCCIO7A					B25				
		VCCIO7A					A22				
		VCCIO8A		L			A7	<u> </u>	ļ	ļ	
		VCCIO8A					L12	<u> </u>	<u> </u>	↓	
		VCCIO8A					J16			 	
		VCCIO8A	 				H13				
	ļ	VCCIO8A	<u> </u>				G10				
		VCCIO8A	 	 	 		F7	 	 	 	
		VCCIO8A	 	 	 		E14	 	 	 	
	 	VCCIO8A VCCIO8A	 	 	 		D11 C8	 	 	 	
			 						 		
		VCCIO8A VCCPD3A	 				B5		 		
	1	VCCPD3A VCCPD3A	+	 	1		AD10 AB11	 	+	+	
		VCCPD3A VCCPD3B4A	+	+	1		AC20	 	+	+	
		VCCPD3B4A VCCPD3B4A	+	 			AC20 AE11	 		 	
		VCCPD3B4A VCCPD3B4A	+	+	 		AE21		+	+	
		VCCPD3B4A VCCPD3B4A	+	 			AD15	 	 	 	
	1	VCCPD3B4A VCCPD3B4A	†	 	1		AC12	 	 	 	t
		VCCPD3B4A VCCPD3B4A	†	1	1		AC17	 	 	†	†
		VCCPD5A	1	T			W23			1	
		VCCPD5A	1	T			W25			1	
		VCCPD5B	1	1			U24	1		1	
		VCCPD5B	1	1			T26	1		1	
		VCCPD6A	1				P24			1	
		VCCPD6A	1				M24		1	1	
		VCCPD6A	1				K23		1	1	
		VCCPD7A8A	1				D24		1		
		VCCPD7A8A					G13				
		VCCPD7A8A VCCPD7A8A					G13 G16				



Pin Information for the Cyclone® V 5CGXFC9 Device

Version 1.1 Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCPD7A8A					F11				
		VCCPD7A8A					F21				
		VCCPD7A8A					F23				
3A	VREFB3AN0	VREFB3AN0					AE8				
3B	VREFB3BN0	VREFB3BN0					AJ13				
4A	VREFB4AN0	VREFB4AN0					AH16				
5A	VREFB5AN0	VREFB5AN0					AC25				
5B	VREFB5BN0	VREFB5BN0					P27				
6A	VREFB6AN0	VREFB6AN0					M26				
7A	VREFB7AN0	VREFB7AN0					B16				
8A	VREFB8AN0	VREFB8AN0					B9				
		VCCH_GXBL					AB6				
		VCCH_GXBL					V6				
		VCCH_GXBL					P6				
		VCCH_GXBL					K6				
		VCCL_GXBL					AC5				
		VCCL_GXBL					W5				
		VCCL_GXBL					R5				
		VCCL_GXBL					L5				
		RREF_TL					C1				
		VCCA_FPLL					Y8				
		VCCA_FPLL					J8				
		VCCA_FPLL					AB23				
		VCCA_FPLL					J24				
		VCC_AUX					G11				
		VCC_AUX					AC10				
		VCC_AUX					AD22				
		VCC_AUX					AC16				
		VCC_AUX					H16				
		VCC_AUX					H22				
		VCCE_GXBL					AD6				
		VCCE_GXBL					AA5				
		VCCE_GXBL					Y6				
		VCCE_GXBL					U5				
		VCCE_GXBL					T6				
		VCCE_GXBL					N5				
		VCCE_GXBL					M6				
		VCCE_GXBL					J5				

(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines, (2) RESET pin is only applicable for DDR3 device.

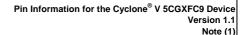


		Note (1											
SECTION	Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2	
SECTION	GXR L3		REECI K3I n					P10					
Mathematics Mathematics			REFCI K3I n										
150.5 150.	GXB_L3												
100 100	GXB_L3		GXB_TX_L11p					F4					
2011 COST 16-10-5	GXB_L3		GXB_RX_L11p,GXB_REFCLK_L11p					G2					
196 1	GXB_L3		GXB_RX_L11n,GXB_REFCLK_L11n										
10 10 10 10 10 10 10 10													
1964			GXB_TX_L10p										
Section Sect													
Sign Pub Sign Pub													
Section Sect													
Col.													
100 1			GXB_RX_L9P,GXB_REFCLK_L9P										
Col.													
SOUTH SOUT			GXB_TX_L6II									_	
See But Mind Reference													
100 1			GXB RX I 8n GXB REFCLK I 8n										
SOLIT SOLI	GXB L2												
Col. Col.	GXB L2		GXB_TX_L7p					P4					
100 100	GXB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					R2					
Section Sect	GXB_L2		GXB_RX_L7n,GXB_REFCLK_L7n										
1985													
100 100	GXB_L2												
Section	GXB_L2		GXB_RX_L6p,GXB_REFCLK_L6p										
			REFCLK2Lp										
Color													
Sign			REFCLK1Lp										
000 BY KLOGOS BEFORK LISE													
100 100													
CORD CORD													
GORD GORD			GXB_TX_LSH,GXB_REFCER_LSH										
Company Comp													
1			GXB RX L4p.GXB REFCLK L4p					AA2					
GOD 1	GXB_L1		GXB RX L4n,GXB REFCLK L4n										
ONE_LL ONE_RX_LEGOR REFCICK_LTS	GXB_L1		GXB_TX_L3n										
GORD GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR REPORT 129 GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR REFORK 129 GORD RY, LEGOUR RY,													
ORS D			GXB_RX_L3p,GXB_REFCLK_L3p					AC2					
OSB OSB TALED													
GOB LO													
ORB ORB RY LENGKEP FEET NET			GXB_TX_L2p					AD4					
GOB LO													
ORS D. ORS TX, Lip													
GORD GORD RK.LIng.ORD REFCIK_LIP													
GXB RX LINGER REPCIX LID			CVD DV 14- CVD DEECLY 14-							-	+		
CASE LO CASE TX LOP CASE			CVP BY LID CVP REFCLY LID										
OXB_TX_LUp OXB_TX_Lup OXB													
GXB LO	GXB L0							AH4					
Alt Alt													
ART ART			GXB_RX_L0n,GXB_REFCLK_L0n		<u> </u>	<u> </u>							
REFLIXION REFL	GXB_L0		REFCLK0Lp					AA11					
TOO TOO	GXB_L0		REFCLK0Ln					AB10					
TMS	3A		TDO					AF11					
AS DATA3	3A												
TCK	3A										ļ		
AS DATA2	3A		AS_DATA3		DATA3			AJ6					
A				ļ		ļ	ļ		ļ	-	.		
AS DATA1	3A									-	-		
DCLK										 	 	\vdash	
AS DATA0,ASDO						1	 		1	 	+		
A	3V									t	t	\vdash	
NREFB3AND O DATAS DIFFIO TX B2n DIFFOUT B2n AM4 DIFFOUT B2n AM5 DIFFOUT B2n AM6 DIFFOUT B2n AM7 DIFFOUT B2n AM8 DO1B	34					DIFFIO RX R1n	DIFFOLIT B1n		DO1B			\vdash	
3A VREFB3ANO O DATAB DIFFO(RX B1p DIFFOUT B1p DATAB DIFFO(RX B1p DIFFOUT B2p DATAB DIFFO(RX B1p DIFFOUT B2p DIFFO	3A	VRFFB3AN0			DATA5	DIFFIO TX B2n	DIFFOUT B2n	AM4	2410	t	†	\vdash	
A	3A								DQ1B	1	1		
A		VREFB3AN0								1	1		
3A VREFB3AND O DATA9 DIFFIO TX B4n DIFFOUT B4n AL7 DQ1B	3A	VREFB3AN0	Ю		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n			l	1		
3A VREFB3ANO O DATA12 DIFFIQ RX B3p DIFFOUT B3p AH12 DOS1B DATA13 DIFFOUT B4p DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DIFFOUT B4p AK7 DO1B DATA15 DATA15 DIFFOUT B4p AK7 DO1B DATA15 DATA15 DIFFOUT B4p DATA15 DATA15 DATA15 DIFFOUT B4p DATA15			Ю				DIFFOUT_B4n						
3A VREFB3ANO IO DATA11 DIFFIO_TX_B4p DIFFOUT_B4p IAX7	3A						DIFFOUT_B3p						
3A VREFB3ANO IO DATA14 DIFFIO_RX_B5n DIFFOUT_B5n AG13 DQ1B 3A VREFB3ANO IO DATA13 DIFFIO_TX_B6n DIFFOUT_B6n AL8 DQ1B 3A VREFB3ANO IO CLKUSR DIFFIO_RX_B5p DIFFOUT_B6p AF13 DQ1B 3A VREFB3ANO IO DATA15 DIFFOUT_B6p JAK8 DQ1B	3A	VREFB3AN0	Ю		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AK7					
3A VREFB3AND IO DATA13 DIFFIQ TX B6n DIFFOUT B6n A.8 DO1B 3A VREFB3AND IO CLKUSR DIFFOUR X B6p DIFFOUT B6p AF13 DO1B 3A VREFB3AND IO DATA15 DIFFIO TX, B6p DIFFOUT B6p AK8 DO1B		VREFB3AN0	Ю		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	AG13					
3A VREFB3AN0 IO DATA15 DIFFIO_TX_B6p DIFFOUT_B6p AK8 D01B	3A	VREFB3AN0	10			DIFFIO_TX_B6n		AL8	DQ1B				
	3A		Ю										
3A VREFB3ANO IO PR_DONE DIFFIO_RX_B7n DIFFOUT_B7n AC12	3A		10						DQ1B				
	3A	VREFB3AN0	10		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AC12		1	1		

Pin List EF35

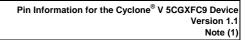


	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment	HMC Pin Assignment
Number					Channel					for DDR3/DDR2 (2)	for LPDDR2
3A	VREFB3AN0			PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AK9	DQ1B			
3A 3A	VREFB3AN0 VREFB3AN0	10		PR_ERROR	DIFFIO_RX_B7p DIFFIO_TX_B8p	DIFFOUT_B7p DIFFOUT_B8p	AC13 AJ9	DQ1B		_	
3A	VREFB3AN0				DIFFIO_TX_B9n	DIFFOUT_B9n	AM6	DQIB			
3A		Ю			DIFFIO_RX_B10n	DIFFOUT_B10n	AK10	DQ2B	DQ1B		
3A 3A	VREFB3AN0 VREFB3AN0	10			DIFFIO_TX_B9p DIFFIO_RX_B10p	DIFFOUT_B9p DIFFOUT_B10p	AL6 AJ10	DQ2B	DQ1B DQ1B	_	
3A		10			DIFFIO_RX_B10p DIFFIO_RX_B11n	DIFFOUT_B11n	AB13	DQ2B DQSn2B	DQ1B DQ1B		
3A	VREFB3AN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AN4	DQ2B	DQ1B		
3A	VREFB3AN0				DIFFIO_RX_B11p	DIFFOUT_B11p	AB14	DQS2B	DQ1B		
3A 3A	VREFB3AN0 VREFB3AN0	10			DIFFIO_TX_B12p DIFFIO_TX_B13n	DIFFOUT_B12p DIFFOUT_B13n	AN5 AP5	DQ2B	DQ1B		
3A		10			DIFFIO_RX_B14n	DIFFOUT_B14n	AJ12	DQ2B	DQ1B		
3A		10			DIFFIO_TX_B13p	DIFFOUT_B13p	AP6	DQ2B	DQ1B		
3A 3A	VREFB3AN0 VREFB3AN0	10			DIFFIO_RX_B14p DIFFIO_RX_B15n	DIFFOUT_B14p DIFFOUT_B15n	AH13 AE14	DQ2B	DQ1B		
3A		10			DIFFIO_TX_B15II	DIFFOUT B16n	AP7	DQ2B	DQ1B		
3A	VREFB3AN0	10			DIFFIO_RX_B15p	DIFFOUT_B15p	AD14				
3A		10			DIFFIO_TX_B16p	DIFFOUT_B16p	AN7	DQ2B	DQ1B		
3A 3A	VREFB3AN0 VREFB3AN0	10			DIFFIO_TX_B17n DIFFIO_RX_B18n	DIFFOUT_B17n DIFFOUT_B18n	AN8 AH14	DQ3B	DQ1B	+	
3A		Ю			DIFFIO_TX_B17p	DIFFOUT_B17p	AM8	DQ3B	DQ1B		
3A	VREFB3AN0	Ю			DIFFIO_RX_B18p	DIFFOUT_B18p	AG14	DQ3B	DQ1B		
3A	VREFB3AN0	10			DIFFIO_RX_B19n	DIFFOUT_B19n	AC14	DQSn3B	DQSn1B	+	
3A 3A	VREFB3AN0 VREFB3AN0	10			DIFFIO_TX_B20n DIFFIO_RX_B19p	DIFFOUT_B20n DIFFOUT_B19p	AN9 AD15	DQ3B DQS3B	DQ1B DQS1B	+	
3A	VREFB3AN0	10			DIFFIO_TX_B20p	DIFFOUT_B20p	AM9			<u> </u>	
3A		10			DIFFIO_TX_B21n	DIFFOUT_B21n	AM10	DQ3B	DQ1B		
3A 3A	VREFB3AN0 VREFB3AN0	10			DIFFIO_RX_B22n DIFFIO_TX_B21p	DIFFOUT_B22n DIFFOUT_B21p	AK14 AL10	DQ3B DQ3B	DQ1B DQ1B		
3A	VREFB3AN0				DIFFIO_IX_B21p	DIFFOUT_B22p	AJ14	DQ3B	DQ1B		
3A	VREFB3AN0	10			DIFFIO_RX_B23n	DIFFOUT_B23n	AB15				
3A		10			DIFFIO_TX_B24n	DIFFOUT_B24n	AK12	DQ3B	DQ1B		
3A 3A	VREFB3AN0 VREFB3AN0	10			DIFFIO_RX_B23p DIFFIO_TX_B24p	DIFFOUT_B23p DIFFOUT_B24p	AA15 AK13	DQ3B	DQ1B		
3B		10			DIFFIO_TX_B25n	DIFFOUT_B25n	AM11	DQ3B	DQIB		
3B	VREFB3BN0	Ю			DIFFIO_RX_B26n	DIFFOUT_B26n	AM15	DQ4B	DQ2B		
3B 3B		10			DIFFIO_TX_B25p DIFFIO_RX_B26p	DIFFOUT_B25p DIFFOUT_B26p	AL11 AL15	DQ4B DQ4B	DQ2B DQ2B		
3B	VREFB3BN0 VREFB3BN0	.0			DIFFIO_RX_B26p DIFFIO_RX_B27n	DIFFOUT_B25p DIFFOUT_B27n	AG15	DQ4B DQSn4B	DQ2B DQ2B		
3B	VREFB3BN0				DIFFIO_TX_B28n	DIFFOUT_B28n	AP9	DQ4B	DQ2B		
3B	VREFB3BN0	10			DIFFIO_RX_B27p	DIFFOUT_B27p	AG16	DQS4B	DQ2B		
3B 3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_TX_B28p DIFFIO_TX_B29n	DIFFOUT_B28p DIFFOUT_B29n	AP10 AP11	DQ4B	DQ2B		
3B		10			DIFFIO_IX_B29II	DIFFOUT_B30n	AK15	DQ4B DQ4B	DQ2B		
3B	VICEI DODITO	Ю			DIFFIO_TX_B29p	DIFFOUT_B29p	AN11	DQ4B	DQ2B		
3B		10			DIFFIO_RX_B30p	DIFFOUT_B30p	AJ15	DQ4B	DQ2B		
3B 3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_RX_B31n DIFFIO_TX_B32n	DIFFOUT_B31n DIFFOUT_B32n	AD16 AL13	DQ4B	DQ2B		
3B	VREFB3BN0	10			DIFFIO_RX_B31p	DIFFOUT_B31p	AC16	DQ.ID	DGLO		
3B		10			DIFFIO_TX_B32p	DIFFOUT_B32p	AL12	DQ4B	DQ2B		
3B 3B		10			DIFFIO_TX_B33n	DIFFOUT_B33n	AP12 AN14	DQ5B	DQ2B	GND B_A_15	GND
3B	VREFB3BN0 VRFFB3BN0	10			DIFFIO_RX_B34n DIFFIO_TX_B33p	DIFFOUT_B34n DIFFOUT_B33p	AN12	DQ5B	DQ2B	B_A_IS B WE#	
3B	VREFB3BN0				DIFFIO_RX_B34p	DIFFOUT_B34p	AM14	DQ5B	DQ2B	B_A_14	
3B		0			DIFFIO_RX_B35n	DIFFOUT_B35n	AB16	DQSn5B	DQSn2B	B_CS#_1	B_CS#_1
3B 3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_TX_B36n DIFFIO_RX_B35p	DIFFOUT_B36n DIFFOUT_B35p	AN13 AA16	DQ5B DQS5B	DQ2B DQS2B	B_A_13 B_CS#_0	B_CS#_0
3B		10	_		DIFFIO_TX_B36p	DIFFOUT_B33p	AM13	_ 4005	- 4025	B_A_12	555
3B	VREFB3BN0				DIFFIO_TX_B37n	DIFFOUT_B37n	AM16	DQ5B	DQ2B	B_A_11	
3B		10			DIFFIO_RX_B38n	DIFFOUT_B38n	AJ16	DQ5B	DQ2B	B_A_9	B_CA_9
3B 3B	VREFB3BN0 VREFB3BN0				DIFFIO_TX_B37p DIFFIO_RX_B38p	DIFFOUT_B37p DIFFOUT_B38p	AL16 AH16	DQ5B DQ5B	DQ2B DQ2B	B_A_10 B_A_8	B CA 8
3B	VREFB3BN0	Ю	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	AC17				'-"
3B	VREFB3BN0				DIFFIO_TX_B40n	DIFFOUT_B40n	AP14	DQ5B	DQ2B	B_RAS#	
3B 3B	VREFB3BN0 VREFB3BN0	10	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p DIFFIO_TX_B40p	DIFFOUT_B39p DIFFOUT_B40p	AD17 AP15	DQ5B	DQ2B	B CAS#	
3B	VREFB3BN0	10	_		DIFFIO_TX_B41n	DIFFOUT_B41n	AP15 AP16	DGJD	DUZE	GND	GND
3B	VREFB3BN0	Ю			DIFFIO_RX_B42n	DIFFOUT_B42n	AP17	DQ6B		B_BA_2	
3B 3B	VREFB3BN0 VRFFB3BN0	10			DIFFIO TX B41p DIFFIO RX B42p	DIFFOUT B41p DIFFOUT B42p	AN16 AN17	DQ6B	 	B BA 0	
3B 3B		10			DIFFIO_RX_B42p DIFFIO_RX_B43n	DIFFOUT_B43n	AN17 AA17	DQ6B DQSn6B	 	B_BA_1 B_CK#	B CK#
3B		10			DIFFIO_TX_B44n	DIFFOUT_B44n	AL17	DQ6B	İ		B_CA_7
3B	VREFB3BN0	Ю			DIFFIO_RX_B43p	DIFFOUT_B43p	AA18	DQS6B	ļ	B_CK	B_CK
3B 3B		10	FPLL BL CLKOUT1,FPLL BL CLKOUTn		DIFFIO_TX_B44p DIFFIO_TX_B45n	DIFFOUT_B44p DIFFOUT_B45n	AK17 AN18	DQ6B	1	B_A_6 B_A_3	B_CA_6 B_CA_3
3B	VREFB3BN0	Ю	IT LE DE GEROUTI,FFEE BE GEROUTII		DIFFIO_IX_B46n	DIFFOUT_B46n	AJ17	DQ6B	1	B_A_5	B_CA_5
3B	VREFB3BN0	Ю	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AM18	DQ6B		B_A_2	B_CA_2
3B	VREFB3BN0	10			DIFFIO_RX_B46p	DIFFOUT_B46p	AH17	DQ6B	L	B_A_4	B_CA_4



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Bank Number 3B 3B 3B 3B 4A 4A 4A 4A 4A 4A 4A 4A 4A	VREFB3BN0 VREFB3BN0	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment
3B 3B 3B 4A 4A 4A 4A 4A 4A 4A 4A	VREFB3BN0 VREFB3BN0	Ю								IOI DDIKG/DDIKE (2)	for LPDDR2
3B 3B 3B 4A 4A 4A 4A 4A 4A 4A 4A	VREFB3BN0 VREFB3BN0		CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	AB18				
3B 3B 4A 4A 4A 4A 4A 4A 4A 4A		10			DIFFIO TX B48n	DIFFOUT B48n	AL18	DQ6B		B A 1	B_CA_1
4A 4A 4A 4A 4A 4A 4A 4A 4A		Ю	CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	AC18				
4A 4A 4A 4A 4A 4A 4A	VREFB3BN0	Ю	•		DIFFIO_TX_B48p	DIFFOUT_B48p	AK18	DQ6B		B_A_0	B_CA_0
4A 4A 4A 4A 4A 4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B49n	DIFFOUT_B49n	AP19				
4A 4A 4A 4A 4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AN19	DQ7B		B DQ 0	B_DQ_0
4A 4A 4A 4A 4A	VREFB4AN0	Ю			DIFFIO_TX_B49p	DIFFOUT_B49p	AP20	DQ7B		B_DQ_2	B_DQ_2
4A 4A 4A 4A					DIFFIO_RX_B50p	DIFFOUT_B50p	AM19	DQ7B			B_DQ_1
4A 4A 4A		IO			DIFFIO_RX_B51n	DIFFOUT_B51n	AC19	DQSn7B			B_DQS#_0
4A 4A		10			DIFFIO_TX_B52n	DIFFOUT_B52n	AP21	DQ7B	ļ		B_DQ_3
4A		IO .			DIFFIO_RX_B51p	DIFFOUT_B51p	AB19	DQS7B		B_DQS_0	B_DQS_0
	VREFB4AN0	IO IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AN21	D07D		B_ODT_0	B_ODT_0
4A	VREFB4AN0 VREFB4AN0	io			DIFFIO_TX_B53n DIFFIO_RX_B54n	DIFFOUT_B53n DIFFOUT_B54n	AK19 AH19	DQ7B DQ7B	 	B_ODT_1 B DQ 4	B_ODT_1 B DQ 4
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B54n DIFFIO_TX_B53p	DIFFOUT_B53p	AH19 AJ19	DQ7B DQ7B			B_DQ_4 B_DQ_6
4A 4A		10			DIFFIO_IX_B53p	DIFFOUT B54n	AG19	DQ7B DQ7B			B_DQ_6 B_DQ_5
4A	VREFB4AN0	10	CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	AG18	DQ/B		B_DQ_3	B_DQ_5
4A		10	GENZII		DIFFIO_TX_B56n	DIFFOUT_B35II	AM21	DQ7B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	10	CLK2p		DIFFIO_TX_B55p	DIFFOUT B55p	AF18	DQ/B		B_DQ_/	B_DQ_/
4A		10	CLNZD		DIFFIO_TX_B56p	DIFFOUT_B35p	AL21	DQ7B	 	B DM 0	B_DM_0
4A 4A	VREFB4AN0	10			DIFFIO_TX_B56p	DIFFOUT B57n	AP22	5415			GND
4A	VREFB4AN0	in			DIFFIO_RX_B58n	DIFFOUT_B58n	AM20	DQ8B	DO3B		B DQ 8
4A		10			DIFFIO TX B57p	DIFFOUT B57p	AN22	DQ8B	DQ3B		B DQ 10
4A		10			DIFFIO_RX_B58p	DIFFOUT_B58p	AL20	DQ8B	DQ3B		B_DQ_10
4A		10			DIFFIO_RX_B59n	DIFFOUT_B59n	AE19	DQSn8B	DQ3B		B_DQS#_1
4A	VREFB4AN0	10			DIFFIO_TX_B60n	DIFFOUT_B60n	AN23	DQ8B	DQ3B	B_DQ_11	B_DQ_11
4A		10			DIFFIO_RX_B59p	DIFFOUT_B59p	AD19	DQS8B	DQ3B		B_DQS_1
4A		10			DIFFIO_TX_B60p	DIFFOUT B60p	AM23				B_CKE_1
4A	VREFB4AN0	10		İ	DIFFIO_TX_B61n	DIFFOUT_B61n	AP26	DQ8B	DQ3B	B CKE 0	B_CKE_0
4A	VREFB4AN0	10			DIFFIO_RX_B62n	DIFFOUT_B62n	AP24	DQ8B	DQ3B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	10			DIFFIO_TX_B61p	DIFFOUT_B61p	AN26	DQ8B	DQ3B	B_DQ_14	B DQ 14
4A	VREFB4AN0	Ю			DIFFIO_RX_B62p	DIFFOUT_B62p	AP25	DQ8B	DQ3B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	Ю	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	AE20				
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AN24	DQ8B	DQ3B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	Ю	CLK3p		DIFFIO_RX_B63p	DIFFOUT_B63p	AD20				
4A	VREFB4AN0	10			DIFFIO_TX_B64p	DIFFOUT_B64p	AM24	DQ8B	DQ3B		B_DM_1
4A	VREFB4AN0	10			DIFFIO_TX_B65n	DIFFOUT_B65n	AL22			GND	GND
4A	VREFB4AN0	Ю			DIFFIO_RX_B66n	DIFFOUT_B66n	AP27	DQ9B	DQ3B	B_DQ_16	B_DQ_16
4A		Ю			DIFFIO_TX_B65p	DIFFOUT_B65p	AK22	DQ9B	DQ3B		B_DQ_18
4A		Ю			DIFFIO_RX_B66p	DIFFOUT_B66p	AN27	DQ9B	DQ3B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AK20	DQSn9B	DQSn3B	B_DQS#_2	B_DQS#_2
4A		IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AJ21	DQ9B	DQ3B		B_DQ_19
4A		IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AJ20	DQS9B	DQS3B		B_DQS_2
4A		IO .			DIFFIO_TX_B68p	DIFFOUT_B68p	AJ22				B_RESET#
4A	VREFB4AN0	10			DIFFIO_TX_B69n	DIFFOUT_B69n	AP29	DQ9B	DQ3B		GND
4A		IO IO			DIFFIO_RX_B70n DIFFIO_TX_B69p	DIFFOUT_B70n DIFFOUT_B69p	AH21 AP30	DQ9B DQ9B	DQ3B DQ3B		B_DQ_20 B_DQ_22
4A 4A		10			DIFFIO_IX_B69p DIFFIO_RX_B70p	DIFFOUT_B70p	AP30 AH22		DQ3B DQ3B		B_DQ_22 B_DQ_21
4A 4A		10			DIFFIO_RX_B70p	DIFFOUT B71n	AB20	DQ9B	DQ3B		GND
4A	VREFB4AN0	10			DIFFIO_TX_B711	DIFFOUT_B72n	AN28	DQ9B	DQ3B	B DQ 23	B DQ 23
4A		10			DIFFIO_TX_B72II	DIFFOUT_B71p	AB21	DQSB	БОЗВ		GND
4A 4A		10			DIFFIO TX B72p	DIFFOUT_B72p	AM28	DQ9B	DQ3B		B_DM_2
4A	VREFB4AN0			1	DIFFIO_TX_B73n	DIFFOUT_B73n	AM25				GND
4A		10			DIFFIO_RX_B74n	DIFFOUT B74n	AL23	DQ10B	DQ4B	B DQ 24	B DQ 24
4A		10			DIFFIO_TX_B73p	DIFFOUT_B73p	AL25	DQ10B	DQ4B		B_DQ_26
4A		10			DIFFIO_RX_B74p	DIFFOUT_B74p	AK23	DQ10B	DQ4B		B_DQ_25
4A		10			DIFFIO_RX_B75n	DIFFOUT_B75n	AA20	DQSn10B	DQ4B	B_DQS#_3	B_DQS#_3
4A	VREFB4AN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AM26	DQ10B	DQ4B		B_DQ_27
4A		IO			DIFFIO_RX_B75p	DIFFOUT_B75p	Y20	DQS10B	DQ4B	B_DQS_3	B_DQS_3
4A		Ю			DIFFIO_TX_B76p	DIFFOUT_B76p	AL26				GND
4A		Ю			DIFFIO_TX_B77n	DIFFOUT_B77n	AP31	DQ10B	DQ4B		GND
4A		Ю			DIFFIO_RX_B78n	DIFFOUT_B78n	AK24	DQ10B	DQ4B		B_DQ_28
4A		Ю			DIFFIO_TX_B77p	DIFFOUT_B77p	AN31	DQ10B	DQ4B		B_DQ_30
4A		10			DIFFIO_RX_B78p	DIFFOUT_B78p	AJ24	DQ10B	DQ4B		B_DQ_29
4A	VREFB4AN0				DIFFIO_RX_B79n	DIFFOUT_B79n	AG21				GND
4A	VICEIDIANO	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AL28	DQ10B	DQ4B		B_DQ_31
4A		IO .			DIFFIO_RX_B79p	DIFFOUT_B79p	AF22				GND
4A		IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AL27	DQ10B	DQ4B		B_DM_3
4A	VREFB4AN0	IO IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AP32	DOLLE	DO 4D		GND D. DO. OO
4A	VREFB4AN0 VREFB4AN0	IO IO			DIFFIO RX B82n DIFFIO TX B81n	DIFFOUT_B82n DIFFOUT_B81n	AH23	DQ11B	DQ4B		B_DQ_32
4A							AN32	DQ11B	DQ4B		B_DQ_34
4A	VREFB4AN0 VREFB4AN0				DIFFIO_RX_B82p DIFFIO_RX_B83n	DIFFOUT_B82p DIFFOUT_B83n	AG23 AD21	DQ11B DQSn11B	DQ4B DQSn4B		B_DQ_33 B DQS# 4
4A 4A	VREFB4AN0 VREFB4AN0	10			DIFFIO_RX_B83n DIFFIO_TX_B84n	DIFFOUT_B83n DIFFOUT_B84n	AD21 AN29	DQSn11B DQ11B	DQSn4B DQ4B	B_DQS#_4 B_DQ_35	B_DQS#_4 B_DQ_35
4A 4A	VREFB4AN0 VRFFB4AN0	10			DIFFIO_IX_B84n DIFFIO_RX_B83p	DIFFOUT_B83p	AC21	DQ11B DQS11B	DQ4B DQS4B		B_DQ_35 B_DQS_4
	VREFB4AN0 VRFFB4AN0	10		1	DIFFIO_RX_B83p DIFFIO_TX_B84p	DIFFOUT_B84p	AC21 AM29	DUSTIB	DW04B		B_DQS_4 GND
	VREFB4AN0 VREFB4AN0			1	DIFFIO_IX_B84p	DIFFOUT B85n	AM29 AK27	DQ11B	DO4B		GND
4A 4A	VIVE D 17410	10			DIFFIO_IX_B65II	DIFFOUT_B86n	AK25	DQ11B DQ11B	DQ4B DQ4B	B DQ 36	B DQ 36
4A 4A 4A		10			DIFFIO_TX_B85p	DIFFOUT_B85p	AK28	DQ11B DQ11B	DQ4B		B_DQ_38



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											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	10			DIFFIO_RX_B86p	DIFFOUT_B86p	AJ25	DQ11B	DQ4B	B DQ 37	B_DQ_37
4A 4A		10			DIFFIO_RX_B87n	DIFFOUT_B87n	AF23	DQTIB	DQ4B	GND	GND
		10			DIFFIO_RA_B07II	DIFFOUT_B88n	AM30	DOMAR	DQ4B	B DO 39	B DO 39
17.	***************************************	10			DIFFIO_IX_B88h	DIFFOUT_B88n DIFFOUT_B87p		DQ11B	DQ4B	GND	GND
		10					AE23	D044D	2012		
	VICEIDINATO	10			DIFFIO_TX_B88p	DIFFOUT_B88p	AL30	DQ11B	DQ4B	B_DM_4	B_DM_4
4A	VREFB4AN0	10			DIFFIO TX B89n	DIFFOUT_B89n	AK29				
4A	VREFB4AN0	10			DIFFIO_RX_B90n	DIFFOUT_B90n	AH24	DQ12B			
	VREFB4AN0	10			DIFFIO_TX_B89p	DIFFOUT_B89p	AJ29	DQ12B			
	VREFB4AN0	10			DIFFIO_RX_B90p	DIFFOUT_B90p	AG24	DQ12B			
4A	VREFB4AN0	10			DIFFIO_RX_B91n	DIFFOUT_B91n	AD22	DQSn12B			
4A	VREFB4AN0	10			DIFFIO_TX_B92n	DIFFOUT_B92n	AM31	DQ12B			
4A	VICEIDINATO	10			DIFFIO_RX_B91p	DIFFOUT_B91p	AC22	DQS12B			
	VICEIDINATO	10			DIFFIO_TX_B92p	DIFFOUT_B92p	AL31				
4A	VREFB4AN0	10			DIFFIO_TX_B93n	DIFFOUT_B93n	AJ26	DQ12B			
	VREFB4AN0	Ю			DIFFIO_RX_B94n	DIFFOUT_B94n	AG26	DQ12B			
4A	VREFB4AN0	Ю			DIFFIO_TX_B93p	DIFFOUT_B93p	AH26	DQ12B			
4A	VREFB4AN0	Ю			DIFFIO_RX_B94p	DIFFOUT_B94p	AG25	DQ12B			
4A	VREFB4AN0	IO			DIFFIO RX B95n	DIFFOUT_B95n	AE25				
	VREFB4AN0	10			DIFFIO_TX_B96n	DIFFOUT_B96n	AJ27	DQ12B			
44		in .			DIFFIO_RX_B95p	DIFFOUT B95p	AF25	DQ12D			
14	VREFB4AN0	10	 		DIFFIO_TX_B96p	DIFFOUT_B96p	AH27	DQ12B	 	†	
E A		10	RZQ 1		DIFFIO_TX_B96p	DIFFOUT_R1p	AD24	DQ12B DQ1R	-	1	
	VREFB5AN0 VREFB5AN0	10	INCU_I	INIT_DONE	DIFFIO_IX_R1p	DIFFOUT_R1p	AC23	DQIK	-	1	
		10	 					DO4D		1	
	VREFB5AN0			PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AD25	DQ1R	l	ł	+
	VICEIDONIO	10		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	AC24				+
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AC27	DQ1R	ļ	ļ	
	VREFB5AN0	10	ļ		DIFFIO_RX_R4p	DIFFOUT_R4p	AB24	DQ1R			
	VREFB5AN0	10		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AC26	DQ1R	<u> </u>		ļ
5A	VICEIDONIO	10			DIFFIO_RX_R4n	DIFFOUT_R4n	AB23	DQ1R			
5A	VREFB5AN0	Ю		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AE29				
5A	VREFB5AN0	Ю		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	AA21	DQS1R			
5A	VREFB5AN0	Ю		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AD29	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	AA22	DQSn1R			
	VREFB5AN0	10			DIFFIO_TX_R7p	DIFFOUT_R7p	AC28	DQ1R			
	VREFB5AN0	10			DIFFIO_RX_R8p	DIFFOUT R8p	Y24	DQ1R			
5A	VREFB5AN0	in .			DIFFIO_TX_R7n	DIFFOUT_R7n	AC29	DQTIC			
EΛ	VREFB5AN0	10			DIFFIO_RX_R8n	DIFFOUT_R8n	Y25	DQ1R			
	VREFB5AN0	10			DIFFIO_RX_R8II	DIFFOUT R9p	AB25	DQTK			+
		10						DOOD	0040		+
5A	VREFB5AN0 VREFB5AN0				DIFFIO_TX_R10p DIFFIO_RX_R9n	DIFFOUT_R10p DIFFOUT_R9n	AF27	DQ2R	DQ1R		+
5A		10					AA25				
5A	VREFB5AN0	10			DIFFIO_TX_R10n	DIFFOUT_R10n	AF26	DQ2R	DQ1R		
	VREFB5AN0	10			DIFFIO_RX_R11p	DIFFOUT_R11p	AB28	DQ2R	DQ1R		
	VREFB5AN0	10			DIFFIO_TX_R12p	DIFFOUT_R12p	AE28	DQ2R	DQ1R		
	VREFB5AN0	10			DIFFIO_RX_R11n	DIFFOUT_R11n	AB29	DQ2R	DQ1R		
5A	VREFB5AN0	Ю			DIFFIO_TX_R12n	DIFFOUT_R12n	AF28	DQ2R	DQ1R		
5A	VREFB5AN0	10			DIFFIO_RX_R13p	DIFFOUT_R13p	AA23	DQS2R	DQS1R		
5A	VREFB5AN0	10			DIFFIO_TX_R14p	DIFFOUT_R14p	AG28				
5A	VREFB5AN0	10			DIFFIO_RX_R13n	DIFFOUT_R13n	Y22	DQSn2R	DQSn1R		
5A	VREFB5AN0	Ю			DIFFIO_TX_R14n	DIFFOUT_R14n	AH28	DQ2R	DQ1R		
5A	VREFB5AN0	Ю			DIFFIO_RX_R15p	DIFFOUT_R15p	AB30	DQ2R	DQ1R		
5A	VREFB5AN0	Ю			DIFFIO_TX_R16p	DIFFOUT_R16p	AG29	DQ2R	DQ1R		
5A		10			DIFFIO RX R15n	DIFFOUT R15n	AA30	DQ2R	DQ1R		
5A	VREFB5AN0	10			DIFFIO_TX_R16n	DIFFOUT_R16n	AH29				
	VREFB5AN0	10			DIFFIO_RX_R17p	DIFFOUT_R17p	AA27				
5A	VREFB5AN0	10			DIFFIO TX R18p	DIFFOUT R18n	AK30	DQ3R	DQ1R		
5A	VREFB5AN0	10			DIFFIO_RX_R17n	DIFFOUT_R17n	AA28			1	
5Δ	VREFB5AN0	10	 		DIFFIO_TX_R18n	DIFFOUT_R18n	AJ30	DQ3R	DQ1R	†	
	VREFB5AN0 VREFB5AN0	10	 	1	DIFFIO_IX_R18h DIFFIO_RX_R19p	DIFFOUT_R18h	AG30	DQ3R DQ3R	DQ1R DQ1R	1	
		10	 							1	
JA EA	VICEI DOVERO	10	 	-	DIFFIO_TX_R20p DIFFIO_RX_R19n	DIFFOUT_R20p DIFFOUT_R19n	AN33 AF30	DQ3R	DQ1R DQ1R	-	-
5A		10						DQ3R		ł	
5A		10	 		DIFFIO_TX_R20n	DIFFOUT_R20n	AM33	DQ3R	DQ1R	1	
011	VICEIDONIO	10			DIFFIO_RX_R21p	DIFFOUT_R21p	Y23	DQS3R	DQ1R		
		10			DIFFIO_TX_R22p	DIFFOUT_R22p	AL32				
5A	VREFB5AN0	Ю			DIFFIO_RX_R21n	DIFFOUT_R21n	W24	DQSn3R	DQ1R		
5A	VREFB5AN0	10			DIFFIO_TX_R22n	DIFFOUT_R22n	AK32	DQ3R	DQ1R		
5A	VREFB5AN0	10			DIFFIO_RX_R23p	DIFFOUT_R23p	AH31	DQ3R	DQ1R		
	VREFB5AN0	10			DIFFIO_TX_R24p	DIFFOUT_R24p	AL33	DQ3R	DQ1R		
5A	VREFB5AN0	10			DIFFIO_RX_R23n	DIFFOUT_R23n	AJ31	DQ3R	DQ1R		
5A	VREFB5AN0	Ю			DIFFIO_TX_R24n	DIFFOUT_R24n	AK33				
5B	VREFB5BN0	Ю			DIFFIO_RX_R25p	DIFFOUT_R25p	AA32				
5B		10			DIFFIO_TX_R26p	DIFFOUT_R26p	AE30	DQ4R	DQ2R		
		10			DIFFIO_RX_R25n	DIFFOUT R25n	Y32				
	VREFB5BN0	10	<u> </u>		DIFFIO_TX_R26n	DIFFOUT_R26n	AD30	DQ4R	DQ2R	1	i e
	VREFB5BN0	10	 		DIFFIO_TX_R2011 DIFFIO_RX_R27p	DIFFOUT_R27p	Y28	DQ4R DQ4R	DQ2R DQ2R	†	
5B	VREFB5BN0	10	 		DIFFIO_RX_R27p	DIFFOUT_R28p	AH32	DQ4R DQ4R	DQ2R DQ2R	†	
5B	VREFB5BN0	10	 		DIFFIO_IX_R26p	DIFFOUT R27n	Y27	DQ4R DQ4R	DQ2R DQ2R	1	
	VREFB5BN0 VRFFB5BN0	10	 		DIFFIO_RX_R2/h	DIFFOUT_R2/n	AJ32	DQ4R DQ4R	DQ2R DQ2R	1	
		10	 	 						 	
28	VREFB5BN0	IU			DIFFIO_RX_R29p	DIFFOUT_R29p	Y29	DQS4R	DQS2R	ł	
5B	VREFB5BN0	IU			DIFFIO_TX_R30p	DIFFOUT_R30p	AG31		l .	l	1



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Bank VRFF Pin Name/Function Optional Function(s) Configuration Function Dedicated Ty/Ry Emulated LVDS Output Channel DOS for X8 DOS for X16 HMC Pin Assignment HMC Pin Assignment Number hannel for DDR3/DDR2 (2) for LPDDR2 DIFFIO_RX_R29n DIFFOUT_R29n DQSn4R VREFB5BN0 IC Y30 DQSn2R DIFFIO_TX_R30n DIFFOUT_R30n DQ4R VREFB5BN0 IC AF31 DQ2R DIFFIO RX R31p DIFFOUT R31 DQ4R VRFFB5BN0 I VREFB5BN0 IO DIFFIO_TX_R32p DIFFOUT_R32p AN34 DQ4R DQ2R VREFB5BN0 IO DIFFIO_RX_R31n DIFFOUT_R31n AC32 DQ4R DQ2R VREFB5BN0 IO DIFFIO_TX_R32n DIFFOUT_R32n AM34 CLK7p,FPLL_BR_FBp DIFFIO_RX_R33p DIFFOUT_R33p W26 VREFB5BN0 IC DIFFIO_TX_R34p DIFFOUT_R34p AA31 DQ5R CLK7n,FPLL_BR_FBn DIFFIO_RX_R33n DIFFOUT_R33n W27 VREFB5BN0 IC DIFFIO_TX_R34n DIFFOUT_R34n DQ5R VREFB5BN0 IO DIFFIO_RX_R35p DIFFOUT_R35p AK34 DQ5R VREFB5BN0 IC DIFFIO_TX_R36p DIFFOUT_R36p AH33 DQ5R VREFB5BN0 I DIFFIO_RX_R35n DIFFOUT_R35n AJ34 DQ5R VREFB5BN0 IO DIFFIO_TX_R36n DIFFOUT_R36n AG33 DQ5R DQ2R DIFFIO_RX_R37p DIFFOUT_R37p VREERSBNO IO DIFFIO TX R38p DIFFOLIT R38r AD31 5B VREERSBNO IO DIFFIO RX R37n DIFFOLIT R37n W30 DOSn5R DO2R 5B VREFB5BN0 IO DIFFIO TX R38n DIFFOLIT R38n AD32 DO5R DO2R VREFB5BN0 IC DIFFIO RX R39p DIFFOUT R39p DQ5R VRFFB5BN0 IC DIFFIO TX R40p DIFFOUT R40p AF32 DQ5R DO2R VRFFB5BN0 DIFFIO RX R39n DIFFOUT R39n V31 DQ5R DO2R VRFFB5BN0 IC DIFFIO TX R40n DIFFOUT R40n AF32 VREFB5BN0 IC CLK6p DIFFIO RX R41p DIFFOUT R41p V28 AG34 DQ6R VREFB5BN0 IC DIFFIO TX R42p DIFFOUT R42p VREFB5BN0 CLK6n DIFFIO RX R41n DIFFOUT R41n V27 DIFFIO TX R42n DO6R VRFFB5BN0 IC DIFFOUT R42r AH34 DIFFIO RX R43p DIFFOUT R43p VRFFB5BN0 I AC33 DO6R FPLL BR CLKOUTO, FPLL BR CLKOUTD, FPLL BR FB VRFFB5BN0 IC DIFFIO TX R44p DIFFOUT R44p AF33 DO6R VREFB5BN0 IC DIFFIO_RX_R43n DIFFOUT_R43n AC34 DQ6R VREFB5BN0 IO FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn DIFFIO_TX_R44n DIFFOUT_R44n AE33 DQ6R VREFB5BN0 IO DIFFIO_RX_R45p DIFFOUT_R45p V24 DQS6R VREFB5BN0 IC DIFFIO_TX_R46p DIFFOUT_R46p AE34 DIFFIO_RX_R45n DIFFOUT_R45n VREFB5BN0 DQSn6F VREFB5BN0 I DIFFIO_TX_R46n DIFFOUT_R46n AD34 DQ6R VREFB5BN0 IC DIFFIO RX R47p DIFFOUT_R47p DQ6R VREFB5BN0 IO DIFFIO_TX_R48p DIFFOUT_R48p AB33 DQ6R 5B VREFB5BN0 IC DIFFIO_RX_R47n DIFFOUT_R47r V32 DQ6R VREFB5BN0 IC DIFFIO_TX_R48n DIFFOUT_R48r AB34 VREFB6AN0 IC DIFFIO_RX_R49p DIFFOUT_R49p DIFFIO_TX_R50p DIFFOUT_R50p VREFB6AN0 IC DIFFIO_RX_R49n DIFFOUT_R49n VREERGAND IC DIFFIO TX R50n DIFFOLIT R50n AA33 DQ7R 64 VREERGAND IO DIFFIO RX R51n DIFFOLIT R51n 1128 DO7R 6A VREERGAND IO EPIL TR CLKOUTO EPIL TR CLKOUTO EPIL TR EB DIFFIO TX R52p DIFFOLIT R52n Y34 DO7R 6A VREFB6AN0 IC DIFFIO RX R51n DIFFOUT R51n VREFB6AN0 I FPLL TR CLKOUT1.FPLL TR CLKOUTn DIFFIO TX R52n DIFFOUT R52r W34 DQ7R VRFFB6AN0 IC DIFFIO_RX_R53p DIFFOUT R53n DQS7R VREFB6AN0 DIFFIO TX R54p DIFFOUT R54p DOSn7R VREERGAND IO DIFFIO RX R53n DIFFOLIT R53n 1125 VREERGAND IO DIFFIO TX R54n DIFFOLIT R54n V/34 DO7R 6A VREFB6AN0 IO DIFFIO RX R55p DIFFOUT R55p R34 DQ7R VRFFB6ANO I DIFFIO TX R56p DIFFOUT R56p U34 DO7R DIFFIO RX R55n VRFFB6ANO IC DIFFOUT R55n P34 DQ7R VRFFB6AN0 IO DIFFIO TX R56n DIFFOUT R56n VREFB6AN0 IO CLK4p.FPLL TR FBc DIFFIO RX R57p DIFFOUT_R57p T31 DIFFIO_TX_R58p VREFB6AN0 IC DIFFOUT R58p DQ8R T30 VREFB6AN0 IC CLK4n,FPLL TR FBr DIFFIO RX R57n DIFFOUT R57r DIFFIO_TX_R58n VREFB6AN0 IC DIFFOUT_R58r DQ8F DIFFIO_RX_R59p VREFB6AN0 I DIFFOUT_R59p DQ8R DQ3R VREFB6AN0 IO DIFFIO_TX_R60p DIFFOUT_R60p M34 DQ8R DQ3R VREFB6AN0 IO DIFFIO_TX_R60n DIFFOUT_R60n M33 DQ8R DQ3R DIFFOUT_R61p U23 DQS8R VREFB6AN0 IC DIFFIO_TX_R62p DIFFOUT_R62p DIFFIO_RX_R61n DQSn8R VREFB6AN0 IO DIFFIO_TX_R62n DIFFOUT_R62n J34 DQ8R DQ3R VRFFB6AN0 IO DIFFIO_RX_R63p DIFFOUT_R63p DQ8R 6A VREFB6AN0 IO DIFFIO TX R64n DIFFOUT R64p 133 DQ8R DQ3R VREERGAND IO DIFFIO RX R63n DIFFOUT R63n N34 DQ8R DQ3R VREFB6AN0 IO DIFFIO_TX_R64n DIFFOUT_R64n

DIFFIO RX R65p

DIFFIO_TX_R66p

DIFFIO RX R65n

DIFFIO TX R66n

DIFFIO RX R67n

DIFFIO TX R68n

DIFFIO TX R68n

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DIFFOUT_R65p

DIFFOUT_R66p

DIFFOUT_R65n

DIFFOLIT Reen

DIFFOLIT R67n

DIFFOLIT R68n

DIFFOUT R68n

DIFFIO RX R67n DIFFOUT R67n

DIFFIO RX R69p DIFFOUT R69p

K33

K32

R27

H34

R28

H33

DQ9R

DO9R

DOGR

DOGR

DQ9R

DQ9R

DQS9R

64

64

6A

6A

VREFB6AN0

VREFB6AN0 IC

VRFFB6AN0 I

VREERGANO IO

VREERGAND IO

VREERGAND IO

VRFFB6AN0 IC

VRFFB6AN0 IC

VRFFB6ANO IO

DQ3R

DO3R

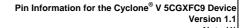
DO3R

DO3R

DQ3R

DQ3R

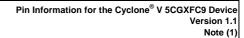
DQ3R



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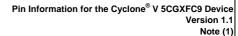
Note (1) Bank VRFF Pin Name/Function Optional Function(s) Configuration Function Dedicated Ty/Ry Emulated LVDS Output Channel F1152 DOS for X8 DOS for X16 HMC Pin Assignment HMC Pin Assignment Number hannel for DDR3/DDR2 (2) for LPDDR2 DIFFIO_TX_R70p DIFFOUT_R70p VREFB6AN0 IO N32 VREFB6AN0 IC DIFFIO RX R69n DIFFOUT_R69n DQSn9R DQ3R R25 DQ9R VRFFB6ANO I DIFFIO TX R70n DIFFOUT R70 VREFB6AN0 IO DIFFIO_RX_R71p DIFFOUT_R71p P32 DQ9R DQ3R VREFB6AN0 IO DIFFIO_TX_R72p DIFFOUT_R72p G34 DQ9R DQ3R VREFB6AN0 IO DIFFIO_RX_R71n DIFFOUT_R71n DQ3R P31 DQ9R DIFFIO_TX_R72n DIFFOUT_R72r VREFB6AN0 IC DIFFIO_RX_R73p DIFFOUT_R73p VREFB6AN0 IC DIFFIO_TX_R74p DIFFOUT_R74p DQ10R VREFB6AN0 IC DIFFIO_RX_R73n DIFFOUT_R73n VREFB6AN0 IO DIFFIO_TX_R74n DIFFOUT_R74n DQ10R DQ4R VREFB6AN0 IC DIFFIO_RX_R75p DIFFOUT_R75p L30 DQ10R VREFB6AN0 I DIFFIO_TX_R76p DIFFOUT_R76p DQ10R VREFB6AN0 IO DIFFIO_RX_R75n DIFFOUT_R75n DQ10R DQ4R DIFFIO TX R76n DIFFOUT_R76r DQ10R VREERGAND IO DIFFIO RX R77n DIFFOLIT R77n R23 DQS10R DOS4R 6A VREERGAND IO DIFFIO TX R78n DIFFOLIT R78n .131 6A VREFB6AN0 IC DIFFIO RX R77n DIFFOLIT R77n R24 DOSn10R DOSn4R VREFB6AN0 IC DIFFIO TX R78n DIFFOUT R78n DQ10R DQ4R VRFFB6AN0 IC DIFFIO RX R79p DIFFOUT R79p DQ10R DO4R VRFFB6AN0 DIFFIO TX R80p DIFFOUT R80g DQ10R DQ4R VRFFB6AN0 IC DIFFIO RX R79n DIFFOUT R79n M28 DQ10R DQ4R VREFB6AN0 IO DIFFIO TX R80n DIFFOUT R80n N29 VREFB6AN0 IC DIFFIO RX R81p DIFFOUT R81p P27 VREFB6AN0 DIFFIO TX R82p DIFFOUT R82p G31 DQ11R DQ4R DIFFIO RX R81n VRFFB6ANO IC DIFFOUT R81n VRFFB6AN0 I DIFFIO TX R82n DIFFOUT R82n DQ11R DQ4R G30 VRFFB6ANO IC DIFFIO RX R83p DIFFOUT R83p M29 DQ11R DQ4R VREFB6AN0 IC DIFFIO TX R84p DIFFOUT R84p DQ11R DQ4R VREFB6AN0 IO DIFFIO_RX_R83n DIFFOUT_R83n M30 DQ11R DQ4R VREFB6AN0 IO DIFFIO_TX_R84n DIFFOUT_R84n DQ11R DQ4R J29 VREFB6AN0 IC DIFFIO_RX_R85p DIFFOUT_R85p P24 DQS11R DQ4R VREFB6AN0 IC DIFFIO_TX_R86p DIFFOUT_R86p VREFB6AN0 I DIFFIO_RX_R85n DIFFOUT_R85n DQSn11R VREFB6AN0 IC DIFFIO_TX_R86n DIFFOUT_R86n DQ11R VREFB6AN0 IO DIFFIO_RX_R87p DIFFOUT_R87p L28 DQ11R VREFB6AN0 IO DIFFIO_TX_R88p DIFFOUT_R88p K29 DIFFIO_RX_R87n VREFB6AN0 IC DIFFOUT_R87r DQ11R VREFB6AN0 IO DIFFIO_TX_R88n DIFFOUT_R88n VREFB7AN0 IO DIFFIO_RX_T1p DIFFOUT_T1p VREERZANO IO DIFFIO TX T20 DIFFOLIT T2r DQ1T 7Α VREERZAND IO DIFFIO RX T1n DIFFOLIT T1n .125 7Δ VREERZAND IO DIFFIO TX T2n DIFFOLIT T2n H26 DO1T VRFFB7AN0 IC DIFFIO RX T3p DIFFOUT T30 DQ1T VRFFB7AN0 I DIFFIO TX T4n DIFFOUT T4r VRFFB7AN0 IC DIFFIO RX T3n DIFFOUT T3n DQ1T DQ1T VREFB7AN0 DIFFIO TX T4n DIFFOUT T4n M24 DOS1T VREERZANO IO DIFFIO RX T5n DIFFOLIT T5n VREERZAND IO DIFFIO TX T6n DIFFOLIT Ton F26 VREFB7AN0 IO DIFFIO RX T5n DIFFOUT T5n N24 DQSn1T VRFFB7AN0 I DIFFIO TX T6n DIFFOUT Ton DIFFIO RX T7p VRFFB7AN0 IO DIFFOUT T7p G24 VRFFB7AN0 IO DIFFIO TX T8p DIFFOUT T8p DO1T VREFB7AN0 IO DIFFIO RX T7n DIFFOUT_T7n H24 DQ1T DIFFIO_TX_T8n VREFB7AN0 IC DIFFOUT T8n E30 M25 DIFFIO RX T9p VREFB7AN0 IC DIFFOUT T90 VREFB7AN0 IC DIFFIO_TX_T10p T_DM_4 DIFFOUT_T10 DQ2T T_DM_4 DIFFIO_RX_T9n DIFFOUT_T9n VREFB7AN0 GND VREFB7AN0 DIFFIO_TX_T10n DIFFOUT_T10r F28 DQ2T DQ1T T_DQ_39 T_DQ_39 VREFB7AN0 IO DIFFIO_TX_T12p DIFFOUT_T12p C32 DQ2T DQ1T T_DQ_38 T_DQ_38 DIFFOUT_T11i D29 DQ2T T_DQ_36 DQ1T T_DQ_36 VREFB7AN0 IC DIFFIO_TX_T12n DIFFOUT_T12r DQ2T DQ1T GND T_DQS_ DQS2T T_DQS_4 VREFB7AN0 IO DIFFIO_TX_T14p DIFFOUT_T14p GND GND VRFFB7AN0 IO DIFFIO_RX_T13n DIFFOUT_T13r DQSn2T DQSn1T T_DQS#_ T_DQS#_ 7Α VREFB7AN0 IO DIFFIO TX T14n DIFFOUT T14n F28 DQ2T DQ1T T_DQ_35 T_DQ_35 VREERZANO IO DIFFIO RX T15n DIFFOUT T15 H23 DQ2T DQ1T T_DQ_33 VREFB7AN0 IO DIFFIO_TX_T16p DIFFOUT_T16 VRFFB7AN0 I DIFFIO RX T15n DIFFOUT_T15i T_DQ_32 T_DQ_3 VREFB7AN0 IC DIFFIO_TX_T16n DIFFOUT_T16r B30 GND GND VRFFB7AN0 I DIFFIO RX T17c DIFFOUT_T17 GND VREERZANO IO DIFFIO TX T18n DIFFOLIT T18r F24 DO3T DO1T T DM 3 T DM 3 VREERZAND IO DIFFIO RX T17n DIFFOLIT T17n K22 GND GND 7A VREERZANO IO DIFFIO TX T18n DIFFOLIT T18n F25 DO3T DO1T T DO 31 T DO 3 7A VRFFB7AN0 IC DIFFIO RX T19p DIFFOUT_T19p DQ3T DQ1T T DQ 29 T_DQ_29 VREFB7AN0 IC DIFFIO_TX_T20p DIFFOUT T20r DQ1T T DQ 30 T_DQ_30 T_DQ_28 VRFFB7AN0 IO DIFFIO RX T19n DIFFOUT T19n DQ3T DQ1T T_DQ_28

Pin List FE35



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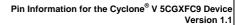
										Note (1)	
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IC			DIFFIO_TX_T20n	DIFFOUT_T20n	C28	DQ3T	DQ1T	GND	GND
7A	VREFB7AN0				DIFFIO_RX_T21p	DIFFOUT_T21p	M23	DQS3T	DQ1T		T_DQS_3
7A		10			DIFFIO_TX_T22p	DIFFOUT T22p	F27	D G CC .	DQ.		GND
7A		10			DIFFIO RX T21n	DIFFOUT_T21n	N23	DQSn3T	DQ1T		T_DQS#_3
7A		10			DIFFIO_TX_T22n	DIFFOUT_T22n	D26	DQ3T	DQ1T		T_DQ_27
7A	VRFFB7AN0	IC			DIFFIO_RX_T23p	DIFFOUT_T23p	H22	DQ3T	DQ1T		T_DQ_25
7A		10			DIFFIO_TX_T24p	DIFFOUT_T24p	B28	DQ3T	DQ1T		T_DQ_26
7A		10			DIFFIO RX T23n	DIFFOUT T23n	H21	DQ3T	DQ1T	T DQ 24	T DQ 24
7A		IO			DIFFIO_TX_T24n	DIFFOUT_T24n	B29	D GO!	DQ.		GND
7A	VRFFB7AN0	IC			DIFFIO_RX_T25p	DIFFOUT T25p	L21				GND
7A	VREFB7AN0	IC			DIFFIO_TX_T26p	DIFFOUT_T26p	E22	DQ4T	DQ2T	T_DM_2	T_DM_2
7A		10			DIFFIO_RX_T25n	DIFFOUT_T25n	L20				GND
		IC			DIFFIO TX T26n	DIFFOUT T26n	F23	DQ4T	DQ2T		T DQ 23
7A	VREFB7AN0	10			DIFFIO_RX_T27p	DIFFOUT_T27p	F21	DQ4T	DQ2T		T_DQ_21
7A	VRFFB7AN0				DIFFIO_TX_T28p	DIFFOUT_T28p	D27	DQ4T	DQ2T		T_DQ_22
7A	VREFB7AN0	10			DIFFIO_RX_T27n	DIFFOUT_T27n	G21	DQ4T	DQ2T		T_DQ_20
7A		10			DIFFIO_TX_T28n	DIFFOUT_T28n	C27	DQ4T	DQ2T		GND
7A		IC			DIFFIO_RX_T29p	DIFFOUT_T29p	N22	DQS4T	DQS2T		T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	D25				T_RESET#
7A		10			DIFFIO_RX_T29n	DIFFOUT T29n	M21	DQSn4T	DQSn2T	T_DQS#_2	T_DQS# 2
7A	VREFB7AN0	10			DIFFIO_TX_T30n	DIFFOUT_T30n	C26	DQ4T	DQ2T		T_DQ_19
7A	VREFB7AN0				DIFFIO_RX_T31p	DIFFOUT_T31p	F20	DQ4T	DQ2T		T_DQ_17
7A		IO IO			DIFFIO_TX_T32p	DIFFOUT_T32p	D24	DQ4T	DQ2T		T_DQ_18
7A	VREFB7AN0	Ю			DIFFIO_RX_T31n	DIFFOUT_T31n	G20	DQ4T	DQ2T		T_DQ_16
7A		10			DIFFIO_TX_T32n	DIFFOUT T32n	C24				GND
7A		IO	CLK11p		DIFFIO_RX_T33p	DIFFOUT_T33p	J20				
7A	VREFB7AN0				DIFFIO_TX_T34p	DIFFOUT_T34p	A28	DQ5T	DQ2T	T_DM_1	T_DM_1
7A		IC	CLK11n		DIFFIO RX T33n	DIFFOUT T33n	K19				
7A	VREFB7AN0	10			DIFFIO_TX_T34n	DIFFOUT_T34n	A27	DQ5T	DQ2T	T_DQ_15	T_DQ_15
7A		10			DIFFIO_RX_T35p	DIFFOUT T35p	D22	DQ5T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IC			DIFFIO_TX_T36p	DIFFOUT_T36p	B26	DQ5T	DQ2T		T_DQ_14
7A	VREFB7AN0				DIFFIO RX T35n	DIFFOUT T35n	C23	DQ5T	DQ2T		T DQ 12
7A	VREFB7AN0	IC			DIFFIO_TX_T36n	DIFFOUT_T36n	B25	DQ5T	DQ2T		T_CKE_0
7A	VREFB7AN0	IC			DIFFIO_RX_T37p	DIFFOUT_T37p	M20	DQS5T	DQ2T		T_DQS_1
7A		IC			DIFFIO_TX_T38p	DIFFOUT T38p	C22				T_CKE_1
7A	VREFB7AN0	IC			DIFFIO_RX_T37n	DIFFOUT_T37n	M19	DQSn5T	DQ2T		T_DQS#_1
7A		10			DIFFIO_TX_T38n	DIFFOUT_T38n	D21	DQ5T	DQ2T		T_DQ_11
7A		10			DIFFIO RX T39p	DIFFOUT T39p	F20	DQ5T	DQ2T		T DQ 9
7A	VREFB7AN0	IC			DIFFIO_TX_T40p	DIFFOUT_T40p	A26	DQ5T	DQ2T		T_DQ_10
7A		IC			DIFFIO RX T39n	DIFFOUT T39n	D20	DQ5T	DQ2T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IC			DIFFIO_TX_T40n	DIFFOUT_T40n	A25			GND	GND
7A		10	CLK10p		DIFFIO RX T41p	DIFFOUT T41p	H19			1	
7A	VREFB7AN0	10			DIFFIO_TX_T42p	DIFFOUT_T42p	B23	DQ6T		T_DM_0	T_DM_0
7A	VREFB7AN0	10	CLK10n		DIFFIO_RX_T41n	DIFFOUT_T41n	H18				
7A		10			DIFFIO_TX_T42n	DIFFOUT_T42n	B24	DQ6T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	Ю			DIFFIO_RX_T43p	DIFFOUT_T43p	C21	DQ6T		T_DQ_5	T_DQ_5
7A		Ю			DIFFIO_TX_T44p	DIFFOUT_T44p	A23	DQ6T			T_DQ_6
7A	VREFB7AN0	Ю			DIFFIO_RX_T43n	DIFFOUT_T43n	B21	DQ6T			T_DQ_4
7A	VREFB7AN0	10			DIFFIO_TX_T44n	DIFFOUT_T44n	A22	DQ6T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	10			DIFFIO_RX_T45p	DIFFOUT_T45p	M18	DQS6T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	10			DIFFIO_TX_T46p	DIFFOUT_T46p	E19			T_ODT_0	T_ODT_0
7A	VREFB7AN0	0			DIFFIO_RX_T45n	DIFFOUT_T45n	L18	DQSn6T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	10			DIFFIO_TX_T46n	DIFFOUT_T46n	D19	DQ6T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	10			DIFFIO_RX_T47p	DIFFOUT_T47p	B20	DQ6T			T_DQ_1
7A	VREFB7AN0	Ю			DIFFIO_TX_T48p	DIFFOUT_T48p	A21	DQ6T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	Ю			DIFFIO_RX_T47n	DIFFOUT_T47n	B19	DQ6T		T_DQ_0	T_DQ_0
7A	VREFB7AN0		RZQ_2		DIFFIO_TX_T48n	DIFFOUT_T48n	A20				
8A		10	CLK9p		DIFFIO_RX_T49p	DIFFOUT_T49p	G18				<u> </u>
8A		10			DIFFIO_TX_T50p	DIFFOUT_T50p	C18	DQ7T		T_A_0	T_CA_0
8A		10	CLK9n		DIFFIO_RX_T49n	DIFFOUT_T49n	F18				ļ
8A		10			DIFFIO_TX_T50n	DIFFOUT_T50n	C17	DQ7T			T_CA_1
	VICEIDONIO	10			DIFFIO_RX_T51p	DIFFOUT_T51p	E18	DQ7T	1		T_CA_4
8A		10	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	B18	DQ7T	1		T_CA_2
8A	VREFB8AN0				DIFFIO_RX_T51n	DIFFOUT_T51n	E17	DQ7T	ļ		T_CA_5
8A	VICEI BOTTE	10	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	A18	DQ7T	ļ		T_CA_3
8A	VREFB8AN0	10			DIFFIO_RX_T53p	DIFFOUT_T53p	M16	DQS7T	ļ		T_CK
8A		10			DIFFIO_TX_T54p	DIFFOUT_T54p	A17	L	<u> </u>		T_CA_6
8A		10			DIFFIO_RX_T53n	DIFFOUT_T53n	L17	DQSn7T	<u> </u>		T_CK#
8A	VREFB8AN0				DIFFIO_TX_T54n	DIFFOUT_T54n	A16	DQ7T	<u> </u>		T_CA_7
8A		10			DIFFIO_RX_T55p	DIFFOUT_T55p	C16	DQ7T		T_BA_1	
8A		10			DIFFIO_TX_T56p	DIFFOUT_T56p	B15	DQ7T		T_BA_0	ļ
	VICEIDONIO	10			DIFFIO_RX_T55n	DIFFOUT_T55n	B16	DQ7T		T_BA_2	ļ
8A		10			DIFFIO_TX_T56n	DIFFOUT_T56n	A15			GND	GND
8A	VREFB8AN0		CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	H17			L	
8A	VICEI BOTTE	10			DIFFIO_TX_T58p	DIFFOUT_T58p	A12	DQ8T	DQ3T	T_CAS#	
8A	VREFB8AN0	Ю	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T57n	DIFFOUT_T57n	H16	L	L	L	ļ
		10		ļ	DIFFIO_TX_T58n	DIFFOUT_T58n	A11	DQ8T	DQ3T	T_RAS#	
8A		10		ļ	DIFFIO_RX_T59p	DIFFOUT_T59p	F17	DQ8T	DQ3T	T_A_8	T_CA_8
8A	VREFB8AN0	10		l	DIFFIO_TX_T60p	DIFFOUT_T60p	B13	DQ8T	DQ3T	T_A_10	



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											Note (1
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignmen for LPDDR2
3A	VREFB8AN0	Ю			DIFFIO_RX_T59n	DIFFOUT_T59n	F16	DQ8T	DQ3T	T_A_9	T_CA_9
3A	VREFB8AN0	Ю			DIFFIO_TX_T60n	DIFFOUT_T60n	A13	DQ8T	DQ3T	T_A_11	
A		Ю			DIFFIO_RX_T61p	DIFFOUT_T61p	M15	DQS8T	DQS3T		T_CS#_0
A	VREFB8AN0	Ю			DIFFIO_TX_T62p	DIFFOUT_T62p	C14			T_A_12	
Ą		10			DIFFIO_RX_T61n	DIFFOUT_T61n	M14	DQSn8T	DQSn3T		T_CS#_1
A	VREFB8AN0				DIFFIO TX T62n	DIFFOUT_T62n	B14	DQ8T	DQ3T	T_A_13	
A	VREFB8AN0				DIFFIO_RX_T63p	DIFFOUT_T63p	D17	DQ8T	DQ3T	T_A_14	
A	VREFB8AN0	10			DIFFIO_TX_T64p	DIFFOUT_T64p	B10	DQ8T	DQ3T	T_WE#	
Α	VREFB8AN0 VREFB8AN0	10			DIFFIO_RX_T63n DIFFIO_TX_T64n	DIFFOUT_T63n DIFFOUT_T64n	D16 A10	DQ8T	DQ3T	T_A_15 GND	GND
A A	VREFB8AN0 VREFB8AN0	10			DIFFIO_IX_164n DIFFIO_RX_T65p	DIFFOUT_164h DIFFOUT_165p	F15			GND	GND
A A	VREFB8AN0 VREFB8AN0	10			DIFFIO_RX_165p	DIFFOUT_165p DIFFOUT_166p	F15 A7	DQ9T	DQ3T		
A	VREFB8AN0	10		1	DIFFIO_TX_T65n	DIFFOUT_165n	G15	DQ91	DQ31	+	
A A		10			DIFFIO_TX_T66n	DIFFOUT_T66n	A6	DQ9T	DQ3T		
A	VREFB8ANO	10			DIFFIO_RX_T67p	DIFFOUT_T67p	B8	DQ9T	DQ3T		
Α	V11121 D071110	10			DIFFIO_TX_T68p	DIFFOUT_T68p	C11	DQ9T	DQ3T		
Ä	VRFFB8AN0	IC			DIFFIO_RX_T67n	DIFFOUT T67n	A8	DQ9T	DO3T		
Ą	VREFB8AN0	IC			DIFFIO_TX_T68n	DIFFOUT_T68n	B11	DQ9T	DQ3T		
A	VREFB8AN0	IC			DIFFIO_RX_T69p	DIFFOUT_T69p	L16	DQS9T	DQ3T		
Ą	VREFB8AN0	IO .			DIFFIO_TX_T70p	DIFFOUT_T70p	C9				
A	VREFB8AN0	Ю			DIFFIO_RX_T69n	DIFFOUT_T69n	L15	DQSn9T	DQ3T		
Ą	VREFB8AN0	Ю			DIFFIO_TX_T70n	DIFFOUT_T70n	B9	DQ9T	DQ3T		
Ą	VREFB8AN0	Ю			DIFFIO_RX_T71p	DIFFOUT_T71p	E15	DQ9T	DQ3T		
A.	VREFB8AN0	Ю			DIFFIO_TX_T72p	DIFFOUT_T72p	C13	DQ9T	DQ3T		
4	VREFB8AN0	Ю			DIFFIO_RX_T71n	DIFFOUT_T71n	D15	DQ9T	DQ3T		
4	VREFB8AN0	Ю			DIFFIO_TX_T72n	DIFFOUT_T72n	C12				
4	VREFB8AN0	10			DIFFIO_RX_T73p	DIFFOUT_T73p	J15				· ·
4	VREFB8AN0	10		ļ	DIFFIO_TX_T74p	DIFFOUT_T74p	B5	DQ10T	DQ4T		
١	VREFB8AN0	10			DIFFIO_RX_T73n	DIFFOUT_T73n	K14				
4		10			DIFFIO_TX_T74n	DIFFOUT_T74n	A5	DQ10T	DQ4T		
4	VREFB8AN0	10			DIFFIO_RX_T75p	DIFFOUT_T75p	E14	DQ10T	DQ4T		
4	VREFB8AN0	10			DIFFIO_TX_T76p	DIFFOUT_T76p	C6	DQ10T	DQ4T		
١.	VREFB8AN0	10			DIFFIO_RX_T75n	DIFFOUT_T75n	D14	DQ10T	DQ4T		
Α	VREFB8AN0	10			DIFFIO_TX_T76n	DIFFOUT_T76n	B6	DQ10T	DQ4T		
١	VREFB8AN0	IO .			DIFFIO_RX_T77p	DIFFOUT_T77p	P14	DQS10T	DQS4T		
Α	VREFB8AN0	10			DIFFIO_TX_T78p	DIFFOUT_T78p	F13				
<u> </u>	VREFB8AN0 VREFB8AN0	10			DIFFIO_RX_T77n DIFFIO_TX_T78n	DIFFOUT_T77n DIFFOUT_T78n	N14 E13	DQSn10T DQ10T	DQSn4T DQ4T		
A		10		1			H14			+	
A A	VREFB8AN0 VREFB8AN0	10		1	DIFFIO_RX_T79p DIFFIO_TX_T80p	DIFFOUT_T79p DIFFOUT_T80p	R4	DQ10T DQ10T	DQ4T DQ4T	+	
Α	VREFB8AN0	0		1	DIFFIO_IX_T60p	DIFFOUT_T79n	G14	DQ10T	DQ4T	+	
A .	VREFB8AN0	10		1	DIFFIO_KX_17911	DIFFOUT T80n	A3	DQ101	DQ41		
Α.		10			DIFFIO_RX_T81p	DIFFOUT_T81p	M13				
A	VREFB8AN0				DIFFIO_TX_T82p	DIFFOUT_T82p	D11	DQ11T	DQ4T		
À	VREFB8AN0	10			DIFFIO_RX_T81n	DIFFOUT_T81n	L13	Dann	DQ		
A	VREFB8AN0	Ю		İ	DIFFIO_TX_T82n	DIFFOUT_T82n	D10	DQ11T	DQ4T		
	VREFB8AN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	G13	DQ11T	DQ4T		
4	VREFB8AN0	Ю			DIFFIO_TX_T84p	DIFFOUT_T84p	C8	DQ11T	DQ4T		
4	VREFB8AN0	10			DIFFIO_RX_T83n	DIFFOUT_T83n	H13	DQ11T	DQ4T		
A	VREFB8AN0	0			DIFFIO_TX_T84n	DIFFOUT_T84n	C7	DQ11T	DQ4T		
\	VREFB8AN0				DIFFIO_RX_T85p	DIFFOUT_T85p	N13	DQS11T	DQ4T		
١		10		ļ	DIFFIO_TX_T86p	DIFFOUT_T86p	A2		1		
١	VREFB8AN0	10		ļ	DIFFIO_RX_T85n	DIFFOUT_T85n	N12	DQSn11T	DQ4T		
A	VREFB8AN0	10			DIFFIO TX T86n	DIFFOUT_T86n	B3	DQ11T	DQ4T		
	VREFB8AN0			!	DIFFIO_RX_T87p	DIFFOUT_T87p	E12	DQ11T	DQ4T	+	
	VREFB8AN0	10		-	DIFFIO_TX_T88p	DIFFOUT_T88p	C1	DQ11T	DQ4T	1	
<u> </u>	VREFB8AN0 VREFB8AN0	<u>10</u>		1	DIFFIO_RX_T87n DIFFIO_TX_T88n	DIFFOUT_T87n DIFFOUT_T88n	D12 B1	DQ11T	DQ4T	 	
A	VREFB8AN0 VREFB8AN0	0	 	 		DIFFOUT_T88p	B1 L12	-	 	+	
λ λ	VREFB8AN0 VREFB8AN0	0	 	 	DIFFIO_RX_T89p DIFFIO_TX_T90p	DIFFOUT_T89p DIFFOUT_T90p	E10	DO12T	 	+	
	VREFB8AN0 VREFB8AN0		 	+	DIFFIO_IX_I90p DIFFIO_RX_T89n	DIFFOUT T89n	F10 K13	DQ12T	}	+	
\	VREFB8AN0	10	 	†	DIFFIO_TX_T90n	DIFFOUT_T89fi DIFFOUT_T90n	E10	DQ12T	 	1	
\	VREFB8AN0	10	 	†	DIFFIO_IX_T90II	DIFFOUT_190ff DIFFOUT_T91p	F12	DQ12T	†	1	
`	VREFB8AN0	10	 	†	DIFFIO_TX_T92p	DIFFOUT_191p DIFFOUT_T92p	F9	DQ12T	†	1	
	VREFB8AN0	IO	<u> </u>	1	DIFFIO_TX_T92p	DIFFOUT_T91n	F11	DQ12T	1	1	
	VREFB8AN0	Ю		1	DIFFIO_TX_T92n	DIFFOUT_T92n	D9	DQ12T			
`	VREFB8AN0	IO			DIFFIO_RX_T93p	DIFFOUT_T93p	L11	DQS12T			
À	VREFB8AN0	Ю			DIFFIO_TX_T94p	DIFFOUT_T94p	E7				
A	VREFB8AN0	Ю			DIFFIO_RX_T93n	DIFFOUT_T93n	K12	DQSn12T			
À		Ю			DIFFIO_TX_T94n	DIFFOUT_T94n	D7	DQ12T			
Ä		10			DIFFIO_RX_T95p	DIFFOUT_T95p	H12	DQ12T			
A	VREFB8AN0	Ю			DIFFIO_TX_T96p	DIFFOUT_T96p	F8	DQ12T			
A	VREFB8AN0	Ю			DIFFIO_RX_T95n	DIFFOUT_T95n	G11	DQ12T			
A	VREFB8AN0	Ю			DIFFIO_TX_T96n	DIFFOUT_T96n	E8				
A		MSEL0		MSEL0			J12				
A		CONF_DONE		CONF_DONE			G10				
A		MSEL1		MSEL1			J11				
A		nSTATUS		nSTATUS			G9				
	1	nCE	1	nCE	1	1	F7	I	1	1	

Pin List EF35



Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment	Note (
umber			(,,	, J	Channel					for DDR3/DDR2 (2)	for LPDDR2
	-			11051.5							
		MSEL2 MSEL3		MSEL2			F6				
		nCONFIG		MSEL3 nCONFIG			K10 G8				
<u> </u>		MSEL4		MSEL4			H7	+			
Δ.		GND		MOEL4			H8	-			
Α		GND					L24	-			
		GND					AP2				
		GND					AP4				
		GND					AP8				
		GND					AP13				
		GND					AP18				
		GND					AP23				
		GND					AP28				
		GND					AP33			_	
		GND					AN6				
		GND GND					AN15 AN25				
	+						AM3	+		_	
	+	GND GND	<u> </u>		+	+	AM3 AM12	1	+		
	1	GND		<u> </u>	†	+	AM22	1	-	1	1
	1	GND					AM32				
		GND			1		AL5	İ		1	1
		GND					AL9				
		GND					AL19				
		GND					AL29				
		GND					AL34				
		GND					AK1				
		GND					AK2				
		GND					AK3				
		GND					AK6 AK16				
		GND GND					AK16 AK26				
		GND					ANZO AJ3				
		GND					AJ4	-			
	+	GND					AJ5	+			
		GND					AJ13				
		GND					AJ23				
		GND					AJ33				
		GND					AH1				
		GND					AH2				
		GND					AH5				
		GND					AH10				
		GND					AH20				
		GND					AH30				
		GND					AG3				
	+	GND GND		 	+	+	AG4 AG5	+		+	
	+	GND			1	+	AG6	1			-
	1	GND			†	<u> </u>	AG7	1	<u> </u>		1
	1	GND					AG17				
		GND					AG27				
		GND					AF1				
		GND					AF2				
		GND					AF5				
		GND			1		AF6				L
		GND			1		AF7				
	1	GND					AF14				ļ
	+	GND			1		AF24	1	_	-	1
	+	GND			 		AF34	 			
	+	GND GND			+	+	AE3 AE4	+		-	
	+	GND	<u> </u>		+	+	AE4 AE5	1	+		1
	+	GND	<u> </u>	<u> </u>	+	+	AE6	1	+	+	1
	+	GND			1	+	AE7	1			1
	1	GND					AE8				
	1	GND					AE9				
	1	GND					AE11				
		GND					AE21				
•		GND					AF31				1

GND

GND GND GND GND GND

GND GND

GND GND GND

AE31

AD1 AD2 AD5 AD6 AD7

AD9 AD10

AD18 AD28 AC3



Pin Information for the Cyclone® V 5CGXFC9 Device Version 1.1 Note (1)

											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		GND					AC4				
		GND					AC5				i
		GND					AC6				
		GND					AC8				
		GND					AC10		ļ		
		GND					AC15		 	 	
		GND GND				 	AC25				———
		GND				 	AB1 AB2		 	+	
		GND				 	AB5		 	+	
		GND					AB6				
		GND					AB7				
		GND					AB9				
		GND					AB11				
		GND					AB12				
		GND					AB22				
		GND					AB32				
		GND					AA3				
		GND					AA4				
		GND					AA5				
		GND		 	 		AA6 AA8		 	 	1
		GND GND		-		t	AA8 AA10		 	 	
		GND		 	1	t	AA10 AA12	 	+	+	
		GND		 	 	 	AA12 AA14		+	+	
		GND				 	AA19		+	 	
		GND					AA29		†		
		GND		İ			AA34		1		
-		GND					Y1				1
		GND					Y2				
		GND					Y5				
		GND					Y6				
		GND					Y7				
		GND					Y9				
		GND					Y10				
		GND					Y11		<u> </u>		
		GND GND				 	Y13 Y15		<u> </u>	 	
		GND				 	Y15 Y17		 	+	
		GND				 	Y19		-	+	
		GND				 	Y21		1	 	
		GND				 	W3		1	 	
		GND					W4				
		GND					W5				i
		GND					W6				
		GND					W8				
		GND					W10				
		GND					W12				
		GND					W14				
		GND					W16				
		GND		 		 	W18		 	 	
		GND	 	-			W20		 	 	
		GND	+	 	1	t	W22		+	 	1
		GND GND					W23 W33		 	+	
		GND					V1		†		
		GND					V2		1		
		GND					V5		1		i
		GND					V6				i
		GND					V7				
		GND	-				V9		↓		
		GND				<u> </u>	V11		<u> </u>		
		GND					V13	└	<u> </u>	ļ	
		GND				 	V15	├		ļ	
		GND		1	1	 	V17	+	 	ļ	
		GND GND		 		 	V19 V21		 	 	
		GND	+	 	1	t	V21 V30		+	 	1
		GND		†		 	V30 U3		 	 	
		GND				 	U4		+	 	
		GND		†	1		U5	t	†	1	1
		GND					U6		1		i
		GND		İ			U8		1		1
		GND		İ			U10		1		1
		GND					U12				i
		GND					U14				ı .
							1140	$\overline{}$			
		GND					U16			1	'
		GND GND GND					U18 U20				



Sion 1.1

					Note (1)						
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignmen for LPDDR2
		GND					U22				ſ
		GND					U27				
		GND					T1				i
		GND					T2				
		GND					T5				i
		GND					T6				
		GND					T7				
		GND					T9				
		GND					T11				ł
		GND					T13				
		GND GND					T15 T17				——
		GND					T19				——
		GND					T21				
		GND					T24				ſ
		GND					T34				
		GND					R3				1
		GND					R4				1
		GND					R5				
		GND					R6				ĺ
		GND					R8				ĺ
		GND					R10				
		GND					R12				
		GND					R14				
		GND					R16				
	.	GND	1	1	ļ		R18	ļ	-	1	
	1	GND		1	-		R20	-	1	1	
		GND					R22 R31		-		
		GND GND		1	-		R31 P1	-	 	-	
				+							
		GND GND					P2 P5				·
		GND					P6				
		GND		†			P7				
		GND		†			P9				
		GND		†			P11				f
		GND					P13				ſ
		GND		1			P15				
		GND					P17				Ī
		GND					P19				Ī
		GND					P21				i
		GND					P28				i
		GND					N3				í
		GND					N4				ĺ
		GND					N5				í
		GND					N6				
		GND					N8				
		GND					N10				
		GND					N11				
		GND					N16				ł
		GND					N18			-	
	 	GND GND		 	 		N20 N25	 		-	
	 			 	 		N25 M1	 		-	
		GND GND	1	1	l		M1 M2	l	t	1	
	l .	GND	 	 	 		M5	 	I		ſ
	1	GND			†		M6	 	<u> </u>		
	1	GND	1	1	1		M7	1	t	1	í
		GND					M9		1		i
	İ	GND					M10		i e		i Total
		GND					M12		i e		i Total
		GND					M17				í
		GND					M22				i .
		GND					M32				
		GND					L3				
		GND					L4				
		GND				-	L5				
		GND					L6				
		GND					L7				
		GND					L8				
		GND					L9				ļ
		GND					L14				ļ
		GND					L19				ļ
		GND					L29				
		GND					L34				
		GND	ļ		ļ		K1	ļ			
		GND	ļ				K2				
		GND	1	ļ	ļ		K5	ļ		ļ	
	1	GND		l .	l	l	K6			1	



Note (1)

								Note (1)			
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignme for LPDDR2
		GND					K7				
		GND					K8				
		GND					K16				
		GND					K26				
		GND					J3				
		GND GND					J4 J5				
		GND		1	-		J13			<u> </u>	
		GND					J23				
		GND					J33				
		GND					H1				
		GND					H2				
		GND GND		1	-		H5 H10			-	
	1	GND				+	H10 H20				
		GND					H30				
		GND					G3				
		GND					G4				
		GND					G5				
		GND					G7				
		GND					G17				
	1	GND GND	+	+	 	+	G27 F1	 	1	 	1
	 	GND	<u> </u>	+	†		F1 F2	†	1	†	
	1	GND		1	†	İ	F5	1	1	†	1
		GND					F14				
		GND					F24				
		GND					F34				
		GND					E2				
		GND					E3				
		GND		1	-		E4 E5			-	
		GND GND					E11				
		GND					E21				
		GND					E31				
		GND					D1				
		GND					D2				
		GND					D5				
		GND					D8				
		GND					D18				
		GND GND		1	-		D28 D33			-	
		GND					C3				
		GND					C4				
		GND					C5				
		GND					C15				
		GND					C25				
		GND					B2				
		GND					B22				
		GND GND		1	-		B32 B34			-	
		GND		1	-		A4			 	
	1	GND					A9				
		GND					A19				
		GND					A29				
		VCC		ļ			N21				
	ļ	VCC				ļ	AA13				
	1	VCC		+	 	1	Y12	1	1	+	
	 	VCC VCC		+	-		Y14 Y16	-	-	-	-
	1	VCC	 	1	 		Y16 Y18	 	1	 	l
	1	VCC		1			W13	<u> </u>			
	İ	VCC		İ	İ		W15	İ		İ	İ
	<u> </u>	VCC					W17				
	1	VCC					W19				
	ļ	VCC		ļ			W21				ļ
	1	VCC		1	1	1	V12	1	1	1	1
	 	VCC		1	 	1	V14	 	1	 	-
	 	VCC		+	-	 	V16	-	-	-	-
	 	vcc vcc		†	 	1	V18 V20	 		 	
	1	VCC		1		1	V20 V22	-	<u> </u>		
	1	VCC		1	†	İ	U13	1	1	†	1
	İ	VCC		İ		<u> </u>	U15				
		VCC					U17				
		VCC					U19				
		VCC					U21				
		VCC					T12		<u> </u>		ļ
	1	VCC		1			T14		1		L

Pin List EF35

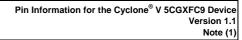


loto (1)

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					Note (1)						
lank lumber	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignmen
		VCC					T16				
		VCC					T18				
		VCC					T20				
		VCC					T22				
		VCC					R13				
		VCC					R15				
		VCC					R17				
		VCC					R19				
		VCC					R21				
		VCC					P12 P16				
		VCC VCC					P16 P18				
		VCC					P18 P20				
		VCC					P22				
		VCC					N15				
		VCC					N17				
		VCC					N19				
		DNU					D4				
		DNU					D3				
		DNU					AG9				
		DNU					AF17				
		DNU					J24				
	ļ	DNU					J17				
		VCCPGM					AF12				
		VCCPGM					AD27				
	 	VCCPGM		.	ļ		H11		-	ļ	
	 	VCCBAT		.	ļ		H9		-	ļ	
	 	VCCIO3A					AD13 AM7	-	-		
		VCCIO3A VCCIO3A	 	+	-		AM7 AK11	-	 	-	
		VCCIO3A VCCIO3A					AJ8 AG12				
		VCCIOSA VCCIOSA					AF9				
		VCCIO3A VCCIO3B					AP9 AB17				
		VCCIO3B VCCIO3B					AN10				
		VCCIO3B					AM17				
		VCCIO3B					AL14				
		VCCIO3B					AH15				
		VCCIO3B					AE16				
		VCCIO4A					AD23				
		VCCIO4A					AN20				
		VCCIO4A					AN30				
		VCCIO4A					AM27				
		VCCIO4A					AL24				
		VCCIO4A					AK21				
		VCCIO4A					AJ18				
		VCCIO4A					AJ28				
		VCCIO4A					AH25				
		VCCIO4A					AG22				
		VCCIO4A					AF19				
	 	VCCIO4A		-			AC20			-	
	 	VCCIO5A VCCIO5A		 	 		AA24 AK31			-	
	 	VCCIO5A VCCIO5A		 	 		AK31 AF29			-	
	l	VCCIOSA VCCIOSA	 	1	l		AF29 AE26		t	1	
	 	VCCIOSA VCCIOSA	<u> </u>	-	 		AB27		 		
	 	VCCIOSA VCCIOSA	<u> </u>	-	 		Y26		 		
	1	VCCIO5A VCCIO5B		t			V25		 		
		VCCIO5B					AG32		1		
		VCCIO5B					AD33		İ		
		VCCIO5B					AC30		İ		
		VCCIO5B					Y31				
		VCCIO5B					W28				
		VCCIO6A					G32				
		VCCIO6A					U32				
		VCCIO6A					T29				
		VCCIO6A					R26				
	l	VCCIO6A					P23				
		VCCIO6A					P33				
		VCCIO6A					N30				
		VCCIO6A					M27				
	ļ	VCCIO6A					K31				
	ļ	VCCIO6A					J28				
		VCCIO7A					A24				
		VCCIO7A					K21				
	ļ	VCCIO7A			ļ		J18				
		VCCIO7A		.	ļ		H25		-	ļ	
	1	VCCIO7A	1	l	l	l	G22	1		l	
		VCCIO7A					F19				

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											Note (1)
Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
		VCCIO7A					F29				
		VCCIO7A					E26				
		VCCIO7A					D23				
		VCCIO7A					C20				
		VCCIO7A					C30				
		VCCIO7A					B27				
		VCCIO8A					B17				
		VCCIO8A					K11				ĺ
		VCCIO8A					H15				1
		VCCIO8A					G12				
		VCCIO8A					F9				-
		VCCIO8A					E6				
		VCCIO8A VCCIO8A					E16 D13				
		VCCIO8A VCCIO8A					C10				
		VCCIO8A VCCIO8A					B7				
		VCCIOSA VCCIOSA					B12				
		VCCIO8A					A14				-
		VCCPD3A					AE15				-
		VCCPD3A					AE13				
		VCCPD3B4A		Ì			AE17				
		VCCPD3B4A					AF15				
		VCCPD3B4A					AF16				
		VCCPD3B4A					AF20				
		VCCPD3B4A					AF21				
		VCCPD3B4A					AE22				
		VCCPD5A					AA26				
		VCCPD5A					AB26				
		VCCPD5B					W25				ļ
		VCCPD5B					V26				L
		VCCPD6A					P26				
		VCCPD6A					U26				
		VCCPD6A					T26				
		VCCPD6A					N26				
		VCCPD7A8A VCCPD7A8A					J22 K15				
		VCCPD7A8A VCCPD7A8A					K17				
		VCCPD7A8A					K20				
		VCCPD7A8A VCCPD7A8A					J14				
		VCCPD7A8A					J16				
		VCCPD7A8A					J19				
		VCCPD7A8A					J21				
3A		VREFB3AN0					AH11				
3B	VREFB3BN0	VREFB3BN0					AH18				
4A		VREFB4AN0					AG20				
	VREFB5AN0	VREFB5AN0					AE27				
5B	VREFB5BN0	VREFB5BN0					V29				
		VREFB6AN0					P29				
7A	VREFB7AN0	VREFB7AN0					G19				
8A	VREFB8AN0	VREFB8AN0					G16				
		NC					AP3		ļ		
		NC					AN1				
		NC					AN2		ļ		
		NC			-		AN3			-	
<u> </u>		NC NC					AM1				
—		NC NC	 				AM2 AL1		-		
—		NC NC					AL1 AL2		-		
		NC NC					AL2 AL3				
		NC NC	 				AL3 AL4		l		
		NC NC					AK4				
		NC		1	l		AH6		1	l	i e
		NC NC					AH7				
		NC					AG8				
		NC					AF8				ſ
		NC					L10				
		NC					L26				
		NC					K9				
		NC					K27				
		NC				-	J6				
		NC					J7				
		NC	1				J8				
		NC	1				J9				
		NC					J27				
ļ		NC			ļ		H6		ļ	ļ	
		NC NC			 		G6			 	
 		NC NC					F31		 		
\vdash		NC NC		.			F32				



Version 1.1 Note (1)

Bank	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Din Accignment	HMC Pin Assignment
Number	AVEL	riii Name/Function	Optional Function(s)	Configuration Function	Channel	Emulated EVD3 Output Channel	F1152	DQ3 IOI A0	Des for A16	for DDR3/DDR2 (2)	for LPDDR2
radiiibei					Chamilei					IOI DDIKO/DDIKZ (2)	IOI LI DDILL
		NC					E32				
	1	NC					E33				
		NC					E34				
	1	NC					D6				
		NC					D31				
		NC				i	D32				
	1	NC					D34				
	1	NC					C2				
		NC					C19				
		NC				i	C33				
	1	NC					C34				
	1	NC					B33				
		NC					A30				
		NC					A31				
		NC					A32				
		NC				i	A33				
	1	VCCH_GXBL					N9				
	1	VCCH_GXBL					AB8				
		VCCH_GXBL				i	W9				
	1	VCCH_GXBL					T8				
		VCCL_GXBL					N7				
		VCCL GXBL					AC7				
	1	VCCL_GXBL					AA7				
	1	VCCL_GXBL					W7				
	1	VCCL GXBL					U7				
	1	VCCL_GXBL					R7				
	1	RREF_TL					E1				
	1	VCCA_FPLL					AC11				
		VCCA_FPLL					M11				
		VCCA_FPLL					AD26				
	1	VCCA_FPLL					M26				
		VCC_AUX					J10				
		VCC_AUX					K18				
		VCC_AUX					K24				
		VCC_AUX					AE24				
		VCC_AUX					AE18				
		VCC_AUX					AE12				
		VCCE_GXBL					P8				
		VCCE_GXBL					AD8				
		VCCE_GXBL					AC9				
		VCCE_GXBL					AA9				
		VCCE_GXBL					Y8				
		VCCE_GXBL					V8				
		VCCE_GXBL					U9				
		VCCE_GXBL					R9				
Notes:		VCCE_GXBL					M8				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the
<u>Cyclone V Device Family Pin Connection Guidelines.</u>
(2) RESET pin is only applicable for DDR3 device.



Pin Information for the Cyclone® V 5CGXFC9 Device Version 1.1

Version Number	Date	Changes Made
1.0	7/3/2012	Initial release.
1.1	5/22/2013	 - Added U484 package. - Updated the column from "HMC Pin Assignment for DDR3" to "HMC Pin Assignment for DDR3/DDR2". - Added notes to the "HMC Pin Assignment for DDR3/DDR2" and "HMC Pin Assignment for LPDDR2" columns.