TMDXEVM6657L / TMDXEVM6657LE Technical Reference Manual Version 1.1

Literature Number: SPRUHG7
Revised August 2012

EVALUATION BOARD/KIT/MODULE (EVM) WARNINGS, RESTRICTIONS AND DISCLAIMER

Not for Diagnostic Use: For Feasibility Evaluation Only in Laboratory/Development Environments

The EVM may not be used for diagnostic purposes.

This EVM is intended solely for evaluation and development purposes. It is not intended for use and may not be used as all or part of an end equipment product.

This EVM should be used solely by qualified engineers and technicians who are familiar with the risks associated with handling electrical and mechanical components, systems and subsystems.

Your Obligations and Responsibilities

Please consult the EVM documentation, including but not limited to any user guides, set up guides or getting started guides and other warnings prior to using the EVM. Any use of the EVM outside of the specified operating range may cause danger to the users and/or produce unintended results, inaccurate operation, and permanent damage to the EVM and associated electronics. You acknowledge and agree that:

You are responsible for compliance with all applicable Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, UL, CSA, VDE, CE, RoHS and WEEE,) that relate to your use (and that of your employees, contractors or designees) of the EVM for evaluation, testing and other purposes.

You are responsible for the safety of you and your employees and contractors when using or handling the EVM. Further, you are responsible for ensuring that any contacts or interfaces between the EVM and any human body are designed to be safe and to avoid the risk of electrical shock.

You will defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, “Claims”) arising out of or in connection with any use of the EVM that is not in accordance with the terms of this agreement. This obligation shall apply whether Claims arise under the law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

Warning

The EVM board may get very hot during use. Specifically, the DSP, its heat sink and power supply circuits all heat up during operation. This will not harm the EVM. Use care when touching the unit when operating or allow it to cool after use before handling. If unit is operated in an environment that limits free air flow, a fan may be needed.

Preface

About this Document

This document is a Technical Reference Manual for the TMS320C6657 Evaluation Module (C6657 Lite EVM) designed and developed by eInfochips Limited for Texas Instruments, Inc.

Notational Conventions

This document uses the following conventions:

Program listings, program examples, and interactive displays are shown in a mono-spaced font. Examples use **bold** for emphasis, and interactive displays use bold to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Square brackets ([and]) identify an optional parameter. If you use an optional parameter, you specify the information within the brackets. Unless the square brackets are in a bold typeface, do not enter the brackets themselves.

Underlined, italicized non-bold text in a command is used to mark place holder text that should be replaced by the appropriate value for the user's configuration.

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Document Revision History

Release	Chapter	Description of Change
0.1	All	Initial Draft
1.1	1.1	TMDXEVM6657LE image changed

Acronyms

Acronym	Description
AMC or AdvancedMC	Advanced Mezzanine Card
CCS	Code Composer Studio
DDR3	Double Data Rate 3 Interface
DIP	Dual-In-Line Package
DSP	Digital Signal Processor
DTE	Data Terminal Equipment
EEPROM	Electrically Erasable Programmable Read Only Memory
EMAC	Ethernet Media Access Controller
EMIF	External Memory Interface
EVM	Evaluation Module
FPGA	Field Programmable Gate Array
I2C	Inter Integrated Circuit
IPMB	Intelligent Platform Management Bus
IPMI	Intelligent Platform Management Interface
JTAG	Joint Test Action Group
LED	Light Emitting Diode
McBSP	Multi Channel Buffered Serial Port
MCH	MicroTCA Carrier Hub
MTCA or MicroTCA	Micro Telecommunication Computing Architecture
MMC	Module Management Controller
PCIe	PCI Express
PICMG®	PCI Industrial Computer Manufacturers Group
RFU	Reserved for Future Use
SDRAM	Synchronous Dynamic Random Access Memory
SERDES	Serializer-Deserializer
SGMII	Serial Gigabit Media Independent Interface
SRIO	Serial RapidIO
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
XDS560v2	Texas Instruments' System Trace Emulator

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1. Overview

This chapter provides an overview of the C6657 Lite EVM along with the key features and block diagram.

1.1 Key Features

The C6657 Lite EVM is a high performance, cost-efficient, standalone development platform that enables users to evaluate and develop applications for the Texas Instruments' TMS320C6657 Digital Signal Processor (DSP). The Evaluation Module (EVM) also serves as a hardware reference design platform for the TMS320C6657 DSP. The EVM's form-factor is equivalent to a single-wide PICMG® AMC.0 R2.0 AdvancedMC module.

TMDSEVM6657LE comes with an integrated, high speed, system trace capable XDS560v2 Mezzanine Emulator

Schematics, code examples and application notes are available, to ease the hardware development process and to reduce the time to market.

The key features of the C6657 Lite EVM are:

- Texas Instruments' fixed point DSP - TMS320C6657
- 512 Mbytes of DDR3 Memory (up to 1024Mbytes supported)
- 128 Mbytes of NAND Flash
- 16 Mbytes of NOR Flash
- One Gigabit Ethernet port supporting 10/100/1000 Mbps data rate – switched between RJ-45 connector and AMC fingers
- 170 pin B+ style AMC Interface
- High performance connector for HyperLink
- 128 kbytes I2C EEPROM for booting
- 4 User Indication LEDs, 4 Software Controlled LEDs and 3 User DIP Switches
- RS232 Serial interface on 3-Pin header or UART over mini-USB connector
- UPP, Timer, SPI, McBSP, UART interfaces on 80-pin expansion header
- On-Board XDS100 type Emulation using USB 2.0 interface
- TI 60-Pin JTAG header to support External Emulator[1]
- High Speed Integrated XDS560v2 Mezzanine Emulator[2]
- Module Management Controller (MMC) for Intelligent Platform Management Interface (IPMI)
- Powered by DC power-brick adaptor (12V/2.5A) or AMC Carrier back-plane
- PICMG® AMC.0 R2.0 single width, full height AdvancedMC module

Note: **[1] - Available in TMDXEVM6657L only.**
[2] - Available in TMDXEVM6657LE only.

1.2 Functional Overview

The C6657 Lite EVM contains dual TMS320C6657 fixed point Digital Signal Processor. The TMS320C6657 device is based on the third-generation high-performance, advanced VelociTI™ very-long-instruction-word (VLIW) architecture, developed by Texas Instruments (TI), designed specifically for high density wireline / wireless media gateway infrastructure. This device is an excellent choice for IP border gateways, video transcoding and translation, video-server and intelligent voice and video recognition applications. The C66x devices are backward code-compatible from previous devices that are part of the C6000™ DSP platform.

The functional block diagram of TMDXEVM6657L is shown in below figure:

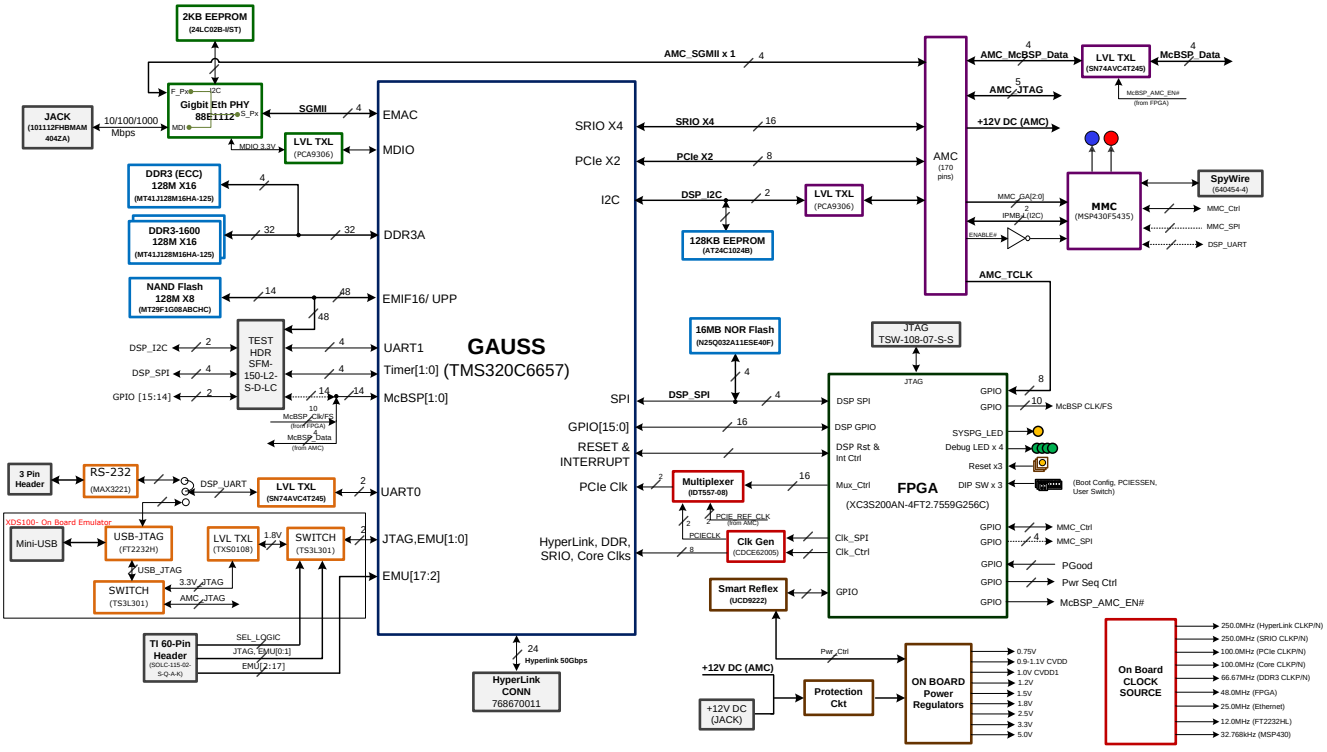


Figure 1.1: Block Diagram of TMDXEVM6657L

The functional block diagram of TMDXEVM6657LE is shown in below figure:

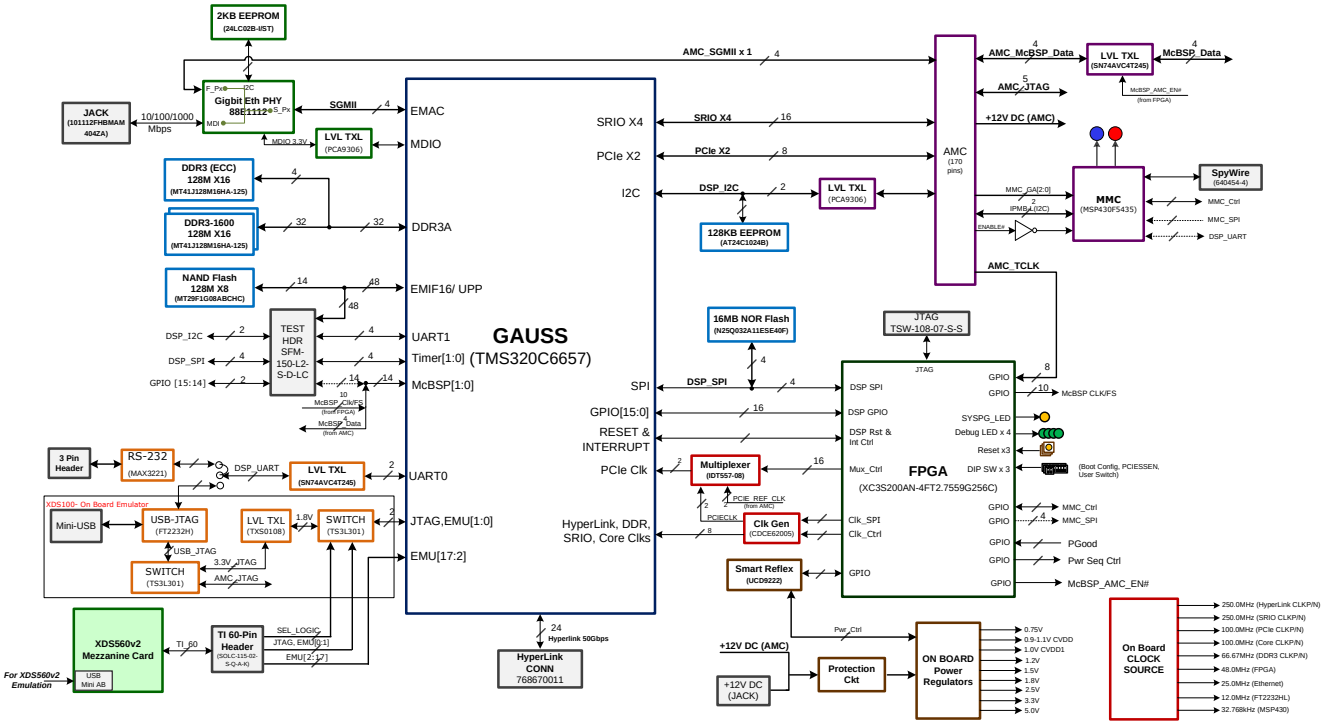


Figure 1.2: Block Diagram of TMDXEVM6657LE

1.3 Basic Operation

The C6657 Lite EVM platform is designed to work with TI's Code Composer Studio (CCS) development environment and ships with a version specifically tailored for this board. CCS can interfaces with the board via on-board emulation circuitry using the USB cable supplied along with this EVM or through external emulator.

The EVM comes with the Texas Instruments Multicore Software Development Kit (MCSDK) for SYS/BIOS OS. The BIOS MCSDK provides the core foundational building blocks that facilitate application software development on TI's high performance and multicore DSPs. It also includes an out-of-box demonstration. Follow the instruction in BIOS MCSDK Getting Started Guide to install all the necessary development tools, drivers and documentation.

To start operating the board, follow instructions in the Quick Start Guide. This guide provides instruction for proper connections and configuration for running the POST and OOB Demos. After completing the POST and OOB Demos, proceed with installing CCS and the EVM support files by following the instructions on the DVD. This process will install all the necessary development tools, drivers and documentation.

After the installation is completed, follow below steps to run Code Composer Studio.

1. Power ON the board using power brick adaptor (12V/2.5A) supplied along with this EVM or Insert this EVM board into MicroTCA chassis or AMC carrier back-plane.
2. Connect USB cable from host PC to EVM board.
3. Launch Code Composer Studio from host PC by double clicking on its icon at PC desktop.

Detailed information about the EVM including examples and reference material is available in the DVD available with this EVM kit.

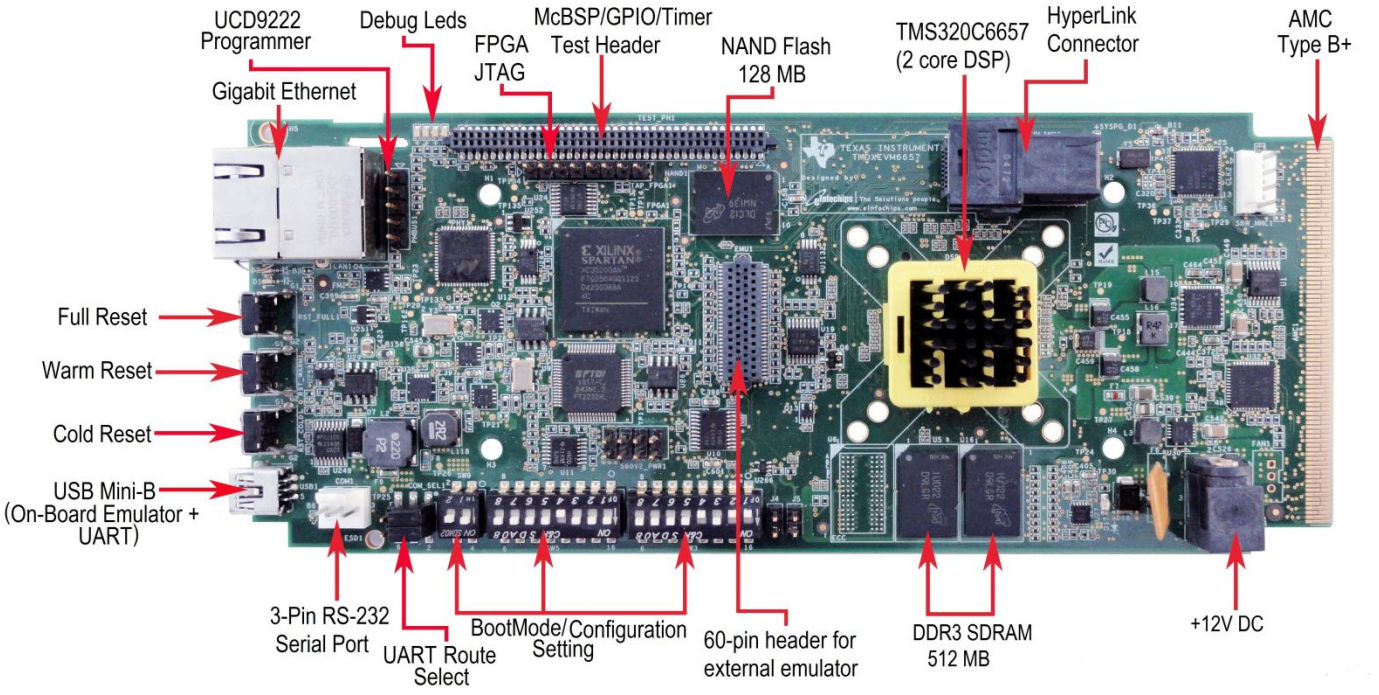


Figure 1.3: TMDXEVM6657L

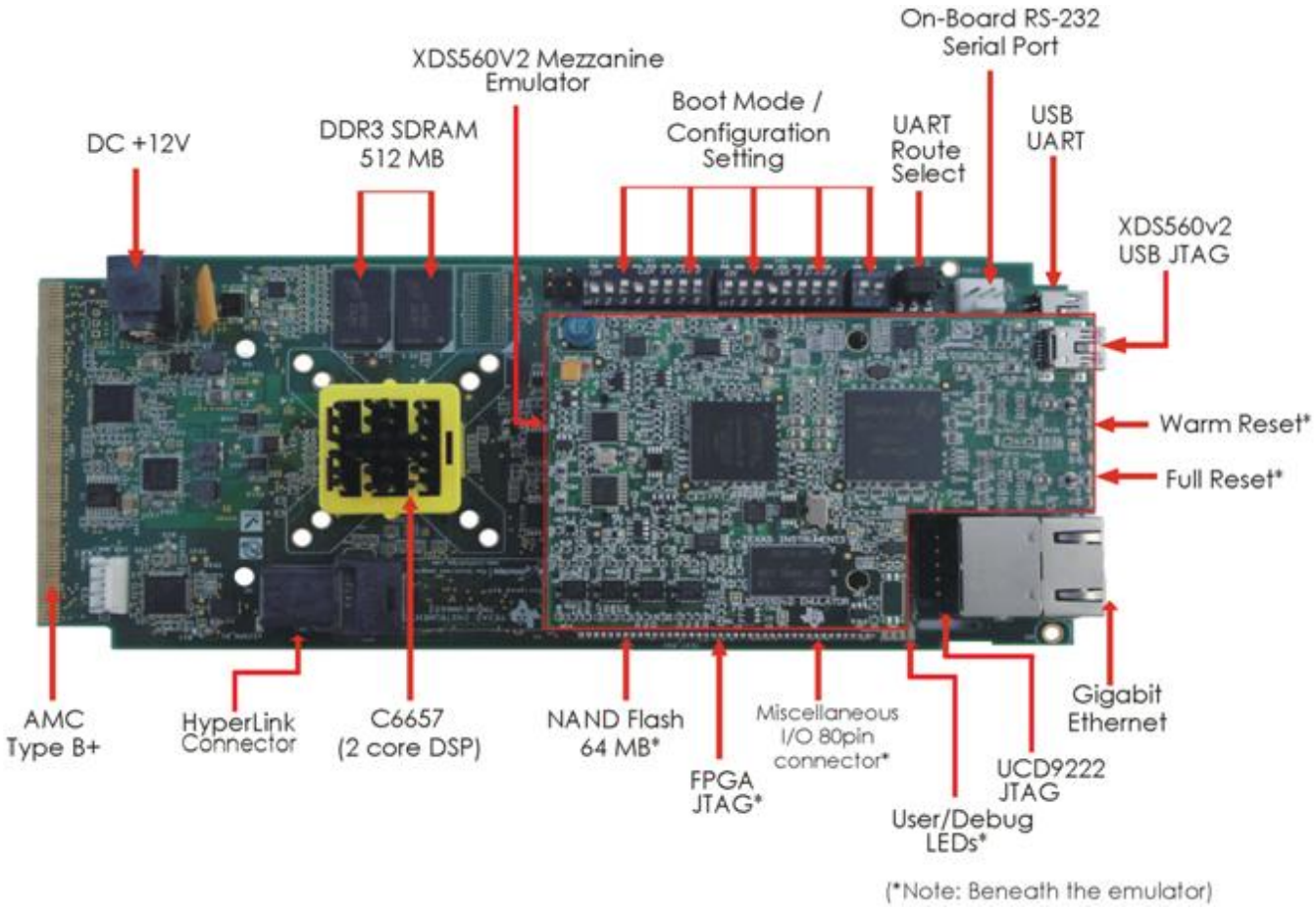


Figure 1.4: TMDXEVM6657LE

1.4 Boot Mode and Boot Configuration Switch Setting

The C6657 Lite EVM has 18 sliding DIP switches (Board Ref. SW3, SW5 and SW9) to determine boot mode, boot configuration, device number, Endian mode, CorePac PLL clock and PCIe mode selection. Mode selection options latch at every reset of the DSP.

1.5 Power Supply

C6657 Lite EVM can be powered from a single +12V / 2.5A DC (30W) external power supply connected to the DC power jack (DC_IN1)). Internally, +12V input is converted into required voltage levels using local DC-DC converters.

- CVDD (+0.90V~+1.05V) used for the DSP Core logic
- +1.0V is used for DSP internal memory and HyperLink/SRIO/SGMII/PCIe SERDES termination of DSP
- +1.5V is used for DDR3 buffers of DSP, HyperLink/SRIO/SGMII/PCIe SERDES regulators in DSP and DDR3 DRAM chips
- +1.8V is used for DSP PLLs, DSP LVCMOS I/Os and FPGA I/Os driving the DSP
- +2.5V is used for Gigabit Ethernet PHY core
- +1.2V is used for FPGA core and Gigabit Ethernet PHY core
- +3.3V is used for FPGA I/Os
- +5V and +3.3V is used to power optional XDS560v2 Mezzanine card
- The DC power jack connector is a 2.5mm barrel-type plug with center-tip as positive polarity

The C6657 Lite EVM can also draw power from the AMC edge connector (AMC1). If the board is inserted into a PICMG® MicroTCA.0 R1.0 compliant system chassis or AMC Carrier back-plane, an external +12V supply from DC jack (DC_IN1) is not required.

2. Introduction to the C6657 Lite EVM board

This chapter provides an introduction and details of interfaces for the C6657 Lite EVM board. It contains:

2.1 Memory Map

The memory map of the TMS320C6657 device is as shown in Table 2.1. The external memory configuration register address ranges in the C6657 device begin at the hex address location 0x7000 0000 for EMIFA and hex address location 0x7800 0000 for DDR3 Memory Controller.

Table 2.1: TMS320C6657 Memory Map

Logical 32-bit Address		Physical 36-bit Address		Bytes	Description
Start	End	Start	End		
00000000	007FFFFF	0 00000000	0 007FFFFF	8M	Reserved
00800000	008FFFFF	0 00800000	0 008FFFFF	1M	Local L2 SRAM
00900000	00DFFFFF	0 00900000	0 00DFFFFF	5M	Reserved
00E00000	00E07FFF	0 00E00000	0 00E07FFF	32K	Local L1P SRAM
00E08000	00EFFFFF	0 00E08000	0 00EFFFFF	1M-32K	Reserved
00F00000	00F07FFF	0 00F00000	0 00F07FFF	32K	Local L1D SRAM
00F08000	017FFFFF	0 00F08000	0 017FFFFF	9M-32K	Reserved
01800000	01BFFFFF	0 01800000	0 01BFFFFF	4M	C66x CorePac Registers
01C00000	01CFFFFF	0 01C00000	0 01CFFFFF	1M	Reserved
01D00000	01D0007F	0 01D00000	0 01D0007F	128	Trace 0
01D00080	01D07FFF	0 01D00080	0 01D07FFF	32K-128	Reserved
01D08000	01D0807F	0 01D08000	0 01D0807F	128	Trace 1 (C6657) or Reserved (C6655)
01D08080	01D3FFFF	0 01D08080	0 01D3FFFF	224K-128	Reserved
01D40000	01D4007F	0 01D40000	0 01D4007F	128	Trace 2 (C6657) or Trace 1 (C6655)
01D40080	01D47FFF	0 01D40080	0 01D47FFF	32K-128	Reserved
01D48000	01D4807F	0 01D48000	0 01D4807F	128	Trace 3 (C6657) or Trace 2 (C6655)
01D48080	01D4FFFF	0 01D48080	0 01D4FFFF	32K-128	Reserved
01D50000	01D5007F	0 01D50000	0 01D5007F	128	Trace 4 (C6657) or Reserved (C6655)
01D50080	01D57FFF	0 01D50080	0 01D57FFF	32K-128	Reserved
01D58000	01D5807F	0 01D58000	0 01D5807F	128	Trace 5 (C6657) or Trace 3 (C6655)
01D58080	01D5FFFF	0 01D58080	0 01D5FFFF	4464K -128	Reserved
021B4000	021B47FF	0 021B4000	0 021B47FF	2K	McBSP0 Registers
021B4800	021B5FFF	0 021B4800	0 021B5FFF	6K	Reserved
021B6000	021B67FF	0 021B6000	0 021B67FF	2K	McBSP0 FIFO Registers
021B6800	021B7FFF	0 021B6800	0 021B7FFF	6K	Reserved
021B8000	021B87FF	0 021B8000	0 021B87FF	2K	McBSP1 Registers
021B8800	021B9FFF	0 021B8800	0 021B9FFF	6K	Reserved
021BA000	021BA7FF	0 021BA000	0 021BA7FF	2K	McBSP1 FIFO Registers
021BA800	021BFFFF	0 021BA800	0 021BFFFF	22K	Reserved
021C0000	021C03FF	0 021C0000	0 021C03FF	1K	TCP3d Registers
021C0400	021CFFFF	0 021C0400	0 021CFFFF	63K	Reserved
021D0000	021D00FF	0 021D0000	0 021D00FF	256	VCP2-A Registers
021D0100	021D3FFF	0 021D0100	0 021D3FFF	16K - 256	Reserved
021D4000	021D40FF	0 021D4000	0 021D40FF	256	VCP2-B Registers
021D4100	021FFFFF	0 021D4100	0 021FFFFF	176K - 256	Reserved
02200000	0220007F	0 02200000	0 0220007F	128	Timer0
02200080	0220FFFF	0 02200080	0 0220FFFF	64K-128	Reserved
02210000	0221007F	0 02210000	0 0221007F	128	Timer1
02210080	0221FFFF	0 02210080	0 0221FFFF	64K-128	Reserved
02220000	0222007F	0 02220000	0 0222007F	128	Timer2

Logical 32-bit Address		Physical 36-bit Address			
Start	End	Start	End	Bytes	Description
02220080	0222FFFF	0 02220080	0 0222FFFF	64K-128	Reserved
02230000	0223007F	0 02230000	0 0223007F	128	Timer3
02230080	0223FFFF	0 02230080	0 0223FFFF	64K-128	Reserved
02240000	0224007F	0 02240000	0 0224007F	128	Timer4
02240080	0224FFFF	0 02240080	0 0224FFFF	64K-128	Reserved
02250000	0225007F	0 02250000	0 0225007F	128	Timer5
02250080	0225FFFF	0 02250080	0 0225FFFF	64K-128	Reserved
02260000	0226007F	0 02260000	0 0226007F	128	Timer6
02260080	0226FFFF	0 02260080	0 0226FFFF	64K-128	Reserved
02270000	0227007F	0 02270000	0 0227007F	128	Timer7
02270080	0230FFFF	0 02270080	0 0230FFFF	640K - 128	Reserved
02310000	023101FF	0 02310000	0 023101FF	512	PLL Controller
02310200	0231FFFF	0 02310200	0 0231FFFF	64K-512	Reserved
02320000	023200FF	0 02320000	0 023200FF	256	GPIO
02320100	0232FFFF	0 02320100	0 0232FFFF	64K-256	Reserved
02330000	023303FF	0 02330000	0 023303FF	1K	SmartReflex
02330400	0234FFFF	0 02330400	0 0234FFFF	127K	Reserved
02350000	02350FFF	0 02350000	0 02350FFF	4K	Power Sleep Controller (PSC)
02351000	0235FFFF	0 02351000	0 0235FFFF	64K-4K	Reserved
02360000	023603FF	0 02360000	0 023603FF	1K	Memory Protection Unit (MPU) 0
02360400	02367FFF	0 02360400	0 02367FFF	31K	Reserved
02368000	023683FF	0 02368000	0 023683FF	1K	Memory Protection Unit (MPU) 1
02368400	0236FFFF	0 02368400	0 0236FFFF	31K	Reserved
02370000	023703FF	0 02370000	0 023703FF	1K	Memory Protection Unit (MPU) 2
02370400	02377FFF	0 02370400	0 02377FFF	31K	Reserved
02378000	023783FF	0 02378000	0 023783FF	1K	Memory Protection Unit (MPU) 3
02378400	0237FFFF	0 02378400	0 0237FFFF	31K	Reserved
02380000	023803FF	0 02380000	0 023803FF	1K	Memory Protection Unit (MPU) 4
02380400	0243FFFF	0 02380400	0 0243FFFF	767K	Reserved
02440000	02443FFF	0 02440000	0 02443FFF	16K	DSP trace formatter 0
02444000	0244FFFF	0 02444000	0 0244FFFF	48K	Reserved
02450000	02453FFF	0 02450000	0 02453FFF	16K	DSP trace formatter 1 (C6657) or Reserved (C6655)
02454000	02521FFF	0 02454000	0 02521FFF	824K	Reserved
02522000	02522FFF	0 02522000	0 02522FFF	4K	Efuse
02523000	0252FFFF	0 02523000	0 0252FFFF	52K	Reserved
02530000	0253007F	0 02530000	0 0253007F	128	I^2C data & control
02530080	0253FFFF	0 02530080	0 0253FFFF	64K-128	Reserved
02540000	0254003F	0 02540000	0 0254003F	64	UART 0
02540400	0254FFFF	0 02540400	0 0254FFFF	64K-64	Reserved
02550000	0255003F	0 02550000	0 0255003F	64	UART 1
02550040	0257FFFF	0 02550040	0 0257FFFF	192K-64	Reserved
02580000	02580FFF	0 02580000	0 02580FFF	4K	UPP
02581000	025FFFFF	0 02581000	0 025FFFFF	508K	Reserved

Logical 32-bit Address		Physical 36-bit Address		Bytes	Description
Start	End	Start	End		
02600000	02601FFF	0 02600000	0 02601FFF	8K	Secondary Interrupt Controller (INTC) 0
02602000	02603FFF	0 02602000	0 02603FFF	8K	Reserved
02604000	02605FFF	0 02604000	0 02605FFF	8K	Secondary Interrupt Controller (INTC) 1
02606000	02607FFF	0 02606000	0 02607FFF	8K	Reserved
02608000	02609FFF	0 02608000	0 02609FFF	8K	Secondary Interrupt Controller (INTC) 2
0260A000	0261FFFF	0 0260A000	0 0261FFFF	88K	Reserved
02620000	026207FF	0 02620000	0 026207FF	2K	Chip-Level Registers
02620800	0263FFFF	0 02620800	0 0263FFFF	126K	Reserved
02640000	026407FF	0 02640000	0 026407FF	2K	Semaphore
02640800	0273FFFF	0 02640800	0 0273FFFF	1022K	Reserved
02740000	02747FFF	0 02740000	0 02747FFF	32K	EDMA Channel Controller (TPCC)
02748000	0278FFFF	0 02748000	0 0278FFFF	288K	Reserved
02790000	027903FF	0 02790000	0 027903FF	1K	EDMA TPCC Transfer Controller (TPTC) 0
02790400	02797FFF	0 02790400	0 02797FFF	31K	Reserved
02798000	027983FF	0 02798000	0 027983FF	1K	EDMA TPCC Transfer Controller (TPTC) 1
02798400	0279FFFF	0 02798400	0 0279FFFF	31K	Reserved
027A0000	027A03FF	0 027A0000	0 027A03FF	1K	EDMA TPCC Transfer Controller (TPTC) 2
027A0400	027A7FFF	0 027A0400	0 027A7FFF	31K	Reserved
027A8000	027A83FF	0 027A8000	0 027A83FF	1K	EDMA TPCC Transfer Controller (TPTC) 3
027A8400	027CFFFF	0 027A8400	0 027CFFFF	159K	Reserved
027D0000	027D0FFF	0 027D0000	0 027D0FFF	4K	TI embedded trace buffer (TETB) - CorePac0
027D1000	027DFFFF	0 027D1000	0 027DFFFF	60K	Reserved
027E0000	027E0FFF	0 027E0000	0 027E0FFF	4K	TI embedded trace buffer (TETB) - CorePac1 (C6657) or Reserved (C6655)
027E1000	0284FFFF	0 027E1000	0 0284FFFF	444K	Reserved
02850000	02857FFF	0 02850000	0 02857FFF	32K	TI embedded trace buffer (TETB) — system
02858000	028FFFFF	0 02858000	0 028FFFFF	672K	Reserved
02900000	02920FFF	0 02900000	0 02920FFF	132K	Serial RapidIO (SRIO) configuration
02921000	029FFFFF	0 02921000	0 029FFFFF	1M-132K	Reserved
02A00000	02AFFFFF	0 02A00000	0 02AFFFFF	1M	Queue manager subsystem configuration
02B00000	02C07FFF	0 02B00000	0 02C07FFF	1056K	Reserved
02C08000	02C8BFFF	0 02C08000	0 02C8BFFF	16K	EMAC subsystem configuration
02C0C000	07FFFFFF	0 02C0C000	0 07FFFFFF	84M - 48K	Reserved
08000000	0800FFFF	0 08000000	0 0800FFFF	64K	Extended memory controller (XMC) configuration
08010000	0BBFFFFF	0 08010000	0 0BBFFFFF	60M-64K	Reserved
0BC00000	0BCFFFFF	0 0BC00000	0 0BCFFFFF	1M	Multicore shared memory controller (MSMC) config
0BD00000	0BFFFFFF	0 0BD00000	0 0BFFFFFF	3M	Reserved
0C000000	0C1FFFFF	0 0C000000	0 0C1FFFFF	1M	Multicore shared memory (MSM)
0C200000	107FFFFF	0 0C200000	0 107FFFFF	71 M	Reserved
10800000	108FFFFF	0 10800000	0 108FFFFF	1M	CorePac0 L2 SRAM
10900000	10DFFFFF	0 10900000	0 10DFFFFF	5M	Reserved
10E00000	10E07FFF	0 10E00000	0 10E07FFF	32K	CorePac0 L1P SRAM
10E08000	10EFFFFF	0 10E08000	0 10EFFFFF	1M-32K	Reserved

Logical 32-bit Address		Physical 36-bit Address			
Start	End	Start	End	Bytes	Description
10F00000	10F07FFF	0 10F00000	0 10F07FFF	32K	CorePac0 L1D SRAM
10F08000	117FFFFF	0 10F08000	0 117FFFFF	9M-32K	Reserved
11800000	118FFFFF	0 11800000	0 118FFFFF	1M	CorePac1 L2 SRAM (C6657) or Reserved (C6655)
11900000	11DFFFFF	0 11900000	0 11DFFFFF	5M	Reserved
11E00000	11E07FFF	0 11E00000	0 11E07FFF	32K	CorePac1 L1P SRAM (C6657) or Reserved (C6655)
11E08000	11EFFFFF	0 11E08000	0 11EFFFFF	1M-32K	Reserved
11F00000	11F07FFF	0 11F00000	0 11F07FFF	32K	CorePac1 L1D SRAM (C6657) or Reserved (C6655)
11F08000	1FFFFFFF	0 11F08000	0 1FFFFFFF	225M-32K	Reserved
20000000	200FFFFF	0 20000000	0 200FFFFF	1M	System trace manager (STM) configuration
20100000	207FFFFF	0 20100000	0 207FFFFF	7M	Reserved
20800000	208FFFFF	0 20080000	0 208FFFFF	1M	TCP3d Data
20900000	20AFFFFF	0 20900000	0 20AFFFFF	2M	Reserved
20B00000	20B1FFFF	0 20B00000	0 20B1FFFF	128K	Boot ROM
20B20000	20BEFFFF	0 20B20000	0 20BEFFFF	832K	Reserved
20BF0000	20BF01FF	0 20BF0000	0 20BF01FF	512	SPI
20BF0400	20BFFFFF	0 20BF0400	0 20BFFFFF	64K -512	Reserved
20C00000	20C000FF	0 20C00000	0 20C000FF	256	EMIF16 config
20C00100	20FFFFFF	0 20C00100	0 20FFFFFF	4M - 256	Reserved
21000000	210001FF	0 21000000	0 210001FF	512	DDR3 EMIF configuration
21000200	213FFFFF	0 21000200	0 213FFFFF	4M-512	Reserved
21400000	214000FF	0 21400000	0 214000FF	256	HyperLink config
21400100	217FFFFF	0 21400100	0 217FFFFF	4M-256	Reserved
21800000	21807FFF	0 21800000	0 21807FFF	32K	PCIe config
21808000	33FFFFFF	0 21808000	0 33FFFFFF	8M-32K	Reserved
22000000	22000FFF	0 22000000	0 22000FFF	4K	McBSP 0 FIFO Data
22000100	223FFFFF	0 22000100	0 223FFFFF	4M-4K	Reserved
22400000	22400FFF	0 22400000	0 22400FFF	4K	McBSP 1FIFO Data
22400100	229FFFFF	0 22400100	0 229FFFFF	6M-4K	Reserved
22A00000	22A0FFFF	0 22A00000	0 22A0FFFF	64K	VCP2-A
22A01000	22AFFFFF	0 22A01000	0 22AFFFFF	1M-64K	Reserved
22B00000	22B0FFFF	0 22B00000	0 22B0FFFF	64K	VCP2-B
22B01000	33FFFFFF	0 22B01000	0 33FFFFFF	277M-64K	Reserved
34000000	341FFFFF	0 34000000	0 341FFFFF	2M	Queue manager subsystem data
34200000	3FFFFFFF	0 34200000	0 3FFFFFFF	190M	Reserved
40000000	4FFFFFFF	0 40000000	0 4FFFFFFF	256M	HyperLink data
50000000	5FFFFFFF	0 50000000	0 5FFFFFFF	256M	Reserved
60000000	6FFFFFFF	0 60000000	0 6FFFFFFF	256M	PCIe data
70000000	73FFFFFF	0 70000000	0 73FFFFFF	64M	EMIF16 CS2 data space, supports NAND, NOR, or SRAM memory [1]
74000000	77FFFFFF	0 74000000	0 77FFFFFF	64M	EMIF16 CS3 data space, supports NAND, NOR, or SRAM memory [1]
78000000	7BFFFFFF	0 78000000	0 7BFFFFFF	64M	EMIF16 CS4 data space, supports NAND, NOR, or SRAM memory [1]
7C000000	7FFFFFFF	0 7C000000	0 7FFFFFFF	64M	EMIF16 CS5 data space, supports NAND, NOR or SRAM memory [1]
80000000	FFFFFFFF	8 80000000	8 FFFFFFFF	2G	DDR3 EMIF data

2.2 EVM Boot mode and Boot Configuration Switch Settings

C6657 Lite EVM has three configuration switches SW3, SW5 and SW9 that contain 18 values latched when reset is released. This occurs when power is applied the board, after the user presses the FULL_RESET push button or after a POR reset is requested from the MMC.

SW3, SW5 and SW9 determine general DSP configuration, Little or Big Endian mode and boot device selection, DSP boot device configuration, CorePac PLL setting and PCIe mode selection and enable.

Please refer to Section 3.3 of this document for default switch setting and details of each switch. For more information on DSP supported Bootmode, refer TMS320C6657 Datasheet and C66x Boot Loader User Guide.

Table 2.2: Boot Configuration Selection

DIP Switch	DSP GPIO/ BM	Primary Function	Selection
SW3 (Pin 1)	ENDIANESS	ENDIANESS	0 - Big Endian 1 - Little Endian
SW3 (Pins [5:2])	BOOTMODE[3:0]	BOOTMODE Device	0000 - Sleep/EMIF16 0001 - SRIO X010 - Ethernet 0011 - NAND 0100 - PCIe X101 - I2C Master 0101 - I2C Slave X110 - SPI 0111 - HyperLink 1000 - UART
SW3 (Pins [6:8]) SW5 (Pins [1:3])	BOOTMODE[9:4]	Boot Device Configuration	Depends on Boot Mode Selection
SW5 (Pins [6:4])	BOOTMODE[12:10]	PLL Multiplier/I2C (Input Clock Frequency)	000 - 50.00 MHz 001 - 66.67 MHz 010 - 80.00 MHz 011 - 100.00 MHz 100 - 156.25 MHz 101 - 250.00 MHz 110 - 312.50 MHz 111 - 122.88 MHz
SW5 (Pins [8:7])	PCIESSMODE[1:0]	Endpt/RootComplex	00 - End-point mode 01 - Legacy End-point mode (support for legacy INTx) 10 - Root complex mode 11 - Reserved
SW9 (Pin 1)	PCIESSEN	PCIESSEN	0 - PCIe module disabled 1 - PCIe module enabled

2.3 Board Revision ID

Board PCB (Printed Circuit Board) and PCA (Printed Circuit Assembly) revision are located below RJ-45 Jack in bottom silk, as shown in Figure 2.1. Table 3 describes the PCA/PCB revisions.

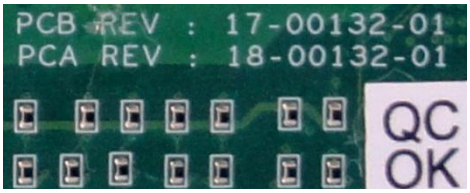


Figure 2.1: EVM Board Revision

Table 2.3: PCA/PCB revision description

PCA Rev	PCB Rev	Description
18-00132-01	17-00132-01	Proto + Alpha Build (Initial engineering samples)
18-00132-02	17-00132-02	Beta Build

Note: Last two digits represent major PCB / PCA revision number.

2.4 JTAG - Emulation Overview

2.4.1 JTAG – TMDXEVM6657L

C6657 Lite EVM has on-board embedded JTAG emulation circuitry; hence user does not require any external emulator to connect EVM with Code Composer Studio. User can connect CCS with target DSP in EVM through USB cable supplied along with this board. The EVM supports two different types of DSP Emulation - “USB mini-B” and “60-pin TI JTAG-DSP”. USB emulation is supported through an on-board, optimized XDS100-class embedded emulation circuit.

In case user wishes to connect external emulator to EVM, the TI 60-pin JTAG header (EMU1) is provided on-board for high speed real-time emulation. The TI 60-pin JTAG supports all standard (XDS510 or XDS560) TI DSP emulators. Please refer to the documentation supplied with your emulator for connection assistance.

On-board embedded JTAG emulator is the default connection to DSP, however when external emulator is connected to EVM, board circuitry switches automatically to give DSP’s emulation access to external emulator. When on-board emulator and external emulator both are connected at the same time, external emulator has priority and on-board emulator is disconnected from DSP.

DSP can also be accessed through the JTAG port on the AMC edge connector. Users who want to connect the DSP through AMC backplane even when XDS100 on-board emulator or 60-pin header with the external emulator is connected can do so by installing jumpers on J4 and J5.

The JTAG interface among the DSP, on-board emulator, external emulator and the AMC edge connector is shown in the below figure.

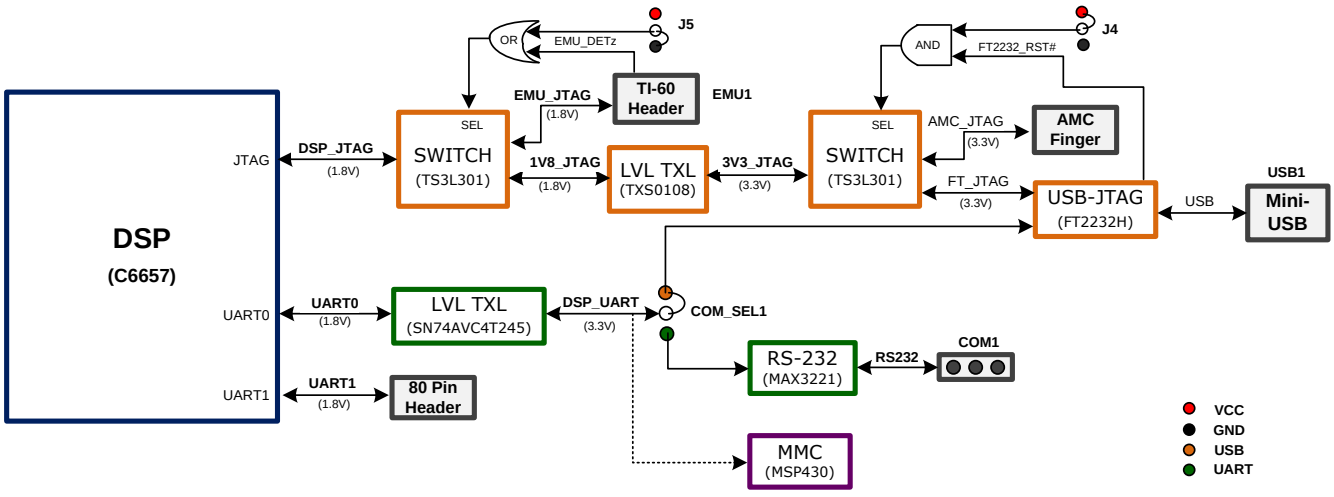


Figure 2.2: TMDXEVM6657L JTAG emulation

2.4.2 JTAG – TMDXEVM6657LE

In TMDXEVM6657LE, high speed real time emulation can be performed without needing an external emulator as it has an integrated, system trace capable XDS560v2 Mezzanine Emulator mounted on its TI 60-pin JTAG header (EMU1). User can connect the EVM to CCS by connecting the USB port of XDS560 Mezzanine Emulator to PC using USB cable supplied with an EVM.

The default priority of high speed XDS560v2 Emulator (when mounted on TI 60-pin header) can be over-ridden, to access the low speed XDS100 emulation, by installing jumper J5.

DSP can also be accessed through the JTAG port on the AMC edge connector. Users who want to connect the DSP through AMC backplane even when XDS100 on-board emulator or 60-pin header with the external emulator is connected can do so by installing jumpers on J4 and J5. For details please refer to table 2.3.

It is important to note that for XDS560v2 emulation, the USB cable needs to be connected to the mini-AB connector (J1) on XDS560v2 Mezzanine Emulator and not to mini-B connector (J11) on the main board. For TMDXEVM6657LE, the mini-B connector (J11) on the main board can be used to access UART-over-USB. Please refer to Section 2.15 of this document for more details.

The interface between DSP and XDS560v2 Mezzanine Emulator is shown in figure below:

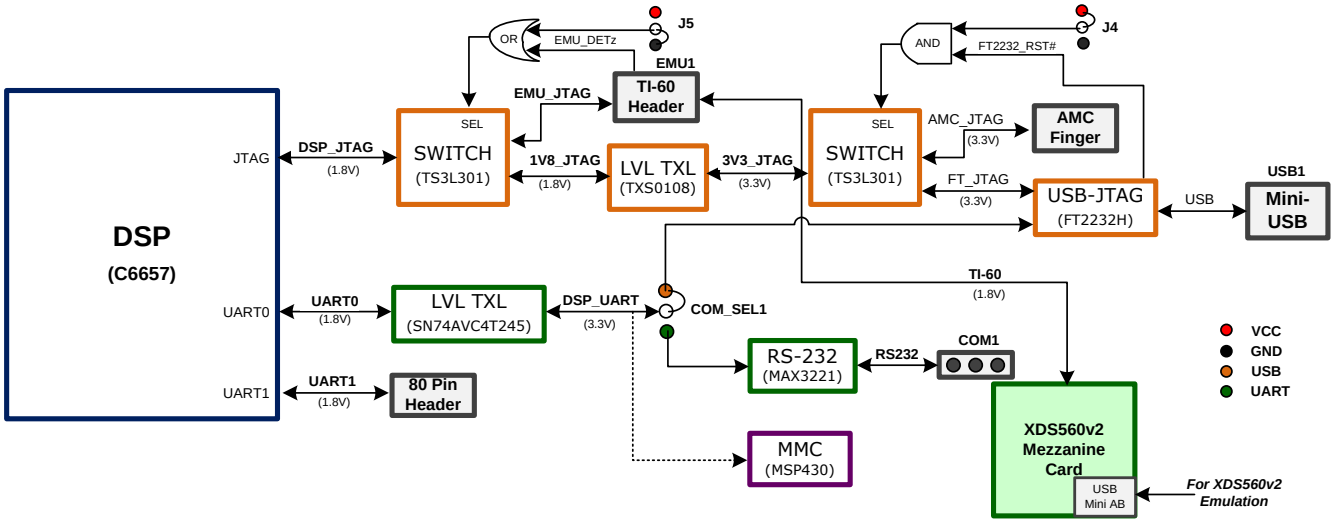


Figure 2.3: TMDXEVM6657LE JTAG Emulation

Table 2.4: Emulator Selection using J4 and J5

J4	J5	Emulator Accessible		
		XDS560v2 Mezzanine	XDS100	AMC
Open	Open	Yes	Yes	Yes
Open	Short	No	Yes	Yes
Short	Open	Yes	No	Yes
Short	Short	No	No	Yes

Note: The left most emulator has the highest priority. If it is accessible & connected, the lower priority emulators cannot be connected.

2.4.2.1. XDS560v2 Mezzanine Emulator Booting

When TMDXEVM6657LE is powered ON, the XDS560v2 Mezzanine Emulator starts booting. It takes approximately half minute to boot-up. The successful booting of XDS560v2 Mezzanine Emulator is indicated by following LEDs sequence:

- Green LED (D3) turns ON
- Yellow LED (D2) and Red LED (D1) turns ON
- Green LED (D3) blinks and turns OFF

After the completion of booting XDS560v2 mezzanine emulator is ready to interface with CCS. Once CCS is connected to the target DSP Green LED D4 turns ON.

The boot failure is indicated by simultaneous blinking of Red LED (D1), Yellow LED (D2) and Green LED (D3). In this case, CCS can't be connected to XDS560v2 mezzanine emulator. The boot failure can happen when Mezzanine emulator is attempted to mount over a non-compatible base EVM.

2.5 Clock Domains

The EVM incorporates variety of clocks to the TMS320C6657 as well as other devices which are configured automatically during the power up configuration sequence. The figure below illustrates the clocking for the system in EVM module.

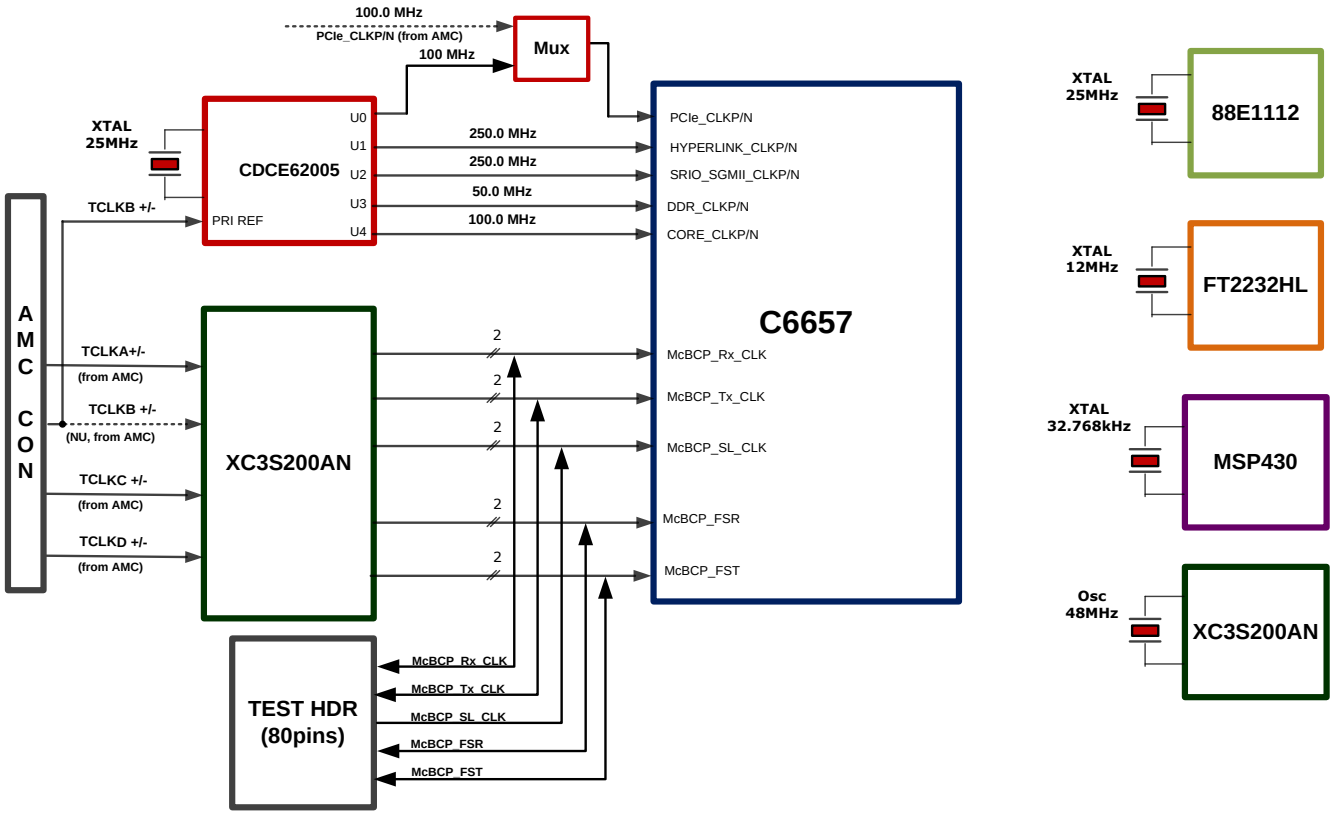


Figure 2.3: C6657 Lite EVM Clock Domains

Table 2.5: Clock Configuration

Clock	Frequency	Description
CORECLKP/N	100.00MHz	Core Clock Input for DSP (Differential)
DDRCLKP/N	50.00MHz	DDR3 Clock Input for DSP (Differential)
DSP_PCIECLKP/N	100.00MHz	PCIe Clock Input for DSP (Differential)
HyperLink_CLKP/N	250.00MHz	Hyperlink Clock Input for DSP (Differential)
SRIOSGMIICLKP/N	250.00MHz	SRIO SGMII Clock Input for DSP (Differential)
TCLKAP/N	16.384MHz	Clock Input for McBSP Interface (Differential)
TCLKBP/N	25.00MHz	Clock Reference for CLK1(Differential)
TCLKCP/N	8.00KHz	Frame Sync Input for McBSP Interface (Differential)
TCLKDP/N	TBD	RFU (Differentail)

2.6 I2C Boot EEPROM / SPI NOR Flash

The I2C modules on the TMS320C6657 may be used by the DSP to control local peripheral ICs (DACs, ADCs, etc.) or may be used to communicate with other controllers in a system or to implement a user interface.

The I2C bus is connected to one EEPROM and to the 80-pin expansion header (TEST_PH1). There are two banks in the I2C EEPROM which respond separately at addresses 0x50 and 0x51. These banks can be loaded with demonstration programs. Currently, the bank at 0x50 contains the I2C boot code and PLL initialization procedure and the bank at 0x51 contains the second level boot-loader program. The second level boot-loader can be used to either run the POST program or launch the OOB demonstration from NOR flash memory.

The Serial Peripheral Interconnect (SPI) module provides an interface between the DSP and other SPI-compliant devices. The primary intent of this interface is to allow for connection to a SPI ROM for boot. The SPI module on TMS320C6657 is supported only in Master mode.

16MB NOR FLASH (part number N25Q032A11 from NUMONYX) is attached to CS0z on TMS320C6657. It contains demonstration programs such as POST or OOB demo. The CS1z of SPI is used by the DSP to access registers within FPGA.

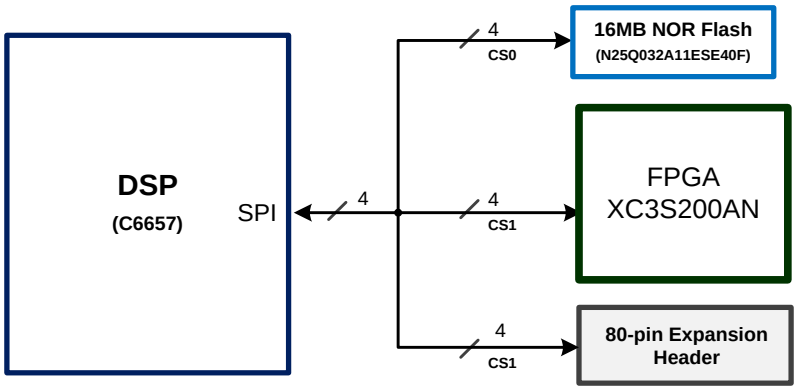


Figure 2.4: C6657 Lite EVM Clock Domains

2.7 FPGA

The FPGA (Xilinx XC3S200AN) controls the reset mechanism of the DSP and provides boot mode and boot configuration data to the DSP through SW3, SW5 and SW9. FPGA also provides the transformation of McBSP Frame Sync and Clock between AMC connector and the DSP. The FPGA also supports 4 user LEDs and 1 user switch through control registers. All FPGA registers are accessible over the SPI interface.

The figure below shows the interface between FPGA, DSP and other peripherals.

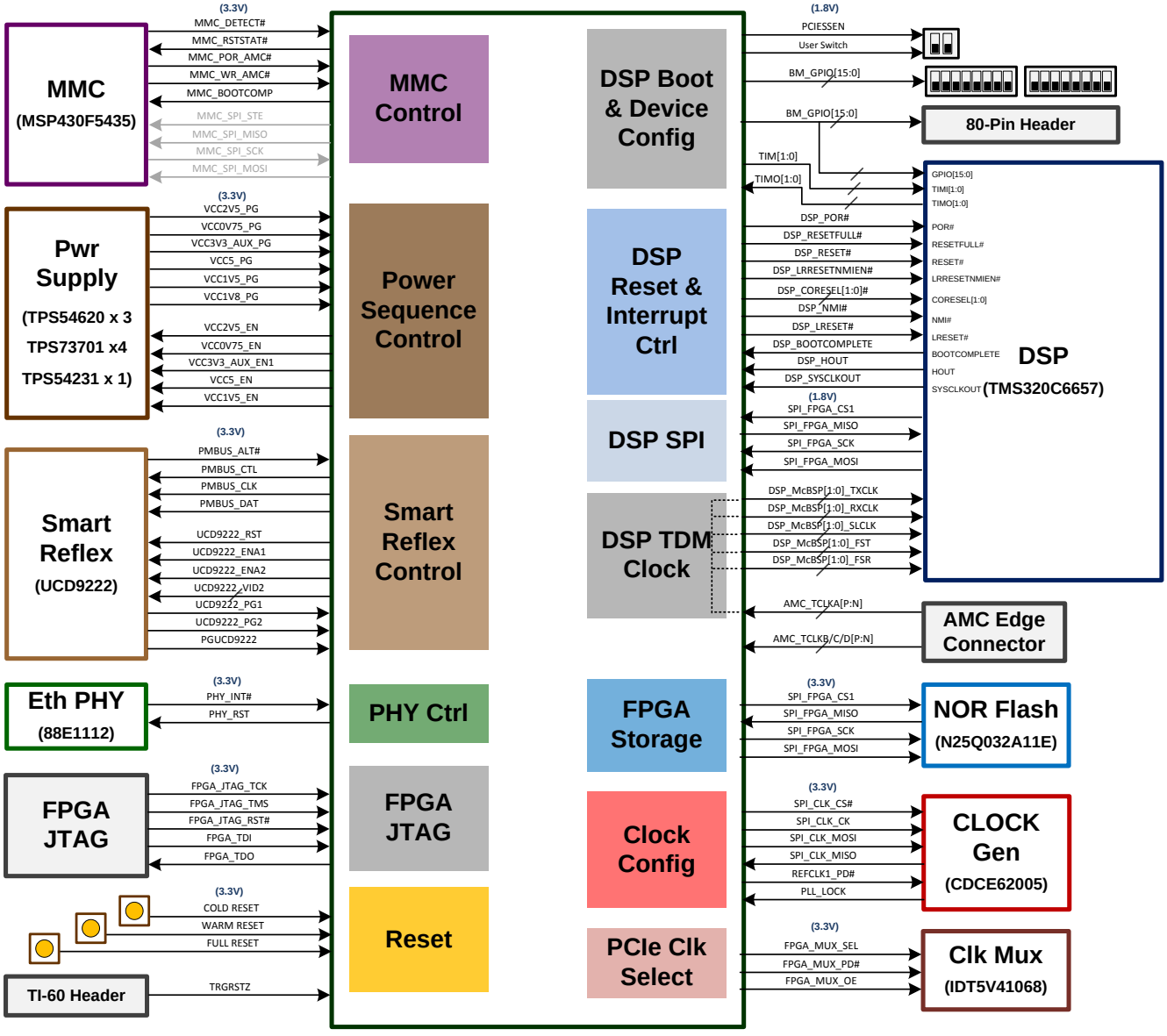


Figure 2.5: C6657 Lite EVM FPGA Connections

2.8 Ethernet Switch

The C6657 Lite EVM supports 1 port of SGMII interface which is multiplexed between Gigabit RJ-45 connector (Copper interface) and AMC finger (backplane SGMII interface) using a Gigabit Ethernet PHY Switch 88E1112 from Marvell. This SGMII port can be accessed either over RJ-45 Jack or AMC fingers (when inserted in chassis) but not both of them simultaneously. When both of them are connected, the default priority is given to RJ-45 Jack.

The figure below shows the interface between the DSP and Ethernet PHY (PHY1):

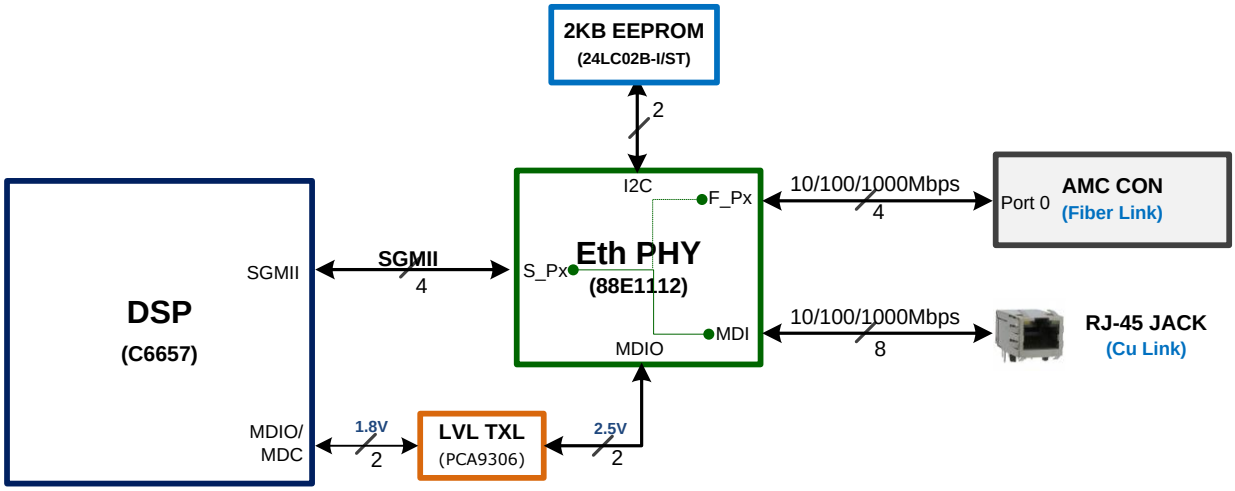


Figure 2.6: C6657 Lite EVM Ethernet PHY Routing

PHY is directly programmed using a 256 Byte EEPROM and DSP intervention is not required. The LEDs (Status 0 and Status 1) indicate the speed of Ethernet link. LED (LOS) indicates the presence of link; ON if there is link and OFF when there is no link. Please refer to table below for more details.

Table 2.6: LED Indication

LED (Colour)	1Gbps		100Mbps		10Mbps	
	Activity	No Activity	Activity	No Activity	Activity	No Activity
Status 0 (Green)	BLINK	SOLID ON	BLINK	SOLID ON	OFF	OFF
Status 1 (Orange)	OFF	OFF	BLINK	SOLID ON	BLINK	SOLID ON

2.9 Serial RapidIO (SRIO) Interface

The C6657 Lite EVM supports high speed SERDES based Serial RapidIO (SRIO) interface. There are total 4 RapidIO ports available on C6657. All SRIO ports are routed to AMC edge connector on board.

The figure below shows the RapidIO connections between the DSP and AMC edge connector.

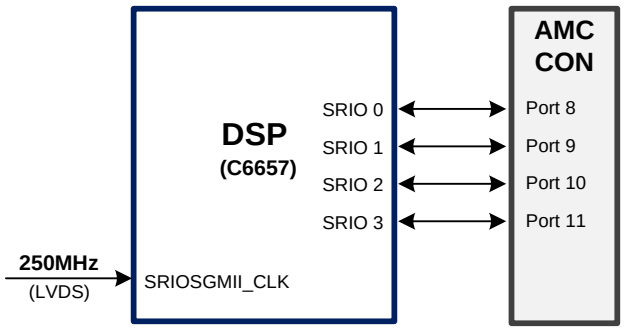


Figure 2.7: C6657 Lite EVM SRIO Port Connections

2.10 DDR3 External Memory Interface

The C6657 Lite EVM DDR3 interface connects to two 2Gbit (128Meg x 16) DDR3 1600 devices. This configuration allows the use of both “narrow (16-bit)”, “normal (32-bit)” modes of the DDR3 EMIF. Micron DDR3 MT41J128M16HA-125 SDRAMs (128Mx16; 800MHz) are used. Upgradation to a total memory size of 4Gbit is supported. For more information, see DDR3 Memory Controller for KeyStone Devices User Guide.

The figure below shows the implementation for the DDR3 SDRAM memory.

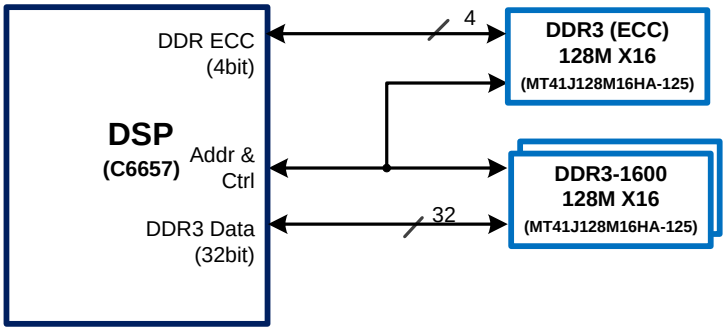


Figure 2.8: C6657 Lite EVM DDR3 Interface

2.11 16-bit Asynchronous External Memory Interface (EMIF-16) & UPP

The C6657 Lite EVM EMIF-16 interface connects to one 1024Mbit (128MB) NAND flash device and 80-pin expansion header (TEST_PH1) on the C6657 Lite EVM. The EMIF16 module provides an interface between DSP and asynchronous external memories such as NAND and NOR flash. Micron MT29F1G08ABCHC is used on board. For more information, see External Memory Interface (EMIF16) for KeyStone Devices User Guide.

The figure below shows the EMIF-16 connections.

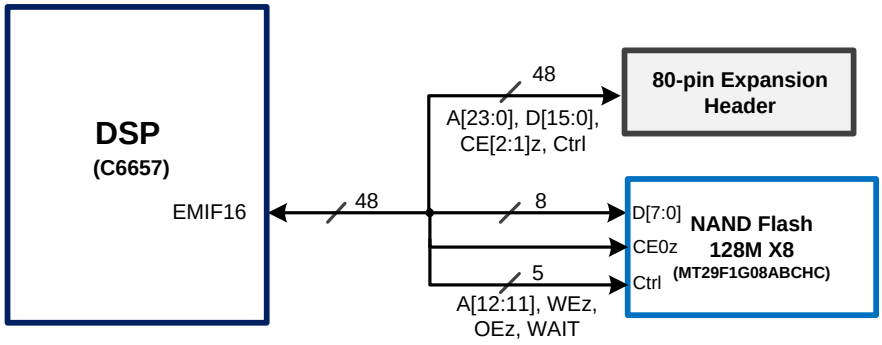


Figure 2.9: C6657 Lite EVM EMIF16 Interface

2.12 HyperLink Interface

TMS320C6657 provides HyperLink bus for companion chip/die interfaces. This is a four lane SerDes interface designed to operate at 12.5 Gbps per lane and is used to connect with external accelerators.

The interface includes the Serial Station Management Interfaces used to send power management and flow messages between devices. This consists of four LVCMOS inputs and four LVCMOS outputs configured as two 2-wire output buses and two 2-wire input buses. Each 2-wire bus includes a data signal and a clock signal. For more information, see Hyperlink Interface for KeyStone Devices User Guide.

The figure below shows Hyperlink bus connections on the C6657 Lite EVM.

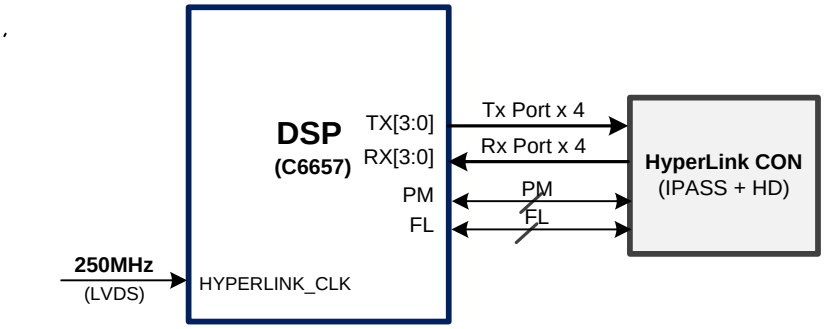


Figure 2.10: C6657 Lite EVM HyperLink Interface

2.13 PCIe Interface

The 2 lane PCI express (PCIe) interface on C6657 Lite EVM provides a connection between the DSP and AMC edge connector. The PCI Express interface provides low pin count, high reliability, and high-speed data transfer at rates of 5.0 Gbps per lane on the serial links. For more information, see the Peripheral Component Interconnect Express (PCIe) for KeyStone Devices User Guide.

The figure below shows the PCIe connectivity to AMC backplane on EVM.

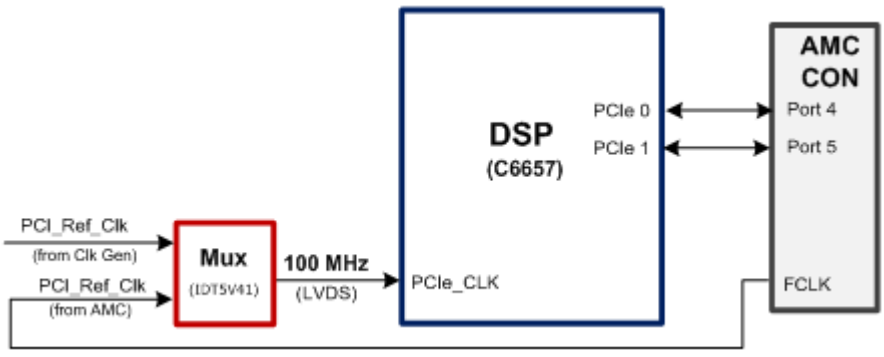


Figure 2.11: C6657 Lite EVM PCIe Interface

2.14 McBSP Interface

McBSP module provides a glueless interface to common telecom serial data streams. The number of active serial links of McBSP0 and McBSP1 is four and they are connected to the AMC edge connector through a level shift IC to support 3.3V I/O on the C6657 Lite EVM. The same signals are also provided on 80-pin Expansion header without level translation (1.8V level). The selection between AMC connector and header is done by McBSP_AMC_EN# signal. If this signal is low McBSP is accessed over AMC edge and FPGA provides the required clocks and frame syncs. If this signal goes high, these clocks and syncs are tri-stated and McBSP is accessed over 80-pin header. For more information, see the McBSP User Guide for the C6657 DSP.

The figure below shows McBSP connectivity to AMC backplane and 80-pin header on EVM.

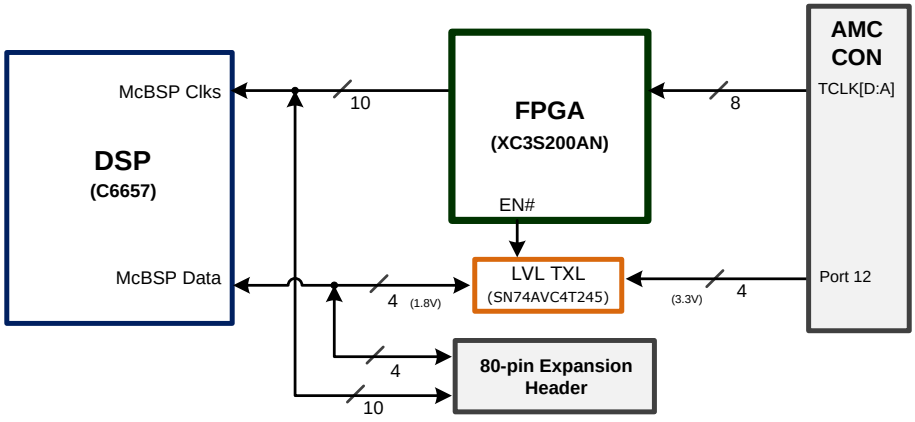


Figure 2.12: C6657 Lite EVM McBSP Interface

The figure below shows the McBSP clock generation by the FPGA and the table below explains the TCLK selection for McBSP Clock and frame sync generation.

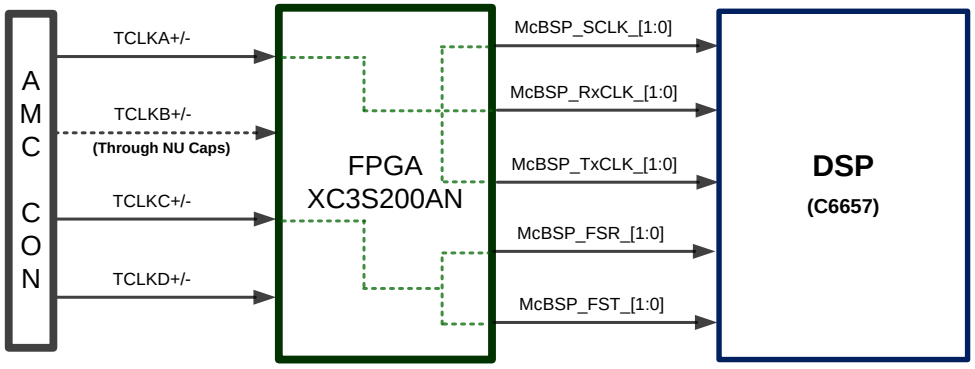


Figure 2.13: C6657 Lite EVM McBSP Clock Generation by FPGA

Table 2.7: McBSP Clock and Frame Sync Generation from TCLK

Reg. Value	FPGA Action	Remarks
00	A) McBSP_AMC_EN# = 0; B) Connect TDM_CLKA to SLCLKs, TxCLKs, RxCLKs; C) Connect TDM_CLKC to FSTs, FSRs.	McBSP accessed over AMC Edge
01	A) McBSP_AMC_EN# = 0; B) Connect TDM_CLKB to SLCLKs, TxCLKs, RxCLKs; C) Connect TDM_CLKC to FSTs, FSRs.	McBSP accessed over AMC Edge. Un-used at this time. Needs NU caps assembly change
10	A) McBSP_AMC_EN# = 0; B) Connect TDM_CLKD to SLCLKs, TxCLKs, RxCLKs; C) Connect TDM_CLKC to FSTs, FSRs.	McBSP accessed over AMC Edge. Un-used at this time.
11	A) McBSP_AMC_EN# = 1; B) Output SLCLKs, TxCLKs, RxCLKs, FSTs, FSRs as tri-state (Hi Z) i.e. no drive.	McBSP accessed over 80-Pin header

2.15 UART Interface

The C6657 has two UART ports- UART0 and UART1. UART1 is directly connected to 80-pin expansion header while a serial port is provided for UART communication using an I2C-UART bridge for UART0. This serial port can be accessed either through USB connector (USB1) or through 3-pin (Tx, Rx and Gnd) serial port header (COM1). The selection can be made through UART Route Select shunt-post COM_SEL1 as follows:

- UART over mini-USB Connector - Shunts installed over COM_SEL1.3- COM_SEL1.1 and COM_SEL1.4 - COM_SEL1.2 **(Default)**
- UART over 3-Pin Header (COM1) - Shunts installed over COM_SEL1.3- COM_SEL1.5 and COM_SEL1.4 - COM_SEL1.6

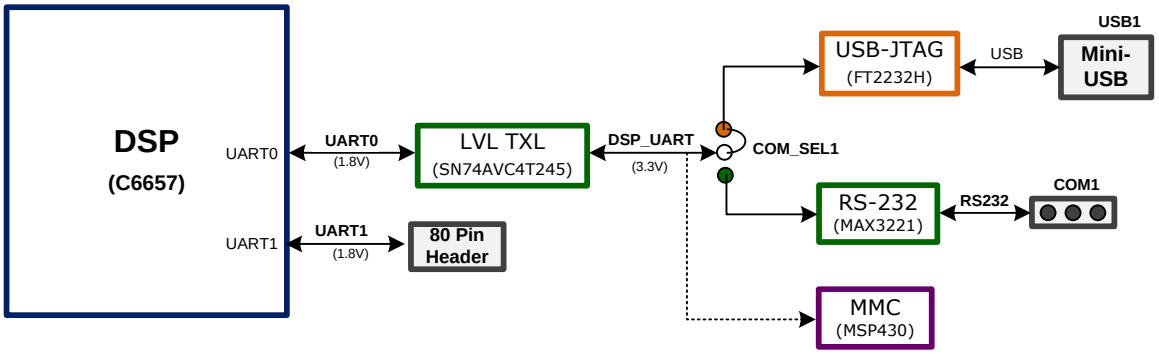


Figure 2.14: C6657 Lite EVM UART Connections

2.16 Module Management Controller (MMC) for IPMI

The C6657 Lite EVM supports limited set of Intelligent Platform Management Interface (IPMI) commands using Module Management Controller (MMC) based on Texas Instruments MSP430F5435 mixed signal processor.

The MMC will communicate with MicroTCA Carrier Hub (MCH) over IPMB (Intelligent Platform Management Bus) when inserted into AMC slot of a PICMG® MTCA.0 R1.0 compliant chassis. The primary purpose of the MMC is to provide necessary information to MCH, to enable the payload power to C6657 Lite EVM EVM when it is inserted into the MicroTCA chassis.

The EVM also supports a Blue LED and LED1 on the front panel as specified in PICMG® AMC.0 R2.0 AdvancedMC base specification. Both of these LEDs will blink as part of initialization process when the MMC will receive management power.

Blue LED (D2):

Blue LED will turn ON when MicroTCA chassis is powered ON and an EVM is inserted into it. It will turn OFF when payload power is enabled to the EVM by the MCH.

RED LED (D1):

This Red colored LED will normally be OFF. It will turn ON to provide basic feedback about failures and out of service conditions.

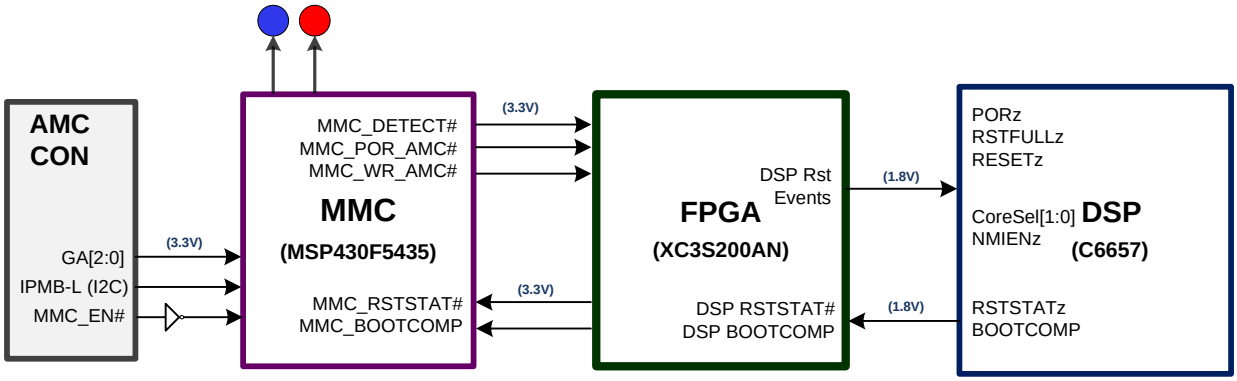


Figure 2.15: C6657 Lite EVM MMC Connections for IPMI

2.17 Expansion Header

The C6657 Lite EVM contains 80 pin header (TEST_PH1) which has UPP (EMIF), McBSP[1:0], TIMI[1:0], TIMO[1:0], I2C, SPI, GPIO[15:14] and UART signal connections. It shall be noted that all signals to this header are of 1.8V level.

3. C6657 Lite EVM Board Physical Specifications

This chapter describes the physical layout of the C6657 Lite EVM board and its connectors, switches and test points. It contains:

3.1 Board Layout

The C6657 Lite EVM board dimension is 7.11” x 2.89” (180.6mm x 73.5mm). It is a 12 layer board and powered through connector DC_IN1. Figure 3-1 and 3-2 shows assembly layout of the C6657 Lite EVM Board.

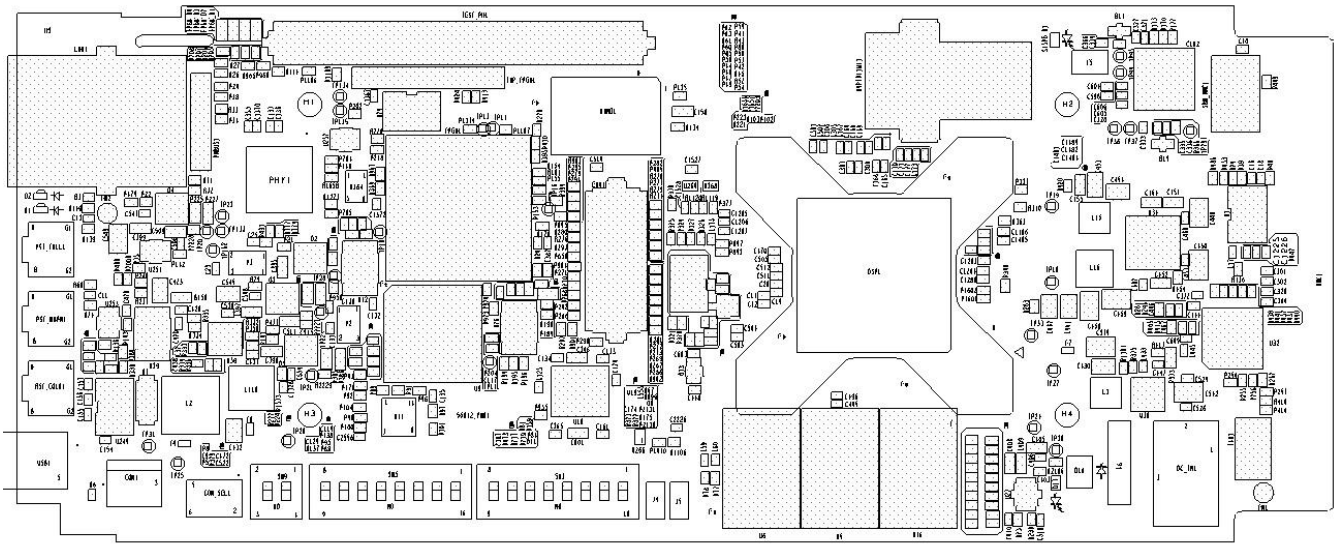


Figure 3.1: C6657 Lite EVM Board Assembly Layout – TOP view

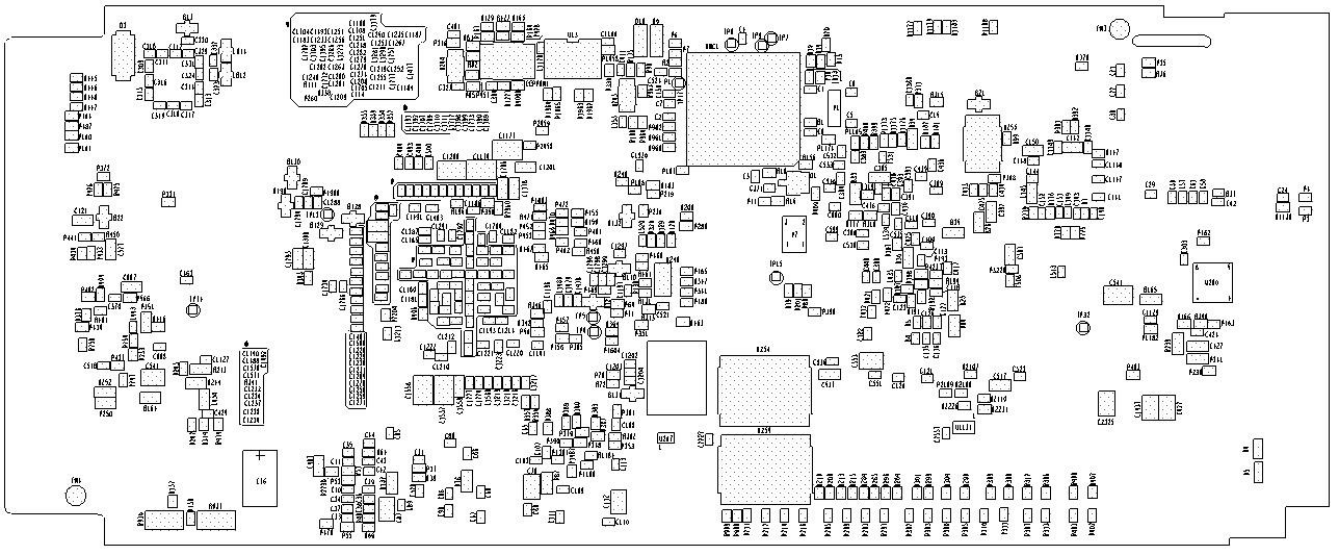


Figure 3.2: C6657 Lite EVM Board layout – Bottom view

3.2 Connector Index

The C6657 Lite EVM Board has several connectors which provide access to various interfaces on the board.

Table 3.1: C6657 Lite EVM Board Connectors

Connector	Pins	Function
560V2_PWR1	8	XDS560v2 Mezzanine Power Connector
AMC1	170	AMC Edge Connector
COM1	3	UART 3-Pin Connector
COM_SEL1	6	UART Route Select Jumper
DC_IN1	3	DC Power Input Jack Connector
EMU1	60	TI 60-Pin DSP JTAG Connector
HyperLink1	36	HyperLink connector for companion chip/die
J4	2	AMC JTAG Selection Header
J5	2	AMC JTAG Selection Header
LAN1	12	Gigabit Ethernet RJ-45 Connector
PMBUS1	5	PMBUS for Smart-Reflex connected to UCD9222
TAP_FPGA1	10	FPGA JTAG Connector
SBW_MMC1	14	MSP430 Spy-Bi-Wire Connector (Factory Use Only)
TEST_PH1	80	EMIF, SPI, I2C, GPIO, TIMI[1:0], TIMO[1:0], and UART1 connections
USB1	5	Mini-USB Connector

3.2.1 560V2_PWR1, XDS560v2 Mezzanine Power Connector

560V2_PWR1 is an 8 pin power connector for XDS560v2 mezzanine emulator board. The pin out for the connector is shown in the figure below:

Table 3.2: XDS560v2 Power Connector pin out

Pin #	Signal Name
1	+5V Supply
2	+5V Supply
3	XDS560V2_IL
4	Ground
5	+3.3V Supply
6	+3.3V Supply
7	Ground
8	Ground

3.2.2 AMC1, AMC Edge Connector

The AMC1 card edge connector plugs into an AMC compatible carrier board and provides a high speed Serial RapidIO, SGMII and IPMB-I2C interfaces to the carrier board. This connector is the 170 pin B+ style. The signals on this connector are shown in the table below:

Table 3.3: AMC Edge Connector

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground Signal	170	GND	Ground Signal
2	VCC12	+12V Power	169	AMC_JTAG_TDI	JTAG Data In
3	PS1#	Presence 1	168	AMC_JTAG_TDO	JTAG Data Out
4	MP	Management Power	167	AMC_JTAG_RST#	JTAG Reset
5	GA0	Geographic Address 0	166	AMC_JTAG_TMS	JTAG TMS
6	RSVD	Reserved	165	AMC_JTAG_TCK	JTAG Clock
7	GND	Ground Signal	164	GND	Ground Signal
8	RSVD	Reserved	163	NC	
9	VCC12	+12V Power	162	NC	
10	GND	Ground Signal	161	GND	Ground Signal
11	AMC_SGMII_TXP	SGMII Port 0-TX	160	NC	
12	AMC_SGMII_TXN	SGMII Port 0-TX	159	NC	
13	GND	Ground Signal	158	GND	Ground Signal
14	AMC_SGMII_RXP	SGMII Port 1-TX	157	NC	
15	AMC_SGMII_RXN	SGMII Port 1-TX	156	NC	
16	GND	Ground Signal	155	GND	Ground Signal
17	GA1	Geographic Address 1	154	NC	
18	VCC12	+12V Power	153	NC	
19	GND	Ground Signal	152	GND	Ground Signal
20	NC		151	NC	
21	NC		150	NC	
22	GND	Ground Signal	149	GND	Ground Signal
23	NC		148	NC	
24	NC		147	NC	
25	GND	Ground Signal	146	GND	Ground Signal

26	GA2	Geographic Address 2	145	NC	
27	VCC12	+12V Power	144	NC	
28	GND	Ground Signal	143	GND	Ground Signal
29	NC		142	NC	
30	NC		141	NC	
31	GND	Ground Signal	140	GND	Ground Signal
32	NC		139	TDM_CLKD_P	Telecom Clock D
33	NC		138	TDM_CLKD_N	Telecom Clock D
34	GND	Ground Signal	137	GND	Ground Signal
35	NC		136	TDM_CLKC_P	Telecom Clock C
36	NC		135	TDM_CLKC_N	Telecom Clock C
37	GND	Ground Signal	134	GND	Ground Signal
38	NC		133	NC	
39	NC		132	NC	
40	GND	Ground Signal	131	GND	Ground Signal
41	ENABLE#	Enable Signal	130	DSP_SDA_AMC	I2C Data
42	VCC12	+12V Power	129	DSP_SCL_AMC	I2C Clock
43	GND	Ground Signal	128	GND	Ground Signal
44	AMCC_P4_PCIe_TX1P	PCIe Port 0-TX	127	NC	
45	AMCC_P4_PCIe_TX1N	PCIe Port 0-TX	126	NC	
46	GND	Ground Signal	125	GND	Ground Signal
47	AMCC_P4_PCIe_RX1P	PCIe Port 0-RX	124	NC	
48	AMCC_P4_PCIe_RX1N	PCIe Port 0-RX	123	NC	
49	GND	Ground Signal	122	GND	Ground Signal
50	AMCC_P5_PCIe_TX1P	PCIe Port 1-TX	121	NC	
51	AMCC_P5_PCIe_TX1N	PCIe Port 1-TX	120	NC	
52	GND	Ground Signal	119	GND	Ground Signal
53	AMCC_P5_PCIe_RX1P	PCIe Port 1-RX	118	NC	
54	AMCC_P5_PCIe_RX1N	PCIe Port 1-RX	117	NC	
55	GND	Ground Signal	116	GND	Ground Signal
56	SMB_SCL_IPMBL		115	AMC_P12_McBSP_TX0	McBSP Port 0-TX
57	VCC12	+12V Power	114	AMC_P12_McBSP_TX1	McBSP Port 1-TX
58	GND	Ground Signal	113	GND	Ground Signal
59	NC		112	AMC_P12_McBSP_RX0	McBSP Port 0-RX
60	NC		111	AMC_P12_McBSP_RX1	McBSP Port 1-RX
61	GND	Ground Signal	110	GND	Ground Signal
62	NC		109	AMC_P11_SRIO4_TXP	SRIO Port 3-TX
63	NC		108	AMC_P11_SRIO4_TXN	SRIO Port 3-TX
64	GND	Ground Signal	107	GND	Ground Signal
65	NC		106	AMC_P11_SRIO4_RXP	SRIO Port 3-RX
66	NC		105	AMC_P11_SRIO4_RXN	SRIO Port 3-RX
67	GND	Ground Signal	104	GND	Ground Signal
68	NC		103	AMC_P10_SRIO3_TXP	SRIO Port 2-TX
69	NC		102	AMC_P10_SRIO3_TXN	SRIO Port 2-TX
70	GND	Ground Signal	101	GND	Ground Signal
71	SDA_IPMB		100	AMC_P10_SRIO3_RXP	SRIO Port 2-RX
72	VCC12	+12V Power	99	AMC_P10_SRIO3_RXN	SRIO Port 2-RX
73	GND	Ground Signal	98	GND	Ground Signal
74	TDM_CLKA_P	Telecom Clock A	97	AMC_P9_SRIO2_TXP	SRIO Port 1-TX
75	TDM_CLKA_N	Telecom Clock A	96	AMC_P9_SRIO2_TXN	SRIO Port 1-TX
76	GND	Ground Signal	95	GND	Ground Signal

77	TDM_CLKB_P	Telecom Clock B	94	AMC_P9_SRIO2_RXP	SRIO Port 1-RX
78	TDM_CLKB_N	Telecom Clock B	93	AMC_P9_SRIO2_RXN	SRIO Port 1-RX
79	GND	Ground Signal	92	GND	Ground Signal
80	NC		91	AMC_P8_SRIO1_TXP	SRIO Port 0-TX
81	NC		90	AMC_P8_SRIO1_TXN	SRIO Port 0-TX
82	GND	Ground Signal	89	GND	Ground Signal
83	PS0#	Presence 0	88	AMC_P8_SRIO1_RXP	SRIO Port 0-RX
84	VCC12	+12V Power	87	AMC_P8_SRIO1_RXN	SRIO Port 0-RX
85	GND	Ground Signal	86	GND	Ground Signal

3.2.3 COM1, UART 3-Pin Connector

COM1 is 3-pin male connector for RS232 serial interface. A 3-Pin female to 9-Pin DTE female, cable is supplied with C6657 Lite EVM to connect with the PC.

Table 3.4: UART Connector pin out

Pin #	Signal Name
1	Ground
2	Transmit
3	Receive

3.2.4 COM_SEL1, UART Route Select Connector

UART port can be accessed either through Mini-USB connector (USB1) or through 3-pin RS232 Serial port header (COM_SEL1). The selection can be made through UART route select connector J13 as follows:

- UART over USB Connector (Default): Shunts installed over COM_SEL1.3- COM_SEL1.1 and COM_SEL1.4 - COM_SEL1.2
- UART over 3-Pin Header COM1 - Shunts installed over COM_SEL1.3- COM_SEL1.5 and COM_SEL1.4 - COM_SEL1.6

The pin out for the connector is shown in the figure below:

Table 3.5: UART Path Select Connector pin out

Pin #	Signal Name	Pin #	Signal Name
1	FT2232H(USB Chip) Transmit	2	FT2232H(USB Chip) Receive
3	UART Transmit	4	UART Receive
5	MAX3221 Transmit	6	MAX3221 Receive

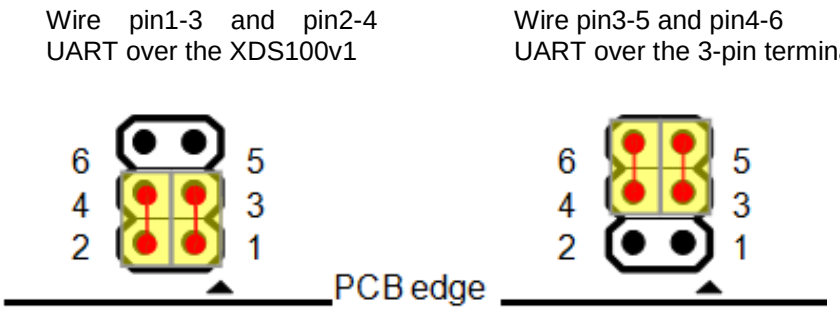


Figure 3.3: COM_SEL1 Jumper Settings

3.2.5 DC_IN1, DC Power Input Jack Connector

DV_IN1 is a DC Power-in Jack Connector for the stand-alone application of C6657 Lite EVM. It is a 2.5mm power jack with positive center tip polarity. Do not use this connector if EVM is inserted into MicroTCA chassis or AMC carrier back-plane.

Table 3.6: DC_IN1 Connector pin out

Pin #	Signal Name
1	NC
2	+12V
3	Ground

3.2.6 EMU1, TI 60 Pin DSP JTAG Connector

EMU1 is a high speed system trace capable TI 60 pin JTAG connector for XDS560v2 type of DSP emulation. The onboard switch multiplexes this interface with the on-board XDS100 type emulator. Whenever an external emulator is plugged into EMU1, the external emulator connects with the DSP. The I/O voltage level on these pins is 1.8V. So any 1.8V level compatible emulator can be used to interface with the C6657 DSP. It should be noted that when an external emulator is plugged into this connector (EMU1), onboard XDS100 type emulation circuitry will be disconnected from the DSP. The pin out for the connector is shown in figure below:

Table 3.7: DSP JTAG Connector pin out

Pin #	Signal Name	Pin #	Signal Name
B1	ID0	D1	NC
A1	Ground	C1	ID2
B2	TMS	D2	Ground
A2	Ground	C2	EMU18
B3	EMU17	D3	Ground
A3	Ground	C3	TRST
B4	TDI	D4	Ground
A4	Ground	C4	EMU16
B5	EMU14	D5	Ground
A5	Ground	C5	EMU15
B6	EMU12	D6	Ground
A6	Ground	C6	EMU13
B7	TDO	D7	Ground
A7	Ground	C7	EMU11
B8	TVD	D8	Type1 (Ground)
A8	Type0 (NC)	C8	TCLKRTN
B9	EMU9	D9	Ground
A9	Ground	C9	EMU10
B10	EMU7	D10	Ground
A10	Ground	C10	EMU8
B11	EMU5	D11	Ground
A11	Ground	C11	EMU6
B12	TCLK	D12	Ground
A12	Ground	C12	EMU4
B13	EMU2	D13	Ground
A13	Ground	C13	EMU3
B14	EMU0	D14	Ground

A14	Ground	C14	EMU1
B15	ID1	D15	Ground
A15	TRGRSTz	C15	ID3

3.2.7 HyperLink1, Hyperlink Connector

The EVM provides a HyperLink connection by a mini-SAS HD+ 4i connector. The connector contains 8 SERDES pairs and 4 sideband sets to carry full HyperLink signals. The connector is shown in Figure 3.4 and its pin out is shown in Table 3.8. This connector is the Molex iPass+HD connector 76867-0011. The Molex cable 1110670200 can be used to connect two EVMs together

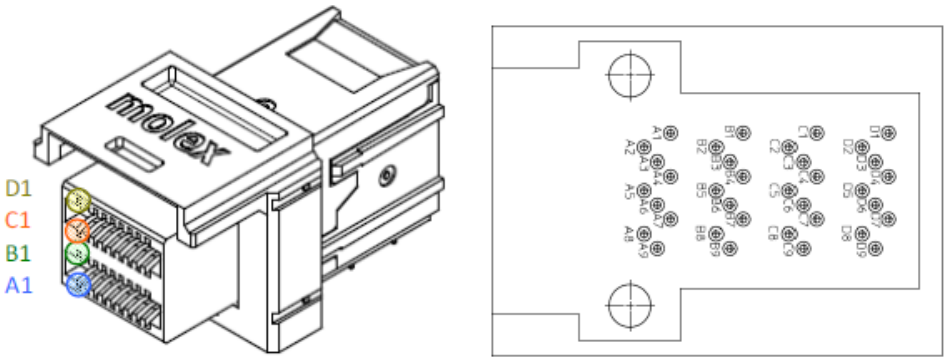


Figure 3.4: HyperLink Connector

Table 3.8: DSP JTAG Connector pin out

Pin #	Signal Name	Pin #	Signal Name
A1	HyperLink_TXFLCLK	B1	HyperLink_RXPMDAT
A2	HyperLink_RXFLCLK	B2	HyperLink_TXFLDAT
A3	GND	B3	GND
A4	HyperLink_RXP1	B4	HyperLink_RXP0
A5	HyperLink_RXN1	B5	HyperLink_RXN0
A6	GND	B6	GND
A7	HyperLink_RXN3	B7	HyperLink_RXP2
A8	HyperLink_RXP3	B8	HyperLink_RXN2
A9	GND	B9	GND
C1	HyperLink_TXPMDAT	D1	HyperLink_RXPMCLK
C2	HyperLink_TXPMCLK	D2	HyperLink_RXFLDAT
C3	GND	D3	GND
C4	HyperLink_TXN3	D4	HyperLink_TXP0
C5	HyperLink_TXP3	D5	HyperLink_TXN0
C6	GND	D6	GND
C7	HyperLink_TXP2	D7	HyperLink_TXP1
C8	HyperLink_TXN2	D8	HyperLink_TXN1
C9	GND	D9	GND

3.2.8 J4 and J5, Emulation Path Selection Connector

J4 and J5 are used to override preference to external emulator and provide an emulation path for AMC JTAG even when on-board XDS100 or external emulator is connected. Their connections are shown in tables below:

Table 3.9: J4 Connector pin out

Pin #	Signal Name
1	VCC3V3_AUX (thru PU)
2	Ground

Table 3.10: J5 Connector pin out

Pin #	Signal Name
1	VCC3V3_AUX
2	Ground (thru PD)

3.2.9 LAN1, Ethernet Connector

LAN1 is a Gigabit RJ45 Ethernet connector with integrated magnetics. It is driven by Marvell Gigabit Ethernet switch 88E1112. The connections are shown in a table below:

Table 3.11: Ethernet Connector pin out

Pin #	Signal Name
1	Center Tap 2
2	MD2-
3	MD2+
4	MD1-
5	MD1+
6	Center Tap 1
7	Center Tap 3
8	MD3+
9	MD3-
10	MD0-
11	MD0+
12	Center Tap 0
13	LED1-
14	LED1+
15	LED2-
16	LED2+
H3	Shield 1
H4	Shield 2

3.2.10 PMBUS1, PMBUS Connector for Smart Reflex Control

The TMS320C6657 DSP core power is supplied by a Smart-Reflex power controller UCD9222 with the Integrated FET Driver UCD7242. PMBUS1 provides a connection between UCD9222 and remote connection during development. Through the USB to GPIO pod provided by TI, the user can trace and configure the parameters in UCD9222 with the Smart-Fusion GUI. The pin out of PMBUS1 is shown in table below.

Table 3.12: PMBUS Connector Pin Out

Pin #	Signal Name
1	PMBUS_CLK
2	PMBUS_DAT
3	PMBUS_ALT
4	PMBUS_CTL
5	Gnd

3.2.11 TAP_FPGA1, FPGA JTAG Connector (For Factory Use Only)

TAP_FPGA1 is an 8-pin JTAG connector for the FPGA programming and the PHY boundary test of the factory only. The pin out for the connector is shown in the figure below:

Table 3.13: FPGA JTAG Header Pin Out

Pin #	Signal Name
1	VCC3V3_FPGA
2	GND
3	FPGA_JTAG_TCK
4	FPGA_JTAG_TDI
5	FPGA_JTAG_TDO
6	FPGA_JTAG_TMS
7	FPGA_JTAG_RST#
8	VCC1V8_AUX

3.2.12 SBW_MMC1, MSP430 SpyBiWire Connector (For Factory Use Only)

SBW_MMC1 is a 4-pin SpyBiWire connector for IPMI software loading into MSP430. The C6657 Lite EVM are supplied with IPMI software already loaded into MSP430. The pin out for the connector is shown in the figure below:

Table 3.14: MSP430 SpyBiWire Connector Pin Out

Pin #	Signal Name
1	GND
2	VCC3V3_MP
3	MMC_SBWTDIO
4	MMC_SBWTCK

3.2.13 TEST_PH1, Expansion Header (EMIF-16, SPI, GPIO, Timer I/O, I2C, McBSP and UART)

TEST_PH1 is an expansion header for several interfaces on the DSP. They are 16-bit EMIF, SPI, GPIO, Timer, I2C, McBSP and UART. All signals on this connector are 1.8V level. The signal connections to the test header are as shown in a table below:

Table 3.15: 80-pin Expansion Header Pin Out

Pin	Signal	Description	Pin	Signal	Description
1	GND	Ground	2	DSP_EMIFA00/UPPXD00	EMIF Addr0
3	DSP_SDA	DSP I2C Data	4	DSP_EMIFA01/UPPXD01	EMIF Addr1
5	DSP_SCL	DSP I2C Clock	6	DSP_EMIFA02/UPPXD02	EMIF Addr2
7	DSP_EMIFD00/UPPD00	EMIF Data0	8	DSP_EMIFA03/UPPXD03	EMIF Addr3
9	DSP_EMIFD01/UPPD01	EMIF Data1	10	DSP_EMIFA04/UPPXD04	EMIF Addr4
11	DSP_EMIFD02/UPPD02	EMIF Data2	12	DSP_EMIFA05/UPPXD05	EMIF Addr5
13	DSP_EMIFD03/UPPD03	EMIF Data3	14	DSP_EMIFA06/UPPXD06	EMIF Addr6
15	DSP_EMIFD04/UPPD04	EMIF Data4	16	DSP_EMIFA07/UPPXD07	EMIF Addr7
17	DSP_EMIFD05/UPPD05	EMIF Data5	18	DSP_EMIFA08/UPPXD08	EMIF Addr8
19	DSP_EMIFD06/UPPD06	EMIF Data6	20	DSP_EMIFA09/UPPXD09	EMIF Addr9
21	DSP_EMIFD07/UPPD07	EMIF Data7	22	DSP_EMIFA10/UPPXD10	EMIF Addr10
23	DSP_EMIFD08/UPPD08	EMIF Data8	24	DSP_EMIFA11/UPPXD11	EMIF Addr11
25	DSP_EMIFD09/UPPD09	EMIF Data9	26	DSP_EMIFA12/UPPXD12	EMIF Addr12
27	DSP_EMIFD10/UPPD10	EMIF Data10	28	DSP_EMIFA13/UPPXD13	EMIF Addr13
29	DSP_EMIFD11/UPPD11	EMIF Data11	30	DSP_EMIFA14/UPPXD14	EMIF Addr14
31	DSP_EMIFD12/UPPD12	EMIF Data12	32	DSP_EMIFA15/UPPXD15	EMIF Addr15
33	DSP_EMIFD13/UPPD13	EMIF Data13	34	DSP_EMIFA16/ UPP_CH0_CLK	EMIF Addr16
35	DSP_EMIFD14/UPPD14	EMIF Data14	36	DSP_EMIFA17/ UPP_CH0_START	EMIF Addr17
37	DSP_EMIFD15/UPPD15	EMIF Data15	38	DSP_EMIFA18/ UPP_CH0_ENABLE	EMIF Addr18
39	DSP_EMIFCE1Z	EMIF Space Enable1	40	DSP_EMIFA19/ UPP_CH0_WAIT	EMIF Addr19
41	DSP_EMIFCE2Z	EMIF Space Enable2	42	DSP_EMIFA20/ UPP_CH1_CLK	EMIF Addr20
43	DSP_EMIFBE0Z	EMIF Byte Enable0	44	DSP_EMIFA21/ UPP_CH1_START	EMIF Addr21
45	DSP_EMIFBE1Z	EMIF Byte Enable1	46	DSP_EMIFA22/ UPP_CH1_ENABLE	EMIF Addr22
47	DSP_EMIFOEZ	EMIF Output Enable	48	DSP_EMIFA23/ UPP_CH1_WAIT	EMIF Addr23
49	DSP_EMIFWEZ	EMIF Write Enable	50	DSP_McBSP0_RXCLK	McBSP Receive Clk 0
51	DSP_EMIFRNW	EMIF Read/Write	52	DSP_McBSP0_TXCLK	McBSP Transmit Clk 0
53	DSP_EMIFWAIT1/ UPP2XTXCLK	EMIF Wait	54	DSP_McBSP0_SLCLK	McBSP Slow Clk 0
55	DSP_TIMI0/GPIO16	Timer input 0	56	DSP_McBSP0_FSR	McBSP Frame Sync Receive 0
57	DSP_TIMO0/GPIO18	Timer output 0	58	DSP_McBSP0_FST	McBSP Frame Sync Transmit 0

59	DSP_TIMI1/GPIO17	Timer input 1	60	DSP_McBSP0_RX	McBSP Data In 0
61	DSP_TIMO1/GPIO19	Timer output 1	62	DSP_McBSP0_TX	McBSP Data Out 0
63	DSP_SSPMISO/GPIO30	SPI data input	64	DSP_McBSP1_RXCLK	McBSP Receive Clk 1
65	DSP_SSPMOSI/GPIO31	SPI data output	66	DSP_McBSP1_TXCLK	McBSP Transmit Clk 1
67	DSP_SSPCS1/GPIO29	SPI chip select	68	DSP_McBSP1_SLCLK	McBSP Slow Clk 1
69	PH_SSPCK	SPI clock	70	DSP_McBSP1_FSR	McBSP Frame Sync Receive 1
71	DSP_UART1_TX	UART Data Out	72	DSP_McBSP1_FST	McBSP Frame Sync Transmit 0
73	DSP_UART1_RX	UART Data In	74	DSP_McBSP1_RX	McBSP Data In 1
75	DSP_UART1_RTS	UART Request To Send	76	DSP_McBSP1_TX	McBSP Data Out 1
77	DSP_UART1_CTS	UART Clear To Send	78	DSP_GPIO_14	DSP GPIO14
79	GND	Ground	80	DSP_GPIO_15	DSP GPIO15

3.2.14 USB1, Mini USB Connector

J11 is a 5 pin Mini-USB connector to connect Code Composer Studio with C6657 DSP using XDS100 type on-board emulation circuitry. Below table shows the pin out of Mini-USB connector.

Table 3.16: Mini-USB Connector pin out

Pin #	Signal Name
1	VBUS
2	D-
3	D+
4	ID (NC)
5	Ground

3.3 DIP and PushButton Switches

The C6657 Lite EVM has three push button switches and three sliding actuator DIP switches. The RST_COLD1, RST_WARM1 and RST_FULL1 are push button switches while SW3, SW5 and SW9 are DIP switches. The function of each of the switches is listed in the table below:

Table 3.17: C6657 Lite EVM Board Switches

Switch	Function
RST_COLD1	Cold Reset Event (RFU)
RST_FULL1	Full Reset Event
RST_WARM1	Warm Reset Event
SW3	DSP Configuration, DSP Boot mode
SW5	DSP Boot mode, PLL setting, PCIe Mode Selection
SW9	PCIe Enable/ Disable, User Switch

3.3.1 RST_COLD1, Cold Reset

The button is reserved for future use.

3.3.2 RST_FULL1, Full Reset

Pressing the RST_FULL1 button switch will issue a RESETFULL# to TMS320C6657 by FPGA. It'll reset DSP and other peripherals.

3.3.3 RST_WARM1, Warm Reset

Pressing the RST_WARM1 button switch will issue a RESET# to TMS320C6657 by FPGA. The FPGA will assert the RESET# signal to DSP and DSP will execute either a HARD or SOFT reset by the configuration in the RSCFG register in PLLCTL.

Note: Users may refer to the TMS320C6657 Data Manual to check the difference between assertion of DSP RESET# and the other reset signals.

3.3.4 SW3, DSP Configuration

SW3 is an 8 position DIP switch, which is used for DSP configuration. A diagram of SW3 switch (with factory default settings) is shown below:

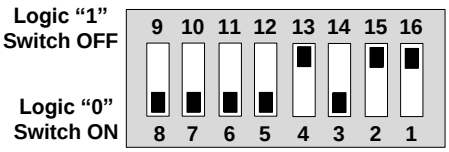


Figure 3.5: SW3 default settings

The following table describes the positions and corresponding function on SW3.

Table 3.18: SW3, DSP Configuration Switch

SW3 Position	Description	Default Value	Function
1	LENDIAN	1(ON)	OFF - Big Endian mode ON - Little Endian mode
2-5	BOOTMODE	0000	DSP Boot Mode Selection Pins
6-8	BOOT DEVICE CONFIG	000	DSP Device Configuration Settings

3.3.5 SW5, DSP Boot mode

SW5 is an 8 position DIP switch, which is used for DSP boot mode selection, device number and as a 2 position User Switch after DSP Boot. A diagram of the SW5 switch (with factory default settings) is shown below:

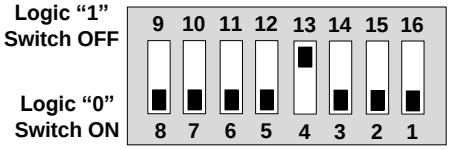


Figure 3.6: SW5 default settings

The following table describes the positions and corresponding function on SW5.

Table 3.19: SW4, DSP Boot Mode Selection Switch

SW5 Position	Description	Default Value	Function
4 - 1	Boot Mode[3:0]	0001	Boot mode selection pins for DSP Master I2C boot mode for I2C address 50h Refer to TMS320C6657 Datasheet for details of other boot modes supported.
8 – 5 *	Device Number [3:0]	0000	Device number selection for multiple DSPs and position 7 and 8 as User Switch-1 and User Switch-2 respectively after DSP boot.

Note: Please change Boot Mode[3:0] to "0010" for NAND boot mode of this EVM. "0010" is primarily a Master I2C boot mode for I2C address 51h for DSP, which works as NAND boot mode in this EVM.

* - SW5 position 7 and 8 is also configured as User Switch-1 and User Switch-2 respectively (after DSP boot). FPGA monitors status of the user switches and stores its value into internal FPGA registers. The DSP can read user switches' value by accessing FPGA's internal registers.

3.4 Test Points

The C6657 Lite EVM Board has 38 test points. The position of each test point is shown in the figure below:

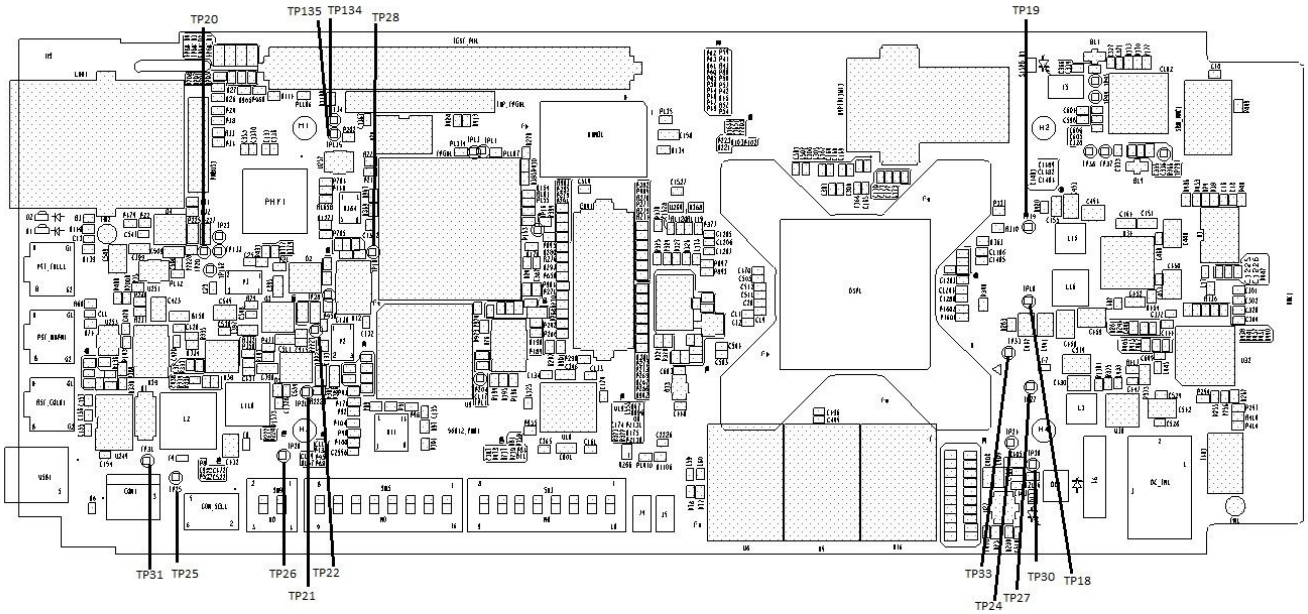


Figure 3.7: Board Test Points (Top)

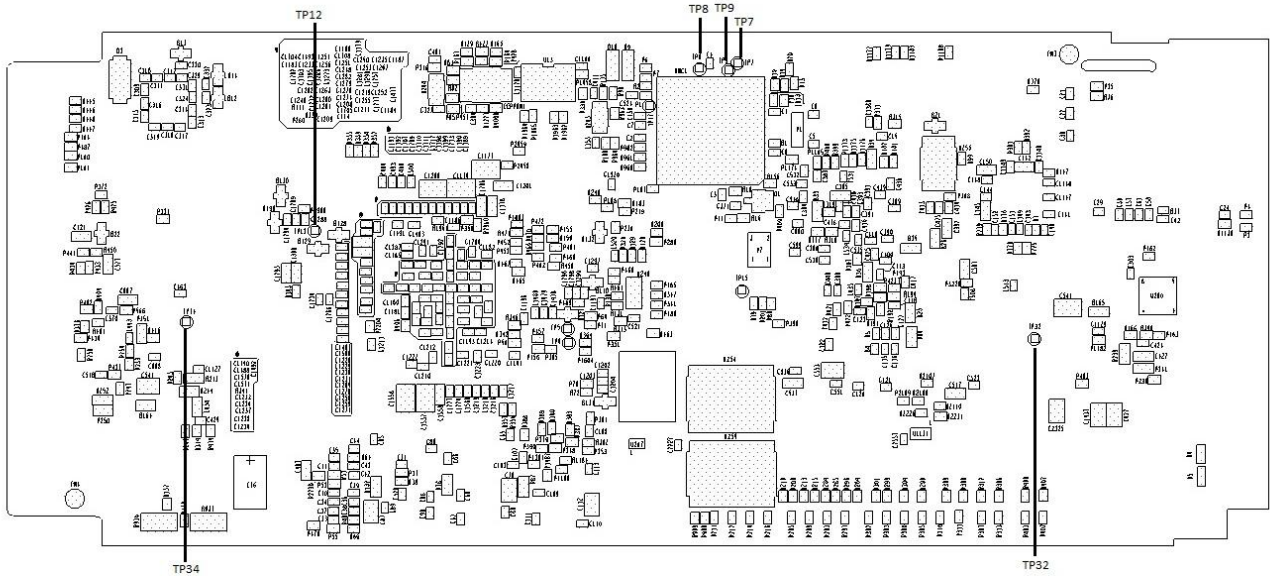


Figure 3.8: Board Test Points (Bottom)

Table 3.20: C6657 Lite EVM Board Test Points

Test Point	Signal
TP7	MSP430 SMCLK
TP8	MSP430 ACLK
TP9	MSP430 MCLK
TP134	DSP UART0 CTS
TP135	DSP UART0 RTS
TP12	DSP SYSCLKOUT
TP31,TP32,TP33,TP34	Ground
TP18	CVDD Supply
TP19	+1.0V Supply
TP30	+12V Input Supply
TP26	+3.3V AUX Supply
TP25	+5.0 Supply
TP27	+1.5V Supply
TP28	+1.2V Supply
TP22	+1.8V AUX Supply
TP20	+2.5V Supply
TP21	+1.8V Supply
TP24	+0.75V Supply

3.5 System LEDs

The C6657 Lite EVM board has eight LEDs. Their positions on the board are indicated in figure below. The description of each LED is listed in table below:

Table 3.21: C6657 Lite EVM Board LEDs

LED#	Color	Description
D1	Red	Failure and Out of service status in AMC chassis
D2	Blue	Hot Swap status in AMC chassis
D17	Green	Board Powered ON Indicator
FPGA_D1-FPGA_D4	Green	Debug LEDs
SYS_PG1	Yellow (Green)	All Power rails are stable on AMC

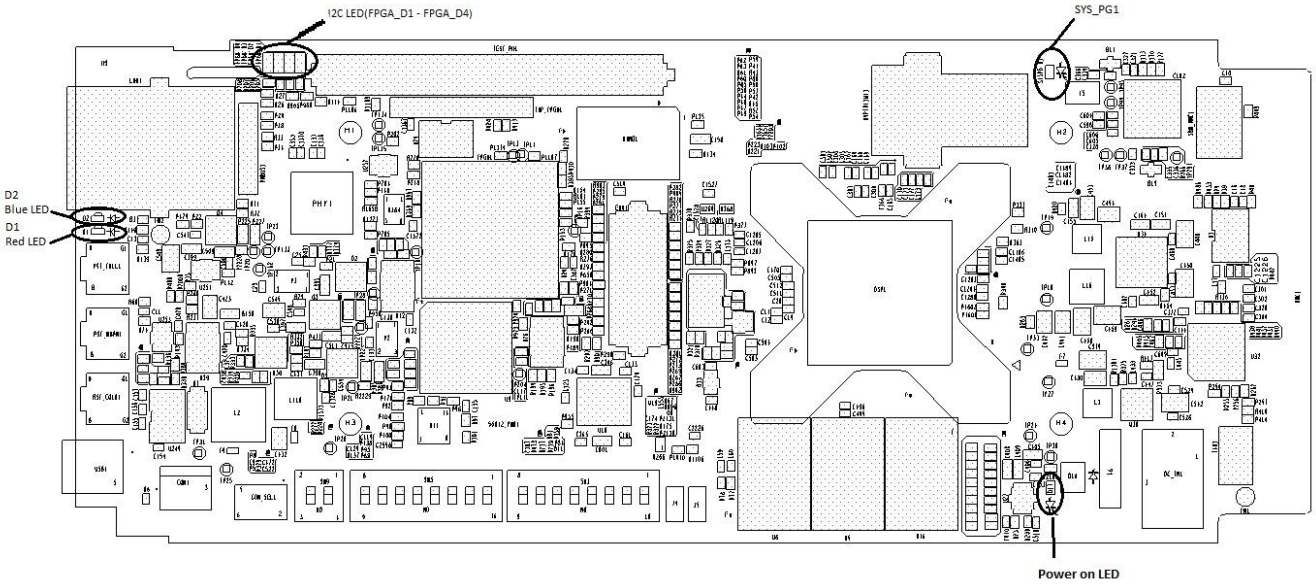


Figure 3.9: Board LEDs

Additional LEDs on TMDXEVM6657LE board are highlighted in figure below and their description is listed in table 3.22.

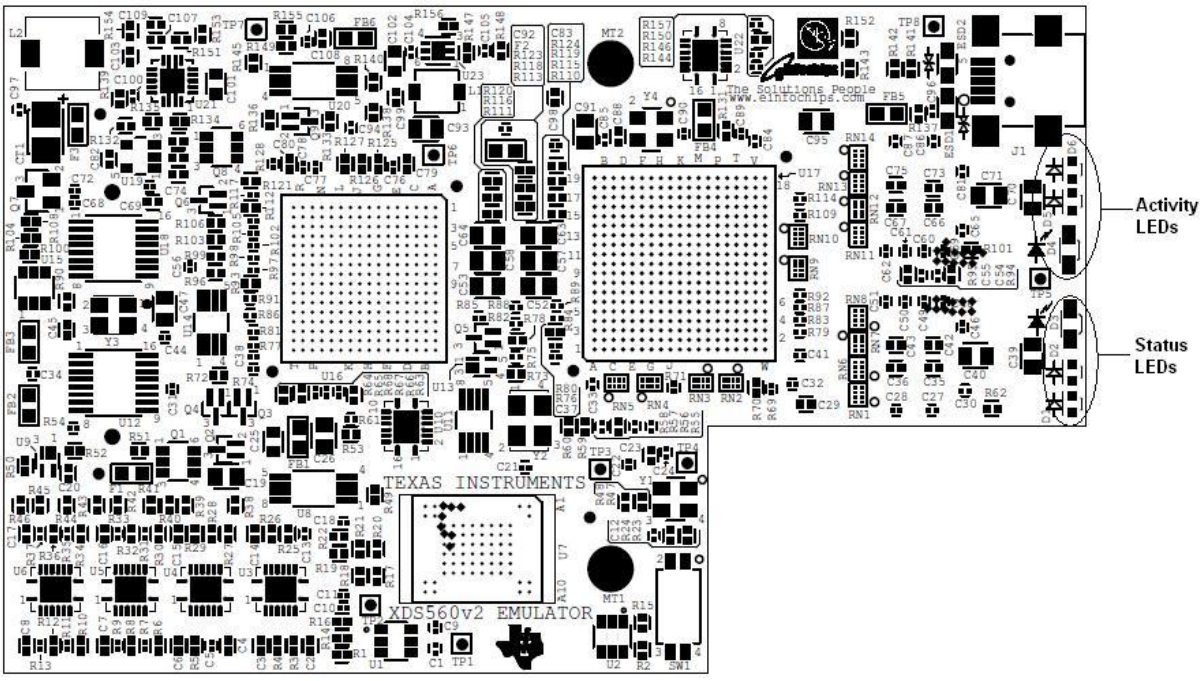


Figure 3.10: TMDXEVM6657LE Board Additional LEDs

Table 3.22: TMDXEVM6657LE Board Additional LEDs

LED#	Color	Description
D1 (Activity LED 1)	Red	ON - DTC Ready OFF - DTC Not Ready
D2 (Activity LED 2)	Yellow	ON - FPGA Programmed OFF - FPGA Not Programmed
D3 (Activity LED 3)	Green	Reserved
D4 (Status LED 3)	Green	ON =CCS Connected OFF= CCS Disconnected
D5 (Status LED 2)	Yellow	DTC to Host Activity
D6 (Status LED 1)	Orange	Target to DTC Trace Activity

4. C6657 Lite EVM System Power Requirements

This chapter describes the power design of C6657 Lite EVM board. It contains:

4.1 Power Requirements

Note that the power estimates stated in this section are maximum limits used in the design of the EVM. They have margin added to allow the EVM to support early silicon samples that normally have higher power consumption than eventual production units.

The maximum EVM power requirements (including 5% margin) are estimated to be:

- FPGA – 0.62W
- Clock Generator & clock sources – 1.73W
- DSP – 4.35W (worse case)
  - Core Supply: 3.7W
  - Peripheral supplies: 0.65W
- DDR3 – 2.60W (including ECC chip), 1.73W (without ECC)
- PHY – 3.07W
- USB – 0.86W
- Misc – 1.23W
- XDS560v2 Mezzanine (if used) – 4.2W

Total EVM Board Consumption is 22.18W approx. Hence, the selected AC/DC 12V adapter should be rated for a minimum of 22.5 Watts.

Table 4.1: Current Consumption on Each Voltage Rail

Device	Net Name	Voltage	Current	Qty	Power Usage		Description
Input	3.3V_MP_AMC	+3.30V					MMC Management Power
	VCC12	+12.00V					Payload Power to AMC
Management	VCC3V3_AUX	+3.30V					3.3V Power Rail
	VCC1V2	+1.20V					1.2V Power Rail
	VCC1V8_AUX	+1.80V					1.8V Power Rail
TMS320C6657	CVDD	+1.00V	2.500A	1	2.50W	4.22W	DSP Core Power
	VCC1V0	+1.00V	1.100A	1	1.10W		DSP Fixed Core Power
	VCC1V8	+1.80V	0.050A	1	0.09W		DSP I/O Power
	VCC1V5	+1.50V	0.350A	1	0.53W		DSP DDR3 & SERDES Power
DDR3 Memory	VCC1V5	+1.50V	0.530A	3	2.39W	2.50W	DDR3 RAM Power
	VCC0V75	+0.75V	0.050A	3	0.11W		DDR3 Termination Power
NAND Flash	VCC1V8	+3.30V	0.015A	1	0.05W	0.05W	NAND Flash Power
NOR Flash	VCC1V8	+1.80V	0.010A	1	0.02W	0.02W	SPI NOR Flash Power
CDCE62005	VCC3V3_AUX	+3.30V	0.500A	1	1.65W	1.65W	Clock Gen Power

PHY (88E112)	VCC2V5	+2.50V	0.340A	1	0.85W	1.23W	PHY Analog & I/O Power
	VCC1V2	+1.20V	0.320A	1	0.38W		PHY Core Power
USB Emulator (FT2232H)	VCC3V3_AUX	+3.30V	0.200A	1	0.66W	0.79W	USB Emulation Power
	VCC1V8_AUX	+1.80V	0.070A	1	0.13W		USB Emulation Power
MMC (MPS430)	VCC3V3_MP	+3.30V	0.048A	1	0.16W	0.16W	MMC Power
FPGA	VCC1V2	+1.20V	0.125A	1	0.15W	0.59W	FPGA Core Power
	VCC3V3_AUX	+3.30V	0.024A	1	0.08W		FPGA +3.3V bank I/O Power
	VCC1V8_AUX	+1.80V	0.200A	1	0.36W		FPGA +1.8V bank I/O Power
XDS560v2 Mezzanine	VCC5	+5.00V	0.600A	1	3.00W	3.99W	XDS560v2 +5V Power
	VCC3V3_AUX	+3.30V	0.300A	1	0.99W		XDS560v2 +3.3V Power
Misc. Logic	VCC3V3_AUX	+3.30V	0.300A	1	0.99W	1.17W	Translator & Logic Power
	VCC1V8_AUX	+1.80V	0.100A	1	0.18W		Translator & Logic Power

Components Part No.	Description	Quantity Per Board	Current Consumed by corresponding device on power supply (mA)											Total Power (mW)
			0.75V	1.00V	1.00V	1.20V	1.50V	1.80V	1.80V	2.50V	3.30V	3.30V	5.00V	
				CVDD	CVDD1			AUX	VCC		AUX	AMC		
TMS320C6657	CPU	1		2500.00	1000.00		350.00		50.00					4115.00
XC3S200AN-4FTG256C	FPGA	1				125.00		200.00			24.00			589.20
MT41J128M16HA-125	DDR3 SDRAM	2	50.00				525.00							1650.00
MT41J128M16HA-125	DDR3 ECC	0	50.00				525.00							0.00
NAND512R3A2SZA6E	NAND Flash (64MB)	1							15.00					27.00
AT25128B	SPI EEPROM	1									10.00			33.00
FT2232H	USB to JTAG convertor	1							70.00		210.00			819.00
88E1112	Ethernet	1				320.00				338.00				1229.00
MSP430	MMC	1										48.00		158.40
CDCE62005	Clock Generator	1									500.00			1650.00
XDS560v2	XDS560v2 Mezzanine	1									300.00		600.00	3990.00
	Misc	1						100.00			300.00			1170.00
Total Current on individual power supply (mA)			100.00	2500.00	1000.00	445.00	1400.00	300.00	135.00	338.00	1344.00	48.00	600.00	
5% margin added over design (mA)			105.00	2625.00	1050.00	467.25	1470.00	315.00	141.75	354.90	1411.20	50.40	630.00	
Power Consumption in (mW)			78.75	2625.00	1050.00	560.70	2205.00	567.00	255.15	887.25	4656.96	166.32	3150.00	16202.13

Vin		
3.3V	TPS73701 -- 3.3V_Aux to 2.5V regulation	372.65 mA
3.3V	TPS73701 -- 3.3V_Aux to 1.8V_Aux regulation	330.75 mA
3.3V	TPS73701 -- 3.3V_Aux to 1.8VCC regulation	148.84 mA
3.3V	TPS73701 -- 3.3V_Aux to 1.2V regulation	490.61 mA
1.5V	TPS51200 -- 1.5V to 0.75V regulation	110.25 mA
12.0V	UCD7242 -- 12V to 1V_CVDD regulation	243.06 mA
12.0V	UCD7242 -- 12V to CVDD1 regulation	97.22 mA
12.0V	TPS54620 -- 12V to 1.5V regulation	219.48 mA
12.0V	TPS54620 -- 12V to 3.3V_AUX regulation	946.70 mA
12.0V	TPS54231 -- 12V to 5V regulation	328.13 mA
	Total Current @12V	1.83A
	Total Current @3.3V_AMC	0.05A
	Total Power Consumption	22.18W

Figure 4.1: C6657 Lite EVM Power Consumption

4.2 Power Supply Distribution

A high-level block diagram of the power supplies is shown in Figure 4.1. It is also shown in the schematic.

In Figure 4.1, the Auxiliary power rails are always on after payload power is supplied. These regulators support all control, sequencing, and boot logic. The Auxiliary Power rails contain:

- VCC3V3_AUX
- VCC1V8_AUX
- VCC1V2
- VCC5

The maximum allowable power is 22.5W from the external AC brick supply or from the 8 AMC header pins.

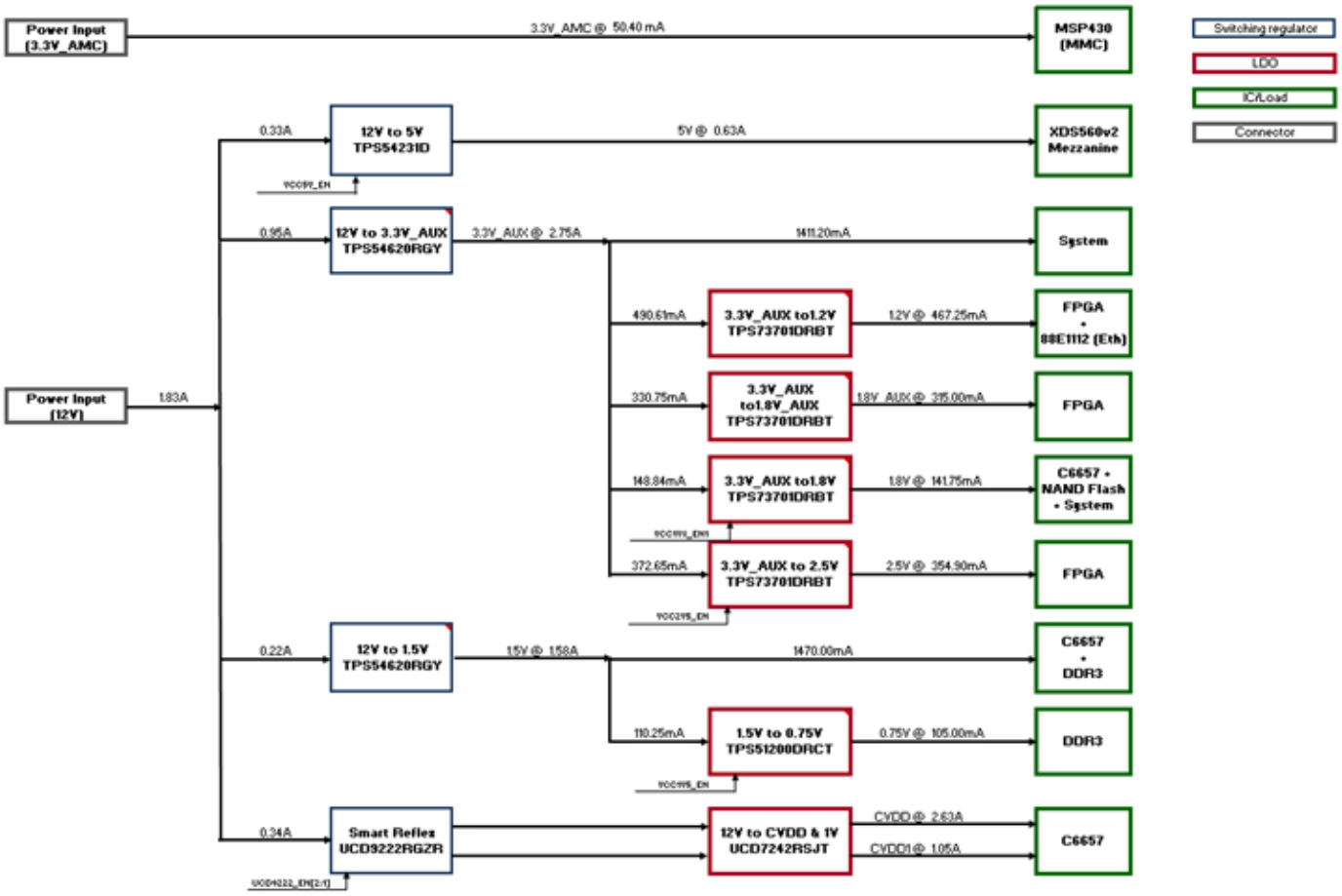


Figure 4.2: C6657 Lite EVM Power Generation Topology

Individual control for each (remaining) voltage regulator is provided to allow flexibility in how the power planes are sequenced (Refer to section 4.3 for specific details). The goal of all power supply designs is to support the ambient temperature range of 0°C to 45°C.

The TMS320C6657 core power is supplied using a dual digital controller coupled to a high performance FET driver IC. Additional DSP supply voltages are provided by discrete TI Swift power supplies. The TMS320C6657 supports a VID interface to enable Smart-Reflex® power supply control for its primary core logic supply. Refer to the TMS320C6657 Data Manual and other documentation for an explanation of the Smart-Reflex® control.

The EVM power topology is a combination of switching supplies and linear supplies. The linear supplies are used to save space for small loads. The switching supplies are implemented for larger loads. The switching supplies are listed below followed by explanations of critical component selection:

- CVDD (AVS core power for TMS320C6657)
- VCC1V0 (1.0V fixed core power for TMS320C6657)
- VCC3V3_AUX (3.3V power for peripherals)
- VCC1V5 (1.5V DDR3 power for TMS320C6657 and DDR3 memories)
- VCC5 (5.0V power for the XDS520V2 mezzanine card)

4.2.1 CVDD and VCC1V0 Design

The **CVDD** and **VCC1V0** power rails are regulated by TI Smart-Reflex controller UCD9222 and the dual synchronous-buck power driver UCD7242 to supply DSP AVS core and CVDD1 core power.

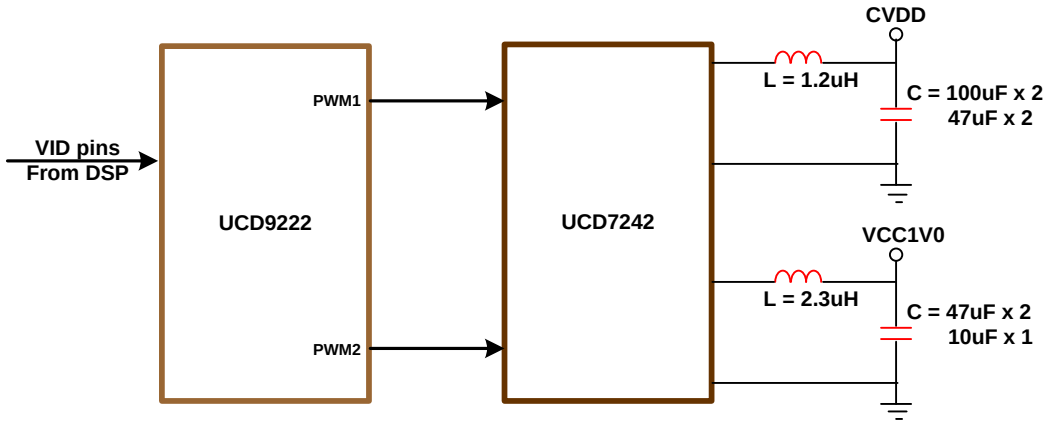
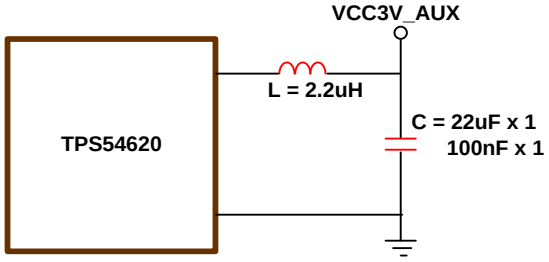


Figure 4.3: CVDD and VCC1V0 Design on C6657 Lite EVM

CVDD Inductor Calculation	**VCC1V0 Inductor Calculation**
$L = ((V_{in(max)} - V_{out})/\Delta I_{out}) * V_{out}/(V_{in(max)} * F_{sw})$ = ((12.5 - 1)/(2.7) * (1 / (12.5 * 750kHz)) = (11.5/2.7) * (1 / (9.375M)) = (4.26) * (0.107u) ≈ 0.46uH Reference Inductor = 1.2uH	$L = ((V_{in(max)} - V_{out})/\Delta I_{out}) * V_{out}/(V_{in(max)} * F_{sw})$ = ((12.5 - 1)/(1.1) * (1 / (12.5 * 750kHz)) = (11.5/1.1) * (1 / (9.375M)) = (4.26) * (0.107u) ≈ 1.12uH Reference Inductor = 2.3uH

4.2.2 VCC3V3_AUX and VCC1V5 Design

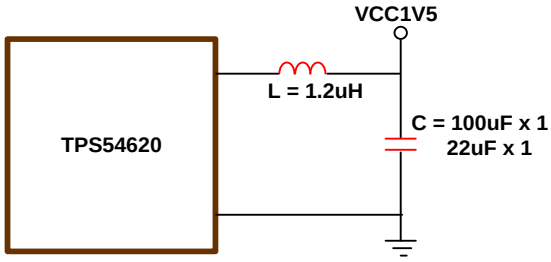
The **VCC3V3_AUX** and **VCC1V5** power rails are regulated by two TI 6A Synchronous Step Down SWIFT™ Converters, TPS54620, to supply the peripherals and other power sources and the DSP DDR3 EMIF and DDR3 memory chips respectively.



Over all tolerance 5%,
DC tolerance is 2.5%
K_{IND} = 0.3

Figure 4.4: VCC3V3_AUX Design on C6657 Lite EVM

Output Capacitor Calculation	**Inductor Calculation**
$C_{out(min1)} = (2*\Delta I_{out}) / (F_{sw}*\Delta V_{out})$ $= (2*1) / (900kHz*0.0825)$ $\approx 2.69uF$ $C_{out(min2)} = 1/(8*f_{sw})*I_{ripple}/V_{ripple}$ $= 1/(8*900kHz)*0.3/0.033$ $\approx 1.26uF$ Reference Capacitor = 22uF + 100nF	$L = ((V_{in(max)} - V_{out})/(I_{out} * K_{ind})) * (V_{out}/(V_{in(max)} * F_{sw}))$ $= ((12.5 - 3.3)/(3 * 0.3) * (3.3 / (12.5 * 900kHz))$ $= ((9.2/(3 * 0.3) * (3.3 / (11.25M))$ $= (10.22) * (0.29u)$ $\approx 2.96uH$ Reference Inductor = 2.2uH

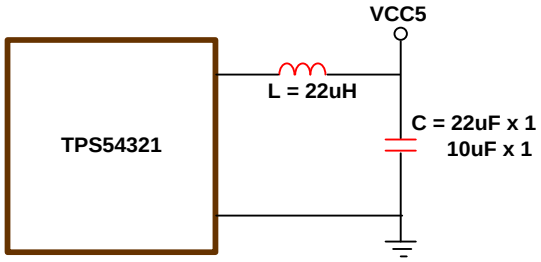


Over all tolerance 5%,
DC tolerance is 2.5%
K_{IND} = 0.3

Figure 4.5: VCC1V5 Power Design on C6657 Lite EVM

Output Capacitor Calculation	**Inductor Calculation**
$C_{out(min)} = (2*\Delta I_{out}) / (F_{sw}*\Delta V_{out})$ $= (2*1)/(900kHz*0.075)$ $\approx 29.62uF$ $C_{out(min2)} = 1/(8*f_{sw})*I_{ripple}/V_{ripple}$ $= 1/(8*900kHz)*0.2/0.015$ $\approx 1.85uF$ Reference Capacitor = 100uF + 22uF	$L = ((V_{in(max)} - V_{out})/(I_{out} * K_{ind})) * (V_{out}/(V_{in(max)} * F_{sw}))$ $= ((12.5 - 1.5)/(2 * 0.3)) * (1.5 / (12.5*900kHz))$ $= (11/0.6) * (1.5 / (11.25M))$ $= (18.33) * (0.1333u)$ $\approx 2.44uH$ Reference Inductor = 1.2uH

4.2.3 VCC5 Design



Over all tolerance 5%,
DC tolerance is 2.5%
K_{IND} = 0.3

Figure 4.6: VCC5 Power Design on C6657 Lite EVM

Output Capacitor Calculation	**Inductor Calculation**
$C_{out(min)} = 1 / (2\pi*(V_o/I_o)*F_{co(max)})$ $= 1/(2 * 3.14 * (5/0.8)* 570kHz)$ $\approx 44.7nF$ Reference Capacitor = 22uF + 10uF	$L = ((V_{in(max)} - V_{out})/(I_{out} * K_{ind})) * (V_{out}/(V_{in(max)} * F_{sw}))$ $= ((12.5 - 5)/(0.8 * 0.3) * (5 / (12.5 * 570kHz))$ $= (7.5/0.24) * (5 / (7.125M))$ $= (31.25) * (0.7M)$ $\approx 21.87uH$ Reference Inductor = 22uH

The **VCC5** power rail is regulated by TI 2A Step Down SWIFT™ DC/DC Converter, TPS54231, to supply the power of the XDS560v2 Mezzanine Card on C6657 Lite EVM.

4.3 Power Supply Boot Sequence

Specific power supply and clock timing sequences are identified below. The TMS320C6657 DSP requires specific power up and power down sequencing. Figure 4.2 and Figure 4.3 illustrate the proper boot up and down sequence. Table 4.3 provides specific timing details for Figure 4.6 and Figure 4.7.

Refer to TMS320C6657 Data Manual for confirmation of specific sequencing and timing requirements.

Table 4.2: Power-up and down timing on C6657 Lite EVM

Step	Power Rails	Timing	Description
	Power-Up		
1	VCC12 (AMC Payload power), VCC3V3_AUX, VCC1V8_AUX VCC1V2	Auto	When 12V power is supplied to C6657 Lite EVM then 3.3V, 1.8V and 1.2V supplies to FPGA will turn on. FPGA outputs to DSP will be locked (held at ground).
2	VCC5,VCC2V5	10ms	Turn on VCC5 and VCC2V5 after VCC3V3 is stable for 10ms.
3	CVDD (DSP AVS core power)	5ms	Enable CVDD (UCD9222 power rail#1) after both of VCC5 and VCC2V5 are stable for 5ms.
4	VCC1V0 (DSP CVDD1 fixed core power)	5ms	Enable VCC1V0 (UCD222 power rail#2) 5ms after CVDD has stabilized. The start-

			delay time is set by UCD9222 configuration file.
5	VCC1V8 (DSP IO power)	5ms	Turn on VCC1V8 after VCC1V0 is stable for 5ms.
6	CDCE62005#2 initiations FPGA 1.8V outputs	5ms	Unlock 1.8V outputs and initiate CDCE62005 after VCC1V8 is stable for 5ms by de-asserting power down (PD#) pins.
7	VCC1V5 (DSP DDR3 power)	5ms	Turn on VCC1V5 5ms after the initiation of CDCE62005.
8	VCC0V75	5ms	Turn on VCC0V75 after VCC1V5 is stable for 5ms. When VCC1V5 is valid, FPGA de-asserts the power down pin of IDT5V41068, PCIe clock multiplexor. When VCC0V75 is valid, FPGA enables mux clock outputs asserting OE pin.
9	RESETz Other reset and NMI pins	5ms	De-asserts RESETz and unlocks other reset and NMI pins for DSP after VCC0V75 is stable and CDCE62005 PLL locked for 5ms. In the meanwhile, FPGA will drive the boot configurations to DSP GPIO pins.
10	PORz	5ms	De-asserts PORz after RESETz is de-asserted for 5ms.
11	RESETFULLz	5ms	De-asserts RESETFULLz after PORz is de-asserted for 5ms.
12	DSP GPIO pins for boot configurations	1ms	Releases DSP GPIO pins after RESETFULLz is de-asserted for 1ms
	Power-Down		
13	RESETFULLz PORz	0ms	If there is a power failure or AMC payload is powered off, FPGA will assert RESETFULLz and PORz signals to DSP.
14	FPGA 1.8V outputs CDCE62005 PD# pins	5ms	Locks 1.8V output pins on FPGA and pull CDCE62005 PD# pin to low to disable DSP clocks
15	CVDD VCC1V0 VCC1V8 VCC1V5 VCC0V75 VCC2V5 IDT5V41068 PD# and OE	0ms	Turns off all main power rails.

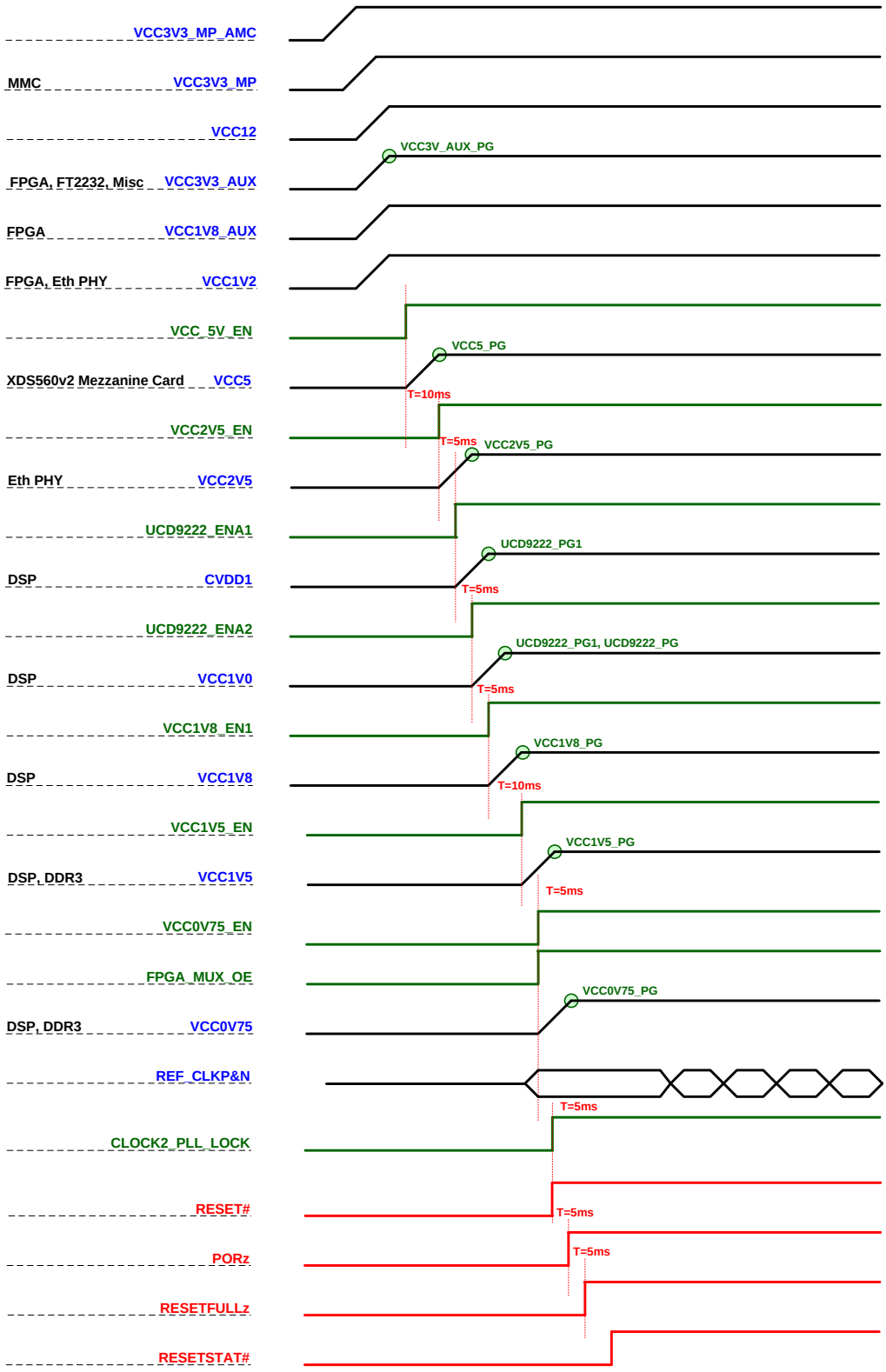


Figure 4.7: Initial Power Up Sequence Timing Diagram

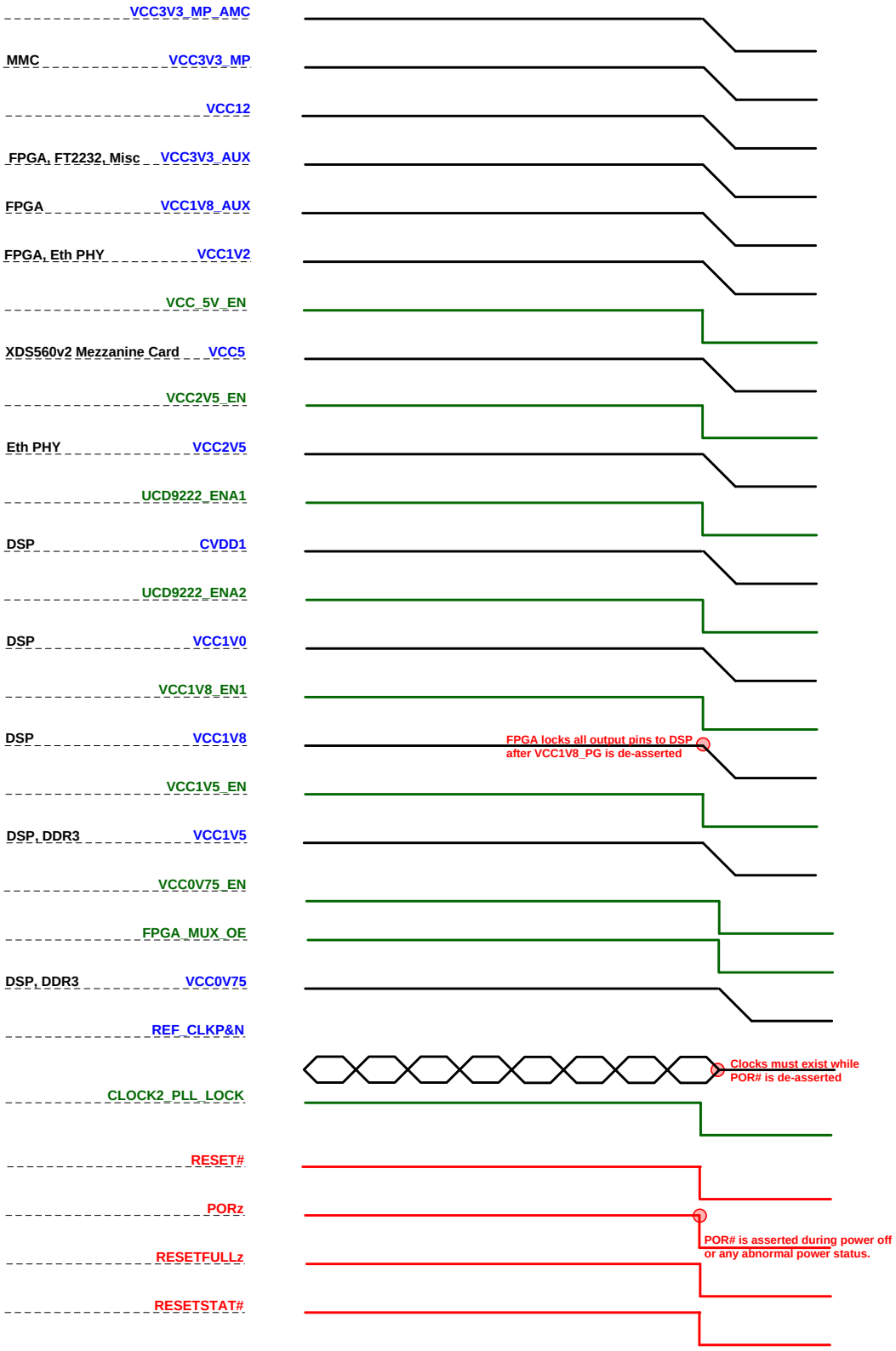


Figure 4.8: Power Down Sequence Timing Diagram

5. C6657 Lite EVM FPGA Functional Description

This chapter describes the FPGA functionality of C6657 Lite EVM board. It contains:

5.1 FPGA Overview

The FPGA (Xilinx XC3S200AN) controls EVM power sequencing, reset mechanism, DSP boot mode configuration and clock initialization. It also provides the transformation of TDM Frame Synchronization signal and Reference Clock between AMC connector and DSP.

The FPGA also supports 4 user LEDs and 1 user switch through control registers. All FPGA registers are accessible by TMS320C6657 DSP.

The key features of C6657 Lite EVM EVM FPGA are:

- C6657 Lite EVM Power Sequence Control
- C6657 Lite EVM Reset Mechanism Control
- C6657 Lite EVM Clock Generator Initialization and Control
- TMS320C6657 DSP SPI Interface for Accessing FPGA Configurable Registers
- Provides Shadow Registers for TMS320C6657 DSP to Access Clock Generator Configurations Registers
- Provides Shadow Registers for TMS320C6657 DSP to Access UCD9222 Devices via PM Bus (RFU)
- Provides TMS320C6657 DSP Boot Mode Configuration switch settings to DSP
- MMC Reset Events Initiation Interface
- Provides transformation of TDM Frame Synchronization and Reference Clock between AMC and DSP
- Provide Ethernet PHY Interrupt (RFU) and Reset Control Interface
- Provides support for Reset Buttons, User Switches and Debug LEDs

5.2 FPGA signals description

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. Throughout this manual, a '#' or 'Z' will be used at the end of a signal name to indicate that the active or asserted state occurs when the signal is at a low voltage level.

The following notations are used to describe the signal and type.

Table 5.1: Pin Type Notation Interpretation

Pin Type	Function
I	Input Pin
O	Output Pin
I/O	Bidirectional Pin
Differential	Differential Pair Pins
PU	Internal Pull-Up
PD	Internal Pull-Down

Table 5.2: C6657 Lite EVM FPGA Pin Description

Pin Name	I/O Type	Description
MMC Control		
MMC_DETECT#	I PU	**MMC Detection on the insertion to an AMC Chassis:** This signal is an insertion indication from MMC. The MMC will drive logic low state when EVM module is inserted into an AMC chassis.
MMC_RSTSTAT#	O	**RESETSTAT# state to MMC:** FPGA will drive the status of DSP RESETSTAT# to MMC via this signal.
MMC_POR_AMC#	I PU	**MMC POR Request:** This signal is used by MMC to request a power-on reset sequence to DSP. A logic Low to High transition on this signal will complete FPGA Full Reset sequence with a specified delay.
MMC_WR_AMC#	I PU	**MMC WARM Request:** This signal is used by MMC to initiate a warm reset request. A logic Low to High transition on this signal will complete FPGA warm reset sequence with a specified delay.
MMC_BOOTCOMP	O	**BOOTCOMPLETE state to MMC:** FPGA will drive the status of DSP BOOTCOMPLETE to MMC via this signal.
Power Sequence Control		
VCC5_PG	I	**5V Voltage Power Good Indication:** Indicates that 5V power is valid.
VCC2V5_PG	I	**2.5V Voltage Power Good Indication:** Indicates that 2.5V power is valid.
VCC3_AUX_PG	I	**3.3V Auxiliary Voltage Power Good Indication:** Indicates that 3.3V auxiliary power is valid.
VCC0P75_PG	I	**0.75V Voltage Power Good Indication:** Indicates that 0.75V power is valid.
VCC1P5_PG	I	**1.5V Voltage Power Good Indication:** Indicates that 1.5V power is valid.
VCC1P8_PG	I	**1.8V Voltage Power Good Indication:** Indicates that 1.8V power is valid.
VCC1V8_EN1	O	**1.8V Voltage Power Supply Enable:** Enable for 1.8V power rail.
VCC0V75_EN	O	**0.75V Voltage Power Supply Enable:** Enable for 0.75V power rail.
VCC2V5_EN	O	**2.5V Voltage Power Supply Enable:** Enable for 2.5V power rail.

VCC_5V_EN	O	**5V Voltage Power Supply Enable:** Enable for 5V power rail.
SYS_PGOOD	O	**System Power Good Indication:** Asserted by FPGA to system when all power supplies are valid.
Clock Configuration		
CLOCK2_SSPCS1	O	**SPI Chip Select Enable:** Connected to Clock Generator SPI_LE pin. Falling edge of SSPCS1 initiates a transfer. If SSPCS1 is high, no data transfer can take place.
CLOCK2_SSPCK	O	**SPI Serial Clock:** Connected to Clock Generator SPI_CLK pin. FPGA SPI bus clocks data in and out on the rising edge of SSPCK. Data transitions therefore occur on the falling edge of this clock.
CLOCK2_SSPSI	O	**SPI Serial Data MOSI:** Connected to Clock Generator MOSI pin. This signal is used for serial data transfers from master (FPGA) output to slave (CDCE62005) input.
CLOCK2_SSPSO	I PU	**SPI Serial Data MISO:** Connected to Clock Generator MISO pin. This signal is used for the serial data transfers from slave (CDCE62005) output to master (FPGA) input.
REFCLK2_PD#	O	**CLOCK Generator Power Down:** Places Clock Generator into power down state forcing the differential clock output into high-impedance state.
UCD9222 Interface :		
UCD9222_PG1	I	**UCD9222 Power Good Indication for CVDD DSP Core Power:** Indicates that CVDD DSP core power is valid.
UCD9222_ENA1	O	**UCD9222 Enable for CVDD DSP Core Power:** Enables CVDD DSP core power rail.
UCD9222_PG2	I	**UCD9222 Power Good Indication for VCC1V0 DSP Core Power:** Indicates that VCC1V0 DSP core power is valid.
UCD9222_ENA2	O	**UCD9222 Enable for CVDD DSP Core Power:** Enables VCC1V0 DSP core power rail.
PGUCD9222	I	**UCD9222 Power Good Indication:** Indicates both DSP core supplies - CVDD and VCC1V0 are valid.
UCD9222_RST#	O	**UCD9222 Reset:** An active low signal will reset UCD9222 device.
PM BUS : (RFU)		
PMBUS_CLK	O	**PM Bus Clock:** FPGA provided clock source on PM bus.
PMBUS_DAT	I/O	**PM Bus Data:** A PM Bus slave device can receive data provided by master (FPGA), or it can also provide data to master (FPGA) via this signal line.
PMBUS_ALT	I	**PM Bus Alert:** A PM Bus device may notify the host (FPGA) via this signal if a fault or warning is detected.
PMBUS_CTL	I PU	**PM Bus Control:** Used to turn on/off the device in conjunction with UCD9222_ENA1 / UCD9222_ENA2 pins.
PHY Interface :		
PHY_INT#	I	Interrupt Request from 88E112 PHY (RFU)

PHY_RST#	O	**Reset to 88E1112 PHY:** Used to reset the PHY device. PHY_RST# will be asserted during active DSP_PORZ or DSP_RESETFULLZ period. The PHY_RST# logic also can be configured by the DSP accessed register.
DSP SPI :		
DSP_SSPCS1	I	**DSP SPI Chip Select 1:** Connected to DSP SPISCS1 pin. The falling edge of SSPCS1 from DSP will initiate a transfer. If SSPCS1 is high, no data transfer can take place.
DSP_SSPCK	I	**DSP SPI Serial Clock:** Connected to DSP SPICLK pin. The FPGA SPI bus clocks data in on the falling edge of SSPCK. Data transitions therefore occur on the rising edge of this clock.
DSP_SSPMISO	O	**DSP SPI Serial Data MISO:** Connected to the DSP SPIDIN pin. This signal is used for serial data transfers from slave (FPGA) output to master (DSP) input in the DSP_SSPCS1 asserted period.
DSP_SSPMOSI	I	**DSP SPI Serial Data MOSI:** Connected to the DSP SPIDOUT pin. This signal is used for serial data transfers from master (DSP) output to slave (FPGA) input.
RESET Buttons and Requests :		
FULL_RESET	I	**Full Reset Button Input:** This button input is used to initiate a Full Reset event.
WARM_RESET	I	**Warm Reset Button Input:** This button input is used to initiate a Warm Reset event.
COLD_RESET (RFU)	I	**Cold Reset Button Input:** Reserved for Future Use (RFU).
FPGA_JTAG_RST# (RFU)	I	**FPGA JTAG Reset Input:** Reserved for Future Use (RFU).
TRGRSTZ	I	**Reset Request from the DSP Emulator Header:** A warm Reset sequence will be initiated if an active TRGRSTZ event is recognized by FPGA.
DSP Boot & Device configurations :		
BM_GPIO[0 : 15]	I	**DSP Boot Mode Strap Configurations:** These switch inputs are used to drive the DSP boot mode configuration during EVM power up period.
DSP_GPIO[0 : 15]	I/O	**DSP GPIO:** In normal operation mode, these signals are not driven by FPGA so that DSP can use them as GPIO pins. During EVM power-on or during RESETFULLz asserted period, FPGA will output the BM_GPIO switch values to DSP on these pins so that DSP can latch the boot mode configuration.
DSP RESET & Interrupts Control :		
DSP_CORESEL[1:0]	O	**DSP Core Selection Bit:** The default value is 0000b and Register bits define the state of these pins.
DSP_PACLKSEL	O	**DSP PACLKSEL:** This pin is used for DSP PASS clock selection setting. The logic of this signal is derived from the BM_GPIO [13:11] state or configured by FPGA registers.

DSP_LRESETNMIENZ	O	**Latch Enable for DSP Local Reset and NMI inputs:** The default value is 1b and a register bit defines the state of this pin.
DSP_NMIZ	O	**DSP NMI:** The default value is 1b and unlocked a register bit defines the state of this pin.
DSP_LRESETZ	O	**DSP Local Reset:** The default value is 1b and a register bit defines the state of this pin.
DSP_HOUT	I	**DSP HOUT**
DSP_BOOTCOMPLETE	I	**DSP Boot Complete Indication**
DSP_SYSCLKOUT	I	**DSP System Clock Output**
DSP_PORZ	O	**DSP Power-On Reset**
DSP_RESETFULLZ	O	**DSP Full Reset**
DSP_RESETZ	O	**DSP Reset**
FPGA Storage (RFU):		
FPGA_SPI_CS#	O	**FPGA SPI Chip Select:** (RFU)
FPGA_SPI_SI	O	**FPGA SPI Serial Data MOSI:** (RFU)
FPGA_SPI_SCK	O	**FPGA SPI Clock Output:** (RFU)
FPGA_SPI_SO	I	**FPGA SPI Serial Data MISO:** (RFU)
DSP TDM CLK :		
DSP_TSIP0_FS[A:B]0		**DSP TSIP0_FS[A:B]0:** The single-ended clock (DSP_TSIP0_FSA0 and DSP_TSIP0_FSB0) outputs are derived from the differential TDM Frame Synchronization (TDM_CLKC) input.
DSP_TSIP1_FS[A:B]1		**DSP TSIP1_FS[A:B]1:** The single-ended clock (DSP_TSIP1_FSA1 and DSP_TSIP1_FSB1) outputs are derived from the differential TDM Frame Synchronization (TDM_CLKC) input.
DSP_TSIP0_CLK[A:B]0		**DSP TSIP0_CLK[A:B]0:** The single-ended clock (DSP_TSIP0_CLKA0 and DSP_TSIP0_CLKB0) outputs are derived from the differential TDM clock (TDM_CLKA) input.
DSP_TSIP1_CLK[A:B]1		**DSP TSIP1_CLK[A:B]1:** The single-ended clock (DSP_TSIP1_CLKA1 and DSP_TSIP1_CLKB1) outputs are derived from the differential TDM clock (TDM_CLKA) input.
TDM_CLKA[p/n]	I, Diff	**TDM_CLKA Different Clock Input Pairs:** The reference clock referring to TSIP0/1 CLKs of DSP.
TDM_CLKB[p/n] (RFU)	I, Diff	**TDM_CLKA Different Clock Input Pairs:** The reference clock referring to TSIP0/1 CLKs of DSP.
TDM_CLKC[p/n]	I, Diff	**TDM_CLKA Different Clock Input Pairs:** The reference clock referring to TSIP0/1 CLKs of DSP.
TDM_CLKD[p/n] (RFU)	I, Diff	**TDM_CLKA Different Clock Input Pairs:** The reference clock referring to TSIP0/1 CLKs of DSP.
DEBUG LED:		
DEBUG_LED[1:4]	O	**Debug LED:** These LEDs are used for debugging purpose only. Can be configured by the FPGA registers
Miscellaneous:		
MAIN_48MHZ_CLK_R	I	**FPGA Main Clock Source:** A 48 MHz clock is used as the FPGA main clock source.

DSP_TIMI0	O	**DSP Timer 0 Clock:** FPGA provides a 24MHz clock to the DSP timer 0 input. During EVM Power-on or RESETFULLZ asserted period, FPGA will drive the PCIESSEN switch state to DSP for latching.
DSP_TIMI1	O	**DSP Timer 1 Clock:** FPGA provides a 24MHz clock to the DSP timer 1 input. During EVM Power-on or RESETFULLZ asserted period, FPGA will drive the PCIESSEN switch state to DSP for latching.
DSP_TIMO0	I	
DSP_TIMO1	I	
DSP_VCL_1 (RFU)	I	**DSP Smart Reflex I2C Clock**
DSP_VD_1 (RFU)	I/O	**DSP Smart Reflex I2C Clock**
PCA9306_EN	O	**PCA9306 Enable:** Used to enable DSP Smart Reflex I2C buffer function.
NAND_WP#	O	**NAND Flash Write Protect:** Used to control NAND flash write-protect function.
NOR_WP#	O	**NOR Flash Write Protect:** Used to control NOR flash write-protect function.
EEPROM_WP	O	**EEPROM Write Protect:** Used to control EEPROM write-protect function.
PCIESSEN	I	**PCIe Subsystem Enable:** Used for PCIESSEN switch input.
USER_DEFINE	I	**User Defined Switch:** Reserved for user defined switch input.
MUX_SEL	O	**PCIe Clock Multiplexor Input selection:** Selects PCIE reference clock from CDCE62005 or AMC edge connector. The default is from CDCE62005. Also, when PCIe boot mode is selected, SW5.3 controls the default level for the register and this clock select.
MUX_PD#	O	**PCIe Clock Multiplexor Power Down:** Used to control PCIe mux PD# pin, it's de-asserted after VCC1V5 valid.
MUX_OE	O	**PCIe Clock Multiplexor Output Enable:** Enables the output of PCIe mux.
VID_OE#	O	**Smart-Reflex VID Enable:** Enables the output of Smart-Reflex VID from DSP to UCD9222.
XDS560_IL	O	**XDS560 IL:** XDS560 IL control signal
FPGA JTAG TAP Control Port:		
JTAG_FPGA_TCK	I	**FPGA JTAG Clock Input**
JTAG_FPGA_TDI	I	**FPGA JTAG Data Input**
JTAG_FPGA_TDI	O	**FPGA JTAG Data Output**
JTAG_FPGA_TMS	I	**FPGA JTAG Mode Select Input**
JTAG_FPGA_RST#	I	**FPGA JTAG Reset** (RFU)

5.3 Sequence of operation

This section describes the FPGA sequence of operation on the EVM. It contains:

5.3.3 Boot Configuration Timing
5.3.4 Boot Configuration Forced in I2C Boot

5.3.1 Power-On Sequence

The following section provides details of the FPGA Power-On sequence of operation.

1. After the EVM 3.3V auxiliary voltage (VCC3V3_AUX_PG) is valid and stable, and FPGA design code is loaded, the FPGA is ready for the Power-On sequence of operation.
2. The FPGA starts to execute the Power-On sequence. Wait for 10 ms, the FPGA enable the 2.5V power.
3. Once the 2.5V voltages (VCC5_PG and VCC2V5_PG) are valid, wait for 5ms, FPGA asserts the UCD9222_ENA1 and UCD9222_ENA2 to enable the CVDD and VCC1V0 DSP core power.
4. After UCD9222_PG1, UCD9222_PG2 and PGUCD9222 are all valid; FPGA waits for 5ms and then enables 1.8V power.
5. After the 1.8V voltage is valid (VCC1V8_PG asserted), wait for 5ms and then:
    a. Unlock the 1.8V outputs on the FPGA,
    b. De-assert clock generator PD# pin; after driving PD# to high for 1ms, FPGA starts to initialize clock generator.
6. After finishing the initiation of clock generator, FPGA waits and then enables 1.5V power rail.
7. Once the 1.5V voltage is valid (VCC1V5_PG), FPGA waits for 5ms and then enables 0.75V power and Level shift component output and initializes the clock mux.
8. After 0.75V voltage is valid (VCC0V75_PG asserted), wait for 5ms and check the clock generator PLL_LOCK states and FPGA asserts clock MUX OE pin, after the PLL state of clock generator is valid, the FPGA de-asserts DSP_RESETz and DSP_LRESETz and keeps DSP_PORz and DSP_RESETFULLz in assertion.
9. After DSP_RESETz and DSP_LRESETz have been de-asserted, FPGA wait for 5ms and then de-asserts DSP_PORz and keeps DSP_RESETFULLz still being asserted. Waits for another 5ms, then FPGA de-asserts DSP_RESETFULLz. The FPGA will drive BM_GPIO switches value to DSP for the DSP boot mode configuration strapping during the period from VCC0P75_PG is valid to the RESETSTAT# being de-asserted. FPGA will also drive the PCIESSEN switch value to DSP_TIMI0 for the DSP boot configuration strapping.
10. Wait for RESETSTAT# signal from DSP to go from low to high. The EVM Power-On sequence is completed.

5.3.2 Power Off Sequence

Following section provides details of FPGA power off sequence of operation.

1. Once the system powers on, any power failure event (any one of power good signals de-asserted) will trigger the FPGA to proceed to the power off sequence.
2. Once any de-asserted Power Good signals have been detected by FPGA, it will assert the DSP_PORz and DSP_RESETFULLz to DSP immediately.
3. Wait for 5ms, FPGA will disable all the system power rails by the enable pins and clock generator by the power down pin, assert all the other DSP resets to DSP, lock the +1.8V output pins from FPGA to DSP.
4. FPGA remains in the power failure state until main 12V power is removed and restored.

5.3.3 Boot Configuration Timing

The boot configuration timing of the power-up and the RESETFULLz event are shown below.

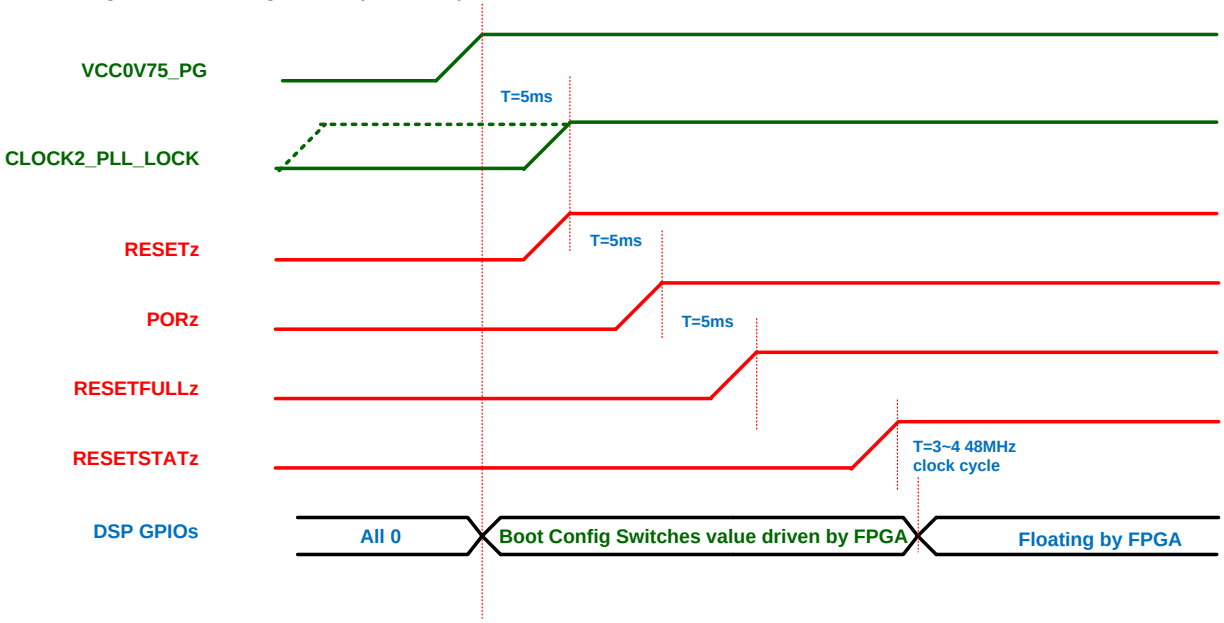


Figure 5.1: Power-On Reset Boot Configuration Timing

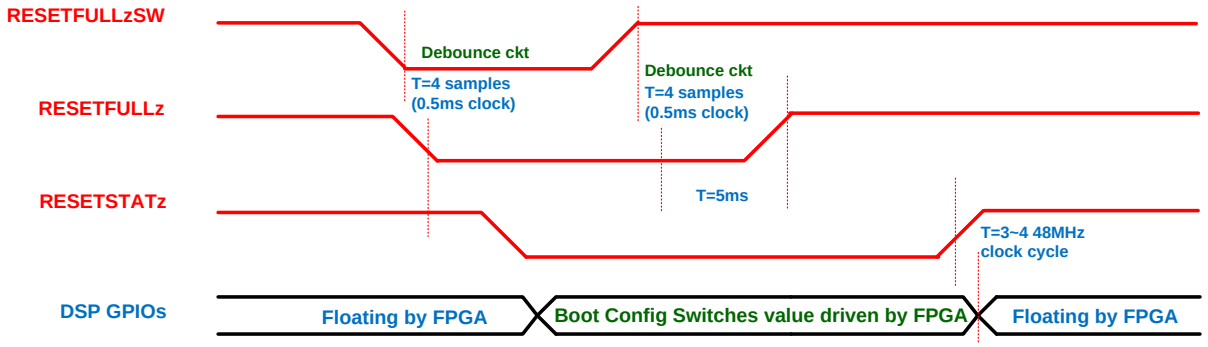


Figure 5.2: Reset-Full Switch/Trigger Boot Configuration Timing

5.3.4 Boot Configuration Forced in I2C Boot

Note: This workaround is only needed with PG1.0 samples of the TMS320C6657 DSP. For reliable PLL operation at boot-up, the FPGA will force the DSP to boot from the I2C by providing the boot configuration value as 0x0405 on the boot mode pins [12:0]. After the code in the I2C SEEPROM executes to initialize the PLLs, it will read the true values on the DIP switches from the registers in the FPGA and then boot as if the normal boot sequence had occurred.

The exception for the forced I2C boot is the emulation boot. The FPGA will not perform the I2C boot configuration override when the DIP switches have the following configuration: BOOTMODE[2:0] (GPIO[3:1]) = [000] and BOOTMODE[5:4] (GPIO[6:5]) = [00]. Therefore, the additional logic of the FPGA will allow the emulation boot to latch directly from the DIP switches.

5.4 Reset definition

5.4.1 Reset Behavior

- **Power-On:** The Power-On behavior includes initiating and sequencing the power sources, clock sources and then DSP startup. Please refer to the section 5.5.1 for detailed sequence and operations.
- **Full Reset:** The RESETFULLz is asserted low to the DSP. This causes RESETSTAT# to go low which triggers the boot configuration to be driven from the FPGA. Reset to the Marvell PHY is also asserted. POR# and RESET# to the DSP remain high. The power supplies and clocks operate without interruption. Please refer to the section 5.5.3 for detailed timing diagrams.
- **Warm Reset:** The RESETz is asserted low to the DSP. The PORz and RESETFULLz to the DSP remain high. The power supplies and clocks operate without interruption.

5.4.2 Reset Switches and Triggers

- **FULL_RESET (RST_FULL1)**: A logic low state with a low to high transition will trigger a Full Reset behavior event.

When the push button switch RST_FULL1 is pressed, FPGA on EVM will assert DSP's RESETFULL# input to issue a total reset of the DSP, everything on the DSP will be reset to its default state in response to this event, boot configurations will be latched and the ROM boot process will be initiated.

This is equivalent to a power cycle of the board but POR and will have following effects:
* Reset DSP
* Reset Gigabit Ethernet PHY
* Reload boot parameters.
* Protect the contents in the I2C EEPROM, NAND flash and SPI NOR flash.

- **WARM_RESET (RST_WARM1):** A logic low state with a low to high transition will trigger a warm reset behavior event.

When the push button Switch RST_WARM1 is pressed, FPGA will assert a DSP RESET# input, which will reset the DSP. Software can program this to be either hard or soft. Hard reset is the default which resets

almost everything. Soft Reset will behave like Hard Reset except that PCIe MMRs, EMIF16 MMRs, DDR3 EMIF MMRs, and External Memory contents are retained.

Boot configurations are not latched by Warm Reset. Also, Warm Reset will not reset blocks supporting Reset Isolation when they are appropriately configured previously by application software. Warm Reset must be used to wake from low-power sleep and hibernation modes.

In the case of a Soft Reset, the clock logic or the power control logic of the peripherals are not affected, and, therefore, the enabled/disabled state of the peripherals is not affected. The following external memory contents are maintained

During a Soft Reset:

- **DDR3 MMRs:** The DDR3 Memory Controller registers are not reset. In addition, the DDR3 SDRAM memory content is retained if the user places the DDR3 SDRAM in self-refresh mode before invoking the soft reset.
- **PCIe MMRs:** The contents of the memory connected to the EMIFA are retained. The EMIFA registers are not reset.

- **COLD_RESET (RST_COLD1):** Not used in current implementation.
- **MMC_POR_IN_AMC#:** A logic low state with a low to high transition will trigger a Full Reset behavior event.
- **MMC_WR_AMC#:** A logic low state with a low to high transition will trigger a warm reset behavior event.
- **TRGRSTz:** A logic low state with a low to high transition on the Target Reset signal from emulation header that will trigger a warm reset behavior event.
- **FPGA_JTAG_RST#:** Not used in current implementation.

5.5 SPI Protocol

This section describes the FPGA SPI bus protocol design specification for interfacing with TMS320C6657 DSP and CDCE62005 clock generator. It contains:

5.5.1 FPGA DSP SPI Protocol
5.5.2 FPGA Clock Generator SPI Protocol

5.5.1 FPGA-DSP SPI Protocol

FPGA supports simple write and read commands for TMS320C6657 DSP to access the FPGA configuration registers through SPI interface. The FPGA SPI bus clocks data in on the falling edge of DSP SPI Clock. Data transitions therefore occur on the rising edge of the clock.

The figures below illustrate a DSP to FPGA SPI write operation.

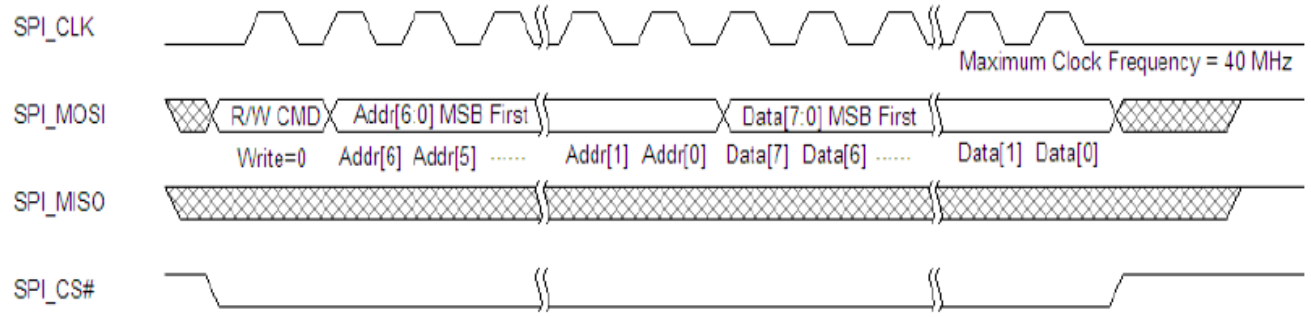


Figure 5.3: SPI access from TMS320C6657 to FPGA (WRITE / high level)

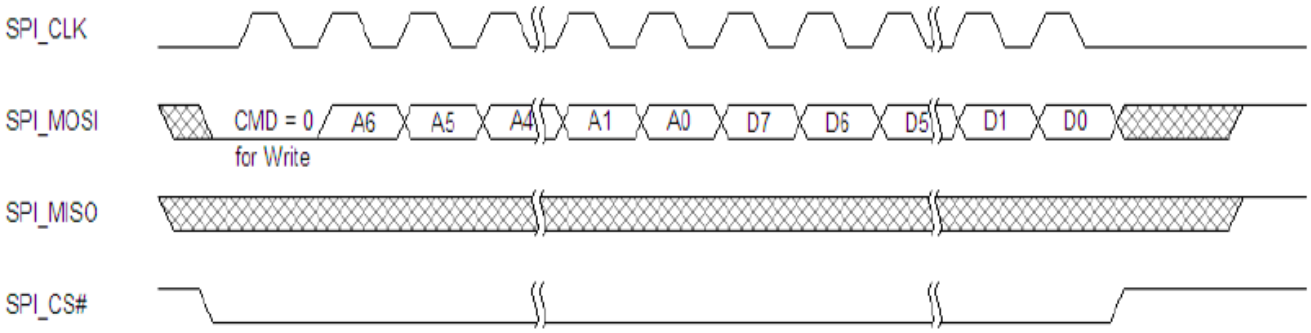


Figure 5.4: SPI access from TMS320C6657 to FPGA (WRITE)

The below figures illustrate a DSP to FPGA SPI read operation.

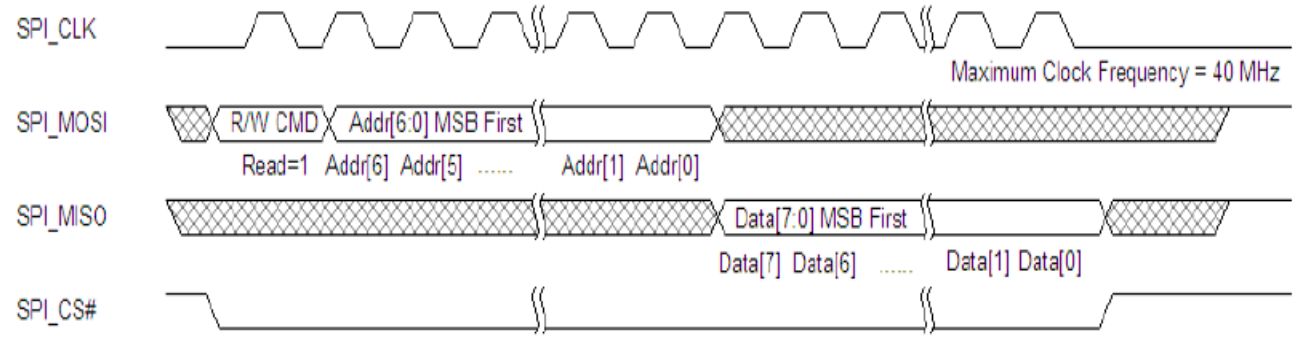


Figure 5.5: SPI access from TMS320C6657 to FPGA (READ / high level)

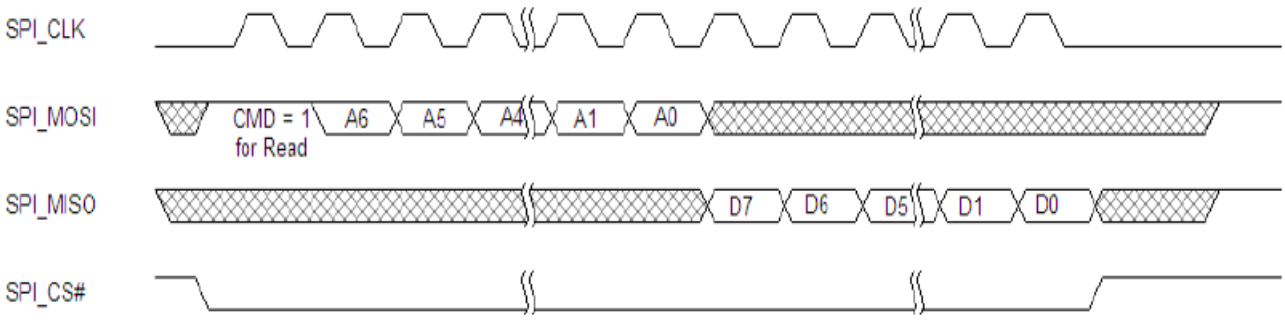


Figure 5.6: SPI access from TMS320C6657 to FPGA (READ)

5.5.2 FPGA- CDCE62005 (Clock Generator) SPI Protocol

The FPGA-Clock Generator SPI interface protocol is compatible to CDCE62005 SPI. The FPGA SPI bus clocks data in on the rising edge of DSP SPI Clock. Data transitions therefore occur on the falling edge of the clock.

The figure below illustrates a FPGA to CDCD62005 SPI write operation.

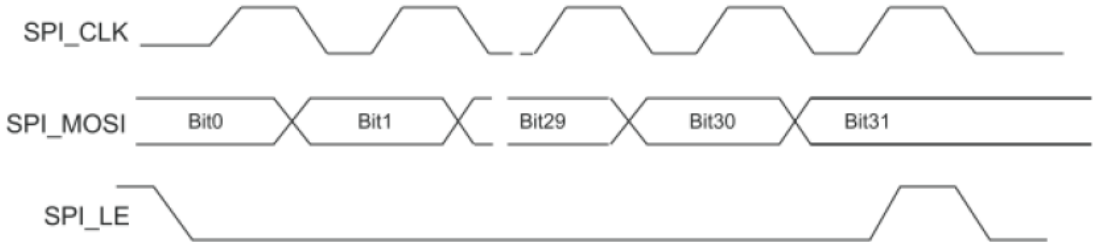


Figure 5.7: SPI access from FPGA to CDCE62005 (WRITE)

The figure below illustrates a FPGA to CDCD62005 SPI read operation.

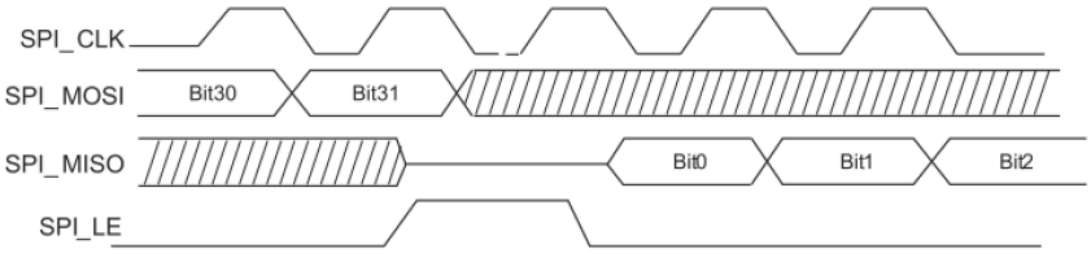


Figure 5.8: SPI access from FPGA to CDCE62005 (READ)

5.6 FPGA Configuration Registers

The TMS320C6657 DSP communicates with the FPGA configuration registers through the SPI interface. These registers are addressed by memory mapped location and defined by the DSP SPI chip enable setting. The following tables list the FPGA configuration registers and the respective descriptions.

Table 5.3: C6657 Lite EVM FPGA Pin Description

Memory Map Base Address	Memory Map Offset Address	Memory
DSP SPI Chip Select 1 0x20BF0000-0x20BF03FF (TMS320C6657 DSP SPI Memory Map Address)	0x00-0x3F	Configuration Registers

5.6.1 FPGA Configuration Registers Summary

Table 5.4: FPGA Configuration Registers Summary

Address Offset	Definition	Attribute (R/W) (RO : Read-Only)	Default Value
00h	FPGA Device ID (Low Byte)	RO	04h
01h	FPGA Device ID (High Byte)	RO	80h
02h	FPGA Revision ID (Low Byte)	RO	**
03h	FPGA Revision ID (High Byte)	RO	00h*
04h	BM GPI Status (Low Byte)	RO	----
05h	BM GPI Status (High Byte)	RO	----
06h	DSP GPI Status (Low Byte)	RO	----
07h	DSP GPI status (High Byte)	RO	----
08h	Debug LED	R/W	00h
09h	MMC Control	RO	----
0Ah	PHY Control	R/W	03h
0Bh	Reset Buttons Status	RO	00h
0Ch	Miscellaneous - 1	R/W	1Ch
0Dh	Miscellaneous - 2	RO	--
0Eh	FPGA FW Update SPI Interface Control Register	R/W	00h
0Fh	Scratch Register	R/W	00h
10h	CLK-GEN 2 Control Register	R/W	00h
11h	CLK-GEN 2 Interface Clock Setting	R/W	03h
13h~12h	Reserved		0s
14h	CLK-GEN 2 Command Byte 0	R/W	00h
15h	CLK-GEN 2 Command Byte 1	R/W	00h

16h	CLK-GEN 2 Command Byte 2	R/W	00h
17h	CLK-GEN 2 Command Byte 3	R/W	00h
18h	CLK-GEN 2 Read Data Byte 0	RO	00h
19h	CLK-GEN 2 Read Data Byte 1	RO	00h
1Ah	CLK-GEN 2 Read Data Byte 2	RO	00h
1Bh	CLK-GEN 2 Read Data Byte 3	RO	00h
1Fh~2Ch	Reserved		0s
3Fh~30h	PM Bus (RFU)	R/W	0s
50h	IDT5V41068 Clock Select Control Register	R/W	0-h
Note : "**" means the value may be changed in the future FPGA FW update release.			

5.6.2 FPGA Configuration Registers Descriptions

Register Address: **SPI Base + 00h**
Register Name: **FPGA Device ID (Low Byte) Register**
Default Value: 04h
Attribute: Read Only

Bit	Description	Read/Write
7-0	**FPGA Device ID (Low Byte)** This offset 01h field combined with this field identifies the particular device. This identifier is allocated by the FPGA design team.	RO

Register Address: **SPI Base + 01h**
Register Name: **FPGA Device ID (High Byte) Register**
Default Value: 80h
Attribute: Read Only

Bit	Description	Read/Write
7-0	**FPGA Device ID (High Byte)** This field combined with the offset 00h field identifies the particular device. This identifier is allocated by the FPGA design team.	RO

Register Address: **SPI Base + 02h**
Register Name: **FPGA Revision ID (High Byte) Register**
Default Value: **
Attribute: Read Only

Bit	Description	Read/Write
7-0	**FPGA Revision ID (Low Byte)** This offset 03h register combined with this register specifies FPGA device specific revision identifier. The value may be changed in future FPGA FW update release.	RO

Register Address: **SPI Base + 03h**
Register Name: **FPGA Revision ID (Low Byte) Register**
Default Value: 00h*
Attribute: Read Only

Bit	Description	Read/Write
7-0	**FPGA Device ID (High Byte)** This register combined with the offset 02h register specifies FPGA device specific revision identifier. The value may be changed in the future FPGA FW update release.	RO

Register Address: **SPI Base + 04h**
Register Name: **BM GPI Status (07-00 Low Byte) Register**
Default Value: ------
Attribute: Read Only

Bit	Description	Read/Write
0	**BM GPIO 00:** This bit reflects the state of the BM general purpose input signal GPIO 00 and writes will have no effect. 0 : BM GPIO 00 state is low 1 : BM GPIO 00 state is high	RO
1	**BM GPIO 01:** This bit reflects the state of the BM general purpose input signal GPIO 01 and writes will have no effect. 0 : BM GPIO 01 state is low 1 : BM GPIO 01 state is high	RO
2	**BM GPIO 02:** This bit reflects the state of the BM general purpose input signal GPIO 02 and writes will have no effect. 0 : BM GPIO 02 state is low 1 : BM GPIO 02 state is high	RO
3	**BM GPIO 03:** This bit reflects the state of the BM general purpose input signal GPIO 03 and writes will have no effect. 0 : BM GPIO 03 state is low 1 : BM GPIO 03 state is high	RO
4	**BM GPIO 04:** This bit reflects the state of the BM general purpose input signal GPIO 04 and writes will have no effect. 0 : BM GPIO 04 state is low 1 : BM GPIO 04 state is high	RO
5	**BM GPIO 05:** This bit reflects the state of the BM general purpose input signal GPIO 05 and writes will have no effect. 0 : BM GPIO 05 state is low 1 : BM GPIO 05 state is high	RO
6	**BM GPIO 06:** This bit reflects the state of the BM general purpose input signal GPIO 06 and writes will have no effect. 0 : BM GPIO 06 state is low 1 : BM GPIO 06 state is high	RO

7	**BM GPIO 07:** This bit reflects the state of the BM general purpose input signal GPIO 07 and writes will have no effect. 0 : BM GPIO 07 state is low 1 : BM GPIO 07 state is high	RO

Register Address: **SPI Base + 05h**
Register Name: **BM GPI Status (15-08 High Byte) Register**
Default Value: ------
Attribute: Read Only

Bit	Description	Read/Write
0	**BM GPIO 08:** This bit reflects the state of the BM general purpose input signal GPIO 08 and writes will have no effect. 0 : BM GPIO 08 state is low 1 : BM GPIO 08 state is high	RO
1	**BM GPIO 09:** This bit reflects the state of the BM general purpose input signal GPIO 09 and writes will have no effect. 0 : BM GPIO 09 state is low 1 : BM GPIO 09 state is high	RO
2	**BM GPIO 10:** This bit reflects the state of the BM general purpose input signal GPIO 10 and writes will have no effect. 0 : BM GPIO 10 state is low 1 : BM GPIO 10 state is high	RO
3	**BM GPIO 11:** This bit reflects the state of the BM general purpose input signal GPIO 11 and writes will have no effect. 0 : BM GPIO 11 state is low 1 : BM GPIO 11 state is high	RO
4	**BM GPIO 12:** This bit reflects the state of the BM general purpose input signal GPIO 12 and writes will have no effect. 0 : BM GPIO 12 state is low 1 : BM GPIO 12 state is high	RO
5	**BM GPIO 13:** This bit reflects the state of the BM general purpose input signal GPIO 13 and writes will have no effect. 0 : BM GPIO 13 state is low 1 : BM GPIO 13 state is high	RO
6	**BM GPIO 14:** This bit reflects the state of the BM general purpose input signal GPIO 14 and writes will have no effect. 0 : BM GPIO 14 state is low 1 : BM GPIO 14 state is high	RO
7	**BM GPIO 15:** This bit reflects the state of the BM general purpose input signal GPIO 15 and writes will have no effect. 0 : BM GPIO 15 state is low 1 : BM GPIO 15 state is high	RO

Register Address: **SPI Base + 06h**
Register Name: **DSP GPI Status (07-00 Low Byte) Register**
Default Value: ------
Attribute: Read Only

Bit	Description	Read/Write
0	**DSP GPIO 00:** This bit reflects the state of the DSP general purpose input signal GPIO 00 and writes will have no effect. 0 : DSP GPIO 00 state is low 1 : DSP GPIO 00 state is high	RO
1	**DSP GPIO 01:** This bit reflects the state of the DSP general purpose input signal GPIO 01 and writes will have no effect. 0 : DSP GPIO 01 state is low 1 : DSP GPIO 01 state is high	RO
2	**DSP GPIO 02:** This bit reflects the state of the DSP general purpose input signal GPIO 02 and writes will have no effect. 0 : DSP GPIO 02 state is low 1 : DSP GPIO 02 state is high	RO
3	**DSP GPIO 03:** This bit reflects the state of the DSP general purpose input signal GPIO 03 and writes will have no effect. 0 : DSP GPIO 03 state is low 1 : DSP GPIO 03 state is high	RO
4	**DSP GPIO 04:** This bit reflects the state of the DSP general purpose input signal GPIO 04 and writes will have no effect. 0 : DSP GPIO 04 state is low 1 : DSP GPIO 04 state is high	RO
5	**DSP GPIO 05:** This bit reflects the state of the DSP general purpose input signal GPIO 05 and writes will have no effect. 0 : DSP GPIO 05 state is low 1 : DSP GPIO 05 state is high	RO
6	**DSP GPIO 06:** This bit reflects the state of the DSP general purpose input signal GPIO 06 and writes will have no effect. 0 : DSP GPIO 06 state is low 1 : DSP GPIO 06 state is high	RO
7	**DSP GPIO 07:** This bit reflects the state of the DSP general purpose input signal GPIO 07 and writes will have no effect. 0 : DSP GPIO 07 state is low 1 : DSP GPIO 07 state is high	RO

Register Address: **SPI Base + 07h**
Register Name: **DSP GPI Status (15-08 High Byte) Register**
Default Value: 00h
Attribute: Read Only

Bit	Description	Read/Write
0	**DSP GPIO 08:** This bit reflects the state of the DSP general purpose input signal GPIO 08 and writes will have no effect. 0 : DSP GPIO 08 state is low 1 : DSP GPIO 08 state is high	RO
1	**DSP GPIO 09:** This bit reflects the state of the DSP general purpose input signal GPIO 09 and writes will have no effect. 0 : DSP GPIO 09 state is low 1 : DSP GPIO 09 state is high	RO
2	**DSP GPIO 10:** This bit reflects the state of the DSP general purpose input signal GPIO 10 and writes will have no effect. 0 : DSP GPIO 10 state is low 1 : DSP GPIO 10 state is high	RO
3	**DSP GPIO 11:** This bit reflects the state of the DSP general purpose input signal GPIO 11 and writes will have no effect. 0 : DSP GPIO 11 state is low 1 : DSP GPIO 11 state is high	RO
4	**DSP GPIO 12:** This bit reflects the state of the DSP general purpose input signal GPIO 12 and writes will have no effect. 0 : DSP GPIO 12 state is low 1 : DSP GPIO 12 state is high	RO
5	**DSP GPIO 13:** This bit reflects the state of the DSP general purpose input signal GPIO 13 and writes will have no effect. 0 : DSP GPIO 13 state is low 1 : DSP GPIO 13 state is high	RO
6	**DSP GPIO 14:** This bit reflects the state of the DSP general purpose input signal GPIO 14 and writes will have no effect. 0 : DSP GPIO 14 state is low 1 : DSP GPIO 14 state is high	RO
7	**DSP GPIO 15:** This bit reflects the state of the DSP general purpose input signal GPIO 15 and writes will have no effect. 0 : DSP GPIO 15 state is low 1 : DSP GPIO 15 state is high	RO

Register Address: **SPI Base + 08h**
Register Name: **Debug LED Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
0	**DEBUG_LED 1:** This bit can be updated by the DSP software to drive a high or low value on the debug LED 1 pin. 0: DEBUG_LED 1 drives low and set the LED 1 to ON. 1: DEBUG_LED 1 drives high and set the LED 1 to OFF.	R/W
1	**DEBUG_LED 2:** This bit can be updated by the DSP software to drive a high or low value on the debug LED 2 pin. 0: DEBUG_LED 2 drives low and set the LED 2 to ON. 1: DEBUG_LED 2 drives high and set the LED 2 to OFF.	R/W
2	**DEBUG_LED 3:** This bit can be updated by the DSP software to drive a high or low value on the debug LED 3 pin 0: DEBUG_LED 3 drives low and set the LED 3 to ON. 1: DEBUG_LED 3 drives high and set the LED 3 to OFF.	R/W
3	**DEBUG_LED 4:** This bit can be updated by the DSP software to drive a high or low value on the debug LED 4 pin 0: DEBUG_LED 4 drives low and set the LED 4 to ON. 1: DEBUG_LED 4 drives high and set the LED 4 to OFF.	R/W
7-4	Reserved	R/W

Register Address: **SPI Base + 09h**
Register Name: **MMC Control Register**
Default Value: --------
Attribute: Read Only

Bit	Description	Read/Write
0	**MMC_DETECT#:** This bit reflects MMC DETECT state and it is used by MMC to indicate the AMC chassis insertion status. 0: State is low to indicate that EVM is inserted into the AMC chassis. 1: State is high to indicate that the EVM is not insterted	RO
1	**MMC_RSTSTAT#:** This bit reflects DSP RESETSTAT state and FPGA will drive the same logic value on the MMC_RSTSTAT# pin (to MMC). 0 : State is low and FPGA drives MMC_RSTSTAT# low to MMC 1 : State is high and FPGA drives MMC_RESETSTAT# high to MMC	RO
2	**MMC_POR_IN_AMC#:** This bit reflects MMC_POR_IN_AMC# state and it is used by the MMC to trigger a Power-On sequence & reset event. 0: State is low to trigger a Power-On sequence & reset event. 1: State is high and the FPGA stays in current state.	RO
3	**MMC_WR_AMC#:** This bit reflects MMC_WR_AMC# state and it is used by the MMC to trigger a warm reset event. 0: State is low to trigger a warm reset event. 1: State is high and the FPGA stays in current state	RO

4	**MMC_BOOTCOMP:** This bit reflects DSP BOOTCOMPLETE state and FPGA will drive the same logic value on the MMC_BOOTCOMP pin (to MMC). 0: State is low and FPGA drives MMC_ BOOTCOMP low to MMC 1: State is high and the FPGA drives MMC_ BOOTCOMP high to MMC	RO
7-5	**Reserved**	RO

Register Address: **SPI Base + 0Ah**
Register Name: **PHY Control Register**
Default Value: 03h
Attribute: Read/Write

Bit	Description	Read/Write
0	**PHY_INT#:** This bit reflects the PHY_INT# state. 0: PHY_INT# state is low. 1: PHY_INT# state is high.	RO
1	**PHY_RST:** This bit can be updated by the DSP software to drive a high or low value on the PHY_RST pin 0: PHY_RST drives low 1: PHY_RST drives high	R/W
7-2	**Reserved**	RO

Register Address: **SPI Base + 0Bh**
Register Name: **Reset Button Status Register**
Default Value: --------
Attribute: Read Only

Bit	Description	Read/Write
0	**FULL_RESET Button Status:** This bit reflects the FULL_RESET button state. This button is used to request a power full reset sequence to DSP. A logic Low to High transition on this button signal will complete the FPGA FULL_RESET sequence with a specified delay time. 0: FULL_RESET button state is low 1: FULL_RESET button state is high	RO
1	**WARM_RESET Button Status:** This bit reflects the WARM_RESET button state. This button is used to request a warm reset sequence to DSP. A logic Low to High transition on this button signal will complete the FPGA WARM_RESET sequence with a specified delay time. 0: WARM_RESET button state is low 1: WARM_RESET button state is high	RO
2	**COLD_RESET Button Status (RFU):** This bit reflects the COLD _RESET button state. Not used in current implementation. 0: COLD_RESET button state is low 1: COLD_RESET button state is high	RO
3	**FPGA_JTAG_RST#** 0: FPGA_JTAG_RST# state is low 1: FPGA_JTAG_RST# state is high	RO

4	**DSP_RESETSTAT#:** This bit reflects the DSP_RESETSTAT# state. 0: DSP_RESETSTAT# state is low 1: DSP_RESETSTAT# state is high	RO
5	**TRGRSTZ:** This bit reflects the TRGRSTZ state. 0: TRGRSTZ state is low 1: TRGRSTZ state is high	RO
6	**PCIESSEN:** This bit reflects the PCIESSEN switch state. 0 : PCIESSEN state is low 1 : PCIESSEN state is high	RO
7	**User_Defined Switch:** This bit reflects the User_Define Switch state. 0 : User_Defined Switch state is low 1 : User_Defined Switch state is high	RO

Register Address: **SPI Base + 0Ch**
Register Name: **Miscellaneous - 1 Register**
Default Value: 1Ch
Attribute: Read/Write

Bit	Description	Read/Write
1-0	**McBSP_AMC_EN#:** These bits can be updated by the DSP software to drive values on the McBSP_AMC_EN# pin and for selection of TCLK for McBSP 00: Drive McBSP_AMC_EN# low. Connect TCLKA to McBSP SLCLKs, TxCLKs & RxCLKs. Connect TCLKC to McBSP FSTs & FSRs. 01: Drive McBSP_AMC_EN# low. Connect TCLKB to McBSP SLCLKs, TxCLKs & RxCLKs. (RFU). Connect TCLKC to McBSP FSTs & FSRs. 10: Drive McBSP_AMC_EN# low. Connect TCLKD to McBSP SLCLKs, TxCLKs & RxCLKs. (RFU) Connect TCLKC to McBSP FSTs & FSRs. 11: Drive McBSP_AMC_EN# high. Output SLCLKs, TxCLKs, RxCLKs, FSTs, FSRs as (Hi Z)	R/W
2	**NAND_WP# :** This bit can be updated by the DSP software to drive a high or low value on the NAND_WP# pin 0 : NAND_WP# drives low 1 : NAND_WP# drives high	R/W
3	**XDS560_IL control** 0 : Disable XDS560 mezzanine card 1 : Enable XDS560 mezzanine card (Default)	R/W
4	**NOR_WP# :** This bit can be updated by the DSP software to drive a high or low value on the NOR_WP# pin 0 : NOR_WP# drives low 1 : NOR_WP# drives high	R/W
5	**EEPROM_WP:** This bit can be updated by the DSP software to drive a high or low value on the EEPROM_WP pin 0 : EEPROM_WP drives low 1 : EEPROM_WP drives high	R/W

6	**PCA9306_EN:** This bit can be updated by the DSP software to drive a high or low value on the PCA9306_EN pin (RFU) 0 : PCA9306_EN drives low (Default) 1 : PCA9306_EN drives high	R/W
7	**Reserved**	RO

Register Address: **SPI Base + 0Dh**
Register Name: **Miscellaneous - 1 Register**
Default Value: --------
Attribute: Read Only

Bit	Description	Read/Write
0	**FPGA FW Update SPI Interface Enable Status:** This bit reflects the FPGA FW Update SPI Interface Enable status. The FPGA FW Update SPI interface can be enabled/disabled through the offset 0Eh register. 0: FPGA FW update SPI interface is disabled. 1: FPGA FW update SPI interface is enabled. DSP_GPIO[12] is mapped to FPGA_FW_SPI_CLK. DSP_GPIO[13] is mapped to FPGA_FW_SPI_CS#. DSP_GPIO[14] is mapped to FPGA_FW_SPI_MOSI. DSP_GPIO[15] is mapped to FPGA_FW_SPI_MISO.	RO
1		
2	**DSP_HOUT Status:** This bit reflects the DSP_HOUT signal state. 0 : DSP_HOUT state is low 1 : DSP_HOUT state is high	RO
3	**DSP_SYSCLKOUT Status:** This bit reflects the DSP_SYSCLKOUT signal state. 0 : DSP_SYSCLKOUT state is low 1 : DSP_SYSCLKOUT state is high	RO
7-4	**Reserved**	RO

Register Address: **SPI Base + EDh**
Register Name: **FPGA FW Update SPI Interface Control Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	**FPGA FW Update SPI Interface Enable Control:** These bits are used to enable/disable the FPGA FW Update SPI Interface. If the value of this register be set to 68h, the FPGA FW Update SPI interface would be enabled. All the other values set to this register would disable the FPGA FW Update SPI interface. 68h: FPGA FW update SPI interface is enabled. Others: FPGA FW update SPI interface is disabled. DSP_GPIO[12] is mapped to FPGA_FW_SPI_CLK. DSP_GPIO[13] is mapped to FPGA_FW_SPI_CS#. DSP_GPIO[14] is mapped to FPGA_FW_SPI_MOSI. DSP_GPIO[15] is mapped to FPGA_FW_SPI_MISO.	R/W

Register Address: **SPI Base + 0Fh**
Register Name: **Scratch Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	**Scratch Data**	R/W

Register Address: **SPI Base + 10h**
Register Name: **CLK-GEN 2 Control Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
0	**Initiate** a data transfer via the SPI bus to update the SPI command to CDCE62005 Clock Generator#2 0: Idle state 1: Write 1 to perform the SPI command update process.	R/W
1	**BUSY** status indication for the CDCE62005 Clock Generator#2 SPI bus 0: The SPI bus for the CDCE62005 Clock Generator #2 is idle. 1: The SPI bus for the CDCE62005 Clock Generator #2 is busy and a SPI command is processing.	RO
7-2	**Reserved**	RO

Register Address: **SPI Base + 11h**
Register Name: **CLK-GEN 2 Interface Setting Register**
Default Value: 03h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register is a clock divider setting to adjust the interface clock for the CDCE62005 Clock Generator #2 SPI bus. 00 : CDCE62005 2 SPI Clock = 12MHz (= 48 / 4) 01 : CDCE62005 2 SPI Clock = 12MHz (= 48 / 4) 02 : CDCE62005 2 SPI Clock = 8 MHz (= 48 / 6) 03 : CDCE62005 2 SPI Clock = 6 MHz (= 48 / 8) 04 : CDCE62005 2 SPI Clock = 4.8 MHz (= 48 /10) 05 : CDCE62005 2 SPI Clock = 4 MHz (= 48 /12) 06 : CDCE62005 2 SPI Clock = 3.42 MHz (= 48 / 14) …… X : CDCE62005 2 SPI Clock = 48 MHz /((X+1)*2) if X != 0	R/W

Register Address: **SPI Base + 12~13h**
Register Name: **Reserved**
Default Value: 00h
Attribute: Read/Write

Register Address: **SPI Base + 14h**
Register Name: **CLK-GEN 2 Command Byte 0 Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 0 to the CDCE62005 Clock Generator #2 3-0 : SPI command address field bit 3 to bit 0 7-4 : SPI command data field bit 3 to bit 0	R/W

Register Address: **SPI Base + 15h**
Register Name: **CLK-GEN 2 Command Byte 1 Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 1 to the CDCE62005 Clock Generator #2 7-0 : SPI command data field bit 11 to bit 4	R/W

Register Address: **SPI Base + 16h**
Register Name: **CLK-GEN 2 Command Byte 2 Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 2 to the CDCE62005 Clock Generator #2 7-0 : SPI command data field bit 19 to bit12	R/W

Register Address: **SPI Base + 17h**
Register Name: **CLK-GEN 2 Command Byte 3 Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register specifies the update SPI command byte 3 to the CDCE62005 Clock Generator #2 7-0 : SPI command data field bit 27 to bit 20	R/W

Register Address: **SPI Base + 18h**
Register Name: **CLK-GEN 2 Read Data Byte 0 Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 0 from the CDCE62005 Clock Generator #2 for responding a host SPI Read Command. 7-0: The SPI read back data bit 7 to bit 0 for a SPI Read Command.	RO

Register Address: **SPI Base + 19h**
Register Name: **CLK-GEN 2 Read Data Byte 1 Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 1 from the CDCE62005 Clock Generator #2 for responding a host SPI Read Command. 7-0: The SPI read back data bit 15 to bit 8 for a SPI Read Command.	RO

Register Address: **SPI Base + 1Ah**
Register Name: **CLK-GEN 2 Read Data Byte 2 Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 0 from the CDCE62005 Clock Generator #2 for responding a host SPI Read Command. 7-0: The SPI read back data bit 23 to bit 16 for a SPI Read Command.	RO

Register Address: **SPI Base + 1Bh**
Register Name: **CLK-GEN 2 Read Data Byte 3 Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	This register reflects the read back data byte 0 from the CDCE62005 Clock Generator #2 for responding a host SPI Read Command. 3-0: The SPI read back data bit 27 to bit 24 for a SPI Read Command. 7-4: Reserved.	RO

Register Address: **SPI Base + 1Ch ~ 2Fh**
Register Name: **Reserved**

Register Address: **SPI Base + 30h ~ 3Fh**
Register Name: **PM Bus Control Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	**TBD**	R/W

Register Address: **SPI Base + 40h ~ 4Fh**
Register Name: **Reserved**

Register Address: **SPI Base + 50h**
Register Name: **CLK-MUX Selection Control Register**
Default Value: 00h
Attribute: Read/Write

Bit	Description	Read/Write
7-0	**CLK_MUX_SEL:** This bit can be updated by the DSP software to drive a high or low value on the CLK_MUX_SEL pin. The default value of this bit is over-ridden when PCIe boot mode is selected by SW5.3 (BM_GPIO_10). 0 : CLK_MUX_SEL drives low 1 : CLK_MUX_SEL drives high	R/W
7-1	**Reserved**	RO

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