# 82540EP/82541(PI/GI/EI) & 82562EZ(EX) Layout Checklist v1.1

| | |
|---|---|
| **Project Name** | |
| **Fab Revision** | |
| **Date** | |
| **Designer** | |
| **Intel Contact** | |
| **Reviewer** | |

| SECTION | CHECK ITEMS | REMARKS | √ DONE | COMMENTS |
|---|---|---|---|---|
| **General** | Have up-to-date product documentation and spec updates | Documents are subject to frequent change | | |
| | Route the transmit and receive differential traces before routing the digital traces. | Layout of differential traces is critical. | | |
| **Ethernet Device** | Place the Ethernet silicon at least one inch from the edge of the board and at least one inch from any integrated magnetics module. | With closer spacing, fields can follow the surface of the magnetics module or wrap past edge of board. EMI may increase. Optimum location is approximately one inch behind the magnetics module. | | |
| | For the 82562EZ(EX) LCI device, the trace impedance for the LCI port is 60 Ω. | | | |
| | For the 82562EZ(EX) LCI device, place the transmit LCI termination carefully. | For the 82562EZ(EX) LCI device, place the transmit LCI termination close to ICH, and place the receive LCI termination close to the 82562EZ(EX) silicon. | | |
| **Clock Source** | Place crystal and load capacitors within 0.75 inches from Ethernet device. | The Ethernet clock plays a key role in EMI. | | |
| **EEPROM and FLASH Memory** | Placement is not critical due to slow signal speeds. | Okay to place a few inches away from Ethernet controller or ICH to provide better spacing of critical components. | | |

| SECTION | CHECK ITEMS | REMARKS | √ DONE | COMMENTS |
|---|---|---|---|---|
| **Transmit and Receive Differential Pairs** | Design traces for 100 Ω differential impedance (±15%). | Primary requirement for 10/100/1000 Mbps Ethernet. Paired 49.9 Ω traces do not make 100 Ω differential. Check impedance calculator. | | |
| | Use short traces. | Keep trace length under four inches from the Ethernet controller through the magnetics to the RJ-45 connector. | | |
| | Avoid highly resistive traces, for example, four mil traces longer than four inches. | If trace length is a problem, use thicker board dielectrics to allow wider traces. Thicker copper is even better than wider traces. | | |
| | Make traces symmetrical. | Try to match the pairs at pads, vias and turns. Establish rules carefully for the autorouter. Asymmetry contributes to impedance mismatch. | | |
| | Do not make 90 degree bends. | Bevel corners with turns based on 45 degree angles. | | |
| | Avoid through holes (vias). | If using through holes (vias), the budget is two per trace. | | |
| | Keep traces close together within differential pairs. | Keep within 30 mils regardless of trace geometry. | | |
| | Keep trace-to-trace length difference within each pair to less than 50 mils. | Minimizes signal skew and common mode noise. Improves long cable performance. | | |
| | Keep differential pairs 100 mils or more away from each other and away from parallel digital traces. | Minimizes crosstalk and noise injection. 300 mil spacing is better. Guard traces are generally not recommended and will reduce the impedance if done incorrectly. | | |
| | Keep traces away from the board edge. | Controls EMI. | | |
| | Avoid unused pads and stubs along the traces | Use 0 Ω resistors sparingly for dual footprint designs. | | |
| | Route traces on layers on appropriate layers. | Run pairs on different layers as needed to improve routing. Use layers adjacent to ground or power layers if possible. Make sure digital signals on adjacent layers cross at 90 degree angles. | | |
| | Place termination resistors (and capacitors if applicable) close to Ethernet device. | Prevents reflections. Use symmetrical pads. | | |

| SECTION | CHECK ITEMS | REMARKS | √ DONE | COMMENTS |
|---|---|---|---|---|
| **Magnetics Module** | Capacitors connected to center taps should be placed very close to magnetics module. | | | |
| **Power Supply and Signal Ground** | When using the internal regulator control circuits of the 82540EP/82541xx controller with external PNP transistors, keep the distance from the CTRL12/CTRL15/ CTRL18 output balls to the transistors very short (less than 1 inch) and use 25 mil (minimum) wide traces. | Reduces oscillation and ripple in the power supply. | | |
| | Use of power planes is essential for optimized performance of the controller | Narrow finger-like planes and very wide traces are not recommended and a continuous plane should be used. | | |
| | Use decoupling and bulk capacitors generously. | Place decoupling and bulk capacitors close to Ethernet device, with some along every side, using short, wide traces and large vias. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector. | | |
| | If using decoupling capacitors on LED lines, place them carefully. | Capacitors on LED lines should be placed near the LEDs. | | |
| | Use a wide ground plane under the area covering the controller, the external transistors (for both 1.2 V and 1.8 V generation) and the filter capacitors. | | | |
| | Bypass the emitter and collector of the external PNP transistors as closely as possible to the body of the transistors. | | | |
| | The bypass capacitor at the emitter should be at least 4.7 µF (preferably 10 to 20 µF). | Ceramic X5R or X7R type capacitors should be placed as closely as possible to the body of the transistors. | | |
| | The larger capacitors should be concentrated near the transistor. | Do not disperse the large capacitors in a large area as this can cause instability to the circuit. | | |
| | The high frequency bypass capacitors (0.1 µF X7R capacitors) for the device should be placed as closely as possible to the corresponding balls. | | | |
| | Trace lengths should have around eight mils of width. | | | |

| SECTION | CHECK ITEMS | REMARKS | √ DONE | COMMENTS |
|---|---|---|---|---|
| **Chassis Ground** | If possible, provide a separate chassis ground "island" to ground the shroud of the RJ-45 connector and to terminate the line side of the magnetics module. This design improves EMI behavior. | Split in ground plane should be at least 50 mils. Split should run under center of magnetics module. Differential pairs never cross the split. | | |
| | Place four to six pairs of pads for "stitching" capacitors to bridge the gap from chassis ground to signal ground. | Determine exact number and values empirically based on EMI performance. For 82562EZ(EX) or 82541xx devices, expect to populate approximately two capacitor sites. | | |
| **Termination Plane** | For designs with non-integrated magnetics modules, lay out Bob Smith termination plane. Term plane floats over chassis ground. | Splits in ground plane should be at least 50 mils. | | |
| **LED Circuits** | Keep LED traces away from sources of noise, for example, high speed digital traces running in parallel. | LED traces can carry noise into integrated magnetics modules, RJ-45 connectors, or out to the edge of the board, increasing EMI. | | |