ATI RADEON E4690 (M96-CSP512) Databook

Technical Reference Manual
Rev 3.00

P/N: 46815_e4690_ds_nda

Advanced Micro Devices, Inc., will not provide any indemnity, pay any royalty, nor provide any license/sublicense to any:

(a) Intellectual property rights relating to any of the following: (i) Advanced Television Systems Committee (ATSC) standard and related technologies; or (ii) the High Definition Multimedia Interface (HDMI) standard and related technologies; or

(b) Audio and/or video codecs or any industry standard technology (e.g., technology or specifications promulgated by any standards development organization, consortium, trade association, special interest group or like entity) .

Trademarks

AMD, the AMD Arrow logo, Athlon, and combinations thereof, ATI, ATI logo, and Radeon are trademarks of Advanced Micro Devices, Inc.

HyperTransport is a licensed trademark of the HyperTransport Technology Consortium.

Microsoft and Windows are registered trademarks of Microsoft Corporation.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.

Disclaimer

The contents of this document are provided in connection with Advanced Micro Devices, Inc. ("AMD") products. AMD makes no representations or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to make changes to specifications and product descriptions at any time without notice. No license, whether express, implied, arising by estoppel, or otherwise, to any intellectual property rights are granted by this publication. Except as set forth in AMD's Standard Terms and Conditions of Sale, AMD assumes no liability whatsoever, and disclaims any express or implied warranty, relating to its products including, but not limited to, the implied warranty of merchantability, fitness for a particular purpose, or infringement of any intellectual property right.

AMD's products are not designed, intended, authorized or warranted for use as components in systems intended for surgical implant into the body, or in other applications intended to support or sustain life, or in any other application in which the failure of AMD's product could create a situation where personal injury, death, or severe property or environmental damage may occur. AMD reserves the right to discontinue or make changes to its products at any time without notice.

Table of Contents

Chapter 1: Introduction

1.1 Introducing ATI RADEON E4690 1-1
1.2 Part Identification 1-2
1.2.1 Packaging Types and Device Ids 1-2
1.2.2 Branded Part Number Interpretation 1-2
1.2.3 Branding Format 1-3

Chapter 2: Functional Overview

2.1 Acceleration Features 2-2
2.2 AvivoTM Display System 2-3
2.2.1 Display Features 2-3
2.2.2 DVI/HDMI/DisplayPort Features 2-3
2.2.3 LVDS 2-5
2.2.4 Dual Analog Output Features 2-6
2.2.5 DVO Interface 2-6
2.3 Motion Video Acceleration Features 2-6
2.4 Bus Support Features 2-7
2.5 Power Management Features 2-7
2.6 Spread Spectrum Support 2-7
2.6.1 LVDS Spread Spectrum Support 2-7
2.6.2 Engine and Memory Spread Spectrum Support 2-7
2.6.3 DisplayPort Internal Spread Spectrum Support 2-8
2.7 Internal Thermal Sensor 2-8
2.8 Thermal Diode 2-8
2.9 PC Design Guide Compliance 2-8
2.10 Test Capability Features 2-8
2.11 Other Features 2-8
2.12 Compliance with US Commerce Department Control List ECCN 4A994 2-8

Chapter 3: Signal Descriptions

3.1 E4690 Pin Assignment 3-2
3.1.1 E4690 Pin Assignment 3-2
3.2 PCI Express Bus Interface 3-4
3.3 Memory Interface (SGRAM, SDRAM) 3-5
3.4 Display Configurations Overview 3-6
3.5 Integrated HDMI / TMDS Interface 3-6
3.5.1 Integrated HDMI / TMDS Configurations 3-7

3.6 DisplayPort Interface ... 3-7
3.7 LVDS/TMDS2 Interface ... 3-8
3.7.1 LVDS Interface Signal Mapping ... 3-8
3.7.2 TMDS2 Signal Mapping ... 3-10
3.8 External TMDS Interface. ... 3-12
3.8.1 12-Bit DDR External TMDS ... 3-12
3.8.2 24-Bit DDR External TMDS ... 3-13
3.9 CrossFire Interface ... 3-14
3.10 Hardware I2C Interface ... 3-15
3.11 Serial Flash Interface ... 3-15
3.12 General Purpose I/O Interface ... 3-16
3.13 Panel Control Interface ... 3-18
3.14 DAC1 (CRT) Interface ... 3-18
3.15 DAC2 (TV) Interface ... 3-19
3.16 Display Identification Interface ... 3-22
3.17 Test/JTAG/Debug Port ... 3-24
3.18 Thermal Information & Management Interface ... 3-24
3.19 External Spread Spectrum Interface (Optional) ... 3-25
3.20 PLLs and Crystal Interface ... 3-26
3.21 POWERPLAY Interface ... 3-26
3.22 Power and Ground Descriptions and Operating Conditions ... 3-27
3.23 Configuration Straps ... 3-29
3.23.1 Pin Based Straps ... 3-29
3.23.2 ROM Based Straps for Add-in Card Design ... 3-32
3.23.3 Readback of Strap Settings ... 3-32

Chapter 4: Timing Specifications

4.1 I^2C Timing ... 4-2
4.1.1 Write Cycle ... 4-2
4.1.2 Read Cycle ... 4-2
4.2 Initialization Sequence and Timing ... 4-4
4.2.1 Standard Boot-up Sequence ... 4-5
4.3 Serial Flash Read/Write Timing ... 4-6
4.4 LCD Panel Power Up/Down Timing ... 4-7
4.5 LCD Panel Backlight Control with PWM ... 4-8
4.6 DVO Timing ... 4-9
4.6.1 12-bit DDR ... 4-9
4.6.2 24-bit SDR ... 4-10
4.6.3 24-bit DDR ... 4-11

Chapter 5: Electrical Characteristics

5.1 Maximum Rating Conditions ... 5-2
5.2 Electrical Design Power ... 5-3
5.3 Power Up/Down Sequence ... 5-4

5.3.1 General Guidelines 5-4
5.3.2 PowerPlay Transitions 5-4
5.4 General Interface 5-5
5.5 TTL Interface 5-5
5.6 Memory Interface 5-6
5.7 DDC I2C Mode Electrical Characteristics 5-6
5.8 DisplayPort AUX Electrical Specification 5-7
5.9 DisplayPort Main Link Electrical Specification 5-7
5.10 DAC Characteristics 5-8
5.10.1 Calculating RSET (CRT DAC Interface) 5-8
5.10.2 Analog Video Levels 5-10

Chapter 6: Thermal Data

6.1 Thermal Equations 6-1
6.2 Thermal Design Power (TDP) 6-1
6.2.1 TDP for E4690 Discrete Variants 6-1
6.3 Thermal Diode Characteristics 6-1

Chapter 7: Mechanical Data

7.1 E4690 Physical Dimensions 7-2
7.2 Pressure Specification 7-5
7.3 Board Solder Reflow Process Recommendations 7-5
7.3.1 Stencil Opening Size for Solderball Pads on PCB 7-5
7.3.2 FCBGA/PBGA Reference Reflow Profile for RoHS/Lead-free Solder 7-6

Chapter 8: Boundary Scan Specification

8.1 Introduction 8-1
8.2 Boundary Scan 8-1
8.3 JTAG Interface Signals 8-1
8.3.1 JTAG Interface 8-1
8.3.2 JTAG Timing Characteristics 8-1
8.4 Boundary Scan Thermal Issues 8-2

Appendix A: Pin Listings

A.1 E4690 Pins Sorted by Ball Reference A-2
A.2 E4690 Pins Sorted by Signal Name A-10

Appendix B: Pin Assignment Diagrams in Black and White

B.1 E4690 Pin Assignment B-1

Appendix C: Revision History

List of Figures

Figure 1-1: Product Branded Part Number Interpretation 1-2
Figure 1-2: E4690 Branding Format 1-3
Figure 2-1: E4690 Display Top-Level Data Flow Diagram 2-3
Figure 3-1: E4690 Pin Assignment - Left Half 3-2
Figure 3-2: E4690 Pin Assignment - Right Half 3-3
Figure 3-3: Crossfire: Master/Slave 2 GPU configuration 3-15
Figure 3-4: Implementation of Board Level Buffers 3-31
Figure 4-1: I^2C Write Cycle 4-2
Figure 4-2: I^2C Read Cycle 4-2
Figure 4-3: E4690 Power-On Reset Sequence 4-4
Figure 4-4: Serial flash write/read timings 4-6
Figure 4-5: LCD Panel Power Up/Down Timing 4-7
Figure 4-6: Backlight PWM Parameters 4-8
Figure 4-7: 12-bit DDR Interface Timing 4-9
Figure 4-8: 24-bit SDR Timing 4-10
Figure 4-9: 24-bit DDR Timing 4-11
Figure 5-1: Ideal Power Up/Down Sequence 5-4
Figure 5-2: Double Termination 5-9
Figure 5-3: Analog Output (DAC) 5-10
Figure 5-4: PS/2 Video Levels 5-10
Figure 5-5: NTSC Video Levels 5-10
Figure 5-6: PAL Video Levels 5-11
Figure 7-1: E4690 Package Outline - Bottom View 7-2
Figure 7-2: E4690 Package Outline - Top View 7-3
Figure 7-3: E4690 Ball Arrangement 7-4
Figure 7-4: FCBGA/PBGA Reference Reflow Profile for RoHS/Lead-Free SMT 7-6
Figure 8-1: Timing of the Boundary Scan Signals with Respect to TCK 8-2
Figure 8-2: Timing of the TAP ports (TDI, TMS, and TDO) with Respect to TCK 8-2
Figure B-1: E4690 Pin Assignment - Left Half B-1
Figure B-2: E4690 Pin Assignment - Right Half B-2

List of Tables

Table 1-1: E4690 Package Information 1-2
Table 2-1: Maximum pixel rates for 4, 2, or 1 lanes at 2.7-GHz link rate 2-4
Table 2-2: HDMI Features 2-4
Table 3-1: PCI Express Bus Interface 3-4
Table 3-2: Memory Interface 3-5
Table 3-3: Display Configurations Overview for Link A, B, C, and D 3-6
Table 3-4: Display Configurations Overview for Link E and F 3-6
Table 3-5: Integrated HDMI / TMDS Interface 3-6
Table 3-6: E4690 Integrated HDMI / TMDS Configurations 3-7
Table 3-7: DisplayPort Interface 3-7
Table 3-8: LVDS/TMDS2 Interface 3-8
Table 3-9: Single-Link LVDS Mode -- Signal Mapping 3-8
Table 3-10: Dual-Link LVDS Mode -- Signal Mapping 3-9
Table 3-11: TMDS2 Signal Mapping for Single and Dual Link 3-10
Table 3-12: External TMDS Interface 3-12
Table 3-13: 12-Bit DDR External TMDS Signal Mapping 3-12
Table 3-14: 24-Bit DDR External TMDS Signal Mapping 3-13
Table 3-15: Crossfire Interface 3-14
Table 3-16: Hardware I2C Interface * 3-15
Table 3-17: Serial Flash Interface 3-15
Table 3-18: General Purpose I/O Interface 3-16
Table 3-19: Panel Control Interface 3-18
Table 3-20: DAC1 (CRT) Interface 3-18
Table 3-21: DAC2 (TV) Interface 3-19
Table 3-22: Display Identification Interface 3-22
Table 3-23: Test/JTAG Interface 3-24
Table 3-24: Debug Port 3-24
Table 3-25: Thermal Interface Signals 3-24
Table 3-26: External Spread Spectrum Interface 3-25
Table 3-27: PLL and Crystal Interface 3-26
Table 3-28: POWERPLAY Interface 3-26
Table 3-29: Power and Ground Descriptions and Operating Conditions 3-27
Table 3-30: Pin Based Straps 3-29
Table 3-31: ROM Configurations 3-30
Table 3-32: Primary Memory Aperture size requested at PCI Configuration 3-31
Table 3-33: ROM Based Straps 3-32
Table 3-34: Configuration registers initialized by straps 3-32
Table 3-35: Strap values that can be read back directly 3-32
Table 4-1: I^2C Write Cycle Timing Parameters 4-2
Table 4-2: I^2C Read Cycle Timing Parameters 4-3
Table 4-3: E4690 Power-On Reset Sequence Timing Parameters 4-4
Table 4-4: Serial Flash Write/Read Timing Parameters for Bootup case SCLK=100 MHz, XTALIN=27 MHz, ROM_CNTL.SCK_PRESCALE_CRYSTAL_CLK=0x1 4-6

Table 4-5: LCD Power Up/Down Timing 4-7
Table 4-6: Registers for Setting Backlight PWM Parameters 4-8
Table 4-7: Backlight PWM Parameters 4-8
Table 4-8: 12-bit DDR Interface Timing 4-9
Table 4-9: 24-bit SDR Timing 4-10
Table 4-10: 24-bit DDR Timing 4-11
Table 5-1: Maximum Rating Conditions 5-2
Table 5-2: Regulator Guidance 5-3
Table 5-3: General Interface Electrical Characteristics 5-5
Table 5-4: TTL Interface (GPIOs) for GPIO, and DVP signals 5-5
Table 5-5: TTL Interface (GPIOs) for SDA, and SCL 5-5
Table 5-6: Memory Interface Electrical Characteristics 5-6
Table 5-7: Transmitter Electrical Specification for DDC I2C 5-6
Table 5-8: Receiver Electrical Specification for the DDC I2C pins 5-6
Table 5-9: DisplayPort AUX Electrical Specification 5-7
Table 5-10: DisplayPort Main Link Electrical Specification 5-7
Table 5-11: DAC Characteristics 5-8
Table 5-12: CRT DAC (DAC1) Electrical Parameters 5-9
Table 5-13: DAC (DAC2) Electrical Parameters 5-9
Table 6-1: TDP for E4690 Discrete Variants 6-1
Table 6-2: E4690 Thermal Diode Characteristics 6-2
Table 7-1: E4690 Physical Dimensions (mm) 7-3
Table 7-2: Recommended Profiling - RoHS/Lead-Free Solder 7-6
Table 8-1: JTAG Pins 8-1
Table 8-2: JTAG Timing Characteristics Table 8-1
Table A-1: E4690 Pins Sorted by Ball Reference A-2
Table A-2: E4690 Pins Sorted by Signal Name A-10

Chapter 1
Introduction

1.1 Introducing ATI RADEON E4690

TheATI RADEON E4690 is designed for the performance embedded system and provides the most advanced and best-in-class graphics performance.

The ATI RADEON E4690 supports PCI Express Revision 2.0, DirectX 10.1 with Shader Model 4.1, VESA DisplayPort technologies, integrated HDMI and HDCP keys, and a Unified Video Decoder 2.0 (UVD 2.0) that supports HD-DVD and Blu-Ray decode (H.264, VC-1 and MPEG 2 formats).

The Databook is updated as necessary following qualification to convert this document to a formal specification.

Please review any Errata Advisories as they identify amendments to the specifications in this databook.

Contact your CSS for the software support schedules of ASIC features.

1.2 Part Identification

1.2.1 Packaging Types and Device Ids

The vendor ID is 0x1002.

Table 1-1 E4690 Package Information

Part	Device ID	HD Audio Controller	HD Audio Codec	Package
E4690	9491	AA38	AA01	1066 FCBGA

The figure below shows how to read the coded information contained in the branded component part number.

1.2.2 Branded Part Number Interpretation

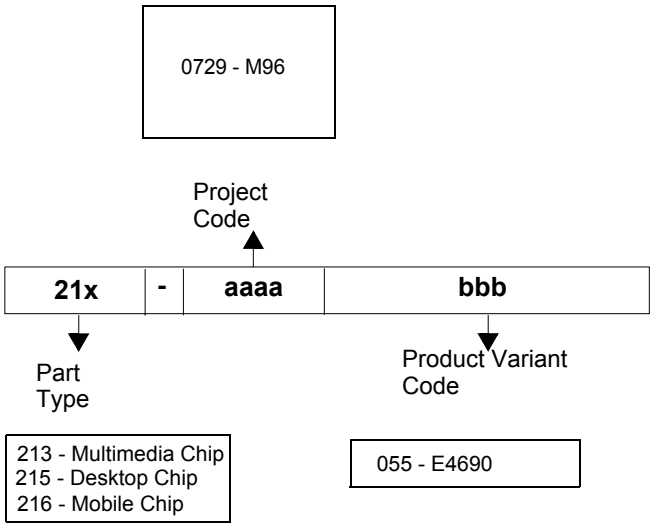


Figure 1-1 Product Branded Part Number Interpretation

1.2.3 Branding Format

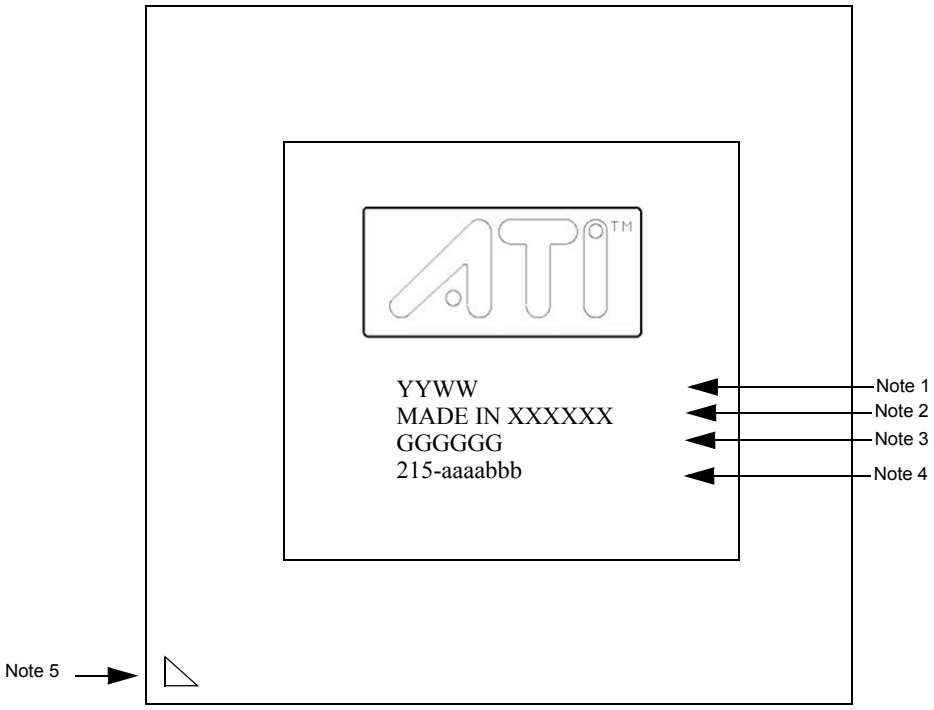


Figure 1-2 E4690 Branding Format

Notes:

1 The date code where YY-assembly start year, WW-assembly start week.

2 Country of origin XXXXXX (Assembly site - USA, SINGAPORE, TAIWAN etc.)

3 GGGGGG-This is wafer foundry's lot number.

4 Part number. (Refer to *Figure 1-2* for part number interpretation.)

5 ASIC pin A1.

Chapter 2
Functional Overview

This chapter describes the major subsystems and interfaces of the E4690. To go to a topic of interest, use the following list of linked cross references:

"Acceleration Features" on page 2-2
"AvivoTM Display System" on page 2-3
"Motion Video Acceleration Features" on page 2-6.
"Bus Support Features" on page 2-7
"Power Management Features" on page 2-7.
"Spread Spectrum Support" on page 2-7
"Internal Thermal Sensor" on page 2-8.
"Thermal Diode" on page 2-8
"PC Design Guide Compliance" on page 2-8.
"Test Capability Features" on page 2-8
"Other Features" on page 2-8.
"Compliance with US Commerce Department Control List ECCN 4A994" on page 2-8

2.1 Acceleration Features

- Fully DirectX 10.1 compliant, including full speed 32-bit floating point per component operations
  - Shader Model 4.0 geometry and pixel support in a unified shader architecture:
    - 32- and 64-bit floating point processing per component.
    - High performance dynamic branching and flow control.
    - Nearly unlimited shader instruction store, using an advance caching system.
    - Advanced shader design, with ultra-threading sequencer for high efficiency operations.
    - Advanced, high performance branching support, including static and dynamic branching.
    - High dynamic range rendering with floating point blending, texture filtering and anti-aliasing support.
    - 16- and 32-bit floating point components for high dynamic range computations.
    - Full anti-aliasing on render surfaces up to and including 128-bit floating point formats.
- Support for OpenGL® 3.0.
- Anti-Aliasing Filtering:
  - 2x/4x/8x modes.
  - Multi-sample algorithm with gamma correction, programmable sample patterns, and centroid sampling.
  - Temporal anti-aliasing.
  - Adaptive anti-aliasing mode.
  - Lossless color compression (up to 8:1) at all resolutions, up to and including widescreen HDTV.
- Anisotropic Filtering:
  - 2x/4x/8x/16x modes
  - Up to 128-tap texture filtering.
  - Anisotropic biasing to allow trading quality for performance.
  - Improved quality mode due to improved subpixel precision and higher precision LOD computations.
  - Advanced Texture Compression (3Dc+™):
  - High quality 4:1 compression for normal maps and luminance maps.
  - Works with any single- or two-channel data format.
- Hardware support to overcome "Small batch" issues in CPU limited applications.
- 3D resources virtualized to a 36-b addressing space, for support of large numbers of render targets and textures.
- New vertex cache and vertex fetch design, to increase vertex throughput from previous generations.
- Up to 8k x 8k textures, including 128-b/pixel texture are supported.
- New multi-level texture cache to give optimal performance.
- High efficiency memory controller:
  - Programmable arbitration logic maximizes memory efficiency, software upgradeable.
  - Fully associative texture, color, and Z cache design.
  - Hierarchical Z & Stencil buffers with Early Z Test.
  - Lossless Z-buffer compression for both Z and Stencil.
  - Fast Z-Buffer Clear.
  - Z cache optimized for real-time shadow rendering.
  - Z and color compression resources virtualized to a 32-bit addressing space, for support of multiple render targets and textures simultaneously.

2.2 Avivo™ Display System

The Avivo™ display system supports VGA, VESA super VGA, and accelerator mode graphics display on two independent display controllers.

The full features of the Avivo™ display system are outlined in the following sections.

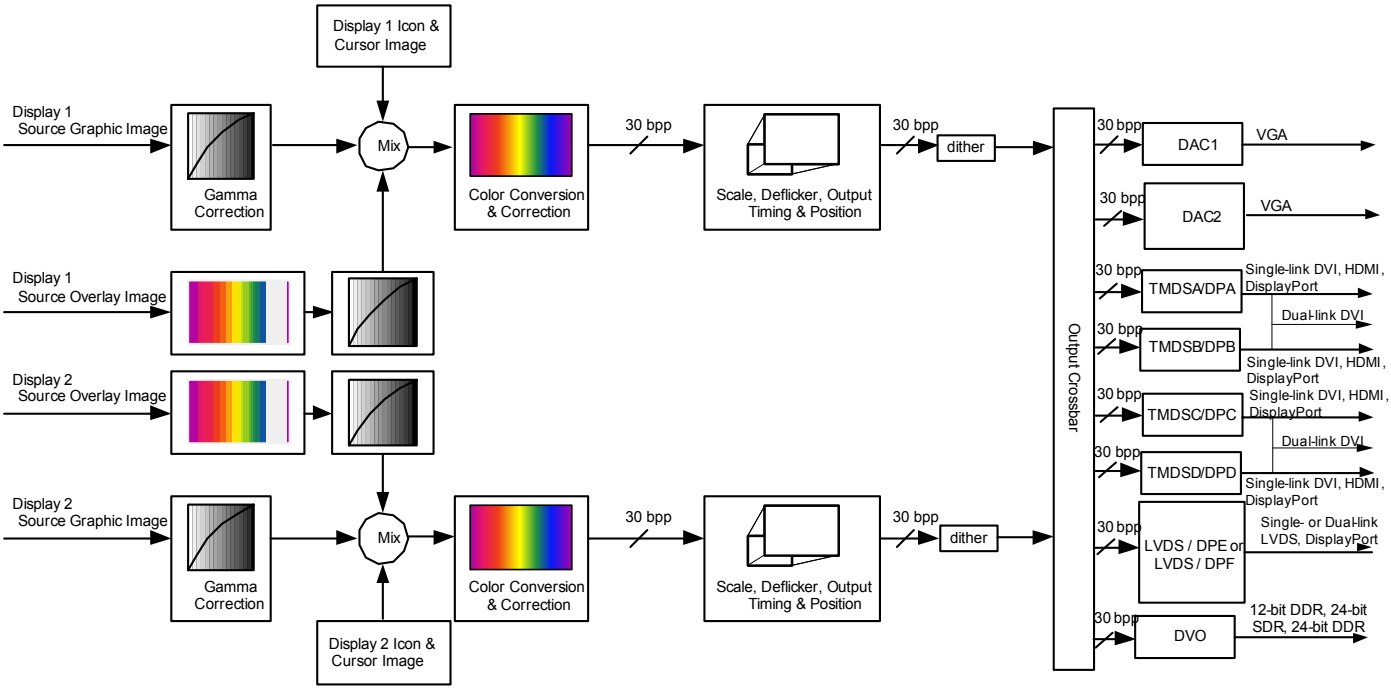


Figure 2-1 E4690 Display Top-Level Data Flow Diagram

2.2.1 Display Features

- Dual independent display controllers that support true 30-bpp throughout the display pipe.
- Full feature symmetry in both controllers.
- Support for display resolutions up to 3840x2400 per display output, which does not oversubscribe available memory bandwidth.
- Flexible support for various combinations of display outputs. Please contact your AMD CSS representative.
- Advanced video capabilities, including high fidelity gamma, color correction and scaling.
- Adaptive per-pixel de-interlacing and frame rate conversion (temporal filtering).
- Enhanced dithering algorithm for LCD panels.
- Full RMX for sources up to 2560 pixels/line.
- YPrPb component output for direct drive of HDTV displays.
- HDCP can be supported on two independent displays (e.g. HDMI, DVI, or DP). (Note: HDCP is available only to licensed HDCP buyers).
- HDCP/DRM Protection
  - Key info stored in the ASIC (i.e., no external ROM needed).
  - Both HDMI/DisplayPort output, and the HD audio are protected.
- Supports all region CGMSA/WSS (including CEA805-A type B packets) on NTSC/PAL/SECAM.

2.2.2 DVI/HDMI/DisplayPort Features

- The following display configurations are supported.
  - Up to three dual-link DVIs (TMDSA/DPA + TMDSB/DPB, TMDSC/DPC + TMDSD/DPD, and TXOUT_L + TXOUT_U when LVDS is not used).

- Four single-link DVIs (TMDSA/DPA, TMDSB/DPB, TMDSC/DPC, and TMDSD/DPD).
- Four DisplayPorts (TMDSA/DPA, TMDSB/DPB, TMDSC/DPC, and TMDSD/DPD).
- HDMI* (TMDSA/DPA, TMDSB/DPB, TMDSC/DPC, or TMDSD/DPD).

* Note: Only one HDMI can be active in a system at a time.

- Optional dithering or frame modulation from the 30-bpp internal display pipeline to 24 or 18-bit outputs on DVI/HDMI/DisplayPort if not using a 30-bpp output mode.
- DisplayPort Features:
  - Supports all the mandatory features of the DisplayPort Version 1.1a Specification and the following optional features:
    - 30-bpp support.
    - YCbCr 444 up to 30 bpp and 422 up to 20 bpp support.
    - HDCP support.
    - DisplayPort extension for test automation features, including test pattern generation.
    - DisplayPort Audio.
  - Each DisplayPort link can support three options for the number of lanes and two options for link data rate as follows:
    - 4, 2, or 1 lane(s).
    - 2.7 or 1.62-GHz link data rate per lane.
  - Supports all video modes supported by the display controller that do not oversubscribe the link bandwidth.
    - Examples of supported pixel rate/resolution support for 4 lanes at 2.7-GHz link rate:
      - Link bandwidth allows pixel clocks of up to 359 MPixels/sec for 24 bpp or 287 MPixels/sec for 30 bpp.
      - 2560x1600@60Hz, 24 bpp is supported.
    - Examples of supported pixel rate/resolution support for 2 lanes at 2.7-GHz link rate:
      - Link bandwidth allows pixel clocks of up to 179 MPixels/sec for 24 bpp or 143 MPixels/sec for 30 bpp.
      - 1920x1200@60Hz, 24 bpp is supported.
    - The following table shows the maximum pixel rates for 4, 2, or 1 lanes at 2.7-GHz link rate.

Table 2-1 Maximum pixel rates for 4, 2, or 1 lanes at 2.7-GHz link rate

	18 bpp	24 bpp	30 bpp
1 lane	119 MPixels/sec	89 MPixels/sec	71 MPixels/sec
2 lane	239 MPixels/sec	179 MPixels/sec	143 MPixels/sec
4 lane	359 MPixels/sec	359 MPixels/sec	287 MPixels/sec

- DVI/HDMI Features:
  - Advanced DVI capability supporting 10-bit HDR output.
  - Supports industry standard CEA-861B video modes including 480p, 720p, 1080i, and 1080p. For a full list of currently supported modes, contact your AMD CSS representative.
  - Maximum pixel rates for 24 bits/pixel outputs are:
    - DVI - 162 MPixels/sec per link (for 30 bpp dual-link; double for 24 bpp dual-link)
    - HDMI - 148.5 MPixels/sec
  - Fully compliant with the DVI electrical specification.
  - HDMI meets Vista logo requirements.

Table 2-2 HDMI Features

HDMI Feature	Compatibility
Link Capabilities	
Maximum TMDS bandwidth (Gbit/s)	1.65
Maximum data bandwidth (Gbit/s)	3.96
Video Capabilities	
Maximum resolution	1080p @ 60 Hz
RGB	Yes

Table 2-2 HDMI Features

HDMI Feature	Compatibility
YCbCr 4:4:4	Yes
YCbCr 4:2:2	Yes
xvYCC	Yes
HDMI 1.3 Deep Color	No
Maximum 4:4:4 Color Depth (bits per pixel)	8
Maximum 4:2:2 Color Depth (bits per component)	10
Audio Capabilities	
Auto lip-sync	Not in OS or audio drivers (Hardware ready).
PCM Audio Capabilities	
PCM Audio Rates Supported	192, 96, 48, 176.4, 88.2, 44.1, 32 kHz
PCM Audio Bits per Sample	24, 20, 16
PCM Maximum Channels	8
PCM Audio Maximum Bandwidth (Rate x Bits x Channels)	36.864 Mbps
Compressed Audio Capabilities	
Compressed Audio Maximum Bandwidth	6.144 Mbps
DRM Limits (Applies to compressed and PCM audio)	
Maximum Sample Rate with DRM Limit	48 kHz
Maximum Bits per Sample with DRM Limit	16
Specific non-PCM Audio Format Support	
IEC 61937 compressed format support (e.g. 5.1 channel Dolby DTS, 5.1 channel AC-3)	Yes
Dolby TrueHD bitstream capable	No
DTS-HD Master Audio bitstream capable	No
DVD-A (DST) support	No
SACD (DSD) support	No
CEC Capabilities	
Consumer Electronic Control (CEC)	No
Updated list of CEC commands	No

2.2.2.1 Integrated HD Audio Controller (Azalia) and Codec

- Integrated HD Audio codec supports linear PCM and Dolby® Digital (7.1) audio formats for HDMI, and DisplayPort outputs. (Note: Player applications may limit the audio output capabilities.)
- Separate logical chip function.
- Can encrypt data onto one associated HDMI or DisplayPort output.
- Compatible Microsoft UAA driver support for basic audio.
  - For advanced functionality, a 3rd party driver is required.
- Internally connected to the integrated HDMI or DisplayPort interface, hence no external cable required.
- Support for basic audio (32, 44.1 or 48-kHz stereo) and Dolby® Digital or DTS at the same sample rates.
- LPCM PCM multi-channel support with up to 24-bps and 192-kHz sampling rate.
- Support for up to 8 channels.
- HDCP content protection support for software audio stack.
- True audio plug-and-play capability for enhanced audio modes.

2.2.3 LVDS

- Single-link or dual-link LVDS transmitter, takes output from either one of the internal display controllers.
- Fully integrated with built-in self-biasing circuitry.
- LVDS can operate in either single- or dual-channel mode supporting displays from XGA (or below) up to QXGA.
- LVDS can drive either 18-bpp or 24-bpp displays with several dithering options from the internal 30-bpp display controller.

- Ratiometric expansion and compression supported on reduced blank panels.
- 3 pairs (+1 clock) and 4 pairs (+1 clock) modes for both single- and dual-channel LVDS.
- FPDI-2 compliant; compatible with receivers from National Semiconductor, Texas Instruments, and THine.
- LVDS eye pattern to improve testability of LVDS module.
- Fully compliant with electrical specification of ANSI/TIA/EIA-644.

2.2.4 Dual Analog Output Features

2.2.4.2 Dual DACs

- Two integrated triple 10-bit DACs with built-in reference circuit, takes output from either one of the internal display controllers (primary or secondary) or the internal analog TV encoder.
- Dual RGB CRT output.
- Support for stereo sync signal to drive a 3D display.
- Maximum pixel frequency of 400 MHz.
- Individual power down feature for each of the three guns.
- Fully compliant with electrical specification of VSIS.
- Fully integrated with built-in bandgap reference circuitry.
- Optional dynamic monitor detection for hot-plug/unplug capability. This feature affects the DAC voltage ranges. Please check with AMD for details before enabling.
- Integrated monitor and TV detection circuit (TV detection for DAC2 only).
- Internal demux in DAC2, allowing it to be output on one of the two output signal groups (TV or CRT), which allows separate external output filters without an external mux. See section below for TV-out features.

2.2.4.3 TVOut (on DAC2)

- Internal CE class TV encoder for YPbPr, NTSC and PAL (all variants supported). Can take its input from either internal display controller and output on DAC2.
- Component output: YPbPr for 480i, 480p, 576i, 576p, 720p, 1080i, and 1080p.
- YC S-video output for NTSC & PAL.
- Composite output for NTSC & PAL.
- Support for underscan in all TV modes.
- Scaling and internal adaptive flicker filtering available on both display paths for interlaced TV outputs.
- Two line comb-on-the-way-out for luma-chroma cross-talk prevention.
- Capable of supporting the following VBI data insertion standards:
  - Line 21 for NTSC data on odd and even fields separately, including Closed Caption, Parental Rating information and other Extended Data Services (EDS).
  - Wide Screen Signaling (WSS) for both PAL and NTSC, including the Analog Copy Generation Management System (CGMS-A).
  - Teletext data for PAL.
  - NABTS data for NTSC.

2.2.5 DVO Interface

- Configurable 12-bit DDR, 24-bit SDR/DDR digital outputs.
- Drives most popular TMDS, TV and HDMI transmitters up to 220-MHz frequency.
- Also supports external SCART encoders.
- DVO capable of driving a 64-bpp digital output.

2.3 Motion Video Acceleration Features

- Motion Video Decode Acceleration technology
  - Dedicated hardware (UVD - Unified Video Decoder) hardware for H.264, VC-1, and MPEG2 decode:
    - H.264 implementation is based on the ISO/IEC 14496-10 specification.

    - VC-1 implementation is based on the SMPTE 421M specification.
    - MPEG2 implementation is based on the ISO 13818-2, and Microsoft DirectX VA 1.01 specifications.
- Motion Video Processing Acceleration
    - Video scaling and fully programmable YCrCb to RGB color space conversion for full-screen / full-speed video playback and fully adjustable color controls.
    - Motion Adaptive and Vector based de-interlacing filter eliminates video artifacts caused by displaying interlaced video on non-interlaced displays, and by analyzing image and using optimal de-interlacing function on a per-pixel basis.
    - HD HQV and SD HQV support: noise removal, detail enchantment, color enhancement, cadence detection, sharpness, and advanced deinterlacing,
- Supports top quality DVD, time-shifted SDTV/HDTV television playback, and Blu-Ray disc with the lowest CPU usage.

2.4 Bus Support Features

- Fully compliant with PCI Express Base Specification Rev. 2.0. Native x16 PCIe bus interface.
- Supports x1, x2, x4, x8, and x16 lane widths.
- Supports x16 lane reversal where the receiver on lanes 0 to 15 on the graphics endpoint are mapped to the transmitter on lanes 15 down to 0 on the root complex.
- Supports x16 lane reversal where the transmitter on lanes 0 to 15 on the graphics endpoint are mapped the receiver on lanes 15 down to 0 on the root complex (requires corresponding support on the root complex).
- Supports x1, x2, x4, x8, and x16 polarity inversion.
- Supports “Mobile Graphics Low-Power Addendum 1.0”.

2.5 Power Management Features

- GPU solution in 55 nm.
- Full ACPI 1.0b, OnNow, and IAPC (Instantly Available PC) power management.
- Static and dynamic power management support (APM as well as ACPI) with full VESA DPM and Energy Star compliance.
- Full POWERPLAY^{TM} 8.0 support.
- The chip power management support logic supports four device power states - On, Standby, Suspend and Off - defined for the OnNow architecture. Each power state can be achieved by software control bits.
- Clocks to every major functional block are controlled by a unique dynamic clock switching technique which is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is significantly reduced during normal operation.
- Hardware automatically switches to a lower engine clock frequency if the ASIC is idle or partially idle.

2.6 Spread Spectrum Support

2.6.1 LVDS Spread Spectrum Support

- Internal LVDS Spread Spectrum Support
    - The E4690 pixel PLL spread spectrum controllers (PPLL and P2PLL) are capable of generating a triangular frequency modulation profile. The amount of spread and the modulation frequency is programmable. The recommended spread is up to 1.4 % center spread with modulation frequencies from 30-40 KHz.
    - Only the LVDS display is available to be spread (i.e., 1 PLL).
- External LVDS Spread Spectrum Support
    - External spread spectrum supported for LVDS transmitter via the GENERICA/GENERICB pin.

2.6.2 Engine and Memory Spread Spectrum Support

- Internal memory and/or core clock spread spectrum support programmable from 0 to 2% downspread.
- External memory and/or core clock spread spectrum support via the GPIO_16_SSIN pin.

2.6.3 DisplayPort Internal Spread Spectrum Support

- 0.5% downspread.
- Modulation frequency between 30 kHz and 33 kHz.

2.7 Internal Thermal Sensor

The E4690 has an integrated thermal sensor that offers the following advantages:

- Provides ASIC die temperature (accuracy ± 5°C) without the need for an external chip.
- High and low notification limits can be defined to generate an interrupt and to change power state.
- Can be used to control a fan through PWM (see *Table 3-25, "Thermal Interface Signals," on page 3-24*).
- A critical temperature limit can be defined to allow the system to protect the ASIC from damage (see GPIO_19_CTF).

2.8 Thermal Diode

The thermal diode in the E4690 is a grounded collector PNP BJT and is compatible with most temperature monitor chips from ADI (i.e. ADM 1020, 1030, etc.), TI, Maxim, and National Semiconductor. The thermal diode has two pins for its interface - DPLUS and DMINUS (see *Table 3-25, "Thermal Interface Signals," on page 3-24*). DPLUS connects to the emitter of the BJT while DMINUS connects its base. The collector is tied to substrate ground.

Note: Thermal diode can only be used when the ASIC is powered (i.e., it cannot be used when in D3 cold).

2.9 PC Design Guide Compliance

E4690 complies with all relevant sections of the current PC design guide specifications from Intel/Microsoft.

- Fully compliant with Windows Logo Program requirements for all target Operating Systems. This includes both the current Logo requirements and the future (draft) requirements that will be enforced during the lifespan of the product.
- Fully compliant with PCI Mobile Design Guide rev 1.1.
- Bi-endian support for compliance on a variety of processor platforms.

2.10 Test Capability Features

The E4690 has a variety of test modes and capabilities that provide a very high fault coverage and low DPM (defect per million) ratio:

- Full scan implementation on the digital core logic which provides high fault coverage through ATPG (Automatic Test Pattern Generation Vectors).
- Dedicated test logic for the on-chip custom memory macros to provide complete coverage on these modules.
- A JTAG test mode (which is largely compliant with the IEEE 1149.1 standard) including internal scan chain for access to chip-level test functions and for some board level connectivity testing.
- Integrated hardware diagnostic tests performed automatically upon initialization.
- Improved access to the analog modules and PLLs in the E4690 in order to allow full evaluation and characterization of these modules.

2.11 Other Features

- Support for serial ROM video BIOS.
- Support for 32 and 64-bit operating systems.

2.12 Compliance with US Commerce Department Control List ECCN 4A994

3D vector rate (as defined by the Wassenaar Agreement) is 133-M 10-pixel vectors per second.

Chapter 3
Signal Descriptions

This chapter describes the signals of the E4690.

The following notations are used:

- All active low signals are shown with the suffix “b” (e.g., CASA0b).
- “PD” denotes a permanent internal pull down. “PD-register” denotes an internal pull down which is register controlled, and by default is turned off. “PD-reset” denotes an internal pull down which is register controlled, and by default is turned on. “PD-reset” also denotes that the internal pull down is active during reset. “PD” or “PD-reset” is not relevant when the pins are in output modes.
- To designate a group of pins that have the same pin name but distinguished by a trailing number only (e.g. QSA_0, QSA_1, etc.), the abbreviation “piname[y: x]” is used, e.g., QSA_[7:0] means pins QSA_7 to QSA_0.
- The following conventions are used in the E4690 pin assignment.
  - NC or NC_* = No Connect
  - RSVD = These pins should not be connected and should be allowed to float
  - VSS = Connect to Ground
- Voltages indicated in the “Type” column of the signal descriptions tables are typical values.

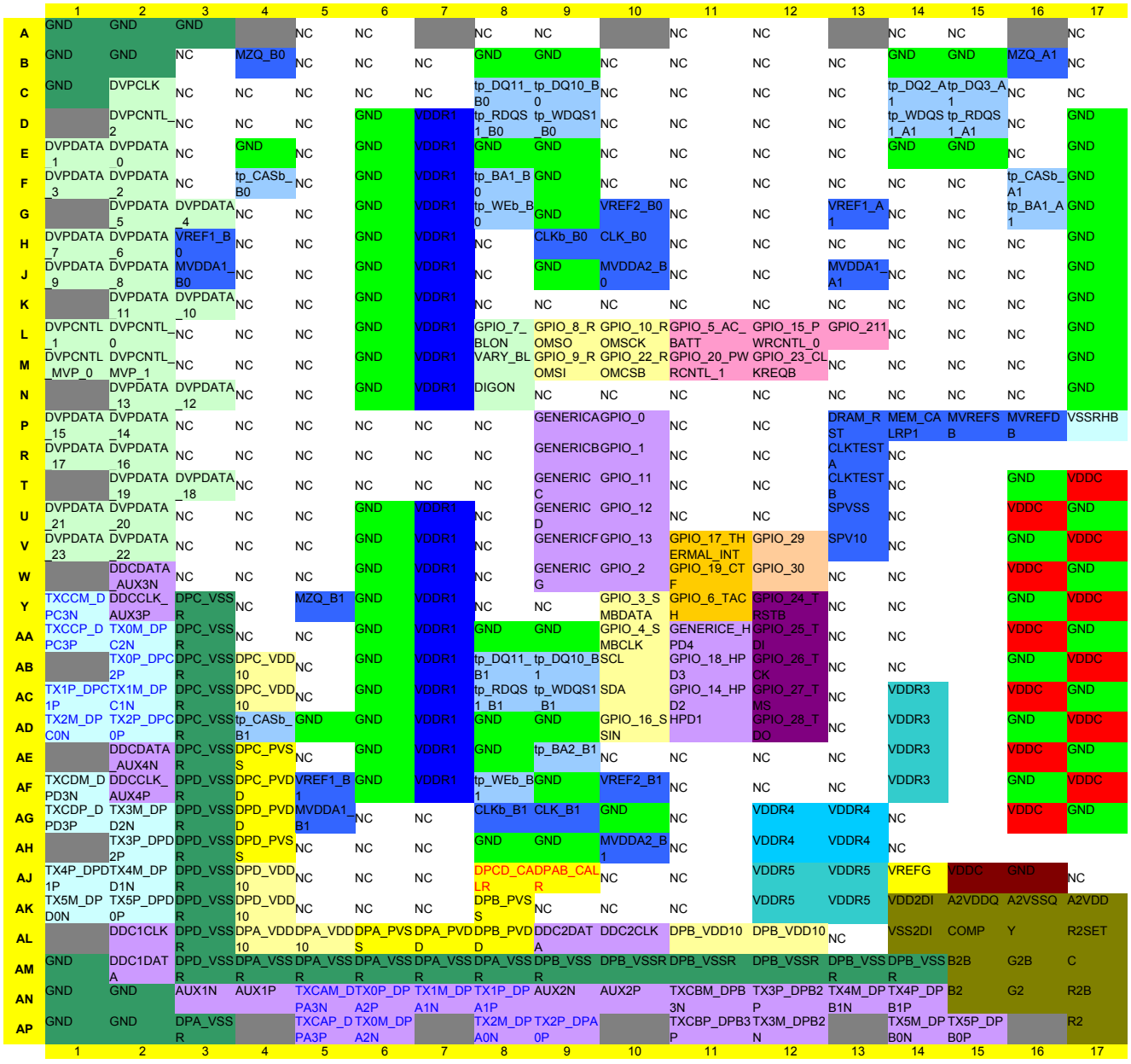
To link to a topic of interest, use the following list of hypertext linked cross references:

“E4690 Pin Assignment” on page 3-2
“PCI Express Bus Interface” on page 3-4
“Memory Interface (SGRAM, SDRAM)” on page 3-5
“Display Configurations Overview” on page 3-6
“Integrated HDMI / TMDS Interface” on page 3-6
“DisplayPort Interface” on page 3-7
“LVDS/TMDS2 Interface” on page 3-8
“External TMDS Interface.” on page 3-12
“CrossFire Interface” on page 3-14
“Hardware I2C Interface” on page 3-15
“Serial Flash Interface” on page 3-15
“General Purpose I/O Interface” on page 3-16
“Panel Control Interface” on page 3-18
“DAC1 (CRT) Interface” on page 3-18
“DAC2 (TV) Interface” on page 3-19
“Display Identification Interface” on page 3-22
“Test/JTAG/Debug Port” on page 3-24
“Thermal Information & Management Interface” on page 3-24
“External Spread Spectrum Interface (Optional)” on page 3-25
“PLLs and Crystal Interface” on page 3-26
“POWERPLAY Interface” on page 3-26
“Power and Ground Descriptions and Operating Conditions” on page 3-27
“Configuration Straps” on page 3-29

3.1 E4690 Pin Assignment

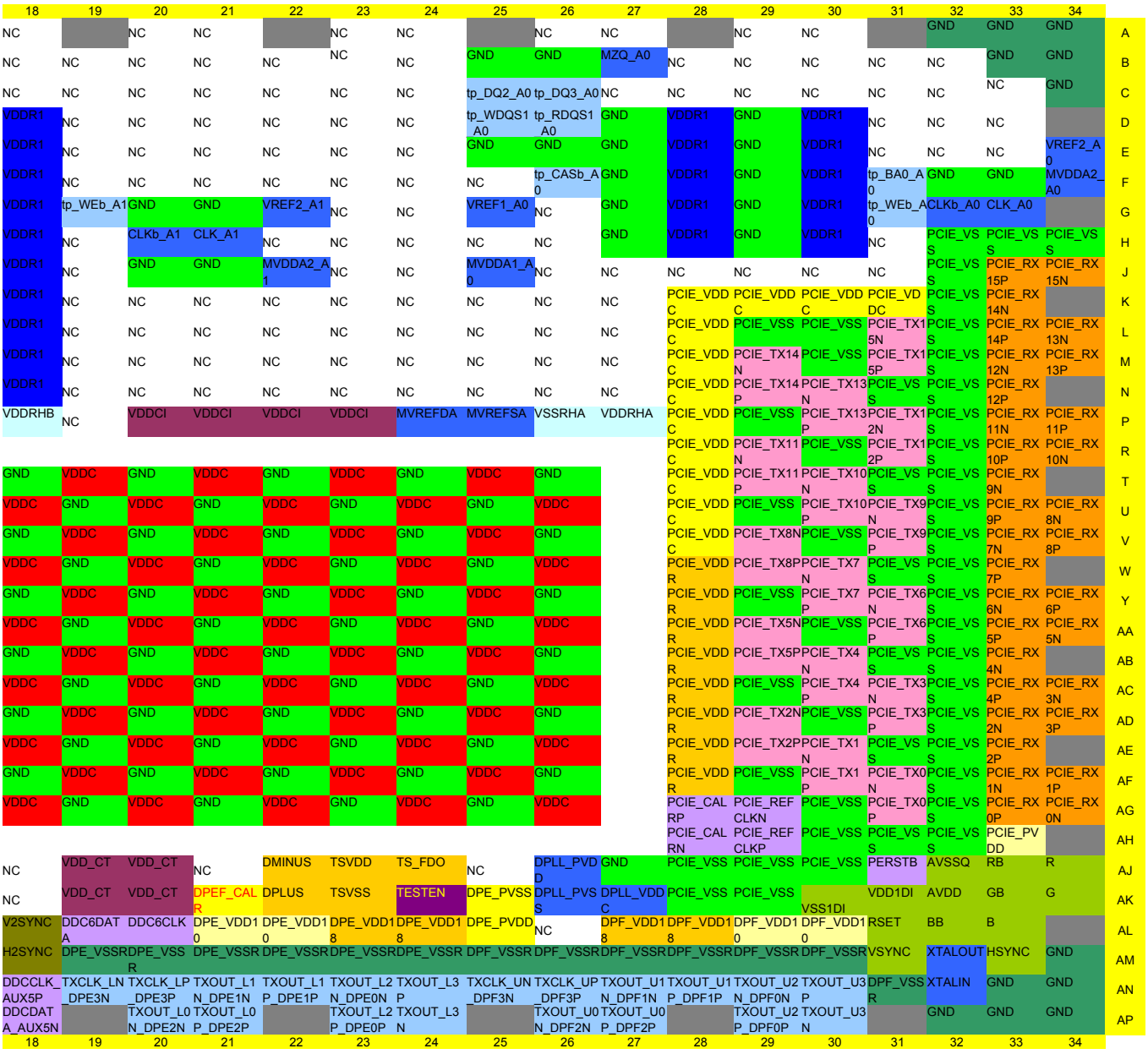
For a black and white version of the pin assignment, please see *Appendix B*.

3.1.1 E4690 Pin Assignment



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND	GND	GND		NC	NC		NC	NC		NC	NC		NC	NC		NC
B	GND	GND	NC	MZQ_B0	NC	NC	NC	GND	GND	NC	NC	NC	NC	GND	GND	MZQ_A1	NC
C	GND	DVPCLK	NC	NC	NC	NC	NC	tp_DQ11_B0	tp_DQ10_B0	NC	NC	NC	NC	tp_DQ2_A1	tp_DQ3_A1	NC	NC
D		DVPCNTL_2	NC	NC	NC	GND	VDDR1	tp_RDQS1_B0	tp_WDQS1_B0	NC	NC	NC	NC	tp_WDQS1_A1	tp_RDQS1_A1	NC	GND
E	DVPDATA_1	DVPDATA_0	NC	GND	NC	GND	VDDR1	GND	GND	NC	NC	NC	NC	GND	GND	NC	GND
F	DVPDATA_3	DVPDATA_2	NC	tp_CASb_B0	NC	GND	VDDR1	tp_BA1_B0	GND	NC	NC	NC	NC	NC	NC	tp_CASb_A1	GND
G		DVPDATA_5	DVPDATA_4	NC	NC	GND	VDDR1	tp_WEb_B0	GND	VREF2_B0	NC	NC	VREF1_A1	NC	NC	tp_BA1_A1	GND
H	DVPDATA_7	DVPDATA_6	VREF1_B0	NC	NC	GND	VDDR1	NC	CLKb_B0	CLK_B0	NC	NC	NC	NC	NC	NC	GND
J	DVPDATA_9	DVPDATA_8	MVDDA1_B0	NC	NC	GND	VDDR1	NC	GND	MVDDA2_B0	NC	NC	MVDDA1_A1	NC	NC	NC	GND
K		DVPDATA_11	DVPDATA_10	NC	NC	GND	VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND
L	DVPCNTL_1	DVPCNTL_0	NC	NC	NC	GND	VDDR1	GPIO_7_BLON	GPIO_8_ROMSO	GPIO_10_ROMSCK	GPIO_5_AC_BATT	GPIO_15_PWRCNTL_0	GPIO_211	NC	NC	NC	GND
M	DVPCNTL_MVP_0	DVPCNTL_MVP_1	NC	NC	NC	GND	VDDR1	VARY_BL	GPIO_9_ROMSI	GPIO_22_ROMCSB	GPIO_20_PWRCNTL_1	GPIO_23_CLKREQB	NC	NC	NC	NC	GND
N		DVPDATA_13	DVPDATA_12	NC	NC	GND	VDDR1	DIGON	NC	NC	NC	NC	NC	NC	NC	NC	GND
P	DVPDATA_15	DVPDATA_14	NC	NC	NC	NC	NC	NC	GENERICA	GPIO_0	NC	NC	DRAM_RST	MEM_CALRP1	MVREFSB	MVREFDB	VSSRHB
R	DVPDATA_17	DVPDATA_16	NC	NC	NC	NC	NC	NC	GENERICB	GPIO_1	NC	NC	CLKTESTA	NC			
T		DVPDATA_19	DVPDATA_18	NC	NC	NC	NC	NC	GENERICC	GPIO_11	NC	NC	CLKTESTB	NC		GND	VDDC
U	DVPDATA_21	DVPDATA_20	NC	NC	NC	GND	VDDR1	NC	GENERICD	GPIO_12	NC	NC	SPVSS	NC		VDDC	GND
V	DVPDATA_23	DVPDATA_22	NC	NC	NC	GND	VDDR1	NC	GENERICF	GPIO_13	GPIO_17_THERMAL_INT	GPIO_29	SPV10	NC		GND	VDDC
W		DDCDATA_AUX3N	NC	NC	NC	GND	VDDR1	NC	GENERICG	GPIO_2	GPIO_19_CTF	GPIO_30	NC	NC		VDDC	GND
Y	TXCCM_DPC3N	DDCCLK_AUX3P	DPC_VSSR	NC	MZQ_B1	GND	VDDR1	NC	NC	GPIO_3_SMBDATA	GPIO_6_TACH	GPIO_24_TRSTB	NC	NC		GND	VDDC
AA	TXCCP_DPC3P	TX0M_DPC2N	DPC_VSSR	NC	NC	GND	VDDR1	GND	GND	GPIO_4_SMBCLK	GENERICE_HPD4	GPIO_25_TDI	NC	NC		VDDC	GND
AB		TX0P_DPC2P	DPC_VSSR	DPC_VDD10	NC	GND	VDDR1	tp_DQ11_B1	tp_DQ10_B1	SCL	GPIO_18_HPD3	GPIO_26_TCK	NC	NC		GND	VDDC
AC	TX1P_DPC1P	TX1M_DPC1N	DPC_VSSR	DPC_VDD10	NC	GND	VDDR1	tp_RDQS1_B1	tp_WDQS1_B1	SDA	GPIO_14_HPD2	GPIO_27_TMS	NC	VDDR3		VDDC	GND
AD	TX2M_DPC0N	TX2P_DPC0P	DPC_VSSR	tp_CASb_B1	GND	GND	VDDR1	GND	GND	GPIO_16_SSIN	HPD1	GPIO_28_TDO	NC	VDDR3		GND	VDDC
AE		DDCDATA_AUX4N	DPC_VSSR	DPC_PVSS	NC	GND	VDDR1	GND	tp_BA2_B1	NC	NC	NC	NC	VDDR3		VDDC	GND
AF	TXCDM_DPD3N	DDCCLK_AUX4P	DPD_VSSR	DPC_PVDD	VREF1_B1	GND	VDDR1	tp_WEb_B1	GND	VREF2_B1	NC	NC	NC	VDDR3		GND	VDDC
AG	TXCDP_DPD3P	TX3M_DPD2N	DPD_VSSR	DPD_PVDD	MVDDA1_B1	NC	NC	CLKb_B1	CLK_B1	GND	NC	VDDR4	VDDR4	NC		VDDC	GND
AH		TX3P_DPD2P	DPD_VSSR	DPD_PVSS	NC	NC	NC	GND	GND	MVDDA2_B1	NC	VDDR4	VDDR4	NC			
AJ	TX4P_DPD1P	TX4M_DPD1N	DPD_VSSR	DPD_VDD10	NC	NC	NC	DPCD_CALR	DPAB_CALR	NC	NC	VDDR5	VDDR5	VREFG	VDDC	GND	NC
AK	TX5M_DPD0N	TX5P_DPD0P	DPD_VSSR	DPD_VDD10	NC	NC	NC	DPB_PVSS	NC	NC	NC	VDDR5	VDDR5	VDD2DI	A2VDDQ	A2VSSQ	A2VDD
AL		DDC1CLK	DPD_VSSR	DPA_VDD10	DPA_VDD10	DPA_PVSS	DPA_PVDD	DPB_PVDD	DDC2DATA	DDC2CLK	DPB_VDD10	DPB_VDD10	NC	VSS2DI	COMP	Y	R2SET
AM	GND	DDC1DATA	DPD_VSSR	DPA_VSSR	DPA_VSSR	DPA_VSSR	DPA_VSSR	DPA_VSSR	DPB_VSSR	DPB_VSSR	DPB_VSSR	DPB_VSSR	DPB_VSSR	DPB_VSSR	B2B	G2B	C
AN	GND	GND	AUX1N	AUX1P	TXCAM_DPA3N	TX0P_DPA2P	TX1M_DPA1N	TX1P_DPA1P	AUX2N	AUX2P	TXCBM_DPB3N	TX3P_DPB2P	TX4M_DPB1N	TX4P_DPB1P	B2	G2	R2B
AP	GND	GND	DPA_VSSR		TXCAP_DPA3P	TX0M_DPA2N		TX2M_DPA0N	TX2P_DPA0P		TXCBP_DPB3P	TX3M_DPB2N		TX5M_DPB0N	TX5P_DPB0P		R2
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Figure 3-1 E4690 Pin Assignment - Left Half



18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
NC		NC	NC		NC	NC		NC	NC		NC	NC		GND	GND	GND	A
NC	NC	NC	NC	NC	NC	NC	GND	GND	MZQ_A0	NC	NC	NC	NC	NC	GND	GND	B
NC	NC	NC	NC	NC	NC	NC	tp_DQ2_A0	tp_DQ3_A0	NC	NC	NC	NC	NC	NC	NC	GND	C
VDDR1	NC	NC	NC	NC	NC	NC	tp_WDQS1_A0	tp_RDQS1_A0	GND	VDDR1	GND	VDDR1	NC	NC	NC		D
VDDR1	NC	NC	NC	NC	NC	NC	GND	GND	GND	VDDR1	GND	VDDR1	NC	NC	NC	VREF2_A0	E
VDDR1	NC	NC	NC	NC	NC	NC	NC	tp_CASb_A0	GND	VDDR1	GND	VDDR1	tp_BA0_A0	GND	GND	MVDDA2_A0	F
VDDR1	tp_WEb_A1	GND	GND	VREF2_A1	NC	NC	VREF1_A0	NC	GND	VDDR1	GND	VDDR1	tp_WEb_A0	CLKb_A0	CLK_A0		G
VDDR1	NC	CLKb_A1	CLK_A1	NC	NC	NC	NC	NC	GND	VDDR1	GND	VDDR1	NC	PCIE_VSS	PCIE_VSS	PCIE_VSS	H
VDDR1	NC	GND	GND	MVDDA2_A1	NC	NC	MVDDA1_A0	NC	NC	NC	NC	NC	NC	PCIE_VSS	PCIE_RX15P	PCIE_RX15N	J
VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	PCIE_VDDC	PCIE_VDDC	PCIE_VDDC	PCIE_VDDC	PCIE_VSS	PCIE_RX14N		K
VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	PCIE_VDDC	PCIE_VSS	PCIE_VSS	PCIE_TX15N	PCIE_VSS	PCIE_RX14P	PCIE_RX13N	L
VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	PCIE_VDDC	PCIE_TX14N	PCIE_VSS	PCIE_TX15P	PCIE_VSS	PCIE_RX12N	PCIE_RX13P	M
VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	PCIE_VDDC	PCIE_TX14P	PCIE_TX13N	PCIE_VSS	PCIE_VSS	PCIE_RX12P		N
VDDRHB	NC	VDDCI	VDDCI	VDDCI	VDDCI	MVREFDA	MVREFSA	VSSRHA	VDDRHA	PCIE_VDDC	PCIE_VSS	PCIE_TX13P	PCIE_TX12N	PCIE_VSS	PCIE_RX11N	PCIE_RX11P	P
										PCIE_VDDC	PCIE_TX11N	PCIE_VSS	PCIE_TX12P	PCIE_VSS	PCIE_RX10P	PCIE_RX10N	R
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDC	PCIE_TX11P	PCIE_TX10N	PCIE_VSS	PCIE_VSS	PCIE_RX9N		T
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDC	PCIE_VSS	PCIE_TX10P	PCIE_TX9N	PCIE_VSS	PCIE_RX9P	PCIE_RX8N	U
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDC	PCIE_TX8N	PCIE_VSS	PCIE_TX9P	PCIE_VSS	PCIE_RX7N	PCIE_RX8P	V
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDR	PCIE_TX8P	PCIE_TX7N	PCIE_VSS	PCIE_VSS	PCIE_RX7P		W
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDR	PCIE_VSS	PCIE_TX7P	PCIE_TX6N	PCIE_VSS	PCIE_RX6N	PCIE_RX6P	Y
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDR	PCIE_TX5N	PCIE_VSS	PCIE_TX6P	PCIE_VSS	PCIE_RX5P	PCIE_RX5N	AA
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDR	PCIE_TX5P	PCIE_TX4N	PCIE_VSS	PCIE_VSS	PCIE_RX4N		AB
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDR	PCIE_VSS	PCIE_TX4P	PCIE_TX3N	PCIE_VSS	PCIE_RX4P	PCIE_RX3N	AC
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDR	PCIE_TX2N	PCIE_VSS	PCIE_TX3P	PCIE_VSS	PCIE_RX3N	PCIE_RX3P	AD
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDR	PCIE_TX2P	PCIE_TX1N	PCIE_VSS	PCIE_VSS	PCIE_RX2P		AE
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDR	PCIE_VSS	PCIE_TX1P	PCIE_TX0N	PCIE_VSS	PCIE_RX1N	PCIE_RX1P	AF
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_CALRP	PCIE_REFCLKN	PCIE_VSS	PCIE_TX0P	PCIE_VSS	PCIE_RX0P	PCIE_RX0N	AG
										PCIE_CALRN	PCIE_REFCLKP	PCIE_VSS	PCIE_VSS	PCIE_VSS	PCIE_PVDD		AH
NC	VDD_CT	VDD_CT	NC	DMINUS	TSVDD	TS_FDO	NC	DPLL_PVDD	GND	PCIE_VSS	PCIE_VSS	PCIE_VSS	PERSTB	AVSSQ	RB	R	AJ
NC	VDD_CT	VDD_CT	DPEF_CALR	DPLUS	TSVSS	TESTEN	DPE_PVSS	DPLL_PVSS	DPLL_VDDC	PCIE_VSS	PCIE_VSS	VSS1DI	VDD1DI	AVDD	GB	G	AK
V2SYNC	DDC6DATA	DDC6CLK	DPE_VDD10	DPE_VDD10	DPE_VDD18	DPE_VDD18	DPE_PVDD	NC	DPF_VDD18	DPF_VDD18	DPF_VDD10	DPF_VDD10	RSET	BB	B		AL
H2SYNC	DPE_VSSR	DPE_VSSR	DPE_VSSR	DPE_VSSR	DPE_VSSR	DPE_VSSR	DPF_VSSR	DPF_VSSR	DPF_VSSR	DPF_VSSR	DPF_VSSR	DPF_VSSR	VSYNC	XTALOUT	HSYNC	GND	AM
DDCCLK_AUX5P	TXCLK_LN_DPE3N	TXCLK_LP_DPE3P	TXOUT_L1N_DPE1N	TXOUT_L1P_DPE1P	TXOUT_L2N_DPE0N	TXOUT_L3P	TXCLK_UN_DPF3N	TXCLK_UP_DPF3P	TXOUT_U1N_DPF1N	TXOUT_U1P_DPF1P	TXOUT_U2N_DPF0N	TXOUT_U3P	DPF_VSSR	XTALIN	GND	GND	AN
DDCDATA_AUX5N		TXOUT_L0N_DPE2N	TXOUT_L0P_DPE2P		TXOUT_L2P_DPE0P	TXOUT_L3N		TXOUT_U0N_DPF2N	TXOUT_U0P_DPF2P		TXOUT_U2P_DPF0P	TXOUT_U3N		GND	GND	GND	AP
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Figure 3-2 E4690 Pin Assignment - Right Half

3.2 PCI Express Bus Interface

For more information on signal definitions and electrical requirements, refer to the "PCI Express Card Electromechanical 2.0 Specification", and "PCI Express Base 2.0 Specification".

Notes:

- E4690 supports x16 lane reversal, where the receiver on lanes 0 to 15 of the graphics endpoint are mapped to the transmitter on lanes 15 down to 0 of the root complex. If x16 lane reversal is employed, both the E4690 receive lanes and E4690 transmit lanes must be reversed. In addition, polarity inversion is supported (i.e. + of the differential pair is connected to the – at the root complex).

Table 3-1 PCI Express Bus Interface

Pin Group	Signal Names	I/O	PU/PD	Description
	PERSTb	I 3.3 V		Fundamental reset. 3.3 V tolerant pad This signal must be present during any FUNDAMENTAL RESET event (i.e. power up, warm boot, reset button press, CTL-ALT-DEL, Window restart, wake from D3, etc.).
PCI Express Reference Clocks	PCIE_REFCLKP/N	I 0.7 V		PCI Express PLL Differential Reference Clock (+/-). 100 MHz (+/-300 ppm) input frequency, 0-0.7 V single-ended swing. Note: A stable PCI Express reference clock must be provided less than 400ns after CLKREQ# is asserted. The reference clock can be disabled whenever CLKREQ# is deasserted.
PCI Express Data Channels	PCIE_TX[15:0]P/N	O 0.4 V		PCI Express transmitter output data channel TX [15:0] (+/-). Differential serial data transmitted at 5.0 GT/s bit rate.
	PCIE_RX[15:0]P/N	I 0.4 V		PCI Express receiver input data channel RX [15:0] (+/-). Differential serial data received at 5.0 GT/s bit rate.
PCI Express Calibration Macro	PCIE_CALRN	A		2 kΩ (1% tolerance) to PCIE_VDDC
	PCIE_CALRP	A		Connect to PCIE_VSS (ground) through a 1.27 kΩ (1%) resistor.
	GPIO_23_CLKREQB	I/O 3.3 V		Reserved.

3.3 Memory Interface (SGRAM, SDRAM)

Table 3-2 Memory Interface

Pin Name	Type	PD/PU	Description
MEM_CALRP1	A		This pin is used to control the variable drive capability of the memory section I/Os. It is connected to memory VSS through a 240-Ω (+/- 1%) resistor. The N transistors of the output buffer in the MEM_CALRP1 I/O will drive a current through this resistor and the resultant voltage is used to measure the drive capability.
DRAM_RST	O		Reset for all populated GDDR3 DRAMs (active low) Can be left unconnected for DDR2.
MVREFD[A:B]	I		Reference voltage per channel (memory data) (0.7 * VDDR1) (for GDDR3)
MVREFS[A:B]	I		Reference voltage per channel (memory strobe) (0.7 * VDDR1) (for GDDR3)

3.4 Display Configurations Overview

Table 3-3 Display Configurations Overview for Link A, B, C, and D

Pin Name	Possible Display Configurations	
TX[2:0]P/M_DPA[0:2]P/N TXCAP/M_DPA3P/N	Dual-link DVI (Links A + B	A DisplayPort or single-link DVI can be connected to either link A, B, C, or D and can be active simultaneously (the four links are independent). HDMI can be connected to either link A, B, C, or D also; however, only one HDMI can be active in a system at a time.
TX[5:3]P/M_DPB[0:2]P/N TXCBP/M_DPB3P/N		
TX[2:0]P/M_DPC[0:2]P/N TXCCP/M_DPC3P/N	Dual-link DVI (Links C + D)	
TX[5:3]P/M_DPD[0:2]P/N TXCDP/M_DPD3P/N		

Table 3-4 Display Configurations Overview for Link E and F

Pin Name	Possible Display Configurations			
TXOUT_L[2:0]P/N_DPE[0:2]P/N TXCLK_LP/N_DPE3P/N	Dual-link LVDS	Single-link LVDS	Dual--link DVI	A DisplayPort or single-link DVI can be connected to either link E or F but only **one can be active** at a time. HDMI can be connected to either link E or F also; however, only one HDMI can be active in a system at a time.
TXOUT_U[2:0]P/N_DPF[0:2]P/N TXCLK_UP/N_DPF3P/N				

3.5 Integrated HDMI / TMDS Interface

Note: The maximum pixel clock rate is 165 MHz, but it may be affected by TMDS signals layout and trace lengths. All signals in this interface can be unconnected if not used.

E4690 can support one single-link HDMI, three dual- or five single-link DVI outputs.

Please refer to the Digital Visual Interface (DVI) 1.0 Specification and the High-Definition Multimedia Interface (HDMI) Specification for additional details.

Table 3-5 Integrated HDMI / TMDS Interface

Pin Name	Type	Description
TX[2:0]P/M_DPA[0:2]P/N TX[5:3]P/M_DPB[0:2]P/N TX[2:0]P/M_DPC[0:2]P/N TX[5:3]P/M_DPD[0:2]P/N TXOUT_L[2:0]P/N_DPE[0:2]P/N TXOUT_U[2:0]P/N_DPF[0:2]P/N	O	TMDS data pairs (+/-) For single and dual-link configurations. See *Table 3-6, "E4690 Integrated HDMI / TMDS Configurations," on page 3-7* below for exact configurations. Transmitting at a bit rate of 10x pixel clock, up to 165-MHz pixel clock. Note: TMDS (DPExx or DPFxx) differential signals can only be configured as single link at a time (mutually exclusive).
TXCAP/M_DPA3P/N TXCBP/M_DPB3P/N TXCCP/M_DPC3P/N TXCDP/M_DPD3P/N TXCLK_LP/N_DPE3P/N TXCLK_UP/N_DPF3P/N	O	TMDS clock channels (+/-) For single and dual-link configurations. See *Table 3-6, "E4690 Integrated HDMI / TMDS Configurations," on page 3-7* below for exact configurations. Notes: TXCLK_LP/N_DPE3P/N is used as the clock pair for dual-link configurations. TMDS (DPExx or DPFxx) differential clock signals can only be configured as one single-link clock at a time (mutually exclusive)
DPAB_CALR DPCD_CALR DPEF_CALR	A	Analog calibration. Connect DP_CALR to VSS through a 150-Ω (1%) resistor.

3.5.1 Integrated HDMI / TMDS Configurations

The table below lists out the HDMI / TMDS configurations for E4690:

Table 3-6 E4690 Integrated HDMI / TMDS Configurations

Configuration	Pin Names		Requirements
Dual-Link DVI	Dual-Link 1: TXCAP/M_DPA3P/N TX[2:0]P/M_DPA[0:2]P/N TX[5:3]P/M_DPB[0:2]P/N Dual-Link 2: TXCCP/M_DPC3P/N TX[2:0]P/M_DPC[0:2]P/N TX[5:3]P/M_DPD[0:2]P/N Dual-Link 3: TXCLK_LP/N_DPE3P/N TXOUT_L[2:0]P/N_DPE[0:2]P/N TXOUT_U[2:0]P/N_DPF[0:2]P/N		A 100-nF capacitor is required on each differential signal placed near the connector. A 500-Ω resistor to ground is required on each differential signal line. One FET is needed to disconnect the path from these 500-Ω resistors to ground when the system is off and the panel is on. Notes: 1). E4690 can support one single-link HDMI, three dual- or five single-link DVI outputs from the available combinations in this table. 2). In single-link configurations, only one Single-Link 5 can only be used at a time (mutually exclusive) and not in multiple single-link configurations.
Single-Link HDMI / DVI	Single-Link 1: TXCAP/M_DPA3P/N TX[2:0]P/M_DPA[0:2]P/N Single-Link 3: TXCCP/M_DPC3P/N TX[2:0]P/M_DPC[0:2]P/N Single-Link 5: TXCLK_LP/N_DPE3P/N TXOUT_L[2:0]P/N_DPE[0:2]P/N	Single-Link 2 TXCBP/M_DPB3P/N TX[5:3]P/M_DPB[0:2]P/N Single-Link 4: TXCDP/M_DPD3P/N TX[5:3]P/M_DPD[0:2]P/N or Single-Link 5: TXCLK_UP/N_DPF3P/N TXOUT_U[2:0]P/N_DPF[0:2]P/N	

Note for single-link HDMI/DVI:

- HSYNC/VSYNC are transmitted on TX0P/M_DP[A, C]2P/N, TXOUT_L0P/N_DPE2P/N, or TX3P/M_DP[B, D]2P/N (Blue) channel during blank

Notes for dual-link DVI:

- HSYNC/VSYNC are transmitted on TX0P/M_DP[A, C]2P/N, TXOUT_L0P/N_DPE2P/N (Blue) channel during blank.
- Even pixel is the start of the active data, i.e. Pixel#0.
- The first pixel is defined as pixel 0 (an even pixel) as opposed to the DVI spec in dual-link TMDS.

3.6 DisplayPort Interface

E4690 supports five DisplayPort links.

Please refer to the DisplayPort Specification Version 1.1 for additional details.

Table 3-7 DisplayPort Interface

Pin Name	Type	Description
TX[2:0]P/M_DPA[0:2]P/N TXCAP/M_DPA3P/N TX[2:0]P/M_DPC[0:2]P/N TXCCP/M_DPC3P/N	I/O	DisplayPort (DPAxx or DPCxx) differential signals. DPAxx and DPCxx can be configured as DisplayPort links. A 100-nF capacitor is required on each differential signal placed near the connector.

Table 3-7 DisplayPort Interface (Continued)

Pin Name	Type	Description
TX[5:3]P/M_DPB[0:2]P/N TXCBP/M_DPB3P/N TX[5:3]P/M_DPD[0:2]P/N TXCDP/M_DPD3P/N	I/O	DisplayPort (DPBxx or DPDxx) differential signals. DPBxx and DPDxx can be configured as DisplayPort links. A 100-nF capacitor is required on each differential signal placed near the connector.
TXOUT_L[2:0]P/N_DPE[0:2]P/N TXCLK_LP/N_DPE3P/N TXOUT_L[2:0]P/N_DPF[0:2]P/N TXCLK_LP/N_DPF3P/N	I/O	DisplayPort (DPExx or DPFxx) differential signals. DPExx and DPFxx can **only** be configured as one DisplayPort link at a time (mutually exclusive). A 100-nF AC-coupled capacitor is required on each differential signal placed near the connector.
AUX1P/N AUX2P/N DDCDATA_AUX3N DDCCLK_AUX3P DDCDATA_AUX4N DDCCLK_AUX4P DDCDATA_AUX5N DDCCLK_AUX5P	I/O	DisplayPort Auxilliary differential signals. See *Table 3-22, "Display Identification Interface," on page 3-22*
DPAB_CALR DPCD_CALR DPEF_CALR	A	Analog calibration. Connect DPxx_CALR to VSS through a 150-Ω (1%) resistor.

3.7 LVDS/TMDS2 Interface

Note: All signals in this interface can be unconnected if not used.

Please refer to the Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits (ANSI/TIA/EIA-644) for additional information.

Table 3-8 LVDS/TMDS2 Interface

Pin Name	Type	Description
TXOUT_L[3:0]N/P TXOUT_L[2:0]N/P_DPE[0:2]N/P	O	LVDS lower data channel [3:0] (-/+) Transmitting at a bit rate of 7x pixel clock, up to 115-MHz pixel clock. This channel is used as the transmitting channel in single link LVDS mode. For pins used in TMDS mode see *Table 3-11, "TMDS2 Signal Mapping for Single and Dual Link," on page 3-10*
TXOUT_U[3:0]N/P TXOUT_U[2:0]N/P_DPF[0:2]N/P	O	LVDS upper data channel [3:0] (-/+) Only used in dual-channel LVDS mode. For pins used in TMDS mode see *Table 3-11, "TMDS2 Signal Mapping for Single and Dual Link," on page 3-10*
TXCLK_UN/P_DPF3N/P	O	LVDS upper clock channel (-/+) Only used in dual-channel LVDS mode.
TXCLK_LN/P_DPE3N/P	O	LVDS lower clock channel (-/+) **or** TMDS2 clock channel This channel is used as the transmitting channel in single-link LVDS or single-/dual-link TMDS2 mode.

3.7.1 LVDS Interface Signal Mapping

3.7.1.1 Single-Link LVDS Mode -- Signal Mapping

Table 3-9 Single-Link LVDS Mode -- Signal Mapping

Pin	Clock	18-bit	24-bit VESA	24-bit LDI
TXOUT_L0P/N_DPE2P/N	Phase 1	R0	R0	R2
	Phase 2	R1	R1	R3
	Phase 3	R2	R2	R4
	Phase 4	R3	R3	R5

Table 3-9 Single-Link LVDS Mode -- Signal Mapping (Continued)

Pin	Clock	18-bit	24-bit VESA	24-bit LDI
	Phase 5	R4	R4	R6
	Phase 6	R5	R5	R7
	Phase 7	G0	G0	G2
TXOUT_L1P/N_DPE1P/N	Phase 1	G1	G1	G3
	Phase 2	G2	G2	G4
	Phase 3	G3	G3	G5
	Phase 4	G4	G4	G6
	Phase 5	G5	G5	G7
	Phase 6	B0	B0	B2
	Phase 7	B1	B1	B3
TXOUT_L2P/N_DPE0_P/N	Phase 1	B2	B2	B4
	Phase 2	B3	B3	B5
	Phase 3	B4	B4	B6
	Phase 4	B5	B5	B7
	Phase 5	HSYNC	HSYNC	HSYNC
	Phase 6	VSYNC	VSYNC	VSYNC
	Phase 7	DATA_ENABLE	DATA_ENABLE	DATA_ENABLE
TXOUT_L3P/N	Phase 1	Not used	R6	R0/
	Phase 2	Not used	R7	R1
	Phase 3	Not used	G6	G0
	Phase 4	Not used	G7	G1
	Phase 5	Not used	B6	B0
	Phase 6	Not used	B7	B1
	Phase 7	Not used	Not used	Not used

3.7.1.2 Dual-Link LVDS Mode -- Signal Mapping

Table 3-10 Dual-Link LVDS Mode -- Signal Mapping

Pin	Clock	18-bit	24-bit VESA	24-bit LDI
TXOUT_L0P/N_DPE2P/N	Phase 1	EVEN_R0	EVEN_R0	EVEN_R2
	Phase 2	EVEN _R1	EVEN_R1	EVEN_R3
	Phase 3	EVEN _R2	EVEN_R2	EVEN_R4
	Phase 4	EVEN _R3	EVEN_R3	EVEN_R5
	Phase 5	EVEN _R4	EVEN_R4	EVEN_R6
	Phase 6	EVEN _R5	EVEN_R5	EVEN_R7
	Phase 7	EVEN _G0	EVEN_G0	EVEN_G2
TXOUT_L1P/N_DPE1P/N	Phase 1	EVEN _G1	EVEN_G1	EVEN_G3
	Phase 2	EVEN_G2	EVEN_G2	EVEN_G4
	Phase 3	EVEN_G3	EVEN_G3	EVEN_G5
	Phase 4	EVEN_G4	EVEN_G4	EVEN_G6
	Phase 5	EVEN_G5	EVEN_G5	EVEN_G7
	Phase 6	EVEN_B0	EVEN_B0	EVEN_B2
	Phase 7	EVEN_B1	EVEN_B1	EVEN_B3
TXOUT_L2P/N_DPE0P/N	Phase 1	EVEN_B2	EVEN_B2	EVEN_B4
	Phase 2	EVEN_B3	EVEN_B3	EVEN_B5
	Phase 3	EVEN_B4	EVEN_B4	EVEN_B6
	Phase 4	EVEN_B5	EVEN_B5	EVEN_B7
	Phase 5	HSYNC	HSYNC	HSYNC
	Phase 6	VSYNC	VSYNC	VSYNC
	Phase 7	DATA_ENABLE	DATA_ENABLE	DATA_ENABLE
TXOUT_L3P/N	Phase 1	Not used	EVEN_R6	EVEN_R0
	Phase 2	Not used	EVEN_R7	EVEN_R1
	Phase 3	Not used	EVEN_G6	EVEN_G0

Table 3-10 Dual-Link LVDS Mode -- Signal Mapping (Continued)

Pin	Clock	18-bit	24-bit VESA	24-bit LDI
	Phase 4	Not used	EVEN_G7	EVEN_G1
	Phase 5	Not used	EVEN_B6	EVEN_B0
	Phase 6	Not used	EVEN_B7	EVEN_B1
	Phase 7	Not used	Not used	Not used
TXOUT_U0P/N_DPF2P/N	Phase 1	ODD_R0	ODD_R0	ODD_R2
	Phase 2	ODD_R1	ODD_R1	ODD_R3
	Phase 3	ODD_R2	ODD_R2	ODD_R4
	Phase 4	ODD_R3	ODD_R3	ODD_R5
	Phase 5	ODD_R4	ODD_R4	ODD_R6
	Phase 6	ODD_R5	ODD_R5	ODD_R7
	Phase 7	ODD_G0	ODD_G0	ODD_G2
TXOUT_U1P/N_DPF1P/N	Phase 1	ODD_G1	ODD_G1	ODD_G3
	Phase 2	ODD_G2	ODD_G2	ODD_G4
	Phase 3	ODD_G3	ODD_G3	ODD_G5
	Phase 4	ODD_G4	ODD_G4	ODD_G6
	Phase 5	ODD_G5	ODD_G5	ODD_G7
	Phase 6	ODD_B0	ODD_B0	ODD_B2
	Phase 7	ODD_B1	ODD_B1	ODD_B3
TXOUT_U2P/N_DPF0P/N	Phase 1	ODD_B2	ODD_B2	ODD_B4
	Phase 2	ODD_B3	ODD_B3	ODD_B5
	Phase 3	ODD_B4	ODD_B4	ODD_B6
	Phase 4	ODD_B5	ODD_B5	ODD_B7
	Phase 5	HSYNC or reg driven	HSYNC or reg driven	HSYNC or reg driven
	Phase 6	VSYNC or reg driven	VSYNC or reg driven	VSYNC or reg driven
	Phase 7	DATA_ENABLE or reg driven	DATA_ENABLE or reg driven	DATA_ENABLE or reg driven
TXOUT_U3P/N	Phase 1	Not used	ODD_R6	ODD_R0
	Phase 2	Not used	ODD_R7	ODD_R1
	Phase 3	Not used	ODD_G6	ODD_G0
	Phase 4	Not used	ODD_G7	ODD_G1
	Phase 5	Not used	ODD_B6	ODD_B0
	Phase 6	Not used	ODD_B7	ODD_B1
	Phase 7	Not used	Not used	Not used

Notes:

1. Even pixel is the start of the active data, i.e. Pixel#0.

2. Our standard LVDS qualification uses HSYNC, VSYNC, and DATA_ENABLE on the lower channel only. (HSYNC, VSYNC and DATA_ENABLE on the upper channel is not qualified.)

3.7.2 TMDS2 Signal Mapping

Table 3-11 TMDS2 Signal Mapping for Single and Dual Link

Pin Name	Data phase	Signal
T2X0M/P_DPE2N/P (Channel 0)	Phase 1	EVEN_B9
	Phase 2	EVEN_B8
	Phase 3	EVEN_B7
	Phase 4	EVEN_B6
	Phase 5	EVEN_B5
	Phase 6	EVEN_B4
	Phase 7	EVEN_B3
	Phase 8	EVEN_B2
	Phase 9	EVEN_B1
	Phase 10	EVEN_B0

Table 3-11 TMDS2 Signal Mapping for Single and Dual Link (Continued)

Pin Name	Data phase	Signal
T2X1M/P_DPE1N/P (Channel 1)	Phase 1	EVEN_G9
	Phase 2	EVEN_G8
	Phase 3	EVEN_G7
	Phase 4	EVEN_G6
	Phase 5	EVEN_G5
	Phase 6	EVEN_G4
	Phase 7	EVEN_G3
	Phase 8	EVEN_G2
	Phase 9	EVEN_G1
	Phase 10	EVEN_G0
T2X2M/P_DPE0N/P (Channel 2)	Phase 1	EVEN_R9
	Phase 2	EVEN_R8
	Phase 3	EVEN_R7
	Phase 4	EVEN_R6
	Phase 5	EVEN_R5
	Phase 6	EVEN_R4
	Phase 7	EVEN_R3
	Phase 8	EVEN_R2
	Phase 9	EVEN_R1
	Phase 10	EVEN_R0
T2X3M/P_DPF2N/P (Channel 3)	Phase 1	ODD_B9
	Phase 2	ODD_B8
	Phase 3	ODD_B7
	Phase 4	ODD_B6
	Phase 5	ODD_B5
	Phase 6	ODD_B4
	Phase 7	ODD_B3
	Phase 8	ODD_B2
	Phase 9	ODD_B1
	Phase 10	ODD_B0
T2X4M/P_DPF1N/P (Channel 4)	Phase 1	ODD_G9
	Phase 2	ODD_G8
	Phase 3	ODD_G7
	Phase 4	ODD_G6
	Phase 5	ODD_G5
	Phase 6	ODD_G4
	Phase 7	ODD_G3
	Phase 8	ODD_G2
	Phase 9	ODD_G1
	Phase 10	ODD_G0
T2X5M/P_DPF0N/P (Channel 5)	Phase 1	ODD_R9
	Phase 2	ODD_R8
	Phase 3	ODD_R7
	Phase 4	ODD_R6
	Phase 5	ODD_R5
	Phase 6	ODD_R4
	Phase 7	ODD_R3
	Phase 8	ODD_R2
	Phase 9	ODD_R1
	Phase 10	ODD_R0

Notes:

- Shaded area (channels 0 to 2) for single link; shaded area + non-shaded area (Channels 0 to 5) for dual link

- H/VYSNC are transmitted on T2X0M/P_DPE2N/P (Blue) channel during blank.
- Even pixel is the start of the active data, i.e. Pixel#0.
- The first pixel is defined as pixel 0 (an even pixel) as opposed to the DVI spec in dual link TMDS.

3.8 External TMDS Interface.

Table 3-12 External TMDS Interface

Pin Name	Functional Name	Type	PD/PU	Description
DVPCLK	LCD_CLK	I/O 1.8 V	PD-reset	External TMDS clock. Set DVO_LSB_VMODE register bit to '0' for 1.8 V. Initialization Behavior: This signal is an input during and after reset (A PCIe reference clock is required to set the default state).
DVPCNTL_2	LCD_DE	I/O 1.8 V	PD-reset	Data Enable. This signal qualifies the active data area. DE is always required by the transmitter and must be high during active display time and low during blanking time. Set DVO_LSB_VMODE register bit to '0' for 1.8 V. Note: Can be left unconnected if not used. Initialization Behavior: This signal is an input during and after reset (no reference clock is required).
DVPCNTL_1	LCD_HSYNC	I/O 1.8 V	PD-reset	Horizontal sync output control signal. Set DVO_LSB_VMODE register bit to '0' for 1.8 V. Note: Can be left unconnected if not used. Initialization Behavior: This signal is an input during and after reset (no reference clock is required).
DVPCNTL_0	LCD_VSYNC	I/O 1.8 V	PD-reset	Vertical sync output control signal. Set DVO_LSB_VMODE register bit to '0' for 1.8 V. Note: Can be left unconnected if not used. Initialization Behavior: This signal is an input during reset (no reference clock is required). After reset, the default state is output low (0 V).
DVPDATA_[23:0]	LCDDATA[23:0]	I/O 1.8 V	PD-reset	External TMDS pixel bus. DVPDATA_[23:12]: Set DVO_MSB_VMODE register bit to '0' for 1.8 V. DVPDATA_[11:0]: Set DVO_LSB_VMODE register bit to '0' for 1.8 V. Notes: This bus has two separate power rails, one for the upper half, and one for the lower half of the 24 pins, so that if 12-bit DDR interface is used, the remaining unused 12 pins can be used as GPIOs at either 3.3 V or 1.8 V. These pins can be left unconnected if not used. Initialization Behavior: These signals are inputs during reset (no reference clock is required). After reset, the default states are output low (0 V).
GPIO_[13:11]	LCD_CNTL[2:0]	I/O 3.3 V	PD-reset	Optional software programmable outputs to connect to the CTL[3:1]/A[3:1]/DK[3:1] multifunction inputs of the TMDS transmitter, if required. These pins can be left unconnected if they are not required by the system designer. See the TMDS transmitter data sheet for more information regarding the function and usage of these pins.

3.8.1 12-Bit DDR External TMDS

Table 3-13 12-Bit DDR External TMDS Signal Mapping

Primary IO	LCD_CLK	Signal Mapping	LCD_CLK	Signal Mapping
DVPDATA_11	Rising edge	LCD_G[3]	Falling edge	LCD_R[7]
DVPDATA_10	Rising edge	LCD_G[2]	Falling edge	LCD_R[6]
DVPDATA_9	Rising edge	LCD_G[1]	Falling edge	LCD_R[5]
DVPDATA_8	Rising edge	LCD_G[0]	Falling edge	LCD_R[4]
DVPDATA_7	Rising edge	LCD_B[7]	Falling edge	LCD_R[3]

Table 3-13 12-Bit DDR External TMDS Signal Mapping (Continued)

Primary IO	LCD_CLK	Signal Mapping	LCD_CLK	Signal Mapping
DVPDATA_6	Rising edge	LCD_B[6]	Falling edge	LCD_R[2]
DVPDATA_5	Rising edge	LCD_B[5]	Falling edge	LCD_R[1]
DVPDATA_4	Rising edge	LCD_B[4]	Falling edge	LCD_R[0]
DVPDATA_3	Rising edge	LCD_B[3]	Falling edge	LCD_G[7]
DVPDATA_2	Rising edge	LCD_B[2]	Falling edge	LCD_G[6]
DVPDATA_1	Rising edge	LCD_B[1]	Falling edge	LCD_G[5]
DVPDATA_0	Rising edge	LCD_B[0]	Falling edge	LCD_G[4]

3.8.2 24-Bit DDR External TMDS

Table 3-14 24-Bit DDR External TMDS Signal Mapping

Primary IO	LCD_CLK	Signal Mapping	LCD_CLK	Signal Mapping
DVPDATA_23	Rising edge	LCD_PIX1_G[3]	Falling edge	LCD_PIX1_R[7]
DVPDATA_22	Rising edge	LCD_PIX1_G[2]	Falling edge	LCD_PIX1_R[6]
DVPDATA_21	Rising edge	LCD_PIX1_G[1]	Falling edge	LCD_PIX1_R[5]
DVPDATA_20	Rising edge	LCD_PIX1_G[0]	Falling edge	LCD_PIX1_R[4]
DVPDATA_19	Rising edge	LCD_PIX1_B[7]	Falling edge	LCD_PIX1_R[3]
DVPDATA_18	Rising edge	LCD_PIX1_B[6]	Falling edge	LCD_PIX1_R[2]
DVPDATA_17	Rising edge	LCD_PIX1_B[5]	Falling edge	LCD_PIX1_R[1]
DVPDATA_16	Rising edge	LCD_PIX1_B[4]	Falling edge	LCD_PIX1_R[0]
DVPDATA_15	Rising edge	LCD_PIX1_B[3]	Falling edge	LCD_PIX1_G[7]
DVPDATA_14	Rising edge	LCD_PIX1_B[2]	Falling edge	LCD_PIX1_G[6]
DVPDATA_13	Rising edge	LCD_PIX1_B[1]	Falling edge	LCD_PIX1_G[5]
DVPDATA_12	Rising edge	LCD_PIX1_B[0]	Falling edge	LCD_PIX1_G[4]
DVPDATA_11	Rising edge	LCD_PIX0_G[3]	Falling edge	LCD_PIX0_R[7]
DVPDATA_10	Rising edge	LCD_PIX0_G[2]	Falling edge	LCD_PIX0_R[6]
DVPDATA_9	Rising edge	LCD_PIX0_G[1]	Falling edge	LCD_PIX0_R[5]
DVPDATA_8	Rising edge	LCD_PIX0_G[0]	Falling edge	LCD_PIX0_R[4]
DVPDATA_7	Rising edge	LCD_PIX0_B[7]	Falling edge	LCD_PIX0_R[3]
DVPDATA_6	Rising edge	LCD_PIX0_B[6]	Falling edge	LCD_PIX0_R[2]
DVPDATA_5	Rising edge	LCD_PIX0_B[5]	Falling edge	LCD_PIX0_R[1]
DVPDATA_4	Rising edge	LCD_PIX0_B[4]	Falling edge	LCD_PIX0_R[0]
DVPDATA_3	Rising edge	LCD_PIX0_B[3]	Falling edge	LCD_PIX0_G[7]
DVPDATA_2	Rising edge	LCD_PIX0_B[2]	Falling edge	LCD_PIX0_G[6]
DVPDATA_1	Rising edge	LCD_PIX0_B[1]	Falling edge	LCD_PIX0_G[5]
DVPDATA_0	Rising edge	LCD_PIX0_B[0]	Falling edge	LCD_PIX0_G[4]

3.9 CrossFire Interface

For CrossFire functionality, the multiplexed pins indicated in the table below must have the I/O voltage set to 1.8 V. See VDDR4 and VDDR5 in *Table 3-29, "Power and Ground Descriptions and Operating Conditions," on page 3-27*.

Table 3-15 Crossfire Interface

Master GPU Signal	Slave GPU Signal	Type	PD/PU	Description
DVPDATA_[11:0]	DVPDATA_[11:0]	I/O 1.8 V	PD-reset	12-bit data Set DVO_LSB_VMODE register bit to '0' for 1.8 V. Initialization Behavior: These signals are inputs during reset (no reference clock is required). After reset, the default states are output low (0 V).
DVPCLK	DVPCLK	I/O 1.8 V	PD-reset	CLK_B for 12-bit data, DVPDATA[11:0]. Set DVO_LSB_VMODE register bit to '0' for 1.8 V. Initialization Behavior: This signal is an input during and after reset (A PCIe reference clock is required to set the default state).
DVPCNTL_2	DVPCNTL_2	I/O 1.8 V	PD-reset	DE_B for 12-bit data, DVPDATA[11:0]. Set DVO_LSB_VMODE register bit to '0' for 1.8 V. Initialization Behavior: This signal is an input during and after reset (no reference clock is required).
DVPDATA_[23:12]	DVPDATA_[23:12]	I/O 1.8 V	PD-reset	12-bit data Set DVO_MSB_VMODE register bit to '0' for 1.8 V. Initialization Behavior: These signals are inputs during reset (no reference clock is required). After reset, the default states are output low (0 V).
DVPCNTL_MVP_1	DVPCNTL_MVP_1	I/O 1.8 V	PD-reset	CLK_A for 12-bit data, DVPDATA[23:12]. Initialization Behavior: This signal is an input during and after reset (A PCIe reference clock is required to set the default state).
DVPCNTL_MVP_0	DVPCNTL_MVP_0	I/O 1.8 V	PD-reset	DE_A for 12-bit data, DVPDATA[23:12]. Initialization Behavior: This signal is an input during and after reset (A PCIe reference clock is required to set the default state).
GENERICD	GENERICD	I/O 3.3 V	PD-reset	FLOW_CNTL_IN: Flow control from the master GPU. For two GPU multi-GPU, this will be output on the master side, and input on the slave side.
GENERICC	GENERICC	I/O 3.3 V	PD-reset	FLOW_CNTL_OUT: This signal is not required for the 2 chip master/slave configuration.
GPIO_2	GPIO_2	I/O 3.3 V	PD-reset	SWAP_LOCK_IN: Control coming from the master GPU to synchronize 3D swap-lock and display-flip. For two GPU multi-GPU, this will be output on the master side, and input on the slave side.
GPIO_1	GPIO_1	I/O 3.3 V	PD-reset	SWAP_LOCK_OUT: This signal is not required for the 2 chip master/slave configuration.

Note:

VREFG is the input reference voltage for 1.8-V receivers. Use a voltage divider to set VREFG = 1.80 V/ 3 (or 0.60-V typ).

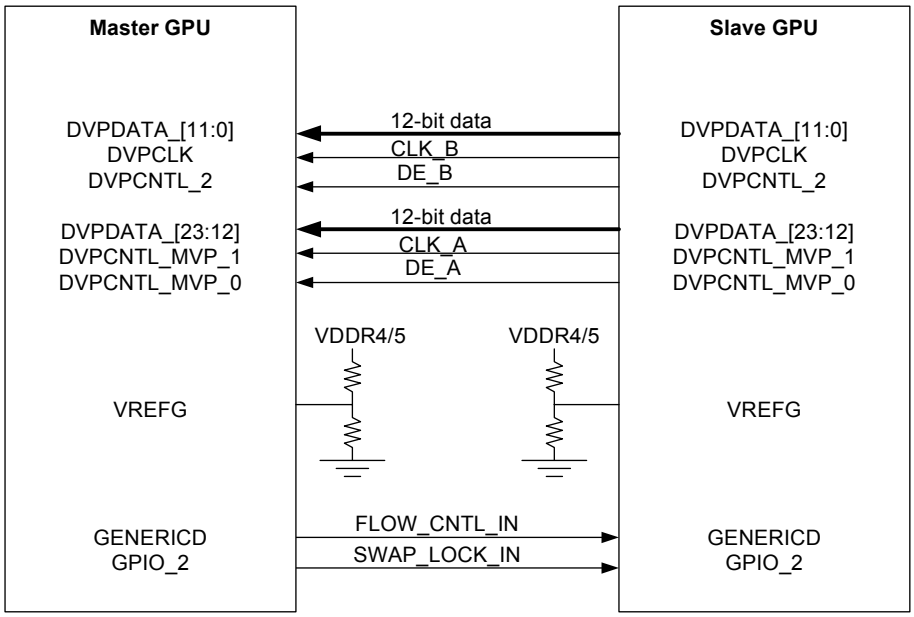


Figure 3-3 Crossfire: Master/Slave 2 GPU configuration

3.10 Hardware I2C Interface

Table 3-16 Hardware I2C Interface *

Pin Name	Functional Name	Type	PD/PU	Description
DVPDATA_19	SCL	I/O 3.3 V	PD-reset	I2C Clock This pin can be used as a general purpose I/O. Note: Can be left unconnected if not used. Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V).
DVPDATA_18	SDA	I/O 3.3 V	PD-reset	I2C Data/Address or general purpose I/O Note: Can be left unconnected if not used. Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V).

* Some GPIO pins can also be used for I2C interface – contact AMD for details.

3.11 Serial Flash Interface

Configuration straps must be set to identify the appropriate flash memory type, *See "Configuration Straps" on page 29.*

Table 3-17 Serial Flash Interface

Pin Name	Type	PD/PU	Description
GPIO_22_ROMCSB	O 3.3 V	PD-reset	BIOS ROM Chip Select Used to enable the ROM for ROM Read and Program operations. Note: A 10-K external pull-up (3.3 V) is required if an external BIOS ROM chip is used. Must be unconnected if no external BIOS ROM chip is used.
GPIO_10_ROMSCK	O 3.3 V	PD-reset	Serial ROM Clock to ROM, general purpose I/O or open drain type output.
GPIO_9_ROMSI	O 3.3 V	PD-reset	Serial ROM Input to ROM, general purpose I/O or open drain type output.
GPIO_8_ROMSO	I 3.3 V	PD-reset	Serial ROM Output from ROM, general purpose I/O or open drain type output.

3.12 General Purpose I/O Interface

Table 3-18 General Purpose I/O Interface

Pin Name	Type	PD/PU	Description
3.3-V GPIO's			
The signals below, if not used for their primary purpose, may be used as GPIO pins. GPIO_[17:0] can be used as level/pulse inputs to generate interrupts GPIO_{23:0] can be programmed to act as open drain outputs.			
GPIO_[6:0] GPIO_7_BLON GPIO_8_ROMSO GPIO_9_ROMSI GPIO_10_ROMSCK GPIO_[13:11]	I/O 3.3 V	PD-reset	General Purpose Input/Output. These signals are also used for other functions such as: External TMDS, **and** initialization pin straps Note: Can be unconnected if not used.
GPIO_14_HPD2	I/O 3.3 V	PD-reset	See *Table 3-22, "Display Identification Interface," on page 3-22* for a description of this pin.
GPIO_15_PWRCNTL_0	I/O 3.3 V	PD-reset	See *Table 3-28, "POWERPLAY Interface," on page 3-26* for a description of this pin.
GPIO_16_SSIN	I/O 3.3 V	PD-reset	See *Table 3-26, "External Spread Spectrum Interface," on page 3-25* for a description of this pin.
GPIO_17_THERMAL_INT	I/O 3.3 V	PD-reset	See *Table 3-25, "Thermal Interface Signals," on page 3-24* for a description of this pin.
GPIO_18_HPD3	I/O 3.3 V	PD-reset	HPD3 (hot plug detect) function. See *Table 3-22, "Display Identification Interface," on page 3-22* for a description of this pin.
GPIO_19_CTF	I/O 3.3 V	PD-reset	Critical temperature fault (active high) CTF will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. *See "Power Up/Down Sequence" on page 4.* The default critical temperature is 110°C; this temperature can be changed by software (VBIOS)
GPIO_20_PWRCNTL_1	I/O 3.3 V	PD-reset	Used together with GPIO_15_PWRCNTL_0 to switch an external regulator between four possible core voltage levels.
GPIO_21	I/O 3.3 V	PD-reset	General Purpose Input/Output. Note: Can be unconnected if not used.
GPIO_22_ROMCSB	I/O 3.3 V	PD-reset	BIOS ROM Chip Select for external serial ROM device, see *Table 3-17, "Serial Flash Interface," on page 3-15*
GPIO_23_CLKREQB	I/O 3.3 V	PD-register	Reserved.
GENERICA	I/O 3.3 V (VDDR3)	PD-register	Stereo display sync signal. See *Table 3-20, "DAC1 (CRT) Interface," on page 3-18* for a description of this pin. Can also be used as reference clock input for external spread spectrum for TMDS / LVDS. See *Table 3-26, "External Spread Spectrum Interface," on page 3-25* for more information. Initialization Behavior: A PCIe reference clock is required to set the default state.
GENERICB	I/O 3.3 V (VDDR3)	PD-register	Special output pin. Can be used as a reference clock input for TMDS / LVDS external spread spectrum. See *Table 3-26, "External Spread Spectrum Interface," on page 3-25* for more information. Can be unconnected if not used. Initialization Behavior: A PCIe reference clock is required to set the default state.
GENERICC	I/O	PD-register	Used as GPIO. Initialization Behavior: A PCIe reference clock is required to set the default state.
GENERICD	I/O	PD-register	Used as GPIO. Initialization Behavior: A PCIe reference clock is required to set the default state.
GENERICE_HPD4	I/O	PD-register	Used as GPIO. Can also be used as HPD4 (Hot Plug Detect) function, see *Table 3-22, "Display Identification Interface," on page 3-22* Initialization Behavior: A PCIe reference clock is required to set the default state.

Table 3-18 General Purpose I/O Interface (Continued)

Pin Name	Type	PD/PU	Description
GENERICF	I/O	PD-register	Used as GPIO. Initialization Behavior: A PCIe reference clock is required to set the default state.
GENERICG	I/O	PD-register	Used as GPIO. Initialization Behavior: A PCIe reference clock is required to set the default state.
3.3-V or 1.8-V GPIO's			
The signals below, if not used for their primary purpose, may be used as GPIO pins.			
DVPCLK	I/O 1.8 V or 3.3 V	PD-reset	See *Table 3-12, "External TMDS Interface," on page 3-12* for a description of this pin. Set DVO_LSB_VMODE register bit to '0' for 1.8 V or "1" for 3.3 V. Note: Can be left unconnected if not used. Initialization Behavior: This signal is an input during and after reset (A PCIe reference clock is required to set the default state).
DVPCNTL_[2:0]	I/O 1.8 V or 3.3 V	PD-reset	See *Table 3-12, "External TMDS Interface," on page 3-12* for a description of these pins. Set DVO_LSB_VMODE register bit to '0' for 1.8 V or "1" for 3.3 V. Note: Can be left unconnected if not used. Initialization Behavior: DVPCNTL{2:1} are inputs during and after reset (no reference clock is required). DVPCNTL0 is an input during reset (no reference clock is required). After reset, the default state is output low (0V).
DVPDATA_[23:0]	I/O 1.8 V or 3.3 V	PD-reset	External TMDS pixel bus. DVPDATA_[23:12]: Set DVO_MSB_VMODE register bit to '0' for 1.8 V or "1" for 3.3 V. DVPDATA_[11:0]: Set DVO_LSB_VMODE register bit to '0' for 1.8 V or "1" for 3.3 V. Note: this bus has two separate power rails, one for the upper half, and one for the lower half of the 24 pins, so that if 12-bit DDR interface is used, the remaining unused 12 pins can be used as GPIOs at either 3.3 V or 1.8 V. Note: These pins can be left unconnected if not used. Initialization Behavior: These signals are inputs during reset (no reference clock is required). After reset, the default states are output low (0 V).
DVPCNTL_MVP_[1:0]	I/O 1.8 V or 3.3 V	PD-reset	Multi-GPU control signals Set DVO_MSB_VMODE register bit to '0' for 1.8 V or "1" for 3.3 V. Initialization Behavior: This signal is an input during and after reset (A PCIe reference clock is required to set the default state).
VREFG	A-I 0.60 V		Input reference voltage for 1.8 V receivers (e.g. DVPData in 1.8 V mode). Use a voltage divider to set VREFG = 1.80 V / 3 (or 0.60 V typ). **Note: This pin is required for all 1.8V I/Os (DVPCLK, DVPCNTL_[2:0], DVPDATA_[23:0], DVPCNTL_MVP_[1:0]). Must always be connected.**

3.13 Panel Control Interface

Note: All signals in this interface can be unconnected if not used.

Table 3-19 Panel Control Interface

Pin Name	Type	PD/PU	Description
DIGON	O 3.3 V	PD	Controls Panel Digital Power On/Off Note: External pull-down recommended.
VARY_BL	O 3.3 V	PD	LCD PWM (Pulse Width Modulated) output to adjust LCD brightness. Active high. LVDS_GEN_CNTL.BL_MOD_LEVEL can be used to control the backlight level by means of pulse width modulation. Alternatively VARY_BL can be used to control backlight on/off (backlight enable) by setting LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_EN = 0. Note: External pull-down recommended
GPIO_7_BLON	I/O 3.3V	PD-reset	Controls Backlight On/Off. Active high. If not needed as the backlight enable signal, it can alternatively be used as a GPIO or an open drain type output. Note: External pull-down recommended

3.14 DAC1 (CRT) Interface

Table 3-20 DAC1 (CRT) Interface

Pin Name	Type	PD/PU	Description
R	A-O		Red for monitor. Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Red pin of the monitor (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Note: Can be unconnected if not used.
RB	A-O		Red Bar for current dump. Together the current through R and RB sum up to be the full-scale current. The R and RB pair should be routed as differential signals up to the termination close to the video connector. RB will be terminated using 37.5 Ω resistor to VSS close to video connector. **If** the differential portion is less than 30% of the total trace length (from the GPU to the connector), or the ground cannot be routed, then a single termination of R (G, B) with RB (GB, BB) connected directly to a well connected ground near the GPU is acceptable. Note: It must NOT be connected to AVSSQ or A2VSSQ (quiet) grounds.
G	A-O		Green for monitor. Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Green pin of the monitor (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Note: Can be unconnected if not used.
GB	A-O		Green Bar for current dump. Together the current through G and GB sum up to be the full-scale current. The G and GB pair should be routed as differential signals up to the termination close to the video connector. GB will be terminated using 37.5 Ω resistor to VSS close to video connector. **If** the differential portion is less than 30% of the total trace length (from the GPU to the connector), or the ground cannot be routed, then a single termination of R (G, B) with RB (GB, BB) connected directly to a well connected ground near the GPU is acceptable. Note: It must NOT be connected to AVSSQ or A2VSSQ (quiet) grounds.

Table 3-20 DAC1 (CRT) Interface (Continued)

Pin Name	Type	PD/PU	Description
B	A-O		Blue for monitor Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Blue pin of the monitor (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Note: Can be unconnected if not used.
BB	A-O		Blue Bar for current dump. Together the current through B and BB sum up to be the full-scale current. The B and BB pair should be routed as differential signals up to the termination close to the video connector. BB will be terminated using 37.5 Ω resistor to VSS close to video connector. **If** the differential portion is less than 30% of the total trace length (from the GPU to the connector), or the ground cannot be routed, then a single termination of R (G, B) with RB (GB, BB) connected directly to a well connected ground near the GPU is acceptable. Note: It must NOT be connected to AVSSQ or A2VSSQ (quiet) grounds.
HSYNC	I/O 3.3 V (VDDR3)	PD	Horizontal sync for monitor This signal requires an on board TTL buffer (e.g. LS125). Note: Can be unconnected if not used.
VSYNC	I/O 3.3 V (VDDR3)	PD	Vertical sync for monitor This signal requires an on board TTL buffer (e.g. LS125). Note: This pin is also used as the AUD[0} pinstrap. See *Table 3-30, "Pin Based Straps," on page 3-29* for more information.
RSET	A-O		DAC1 Reference Resistor Used to set the full scale DAC current through a high precision resistor (1%) of 499 Ω placed between this pin and AVSSQ.
GENERICA	I/O 3.3 V (VDDR3)	PD	Stereo display sync signal. Indicates left/right frame, or top/bottom field. Can be left unconnected if not used. Can also be used as reference clock input for external spread spectrum for TMDS / LVDS. See *Table 3-26, "External Spread Spectrum Interface," on page 3-25* for more information.

3.15 DAC2 (TV) Interface

The E4690 DAC2 has an internal demultiplexer which allows it to be output on one of the two output signal groups (TV or CRT). It saves on an external demultiplexer that would have been needed otherwise.

DAC2 is used as a PS2 (CRT) output.

Table 3-21 DAC2 (TV) Interface

Pin Name	Type	PD/PU	Description
H2SYNC	I/O 3.3 V (VDDR3)	PD	Horizontal Sync for 2nd CRT This signal requires an on board TTL buffer (e.g. LS125). Note: Can be unconnected if not used.
V2SYNC	I/O 3.3 V (VDDR3)	PD	Vertical Sync for 2nd CRT This signal requires an on board TTL buffer (e.g. LS125). Note: Can be unconnected if not used.
R2SET	A-O		DAC2 Reference Resistor. Used to set the full scale DAC current through a high precision resistor (1%) of 715 Ω placed between this pin and A2VSSQ. Note: Must be connected even if DAC2 is unused.

Table 3-21 DAC2 (TV) Interface (Continued)

Pin Name	Type	PD/PU	Description
Y	A-O		SVID Y output for SVideo-out **or** Y for component out. Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the SVID Y or Luminance pin of the monitor (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Notes: Can be unconnected if DAC2 is not used; however, if any of the 3 outputs (Y, C, and COMP) are used, then 75 Ω termination is required for all 3 outputs. Internal MUX directs output to either Y or G2. These two separate output paths allow one to use different output filters.
G2	A-O		Green for 2nd CRT monitor. Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Green pin of the monitor. (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Notes: Can be unconnected if DAC2 is not used; however, if any of the 3 outputs (G2, R2, and B2) are used, then 75 Ω termination is required for all 3 outputs. Internal MUX directs output to either Y or G2. These two separate output paths allow one to use different output filters.
G2B	A-O		2nd monitor Green Bar for current dump. Together the current through G2/Y and G2B sum up to be the full-scale current. The G2/G2B and Y/G2B pairs should be routed as differential signals up to the termination close to the video connector. G2B will be terminated to VSS using a 37.5 Ω on-board resistor close to the video connector. **If** the differential portion is less than 30% of the total trace length (from the GPU to the connector), or the ground cannot be routed, then a **single termination** of R2 (G2, B2) with R2B (G2B, B2B) connected directly to a ground near the GPU is acceptable. Note: It MUST NOT be connected to a clean (i.e. AVSSQ) ground. For standard TV out (i.e., S-video, composite video) only, differential termination is not required. **Single termination** is sufficient. Note: For TV out, the signals to be routed are C, Y, and COMP, instead of R2, G2, and B2.
C	A-O		SVID C output for SVideo-out **or** Pr for component out. Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the SVID C or Pr pin of the monitor (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Notes: Can be unconnected if DAC2 is not used; however, if any of the 3 outputs (Y, C, and COMP) are used, then 75 Ω termination is required for all 3 outputs. Internal MUX directs output to either C or R2. These two separate output paths allow one to use different output filters.
R2	A-O		Red for 2nd CRT monitor. Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Red pin of the monitor (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Notes: Can be unconnected if DAC2 is not used; however, if any of the 3 outputs (G2, R2, and B2) are used, then 75 Ω termination is required for all 3 outputs. Internal MUX directs output to either C or R2. These two separate output paths allow one to use different output filters.

Table 3-21 DAC2 (TV) Interface (Continued)

Pin Name	Type	PD/PU	Description
R2B	A-O		2nd monitor Red Bar for current dump. Together the current through R2/C and R2B sum up to be the full-scale current. The R2/R2B and C/R2B pairs should be routed as differential signals up to the termination close to the video connector. R2B will be terminated to VSS using a 37.5 Ω on-board resistor close to the video connector. **If** the differential portion is less than 30% of the total trace length (from the GPU to the connector), or the ground cannot be routed, then a **single termination** of R2 (G2, B2) with R2B (G2B, B2B) connected directly to a ground near the GPU is acceptable. Note: It MUST NOT be connected to a clean (i.e. AVSSQ) ground. For standard TV out (i.e., S-video, composite video) only, differential termination is not required. **Single termination** is sufficient. Note: For TV out, the signals to be routed are C, Y, and COMP, instead of R2, G2, and B2.
COMP	A-O		Composite Video for SVideo-out **or** Pb for component out. Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Composite Video or Pb pin of the monitor (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Notes: Can be unconnected if DAC2 is not used; however, if any of the 3 outputs (Y, C, and COMP) are used, then 75 Ω termination is required for all 3 outputs. Internal MUX directs output to either COMP or B2. These two separate output paths allow one to use different output filters.
B2	A-O		Blue for 2nd CRT monitor Analog DAC output, designed to drive a 37.5 Ω equivalent load, driving the Blue pin of the monitor (37.5 Ω = 75 Ω pull-down resistor to VSS on board in parallel with the 75 Ω CRT load/Impedance). Notes: Can be unconnected if DAC2 is not used; however, if any of the 3 outputs (G2, R2, and B2) are used, then 75 Ω termination is required for all 3 outputs. Internal MUX directs output to either COMP or B2. These two separate output paths allow one to use different output filters.
B2B	A-O		2nd monitor Blue Bar for current dump. Together the current through B2/COMP and B2B sum up to be the full-scale current. The B2/B2B and COMP/B2B pairs should be routed as differential signals up to the termination close to the video connector. B2B will be terminated to VSS using a 37.5 Ω on-board resistor close to the video connector. **If** the differential portion is less than 30% of the total trace length (from the GPU to the connector), or the ground cannot be routed, then a **single termination** of R2 (G2, B2) with R2B (G2B, B2B) connected directly to a ground near the GPU is acceptable. Note: It MUST NOT be connected to a clean (i.e. AVSSQ) ground. For standard TV out (i.e., S-video, composite video) only, differential termination is not required. **Single termination** is sufficient. Note: For TV out, the signals to be routed are C, Y, and COMP, instead of R2, G2, and B2.

3.16 Display Identification Interface

Table 3-22 Display Identification Interface

Pin Name	Type	PD/PU	Description
DDC1DATA/DDC1CLK or AUX1P/N	I/O 3.3 V (VDDR3)		DDC1DATA/DDC1CLK and AUX1P/N signal pairs are mutually exclusive. A design can use either the DDC1, or AUX1 pair on one display connector. Alternatively, DDC1DATA can be connected with AUX1N, and DDC1CLK can be connected to AUX1P for use on one DisplayPort connector (see reference schematics). For DDC function: DDC data and clock signals (I2C master): If DDC (I2C master) functionality is not used these pins can be associated with another DDC interface such as an LCD or a second (external) TMDS interface. Alternatively, they can be used as GPIOs for purposes such as detecting the panel type or memory type. These pins can be used to support internal High-bandwidth Digital Content Protection (HDCP) functionality. Note: Can be unconnected if not used. Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up. For AUX function: Auxiliary differential signals for DisplayPort: 1) 100-nF AC coupling capacitor is required on each differential signal placed near the connector, and 2) A source detection pull-down resistor (100-kΩ 5% tolerance) is required on each AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on each AUXN signal.
DDC2DATA/DDC2CLK or AUX2P/N	I/O 3.3 V (VDDR3)		DDC2DATA/DDC2CLK and AUX2P/N signal pairs are mutually exclusive. A design can use either the DDC2, or AUX2 pair on one display connector. Alternatively, DDC2DATA can be connected with AUX2N, and DDC2CLK can be connected to AUX2P for use on one DisplayPort connector (see reference schematics). For DDC function: DDC data and clock signals (I2C master): If DDC (I2C master) functionality is not used these pins can be associated with another DDC interface such as an LCD or a second (external) TMDS interface. Alternatively, they can be used as GPIOs for purposes such as detecting the panel type or memory type. These pins can be used to support internal High-bandwidth Digital Content Protection (HDCP) functionality. Note: Can be unconnected if not used. Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) before VDDC is powered up. For AUX function: Auxiliary differential signals for DisplayPort: 1) 100-nF AC coupling capacitor is required on each differential signal placed near the connector, and 2) A source detection pull-down resistor (100-kΩ 5% tolerance) is required on each AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on each AUXN signal.
DDC6DATA DDC6CLK	I/O 3.3 V (VDDR3)		DDC data and clock signals (I2C master). If DDC (I2C master) functionality is not used these pins can be associated with another DDC interface such as an LCD or a second (external) TMDS interface. Alternatively, they can be used as GPIOs for purposes such as detecting the panel type or memory type These pins can be used to support internal High-bandwidth Digital Content Protection (HDCP) functionality. Note: Can be unconnected if not used. Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) **before VDDC** is powered up.

Table 3-22 Display Identification Interface (Continued)

Pin Name	Type	PD/PU	Description
DDCDATA_AUX3N DDCCLK_AUX3P DDCDATA_AUX4N DDCCLK_AUX4P DDCDATA_AUX5N DDCCLK_AUX5P	I/O 3.3 V (VDDR3)		DDC data/clock for DVI/HDMI or auxiliary differential signals for DisplayPort (I2C master). For AUX mode: 1) 100-nF AC coupling capacitor is required on each differential signal placed near the connector, and 2) A source detection pull-down resistor (100-kΩ 5% tolerance) is required on each AUXP signal and a pull-up resistor (100-kΩ 5% tolerance) to 3.3 V is required on each AUXN signal. For I2C mode: Outputs are open drain and 5-V tolerant. External pull-up resistors to 5 V are required. These signals must be pulled high (to 3.3 V or 5 V) **before VDDC** is powered up.
HPD1 GPIO_14_HPD2 GPIO_18_HPD3 GENERICE_HPD4	I/O 3.3 V (VDDR3)	PD	Hot Plug Detect. These signals are used for hot plug detection with a TMDS panel. HPD will cause the GPU to raise an interrupt when HPD level is high (3.3 V). When the TMDS panel is used with the internal TMDS transmitter, it should be connected to the Hot Plug Detect pin of the DVI connector and protected from voltages above 3.3 V and below 0 V. When the TMDS panel is used with an external TMDS transmitter, it should be connected to the MSEN (Monitor Sense) pin of the external transmitter. When these signals are not used as hot plug detect, they can be used as generic interrupts.

3.17 Test/JTAG/Debug Port

In order to debug issues, AMD requires access to the JTAG (see *Chapter 8*) and debug ports on all prototype designs.

Test points can be used on the JTAG and debug ports' signals to minimize the PCB space needed.

Note that a separate video ROM is also required to enable this debug port.

Table 3-23 Test/JTAG Interface

Pin Name	Type	PD/PU	Description / JTAG Function
TESTEN	I 3.3 V (VDDR3)	PD	Reserved signal -- must be tied to ground 0 V through a 1 K resistor for normal ASIC operation
CLKTESTA	I		Internal use only (test pin). Connected to ground through a 4.7-K resistor.
CLKTESTB	I		Internal use only (test pin). Connected to ground through a 4.7-K resistor.
JTAG_TRSTB	I/O 3.3 V	PU	TRSTb (Tap Controller ASYNC Reset) When TESTEN=0 V, then input is a 'don't care'. JTAG mode: Pulled high (inactive) to 3.3 V..
JTAG_TDI	I/O 3.3 V	PU	TDI (Test Data Input)
JTAG_TCK	I/O 3.3 V	PD	TCK (Test Clock)
JTAG_TMS	I/O 3.3 V	PU	TMS (Test Mode Select)
JTAG_TDO	I/O 3.3 V	PD	TDO (Test Data Output)

Table 3-24 Debug Port

Pin Name	Functional Name
SCL	Serial Debug Port CLOCK
SDA	Serial Debug Port DATA
DVPDATA_[23:0]	TESTOUT[23:0]

3.18 Thermal Information & Management Interface

Table 3-25 Thermal Interface Signals

Pin Name	Type	PU/PD	Description
DPLUS	A-O		Thermal Diode plus side (anode), used by external temperature controller to obtain ASIC die temperature. Note: Can be unconnected if not used.
DMINUS	A-I		Thermal Diode minus side (cathode). Note: Can be unconnected if not used.
GPIO_17_THERMAL_INT	Bi-dir 3.3 V (VDDR3)	PD-reset	Thermal monitor interrupt Can be set as either: 1) An input from an external temperature sensor (ALERTb) , or 2) An output signaling that the ASIC temp (measured by the internal sensor) is above the high threshold or below the low threshold. Output can be open drain or 3.3-V output. (active low by default)
TS_FDO	O		Fan Drive Output (output to control fan) In PWM mode, the signal is an open drain output. The PWM frequency is 100 kHz to 12.5 MHz. Requires a 2.61-kΩ pull-up resistor.

Table 3-25 Thermal Interface Signals

Pin Name	Type	PU/PD	Description
GPIO_19_CTF	O	PD-reset	Critical temperature fault (active high) CTF will output 3.3 V if the on-die temperature sensor exceeds a critical temperature so that the motherboard can protect the ASIC from damage by removing power. *See "Power Up/Down Sequence" on page 4.* The default critical temperature is 110°C; this temperature can be changed by software (VBIOS).
GPIO_3_SMBDATA	Bi-dir 3.3 V (VDDR3)	PD-reset	SMBus Data. Connected to the SMBDATA line of the SMBus master with an external pull-up resistor. Supports a subset of the SMBus 2.0 protocol (Note that the following SMBus features are not supported: Dynamically Assigned Addresses, Packet Error Checking, Address Resolution Protocol (ARP), UDID, SMBSUS#, or SMBALERT) The SMBus slave id is programmable (default 0x41). In Power Xpress/Switchable graphics designs, the SMBus signals will pull-down the SMBus when the GPU is powered off. In these cases, isolation is required.
GPIO_4_SMBCLK	Bi-dir 3.3 V (VDDR3)	PD-reset	SMBus Clock. Connected to the line of the SMBus master with an external pull-up resistor. Supports a subset of the SMBus 2.0 protocol (Note that the following SMBus features are not supported: Dynamically Assigned Addresses, Packet Error Checking, Address Resolution Protocol (ARP), UDID, SMBSUS#, or SMBALERT) The SMBus slave id is programmable (default 0x41). In Power Xpress/Switchable graphics designs, the SMBus signals will pull-down the SMBus when the GPU is powered off. In these cases, isolation is required.

3.19 External Spread Spectrum Interface (Optional)

Note: All signals in this interface can be unconnected if not used.

Memory clock, engine clock and LVDS clock can all be spread by the GPU PLLs and therefore external spreading is optional.

Table 3-26 External Spread Spectrum Interface

Pin Name	Type	PD/PU	Description
GPIO_16_SSIN	I/O 3.3 V	PD-reset	Spread Spectrum clock input for memory clock and/or engine clock (maximum down spread of -2.5%). Requires a spread version of 27 MHz (please see description of XTALIN in *Table 3-27, "PLL and Crystal Interface," on page 3-26*). The modulation rate is 30-50 KHz. Note: When not used as the external Spread Spectrum clock input, GPIO_16_SSIN can be used as a General Purpose Input/Output or an open drain type output.
GENERICA GENERICB		PD-register	Reference clock input from the external spreading chip for LVDS (optional; 27 MHz with a maximum center spread of +/-1.4%). Either of the two available pixel PLLs can use the external spread spectrum reference clock as the source. The selection will depend on which PLL drives the panel.

3.20 PLLs and Crystal Interface

Table 3-27 PLL and Crystal Interface

Pin Name	Type	Description
XTALIN	A-I 1.8 V	An external 27-MHz LVTTL oscillator is connected to XTALIN to provide the reference clock. In order to provide reliable functionality, proper video synchronization and high quality display, it is recommended that the oscillator have as small an error and jitter as possible, with a balanced duty cycle (55-45 worst case). Oscillator characteristics: -Frequency: 27.000000 MHz -Voltage Swing: 1.8 V -Accuracy: +/- 10 ppm at room temp, (+/-30 ppm overall (including temperature drift) -Duty cycle (worst case): 45-55 (max) -Jitter: 200 ps (max) cycle to cycle jitter 300 ps (max) long term jitter (300 s delay after triggered edge) - Use an external resistor divider to bring XTALIN signal to 1.8-V level. The voltage divided XTALIN signal should still meet the jitter requirement specified above. - Additional requirement for crystals: use crystals with 30-Ω ESR (or less). The accuracy of the reference clock circuit is important to ensure that the color burst frequency is within range for NTSC or PAL TV output. For each design, color burst error should be verified across a sample of boards to ensure that it is within +/-100 Hz. Designs which use a crystal to support NTSC and PAL TV output should attempt to achieve a center frequency of 27.000000 MHz to meet both color burst error measurements. Since the crystal output frequency cannot be measured directly, one needs to verify the reference output from the spread spectrum chip. If this reference output is not available, then verifying the color burst error is the only means to tune the center frequency.
XTALOUT	A-O 1.8 V	PLL Reference Clock Instead of an oscillator, a series resonant crystal can be connected between XTALIN and XTALOUT to provide the reference clock for the internal PLLs of the E4690. A 1-MΩ resistor must be connected between XTALIN and XTALOUT when a crystal is used. Note: Designs which use an oscillator (TTL type input) must connect to XTALIN only. (An oscillator cannot be connected to XTALOUT.) Designs which use a crystal must connect the crystal to both XTALIN and XTALOUT in order to generate the clock input.

3.21 POWERPLAY Interface

Table 3-28 POWERPLAY Interface

Pin Name	Type	PD/PU	Description
GPIO_5_AC_BATT	I/O	PD-reset	GPIO_5_AC_BATT is an **optional** input which allows the system to request a fast power reduction by setting GPIO_5_AC_BATT to low (0 V). The resulting state transition may disturb the display momentarily. Power reductions that are less time critical should use the standard software methods only in order to prevent display disturbances.
GPIO_6 GPIO_15_PWRCNTL_0 GPIO_16_SSIN GPIO_20_PWRCNTL_1	I/O	PD-reset	Voltage control signals for the core (VDDC) and memory voltage regulators. GPIO_16_SSIN is only available for voltage control if external spread spectrum is not required. At Reset, these signals will be inputs with weak internal pull-down resistors. VBIOS can define all voltage control signals to be either 3.3-V or open drain outputs (all signals must be the same type). The output state (high/low) of these signals is programmable for each PowerPlay state.

3.22 Power and Ground Descriptions and Operating Conditions

Note 1: Power and ground pins, even if not used, must always be connected.

Note 2: All LVDS, TMDS, DAC and PLL power and ground pins (with the exception of the current dump pins) are sensitive to noise and should be provided with as clean a ground as possible. Bypass and bulk capacitors should be provided as necessary to maintain low noise on the power pins.

Note 3: The tolerances can be found at *Table 5-2, "Regulator Guidance," on page 5-3*

Table 3-29 Power and Ground Descriptions and Operating Conditions

Pin Name	Value	Description
Main Power and Ground Pins		
VDDC	0.9 V - 1.2 V	Dedicated core power, provides power to the internal logic. Note: The tolerance includes all sources of variation under all conditions (e.g. the regulator design error, fluctuations due to engine activity, etc.) as measured at the ASIC ball. PCB designers should verify that the VDDC voltage at the ASIC ball under maximum load (e.g. 3D benchmark) does not exceed this specified tolerance. Particular attention should be paid to minimize AC ripple on VDDCI.
VDDCI	Same as VDDC	Isolated (clean) core power for the I/O logic. Voltage level should match that of VDDC.
PCIE_PVDD	1.8 V	PCIe PLL power. If this rail is shared with the other PCIe power rails, it must have a separate filter. Note: A linear regulator is the optimal solution. However, if a switching regulator is used, the switching frequency must be < 300 kHz.
PCIE_VDDC	1.0 V to 1.1 V	PCIe Digital Power Supply (either 1.0 V or 1.1 V) If this rail is shared with the other PCIe power rails, it must have a separate filter. Note: A linear regulator is the optimal solution. However, if a switching regulator is used, the switching frequency must be < 300 kHz.
PCIE_VSS	Gnd	I/O ground.
PCIE_VDDR	1.8 V	PCIe I/O power.
TSVSS	Gnd	On-die thermal sensor ground.
TSVDD	1.8 V	On-die thermal sensor power.
VDDR1 (memory)	1.5 V - 2.0 V See memory specifications also.	I/O power for the memory interface on E4690
VDDRH[A:B]	1.5 V - 2.0 V	Dedicated power pins for memory clock pads for each channel. Should have the same voltage level as VDDR1.
VSSRH[A:B]	Gnd	Dedicated ground pins for memory clock pads for each channel.
VDDR5 (other digital)	1.8 V or 3.3 V	Power for DVP control pins (DVPCNTL_[0-2] and DVPCLK) and DVPDATA_[11:0] - external TMDS or GPIO; corresponds to DVO_LSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V;
VDDR4 (other digital)	1.8 V or 3.3 V	Power for DVPDATA_[23:12] - external TMDS or GPIO; corresponds to DVO_MSB_VMODE register bit; '1' - 3.3 V(default); '0' - 1.8 V;
VDDR3 (other digital)	3.3 V	IO power for 3.3 V pins (e.g. GPIO's).
VDD_CT	1.8 V	Level translation between core and I/O, excluding memory receivers. VDD_CT must remain powered whenever the ASIC is powered.
VSS	Gnd	Ground
LVDS/TMDS2/DP Power and Ground Pins		
DPE_PVDD	1.8 V	Analog Power for transmitter PLL. It should be a power for the PLL block of the macro.
DPE_PVSS	Gnd	Analog Ground for transmitter PLL. It should be a low-impedance ground return path for the PLL block of the macro.
DP[F:E]_VDD18	1.8 V	Output Driver Analog Power Supply.
DP[F:E]_VDD10	1.1 V	Output Driver Digital Power Supply.
DP[F:E]_VSSR	Gnd	Analog Ground for transmitter line drivers. It should be a low-impedance ground return path for the line drivers of the macro.

Table 3-29 Power and Ground Descriptions and Operating Conditions (Continued)

Pin Name	Value	Description
DP/TMDS Power and Ground Pins		
DP[B:A]_PVDD DP[D:C]_PVDD	1.8 V	DP/TMDS PLL Power (Links D, C, B, A) Each of the DP PLL Power Links has its own dedicated PLL analog power balls, because they can be operating at different output modes with different link clock frequencies. Separating on-chip power can provide improved isolation from periodic noise.
DP[B:A]_PVSS DP[D:C]_PVSS	Gnd	DP/TMDS PLL Ground (Links D, C, B, A) Each of the DP PLL Ground Links has its own dedicated PLL analog ground balls, because they can be operating at different output modes with different link clock frequencies. Separating on-chip ground can provide improved isolation from periodic noise.
DP[B:A]_VDD10 DP[D:C]_VDD10	1.1 V	DP/TMDS Transmitter Power (Links D, C, B, A)
DP[B:A]_VSSR DP[D:C]_VSSR	Gnd	DP/TMDS Transmitter Ground (Links D, C, B, A)
DAC1 and DAC2 Power and Ground Pins		
AVDD	1.8 V	DAC1 Analog Power Dedicated power for DAC1.
AVSSQ	Gnd	Bandgap Reference VSS (clean ground; used for bandgap) Dedicated ground for the CRT bandgap reference (DAC1) It should be a well-regulated, low-impedance clean ground reference for the bandgap of the macro. It should connect to the main pcb ground at a clean location, where there is no severe ground bounce activities.
VDD1DI	1.8 V	DAC1 Digital Power.
VSS1DI	Gnd	DAC1 Digital Ground
A2VDD	3.3 V	DAC2 Analog Power.
A2VDDQ	1.8 V	DAC2 Band Gap (clean) power supply. Need to be well regulated and must be isolated from noisy digital power supplies.
A2VSSQ	Gnd	DAC2 VSS (clean ground; used for bandgap) It should connect to the main pcb ground at a clean location, where there is no severe ground bounce activities.
VDD2DI	1.8 V	DAC2 Digital Power.
VSS2DI	Gnd	DAC2 Digital Ground
Main PLL and Memory PLL Power and Ground Pins		
DPLL_PVDD	1.8 V	Phase Lock Loop Power Dedicated analog power pin for display PLLs.
DPLL_VDDC	1.1 V	Phase Lock Loop Power Dedicated digital power pin for display PLLs.
DPLL_PVSS	Gnd	Phase Lock Loop Ground Dedicated ground for display PLLs.
SPV10	Same as VDDC	Engine Phase Lock Loop Power Dedicated power pin for engine, memory, and UVD PLL. Requires the same voltage as VDDC. Provide a filtered/quiet supply from VDDC.
SPVSS	Gnd	Engine Phase Lock Loop Ground Dedicated ground for engine PLL.
Other Signals		
VSS_MECH	Gnd	The primary purpose of these balls is to provide additional mechanical strength between the ASIC and PCB. The PCB pads for the VSS_MECH balls should be not connected (NC) on the PCB. VSS_MECH balls are electrically connected to the ASIC's ground plane (VSS) however they are not needed as ground signals.

3.23 Configuration Straps

3.23.1 Pin Based Straps

Each configuration pin strap has an internal pull-down resistor which provides a default value of 0. Nevertheless, each pin strap (including the reserved pin straps) still requires a resistor pad which provides the option of pulling the pin strap to 3.3 V at reset. These pads need to be provided since a) the ideal settings are defined during ASIC qualification, and b) pin compatible chips may require different settings. Other external logic on these pins must not conflict with the voltage level of the pin straps at reset.

Table 3-30 Pin Based Straps

Strap Name	Pin Name	Description	ASIC Default	Recommended Settings
CONFIGURATION STRAPS **Allow for pull-up pads for these straps and if these GPIOs are used, they must not conflict during reset.**				
VGA_DIS	GPIO_9_ROMSI	VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in the PCI configuration space): 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0 (Internal pulldown)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
TX_PWRS_ENB	GPIO_0	Transmitter Power Savings Enable 0: 50% Tx output swing Note: This setting can only be used if the PCIe bus design meets the "Low Loss Interconnect" requirements (see the PCI Express -- Mobile Graphics Low-Power Addendum.) 1: Full Tx output swing	0 (Internal pulldown)	0 (if the PCIe bus design meets the "Low Loss Interconnect" requirements) Otherwise: 1 Must be pulled to 3.3 V at reset using ~10-K (5%) resistor
TX_DEEMPH_EN	GPIO_1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled	0 (Internal pulldown)	0 (if the PCIe bus design meets the "Low Loss Interconnect" requirements. e.g. motherboard implementations.) Otherwise: 1 Must be pulled to 3.3 V at reset using ~10 K (5%) resistor (e.g. MXM and add-in boards).
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO_13 GPIO_12 GPIO_11	a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. See *"ROM Configurations" on page 3-30* b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. See *"Primary Memory Aperture size requested at PCI Configuration" on page 3-31*	0 (Internal pulldown)	Design dependent. See description for more information.
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0: Disable external BIOS ROM device 1: Enable external BIOS ROM device Note that when an external BIOS ROM device is used, GPIO_22_ROMCSB also connects to the ROM device's chip select (active low).	0 (Internal pulldown)	Design dependent. See description for more information.

Table 3-30 Pin Based Straps

Strap Name	Pin Name	Description	ASIC Default	Recommended Settings
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0]: 00 - No audio function; 01 - Audio for DisplayPort only; 10 - Audio for DisplayPort and HDMI if dongle is detected; 11 - Audio for both DisplayPort and HDMI. HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.	0 (Internal pulldown)	Design dependent. See description for more information.
BIF_GEN2_EN_A	GPIO_2	0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on. Note: This pin strap should be pulled to high (GPIO_2 = 1) when performing PCI Express electrical compliance testing at 5 GT/s using a CBB (compliance base board).	0 (Internal pulldown)	0 5.0 GT/s capability will be controlled by software.
RESERVED CONFIGURATION STRAPS				
Allow for pull-up pads for these straps and if these GPIOs are used, they must not conflict during reset				
RESERVED	H2SYNC GPIO_8_ROMSO	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0 (Internal pulldown)	0 Do not populate. Provide pad with option to pull to 3.3 V (VDDR3).
Pull-up pads are not required for these straps but if these GPIOs are used, they must not conflict during reset.				
RESERVED	GPIO_21 GENERICC	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected, however, if it is connected to additional logic on the board, the logic must not allow this signal to be driven or pulled to any value except GND at reset.	0 (Internal pulldown)	No PAD required. Ensure that no logic conflicts with these signals during Reset.

Table 3-31 ROM Configurations

Manufacturer	Part Number	CONFIG[2:0]
Numonyx (formerly ST Microelectronics)	M25P05A	100
	M25P10A	101
	M25P20	101
	M25P40	101
	M25P80	101
Chingis (formerly PMC)	Pm25LV512A	100
	Pm25LV010A	101

Note: Other ROM devices may be compatible. Contact AMD if ROM device other than those listed is desired.

Table 3-32 Primary Memory Aperture size requested at PCI Configuration

Size of the primary memory apertures	CONFIG[3:0]
128 MB	000
256 MB	001
64 MB	010
32 MB	Not Supported
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

The memory aperture defines the address range that the CPU can access. The default memory aperture size is 128 MB, however, it can be altered using pin straps or using a separate video ROM. The memory aperture size assigned to the GPU by the system BIOS is different from the physical memory size that the AMD graphics driver reports to the OS and control panel. It does not limit the GPU's ability to use the entire frame buffer memory at any time. Modern graphics and multimedia applications utilize drivers to alter the frame buffer contents – direct manipulation of the frame buffer by the CPU is limited. Therefore, having a memory aperture size that is smaller than the physical frame buffer size does not limit performance. The AMD graphics driver reports the memory size based on the amount of physical VRAM installed on the card rather than the memory aperture size.

Due to memory management constraints, the aperture size should be the same size as the frame buffer for 64 MB, 128 MB and 256 MB. For frame buffers larger than 256 MB (e.g. 512 MB, 1 GB) the aperture size should be 256 MB.

Note on Pin Based Straps:

For straps which must be set on the board, the use of 4.7 kΩ (Min) to 10 kΩ (Max) resistors is recommended (for pull-ups to power (3.3 V) or pull-downs to ground). 4.7 kΩ provides more noise immunity, whereas 10 kΩ will result in lower static power dissipation.

Please ensure that any circuitry connected to signals with pin straps does not interfere with the proper pin strap value at reset.

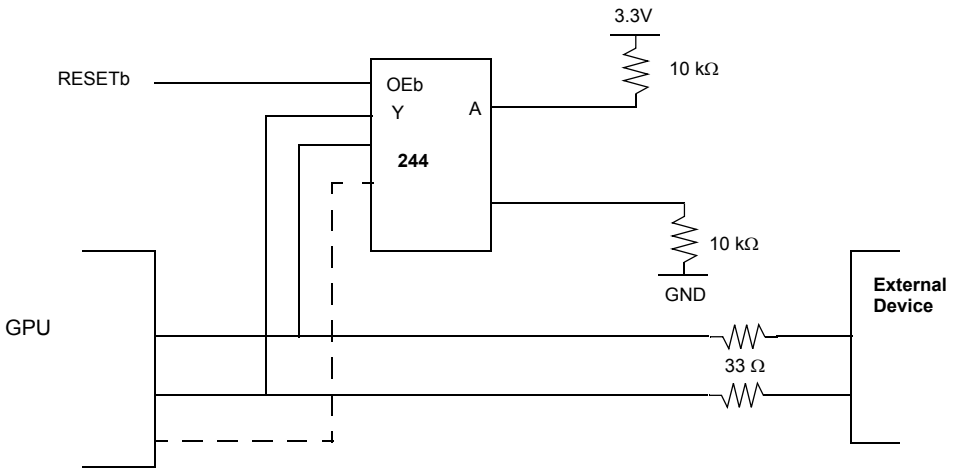


Figure 3-4 Implementation of Board Level Buffers

3.23.2 ROM Based Straps for Add-in Card Design

If ROM is attached (see CONFIG[2:0] pin based straps), then after RSTb goes inactive (high), the ROM is read at the addresses listed below to default to the internal settings.

The ROM based straps are ORed with the pin based straps.

Table 3-33 ROM Based Straps

Strap Name	Description	BIOS Address	Default BIOS Setting
F0_64BAR_EN_A	Enable 64-bit BAR for Function 0. Affects bit 2 of BLOCK_MEM_TYPE for each BAR register in PCI configuration space. Most commonly this strap is set to enable 64-bit BAR on desktop.	0x78 Bit 5	1
SUBSYS_VEN_ID[15:0]	Subsystem Vendor ID (SSVID) in the PCI configuration space. If the VBIOS ROM is not used, then the SBIOS is permitted to overwrite this register for each PCI function on the device before the enumeration cycle is initiated; otherwise the default value is used.	0x7C Bits 15 to 0	0x1002
F0_SUBSYS_ID[15:0]	Subsystem ID (SSID) for PCI configuration space for Function 0. If enabled, SSID for secondary display function (F1) is the set to the same value as the primary display function (F0) with bit 0 inverted.	0x7C Bits 31 to 16	0x1002
MEM_AP_SIZE[2:0]	Size of the primary memory apertures claimed in PCI configuration space 000 = 128 MB 001 = 256 MB 010 = 64 MB 011 = Reserved 1xx - Reserved It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.	0x78 Bits 9 to 7	Depends on board configuration.
VGA_DIS	VGA Disable determines whether or not the card will be recognized as the system's VGA controller (via the SUBCLASS field in PCI configuration space): 0 – VGA Controller capacity enabled. 1 – The device will not be recognized as the system's VGA controller.	0x80 Bit 27	0
DEBUG_ACCESS	Debug access sets the debug mux settings from the ROM in order to bring out internal signals for observation when registers are inaccessible through the host interface.	0x84 Bit 22	0

3.23.3 Readback of Strap Settings

Registers whose value is initialized or otherwise controlled by straps settings can be read back so that they can be examined by software.

The following configuration registers are initialized by straps:

Table 3-34 Configuration registers initialized by straps

Strap	Configuration Register	Register Read Address	Register Write Address
VGA_DIS	SUB_CLASS	PCICFG_F0 0xe	No write
SUBSYS_ID	SUBSYSTEM_ID	PCICFG_F0 0x2e-0x2f	PCICFG_F0 0x4e-0x4f
SUBSYS_VENDOR_ID	SUBSYSTEM_VENDOR_ID	PCICFG_F0 0x2c-0x2d	PCICFG_F0 0x4c-0x4d

Table 3-35 Strap values that can be read back directly

Strap	Register Read Address
TX_DEEMPH_EN	0x541c Bit 7
TX_PWRS_ENB	0x541c Bit 8
DEBUG_ACCESS	0x541c Bit 4
MEM_AP_SIZE	0x5408 Bits 9:7
BIOS_ROM_EN	0x17a8 Bit 19

Table 3-35 Strap values that can be read back directly (Continued)

Strap	Register Read Address
CONFIG[2]	0x17a8 Bit 13
CONFIG[1]	0x17a8 Bit 12
CONFIG[0]	0x17a8 Bit 11

Chapter 4
Timing Specifications

This chapter describes bus and memory timing specifications of the E4690.

To link to a topic of interest, use the following list of linked cross references:

"I2C Timing" on page 4-2

"Initialization Sequence and Timing" on page 4-4

"Serial Flash Read/Write Timing" on page 4-6

"LCD Panel Power Up/Down Timing" on page 4-7

"LCD Panel Backlight Control with PWM" on page 4-8.

"DVO Timing" on page 4-9

4.1 I²C Timing

4.1.1 Write Cycle

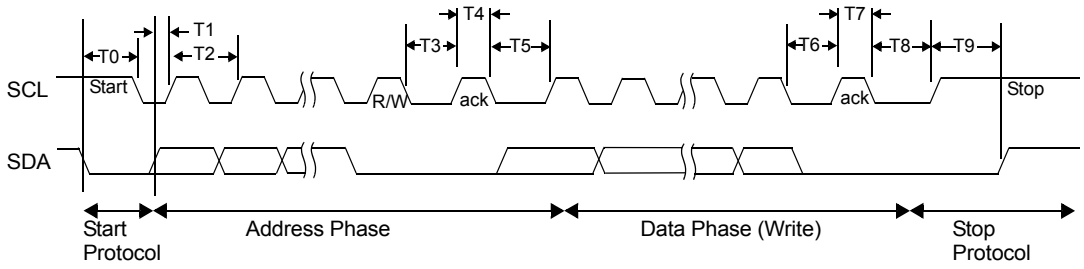


Figure 4-1 I²C Write Cycle

Table 4-1 I²C Write Cycle Timing Parameters

Symbol	Description	Min	Max
T0	Time for the start protocol	$T_{period}/2$	T_{period}
T1	Setup time for outbound address/data	$T_{period}/4$	$T_{period}/4$
T2 (T_{period})	Period of SCL	T_{period}	T_{period}
T3	Time elapse from the R/W bit to ACK	T_{period}	T_{period}
T4	Time for SCL high during ACK	$3T_{period}/4$	$3T_{period}/4$
T5	Time elapse from ACK to the first bit of data	T_{period}	T_{period}
T6	Time elapse from the negative edge of the SCL for the last bit of writing data to the ACK from slave	$7T_{period}/4$	$7T_{period}/4$
T7	Time for SCL high during ACK	$T_{period}/4$	$T_{period}/4$
T8	Time from ACK to STOP protocol	$3T_{period}/4$	$3T_{period}/4$
T9	Setup for stop protocol	$T_{period}/2$	$T_{period}/2$

4.1.2 Read Cycle

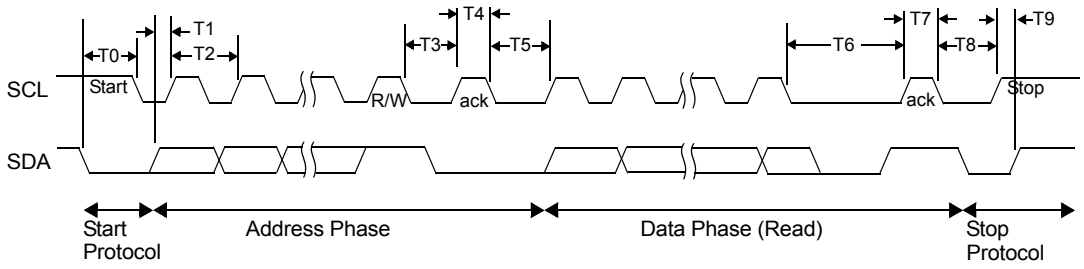


Figure 4-2 I²C Read Cycle

Table 4-2 I²C Read Cycle Timing Parameters

Symbol	Description	Min	Max
T0	Time for the start protocol	$T_{period}/2$	T_{period}
T1	Setup time for outbound address/data	$T_{period}/4$	$T_{period}/4$
T2 (T_{period})	Period of SCL	T_{period}	T_{period}
T3	Time elapse from the R/W bit to ACK	T_{period}	T_{period}
T4	Time for SCL high during ACK	$3T_{period}/4$	$3T_{period}/4$
T5	Time elapse from ACK to the first bit of data	T_{period}	T_{period}
T6	Time elapse from the negative edge of the SCL for the last bit of reading data to ACK from master	$3T_{period}/4$	$3T_{period}/4$
T7	Time for SCL high during ACK	$T_{period}/4$	$T_{period}/4$
T8	Time from ACK to STOP protocol	T_{period}	T_{period}
T9	Setup for stop protocol	$T_{period}/2$	$T_{period}/2$

4.2 Initialization Sequence and Timing

1a) Chip reset (PERSTb) is asserted.
1b) All GPIOs (except GPIO_23_CLKREQB) go to a tristated (input) mode at RESETb. Some GPIOs have internal pull-down (PD) resistors - see signal descriptions.
1c) PCIe REFCLK starts running.
2) External pin straps are driving their values onto the ASIC pins.
3) Chip reset (PERSTb) is deasserted. Note: For cases in which reset is provided while power remains on, the reset must be asserted for a minimum duration of 1ms before PERSTb is deasserted.
4) External pin strap values are latched internally.
5) E-Fuse state machine begins to read “E-Fuse straps”.
6) If ROM exists (and programmed), then ROM controller is requested to begin reading “ROM straps”. Note that this operation occurs only in the add-in card implementation. Step 5 and 6 occur in parallel.
7) E-fuse and ROM straps are “forwarded” to PHY.
8) If ASIC memory repair is required, then memory repair starts.
9) E-fuse and ROM straps are “forwarded” to other block in the ASIC
10) PHYPLL calibration starts after PCIe PERSTb deasserts, followed by PHY RX input calibration. Steps 8 and 9 occur in parallel.
11) The ASIC undergoes Link training according to the PCIe specification.
12) After Link Training is complete and step 9 is complete, the system is ready for the first transaction, e.g., configuration space request.

The figure and the table below provide an outline of the E4690 internal reset and strap latching sequence.

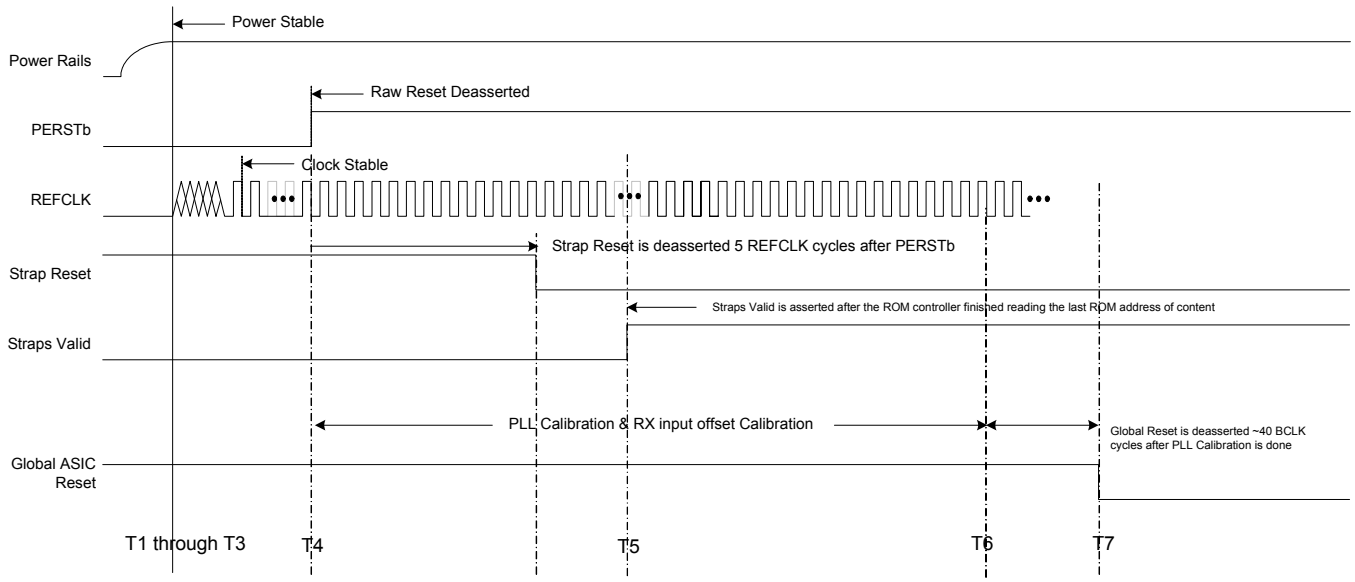


Figure 4-3 E4690 Power-On Reset Sequence

Table 4-3 E4690 Power-On Reset Sequence Timing Parameters

Time	Event	Actions
T1	Chip reset (PERSTb) is asserted	All ASIC output pins tri-state
T2	PCIe REFCLK starts running	
T3	PCIe is running	All internal clocks start running at PCIe REFCLK.
T4	Chip reset (PERSTb) is deasserted	Pin straps are latched.
T4+16 REFCLK cycles	Global reset is asserted	All internal clocks start running at PCIe REFCLK speed. All internal registers go to their default values.
T5	E-fuse & ROM straps are read (& distributed to the client logic)	PHY {calibration/} training starts.
T6	E-fuse & ROM straps distribution is done	

Table 4-3 E4690 Power-On Reset Sequence Timing Parameters (Continued)

Time	Event	Actions
T7	PCIe Link Training starts	

4.2.1 Standard Boot-up Sequence

1. PERSTb (i.e. fundamental reset) is asserted to the board.
2. Select internal strap values are determined by the configuration of pin-straps on a subset of GPIOs on the board.
3. PERSTb is deasserted, and pin-strap settings are latched permanently into the device (until PERSTb is asserted again, or the power is removed).
4. Device begins to read “e-fuse straps”.
5. For an add-in card implementation, the device (in parallel to #3) begins to read “ROM-based straps” from its external ROM.
6. The system begins enumerating the devices attached to it by issuing configuration transactions. The system may issue a configuration transaction to the device at this time; however, the device may not respond to it until its internal reset sequence is complete.
7. For an add-in card implementation, the device completes reading the “ROM-based straps”. ROM straps are only read in once when the device is initially booted.
8. Device internal reset is complete.
9. The chip responds to any pending transaction requests. The system continues PCI Express enumeration, which sets up the configuration registers of the device.
10. The system copies the contents of the ROM into system memory, and executes the video BIOS, completing the device initialization. This occurs before POST begins in the system BIOS, as per PC98.
11. The device is ready for normal operation.

There are three configurations for strap/BIOS implementation:

Configuration 1. The controller is located on an add-in card, and there is access to a local video BIOS serial Flash memory.

The ROM state machine of the E4690 will read in all the “ROM based straps” right after PERSTb reset is deasserted. There are a total of 36 bytes worth of “ROM based straps” which are stored at byte location 0x70 through 0x93 in the serial Flash memory. See *Table 3-33, “ROM Based Straps,” on page 3-32* for details.

Configuration 2. The controller is located on the system motherboard and the video BIOS is stored in the system BIOS serial Flash memory.

The System BIOS will be responsible for loading the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID through an aliased address in the controller chip's reserved configuration space. The reason for writing through an aliased address (16#4c) is that the config location 16#2c is read only. Any writes to this location (16#4c) will also change the content of the SUBSYSTEM_VENDOR_ID at 16#2c.

Configuration 3. Combination of configurations **1** and **2** (add-in card and device on motherboard)

The system BIOS will take care of the graphics device on the motherboard as in case 2, while the chip on the add-in board will be taken care of as in case 1. This should cover the situation where the OS does not read the add-in card’s video BIOS because the ROM state machine from the graphics chip reads the “ROM based straps” independently from the video BIOS.

Note: If neither the system BIOS nor the add-in card video BIOS supply the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID, their values are defaulted to DEVICE_ID and VENDOR_ID (1002h) respectively inside the chip.

4.3 Serial Flash Read/Write Timing

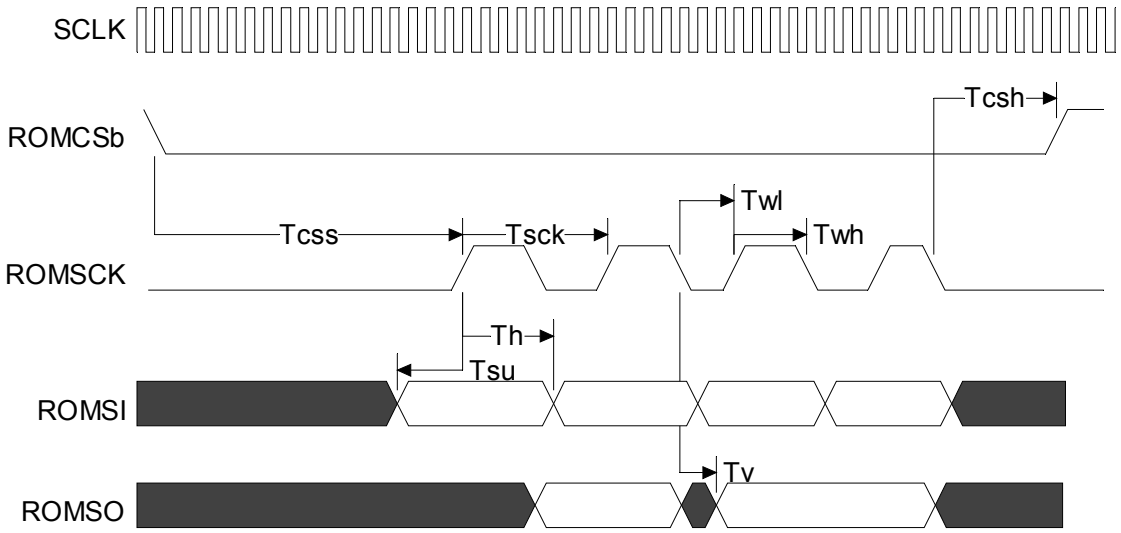


Figure 4-4 Serial flash write/read timings

Table 4-4 Serial Flash Write/Read Timing Parameters for Bootup case SCLK=100 MHz, XTALIN=27 MHz, ROM_CNTL.SCK_PRESCALE_CRYSTAL_CLK=0x1

Symbol	Description	Min (ns)	Max (ns)
Tcss	ROMCSb falling edge to first clock sent to the device	110	
Tsck	ROMSCK period	70	
Twl	ROMCSK low time	30	
Twh	ROMSCK high time	30	
Tsu	ROMSI data setup	20	
Th	ROMSI data hold	40	
Ty	ROMSO data valid	0	20
Tcsh	Last clock sent to ROMCSb rising edge	70	

4.4 LCD Panel Power Up/Down Timing

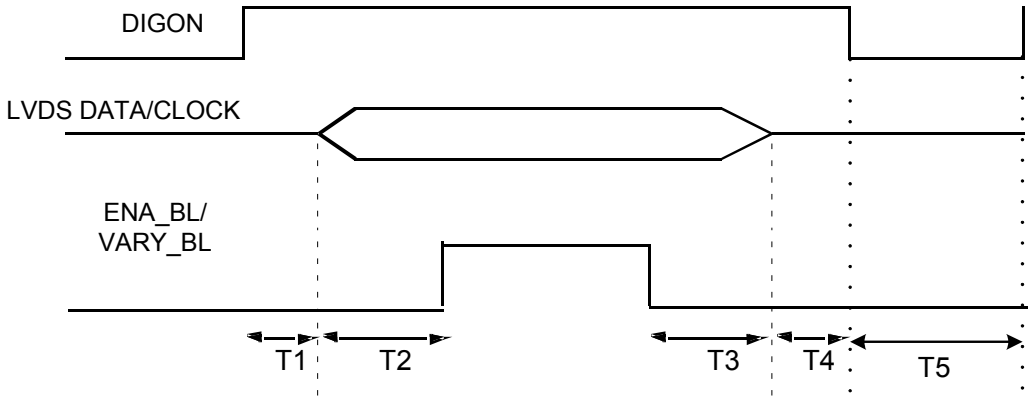


Figure 4-5 LCD Panel Power Up/Down Timing

Note: When ENA_BL is off, VARY_BL is also off. When ENA_BL is on, VARY_BL may toggle depending on programming.

Table 4-5 LCD Power Up/Down Timing

Parameter	Description	Time (ms)
T1	Delay from DIGON active to LVDS data/clock	PWRSEQ_REF * LVTMA_PWRUP_DELAY1
T2	Delay from LVDS data/clock to ENA_BL/VARY_BL active	PWRSEQ_REF * LVTMA_PWRUP_DELAY2
T3	Delay from ENA_BL/VARY_BL inactive to LVDS inactive	PWRSEQ_REF * LVTMA_PWRDN_DELAY1
T4	Delay from LVDS inactive to DIGON inactive	PWRSEQ_REF * LVTMA_PWRDN_DELAY2
T5	Minimum panel off duration (off time is >= T5)	PWRSEQ_REF * LVTMA_PWRDN_MIN_LENGTH

The fields above are in the registers DISPOUT.LVTMA_PWRSEQ_DELAY1 and DISPOUT.LVTMA_PWRSEQ_DELAY2

PWRSEQ_REF = MICROSECOND_REF / (DISPOUT.LVTMA_PWRSEQ_REF_DIV.LVTMA_PWRSEQ_REF_DIV + 1).

MICORSECOND_REF is normally approximately 1 MHz but is programmable.

4.5 LCD Panel Backlight Control with PWM

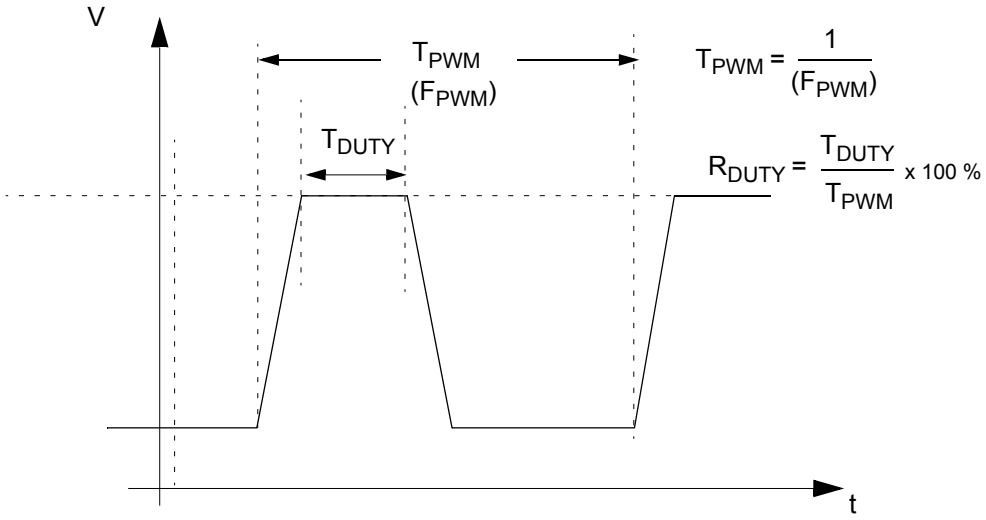


Figure 4-6 Backlight PWM Parameters

Table 4-6 Registers for Setting Backlight PWM Parameters

Register Field	Description
DISPOUT.LVTMA_PWRSEQ_REF_DIV.LVTMA_BL_MOD_REF_DIV	PWM frequency coarse control based on REF frequency.
DISPOUT.LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_EN	Set to 1 to enable PWM
DISPOUT.LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_RES	PWM frequency fine control (also sets number of backlight modulation steps).
DISPOUT.LVTMA_BL_MOD_CNTL.LVTMA_BL_MOD_LEVEL	Controls duty cycle (valid range is 0 .. BL_MOD_RES).

Table 4-7 Backlight PWM Parameters

Parameter	Description	Min	Typ	Max	Unit
REF	xtal_freq **or** xtal_freq * 2	-	27 **or** 54	-	MHz
F_{PWM}	PWM frequency = REF / ((BL_MOD_RES+1) * (BL_MOD_REF_DIV + 1)) Typical Range: 55 Hz to 50 kHz	55	-	50 K	Hz
R_{DUTY}	Duty Ratio = BL_MOD_LEVEL / (BL_MOD_RES+1)	0	-	255 /256*	%

To set the backlight modulation, first select BL_MOD_REF_DIV:

$$BL\_MOD\_REF\_DIV = ceil\ (REF / (256 * F_{TARGET})) - 1$$

Then compute coarse frequency and relative error:

$$F_{INIT} = REF / (256 * (BL\_MOD\_REF\_DIV+1))$$

$$E_{INIT} = (F_{TARGET} - F_{INIT}) / F_{INIT}$$

Finally, compute BL_MOD_RES to correct error:

$$BL\_MOD\_RES = round\ (256 * (1 - E_{INIT})) - 1$$

Notes:

For 50 kHz F_{TARGET}, E_{INIT} should be no more than 0.3, so BL_MOD_RES should be at least 174.

The number of usable backlight modulation steps is BL_MOD_RES+1.

4.6 DVO Timing

Digital interface supports SDR/DDR protocols. The color components and the primary IO's are mapped as follows.

4.6.1 12-bit DDR

This mode supports a clock frequency of up to 220 MHz and a pixel rate of up to 220 M pixels. The relationships between clock, control and data are shown in *Figure 4-7* below. VSYNC is not shown in the diagram as it only indicates horizontal timing.

LS: Least significant bits of the pixel. They are packed as shown in *Table 4-8, "12-bit DDR Interface Timing," on page 4-9*.

MS: Most significant bits of the pixel. They are packed as shown in *Table 4-8, "12-bit DDR Interface Timing," on page 4-9*.

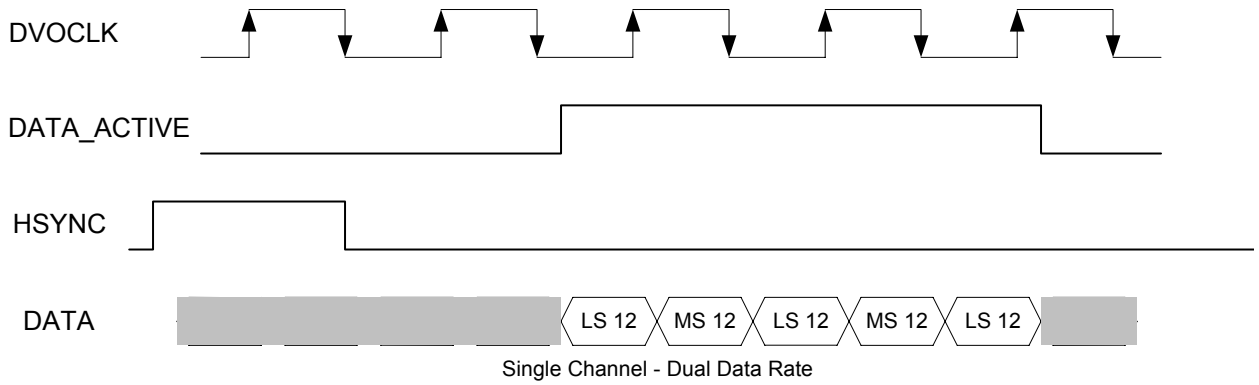


Figure 4-7 12-bit DDR Interface Timing

Table 4-8 12-bit DDR Interface Timing

Primary IO	DVOCLK	Signal Mapping	DVOCLK	Signal Mapping
DVPDATA(11)	Rising edge	G(3)	Falling edge	R(7)
DVPDATA(10)	Rising edge	G(2)	Falling edge	R(6)
DVPDATA(9)	Rising edge	G(1)	Falling edge	R(5)
DVPDATA(8)	Rising edge	G(0)	Falling edge	R(4)
DVPDATA(7)	Rising edge	B(7)	Falling edge	R(3)
DVPDATA(6)	Rising edge	B(6)	Falling edge	R(2)
DVPDATA(5)	Rising edge	B(5)	Falling edge	R(1)
DVPDATA(4)	Rising edge	B(4)	Falling edge	R(0)
DVPDATA(3)	Rising edge	B(3)	Falling edge	G(7)
DVPDATA(2)	Rising edge	B(2)	Falling edge	G(6)
DVPDATA(1)	Rising edge	B(1)	Falling edge	G(5)
DVPDATA(0)	Rising edge	B(0)	Falling edge	G(4)

4.6.2 24-bit SDR

This mode supports 220 M pixels and a clock up to 220 MHz. The relationships between clock, control and data are shown in *Figure 4-8* below. VSYNC is not shown in the diagram as it only indicates horizontal timing.

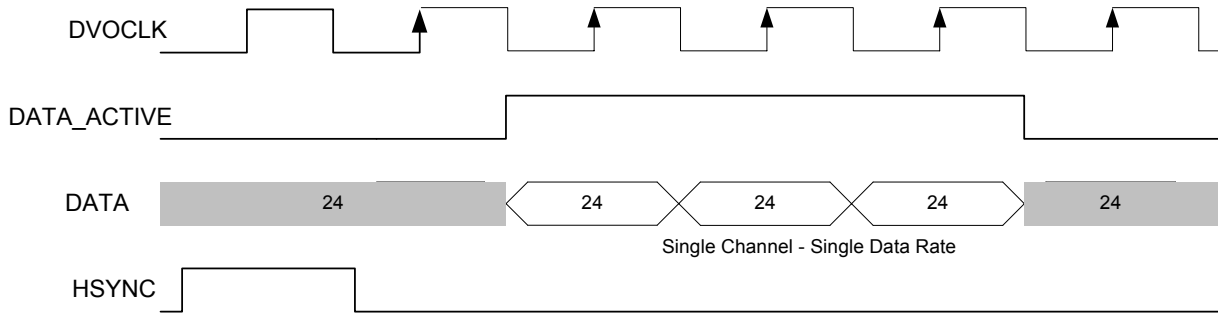


Figure 4-8 24-bit SDR Timing

Table 4-9 24-bit SDR Timing

Primary IO	DVOCLK	Signal Mapping
DVPDATA(23)	Rising edge	R(7)
DVPDATA(22)	Rising edge	R(6)
DVPDATA(21)	Rising edge	R(5)
DVPDATA(20)	Rising edge	R(4)
DVPDATA(19)	Rising edge	R(3)
DVPDATA(18)	Rising edge	R(2)
DVPDATA(17)	Rising edge	R(1)
DVPDATA(16)	Rising edge	R(0)
DVPDATA(15)	Rising edge	G(7)
DVPDATA(14)	Rising edge	G(6)
DVPDATA(13)	Rising edge	G(5)
DVPDATA(12)	Rising edge	G(4)
DVPDATA(11)	Rising edge	G(3)
DVPDATA(10)	Rising edge	G(2)
DVPDATA(9)	Rising edge	G(1)
DVPDATA(8)	Rising edge	G(0)
DVPDATA(7)	Rising edge	B(7)
DVPDATA(6)	Rising edge	B(6)
DVPDATA(5)	Rising edge	B(5)
DVPDATA(4)	Rising edge	B(4)
DVPDATA(3)	Rising edge	B(3)
DVPDATA(2)	Rising edge	B(2)
DVPDATA(1)	Rising edge	B(1)
DVPDATA(0)	Rising edge	B(0)

4.6.3 24-bit DDR

This mode supports a clock frequency of up to 220 MHz, and a data rate of up to 440 M pixels. The relationships between clock, control and data are shown in *Figure 4-9* below. VSYNC is not shown in the diagram as it only indicates horizontal timing. LS = Least significant bits; MS = Most significant bits

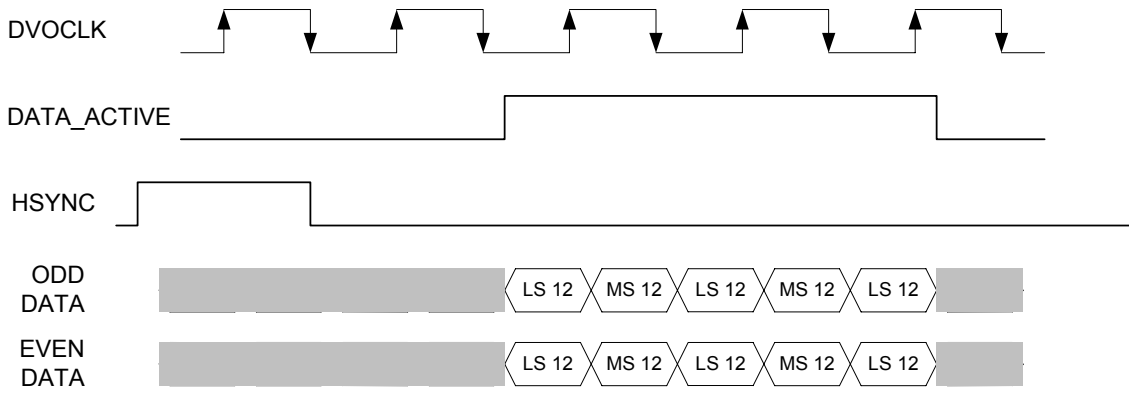


Figure 4-9 24-bit DDR Timing

Table 4-10 24-bit DDR Timing

Primary IO	DVOCLK	Signal Mapping	DVOCLK	Signal Mapping
DVPDATA(23)	Rising edge	ODD_G(3)	Falling edge	ODD_R(7)
DVPDATA(22)	Rising edge	ODD_G(2)	Falling edge	ODD_R(6)
DVPDATA(21)	Rising edge	ODD_G(1)	Falling edge	ODD_R(5)
DVPDATA(20)	Rising edge	ODD_G(0)	Falling edge	ODD_R(4)
DVPDATA(19)	Rising edge	ODD_B(7)	Falling edge	ODD_R(3)
DVPDATA(18)	Rising edge	ODD_B(6)	Falling edge	ODD_R(2)
DVPDATA(17)	Rising edge	ODD_B(5)	Falling edge	ODD_R(1)
DVPDATA(16)	Rising edge	ODD_B(4)	Falling edge	ODD_R(0)
DVPDATA(15)	Rising edge	ODD_B(3)	Falling edge	ODD_G(7)
DVPDATA(14)	Rising edge	ODD_B(2)	Falling edge	ODD_G(6)
DVPDATA(13)	Rising edge	ODD_B(1)	Falling edge	ODD_G(5)
DVPDATA(12)	Rising edge	ODD_B(0)	Falling edge	ODD_G(4)
DVPDATA(11)	Rising edge	EVEN_G(3)	Falling edge	EVEN_R(7)
DVPDATA(10)	Rising edge	EVEN_G(2)	Falling edge	EVEN_R(6)
DVPDATA(9)	Rising edge	EVEN_G(1)	Falling edge	EVEN_R(5)
DVPDATA(8)	Rising edge	EVEN_G(0)	Falling edge	EVEN_R(4)
DVPDATA(7)	Rising edge	EVEN_B(7)	Falling edge	EVEN_R(3)
DVPDATA(6)	Rising edge	EVEN_B(6)	Falling edge	EVEN_R(2)
DVPDATA(5)	Rising edge	EVEN_B(5)	Falling edge	EVEN_R(1)
DVPDATA(4)	Rising edge	EVEN_B(4)	Falling edge	EVEN_R(0)
DVPDATA(3)	Rising edge	EVEN_B(3)	Falling edge	EVEN_G(7)
DVPDATA(2)	Rising edge	EVEN_B(2)	Falling edge	EVEN_G(6)
DVPDATA(1)	Rising edge	EVEN_B(1)	Falling edge	EVEN_G(5)
DVPDATA(0)	Rising edge	EVEN_B(0)	Falling edge	EVEN_G(4)

Chapter 5
Electrical Characteristics

This chapter describes the electrical characteristics of the E4690.

All voltages are with respect to VSS unless specified otherwise.

To link to a topic of interest, use the following list of linked cross references:

"Maximum Rating Conditions" on page 5-2

"Electrical Design Power" on page 5-3

"Power Up/Down Sequence" on page 5-4

"General Interface" on page 5-5

"TTL Interface" on page 5-5

"Memory Interface" on page 5-6

"DDC I2C Mode Electrical Characteristics" on page 5-6

"DisplayPort AUX Electrical Specification" on page 5-7

"DisplayPort Main Link Electrical Specification" on page 5-7

"DAC Characteristics" on page 5-8

5.1 Maximum Rating Conditions

Note: These are stress ratings only, i.e., operation of the device at these conditions is not implied. Ratings are referenced to VDD. Any stress greater than the *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 5-1 Maximum Rating Conditions

Power	Maximum Range
Core Power (VDDC, VDDCI)	0 V to 1.27 V
I/O Power (VDDR3, VDDR4, VDDR5)	0 V to 1.89 V or 0 V to 3.47 V
I/O Level Shift Power (VDD_CT)	0 V to 1.89 V
Memory Power (VDDR1, VDDRHA, VDDRHB)	2.1 V (max)
Engine PLL Power (SPV10)	same as VDDC
PCI Express PLL Power (PCIE_PVDD)	0 V to 1.89 V
PCI Express I/O Power (PCIE_VDDR)	0 V to 1.89 V
PCI Express I/O Power (PCIE_VDDC)	0 V to 1.16 V
Phase Lock Loop Digital Power (DPLL_VDDC)	0 V to 1.16 V
Analog Power (AVDD)	0 V to 1.89 V
Analog Power (DP[F:E]_VDD18, DP[E:A]_PVDD)	0 V to 1.89 V
Analog Power (DPLL_PVDD)	0 V to 1.98 V
Analog Power (DP[F:A]_VDD10)	0 V to 1.16 V
DAC2 Supply (A2VDD)	0 V to 3.7 V
DAC1/DAC2 Digital Supply (VDD1DI/VDD2DI)	0 V to 2.1 V
DC Forward Bias Current	-12 mA (source), +24 mA (sink)

5.2 Electrical Design Power

The following table identifies the estimated peak currents under the conditions identified below. This peak current is intended as a design point; it is not an absolute maximum under all conditions.

To allow for driver optimizations, faster CPUs, and new applications, designers need to provide adequate electrical margin.

Table 5-2 Regulator Guidance

Signal Name	Nominal Voltage	DC Tolerance	AC Tolerance	Maximum RMS Current	Notes
VDDC	1.15 V	± 3%	± 3%	29.5 A	2, 5, 8, 11
VDDCI	1.15 V	± 3%	± 3%	375 mA	
VDDR1+VDDRHA+VDDRHB	1.50 V or 1.80 V	± 5%	± 5%	2.9 A	
VDD_CT	1.80 V	± 5%	± 5%	136 mA	
DP[E:A]_PVDD	1.80 V	± 3%	± 3%	20 mA	6, 9, 10
DP[D:A]_VDD10	1.10 V	± 3%	± 3%	200 mA	6, 9, 10
DP[F:E]_VDD10	1.10 V	± 3%	± 3%	100 mA (LVDS) 170 mA (DisplayPort/TMDS)	6, 9, 10
DP[F:E]_VDD18	1.80 V	± 3%	± 3%	200 mA (LVDS) 110 mA (DisplayPort/TMDS)	6, 9, 10
SPV10	Same as VDDC	± 3%	± 3%	136 mA	4
DPLL_VDDC	1.10 V	± 5%	± 5%	150 mA	5, 9
DPLL_PVDD	1.80 V	± 3%	± 3%	120 mA	5, 9
PCIE_PVDD	1.80 V	± 5%	± 5%	68 mA	9
PCIE_VDDC	1.00 V - 1.10 V	± 5%	± 5%	1.4 A	3, 9
PCIE_VDDR	1.80 V	± 5%	± 5%	210 mA	9
TSVDD	1.80 V	± 5%	± 5%	20 mA	
VDDR3	3.30 V	± 5%	± 5%	60 mA	
VDDR4	1.80 V or 3.30 V	± 5%	± 5%	170 mA	
VDDR5	1.80 V or 3.30 V	± 5%	± 5%	170 mA	
AVDD	1.80 V	± 5%	± 5%	70 mA	
VDD1DI	1.80 V	± 5%	± 5%	45 mA	
A2VDD	3.30 V	± 10%	± 5%	65 mA	7
VDD2DI	1.80 V	± 5%	± 5%	40 mA	
A2VDDQ	1.80 V	± 5%	± 5%	20 mA	

Notes:
1. Maximum RMS current is specified at the maximum nominal voltage (if a range is given), plus the maximum DC tolerance (e.g. 1.10 V +5% for **VDDC**) at 105°C.
2. Maximum RMS current is specified for GDDR3 mode, at 1.5 Gb/s per-pin.
3. Supply noise above 900 kHz must be filtered.
4. SPV10 should track VDDC, and ideally share the same regulator.
5. If a switching regulator is used, the 6 dB bandwidth of the supply filter is required to be at least one (1) decade below the switching frequency of the regulator.
6. AMD generally recommends a set of dedicated decoupling capacitors (values 10 µF, 1 µF, and 100 nF) for this supply, though specific implementations may vary.
7. PAL mode.
8. **VDDC** and **VDDCI** should share a common regulator and common filter network.
9. Must use either a linear supply or switching regulator with a frequency of 300 kHz or less.
10. The current shown is for each of the rails (not all rails combined).
11. Measured at VDDC ±5%.

5.3 Power Up/Down Sequence

An ideal power up/down sequence for E4690 is illustrated as follows.

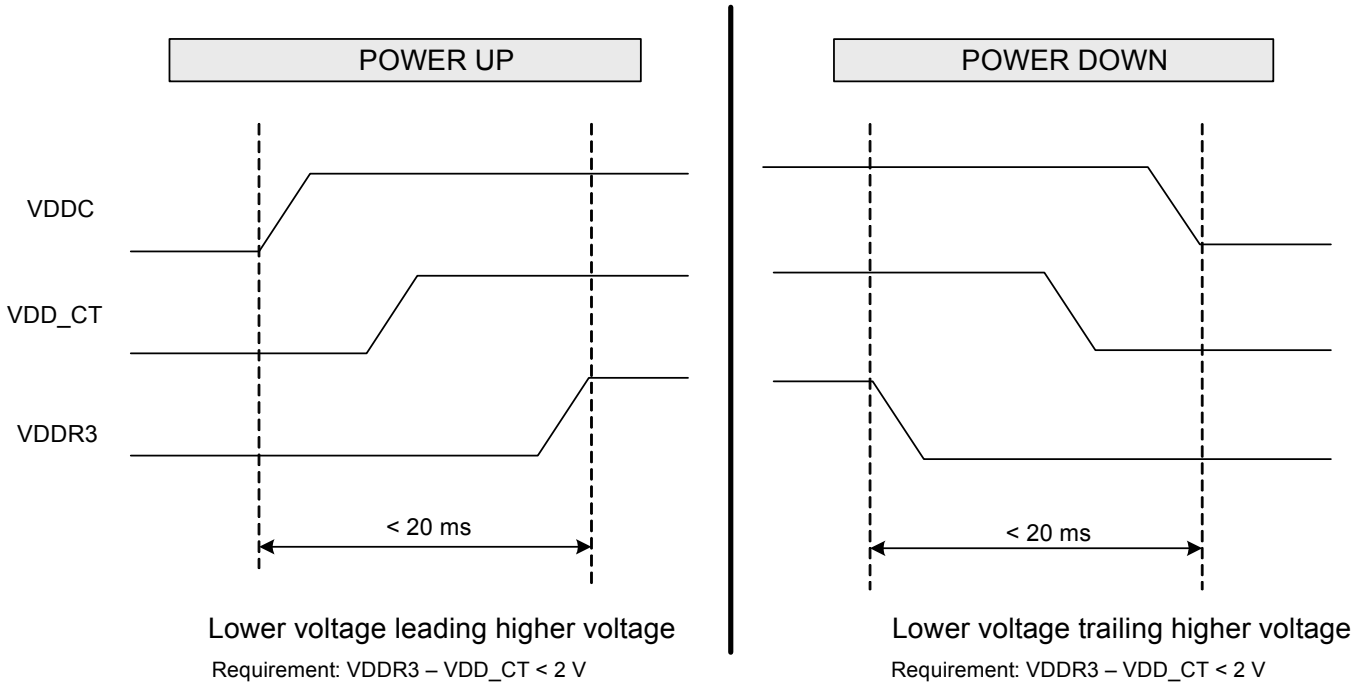


Figure 5-1 Ideal Power Up/Down Sequence

5.3.1 General Guidelines

E4690 has the following requirements with regards to power supply sequencing to avoid damaging the ASIC.

- All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.
- VDDC (including VDDCI and SPV10 should ramp first.
- 1.8-V rails should ramp before the 3.3-V rails. (If 1.8 V does not precede 3.3 V, then a momentary pulse may be observed on the 3.3-V GPIOs (e.g. GPIO_19_CTF).
- Rails of the same nominal voltage level should ramp together if design constraints allow.
- VDDC must ramp before DPx_VDD10, DPx_VDD18 and DPx_PVDD.
- Do not drive any IOs before VDDR3 is ramped up.

Note: For the purpose of sequencing description, VDD_CT is considered to be a 1.8-V nominal rail.

5.3.2 PowerPlay Transitions

- E4690 provides a 1-ms delay (default) between signaling a VDDC transition and raising the clocks. This delay is software programmable.

5.4 General Interface

The table below applies to all signals in the chip.

Table 5-3 General Interface Electrical Characteristics

Parameter	Condition	Min	Typical	Max
IIL - Low Level Input Current	VI = VSS	-	-	-1 µA *
IIH - High Level Input Current	VI = VCC	-	-	+1 µA
IOZ - Tristate Output Leakage	VO = 0 V or VCC	-	-	±1 µA
CIN - Input Capacitance	Freq = 1 MHz @ 0 V	-	4 pF	8 pF
CO - Output Capacitance	Freq = 1 MHz @ 0 V	-	6 pF	-
CIO - Bidirectional I/O Capacitance	Freq = 1 MHz @ 0 V	-	6 pF	8 pF
IKLU - I/O Latch-up Current	V<VSS, V>VCC	200 mA	-	-
VEPO - Electrostatic Protection	C=100 pF R=1.5 kΩ	TBD	-	-

* Current into chip is defined positive.

5.5 TTL Interface

The following tables provide the electrical characteristics of the TTL Interface (GPIOs).

Table 5-4 TTL Interface (GPIOs) for GPIO, and DVP signals

Parameter	Condition	1.8-V GPIO			3.3-V GPIO		
		Min.	Typical	Max.	Min.	Typical	Max.
V_{IL} - Low Level Input Voltage	-	VREFG-50 mV	-	VREFG+50 mV	865 mV	1.08 V	1.155 V
V_{IH} - High Level Input Voltage	-	VREFG-50 mV	-	VREFG+50 mV	1.2 V	-	3.3 V + 10%
V_{OL} - Low Level Output Voltage	@I_{OL} (~ 2 mA) *	-	-	0.4 V	-	-	0.6 V
V_{OH} - High Level Output Voltage	@ 50% I_{OH} (~ 2 mA) *	1.4 V	-	-	2.8 V	-	-
I_{OH}	Output Voltage = V_{OH}	-	-	1 µA	-	-	1 µA
I_{OL}	Output Voltage = V_{OL}	-	-	1 µA	-	-	1 µA
VREFG		-	600 mV	-	-	-	-

* For actual output currents for all voltages refer to the E4690 *ibis model* document

Table 5-5 TTL Interface (GPIOs) for SDA, and SCL

Parameter	Condition	3.3-V GPIO		
		Min.	Typical	Max.
V_{IL} - Low Level Input Voltage	-	-	-	1.5 V
V_{IH} - High Level Input Voltage	-	2.3 V	-	3.3 V + 10%
V_{OL} - Low Level Output Voltage	@I_{OL} (~ 2 mA) *	-	-	0.6 V
V_{OH} - High Level Output Voltage	@ 50% I_{OH} (~ 2 mA) *	2.8 V	-	-
I_{OH}	Output Voltage = V_{OH}	-	-	1 µA
I_{OL}	Output Voltage = V_{OL}	-	-	1 µA
VREFG		-	-	-

* For actual output currents for all voltages refer to the E4690 *ibis model* document

5.6 Memory Interface

The following table provides the electrical characteristics of the memory interface.

Table 5-6 Memory Interface Electrical Characteristics

Parameters	Min	Typical	Max
GDDR3: MVREFSx, MVREFDx - Input reference voltage	0.69 x VDDR1	0.7 x VDDR1	0.71 x VDDR1
V_{TT} - Termination voltage	MVREFDx - 40 mV	MVREFDx	MVREFDx + 40 mV
V_{IH-DC} - DC input logic HIGH	MVREFDx + 150 mV	-	VDDR1
V_{IL-DC} - DC input logic LOW	0	-	MVREFDx - 150 mV
V_{IH-AC} - AC input logic HIGH	MVREFDx + 300 mV	-	-
V_{IL-AC} - AC input logic LOW	-	-	MVREFDx - 300 mV
Delta V_{out1} (7.6 mA x 50 Ω)	380 mV	380 mV	380 mV
Delta V_{out2} (0.38 V + (0.38 V / 2))	570 mV	570 mV	570 mV
Output High Driver (worst case):			
V_{min} at VIN (1.11 V + 350 mV)	1.47 V	1.47 V	1.47 V
V_{min} at VOUT (1.11 V + 0.57 V)	1.69 V	1.69 V	1.69 V
I_{min} output (0.57 V + 0.38 V) / 25 Ω	-7.6 mA	-7.6 mA	-7.6 mA
Max.ON resistor (2.5 V - 1.25 V - 0.57 V) / 7.6 mA	80.26 Ω	89.4 7Ω	98.68 Ω
Output Low Driver (worst case):			
V_{max} at VIN (1.11 V - 0.35 V)	0.77 V	0.90 V	1.03 V
V_{max} at VOUT(1.11 V - 0.57 V)	0.55 V	0.68 V	0.81 V
I_{min} output	7.6 mA	7.6 mA	7.6 mA
Max.ON resistor	72.37 Ω	89.47 Ω	106.58 Ω

Notes:

1. Peak to peak AC noise on MVREFDx/MVREFSx may not exceed ± 25 mV (± 0.2% VREF).

2. VTT of transmitting device must track VREF of receiving device.

3. The 1 V/ns input signal minimum slew rate is to be maintained.

5.7 DDC I2C Mode Electrical Characteristics

The following tables provide the electrical characteristics for the DDCx pins in I2C mode.

Table 5-7 Transmitter Electrical Specification for DDC I2C

Symbol	Description	Min.	Max.	Unit	Notes
I2C_TxFreq	Supported transmit data rate	-	500	kHz	
I2C_V_{OL}	Maximum output low voltage @ I = 3 mA	-	86	mV	2, 3, 4
I2C_V_{OL}	Maximum output low voltage @ I = 8 mA	-	230	mV	2, 3, 4
I2C_V_{OH}	Minimum output high voltage	VDD5-0.25	-	mV	2, 3, 4, 5
I2C_I_{OL}	Minimum output low current @ V = 0.1 V	0.55	6.25	mA	2, 3, 4

Notes:

1. Measured with edge rate of 1 µs at PAD pin.
2. For detailed current/voltage characteristics please refer to IBIS model.
3. Measurement taken with PMOS/NMOS strength set to default values, PVT=Noml Case.
4. I2C interface is open drain circuit, pull high is determined by external power.
5. VDD5 is external pull-up power supply.

Table 5-8 Receiver Electrical Specification for the DDC I2C pins

Symbol	Description	Min.	Max.	Unit	Notes
I2C_Y_VIH-AC	Minimum AC voltage at PAD pin that will produce a stable high at the I2C_Y pin of macro.	2.3		V	3

Table 5-8 Receiver Electrical Specification for the DDC I2C pins

Symbol	Description	Min.	Max.	Unit	Notes
I2C_Y_VIL-AC	Maximum AC voltage at PAD pin that will produce a stable low at the I2C_Y pin of macro.		1.5	V	3
I2C_Y_VIH-DC	Minimum DC voltage at PAD pin that will produce a stable high at the I2C_Y pin of macro.	2.3		V	1
I2C_Y_VIL-DC	Maximum DC voltage at PAD pin that will produce a stable low at the I2C_Y pin of macro.		1.5	V	1
I2C_Y_RxFreq	Supported received frequency.		400	kHz	
$I2C\_Y_{dc}$	I2C_Y output duty cycle	40	60	%	2

Notes:
1. Measured with edge rate of 1 µs at PAD pin.
2. Assuming perfect duty cycle on input.
3. Measured at max operating frequency
4. This specification applies to I2C on the DDCx signals.

5.8 DisplayPort AUX Electrical Specification

This table provides the electrical characteristics of the DisplayPort AUX.

Table 5-9 DisplayPort AUX Electrical Specification

Symbol	Description	Min.	Max.	Unit	Notes
AUX_V_{cm}	Input/output common mode voltage	550	653	mV	
AUX_V_{diff}	Pad differential output swing	593	707	mV	
AUX_TxFreq	Supported transmit data rate	-	20	MHz	
AUX_RxFreq	Supported received frequency	-	20	MHz	
AUX_Pad_{dc}	PADP/N output duty cycle	48	52	%	1

Notes:
1. Assuming 50/50 duty cycle on input.

5.9 DisplayPort Main Link Electrical Specification

Table 5-10 DisplayPort Main Link Electrical Specification

Symbol	Parameter	Min	Typ	Max	Unit	Notes
UI_{HIGH_RATE}	Unit Interval for DP High Bit Rate (2.7 Gbps/lane)	-	370	-	ps	High limit = +300 ppm Low limit = -5300 ppm
UI_{LOW_RATE}	Unit Interval for DP Reduced Bit Rate (1.62 Gbps/lane)	-	617	-	ps	High limit = +300 ppm Low limit = -5300 ppm
$V_{TX\text{-}DIFFp\_p}$	Differential Peak-to-Peak Output Voltage Level	0.34	-	0.92	V	-
$V_{TX\text{-}PREMMP\text{-}RATIO}$	Pre-emphasis Level	0	-	7.2	dB	-

5.10 DAC Characteristics

Table 5-11 DAC Characteristics

Parameter	Min	Typ	Max	Notes
Resolution	10 bits	-	-	a
Maximum PS/2 setting Output Voltage		0.7 V		a, j
Maximum PS/2 setting Output Current		18.7 mA		a, j
Full Scale Error	0	-	-5%/+10%	b,c
DAC to DAC Correlation	-2%	-	+2%	a,d
Differential Linearity	-2 LSB		+2 LSB	a,e
Integral Linearity	-2 LSB	-	+2 LSB	a,e
Rise Time (10% to 90%)	0.58 ns	-	1.7 ns	a,f
Full Scale Settling Time	-	2.5 ns	-	a,g,h
Glitch Energy	-	10 pV-s	-	a,h
Monotonicity	-	-	-	i

Notes:
1. Tested over the operating temperature range, at nominal supply voltage, with an Iref of -1.50 mA. Iref is the level of the current flowing out of the Rset resistor.
2. Tested over the operating temperature range, at reduced supply voltage, with an Iref of -1.50 mA. Iref is the level of the current flowing out of the Rset resistor.
3. Full scale error from manufacturing screening.
4. About the mid point of the distribution of the three DACs measured at full scale deflection.
5. Linearity measured from the best fit line through the DAC characteristics. Monotonicity guaranteed.
6. Load = 37.5 Ω + 20 pF with Iref = -1.50 mA (Iref is the current flowing out of the Rset resistor).
7. Measured from the end of the overshoot to the point where the amplitude of the video ringing is down to +/-5% of the final steady state value
8. This parameter is sampled, not 100% tested.
9. Monotonicity is guaranteed.
10. Levels are 7.8% higher with setup pedestal enabled.

5.10.1 Calculating RSET (CRT DAC Interface)

Note: The following information is for reference purposes only. It is strongly recommended that the values specified in the relevant board design kit be used as is.

A precision resistor (with 1% of nominal) is placed between RSET (or R2SET) and analog ground AVSS (or A2VSS) to set the full-scale DAC current. This required resistor value can be calculated using the formula below.

$$\mathbf{RSET\ (\Omega) = (G \times V_{REF} \times \alpha \times \beta) / I_{OUT}}$$

where:

G =1023/N is the idealized 10-bit gain constant (N is the number of current sources for a particular display mode, see *Table 5-12* and *Table 5-13*)

$\mathbf{V_{REF}}$ is the idealized reference voltage (0.75V for CRT)

α is the systematic **composite** skew on idealized V_{REF} and gain constant, which can be assumed to be 1

β is a scaling factor (1 for RGB)

$\mathbf{I_{OUT} = V_{WHITE} / Z_{EFF}}$ is the required DAC full-scale current. ($\mathbf{Z_{EFF}}$ = 37.5 Ω (double terminated 75 Ω, see figure below))

For values of $\mathbf{V_{REF}}$, $\mathbf{V_{WHITE}}$ and $\mathbf{I_{OUT}}$, see *Table 5-12 and Table 5-13.*

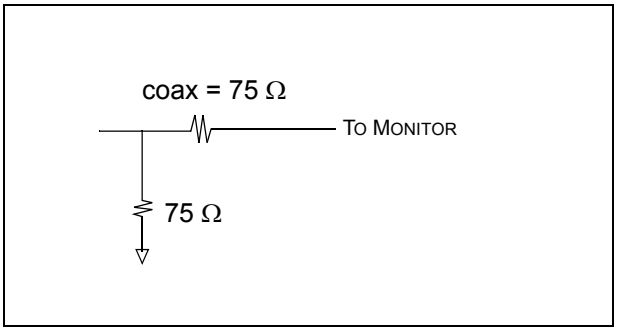


Figure 5-2 Double Termination

Defining RSET (or R2SET) in this fashion allows for a one-time compensation for the systematic skew due to shifts on both V_{REF} and the gain constant on the output white level by adjustment of α.

Table 5-12 CRT DAC (DAC1) Electrical Parameters

Mode	V_{REF} (V)	V_{white} (V)			I_{out} (mA)			N (# of Current Sources)
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PS-2	0.75	0.665	0.700	0.770	-5%	18.66	+10%	82

Calculating RSET for PS-2 Case (N=82)

$$\text{RSET } (\Omega) = (1023/82 \times V_{REF} \times \alpha \times \beta) / I_{OUT}$$
$$= (12.47 \times 0.75 \times 1 \times 1) / 0.0186$$
$$= 503\ \Omega$$

However the closest standard 1% tolerant resistor is **499** Ω.

Table 5-13 DAC (DAC2) Electrical Parameters

Mode	V_{REF} (V)	V_{white} (V)			I_{out} (mA)			N (# of Current Sources)
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PS-2	1.00	0.665	0.700	0.770	-5%	18.66	+10%	76

Calculating R2SET

PS-2 Case (N=76)

$$\text{R2SET } (\Omega) = (1023/76 \times V_{REF} \times \alpha \times \beta) / I_{OUT}$$
$$= (13.46 \times 1 \times 1 \times 1) / 0.0187$$
$$= 719.81\ \Omega$$

However closest standard 1% tolerant resistor is **715** Ω.

5.10.2 Analog Video Levels

Conceptually, each 10-bit DAC can be viewed as two current sources connected in parallel. Each current source is controlled independently as shown below.

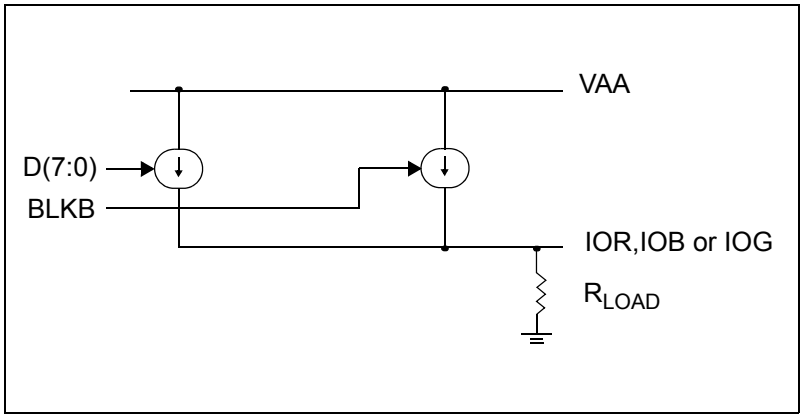


Figure 5-3 Analog Output (DAC)

The following diagrams show video levels for PS/2, NTSC and PAL.

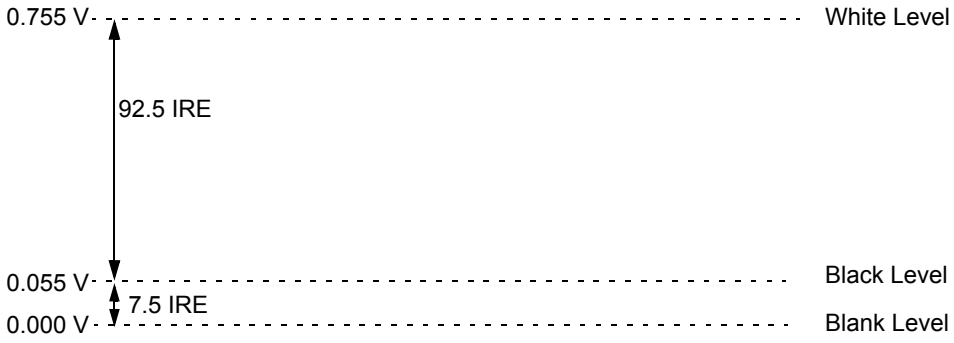


Figure 5-4 PS/2 Video Levels

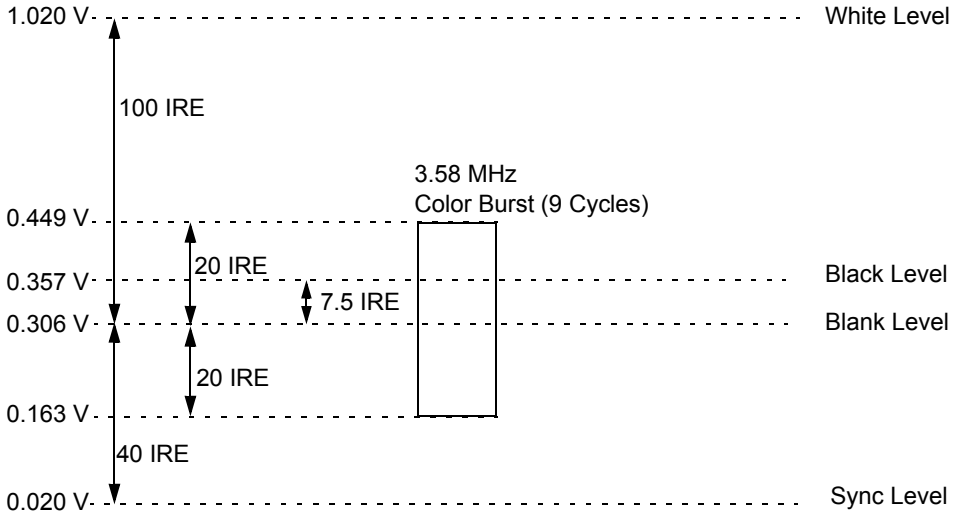


Figure 5-5 NTSC Video Levels

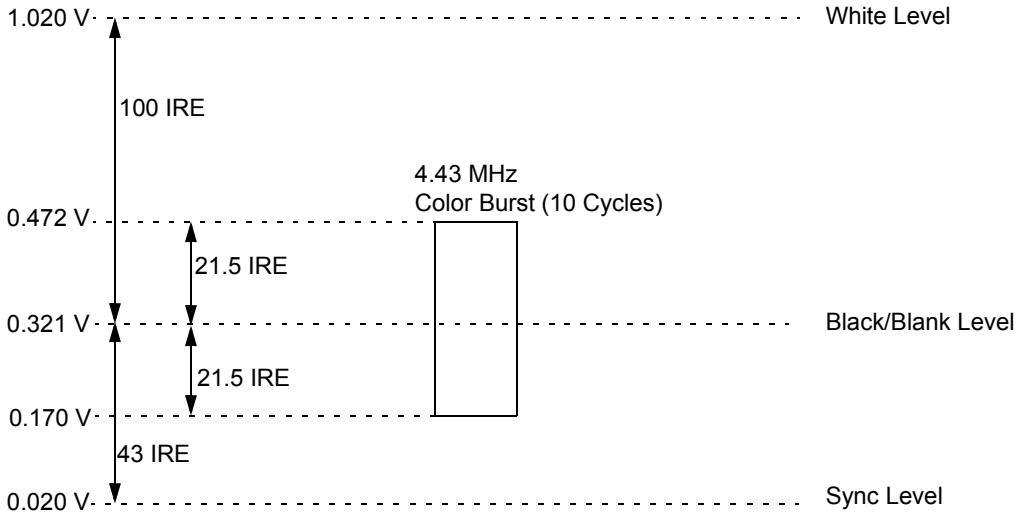


Figure 5-6 PAL Video Levels

Chapter 6
Thermal Data

6.1 Thermal Equations

For the thermal equations, the Delphi Model is recommended.

Notes:

Thermal Simulation Models are available. Please refer to the AMD OEM Resource Center for more information.

6.2 Thermal Design Power (TDP)

The Thermal Design Power is defined as the worst-case power dissipated while running currently available applications at nominal voltages and at the maximum recommended operating temperature (105°C). The TDP is intended as a **recommended design point**; it is **not** an absolute maximum power under all conditions. To allow for driver optimizations, faster CPU's, and new applications, thermal designers need to provide adequate thermal margin.

TDP Conditions / Assumptions

- To account for process variation, measurements are taken on ASICs near the high power limit.
- The TDP is determined with a single display (1600x1200, 32-bpp LVDS).
- The TDP is determined by averaging samples taken every second over a period of approximately 60 seconds.
- The DVO port is assumed to be unused in this typical configuration.

6.2.1 TDP for E4690 Discrete Variants

Table 6-1 TDP for E4690 Discrete Variants

Variant	E4690
VDDC	1.15 V
Engine	600 MHz
Memory	700 MHz
ASIC Leakage	Maximum
ASIC Die Temp	105°C
Memory Interface	128 bits
Driver	8.62
Test Platform	Shiner RS780/SB700 A13, AM2 2 G, DDR2 667 2 G, 1-GB RAM
PCIe Config	x16
TDP-Target *	37.6 W

* Designers should add adequate TDP margin in order to anticipate future changes such as new 3D applications or driver optimizations.

6.3 Thermal Diode Characteristics

E4690 has an on-die thermal diode. Combined with a thermal sensor circuit, the diode temperature (T), and hence the GPU temperature, can be derived from a differential voltage reading (ΔV). The equation relating T to ΔV is given below. (For details on how this equation is derived and how it can be used for measuring temperatures, please refer to published articles on thermal diode usage and/or thermal diode sensor technical specifications.)

$$\Delta V = \frac{\eta \times K \times T \times \ln(N)}{q}$$

where:

ΔV = Difference of two base-to-emitter voltage readings, one using current = I and the other using current = N x I

N = Ratio of the two thermal diode currents (=10 when using an ADI thermal sensor, e.g.: ADM 1020, 1030)

η = Ideality factor of the diode

K = Boltzman's Constant

T = Temperature in Kelvin

q = Electron charge

The series resistance of the thermal diode (R_T) must be taken into account as it introduces an error in the reading (for every Ω, ~ 0.8 degree C is added to the reading). The sensor circuit should be calibrated to offset the R_T induced, plus any other known fixed error.

The on-die thermal diode has the following characteristics:

Table 6-2 E4690 Thermal Diode Characteristics

Parameter	60°C	80°C	100°C	120°C
η	0.976	0.961	0.961	0.970
R_T	12.05	14.69	15.84	16.65

Chapter 7
Mechanical Data

This chapter contains the mechanical drawings for the E4690. To go to a topic of interest, use the following list of linked cross references:

"E4690 Physical Dimensions" on page 7-2

"Pressure Specification" on page 7-5

"Stencil Opening Size for Solderball Pads on PCB" on page 7-5

"FCBGA/PBGA Reference Reflow Profile for RoHS/Lead-free Solder" on page 7-6

7.1 E4690 Physical Dimensions

Package Outline: FCBGA 35 mm x 35 mm - 1066 pins

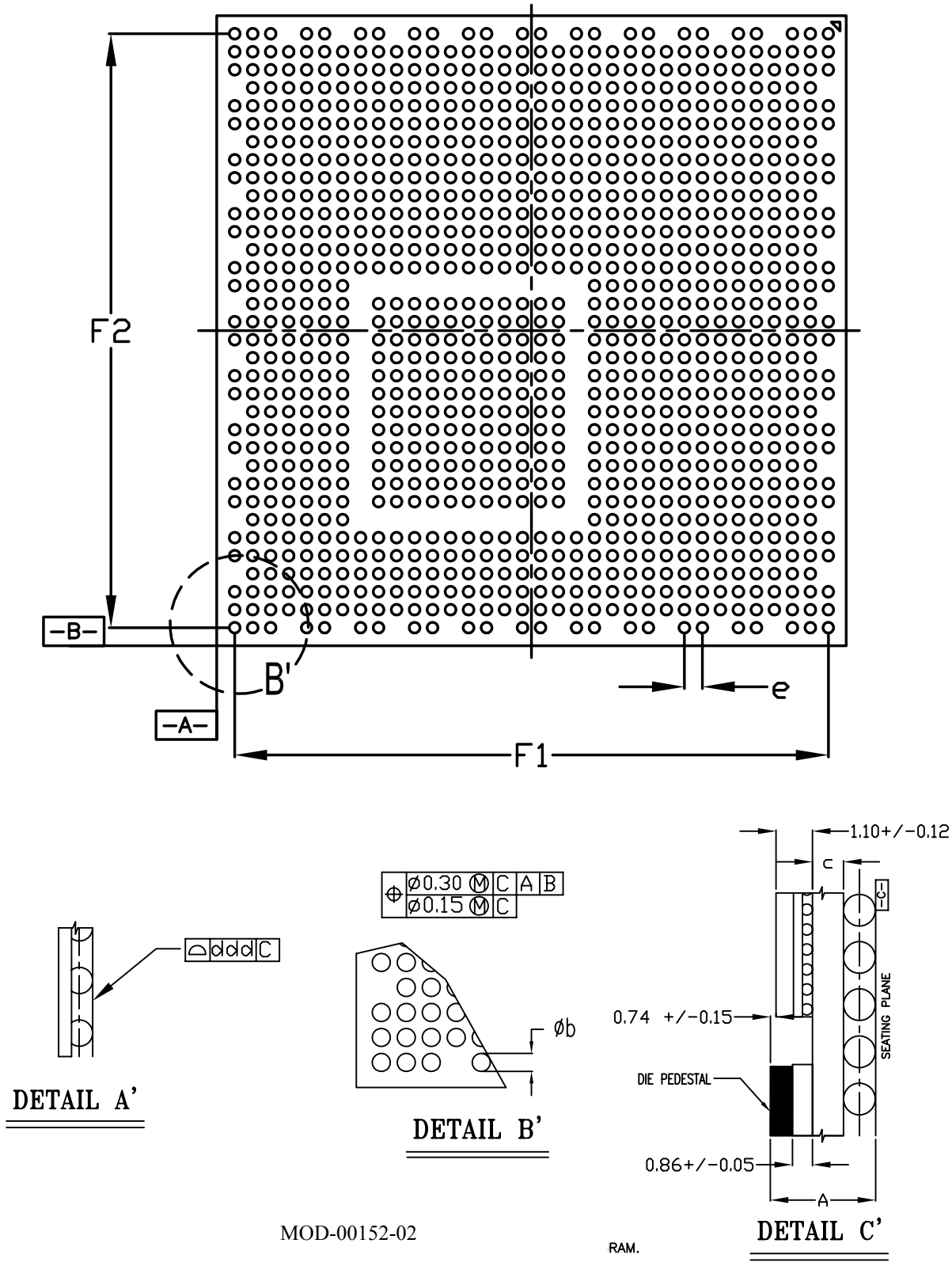


Figure 7-1 E4690 Package Outline - Bottom View

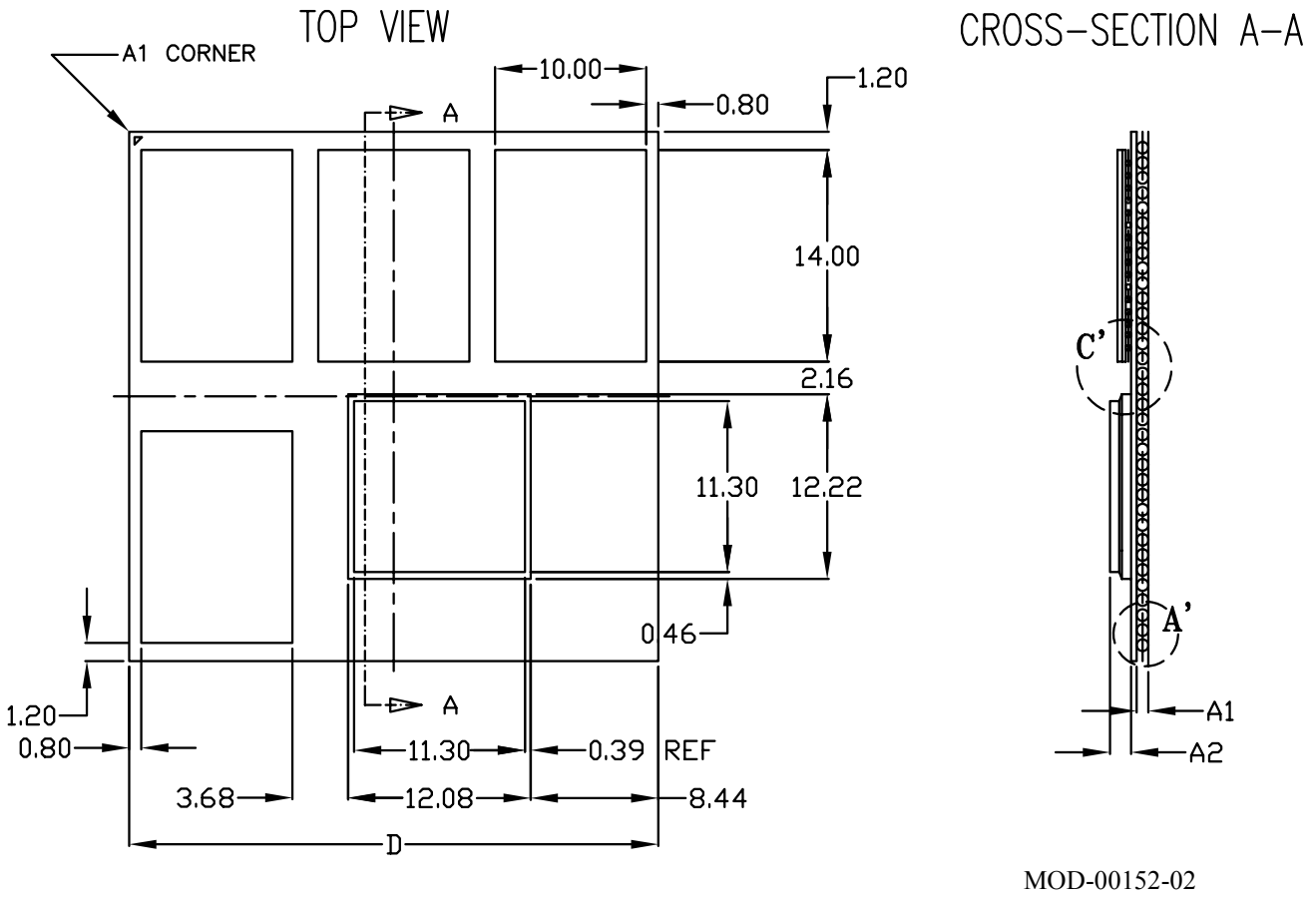
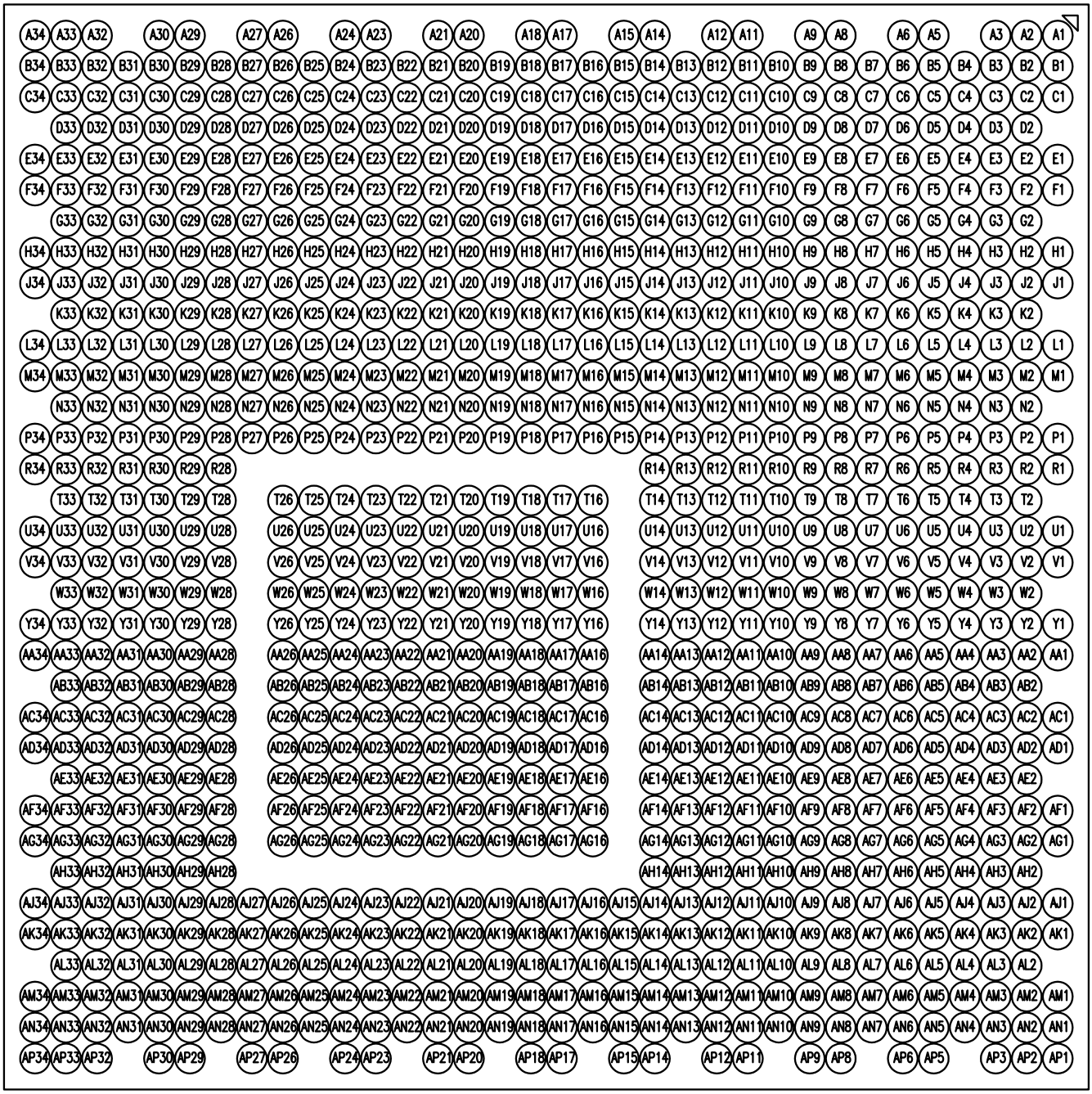


Figure 7-2 E4690 Package Outline - Top View

Table 7-1 E4690 Physical Dimensions (mm)

Ref	Min	Normal	Max
c	1.05	1.15	1.25
A	3.29	3.49	3.69
A1	0.40	0.50	0.60
A2	1.77	1.84	1.91
ϕb	0.50	0.60	0.70
D1	34.80	35.00	35.20
E1	34.80	35.00	35.20
F1	-	33.00	-
F2	-	33.00	-
e	-	1.00 (min pitch)	-
ddd	-	-	0.20



MOD-00152-02

Figure 7-3 E4690 Ball Arrangement

7.2 Pressure Specification

To avoid damage to the ASIC (die or solder ball joint cracks) caused by improper mechanical assembly of the cooling device, follow the recommendations below:

- It is recommended that the maximum pressure which is evenly applied across the contact area between the thermal management device and the die does not exceed 65 PSI. It is important to remind the reader that a contact pressure of 30-40 PSI is adequate to secure the thermal management device and achieve the lowest thermal contact resistance with a temperature drop across the thermal interface material of no more than 3°C. Also, the surface flatness of the metal spreader should be 0.001 inch/1 inch.
- Pre-test the assembly fixture with a strain gauge to make sure that the flexing of the final assembled board and the pressure applying around the ASIC package will not exceed 600 micron strain under any circumstances.
- Ensure that any distortion (bow or twist) of the board after SMT and cooling device assembly is within industry guidelines (IPC/EIA J-STD-001). For measurement method refer to the industry approved technique described in the manual IPC-TM-650, section 2.4.22.

7.3 Board Solder Reflow Process Recommendations

7.3.1 Stencil Opening Size for Solderball Pads on PCB

Warpage of the PCB and the package may cause solderjoint quality issues at the surface mount. Therefore, it is recommended that the stencil opening sizes be adjusted to compensate for the warpage. The recommendation is for the stencil aperture of the solderballs to be kept at the same size as the pads'.

7.3.2 FCBGA/PBGA Reference Reflow Profile for RoHS/Lead-free Solder

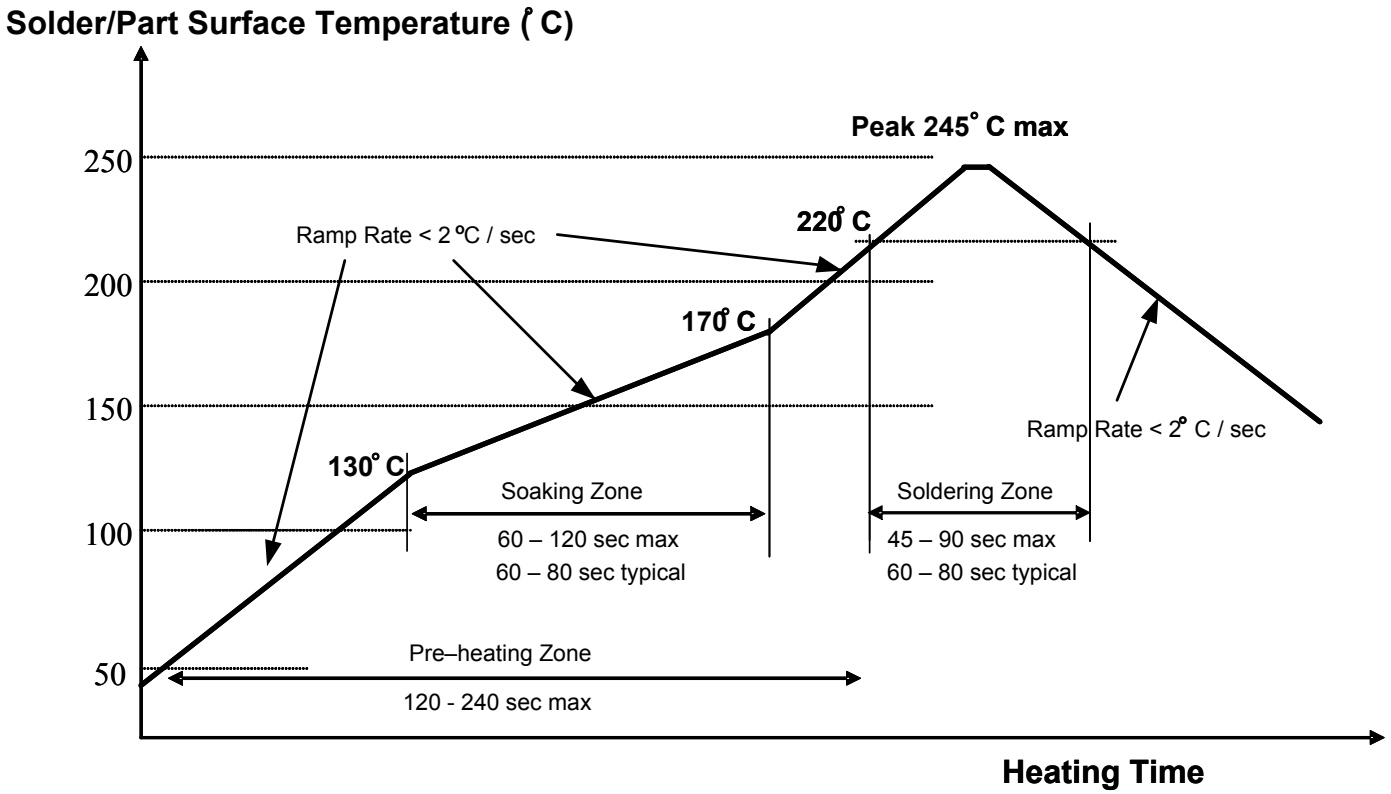


Figure 7-4 FCBGA/PBGA Reference Reflow Profile for RoHS/Lead-Free SMT

Notes when using RoHS/Lead-free solder (SAC105/305/405 Tin-Silver-Cu):

- The final reflow temperature profile will depend on the type of solder paste and chemistry of flux used in the SMT process. Modifications to this reference reflow profile may also be required in order to accommodate the requirements of the other components in the application.
- The use of a reflow oven with 10 heating zones or above is recommended.
- To ensure that the reflow profile meets the target specification on both sides of the board, a different profile board and oven recipe for the first and second reflow may be required.
- Mechanical stiffening can be used to minimize board warpage during reflow.
- It is suggested to decrease temperature cooling rate to minimize board warpage.
- This reflow profile applies only to RoHS/lead-free (high temperature) soldering process and it should not be used for Eutectic solder packages. Damage may result if this condition is violated.
- Maximum 3 reflows are allowed on the same part.

Table 7-2 Recommended Profiling - RoHS/Lead-Free Solder

Profiling Stage	Temperature	Process Range
Overall Preheat	Room temp to 220°C	2 mins to 4 mins
Soaking Time	130 to 170°C	Typical 60 – 80 seconds
Liquidus	220°C	Typical 60 – 80 seconds
Ramp Rate	Ramp up and Cooling	<2°C / second
Peak	Max. 245°C	235°C +/-5°C
Temperature at peak within 5°C	240°C to 245°C	10 – 30 sec

Chapter 8
Boundary Scan Specification

8.1 Introduction

The E4690 has a JTAG 1149.1 compliant TAP controller. The boundary scan implementation is not compliant but allows for some board level connectivity testing. The implementation supports BYPASS, EXTEST, and SAMPLE/PRELOAD instructions. There are 2 sets of TAP ports. Access to each of these ports is described in *"JTAG Interface Signals" on page 8-1*. A BSDL file for each of the modes can be obtained from the AMD OEM Resource Center.

8.2 Boundary Scan

The E4690 boundary scan can perform board level capturing on all pins. While DVO and GPIO pins are voltage programmable (1.8 or 3.3 V), only 3.3-V mode is supported during boundary scan.

8.3 JTAG Interface Signals

8.3.1 JTAG Interface

Table 8-1 JTAG Pins

Pin-name	I/O	Description
JTAG_TCK	I	TCK: Test Clock
JTAG_TMS	I	TMS: Test Mode Select
JTAG_TDI	I	TDI: Test Data In
JTAG_TDO	O	TDO: Test Data Out
JTAG_TRSTB		TRSTb: Test Async Reset
TESTEN	I	Compliand Pin: Set to 1

8.3.2 JTAG Timing Characteristics

Table 8-2 JTAG Timing Characteristics Table

Symbol	Description	Min	Max
f_{cyc}	Frequency of operation	0.001 Mhz	10 Mhz
t_{cyc}	TCLK cycle period	0.10 µs	1000 µs
t_{bsst}	Input data setup time to TCLK rise	15 ns	
t_{bsht}	Input data hold time to TCLK rise	20 ns	
t_{bsdv}	TCLK low to output data valid	0.0 µs	0.05 µs
t_{tcst}	TDI, TMS setup time to TCLK rise	2.5 ns	
t_{tcht}	TDI, TMS hold time to TCLK rise	3.0 ns	
t_{tcdv}	TCLK low to TDO data valid	0.0 µs	0.05 µs

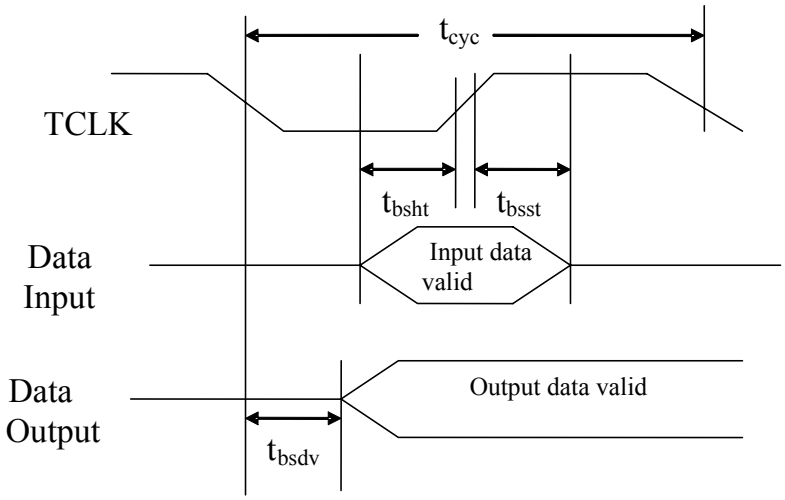


Figure 8-1 Timing of the Boundary Scan Signals with Respect to TCK

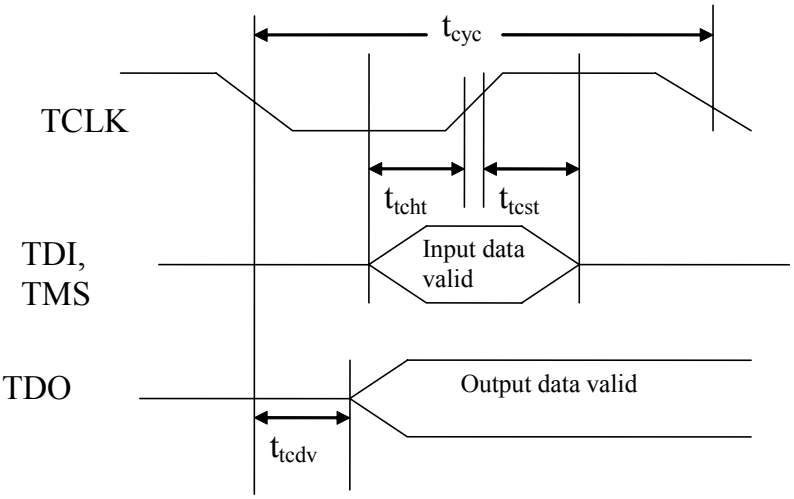


Figure 8-2 Timing of the TAP ports (TDI, TMS, and TDO) with Respect to TCK

8.4 Boundary Scan Thermal Issues

Since all clocks are enabled by default, running boundary scan after power-up without a cooling solution on the device will cause thermal runaway. This will result in unstable or improper operation of the boundary scan control. To prevent over-heating, one or more of the following is recommended:

- Do not provide a clock on the PCIE_REFCLKP/N pins or XTALIN pin.
- Only run boundary scan with a cooling solution on the device (ie- heat sink or fan).

Appendix A
Pin Listings

This appendix contains pin listings for E4690 sorted in two ways. To go to the listing of interest, use the following list of linked cross references:

"E4690 Pins Sorted by Ball Reference" on page -2
"E4690 Pins Sorted by Signal Name" on page -10

A.1 E4690 Pins Sorted by Ball Reference

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
A1	GND
A11	NC
A12	NC
A14	NC
A15	NC
A17	NC
A18	NC
A2	GND
A20	NC
A21	NC
A23	NC
A24	NC
A26	NC
A27	NC
A29	NC
A3	GND
A30	NC
A32	GND
A33	GND
A34	GND
A5	NC
A6	NC
A8	NC
A9	NC
AA1	TXCCP_DPC3P
AA10	GPIO_4_SMBCLK
AA11	GENERICE_HPD4
AA12	GPIO_25_TDI
AA13	NC
AA14	NC
AA16	VDDC
AA17	GND
AA18	VDDC
AA19	GND
AA2	TX0M_DPC2N
AA20	VDDC
AA21	GND
AA22	VDDC
AA23	GND
AA24	VDDC
AA25	GND

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AA26	VDDC
AA28	PCIE_VDDR
AA29	PCIE_TX5N
AA3	DPC_VSSR
AA30	PCIE_VSS
AA31	PCIE_TX6P
AA32	PCIE_VSS
AA33	PCIE_RX5P
AA34	PCIE_RX5N
AA4	NC
AA5	NC
AA6	GND
AA7	VDDR1
AA8	GND
AA9	GND
AB10	SCL
AB11	GPIO_18_HPD3
AB12	GPIO_26_TCK
AB13	NC
AB14	NC
AB16	GND
AB17	VDDC
AB18	GND
AB19	VDDC
AB2	TX0P_DPC2P
AB20	GND
AB21	VDDC
AB22	GND
AB23	VDDC
AB24	GND
AB25	VDDC
AB26	GND
AB28	PCIE_VDDR
AB29	PCIE_TX5P
AB3	DPC_VSSR
AB30	PCIE_TX4N
AB31	PCIE_VSS
AB32	PCIE_VSS
AB33	PCIE_RX4N
AB4	DPC_VDD10
AB5	NC
AB6	GND
AB7	VDDR1
AB8	tp_DQ11_B1
AB9	tp_DQ10_B1

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AC1	TX1P_DPC1P
AC10	SDA
AC11	GPIO_14_HPD2
AC12	GPIO_27_TMS
AC13	NC
AC14	VDDR3
AC16	VDDC
AC17	GND
AC18	VDDC
AC19	GND
AC2	TX1M_DPC1N
AC20	VDDC
AC21	GND
AC22	VDDC
AC23	GND
AC24	VDDC
AC25	GND
AC26	VDDC
AC28	PCIE_VDDR
AC29	PCIE_VSS
AC3	DPC_VSSR
AC30	PCIE_TX4P
AC31	PCIE_TX3N
AC32	PCIE_VSS
AC33	PCIE_RX4P
AC34	PCIE_RX3N
AC4	DPC_VDD10
AC5	NC
AC6	GND
AC7	VDDR1
AC8	tp_RDQS1_B1
AC9	tp_WDQS1_B1
AD1	TX2M_DPC0N
AD10	GPIO_16_SSIN
AD11	HPD1
AD12	GPIO_28_TDO
AD13	NC
AD14	VDDR3
AD16	GND
AD17	VDDC
AD18	GND
AD19	VDDC
AD2	TX2P_DPC0P
AD20	GND
AD21	VDDC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AD22	GND
AD23	VDDC
AD24	GND
AD25	VDDC
AD26	GND
AD28	PCIE_VDDR
AD29	PCIE_TX2N
AD3	DPC_VSSR
AD30	PCIE_VSS
AD31	PCIE_TX3P
AD32	PCIE_VSS
AD33	PCIE_RX2N
AD34	PCIE_RX3P
AD4	tp_CASb_B1
AD5	GND
AD6	GND
AD7	VDDR1
AD8	GND
AD9	GND
AE10	NC
AE11	NC
AE12	NC
AE13	NC
AE14	VDDR3
AE16	VDDC
AE17	GND
AE18	VDDC
AE19	GND
AE2	DDCDATA_AUX4N
AE20	VDDC
AE21	GND
AE22	VDDC
AE23	GND
AE24	VDDC
AE25	GND
AE26	VDDC
AE28	PCIE_VDDR
AE29	PCIE_TX2P
AE3	DPC_VSSR
AE30	PCIE_TX1N
AE31	PCIE_VSS
AE32	PCIE_VSS
AE33	PCIE_RX2P
AE4	DPC_PVSS
AE5	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AE6	GND
AE7	VDDR1
AE8	GND
AE9	tp_BA2_B1
AF1	TXCDM_DPD3N
AF10	VREF2_B1
AF11	NC
AF12	NC
AF13	NC
AF14	VDDR3
AF16	GND
AF17	VDDC
AF18	GND
AF19	VDDC
AF2	DDCCLK_AUX4P
AF20	GND
AF21	VDDC
AF22	GND
AF23	VDDC
AF24	GND
AF25	VDDC
AF26	GND
AF28	PCIE_VDDR
AF29	PCIE_VSS
AF3	DPD_VSSR
AF30	PCIE_TX1P
AF31	PCIE_TX0N
AF32	PCIE_VSS
AF33	PCIE_RX1N
AF34	PCIE_RX1P
AF4	DPC_PVDD
AF5	VREF1_B1
AF6	GND
AF7	VDDR1
AF8	tp_WEb_B1
AF9	GND
AG1	TXCDP_DPD3P
AG10	GND
AG11	NC
AG12	VDDR4
AG13	VDDR4
AG14	NC
AG16	VDDC
AG17	GND
AG18	VDDC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AG19	GND
AG2	TX3M_DPD2N
AG20	VDDC
AG21	GND
AG22	VDDC
AG23	GND
AG24	VDDC
AG25	GND
AG26	VDDC
AG28	PCIE_CALRP
AG29	PCIE_REFCLKN
AG3	DPD_VSSR
AG30	PCIE_VSS
AG31	PCIE_TX0P
AG32	PCIE_VSS
AG33	PCIE_RX0P
AG34	PCIE_RX0N
AG4	DPD_PVDD
AG5	MVDDA1_B1
AG6	NC
AG7	NC
AG8	CLKb_B1
AG9	CLK_B1
AH10	MVDDA2_B1
AH11	NC
AH12	VDDR4
AH13	VDDR4
AH14	NC
AH2	TX3P_DPD2P
AH28	PCIE_CALRN
AH29	PCIE_REFCLKP
AH3	DPD_VSSR
AH30	PCIE_VSS
AH31	PCIE_VSS
AH32	PCIE_VSS
AH33	PCIE_PVDD
AH4	DPD_PVSS
AH5	NC
AH6	NC
AH7	NC
AH8	GND
AH9	GND
AJ1	TX4P_DPD1P
AJ10	NC
AJ11	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AJ12	VDDR5
AJ13	VDDR5
AJ14	VREFG
AJ15	VDDC
AJ16	GND
AJ17	NC
AJ18	NC
AJ19	VDD_CT
AJ2	TX4M_DPD1N
AJ20	VDD_CT
AJ21	NC
AJ22	DMINUS
AJ23	TSVDD
AJ24	TS_FDO
AJ25	NC
AJ26	DPLL_PVDD
AJ27	GND
AJ28	PCIE_VSS
AJ29	PCIE_VSS
AJ3	DPD_VSSR
AJ30	PCIE_VSS
AJ31	PERSTB
AJ32	AVSSQ
AJ33	RB
AJ34	R
AJ4	DPD_VDD10
AJ5	NC
AJ6	NC
AJ7	NC
AJ8	DPCD_CALR
AJ9	DPAB_CALR
AK1	TX5M_DPD0N
AK10	NC
AK11	NC
AK12	VDDR5
AK13	VDDR5
AK14	VDD2DI
AK15	A2VDDQ
AK16	A2VSSQ
AK17	A2VDD
AK18	NC
AK19	VDD_CT
AK2	TX5P_DPD0P
AK20	VDD_CT
AK21	DPEF_CALR

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AK22	DPLUS
AK23	TSVSS
AK24	TESTEN
AK25	DPE_PVSS
AK26	DPLL_PVSS
AK27	DPLL_VDDC
AK28	PCIE_VSS
AK29	PCIE_VSS
AK3	DPD_VSSR
AK30	VSS1DI
AK31	VDD1DI
AK32	AVDD
AK33	GB
AK34	G
AK4	DPD_VDD10
AK5	NC
AK6	NC
AK7	NC
AK8	DPB_PVSS
AK9	NC
AL10	DDC2CLK
AL11	DPB_VDD10
AL12	DPB_VDD10
AL13	NC
AL14	VSS2DI
AL15	COMP
AL16	Y
AL17	R2SET
AL18	V2SYNC
AL19	DDC6DATA
AL2	DDC1CLK
AL20	DDC6CLK
AL21	DPE_VDD10
AL22	DPE_VDD10
AL23	DPE_VDD18
AL24	DPE_VDD18
AL25	DPE_PVDD
AL26	NC
AL27	DPF_VDD18
AL28	DPF_VDD18
AL29	DPF_VDD10
AL3	DPD_VSSR
AL30	DPF_VDD10
AL31	RSET
AL32	BB

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AL33	B
AL4	DPA_VDD10
AL5	DPA_VDD10
AL6	DPA_PVSS
AL7	DPA_PVDD
AL8	DPB_PVDD
AL9	DDC2DATA
AM1	GND
AM10	DPB_VSSR
AM11	DPB_VSSR
AM12	DPB_VSSR
AM13	DPB_VSSR
AM14	DPB_VSSR
AM15	B2B
AM16	G2B
AM17	C
AM18	H2SYNC
AM19	DPE_VSSR
AM2	DDC1DATA
AM20	DPE_VSSR
AM21	DPE_VSSR
AM22	DPE_VSSR
AM23	DPE_VSSR
AM24	DPE_VSSR
AM25	DPF_VSSR
AM26	DPF_VSSR
AM27	DPF_VSSR
AM28	DPF_VSSR
AM29	DPF_VSSR
AM3	DPD_VSSR
AM30	DPF_VSSR
AM31	VSYNC
AM32	XTALOUT
AM33	HSYNC
AM34	GND
AM4	DPA_VSSR
AM5	DPA_VSSR
AM6	DPA_VSSR
AM7	DPA_VSSR
AM8	DPA_VSSR
AM9	DPB_VSSR
AN1	GND
AN10	AUX2P
AN11	TXCBM_DPB3N
AN12	TX3P_DPB2P

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AN13	TX4M_DPB1N
AN14	TX4P_DPB1P
AN15	B2
AN16	G2
AN17	R2B
AN18	DDCCLK_AUX5P
AN19	TXCLK_LN_DPE3N
AN2	GND
AN20	TXCLK_LP_DPE3P
AN21	TXOUT_L1N_DPE1N
AN22	TXOUT_L1P_DPE1P
AN23	TXOUT_L2N_DPE0N
AN24	TXOUT_L3P
AN25	TXCLK_UN_DPF3N
AN26	TXCLK_UP_DPF3P
AN27	TXOUT_U1N_DPF1N
AN28	TXOUT_U1P_DPF1P
AN29	TXOUT_U2N_DPF0N
AN3	AUX1N
AN30	TXOUT_U3P
AN31	DPF_VSSR
AN32	XTALIN
AN33	GND
AN34	GND
AN4	AUX1P
AN5	TXCAM_DPA3N
AN6	TX0P_DPA2P
AN7	TX1M_DPA1N
AN8	TX1P_DPA1P
AN9	AUX2N
AP1	GND
AP11	TXCBP_DPB3P
AP12	TX3M_DPB2N
AP14	TX5M_DPB0N
AP15	TX5P_DPB0P
AP17	R2
AP18	DDCDATA_AUX5N
AP2	GND
AP20	TXOUT_L0N_DPE2N
AP21	TXOUT_L0P_DPE2P
AP23	TXOUT_L2P_DPE0P
AP24	TXOUT_L3N
AP26	TXOUT_U0N_DPF2N
AP27	TXOUT_U0P_DPF2P
AP29	TXOUT_U2P_DPF0P

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
AP3	DPA_VSSR
AP30	TXOUT_U3N
AP32	GND
AP33	GND
AP34	GND
AP5	TXCAP_DPA3P
AP6	TX0M_DPA2N
AP8	TX2M_DPA0N
AP9	TX2P_DPA0P
B1	GND
B10	NC
B11	NC
B12	NC
B13	NC
B14	GND
B15	GND
B16	MZQ_A1
B17	NC
B18	NC
B19	NC
B2	GND
B20	NC
B21	NC
B22	NC
B23	NC
B24	NC
B25	GND
B26	GND
B27	MZQ_A0
B28	NC
B29	NC
B3	NC
B30	NC
B31	NC
B32	NC
B33	GND
B34	GND
B4	MZQ_B0
B5	NC
B6	NC
B7	NC
B8	GND
B9	GND
C1	GND
C10	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
C11	NC
C12	NC
C13	NC
C14	tp_DQ2_A1
C15	tp_DQ3_A1
C16	NC
C17	NC
C18	NC
C19	NC
C2	DVPCLK
C20	NC
C21	NC
C22	NC
C23	NC
C24	NC
C25	tp_DQ2_A0
C26	tp_DQ3_A0
C27	NC
C28	NC
C29	NC
C3	NC
C30	NC
C31	NC
C32	NC
C33	NC
C34	GND
C4	NC
C5	NC
C6	NC
C7	NC
C8	tp_DQ11_B0
C9	tp_DQ10_B0
D10	NC
D11	NC
D12	NC
D13	NC
D14	tp_WDQS1_A1
D15	tp_RDQS1_A1
D16	NC
D17	GND
D18	VDDR1
D19	NC
D2	DVPCNTL_2
D20	NC
D21	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
D22	NC
D23	NC
D24	NC
D25	tp_WDQS1_A0
D26	tp_RDQS1_A0
D27	GND
D28	VDDR1
D29	GND
D3	NC
D30	VDDR1
D31	NC
D32	NC
D33	NC
D4	NC
D5	NC
D6	GND
D7	VDDR1
D8	tp_RDQS1_B0
D9	tp_WDQS1_B0
E1	DVPDATA_1
E10	NC
E11	NC
E12	NC
E13	NC
E14	GND
E15	GND
E16	NC
E17	GND
E18	VDDR1
E19	NC
E2	DVPDATA_0
E20	NC
E21	NC
E22	NC
E23	NC
E24	NC
E25	GND
E26	GND
E27	GND
E28	VDDR1
E29	GND
E3	NC
E30	VDDR1
E31	NC
E32	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
E33	NC
E34	VREF2_A0
E4	GND
E5	NC
E6	GND
E7	VDDR1
E8	GND
E9	GND
F1	DVPDATA_3
F10	NC
F11	NC
F12	NC
F13	NC
F14	NC
F15	NC
F16	tp_CASb_A1
F17	GND
F18	VDDR1
F19	NC
F2	DVPDATA_2
F20	NC
F21	NC
F22	NC
F23	NC
F24	NC
F25	NC
F26	tp_CASb_A0
F27	GND
F28	VDDR1
F29	GND
F3	NC
F30	VDDR1
F31	tp_BA0_A0
F32	GND
F33	GND
F34	MVDDA2_A0
F4	tp_CASb_B0
F5	NC
F6	GND
F7	VDDR1
F8	tp_BA1_B0
F9	GND
G10	VREF2_B0
G11	NC
G12	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
G13	VREF1_A1
G14	NC
G15	NC
G16	tp_BA1_A1
G17	GND
G18	VDDR1
G19	tp_WEb_A1
G2	DVPDATA_5
G20	GND
G21	GND
G22	VREF2_A1
G23	NC
G24	NC
G25	VREF1_A0
G26	NC
G27	GND
G28	VDDR1
G29	GND
G3	DVPDATA_4
G30	VDDR1
G31	tp_WEb_A0
G32	CLKb_A0
G33	CLK_A0
G4	NC
G5	NC
G6	GND
G7	VDDR1
G8	tp_WEb_B0
G9	GND
H1	DVPDATA_7
H10	CLK_B0
H11	NC
H12	NC
H13	NC
H14	NC
H15	NC
H16	NC
H17	GND
H18	VDDR1
H19	NC
H2	DVPDATA_6
H20	CLKb_A1
H21	CLK_A1
H22	NC
H23	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
H24	NC
H25	NC
H26	NC
H27	GND
H28	VDDR1
H29	GND
H3	VREF1_B0
H30	VDDR1
H31	NC
H32	PCIE_VSS
H33	PCIE_VSS
H34	PCIE_VSS
H4	NC
H5	NC
H6	GND
H7	VDDR1
H8	NC
H9	CLKb_B0
J1	DVPDATA_9
J10	MVDDA2_B0
J11	NC
J12	NC
J13	MVDDA1_A1
J14	NC
J15	NC
J16	NC
J17	GND
J18	VDDR1
J19	NC
J2	DVPDATA_8
J20	GND
J21	GND
J22	MVDDA2_A1
J23	NC
J24	NC
J25	MVDDA1_A0
J26	NC
J27	NC
J28	NC
J29	NC
J3	MVDDA1_B0
J30	NC
J31	NC
J32	PCIE_VSS
J33	PCIE_RX15P

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
J34	PCIE_RX15N
J4	NC
J5	NC
J6	GND
J7	VDDR1
J8	NC
J9	GND
K10	NC
K11	NC
K12	NC
K13	NC
K14	NC
K15	NC
K16	NC
K17	GND
K18	VDDR1
K19	NC
K2	DVPDATA_11
K20	NC
K21	NC
K22	NC
K23	NC
K24	NC
K25	NC
K26	NC
K27	NC
K28	PCIE_VDDC
K29	PCIE_VDDC
K3	DVPDATA_10
K30	PCIE_VDDC
K31	PCIE_VDDC
K32	PCIE_VSS
K33	PCIE_RX14N
K4	NC
K5	NC
K6	GND
K7	VDDR1
K8	NC
K9	NC
L1	DVPCNTL_1
L10	GPIO_10_ROMSCK
L11	GPIO_5_AC_BATT
L12	GPIO_15_PWRCNTL_0
L13	GPIO_21
L14	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
L15	NC
L16	NC
L17	GND
L18	VDDR1
L19	NC
L2	DVPCNTL_0
L20	NC
L21	NC
L22	NC
L23	NC
L24	NC
L25	NC
L26	NC
L27	NC
L28	PCIE_VDDC
L29	PCIE_VSS
L3	NC
L30	PCIE_VSS
L31	PCIE_TX15N
L32	PCIE_VSS
L33	PCIE_RX14P
L34	PCIE_RX13N
L4	NC
L5	NC
L6	GND
L7	VDDR1
L8	GPIO_7_BLON
L9	GPIO_8_ROMSO
M1	DVPCNTL_MVP_0
M10	GPIO_22_ROMCSB
M11	GPIO_20_PWRCNTL_1
M12	GPIO_23_CLKREQB
M13	NC
M14	NC
M15	NC
M16	NC
M17	GND
M18	VDDR1
M19	NC
M2	DVPCNTL_MVP_1
M20	NC
M21	NC
M22	NC
M23	NC
M24	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
M25	NC
M26	NC
M27	NC
M28	PCIE_VDDC
M29	PCIE_TX14N
M3	NC
M30	PCIE_VSS
M31	PCIE_TX15P
M32	PCIE_VSS
M33	PCIE_RX12N
M34	PCIE_RX13P
M4	NC
M5	NC
M6	GND
M7	VDDR1
M8	VARY_BL
M9	GPIO_9_ROMSI
N10	NC
N11	NC
N12	NC
N13	NC
N14	NC
N15	NC
N16	NC
N17	GND
N18	VDDR1
N19	NC
N2	DVPDATA_13
N20	NC
N21	NC
N22	NC
N23	NC
N24	NC
N25	NC
N26	NC
N27	NC
N28	PCIE_VDDC
N29	PCIE_TX14P
N3	DVPDATA_12
N30	PCIE_TX13N
N31	PCIE_VSS
N32	PCIE_VSS
N33	PCIE_RX12P
N4	NC
N5	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
N6	GND
N7	VDDR1
N8	DIGON
N9	NC
P1	DVPDATA_15
P10	GPIO_0
P11	NC
P12	NC
P13	DRAM_RST
P14	MEM_CALRP1
P15	MVREFSB
P16	MVREFDB
P17	VSSRHB
P18	VDDRHB
P19	NC
P2	DVPDATA_14
P20	VDDCI
P21	VDDCI
P22	VDDCI
P23	VDDCI
P24	MVREFDA
P25	MVREFSA
P26	VSSRHA
P27	VDDRHA
P28	PCIE_VDDC
P29	PCIE_VSS
P3	NC
P30	PCIE_TX13P
P31	PCIE_TX12N
P32	PCIE_VSS
P33	PCIE_RX11N
P34	PCIE_RX11P
P4	NC
P5	NC
P6	NC
P7	NC
P8	NC
P9	GENERICA
R1	DVPDATA_17
R10	GPIO_1
R11	NC
R12	NC
R13	CLKTESTA
R14	NC
R2	DVPDATA_16

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
R28	PCIE_VDDC
R29	PCIE_TX11N
R3	NC
R30	PCIE_VSS
R31	PCIE_TX12P
R32	PCIE_VSS
R33	PCIE_RX10P
R34	PCIE_RX10N
R4	NC
R5	NC
R6	NC
R7	NC
R8	NC
R9	GENERICB
T10	GPIO_11
T11	NC
T12	NC
T13	CLKTESTB
T14	NC
T16	GND
T17	VDDC
T18	GND
T19	VDDC
T2	DVPDATA_19
T20	GND
T21	VDDC
T22	GND
T23	VDDC
T24	GND
T25	VDDC
T26	GND
T28	PCIE_VDDC
T29	PCIE_TX11P
T3	DVPDATA_18
T30	PCIE_TX10N
T31	PCIE_VSS
T32	PCIE_VSS
T33	PCIE_RX9N
T4	NC
T5	NC
T6	NC
T7	NC
T8	NC
T9	GENERICC
U1	DVPDATA_21

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
U10	GPIO_12
U11	NC
U12	NC
U13	SPVSS
U14	NC
U16	VDDC
U17	GND
U18	VDDC
U19	GND
U2	DVPDATA_20
U20	VDDC
U21	GND
U22	VDDC
U23	GND
U24	VDDC
U25	GND
U26	VDDC
U28	PCIE_VDDC
U29	PCIE_VSS
U3	NC
U30	PCIE_TX10P
U31	PCIE_TX9N
U32	PCIE_VSS
U33	PCIE_RX9P
U34	PCIE_RX8N
U4	NC
U5	NC
U6	GND
U7	VDDR1
U8	NC
U9	GENERICD
V1	DVPDATA_23
V10	GPIO_13
V11	GPIO_17_THERMAL_IN T
V12	GPIO_29
V13	SPV10
V14	NC
V16	GND
V17	VDDC
V18	GND
V19	VDDC
V2	DVPDATA_22
V20	GND
V21	VDDC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
V22	GND
V23	VDDC
V24	GND
V25	VDDC
V26	GND
V28	PCIE_VDDC
V29	PCIE_TX8N
V3	NC
V30	PCIE_VSS
V31	PCIE_TX9P
V32	PCIE_VSS
V33	PCIE_RX7N
V34	PCIE_RX8P
V4	NC
V5	NC
V6	GND
V7	VDDR1
V8	NC
V9	GENERICF
W10	GPIO_2
W11	GPIO_19_CTF
W12	GPIO_30
W13	NC
W14	NC
W16	VDDC
W17	GND
W18	VDDC
W19	GND
W2	DDCDATA_AUX3N
W20	VDDC
W21	GND
W22	VDDC
W23	GND
W24	VDDC
W25	GND
W26	VDDC
W28	PCIE_VDDR
W29	PCIE_TX8P
W3	NC
W30	PCIE_TX7N
W31	PCIE_VSS
W32	PCIE_VSS
W33	PCIE_RX7P
W4	NC
W5	NC

Table A-1 E4690 Pins Sorted by Ball Reference

Ball Reference	Signal Name
W6	GND
W7	VDDR1
W8	NC
W9	GENERICG
Y1	TXCCM_DPC3N
Y10	GPIO_3_SMBDATA
Y11	GPIO_6_TACH
Y12	GPIO_24_TRSTB
Y13	NC
Y14	NC
Y16	GND
Y17	VDDC
Y18	GND
Y19	VDDC
Y2	DDCCLK_AUX3P
Y20	GND
Y21	VDDC
Y22	GND
Y23	VDDC
Y24	GND
Y25	VDDC
Y26	GND
Y28	PCIE_VDDR
Y29	PCIE_VSS
Y3	DPC_VSSR
Y30	PCIE_TX7P
Y31	PCIE_TX6N
Y32	PCIE_VSS
Y33	PCIE_RX6N
Y34	PCIE_RX6P
Y4	NC
Y5	MZQ_B1
Y6	GND
Y7	VDDR1
Y8	NC
Y9	NC

A.2 E4690 Pins Sorted by Signal Name

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
AK17	A2VDD
AK15	A2VDDQ
AK16	A2VSSQ
AN3	AUX1N
AN4	AUX1P
AN9	AUX2N
AN10	AUX2P
AK32	AVDD
AJ32	AVSSQ
AL33	B
AN15	B2
AM15	B2B
AL32	BB
AM17	C
G33	CLK_A0
H21	CLK_A1
H10	CLK_B0
AG9	CLK_B1
G32	CLKb_A0
H20	CLKb_A1
H9	CLKb_B0
AG8	CLKb_B1
R13	CLKTESTA
T13	CLKTESTB
AL15	COMP
AL2	DDC1CLK
AM2	DDC1DATA
AL10	DDC2CLK
AL9	DDC2DATA
AL20	DDC6CLK
AL19	DDC6DATA
Y2	DDCCLK_AUX3P
AF2	DDCCLK_AUX4P
AN18	DDCCLK_AUX5P
W2	DDCDATA_AUX3N
AE2	DDCDATA_AUX4N
AP18	DDCDATA_AUX5N
N8	DIGON
AJ22	DMINUS
AL7	DPA_PVDD
AL6	DPA_PVSS

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
AL4	DPA_VDD10
AL5	DPA_VDD10
AM4	DPA_VSSR
AM5	DPA_VSSR
AM6	DPA_VSSR
AM7	DPA_VSSR
AM8	DPA_VSSR
AP3	DPA_VSSR
AJ9	DPAB_CALR
AL8	DPB_PVDD
AK8	DPB_PVSS
AL11	DPB_VDD10
AL12	DPB_VDD10
AM10	DPB_VSSR
AM11	DPB_VSSR
AM12	DPB_VSSR
AM13	DPB_VSSR
AM14	DPB_VSSR
AM9	DPB_VSSR
AF4	DPC_PVDD
AE4	DPC_PVSS
AB4	DPC_VDD10
AC4	DPC_VDD10
AA3	DPC_VSSR
AB3	DPC_VSSR
AC3	DPC_VSSR
AD3	DPC_VSSR
AE3	DPC_VSSR
Y3	DPC_VSSR
AJ8	DPCD_CALR
AG4	DPD_PVDD
AH4	DPD_PVSS
AJ4	DPD_VDD10
AK4	DPD_VDD10
AF3	DPD_VSSR
AG3	DPD_VSSR
AH3	DPD_VSSR
AJ3	DPD_VSSR
AK3	DPD_VSSR
AL3	DPD_VSSR
AM3	DPD_VSSR
AL25	DPE_PVDD
AK25	DPE_PVSS
AL21	DPE_VDD10
AL22	DPE_VDD10

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
AL23	DPE_VDD18
AL24	DPE_VDD18
AM19	DPE_VSSR
AM20	DPE_VSSR
AM21	DPE_VSSR
AM22	DPE_VSSR
AM23	DPE_VSSR
AM24	DPE_VSSR
AK21	DPEF_CALR
AL29	DPF_VDD10
AL30	DPF_VDD10
AL27	DPF_VDD18
AL28	DPF_VDD18
AM25	DPF_VSSR
AM26	DPF_VSSR
AM27	DPF_VSSR
AM28	DPF_VSSR
AM29	DPF_VSSR
AM30	DPF_VSSR
AN31	DPF_VSSR
AJ26	DPLL_PVDD
AK26	DPLL_PVSS
AK27	DPLL_VDDC
AK22	DPLUS
P13	DRAM_RST
C2	DVPCLK
L2	DVPCNTL_0
L1	DVPCNTL_1
D2	DVPCNTL_2
M1	DVPCNTL_MVP_0
M2	DVPCNTL_MVP_1
E2	DVPDATA_0
E1	DVPDATA_1
K3	DVPDATA_10
K2	DVPDATA_11
N3	DVPDATA_12
N2	DVPDATA_13
P2	DVPDATA_14
P1	DVPDATA_15
R2	DVPDATA_16
R1	DVPDATA_17
T3	DVPDATA_18
T2	DVPDATA_19
F2	DVPDATA_2
U2	DVPDATA_20

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
U1	DVPDATA_21
V2	DVPDATA_22
V1	DVPDATA_23
F1	DVPDATA_3
G3	DVPDATA_4
G2	DVPDATA_5
H2	DVPDATA_6
H1	DVPDATA_7
J2	DVPDATA_8
J1	DVPDATA_9
AK34	G
AN16	G2
AM16	G2B
AK33	GB
P9	GENERICA
R9	GENERICB
T9	GENERICC
U9	GENERICD
AA11	GENERICE_HPD4
V9	GENERICF
W9	GENERICG
AJ16	GND
A1	GND
A2	GND
A3	GND
A32	GND
A33	GND
A34	GND
AA17	GND
AA19	GND
AA21	GND
AA23	GND
AA25	GND
AA6	GND
AA8	GND
AA9	GND
AB16	GND
AB18	GND
AB20	GND
AB22	GND
AB24	GND
AB26	GND
AB6	GND
AC17	GND
AC19	GND

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
AC21	GND
AC23	GND
AC25	GND
AC6	GND
AD16	GND
AD18	GND
AD20	GND
AD22	GND
AD24	GND
AD26	GND
AD5	GND
AD6	GND
AD8	GND
AD9	GND
AE17	GND
AE19	GND
AE21	GND
AE23	GND
AE25	GND
AE6	GND
AE8	GND
AF16	GND
AF18	GND
AF20	GND
AF22	GND
AF24	GND
AF26	GND
AF6	GND
AF9	GND
AG10	GND
AG17	GND
AG19	GND
AG21	GND
AG23	GND
AG25	GND
AH8	GND
AH9	GND
AJ27	GND
AM1	GND
AM34	GND
AN1	GND
AN2	GND
AN33	GND
AN34	GND
AP1	GND

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
AP2	GND
AP32	GND
AP33	GND
AP34	GND
B1	GND
B14	GND
B15	GND
B2	GND
B25	GND
B26	GND
B33	GND
B34	GND
B8	GND
B9	GND
C1	GND
C34	GND
D17	GND
D27	GND
D29	GND
D6	GND
E14	GND
E15	GND
E17	GND
E25	GND
E26	GND
E27	GND
E29	GND
E4	GND
E6	GND
E8	GND
E9	GND
F17	GND
F27	GND
F29	GND
F32	GND
F33	GND
F6	GND
F9	GND
G17	GND
G20	GND
G21	GND
G27	GND
G29	GND
G6	GND
G9	GND

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
H17	GND
H27	GND
H29	GND
H6	GND
J17	GND
J20	GND
J21	GND
J6	GND
J9	GND
K17	GND
K6	GND
L17	GND
L6	GND
M17	GND
M6	GND
N17	GND
N6	GND
T16	GND
T18	GND
T20	GND
T22	GND
T24	GND
T26	GND
U17	GND
U19	GND
U21	GND
U23	GND
U25	GND
U6	GND
V16	GND
V18	GND
V20	GND
V22	GND
V24	GND
V26	GND
V6	GND
W17	GND
W19	GND
W21	GND
W23	GND
W25	GND
W6	GND
Y16	GND
Y18	GND
Y20	GND

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
Y22	GND
Y24	GND
Y26	GND
Y6	GND
P10	GPIO_0
R10	GPIO_1
L10	GPIO_10_ROMSCK
T10	GPIO_11
U10	GPIO_12
V10	GPIO_13
AC11	GPIO_14_HPD2
L12	GPIO_15_PWRCNTL_0
AD10	GPIO_16_SSIN
V11	GPIO_17_THERMAL_IN T
AB11	GPIO_18_HPD3
W11	GPIO_19_CTF
W10	GPIO_2
M11	GPIO_20_PWRCNTL_1
L13	GPIO_21
M10	GPIO_22_ROMCSB
M12	GPIO_23_CLKREQB
Y12	GPIO_24_TRSTB
AA12	GPIO_25_TDI
AB12	GPIO_26_TCK
AC12	GPIO_27_TMS
AD12	GPIO_28_TDO
V12	GPIO_29
Y10	GPIO_3_SMBDATA
W12	GPIO_30
AA10	GPIO_4_SMBCLK
L11	GPIO_5_AC_BATT
Y11	GPIO_6_TACH
L8	GPIO_7_BLON
L9	GPIO_8_ROMSO
M9	GPIO_9_ROMSI
AM18	H2SYNC
AD11	HPD1
AM33	HSYNC
P14	MEM_CALRP1
J25	MVDDA1_A0
J13	MVDDA1_A1
J3	MVDDA1_B0
AG5	MVDDA1_B1
F34	MVDDA2_A0

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
J22	MVDDA2_A1
J10	MVDDA2_B0
AH10	MVDDA2_B1
P24	MVREFDA
P16	MVREFDB
P25	MVREFSA
P15	MVREFSB
B27	MZQ_A0
B16	MZQ_A1
B4	MZQ_B0
Y5	MZQ_B1
A11	NC
A12	NC
A14	NC
A15	NC
A17	NC
A18	NC
A20	NC
A21	NC
A23	NC
A24	NC
A26	NC
A27	NC
A29	NC
A30	NC
A5	NC
A6	NC
A8	NC
A9	NC
AA13	NC
AA14	NC
AA4	NC
AA5	NC
AB13	NC
AB14	NC
AB5	NC
AC13	NC
AC5	NC
AD13	NC
AE10	NC
AE11	NC
AE12	NC
AE13	NC
AE5	NC
AF11	NC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
AF12	NC
AF13	NC
AG11	NC
AG14	NC
AG6	NC
AG7	NC
AH11	NC
AH14	NC
AH5	NC
AH6	NC
AH7	NC
AJ10	NC
AJ11	NC
AJ17	NC
AJ18	NC
AJ21	NC
AJ25	NC
AJ5	NC
AJ6	NC
AJ7	NC
AK10	NC
AK11	NC
AK18	NC
AK5	NC
AK6	NC
AK7	NC
AK9	NC
AL13	NC
AL26	NC
B10	NC
B11	NC
B12	NC
B13	NC
B17	NC
B18	NC
B19	NC
B20	NC
B21	NC
B22	NC
B23	NC
B24	NC
B28	NC
B29	NC
B3	NC
B30	NC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
B31	NC
B32	NC
B5	NC
B6	NC
B7	NC
C10	NC
C11	NC
C12	NC
C13	NC
C16	NC
C17	NC
C18	NC
C19	NC
C20	NC
C21	NC
C22	NC
C23	NC
C24	NC
C27	NC
C28	NC
C29	NC
C3	NC
C30	NC
C31	NC
C32	NC
C33	NC
C4	NC
C5	NC
C6	NC
C7	NC
D10	NC
D11	NC
D12	NC
D13	NC
D16	NC
D19	NC
D20	NC
D21	NC
D22	NC
D23	NC
D24	NC
D3	NC
D31	NC
D32	NC
D33	NC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
D4	NC
D5	NC
E10	NC
E11	NC
E12	NC
E13	NC
E16	NC
E19	NC
E20	NC
E21	NC
E22	NC
E23	NC
E24	NC
E3	NC
E31	NC
E32	NC
E33	NC
E5	NC
F10	NC
F11	NC
F12	NC
F13	NC
F14	NC
F15	NC
F19	NC
F20	NC
F21	NC
F22	NC
F23	NC
F24	NC
F25	NC
F3	NC
F5	NC
G11	NC
G12	NC
G14	NC
G15	NC
G23	NC
G24	NC
G26	NC
G4	NC
G5	NC
H11	NC
H12	NC
H13	NC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
H14	NC
H15	NC
H16	NC
H19	NC
H22	NC
H23	NC
H24	NC
H25	NC
H26	NC
H31	NC
H4	NC
H5	NC
H8	NC
J11	NC
J12	NC
J14	NC
J15	NC
J16	NC
J19	NC
J23	NC
J24	NC
J26	NC
J27	NC
J28	NC
J29	NC
J30	NC
J31	NC
J4	NC
J5	NC
J8	NC
K10	NC
K11	NC
K12	NC
K13	NC
K14	NC
K15	NC
K16	NC
K19	NC
K20	NC
K21	NC
K22	NC
K23	NC
K24	NC
K25	NC
K26	NC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
K27	NC
K4	NC
K5	NC
K8	NC
K9	NC
L14	NC
L15	NC
L16	NC
L19	NC
L20	NC
L21	NC
L22	NC
L23	NC
L24	NC
L25	NC
L26	NC
L27	NC
L3	NC
L4	NC
L5	NC
M13	NC
M14	NC
M15	NC
M16	NC
M19	NC
M20	NC
M21	NC
M22	NC
M23	NC
M24	NC
M25	NC
M26	NC
M27	NC
M3	NC
M4	NC
M5	NC
N10	NC
N11	NC
N12	NC
N13	NC
N14	NC
N15	NC
N16	NC
N19	NC
N20	NC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
N21	NC
N22	NC
N23	NC
N24	NC
N25	NC
N26	NC
N27	NC
N4	NC
N5	NC
N9	NC
P11	NC
P12	NC
P19	NC
P3	NC
P4	NC
P5	NC
P6	NC
P7	NC
P8	NC
R11	NC
R12	NC
R14	NC
R3	NC
R4	NC
R5	NC
R6	NC
R7	NC
R8	NC
T11	NC
T12	NC
T14	NC
T4	NC
T5	NC
T6	NC
T7	NC
T8	NC
U11	NC
U12	NC
U14	NC
U3	NC
U4	NC
U5	NC
U8	NC
V14	NC
V3	NC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
V4	NC
V5	NC
V8	NC
W13	NC
W14	NC
W3	NC
W4	NC
W5	NC
W8	NC
Y13	NC
Y14	NC
Y4	NC
Y8	NC
Y9	NC
AH28	PCIE_CALRN
AG28	PCIE_CALRP
AH33	PCIE_PVDD
AG29	PCIE_REFCLKN
AH29	PCIE_REFCLKP
AG34	PCIE_RX0N
AG33	PCIE_RX0P
R34	PCIE_RX10N
R33	PCIE_RX10P
P33	PCIE_RX11N
P34	PCIE_RX11P
M33	PCIE_RX12N
N33	PCIE_RX12P
L34	PCIE_RX13N
M34	PCIE_RX13P
K33	PCIE_RX14N
L33	PCIE_RX14P
J34	PCIE_RX15N
J33	PCIE_RX15P
AF33	PCIE_RX1N
AF34	PCIE_RX1P
AD33	PCIE_RX2N
AE33	PCIE_RX2P
AC34	PCIE_RX3N
AD34	PCIE_RX3P
AB33	PCIE_RX4N
AC33	PCIE_RX4P
AA34	PCIE_RX5N
AA33	PCIE_RX5P
Y33	PCIE_RX6N
Y34	PCIE_RX6P

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
V33	PCIE_RX7N
W33	PCIE_RX7P
U34	PCIE_RX8N
V34	PCIE_RX8P
T33	PCIE_RX9N
U33	PCIE_RX9P
AF31	PCIE_TX0N
AG31	PCIE_TX0P
T30	PCIE_TX10N
U30	PCIE_TX10P
R29	PCIE_TX11N
T29	PCIE_TX11P
P31	PCIE_TX12N
R31	PCIE_TX12P
N30	PCIE_TX13N
P30	PCIE_TX13P
M29	PCIE_TX14N
N29	PCIE_TX14P
L31	PCIE_TX15N
M31	PCIE_TX15P
AE30	PCIE_TX1N
AF30	PCIE_TX1P
AD29	PCIE_TX2N
AE29	PCIE_TX2P
AC31	PCIE_TX3N
AD31	PCIE_TX3P
AB30	PCIE_TX4N
AC30	PCIE_TX4P
AA29	PCIE_TX5N
AB29	PCIE_TX5P
Y31	PCIE_TX6N
AA31	PCIE_TX6P
W30	PCIE_TX7N
Y30	PCIE_TX7P
V29	PCIE_TX8N
W29	PCIE_TX8P
U31	PCIE_TX9N
V31	PCIE_TX9P
K28	PCIE_VDDC
K29	PCIE_VDDC
K30	PCIE_VDDC
K31	PCIE_VDDC
L28	PCIE_VDDC
M28	PCIE_VDDC
N28	PCIE_VDDC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
P28	PCIE_VDDC
R28	PCIE_VDDC
T28	PCIE_VDDC
U28	PCIE_VDDC
V28	PCIE_VDDC
AA28	PCIE_VDDR
AB28	PCIE_VDDR
AC28	PCIE_VDDR
AD28	PCIE_VDDR
AE28	PCIE_VDDR
AF28	PCIE_VDDR
W28	PCIE_VDDR
Y28	PCIE_VDDR
AA30	PCIE_VSS
AA32	PCIE_VSS
AB31	PCIE_VSS
AB32	PCIE_VSS
AC29	PCIE_VSS
AC32	PCIE_VSS
AD30	PCIE_VSS
AD32	PCIE_VSS
AE31	PCIE_VSS
AE32	PCIE_VSS
AF29	PCIE_VSS
AF32	PCIE_VSS
AG30	PCIE_VSS
AG32	PCIE_VSS
AH30	PCIE_VSS
AH31	PCIE_VSS
AH32	PCIE_VSS
AJ28	PCIE_VSS
AJ29	PCIE_VSS
AJ30	PCIE_VSS
AK28	PCIE_VSS
AK29	PCIE_VSS
H32	PCIE_VSS
H33	PCIE_VSS
H34	PCIE_VSS
J32	PCIE_VSS
K32	PCIE_VSS
L29	PCIE_VSS
L30	PCIE_VSS
L32	PCIE_VSS
M30	PCIE_VSS
M32	PCIE_VSS

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
N31	PCIE_VSS
N32	PCIE_VSS
P29	PCIE_VSS
P32	PCIE_VSS
R30	PCIE_VSS
R32	PCIE_VSS
T31	PCIE_VSS
T32	PCIE_VSS
U29	PCIE_VSS
U32	PCIE_VSS
V30	PCIE_VSS
V32	PCIE_VSS
W31	PCIE_VSS
W32	PCIE_VSS
Y29	PCIE_VSS
Y32	PCIE_VSS
AJ31	PERSTB
AJ34	R
AP17	R2
AN17	R2B
AL17	R2SET
AJ33	RB
AL31	RSET
AB10	SCL
AC10	SDA
V13	SPV10
U13	SPVSS
AK24	TESTEN
F31	tp_BA0_A0
G16	tp_BA1_A1
F8	tp_BA1_B0
AE9	tp_BA2_B1
F26	tp_CASb_A0
F16	tp_CASb_A1
F4	tp_CASb_B0
AD4	tp_CASb_B1
C9	tp_DQ10_B0
AB9	tp_DQ10_B1
C8	tp_DQ11_B0
AB8	tp_DQ11_B1
C25	tp_DQ2_A0
C14	tp_DQ2_A1
C26	tp_DQ3_A0
C15	tp_DQ3_A1
D26	tp_RDQS1_A0

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
D15	tp_RDQS1_A1
D8	tp_RDQS1_B0
AC8	tp_RDQS1_B1
D25	tp_WDQS1_A0
D14	tp_WDQS1_A1
D9	tp_WDQS1_B0
AC9	tp_WDQS1_B1
G31	tp_WEb_A0
G19	tp_WEb_A1
G8	tp_WEb_B0
AF8	tp_WEb_B1
AJ24	TS_FDO
AJ23	TSVDD
AK23	TSVSS
AP6	TX0M_DPA2N
AA2	TX0M_DPC2N
AN6	TX0P_DPA2P
AB2	TX0P_DPC2P
AN7	TX1M_DPA1N
AC2	TX1M_DPC1N
AN8	TX1P_DPA1P
AC1	TX1P_DPC1P
AP8	TX2M_DPA0N
AD1	TX2M_DPC0N
AP9	TX2P_DPA0P
AD2	TX2P_DPC0P
AP12	TX3M_DPB2N
AG2	TX3M_DPD2N
AN12	TX3P_DPB2P
AH2	TX3P_DPD2P
AN13	TX4M_DPB1N
AJ2	TX4M_DPD1N
AN14	TX4P_DPB1P
AJ1	TX4P_DPD1P
AP14	TX5M_DPB0N
AK1	TX5M_DPD0N
AP15	TX5P_DPB0P
AK2	TX5P_DPD0P
AN5	TXCAM_DPA3N
AP5	TXCAP_DPA3P
AN11	TXCBM_DPB3N
AP11	TXCBP_DPB3P
Y1	TXCCM_DPC3N
AA1	TXCCP_DPC3P
AF1	TXCDM_DPD3N

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
AG1	TXCDP_DPD3P
AN19	TXCLK_LN_DPE3N
AN20	TXCLK_LP_DPE3P
AN25	TXCLK_UN_DPF3N
AN26	TXCLK_UP_DPF3P
AP20	TXOUT_L0N_DPE2N
AP21	TXOUT_L0P_DPE2P
AN21	TXOUT_L1N_DPE1N
AN22	TXOUT_L1P_DPE1P
AN23	TXOUT_L2N_DPE0N
AP23	TXOUT_L2P_DPE0P
AP24	TXOUT_L3N
AN24	TXOUT_L3P
AP26	TXOUT_U0N_DPF2N
AP27	TXOUT_U0P_DPF2P
AN27	TXOUT_U1N_DPF1N
AN28	TXOUT_U1P_DPF1P
AN29	TXOUT_U2N_DPF0N
AP29	TXOUT_U2P_DPF0P
AP30	TXOUT_U3N
AN30	TXOUT_U3P
AL18	V2SYNC
M8	VARY_BL
AJ19	VDD_CT
AJ20	VDD_CT
AK19	VDD_CT
AK20	VDD_CT
AK31	VDD1DI
AK14	VDD2DI
AJ15	VDDC
AA16	VDDC
AA18	VDDC
AA20	VDDC
AA22	VDDC
AA24	VDDC
AA26	VDDC
AB17	VDDC
AB19	VDDC
AB21	VDDC
AB23	VDDC
AB25	VDDC
AC16	VDDC
AC18	VDDC
AC20	VDDC
AC22	VDDC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
AC24	VDDC
AC26	VDDC
AD17	VDDC
AD19	VDDC
AD21	VDDC
AD23	VDDC
AD25	VDDC
AE16	VDDC
AE18	VDDC
AE20	VDDC
AE22	VDDC
AE24	VDDC
AE26	VDDC
AF17	VDDC
AF19	VDDC
AF21	VDDC
AF23	VDDC
AF25	VDDC
AG16	VDDC
AG18	VDDC
AG20	VDDC
AG22	VDDC
AG24	VDDC
AG26	VDDC
T17	VDDC
T19	VDDC
T21	VDDC
T23	VDDC
T25	VDDC
U16	VDDC
U18	VDDC
U20	VDDC
U22	VDDC
U24	VDDC
U26	VDDC
V17	VDDC
V19	VDDC
V21	VDDC
V23	VDDC
V25	VDDC
W16	VDDC
W18	VDDC
W20	VDDC
W22	VDDC
W24	VDDC

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
W26	VDDC
Y17	VDDC
Y19	VDDC
Y21	VDDC
Y23	VDDC
Y25	VDDC
P20	VDDCI
P21	VDDCI
P22	VDDCI
P23	VDDCI
AA7	VDDR1
AB7	VDDR1
AC7	VDDR1
AD7	VDDR1
AE7	VDDR1
AF7	VDDR1
D18	VDDR1
D28	VDDR1
D30	VDDR1
D7	VDDR1
E18	VDDR1
E28	VDDR1
E30	VDDR1
E7	VDDR1
F18	VDDR1
F28	VDDR1
F30	VDDR1
F7	VDDR1
G18	VDDR1
G28	VDDR1
G30	VDDR1
G7	VDDR1
H18	VDDR1
H28	VDDR1
H30	VDDR1
H7	VDDR1
J18	VDDR1
J7	VDDR1
K18	VDDR1
K7	VDDR1
L18	VDDR1
L7	VDDR1
M18	VDDR1
M7	VDDR1
N18	VDDR1

Table A-2 E4690 Pins Sorted by Signal Name

Ball Reference	Signal Name
N7	VDDR1
U7	VDDR1
V7	VDDR1
W7	VDDR1
Y7	VDDR1
AC14	VDDR3
AD14	VDDR3
AE14	VDDR3
AF14	VDDR3
AG12	VDDR4
AG13	VDDR4
AH12	VDDR4
AH13	VDDR4
AJ12	VDDR5
AJ13	VDDR5
AK12	VDDR5
AK13	VDDR5
P27	VDDRHA
P18	VDDRHB
G25	VREF1_A0
G13	VREF1_A1
H3	VREF1_B0
AF5	VREF1_B1
E34	VREF2_A0
G22	VREF2_A1
G10	VREF2_B0
AF10	VREF2_B1
AJ14	VREFG
AK30	VSS1DI
AL14	VSS2DI
P26	VSSRHA
P17	VSSRHB
AM31	VSYNC
AN32	XTALIN
AM32	XTALOUT
AL16	Y

Appendix B

Pin Assignment Diagrams in Black and White

B.1 E4690 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND	GND	GND		NC	NC		NC	NC		NC	NC		NC	NC		NC
B	GND	GND	NC	MZQ_B0	NC	NC	NC	GND	GND	NC	NC	NC	NC	GND	GND	MZQ_A1	NC
C	GND	DVPCLK	NC	NC	NC	NC	NC	tp_DQ11_B0	tp_DQ10_B0	NC	NC	NC	NC	tp_DQ2_A1	tp_DQ3_A1	NC	NC
D		DVPCNTL_2	NC	NC	NC	GND	VDDR1	tp_RDQS1_B0	tp_WDQS1_B0	NC	NC	NC	NC	tp_WDQS1_A1	tp_RDQS1_A1	NC	GND
E	DVPDATA_1	DVPDATA_0	NC	GND	NC	GND	VDDR1	GND	GND	NC	NC	NC	NC	GND	GND	NC	GND
F	DVPDATA_3	DVPDATA_2	NC	tp_CASb_B0	NC	GND	VDDR1	tp_BA1_B0	GND	NC	NC	NC	NC	NC	NC	tp_CASb_A1	GND
G		DVPDATA_5	DVPDATA_4	NC	NC	GND	VDDR1	tp_WEb_B0	GND	VREF2_B0	NC	NC	VREF1_A1	NC	NC	tp_BA1_A1	GND
H	DVPDATA_7	DVPDATA_6	VREF1_B0	NC	NC	GND	VDDR1	NC	CLKb_B0	CLK_B0	NC	NC	NC	NC	NC	NC	GND
J	DVPDATA_9	DVPDATA_8	MVDDA1_B0	NC	NC	GND	VDDR1	NC	GND	MVDDA2_B0	NC	NC	MVDDA1_A1	NC	NC	NC	GND
K		DVPDATA_11	DVPDATA_10	NC	NC	GND	VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	GND
L	DVPCNTL_1	DVPCNTL_0	NC	NC	NC	GND	VDDR1	GPIO_7_BLON	GPIO_8_ROMSO	GPIO_10_ROMSCK	GPIO_5_AC_BATT	GPIO_15_PWRCNTL_0	GPIO_21	NC	NC	NC	GND
M	DVPCNTL_MVP_0	DVPCNTL_MVP_1	NC	NC	NC	GND	VDDR1	VARY_BL	GPIO_9_ROMSI	GPIO_22_ROMCSB	GPIO_20_PWRCNTL_1	GPIO_23_CLKREQB	NC	NC	NC	NC	GND
N		DVPDATA_13	DVPDATA_12	NC	NC	GND	VDDR1	DIGON	NC	NC	NC	NC	NC	NC	NC	NC	GND
P	DVPDATA_15	DVPDATA_14	NC	NC	NC	NC	NC	NC	GENERICA	GPIO_0	NC	NC	DRAM_RST	MEM_CALRP1	MVREFSB	MVREFDB	VSSRHB
R	DVPDATA_17	DVPDATA_16	NC	NC	NC	NC	NC	NC	GENERICB	GPIO_1	NC	NC	CLKTESTA	NC			
T		DVPDATA_19	DVPDATA_18	NC	NC	NC	NC	NC	GENERICC	GPIO_11	NC	NC	CLKTESTB	NC		GND	VDDC
U	DVPDATA_21	DVPDATA_20	NC	NC	NC	GND	VDDR1	NC	GENERICD	GPIO_12	NC	NC	SPVSS	NC		VDDC	GND
V	DVPDATA_23	DVPDATA_22	NC	NC	NC	GND	VDDR1	NC	GENERICF	GPIO_13	GPIO_17_THERMAL_INT	GPIO_29	SPV10	NC		GND	VDDC
W		DDCDATA_AUX3N	NC	NC	NC	GND	VDDR1	NC	GENERICG	GPIO_2	GPIO_19_CTF	GPIO_30	NC	NC		VDDC	GND
Y	TXCCM_DPC3N	DDCCLK_AUX3P	DPC_VSSR	NC	MZQ_B1	GND	VDDR1	NC	NC	GPIO_3_SMBDATA	GPIO_6_TACH	GPIO_24_TRSTB	NC	NC		GND	VDDC
AA	TXCCP_DPC3P	TX0M_DPC2N	DPC_VSSR	NC	NC	GND	VDDR1	GND	GND	GPIO_4_SMBCLK	GENERICE_HPD4	GPIO_25_TDI	NC	NC		VDDC	GND
AB		TX0P_DPC2P	DPC_VSSR	DPC_VDD10	NC	GND	VDDR1	tp_DQ11_B1	tp_DQ10_B1	SCL	GPIO_18_HPD3	GPIO_26_TCK	NC	NC		GND	VDDC
AC	TX1P_DPC1P	TX1M_DPC1N	DPC_VSSR	DPC_VDD10	NC	GND	VDDR1	tp_RDQS1_B1	tp_WDQS1_B1	SDA	GPIO_14_HPD2	GPIO_27_TMS	NC	VDDR3		VDDC	GND
AD	TX2M_DPC0N	TX2P_DPC0P	DPC_VSSR	tp_CASb_B1	GND	GND	VDDR1	GND	GND	GPIO_16_SSIN		GPIO_28_TDO	NC	VDDR3		GND	VDDC
AE		DDCDATA_AUX4N	DPC_VSSR	DPC_PVSS	NC	GND	VDDR1	GND	tp_BA2_B1	NC	NC	NC	NC	VDDR3		VDDC	GND
AF	TXCDM_DPD3N	DDCCLK_AUX4P	DPD_VSSR	DPC_PVDD	VREF1_B1	GND	VDDR1	tp_WEb_B1	GND	VREF2_B1	NC	NC	NC	VDDR3		GND	VDDC
AG	TXCDP_DPD3P	TX3M_DPD2N	DPD_VSSR	DPD_PVDD	MVDDA1_B1	NC	NC	CLKb_B1	CLK_B1	GND	NC	VDDR4	VDDR4	NC		VDDC	GND
AH		TX3P_DPD2P	DPD_VSSR	DPD_PVSS	NC	NC	NC	GND	GND	MVDDA2_B1	NC	VDDR4	VDDR4	NC			
AJ	TX4P_DPD1P	TX4M_DPD1N	DPD_VSSR	DPD_VDD10	NC	NC	NC	DPCD_CADLR	PAB_CALR	NC	NC	VDDR5	VDDR5	VREFG	VDDC	GND	NC
AK	TX5M_DPD0N	TX5P_DPD0P	DPD_VSSR	DPD_VDD10	NC	NC	NC	DPB_PVSS	NC	NC	NC	VDDR5	VDDR5	VDD2DI	A2VDDQ	A2VSSQ	A2VDD
AL		DDC1CLK	DPD_VSSR	DPA_VDD10	DPA_VDD10	DPA_PVSS	DPA_PVDD	DPB_PVDD	DDC2DATA	DDC2CLK	DPB_VDD10	DPB_VDD10	NC	VSS2DI	COMP	Y	R2SET
AM	GND	DDC1DATA	DPD_VSSR	DPA_VSSR	DPA_VSSR	DPA_VSSR	DPA_VSSR	DPA_VSSR	DPB_VSSR	DPB_VSSR	DPB_VSSR	DPB_VSSR	DPB_VSSR	DPB_VSSR	B2B	G2B	C
AN	GND	GND	AUX1N	AUX1P	TXCAM_DPA3N	TX0P_DPA2P	TX1M_DPA1N	TX1P_DPA1P	AUX2N	AUX2P	TXCBM_DPB3N	TX3P_DPB2P	TX4M_DPB1N	TX4P_DPB1P	B2	G2	R2B
AP	GND	GND	DPA_VSSR		TXCAP_DPA3P	TX0M_DPA2N		TX2M_DPA0N	TX2P_DPA0P		TXCBP_DPB3P	TX3M_DPB2N		TX5M_DPB0N	TX5P_DPB0P		R2
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

Figure B-1 E4690 Pin Assignment - Left Half

18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	
NC		NC	NC		NC	NC		NC	NC		NC	NC		GND	GND	GND	A
NC	NC	NC	NC	NC	NC	NC	GND	GND	MZQ_A0	NC	NC	NC	NC	NC	GND	GND	B
NC	NC	NC	NC	NC	NC	NC	tp_DQ2_A0	tp_DQ3_A0	NC	NC	NC	NC	NC	NC	NC	GND	C
VDDR1	NC	NC	NC	NC	NC	NC	tp_WDQS1_A0	tp_RDQS1_A0	GND	VDDR1	GND	VDDR1	NC	NC	NC		D
VDDR1	NC	NC	NC	NC	NC	NC	GND	GND	GND	VDDR1	GND	VDDR1	NC	NC	NC	VREF2_A0	E
VDDR1	NC	NC	NC	NC	NC	NC	NC	tp_CASb_A0	GND	VDDR1	GND	VDDR1	tp_BA0_A0	GND	GND	MVDDA2_A0	F
VDDR1	tp_WEb_A1	GND	GND	VREF2_A1	NC	NC	VREF1_A0	NC	GND	VDDR1	GND	VDDR1	tp_WEb_A0	CLKb_A0	CLK_A0		G
VDDR1	NC	CLKb_A1	CLK_A1	NC	NC	NC	NC	NC	GND	VDDR1	GND	VDDR1	NC	PCIE_VSS	PCIE_VSS	PCIE_VSS	H
VDDR1	NC	GND	GND	MVDDA2_A1	NC	NC	MVDDA1_A0	NC	NC	NC	NC	NC	NC	PCIE_VSS	PCIE_RX15P	PCIE_RX15N	J
VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	PCIE_VDDC	PCIE_VDDC	PCIE_VDDC	PCIE_VDDC	PCIE_VSS	PCIE_RX14N		K
VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	PCIE_VDDC	PCIE_VSS	PCIE_VSS	PCIE_TX15N	PCIE_VSS	PCIE_RX14P	PCIE_RX13N	L
VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	PCIE_VDDC	PCIE_TX14N	PCIE_VSS	PCIE_TX15P	PCIE_VSS	PCIE_RX12N	PCIE_RX13P	M
VDDR1	NC	NC	NC	NC	NC	NC	NC	NC	NC	PCIE_VDDC	PCIE_TX14P	PCIE_TX13N	PCIE_VSS	PCIE_VSS	PCIE_RX12P		N
VDDRHB	NC	VDDCI	VDDCI	VDDCI	VDDCI	MVREFDA	MVREFSA	VSSRHA	VDDRHA	PCIE_VDDC	PCIE_VSS	PCIE_TX13P	PCIE_TX12N	PCIE_VSS	PCIE_RX11N	PCIE_RX11P	P
										PCIE_VDDC	PCIE_TX11N	PCIE_VSS	PCIE_TX12P	PCIE_VSS	PCIE_RX10P	PCIE_RX10N	R
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDC	PCIE_TX11P	PCIE_TX10N	PCIE_VSS	PCIE_VSS	PCIE_RX9N		T
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDC	PCIE_VSS	PCIE_TX10P	PCIE_TX9N	PCIE_VSS	PCIE_RX9P	PCIE_RX8N	U
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDC	PCIE_TX8N	PCIE_VSS	PCIE_TX9P	PCIE_VSS	PCIE_RX7N	PCIE_RX8P	V
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDR	PCIE_TX8P	PCIE_TX7N	PCIE_VSS	PCIE_VSS	PCIE_RX7P		W
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDR	PCIE_VSS	PCIE_TX7P	PCIE_TX6N	PCIE_VSS	PCIE_RX6N	PCIE_RX6P	Y
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDR	PCIE_TX5N	PCIE_VSS	PCIE_TX6P	PCIE_VSS	PCIE_RX5P	PCIE_RX5N	AA
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDR	PCIE_TX5P	PCIE_TX4N	PCIE_VSS	PCIE_VSS	PCIE_RX4N		AB
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDR	PCIE_VSS	PCIE_TX4P	PCIE_TX3N	PCIE_VSS	PCIE_RX4P	PCIE_RX3N	AC
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDR	PCIE_TX2N	PCIE_VSS	PCIE_TX3P	PCIE_VSS	PCIE_RX2N	PCIE_RX3P	AD
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_VDDR	PCIE_TX2P	PCIE_TX1N	PCIE_VSS	PCIE_VSS	PCIE_RX2P		AE
GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND		PCIE_VDDR	PCIE_VSS	PCIE_TX1P	PCIE_TX0N	PCIE_VSS	PCIE_RX1N	PCIE_RX1P	AF
VDDC	GND	VDDC	GND	VDDC	GND	VDDC	GND	VDDC		PCIE_CALRP	PCIE_REFCLKN	PCIE_VSS	PCIE_TX0P	PCIE_VSS	PCIE_RX0P	PCIE_RX0N	AG
										PCIE_CALRN	PCIE_REFCLKP	PCIE_VSS	PCIE_VSS	PCIE_VSS	PCIE_PVDD		AH
NC	VDD_CT	VDD_CT	NC	DMINUS	TSVDD	TS_FDO	NC	DPLL_PVDD	GND	PCIE_VSS	PCIE_VSS	PCIE_VSS	PERSTB	AVSSQ	RB	R	AJ
NC	VDD_CT	VDD_CT	DPEF_CALR	DPLUS	TSVSS	TESTEN	DPE_PVSS	DPLL_PVSS	DPLL_VDDC	PCIE_VSS	PCIE_VSS		VDD1DI	AVDD	GB	G	AK
V2SYNC	DDC6DATA	DDC6CLK	DPE_VDD10	DPE_VDD10	DPE_VDD18	DPE_VDD18	DPE_PVDD	NC	DPF_VDD18	DPF_VDD18	DPF_VDD10	VSS1DI DPF_VDD10	RSET	BB	B		AL
H2SYNC	DPE_VSSR	DPE_VSSR	DPE_VSSR	DPE_VSSR	DPE_VSSR	DPE_VSSR	DPF_VSSR	DPF_VSSR	DPF_VSSR	DPF_VSSR	DPF_VSSR	DPF_VSSR	VSYNC	XTALOUT	HSYNC	GND	AM
DDCCLK_AUX5P	TXCLK_LN_DPE3N	TXCLK_LP_DPE3P_DPE2N	TXOUT_L1N_DPE1N	TXOUT_L1P_DPE1P	TXOUT_L2N_DPE0N_DPE0P	TXOUT_L3P	TXCLK_UN_DPF3N	TXCLK_UP_DPF3P	TXOUT_U1N_DPF1N	TXOUT_U1P_DPF1P	TXOUT_U2N_DPF0N_DPF0P	TXOUT_U3P	DPF_VSSR	XTALIN	GND	GND	AN
DDCDATA_AUX5N		TXOUT_L0N_DPE2N	TXOUT_L0P_DPE2P		TXOUT_L2P_DPE0P	TXOUT_L3N		TXOUT_U0N_DPF2N	TXOUT_U0P_DPF2P		TXOUT_U2P_DPF0P	TXOUT_U3N		GND	GND	GND	AP
18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	

Figure B-2 E4690 Pin Assignment - Right Half

Appendix C
Revision History

Note: The release states are defined as:

Preliminary Releases — Revision numbers 0.xx are rough works.

Revision numbers 1.xx are documents with substantial info

Revision numbers 2.xx are documents with complete information.

Full Release — Revision numbers 3.xx are for production.

Rev 3.00 (June 2010)

- Production release.