Power Management Modes
PEX 8600 Product Family

White Paper

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Website: www.plxtech.com
Technical Support: www.plxtech.com/support

1 Introduction

Given the importance of lower power consumption and the rapid rise in power requirements of ever-escalating circuit densities and operating frequencies, PLX has designed multiple power saving features that enable best-in-class power savings for markets ranging from mobile to high-end storage applications.

2 Chip Architecture

PLX PCIe Gen 2 chips use a building block design in its architecture in order to deliver large switches and provide more control on power management for customers. For example, the PEX 8648 design is partitioned into three “stations” with each supporting 16 lanes of PCI Express Gen 2 SerDes and the “central-box” (CROSS-BAR) that is the interconnect between the various stations. The following text describes the various sections that can be powered off to achieve incremental savings based on the usage models and traffic types.

A large percentage of the total power contribution is due to the SerDes which consume approximately 60-70% of the total chip’s power. The actual power savings will depend on the total number of lanes in a specific device and the number of lanes controlled through the techniques listed below.

3 SerDes Power Saving Modes

3.1 Turning Off Lanes

Individual SerDes lanes can be turned off when not being used to reduce power consumption. Expected power savings will be 50-70mW per lane, depending on the number of lanes being turned off.

3.2 Reducing Drive Strengths

For short traces, the drive strength of the SerDes can be adjusted to reduce power per lane.

3.3 Turning Off Ports

For configurations where the downstream ports of the switch are not used, the port specific logic dedicated to the given port can be turned off. Expected typical power savings will be in the order of 100mW per port.

3.4 Turning Off Stations

If all the ports in a given station are unused, then additional savings can be realized by turning off the whole station. The typical power savings will be approximately 300mW per station.

4 PCI Express Power Management Modes

4.1 ASPM

Hardware enabled Active State Power Management modes are supported and the power savings are substantial based on the traffic density. For an idle switch with ASPM enabled, the power consumption is reduced by 40% under typical conditions. For example, enabling ASPM under typical conditions for the PEX 8648 results in a total power consumption drop from 4.0W to 3.3W.

4.2 L1-ASPM-Mode 1

L1-Active State Power Management is software initiated and the power savings are greater than hardware ASPM since all the ports are turned off when not active. The power consumption is reduced by 68%. For example, this results in a total power consumption drop from 4.0W down to 1.7 Watts under typical conditions for the PEX 8648.

4.3 L1-ASPM-Mode 2 (PLX specific)

The PEX 8600 switches have implemented an advance power optimization technique which, when enabled during L1-ASPM modes, reduces power consumption by 80%. For example, this results in a total power consumption of 1.05 Watts under typical conditions for the PEX 8648.

5 Other Power Saving Modes

5.1 Dynamic Link Width & Speed Adjustment

The PEX 8600 switches support configurable options that allow software to dynamically change the width and the speed of the link based on the traffic density or other system-specific usage modes. When traffic density is low, dynamic link width adjustment allows for unnecessary SerDes lanes to be dynamically turned off for power savings. Similarly, dynamic speed adjustment allows for the SerDes lanes to dynamically train down to Gen 1 (2.5 GT/s) speeds when traffic density is low to save power.