82540EP/82541(PI/GI/EI) & 82562EZ(EX) Dual Footprint Design Guide

Application Note

Networking Silicon

317506-001
Revision 2.9

Revision History

Revision	Revision Date	Description
0.25	Aug 2002	Initial publication of preliminary design guide information.
0.75	Sep 2002	Revised Design Guide information. Replaced reference design schematic. Revised EEPROM map and bit descriptions.
1.0	Oct 2002	Revised Design Guide Information Removed EEPROM information due to publication of separate guides.
1.5	Sep 2003	Published revised design guide information: • Added 82541GI coverage • Removed Confidential status • Updated schematics, removing redundant caps • Revised LAN disable circuit
2.0	Mar 2004	Published revised and updated design guide information: • Added information for the 82541PI • Updated schematics to include 82541PI
2.1	July 2004	Revised title for more clarification.
2.2	Oct 2004	Added crystal start-up information. Information includes: • New crystal parameters • Crystal selection guidelines • Crystal validation methods • Crystal testing methods Added 82562EX applicability. Added new values for TX and RX terminations (next to LAN silicon). New values are now 110 Ω for both TX and RX terminations. Added new starting values for RBIAS100 and RBIAS10. New starting values are now 649 Ω for RBIAS100 and 619 Ω for RBIAS10. Updated reference schematics to reflect new Tx and Rx termination values, new LAN disable circuit, RBIAS100/RBIAS10 values, and VIO signaling connection and pullup resistor value.
2.3	Nov 2004	Change resistor value for pin A13 from 3.3K Ω to 1K Ω
2.4	Jan 2005	• Changed text in the Catalyst EEPROM revision H table note from “Revision H or higher not supported” to “Revision H is not supported”. • Added a 0.01 µf capacitor between Ball C2 (M66EN) and ground to meet IEEE PCI specification (sheet 2 of reference schematics). • Removed the Design and Layout Checklists. These checklists are now separate Microsoft* Excel spreadsheets.
2.5	Jan 2005	Updated reference schematics to reflect current differential pair termination resistor values for the 82541(PI/GI/EI) and 82540EP. Updated section 4.2.1 “Termination Resistors for Designs Based on 82562EZ/EX PLC Device” to reflect current resistor and RBIAS values. Updated section 4.3.1 “Termination Resistors for Designs Based on 82541xx” to reflect current resistor values.
2.6	Apr 2005	Added revision history to reference schematics. Changed signal name SUPER_IO_GP to SUPER_IO_DISABLE on reference schematics sheet 2.
2.7	June 2006	Removed 82540EP LAN disable note from Section 3.3.1.
2.8	June 2006	Added Pulse H5007 discrete magnetics reference to Table 10.
2.9	January 2008	Updated reference schematics: sheets 2 through 5. Added link to Design and Board Layout Checklists in Section 5.0. Added recommended crystals for the 82541PI.

Note: This page is intentionally left blank.

Contents

Figures

Tables

Note: This page intentionally left blank.

1.0 Introduction

Intel currently supports several footprint compatible Ethernet options depending upon the target application. The term “footprint compatible” means that the silicon devices are all manufactured in a 15 mm x 15 mm, 196-ball grid array package with the same ball pattern. Many of the critical signal pin locations are identical, allowing designers to create a single LAN on Motherboard (LOM) design that accommodates all devices. This is a flexible, cost-effective, multipurpose design technique that allowing maximized value while matching performance needs.

Note: Since some of the signal pins have different usages, the term “pin-compatible” is not applicable.

Available LAN components with the same footprint include the 82540EP/82541xx Family of Gigabit Ethernet Controllers and the 82562EZ(EX) Platform LAN Connect components.

Note: Throughout this document, the notation “82541xx” will be used to denote the 82541 Family of Gigabit Controllers (82541PI, 82541GI, and 82541EI).

The LAN component used on a specific platform depends on the end user’s need for connection speed and manageability. As the requirements change, footprint compatibility makes it possible to re-focus the platform without the need to redesign a new a motherboard.

Table 1. LAN Component Connections/Features

LAN Component	Interface	Connection	Features
82541xx	PCI	Gigabit Ethernet (1000BASE-T) with Alert Standard Format (ASF) alerting	Gigabit Ethernet, ASF 2.0 alerting
82562EX (196 BGA)	LCI	10/100 Ethernet with ASF alerting	Ethernet 10/100 connection, ASF 1.0 alerting
82562EZ (196 BGA)	LCI	Basic 10/100 Ethernet	Ethernet 10/100 connection
82540EP	PCI	Gigabit Ethernet (1000BASE-T) with ASF alerting	Gigabit Ethernet, ASF 1.0 alerting

1.1 Scope

This application note contains Ethernet design guidelines applicable to LOM designs based on the Intel® 865 Chipset and Intel® 875 Chipset. The document identifies similarities and differences between the 82562EZ(EX) Platform LAN Connect device and the 82540EP/82541xx Gigabit Ethernet Controller.

- Section 2 describes the port interfaces specific to each device.
- Section 3 explains the requirements for connecting an Ethernet device to the system.
- Section 4 describes board layout techniques applicable to these devices.
- Section 5 provides a reference to the design and layout checklists.

- Section 6 compares pin names and numbers between the two components.
- Section 7 provides a reference design schematic of the full dual footprint configuration.

Note: It is assumed that the reader is acquainted with high-speed design and board layout techniques. Additional documents may be referred to for further information.

1.2 Reference Documents

- PCI Bus Power Management Interface Specification, Rev. 1.1. PCI Special Interest Group.
- IEEE Standard 802.3, 2000 Edition. Incorporating various IEEE standards previously published separately.
- 82562EZ 10/100 Mbps Platform LAN Connect (PLC) Networking Silicon Datasheet. Intel Corporation.
- 82562ET/EM Platform LAN Connect Printed Circuit Board (PCB) Design Guide. Intel Corporation.
- 82547GI(EI)/82541GI(EI)/82541ER EEPROM Map and Programming Information. Intel Corporation.
- ICH2 Integrated LAN Controller Function Disable and Power Control. Intel Corporation.
- 82540EP Gigabit Ethernet Controller Datasheet. Intel Corporation.
- 82541 Family of Gigabit Ethernet Controllers Datasheet. Intel Corporation.
- I/O Control Hub 2, 3, and 4 EEPROM Map and Programming Information. Intel Corporation.
- I/O Control Hub 5, 6, and 7 EEPROM Map and Programming Information. Intel Corporation.

Programming information can be obtained through your local Intel representative.

1.3 Product Codes

Table 2 lists the product ordering codes for the 82562EZ(EX), 82541xx, and 82540EP.

Table 2. Product Ordering Codes

Device	Product Code	Product Code (Lead Free)
82562EZ	GD82562EZ	LU82562EZ
82562EX	GD82562EX	LU82562EX
82541PI	GD82541PI	LU82541PI
82541GI	GD82541GI	LU82541GI
82541EI	GD82541EI	LU82541EI
82540EP	GD82540EP	LU82540EP

2.0 System Data Port Interfaces

The 82562EZ/EX Platform LAN Connect Device and the 82540EP/82541xx Gigabit Ethernet controller employ different system interfaces as illustrated below.

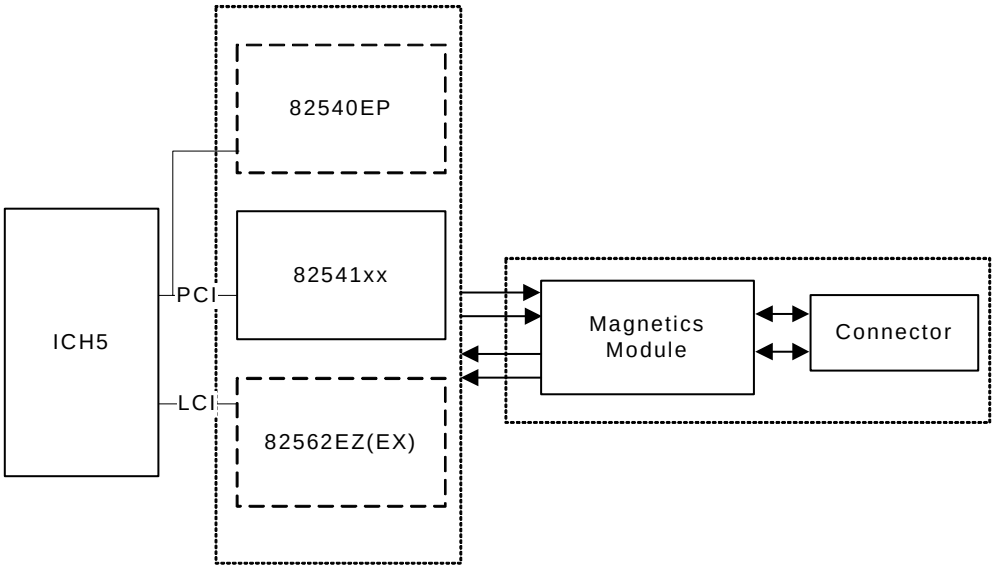


Figure 1. ICH5 Platform LAN Connect Sections

2.1 LCI Connection to 82562EZ(EX) Platform LAN Connect Device

The 82562EZ(EX) Platform LAN Connect device uses the LAN Connect Interface (LCI) to connect to the I/O Control Hub 5 (ICH5). LCI is a point-to-point interface optimized to support one device.

Line termination mechanisms are not specified for the LCI. Slew rate controlled output buffers achieve acceptable signal integrity by controlling signal reflection, undershoot and ringing.

For details about how to connect the LCI interface between the 82562EZ(EX) Platform LAN Connect device and ICH5, please refer to the *82562ET/EM Platform LAN Connect Printed Circuit Board (PCB) Design Guide*, the Intel® 865 Chipset design guide, or the Intel® 875 Chipset design guide.

2.2 PCI Interface for 82540EP/82541xx Family of Gigabit Controllers

The 82540EP and 82541xx controllers provide 32-bit interfaces for a 33 MHz or 66 MHz PCI bus meeting PCI 2.3 Specifications. The PCI 2.3 Specification trace routing instructions should be followed.

The Ethernet controllers operate as PCI slave devices for configuration and register programming. After the devices have been properly initialized, they can also operate as PCI masters to fetch memory descriptors and to read/write data buffers.

The devices are capable of operating in either a 5 V or 3.3 V signaling environment. The VIO terminals can be connected to either 3.3 V or 5 V to choose the appropriate PCI bus levels. These connections bias the controller PCI I/O buffers for the correct switching strength. However, all other digital inputs and outputs use 3.3 V signaling unless specified separately.

3.0 Ethernet Component Design Guidelines

This section provides recommendations for selecting components and connecting special pins. The main design elements are the 82562EZ(EX) Platform LAN Connect device or the 82540EP/82541xx Gigabit Ethernet Controller, a magnetics module with RJ-45 connector, and a crystal clock source.

3.1 General Design Considerations for Ethernet Controllers

These recommendations apply to all designs, 10/100 Mbps or 10/100/1000 Mbps.

Good engineering practices should be followed with respect to unused inputs by terminating them with pull-up or pull-down resistors, unless the datasheet, design guide or reference schematic indicates otherwise. Do not attach pull-up or pull-down resistors to any balls identified as RESERVED (unless explicitly included in the reference schematic). These devices may have special test modes that could be entered inadvertently.

3.1.1 Crystal Selection Parameters

Quartz crystals are generally considered to be the mainstay of frequency control components due to their low cost and ease of implementation. They are available from numerous vendors in many package types and with various specification options.

All crystals used with Intel® Ethernet controllers are described as “AT-cut”, which refers to the angle at which the unit is sliced with respect to the long axis of the quartz stone.

Table 3 lists the crystal electrical parameters and provides suggested values for typical designs. The parameters listed are described in the following subsections.

Table 3. Crystal Parameters

Parameter	Suggested Value
Vibration Mode	Fundamental
Nominal Frequency	25,000 MHz at 25° C (required)
Frequency Tolerance	• ±30 ppm recommended; ±50 ppm across the entire operating temperature range as required by IEEE specifications • ±30 ppm required for the 82541EI/GI
Temperature Stability	• ±50 ppm at 0° C to 70° C • ±30 ppm at 0° C to 70° C required for the 82541EI/GI
Calibration Mode	Parallel
Load Capacitance	• 16 pF to 20 pF • 18 pF required for the 82541EI/GI
Shunt Capacitance	6 pF maximum
Equivalent Series Resistance	• 50 Ω maximum • 20 Ω maximum required for the 82541EI/GI
Drive Level	0.5 mW maximum
Aging	±5 ppm per year maximum

.Table 4 lists the approved crystals for use with the 82541PI C0 stepping.

Table 4. 82541PI Recommended Crystals

Manufacturer	Manufacturer's Part Number
Raltron (<20 Ω ESR and +/-30 ppm)	AS-25.000-20-F-SMD-TR
Citizen	HCM family that meets the crystal specifications.
TXC	6C25000131

3.1.1.1 Vibration Mode

Crystals in the frequency range listed in Table 3 are available in both fundamental and third overtone. Unless there is a special need for third overtone, use fundamental mode crystals.

At any given operating frequency, third overtone crystals are thicker and more rugged than fundamental mode crystals. Third overtone crystals are more suitable for use in military or harsh industrial environments. Third overtone crystals require a trap circuit (extra capacitor and inductor) in the load circuitry to suppress fundamental mode oscillation as the circuit powers up. Selecting values for these components is beyond the scope of this document.

3.1.1.2 Nominal Frequency

Intel® Ethernet controllers use a crystal frequency of 25.000 MHz. The 25 MHz input is used to generate a 125 MHz transmit clock for 100BASE-TX and 1000BASE-TX operation; 10 MHz and 20 MHz transmit clocks, for 10BASE-T operation.

3.1.1.3 Frequency Tolerance

The frequency tolerance for an Ethernet physical layer device is dictated by the IEEE 802.3 specification as ±50 parts per million (ppm). This measurement is referenced to a standard temperature of 25° C.

Note: Intel recommends a frequency tolerance of ±30 ppm.

3.1.1.4 Temperature Stability and Environmental Requirements

Temperature stability is a standard measure of how the oscillation frequency varies over the full operational temperature range (and beyond). Several optional temperature ranges are currently available, including -40° C to +85° C for industrial environments. Some vendors separate operating temperatures from temperature stability. Manufacturers may also list temperature stability as 50 ppm in their data sheets.

Note: Crystals also carry other specifications for storage temperature, shock resistance, and reflow solder conditions. Crystal vendors should be consulted early in the design cycle to discuss the application and its environmental requirements.

3.1.1.5 Calibration Mode

The terms “series-resonant” and “parallel-resonant” are often used to describe crystal circuits. Specifying parallel mode is critical to determining how the crystal frequency is calibrated at the factory.

A crystal specified and tested as series resonant oscillates without problem in a parallel-resonant circuit, but the frequency is higher than nominal by several hundred parts per million. The purpose of adding load capacitors to a crystal circuit is to establish resonance at a frequency higher than the crystal’s inherent series resonant frequency.

Figure 2 illustrates a simplified schematic of the 82562EZ(EX) and the 82540EP/82541xx controller’s crystal circuit. The crystal and the capacitors form a feedback element for the internal inverting amplifier. This combination is called parallel-resonant, because it has positive reactance at the selected frequency. In other words, the crystal behaves like an inductor in a parallel LC circuit.

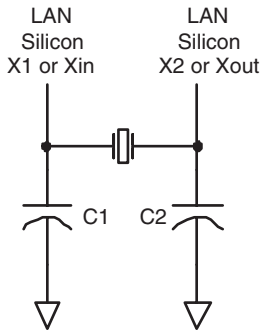


Figure 2. Crystal Circuit

3.1.1.6 Load Capacitance

The formula for crystal load capacitance is as follows:

$$C_L = \frac{(C1 \cdot C2)}{(C1 + C2)} + C_{stray}$$

where C1 = C2 = 22 pF (as suggested in most Intel reference designs)
and C_{stray} = allowance for additional capacitance in pads, traces and the chip carrier within the Ethernet controller package

An allowance of 3 pF to 7 pF accounts for lumped stray capacitance. The calculated load capacitance is 16 pF with an estimated stray capacitance of about 5 pF.

Individual stray capacitance components can be estimated and added. For example, surface mount pads for the load capacitors add approximately 2.5 pF in parallel to each capacitor. This technique is especially useful if Y1, C1 and C2 must be placed farther than approximately one-half (0.5) inch from the controller. It is worth noting that thin circuit boards generally have higher stray capacitance than thick circuit boards.

Standard capacitor loads used by crystal manufacturers include 16 pF, 18 pF and 20 pF. Any of these values will generally operate with the controller. However, a difference of several picofarads between the calibrated load and the actual load will pull the oscillator slightly off frequency.

Note: C1 and C2 may vary by as much as 5% (approximately 1 pF) from their nominal values.

3.1.1.7 Shunt Capacitance

The shunt capacitance parameter is relatively unimportant compared to load capacitance. Shunt capacitance represents the effect of the crystal's mechanical holder and contacts. The shunt capacitance should equal a maximum of 6 pF (7 pF is also acceptable).

3.1.1.8 Equivalent Series Resistance

Equivalent Series Resistance (ESR) is the real component of the crystal's impedance at the calibration frequency, which the inverting amplifier's loop gain must overcome. ESR varies inversely with frequency for a given crystal family. The lower the ESR, the faster the crystal starts up. Use crystals with an ESR value of 50 Ω or better.

Note: Check the specific controller documentation carefully; some devices may have tighter ESR requirements. For example, Intel recommends that 82541EI/GI devices use crystals with an ESR value of 20 Ω or less.

3.1.1.9 Drive Level

Drive level refers to power dissipation in use. The allowable drive level for a Surface Mounted Technology (SMT) crystal is less than its through-hole counterpart, because surface mount crystals are typically made from narrow, rectangular AT strips, rather than circular AT quartz blanks.

Some crystal data sheets list crystals with a maximum drive level of 1 mW. However, Intel® Ethernet controllers drive crystals to a level less than the suggested 0.5 mW value. This parameter does not have much value for on-chip oscillator use.

3.1.1.10 Aging

Aging is a permanent change in frequency (and resistance) occurring over time. This parameter is most important in its first year because new crystals age faster than old crystals. Use crystals with a maximum of ±5 ppm per year aging.

3.1.2 Reference Crystal

The normal tolerances of the discrete crystal components can contribute to small frequency offsets with respect to the target center frequency. To minimize the risk of tolerance-caused frequency offsets causing a small percentage of production line units to be outside of the acceptable frequency range, it is important to account for those shifts while empirically determining the proper values for the discrete loading capacitors, C1 and C2.

Even with a perfect support circuit, most crystals will oscillate slightly higher or slightly lower than the exact center of the target frequency. Therefore, frequency measurements (which determine the correct value for C1 and C2) should be performed with an ideal reference crystal. When the capacitive load is exactly equal to the crystal's load rating, an ideal reference crystal will be perfectly centered at the desired target frequency.

3.1.3 Reference Crystal Selection

There are several methods available for choosing the appropriate reference crystal:

- If a Saunders and Associates (S&A) crystal network analyzer is available, then discrete crystal components can be tested until one is found with zero or nearly zero ppm deviation (with the appropriate capacitive load). A crystal with zero or near zero ppm deviation will be a good reference crystal to use in subsequent frequency tests to determine the best values for C1 and C2.
- If a crystal analyzer is not available, then the selection of a reference crystal can be done by measuring a statistically valid sample population of crystals, which has units from multiple lots and approved vendors. The crystal, which has an oscillation frequency closest to the center of the distribution, should be the reference crystal used during testing to determine the best values for C1 and C2.
- It may also be possible to ask the approved crystal vendors or manufacturers to provide a reference crystal with zero or nearly zero deviation from the specified frequency when it has the specified CLoad capacitance.

Note: For the 82541EI/GI devices, Intel® recommends choosing a crystal with a ESR value of 20 Ω or less, an equivalent Cload of 18 pF, and a maximum of 30 ppm frequency shift. Cload is defined to be the load capacitance of the crystal, specified by the crystal vendor.

When choosing a crystal, customers must keep in mind that to comply with IEEE specifications for 10/100 and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be precise within ±50 ppm. Intel® recommends customers to use a transmitter reference frequency that is accurate to within ±30 ppm to account for variations in crystal accuracy due to crystal manufacturing tolerance. For information about measuring transmitter reference frequency, refer to Appendix A, "Measuring LAN Reference Frequency Using a Frequency Counter".

3.1.4 Circuit Board

Since the dielectric layers of the circuit board are allowed some reasonable variation in thickness, the stray capacitance from the printed board (to the crystal circuit) will also vary. If the thickness tolerance for the outer layers of dielectric are controlled within ±17 percent of nominal, then the circuit board should not cause more than ±2 pF variation to the stray capacitance at the crystal. When tuning crystal frequency, it is recommended that at least three circuit boards are tested for frequency. These boards should be from different production lots of bare circuit boards.

Alternatively, a larger sample population of circuit boards can be used. A larger population will increase the probability of obtaining the full range of possible variations in dielectric thickness and the full range of variation in stray capacitance.

Next, the exact same crystal and discrete load capacitors (C1 and C2) must be soldered onto each board, and the LAN reference frequency should be measured on each circuit board.

The circuit board, which has a LAN reference frequency closest to the center of the frequency distribution, should be used while performing the frequency measurements to select the appropriate value for C1 and C2.

3.1.5 Temperature Changes

Temperature changes can cause the crystal frequency to shift. Therefore, frequency measurements should be done in the final system chassis across the system’s rated operating temperature range.

3.1.6 Integrated Magnetics Module

The magnetics module has a critical effect on overall IEEE and regulatory conformance. The device should meet the performance required for a design with reasonable margin to allow for manufacturing variation. Occasionally, components that meet basic specifications may cause the system to fail IEEE testing because of interactions with other components or the printed circuit board itself. Carefully qualifying new magnetics modules can go a long way toward preventing this type of problem.

The steps involved in magnetics module qualification are similar to those for oscillator qualification:

1. Verify that the vendor's published specifications in the component datasheet meet the required IEEE specifications.
2. Independently measure the component's electrical parameters on the test bench, checking samples from multiple lots. Check that the measured behavior is consistent from sample to sample as well as meeting the published specifications.
3. Perform physical layer conformance testing and EMC (FCC and EN) testing in real systems. Vary temperature and voltage while performing system level tests (for IEEE only).

Magnetics modules for 1000BASE-T Ethernet are similar to those designed solely for 10/100 Mbps, with the exception of four differential signal pairs instead of two for 10/100 Mbps.

3.2 Designing with the 82562EZ(EX) Platform LAN Connect Device

This section provides design guidelines specific to the PLC device.

3.2.1 82562EZ(EX) PLC Device LAN Disable Guidelines

Note: ICHx Integrated LAN Controller resides on the ICHx VccSus3_3 and VccSus1_8 power wells (typically referred to as “auxiliary” (“aux”) or “standby” supplies at the platform level).

The ICHx Integrated LAN’s RST# is the ICHx Resume-well input. It can be held low indefinitely to keep the ICHx Integrated LAN Controller in a reset state. The LAN Reset (RST#) signal must not be deasserted sooner than 10 ms after the Resume power supply reaches its nominal voltage. This ensures that the ICHx Integrated LAN Controller is initialized. Figure 3 illustrates a possible solution for ICHx Integrated LAN disable.

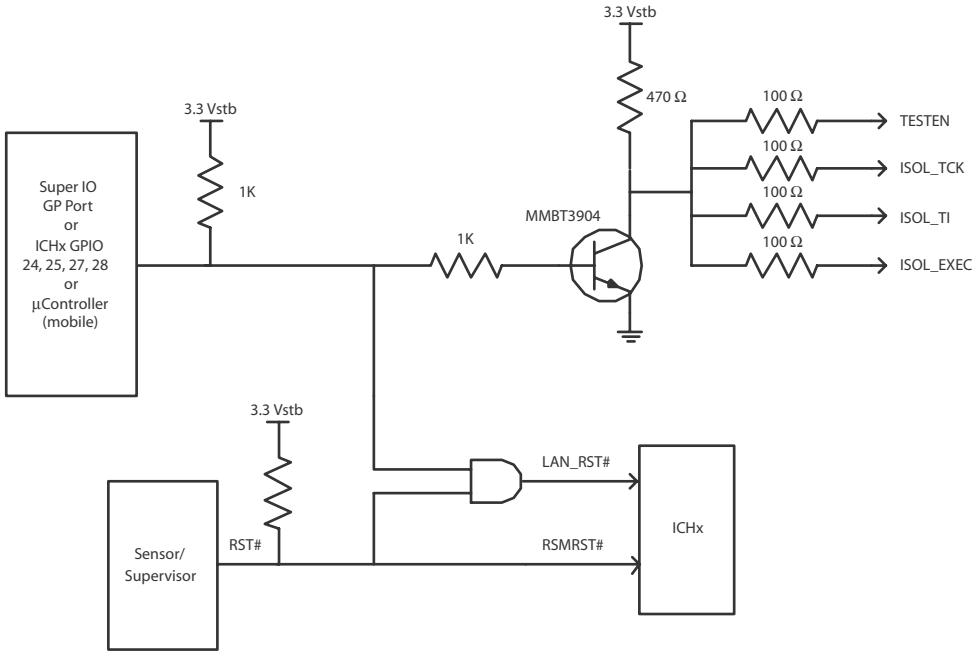


Figure 3. 82562EZ(EX) LAN Disable Circuitry

Note: The 100 Ω resistors for the Test Mode signals are required for the Exclusive OR (XOR) Tree and Isolate Mode.

3.2.2 Serial EEPROM for 82562EZ(EX) Implementations

Serial EEPROM for LAN implementations based on 82562EZ(EX) devices connects to the ICH5. Depending upon the size of the EEPROM, the 82562EZ(EX) may or may not support legacy manageability. Table 5 and Table 6 list the EEPROM map for the 82562EZ(EX) PLC device. For details on the EEPROM, refer to the appropriate *I/O Control Hub 2, 3,4,5, 6, or 7 EEPROM Map and Programming Information*.

Table 5. 82562EZ(EX) Memory Layout (128 Byte EEPROM)

00h **3Fh**	HW/SW Reserved Area

NOTE: No manageability provided.

Table 6. 82562EZ(EX) Memory Layout (512 Byte EEPROM)

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability

3.2.3 Magnetics Modules for 82562EZ(EX) PLC Device

A 5-core magnetics module should be carefully selected for your design. Table 7 lists suggested integrated magnetics modules for use with the 82562EZ(EX) PLC device. These modules also contain integrated USB jacks.

Note: These components are pin-compatible with the magnetics modules listed in Table 11 for the 82541xx controller.

Table 7. 82562EZ(EX) Recommended Magnetics Modules

Manufacturer	Manufacturer's Part Number
Pulse	JW0A1P01R-E
Stewart	SI-70027
Foxconn	UBC11123-J51

3.2.4 Power Supplies for 82562EZ(EX) PLC Implementations

The 82562EZ(EX) PLC device uses a single 3.3 V power supply. The 3.3 V supply must provide approximately 90 mA current for full speed operation. Standby power must be furnished in order to wake up from powerdown.

3.2.5 82562EZ(EX) Device Test Capability

The device contains an XOR test tree mechanism for simple board tests. Details of the XOR tree operation are contained in the *82562ET LAN on Motherboard Design Guide*.

3.3 Designing with the 82541xx Gigabit Controllers

This section provides design guidelines specific to the 82541xx Gigabit Ethernet Controllers.

3.3.1 82541xx Ethernet Controller LAN Disable Guidelines

The 82541xx controller has a LAN disable function that is present on FLSH_SO, ball P9. This pin can be connected to a Super IO component to allow the BIOS to disable the Ethernet port (see Figure 4). If the serial Flash interface is populated, the Flash serial output pin must not interfere with this function.

Do not attempt to use the LAN_POWER_GOOD signal for a LAN disable input on the 82541xx device. This pin is intended to operate as a power-on reset connected to a power monitor circuit.

The input of the 82541xx FLSH_SO (pin P9) is the LAN_DISABLE# signal. It is sampled on the rising edge of LAN_PWR_GOOD or RST#. The signal must be held valid for 80 ns after either rising edge.

If it is sampled high, the LAN functions normally. If it is sampled low, then the following occurs:

1. The LAN is disabled.
2. The PHY is powered down.
3. Most MAC clock domains are gated.
4. Most functional blocks are held in reset.
5. PCI inputs and outputs are floated.
6. The device will not respond to PCI cycles (including configuration cycles).
7. The device is put in a low power state, which is equivalent to D3 without wakeup or manageability.

Note: To use this configuration for the 82562EZ(EX) Platform LAN Connect device, be sure the AND gate U1 is populated. Depopulate the 0 Ω resistor R2.

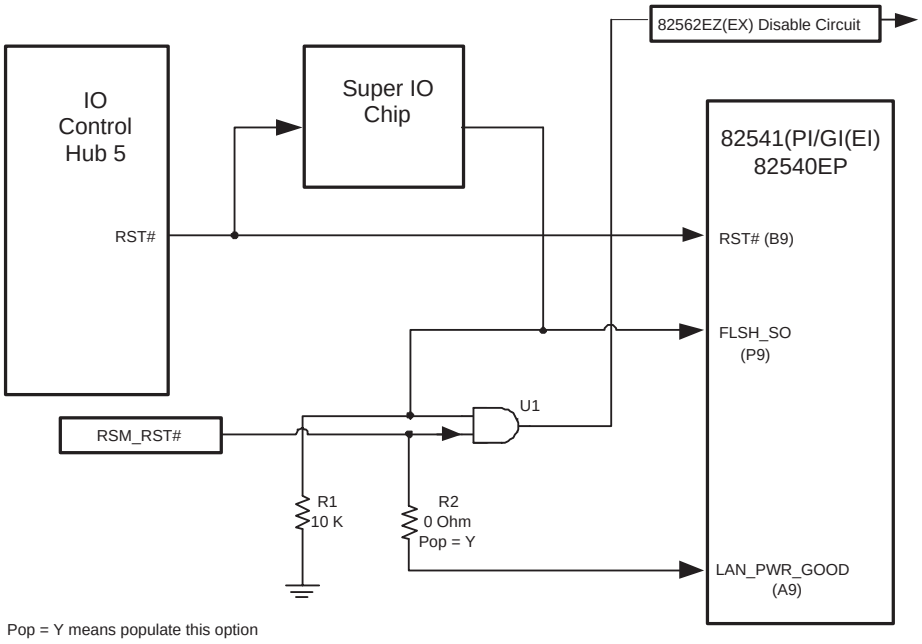


Figure 4. 82541xx LAN Disable Circuitry

3.3.2 Serial EEPROM for 82541xx Controller Implementations

82541xx Gigabit Ethernet Controllers can use either a Microwire* or an SPI* serial EEPROM. The EEPROM mode is selected on the EEMODE input (pin J4). A pull-up resistor to V_{CC} denotes an SPI* EEPROM (82541GI/EI only). A pull-down resistor to ground denotes a Microwire EEPROM. Several words of the EEPROM are accessed automatically by the device after reset to provide pre-boot configuration data before it is accessed by host software. The remainder of the EEPROM space is available to software for storing the MAC address, serial numbers, and additional information.

For non-ASF applications, a 64 register by 16-bit Microwire serial EEPROM should be used, and for ASF 1.0 applications, a larger 93C66 Microwire or AT25040 SPI* serial EEPROM. ASF 2.0 requires an 8 KB SPI* serial EEPROM.

Intel has an MS-DOS* software utility called EEUPDATE, which can be used to program EEPROM images in development or production line environments. To obtain a copy of this program, contact your Intel representative.

The EEPROM access algorithm programmed into the 82541xx controller is compatible with most, but not all, commercially available 3.3 V Microwire* interface, serial EEPROM devices, with 64 x 16 (or 256 x 16) organization and a 1 MHz speed rating. The 82541xx EEPROM access algorithm drives extra pulses on the shift clock at the beginnings and ends of read and write cycles. The extra pulses may violate the timing specifications of some EEPROM devices. In selecting a serial EEPROM, choose a device that specifies “don't care” shift clock states between accesses.

Microwire EEPROMs that have been found to work satisfactorily with the 82541xx Gigabit Ethernet Controller are listed in the following table:

Table 8. Microwire 64 x 16 Serial EEPROMs

Manufacturer	Manufacturer's Part Number
Atmel	AT93C46[1]
Catalyst	CAT93C46[1,2]

1. No manageability provided.
2. Revision H is not supported. Product die revision letter is marked on top of the package as a suffix to the production data code (e.g., AYWW**H**.)

SPI* EEPROMs that have been found to work satisfactorily with the 82541xx device are listed in Table 9. SPI* EEPROMs must be rated for a clock rate of at least 2 MHz.

Table 9. SPI* Serial EEPROMs for 82541xx Controller

Application	Manufacturer	Manufacturer's Part Number
ASF 1.0 or IMPI pass through	ATMEL	AT25040
ASF 2.0 or IMPI advanced pass through	ATMEL	AT25080

3.3.3 EEPROM Map Information

Table 10 lists the EEPROM map for the 82541xx Gigabit Ethernet Controller.

Table 10. 82541xx EEPROM Memory Layout

00h **3Fh**	HW/SW Reserved Area
40h **FFh**	ASF and Legacy Manageability
100h **19F**	Manageability Packet Filter Data
1A0 **...** **EEPROM END**	Loadable Manageability Firmware Code

NOTE: Full manageability provided.

3.3.4 Magnetics Modules for 82541xx Controller Applications

There are several different types of magnetics modules. For example, some magnetics modules have USB connectors or RJ-45 connectors. There are also several discrete modules that can be used for optimal performance. A gigabit magnetics module should be carefully selected for your design.

Table 11 lists suggested integrated magnetics modules for use with the 82541xx device. These modules also contain integrated USB jacks. A good quality Gigabit Ethernet controller can also be used with the 82562EZ(EX) PLC device.

Note: These components are pin-compatible with the magnetics modules shown in Table 7 for the 82562EZ(EX) PLC device.

Table 11. 82541xx Recommended Magnetics Modules

Manufacturer	Manufacturer's Part Number
Pulse (integrated)	JW0A2P019D
Pulse (discrete)	H5007

3.3.5 Oscillators for 82541PI(GI) Controllers

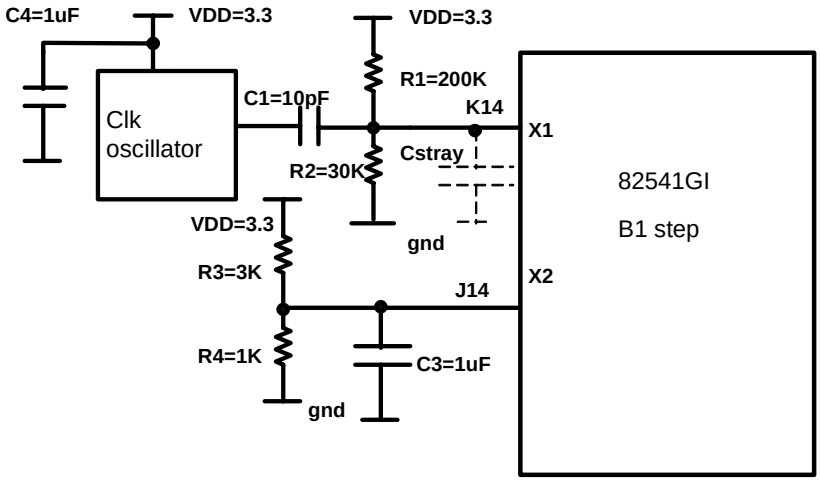
The 82541PI(GI) clock input circuit is optimized for use with an external crystal. However, an oscillator may also be used in place of the crystal with the proper design considerations:

- The clock oscillator has an internal voltage regulator of 1.2 V to isolate it from the external noise of other circuits to minimize jitter. If an external clock is used, this imposes a maximum input clock amplitude of 1.2 V.
- The input capacitance introduced by the 82541PI(GI) (approximately 20 pF) is greater than the capacitance specified by a typical oscillator (approximately 15 pF).
- The input clock jitter from the oscillator can impact the 82541PI(GI) clock and its performance.

Table 12. 82541PI(GI) Clock Oscillator Specifications

Symbol	Parameter	Specifications			Units
		Min	Typical	Max	
f0	Frequency		25		MHz
df0	Frequency Variation	-50		+30	ppm
Dc	Duty Cycle	40		60	%
tr	Rise Time			5	ns
tf	Fall Time			5	ns
σi	Clock Jitter, rms (if specified)			50	ps
C1	Clock Capacitance (pushed by clock)		15	50	pF
VDD	Supply Voltage		3.3 or 1.8		V
Operating temperature				70	° C
CMOS output levels	Voltage Output High (Voh), Voltage Output Low (Vol)	80% VDD		 20% VDD	V V

3.3.5.1 82541GI (B1 Stepping) Oscillator Solution



The oscillator solution for the 82541GI includes capacitor C1, which forms a capacitor divider with capacitor C_{stray} of approximately 20 pF. This attenuates the input clock amplitude and adjusts the oscillator load capacitance where

$$V_{in} = VDD * (C1/(C1 + C_{stray}))$$
$$V_{in} = 3.3 * (C1/(C1 + C_{stray}))$$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

The architecture of the 82541 crystal oscillator requires a differential clock on the X1 and X2 input signals or a single ended clock input on the X1 pin with common mode biasing of the X2 pin. A relatively low drive strength of the 82541GI crystal driver does not guarantee the differential X1 and X2 inputs with a single ended external clock oscillator. Therefore, the resistive common mode bias circuitry should be added to produce a common mode voltage (V_{CM}) of approximately 0.6 V on the X2 pin. The resistive divider (R3 and R4) and the decoupling capacitor (C3) are required to form and stabilize the biasing circuit for the X2 pin. The resistive divider R1 and R2 produces a V_{CM} of about 0.6 V for the input clock of the X1 pin.

Note: The resistor tolerance should be within ±10%.

Note: The power consumption of additional circuitry equals about 1.5 mW.

3.3.5.2 82541PI (C0 Stepping) Oscillator Solution

There are two oscillator solutions for the 82541PI: high voltage and low voltage.

High Voltage Solution (VDD = 3.3 V)

This solution involves capacitor C1, which forms a capacitor divider with C_{stray} of about 20 pF. This attenuates the input clock amplitude and adjusts the clock oscillator load capacitance.

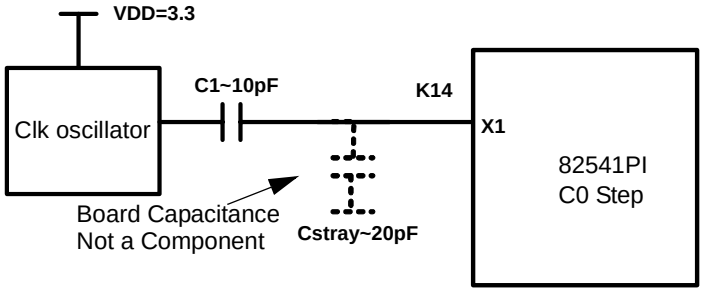
$V_{in} = VDD * (C1/(C1 + C_{stray}))$

$V_{in} = 3.3 * (C1/(C1 + C_{stray}))$

This enables load clock oscillators of 15 pF to be used. If the value of C_{stray} is unknown, C1 should be adjusted by tuning the input clock amplitude to approximately 1 V_{ptp}. If C_{stray} equals 20 pF, then C1 is 10 pF ±10%.

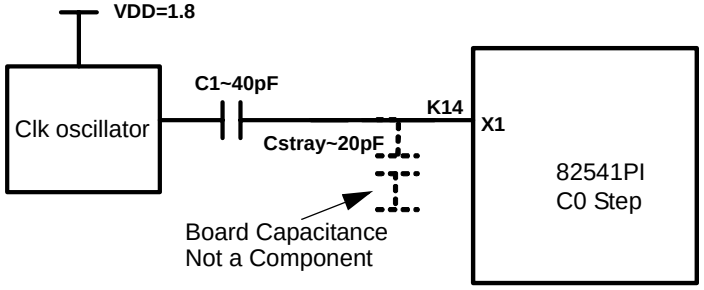
A low capacitance, high impedance probe (C < 1 pF, R > 500 K Ω) should be used for testing. Probing the parameters can affect the measurement of the clock amplitude and cause errors in the adjustment. A test should also be done after the probe has been removed for circuit operation.

If jitter performance is poor, a lower jitter clock oscillator can be implemented.



Low Voltage Solution (VDD = 1.8 V)

The low voltage solution is similar to the high voltage solution. However, the low voltage includes a low consumption and low jitter clock oscillator that uses a 1.8 V external power supply. In this case, C1 will require adjusting according to the stray capacitance from X1.



3.3.6 Power Supplies for the 82541xx Controller

The 82541xx controller requires three power supplies: 1.2 V, 1.8 V, and 3.3 V. The 1.2 V supply must provide approximately 500 mA current, and the 1.8 V supply, approximately 230 mA current. The 3.3 V supply must provide only 30 mA current.

A central power supply can provide all the required voltage sources, or the power can be derived and regulated locally near the Ethernet control circuitry. All voltage sources must remain present during powerdown in order to use the 82541xx LAN wake up capability. This consideration makes it more likely that at least some of the voltage sources will be local.

Instead of using external regulators to supply 1.2 V and 1.8 V, power transistors can be used in conjunction with on-chip regulation circuitry. (See the reference schematic for an implementation example.)

The 82541xx controller has a LAN_PWR_GOOD input. Treat this signal as an external device reset which works in conjunction with the internal power-on reset circuitry. In the situation where a central power supply furnishes all the voltage sources, LAN_PWR_GOOD can be tied to the POWER_GOOD output of the power supply. Designs that generate some of the voltages locally can connect LAN_PWR_GOOD to a power monitor chip.

The power sources are all expected to ramp up during a brief power-up interval (approximately 20 ms) with LAN_PWR_GOOD de-asserted. The 82541xx controller must not be left in a prolonged state where some, but not all, voltages are applied. The 3.3 V source should be powered up prior to the 1.2 V or 1.8 V sources. The 1.2 V and 1.8 V power supplies may power up simultaneously. At any time during power up, the supply voltages must be: 1.2 V < 1.8 V < 3.3 V.

3.3.7 82541xx Controller Power Supply Filtering

The 82541xx controller switches relatively high currents at high frequencies, requiring generous use of both bulk capacitance and high speed decoupling capacitance adjacent to the device.

Bypass capacitors for each power rail should be 0.1 µF. If possible, orient the capacitors close to the device and adjacent to power pads. Decoupling capacitors should connect to the power and ground planes with short, thick traces (15 mils or 0.4 mm or more), and 14 mil (3.5 mm) vias per capacitor pad.

Furnish approximately 20 µF of bulk capacitance for each of the main 1.2 V and 1.8 V levels. This can be easily achieved by using two 10 µF capacitors, placing them as close to the device power connections as possible.

3.3.8 82541xx Controller Power Management and Wake Up

The 82541xx Gigabit Ethernet Controller supports low power operation as defined in the PCI Bus Power Management Specification. There are two defined power states, D0 and D3. The D0 state provides full power operation and is divided into two sub-states: D0u (uninitialized) and D0a (active). The D3 state provides low power operation and is also divided into two sub-states: D3hot and D3cold.

To enter the low power state, the software driver must stop data transmission and reception. Either the operating system or the driver must program the Power Management Control/Status Register (PMCSR) and the Wakeup Control Register (WUC). If wakeup is desired, the appropriate wakeup LAN address filters must also be set. The initial power management settings are specified by EEPROM bits.

When the 82541xx controller transitions to either of the D3 low power states, the 1.2 V, 1.8 V, and 3.3 V sources must continue to be supplied to the device. Otherwise, it will not be possible to use a wakeup mechanism. The AUX_POWER signal is a logic input to the 82541xx controller that denotes auxiliary power is available. If AUX_POWER is asserted, the 82541xx device will advertise that it supports wake up from a D3cold state.

The 82541xx device supports both Advanced Power Management (APM) wakeup and Advanced Configuration and Power Interface (ACPI) wakeup. APM wakeup has also been known in the past as “Wake on LAN.”

Wakeup uses the PME# signal to wake the system. PME# is an active low signal connected to a GPIO port on the ICH5 that goes active in response to receiving a Magic Packet*, a network wake-up packet, or link status change indication. PME# remains asserted until it is disabled through the Power Management Control/Status Register.

3.3.9 82541xx Device Test Capability

The 82541xx Gigabit Ethernet Controller contains a test access port conforming to the IEEE 1149.1a-1994 (JTAG) Boundary Scan specification. To use the test access port, these balls need to be connected to pads accessible by the test equipment. The TRST# input also needs to be connected to ground through a pull-down resistor (approximately 1 K Ω value for the 82541GI(EI) and 100 Ω for the 82541PI) so that the test capability cannot be invoked by mistake.

A Boundary Scan Definition Language (BSDL) file describing the 82541xx device is available for use in your test environment.

The controller also contains an XOR test tree mechanism for simple board tests. Details of XOR tree operation may be obtained through your Intel representative.

4.0 Ethernet Component Layout Guidelines

These sections provide recommendations for performing printed circuit board layouts. Good layout practices are essential to meet IEEE PHY conformance specifications and EMI regulatory requirements.

4.1 General Layout Considerations for Ethernet Controllers

Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals, including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading.

Since the transmission line medium extends onto the printed circuit board, special attention must be paid to layout and routing of the differential signal pairs.

Designing for Gigabit operation is very similar to designing for 10/100 Mbps. For the 82541xx Gigabit Ethernet Controller, system level tests should be performed at all three speeds.

4.1.1 Guidelines for Component Placement

Component placement can affect signal quality, emissions, and component operating temperature. This section provides guidelines for component placement. Careful component placement can:

- Decrease potential problems directly related to Electromagnetic Interference (EMI), which could cause failure to meet applicable government test specifications.
- Simplify the task of routing traces. To some extent, component orientation will affect the complexity of trace routing. The overall objective is to minimize turns and crossovers between traces.

Minimizing the amount of required space for the Ethernet LAN interface is important because other interfaces will compete for physical space on a motherboard near the connector. The Ethernet LAN circuits need to be as close as possible to the connector (see Figure 5).

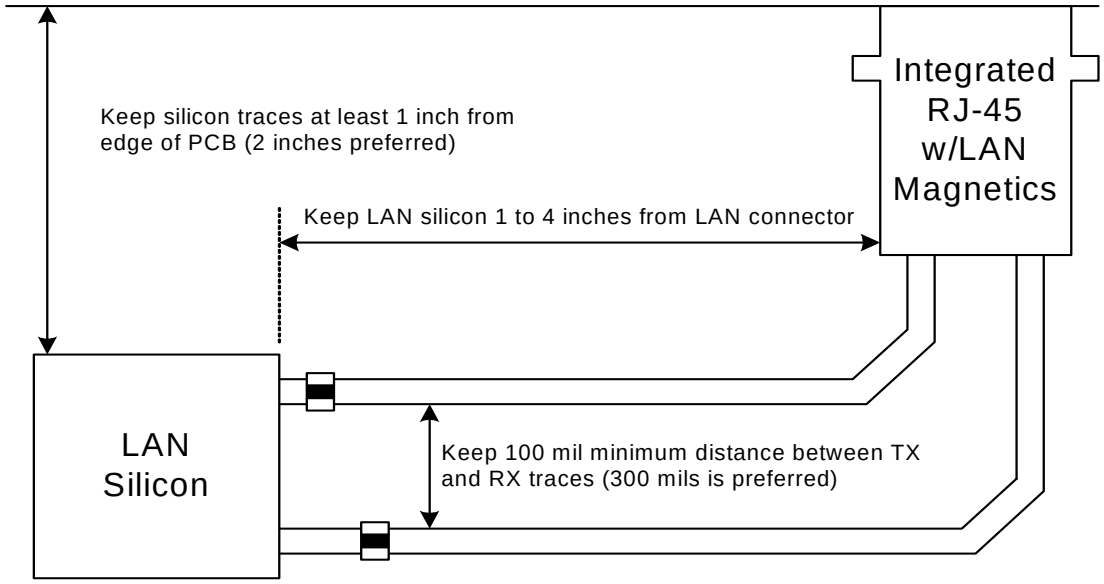


Figure 5. General Placement Distances

Figure 5 shows some basic placement distance guidelines. The figure shows two differential pairs, but can be generalized for a Gigabit system with four analog pairs. The ideal placement for the Ethernet silicon would be approximately one inch behind the magnetics module.

While it is generally a good practice to minimize lengths and distances, this figure also illustrates the need to keep the LAN silicon away from the edge of the board and the magnetics module for best EMI performance.

4.1.2 Crystals

Crystals should not be placed near I/O ports or board edges. Radiation from these devices may be coupled onto the I/O ports or out of the system chassis. Crystals should also be kept away from the Ethernet magnetics module to prevent interference. Traces should be referenced to a continuous, low impedance plane.

Place the crystal and load capacitors on the printed circuit boards as close to the Ethernet component as possible, within 0.75 inch. Keep other potentially noisy traces away from the crystal traces.

4.1.3 Board Stackup Recommendations

Printed Circuit Boards (PCBs) for these designs typically have four, six, eight, or more layers. Following is a description of a typical four-layer board stackup:

- Layer 1 is a signal layer. It can contain the differential analog pairs from the Ethernet device to the magnetics module.
- Layer 2 is a signal ground layer. Chassis ground may also be fabricated in Layer 2 under the connector side of the magnetics module.
- Layer 3 is used for power planes.
- Layer 4 is a signal layer.

This board stackup configuration can be adjusted to conform to an OEM's design rules.

4.1.4 Differential Pair Trace Routing

Trace routing considerations are important to minimize the effects of crosstalk and propagation delays on sections of the board where high-speed signals exist. Signal traces should be kept as short as possible to decrease interference from other signals, including those propagated through power and ground planes. Observe the following suggestions to help optimize board performance:

- Maintain constant symmetry and spacing between the traces within a differential pair.
- Keep the signal trace lengths of a differential pair equal to each other. Do not use serpentines to try to match trace lengths in the differential pair. Serpentines cause impedance variations causing signal reflections, which can be a source of signal distortion. Try to keep the length difference of the differential pair less than 100 mil (~15 pS). Always go straight to the required via or pad.
- Keep the total length of each differential pair under four inches. Designs with differential traces longer than five inches are much more likely to have degraded receive Bit Error Rate (BER) performance, IEEE PHY conformance failures, or excessive Electromagnetic Interference (EMI) radiation.
- Do not route the transmit differential traces closer than 100 mils to the receive differential traces for 10/100 Mbps.
- Do not route any other signal traces (including other differential pairs) parallel to the differential traces and closer than 100 mils to the differential traces.
- Separate traces within a differential pair as small as possible down to five to eight mils. Close separation of the traces allows the traces to couple well to each other.
- For high-speed signals, the number of corners and vias should be kept to a minimum. If a 90° bend is required, it is recommended to use two 45° bends instead. (see Figure 6.)

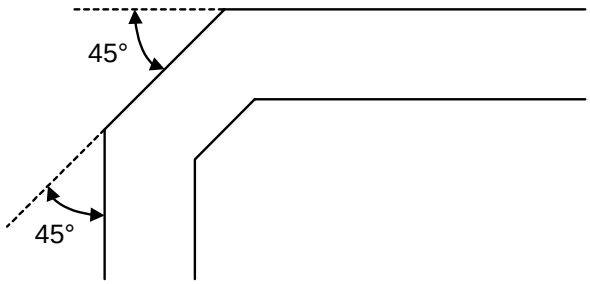


Figure 6. Trace Routing

- Traces should be routed away from board edges by a distance greater than the trace height above the ground plane. This allows the field around the trace to couple more easily to the ground plane rather than to adjacent wires or boards.
- Do not route traces and vias under crystals or oscillators. This will prevent coupling to or from the clock. And as a general rule, place traces from clocks and drives at a minimum distance from apertures by a distance that is greater than the largest aperture dimension.
- The reference plane for the differential pairs should be continuous and low impedance. It is recommended that the reference plane be either ground or 1.8 V (the voltage used by the PHY). This provides an adequate return path for any high frequency noise currents.
- Do not route differential pairs over splits in the associated reference plane.
- Differential termination components should be placed as close as possible to the LAN silicon.

4.1.5 Signal Trace Geometry

The key factors in controlling trace EMI radiation are the trace length and the ratio of trace-width to trace-height above the ground plane. To minimize trace inductance, high-speed signals and signal layers that are close to a ground or power plane should be as short and wide as practical. Ideally, this trace width to height above the ground plane ratio is between 1:1 and 3:1. To maintain trace impedance, the width of the trace should be modified when changing from one board layer to another if the two layers are not equidistant from the power or ground plane.

Each pair of signals should have a differential impedance of 100 Ω ±20%. If a particular tool cannot design differential traces, it is permissible to specify 55 to 65 Ω single-ended traces as long as the spacing between the two traces is minimized. As an example, consider a differential trace pair on Layer 1 that is eight mils (0.2 mm) wide and two mils (0.05 mm) thick, with a spacing of eight mils (0.2 mm). If the fiberglass layer is eight mils (0.2 mm) thick with a dielectric constant, E_R, of 4.7, the calculated single-ended impedance would be approximately 61 Ω and the calculated differential impedance would be approximately 100 Ω.

When performing a board layout, do not allow the CAD tool auto-router to route the differential pairs without intervention. In most cases, the differential pairs will have to be routed manually. The components should be laid out in the following order of priority:

1. Differential traces
2. Termination resistors
3. Bypass capacitors
4. Other components

This allows placing those components in the best locations and avoids using critical space by non-critical components.

Note: Measuring trace impedance for layout designs targeting 100 Ω often results in lower actual impedance. Designers should verify actual trace impedance and adjust the layout accordingly. If the actual impedance is consistently low, a target of 105 to 110 Ω should compensate for second order effects.

It is necessary to compensate for trace-to-trace edge coupling, which can lower the differential impedance by up to 10 Ω, when the traces within a pair are closer than 30 mils (edge to edge).

4.1.6 Trace Length and Symmetry

As indicated earlier in Section 4.1.4, the overall length of differential pairs should be less than four inches measured from the Ethernet device to the magnetics.

The differential traces should be equal within 50 mils (1.25 mm) within each pair and as symmetrical as possible. Asymmetrical and unequal length traces in the differential pairs contribute to common mode noise. Common mode noise can degrade the receive circuit's performance and contribute to radiated emissions.

4.1.7 Impedance Discontinuities

Impedance discontinuities cause unwanted signal reflections. Avoid vias (signal through holes) and other transmission line irregularities. If vias must be used, a reasonable budget is two per differential trace. Unused pads and stub traces should also be avoided.

4.1.8 Reducing Circuit Inductance

Traces should be routed over a continuous ground plane with no interruptions. If there are vacant areas on a ground or power plane, the signal conductors should not cross the vacant area. This increases inductance and associated radiated noise levels. Noisy logic grounds should be separated from analog signal grounds to reduce coupling. Noisy logic grounds can sometimes affect sensitive DC subsystems such as analog to digital conversion, operational amplifiers, etc. All ground vias should be connected to every ground plane; and similarly, every power via, to all power planes at equal potential. This helps reduce circuit inductance. Another recommendation is to physically locate grounds to minimize the loop area between a signal path and its return path. Rise and fall times should be as slow as possible. Because signals with fast rise and fall times contain many high frequency harmonics, which can radiate significantly. The most sensitive signal returns closest to the chassis ground should be connected together. This will result in a smaller loop area and reduce the likelihood of crosstalk. The effect of different configurations on the amount of crosstalk can be studied using electronics modeling software.

4.1.9 Signal Isolation

To maintain best signal integrity, keep digital signals far away from the analog traces. A good rule of thumb is no digital signal should be within 300 mils (7.5 mm) of the differential pairs. If digital signals on other board layers cannot be separated by a ground plane, they should be routed at right angles with respect to the differential pairs. If there is another LAN controller on the board, take care to keep the differential pairs from that circuit away.

Some rules to follow for signal isolation:

- Separate and group signals by function on separate layers if possible. Maintain a gap of 100 mils between all differential pairs (Ethernet) and other nets, but group associated differential pairs together. Over the length of the trace run, each differential pair should be at least 0.1 inch away from any parallel signal traces.
- Physically group together all components associated with one clock trace to reduce trace length and radiation.
- Isolate I/O signals from high-speed signals to minimize crosstalk, which can increase EMI emission and susceptibility to EMI from other signals.
- Avoid routing high-speed LAN traces near other high-frequency signals associated with a video controller, cache controller, processor, or other similar devices.

4.1.10 Power and Ground Planes

Good grounding requires minimizing inductance levels in the interconnections and keeping ground returns short, signal loop areas small, and power inputs bypassed to signal return, will significantly reduce EMI radiation.

The following guidelines help reduce circuit inductance in both back planes and motherboards:

- Route traces over a continuous plane with no interruptions. Do not route over a split power or ground plane. If there are vacant areas on a ground or power plane, avoid routing signals over the vacant area. This will increase inductance and EMI radiation levels.
- Separate noisy digital grounds from analog grounds to reduce coupling. Noisy digital grounds may affect sensitive DC subsystems.
- All ground vias should be connected to every ground plane and every power via should be connected to all power planes at equal potential. This helps reduce circuit inductance.
- Use vias in pairs. Two (or more) small vias have less inductance and are preferable over large vias. The small vias may also require less board space.
- Physically locate grounds between a signal path and its return. This will minimize the loop area.
- Avoid fast rise/fall times as much as possible. Signals with fast rise and fall times contain many high frequency harmonics, which can radiate EMI.
- The ground plane beneath the magnetics module should be split. The RJ-45 connector side of the transformer module should have chassis ground beneath it.
- Power planes are not recommended as reference (or AC ground) planes for the differential since most of them are noisy and can contaminate signals.

4.1.11 Traces for Decoupling Capacitors

Traces between decoupling and I/O filter capacitors should be as short and wide as practical. Long and thin traces are more inductive and would reduce the intended effect of decoupling capacitors. Also for similar reasons, traces to I/O signals and signal terminations should be as short as possible. Vias to the decoupling capacitors should be sufficiently large in diameter to decrease series inductance.

4.1.12 Ground Planes Under the Magnetics Module

The magnetics module chassis or output ground (secondary side of transformer) should be separated from the digital or input ground (primary side) by a physical separation of 100 mils minimum. Splitting the ground planes beneath the transformer minimizes noise coupling between the primary and secondary sides of the transformer and between the adjacent coils in the magnetics. This arrangement also improves the common mode choke functionality of magnetics module.

Figure 7 illustrates the split plane layout for a discrete magnetics module. Capacitors are used to interconnect chassis ground and signal ground.

.

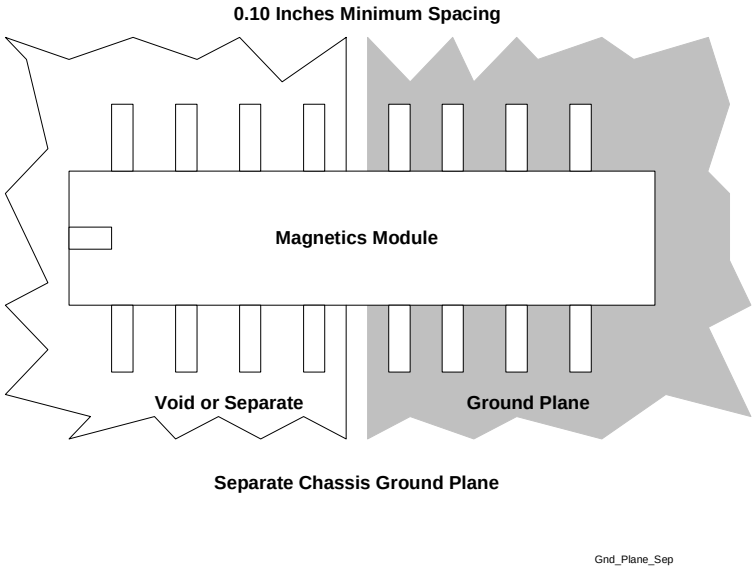


Figure 7. Ground Plane Separation

Figure 8 below shows the preferred method for implementing a ground split under an integrated magnetics module/RJ-45 connector. The capacitor stuffing options (C1 through C6) are used to reduce/filter high frequency emissions. The value(s) of the capacitor stuffing options may be different for each board. Experiments will need to be performed to determine which value(s) provide best EMI performance.

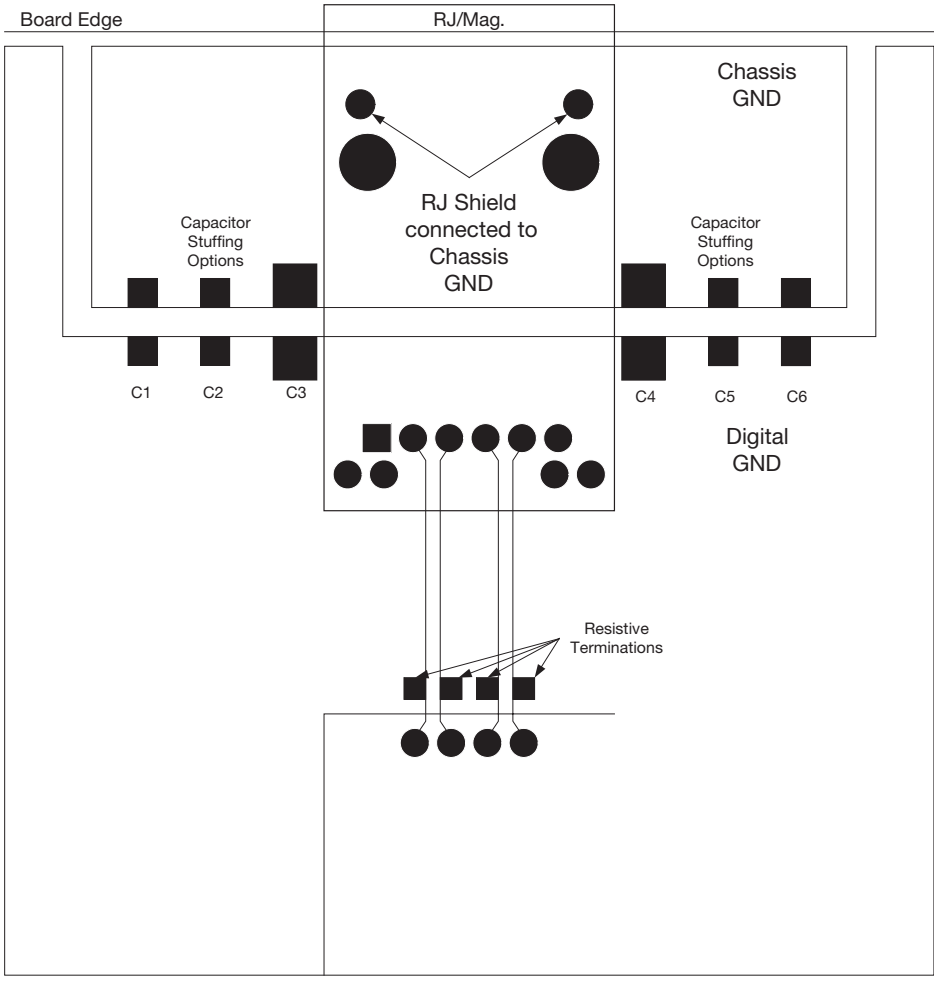


Figure 8. Ideal Ground Split Implementation

The following table lists the reference starting values for these capacitors.

Capacitors	Value
C3, C4	4.7µF or 10 µF
C1, C2, C5, C6	470 pF to 0.1 µF

The placement of C1 through C6 may also be different for each board design (in other words, not all of the capacitors may need to be populated). Also, the capacitors may not be needed on both sides of the magnetics module.

Systems with integrated USB ports on the magnetics module may have difficulty using a chassis ground configuration due to the need to get DC ground to certain USB pins. One technique is to fabricate an incomplete ground split (partially open on one end). By connecting the ground planes around the RJ magnetics module through a slim, high impedance connection, the path of the high frequency noise can be controlled.

4.1.13 Non-Integrated Magnetics Modules and RJ-45 Connectors

It is possible to employ discrete (non-integrated) magnetics modules and RJ-45 connectors. Similar rules will apply to design and layout. The differential pairs should be routed to be as short and symmetrical as possible and the overall lengths of the differential pairs (including the width of the magnetics module) should not exceed approximately four inches.

Additional design and layout steps will be required to add a dedicated board termination plane parallel to chassis ground, 75 Ω termination resistors, and a 1500 pF capacitor. This “Bob Smith” termination scheme is normally contained inside an integrated magnetics module. The 75 Ω termination resistors are required to terminate the common mode of the twisted pairs that behave as a transmission line. These resistors help ensure that emission requirements are met.

In Ethernet designs, it is common practice to terminate unused connections on the RJ-45 connector and the magnetics module to ground. Depending on overall shielding and grounding design, this may be done to the chassis ground, signal ground, or a termination plane. Care must be taken when using various grounding methods to insure that emission requirements are met. In the “Bob Smith” termination method, a floating termination plane is cut out of a power plane layer. This floating plane acts as a plate of a capacitor with an adjacent ground plane. The signals can be routed through 75 Ω resistors to the plane. Stray energy on unused pins is then carried to the plane.

It is recommended that the termination plane capacitance equal a minimum value of 1500 pF. This helps reduce the amount of crosstalk on the differential pairs from the unused pairs of the RJ-45 connector. Pads may be placed for an additional capacitance to chassis ground, which may be required if the termination plane capacitance is not large enough to pass Electrical Fast Transient (EFT) testing. If a discrete capacitor is used, it should be rated for at least 1000 Vac to meet the EFT requirements.

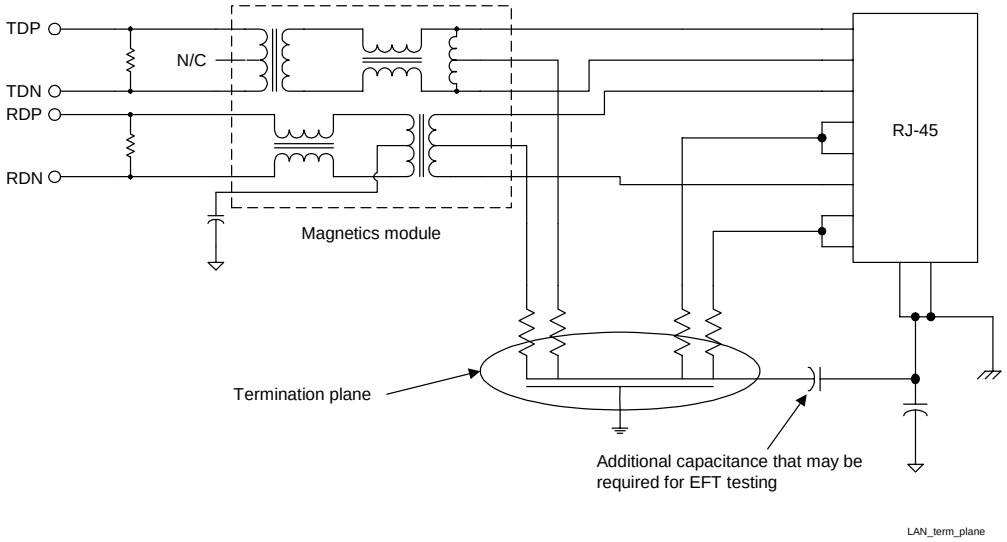


Figure 9. Termination Plane Example for 82562EZ(EX) PLC Device and Discrete Magnetics

4.2 Layout for the 82562EZ(EX) PLC Device

This section provides layout guidelines specific to the 82562EZ(EX) PLC device.

4.2.1 Termination Resistors for Designs Based on 82562EZ(EX) PLC

Two differential pairs are terminated using 54.9 Ω (1% tolerance) resistors, placed near the LAN controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace (see Figure 10).

Termination resistor values were recently increased from 49.9 Ω to 54.9 Ω to improve return loss. However, on some designs, this change caused the PCB's output amplitude to be slightly above the peak-to-peak center of the IEEE specification. As a result, RBIAS resistor values were increased (RBIAS10 549 to 619 Ω and RBIAS100 619 to 649 Ω) to reduce the PCB's output amplitude to better meet the IEEE peak-to-peak center specification.

For 100Base-TX designs, the IEEE specification allows a -950 mVpk to -1050 mVpk for the negative peak and +950 mVpk to +1050 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -975 mVpk to -1025 mVpk for the negative peak and +975 mVpk to +1025 mVpk for the positive peak.

For 10Base-T designs, the IEEE specification allows a -2.2 mVpk to -2.8 mVpk for the negative peak and +2.2 mVpk to +2.8 mVpk for the positive peak. Ideally, a typical PCB output amplitude should be within -2.35 mVpk to -2.55 mVpk for the negative peak and +2.35 mVpk to +2.55 mVpk for the positive peak.

The RBIAS values previously listed should be considered starting values. Intel recommends that board designers measure each of their PCB's output amplitude and then adjust the RBIAS values as required.

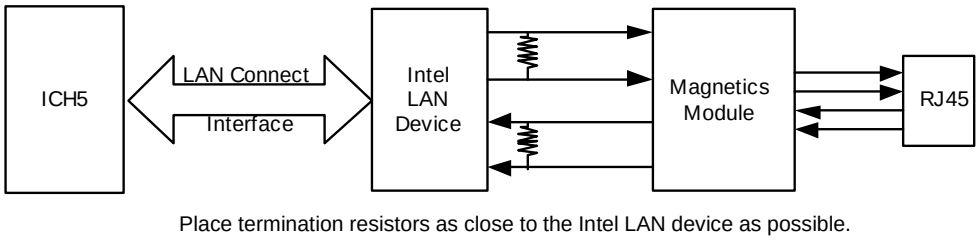


Figure 10. 82562EZ(EX) PLC Device Differential Signal Termination

4.2.2 Light Emitting Diodes for Designs Based on 82562EZ(EX) PLC

The 82562EZ(EX) PLC device has three high-current outputs to directly drive LEDs for link, activity and speed indication. Since LEDs are likely to be integral to a magnetics module, take care to route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

4.3 Layout for the 82541xx Gigabit Ethernet Controller

4.3.1 Termination Resistors for Designs Based on 82541xx

The four differential pairs are terminated with 49.9 Ω (1% tolerance) resistors, placed near the 82541xx controller. One resistor connects to the MDI+ (MDI positive) signal trace and another resistor connects to the MDI- (MDI negative) signal trace. The opposite ends of the resistors, using a wide trace, connect together and to ground through a single 0.1 µF capacitor. The capacitor should be placed as close as possible to the 49.9 Ω resistors using a wide trace.

Do not vary the suggested component values. Be sure to lay out symmetrical pads and traces for these components such that the length and symmetry of the differential pairs are not disturbed.

4.3.2 Light Emitting Diodes for Designs Based on 82541xx

The 82541xx controller provides four programmable high-current outputs to directly drive LEDs for link activity and speed indication. Since the LEDs are likely to be integral to a magnetics module, route the LED traces away from potential sources of EMI noise. In some cases, it may be desirable to attach filter capacitors.

4.4 Physical Layer Conformance Testing

Physical layer conformance testing (also known as IEEE testing) is a fundamental capability for all companies with Ethernet LAN products. PHY testing is the final determination that a layout has been performed successfully. If your company does not have the resources and equipment to perform these tests, consider contracting the tests to an outside facility.

Crucial tests are as follows, listed in priority order:

1. Bit Error Rate (BER). This test is a good indicator of real world network performance. It should be done with long and short cables and many link partners. The test limit is 10 to 11 errors (10/100/1000 Mbps).
2. Output Amplitude, Rise and Fall Time (10/100 Mbps), Symmetry and Droop (1000 Mbps). For the 82541xx controller, use the appropriate PHY test waveform.
3. Return Loss. This test indicates proper impedance matching, measured through the RJ-45 connector back toward the magnetics module.
4. Jitter Test (10/100 Mbps) or Unfiltered Jitter Test (1000 Mbps). This test indicates clock recovery ability (master and slave for Gigabit controller).
5. Harmonic Content for 10 Mbps.
6. Output Symmetry for 100/1000 Mbps.
7. Rise and Fall Time for 100 Mbps.
8. Droop for 1000 Mbps.
9. Duty Cycle Distortion for 100 Mbps.

4.5 Troubleshooting Common Physical Layout Issues

The following is a list of common physical layer design and layout mistakes in LAN on Motherboard designs.

1. Unequal length of the two traces within a differential pair. Inequalities create common-mode noise and will distort the transmit or receive waveforms.
2. Lack of symmetry between the two traces within a differential pair. Asymmetry can create common-mode noise and distort the waveforms. For each component or via that one trace encounters, the other trace should encounter the same component or a via at the same distance from the Ethernet silicon.
3. Excessive distance between the Ethernet silicon and the magnetics. Long traces on FR4 fiberglass epoxy substrate will attenuate and distort the analog signals. In addition, any impedance mismatch in the traces will be aggravated if they are longer than the four inch rule.
4. Routing any other trace parallel to and close to one of the differential traces. Crosstalk getting onto the receive channel will cause degraded long cable BER. Crosstalk getting onto the transmit channel can cause excessive EMI emissions and can cause poor transmit BER on long cables. At a minimum, other signals should be kept 0.1 inch from the differential traces.
5. Routing one pair of differential traces too close to another pair of differential traces. After exiting the Ethernet silicon, the trace pairs should be kept 0.1 inch or more away from the other trace pairs. The only possible exceptions are in the vicinities where the traces enter or exit the magnetics, the RJ-45 connector, and the Ethernet silicon.
6. Using a low quality magnetics module.
7. Re-use of an out-of-date physical layer schematic in an Ethernet silicon design. The terminations and decoupling can be different from one PHY to another.

8. Incorrect differential trace impedances. It is important to have approximately 100 Ω impedance between the two traces within a differential pair. This becomes even more important as the differential traces become longer. To calculate differential impedance, many impedance calculators only multiply the single-ended impedance by two. This does not take into account edge to edge capacitive coupling between the two traces or other edge effects. When the two traces within a differential pair are kept close to each other, the edge coupling can lower the effective differential impedance by 5 Ω to 20 Ω. Short traces will have fewer problems if the differential impedance is slightly off target.
9. For 82562EZ(EX) PLC designs, use of capacitor that is too large between the transmit traces or too much capacitance on the magnetics module's transmit center tap to ground. Using capacitors more than a few picoFarads in either of these locations can slow the 100 Mbps rise and fall time. This will also cause return loss to fail at higher frequencies and will degrade the transmit BER performance. If capacitors are used, the total of all capacitors placed on the transmit traces and the center tap should equal less than 22 pF.

Note: This page intentionally left blank.

5.0 Design and Layout Checklists

The Design and Layout Checklists are in Portable Data Format (PDF) and available to aid designers via http://developer.intel.com. at:

http://www.intel.com/design/network/products/lan/docs/82541pi_docs.htm

Note: This page intentionally left blank.

6.0 Ball Number to Signal Mapping with Population Options

Table 13 below shows the ball names for both devices corresponding to the shared ball number. The signal names may vary slightly from the names in Section 7.0 since the names used in the reference schematics follow conventions used by Intel design engineers on their design tools.

Table 13. Ball Number to Signal Mapping (Sheet 1 of 8)

						Population Options			
Ball Ref	**82541xx Pin Name**	**82540EP Pin Name**	**82562EZ Pin Name**	**D[1]**	**K[2]**	**82541xx**	**82540EP**	**82562EZ**	**Comments**
A1	NC	NC	NC						
A2	SERR#	SERR#	NC	X		SERR#	SERR#	SERR#	
A3	3.3 V	3.3 V	3.3 V						
A4	IDSEL	IDSEL	NC	X		IDSEL	IDSEL	IDSEL	
A5	AD[25]	AD[25]	NC	X		AD[25]	AD[25]	AD[25]	
A6	PME#	PME#	NC	X		PME#	PME#	PME#	
A7	3.3 V	3.3 V	3.3 V						
A8	AD[30]	AD[30]	NC	X		AD[30]	AD[30]	AD[30]	
A9	LAN_PWR_ GOOD	LAN_PWR_ GOOD	NC	X		Supervisor IC	Supervisor IC	No stuff	
A10	SMBCLK	SMBCLK	NC	X		SMBCLK	SMBCLK	SMBCLK	
A11	3.3 V	3.3 V	VCCT	X	X	3.3 V	3.3 V	3.3 V	VCCT = 3.3 V
A12	LED0/LINK_UP#	LINK_UP#	LILED#	X	X	LINK_LED	LINK_LED	LINK_LED	Same signal - different names.
A13	TEST	TEST	TESTEN	X	X	Pull-down	Pull-down	Pull-down	May have LAN Disable logic connected to this signal for 82562EZ(EX).
A14	NC	NC	NC						
B1	AD[22]	AD[22]	NC	X		AD[22]	AD[22]	AD[22]	
B2	AD[23]	AD[23]	NC	X		AD[23]	AD[23]	AD[23]	
B3	VSS	VSS	VSS						
B4	AD[24]	AD[24]	NC	X		AD[24]	AD[24]	AD[24]	
B5	AD[26]	AD[26]	NC	X		AD[26]	AD[26]	AD[26]	
B6	AD[27]	AD[27]	NC	X		AD[27]	AD[27]	AD[27]	
B7	VSS	VSS	VSS						
B8	AD[31]	AD[31]	NC	X		AD[31]	AD[31]	AD[31]	
B9	RST#	RST#	NC	X		RST#	RST#	RST#	
B10	SMB_ALERT#/ LAN_PWR_ GOOD	SMB_ALERT#	NC	X		SMB_ALERT#	SMB_ALERT#	SMB_ALERT#	
B11	LED2/LINK100#	LINK100#	SPDLED#	X	X	LED	LED	LED	Same signal - different names.

Table 13. Ball Number to Signal Mapping (Sheet 2 of 8) (Continued)

						Population Options			
Ball Ref	**82541xx Pin Name**	**82540EP Pin Name**	**82562EZ Pin Name**	**D[1]**	**K[2]**	**82541xx**	**82540EP**	**82562EZ**	**Comments**
B12	LED3/LINK1000#	LINK1000#	TOUT	X	X	LED	LED	No stuff	Testability output for 82562EZ(EX).
B13	CTRL18	CTRL25	RBIAS100	X	X	Pwr Regulator	Pwr Regulator	649 pull-down	Connect to PNP or to pull-down.
B14	IEEE_TEST+	PHY REF	RBIAS10	X	X	NC	2.49K pull-down	619 pull-down	Install resistor or not.
C1	AD[21]	AD[21]	NC	X		AD[21]	AD[21]	AD[21]	
C2	M66EN	M66EN	NC	X		M66EN	M66EN	M66EN	
C3	REQ#	REQ#	NC	X		REQ#	REQ#	REQ#	
C4	C/BE#[3]	C/BE#[3]	NC	X		C/BE#[3]	C/BE#[3]	C/BE#[3]	
C5	RSVD_NC	NC	NC	X		NC	NC	NC	
C6	AD[28]	AD[28]	NC	X		AD[28]	AD[28]	AD[28]	
C7	AD[29]	AD[29]	NC	X		AD[29]	AD[29]	AD[29]	
C8	CLK_RUN#	CLK_RUN#	NC	X		CLK_RUN#	CLK_RUN#	CLK_RUN#	
C9	SMBDATA	SMBDATA	NC	X		SMBDATA	SMBDATA	SMBDATA	
C10	VSS	VSS	VSS						
C11	LED1/ACTIVITY#	ACTIVITY#	ACTLED#	X	X	LED	LED	LED	Same signal - different names.
C12	AVSS	VSS	VSSA	X	X	VSS	VSS	VSS	AVSS = VSSA = VSS
C13	MDI[0]+	MDI[0]+	TDP	X	X	MDI	MDI	MDI	Same signal - different names.
C14	MDI[0]-	MDI[0]-	TDN	X	X	MDI	MDI	MDI	Same signal - different names.
D1	AD[18]	AD[18]	NC	X		AD[18]	AD[18]	AD[18]	
D2	AD[19]	AD[19]	NC	X		AD[19]	AD[19]	AD[19]	
D3	AD[20]	AD[20]	NC	X		AD[20]	AD[20]	AD[20]	
D4	RVSD_VSS	ALT_CLK125	VSS	X	X	VSS	VSS	VSS	
D5	VSS	VSS	VSS						
D6	VSS	VSS	VSS						
D7	VSS	VSS	VSS						
D8	VSS	VSS	VSS						
D9	NC	2.5 V	NC	X		1.8V	2.5 V	No stuff	PHY Power Plane
D10	NC	NC	ISOL_EXEC	X	X	NC	NC	NC	May have LAN Disable logic connected to this signal for 82562EZ(EX).
D11	ANALOG_1.8V	2.5 V	NC	X		1.8V	2.5 V	No stuff	PHY Power Plane

Table 13. Ball Number to Signal Mapping (Sheet 3 of 8) (Continued)

						Population Options			
Ball Ref	**82541xx Pin Name**	**82540EP Pin Name**	**82562EZ Pin Name**	**D[1]**	**K[2]**	**82541xx**	**82540EP**	**82562EZ**	**Comments**
D12	CLKR_1.8V	NC	ISOL_TI	X	X	1.8V	2.5 V	No stuff	May have LAN Disable logic connected to this signal for 82562EZ(EX).
D13	AVSS	VSS	VSSA	X	X	VSS	VSS	VSS	AVSS = VSSA = VSS
D14	IEEE_TEST-	NC	ISOL_TCK	X	X	2-pin header	NC	NC	May have LAN Disable logic connected to this signal for 82562EZ(EX).
E1	3.3 V	3.3 V	3.3 V						
E2	VSS	VSS	VSS						
E3	AD[17]	AD[17]	NC	X		AD[17]	AD[17]	AD[17]	
E4	RVSD_VSS	VSS	VSS						
E5	VSS	VSS	VSS						
E6	VSS	VSS	VSS						
E7	VSS	VSS	VSS						
E8	VSS	VSS	VSS						
E9	VSS	VSS	VSS						
E10	VSS	VSS	VSS						
E11	ANALOG_1.2V	1.5 V	VCCT	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
E12	ANALOG_1.2V	1.5 V	VCCT	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
E13	MD[1]+	MDI[1]+	RDP	X	X	MDI	MDI	MDI	Same signal - different names.
E14	MDI[1]-	MDI[1]-	RDN	X	X	MDI	MDI	MDI	Same signal - different names.
F1	IRDY#	IRDY#	NC	X		IRDY#	IRDY#	IRDY#	
F2	FRAME#	FRAME#	NC	X		FRAME#	FRAME#	FRAME#	
F3	C/BE#[2]	C/BE#[2]	NC	X		C/BE#[2]	C/BE#[2]	C/BE#[2]	
F4	VSS	VSS	VSSR	X	X	VSS	VSS	VSS	VSSR = VSS
F5	VSS	VSS	VSSR	X	X	VSS	VSS	VSS	VSSR = VSS
F6	VSS	VSS	VSS						
F7	VSS	VSS	VSS						
F8	VSS	VSS	VSS						
F9	VSS	VSS	VSS						
F10	VSS	VSS	VSS						
F11	AVSS	VSS	VSS	X	X	VSS	VSS	VSS	AVSS = VSS
F12	NC	PHY_TSTPT	NC	X		NC	NC	NC	

Table 13. Ball Number to Signal Mapping (Sheet 4 of 8) (Continued)

						Population Options			
Ball Ref	**82541xx Pin Name**	**82540EP Pin Name**	**82562EZ Pin Name**	**D[1]**	**K[2]**	**82541xx**	**82540EP**	**82562EZ**	**Comments**
F13	MDI[2]+	MDI[2]+	NC	X		Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
F14	MDI[2]-	MDI[2]-	NC	X		Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
G1	CLK	CLK	NC	X		CLK	CLK	CLK	
G2	VIO	VIO	NC	X		VIO	VIO	VIO	
G3	TRDY#	TRDY#	NC	X		TRDY#	TRDY#	TRDY#	
G4	PLL_1.2V	ZP_COMP	NC	X		1.2 V	1.5 V	3.3 V	Requires 82540EP ZCOMP logic to be in bypass mode
G5	1.2 V	1.5 V	VCCR	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
G6	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
G7	VSS	VSS	VSS						
G8	VSS	VSS	VSS						
G9	VSS	VSS	VSS						
G10	VSS	VSS	VSS						
G11	AVSS	VSS	VSS	X	X	VSS	VSS	VSS	AVSS = VSS
G12	ANALOG_1.8V	2.5 V	NC	X		1.8V	2.5 V	No stuff	PHY Power Plane
G13	ANALOG_1.2V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
G14	AVSS	VSS	VSS	X	X	VSS	VSS	VSS	AVSS = VSS
H1	STOP#	STOP#	NC	X		STOP#	STOP#	STOP#	
H2	INTA#	INTA#	NC	X		INTA#	INTA#	INTA#	
H3	DEVSEL#	DEVSEL#	NC	X		DEVSEL#	DEVSEL#	DEVSEL#	
H4	PLL_1.2V	ZN_COMP	NC	X		1.2 V	1.5 V	3.3 V	Requires 82540EP ZCOMP logic to be in bypass mode
H5	1.2 V	1.5 V	VCCR	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
H6	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
H7	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
H8	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
H9	VSS	VSS	VSS						
H10	VSS	VSS	VSS						
H11	ANALOG_1.2V	1.5 V	3.3 V	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane

Table 13. Ball Number to Signal Mapping (Sheet 5 of 8) (Continued)

						Population Options			
Ball Ref	**82541xx Pin Name**	**82540EP Pin Name**	**82562EZ Pin Name**	**D[1]**	**K[2]**	**82541xx**	**82540EP**	**82562EZ**	**Comments**
H12	NC	HSDACN	NC	X		NC	NC	NC	
H13	MDI[3]+	MDI[3]+	NC	X		Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
H14	MDI[3]-	MDI[3]-	NC	X		Magnetics	Magnetics	Magnetics	10/100 Magnetics will not have a pin connected here
J1	PAR	PAR	NC	X		PAR	PAR	PAR	
J2	PERR#	PERR#	NC	X		PERR#	PERR#	PERR#	
J3	GNT#	GNT#	NC	X		GNT#	GNT#	GNT#	
J4	EEMODE	NC	NC	X		Pull-down or NC	NC	NC	82541xx: Connect a pull-down for Microwire and a pull-up for SPI* (82541GI/EI only)
J5	1.2 V	1.5 V	VCCR	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
J6	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
J7	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
J8	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
J9	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
J10	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
J11	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
J12	AUX_PWR	AUX_PWR	NC	X		AUX_PWR	AUX_PWR	AUX_PWR	
J13	XTAL_1.8V	HSDACP	NC	X		1.8V	2.5 V	No stuff	PHY Power Plane
J14	XTAL2	XTAL2	X2						
K1	AD[16]	AD[16]	NC	X		AD[16]	AD[16]	AD[16]	
K2	VSS	VSS	VSS						
K3	3.3 V	3.3 V	VCC						
K4	3.3 V	3.3 V	VCC						
K5	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
K6	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
K7	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
K8	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
K9	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane

Table 13. Ball Number to Signal Mapping (Sheet 6 of 8) (Continued)

						Population Options			
Ball Ref	**82541xx Pin Name**	**82540EP Pin Name**	**82562EZ Pin Name**	**D[1]**	**K[2]**	**82541xx**	**82540EP**	**82562EZ**	**Comments**
K10	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
K11	1.2 V	1.5 V	VCC	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
K12	AVSS	VSS	VSSP	X	X	VSS	VSS	VSS	AVSS = VSSP = VSS
K13	3.3 V	3.3 V	VCC	X	X	3.3 V	3.3 V	3.3 V	VCCP = 3.3 V
K14	XTAL1	XTAL1	X1						
L1	AD[14]	AD[14]	NC	X		AD[14]	AD[14]	AD[14]	
L2	AD[15]	AD[15]	NC	X		AD[15]	AD[15]	AD[15]	
L3	C/BE#[1]	C/BE#[1]	NC	X		C/BE#[1]	C/BE#[1]	C/BE#[1]	
L4	1.2 V	1.5 V	3.3 V	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
L5	1.2 V	1.5 V	3.3 V	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
L6	VSS	VSS	VSS	X	X	VSS	VSS	VSS	VSSA = VSS
L7	RVSD_NC	CLK_BYP#	ADV10	X	X	NC	NC	NC	
L8	NC	2.5 V	NC	X		1.8V	2.5 V	No stuff	PHY Power Plane
L9	1.2 V	1.5 V	3.3 V	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
L10	1.2 V	1.5 V	3.3 V	X	X	1.2 V	1.5 V	3.3 V	Core Power Plane
L11	VSS	VSS	VSS	X	X	VSS	VSS	VSS	VSSP = VSS
L12	JTAG_TMS	JTAG_TMS	NC	X		NC	NC	NC	
L13	JTAG_TRST#	JTAG_TRST#	JTXD[1]	X	X	LCI	LCI	LCI	ICH drives this signal low. TRST needs to be grounded to disable JTAG. JTAG becomes difficult to use.
L14	JTAG_TCK	JTAG_TCK	JTXD[2]	X	X	LCI	LCI	LCI	ICH drives this signal low. TCK needs to be biased. JTAG becomes difficult to use.
M1	AD[11]	AD[11]	NC	X		AD[11]	AD[11]	AD[11]	
M2	AD[12]	AD[12]	NC	X		AD[12]	AD[12]	AD[12]	
M3	AD[13]	AD[13]	NC	X		AD[13]	AD[13]	AD[13]	
M4	C/BE#[0]	C/BE#[0]	NC	X		C/BE#[0]	C/BE#[0]	C/BE#[0]	
M5	AD[5]	AD[5]	NC	X		AD[5]	AD[5]	AD[5]	
M6	VSS	VSS	VSSA	X	X	VSS	VSS	VSS	VSSA = VSS
M7	AD[1]	AD[1]	NC	X		AD[1]	AD[1]	AD[1]	
M8	RVSD_NC	CLK_VIEW	NC	X		NC	NC	NC	
M9	FLSH_CE#	FLSH_CE#	NC	X		NC	NC	NC	

Table 13. Ball Number to Signal Mapping (Sheet 7 of 8) (Continued)

						Population Options			
Ball Ref	**82541xx Pin Name**	**82540EP Pin Name**	**82562EZ Pin Name**	**D[1]**	**K[2]**	**82541xx**	**82540EP**	**82562EZ**	**Comments**
M10	EESK	EESK	NC	X		EESK	EESK	EESK	If EE from ICH and 82540EP are shared, a 0 Ω pop is required because ICH drives this in reset.
M11	FLSH_SI	FLSH_SI	NC	X		NC	NC	NC	
M12	SDP[7]	SDP[7]	JRXD[2]	X	X	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
M13	JTAG_TDI	JTAG_TDI	JRSTSYNC	X	X	LCI	LCI	LCI	ICH expects this signal to be high or undriven. JTAG becomes difficult to use.
M14	JTAG_TDO	JTAG_TDO	JTXD[0]	X	X	LCI	LCI	LCI	ICH expects this signal to be high or undriven. JTAG becomes difficult to use.
N1	VSS	VSS	VSS						
N2	AD[10]	AD[10]	NC	X		AD[10]	AD[10]	AD[10]	
N3	AD[9]	AD[9]	NC	X		AD[9]	AD[9]	AD[9]	
N4	AD[7]	AD[7]	NC	X		AD[7]	AD[7]	AD[7]	
N5	AD[4]	AD[4]	NC	X		AD[4]	AD[4]	AD[4]	
N6	3.3 V	3.3 V	VCCA	X	X	3.3 V	3.3 V	3.3 V	VCCA = 3.3 V
N7	AD[0]	AD[0]	NC	X		AD[0]	AD[0]	AD[0]	
N8	3.3 V	3.3 V	VCCA	X	X	3.3 V	3.3 V	3.3 V	VCCA = 3.3 V
N9	FLSH_SCK	FLSH_SCK	NC	X		NC	NC	NC	
N10	EEDO	EEDO	NC	X		EEDO	EEDO	EEDO	If desired, this can be shorted to the ICH EEDI b/c it is an input in ICH in reset.
N11	RVSD_NC	NC	NC	X		NC	NC	NC	
N12	VSS	VSS	VSSP	X	X	VSS	VSS	VSS	VSSP = VSS
N13	SDP[6]	SDP[6]	JRXD[1]	X	X	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
N14	SDP[0]	SDP[0]	JCLK	X	X	LCI	LCI	LCI	ICH expects this signal to be low or undriven.
P1	NC	NC	NC						
P2	3.3 V	3.3 V	3.3 V						
P3	AD[8]	AD[8]	NC	X		AD[8]	AD[8]	AD[8]	
P4	AD[6]	AD[6]	NC	X		AD[6]	AD[6]	AD[6]	

Table 13. Ball Number to Signal Mapping (Sheet 8 of 8) (Continued)

						Population Options			
Ball Ref	**82541xx Pin Name**	**82540EP Pin Name**	**82562EZ Pin Name**	**D[1]**	**K[2]**	**82541xx**	**82540EP**	**82562EZ**	**Comments**
P5	AD[3]	AD[3]	NC	X		AD[3]	AD[3]	AD[3]	
P6	AD[2]	AD[2]	NC	X		AD[2]	AD[2]	AD[2]	
P7	EECS	EECS	NC	X		EECS	EECS	EECS	If EE from ICH and 82540EP are shared, a 0 Ω pop is required because ICH drives this in reset.
P8	VSS	VSS	VSSA	X	X	VSS	VSS	VSS	VSSA = VSS
P9	FLSH_SO/ LAN_DISABLE#	FLSH_SO	NC	X		LAN_EN	LAN_EN	LAN_EN	Connect to LAN Enable signal
P10	EEDI	EEDI	NC	X		EEDI	EEDI	EEDI	If desired, this can be shorted to the ICH EEDI because it is an input in ICH in reset.
P11	CTRL12	CTRL15	NC	X		Pwr Regulator	Pwr Regulator	No stuff	Connect to PNP. Don't' stuff PNP on 82562EZ(EX).
P12	3.3 V	3.3 V	VCC	X	X	3.3 V	3.3 V	3.3 V	VCCP = 3.3 V
P13	SDP[1]	SDP[1]	JRXD[0]	X	X	LCI	LCI	LCI	ICH expects this signal to be high or undriven.
P14	NC	NC	NC			NC	NC	NC	

1. This column will be checked if the 82562EZ pin names are different from their 82540EP/82541xx counterparts.
2. This column will be checked if the 82562EZ signal is different from the 82540EP/82541xx AND the 82562EZ gets a connection.

7.0 Dual Footprint Reference Schematic

The following pages illustrate a dual purpose 10/100 Mbps and 10/100/1000 Mbps design using the 82562EZ(EX) Platform LAN Connect device and the 82540EP/82541xx Gigabit Ethernet Controller.

REVISIONS		
REV	DESCRIPTION	DATE

82541PI/GI/EI, 82540EP, 82562EZ/EX REFERENCE DESIGN

15mm x 15mm BGA

1mm pitch

***A* = Install component if using 82541PI/GI/EI MAC/PHY**

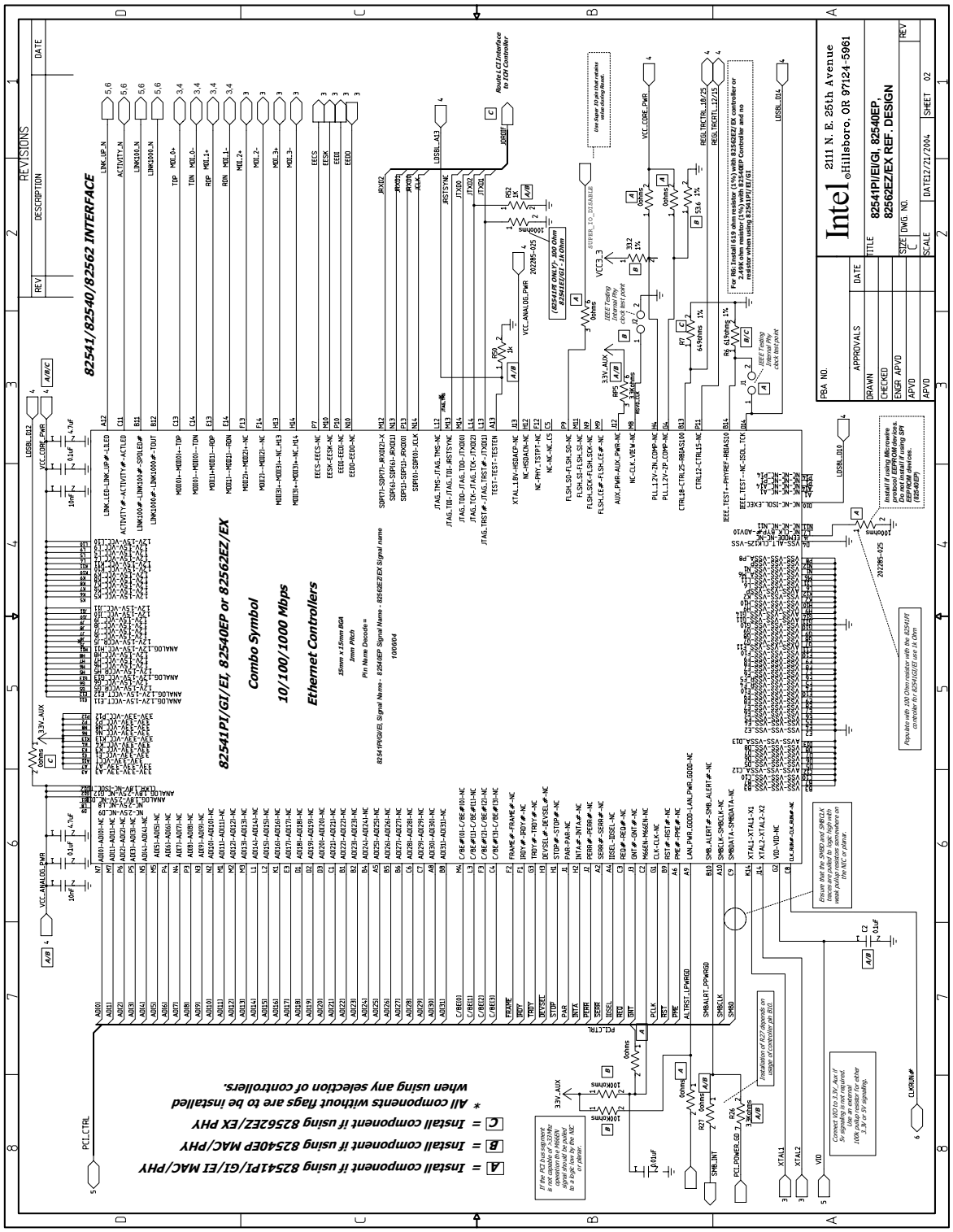
***B* = Install component if using 82540EP MAC/PHY**

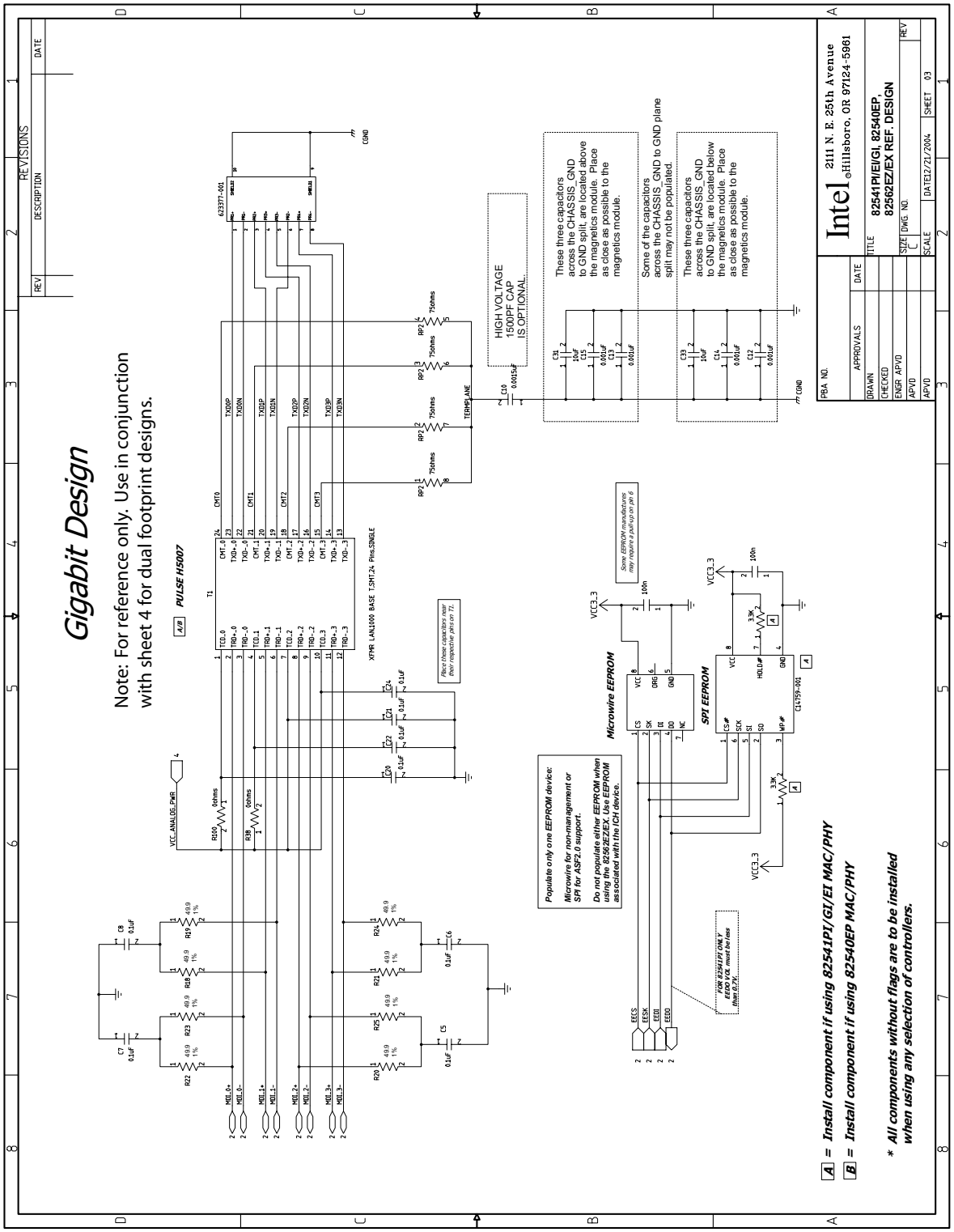
***C* = Install component if using 82562EZ/EX PHY**

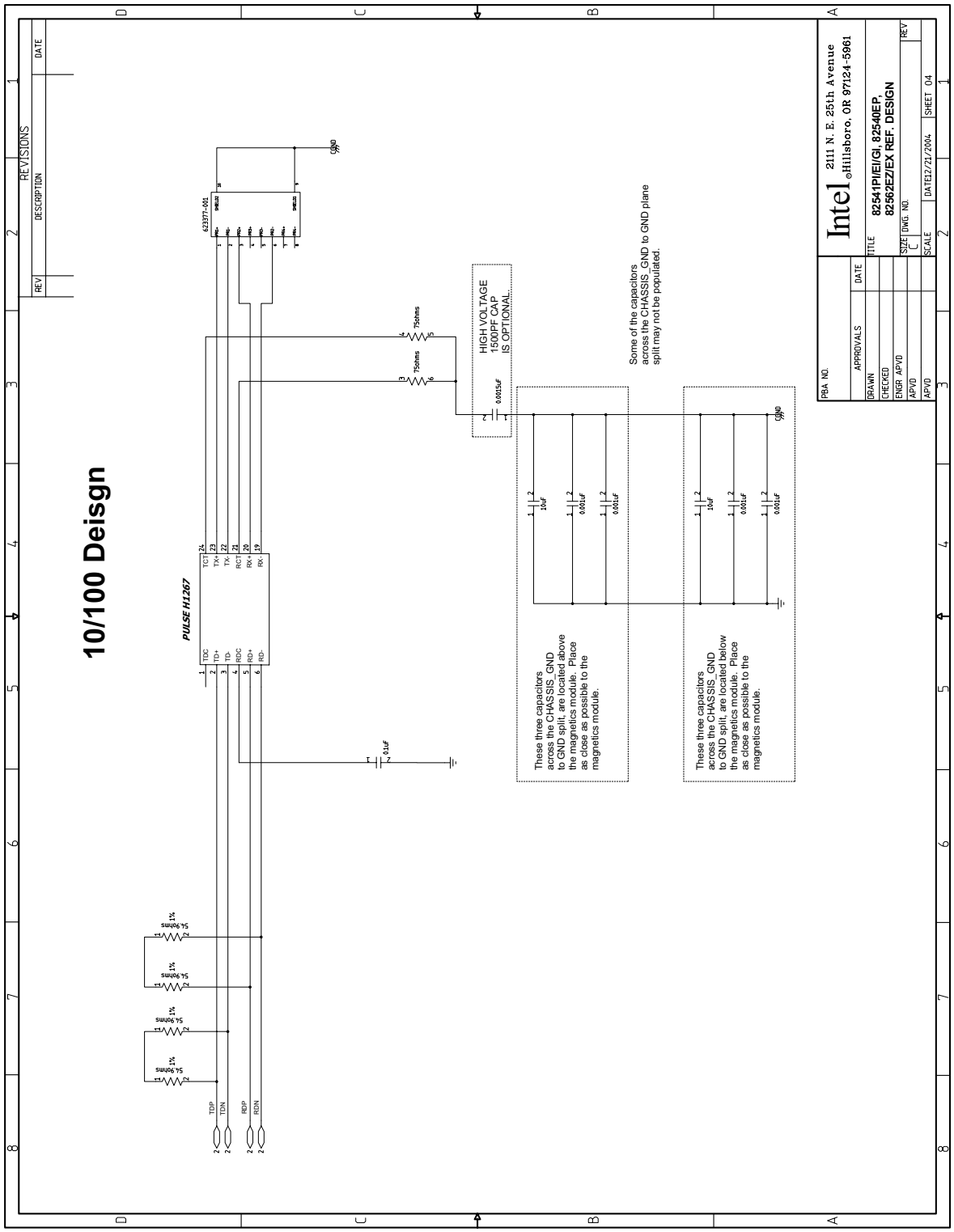
*** All components without flags are to be installed when using any selection of controllers.**

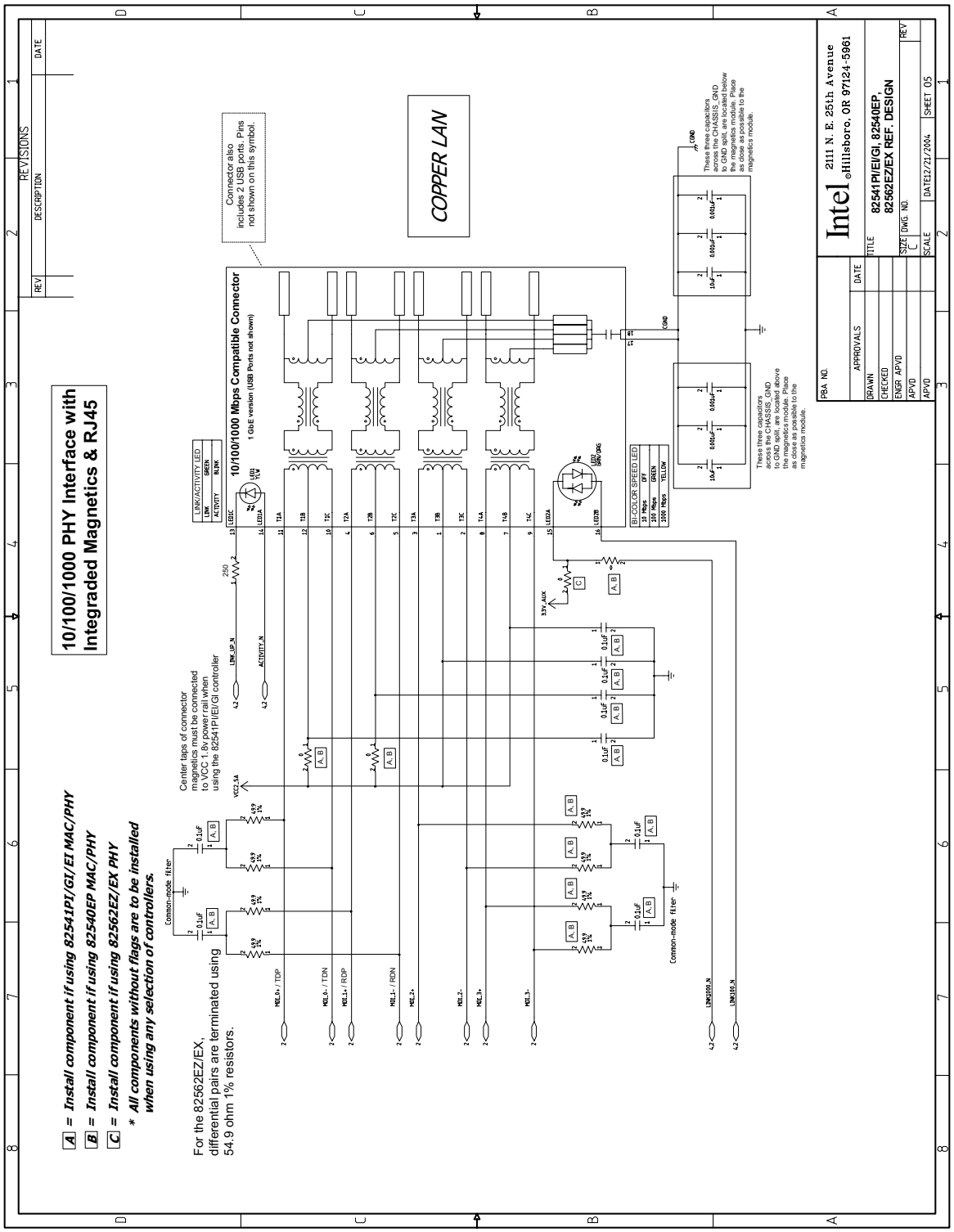
Rev. 2.5
12/21/04

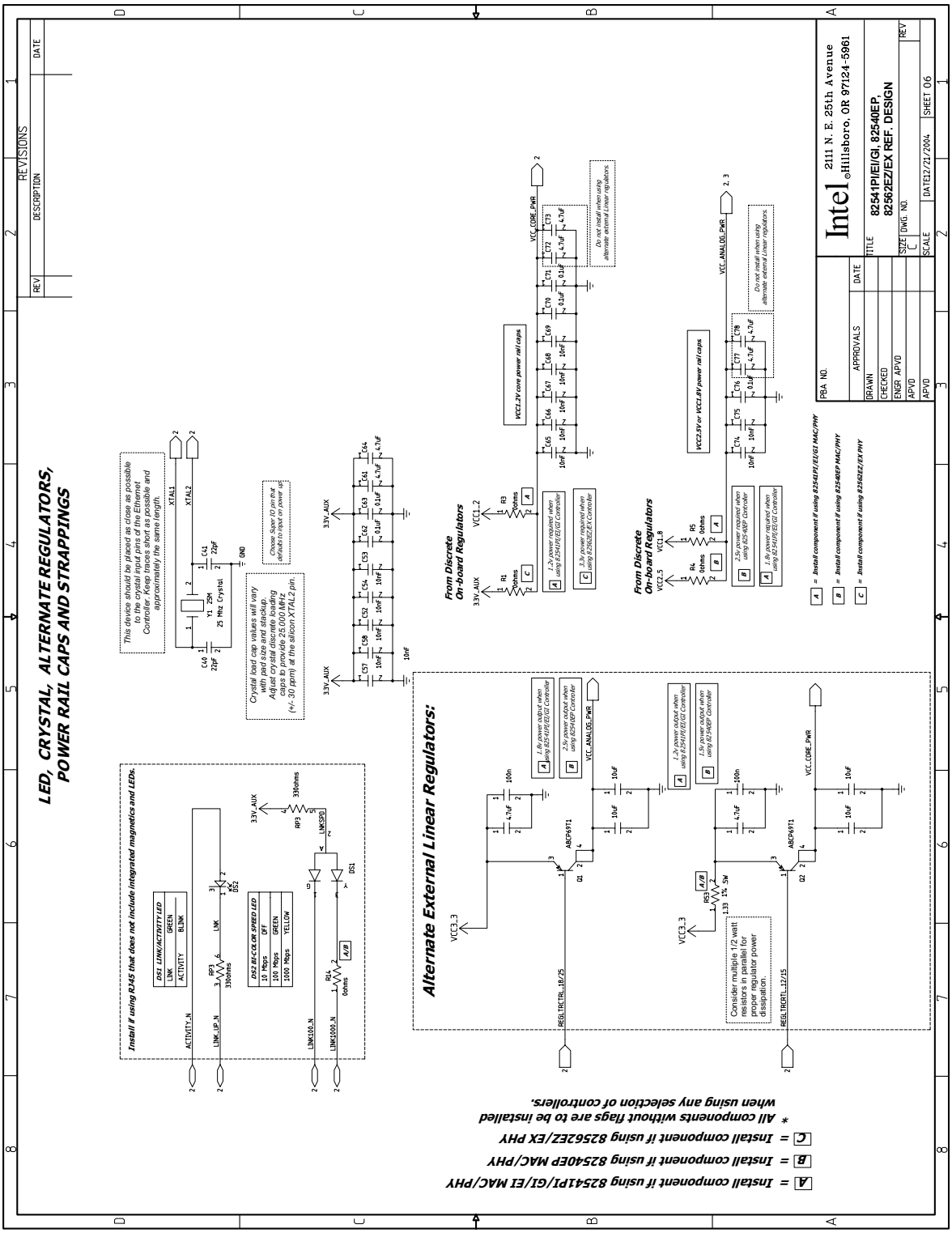
PBA NO.		Intel 2111 N. E. 25th Avenue ©Hillsboro, OR 97124-5961		
APPROVALS	DATE	TITLE	82541PI/EI/GI, 82540EP, 82562EZ/EX REF. DESIGN	
DRAWN		SIZE C	DWG. NO.	REV
CHECKED		SCALE	DATE 12/21/2004	SHEET 01
ENGR APVD				
APVD				
APVD				

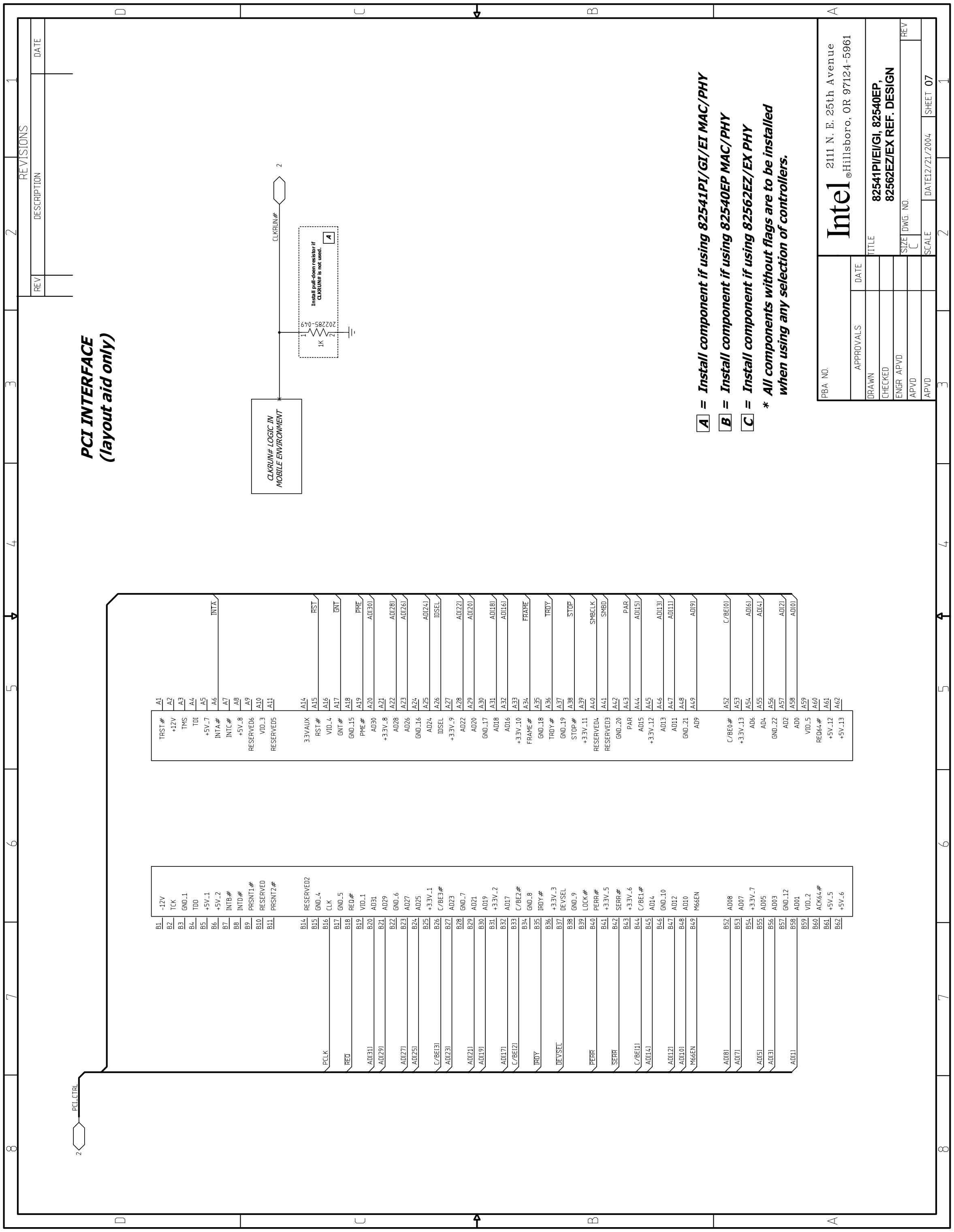

82541/82540/82562 INTERFACE
82541PI/GI/EI, 82540EP or 82562EZ/EX
Combo Symbol
10/100/1000 Mbps
Ethernet Controllers
15mm x 15mm BGA
1mm Pitch
Pin Name Decode =
82541PI/GI/EI Signal Name - 82540EP Signal Name - 82562EZ/EX Signal name
1001604
A = Install component if using 82541PI/GI/EI MAC/PHY
B = Install component if using 82540EP MAC/PHY
C = Install component if using 82562EZ/EX PHY
* All components without flags are to be installed when using any selection of controllers.
REVISIONS
DESCRIPTION
DATE
Intel ©Hillsboro, OR 97124-5961
2111 N. E. 25th Avenue
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
TITLE
82541PI/EI/GI, 82540EP,
82562EZ/EX REF. DESIGN
SIZE
C
DWG. NO.
REV
SCALE
DATE12/21/2004
SHEET 02


Gigabit Design
Note: For reference only. Use in conjunction with sheet 4 for dual footprint designs.
A/B PULSE H5007
XFMR LAN1000 BASE T SMT,24 Pins,SINGLE
HIGH VOLTAGE 1500PF CAP IS OPTIONAL
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
Some of the capacitors across the CHASSIS_GND to GND plane split may not be populated.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Microwire EEPROM
SPI EEPROM
Populate only one EEPROM device:
Microwire for non-management or SPI for ASF2.0 support.
Do not populate either EEPROM when using the 82562EZ/EX. Use EEPROM associated with the ICH device.
Some EEPROM manufactures may require a pull-up on pin 6
Place these capacitors near their respective pairs on T1.
FOR 82541PI ONLY EEDO VOL must be less than 0.2V.
A = Install component if using 82541PI/GI/EI MAC/PHY
B = Install component if using 82540EP MAC/PHY
* All components without flags are to be installed when using any selection of controllers.
Intel 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961
82541PI/EI/GI, 82540EP, 82562EZ/EX REF. DESIGN


10/100 Deisgn
REVISIONS
REV
DESCRIPTION
DATE
PULSE H1267
TDC
TD+
TD-
RDC
RD+
RD-
TCT
TX+
TX-
RCT
RX+
RX-
TDP
TDN
RDP
RDN
54.9ohms 1%
75ohms
HIGH VOLTAGE
1500PF CAP
IS OPTIONAL
0.0015uF
0.1uF
10uF
0.001uF
These three capacitors across the CHASSIS_GND to GND split, are located above the magnetics module. Place as close as possible to the magnetics module.
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
Some of the capacitors across the CHASSIS_GND to GND plane split may not be populated.
GND
623177-A01
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82541PI/EI/GI, 82540EP,
82562EZ/EX REF. DESIGN
SIZE
C
DWG. NO.
REV
SCALE
DATE12/21/2004
SHEET 04


10/100/1000 PHY Interface with Integraded Magnetics & RJ45
COPPER LAN
10/100/1000 Mbps Compatible Connector
1 GbE version (USB Ports not shown)
Connector also includes 2 USB ports. Pins not shown on this symbol.
LINK/ACTIVITY LED
BI-COLOR SPEED LED
Center taps of connector magnetics must be connected to VCC 1.8v power rail when using the 82541PI/EI/GI controller
For the 82562EZ/EX, differential pairs are terminated using 54.9 ohm 1% resistors.
Common-mode filter
These three capacitors across the CHASSIS_GND to GND split, are located below the magnetics module. Place as close as possible to the magnetics module.
A = Install component if using 82541PI/GI/EI MAC/PHY
B = Install component if using 82540EP MAC/PHY
C = Install component if using 82562EZ/EX PHY
* All components without flags are to be installed when using any selection of controllers.
REVISIONS
REV
DESCRIPTION
DATE
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82541PI/EI/GI, 82540EP,
82562EZ/EX REF. DESIGN
SIZE
C
DWG. NO.
REV
SCALE
DATE12/21/2004
SHEET 05


LED, CRYSTAL, ALTERNATE REGULATORS, POWER RAIL CAPS AND STRAPPINGS
Alternate External Linear Regulators:
From Discrete On-board Regulators
VCC1.2V core power rail caps
VCC2.5V or VCC1.8V power rail caps
Crystal load cap values will vary with pad size and stackup. Adjust crystal discrete loading caps to provide 22.000 MHz (+/- 30 ppm) at the silicon XTAL2 pin.
Consider multiple 1/2 watt resistors in parallel for proper regulator power dissipation.
A = Install component if using 82541PI/GI/EI MAC/PHY
B = Install component if using 82540EP MAC/PHY
C = Install component if using 82562EZ/EX PHY
* All components without flags are to be installed when using any selection of controllers.
Intel 2111 N. E. 25th Avenue Hillsboro, OR 97124-5961
82541PI/EI/GI, 82540EP, 82562EZ/EX REF. DESIGN


PCI INTERFACE
(layout aid only)
CLKRUN# LOGIC IN MOBILE ENVIRONMENT
CLKRUN#
Install pull-down resistor if CLKRUN# is not used.
A = Install component if using 82541PI/GI/EI MAC/PHY
B = Install component if using 82540EP MAC/PHY
C = Install component if using 82562EZ/EX PHY
* All components without flags are to be installed when using any selection of controllers.
PCI_CTRL
REVISIONS
REV
DESCRIPTION
DATE
PBA NO.
APPROVALS
DATE
DRAWN
CHECKED
ENGR APVD
APVD
APVD
Intel
2111 N. E. 25th Avenue
Hillsboro, OR 97124-5961
TITLE
82541PI/EI/GI, 82540EP,
82562EZ/EX REF. DESIGN
SIZE C
DWG. NO.
REV
SCALE
DATE 12/21/2004
SHEET 07

Appendix A Measuring LAN Reference Frequency Using a Frequency Counter

A.1 Background

To comply with IEEE specifications for 10/100 Mbps and 10/100/1000Base-T Ethernet LAN, the transmitter reference frequency must be correct and accurate within ±50 parts per million (ppm).

Note: Intel recommends a frequency tolerance of ±30 (ppm).

Most Intel LAN devices will operate properly with a 25.000 MHz reference crystal, provided it meets the recommended requirements for frequency stability, equivalent series resistance at resonance (ESR), and load capacitance.

Most circuits for series resonant crystals include two discrete capacitors (typically C1 and C2), with values between 5 pF and 36 pF.

The most accurate way to determine the appropriate value for the discrete capacitors is to install the approximately correct values for C1 and C2. Next, a frequency counter should be used to measure the transmitter reference frequency (or transmitter reference clock).

- If the transmitter reference frequency is more than 20 ppm below the target frequency, then the values for C1 and C2 are too big and should be decreased.
- If the transmitter reference frequency is more than 20 ppm above the target frequency, then the values for C1 and C2 are too small and should be increased.

This Appendix provides instructions and illustrations that explain how to use a frequency counter and probe to determine the Ethernet LAN device transmit center frequency. An example describing how to calculate the frequency accuracy of the measured and averaged center frequency with respect to the target center frequency is also included.

A.2 Required Test Equipment

- Tektronix CMC-251, or similar high resolution, digital counter
- Tektronix P6246, or similar high bandwidth, low capacitance (less than 1 pF) probe
- Tektronix 1103, or similar probe power supply or probe amplifier
- BNC, 50 Ω coaxial cable (less than 6 feet long)
- System with power supply and test software for the LAN circuit to be tested

A.3 Indirect Probing Method

The indirect probing test method is applicable foremost devices that support 100BASE-T. Since probe capacitance can load the reference crystal and affect the measured frequency, the preferred method is to use the indirect probing test method when possible.

Almost all Intel LAN silicon that support 1000BASE-T Ethernet can provide a buffered 125 MHz clock, which can be used for indirect probing of the transmitter reference clock. The buffered 125 MHz clock will be a 5X multiple of the crystal circuit's reference frequency (Figure 11).

Different LAN devices may require different register settings, to enable the buffered 125 MHz reference frequency. Please obtain the settings or instructions that are appropriate for the LAN controller you are using.

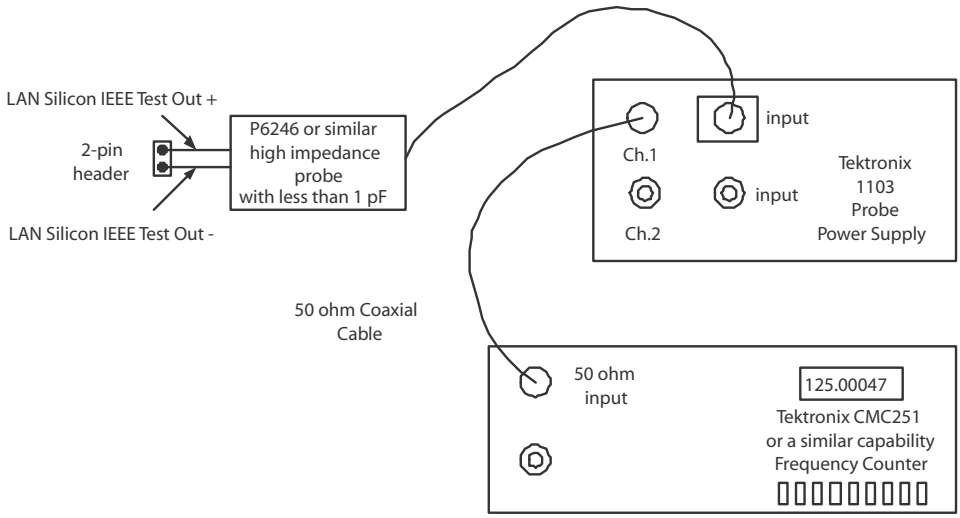


Figure 11. Indirect Probing Setup

A.4 Indirect Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 11.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~125.0000 MHz with at least four decimal places frequency resolution.
4. Enable the 125 MHz buffered reference clock. An example can be found in Appendix B, “GigConf.exe Register Settings for 82541GI(EI) Devices”.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 125.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 1.

Given: The measured averaged center frequency is 124.99942 MHz (or 124,999,420 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(124999420 - 125000000)}{(125000000 / 1000000)} = -4.64ppm$$

Example 2.

Given: The measured averaged center frequency is 125.00087 MHz (or 125,000,870 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(125000870 - 125000000)}{(125000000/1000000)} = 6.96ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

A.5 Direct Probing Test Method, Applicable for Most 10/100 Devices (Devices that do NOT support 1000Base-T)

Because probe capacitance can load the reference crystal affecting the measured frequency, it is preferable to use a probe with less than 1 pF capacitance.

Note: Direct probing is not recommended for the 82541GI(EI) LAN silicon.

The probe should be connected between the X2 (or Xout) pin of the LAN device and a nearby ground. Typically, it is possible to connect the probe pins across one of the discrete load capacitors (C2 in Figure 12).

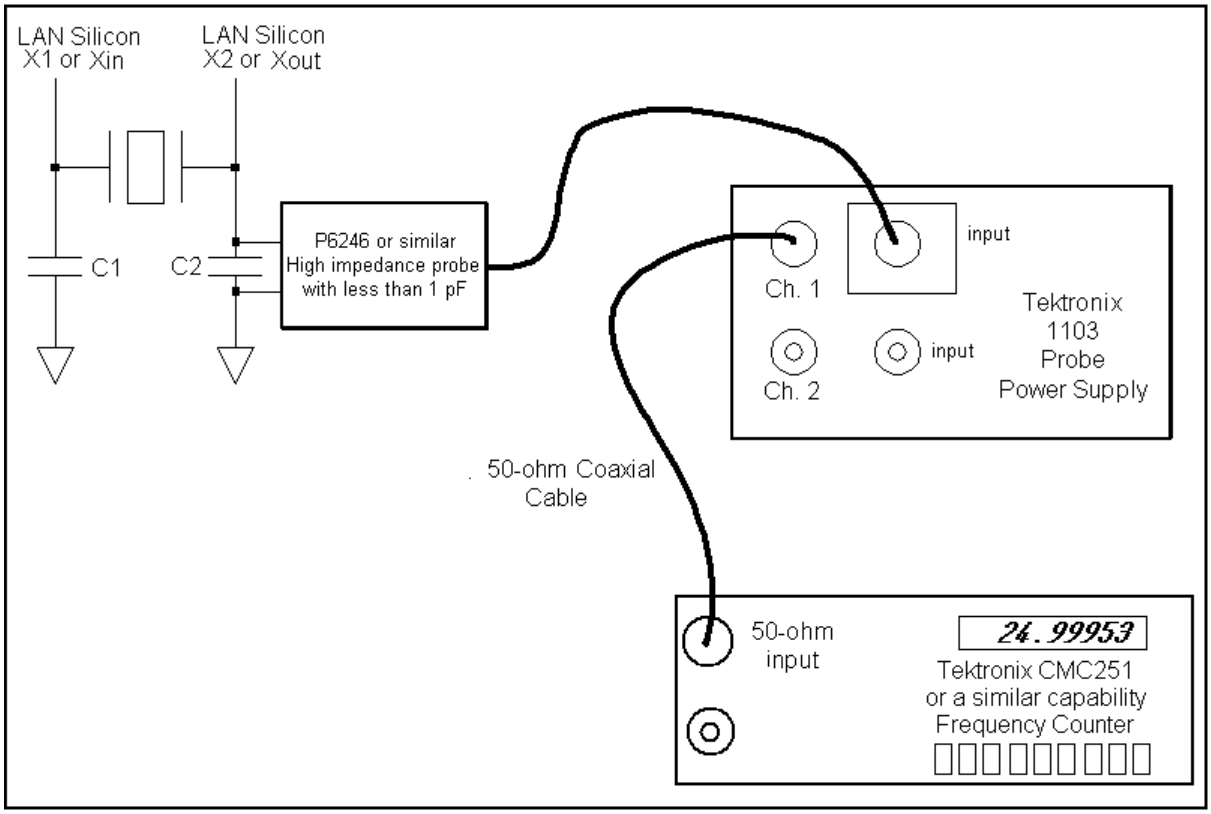


Figure 12. Direct Probing Method

A.6 Direct Frequency Measurement and Frequency Accuracy Calculation Steps

1. Make sure the system BIOS has the LAN controller enabled.
2. Connect the test equipment as shown in Figure 12.
3. Using the appropriate controls for your model of high resolution digital counter, make sure it can display ~25.0000 MHz with at least four decimal places frequency resolution.
4. Ensure the LAN circuits are powered.
5. Determine the center reference frequency as accurately as possible. This can be done by taking 30 to 50 different readings using the frequency counter and then calculating the average results of the readings.
6. Calculate the accuracy of the measured and averaged center frequency with respect to an ideal 25.0000 MHz reference frequency.

$$FrequencyAccuracy(ppm) = \frac{(x - y)}{(y / 1000000)}$$

where x = Average measured frequency in Hertz and
y = Ideal reference frequency in Hertz

Example 3.

Given: The measured averaged center frequency is 24.99963 MHz (or 24,999,630 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(24999630 - 25000000)}{(25000000 / 1000000)} = -14.8ppm$$

Example 4.

Given: The measured averaged center frequency is 25.00027 MHz (or 25,000,270 Hertz).

$$FrequencyAccuracy(ppm) = \frac{(25000270 - 25000000)}{(25000000 / 1000000)} = 10.8ppm$$

Note: The following items should be noted for an ideal reference crystal on a typical printed circuit board.

- If the transmitter reference frequency is more than 8 ppm below the target frequency, then the values for C1 and C2 are too big and they should be decreased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.
- If the transmitter reference frequency is more than 8 ppm above the target frequency, then the values for C1 and C2 are too small and they should be increased. When tests are performed across temperature, it may be acceptable for the center frequency deviation to be a little greater than 8 ppm.

Appendix B GigConf.exe Register Settings for 82541GI(EI) Devices

The following steps describe the indirect probing test method using GigConf.exe for 82541GI(EI) devices.

1. Boot to DOS using a DOS Boot Diskette.
2. Launch Gigconf from the diskette (gigconf.exe).
3. Select the Intel network connection to be measured.
   a. If multiple adapters are installed, use the arrow keys to navigate to highlight the selected adapter and press Enter.
4. Select Registers by pressing “R”.
5. Select PHY Registers by pressing “P”.
6. Use the arrow keys to navigate to the value listed next to address 0000.
7. Press Enter when the value is highlighted and then use Backspace to clear out the current value.
8. Type “0100” for the value and then press Enter.
9. Navigate to the value listed next to address 0012.
10. Press Enter to select the highlighted value and use Backspace to clear the current value.
11. Type “8000” for the value and then press Enter.
12. Navigate to the Set Address field on the right side of the screen (use the right arrow key)
13. Press Enter to select the highlighted value and then use Backspace to clear out the current value.
14. Type “4011” for the value and then press Enter.
    This changes the PHY register screen and updates it with new addresses and values.
15. Use the arrow keys to navigate to the value for address 4011.
16. Press Enter when the value is highlighted and then use Backspace to clear the current value.
17. Type “8000” for the value and then press Enter.
18. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
19. Press Enter when the value is highlighted and use Backspace to clear the current value.
20. Enter “2F5B” (capital letters are not required) for the address and then press Enter.
21. Use the arrow keys to navigate to the value for address “2F5B”.
22. Press Enter when the value is highlighted and then use Backspace to clear the current value.
23. Type “0003” for the value and then press Enter.
24. Use the right arrow key to navigate to the Set Address field on the right side of the screen.
25. Press Enter when the value is highlighted and then use Backspace to clear the current value.

Note: This page intentionally left blank.