PEX 86xx Gen 2 Switch Compatibility with Gen 1 Devices

Application Note

Version 1.2

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Website: www.plxtech.com
Technical Support: www.plxtech.com/support

Background

PLX's Gen 2 switches (PEX 86xx) support Data Rate Identifier bits [6,2] in Training Sequences, as described in the PCIe Base Specification, r2.0. These bits are reserved in prior PCIe specification revisions. PCIe Gen 1 devices/endpoints that do not support the functionality of these PCIe r2.0 bits are expected to ignore these bits within PCIe training sets. However, some non-compliant devices fail to ignore these bits and consequently do not link up with PEX 86xx switches. This Application Note describes the issue as well as the workaround to enable the non-compliant endpoint to link up with a PEX 86xx switch.

Description

Data Rate Identifier bits two and six indicate support for Gen 2 data rate, and Autonomous Change / Link Upconfigure Capability / Selectable De-emphasis, respectively. When non-compliant endpoints receive Data Rate Identifier bits [6,2] that are set (non-zero) in the link training sequences, they attempt to retrain. The retraining yields the same result and the device remains stuck in retraining indefinitely, unable to link up.

This phenomenon manifests itself when trying to link up with products in the following PLX Gen 2 switch family's:

Switch Family	Products
A	*PEX 8648, PEX 8647, PEX 8632, PEX 8624, PEX 8616, PEX 8612*
B	*PEX 8636, PEX 8625, PEX 8619, PEX8618, PEX 8617, PEX 8615, PEX 8614, PEX 8613, PEX 8609, PEX 8608, PEX 8606, PEX 8604*
C	*PEX 8696, PEX 8680, PEX 8664, PEX 8649*

Workaround

The following workaround may be used to allow these non-compliant devices to link up with the aforementioned PEX 86xx switches:

1. For Switch Family A devices
   - A test bit specific to the station the endpoint is being plugged into needs to be set. Set bit *x*22Ch[6] to 1, where *x* is the port number.
   - The specific port in question must be configured as a Gen 1 port. To set a particular port to Gen 1, program the EEPROM to:
     - Set Target Link Speed (*x*098h[3:0]) to '0001', where *x* is the port number.
     - Set Supported Link Speeds (*x*074h[3:0]) to '0001', where *x* is the port number.
2. For Switch Family B devices
   - A test bit specific to the station the endpoint is being plugged into needs to be set. Set bit *x*23Ch[6] to 1, where *x* is the port number.
   - The specific port in question must be configured as a Gen 1 port. To set a particular port to Gen 1, program the EEPROM to:
     - Set Target Link Speed (*x*098h[3:0]) to '0001', where *x* is the port number.
     - Set Supported Link Speeds (*x*074h[3:0]) to '0001', where *x* is the port number.
3. For Switch Family C devices
   - A test bit specific to the station the endpoint is being plugged into needs to be set. Set bit *x*224h[3:0] to 1, where *x* is the port number.
   - The specific port in question must be configured as a Gen 1 port. To set a particular port to Gen 1, program the EEPROM to:

- Set Target Link Speed (*x*098h[3:0]) to '0001', where *x* is the port number.
- Set Supported Link Speeds (*x*074h[3:0]) to '0001', where *x* is the port number.

When this workaround is implemented, the port *never* support Gen 2 data rate. Therefore, this workaround should be implemented only if needed for a non-compliant Gen 1 device.

Enhanced Silicon Revisions

As a proactive measure to allow non-compliant devices to avoid this issue, PLX has implemented an innovative solution into all silicon revisions of the PEX 86xx switches. This solution is implemented using the SPARE4 (or, for some devices, STRAP_G1_COMPATIBLE) pin. When SPARE4 (or STRAP_G1_COMPATIBLE) is pulled High, the switch will advertise support for Gen 2 data rates as well as Autonomous Change / Link Upconfigure Capability / Selectable De-emphasis. When SPARE4 (or STRAP_G1_COMPATIBLE) is pulled Low, if a port initially fails linkup during Configuration state, the port will attempt to train with Data Rate Identifier bits [6,2] cleared, allowing the switch to link up with the non-compliant endpoint. For more details, please see the SPARE4 (or STRAP_G1_COMPATIBLE) pin description in the appropriate PEX 86xx Data Book.