Stratix FPGA Family

January 2007, ver. 3.1 Errata Sheet

This errata sheet provides updated information on Stratix® devices. This document addresses known issues and includes methods to work around the issues.

Table 1 shows these issues and which Stratix devices each issue affects.

Table 1. Stratix Family Issues (Part 1 of 2)

Issue	Affected Devices	Fixed Devices
Certain instances of PLL reconfiguration causes the `scandataout` signal to become stuck in the high position. $T_{RECONFIGWAIT}$ specification added to this section ensures proper reconfiguration.	All Stratix Devices	
Configuration control block silicon issue, which causes program file incompatibility between engineering sample (ES) and production devices.	EP1S10 ES devices	EP1S10 production devices. Designers must recompile designs when moving from ES to production designs.
I/O element (IOE) register synchronous clear and preset.	EP1S25 revision A and B devices	EP1S25 revision C and later devices.
Release clears before tri-state.	EP1S25 revision A and B devices	EP1S25 revision C and later devices.
High current on power up.	EP1S10 ES devices EP1S25 ES devices	*(1)* EP1S25 production devices.
Enhanced and fast phase-locked loop (PLL) lock circuit does not operate below –20 °C for phase frequency detector (PFD) frequencies of 200 MHz or below.	All industrial temperature grade Stratix devices. Designs that do not use the `LOCK` signal are not affected by this issue.	*(2)*
Gated lock (`GLOCK`).	All Stratix devices	*(3)*
Enhanced PLL clock switchover glitch.	All Stratix devices	*(4)*

Table 1. Stratix Family Issues (Part 2 of 2)

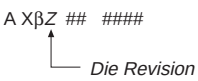
Issue	Affected Devices	Fixed Devices
Parallel on-chip termination feature is not functional. Series and differential on-chip termination features are functional, with updated details.	All Stratix devices	*(2)*
V_{CCSEL} dedicated input	All Stratix devices	See "V_{CCSEL} Dedicated Input" on page 9 for more information.
Configuration RAM bit errors not due to a single event upset (SEU) may occur when the Error Detection CRC feature is enabled on Stratix devices.	All Stratix devices	*(5)*

Notes to Table 1:

(1) Contact Altera® Applications for information on EP1S10 devices regarding this problem.
(2) Contact Altera Applications for more information regarding this issue.
(3) Altera is offering a permanent work around for this feature. See "Gated Lock (GLOCK)" on page 5 for more information.
(4) Altera is offering a permanent work around for this feature. See "Enhanced PLL Clock Switchover Glitch" on page 7 for more information.
(5) Altera is implementing a permanent solution for this feature. See "The maximum wait time between a reconfiguration is done and the `areset` signal is asserted is 2 µs." on page 12 for more information.

The die revision is identified by the alphanumeric character (Z) before the fab code (first two alphanumeric characters) in the date code printed on the top side of the device. Figure 1 shows a Stratix device's top side date code.

Figure 1. Stratix Device Top Side Lot Number



The information found in "Stratix Family Issues" on page 5 also applies to Stratix GX devices.

EP1S10 Device Issue

There is a silicon issue in the control block circuitry that affects all modes of configuration, requiring a software change in the Quartus® II configuration algorithms for ES devices. The Quartus II software version 2.1 service pack 1 and higher enables correct configuration support for EP1S10 ES devices. Designers must recompile their design when moving from EP1S10 ES devices to EP1S10 production devices. EP1S10 ES devices

cannot be configured by production EP1S10 device configuration files and production EP1S10 devices cannot be configured by EP1S10 ES device configuration files.

When designing with Stratix EP1S10 devices, designers must use the EP1S10 ES ordering codes in the Quartus II software version 2.1 service pack 1 and higher. In the Quartus II software (versions later than 2.1 service pack 1), EP1S10 ES ordering codes may be hidden. For assistance on using hidden ordering codes, contact Altera Applications. When targeting EP1S10 ES devices, the Quartus II software version 2.1 service pack 1 generates correct configuration files for the ES devices. Designers must use the ES ordering codes in the Quartus II software when compiling for ES devices and the production ordering codes when compiling for production devices. EP1S10 ES devices cannot be configured by production EP1S10 device configuration files and production EP1S10 devices cannot be configured by EP1S10 ES device configuration files. The Quartus II software version 2.2 service pack 2 has full support for EP1S10 production ordering codes.

Designs for EP1S10 ES devices must be recompiled when moving to EP1S10 production devices. The EP1S10 ES device Serial Object File (**.sof**) size will remain the same as the production file. The configuration algorithm that accesses the SOF and configures the device(s) contains updated information that allows both EP1S10 ES and production devices to configure correctly. All other configuration files contain overhead bits that identify the device as an EP1S10 ES device. Programmer Object File (**.pof**), Raw Binary File (**.rbf**), Tabular Text File (**.ttf**), and Hexidecimal File (**.hex**) programming files for revision A and B devices generated by the Quartus II software version 2.1 service pack 1 are larger than documented production file sizes because of the required changes in the overhead bits. The file sizes for the production EP1S10 devices match the documented file sizes.

No board or pin-out change is required when moving from EP1S10 ES devices to EP1S10 production devices.

EP1S25 Device Issues

The following silicon issues only affect the EP1S25 revision A and B devices:

- IOE register synchronous clear and preset
- `RELEASE_CLEARS_BEFORE_TRI_STATES` logic option

IOE Register Synchronous Clear and Preset

Synchronous clear and preset signals cannot be used on IOE input registers.

Contact a local Altera FAE or Altera Applications for software support on this issue.

Release Clears Before Tri-States

When the RELEASE_CLEARS_BEFORE_TRI_STATES option is used with EP1S25 revision A and B devices, registers clocked by internal global clock nets (including PLL outputs) will power up in an unknown state instead of the state specified by the user.

When the RELEASE_CLEARS_BEFORE_TRI_STATES option is turned on, the designer must reset the device to operate correctly.

The RELEASE_CLEARS_BEFORE_TRI_STATES configuration option directs the device to release the clear signal on registered logic cells and I/O cells before releasing the output enable override on tri-state buffers. If this option is turned off, the output enable signals are released before the clear overrides are released. This option will be turned off by default. When the designer turns this option on, the Quartus II software generates the following warning message: "Release clears before tri-states option is turned on. If you are using EP1S25 revision A or B devices, contact Altera Applications."

EP1S10 & EP1S25 High Power-Up Current Issue

EP1S10 ES devices typically require a 750-mA current on the V_{CCINT} voltage supply to successfully power up. EP1S25 ES devices typically require a 2.5-A current on the V_{CCINT} voltage supply to successfully power up the device. Designers should select power supplies and regulators that can supply this amount of current when designing with EP1S10 and EP1S25 ES devices.

EP1S25 production devices are fixed and require significantly less power-up current.

For more information on EP1S10 devices, contact Altera Applications.

Stratix Industrial Temperature Grade Device Issues

The PLL lock circuit in Stratix industrial temperature grade devices is not functional when the ambient temperature is below –20 °C and the PFD frequency is at or below 200 MHz.

To work around this issue, choose a higher input frequency and an *N* counter value such that the input frequency to the PFD (inclk/*N*) is above 200 MHz. This guarantees correct operation of the LOCK signal.

Although the LOCK signal on the enhanced and fast PLL toggles under the conditions outlined above, the PLL is still in LOCK and the output clock is within specifications. This issue is a limitation of the LOCK circuit inside the Stratix PLLs.

Stratix Family Issues

The following issues affect all Stratix and Stratix GX devices.

- Gated lock (GLOCK)
- Enhanced PLL clock switchover glitch
- On-chip termination value tolerance
- V_{CCSEL} dedicated input
- Error detection CRC issue

Gated Lock (GLOCK)

The enhanced PLL includes a programmable counter that holds the lock signal low for a user-selected number of input clock transitions. This allows the PLL to lock before enabling the lock signal.

There is a run-through problem in the GLOCK counter that causes the counter to operate incorrectly. Support for the gated_lock circuitry was disabled in the Quartus II software version 2.1. Therefore, the gated_lock feature is unavailable in Stratix devices.

The work around for this problem is to gate the lock signal in internal logic. Altera recommends using a two-input AND gate to gate the lock signal with a counter. The number of bits in the counter (LPM_WIDTH) can be adjusted to control how many clock cycles before the gated_lock signal is released. The counter width in the reference design is currently 3. See Figure 2.

Figure 2. Gated Lock in Internal Logic Circuit

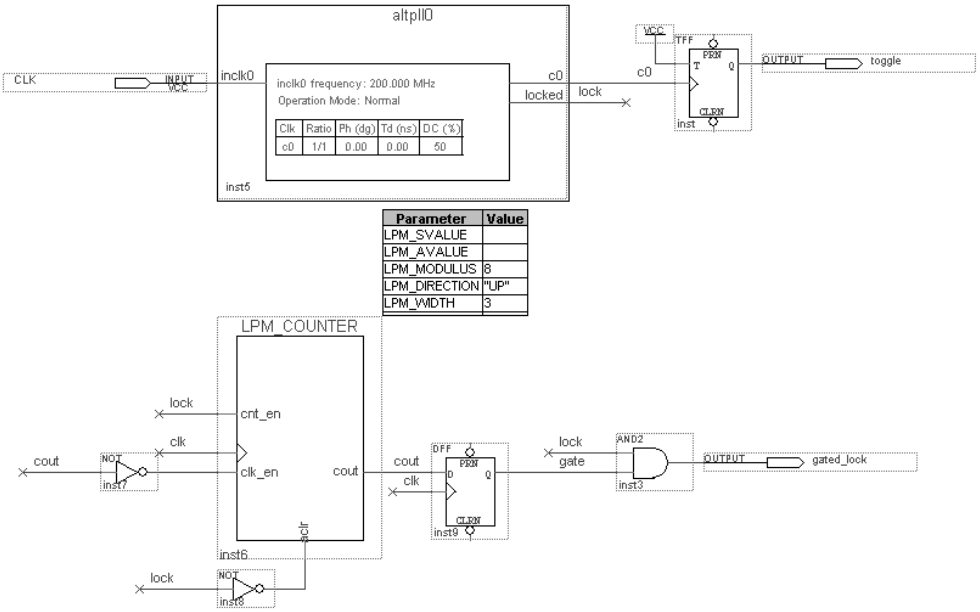
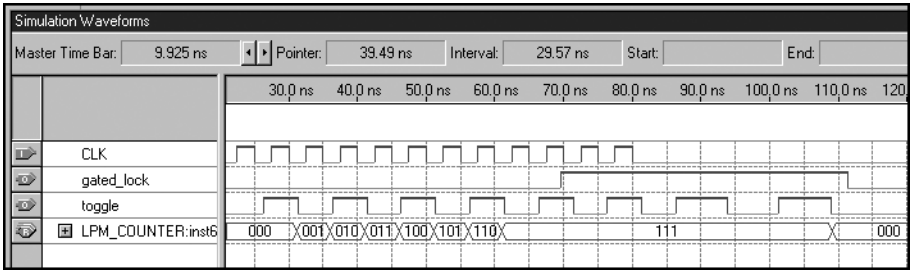


Figure 3 shows the simulation waveform of the gated lock signal.The `gated_lock` signal transitions high on the 10th clock cycle and is driven low after the PLL loses lock. The toggle signal frequency decreases as the V_{CO} frequency of the PLL begins to drift.

Figure 3. Gated Lock Signal Simulation Waveform



Enhanced PLL Clock Switchover Glitch

The CLKBAD0 and CLKBAD1 signals have a design flaw that cause a glitch on the signals. The glitches last for up to a half clock cycle of the input clock to the PLL. To prevent switchover from happening prematurely, a monitoring circuit is used to require the CLKBAD signal for the selected clock to be high for four consecutive system clock cycles before the PLL will switchover to the other clock.

The activeclock output port of the PLL megafunction is used to indicate which input clock is currently selected by the switchover circuitry. A low signal on activeclock indicates that inclk0 is selected and a high signal indicates inclk1 is selected. CLKBAD0, CLKBAD1, and activeclock are available outputs of the ALTPLL megafunction and can be used by designers to control the switchover internally.

To work around this issue, designers need to use the monitoring circuit as shown in Figure 4 when designing for clock switchover. The monitoring circuit watches CLKBAD0, CLKBAD1, and the activeclock signals from the PLL. The monitoring circuit switches the PLL from inclk0 to inclk1 when CLKBAD0 is detected for four consecutive system clock cycles; the monitoring circuit switches the PLL back from inclk1 to inclk0 when CLKBAD1 is detected for four consecutive system clock cycles.

In the circuit shown in Figure 4, CLK0 is the primary clock and CLK1 is the secondary clock. The locked signal can be used in the core and external to the device for monitoring the lock status of the PLL. The ALTPLL megafunction also has a clkloss output signal that can be monitored to determine when the clock switchover circuit initiates. clkloss goes high when the input clock is lost. If the primary clock fails and the secondary clock is not available, the clock switchover circuit continues to wait for a good secondary clock. The activeclock signal can be used in the core and external to the device for monitoring whether inclk0 or inclk1 is selected as the input clock to the PLL. A system clock that is guaranteed to be running at all times after the Stratix device is configured should be used to clock the monitoring circuit. Verilog HDL, VHDL, and schematic files are available in the reference design. It also contains waveform simulation and Verilog HDL and VHDL test bench files.

Figure 4. Clock Switchover Circuit

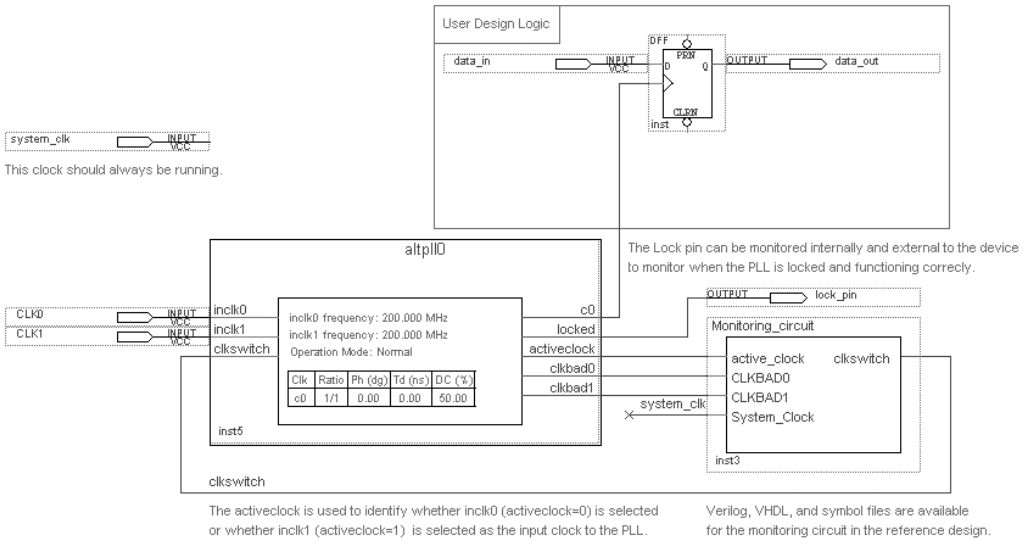


Figure 5 shows the simulation waveform of the PLL switching events. When CLKBAD0 is high for four consecutive system clock cycles, the PLL switches to CLK1 as the primary clock. After CLKBAD1 is high for four consecutive system clock cycles, the PLL switches back to CLK0 as the primary clock.

Figure 5. Simulation Results of Switchover Event

On-Chip Termination Value Tolerance

The specification for on-chip termination in Stratix devices has been updated. The parallel on-chip termination circuitry does not conform to the initial specification and is not functional. Differential termination is functional and the updated specifications are shown in Table 2. Series on-chip termination is available with a programmable drive strength solution. For more details, please contact your Altera representative.

Table 2. Stratix Termination Performance

On-Chip Termination Type	Accuracy Specification				Notes
	Min	Typ	Max	Unit	
Parallel	Not functional.				Designs must use external resistors.
Series	Please contact your Altera representative.				Implemented with programmable drive strength.
Differential (LVDS)	110	137.5	165	Ω	Commercial temperature grade devices *(1)*.
	100	135	170	Ω	Industrial temperature grade devices *(1)*.

Note to Table 2:
(1) See the *Stratix Device Family Data Sheet* in Volume 1 of the *Stratix Device Handbook* for more detailed specifications.

The Stratix device on-chip termination circuitry will not be updated. Designers should not use parallel on-chip termination in Stratix devices. Altera recommends using external resistors. Series and differential on-chip termination are functional and should be used with appropriate simulations.

V_{CCSEL} Dedicated Input

V_{CCSEL} is a dedicated input that is used to choose the input buffer for the dedicated configuration input pins and was originally described as follows:

- V_{CCSEL}=0 is used when interfacing with 2.5 V/3.3 V configuration signals
- V_{CCSEL}=1 is used when interfacing with 1.5 V/1.8 V configuration signals

However, what was not originally documented is that V_{CCSEL} also sets the power-on reset (POR) trip point for all the configuration related I/O banks to ensure that these I/O banks have powered up to the appropriate voltage levels before configuration begins.

Issue

Upon power-up, the FPGA will not release `nSTATUS` until the core V_{CC} and all of the V_{CCIO} of the configuration related I/O banks (including top/bottom I/O banks numbered 3, 4, 7, and 8) are above their POR trip points.

If a user selects V_{CCSEL}=0, this sets the POR trip point for all configuration related I/O banks to a voltage consistent with 3.3-V signaling. When VCCSEL=0, the POR trip point for these IO banks may be as high as 1.8 volts. If the voltage supplied to the V_{CCIO} pins of the configuration banks is < 1.8 V, it is possible that these banks may never reach the POR trip point, causing the device to never attempt configuration.

Both 1.8 V and 1.5-V V_{CCIO} settings are affected because the minimum allowable V_{CCIO} for either is <1.8 V, which is lower than the trip point.

Impact

This problem only affects designs with all of the following characteristics:

- Use a configuration solution that is 2.5/3.3 V
- Set V_{CCIO} to 1.5 or 1.8V in any of the configuration I/O banks
- Set the V_{CCSEL} to 0

A good example of this is an RLDRAM II (1.5-V HSTL) user with an EPC8 used to configure a EP1S25 with V_{CCSEL} set to 0.

Solution

Designs that require 2.5/3.3 V configuration signaling and 1.5 or 1.8-V I/O V_{CCIO} in configuration banks (banks 3, 4, 7, or 8) must tie V_{CCSEL} to V_{CCIO} or a stable logic-level 1 in order to lower the POR trip point and enable successful configuration. This solution has been tested by Altera and this requirement will be cited in all current and future documentation (including the Device and Configuration Handbooks).

Altera recommends that V_{CCSEL} be pulled to the V_{CCIO} of the bank in which it resides although V_{CCSEL} could also be tied to a logic-level 1 that is guaranteed to be stable and completely powered during FPGA power-up.

Timing Model Update for I/O Timing

The Stratix I/O timing model is scheduled to be updated in the Quartus II software version 4.1 to address the inaccuracy of the I/O timing reported in the Quartus II software version 4.0 and earlier. There is no change or impact to the I/O performance or I/O timing of the silicon.

For more information on this issue, contact Altera Applications or check the Altera Support Center on the Altera web site.

PLL Reconfiguration

Certain instances of PLL reconfiguration cause the `scandataout` signal to become stuck in the high position. The following cases explain when this incorrect device operation will occur. These sections also provide work arounds for the issue.

Reconfiguring Post-Scale Counters

After all the `scandata` bits are loaded into the scan chain, any changes to the post-scale (G,L, and E) counters are updated automatically and correctly, but the `scandataout` signal will remain high. The `busy` signal in the altpll_reconfig megafunction will also be affected by this issue since the `busy` signal follows the `scandataout` signal generated from the reconfiguration block. To work around this problem after the `scandataout` signal goes high, wait for a certain time specified by $T_{RECONFIGWAIT}$, then reset the PLL for at least 500 ns using the PLLs `areset` signal to ensure that the `scandataout` signal goes back low. The time required for the wait after the reconfiguration is done and the areset is applied can be calculated by the formula:

$T_{RECONFIGWAIT}$ = (Max C-counter)/(0.8*VCO freq)

The maximum wait time between a reconfiguration is done and the `areset` signal is asserted is 2 µs.

Reconfiguring N or M Counters

After all the `scandata` bits are loaded into the scan chain, any changes to the *N* or *M* (count value) are not updated and the `scandataout` signal will remain high. To work around this problem, after the `scandataout` signal goes high, wait for a certain time specified by $T_{RECONFIGWAIT}$ and then reset the PLL for at least 500 ns using the PLLs `areset` signal to ensure that the `scandone` signal goes back low and the new (N, M) counter settings are updated successfully. The time required for the wait after the reconfiguration is done and the `areset` is applied can be calculated by the formula:

$T_{RECONFIGWAIT}$ = (Max C-counter)/(0.8*VCO freq)

The maximum wait time between a reconfiguration is done and the `areset` signal is asserted is 2 µs.

Error Detection CRC Issue

A single event upset (SEU) can cause configuration RAM bits to change. The Error Detection CRC feature on Stratix devices detects a configuration RAM bit flip due to such events. However, the Error Detection CRC circuitry itself may corrupt the configuration RAM bits in certain cases, possibly resulting in functional failures. This issue affects all Stratix devices.

The solution to this issue is to restrict the use of certain routing resources. This solution is available beginning with version 5.0 SP2 of the Quartus II software. The solution takes effect only when the Error Detection CRC feature is enabled. Designers using the Error Detection CRC feature need to recompile their designs using the updated software to prevent the issue from happening.

This solution may increase fit time and routing resource usage. The solution may also decrease device core f_{MAX}. Designers must check recompiled results to ensure all original design targets are still met. If the design cannot meet constraints and timing after recompilation, designers can disable the Error Detection CRC feature without any performance, fit time, and routing resource changes. Contact Altera Technical Support for this option.

Revision History

The information contained in the *Stratix FPGA Family Errata Sheet* version 3.1 supersedes information published in previous versions.

Version 3.1

The *Stratix FPGA Family Errata Sheet* version 3.1 contains the following changes.

Updated "PLL Reconfiguration"section with the $T_{RECONFIGWAIT}$ specification.

Version 3.0

The *Stratix FPGA Family Errata Sheet* version 3.0 contains the following changes.

Updated "Stratix Family Issues"section.

Version 2.9

The *Stratix FPGA Family Errata Sheet* version 2.9 contains the following changes.

Added the "The maximum wait time between a reconfiguration is done and the `areset` signal is asserted is 2 µs." section.

Version 2.8

The *Stratix FPGA Family Errata Sheet* version 2.8 contains the following changes.

Added the "PLL Reconfiguration" section.

Version 2.7

The *Stratix FPGA Family Errata Sheet* version 2.7 contains the following changes.

Added the "Timing Model Update for I/O Timing" section.

Version 2.6

The *Stratix FPGA Family Errata Sheet* version 2.6 contains the following changes.

Added the "V_{CCSEL} Dedicated Input" section.

Version 2.5

The *Stratix FPGA Family Errata Sheet* version 2.5 contains the following changes.

- Updated Table 1 with on-chip termination information.
- Updated the "On-Chip Termination Value Tolerance" section.

Version 2.4

The *Stratix FPGA Family Errata Sheet* version 2.4 contains the following changes.

- Updated Table 1 with fast and enhanced PLL information.
- Added the "Stratix Industrial Temperature Grade Device Issues" section.

101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
www.altera.com
Applications Hotline:
(800) 800-EPLD
Literature Services:
lit_req@altera.com