Pin Information for the Cyclone® V 5CGXFC9 Device
Version 1.1
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
GXB_L1		REFCLK1Ln					G4				
GXB_L1		REFCLK1Lp					F5				
GXB_L1		GXB_TX_L4n					E1				
GXB_L1		GXB_TX_L4p					E2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
GXB_L1		GXB_TX_L3n					J1				
GXB_L1		GXB_TX_L3p					J2				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1				
GXB_L0		GXB_TX_L2n					N1				
GXB_L0		GXB_TX_L2p					N2				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1				
GXB_L0		GXB_TX_L1n					U1				
GXB_L0		GXB_TX_L1p					U2				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					W2				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1				
GXB_L0		GXB_TX_L0n					Y3				
GXB_L0		GXB_TX_L0p					Y4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1				
GXB_L0		REFCLK0Lp					V4				
GXB_L0		REFCLK0Ln					U4				
3A		TDO		TDO			V3				
3A		nCSO		DATA4			AB6				
3A		TMS		TMS			R4				
3A		AS_DATA3		DATA3			AA5				
3A		TCK		TCK			V5				
3A		AS_DATA2		DATA2			T5				
3A		TDI		TDI			P5				
3A		AS_DATA1		DATA1			W5				
3A		DCLK		DCLK			M5				
3A		AS_DATA0,ASDO		DATA0			AB4				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	P6	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	N6	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U6	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	M6	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	R5	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	M7	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	R6				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R7	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	L7	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T7	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	L8	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	T8				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	P7	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	T9				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P8	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	V8			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	N8	DQ5B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	W8	DQ5B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	M8	DQ5B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	N9	DQSn5B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA7	DQ5B		B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	N10	DQS5B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AB7			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	Y7	DQ5B		B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	U8	DQ5B		B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	W7	DQ5B		B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	V9	DQ5B		B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	R9				
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AB8	DQ5B		B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p	DIFFOUT_B39p	P9				
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AA8	DQ5B		B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	Y10			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AA9	DQ6B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AA10	DQ6B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	Y9	DQ6B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	L9	DQSn6B		B_CK#	B_CK#

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	W11	DQ6B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	M10	DQS6B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	Y11			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B45n	DIFFOUT_B45n	AB10	DQ6B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	U10	DQ6B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AB11	DQ6B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	U11	DQ6B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	T10				
3B	VREFB3BN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	R11	DQ6B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	R10				
3B	VREFB3BN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	P12	DQ6B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B49n	DIFFOUT_B49n	AA13				
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	W12	DQ7B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB13	DQ7B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	Y12	DQ7B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	U12	DQSn7B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	R12	DQ7B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	T12	DQS7B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	T13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AB15	DQ7B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	W13	DQ7B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AB16	DQ7B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	V13	DQ7B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	T14				
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AB18	DQ7B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B55p	DIFFOUT_B55p	U13				
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AA18	DQ7B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AA19			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	Y14	DQ8B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	Y19	DQ8B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	W14	DQ8B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	P14	DQSn8B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AA20	DQ8B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	R14	DQS8B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	Y20			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AA15	DQ8B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	U15	DQ8B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	Y15	DQ8B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	V15	DQ8B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	R15				
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AB20	DQ8B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B63p	DIFFOUT_B63p	T15				
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AB21	DQ8B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AB22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	Y16	DQ9B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AA22	DQ9B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	Y17	DQ9B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	U16	DQSn9B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AA17	DQ9B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	U17	DQS9B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AB17			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	Y22	DQ9B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	V18	DQ9B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	Y21	DQ9B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	W18	DQ9B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	W16			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	W21	DQ9B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	W17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	W22	DQ9B	DQ1B	B_DM_2	B_DM_2
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	U22	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	V20				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	U21	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V19				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T17	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	T20	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	T18	DQ1R			
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	T22				
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	R22	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	R20	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	R19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	R21				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P19	DQ1R			
5B	VREFB5BN0	IO			DIFFIO_RX_R25p	DIFFOUT_R25p	P16				
5B	VREFB5BN0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	P21	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_RX_R25n	DIFFOUT_R25n	N16				
5B	VREFB5BN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	P22	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	N20	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_TX_R28p	DIFFOUT_R28p	M22	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	N21	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_TX_R28n	DIFFOUT_R28n	L22	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	P18	DQS4R			
5B	VREFB5BN0	IO			DIFFIO_TX_R30p	DIFFOUT_R30p	K22				
5B	VREFB5BN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	N18	DQSn4R			
5B	VREFB5BN0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	J22	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	M21	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	F22	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	M20	DQ4R			
5B	VREFB5BN0	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	E22				
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R33p	DIFFOUT_R33p	M16				
5B	VREFB5BN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	E21	DQ5R			
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	M17				
5B	VREFB5BN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	D22	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	L19	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R36p	DIFFOUT_R36p	K21	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	L20	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R36n	DIFFOUT_R36n	J21	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	L15	DQS5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	G22				
5B	VREFB5BN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	K15	DQSn5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	G21	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	L18	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	G20	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	K19	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	H21				
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R41p	DIFFOUT_R41p	L17				
5B	VREFB5BN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	E20	DQ6R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R41n	DIFFOUT_R41n	K17				
5B	VREFB5BN0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	F20	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	H20	DQ6R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	G18	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	H19	DQ6R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	G17	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	K16	DQS6R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	F19				
5B	VREFB5BN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	J16	DQSn6R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	F18	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	J17	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	J19	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	J18	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	H18				
		GND					F17				
7A	VREFB7AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	H16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C21	DQ4T	DQ1T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	G16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C20	DQ4T	DQ1T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	D18	DQ4T	DQ1T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	B20	DQ4T	DQ1T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	E17	DQ4T	DQ1T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B21	DQ4T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	G15	DQS4T	DQS1T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B22			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	G14	DQSn4T	DQSn1T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	A22	DQ4T	DQ1T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	E16	DQ4T	DQ1T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	A20	DQ4T	DQ1T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	D17	DQ4T	DQ1T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	A19			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T33p	DIFFOUT_T33p	G13				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	C19	DQ5T	DQ1T	T_DM_1	T_DM_1

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T33n	DIFFOUT_T33n	F14				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	C18	DQ5T	DQ1T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	C16	DQ5T	DQ1T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	B16	DQ5T	DQ1T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C15	DQ5T	DQ1T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	B15	DQ5T	DQ1T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	G12	DQS5T	DQ1T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	A18			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	H12	DQSn5T	DQ1T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	A17	DQ5T	DQ1T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	F15	DQ5T	DQ1T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	B18	DQ5T	DQ1T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	E14	DQ5T	DQ1T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	B17			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T41p	DIFFOUT_T41p	H10				
7A	VREFB7AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	A15	DQ6T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T41n	DIFFOUT_T41n	G11				
7A	VREFB7AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	A14	DQ6T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	D13	DQ6T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	C14	DQ6T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	C13	DQ6T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	D14	DQ6T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	H9	DQS6T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	A13			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	G8	DQSn6T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	B13	DQ6T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	E12	DQ6T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	B12	DQ6T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	F12	DQ6T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T48n	DIFFOUT_T48n	A12				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T49p	DIFFOUT_T49p	G10				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	C11	DQ7T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T49n	DIFFOUT_T49n	F10				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	B11	DQ7T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	D11	DQ7T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	A8	DQ7T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	E11	DQ7T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	A7	DQ7T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	J9	DQS7T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	F8			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	J8	DQSn7T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	E7	DQ7T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	C10	DQ7T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	C6	DQ7T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	C9	DQ7T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	D7			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	K7				
8A	VREFB8AN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	A10	DQ8T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T57n	DIFFOUT_T57n	J7				
8A	VREFB8AN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	A9	DQ8T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	D9	DQ8T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	B6	DQ8T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	D8	DQ8T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	B5	DQ8T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T61p	H8	DQS8T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	C8			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T61n	G7	DQSn8T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	B8	DQ8T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	H6	DQ8T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	E6	DQ8T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	G6	DQ8T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	F7			GND	GND
9A		MSEL0		MSEL0			L6				
9A		CONF_DONE		CONF_DONE			J6				
9A		MSEL1		MSEL1			K6				
9A		nSTATUS		nSTATUS			G5				
9A		nCE		nCE			H5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			E5				
9A		nCONFIG		nCONFIG			A4				
9A		MSEL4		MSEL4			C5				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					F3				
		GND					M9				
		GND					V22				
		GND					L3				
		GND					N11				
		GND					W20				
		GND					F11				
		GND					C3				
		GND					Y8				
		GND					K14				
		GND					D1				
		GND					K8				
		GND					V2				
		GND					C7				
		GND					A5				
		GND					B2				
		GND					M14				
		GND					M4				
		GND					G9				
		GND					D2				
		GND					L5				
		GND					J5				
		GND					K1				
		GND					F1				
		GND					C22				
		GND					AB1				
		GND					L16				
		GND					C4				
		GND					H2				
		GND					H1				
		GND					J13				
		GND					AB2				
		GND					E4				
		GND					AB19				
		GND					D5				
		GND					J20				
		GND					V17				
		GND					A11				
		GND					U5				
		GND					G3				
		GND					H14				
		GND					T11				
		GND					M2				
		GND					J15				
		GND					D10				
		GND					J3				
		GND					L13				
		GND					F6				
		GND					H4				
		GND					U9				
		GND					N7				
		GND					U19				
		GND					N15				
		GND					K12				
		GND					AA11				
		GND					K2				
		GND					E3				
		GND					P10				
		GND					A21				
		GND					F2				
		GND					M1				
		GND					P1				
		GND					K10				
		GND					Y5				
		GND					D20				
		GND					B14				
		GND					Y2				
		GND					T2				
		GND					K4				
		GND					P4				
		GND					C17				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					M12				
		GND					N22				
		GND					Y1				
		GND					N13				
		GND					W4				
		GND					AA3				
		GND					B1				
		GND					U14				
		GND					R3				
		GND					AA16				
		GND					T1				
		GND					AA4				
		GND					H3				
		GND					V1				
		GND					F21				
		GND					N5				
		GND					M19				
		GND					U3				
		GND					J11				
		GND					Y13				
		GND					E13				
		GND					P2				
		GND					N3				
		GND					R13				
		GND					L11				
		GND					W3				
		GND					F16				
		VCC					M13				
		VCC					K13				
		VCC					J10				
		VCC					M11				
		VCC					P13				
		VCC					H15				
		VCC					M15				
		VCC					N14				
		VCC					L12				
		VCC					J12				
		VCC					H13				
		VCC					L10				
		VCC					K9				
		VCC					P11				
		VCC					P15				
		VCC					N12				
		VCC					H11				
		VCC					J14				
		VCC					L14				
		VCC					K11				
		DNU					B3				
		DNU					B4				
		DNU					AB3				
		DNU					V11				
		DNU					D21				
		DNU					E10				
		VCCPGM					Y6				
		VCCPGM					U20				
		VCCPGM					B7				
		VCCBAT					A3				
		VCCIO3A					AA6				
		VCCIO3A					T6				
		VCCIO3B					R8				
		VCCIO3B					AB9				
		VCCIO3B					W10				
		VCCIO3B					V7				
		VCCIO4A					Y18				
		VCCIO4A					W15				
		VCCIO4A					T16				
		VCCIO4A					V12				
		VCCIO4A					AB14				
		VCCIO4A					AA21				
		VCCIO5A					T21				
		VCCIO5A					R18				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	U484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		VCCIO5B					G19				
		VCCIO5B					N17				
		VCCIO5B					P20				
		VCCIO5B					K18				
		VCCIO5B					L21				
		VCCIO5B					H22				
		VCCIO7A					H17				
		VCCIO7A					C12				
		VCCIO7A					D15				
		VCCIO7A					B19				
		VCCIO7A					A16				
		VCCIO7A					E18				
		VCCIO8A					E8				
		VCCIO8A					A6				
		VCCIO8A					H7				
		VCCIO8A					B9				
		VCCPD3A					V6				
		VCCPD3B4A					V14				
		VCCPD3B4A					V10				
		VCCPD3B4A					W9				
		VCCPD3B4A					V16				
		VCCPD5A					P17				
		VCCPD5B					N19				
		VCCPD5B					M18				
		VCCPD7A8A					E9				
		VCCPD7A8A					F13				
		VCCPD7A8A					F9				
		VCCPD7A8A					E15				
3A	VREFB3AN0	VREFB3AN0					W6				
3B	VREFB3BN0	VREFB3BN0					AB12				
4A	VREFB4AN0	VREFB4AN0					AA14				
5A	VREFB5AN0	VREFB5AN0					V21				
5B	VREFB5BN0	VREFB5BN0					K20				
7A	VREFB7AN0	VREFB7AN0					D16				
8A	VREFB8AN0	VREFB8AN0					B10				
		NC					C2				
		NC					C1				
		NC					D4				
		NC					D3				
		VCCH_GXBL					T3				
		VCCH_GXBL					M3				
		VCCL_GXBL					P3				
		VCCL_GXBL					K3				
		RREF_TL					A1				
		VCCA_FPLL					T4				
		VCCA_FPLL					F4				
		VCCA_FPLL					U18				
		VCCA_FPLL					E19				
		VCC_AUX					D19				
		VCC_AUX					AA12				
		VCC_AUX					W19				
		VCC_AUX					D6				
		VCC_AUX					D12				
		VCC_AUX					AB5				
		VCCE_GXBL					N4				
		VCCE_GXBL					L4				
		VCCE_GXBL					J4				
		VCCE_GXBL					K5				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2), (3)*	HMC Pin Assignment for LPDDR2 *(3)*
GXB_L1		REFCLK1Ln					F5				
GXB_L1		REFCLK1Lp					G4				
GXB_L1		GXB_TX_L5n					D3				
GXB_L1		GXB_TX_L5p					D4				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					C2				
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					C1				
GXB_L1		GXB_TX_L4n					E1				
GXB_L1		GXB_TX_L4p					E2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					G2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					G1				
GXB_L1		GXB_TX_L3n					J1				
GXB_L1		GXB_TX_L3p					J2				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					L2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					L1				
GXB_L0		GXB_TX_L2n					N1				
GXB_L0		GXB_TX_L2p					N2				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					R2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					R1				
GXB_L0		GXB_TX_L1n					U1				
GXB_L0		GXB_TX_L1p					U2				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					W2				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					W1				
GXB_L0		GXB_TX_L0n					Y3				
GXB_L0		GXB_TX_L0p					Y4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AA2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AA1				
GXB_L0		REFCLK0Lp					V4				
GXB_L0		REFCLK0Ln					U4				
3A		TDO		TDO			M5				
3A		nCSO		DATA4			R4				
3A		TMS		TMS			P5				
3A		AS_DATA3		DATA3			T4				
3A		TCK		TCK			V5				
3A		AS_DATA2		DATA2			AA5				
3A		TDI		TDI			W5				
3A		AS_DATA1		DATA1			AB3				
3A		DCLK		DCLK			V3				
3A		AS_DATA0,ASDO		DATA0			AB4				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	R6	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	R5	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	U8	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	P6	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	W8	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	N6	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	W9				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	T7	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	U6	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T8	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V6	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	M6				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	R7	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	M7				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	P7	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AB6			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	V9	DQ2B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AB5	DQ2B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	V10	DQ2B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	P8	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AA7	DQ2B		B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	N8	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AB7			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AA8	DQ2B		B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	T9	DQ2B		B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AB8	DQ2B		B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	U10	DQ2B		B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	M8				
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AA10	DQ2B		B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p	DIFFOUT_B39p	M9				
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AA9	DQ2B		B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	Y10			GND	GND

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2), (3)*	HMC Pin Assignment for LPDDR2 *(3)*
3B	VREFB3BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	T10	DQ3B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	Y9	DQ3B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	R9	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	U11	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	R12	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	U12	DQS3B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	P12			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B45n	DIFFOUT_B45n	AB10	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	R10	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AB11	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	R11	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	P9				
3B	VREFB3BN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	Y11	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	N9				
3B	VREFB3BN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AA12	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B49n	DIFFOUT_B49n	AB13				
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	V13	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AB12	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	U13	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	T12	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AA14	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	T13	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AA13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AB15	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	Y14	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AA15	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	Y15	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	V14				
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AB17	DQ4B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B55p	DIFFOUT_B55p	V15				
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AB18	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AB20			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	Y16	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AB21	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	Y17	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	T14	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AA17	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	U15	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AA18			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AA19	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	V20	DQ5B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AA20	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	W19	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	V16				
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AB22	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B63p	DIFFOUT_B63p	W16				
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AA22	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	Y22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	Y20	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	W22	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	Y19	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	P14	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	Y21	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	R14	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	W21			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	U22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	V19	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	V21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	V18	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	U16			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	U21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	U17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	U20	DQ6B	DQ1B	B_DM_2	B_DM_2
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	T19	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	T18				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	T20	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	T17				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	T22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	T15	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	R22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	R15	DQ1R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2), (3)*	HMC Pin Assignment for LPDDR2 *(3)*
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	R21				
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	R16	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	P22	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	R17	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	P19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	P16	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	P18				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	P17	DQ1R			
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R41p	DIFFOUT_R41p	N16				
5B	VREFB5BN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	N20	DQ2R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R41n	DIFFOUT_R41n	M16				
5B	VREFB5BN0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	N21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	N19	DQ2R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	M22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	M18	DQ2R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	L22	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	K17	DQS2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	M20				
5B	VREFB5BN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	L17	DQSn2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	M21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	L19	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	K21	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	L18	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	K22				
7A		GND					F17				
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	H21			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	E21	DQ1T		T_DM_4	T_DM_4
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	G21			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	D21	DQ1T		T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	E19	DQ1T		T_DQ_37	T_DQ_37
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C20	DQ1T		T_DQ_38	T_DQ_38
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	D19	DQ1T		T_DQ_36	T_DQ_36
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	B20	DQ1T		GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	J21	DQS1T		T_DQS_4	T_DQS_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	B18			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	J22	DQSn1T		T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	B17	DQ1T		T_DQ_35	T_DQ_35
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	C21	DQ1T		T_DQ_33	T_DQ_33
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	G22	DQ1T		T_DQ_34	T_DQ_34
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	B21	DQ1T		T_DQ_32	T_DQ_32
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	F22			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	K20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	B16	DQ2T	DQ1T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	K19			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	C16	DQ2T	DQ1T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	D17	DQ2T	DQ1T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	G17	DQ2T	DQ1T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	E16	DQ2T	DQ1T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	G16	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	G18	DQS2T	DQS1T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	J19			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	H18	DQSn2T	DQSn1T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	J18	DQ2T	DQ1T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	E15	DQ2T	DQ1T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	A15	DQ2T	DQ1T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	F15	DQ2T	DQ1T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	A14			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T33p	DIFFOUT_T33p	H16				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	J17	DQ3T	DQ1T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T33n	DIFFOUT_T33n	H15				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	K16	DQ3T	DQ1T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	C15	DQ3T	DQ1T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	G15	DQ3T	DQ1T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	B15	DQ3T	DQ1T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	F14	DQ3T	DQ1T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	H14	DQS3T	DQ1T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	B13			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	J13	DQSn3T	DQ1T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	A13	DQ3T	DQ1T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E14	DQ3T	DQ1T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	J11	DQ3T	DQ1T	T_DQ_10	T_DQ_10

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2), (3)*	HMC Pin Assignment for LPDDR2 *(3)*
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	F13	DQ3T	DQ1T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	H10			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T41p	DIFFOUT_T41p	H13				
7A	VREFB7AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	G11	DQ4T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T41n	DIFFOUT_T41n	G13				
7A	VREFB7AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	F12	DQ4T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	D13	DQ4T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	B12	DQ4T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	C13	DQ4T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	A12	DQ4T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	H11	DQS4T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	L8			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	G12	DQSn4T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	K9	DQ4T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	D12	DQ4T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C11	DQ4T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	E12	DQ4T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T48n	DIFFOUT_T48n	B11				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T49p	DIFFOUT_T49p	G10				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	L7	DQ5T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T49n	DIFFOUT_T49n	F10				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	K7	DQ5T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	J7	DQ5T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	H8	DQ5T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	J8	DQ5T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	G8	DQ5T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	J9	DQS5T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	A10			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	H9	DQSn5T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	A9	DQ5T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	B10	DQ5T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	A5	DQ5T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	C9	DQ5T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	B5			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	E10				
8A	VREFB8AN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	B6	DQ6T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T57n	DIFFOUT_T57n	F9				
8A	VREFB8AN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	B7	DQ6T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	A8	DQ6T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	C6	DQ6T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	A7	DQ6T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	D6	DQ6T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T61p	E9	DQS6T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	D7			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T61n	D9	DQSn6T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	C8	DQ6T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	G6	DQ6T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	F7	DQ6T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	H6	DQ6T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	E7			GND	GND
9A		MSEL0		MSEL0			L6				
9A		CONF_DONE		CONF_DONE			K6				
9A		MSEL1		MSEL1			J6				
9A		nSTATUS		nSTATUS			H5				
9A		nCE		nCE			G5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			E5				
9A		nCONFIG		nCONFIG			A4				
9A		MSEL4		MSEL4			F3				
9A		GND					C5				
		GND					J20				
		GND					L21				
		GND					N22				
		GND					T21				
		GND					Y18				
		GND					AB14				
		GND					V12				
		GND					AA6				
		GND					V7				
		GND					U5				
		GND					AA4				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2), (3)*	HMC Pin Assignment for LPDDR2 *(3)*
		GND					Y5				
		GND					U3				
		GND					R3				
		GND					P4				
		GND					P2				
		GND					N5				
		GND					L3				
		GND					M4				
		GND					L5				
		GND					K2				
		GND					J3				
		GND					K4				
		GND					H2				
		GND					H3				
		GND					J5				
		GND					G3				
		GND					H4				
		GND					F2				
		GND					B1				
		GND					E3				
		GND					AB19				
		GND					AB9				
		GND					AB2				
		GND					AB1				
		GND					AA11				
		GND					AA3				
		GND					Y2				
		GND					Y1				
		GND					W4				
		GND					W3				
		GND					V22				
		GND					V17				
		GND					V2				
		GND					V1				
		GND					U9				
		GND					T16				
		GND					T2				
		GND					T1				
		GND					R13				
		GND					P10				
		GND					P1				
		GND					N17				
		GND					N15				
		GND					N13				
		GND					N11				
		GND					N7				
		GND					N3				
		GND					M14				
		GND					M12				
		GND					M10				
		GND					M2				
		GND					M1				
		GND					L15				
		GND					L13				
		GND					L11				
		GND					K14				
		GND					K12				
		GND					K10				
		GND					K8				
		GND					K1				
		GND					J15				
		GND					H22				
		GND					H12				
		GND					H7				
		GND					H1				
		GND					G19				
		GND					G9				
		GND					F16				
		GND					F6				
		GND					F1				
		GND					E13				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2), (3)*	HMC Pin Assignment for LPDDR2 *(3)*
		GND					E4				
		GND					D20				
		GND					D10				
		GND					D5				
		GND					D2				
		GND					D1				
		GND					C17				
		GND					C4				
		GND					C3				
		GND					B14				
		GND					B9				
		GND					B2				
		GND					A21				
		GND					A11				
		VCC					P15				
		VCC					P13				
		VCC					P11				
		VCC					N14				
		VCC					N12				
		VCC					N10				
		VCC					M15				
		VCC					M13				
		VCC					M11				
		VCC					L16				
		VCC					L14				
		VCC					L12				
		VCC					L10				
		VCC					K15				
		VCC					K13				
		VCC					K11				
		VCC					J16				
		VCC					J14				
		VCC					J12				
		VCC					J10				
		DNU					B3				
		DNU					B4				
		DNU					Y6				
		DNU					V11				
		DNU					E17				
		DNU					L9				
		VCCPGM					V8				
		VCCPGM					R19				
		VCCPGM					F8				
		VCCBAT					A3				
		VCCIO3A					T6				
		VCCIO3A					Y8				
		VCCIO3B					R8				
		VCCIO3B					Y13				
		VCCIO3B					W10				
		VCCIO3B					T11				
		VCCIO4A					U19				
		VCCIO4A					AA21				
		VCCIO4A					AA16				
		VCCIO4A					W20				
		VCCIO4A					W15				
		VCCIO4A					U14				
		VCCIO5A					P20				
		VCCIO5A					R18				
		VCCIO5B					M19				
		VCCIO5B					K18				
		VCCIO7A					B19				
		VCCIO7A					H17				
		VCCIO7A					G14				
		VCCIO7A					F21				
		VCCIO7A					F11				
		VCCIO7A					E18				
		VCCIO7A					D15				
		VCCIO7A					C22				
		VCCIO7A					C12				
		VCCIO7A					A16				
		VCCIO8A					A6				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F484	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2), (3)*	HMC Pin Assignment for LPDDR2 *(3)*
		VCCIO8A					G7				
		VCCIO8A					E8				
		VCCIO8A					C7				
		VCCPD3A					W6				
		VCCPD3B4A					W12				
		VCCPD3B4A					W17				
		VCCPD3B4A					W14				
		VCCPD3B4A					W11				
		VCCPD5A					P21				
		VCCPD5B					M17				
		VCCPD5B					N18				
		VCCPD7A8A					D8				
		VCCPD7A8A					E11				
		VCCPD7A8A					D16				
		VCCPD7A8A					D14				
		VCCPD7A8A					C10				
3A	VREFB3AN0	VREFB3AN0					Y7				
3B	VREFB3BN0	VREFB3BN0					Y12				
4A	VREFB4AN0	VREFB4AN0					AB16				
5A	VREFB5AN0	VREFB5AN0					R20				
5B	VREFB5BN0	VREFB5BN0					L20				
7A	VREFB7AN0	VREFB7AN0					C14				
8A	VREFB8AN0	VREFB8AN0					B8				
		NC					H20				
		NC					G20				
		NC					F20				
		NC					F19				
		NC					F18				
		NC					E22				
		NC					E20				
		NC					D22				
		NC					C19				
		NC					C18				
		NC					B22				
		NC					A22				
		NC					A20				
		NC					A19				
		NC					A18				
		NC					A17				
		VCCH_GXBL					M3				
		VCCH_GXBL					T3				
		VCCL_GXBL					K3				
		VCCL_GXBL					P3				
		RREF_TL					A1				
		VCCA_FPLL					T5				
		VCCA_FPLL					F4				
		VCCA_FPLL					U18				
		VCCA_FPLL					H19				
		VCC_AUX					E6				
		VCC_AUX					D11				
		VCC_AUX					W18				
		VCC_AUX					W13				
		VCC_AUX					W7				
		VCC_AUX					D18				
		VCCE_GXBL					J4				
		VCCE_GXBL					N4				
		VCCE_GXBL					L4				
		VCCE_GXBL					K5				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the
Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.
(3) This package supports only a 24-bit HMC using T_DQ_[0..23] pins. The T_DQ_[32..39] pins cannot be used for HMC.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
GXB_L2		GXB_TX_L8n					C3				
GXB_L2		GXB_TX_L8p					C4				
GXB_L2		GXB_RX_L8p,GXB_REFCLK_L8p					D2				
GXB_L2		GXB_RX_L8n,GXB_REFCLK_L8n					D1				
GXB_L2		GXB_TX_L7n					E3				
GXB_L2		GXB_TX_L7p					E4				
GXB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					F2				
GXB_L2		GXB_RX_L7n,GXB_REFCLK_L7n					F1				
GXB_L2		GXB_TX_L6n					G3				
GXB_L2		GXB_TX_L6p					G4				
GXB_L2		GXB_RX_L6p,GXB_REFCLK_L6p					H2				
GXB_L2		GXB_RX_L6n,GXB_REFCLK_L6n					H1				
GXB_L2		REFCLK2Lp					M6				
GXB_L2		REFCLK2Ln					L5				
GXB_L1		REFCLK1Ln					P6				
GXB_L1		REFCLK1Lp					N7				
GXB_L1		GXB_TX_L5n					K1				
GXB_L1		GXB_TX_L5p					K2				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					M2				
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					M1				
GXB_L1		GXB_TX_L4n					P1				
GXB_L1		GXB_TX_L4p					P2				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					T2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					T1				
GXB_L1		GXB_TX_L3n					W3				
GXB_L1		GXB_TX_L3p					W4				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					V2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					V1				
GXB_L0		GXB_TX_L2n					AA3				
GXB_L0		GXB_TX_L2p					AA4				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					Y2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					Y1				
GXB_L0		GXB_TX_L1n					AC3				
GXB_L0		GXB_TX_L1p					AC4				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AB2				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AB1				
GXB_L0		GXB_TX_L0n					AE3				
GXB_L0		GXB_TX_L0p					AE4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AD2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AD1				
GXB_L0		REFCLK0Lp					V6				
GXB_L0		REFCLK0Ln					W6				
3A		TDO		TDO			V7				
3A		nCSO		DATA4			Y6				
3A		TMS		TMS			R6				
3A		AS_DATA3		DATA3			U6				
3A		TCK		TCK			Y5				
3A		AS_DATA2		DATA2			AB5				
3A		TDI		TDI			T6				
3A		AS_DATA1		DATA1			AD5				
3A		DCLK		DCLK			N8				
3A		AS_DATA0,ASDO		DATA0			AF5				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	T7	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	U7				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	T8	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	V8	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	W8	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AB6	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	Y9	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AA6				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R10	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AA7	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	R9	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	Y8	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	R8				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AD6	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	P8				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AD7	DQ1B			
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	U9			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	Y11	DQ2B		B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	T9	DQ2B		B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	W11	DQ2B		B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	T11	DQSn2B		B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AC10	DQ2B		B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	R11	DQS2B		B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AB10			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AC8	DQ2B		B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AB11	DQ2B		B_A_9	B_CA_9

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AC9	DQ2B		B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AB12	DQ2B		B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	T12				
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	Y10	DQ2B		B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p	DIFFOUT_B39p	T13				
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	W10	DQ2B		B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	V9			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AE8	DQ3B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	V10	DQ3B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AD8	DQ3B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	P10	DQSn3B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AF9	DQ3B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	N10	DQS3B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AE9			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B45n	DIFFOUT_B45n	AF8	DQ3B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	U11	DQ3B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AF7	DQ3B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	U10	DQ3B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	P12				
3B	VREFB3BN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AF6	DQ3B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	P11				
3B	VREFB3BN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AE6	DQ3B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B49n	DIFFOUT_B49n	AE11				
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AA14	DQ4B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AD11	DQ4B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	Y14	DQ4B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	W13	DQSn4B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AD12	DQ4B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	V13	DQS4B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AD13			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AE10	DQ4B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	Y13	DQ4B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AD10	DQ4B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	W12	DQ4B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	V12				
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AF12	DQ4B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B55p	DIFFOUT_B55p	U12				
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AF11	DQ4B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AC13			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AC15	DQ5B	DQ1B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AC14	DQ5B	DQ1B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AB15	DQ5B	DQ1B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	V14	DQSn5B	DQ1B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AF13	DQ5B	DQ1B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	U14	DQS5B	DQ1B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AE13			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AF14	DQ5B	DQ1B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AB16	DQ5B	DQ1B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AE14	DQ5B	DQ1B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AA16	DQ5B	DQ1B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	Y16				
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AF18	DQ5B	DQ1B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B63p	DIFFOUT_B63p	Y15				
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AE18	DQ5B	DQ1B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AD18			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AD16	DQ6B	DQ1B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AC18	DQ6B	DQ1B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AD17	DQ6B	DQ1B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	W15	DQSn6B	DQSn1B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AF19	DQ6B	DQ1B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	V15	DQS6B	DQS1B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AE19			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AF22	DQ6B	DQ1B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AC17	DQ6B	DQ1B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AF21	DQ6B	DQ1B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AB17	DQ6B	DQ1B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	U17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AE21	DQ6B	DQ1B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	T17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AE20	DQ6B	DQ1B	B_DM_2	B_DM_2
4A	VREFB4AN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AD20			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AE15	DQ7B	DQ2B	B_DQ_24	B_DQ_24
4A	VREFB4AN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AC20	DQ7B	DQ2B	B_DQ_26	B_DQ_26
4A	VREFB4AN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AE16	DQ7B	DQ2B	B_DQ_25	B_DQ_25
4A	VREFB4AN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	W17	DQSn7B	DQ2B	B_DQS#_3	B_DQS#_3
4A	VREFB4AN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AD21	DQ7B	DQ2B	B_DQ_27	B_DQ_27
4A	VREFB4AN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	W16	DQS7B	DQ2B	B_DQS_3	B_DQS_3
4A	VREFB4AN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AD22			GND	GND

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AE23	DQ7B	DQ2B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	AF16	DQ7B	DQ2B	B_DQ_28	B_DQ_28
4A	VREFB4AN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AD23	DQ7B	DQ2B	B_DQ_30	B_DQ_30
4A	VREFB4AN0	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	AF17	DQ7B	DQ2B	B_DQ_29	B_DQ_29
4A	VREFB4AN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	U16			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AF23	DQ7B	DQ2B	B_DQ_31	B_DQ_31
4A	VREFB4AN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	U15			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AE24	DQ7B	DQ2B	B_DM_3	B_DM_3
4A	VREFB4AN0	IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AF24			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B82n	DIFFOUT_B82n	AA18	DQ8B	DQ2B	B_DQ_32	B_DQ_32
4A	VREFB4AN0	IO			DIFFIO_TX_B81p	DIFFOUT_B81p	AE25	DQ8B	DQ2B	B_DQ_34	B_DQ_34
4A	VREFB4AN0	IO			DIFFIO_RX_B82p	DIFFOUT_B82p	Y18	DQ8B	DQ2B	B_DQ_33	B_DQ_33
4A	VREFB4AN0	IO			DIFFIO_RX_B83n	DIFFOUT_B83n	V17	DQSn8B	DQSn2B	B_DQS#_4	B_DQS#_4
4A	VREFB4AN0	IO			DIFFIO_TX_B84n	DIFFOUT_B84n	AE26	DQ8B	DQ2B	B_DQ_35	B_DQ_35
4A	VREFB4AN0	IO			DIFFIO_RX_B83p	DIFFOUT_B83p	V18	DQS8B	DQS2B	B_DQS_4	B_DQS_4
4A	VREFB4AN0	IO			DIFFIO_TX_B84p	DIFFOUT_B84p	AD26			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B85n	DIFFOUT_B85n	AC19	DQ8B	DQ2B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B86n	DIFFOUT_B86n	Y19	DQ8B	DQ2B	B_DQ_36	B_DQ_36
4A	VREFB4AN0	IO			DIFFIO_TX_B85p	DIFFOUT_B85p	AB19	DQ8B	DQ2B	B_DQ_38	B_DQ_38
4A	VREFB4AN0	IO			DIFFIO_RX_B86p	DIFFOUT_B86p	Y20	DQ8B	DQ2B	B_DQ_37	B_DQ_37
4A	VREFB4AN0	IO			DIFFIO_RX_B87n	DIFFOUT_B87n	W18			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B88n	DIFFOUT_B88n	AA21	DQ8B	DQ2B	B_DQ_39	B_DQ_39
4A	VREFB4AN0	IO			DIFFIO_RX_B87p	DIFFOUT_B87p	V19			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B88p	DIFFOUT_B88p	AB22	DQ8B	DQ2B	B_DM_4	B_DM_4
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AC22	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	U19				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AC23	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	V20				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AA22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	W20	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AA23	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	W21	DQ1R			
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AC24				
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	V22	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AB24	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	U22	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	Y23	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	T19	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	Y24				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	U20	DQ1R			
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R33p	DIFFOUT_R33p	T21				
5B	VREFB5BN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	V23	DQ2R			
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	T22				
5B	VREFB5BN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	V24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	T23	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R36p	DIFFOUT_R36p	AA24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	T24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R36n	DIFFOUT_R36n	AB25	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	R23	DQS2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	AD25				
5B	VREFB5BN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	P23	DQSn2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	AC25	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	R24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	U24	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	R25	DQ2R			
5B	VREFB5BN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	V25				
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R41p	DIFFOUT_R41p	R20				
5B	VREFB5BN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	AB26	DQ3R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R41n	DIFFOUT_R41n	P20				
5B	VREFB5BN0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	AA26	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	T26	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	Y25	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	R26	DQ3R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	Y26	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	P21	DQS3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	W25				
5B	VREFB5BN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	P22	DQSn3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	W26	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	N25	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	U25	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	P26	DQ3R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	U26				
6A	VREFB6AN0	IO	CLK5p		DIFFIO_RX_R49p	DIFFOUT_R49p	N20				
6A	VREFB6AN0	IO			DIFFIO_TX_R50p	DIFFOUT_R50p	J25	DQ4R			
6A	VREFB6AN0	IO	CLK5n		DIFFIO_RX_R49n	DIFFOUT_R49n	M21				
6A	VREFB6AN0	IO			DIFFIO_TX_R50n	DIFFOUT_R50n	J26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R51p	DIFFOUT_R51p	N24	DQ4R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R52p	DIFFOUT_R52p	F26	DQ4R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
6A	VREFB6AN0	IO			DIFFIO_RX_R51n	DIFFOUT_R51n	M24	DQ4R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R52n	DIFFOUT_R52n	G26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R53p	DIFFOUT_R53p	N23	DQS4R			
6A	VREFB6AN0	IO			DIFFIO_TX_R54p	DIFFOUT_R54p	G25				
6A	VREFB6AN0	IO			DIFFIO_RX_R53n	DIFFOUT_R53n	M22	DQSn4R			
6A	VREFB6AN0	IO			DIFFIO_TX_R54n	DIFFOUT_R54n	H25	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R55p	DIFFOUT_R55p	M25	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_TX_R56p	DIFFOUT_R56p	D26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_RX_R55n	DIFFOUT_R55n	M26	DQ4R			
6A	VREFB6AN0	IO			DIFFIO_TX_R56n	DIFFOUT_R56n	E26				
6A	VREFB6AN0	IO	CLK4p,FPLL_TR_FBp		DIFFIO_RX_R57p	DIFFOUT_R57p	K25				
6A	VREFB6AN0	IO			DIFFIO_TX_R58p	DIFFOUT_R58p	E24	DQ5R			
6A	VREFB6AN0	IO	CLK4n,FPLL_TR_FBn		DIFFIO_RX_R57n	DIFFOUT_R57n	K26				
6A	VREFB6AN0	IO			DIFFIO_TX_R58n	DIFFOUT_R58n	E25	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R59p	DIFFOUT_R59p	K24	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R60p	DIFFOUT_R60p	F24	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R59n	DIFFOUT_R59n	K23	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R60n	DIFFOUT_R60n	G24	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R61p	DIFFOUT_R61p	L23	DQS5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R62p	DIFFOUT_R62p	H23				
6A	VREFB6AN0	IO			DIFFIO_RX_R61n	DIFFOUT_R61n	L24	DQSn5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R62n	DIFFOUT_R62n	H24	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R63p	DIFFOUT_R63p	H22	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R64p	DIFFOUT_R64p	F23	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_RX_R63n	DIFFOUT_R63n	J23	DQ5R			
6A	VREFB6AN0	IO			DIFFIO_TX_R64n	DIFFOUT_R64n	G22				
6A	VREFB6AN0	IO			DIFFIO_RX_R73p	DIFFOUT_R73p	L22				
6A	VREFB6AN0	IO			DIFFIO_TX_R74p	DIFFOUT_R74p	B25	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R73n	DIFFOUT_R73n	K21				
6A	VREFB6AN0	IO			DIFFIO_TX_R74n	DIFFOUT_R74n	B26	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R75p	DIFFOUT_R75p	H19	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R76p	DIFFOUT_R76p	D25	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R75n	DIFFOUT_R75n	H20	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R76n	DIFFOUT_R76n	C25	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R77p	DIFFOUT_R77p	J20	DQS6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R78p	DIFFOUT_R78p	D22				
6A	VREFB6AN0	IO			DIFFIO_RX_R77n	DIFFOUT_R77n	J21	DQSn6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R78n	DIFFOUT_R78n	E23	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R79p	DIFFOUT_R79p	G20	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R80p	DIFFOUT_R80p	E21	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R79n	DIFFOUT_R79n	F21	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R80n	DIFFOUT_R80n	F22				
7A		GND					D23				
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	H15			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	C23	DQ1T	DQ1T	T_DM_4	T_DM_4
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	J16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	C22	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	B24	DQ1T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	A23	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	A24	DQ1T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	A22	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	H18	DQS1T	DQS1T	T_DQS_4	T_DQS_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	B22			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	H17	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	A21	DQ1T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	D21	DQ1T	DQ1T	T_DQ_33	T_DQ_33
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	B21	DQ1T	DQ1T	T_DQ_34	T_DQ_34
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	D20	DQ1T	DQ1T	T_DQ_32	T_DQ_32
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	B20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	G16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	C20	DQ2T	DQ1T	T_DM_3	T_DM_3
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	G17			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	B19	DQ2T	DQ1T	T_DQ_31	T_DQ_31
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	E20	DQ2T	DQ1T	T_DQ_29	T_DQ_29
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	C19	DQ2T	DQ1T	T_DQ_30	T_DQ_30
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	E19	DQ2T	DQ1T	T_DQ_28	T_DQ_28
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	C18	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	J12	DQS2T	DQ1T	T_DQS_3	T_DQS_3
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	A19			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	J11	DQSn2T	DQ1T	T_DQS#_3	T_DQS#_3
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	A18	DQ2T	DQ1T	T_DQ_27	T_DQ_27
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	D18	DQ2T	DQ1T	T_DQ_25	T_DQ_25
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A17	DQ2T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	D17	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A16			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	H14			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C17	DQ3T	DQ2T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	H13			GND	GND

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	B17	DQ3T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	E18	DQ3T	DQ2T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	A14	DQ3T	DQ2T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	F18	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	B14	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	L12	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B15			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	K11	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C15	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	C14	DQ3T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	A8	DQ3T	DQ2T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	D15	DQ3T	DQ2T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	A9			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T33p	DIFFOUT_T33p	G15				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	C9	DQ4T	DQ2T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T33n	DIFFOUT_T33n	G14				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	B9	DQ4T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	E16	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	D10	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	D16	DQ4T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	C10	DQ4T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	N12	DQS4T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	B10			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	M12	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	A11	DQ4T	DQ2T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	F16	DQ4T	DQ2T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	E10	DQ4T	DQ2T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	E15	DQ4T	DQ2T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	E11			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T41p	DIFFOUT_T41p	H12				
7A	VREFB7AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	B12	DQ5T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T41n	DIFFOUT_T41n	G11				
7A	VREFB7AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	A13	DQ5T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	G12	DQ5T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	A12	DQ5T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	F12	DQ5T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	B11	DQ5T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	M11	DQS5T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	C13			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	L11	DQSn5T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	C12	DQ5T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	E13	DQ5T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	D11	DQ5T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	D13	DQ5T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T48n	DIFFOUT_T48n	D12				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T49p	DIFFOUT_T49p	N9				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	A5	DQ6T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T49n	DIFFOUT_T49n	M10				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	B6	DQ6T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	H8	DQ6T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	A7	DQ6T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	H9	DQ6T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	B7	DQ6T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	M9	DQS6T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	D6			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	L9	DQSn6T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	E6	DQ6T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	H10	DQ6T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	D7	DQ6T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	G10	DQ6T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	C7			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	L8				
8A	VREFB8AN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	F6	DQ7T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T57n	DIFFOUT_T57n	K9				
8A	VREFB8AN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	G6	DQ7T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	K8	DQ7T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	G7	DQ7T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	J8	DQ7T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	F7	DQ7T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T61p	K10	DQS7T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	H7			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T61n	J10	DQSn7T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	J7	DQ7T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	L7	DQ7T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	D8	DQ7T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	K6	DQ7T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	E9			GND	GND
9A		MSEL0		MSEL0			M7				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
9A		CONF_DONE		CONF_DONE			A6				
9A		MSEL1		MSEL1			L6				
9A		nSTATUS		nSTATUS			B5				
9A		nCE		nCE			D5				
9A		MSEL2		MSEL2			A2				
9A		MSEL3		MSEL3			K5				
9A		nCONFIG		nCONFIG			F5				
9A		MSEL4		MSEL4			J5				
9A		GND					H5				
		GND					E7				
		GND					G5				
		GND					C11				
		GND					D14				
		GND					E17				
		GND					F20				
		GND					G23				
		GND					L25				
		GND					N21				
		GND					P24				
		GND					P19				
		GND					T20				
		GND					U23				
		GND					Y22				
		GND					AA15				
		GND					AE17				
		GND					AD14				
		GND					M8				
		GND					A25				
		GND					D24				
		GND					H26				
		GND					V26				
		GND					AA25				
		GND					AC26				
		GND					AF25				
		GND					K22				
		GND					AD24				
		GND					C21				
		GND					L20				
		GND					K19				
		GND					M19				
		GND					W19				
		GND					AC21				
		GND					AF20				
		GND					B18				
		GND					L18				
		GND					K17				
		GND					J18				
		GND					N18				
		GND					M17				
		GND					R18				
		GND					P17				
		GND					AB18				
		GND					A15				
		GND					H16				
		GND					L16				
		GND					L14				
		GND					K15				
		GND					J14				
		GND					N16				
		GND					N14				
		GND					M15				
		GND					T15				
		GND					R16				
		GND					R14				
		GND					P15				
		GND					V16				
		GND					G13				
		GND					K13				
		GND					K12				
		GND					M13				
		GND					R12				
		GND					P13				
		GND					U13				
		GND					Y12				
		GND					F10				
		GND					L10				
		GND					J9				
		GND					N11				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					T10				
		GND					P9				
		GND					W9				
		GND					AC11				
		GND					AF10				
		GND					B8				
		GND					H6				
		GND					N6				
		GND					R7				
		GND					P7				
		GND					AB8				
		GND					AE7				
		GND					C5				
		GND					B4				
		GND					F4				
		GND					E5				
		GND					D4				
		GND					H4				
		GND					L4				
		GND					J4				
		GND					N4				
		GND					M5				
		GND					T5				
		GND					R4				
		GND					P5				
		GND					V5				
		GND					V4				
		GND					U4				
		GND					AA5				
		GND					Y4				
		GND					W5				
		GND					AC5				
		GND					AB4				
		GND					AF4				
		GND					AE5				
		GND					AD4				
		GND					C2				
		GND					C1				
		GND					B3				
		GND					B2				
		GND					F3				
		GND					E2				
		GND					E1				
		GND					D3				
		GND					H3				
		GND					G2				
		GND					G1				
		GND					L2				
		GND					L1				
		GND					K3				
		GND					J2				
		GND					J1				
		GND					N2				
		GND					N1				
		GND					M3				
		GND					T3				
		GND					R2				
		GND					R1				
		GND					P3				
		GND					V3				
		GND					U2				
		GND					U1				
		GND					AA2				
		GND					AA1				
		GND					Y3				
		GND					W2				
		GND					W1				
		GND					AC2				
		GND					AC1				
		GND					AB3				
		GND					AF3				
		GND					AF2				
		GND					AE2				
		GND					AE1				
		GND					AD3				
		VCC					J19				
		VCC					L19				
		VCC					K20				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		VCC					N19				
		VCC					M20				
		VCC					R19				
		VCC					L17				
		VCC					K18				
		VCC					J17				
		VCC					N17				
		VCC					M18				
		VCC					T18				
		VCC					R17				
		VCC					P18				
		VCC					L15				
		VCC					K16				
		VCC					K14				
		VCC					J15				
		VCC					N15				
		VCC					M16				
		VCC					M14				
		VCC					T16				
		VCC					T14				
		VCC					R15				
		VCC					P16				
		VCC					P14				
		VCC					L13				
		VCC					J13				
		VCC					N13				
		VCC					R13				
		DNU					A4				
		DNU					A3				
		DNU					AB7				
		DNU					AA12				
		DNU					C24				
		DNU					F14				
		VCCPGM					AA9				
		VCCPGM					W22				
		VCCPGM					F8				
		VCCBAT					E8				
		VCCIO3A					Y7				
		VCCIO3A					AC6				
		VCCIO3B					V11				
		VCCIO3B					AA10				
		VCCIO3B					AD9				
		VCCIO3B					U8				
		VCCIO4A					U18				
		VCCIO4A					AE22				
		VCCIO4A					AA20				
		VCCIO4A					AD19				
		VCCIO4A					Y17				
		VCCIO4A					W14				
		VCCIO4A					AC16				
		VCCIO4A					AF15				
		VCCIO4A					AB13				
		VCCIO4A					AE12				
		VCCIO5A					V21				
		VCCIO5A					AB23				
		VCCIO5B					N26				
		VCCIO5B					T25				
		VCCIO5B					W24				
		VCCIO5B					R22				
		VCCIO6A					C26				
		VCCIO6A					F25				
		VCCIO6A					J24				
		VCCIO6A					E22				
		VCCIO6A					M23				
		VCCIO6A					H21				
		VCCIO7A					B23				
		VCCIO7A					A20				
		VCCIO7A					D19				
		VCCIO7A					G18				
		VCCIO7A					C16				
		VCCIO7A					F15				
		VCCIO7A					B13				
		VCCIO7A					E12				
		VCCIO7A					A10				
		VCCIO7A					H11				
		VCCIO8A					C6				
		VCCIO8A					D9				
		VCCIO8A					G8				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F672	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		VCCIO8A					K7				
		VCCPD3A					AB9				
		VCCPD3B4A					AA17				
		VCCPD3B4A					AA11				
		VCCPD3B4A					AA19				
		VCCPD3B4A					AB21				
		VCCPD3B4A					AA13				
		VCCPD5A					U21				
		VCCPD5B					N22				
		VCCPD5B					R21				
		VCCPD6A					J22				
		VCCPD6A					L21				
		VCCPD7A8A					F19				
		VCCPD7A8A					F17				
		VCCPD7A8A					F13				
		VCCPD7A8A					F11				
		VCCPD7A8A					F9				
3A	VREFB3AN0	VREFB3AN0					AC7				
3B	VREFB3BN0	VREFB3BN0					AC12				
4A	VREFB4AN0	VREFB4AN0					AD15				
5A	VREFB5AN0	VREFB5AN0					W23				
5B	VREFB5BN0	VREFB5BN0					P25				
6A	VREFB6AN0	VREFB6AN0					L26				
7A	VREFB7AN0	VREFB7AN0					B16				
8A	VREFB8AN0	VREFB8AN0					C8				
		VCCH_GXBL					R3				
		VCCH_GXBL					T4				
		VCCH_GXBL					L3				
		VCCL_GXBL					J3				
		VCCL_GXBL					N3				
		VCCL_GXBL					U3				
		RREF_TL					B1				
		VCCA_FPLL					W7				
		VCCA_FPLL					J6				
		VCCA_FPLL					Y21				
		VCCA_FPLL					G21				
		VCC_AUX					G9				
		VCC_AUX					E14				
		VCC_AUX					G19				
		VCC_AUX					AB20				
		VCC_AUX					AB14				
		VCC_AUX					AA8				
		VCCE_GXBL					U5				
		VCCE_GXBL					K4				
		VCCE_GXBL					N5				
		VCCE_GXBL					M4				
		VCCE_GXBL					R5				
		VCCE_GXBL					P4				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
GXB_L3		REFCLK3Ln					L7				
GXB_L3		REFCLK3Lp					K8				
GXB_L3		GXB_TX_L11n					D3				
GXB_L3		GXB_TX_L11p					D4				
GXB_L3		GXB_RX_L11p,GXB_REFCLK_L11p					E2				
GXB_L3		GXB_RX_L11n,GXB_REFCLK_L11n					E1				
GXB_L3		GXB_TX_L10n					F3				
GXB_L3		GXB_TX_L10p					F4				
GXB_L3		GXB_RX_L10p,GXB_REFCLK_L10p					G2				
GXB_L3		GXB_RX_L10n,GXB_REFCLK_L10n					G1				
GXB_L3		GXB_TX_L9n					H3				
GXB_L3		GXB_TX_L9p					H4				
GXB_L3		GXB_RX_L9p,GXB_REFCLK_L9p					J2				
GXB_L3		GXB_RX_L9n,GXB_REFCLK_L9n					J1				
GXB_L2		GXB_TX_L8n					K3				
GXB_L2		GXB_TX_L8p					K4				
GXB_L2		GXB_RX_L8p,GXB_REFCLK_L8p					L2				
GXB_L2		GXB_RX_L8n,GXB_REFCLK_L8n					L1				
GXB_L2		GXB_TX_L7n					M3				
GXB_L2		GXB_TX_L7p					M4				
GXB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					N2				
GXB_L2		GXB_RX_L7n,GXB_REFCLK_L7n					N1				
GXB_L2		GXB_TX_L6n					P3				
GXB_L2		GXB_TX_L6p					P4				
GXB_L2		GXB_RX_L6p,GXB_REFCLK_L6p					R2				
GXB_L2		GXB_RX_L6n,GXB_REFCLK_L6n					R1				
GXB_L2		REFCLK2Lp					P8				
GXB_L2		REFCLK2Ln					N7				
GXB_L1		REFCLK1Ln					R7				
GXB_L1		REFCLK1Lp					R8				
GXB_L1		GXB_TX_L5n					T3				
GXB_L1		GXB_TX_L5p					T4				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					U2				
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					U1				
GXB_L1		GXB_TX_L4n					V3				
GXB_L1		GXB_TX_L4p					V4				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					W2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					W1				
GXB_L1		GXB_TX_L3n					Y3				
GXB_L1		GXB_TX_L3p					Y4				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					AA2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					AA1				
GXB_L0		GXB_TX_L2n					AB3				
GXB_L0		GXB_TX_L2p					AB4				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AC2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AC1				
GXB_L0		GXB_TX_L1n					AD3				
GXB_L0		GXB_TX_L1p					AD4				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AE2				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AE1				
GXB_L0		GXB_TX_L0n					AF3				
GXB_L0		GXB_TX_L0p					AF4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AG2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AG1				
GXB_L0		REFCLK0Lp					W8				
GXB_L0		REFCLK0Ln					W7				
3A		TDO		TDO			W9				
3A		nCSO		DATA4			AA7				
3A		TMS		TMS			V7				
3A		AS_DATA3		DATA3			AB7				
3A		TCK		TCK			AC7				
3A		AS_DATA2		DATA2			AE7				
3A		TDI		TDI			U7				
3A		AS_DATA1		DATA1			AE5				
3A		DCLK		DCLK			T7				
3A		AS_DATA0,ASDO		DATA0			AG5				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	U12	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AA10				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	U11	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	Y10	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	Y11	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AD9	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AA11	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AC9				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	R10	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	W10	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	T11	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	V9	DQ1B			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	V10				
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AF6	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	V11				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AF7	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AB9				
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AH6	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AA9	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	AG6	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	U8	DQSn2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AG8	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	T9	DQS2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AF8				
3A	VREFB3AN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AB8	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AH5	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AA8	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	AH4	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	U9				
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AH7	DQ2B			
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	T10				
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AG7	DQ2B			
3B	VREFB3BN0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	AF10				
3B	VREFB3BN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AD13	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AE10	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AD12	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	W12	DQSn3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AJ2	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	V12	DQS3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AJ1				
3B	VREFB3BN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AK3	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AE13	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AJ3	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AE12	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_RX_B31n	DIFFOUT_B31n	AB13				
3B	VREFB3BN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AJ5	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_RX_B31p	DIFFOUT_B31p	AB12				
3B	VREFB3BN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AJ4	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AK6			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AG12	DQ4B	DQ1B	B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AK5	DQ4B	DQ1B	B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AF13	DQ4B	DQ1B	B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AA13	DQSn4B	DQSn1B	B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AK7	DQ4B	DQ1B	B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	Y12	DQS4B	DQS1B	B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AJ7			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AK8	DQ4B	DQ1B	B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AG11	DQ4B	DQ1B	B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AJ8	DQ4B	DQ1B	B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AF11	DQ4B	DQ1B	B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	AC14				
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AG9	DQ4B	DQ1B	B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p	DIFFOUT_B39p	AB14				
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AF9	DQ4B	DQ1B	B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AJ9			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AJ10	DQ5B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AH9	DQ5B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AH10	DQ5B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AA14	DQSn5B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AK11	DQ5B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	Y13	DQS5B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AK10			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B45n	DIFFOUT_B45n	AH12	DQ5B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AG14	DQ5B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AH11	DQ5B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AG13	DQ5B		B_A_4	B_CA_4
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	AA15				
3B	VREFB3BN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AK12	DQ5B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	Y15				
3B	VREFB3BN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AJ12	DQ5B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B49n	DIFFOUT_B49n	AK13				
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AF15	DQ6B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AJ14	DQ6B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AE16	DQ6B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	AA16	DQSn6B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AH15	DQ6B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	Y16	DQS6B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AH14			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AK15	DQ6B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AE17	DQ6B		B_DQ_4	B_DQ_4

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AJ15	DQ6B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AD17	DQ6B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	AC15				
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AF14	DQ6B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B55p	DIFFOUT_B55p	AB16				
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AE15	DQ6B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AH17			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AK17	DQ7B	DQ2B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AG17	DQ7B	DQ2B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AK16	DQ7B	DQ2B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	Y18	DQSn7B	DQ2B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AJ18	DQ7B	DQ2B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	Y17	DQS7B	DQ2B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AJ17			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AK18	DQ7B	DQ2B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AG16	DQ7B	DQ2B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AJ19	DQ7B	DQ2B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AF16	DQ7B	DQ2B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	AB18				
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AH20	DQ7B	DQ2B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B63p	DIFFOUT_B63p	AB17				
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AH19	DQ7B	DQ2B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AK20			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AE18	DQ8B	DQ2B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AJ20	DQ8B	DQ2B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AD18	DQ8B	DQ2B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AA20	DQSn8B	DQS2B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AK22	DQ8B	DQ2B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	Y20	DQS8B	DQS2B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AK21			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AJ22	DQ8B	DQ2B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AF19	DQ8B	DQ2B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AH21	DQ8B	DQ2B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AF18	DQ8B	DQ2B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	AA19			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AK23	DQ8B	DQ2B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AA18			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AJ23	DQ8B	DQ2B	B_DM_2	B_DM_2
4A	VREFB4AN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AJ24			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AG19	DQ9B	DQ3B	B_DQ_24	B_DQ_24
4A	VREFB4AN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AH24	DQ9B	DQ3B	B_DQ_26	B_DQ_26
4A	VREFB4AN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AG18	DQ9B	DQ3B	B_DQ_25	B_DQ_25
4A	VREFB4AN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AC19	DQSn9B	DQ3B	B_DQS#_3	B_DQS#_3
4A	VREFB4AN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AK25	DQ9B	DQ3B	B_DQ_27	B_DQ_27
4A	VREFB4AN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	AB19	DQS9B	DQ3B	B_DQS_3	B_DQS_3
4A	VREFB4AN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AJ25			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AH25	DQ9B	DQ3B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	AE20	DQ9B	DQ3B	B_DQ_28	B_DQ_28
4A	VREFB4AN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AG24	DQ9B	DQ3B	B_DQ_30	B_DQ_30
4A	VREFB4AN0	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	AD19	DQ9B	DQ3B	B_DQ_29	B_DQ_29
4A	VREFB4AN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AB21			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AK26	DQ9B	DQ3B	B_DQ_31	B_DQ_31
4A	VREFB4AN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AA21			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AJ27	DQ9B	DQ3B	B_DM_3	B_DM_3
4A	VREFB4AN0	IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AK28			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B82n	DIFFOUT_B82n	AG21	DQ10B	DQ3B	B_DQ_32	B_DQ_32
4A	VREFB4AN0	IO			DIFFIO_TX_B81p	DIFFOUT_B81p	AK27	DQ10B	DQ3B	B_DQ_34	B_DQ_34
4A	VREFB4AN0	IO			DIFFIO_RX_B82p	DIFFOUT_B82p	AF20	DQ10B	DQ3B	B_DQ_33	B_DQ_33
4A	VREFB4AN0	IO			DIFFIO_RX_B83n	DIFFOUT_B83n	AD20	DQSn10B	DQSn3B	B_DQS#_4	B_DQS#_4
4A	VREFB4AN0	IO			DIFFIO_TX_B84n	DIFFOUT_B84n	AH26	DQ10B	DQ3B	B_DQ_35	B_DQ_35
4A	VREFB4AN0	IO			DIFFIO_RX_B83p	DIFFOUT_B83p	AC21	DQS10B	DQS3B	B_DQS_4	B_DQS_4
4A	VREFB4AN0	IO			DIFFIO_TX_B84p	DIFFOUT_B84p	AG26			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B85n	DIFFOUT_B85n	AF23	DQ10B	DQ3B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B86n	DIFFOUT_B86n	AG22	DQ10B	DQ3B	B_DQ_36	B_DQ_36
4A	VREFB4AN0	IO			DIFFIO_TX_B85p	DIFFOUT_B85p	AE22	DQ10B	DQ3B	B_DQ_38	B_DQ_38
4A	VREFB4AN0	IO			DIFFIO_RX_B86p	DIFFOUT_B86p	AF21	DQ10B	DQ3B	B_DQ_37	B_DQ_37
4A	VREFB4AN0	IO			DIFFIO_RX_B87n	DIFFOUT_B87n	AC22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B88n	DIFFOUT_B88n	AH22	DQ10B	DQ3B	B_DQ_39	B_DQ_39
4A	VREFB4AN0	IO			DIFFIO_RX_B87p	DIFFOUT_B87p	AB22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B88p	DIFFOUT_B88p	AG23	DQ10B	DQ3B	B_DM_4	B_DM_4
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AD23	DQ1R			
5A	VREFB5AN0	IO		INIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	W22				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AC24	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	Y21				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AD24	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	Y25	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AD25	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	Y26	DQ1R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AB26				
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	Y23	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AA26	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	W24	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	AC26	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	Y22	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	AC27				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	AA23	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	AA24				
5A	VREFB5AN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	AE23	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	AA25				
5A	VREFB5AN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	AF24	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	AE27	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_TX_R20p	DIFFOUT_R20p	AE25	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	AD27	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_TX_R20n	DIFFOUT_R20n	AE26	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	V21	DQS2R			
5A	VREFB5AN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	AF25				
5A	VREFB5AN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	V22	DQSn2R			
5A	VREFB5AN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	AF26	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	Y27	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	AH27	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	W27	DQ2R			
5A	VREFB5AN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	AG27				
5B	VREFB5BN0	IO			DIFFIO_RX_R25p	DIFFOUT_R25p	V24				
5B	VREFB5BN0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	AJ28	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R25n	DIFFOUT_R25n	V25				
5B	VREFB5BN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	AJ29	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	AA28	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R28p	DIFFOUT_R28p	AH29	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	Y28	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R28n	DIFFOUT_R28n	AG29	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	V26	DQS3R	DQS1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R30p	DIFFOUT_R30p	AJ30				
5B	VREFB5BN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	U26	DQSn3R	DQSn1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	AH30	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	AE30	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	AG28	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	AD30	DQ3R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	AF28				
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R33p	DIFFOUT_R33p	U21				
5B	VREFB5BN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	AF29	DQ4R	DQ1R		
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	U22				
5B	VREFB5BN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	AF30	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	V27	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R36p	DIFFOUT_R36p	AE28	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	W28	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R36n	DIFFOUT_R36n	AD28	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	U27	DQS4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	AD29				
5B	VREFB5BN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	U28	DQSn4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	AC29	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	AA29	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	AB27	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	AA30	DQ4R	DQ1R		
5B	VREFB5BN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	AB28				
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R41p	DIFFOUT_R41p	U23				
5B	VREFB5BN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	AB29	DQ5R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R41n	DIFFOUT_R41n	T24				
5B	VREFB5BN0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	AC30	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	T28	DQ5R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	Y30	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	T29	DQ5R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	W30	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	T25	DQS5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	V29				
5B	VREFB5BN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	R26	DQSn5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	W29	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	T30	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	U29	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	R30	DQ5R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	V30				
6A	VREFB6AN0	IO	CLK5p		DIFFIO_RX_R49p	DIFFOUT_R49p	T23				
6A	VREFB6AN0	IO			DIFFIO_TX_R50p	DIFFOUT_R50p	P28	DQ6R			
6A	VREFB6AN0	IO	CLK5n		DIFFIO_RX_R49n	DIFFOUT_R49n	R23				
6A	VREFB6AN0	IO			DIFFIO_TX_R50n	DIFFOUT_R50n	N29	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R51p	DIFFOUT_R51p	P29	DQ6R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R52p	DIFFOUT_R52p	M29	DQ6R			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
6A	VREFB6AN0	IO			DIFFIO_RX_R51n	DIFFOUT_R51n	P30	DQ6R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R52n	DIFFOUT_R52n	N30	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R53p	DIFFOUT_R53p	P25	DQS6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R54p	DIFFOUT_R54p	L28				
6A	VREFB6AN0	IO			DIFFIO_RX_R53n	DIFFOUT_R53n	R25	DQSn6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R54n	DIFFOUT_R54n	K28	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R55p	DIFFOUT_R55p	R27	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R56p	DIFFOUT_R56p	M27	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_RX_R55n	DIFFOUT_R55n	R28	DQ6R			
6A	VREFB6AN0	IO			DIFFIO_TX_R56n	DIFFOUT_R56n	M28				
6A	VREFB6AN0	IO	CLK4p,FPLL_TR_FBp		DIFFIO_RX_R57p	DIFFOUT_R57p	P22				
6A	VREFB6AN0	IO			DIFFIO_TX_R58p	DIFFOUT_R58p	K25	DQ7R	DQ2R		
6A	VREFB6AN0	IO	CLK4n,FPLL_TR_FBn		DIFFIO_RX_R57n	DIFFOUT_R57n	P23				
6A	VREFB6AN0	IO			DIFFIO_TX_R58n	DIFFOUT_R58n	K26	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R59p	DIFFOUT_R59p	N26	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R60p	DIFFOUT_R60p	L29	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R59n	DIFFOUT_R59n	N27	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R60n	DIFFOUT_R60n	L30	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R61p	DIFFOUT_R61p	N24	DQS7R	DQS2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R62p	DIFFOUT_R62p	K30				
6A	VREFB6AN0	IO			DIFFIO_RX_R61n	DIFFOUT_R61n	N25	DQSn7R	DQSn2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R62n	DIFFOUT_R62n	J30	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R63p	DIFFOUT_R63p	L25	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R64p	DIFFOUT_R64p	G27	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R63n	DIFFOUT_R63n	L26	DQ7R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R64n	DIFFOUT_R64n	G28				
6A	VREFB6AN0	IO			DIFFIO_RX_R65p	DIFFOUT_R65p	R21				
6A	VREFB6AN0	IO			DIFFIO_TX_R66p	DIFFOUT_R66p	J28	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R65n	DIFFOUT_R65n	R22				
6A	VREFB6AN0	IO			DIFFIO_TX_R66n	DIFFOUT_R66n	J29	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R67p	DIFFOUT_R67p	K27	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R68p	DIFFOUT_R68p	H29	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R67n	DIFFOUT_R67n	J27	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R68n	DIFFOUT_R68n	H30	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R69p	DIFFOUT_R69p	N22	DQS8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R70p	DIFFOUT_R70p	H27				
6A	VREFB6AN0	IO			DIFFIO_RX_R69n	DIFFOUT_R69n	M23	DQSn8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R70n	DIFFOUT_R70n	G26	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R71p	DIFFOUT_R71p	F25	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R72p	DIFFOUT_R72p	F30	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_RX_R71n	DIFFOUT_R71n	F26	DQ8R	DQ2R		
6A	VREFB6AN0	IO			DIFFIO_TX_R72n	DIFFOUT_R72n	E30				
6A	VREFB6AN0	IO			DIFFIO_RX_R73p	DIFFOUT_R73p	R20				
6A	VREFB6AN0	IO			DIFFIO_TX_R74p	DIFFOUT_R74p	G29	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R73n	DIFFOUT_R73n	T21				
6A	VREFB6AN0	IO			DIFFIO_TX_R74n	DIFFOUT_R74n	F29	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R75p	DIFFOUT_R75p	L23	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R76p	DIFFOUT_R76p	D30	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R75n	DIFFOUT_R75n	L24	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R76n	DIFFOUT_R76n	C30	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R77p	DIFFOUT_R77p	N21	DQS9R	DQS3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R78p	DIFFOUT_R78p	F28				
6A	VREFB6AN0	IO			DIFFIO_RX_R77n	DIFFOUT_R77n	M22	DQSn9R	DQSn3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R78n	DIFFOUT_R78n	E28	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R79p	DIFFOUT_R79p	K21	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R80p	DIFFOUT_R80p	C29	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R79n	DIFFOUT_R79n	K22	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R80n	DIFFOUT_R80n	B29				
6A	VREFB6AN0	IO			DIFFIO_RX_R81p	DIFFOUT_R81p	M21				
6A	VREFB6AN0	IO			DIFFIO_TX_R82p	DIFFOUT_R82p	B28	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R81n	DIFFOUT_R81n	L21				
6A	VREFB6AN0	IO			DIFFIO_TX_R82n	DIFFOUT_R82n	A29	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R83p	DIFFOUT_R83p	H25	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R84p	DIFFOUT_R84p	D28	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R83n	DIFFOUT_R83n	H26	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R84n	DIFFOUT_R84n	D29	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R85p	DIFFOUT_R85p	P20	DQS10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R86p	DIFFOUT_R86p	E27				
6A	VREFB6AN0	IO			DIFFIO_RX_R85n	DIFFOUT_R85n	N20	DQSn10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R86n	DIFFOUT_R86n	D27	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R87p	DIFFOUT_R87p	J22	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R88p	DIFFOUT_R88p	H24	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R87n	DIFFOUT_R87n	J23	DQ10R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R88n	DIFFOUT_R88n	J25				
7A		GND					G24				
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	H21			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	E26	DQ1T	DQ1T	T_DM_4	T_DM_4
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	G21			GND	GND

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	E25	DQ1T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	G22	DQ1T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C27	DQ1T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	G23	DQ1T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	C26	DQ1T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	L20	DQS1T	DQS1T	T_DQS_4	T_DQS_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	B27			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	L19	DQSn1T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	A28	DQ1T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	E22	DQ1T	DQ1T	T_DQ_33	T_DQ_33
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	B26	DQ1T	DQ1T	T_DQ_34	T_DQ_34
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	E21	DQ1T	DQ1T	T_DQ_32	T_DQ_32
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	A26			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	J20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	D25	DQ2T	DQ1T	T_DM_3	T_DM_3
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	H20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	C25	DQ2T	DQ1T	T_DQ_31	T_DQ_31
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	C21	DQ2T	DQ1T	T_DQ_29	T_DQ_29
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	D23	DQ2T	DQ1T	T_DQ_30	T_DQ_30
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	C20	DQ2T	DQ1T	T_DQ_28	T_DQ_28
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	C22	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	K20	DQS2T	DQ1T	T_DQS_3	T_DQS_3
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	E23			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	J19	DQSn2T	DQ1T	T_DQS#_3	T_DQS#_3
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	D22	DQ2T	DQ1T	T_DQ_27	T_DQ_27
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	D20	DQ2T	DQ1T	T_DQ_25	T_DQ_25
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	A25	DQ2T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	C19	DQ2T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	A24			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	F20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	C24	DQ3T	DQ2T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	E20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	B24	DQ3T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	F19	DQ3T	DQ2T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	B23	DQ3T	DQ2T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	E18	DQ3T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	A23	DQ3T	DQ2T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	L18	DQS3T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	B22			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	K18	DQSn3T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	B21	DQ3T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	D19	DQ3T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	A21	DQ3T	DQ2T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	D18	DQ3T	DQ2T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	A20			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T33p	DIFFOUT_T33p	H19				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	B19	DQ4T	DQ2T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T33n	DIFFOUT_T33n	J18				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A19	DQ4T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	G18	DQ4T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	B18	DQ4T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	F18	DQ4T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	A18	DQ4T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	K16	DQS4T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	D14			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	L16	DQSn4T	DQ2T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	C14	DQ4T	DQ2T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	C17	DQ4T	DQ2T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	A16	DQ4T	DQ2T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	B17	DQ4T	DQ2T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	A15			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T41p	DIFFOUT_T41p	H17				
7A	VREFB7AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	B14	DQ5T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T41n	DIFFOUT_T41n	G17				
7A	VREFB7AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	A14	DQ5T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	E17	DQ5T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	D12	DQ5T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	D17	DQ5T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	C12	DQ5T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	K17	DQS5T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	B13			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	J17	DQSn5T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	A13	DQ5T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	C16	DQ5T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	C11	DQ5T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	C15	DQ5T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T48n	DIFFOUT_T48n	B12				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T49p	DIFFOUT_T49p	L15				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	B11	DQ6T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T49n	DIFFOUT_T49n	K15				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	A11	DQ6T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	F16	DQ6T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	F9	DQ6T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	E16	DQ6T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	E10	DQ6T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	M9	DQS6T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	D9			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	M8	DQSn6T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	C10	DQ6T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	F15	DQ6T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	A10	DQ6T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	E15	DQ6T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	A9			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	L14				
8A	VREFB8AN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	C9	DQ7T		T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T57n	DIFFOUT_T57n	L13				
8A	VREFB8AN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	B8	DQ7T		T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	E12	DQ7T		T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	B7	DQ7T		T_A_10	
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	D13	DQ7T		T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	A8	DQ7T		T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T61p	J15	DQS7T		T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	B6			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T61n	H15	DQSn7T		T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	A6	DQ7T		T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	E11	DQ7T		T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	C7	DQ7T		T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	D10	DQ7T		T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	C6			GND	GND
8A	VREFB8AN0	IO			DIFFIO_RX_T65p	DIFFOUT_T65p	L10				
8A	VREFB8AN0	IO			DIFFIO_TX_T66p	DIFFOUT_T66p	F13	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_RX_T65n	DIFFOUT_T65n	L9				
8A	VREFB8AN0	IO			DIFFIO_TX_T66n	DIFFOUT_T66n	E13	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_RX_T67p	DIFFOUT_T67p	G14	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	A5	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_RX_T67n	DIFFOUT_T67n	F14	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	A4	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_RX_T69p	DIFFOUT_T69p	J14	DQS8T			
8A	VREFB8AN0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	J7				
8A	VREFB8AN0	IO			DIFFIO_RX_T69n	DIFFOUT_T69n	H14	DQSn8T			
8A	VREFB8AN0	IO			DIFFIO_TX_T70n	DIFFOUT_T70n	H7	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	L11	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	J9	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	K11	DQ8T			
8A	VREFB8AN0	IO			DIFFIO_TX_T72n	DIFFOUT_T72n	H9				
8A	VREFB8AN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	P12				
8A	VREFB8AN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	G9	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	N12				
8A	VREFB8AN0	IO			DIFFIO_TX_T74n	DIFFOUT_T74n	F8	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	H12	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	E8	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	G12	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T76n	DIFFOUT_T76n	D8	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	K13	DQS9T	DQS3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	A3				
8A	VREFB8AN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	J13	DQSn9T	DQSn3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	A2	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	P10	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	D7	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	N11	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	D6				
8A	VREFB8AN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	R12				
8A	VREFB8AN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	E7	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	R11				
8A	VREFB8AN0	IO			DIFFIO_TX_T82n	DIFFOUT_T82n	E6	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	K12	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	K10	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	J12	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T84n	DIFFOUT_T84n	J10	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T85p	DIFFOUT_T85p	N10	DQS10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T86p	DIFFOUT_T86p	G6				
8A	VREFB8AN0	IO			DIFFIO_RX_T85n	DIFFOUT_T85n	N9	DQSn10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T86n	DIFFOUT_T86n	F6	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T87p	DIFFOUT_T87p	M12	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T88p	DIFFOUT_T88p	G8	DQ10T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T87n	DIFFOUT_T87n	M11	DQ10T	DQ3T		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
8A	VREFB8AN0	IO			DIFFIO_TX_T88n	DIFFOUT_T88n	G7				
9A		MSEL0		MSEL0			T8				
9A		CONF_DONE		CONF_DONE			L8				
9A		MSEL1		MSEL1			P9				
9A		nSTATUS		nSTATUS			K7				
9A		nCE		nCE			H6				
9A		MSEL2		MSEL2			G5				
9A		MSEL3		MSEL3			P7				
9A		nCONFIG		nCONFIG			C5				
9A		MSEL4		MSEL4			M7				
9A		GND					E5				
		GND					F22				
		GND					AK2				
		GND					AK14				
		GND					AK24				
		GND					AK29				
		GND					AJ6				
		GND					AJ11				
		GND					AJ21				
		GND					AH1				
		GND					AH2				
		GND					AH3				
		GND					AH8				
		GND					AH18				
		GND					AH28				
		GND					AG3				
		GND					AG4				
		GND					AG15				
		GND					AG25				
		GND					AF1				
		GND					AF2				
		GND					AF5				
		GND					AF12				
		GND					AF22				
		GND					AE3				
		GND					AE4				
		GND					AE6				
		GND					AE9				
		GND					AE19				
		GND					AE29				
		GND					AD1				
		GND					AD2				
		GND					AD5				
		GND					AD7				
		GND					AD16				
		GND					AD26				
		GND					AC3				
		GND					AC4				
		GND					AC6				
		GND					AC13				
		GND					AC23				
		GND					AB1				
		GND					AB2				
		GND					AB5				
		GND					AB10				
		GND					AB20				
		GND					AB30				
		GND					AA3				
		GND					AA4				
		GND					AA6				
		GND					AA17				
		GND					AA27				
		GND					Y1				
		GND					Y2				
		GND					Y5				
		GND					Y7				
		GND					Y14				
		GND					Y24				
		GND					W3				
		GND					W4				
		GND					W6				
		GND					W11				
		GND					W13				
		GND					W15				
		GND					W17				
		GND					W19				
		GND					W21				
		GND					V1				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					V2				
		GND					V5				
		GND					V8				
		GND					V14				
		GND					V16				
		GND					V18				
		GND					V20				
		GND					V23				
		GND					V28				
		GND					U3				
		GND					U4				
		GND					U6				
		GND					U13				
		GND					U15				
		GND					U17				
		GND					U19				
		GND					U25				
		GND					T1				
		GND					T2				
		GND					T5				
		GND					T12				
		GND					T14				
		GND					T16				
		GND					T18				
		GND					T20				
		GND					T22				
		GND					R3				
		GND					R4				
		GND					R6				
		GND					R9				
		GND					R13				
		GND					R15				
		GND					R17				
		GND					R19				
		GND					R29				
		GND					P1				
		GND					P2				
		GND					P5				
		GND					P11				
		GND					P14				
		GND					P16				
		GND					P18				
		GND					P26				
		GND					N3				
		GND					N4				
		GND					N6				
		GND					N8				
		GND					N13				
		GND					N15				
		GND					N17				
		GND					N19				
		GND					N23				
		GND					M1				
		GND					M2				
		GND					M5				
		GND					M10				
		GND					M14				
		GND					M16				
		GND					M18				
		GND					M20				
		GND					M30				
		GND					L3				
		GND					L4				
		GND					L6				
		GND					L17				
		GND					L27				
		GND					K1				
		GND					K2				
		GND					K5				
		GND					K9				
		GND					K14				
		GND					K24				
		GND					J3				
		GND					J4				
		GND					J6				
		GND					J11				
		GND					J21				
		GND					H1				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					H2				
		GND					H5				
		GND					H8				
		GND					H11				
		GND					H18				
		GND					H28				
		GND					G3				
		GND					G4				
		GND					G15				
		GND					G25				
		GND					F1				
		GND					F2				
		GND					F5				
		GND					F12				
		GND					E3				
		GND					E4				
		GND					E9				
		GND					E19				
		GND					E29				
		GND					D1				
		GND					D2				
		GND					D5				
		GND					D16				
		GND					D26				
		GND					C2				
		GND					C3				
		GND					C4				
		GND					C13				
		GND					C23				
		GND					B1				
		GND					B2				
		GND					B10				
		GND					B20				
		GND					B30				
		GND					A12				
		GND					A17				
		GND					A27				
		VCC					M15				
		VCC					W14				
		VCC					W16				
		VCC					W18				
		VCC					W20				
		VCC					V13				
		VCC					V15				
		VCC					V17				
		VCC					V19				
		VCC					U14				
		VCC					U16				
		VCC					U18				
		VCC					U20				
		VCC					T13				
		VCC					T15				
		VCC					T17				
		VCC					T19				
		VCC					R14				
		VCC					R16				
		VCC					R18				
		VCC					P13				
		VCC					P15				
		VCC					P17				
		VCC					P19				
		VCC					N14				
		VCC					N16				
		VCC					N18				
		VCC					M13				
		VCC					M17				
		VCC					M19				
		DNU					B4				
		DNU					B3				
		DNU					AD8				
		DNU					AD14				
		DNU					F24				
		DNU					D15				
		VCCPGM					AC11				
		VCCPGM					AB24				
		VCCPGM					F10				
		VCCBAT					H10				
		VCCIO3A					U10				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		VCCIO3A					AD11				
		VCCIO3A					AC8				
		VCCIO3A					Y9				
		VCCIO3B					AA12				
		VCCIO3B					AK4				
		VCCIO3B					AK9				
		VCCIO3B					AH13				
		VCCIO3B					AG10				
		VCCIO3B					AE14				
		VCCIO4A					AK19				
		VCCIO4A					AJ16				
		VCCIO4A					AJ26				
		VCCIO4A					AH23				
		VCCIO4A					AG20				
		VCCIO4A					AF17				
		VCCIO4A					AD21				
		VCCIO4A					AC18				
		VCCIO4A					AB15				
		VCCIO4A					Y19				
		VCCIO5A					AF27				
		VCCIO5A					AE24				
		VCCIO5A					AB25				
		VCCIO5A					AA22				
		VCCIO5B					AG30				
		VCCIO5B					AC28				
		VCCIO5B					Y29				
		VCCIO5B					W26				
		VCCIO5B					U30				
		VCCIO5B					T27				
		VCCIO6A					R24				
		VCCIO6A					P21				
		VCCIO6A					N28				
		VCCIO6A					M25				
		VCCIO6A					L22				
		VCCIO6A					K29				
		VCCIO6A					J26				
		VCCIO6A					G30				
		VCCIO6A					F27				
		VCCIO6A					C28				
		VCCIO7A					K19				
		VCCIO7A					H23				
		VCCIO7A					G20				
		VCCIO7A					F17				
		VCCIO7A					E24				
		VCCIO7A					D21				
		VCCIO7A					C18				
		VCCIO7A					B15				
		VCCIO7A					B25				
		VCCIO7A					A22				
		VCCIO8A					A7				
		VCCIO8A					L12				
		VCCIO8A					J16				
		VCCIO8A					H13				
		VCCIO8A					G10				
		VCCIO8A					F7				
		VCCIO8A					E14				
		VCCIO8A					D11				
		VCCIO8A					C8				
		VCCIO8A					B5				
		VCCPD3A					AD10				
		VCCPD3A					AB11				
		VCCPD3B4A					AC20				
		VCCPD3B4A					AE11				
		VCCPD3B4A					AE21				
		VCCPD3B4A					AD15				
		VCCPD3B4A					AC12				
		VCCPD3B4A					AC17				
		VCCPD5A					W23				
		VCCPD5A					W25				
		VCCPD5B					U24				
		VCCPD5B					T26				
		VCCPD6A					P24				
		VCCPD6A					M24				
		VCCPD6A					K23				
		VCCPD7A8A					D24				
		VCCPD7A8A					G13				
		VCCPD7A8A					G16				
		VCCPD7A8A					G19				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F896	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		VCCPD7A8A					F11				
		VCCPD7A8A					F21				
		VCCPD7A8A					F23				
3A	VREFB3AN0	VREFB3AN0					AE8				
3B	VREFB3BN0	VREFB3BN0					AJ13				
4A	VREFB4AN0	VREFB4AN0					AH16				
5A	VREFB5AN0	VREFB5AN0					AC25				
5B	VREFB5BN0	VREFB5BN0					P27				
6A	VREFB6AN0	VREFB6AN0					M26				
7A	VREFB7AN0	VREFB7AN0					B16				
8A	VREFB8AN0	VREFB8AN0					B9				
		VCCH_GXBL					AB6				
		VCCH_GXBL					V6				
		VCCH_GXBL					P6				
		VCCH_GXBL					K6				
		VCCL_GXBL					AC5				
		VCCL_GXBL					W5				
		VCCL_GXBL					R5				
		VCCL_GXBL					L5				
		RREF_TL					C1				
		VCCA_FPLL					Y8				
		VCCA_FPLL					J8				
		VCCA_FPLL					AB23				
		VCCA_FPLL					J24				
		VCC_AUX					G11				
		VCC_AUX					AC10				
		VCC_AUX					AD22				
		VCC_AUX					AC16				
		VCC_AUX					H16				
		VCC_AUX					H22				
		VCCE_GXBL					AD6				
		VCCE_GXBL					AA5				
		VCCE_GXBL					Y6				
		VCCE_GXBL					U5				
		VCCE_GXBL					T6				
		VCCE_GXBL					N5				
		VCCE_GXBL					M6				
		VCCE_GXBL					J5				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
GXB_L3		REFCLK3Ln					P10				
GXB_L3		REFCLK3Lp					R11				
GXB_L3		GXB_TX_L11n					F3				
GXB_L3		GXB_TX_L11p					F4				
GXB_L3		GXB_RX_L11p,GXB_REFCLK_L11p					G2				
GXB_L3		GXB_RX_L11n,GXB_REFCLK_L11n					G1				
GXB_L3		GXB_TX_L10n					H3				
GXB_L3		GXB_TX_L10p					H4				
GXB_L3		GXB_RX_L10p,GXB_REFCLK_L10p					J2				
GXB_L3		GXB_RX_L10n,GXB_REFCLK_L10n					J1				
GXB_L3		GXB_TX_L9n					K3				
GXB_L3		GXB_TX_L9p					K4				
GXB_L3		GXB_RX_L9p,GXB_REFCLK_L9p					L2				
GXB_L3		GXB_RX_L9n,GXB_REFCLK_L9n					L1				
GXB_L2		GXB_TX_L8n					M3				
GXB_L2		GXB_TX_L8p					M4				
GXB_L2		GXB_RX_L8p,GXB_REFCLK_L8p					N2				
GXB_L2		GXB_RX_L8n,GXB_REFCLK_L8n					N1				
GXB_L2		GXB_TX_L7n					P3				
GXB_L2		GXB_TX_L7p					P4				
GXB_L2		GXB_RX_L7p,GXB_REFCLK_L7p					R2				
GXB_L2		GXB_RX_L7n,GXB_REFCLK_L7n					R1				
GXB_L2		GXB_TX_L6n					T3				
GXB_L2		GXB_TX_L6p					T4				
GXB_L2		GXB_RX_L6p,GXB_REFCLK_L6p					U2				
GXB_L2		GXB_RX_L6n,GXB_REFCLK_L6n					U1				
GXB_L2		REFCLK2Lp					U11				
GXB_L2		REFCLK2Ln					T10				
GXB_L1		REFCLK1Ln					V10				
GXB_L1		REFCLK1Lp					W11				
GXB_L1		GXB_TX_L5n					V3				
GXB_L1		GXB_TX_L5p					V4				
GXB_L1		GXB_RX_L5p,GXB_REFCLK_L5p					W2				
GXB_L1		GXB_RX_L5n,GXB_REFCLK_L5n					W1				
GXB_L1		GXB_TX_L4n					Y3				
GXB_L1		GXB_TX_L4p					Y4				
GXB_L1		GXB_RX_L4p,GXB_REFCLK_L4p					AA2				
GXB_L1		GXB_RX_L4n,GXB_REFCLK_L4n					AA1				
GXB_L1		GXB_TX_L3n					AB3				
GXB_L1		GXB_TX_L3p					AB4				
GXB_L1		GXB_RX_L3p,GXB_REFCLK_L3p					AC2				
GXB_L1		GXB_RX_L3n,GXB_REFCLK_L3n					AC1				
GXB_L0		GXB_TX_L2n					AD3				
GXB_L0		GXB_TX_L2p					AD4				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AE2				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AE1				
GXB_L0		GXB_TX_L1n					AF3				
GXB_L0		GXB_TX_L1p					AF4				
GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p					AG2				
GXB_L0		GXB_RX_L1n,GXB_REFCLK_L1n					AG1				
GXB_L0		GXB_TX_L0n					AH3				
GXB_L0		GXB_TX_L0p					AH4				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AJ2				
GXB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AJ1				
GXB_L0		REFCLK0Lp					AA11				
GXB_L0		REFCLK0Ln					AB10				
3A		TDO		TDO			AF11				
3A		nCSO		DATA4			AG10				
3A		TMS		TMS			AG11				
3A		AS_DATA3		DATA3			AJ6				
3A		TCK		TCK			AK5				
3A		AS_DATA2		DATA2			AH8				
3A		TDI		TDI			AE10				
3A		AS_DATA1		DATA1			AJ7				
3A		DCLK		DCLK			AF10				
3A		AS_DATA0,ASDO		DATA0			AH9				
3A	VREFB3AN0	IO		DATA6	DIFFIO_RX_B1n	DIFFOUT_B1n	AD11	DQ1B			
3A	VREFB3AN0	IO		DATA5	DIFFIO_TX_B2n	DIFFOUT_B2n	AM4				
3A	VREFB3AN0	IO		DATA8	DIFFIO_RX_B1p	DIFFOUT_B1p	AD12	DQ1B			
3A	VREFB3AN0	IO		DATA7	DIFFIO_TX_B2p	DIFFOUT_B2p	AM5	DQ1B			
3A	VREFB3AN0	IO		DATA10	DIFFIO_RX_B3n	DIFFOUT_B3n	AJ11	DQSn1B			
3A	VREFB3AN0	IO		DATA9	DIFFIO_TX_B4n	DIFFOUT_B4n	AL7	DQ1B			
3A	VREFB3AN0	IO		DATA12	DIFFIO_RX_B3p	DIFFOUT_B3p	AH12	DQS1B			
3A	VREFB3AN0	IO		DATA11	DIFFIO_TX_B4p	DIFFOUT_B4p	AK7				
3A	VREFB3AN0	IO		DATA14	DIFFIO_RX_B5n	DIFFOUT_B5n	AG13	DQ1B			
3A	VREFB3AN0	IO		DATA13	DIFFIO_TX_B6n	DIFFOUT_B6n	AL8	DQ1B			
3A	VREFB3AN0	IO		CLKUSR	DIFFIO_RX_B5p	DIFFOUT_B5p	AF13	DQ1B			
3A	VREFB3AN0	IO		DATA15	DIFFIO_TX_B6p	DIFFOUT_B6p	AK8	DQ1B			
3A	VREFB3AN0	IO		PR_DONE	DIFFIO_RX_B7n	DIFFOUT_B7n	AC12				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3A	VREFB3AN0	IO		PR_READY	DIFFIO_TX_B8n	DIFFOUT_B8n	AK9	DQ1B			
3A	VREFB3AN0	IO		PR_ERROR	DIFFIO_RX_B7p	DIFFOUT_B7p	AC13				
3A	VREFB3AN0	IO			DIFFIO_TX_B8p	DIFFOUT_B8p	AJ9	DQ1B			
3A	VREFB3AN0	IO			DIFFIO_TX_B9n	DIFFOUT_B9n	AM6				
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B10n	AK10	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B9p	DIFFOUT_B9p	AL6	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B10p	AJ10	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B11n	AB13	DQSn2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B12n	DIFFOUT_B12n	AN4	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B11p	AB14	DQS2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AN5				
3A	VREFB3AN0	IO			DIFFIO_TX_B13n	DIFFOUT_B13n	AP5	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B14n	DIFFOUT_B14n	AJ12	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B13p	DIFFOUT_B13p	AP6	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B14p	DIFFOUT_B14p	AH13	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B15n	DIFFOUT_B15n	AE14				
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AP7	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B15p	DIFFOUT_B15p	AD14				
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AN7	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B17n	DIFFOUT_B17n	AN8				
3A	VREFB3AN0	IO			DIFFIO_RX_B18n	DIFFOUT_B18n	AH14	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B17p	DIFFOUT_B17p	AM8	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B18p	DIFFOUT_B18p	AG14	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AC14	DQSn3B	DQSn1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B20n	DIFFOUT_B20n	AN9	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AD15	DQS3B	DQS1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B20p	DIFFOUT_B20p	AM9				
3A	VREFB3AN0	IO			DIFFIO_TX_B21n	DIFFOUT_B21n	AM10	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B22n	DIFFOUT_B22n	AK14	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B21p	DIFFOUT_B21p	AL10	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B22p	DIFFOUT_B22p	AJ14	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B23n	DIFFOUT_B23n	AB15				
3A	VREFB3AN0	IO			DIFFIO_TX_B24n	DIFFOUT_B24n	AK12	DQ3B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_RX_B23p	DIFFOUT_B23p	AA15				
3A	VREFB3AN0	IO			DIFFIO_TX_B24p	DIFFOUT_B24p	AK13	DQ3B	DQ1B		
3B	VREFB3BN0	IO			DIFFIO_TX_B25n	DIFFOUT_B25n	AM11				
3B	VREFB3BN0	IO			DIFFIO_RX_B26n	DIFFOUT_B26n	AM15	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_TX_B25p	DIFFOUT_B25p	AL11	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B26p	DIFFOUT_B26p	AL15	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B27n	DIFFOUT_B27n	AG15	DQSn4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_TX_B28n	DIFFOUT_B28n	AP9	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B27p	DIFFOUT_B27p	AG16	DQS4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_TX_B28p	DIFFOUT_B28p	AP10				
3B	VREFB3BN0	IO			DIFFIO_TX_B29n	DIFFOUT_B29n	AP11	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B30n	DIFFOUT_B30n	AK15	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_TX_B29p	DIFFOUT_B29p	AN11	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B30p	DIFFOUT_B30p	AJ15	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B31n	DIFFOUT_B31n	AD16				
3B	VREFB3BN0	IO			DIFFIO_TX_B32n	DIFFOUT_B32n	AL13	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_RX_B31p	DIFFOUT_B31p	AC16				
3B	VREFB3BN0	IO			DIFFIO_TX_B32p	DIFFOUT_B32p	AL12	DQ4B	DQ2B		
3B	VREFB3BN0	IO			DIFFIO_TX_B33n	DIFFOUT_B33n	AP12			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B34n	DIFFOUT_B34n	AN14	DQ5B	DQ2B	B_A_15	
3B	VREFB3BN0	IO			DIFFIO_TX_B33p	DIFFOUT_B33p	AN12	DQ5B	DQ2B	B_WE#	
3B	VREFB3BN0	IO			DIFFIO_RX_B34p	DIFFOUT_B34p	AM14	DQ5B	DQ2B	B_A_14	
3B	VREFB3BN0	IO			DIFFIO_RX_B35n	DIFFOUT_B35n	AB16	DQSn5B	DQSn2B	B_CS#_1	B_CS#_1
3B	VREFB3BN0	IO			DIFFIO_TX_B36n	DIFFOUT_B36n	AN13	DQ5B	DQ2B	B_A_13	
3B	VREFB3BN0	IO			DIFFIO_RX_B35p	DIFFOUT_B35p	AA16	DQS5B	DQS2B	B_CS#_0	B_CS#_0
3B	VREFB3BN0	IO			DIFFIO_TX_B36p	DIFFOUT_B36p	AM13			B_A_12	
3B	VREFB3BN0	IO			DIFFIO_TX_B37n	DIFFOUT_B37n	AM16	DQ5B	DQ2B	B_A_11	
3B	VREFB3BN0	IO			DIFFIO_RX_B38n	DIFFOUT_B38n	AJ16	DQ5B	DQ2B	B_A_9	B_CA_9
3B	VREFB3BN0	IO			DIFFIO_TX_B37p	DIFFOUT_B37p	AL16	DQ5B	DQ2B	B_A_10	
3B	VREFB3BN0	IO			DIFFIO_RX_B38p	DIFFOUT_B38p	AH16	DQ5B	DQ2B	B_A_8	B_CA_8
3B	VREFB3BN0	IO	CLK0n,FPLL_BL_FBn		DIFFIO_RX_B39n	DIFFOUT_B39n	AC17				
3B	VREFB3BN0	IO			DIFFIO_TX_B40n	DIFFOUT_B40n	AP14	DQ5B	DQ2B	B_RAS#	
3B	VREFB3BN0	IO	CLK0p,FPLL_BL_FBp		DIFFIO_RX_B39p	DIFFOUT_B39p	AD17				
3B	VREFB3BN0	IO			DIFFIO_TX_B40p	DIFFOUT_B40p	AP15	DQ5B	DQ2B	B_CAS#	
3B	VREFB3BN0	IO			DIFFIO_TX_B41n	DIFFOUT_B41n	AP16			GND	GND
3B	VREFB3BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B42n	AP17	DQ6B		B_BA_2	
3B	VREFB3BN0	IO			DIFFIO_TX_B41p	DIFFOUT_B41p	AN16	DQ6B		B_BA_0	
3B	VREFB3BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B42p	AN17	DQ6B		B_BA_1	
3B	VREFB3BN0	IO			DIFFIO_RX_B43n	DIFFOUT_B43n	AA17	DQSn6B		B_CK#	B_CK#
3B	VREFB3BN0	IO			DIFFIO_TX_B44n	DIFFOUT_B44n	AL17	DQ6B		B_A_7	B_CA_7
3B	VREFB3BN0	IO			DIFFIO_RX_B43p	DIFFOUT_B43p	AA18	DQS6B		B_CK	B_CK
3B	VREFB3BN0	IO			DIFFIO_TX_B44p	DIFFOUT_B44p	AK17			B_A_6	B_CA_6
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT1,FPLL_BL_CLKOUTn		DIFFIO_TX_B45n	DIFFOUT_B45n	AN18	DQ6B		B_A_3	B_CA_3
3B	VREFB3BN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AJ17	DQ6B		B_A_5	B_CA_5
3B	VREFB3BN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB		DIFFIO_TX_B45p	DIFFOUT_B45p	AM18	DQ6B		B_A_2	B_CA_2
3B	VREFB3BN0	IO			DIFFIO_RX_B46p	DIFFOUT_B46p	AH17	DQ6B		B_A_4	B_CA_4

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
3B	VREFB3BN0	IO	CLK1n		DIFFIO_RX_B47n	DIFFOUT_B47n	AB18				
3B	VREFB3BN0	IO			DIFFIO_TX_B48n	DIFFOUT_B48n	AL18	DQ6B		B_A_1	B_CA_1
3B	VREFB3BN0	IO	CLK1p		DIFFIO_RX_B47p	DIFFOUT_B47p	AC18				
3B	VREFB3BN0	IO			DIFFIO_TX_B48p	DIFFOUT_B48p	AK18	DQ6B		B_A_0	B_CA_0
4A	VREFB4AN0	IO	RZQ_0		DIFFIO_TX_B49n	DIFFOUT_B49n	AP19				
4A	VREFB4AN0	IO			DIFFIO_RX_B50n	DIFFOUT_B50n	AN19	DQ7B		B_DQ_0	B_DQ_0
4A	VREFB4AN0	IO			DIFFIO_TX_B49p	DIFFOUT_B49p	AP20	DQ7B		B_DQ_2	B_DQ_2
4A	VREFB4AN0	IO			DIFFIO_RX_B50p	DIFFOUT_B50p	AM19	DQ7B		B_DQ_1	B_DQ_1
4A	VREFB4AN0	IO			DIFFIO_RX_B51n	DIFFOUT_B51n	AC19	DQSn7B		B_DQS#_0	B_DQS#_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52n	DIFFOUT_B52n	AP21	DQ7B		B_DQ_3	B_DQ_3
4A	VREFB4AN0	IO			DIFFIO_RX_B51p	DIFFOUT_B51p	AB19	DQS7B		B_DQS_0	B_DQS_0
4A	VREFB4AN0	IO			DIFFIO_TX_B52p	DIFFOUT_B52p	AN21			B_ODT_0	B_ODT_0
4A	VREFB4AN0	IO			DIFFIO_TX_B53n	DIFFOUT_B53n	AK19	DQ7B		B_ODT_1	B_ODT_1
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B54n	AH19	DQ7B		B_DQ_4	B_DQ_4
4A	VREFB4AN0	IO			DIFFIO_TX_B53p	DIFFOUT_B53p	AJ19	DQ7B		B_DQ_6	B_DQ_6
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B54p	AG19	DQ7B		B_DQ_5	B_DQ_5
4A	VREFB4AN0	IO	CLK2n		DIFFIO_RX_B55n	DIFFOUT_B55n	AG18				
4A	VREFB4AN0	IO			DIFFIO_TX_B56n	DIFFOUT_B56n	AM21	DQ7B		B_DQ_7	B_DQ_7
4A	VREFB4AN0	IO	CLK2p		DIFFIO_RX_B55p	DIFFOUT_B55p	AF18				
4A	VREFB4AN0	IO			DIFFIO_TX_B56p	DIFFOUT_B56p	AL21	DQ7B		B_DM_0	B_DM_0
4A	VREFB4AN0	IO			DIFFIO_TX_B57n	DIFFOUT_B57n	AP22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B58n	AM20	DQ8B	DQ3B	B_DQ_8	B_DQ_8
4A	VREFB4AN0	IO			DIFFIO_TX_B57p	DIFFOUT_B57p	AN22	DQ8B	DQ3B	B_DQ_10	B_DQ_10
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B58p	AL20	DQ8B	DQ3B	B_DQ_9	B_DQ_9
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B59n	AE19	DQSn8B	DQ3B	B_DQS#_1	B_DQS#_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60n	DIFFOUT_B60n	AN23	DQ8B	DQ3B	B_DQ_11	B_DQ_11
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B59p	AD19	DQS8B	DQ3B	B_DQS_1	B_DQS_1
4A	VREFB4AN0	IO			DIFFIO_TX_B60p	DIFFOUT_B60p	AM23			B_CKE_1	B_CKE_1
4A	VREFB4AN0	IO			DIFFIO_TX_B61n	DIFFOUT_B61n	AP26	DQ8B	DQ3B	B_CKE_0	B_CKE_0
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B62n	AP24	DQ8B	DQ3B	B_DQ_12	B_DQ_12
4A	VREFB4AN0	IO			DIFFIO_TX_B61p	DIFFOUT_B61p	AN26	DQ8B	DQ3B	B_DQ_14	B_DQ_14
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B62p	AP25	DQ8B	DQ3B	B_DQ_13	B_DQ_13
4A	VREFB4AN0	IO	CLK3n		DIFFIO_RX_B63n	DIFFOUT_B63n	AE20				
4A	VREFB4AN0	IO			DIFFIO_TX_B64n	DIFFOUT_B64n	AN24	DQ8B	DQ3B	B_DQ_15	B_DQ_15
4A	VREFB4AN0	IO	CLK3p		DIFFIO_RX_B63p	DIFFOUT_B63p	AD20				
4A	VREFB4AN0	IO			DIFFIO_TX_B64p	DIFFOUT_B64p	AM24	DQ8B	DQ3B	B_DM_1	B_DM_1
4A	VREFB4AN0	IO			DIFFIO_TX_B65n	DIFFOUT_B65n	AL22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B66n	DIFFOUT_B66n	AP27	DQ9B	DQ3B	B_DQ_16	B_DQ_16
4A	VREFB4AN0	IO			DIFFIO_TX_B65p	DIFFOUT_B65p	AK22	DQ9B	DQ3B	B_DQ_18	B_DQ_18
4A	VREFB4AN0	IO			DIFFIO_RX_B66p	DIFFOUT_B66p	AN27	DQ9B	DQ3B	B_DQ_17	B_DQ_17
4A	VREFB4AN0	IO			DIFFIO_RX_B67n	DIFFOUT_B67n	AK20	DQSn9B	DQSn3B	B_DQS#_2	B_DQS#_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68n	DIFFOUT_B68n	AJ21	DQ9B	DQ3B	B_DQ_19	B_DQ_19
4A	VREFB4AN0	IO			DIFFIO_RX_B67p	DIFFOUT_B67p	AJ20	DQS9B	DQS3B	B_DQS_2	B_DQS_2
4A	VREFB4AN0	IO			DIFFIO_TX_B68p	DIFFOUT_B68p	AJ22			B_RESET#	B_RESET#
4A	VREFB4AN0	IO			DIFFIO_TX_B69n	DIFFOUT_B69n	AP29	DQ9B	DQ3B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B70n	DIFFOUT_B70n	AH21	DQ9B	DQ3B	B_DQ_20	B_DQ_20
4A	VREFB4AN0	IO			DIFFIO_TX_B69p	DIFFOUT_B69p	AP30	DQ9B	DQ3B	B_DQ_22	B_DQ_22
4A	VREFB4AN0	IO			DIFFIO_RX_B70p	DIFFOUT_B70p	AH22	DQ9B	DQ3B	B_DQ_21	B_DQ_21
4A	VREFB4AN0	IO			DIFFIO_RX_B71n	DIFFOUT_B71n	AB20			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AN28	DQ9B	DQ3B	B_DQ_23	B_DQ_23
4A	VREFB4AN0	IO			DIFFIO_RX_B71p	DIFFOUT_B71p	AB21			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AM28	DQ9B	DQ3B	B_DM_2	B_DM_2
4A	VREFB4AN0	IO			DIFFIO_TX_B73n	DIFFOUT_B73n	AM25			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B74n	DIFFOUT_B74n	AL23	DQ10B	DQ4B	B_DQ_24	B_DQ_24
4A	VREFB4AN0	IO			DIFFIO_TX_B73p	DIFFOUT_B73p	AL25	DQ10B	DQ4B	B_DQ_26	B_DQ_26
4A	VREFB4AN0	IO			DIFFIO_RX_B74p	DIFFOUT_B74p	AK23	DQ10B	DQ4B	B_DQ_25	B_DQ_25
4A	VREFB4AN0	IO			DIFFIO_RX_B75n	DIFFOUT_B75n	AA20	DQSn10B	DQ4B	B_DQS#_3	B_DQS#_3
4A	VREFB4AN0	IO			DIFFIO_TX_B76n	DIFFOUT_B76n	AM26	DQ10B	DQ4B	B_DQ_27	B_DQ_27
4A	VREFB4AN0	IO			DIFFIO_RX_B75p	DIFFOUT_B75p	Y20	DQS10B	DQ4B	B_DQS_3	B_DQS_3
4A	VREFB4AN0	IO			DIFFIO_TX_B76p	DIFFOUT_B76p	AL26			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AP31	DQ10B	DQ4B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B78n	DIFFOUT_B78n	AK24	DQ10B	DQ4B	B_DQ_28	B_DQ_28
4A	VREFB4AN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AN31	DQ10B	DQ4B	B_DQ_30	B_DQ_30
4A	VREFB4AN0	IO			DIFFIO_RX_B78p	DIFFOUT_B78p	AJ24	DQ10B	DQ4B	B_DQ_29	B_DQ_29
4A	VREFB4AN0	IO			DIFFIO_RX_B79n	DIFFOUT_B79n	AG21			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B80n	DIFFOUT_B80n	AL28	DQ10B	DQ4B	B_DQ_31	B_DQ_31
4A	VREFB4AN0	IO			DIFFIO_RX_B79p	DIFFOUT_B79p	AF22			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B80p	DIFFOUT_B80p	AL27	DQ10B	DQ4B	B_DM_3	B_DM_3
4A	VREFB4AN0	IO			DIFFIO_TX_B81n	DIFFOUT_B81n	AP32			GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B82n	DIFFOUT_B82n	AH23	DQ11B	DQ4B	B_DQ_32	B_DQ_32
4A	VREFB4AN0	IO			DIFFIO_TX_B81p	DIFFOUT_B81p	AN32	DQ11B	DQ4B	B_DQ_34	B_DQ_34
4A	VREFB4AN0	IO			DIFFIO_RX_B82p	DIFFOUT_B82p	AG23	DQ11B	DQ4B	B_DQ_33	B_DQ_33
4A	VREFB4AN0	IO			DIFFIO_RX_B83n	DIFFOUT_B83n	AD21	DQSn11B	DQSn4B	B_DQS#_4	B_DQS#_4
4A	VREFB4AN0	IO			DIFFIO_TX_B84n	DIFFOUT_B84n	AN29	DQ11B	DQ4B	B_DQ_35	B_DQ_35
4A	VREFB4AN0	IO			DIFFIO_RX_B83p	DIFFOUT_B83p	AC21	DQS11B	DQS4B	B_DQS_4	B_DQS_4
4A	VREFB4AN0	IO			DIFFIO_TX_B84p	DIFFOUT_B84p	AM29			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B85n	DIFFOUT_B85n	AK27	DQ11B	DQ4B	GND	GND
4A	VREFB4AN0	IO			DIFFIO_RX_B86n	DIFFOUT_B86n	AK25	DQ11B	DQ4B	B_DQ_36	B_DQ_36
4A	VREFB4AN0	IO			DIFFIO_TX_B85p	DIFFOUT_B85p	AK28	DQ11B	DQ4B	B_DQ_38	B_DQ_38

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
4A	VREFB4AN0	IO			DIFFIO_RX_B86p	DIFFOUT_B86p	AJ25	DQ11B	DQ4B	B_DQ_37	B_DQ_37
4A	VREFB4AN0	IO			DIFFIO_RX_B87n	DIFFOUT_B87n	AF23			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B88n	DIFFOUT_B88n	AM30	DQ11B	DQ4B	B_DQ_39	B_DQ_39
4A	VREFB4AN0	IO			DIFFIO_RX_B87p	DIFFOUT_B87p	AE23			GND	GND
4A	VREFB4AN0	IO			DIFFIO_TX_B88p	DIFFOUT_B88p	AL30	DQ11B	DQ4B	B_DM_4	B_DM_4
4A	VREFB4AN0	IO			DIFFIO_TX_B89n	DIFFOUT_B89n	AK29				
4A	VREFB4AN0	IO			DIFFIO_RX_B90n	DIFFOUT_B90n	AH24	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_TX_B89p	DIFFOUT_B89p	AJ29	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_RX_B90p	DIFFOUT_B90p	AG24	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_RX_B91n	DIFFOUT_B91n	AD22	DQSn12B			
4A	VREFB4AN0	IO			DIFFIO_TX_B92n	DIFFOUT_B92n	AM31	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_RX_B91p	DIFFOUT_B91p	AC22	DQS12B			
4A	VREFB4AN0	IO			DIFFIO_TX_B92p	DIFFOUT_B92p	AL31				
4A	VREFB4AN0	IO			DIFFIO_TX_B93n	DIFFOUT_B93n	AJ26	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_RX_B94n	DIFFOUT_B94n	AG26	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_TX_B93p	DIFFOUT_B93p	AH26	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AG25	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_RX_B95n	DIFFOUT_B95n	AE25				
4A	VREFB4AN0	IO			DIFFIO_TX_B96n	DIFFOUT_B96n	AJ27	DQ12B			
4A	VREFB4AN0	IO			DIFFIO_RX_B95p	DIFFOUT_B95p	AF25				
4A	VREFB4AN0	IO			DIFFIO_TX_B96p	DIFFOUT_B96p	AH27	DQ12B			
5A	VREFB5AN0	IO	RZQ_1		DIFFIO_TX_R1p	DIFFOUT_R1p	AD24	DQ1R			
5A	VREFB5AN0	IO		nINIT_DONE	DIFFIO_RX_R2p	DIFFOUT_R2p	AC23				
5A	VREFB5AN0	IO		PR_REQUEST	DIFFIO_TX_R1n	DIFFOUT_R1n	AD25	DQ1R			
5A	VREFB5AN0	IO		CRC_ERROR	DIFFIO_RX_R2n	DIFFOUT_R2n	AC24				
5A	VREFB5AN0	IO		nCEO	DIFFIO_TX_R3p	DIFFOUT_R3p	AC27	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R4p	AB24	DQ1R			
5A	VREFB5AN0	IO		CvP_CONFDONE	DIFFIO_TX_R3n	DIFFOUT_R3n	AC26	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R4n	AB23	DQ1R			
5A	VREFB5AN0	IO		DEV_OE	DIFFIO_TX_R5p	DIFFOUT_R5p	AE29				
5A	VREFB5AN0	IO		nPERSTL0	DIFFIO_RX_R6p	DIFFOUT_R6p	AA21	DQS1R			
5A	VREFB5AN0	IO		DEV_CLRn	DIFFIO_TX_R5n	DIFFOUT_R5n	AD29	DQ1R			
5A	VREFB5AN0	IO		nPERSTL1	DIFFIO_RX_R6n	DIFFOUT_R6n	AA22	DQSn1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R7p	AC28	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R8p	Y24	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R7n	AC29				
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R8n	Y25	DQ1R			
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R9p	AB25				
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R10p	AF27	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R9n	AA25				
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R10n	AF26	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R11p	AB28	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R12p	AE28	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R11n	AB29	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R12n	AF28	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	AA23	DQS2R	DQS1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R14p	DIFFOUT_R14p	AG28				
5A	VREFB5AN0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	Y22	DQSn2R	DQSn1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R14n	DIFFOUT_R14n	AH28	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R15p	DIFFOUT_R15p	AB30	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R16p	DIFFOUT_R16p	AG29	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R15n	DIFFOUT_R15n	AA30	DQ2R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R16n	DIFFOUT_R16n	AH29				
5A	VREFB5AN0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	AA27				
5A	VREFB5AN0	IO			DIFFIO_TX_R18p	DIFFOUT_R18p	AK30	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	AA28				
5A	VREFB5AN0	IO			DIFFIO_TX_R18n	DIFFOUT_R18n	AJ30	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R19p	DIFFOUT_R19p	AG30	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R20p	DIFFOUT_R20p	AN33	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R19n	DIFFOUT_R19n	AF30	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R20n	DIFFOUT_R20n	AM33	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R21p	DIFFOUT_R21p	Y23	DQS3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R22p	DIFFOUT_R22p	AL32				
5A	VREFB5AN0	IO			DIFFIO_RX_R21n	DIFFOUT_R21n	W24	DQSn3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R22n	DIFFOUT_R22n	AK32	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R23p	DIFFOUT_R23p	AH31	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R24p	DIFFOUT_R24p	AL33	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_RX_R23n	DIFFOUT_R23n	AJ31	DQ3R	DQ1R		
5A	VREFB5AN0	IO			DIFFIO_TX_R24n	DIFFOUT_R24n	AK33				
5B	VREFB5BN0	IO			DIFFIO_RX_R25p	DIFFOUT_R25p	AA32				
5B	VREFB5BN0	IO			DIFFIO_TX_R26p	DIFFOUT_R26p	AE30	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R25n	DIFFOUT_R25n	Y32				
5B	VREFB5BN0	IO			DIFFIO_TX_R26n	DIFFOUT_R26n	AD30	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R27p	DIFFOUT_R27p	Y28	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R28p	DIFFOUT_R28p	AH32	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R27n	DIFFOUT_R27n	Y27	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R28n	DIFFOUT_R28n	AJ32	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	Y29	DQS4R	DQS2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R30p	DIFFOUT_R30p	AG31				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
5B	VREFB5BN0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	Y30	DQSn4R	DQSn2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R30n	DIFFOUT_R30n	AF31	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R31p	DIFFOUT_R31p	AC31	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R32p	DIFFOUT_R32p	AN34	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R31n	DIFFOUT_R31n	AC32	DQ4R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R32n	DIFFOUT_R32n	AM34				
5B	VREFB5BN0	IO	CLK7p,FPLL_BR_FBp		DIFFIO_RX_R33p	DIFFOUT_R33p	W26				
5B	VREFB5BN0	IO			DIFFIO_TX_R34p	DIFFOUT_R34p	AA31	DQ5R	DQ2R		
5B	VREFB5BN0	IO	CLK7n,FPLL_BR_FBn		DIFFIO_RX_R33n	DIFFOUT_R33n	W27				
5B	VREFB5BN0	IO			DIFFIO_TX_R34n	DIFFOUT_R34n	AB31	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R35p	DIFFOUT_R35p	AK34	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R36p	DIFFOUT_R36p	AH33	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R35n	DIFFOUT_R35n	AJ34	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R36n	DIFFOUT_R36n	AG33	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R37p	DIFFOUT_R37p	W29	DQS5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R38p	DIFFOUT_R38p	AD31				
5B	VREFB5BN0	IO			DIFFIO_RX_R37n	DIFFOUT_R37n	W30	DQSn5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R38n	DIFFOUT_R38n	AD32	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R39p	DIFFOUT_R39p	W31	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R40p	DIFFOUT_R40p	AE32	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_RX_R39n	DIFFOUT_R39n	V31	DQ5R	DQ2R		
5B	VREFB5BN0	IO			DIFFIO_TX_R40n	DIFFOUT_R40n	AF32				
5B	VREFB5BN0	IO	CLK6p		DIFFIO_RX_R41p	DIFFOUT_R41p	V28				
5B	VREFB5BN0	IO			DIFFIO_TX_R42p	DIFFOUT_R42p	AG34	DQ6R			
5B	VREFB5BN0	IO	CLK6n		DIFFIO_RX_R41n	DIFFOUT_R41n	V27				
5B	VREFB5BN0	IO			DIFFIO_TX_R42n	DIFFOUT_R42n	AH34	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43p	DIFFOUT_R43p	AC33	DQ6R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB		DIFFIO_TX_R44p	DIFFOUT_R44p	AF33	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R43n	DIFFOUT_R43n	AC34	DQ6R			
5B	VREFB5BN0	IO	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_R44n	DIFFOUT_R44n	AE33	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R45p	DIFFOUT_R45p	V24	DQS6R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46p	DIFFOUT_R46p	AE34				
5B	VREFB5BN0	IO			DIFFIO_RX_R45n	DIFFOUT_R45n	V23	DQSn6R			
5B	VREFB5BN0	IO			DIFFIO_TX_R46n	DIFFOUT_R46n	AD34	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	W32	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48p	DIFFOUT_R48p	AB33	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	V32	DQ6R			
5B	VREFB5BN0	IO			DIFFIO_TX_R48n	DIFFOUT_R48n	AB34				
6A	VREFB6AN0	IO	CLK5p		DIFFIO_RX_R49p	DIFFOUT_R49p	U31				
6A	VREFB6AN0	IO			DIFFIO_TX_R50p	DIFFOUT_R50p	Y33	DQ7R			
6A	VREFB6AN0	IO	CLK5n		DIFFIO_RX_R49n	DIFFOUT_R49n	U30				
6A	VREFB6AN0	IO			DIFFIO_TX_R50n	DIFFOUT_R50n	AA33	DQ7R			
6A	VREFB6AN0	IO			DIFFIO_RX_R51p	DIFFOUT_R51p	U28	DQ7R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB		DIFFIO_TX_R52p	DIFFOUT_R52p	Y34	DQ7R			
6A	VREFB6AN0	IO			DIFFIO_RX_R51n	DIFFOUT_R51n	U29	DQ7R			
6A	VREFB6AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_R52n	DIFFOUT_R52n	W34	DQ7R			
6A	VREFB6AN0	IO			DIFFIO_RX_R53p	DIFFOUT_R53p	U24	DQS7R			
6A	VREFB6AN0	IO			DIFFIO_TX_R54p	DIFFOUT_R54p	V33				
6A	VREFB6AN0	IO			DIFFIO_RX_R53n	DIFFOUT_R53n	U25	DQSn7R			
6A	VREFB6AN0	IO			DIFFIO_TX_R54n	DIFFOUT_R54n	V34	DQ7R			
6A	VREFB6AN0	IO			DIFFIO_RX_R55p	DIFFOUT_R55p	R34	DQ7R			
6A	VREFB6AN0	IO			DIFFIO_TX_R56p	DIFFOUT_R56p	U34	DQ7R			
6A	VREFB6AN0	IO			DIFFIO_RX_R55n	DIFFOUT_R55n	P34	DQ7R			
6A	VREFB6AN0	IO			DIFFIO_TX_R56n	DIFFOUT_R56n	U33				
6A	VREFB6AN0	IO	CLK4p,FPLL_TR_FBp		DIFFIO_RX_R57p	DIFFOUT_R57p	T31				
6A	VREFB6AN0	IO			DIFFIO_TX_R58p	DIFFOUT_R58p	T33	DQ8R	DQ3R		
6A	VREFB6AN0	IO	CLK4n,FPLL_TR_FBn		DIFFIO_RX_R57n	DIFFOUT_R57n	T30				
6A	VREFB6AN0	IO			DIFFIO_TX_R58n	DIFFOUT_R58n	T32	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R59p	DIFFOUT_R59p	T27	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R60p	DIFFOUT_R60p	M34	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R59n	DIFFOUT_R59n	T28	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R60n	DIFFOUT_R60n	M33	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R61p	DIFFOUT_R61p	U23	DQS8R	DQS3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R62p	DIFFOUT_R62p	K34				
6A	VREFB6AN0	IO			DIFFIO_RX_R61n	DIFFOUT_R61n	T23	DQSn8R	DQSn3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R62n	DIFFOUT_R62n	J34	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R63p	DIFFOUT_R63p	N33	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R64p	DIFFOUT_R64p	L33	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R63n	DIFFOUT_R63n	N34	DQ8R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R64n	DIFFOUT_R64n	L32				
6A	VREFB6AN0	IO			DIFFIO_RX_R65p	DIFFOUT_R65p	R32				
6A	VREFB6AN0	IO			DIFFIO_TX_R66p	DIFFOUT_R66p	K33	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R65n	DIFFOUT_R65n	R33				
6A	VREFB6AN0	IO			DIFFIO_TX_R66n	DIFFOUT_R66n	K32	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R67p	DIFFOUT_R67p	R27	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R68p	DIFFOUT_R68p	H34	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R67n	DIFFOUT_R67n	R28	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R68n	DIFFOUT_R68n	H33	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R69p	DIFFOUT_R69p	T25	DQS9R	DQ3R		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
6A	VREFB6AN0	IO			DIFFIO_TX_R70p	DIFFOUT_R70p	N32				
6A	VREFB6AN0	IO			DIFFIO_RX_R69n	DIFFOUT_R69n	R25	DQSn9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R70n	DIFFOUT_R70n	N31	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R71p	DIFFOUT_R71p	P32	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R72p	DIFFOUT_R72p	G34	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_RX_R71n	DIFFOUT_R71n	P31	DQ9R	DQ3R		
6A	VREFB6AN0	IO			DIFFIO_TX_R72n	DIFFOUT_R72n	G33				
6A	VREFB6AN0	IO			DIFFIO_RX_R73p	DIFFOUT_R73p	R30				
6A	VREFB6AN0	IO			DIFFIO_TX_R74p	DIFFOUT_R74p	M31	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R73n	DIFFOUT_R73n	R29				
6A	VREFB6AN0	IO			DIFFIO_TX_R74n	DIFFOUT_R74n	L31	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R75p	DIFFOUT_R75p	L30	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R76p	DIFFOUT_R76p	J32	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R75n	DIFFOUT_R75n	K30	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R76n	DIFFOUT_R76n	H32	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R77p	DIFFOUT_R77p	R23	DQS10R	DQS4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R78p	DIFFOUT_R78p	J31				
6A	VREFB6AN0	IO			DIFFIO_RX_R77n	DIFFOUT_R77n	R24	DQSn10R	DQSn4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R78n	DIFFOUT_R78n	H31	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R79p	DIFFOUT_R79p	N28	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R80p	DIFFOUT_R80p	P30	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R79n	DIFFOUT_R79n	M28	DQ10R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R80n	DIFFOUT_R80n	N29				
6A	VREFB6AN0	IO			DIFFIO_RX_R81p	DIFFOUT_R81p	P27				
6A	VREFB6AN0	IO			DIFFIO_TX_R82p	DIFFOUT_R82p	G31	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R81n	DIFFOUT_R81n	N27				
6A	VREFB6AN0	IO			DIFFIO_TX_R82n	DIFFOUT_R82n	G30	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R83p	DIFFOUT_R83p	M29	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R84p	DIFFOUT_R84p	J30	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R83n	DIFFOUT_R83n	M30	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R84n	DIFFOUT_R84n	J29	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R85p	DIFFOUT_R85p	P24	DQS11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R86p	DIFFOUT_R86p	H29				
6A	VREFB6AN0	IO			DIFFIO_RX_R85n	DIFFOUT_R85n	P25	DQSn11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R86n	DIFFOUT_R86n	H28	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R87p	DIFFOUT_R87p	L28	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R88p	DIFFOUT_R88p	K29	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_RX_R87n	DIFFOUT_R87n	L27	DQ11R	DQ4R		
6A	VREFB6AN0	IO			DIFFIO_TX_R88n	DIFFOUT_R88n	K28				
7A		GND					J26				
7A	VREFB7AN0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	K25				
7A	VREFB7AN0	IO			DIFFIO_TX_T2p	DIFFOUT_T2p	H27	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	J25				
7A	VREFB7AN0	IO			DIFFIO_TX_T2n	DIFFOUT_T2n	H26	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T3p	G25	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_TX_T4p	DIFFOUT_T4p	G28	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T3n	F25	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_TX_T4n	DIFFOUT_T4n	G29	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T5p	M24	DQS1T			
7A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p	F26				
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T5n	N24	DQSn1T			
7A	VREFB7AN0	IO			DIFFIO_TX_T6n	DIFFOUT_T6n	G26	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T7p	G24	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_TX_T8p	DIFFOUT_T8p	F30	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T7n	H24	DQ1T			
7A	VREFB7AN0	IO			DIFFIO_TX_T8n	DIFFOUT_T8n	E30				
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T9p	M25			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10p	DIFFOUT_T10p	F27	DQ2T	DQ1T	T_DM_4	T_DM_4
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T9n	L25			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T10n	DIFFOUT_T10n	F28	DQ2T	DQ1T	T_DQ_39	T_DQ_39
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T11p	D30	DQ2T	DQ1T	T_DQ_37	T_DQ_37
7A	VREFB7AN0	IO			DIFFIO_TX_T12p	DIFFOUT_T12p	C32	DQ2T	DQ1T	T_DQ_38	T_DQ_38
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T11n	D29	DQ2T	DQ1T	T_DQ_36	T_DQ_36
7A	VREFB7AN0	IO			DIFFIO_TX_T12n	DIFFOUT_T12n	C31	DQ2T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13p	DIFFOUT_T13p	L23	DQS2T	DQS1T	T_DQS_4	T_DQS_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14p	DIFFOUT_T14p	E29			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T13n	DIFFOUT_T13n	K23	DQSn2T	DQSn1T	T_DQS#_4	T_DQS#_4
7A	VREFB7AN0	IO			DIFFIO_TX_T14n	DIFFOUT_T14n	E28	DQ2T	DQ1T	T_DQ_35	T_DQ_35
7A	VREFB7AN0	IO			DIFFIO_RX_T15p	DIFFOUT_T15p	H23	DQ2T	DQ1T	T_DQ_33	T_DQ_33
7A	VREFB7AN0	IO			DIFFIO_TX_T16p	DIFFOUT_T16p	B31	DQ2T	DQ1T	T_DQ_34	T_DQ_34
7A	VREFB7AN0	IO			DIFFIO_RX_T15n	DIFFOUT_T15n	G23	DQ2T	DQ1T	T_DQ_32	T_DQ_32
7A	VREFB7AN0	IO			DIFFIO_TX_T16n	DIFFOUT_T16n	B30			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T17p	DIFFOUT_T17p	L22			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18p	DIFFOUT_T18p	E24	DQ3T	DQ1T	T_DM_3	T_DM_3
7A	VREFB7AN0	IO			DIFFIO_RX_T17n	DIFFOUT_T17n	K22			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T18n	DIFFOUT_T18n	E25	DQ3T	DQ1T	T_DQ_31	T_DQ_31
7A	VREFB7AN0	IO			DIFFIO_RX_T19p	DIFFOUT_T19p	F23	DQ3T	DQ1T	T_DQ_29	T_DQ_29
7A	VREFB7AN0	IO			DIFFIO_TX_T20p	DIFFOUT_T20p	C29	DQ3T	DQ1T	T_DQ_30	T_DQ_30
7A	VREFB7AN0	IO			DIFFIO_RX_T19n	DIFFOUT_T19n	F22	DQ3T	DQ1T	T_DQ_28	T_DQ_28

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
7A	VREFB7AN0	IO			DIFFIO_TX_T20n	DIFFOUT_T20n	C28	DQ3T	DQ1T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21p	DIFFOUT_T21p	M23	DQS3T	DQ1T	T_DQS_3	T_DQS_3
7A	VREFB7AN0	IO			DIFFIO_TX_T22p	DIFFOUT_T22p	E27			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T21n	DIFFOUT_T21n	N23	DQSn3T	DQ1T	T_DQS#_3	T_DQS#_3
7A	VREFB7AN0	IO			DIFFIO_TX_T22n	DIFFOUT_T22n	D26	DQ3T	DQ1T	T_DQ_27	T_DQ_27
7A	VREFB7AN0	IO			DIFFIO_RX_T23p	DIFFOUT_T23p	H22	DQ3T	DQ1T	T_DQ_25	T_DQ_25
7A	VREFB7AN0	IO			DIFFIO_TX_T24p	DIFFOUT_T24p	B28	DQ3T	DQ1T	T_DQ_26	T_DQ_26
7A	VREFB7AN0	IO			DIFFIO_RX_T23n	DIFFOUT_T23n	H21	DQ3T	DQ1T	T_DQ_24	T_DQ_24
7A	VREFB7AN0	IO			DIFFIO_TX_T24n	DIFFOUT_T24n	B29			GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T25p	DIFFOUT_T25p	L21			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26p	DIFFOUT_T26p	E22	DQ4T	DQ2T	T_DM_2	T_DM_2
7A	VREFB7AN0	IO			DIFFIO_RX_T25n	DIFFOUT_T25n	L20			GND	GND
7A	VREFB7AN0	IO			DIFFIO_TX_T26n	DIFFOUT_T26n	E23	DQ4T	DQ2T	T_DQ_23	T_DQ_23
7A	VREFB7AN0	IO			DIFFIO_RX_T27p	DIFFOUT_T27p	F21	DQ4T	DQ2T	T_DQ_21	T_DQ_21
7A	VREFB7AN0	IO			DIFFIO_TX_T28p	DIFFOUT_T28p	D27	DQ4T	DQ2T	T_DQ_22	T_DQ_22
7A	VREFB7AN0	IO			DIFFIO_RX_T27n	DIFFOUT_T27n	G21	DQ4T	DQ2T	T_DQ_20	T_DQ_20
7A	VREFB7AN0	IO			DIFFIO_TX_T28n	DIFFOUT_T28n	C27	DQ4T	DQ2T	GND	GND
7A	VREFB7AN0	IO			DIFFIO_RX_T29p	DIFFOUT_T29p	N22	DQS4T	DQS2T	T_DQS_2	T_DQS_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30p	DIFFOUT_T30p	D25			T_RESET#	T_RESET#
7A	VREFB7AN0	IO			DIFFIO_RX_T29n	DIFFOUT_T29n	M21	DQSn4T	DQSn2T	T_DQS#_2	T_DQS#_2
7A	VREFB7AN0	IO			DIFFIO_TX_T30n	DIFFOUT_T30n	C26	DQ4T	DQ2T	T_DQ_19	T_DQ_19
7A	VREFB7AN0	IO			DIFFIO_RX_T31p	DIFFOUT_T31p	F20	DQ4T	DQ2T	T_DQ_17	T_DQ_17
7A	VREFB7AN0	IO			DIFFIO_TX_T32p	DIFFOUT_T32p	D24	DQ4T	DQ2T	T_DQ_18	T_DQ_18
7A	VREFB7AN0	IO			DIFFIO_RX_T31n	DIFFOUT_T31n	G20	DQ4T	DQ2T	T_DQ_16	T_DQ_16
7A	VREFB7AN0	IO			DIFFIO_TX_T32n	DIFFOUT_T32n	C24			GND	GND
7A	VREFB7AN0	IO	CLK11p		DIFFIO_RX_T33p	DIFFOUT_T33p	J20				
7A	VREFB7AN0	IO			DIFFIO_TX_T34p	DIFFOUT_T34p	A28	DQ5T	DQ2T	T_DM_1	T_DM_1
7A	VREFB7AN0	IO	CLK11n		DIFFIO_RX_T33n	DIFFOUT_T33n	K19				
7A	VREFB7AN0	IO			DIFFIO_TX_T34n	DIFFOUT_T34n	A27	DQ5T	DQ2T	T_DQ_15	T_DQ_15
7A	VREFB7AN0	IO			DIFFIO_RX_T35p	DIFFOUT_T35p	D22	DQ5T	DQ2T	T_DQ_13	T_DQ_13
7A	VREFB7AN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	B26	DQ5T	DQ2T	T_DQ_14	T_DQ_14
7A	VREFB7AN0	IO			DIFFIO_RX_T35n	DIFFOUT_T35n	C23	DQ5T	DQ2T	T_DQ_12	T_DQ_12
7A	VREFB7AN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	B25	DQ5T	DQ2T	T_CKE_0	T_CKE_0
7A	VREFB7AN0	IO			DIFFIO_RX_T37p	DIFFOUT_T37p	M20	DQS5T	DQ2T	T_DQS_1	T_DQS_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	C22			T_CKE_1	T_CKE_1
7A	VREFB7AN0	IO			DIFFIO_RX_T37n	DIFFOUT_T37n	M19	DQSn5T	DQ2T	T_DQS#_1	T_DQS#_1
7A	VREFB7AN0	IO			DIFFIO_TX_T38n	DIFFOUT_T38n	D21	DQ5T	DQ2T	T_DQ_11	T_DQ_11
7A	VREFB7AN0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	E20	DQ5T	DQ2T	T_DQ_9	T_DQ_9
7A	VREFB7AN0	IO			DIFFIO_TX_T40p	DIFFOUT_T40p	A26	DQ5T	DQ2T	T_DQ_10	T_DQ_10
7A	VREFB7AN0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	D20	DQ5T	DQ2T	T_DQ_8	T_DQ_8
7A	VREFB7AN0	IO			DIFFIO_TX_T40n	DIFFOUT_T40n	A25			GND	GND
7A	VREFB7AN0	IO	CLK10p		DIFFIO_RX_T41p	DIFFOUT_T41p	H19				
7A	VREFB7AN0	IO			DIFFIO_TX_T42p	DIFFOUT_T42p	B23	DQ6T		T_DM_0	T_DM_0
7A	VREFB7AN0	IO	CLK10n		DIFFIO_RX_T41n	DIFFOUT_T41n	H18				
7A	VREFB7AN0	IO			DIFFIO_TX_T42n	DIFFOUT_T42n	B24	DQ6T		T_DQ_7	T_DQ_7
7A	VREFB7AN0	IO			DIFFIO_RX_T43p	DIFFOUT_T43p	C21	DQ6T		T_DQ_5	T_DQ_5
7A	VREFB7AN0	IO			DIFFIO_TX_T44p	DIFFOUT_T44p	A23	DQ6T		T_DQ_6	T_DQ_6
7A	VREFB7AN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	B21	DQ6T		T_DQ_4	T_DQ_4
7A	VREFB7AN0	IO			DIFFIO_TX_T44n	DIFFOUT_T44n	A22	DQ6T		T_ODT_1	T_ODT_1
7A	VREFB7AN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	M18	DQS6T		T_DQS_0	T_DQS_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46p	DIFFOUT_T46p	E19			T_ODT_0	T_ODT_0
7A	VREFB7AN0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	L18	DQSn6T		T_DQS#_0	T_DQS#_0
7A	VREFB7AN0	IO			DIFFIO_TX_T46n	DIFFOUT_T46n	D19	DQ6T		T_DQ_3	T_DQ_3
7A	VREFB7AN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	B20	DQ6T		T_DQ_1	T_DQ_1
7A	VREFB7AN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p	A21	DQ6T		T_DQ_2	T_DQ_2
7A	VREFB7AN0	IO			DIFFIO_RX_T47n	DIFFOUT_T47n	B19	DQ6T		T_DQ_0	T_DQ_0
7A	VREFB7AN0	IO	RZQ_2		DIFFIO_TX_T48n	DIFFOUT_T48n	A20				
8A	VREFB8AN0	IO	CLK9p		DIFFIO_RX_T49p	DIFFOUT_T49p	G18				
8A	VREFB8AN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	C18	DQ7T		T_A_0	T_CA_0
8A	VREFB8AN0	IO	CLK9n		DIFFIO_RX_T49n	DIFFOUT_T49n	F18				
8A	VREFB8AN0	IO			DIFFIO_TX_T50n	DIFFOUT_T50n	C17	DQ7T		T_A_1	T_CA_1
8A	VREFB8AN0	IO			DIFFIO_RX_T51p	DIFFOUT_T51p	E18	DQ7T		T_A_4	T_CA_4
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB		DIFFIO_TX_T52p	DIFFOUT_T52p	B18	DQ7T		T_A_2	T_CA_2
8A	VREFB8AN0	IO			DIFFIO_RX_T51n	DIFFOUT_T51n	E17	DQ7T		T_A_5	T_CA_5
8A	VREFB8AN0	IO	FPLL_TL_CLKOUT1,FPLL_TL_CLKOUTn		DIFFIO_TX_T52n	DIFFOUT_T52n	A18	DQ7T		T_A_3	T_CA_3
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T53p	M16	DQS7T		T_CK	T_CK
8A	VREFB8AN0	IO			DIFFIO_TX_T54p	DIFFOUT_T54p	A17			T_A_6	T_CA_6
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T53n	L17	DQSn7T		T_CK#	T_CK#
8A	VREFB8AN0	IO			DIFFIO_TX_T54n	DIFFOUT_T54n	A16	DQ7T		T_A_7	T_CA_7
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T55p	C16	DQ7T		T_BA_1	
8A	VREFB8AN0	IO			DIFFIO_TX_T56p	DIFFOUT_T56p	B15	DQ7T		T_BA_0	
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T55n	B16	DQ7T		T_BA_2	
8A	VREFB8AN0	IO			DIFFIO_TX_T56n	DIFFOUT_T56n	A15			GND	GND
8A	VREFB8AN0	IO	CLK8p,FPLL_TL_FBp		DIFFIO_RX_T57p	DIFFOUT_T57p	H17				
8A	VREFB8AN0	IO			DIFFIO_TX_T58p	DIFFOUT_T58p	A12	DQ8T	DQ3T	T_CAS#	
8A	VREFB8AN0	IO	CLK8n,FPLL_TL_FBn		DIFFIO_RX_T57n	DIFFOUT_T57n	H16				
8A	VREFB8AN0	IO			DIFFIO_TX_T58n	DIFFOUT_T58n	A11	DQ8T	DQ3T	T_RAS#	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T59p	F17	DQ8T	DQ3T	T_A_8	T_CA_8
8A	VREFB8AN0	IO			DIFFIO_TX_T60p	DIFFOUT_T60p	B13	DQ8T	DQ3T	T_A_10	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 (2)	HMC Pin Assignment for LPDDR2
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T59n	F16	DQ8T	DQ3T	T_A_9	T_CA_9
8A	VREFB8AN0	IO			DIFFIO_TX_T60n	DIFFOUT_T60n	A13	DQ8T	DQ3T	T_A_11	
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T61p	M15	DQS8T	DQS3T	T_CS#_0	T_CS#_0
8A	VREFB8AN0	IO			DIFFIO_TX_T62p	DIFFOUT_T62p	C14			T_A_12	
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T61n	M14	DQSn8T	DQSn3T	T_CS#_1	T_CS#_1
8A	VREFB8AN0	IO			DIFFIO_TX_T62n	DIFFOUT_T62n	B14	DQ8T	DQ3T	T_A_13	
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T63p	D17	DQ8T	DQ3T	T_A_14	
8A	VREFB8AN0	IO			DIFFIO_TX_T64p	DIFFOUT_T64p	B10	DQ8T	DQ3T	T_WE#	
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T63n	D16	DQ8T	DQ3T	T_A_15	
8A	VREFB8AN0	IO			DIFFIO_TX_T64n	DIFFOUT_T64n	A10			GND	GND
8A	VREFB8AN0	IO			DIFFIO_RX_T65p	DIFFOUT_T65p	F15				
8A	VREFB8AN0	IO			DIFFIO_TX_T66p	DIFFOUT_T66p	A7	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T65n	DIFFOUT_T65n	G15				
8A	VREFB8AN0	IO			DIFFIO_TX_T66n	DIFFOUT_T66n	A6	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T67p	DIFFOUT_T67p	B8	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T68p	DIFFOUT_T68p	C11	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T67n	DIFFOUT_T67n	A8	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T68n	DIFFOUT_T68n	B11	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T69p	DIFFOUT_T69p	L16	DQS9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T70p	DIFFOUT_T70p	C9				
8A	VREFB8AN0	IO			DIFFIO_RX_T69n	DIFFOUT_T69n	L15	DQSn9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T70n	DIFFOUT_T70n	B9	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T71p	DIFFOUT_T71p	E15	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T72p	DIFFOUT_T72p	C13	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n	D15	DQ9T	DQ3T		
8A	VREFB8AN0	IO			DIFFIO_TX_T72n	DIFFOUT_T72n	C12				
8A	VREFB8AN0	IO			DIFFIO_RX_T73p	DIFFOUT_T73p	J15				
8A	VREFB8AN0	IO			DIFFIO_TX_T74p	DIFFOUT_T74p	B5	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T73n	DIFFOUT_T73n	K14				
8A	VREFB8AN0	IO			DIFFIO_TX_T74n	DIFFOUT_T74n	A5	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T75p	DIFFOUT_T75p	E14	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T76p	DIFFOUT_T76p	C6	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T75n	DIFFOUT_T75n	D14	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T76n	DIFFOUT_T76n	B6	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T77p	DIFFOUT_T77p	P14	DQS10T	DQS4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	F13				
8A	VREFB8AN0	IO			DIFFIO_RX_T77n	DIFFOUT_T77n	N14	DQSn10T	DQSn4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	E13	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T79p	DIFFOUT_T79p	H14	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T80p	DIFFOUT_T80p	B4	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T79n	DIFFOUT_T79n	G14	DQ10T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T80n	DIFFOUT_T80n	A3				
8A	VREFB8AN0	IO			DIFFIO_RX_T81p	DIFFOUT_T81p	M13				
8A	VREFB8AN0	IO			DIFFIO_TX_T82p	DIFFOUT_T82p	D11	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T81n	DIFFOUT_T81n	L13				
8A	VREFB8AN0	IO			DIFFIO_TX_T82n	DIFFOUT_T82n	D10	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T83p	DIFFOUT_T83p	G13	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T84p	DIFFOUT_T84p	C8	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T83n	DIFFOUT_T83n	H13	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T84n	DIFFOUT_T84n	C7	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T85p	DIFFOUT_T85p	N13	DQS11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T86p	DIFFOUT_T86p	A2				
8A	VREFB8AN0	IO			DIFFIO_RX_T85n	DIFFOUT_T85n	N12	DQSn11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T86n	DIFFOUT_T86n	B3	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T87p	DIFFOUT_T87p	E12	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T88p	DIFFOUT_T88p	C1	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_RX_T87n	DIFFOUT_T87n	D12	DQ11T	DQ4T		
8A	VREFB8AN0	IO			DIFFIO_TX_T88n	DIFFOUT_T88n	B1				
8A	VREFB8AN0	IO			DIFFIO_RX_T89p	DIFFOUT_T89p	L12				
8A	VREFB8AN0	IO			DIFFIO_TX_T90p	DIFFOUT_T90p	F10	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_RX_T89n	DIFFOUT_T89n	K13				
8A	VREFB8AN0	IO			DIFFIO_TX_T90n	DIFFOUT_T90n	E10	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_RX_T91p	DIFFOUT_T91p	F12	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T92p	DIFFOUT_T92p	E9	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_RX_T91n	DIFFOUT_T91n	F11	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T92n	DIFFOUT_T92n	D9	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_RX_T93p	DIFFOUT_T93p	L11	DQS12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T94p	DIFFOUT_T94p	E7				
8A	VREFB8AN0	IO			DIFFIO_RX_T93n	DIFFOUT_T93n	K12	DQSn12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T94n	DIFFOUT_T94n	D7	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_RX_T95p	DIFFOUT_T95p	H12	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T96p	DIFFOUT_T96p	F8	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_RX_T95n	DIFFOUT_T95n	G11	DQ12T			
8A	VREFB8AN0	IO			DIFFIO_TX_T96n	DIFFOUT_T96n	E8				
9A		MSEL0		MSEL0			J12				
9A		CONF_DONE		CONF_DONE			G10				
9A		MSEL1		MSEL1			J11				
9A		nSTATUS		nSTATUS			G9				
9A		nCE		nCE			F7				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
9A		MSEL2		MSEL2			F6				
9A		MSEL3		MSEL3			K10				
9A		nCONFIG		nCONFIG			G8				
9A		MSEL4		MSEL4			H7				
9A		GND					H8				
		GND					L24				
		GND					AP2				
		GND					AP4				
		GND					AP8				
		GND					AP13				
		GND					AP18				
		GND					AP23				
		GND					AP28				
		GND					AP33				
		GND					AN6				
		GND					AN15				
		GND					AN25				
		GND					AM3				
		GND					AM12				
		GND					AM22				
		GND					AM32				
		GND					AL5				
		GND					AL9				
		GND					AL19				
		GND					AL29				
		GND					AL34				
		GND					AK1				
		GND					AK2				
		GND					AK3				
		GND					AK6				
		GND					AK16				
		GND					AK26				
		GND					AJ3				
		GND					AJ4				
		GND					AJ5				
		GND					AJ13				
		GND					AJ23				
		GND					AJ33				
		GND					AH1				
		GND					AH2				
		GND					AH5				
		GND					AH10				
		GND					AH20				
		GND					AH30				
		GND					AG3				
		GND					AG4				
		GND					AG5				
		GND					AG6				
		GND					AG7				
		GND					AG17				
		GND					AG27				
		GND					AF1				
		GND					AF2				
		GND					AF5				
		GND					AF6				
		GND					AF7				
		GND					AF14				
		GND					AF24				
		GND					AF34				
		GND					AE3				
		GND					AE4				
		GND					AE5				
		GND					AE6				
		GND					AE7				
		GND					AE8				
		GND					AE9				
		GND					AE11				
		GND					AE21				
		GND					AE31				
		GND					AD1				
		GND					AD2				
		GND					AD5				
		GND					AD6				
		GND					AD7				
		GND					AD9				
		GND					AD10				
		GND					AD18				
		GND					AD28				
		GND					AC3				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					AC4				
		GND					AC5				
		GND					AC6				
		GND					AC8				
		GND					AC10				
		GND					AC15				
		GND					AC25				
		GND					AB1				
		GND					AB2				
		GND					AB5				
		GND					AB6				
		GND					AB7				
		GND					AB9				
		GND					AB11				
		GND					AB12				
		GND					AB22				
		GND					AB32				
		GND					AA3				
		GND					AA4				
		GND					AA5				
		GND					AA6				
		GND					AA8				
		GND					AA10				
		GND					AA12				
		GND					AA14				
		GND					AA19				
		GND					AA29				
		GND					AA34				
		GND					Y1				
		GND					Y2				
		GND					Y5				
		GND					Y6				
		GND					Y7				
		GND					Y9				
		GND					Y10				
		GND					Y11				
		GND					Y13				
		GND					Y15				
		GND					Y17				
		GND					Y19				
		GND					Y21				
		GND					W3				
		GND					W4				
		GND					W5				
		GND					W6				
		GND					W8				
		GND					W10				
		GND					W12				
		GND					W14				
		GND					W16				
		GND					W18				
		GND					W20				
		GND					W22				
		GND					W23				
		GND					W33				
		GND					V1				
		GND					V2				
		GND					V5				
		GND					V6				
		GND					V7				
		GND					V9				
		GND					V11				
		GND					V13				
		GND					V15				
		GND					V17				
		GND					V19				
		GND					V21				
		GND					V30				
		GND					U3				
		GND					U4				
		GND					U5				
		GND					U6				
		GND					U8				
		GND					U10				
		GND					U12				
		GND					U14				
		GND					U16				
		GND					U18				
		GND					U20				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					U22				
		GND					U27				
		GND					T1				
		GND					T2				
		GND					T5				
		GND					T6				
		GND					T7				
		GND					T9				
		GND					T11				
		GND					T13				
		GND					T15				
		GND					T17				
		GND					T19				
		GND					T21				
		GND					T24				
		GND					T34				
		GND					R3				
		GND					R4				
		GND					R5				
		GND					R6				
		GND					R8				
		GND					R10				
		GND					R12				
		GND					R14				
		GND					R16				
		GND					R18				
		GND					R20				
		GND					R22				
		GND					R31				
		GND					P1				
		GND					P2				
		GND					P5				
		GND					P6				
		GND					P7				
		GND					P9				
		GND					P11				
		GND					P13				
		GND					P15				
		GND					P17				
		GND					P19				
		GND					P21				
		GND					P28				
		GND					N3				
		GND					N4				
		GND					N5				
		GND					N6				
		GND					N8				
		GND					N10				
		GND					N11				
		GND					N16				
		GND					N18				
		GND					N20				
		GND					N25				
		GND					M1				
		GND					M2				
		GND					M5				
		GND					M6				
		GND					M7				
		GND					M9				
		GND					M10				
		GND					M12				
		GND					M17				
		GND					M22				
		GND					M32				
		GND					L3				
		GND					L4				
		GND					L5				
		GND					L6				
		GND					L7				
		GND					L8				
		GND					L9				
		GND					L14				
		GND					L19				
		GND					L29				
		GND					L34				
		GND					K1				
		GND					K2				
		GND					K5				
		GND					K6				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		GND					K7				
		GND					K8				
		GND					K16				
		GND					K26				
		GND					J3				
		GND					J4				
		GND					J5				
		GND					J13				
		GND					J23				
		GND					J33				
		GND					H1				
		GND					H2				
		GND					H5				
		GND					H10				
		GND					H20				
		GND					H30				
		GND					G3				
		GND					G4				
		GND					G5				
		GND					G7				
		GND					G17				
		GND					G27				
		GND					F1				
		GND					F2				
		GND					F5				
		GND					F14				
		GND					F24				
		GND					F34				
		GND					E2				
		GND					E3				
		GND					E4				
		GND					E5				
		GND					E11				
		GND					E21				
		GND					E31				
		GND					D1				
		GND					D2				
		GND					D5				
		GND					D8				
		GND					D18				
		GND					D28				
		GND					D33				
		GND					C3				
		GND					C4				
		GND					C5				
		GND					C15				
		GND					C25				
		GND					B2				
		GND					B22				
		GND					B32				
		GND					B34				
		GND					A4				
		GND					A9				
		GND					A19				
		GND					A29				
		VCC					N21				
		VCC					AA13				
		VCC					Y12				
		VCC					Y14				
		VCC					Y16				
		VCC					Y18				
		VCC					W13				
		VCC					W15				
		VCC					W17				
		VCC					W19				
		VCC					W21				
		VCC					V12				
		VCC					V14				
		VCC					V16				
		VCC					V18				
		VCC					V20				
		VCC					V22				
		VCC					U13				
		VCC					U15				
		VCC					U17				
		VCC					U19				
		VCC					U21				
		VCC					T12				
		VCC					T14				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		VCC					T16				
		VCC					T18				
		VCC					T20				
		VCC					T22				
		VCC					R13				
		VCC					R15				
		VCC					R17				
		VCC					R19				
		VCC					R21				
		VCC					P12				
		VCC					P16				
		VCC					P18				
		VCC					P20				
		VCC					P22				
		VCC					N15				
		VCC					N17				
		VCC					N19				
		DNU					D4				
		DNU					D3				
		DNU					AG9				
		DNU					AF17				
		DNU					J24				
		DNU					J17				
		VCCPGM					AF12				
		VCCPGM					AD27				
		VCCPGM					H11				
		VCCBAT					H9				
		VCCIO3A					AD13				
		VCCIO3A					AM7				
		VCCIO3A					AK11				
		VCCIO3A					AJ8				
		VCCIO3A					AG12				
		VCCIO3A					AF9				
		VCCIO3B					AB17				
		VCCIO3B					AN10				
		VCCIO3B					AM17				
		VCCIO3B					AL14				
		VCCIO3B					AH15				
		VCCIO3B					AE16				
		VCCIO4A					AD23				
		VCCIO4A					AN20				
		VCCIO4A					AN30				
		VCCIO4A					AM27				
		VCCIO4A					AL24				
		VCCIO4A					AK21				
		VCCIO4A					AJ18				
		VCCIO4A					AJ28				
		VCCIO4A					AH25				
		VCCIO4A					AG22				
		VCCIO4A					AF19				
		VCCIO4A					AC20				
		VCCIO5A					AA24				
		VCCIO5A					AK31				
		VCCIO5A					AF29				
		VCCIO5A					AE26				
		VCCIO5A					AB27				
		VCCIO5A					Y26				
		VCCIO5B					V25				
		VCCIO5B					AG32				
		VCCIO5B					AD33				
		VCCIO5B					AC30				
		VCCIO5B					Y31				
		VCCIO5B					W28				
		VCCIO6A					G32				
		VCCIO6A					U32				
		VCCIO6A					T29				
		VCCIO6A					R26				
		VCCIO6A					P23				
		VCCIO6A					P33				
		VCCIO6A					N30				
		VCCIO6A					M27				
		VCCIO6A					K31				
		VCCIO6A					J28				
		VCCIO7A					A24				
		VCCIO7A					K21				
		VCCIO7A					J18				
		VCCIO7A					H25				
		VCCIO7A					G22				
		VCCIO7A					F19				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		VCCIO7A					F29				
		VCCIO7A					E26				
		VCCIO7A					D23				
		VCCIO7A					C20				
		VCCIO7A					C30				
		VCCIO7A					B27				
		VCCIO8A					B17				
		VCCIO8A					K11				
		VCCIO8A					H15				
		VCCIO8A					G12				
		VCCIO8A					F9				
		VCCIO8A					E6				
		VCCIO8A					E16				
		VCCIO8A					D13				
		VCCIO8A					C10				
		VCCIO8A					B7				
		VCCIO8A					B12				
		VCCIO8A					A14				
		VCCPD3A					AE15				
		VCCPD3A					AE13				
		VCCPD3B4A					AE17				
		VCCPD3B4A					AF15				
		VCCPD3B4A					AF16				
		VCCPD3B4A					AF20				
		VCCPD3B4A					AF21				
		VCCPD3B4A					AE22				
		VCCPD5A					AA26				
		VCCPD5A					AB26				
		VCCPD5B					W25				
		VCCPD5B					V26				
		VCCPD6A					P26				
		VCCPD6A					U26				
		VCCPD6A					T26				
		VCCPD6A					N26				
		VCCPD7A8A					J22				
		VCCPD7A8A					K15				
		VCCPD7A8A					K17				
		VCCPD7A8A					K20				
		VCCPD7A8A					J14				
		VCCPD7A8A					J16				
		VCCPD7A8A					J19				
		VCCPD7A8A					J21				
3A	VREFB3AN0	VREFB3AN0					AH11				
3B	VREFB3BN0	VREFB3BN0					AH18				
4A	VREFB4AN0	VREFB4AN0					AG20				
5A	VREFB5AN0	VREFB5AN0					AE27				
5B	VREFB5BN0	VREFB5BN0					V29				
6A	VREFB6AN0	VREFB6AN0					P29				
7A	VREFB7AN0	VREFB7AN0					G19				
8A	VREFB8AN0	VREFB8AN0					G16				
		NC					AP3				
		NC					AN1				
		NC					AN2				
		NC					AN3				
		NC					AM1				
		NC					AM2				
		NC					AL1				
		NC					AL2				
		NC					AL3				
		NC					AL4				
		NC					AK4				
		NC					AH6				
		NC					AH7				
		NC					AG8				
		NC					AF8				
		NC					L10				
		NC					L26				
		NC					K9				
		NC					K27				
		NC					J6				
		NC					J7				
		NC					J8				
		NC					J9				
		NC					J27				
		NC					H6				
		NC					G6				
		NC					F31				
		NC					F32				
		NC					F33				

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8	DQS for X16	HMC Pin Assignment for DDR3/DDR2 *(2)*	HMC Pin Assignment for LPDDR2
		NC					E32				
		NC					E33				
		NC					E34				
		NC					D6				
		NC					D31				
		NC					D32				
		NC					D34				
		NC					C2				
		NC					C19				
		NC					C33				
		NC					C34				
		NC					B33				
		NC					A30				
		NC					A31				
		NC					A32				
		NC					A33				
		VCCH_GXBL					N9				
		VCCH_GXBL					AB8				
		VCCH_GXBL					W9				
		VCCH_GXBL					T8				
		VCCL_GXBL					N7				
		VCCL_GXBL					AC7				
		VCCL_GXBL					AA7				
		VCCL_GXBL					W7				
		VCCL_GXBL					U7				
		VCCL_GXBL					R7				
		RREF_TL					E1				
		VCCA_FPLL					AC11				
		VCCA_FPLL					M11				
		VCCA_FPLL					AD26				
		VCCA_FPLL					M26				
		VCC_AUX					J10				
		VCC_AUX					K18				
		VCC_AUX					K24				
		VCC_AUX					AE24				
		VCC_AUX					AE18				
		VCC_AUX					AE12				
		VCCE_GXBL					P8				
		VCCE_GXBL					AD8				
		VCCE_GXBL					AC9				
		VCCE_GXBL					AA9				
		VCCE_GXBL					Y8				
		VCCE_GXBL					V8				
		VCCE_GXBL					U9				
		VCCE_GXBL					R9				
		VCCE_GXBL					M8				

Notes:
(1) For more information about pin definition and pin connection guidelines, refer to the Cyclone V Device Family Pin Connection Guidelines.
(2) RESET pin is only applicable for DDR3 device.

Version Number	Date	Changes Made
1.0	7/3/2012	Initial release.
1.1	5/22/2013	- Added U484 package. - Updated the column from "HMC Pin Assignment for DDR3" to "HMC Pin Assignment for DDR3/DDR2". - Added notes to the "HMC Pin Assignment for DDR3/DDR2" and "HMC Pin Assignment for LPDDR2" columns.