DEVICE
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DEI1041
ARINC 429 LINE RECEIVER

FEATURES

- ARINC 429 to TTL/CMOS logic line receiver
- Operates from single +5V ± 10% or 3.3V ± 10% power supply
- ARINC inputs internally protected to lightning requirements of DO-160D Level A3
- Operates in high noise environment
  - Input Common Voltage Range: ± 20V
  - 2V minimum Input hysteresis
- Logic level TEST inputs bypass analog inputs.
- 8 Lead SOIC.
- Replacement for HI-8588 and HI-8588-10

TERMINAL DESCRIPTION

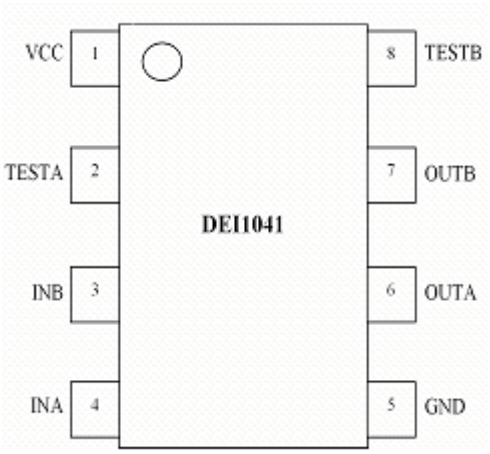


Table 1 Terminal Description

NAME	DESCRIPTION
INA	**429 INPUT.** ARINC 429 format serial digital data "A" input.
INB	**429 INPUT.** ARINC 429 format serial digital data "B" input.
TESTA	**LOGIC INPUT.** Test input A.
TESTB	**LOGIC INPUT.** Test input B.
OUTA	**LOGIC OUTPUT.** CMOS/TTL format serial digital data "A" output.
OUTB	**LOGIC OUTPUT.** CMOS/TTL format serial digital data "B" output.
VDD	**POWER INPUT.** 5 VDC OR 3.3VDC.
GND	**POWER INPUT.** Ground.

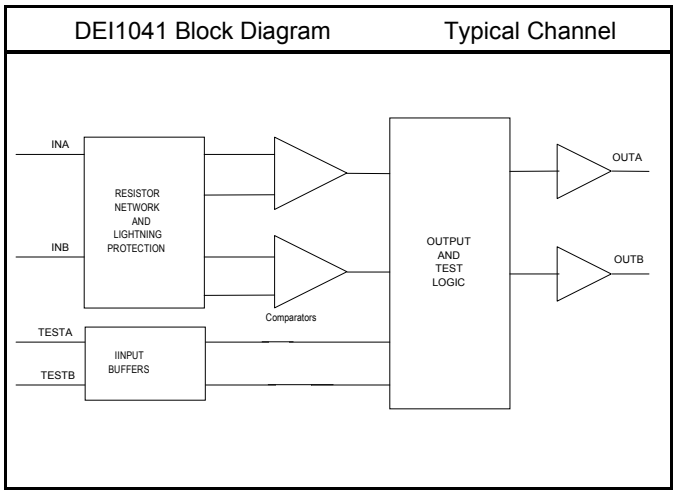
FUNCTIONAL DESCRIPTION

The DEI1041 is a BICMOS device which contains one ARINC 429 differential line receiver. It translates incoming ARINC 429 data bus signals (tri-level RZ bipolar differential modulation) to a pair of TTL/CMOS logic outputs. It meets the requirements of the ARINC 429 Digital Information Transfer Standard. Refer to Figure 1 " DEI1041 Block Diagram and Truth Table".

The device is designed to operate in a high noise environment. Inputs are accepted over a +/- 20V common mode voltage range and the receivers provide over 2 Volts of hysteresis. Circuit speed is optimized to reject high frequency transients.

All ARINC input pins are designed with internal protection from damage due to transients meeting the lightning induced transient requirements of DO-160D Level A3. The ARINC inputs may optionally be connected to ARINC bus through external 10k ohm series resistors. These resistors may be added in combination with transient voltage suppressors to achieve lighting protection beyond the Level A3 limits due to high input impedance.

The DEI1041 device provides logic level TEST inputs for built in system test. They force the receiver outputs to the specified ZERO, ONE or NULL state. The ARINC inputs are ignored when the device is in test mode.



DEI1041 Truth Table					
INPUTS			OUTPUTS		
TEST INPUTS (TTL/CMOS)		ARINC INPUTS	TTL/CMOS		
TEST A	TEST B	$A_{IN} - B_{IN}$ V	OUT A	OUT B	Logic
0	0	≥6.5v	1	0	ONE
0	0	≤-6.5V	0	1	ZERO
0	0	-2.5 to +2.5	0	0	NULL
0	1	X	0	1	ZERO
1	0	X	1	0	ONE
1	1	X	0	0	NULL

Figure 1 DEI1041 Block Diagram and Truth Table

ELECTRICAL DESCRIPTION

Table 2 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	Vdd	+5V ± 10% +3.3V ± 10%
Logic Input Levels	$V_{TESTA,B}$	0 to Vdd
Operating Temperature -SES -SMS	Ta	 -55 to +85°C -55 to +125°C

Table 3 Absolute Maximum Rating

PARAMETER	MIN	MAX	UNITS
Supply Voltage (with respect to V_{SS})	-0.3	7.0	V
Storage Temperature	-65	+150	°C
Input Voltage, continuous (ARINC Inputs)	-40	+40	V
Input Voltage (Test Inputs)	V_{SS} – 0.3	V_{DD}+0.3	V
Power Dissipation @ 85 °C		500	mW
Junction Temperature: Tjmax, (limited by molding compound Tg)		145	°C
Peak Body Temperature, - G Package		260	°C
Lightning Protection (ARINC 429 Channel Inputs and TESTA/TESTB Inputs) Waveform 3 (2) Waveform 4, 5A, 5B* (2) (3)	 -600 -300	 +600 +300	 V V
ESD per JEDEC A114-A Human Body Model	-1000	1000	V

Notes:
1. Stresses above these limits can cause permanent damage.
2. Per DO160D, Sect 22 Level 3A. See Figures 4-6.
3. Inputs can be protected to withstand higher stress by adding series resistors and shunt TVS on inputs. Inputs withstand 1500V Waveform 5A when clipped ≤ 600V.

Table 4 Electrical Characteristics

Conditions: Temperature: -55°C to +85°C (SES) : -55°C to +125°C (SMS); V_{DD} = +5V ± 10% or 3.3V ± 10%

PARAMETER	TEST CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
ARINC INPUTS						
$V_A – V_B$ = Logic +1	OUTA = 1	V_{+1}	6.5	10	13	V
$V_A – V_B$ = Logic -1	OUTB = 1	V_{-1}	-6.5	-10	-13	V
$V_A – V_B$ = Logic Null	OUTA = 0 OUTB = 0	V_{NULL}	-2.5	0	2.5	V
Input Hysteresis		V_{HY}	2.0		4.0	V
$V_A – V_B$ = Null to +1 transition	OUTA = 0→1	V_{T+1+}	5.5		6.5	V
$V_A – V_B$ = +1 to Null transition	OUTA = 1→0	V_{T+1-}	2.5		3.5	V
$V_A – V_B$ = Null to -1 transition	OUTB = 0→1	V_{T-1+}	-6.5		-5.5	V
$V_A – V_B$ = -1 to Null transition	OUTB = 1→0	V_{T-1-}	-3.5		-2.5	V
Input Common Mode Voltage Range	Logic +1, Null, Logic -1	V_{CM}	-20		+20	V
Input Resistance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V (1)	R_{IN}	280k	780K		Ω
Input Resistance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V	R_S	140k	390K		Ω
Input Capacitance IN_A to IN_B	V_{DD} open, Shorted to V_{SS} or +5V (1)	C_{IN}			10	pF

Conditions: Temperature: -55°C to +85°C (SES) : -55°C to +125°C (SMS); V_{DD} = +5V ± 10% or 3.3V ± 10%						
PARAMETER	**TEST CONDITION**	**SYMBOL**	**MIN**	**NOM**	**MAX**	**UNITS**
Input Capacitance IN_A or IN_B to V_{SS}	V_{DD} open, Shorted to V_{SS} or +5V (1)	C_S			10	pF
TEST INPUTS						
Logic 0 Voltage		V_{IL}			0.8	V
Logic 1 Voltage		V_{IH}	2.0			V
Logic 0 Current	V_{IL} = 0.8	I_{IL}			20	µA
Logic 1 Current	V_{IH} = 2.0	I_{IH}			20	µA
LOGIC OUTPUTS						
OUT A or OUT B	I_{OH} = 5mA (5V Vdd) I_{OH} = 1.5mA (3.3V Vdd) TTL Compatible	V_{OH}	2.4			V
OUT A or OUT B	I_{OL} = 5mA (5V Vdd)	V_{OL}			0.5	V
	I_{OL} = 1.5mA (3.3V Vdd)				0.4	
	TTL Compatible					
OUT A or OUT B	I_{OH} = 100µA CMOS Compatible	V_{OH}	V_{DD} – 50mV			V
OUT A or OUT B	I_{OL} = 100µA CMOS Compatible	V_{OH}			V_{SS} + 50mV	V
SUPPLY CURRENT						
V_{DD} Current	Data Rate = 0MHz, A/BIN =open, A/BOUT=open, Vdd = 5.5V or 3.63V	I_{DD}		2.5	5	mA

Notes:
1. Guaranteed by design, not production tested.
2. Current flowing into device is positive. Current flowing out of device is negative. All voltages are with respect to Ground unless otherwise noted.

Table 5 Switching Characteristics

PARAMETER	TEST CONDITION	SYMBOL	MAX	MAX	UNITS
			Vdd 3.3V	Vdd 5V	
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C_L = 50pF	t_{LH}	1000	900	ns
INA/B to OUT A/B Prop Delay	TESTA = TESTB = 0 C_L = 50pF	t_{HL}	1000	900	ns
Matching of t_{LH} and t_{HL}		Dtp	500	500	ns
OUT A/B rise time	10% to 90%, C_L = 50pF	t_r	50	25	ns
OUT A/B fall time	10% to 90%, C_L = 50pF	t_f	50	25	ns
TESTA/B to OUTA/B Prop delay	C_L = 50pF	t_{TOH}	100	60	ns
TESTA/B to OUTA/B Prop delay	C_L = 50pF	t_{TOL}	100	60	ns

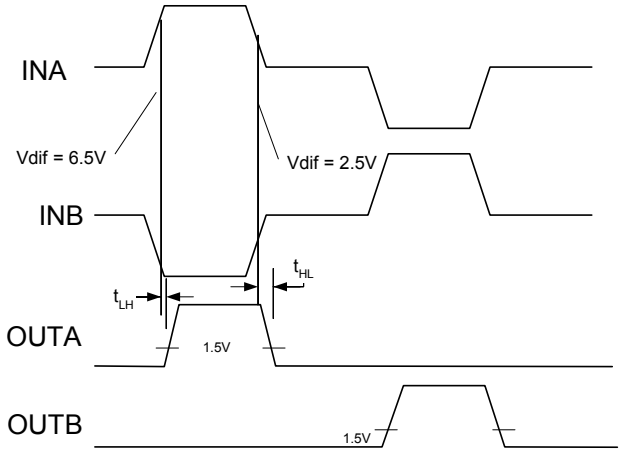


Figure 2 ARINC 429 Input to Logic Output Switching Waveform

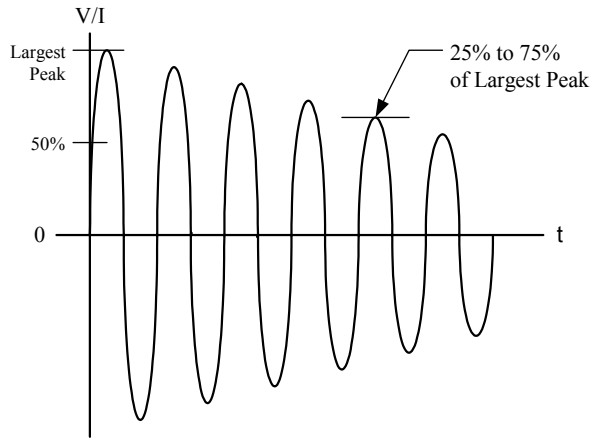


Figure 4 DO160D Lightning Induced Transient Voltage Waveform #3.
Voc = 600V, Isc = 24A, Frequency =1MHz +-20%

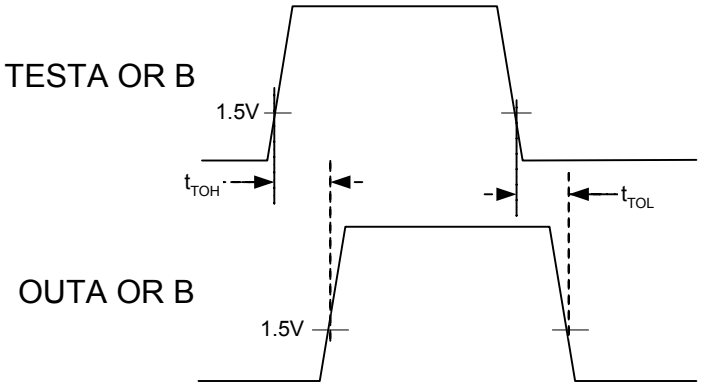


Figure 3 TEST Input to Logic Output Switching Waveform

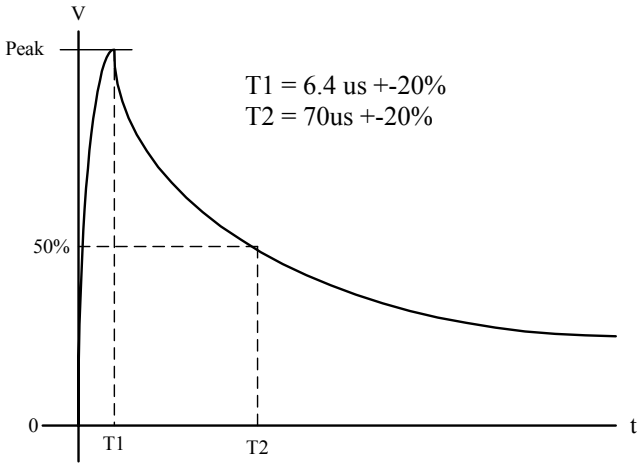


Figure 5 DO160D Lightning Induced Transient Voltage Waveform #4.
Voc = 300V, Isc = 60A

LIGHTNING TRANSIENT NOTES:

1. Voc = Peak Open Circuit Voltage available at the calibration point.
2. Isc = Peak Short Circuit Current available at the calibration point.
3. Amplitude tolerances: +10%, -0%.
4. The ratio of Voc to Isc is the generator source impedance to be used for generating the waveforms.

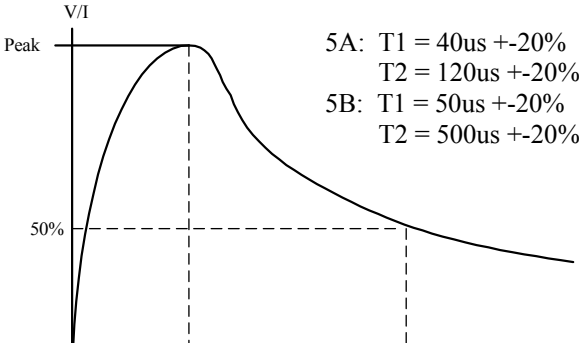


Figure 6 DO160D Lightning Induced Transient Voltage Waveform #5.
Voc = 300V, Isc = 300A

PACKAGE DESCRIPTION

8 Lead NB SOIC

Table 6 - 8 Lead NB SOIC Package Characteristics

Table 6: Package Characteristics Table	
PACKAGE TYPE	**16 Lead SOIC Narrow Body, Green**
REFERENCE	8L NB SOIC G
THERMAL RESISTANCE:	
θ_{JA} (4 layer PCB with Power Planes)	55 °C/W
θ_{JC}	24 °C/W
JEDEC MOISTURE SENSITIVITY LEVEL (MSL)	MSL 1 / 260°C
LEAD FINISH MATERIAL / JEDEC Pb-free CODE	NiPdAu e4
Pb-Free DESIGNATION	RoHS Compliant
JEDEC REFERENCE	MS-012-AC

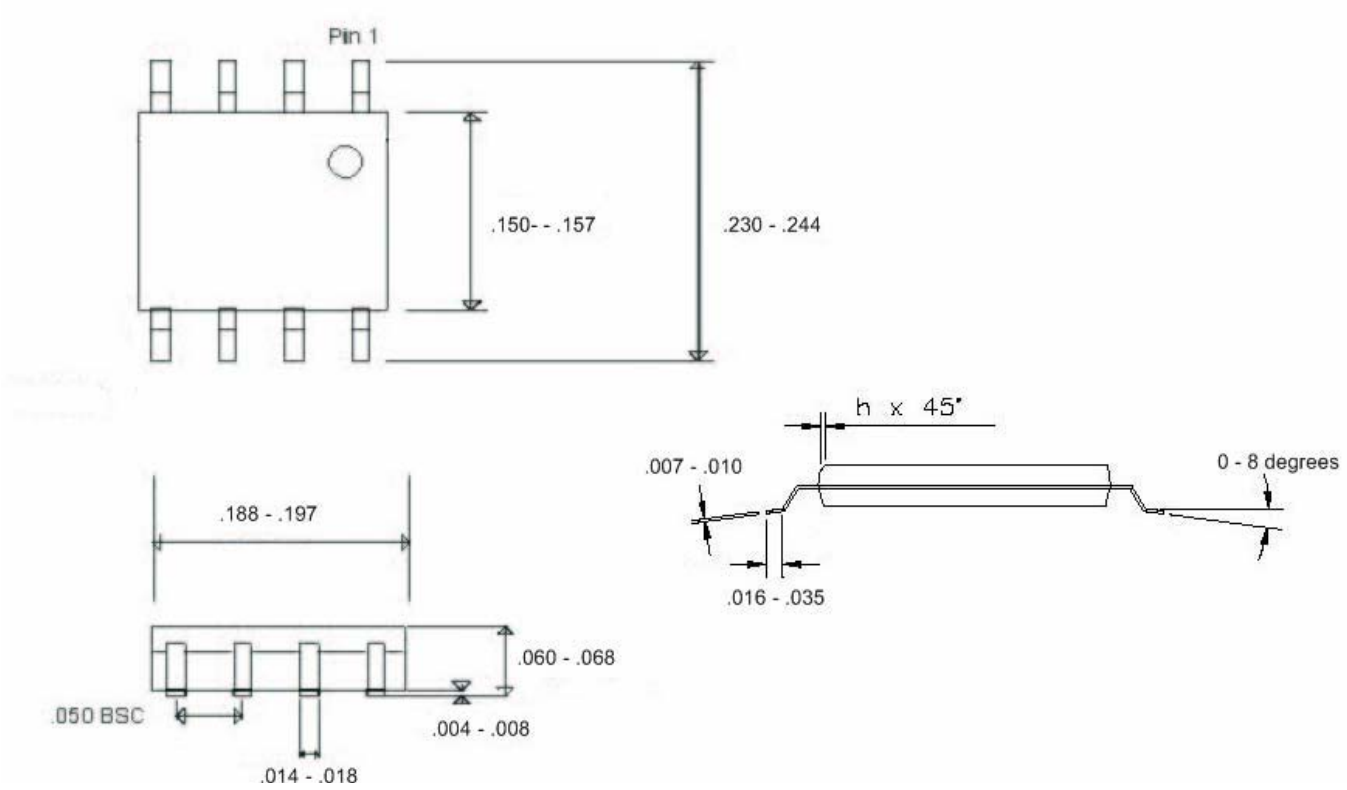


Figure 7 Mechanical Outline, 8L NB SOIC G – Green Package

PROCESS FLOW

Table 7 Process Flow

PROCESS STEP	PLASTIC STANDARD	PLASTIC BURN-IN
PRE-BURN-IN Electrical Test	N/A	YES
BURN IN (1)	N/A	96hrs @ +125 °C
FINAL ELECTRICAL TEST, Room Temperature	100%	100%
FINAL ELECTRICAL TEST, High Temperature	100% @ +85 or +125°C	100% @ +85 or +125°C
FINAL ELECTRICAL TEST, Low Temperature	0.65% AQL @ -55°C	0.65% AQL @ -55°C

NOTES:
1. Burn-in conditions: 125°C, 96 hrs, Vcc = 5.0V Inputs = 0V, Outputs open.

ORDERING INFORMATION

Table 8 Ordering Information

DEI PN	PART MARKING	TEMPERATURE RANGE	BURN-IN	PACKAGE TYPE
DEI1041-SES - G	DEI1041 E4	-55/+85 ºC	NO	8L NB SOIC G
DEI1041-SMS-G	DE1041M E4	-55/+125 ºC	NO	8L NB SOIC G
DEI1041-SMB-G	DE1041B E4	-55/+125 ºC	YES	8L NB SOIC G

NOTES:
1. All packages marked with Lot Code and Date Code. "E4" after Date Code denotes Pb Free category.