GLS85LS1016P / 1032P
Industrial Grade **SATA NANDrive™**

Greenliant Systems Proprietary & Confidential

Data Sheet 01.600
August 2015

Features

- **Industry Standard Serial ATA (SATA) Host Interface**
  - SATA 1.5 Gb/s or SATA 3.0 Gb/s [1)]
  - ATA/ATAPI-8 compliant
  - Supports 48-bit address feature set
- **Performance**
  - Sequential data read - Up to 120 MByte/sec*
  - Sequential data write - Up to 80 MByte/sec*
    * measured using 128 KByte transfer size
- **Power Management**
  - 3.3V and 1.2Vpower supply
  - Host SATA interface power management
  - Immediate disabling of unused circuitry without host intervention
- **Power Specifications** [2)]
  - Active mode:
    855mW typical (GLS85LS1032P)
    590mW typical (GLS85LS1016P)
  - Idle / Standby mode: 210mW typical
  - Sleep mode: 70mW typical
- **Integrated Voltage Detector**
  - Detects supply voltage fluctuations and generates reset during power-up and power-down to prevent inadvertent writes
- **Supports SMART Commands**
- **20-Byte Serial Number**
  - Factory pre-programmed 10-Byte unique ID
  - User-programmable 10-Byte ID
- **Robust Built-in ECC**
- **NAND Configuration**
  - 1 bit per cell (SLC)
- **Industrial Temperature Range**
  - -40°C to 85°C
- **FBGA package**
  - 14.0 mm x 24.0 mm x 1.95 mm, 145-ball, 1.0 mm ball pitch, FZJE
- **All Devices are RoHS Compliant**

1) Current product revision supports SATA Revision 1.x with host transfer rate of up to 1.5 Gb/s (i.e. SATA 1.5 Gb/s). SATA 3.0 Gb/s refers to SATA Revision 2.x and will be supported by our planned future product revisions.
2) For management of the Sleep Mode, refer to "SATA NANDrive Application Design Guide."

Product Description

The GLS85LS1016P / 1032P Industrial Grade SATA NANDrive™ devices (referred to as "SATA NANDrive" in this data sheet) are fully integrated solid state drives. They combine an advanced Greenliant NAND controller and 16 or 32 GByte of NAND flash in a multi-chip package. These products are ideal for embedded and portable applications that require smaller form-factor and more reliable data storage.

SATA-interface solid state mass storage technology is widely used in portable and industrial computers, set-top boxes, multi-functional printers, point-of-sales terminals, video and audio recorders, medical instruments and car infotainment systems.

SATA NANDrive is a single device, solid state drive (SSD) that provides the functionality and compatibility of a complete SATA hard disk drive (HDD) in a 14 mm x 24 mm BGA package for easy, space saving mounting to a system motherboard. These products surpass traditional storage in their small size, security, reliability, ruggedness and low power consumption.

The integrated NAND flash controller with built-in advanced NAND management firmware communicates with the host through the standard SATA protocol. It does not require any additional or proprietary software such as the Flash File System (FFS) and Memory Technology Driver (MTD).

SATA NANDrive is pre-programmed with a 10-Byte unique serial ID and has the option of programming an additional 10-Byte serial ID for even greater system security.

SATA NANDrive's advanced NAND management technology enhances data reliability and security, improves endurance and accurately estimates the remaining life of the NAND flash devices. This innovative technology combines robust NAND controller hardware error correction capabilities with advanced wear-leveling algorithms and bad block management to significantly extend the life of the product.

SATA NANDrive devices are offered in a 145-ball BGA, 1 mm ball pitch package. Refer to Figure 3-1 for the pin assignments.

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Industrial Grade **SATA NANDrive™**

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1.0 GENERAL DESCRIPTION

Each SATA NANDrive contains an integrated SATA NAND flash memory controller and up to eight discrete NAND flash die in a BGA package. Refer to Figure 2-1 for the SATA NANDrive block diagram.

1.1 Optimized SATA NANDrive

The heart of SATA NANDrive is the SATA NAND flash memory controller which translates standard SATA signals into flash media data and control signals. The following components contribute to SATA NANDrive's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU translates SATA commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

SATA NANDrive uses internal DMA allowing instant data transfer from/to buffer to/from flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The PMU controls the power consumption of SATA NANDrive. The PMU dramatically reduces the power consumption of SATA NANDrive by putting the part of the circuitry that is not in operation into sleep mode. [3)]

The Flash File System handles inadvertent power interrupts and has auto-recovery capability to ensure SATA NANDrive firmware integrity. For regular power management, the host must send a STANDBY_IMMEDIATE (E0h), IDLE_IMMEDIATE (E1h), STANDBY (E2h) or IDLE (E3h) command and wait for command ready before powering down SATA NANDrive.

3) For management of the Sleep Mode, refer to "SATA NANDrive Application Design Guide."

1.1.4 Embedded Flash File System

The embedded flash file system is an integral part of SATA NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads
2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media
3. Keeps track of data file structures
4. Manages system security for the selected protection zones

1.1.5 Error Correction Code (ECC)

High performance is achieved through optimized hardware error detection and correction.

1.1.6 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for error reporting. During the product development stage, it is recommended to provide the SCI port on the PCB to aid in design validation.

1.1.7 Multi-tasking Interface

The multi-tasking interface enables fast, sequential write performance by allowing concurrent Read, Program and Erase operations to multiple flash media.

1.2 SMT Reflow Consideration

The SATA NANDrive family utilizes standard NAND flash for data storage. Because the high temperature in a surface-mount soldering reflow process may alter the content on NAND flash, it is recommended to program SATA NANDrive after the reflow process.

1.3 Advanced NAND Management

SATA NANDrive's integrated controller uses advanced wear-leveling algorithms to substantially increase the longevity of NAND flash media. Wear caused by data writes is evenly distributed in all or select blocks in the device that prevents "hot spots" in locations that are programmed and erased extensively. This effective wear-leveling technique results in optimized device endurance, enhanced data retention and higher reliability required by long-life applications.

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2.0 FUNCTIONAL BLOCKS

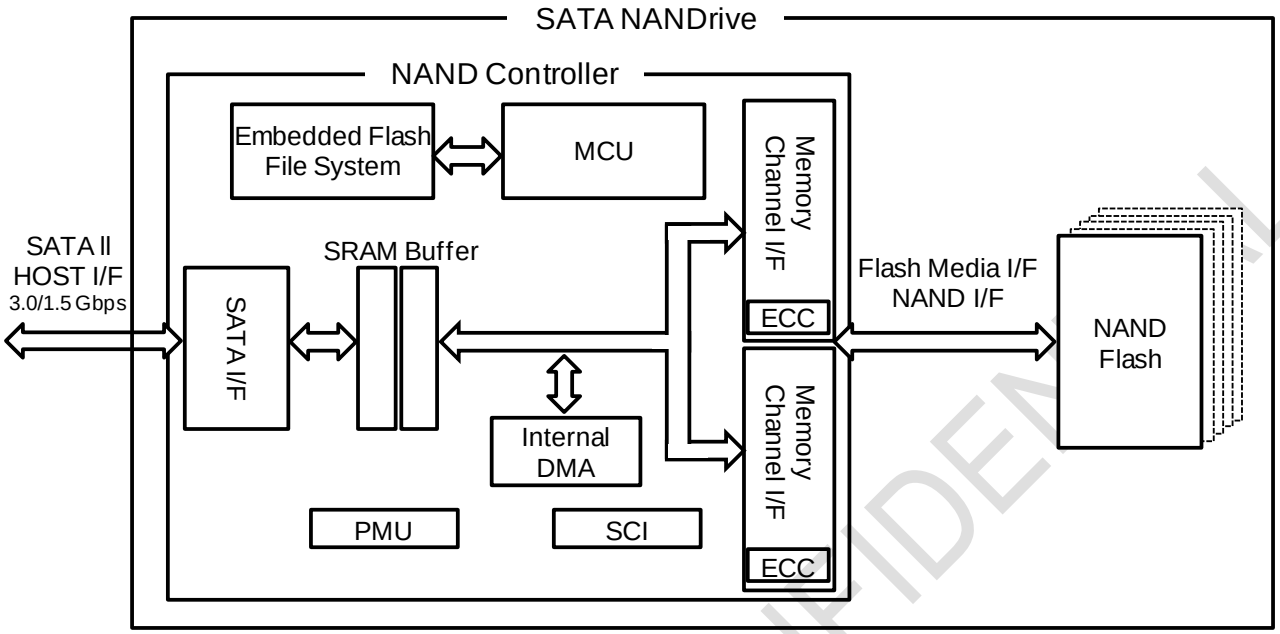

Figure 2-1: SATA NANDrive Block Diagram

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output or Input/Output.

TOP VIEW (balls facing down)

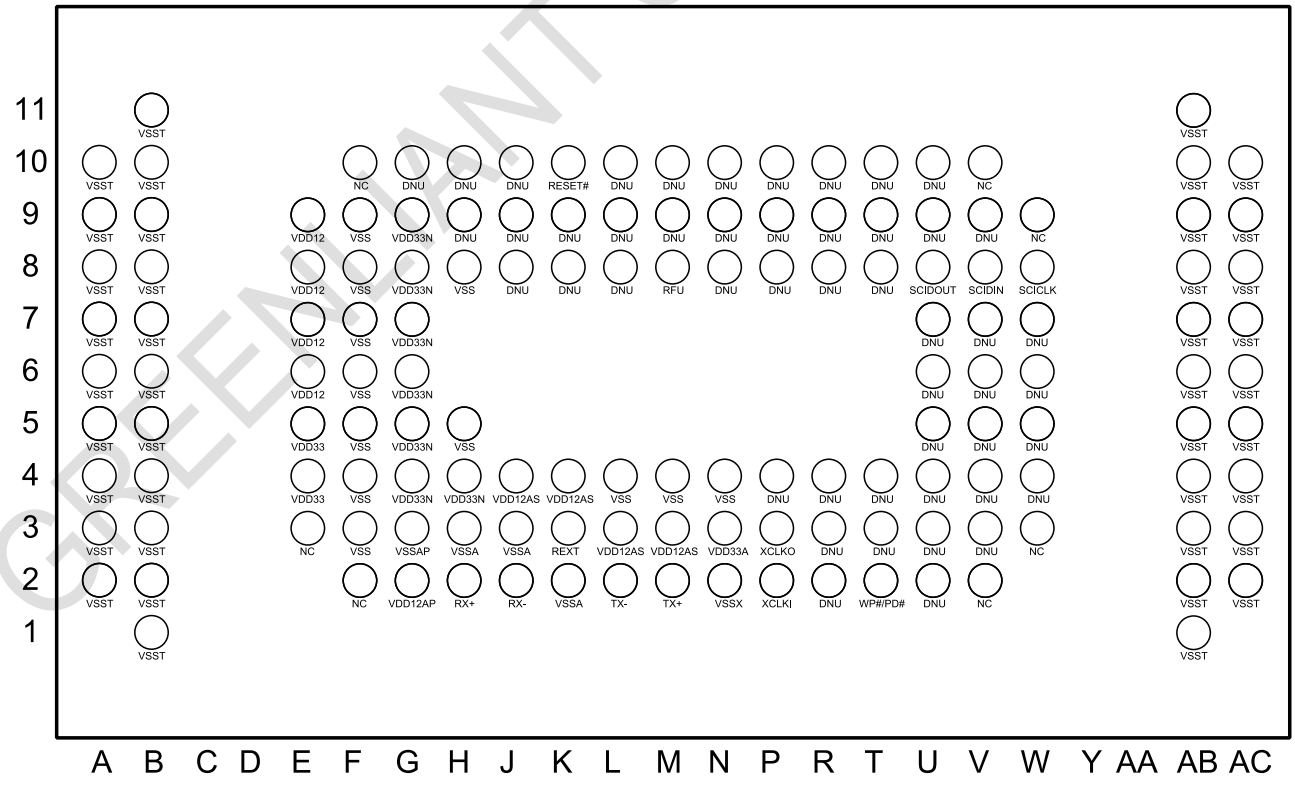

Figure 3-1: Pin Assignments for 145-Ball BGA

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Table 3-1: Pin Assignments

Symbol	Ball No.	Ball Type	IO Type	Name and Functions
Host Side Interface				
RX+	H2	I	I3	Analog Differential Input (+)
RX-	J2	I	I3	Analog Differential Input (-)
TX+	M2	O	O3	Analog Differential Output (+)
TX-	L2	O	O3	Analog Differential Output(-)
Serial Communication Interface (SCI)				
$SCID_{IN}$	V8	I	I2U	SCI port data input
$SCID_{OUT}$	U8	O	O1	SCI port data output. No external pull-up or pull-down resistor should connect to this signal.
SCICLK	W8	I	I2D	SCI port clock
Miscellaneous				
RFU	M8			Reserved for Future Use
Rext	K3	I	I3	External Resistor, 1Kohms (1%) connected to GND
RESET#	K10	I	I2U	This input is the active low hardware reset from host.
WP#/PD#	T2 [4)]	I	I2U	The WP#/PD# can be used for either the Write Protect mode or Power Down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
XCLKI [5)]	P2	I	XI	External clock source input for main clock; 25MHz crystal, need external 20pf capacitor to ground
XCLKO [5)]	P3	O	XO	External clock source output for main clock; 25MHz crystal, need external 20pf capacitor to ground
NC	E3, F2, F10, V2, V10, W3, W9			No connect
DNU	G10, H9, H10, J8, J9, J10, K8, K9, L8, L9, L10, M9, M10, N8, N9, N10, P4, P8, P9, P10, R2, R3, R4, R8, R9, R10, T3, T4, T8, T9, T10, U2, U3, U4, U5, U6, U7, U9, U10, V3, V4, V5, V6, V7, V9, W4, W5, W6, W7			Do Not Use. All these pins should not be connected.
Power and Ground				
V_{DD33}	E4, E5	Digital PWR		Supply voltage 3.3V
VDD33A	N3	Analog PWR		
V_{DD33N}	G4, G5, G6, G7, G8, G9, H4	Digital PWR		
V_{DD12}	E6, E7, E8, E9	Digital PWR		Supply voltage 1.2V
V_{DD12AS}	J4, K4, L3, M3	Analog PWR		Analog supply voltage 1.2V (200mA max. total for both 1.2V analog power rails, VDD12AS and VDD12AP)
V_{DD12AP}	G2	Analog PWR		
V_{SS}	F3, F4, F5, F6, F7, F8, F9, H5, H8, L4, M4, N4	Digital GND		Digital ground
VSSX	N2	Analog GND		Analog ground
V_{SST}	A2, A3, A4, A5, A6, A7, A8, A9, A10, B1, B2, B3, B4, B5, B6, B7, B8, B9, B10, B11, AB1, AB2, AB3, AB4, AB5, AB6, AB7, AB8, AB9, AB10, AB11, AC2, AC3, AC4, AC5, AC6, AC7, AC8, AC9, AC10	GND		Connected to PCB ground plane for thermal dissipation. Not connected to any internal signal.
V_{SSA}	H3, J3, K2	Analog GND		Analog ground
V_{SSAP}	G3			Analog ground

Table 3-2: I/O Type

I/O Type	Description
I3	Analog Input
O3	Analog Output
I2D	Input with Pull-down
I2U	Input with Pull-up
O1	Output
XI	Crystal Clock Input
XO	Crystal Clock Output

4) The command to configure the T2 pin in either PD# or WP# is prepared by the vendor-unique command. Please ask your Greenliant contact for details on the SMART command specification.

5) It is recommended to use a crystal as the clock input source. When using XCLKI and XCLKO signals with a crystal, it is required to install a 1Mohms (1%) external resistor across the XCLKI and XCLKO signals. No external resistor is required if an oscillator or system clock is used as the clock input source and only connected to XCLKI.

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4.0 KEY PARAMETERS

Table 4-1 shows the SATA NANDrive default capacity. At production time, the manufacturer can change the default settings in the drive ID table. Please contact Greenliant for details.

Table 4-1: Default SATA NANDrive Settings

Capacity	Total Bytes	Max LBA (Logical Block Addressing)
16 GByte	16,013,942,784	31,277,232
32 GByte	32,017,047,552	62,533,296

Table 4-2: Sustained Performance[6)]

Product	Product Revision	Write Performance	Read Performance
GLS85LS1016P-S-I-FZJE-ND101	CC0	Up to 55 MByte/sec	Up to 70 MByte/sec
GLS85LS1016P-S-I-FZJE-ND104	CC1	Up to 55 MByte/sec	Up to 70 MByte/sec
GLS85LS1032P-S-I-FZJE-ND101	CC0	Up to 80 MByte/sec	Up to 120 MByte/sec
GLS85LS1032P-S-I-FZJE-ND104	CC1	Up to 80 MByte/sec	Up to 120 MByte/sec

6) Actual performance may vary based on the application, host device and operating system.

Table 4-3: Total NAND Program / Erase (P/E) Cycles[7)]

Product	Product Revision	Total P/E Cycles Per Block
16/ 32 GByte	CC0 / CC1	60,000 (Typical)

7) This NAND P/E cycling reference does not account for the benefits of NANDrive's integrated controller, which uses advanced wear-leveling algorithms to substantially increase the longevity of NAND flash media

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5.0 CONFIGURABLE WRITE PROTECT / POWER-DOWN MODES [2)]

The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Either mode can be selected through the host command, Set-WP#/PD#-Mode.

Once the mode is set with this command, the device will stay in the configured mode until the next time this command is issued. Power-off or reset will not change the configured mode.

5.1 Write Protect Mode [2)]

When the device is configured in the Write Protect mode, the WP#/PD# pin offers extended data protection. This feature can be either selected through a jumper or host logic to protect the stored data from inadvertent system writes or erases, and viruses. The Write Protect feature protects the full address space of the data stored on the flash media.

In the Write Protect mode, the WP#/PD# pin should be asserted prior to issuing the destructive commands: Erase- Sector, Format-Track, Write-DMA, Write-Multiple or Write-Sector(s). This will force SATA NANDrive to reject any destructive commands from the SATA interface. All destructive commands will return 51H in the Status register and 04H in the Error register signifying an invalid command. All non-destructive commands will be executed normally.

5.2 Power-down Mode [2)]

When the device is configured in the Power-down mode, if the WP#/PD# pin is asserted during a command, SATA NANDrive stops the ongoing command and immediately enters Power-down mode. Afterwards, the device will not accept any other commands. Only a Power-on Reset (POR) or hardware reset will bring the device to normal operation with the WP#/PD# pin de-asserted.

A filter algorithm is built to the WP#/PD# pin to avoid any signal noise or glitch that will cause SATA NANDrive to inadvertently enter Power-down mode. To ensure the device is entering Power-down mode properly, it is recommended that WP#/PD# pin has to be asserted for at least 5µs. Refer to application note “Power Interrupt Protection Design Consideration” for more details.

6.0 POWER-ON INITIALIZATION

SATA NANDrive is self-initialized during the first power-up. As soon as the power is applied to SATA NANDrive it reports busy for typically up to seven seconds while performing search for bad blocks and low-level format. This initialization is a one-time event.

During the first self-initialization, the SATA NANDrive firmware scans all connected flash media devices and reads their device ID. If the device ID matches the listed flash media devices, SATA NANDrive performs drive recognition based on the algorithm provided by the flash media suppliers, including setting up the bad block table, executing all the necessary handshaking routines for flash media support and performing the low-level format.

7.0 DEBUGGING/MONITORING TOOL

7.1 Manufacturing Debug Tool

Greenliant provides a Linux/Windows/DOS-based executable file that allows users to send manufacturer interface commands to the device via SATA host interface and can be used as a debugging utility. Refer to application note “Windows PT2 User Guide” for more details.

7.2 Serial Communication Interface (SCI)

For additional manufacturing flexibility, the SCI bus can be used for error reporting. The SCI consists of 3 active signals: SCIDOUT, SCIDIN, and SCICLK. Always provide access to the SCI port in the PCB design to aid in design validation. Refer to application note “Serial Communication Interface (SCI)” for more details.

8.0 DATA SECURITY

For applications where data security is essential, SATA NANDrive with advanced NAND management technology offers two additional protection features - protection zones and password protection.

Protection Zones - Up to four independent protection zones can be enabled as either Read-only or Hidden (Read/Write protected). If the zones are not enabled, the data is unprotected (default configuration).

Password Protection - Requires a customer-unique password to access information within the protected zones.

For information on other NANDrive features, refer to application notes in Table 12-4.

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9.0 POWER-ON AND BROWN-OUT RESET CHARACTERISTICS

Figure 9-1 and Table 9-1 detail the Power-on and Brown-out reset characteristics of SATA NANDrive.

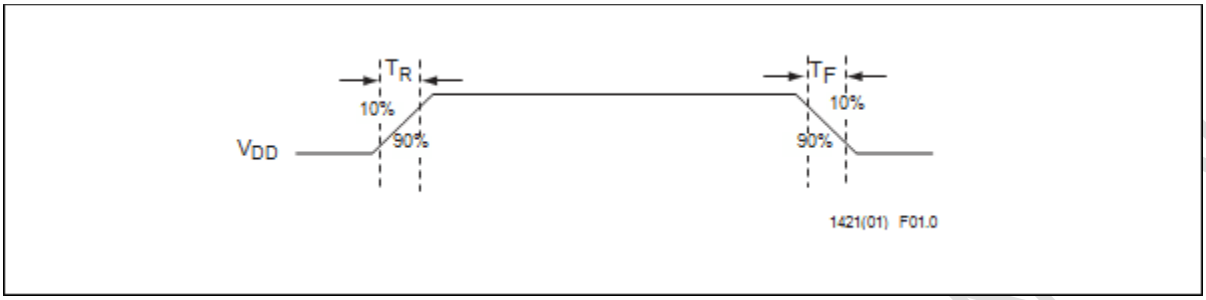

Figure 9-1: Power-on and Brown-out Reset Timing

Table 9-1: Power-on and Brown-out Reset Timing

Item	Symbol	Min	Max	Units
V_{DD} Rise Time	T_R	0	250	ms
V_{DD} Fall Time [8)]	T_F	0	250	ms

8) This is a case that NANDrive has entered a non-operating state after receiving and finishing STANDBY_IMMEDIATE (E0h), IDLE_IMMEDIATE (E1h), STANDBY (E2h) or IDLE (E3h) commands prior to power-off as recommended in ATA standard specification. For other cases, refer to application note "NANDrive Power Interrupt Protection Design Considerations."

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10.0 SOFTWARE INTERFACE

10.1 48-bit Address Feature Set

The 48-bit address feature set allows SATA NANDrive to have a capacity of up to 281,474,976,710,656 sectors, or 144,115,188,075,855,872 Bytes. This feature also increases the allowable sector count to 16 bits, which means more sectors can be transferred by a single command. The Features, Sector Count, LBA Low, LBA Mid and LBA High registers are each two Bytes deep. When SATA NANDrive writes to one of these registers, it writes the new content to the "most recently written" location and moves the data previously in that location to the "previous content" section of the register. The address used by SATA NANDrive during 48-bit addressing is shown in the following table.

Table 10-1: 48-bit Address

Register	Most Recently Written	Previous Content
Features	N/A	N/A
Sector Count	Sector Count [7:0]	Sector Count [15:8]
LBA Low	LBA [7:0]	LBA [31:24]
LBA Mid	LBA [15:8]	LBA [39:32]
LBA High	LBA [23:16]	LBA [47:40]
Drive/Head	Bit 7 and 5 are obsolete. Set LBA to '1', the Dev bit to indicate the selected device. Bit 3 to bit 0 are reserved	N/A

10.2 28-bit Address Feature Set

The 28-bit address feature set is shown in the following table.

Table 10-2: 28-bit Address

Register	Most Recently Written	Previous Content
Features	N/A	N/A
Sector Count	Sector Count [7:0]	N/A
LBA Low	LBA [7:0]	N/A
LBA Mid	LBA [15:8]	N/A
LBA High	LBA [23:16]	N/A
Drive/Head	Bit 7 and 5 are obsolete. Set LBA to '1', the Dev bit to indicate the selected device. Bit 3 to bit 0 specify LBA [27:24].	N/A

10.3 Frame Information Structure (FIS) Definitions and Protocol

This section defines the Frame Information Structure (FIS) and the protocol used to address them. The implementation of FIS support is shown in the following table.

Table 10-3: FIS Type Value Assignments

Type Field Value	Description	Direction
27h	Register	Host to Device
34h	Register	Device to Host
39h	DMA Activate	Device to Host
41h	DMA Setup	Bi-directional
46h	Data	Bi-directional
58h	BIST Activate	Bi-directional
5Fh	PIO Setup	Device to Host
A1h	Set Device Bits	Device to Host

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10.4 Command Description

This section defines the software requirements and the format of the commands the host sends to SATA NANDrive. Commands are issued to SATA NANDrive by loading the required registers in the command block with the supplied parameters, and then writing the command code to the Command register.

Table 10-4: ATA Support Command Set

Command	Code	Command	Code
NOP	00h	Get Media Status	DAh
Device Reset	08h	Standby Immediate	E0h
Data Set Management	06h	Idle Immediate	E1h
Read Sector(s)	20h	Standby	E2h
Read Sector(s) EXT	24h	Idle	E3h
Read DMA EXT	25h	Read Buffer	E4h
Read Native Max Address EXT	27h	Check Power Mode	E5h
Read Multiple EXT	29h	Set Sleep Mode	E6h
Read Log EXT	2Fh	Flush Cache	E7h
Write Sector(s)	30h	Write Buffer	E8h
Write Sector(s) EXT	34h	Flush Cache EXT	EAh
Write DMA EXT	35h	Identify Drive	ECh
Set Max Address EXT	37h	Set Features	EFh
Write Multiple EXT	39h	Security Set Password	F1h
Read Verify Sector(s)	40h	Security Unlock	F2h
Read Verify Sector(s) EXT	42h	Security Erase Prepare	F3h
Execute Device Diagnostic	90h	Security Erase Unit	F4h
Packet	A0h	Security Freeze Lock	F5h
SMART [9)]	B0h	Security Disable Password	F6h
Read Multiple	C4h	Read Native Max Address	F8h
Write Multiple	C5h	Set Max Set Password	F9h/01h
Set Multiple Mode	C6h	Set Max Lock	F9h/02h
Read DMA	C8h	Set Max Unlock	F9h/03h
Write DMA	CAh	Set Max Freeze Lock	F9h/04h
Obsolete CMD by the ATA/ATAPI specifications			
Recalibrate	10h	Standby	96h
Read Sectors Without Retry	21h	Idle	97h
Write Sectors Without Retry	31h	Check Power Mode	98h
Read Verify Sectors Without Retry	41h	Sleep	99h
Seek	70h	Read DMA Without Retry	C9h
Initialize Device Parameters	91h	Write DMA Without Retry	CBh
Standby Immediate	94h	Set Max Address	F9h/00h
Idle Immediate	95h		

9) Please ask your Greenliant contact about SMART command support.

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10.4.1 Identify-Drive – ECh

The Identify-Drive command enables the host to receive parameter information from SATA NANDrive. This command has the same protocol as the Read-Sector(s) command. The parameter Words in the buffer have the arrangement and meanings defined in the following table. All reserved bits or Words are zero. The following table gives the definition for each field in the Identify-Drive information.

Table 10-5: Identify-Drive Information (1 of 2)

Word Address	Total Bytes	Default Value	Data Field Type Information
0	2	427Ah	General configuration bit
1	2	xxxxh [10)]	Obsolete
2	2	0000h	Specific configuration
3	2	xxxxh [10)]	Obsolete
4-5	4	0000h-0000h	Retired
6	2	xxxxh [10)]	Obsolete
7-8	4	xxxxh [10)]	Reserved for the CompactFlash™ Association
9	2	0000h	Retired
10-14	10	eeeeh [13)]	User-programmable serial number in ASCII
15-19	10	ddddh [14)]	Greenliant preset unique ID in ASCII
20-21	4	0003h-8000h	Retired
22	2	0053h	Obsolete
23-26	8	aaaah [15)]	Firmware revision in ASCII
27-46	40	cccch [16)]	User definable model number
47	2	8001h	Maximum number of sectors on Read/Write-Multiple command
48	2	0000h	Trusted Computing feature set options
49	2	0F00h	Capabilities
50	2	4000h	Capabilities
51-52	4	xxxxh [10)]	Obsolete
53	2	0007h	Field Validity
54-58	10	xxxxh [10)]	Obsolete
59	2	0100h	Multiple sector setting is valid, one sector shall be transferred per interrupt on R/W Multiple command
60-61	4	nnnnh [12)]	Total number of user addressable logical sectors for 28-bit commands
62	2	xxxxh [10)]	Obsolete
63	2	0007h	DMA data transfer is supported in Device
64	2	0003h	Advanced PIO Transfer mode supported
65	2	0078h	Minimum Multiword DMA transfer cycle time per Word
66	2	0078h	Manufacturer's recommended Multiword DMA transfer cycle time
67	2	0078h	Minimum PIO transfer cycle time without flow control
68	2	0078h	Minimum PIO transfer cycle time with IORDY flow control
69	2	0000h	Reserved
70	2	0000h	Reserved
71-74	8	xxxxh [10)]	Reserved for the IDENTIFY PACKET DEVICE command
75	2	0000h	Queue length
76	2	0202h	Serial ATA Capabilities
77	2	0000h	Serial ATA Additional Capabilities: SATA Gen1 1.5 Gbit/sec / Gen2 3.0 Gbit/sec
78	2	0048h	Serial ATA features supported
79	2	0040h	Serial ATA features enabled
80	2	01F0h	Major Version Number. Bit1~3 Obsolete
81	2	0000h	Minor version number
82	2	302Bh	Commands and feature sets supported
83	2	7408h	Commands and feature sets supported
84	2	4000h	Commands and feature sets supported
85	2	3008h	Commands and feature sets supported or enabled
86	2	3408h	Commands and feature sets supported or enabled
87	2	4000h	Commands and feature sets supported or enabled
88	2	407Fh	UDMA modes
89	2	000Fh	Time required for Normal Erase mode command
90	2	0000h	Time required for Enhanced Erase mode command
91	2	0080h	Current APM level value

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Table 10-5: Identify-Drive Information (2 of 2)

Word Address	Total Bytes	Default Value	Data Field Type Information
92	2	FFFEh	Master Password Identifier
93	2	0000h	Hardware reset result
94	2	0000h	Current AAM value
95	2	0000h	Stream minimum request size
96	2	0000h	Streaming Transfer Time –DMA
97	2	0000h	Streaming Access Latency – DMA and PIO
98-99	4	0000h-0000h	Streaming Performance Granularity (DWord)
100-103	8	nnnnh [12)]	Total # of user addressable logical sectors for the 48-bit Add feature set (QWord)
104	2	0000h	Streaming Transfer time - PIO
105	2	0001h	Maximum number of 512-Byte blocks of LBA Range Entries
106	2	0000h	Physical sector size / logical sector size
107	2	0000h	Inter-seek delay for ISO 7779 standard acoustic testing
108	2	0000h	NAA / IEEE OUI
109	2	0000h	IEEE / OUI
110	2	0000h	Unique ID
111	2	0000h	Unique ID
112-115	8	xxxxh [10)]	Reserved for word wide name extension to 128 bits
116	2	0000h	Reserved for TLC
117-118	4	bbbbh [11)]	Logical sector size (DWord)
119	2	0000h	Commands and feature sets supported
120	2	0000h	Commands and feature sets supported or enabled
121-126	10	xxxxh [10)]	Reserved for expanded supported and enabled settings
127	2	0000h	Obsolete
128	2	0001h	Security status
129-159	62	xxxxh [10)]	Vendor specific
160	2	0000h	CFA power mode
161-167	30	xxxxh [10)]	Reserved for the CompactFlash™ Association
169	2	0001h	01 = the Trim bit in the DATA SET MANAGEMENT is supported
176-205	60	xxxxh [10)]	Current media serial number
206	2	0000h	SCT command transport
207-208	4	xxxxh [10)]	Reserved for CE-ATA
209	2	0000h	Alignment of logical blocks within a physical block
210-211	4	0000h-0000h	Write-Read-Verify sector count mode 3 (DWord)
212-213	4	0000h-0000h	Write-Read-Verify sector count mode 2 (DWord)
214	2	0000h	NV cache capabilities
215-216	4	0000h-0000h	NV cache size in logical blocks (DWord)
217	2	0001h	Nominal media rotation rate
218	2	0000h	Reserved
219	2	0000h	NV cache options
220	2	0000h	Write-Read-Verify feature set current mode
221	2	0000h	Reserved
222	2	0000h	Transport major version number
223	2	0000h	Transport minor version number
224-233	20	xxxxh [10)]	Reserved for CE-ATA
234	2	0000h	Min # of 512-Byte data block per DOWNLOAD MICROCODE CMD for mode 03h
235	2	0000h	Max # of 512-Byte data block per DOWNLOAD MICROCODE CMD for mode 03h
236-254	38	xxxxh [10)]	Reserved
255	2	ddddh [14)]	Integrity Word

10) xxxx - Don't care. This field is subject to change by the host or the device.
11) bbbb - default value set by the controller. The selections could be user programmable.
12) n - calculated data based on product configuration
13) eeee - the default value is '0000000000'
14) dddd - unique number of each device
15) aaaa - any unique Greenliant firmware revision
16) cccc - the default value is "85LS1XXXP SATA NANDrive" where xxx is the flash drive capacity. The user has an option to change the model number during manufacturing.

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Word 0: General Configuration Bit

Bit 15 shall be cleared to zero. Bits (7:6) are obsolete. If bit 2 of Word 0 is set to one, then the content of the IDENTIFY DEVICE data is incomplete.

Word 1: Obsolete

Word 2: Specific Configuration

Word 3: Obsolete

Word 4-5: Retired

Word 6: Obsolete

Word 7-8: Reserved for assignment by the CompactFlash™ Association

Word 9: Retired

Word 10-19: Serial Number

This field contains the serial number of the device. The content of this field is an ATA string of user-programmable 20 bytes. The contents of this field are right justified and padded with spaces (20h).

Word 20-21: Retired

Word 22: Obsolete

Word 23-26: Firmware Revision

This field contains the firmware revision for this product.

Word 27-46: Model Number

This field contains the model number for this product.

Word 47: READ/WRITE MULTIPLE Support

Bit	Function
15-8	80h (Fixed)
7-0	The maximum number of logical sectors that can be read or written per interrupt using the READ MULTIPLE or WRITE MULTIPLE command.

Word 48: Trusted Computing Feature Set Options

The Trusted Computing feature set is supported by setting the value to one.

Word 49: Capabilities

Bit	Function
13	Standby Timer for the Sleep Mode 1: Standby timer values as specified in this standard are supported 0: Standby timer values shall be managed by the device
11	IORDY Support 1: Supports PIO Mode-6
10	IORDY Disable 1: IORDY may be disabled
9	LBA Support 1: Supports LBA mode addressing
8	DMA Support 1: Supports DMA mode

Word 50: Capabilities

Bit	Function
14	Shall be set to '1'

Words 51-52: Obsolete

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Word 53: Field Validity

Bit	Function
2	1: word 88 is valid to support UDMA data transfer
1	1: words 64-70 are valid to support respective PIO modes.

Words 54-58: Obsolete

Word 59: Multiple Sector Setting

If bit 8 is set to one, then bits (7:0) indicate the number of logical sectors that will be transferred for a READ MULTIPLE command or a WRITE MULTIPLE command.

Words 60-61: Total number of user addressable logical sectors for 28-bit commands

This field contains a value that is one greater than the maximum user addressable LBA. The maximum value that shall be placed in this field is 0FFF_FFFFh. If this field contains 0FFF_FFFFh and the device has user addressable LBAs greater than or equal to 0FFF_FFFFh, then Words 100 -103 contain the maximum user addressable LBA.

Word 62: Obsolete

Word 63: Multiword DMA Transfer

This field identifies the Multiword DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is enabled, then no Multiword DMA mode shall be enabled and vice versa.

Bit	Function
15-11	Reserved
10	Multiword DMA mode 2 selected 1: Multiword DMA mode 2 is selected and bits 8 and 9 are cleared to 0 0: Multiword DMA mode 2 is not selected
9	Multiword DMA mode 1 selected 1: Multiword DMA mode 1 is selected and bits 8 and 10 are cleared to 0 0: Multiword DMA mode 1 is not selected
8	Multiword DMA mode 0 selected 1: Multiword DMA mode 2 is selected and bits 9 and 10 are cleared to 0 0: Multiword DMA mode 2 is not selected
7-3	Reserved
2	Multiword DMA mode 2 supported 1: Multiword DMA mode 2 and below are supported and bits 0 and 1 are set to 1
1	Multiword DMA mode 1 supported 1: Multiword DMA mode 1 and below are supported
0	Multiword DMA mode 0 supported 1: Multiword DMA mode 0 is supported

Word 64: PIO Transfer Modes Supported

Bits (7:0) are defined as the PIO data and register transfer supported field. If this field is supported, bit 1 of Word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate the PIO modes the device is capable of supporting. Of these bits, bits (7:2) are reserved for future PIO modes.

Bit	Function
1	1: Device supports PIO Mode 6
0	1: Device supports PIO Mode 5

Word 65: Minimum Multiword DMA Transfer Cycle Time per Word

This field defines the minimum Multiword DMA transfer cycle time per Word. This field defines, in nanoseconds, the minimum cycle time that the device supports when performing Multiword DMA transfers on a per Word basis. This field is set to 120ns for this product.

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Word 66: Device Recommended Multiword DMA Transfer Cycle Time

This field contains the Multiword DMA transfer cycle time recommended by the device in nanoseconds. This field shall be set to 78h to indicate 120ns.

Word 67: Minimum PIO Transfer Cycle Time without IORDY Flow Control

This field defines, in ns, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of IORDY flow control. This field shall be set to indicate 120ns in this product.

Word 68: Minimum PIO Transfer Cycle Time with IORDY Flow Control

This field defines, in ns, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control. This field shall be set to indicate 120ns in this product.

Words 69-74: Reserved

Word 75: Queue Depth

Bits (4:0) of Word 75 indicate the maximum queue depth supported by the device. The queue depth includes all commands for which command acceptance has occurred and command completion has not occurred. The value in this field equals (maximum queue depth - 1). If bit 1 of Word 83 is cleared to zero indicating that the device does not support TCQ feature set commands, or if bit 6 of Word 76 is cleared to zero indicating that the device does not support NCQ feature set commands, the value in this field shall be zero. Support of this Word is mandatory if the TCQ or NCQ feature sets are supported.

Word 76: Serial ATA Capabilities

Word 76 shall not set to 0000h or FFFFh to claim compliance with the Serial ATA specification. Bits (15:11) of Word 76 are reserved for Serial ATA.

Bit	Function
10	0: not supporting the SATA PHY Event Counters log
9	1: supports Partial and Slumber interface power management states when initiated by the host
8	0: not supporting NCQ feature set
7:3	reserved for Serial ATA
2	0: not supporting Gen2 signaling rate of 3.0Gbit/sec
1	1: supports Gen1 signaling rate of 1.5Gbit/sec
0	shall be cleared to zero

Word 77: Reserved for Serial ATA

Word 77 is reserved for future Serial ATA definition and shall be cleared to zero.

Word 78: Serial ATA Features Supported

If Word 76 is not 0000h or FFFFh, Word 78 reports the optional features supported by the device.

Word 79: Serial ATA Features Enabled

If Word 76 is not 0000h or FFFFh, Word 79 reports which optional features supported by the device are enabled. This word shall be supported if optional Word 78 is supported.

Word 80: Major Version Number

Bit	Function
8	1: Support ATA8-ACS
7	1: Support ATA/ATAPI-7
6	1: Support ATA/ATAPI-6
5	1: Support ATA/ATAPI-5
4	1: Support ATA/ATAPI-4

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Word 81: Minor Version Number

This field indicates the version of the standard that guided the implementation.

Table 10-6: Minor Version Number

Value	Minor Version
0000h	Minor version is not reported
0018h	ATA/ATAPI-6 T13 1410D version 0
0019h	ATA/ATAPI-6 T13 1410D version 3a
001Ah	ATA/ATAPI-7 T13 1532D version 1
001Bh	ATA/ATAPI-6 T13 1410D version 2
001Ch	ATA/ATAPI-6 T13 1410D version 1
001Dh	ATA/ATAPI-7 published ANSI INCITS 397-2005
001Eh	ATA/ATAPI-7 T13 1532D version 0
0021h	ATA/ATAPI-7 T13 1532D version 4a
0022h	ATA/ATAPI-6 published, ANSI INCITS 361-2002
0027h	ATA8-ACS version 3c
0029h	ATA8-ACS version 4
0033h	ATA8-ACS version 3e
0039h	ATA8-ACS version 4c
0042h	ATA8-ACS version 3f
0052h	ATA8-ACS version 3b
0107h	ATA8-ACS version 2d
FFFFh	Minor version is not reported

Words 82-84, 119: Commands and Feature Sets Supported

Words 82, 83, and 84 indicate the features and command sets supported. A value of 706BH is reported.

Word 82

Bit	Function
15	0: Obsolete
14	0: not supporting NOP command
13	1: READ BUFFER command is supported
12	1: WRITE BUFFER command is supported
11	0: Obsolete
10	0: not supporting Host Protected Area feature set
9	0: not supporting DEVICE RESET command
8	0: not supporting SERVICE interrupt
7	0: not supporting Release interrupt
6	0: not supporting Read Look-ahead
5	1: Write cache is supported
4	0: indicate that the PACKET Command feature set is not supported
3	1: Power Management feature set is supported
2	0: Obsolete (Fixed)
1	1: Security Mode feature set is supported
0	1: SMART feature set is supported

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Word 83

Bit	Function
14	Shall be set to 1
13	1: FLUSH CACHE EXT command is supported
12	Shall be set to 1 to indicate mandatory FLUSH CACHE command is supported
11	0: not supporting DCO feature set
10	1: 48-bit Address feature set is supported
9	0: not supporting AAM (Automatic Acoustic Management) feature set
8	0: not supporting Host Protected Area Security Extensions
7	0: Reserved for Address Offset Reserved Area Boot Method
6	0: SET FEATURES is required to spin-up after power-up
5	0: not supporting PUIS feature set
4	0: Obsolete
3	1: APM feature set is supported
2	0: not supporting CFA feature set
1	0: not supporting TCQ feature set
0	0: not supporting DOWNLOAD MICROCODE command

Word 84

Bit	Function
14	Shall be set to 1
13	1: IDLE IMMEDIATE command is supported
12	reserved for TLC
11	reserved for TLC
10	Obsolete
9	Obsolete
8	shall be set to 1 to indicate the mandatory World Wide Name in Words 108-111 is supported
7	1: WRITE DMA QUEUED FUA EXT command is supported
6	1: WRITE DMA FUA EXT command and WRITE MULTIPLE FUA EXT command is supported
5	1: GPL feature set is supported
4	1: Streaming feature set is supported
3	1: Media Card Pass Through Command feature set is supported
2	1: media serial number field in Words 176-205 is supported
1	1: SMART self-test is supported. This bit is valid if bit 1 of Word 82 is set to 1
0	1: SMART error logging is supported. This bit is valid if bit 1 of Word 82 is set to 1

Word 119

Bit	Function
5	1: Free-fall Control feature set is supported
4	1: DOWNLOAD MICROCODE command requesting the offset transfer method is supported
3	1: the optional GPL feature set commands READ LOG DMA EXT and WRITE LOG DMA EXT are supported. This bit shall only be set to 1 if Word 84 bit 5 is set to 1
2	1: WRITE UNCORRECTABLE EXT command is supported
1	1: Write-Read-Verify feature set is supported
0	0: reserved for DDT

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Words 85-87, 120: Commands and Feature Sets Supported or Enabled

Words 85, 86, 87 and 120 indicate features/command sets enabled.

Word 85

Bit	Function
14	same as in bit 14 of Word 82
13	same as in bit 13 of Word 82
12	same as in bit 12 of Word 82
10	same as in bit 10 of Word 82
9	shall be cleared to zero to indicate that the DEVICE RESET command is not supported
8	0: not supporting SERVICE interrupt
7	0: not supporting Release interrupt
6	0: not supporting Read Look-ahead
5	0: Write cache is disabled. This bit is valid if bit 5 of Word 82 is set to 1
4	same as in bit 4 of Word 82
3	same as in bit 3 of Word 82
2	0: not supporting Removable Media feature set
1	0: Security Mode feature set is disabled. The Security Mode feature set can be enabled via the SECURITY SET PASSWORD command. This bit is valid if bit 1 of Word 82 is set to 1
0	0: SMART feature set is disabled. The SMART feature set can be enabled via the SMART ENABLE OPERATIONS command. This bit is valid if bit 0 of Word 82 is set to 1

Word 86

Bit	Function
13	same as in bit 13 of Word 83
12	same as in bit 12 of Word 83
11	same as in bit 11 of Word 83
10	same as in bit 10 of Word 83
9	1: Automatic Acoustic Management feature set is enabled. This bit is valid if bit 9 of Word 83 is set to 1
8	1: Host Protected Area Security Extensions are enabled. This bit is valid if bit 8 of Word 83 is set to 1
7	Reserved for Address Offset Reserved Area Boot Method
6	same as in bit 6 of Word 83
5	1: PUIS feature set is enabled. This bit is valid if bit 5 of Word 83 is set to 1
3	1: APM feature set is enabled. This bit is valid if bit 3 of Word 83 is set to 1
2	same as in bit 2 of Word 83
1	same as in bit 1 of Word 83
0	same as in bit 0 of Word 83

Word 87

Bit	Function
13	same as in bit 13 of Word 84
12	Reserved for TLC
11	Reserved for TLC
8	same as in bit 8 of Word 84
7	same as in bit 7 of Word 84
6	1: 48-bit feature set is supported. When this bit is set to 1, the WRITE DMA FUA EXT command and the WRITE MULTIPLE FUA EXT command are supported
5	same as in bit 5 of Word 84
3	1: Media Card Pass Through feature set is enabled.
2	1: Media serial number field in Word 176-205 is valid. This bit shall be cleared to zero if the media does not contain a valid serial number or if no media is present. This bit is valid if bit 2 of Word 84 is set to one indicating Media serial number is supported.
1	same as in bit 1 of Word 84
0	same as in bit 0 of Word 84

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Word 120

Bit	Function
5	1: Free-fall Control feature set is enabled
4	same as in bit 4 of Word 119
3	same as in bit 3 of Word 119
2	same as in bit 2 of Word 119
1	1: Write-Read-Verify feature set is enabled
0	reserved for DDT

Word 88: Ultra DMA Modes

This field identifies the Ultra DMA transfer modes supported by the device and indicates the mode that is currently selected. Only one DMA mode shall be selected at any given time. If an Ultra DMA mode is selected, then no Multiword DMA mode shall be selected and vice versa. Support of this word is mandatory if any Ultra DMA mode is supported.

Bit	Function
15	Reserved
14	1: Ultra DMA mode 6 is selected 0: Ultra DMA mode 6 is not selected
13	1: Ultra DMA mode 5 is selected 0: Ultra DMA mode 5 is not selected
12	1: Ultra DMA mode 4 is selected 0: Ultra DMA mode 4 is not selected
11	1: Ultra DMA mode 3 is selected 0: Ultra DMA mode 3 is not selected
10	1: Ultra DMA mode 2 is selected 0: Ultra DMA mode 2 is not selected
9	1: Ultra DMA mode 1 is selected 0: Ultra DMA mode 1 is not selected
8	1: Ultra DMA mode 0 is selected 0: Ultra DMA mode 0 is not selected
7	Reserved
6	1: Ultra DMA modes 6 and below are supported
5	1: Ultra DMA modes 5 and below are supported
4	1: Ultra DMA modes 4 and below are supported
3	1: Ultra DMA modes 3 and below are supported
2	1: Ultra DMA modes 2 and below are supported
1	1: Ultra DMA modes 1 and below are supported
0	1: Ultra DMA mode 0 is supported

Word 89: Time Required for a Normal Erase Mode SECURITY ERASE UNIT Command

Word 89 specifies the estimated time required for the Security Erase Unit command to complete its normal mode erasure as defined in the following table.

Table 10-7: Normal Erase Mode Time

Value	Time
0	Value not specified
1-254	(Value ∗ 2) minutes
255	> 508 minutes

Word 90: Time Required for an Enhanced Erase Mode SECURITY ERASE UNIT Command

Word 90 specifies the estimated time required for the Security Erase Unit command to complete its enhanced mode erasure as defined in the following table.

Table 10-8: Enhanced Erase Mode Time

Value	Time
0	Value not specified
1-254	(Value ∗ 2) minutes
255	> 508 minutes

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Word 91: Current Advanced Power Management Level Value

Bits (7:0) of Word 91 contain the current APM level setting. Support of this Word is mandatory if the APM feature set is supported. This Word is valid if bit 3 of Word 83 and bit 3 of Word 86 are set to one indicating the APM feature set is supported.

Word 92: Master Password Identifier

If the Security feature set is not supported (i.e., bit 1 of Word 82 is cleared to zero) or the Master Password Identifier feature is not supported, then Word 92 shall contain 0000h or FFFFh. If the Security feature set and the Master Password Identifier feature are supported, then Word 92 contains the value of the Master Password Identifier set when the Master Password was last changed.

Word 93: Hardware Reset Results

Word 93 shall be set to the value 0000h.

Word 94: Current AAM Value

Bits (15:8) contain the device's recommended AAM level. If the host requires the device to perform with highest performance, then the host should set the AAM level to FEh. If the host requires the device's recommended AAM level, then the host should set the AAM level to the value returned in these bits. The use of this setting may not provide the lowest acoustics, or the best trade-off of acoustics and performance, in all configurations. Support of this word is mandatory if the AAM feature set is supported.
Bits (7:0) contain the current AAM level.
This word is valid if the 9 of Word 83 is set to one indicating that the AAM feature set is supported.

Word 95: Stream Minimum Request Size

Word 95 contains the number of logical sectors that provides optimum performance in a streaming environment. This number shall be a power of two, with a minimum of eight logical sectors. The starting LBA value for each streaming command should be evenly divisible by this request size. This Word is valid if bit 4 of Word 84 is set to one, indicating that the Streaming feature set is supported. If the Streaming feature set is not supported by the device, the content of Word 95 shall be zero.

Word 96: Streaming Transfer Time – DMA

Word 96 defines the Streaming Transfer Time for DMA mode. The worst-case sustainable transfer time per logical sector for the device is calculated as follows:

Streaming Transfer Time = (Word 96) ∗ (Streaming Performance Granularity / 65536)

The content of Word 96 may be affected by the host issuing a Set Maximum Host Interface Sector Times. Because of this effect, the host should issue an IDENTIFY DEVICE command after issuing a SET FEATURES command that may affect this Word. If the Streaming feature set is not supported by the device, the content of Word 96 shall be zero.

This Word is valid if bit 4 of Word 84 is set to one indicating that the Streaming feature set is supported.

Word 97: Streaming Access Latency – DMA and PIO

Word 97 defines the Streaming Access Latency for DMA and PIO mode. The worst-case access latency of the device for a streaming command is calculated as follows:

Access Latency = (Word 97) ∗ (Streaming Performance Granularity / 256)

The content of Word 97 may be affected by the host issuing a SET FEATURES subcommand 42h or C2h. Because of this effect, the host should issue an IDENTIFY DEVICE command after issuing a SET FEATURES command that may affect this Word. If the Streaming feature set is not supported by the device, the content of Word 97 shall be zero.

This Word is valid if bit 4 of Word 84 is set to one indicating that the Streaming feature set is supported.

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Words 98-99: Streaming Performance Granularity

These Words define the fixed unit of time that is used in IDENTIFY DEVICE data Word 96, Word 97, and Word 104, SET FEATURES subcommand Set Maximum Host Interface Sector Times, and in the Command Completion Time Limit that is passed in streaming commands. The unit of time for this parameter shall be in microseconds, then:

a) the Command Completion Time Limit in the Feature field for a streaming command shall be yy microseconds;
b) the Streaming Transfer Time shall be:
    a. ((Word 96) ∗ (yy/65536)) microseconds;
    b. ((Word 104) ∗ (yy/65536)) microseconds; or
c) the Streaming Access Latency shall be ((Word 97) ∗ (yy/256)) microseconds;
d) taking these units into account, the host may calculate the estimated time for a streaming command of size S logical sectors as:
    a. for PIO ((Word 104) ∗ S / 65536) + (Word 97 / 256)) ∗ yy microseconds; or
    b. for PIO ((Word 96) ∗ S / 65536) + (Word 97 / 256)) ∗ yy microseconds

This Word is valid if bit 4 of Word 84 is set to one indicating that the Streaming feature set is supported.

Words 100-103: Total Number of User Addressable Sectors for the 48-bit Address feature set

Words 100-103 contain a value that is one greater than the maximum LBA in user accessible space when the 48-bit Addressing feature set is supported. The maximum value that shall be placed in this field is 0000_FFFF_FFFF_FFFFh. Support of these Words is mandatory if the 48-bit Address feature set is supported.

Word 104: Streaming Transfer Time – PIO

Word 104 defines Streaming Transfer Time for PIO mode. The worst-case sustainable transfer time per logical sector for the device is calculated as follows:

Streaming Transfer Time = (Word 104) ∗ (Streaming Performance Granularity / 65536)

The content of Word 104 may be affected by the host issuing a Set Maximum Host Interface Sector Times. Because of this effect, the host should issue an IDENTIFY DEVICE command after issuing a SET FEATURES command that may affect this Word.

The Word is valid if bit 4 of Word 84 is set to one indicating that the Streaming feature set is supported.

Word 105: Maximum number of 512-Byte blocks of LBA Range Entries

Word 106: Physical Sector Size / Logical Sector Size

If bit 14 is set to one and bit 15 is cleared to zero, the contents of Word 106 contain valid information. If not, information is not valid in this word.

Bit	Function
13	1: Device has more than one logical sector per physical sector
12	1: Device has been formatted with a logical sector size larger than 256 Words 0: Words 117-118 are invalid and the logical sector size is 256 Words
11:4	Reserved
3:0	the size of the device physical sectors in power of two logical sectors

Examples:

Bits (3:0): 0 = 2^0 = 1 logical sector per physical sector
Bits (3:0): 1 = 2^1 = 2 logical sectors per physical sector
Bits (3:0): 2 = 2^2 = 4 logical sectors per physical sector
Bits (3:0): 3 = 2^3 = 8 logical sectors per physical sector

Word 107: Inter-seek Delay for ISO 7779 Standard Acoustic Testing

Word 107 is the manufacturer's recommended time delay between seeks in microseconds during ISO 7779 standard acoustic testing.

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Words 108-111: World Wider Name

Words 108-111 contain a mandatory World Wide Name (WWN) in the NAA IEEE Registered identifier format.

Word 108 bits (15:12) shall contain 5h, indicating that the naming authority is IEEE. All other values are reserved.

Word 109 bits (11:0) and Word 109 bits (15:4) shall contain the Organization Unique Identifier (OUI) for the device manufacturer assigned by the IEEE.

The identifier may be obtained from the IEEE.

Word 109 bits (3:0), Word 110, and Word 111 shall contain a value assigned by the vendor that is unique for the device in the OUI domain.

Words 112-115: Reserved for a 128-bit World Wide Name

Word 116: Reserved for TLC

Words 117-118: Logical Sector Size

Words 117-118 are a DWord field that indicates the size of device logical sectors in Words. The value of logical sector size shall be equal to or greater than 256. The value of logical sector size shall be valid when bit 12 of Word 106 is set to one. All logical sectors on device shall be this length. When bit 12 of Word 106 is cleared to zero Words 117-118 shall be cleared to zero.

Word 119: See Words 82-84

Words 120: See Words 85-87

Words 121-126: Reserved for Expanded Supported and Enabled Settings

Word 127: Obsolete

Word 128: Security Status

Bit	Function
8	Master Password Capability Security mode is enabled and Master Password Capability is high: 0 Security mode is enabled and Master Password Capability is maximum: 1 Security mode is disabled: -
5	1: the enhanced mode of the SECURITY ERASE UNIT command is supported
4	1: the password attempt counter has decremented to zero. This is also known as the Password Attempt Counter Exceeded bit.
3	1: security is frozen
2	1: security is locked
1	1: security is enabled
0	1: security feature set is supported

Word 160: CFA Power Mode

Word 160 indicates the presence and status of CFA feature set. Support of this Word is mandatory if CFA Power Mode 1 is supported.

If bit 13 is set to one, the device shall be in CFA Power Mode 1 to perform one or more commands implemented by the device.

If bit 12 is set to one, the device is in CFA Power Mode 0.

Bits (11:0) indicate the maximum average RMS current in Milliamperes required during 3.3V or 5V operation in CFA Power Mode 1.

Words 161-167: Reserved for Assignment by the CompactFlash™ Association

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Word 168: Nominal Form Factor

Bits (3:0) indicate the nominal form factor of the device and are defined below:

Value	Description
0h	Nominal form factor not reported
1h	5.25” nominal form factor
2h	3.25” nominal form factor
3h	2.5” nominal form factor
4h	1.8” nominal form factor
5h	< 1.8” nominal form factor
6h-Fh	Reserved

Word 169: DATA SET MANAGEMENT Supported

Words 170-175: Reserved

Words 176-205: Current Media Serial Number

Words 176-205 contain the current media serial number. Media serial numbers shall be an ATA string of 60 Bytes. The first 40 Bytes shall indicate the media serial number and the remaining 20 Bytes shall indicate the media manufacturer.

Word 206: SCT Command Transport

Bit	Function
15:12	support for vendor specific action codes
11:6	reserved
5	1: SCT Data Tables are supported
4	1: supports SCT Features Control
3	1: supports SCT Error Recovery Control
2	1: supports SCT Write Same
1	1: supports SCT Long Sector Access
0	1: supports SCT Command Transport including SCT Read Status

Word 209: Alignment of Logical Blocks within a Physical Block

Word 209 shall report the location of LBA0 within the first physical sector of the media. This bit is valid if the bit 13 of Word 106 is set to 1 indicating device has multiple sectors per physical sector.

Words 210-211: Write-Read-Verify Sector Count Mode 3

Words 210-211 shall indicate the number of logical sectors to be verified after every spin-up, as set by the SET FEATURES command for the Enable Write-Read-Verify subcommand. This count only applies to mode 3.

Words 212-213: Write-Read-Verify Sector Count Mode 2

Words 211-213 shall indicate the number of logical sectors to be verified after every spin-up, as set by the SET FEATURES command for the Enable Write-Read-Verify subcommand. This count only applies to mode 2.

Word 214: NV Cache Capabilities

Both the NV Cache Power Mode feature set version (Word 214 bits (11:8)) and the NV Cache feature set version (Word 214 bits (15:12)) shall be set to 0. If bit 4 of Word 214 is set to one, the NV Cache feature set is enabled. If bit 1 of Word 214 is set to one, the NV Cache Power Management feature is enabled. This capability is enabled by issuing a SET NV CACHE POWER MODE and disabled by issuing a RETURN FROM NV CACHE POWER MODE.

If bit 0 of Word 214 is set to one, the NV Cache Power Management feature set is supported.

Words 215-216: NV Cache Size in Logical Blocks

Words 215-216 indicate the maximum number of logical sectors that the device’s NV Cache Set contains for the host to pin. This field is valid if Word 214 bit 0 or bit 4 is set to one indicating the NV Cache feature set is supported.

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Word 217: Nominal Media Rotation Rate

Word 217 indicates the nominal media rotation rate of the device. Default value: 0001h – non-rotating media.

Word 218: Reserved

Word 219: NV Cache Options

Word 219 bits (7:0) contain the device's estimate of the amount of time in seconds it takes for the device to satisfy a read or write request from its rotational media when the read or write request is received while the rotational media is not spinning. This field is valid if bit 4 of Word 214 is set to one. Default is not valid – non-rotating media.

Word 220: Write-Read-Verify Mode

Word 220 contains the current mode of the Write-Read-Verify feature set, as set by the SET FEATURES Enable/Disable Write-Read-Verify subcommand.

Bits (15:8) are reserved.
Bits (7:0) indicate the current mode of the Write-Read-Verify feature set.

Word 221: Reserved

Word 222: Transport Major Version Number

If Word 222 is not set to FFFFh or 0000h, then the device claims compliance with one or more of the ATA transport standard major versions as indicated by bits (6:3) being set to one. Values other than 0000h and FFFFh are bit significant

Word 223: Transport Minor Version Number

The following table defines the value that shall be reported in Word 223 to indicate the version of the standard that guided the implementation.

Table 10-9: Transport Minor Version Number

Value	Minor Version
0000h	Minor version not reported
0001h-0020h	Reserved
0021h	ATA8-AST T13 Project D1697 Version 0b
0022h-FFFEh	Reserved
FFFFh	Minor version not reported

Words 224-233: Reserved for CE-ATA

Word 234: Minimum Number of 512-Byte Data Blocks per DOWNLOAD MICROCODE Command Mode 03h

Word 234 contains the minimum number of 512-Byte data blocks per DOWNLOAD MICROCODE command when using the offset transfer method. This Word is valid if bit 0 of Word 83, bit 0 of Word 86, and bit 4 of Word 120 are set to one, indicating that the DOWNLOAD MICROCODE command using the offset transfer method is supported. The values 0000h and FFFFh indicate the no minimum specified.

Word 235: Maximum Number of 512-Byte Data Blocks per DOWNLOAD MICROCODE Command Mode 03h

Word 235 contains the maximum number of 512-Byte data blocks per DOWNLOAD MICROCODE command when using the offset transfer method. This Word is valid if bit 0 of Word 83, bit 0 of Word 86, and bit 4 of Word 120 are set to one, indicating that the DOWNLOAD MICROCODE command using the offset transfer method is supported. The values 0000h and FFFFh indicate there is no maximum specified.

Words 236-254: Reserved

Word 255: Integrity Word

The use of this Word is optional. If bits (7:0) of this Word contain the signature A5h and bits (15:8) contain the data structure checksum. The data structure checksum is the two's complement of the sum of all bytes in Words 0-254 and the Byte consisting of bits (7:0) in word 255. Each byte shall be added with unsigned arithmetic and overflow shall be ignored. The sum of all 512 bytes is zero when the checksum is correct.

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10.4.2 Set-Features – EFh

This command is used by the host to establish or select certain features. The following table defines all features that are supported.

Table 10-10: Features Supported

Feature	Operation
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register
05h	Enable the APM feature set
06h	Enable Power-Up In Standby feature set
07h	Power-Up In Standby feature set device spin-up
10h	Enable use of SATA feature
55h	Disable read look-ahead feature
66h	Disable Power-On Reset (POR) establishment of defaults at software reset
82h	Disable write cache
85h	Disable the APM feature set
86h	Disable Power-Up In Standby feature set
90h	Disable use of SATA feature
AAh	Enable read look-ahead feature
CCh	Enable Power-On Reset (POR) establishment of defaults at software reset

Features 02h and 82h allow the host to enable or disable write cache in the Devices that implement write cache. When the subcommand Disable-Write-Cache is issued, the device should initiate the sequence to flush cache to non-volatile memory before command completion.

Feature 03h allows the host to select the transfer mode by specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value. The host may change the selected modes by the SET FEATURES command.

Feature 05h allows the host to enable Advanced Power Management. To enable Advanced Power Management, the host writes the Sector Count register with the desired advanced power management level and then executes a SET FEATURES command with subcommand code 05h. Feature 85h disables Advanced Power Management.

Table 10-11: Advanced power management levels

Level Sector	Count value
Maximum performance	FEh
Intermediate power management levels without Standby	81h-FDh
Minimum power consumption without Standby	80h
Intermediate power management levels with Standby	02h-7Fh
Minimum power consumption with Standby	01h
Reserved	00h, FFh

Feature 10h and 90h allow the host to enable or disable Serial ATA features. The Count field contains the specific Serial ATA feature to enable or disable. The specific Serial ATA features are defined in table 10-12.

Table 10-12: SATA Features

Count	Description
00h	Reserved for Serial ATA
01h	Non-zero Buffer Offsets
02h	DMA Setup FIS Auto-Activate optimization
03h	Device-initiated interface power state transitions
04h	Guaranteed In-Order Data Delivery
05h	Asynchronous Notification
06h	Software Settings Preservation
07h-FFh	Reserved Serial ATA

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Feature 55h is the default feature for the device. Therefore, the host does not have to issue Set-Features command with this feature unless it is necessary for compatibility reasons.

Features 66h and CCh can be used to enable and disable whether the Power-on Reset (POR) Defaults will be set when a software reset occurs.

10.4.3 Idle/Partial – E3h

This command causes the device to enter the Idle mode. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and automatic power-down mode is enabled. If the sector count is zero, the automatic power-down mode is also enabled, the timer count is set to 3, with each count being 5ms.

10.4.4 Standby / Slumber – E2h

This command causes the device to enter the Standby mode. Recovery from standby mode is accomplished by simply issuing another command (a reset is permitted, but not required).

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10.5 Error Posting

The following table summarizes the valid status and error values for the SATA NANDrive command set.

Table 10-13: Error and Status Register [17]

Command	Error Register					Status Register				
	ICRC/ BBK	UNC	IDNF	ABRT	AMNF	RDY	DWF	DSC	CORR	ERR
Check-Power-Mode				V		V	V	V		V
Execute-Drive-Diagnostic [18]						V		V		V
Flush-Cache				V		V	V	V		V
Flush-Cache-EXT [19]				V		V	V	V		V
Get-Media-Status				V		V	V	V		V
Identify-Drive				V		V	V	V		V
Idle				V		V	V	V		V
Idle-Immediate				V		V	V	V		V
NOP				V		V	V			V
Packet				V		V	V	V		V
Read-Buffer				V		V	V	V		V
Read-DMA	V	V	V	V	V	V	V	V	V	V
Read-DMA-EXT [19]	V	V	V	V	V	V	V	V	V	V
Read-Multiple	V	V	V	V	V	V	V	V	V	V
Read-Multiple-EXT [19]	V	V	V	V	V	V	V	V	V	V
Read-Native-Max-Address			V	V		V	V	V		V
Read-Native-Max-Address-EXT [19]			V	V		V	V	V		V
Read-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Sector(s)-EXT [19]	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)	V	V	V	V	V	V	V	V	V	V
Read-Verify-Sector(s)-EXT [19]	V	V	V	V	V	V	V	V	V	V
Security-Disable-Password				V		V	V	V		V
Security-Erase-Prepare				V		V	V	V		V
Security-Erase-Unit				V		V	V	V		V
Security-Freeze-Lock				V		V	V	V		V
Security-Set-Password				V		V	V	V		V
Security-Unlock				V		V	V	V		V
Set-Features				V		V	V	V		V
Set-Max-Address-EXT[19]			V	V		V	V	V		V
Set-Max-Lock			V	V		V	V	V		V
Set-Max-Set-Password			V	V		V	V	V		V
Set-Max –Unlock			V	V		V	V	V		V
Set-Multiple-Mode				V		V	V	V		V
Sleep				V		V	V	V		V
SMART				V		V		V		V
Standby				V		V	V	V		V
Standby-Immediate				V		V	V	V		V
Write-Buffer				V		V	V	V		V
Write-DMA	V		V	V	V	V	V	V		V
Write-DMA-EXT [19]	V		V	V	V	V	V	V		V
Write-Multiple	V		V	V	V	V	V	V		V
Write-Multiple-EXT [19]	V		V	V	V	V	V	V		V
Write-Sector(s)	V		V	V	V	V	V	V		V
Write-Sector(s)-EXT [19]	V		V	V	V	V	V	V		V
Invalid-Command-Code				V		V	V	V		V

17) The host is required to reissue any media access command (such as Read-Sector and Write-Sector) that ends with an error condition.
18) See Table “Features Supported” V = valid on this command
19) EXT – 48-bit LBA
20) No description for the obsolete command is addressed.

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11.0 ELECTRICAL SPECIFICATIONS

11.1 Absolute Maximum Ratings

Absolute Maximum Stress Ratings - Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.

Storage Temperature[21]:
- 40°C to +85°C (3,000 hours for 10% cycled device / 300 hours for 100% cycled device) [22]
- 40°C to +55°C (10 years for 10% cycled device / 1 year for 100% cycled device) [22]

D.C. Voltage on Pin types[23] I2x and O1 to Ground Potential ..... - 0.5V to V_{DD33}+0.5V
D.C. Voltage on Analog core Pin types[23] I3 and O3 to Ground Potential ..... -0.1V min to 1.6V max
Transient Voltage (<20 ns) on Pin types[23] I2x and O1 to Ground Potential ..... - 2.0V to V_{DD33}+2.0V
Package Power Dissipation Capability (T_A = 25°C) 1.5W
Surface Mount Solder Reflow Temperature[24] ..... 260°C for 10 seconds
Output Short Circuit Current[25] 60mA

21) Recommended maximum storage duration when the device is not powered up. Refer to Table 4-3 for P/E cycle estimates. Contact Greenliant for details.
22) The cycling condition shall be either under the normal usage situation with sufficient relaxation time between cycles (maximum one P/E cycle through the entire device per 10 minutes), or under an accelerated test condition at an elevated temperature (85°C) as specified by JEDEC.
23) Refer to Table 3-1 "Pin Assignments"
24) Refer to Figure 11-1
25) Outputs shorted for no more than 1 second. No more than one output shorted at a time.

11.1.1 Absolute Maximum Power Pin Stress Ratings

Table 11-1: Absolute Maximum Power Pin Stress Ratings

Parameter	Symbol	Conditions
Input Power 1.2V	V_{DD12}, V_{DD12AS}, V_{DD12AP}	-0.1V min to 1.6V max
Input Power 3.3V	V_{DD33}, V_{DD33A}, V_{DD33N}	-0.3V min to 4.0V max
Ground	V_{SS}, V_{SSX}, V_{SST}, V_{SSA}, V_{SSAP}	-0.5V min to V_{DD} + 0.5V max

11.2 Operating Ratings

Table 11-2: Operating Ranges

Range	Ambient Temperature	V_{DD33}, V_{DD33A}, V_{DD33N}	V_{DD12}, V_{DD12AS}, V_{DD12AP}
Industrial	-40°C to +85°C	3.135 - 3.465V	1.14 – 1.26V

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11.3 AC Characteristics

11.3.1 AC Conditions of Test

Table 11-3: AC Conditions of Test

Input Rise/Fall Time	Output Load
5 ns	C_L = 50pF

11.3.2 For all logic pins (except SATA IO)

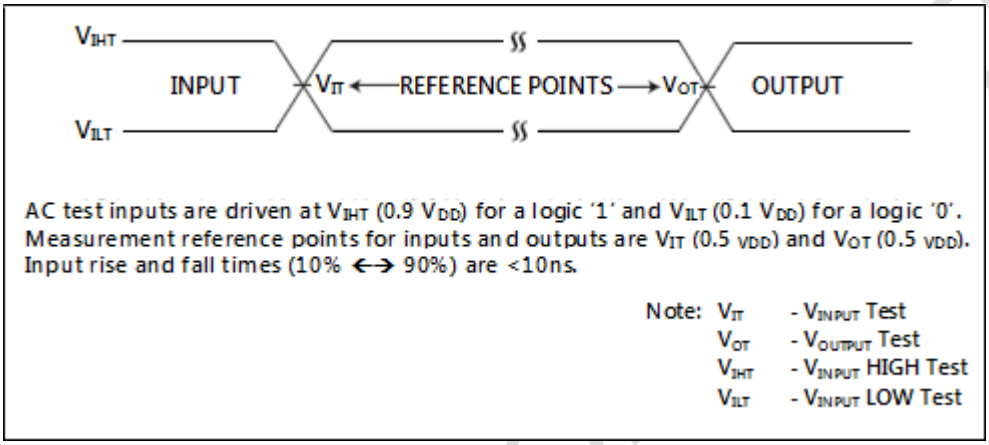

Figure 11-1: AC Input/Output Reference Waveforms

11.3.3 Host Side Interface Timing Specifications

Refer to SATA Revision 2.6 for standard SATA host timing specifications.

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11.4 Recommended System Power-on Timing

Table 11-4: Recommended System Power-on Timing

Symbol	Parameter	Specification			Unit
		Min	Typ	Max	
$T_{PU-INITIAL}$	Drive Initialization to Ready		7	50	s
$T_{PU-READY}$	Host Power-on/ Reset to Ready Operation		800	2,000[8)]	ms
$T_{PU-WRITE}$	Host Power-on/ Reset to Write Operation		800	2,000[8)]	ms
T_{PWR}	Time delay from power stabilization to normal Rx/Tx operation	1			ms
$T_{PM\_PARTIAL0}$	Time for active to partial mode	1			µs
$T_{PM\_PARTIAL1}$	Time for partial to active mode	10			µs
$T_{PM\_SLUMBER0}$	Time for active to slumber mode	1			µs
$T_{PM\_SLUMBER1}$	Time for slumber to active mode	10			µs
T_{PD1}	Time for active to power down mode	1			µs
$T_{Tx\_LAT\_Gen1}$	Tx latency, Gen1			24	Gen 1 UI
$T_{Tx\_LAT\_Gen2}$	Tx latency, Gen2			24	Gen 2 UI
$T_{Rx\_LAT\_Gen1}$	Rx latency, Gen1			100	Gen1 UI
$T_{Rx\_LAT\_Gen2}$	Rx latency, Gen2			100	Gen2 UI

11.5 Reliability Characteristics

Table 11-5: Reliability Characteristics [26)]

Symbol	Parameter	Minimum Specification	Units	Test Method
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

26) This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

11.6 Purge Erase Time

Table 11-6: Purge Erase Time

Product	Product Revision	Typ. [sec]	Max. [sec]
GLS85LS1016P-S-I-FZJE	CC0 / CC1	650	1300
GLS85LS1032P-S-I-FZJE	CC0 / CC1	750	1500

11.7 Power-Down Mode Entry Time

Table 11-7: Power-Down Mode Entry Time

Symbol	Parameter	Min. [µs]
$T_{POWER-DOWN}$	Time to assert PD#/WP# pin to enter Power-down mode	5

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11.8 XTAL Reference Clock Input Requirements

Table 11-8: XTAL Reference Clock Input Requirements

Symbol	Parameter	Specification			Unit
		Min	Typ	Max	
T_{CLKI_FREQ}	Nominal Frequency		25		MHz
T_{CLKI_J}	CLKI frequency tolerance	-100		+100	ppm
$T_{CLKI\_RC\_DUTY}$	CLKI duty cycle	30		70	%
V_{IH} [27]	Input high level	2			V
V_{IL} [27]	Input low level			0.8	V
V_{OVER}	Input overshoot			3.3+0.4	V
V_{UNDER}	Input undershoot	-0.4			V
SL_{rise}	Rise edge rate	0.3			V/ns
SL_{fall}	Fall edge rate	0.3			V/ns

27) These parameters also apply to the WP#/PD# and RESET# pin.

11.9 SATA Interface Timing Specification

Table 11-9: SATA Interface Timing Specifications

Symbol	Parameter	Condition	Specification			Unit
			Min	Typ	Max	
$T_{TX\_RIST\_FAIL}$	Rise and Fall time at transmitter	20% - 80% Gen1	100		274	ps
		20% - 80% Gen2	67		136	
T_{TX_SKEW}	Tx differential skew				20	ps
$T_{TX\_DC\_FREQ}$	Tx DC clock frequency skew		-350		350	ppm
$T_{TX\_AC\_FREQ}$	Tx AC clock frequency skew	Ref Clk = SSC AC modulation, subject to the “Downspread SSC” triangular modulation (30 – 33KHz) profile	-5,000		0	ppm

11.10 SATA Interface Transmitter Output Jitter Characteristics

Table 11-10: SATA Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Specification			Unit
			Min	Typ	Max	
RJ_{5UI}	5UI later Random Jitter	Measured at Tx output pins 1sigma deviation		3.5		ps rms
RJ_{250UI}	250UI later Random Jitter	Measured at Tx output pins 1sigma deviation		4.5		ps rms
DJ_{5UI}	5UI later Deterministic Jitter	Measured at Tx output pins peak-to-peak phase variation Random data pattern		30		ps
DJ_{250UI}	250UI later Deterministic Jitter	Measured at Tx output pins peak-to-peak phase variation Random data pattern		40		ps
$RJ_{1/10UI}$ [28]	High frequency random jitter			3.5		ps
$RJ_{1/500UI}$	Low frequency random jitter			4.5		ps
$DJ_{1/10UI}$	High frequency deterministic jitter			30		ps
$DJ_{1/500UI}$	Low frequency deterministic jitter			40		ps

28) The spread spectrum frequency will create additional jitter for the Tx jitter. This typical value is for cases where there is no spread spectrum clock generator.

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11.11 DC Characteristics

Table 11-11: DC Characteristics for SATA Host Interface

Symbol	Parameter	Condition	Specification			Unit
			Min	Typ	Max	
V_{DD12}	1.2V supply voltage		1.14	1.2	1.26	V
V_{DD33}	3.3V supply voltage for XTAL driver		3.135	3.3	3.465	V
$I_{DD12, Gen1}$	Gen1 1.2V supply current			105	157[29)]	mA
$I_{DD12, Gen2}$	Gen2 1.2V supply current			112	168[29)]	mA
$I_{DD12, Partial}$	Partial 1.2V supply current			60	90[29)]	mA
$I_{DD12, Slumber}$	Slumber 1.2V supply current			55	83[29)]	mA
$I_{DD12, PD}$	Power down 1.2V supply current			4	10[29)]	mA
I_{DD33A}	3.3V supply current for XTAL			3	4.5[29)]	mA
$V_{DOUT, Gen1i}$	TX+/TX- differential peak-to-peak voltage swing	Terminated by 50Ω single ended. AC coupling Nominal Tx amplitude	400	500	600	mV
$V_{DOUT, Gen1m}$	TX+/TX- differential peak-to-peak voltage swing	Terminated by 50Ω single ended. AC coupling Nominal Tx amplitude. Need pphycfg [0:4] change for center adjustment	500	550	600	mV
$V_{DOUT, Gen2i}$	TX+/TX- differential peak-to-peak voltage swing	Terminated by 50Ω single ended. AC coupling Nominal Tx amplitude. Need pphycfg[0:4] change for center adjustment	400	550	700	mV
Z_{DOUT}	Differential output impedance		85	100	115	Ω
$T_{TR, Gen1i}$	TX+/TX- differential transition (rise/fall) time	Measured at the lab load. 20% - 80% transition time	0.15		0.41	UI
$T_{TR, Gen1m}$	TX+/TX- differential transition (rise/fall) time	Measured at the lab load. 20% - 80% transition time	0.15		0.41	UI
$T_{TR, Gen2i}$	TX+/TX- differential transition (rise/fall) time	Measured at the lab load. 20% - 80% transition time	0.20		0.41	UI
V_{DIN}	RX+/RX- differential peak-to-peak input sensitivity		225			mV
V_{DIH}	RX+/RX- differential input common-mode voltage		-50	0	50	mV

29) Number is the worst case estimation.

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Table 11-12: Power Consumption of NANDrive

Symbol	Type	Device	Product Revision	Parameter	Typ		Total Typ	Max		Total Max	Units	Conditions
					1.2V	3.3V		1.2V	3.3V			
IDD	PWR	GLS85LS1032P	CC0 / CC1	Active (TA = -40°C to +85°C)	285	570	855	370	1,110	1,480	mW	V_{DD}=V_{DD} Max
ISTB	PWR			Standby/Idle (TA = -40°C to +85°C)	170	40	210	200	50	250	mW	V_{DD}=V_{DD} Max
ISP[2)]	PWR			Sleep (TA = -40°C to +85°C)	65	5	70	93	7	100	mW	V_{DD}=V_{DD} Max
IDD	PWR	GLS85LS1016P	CC0 / CC1	Active (TA = -40°C to +85°C)	225	365	590	340	540	880	mW	V_{DD}=V_{DD} Max
ISTB	PWR			Standby/Idle (TA = -40°C to +85°C)	170	40	210	200	50	250	mW	V_{DD}=V_{DD} Max
ISP[2)]	PWR			Sleep (TA = -40°C to +85°C)	65	5	70	93	7	100	mW	V_{DD}=V_{DD} Max

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12.0 APPENDIX

12.1 Reflow Profile

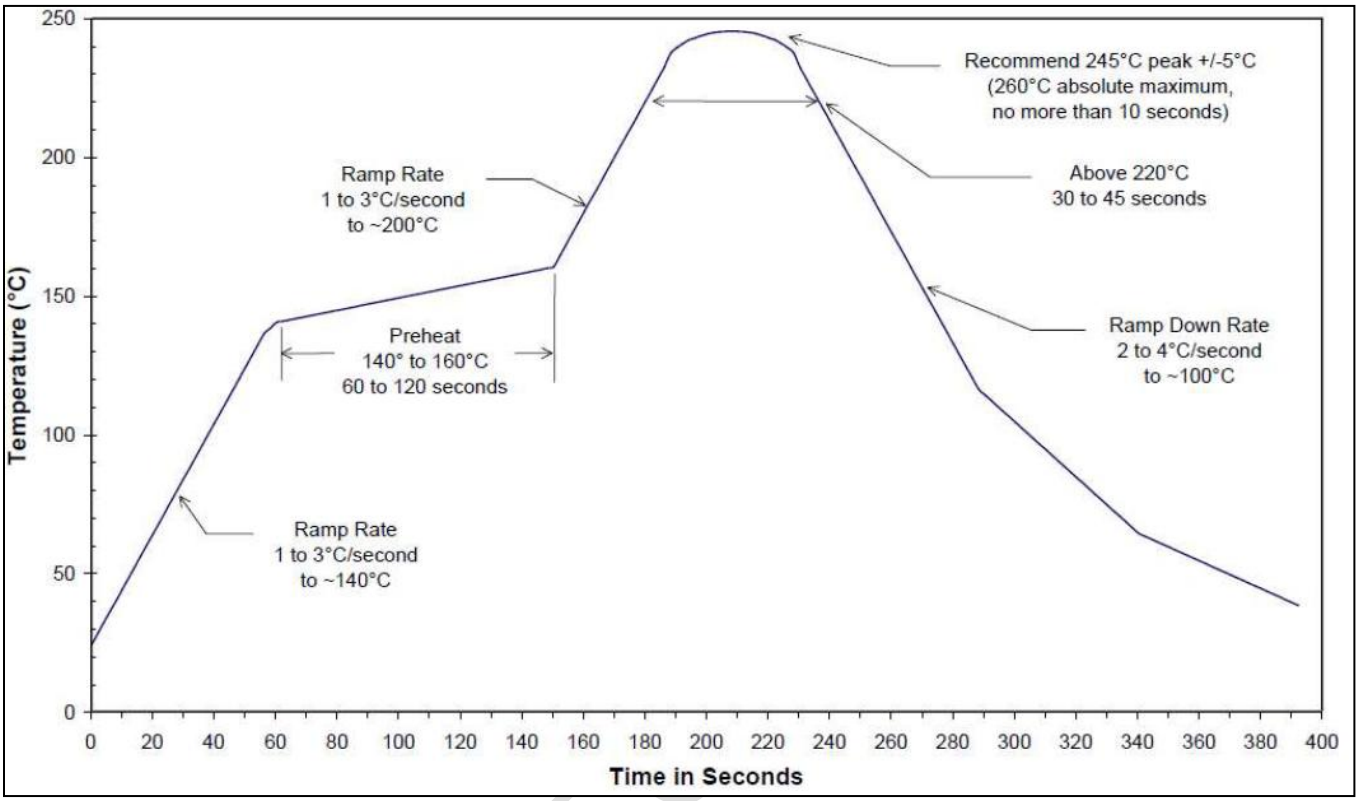

Figure 12-1: Soldering Reflow Profile

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12.2 Product Ordering Information

GLS 85 LS 1 0xxP - S - I - FZJE - NDxxx
XX XX X XXXX - X - X - XXXX - XXXXX

Ordering Code [30)]
NDxxx = NANDrive revision
EDxxx = Evaluation Board revision

Environmental Attribute
E = non-Pb solder (RoHS Compliant)

Package Modifier
ZJ = 145-ball positions

Package Type
F = FBGA

Operation Temperature
I = Industrial: -40°C to +85°C

NAND Configuration
S = 1 bit per cell

Generation / Product Configuration
P = First generation

Capacity
016 = 16 GByte
032 = 32 GByte

MByte or GByte Designator
0 = MByte
1 = GByte

Interface
S = SATA

Voltage
L = 3.3V

Product Series
85 = NANDrive

30) Note that the top side marking on the package typically does not include ordering codes (e.g. NDxxx), unless it is a special C-SPEC (custom specification) which is required by the end-customer to be marked on the device.

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Valid Combinations

Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid combinations and to determine availability of new product combinations.

Table 12-1: SATA NANDrive Product Valid Ordering Numbers

Capacity	Operating Temperature	Part Number	Package
16GB	Industrial (-40°C to 85°C)	GLS85LS1016P-S-I-FZJE-ND101	FZJE, 14x24x1.95mm
16GB	Industrial (-40°C to 85°C)	GLS85LS1016P-S-I-FZJE-ND104	FZJE, 14x24x1.95mm
32GB	Industrial (-40°C to 85°C)	GLS85LS1032P-S-I-FZJE-ND101	FZJE, 14x24x1.95mm
32GB	Industrial (-40°C to 85°C)	GLS85LS1032P-S-I-FZJE-ND104	FZJE, 14x24x1.95mm

Table 12-2: SATA NANDrive Evaluation Board Valid Ordering Numbers

Capacity	Operating Temperature	Part Number	Form Factor
16GB	Industrial (-40°C to 85°C)	GLS85LS1016P-S-I-1S-ED101	Module with SATA connector
16GB	Industrial (-40°C to 85°C)	GLS85LS1016P-S-I-1S-ED104	Module with SATA connector
32GB	Industrial (-40°C to 85°C)	GLS85LS1032P-S-I-1S-ED101	Module with SATA connector
32GB	Industrial (-40°C to 85°C)	GLS85LS1032P-S-I-1S-ED104	Module with SATA connector

Table 12-3: SATA NANDrive miniSATA Evaluation Board Valid Ordering Numbers

Capacity	Operating Temperature	Part Number	Form Factor
16GB	Industrial (-40°C to 85°C)	GLS85LS1016P-S-I-1MS-ED101	JEDEC MO-300
16GB	Industrial (-40°C to 85°C)	GLS85LS1016P-S-I-1MS-ED104	JEDEC MO-300
32GB	Industrial (-40°C to 85°C)	GLS85LS1032P-S-I-1MS-ED101	JEDEC MO-300
32GB	Industrial (-40°C to 85°C)	GLS85LS1032P-S-I-1MS-ED104	JEDEC MO-300

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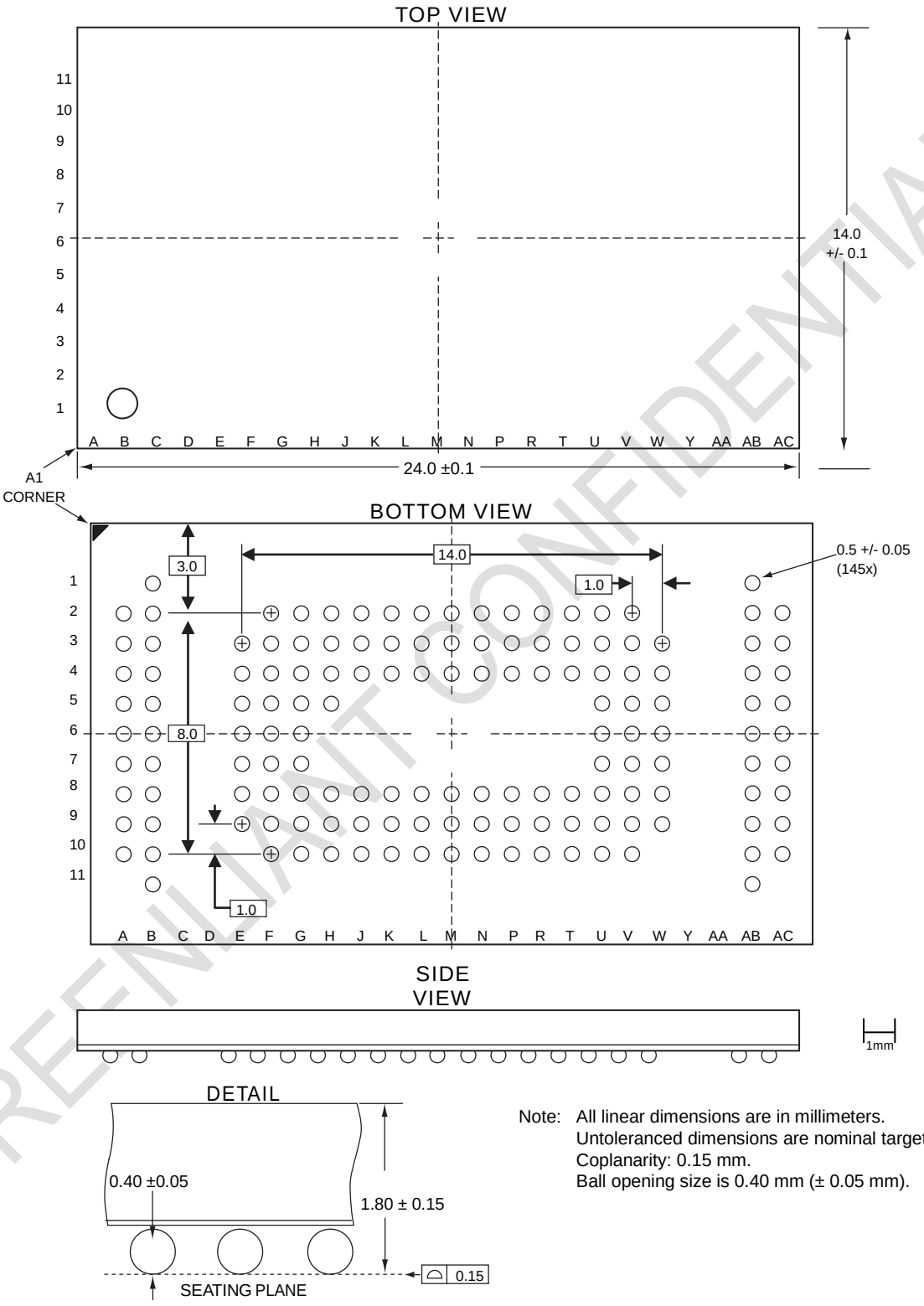
12.3 Package Diagram



Note: All linear dimensions are in millimeters.
Untoleranced dimensions are nominal target values.
Coplanarity: 0.15 mm.
Ball opening size is 0.40 mm (± 0.05 mm).

Figure 12-2: SATA NANDrive 145-Ball, Ball Grid Array (BGA) Greenliant Package Code: FZJ

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12.4 Greenliant Internal Test Pad Information

12.4.1 Part Numbers and Product Revisions of Affected Devices

Part Number	Product Revision
GLS85LS1xxxP-S-I-FZJE-ND1xx	CCx

12.4.2 Greenliant Internal Test Pads

SATA NANDrive package "FZJE" has test pads that are used by Greenliant. **No solder balls are mounted on the test pads**. These pads may be rejected by Surface Mount Technology (SMT) equipment or other machines at assembly vendors, if such equipment is not programmed accordingly. Figure 12-3 shows the locations of the test pads, which are colored in gray. These pads are **Do Not Use (DNU) pads for all users**, and must be open (no connection).

- Pitch (pad to pad): 1mm (+/- 0.05mm) and aligned with solder balls
- Pad opening size and shape: 0.4mm x 0.4mm (+/- 0.05mm), square
- Number of test pads: 28 pads
- Land pattern: SMD type (Solder Mask Defined)
- Material: Electro Ni and Electro Au

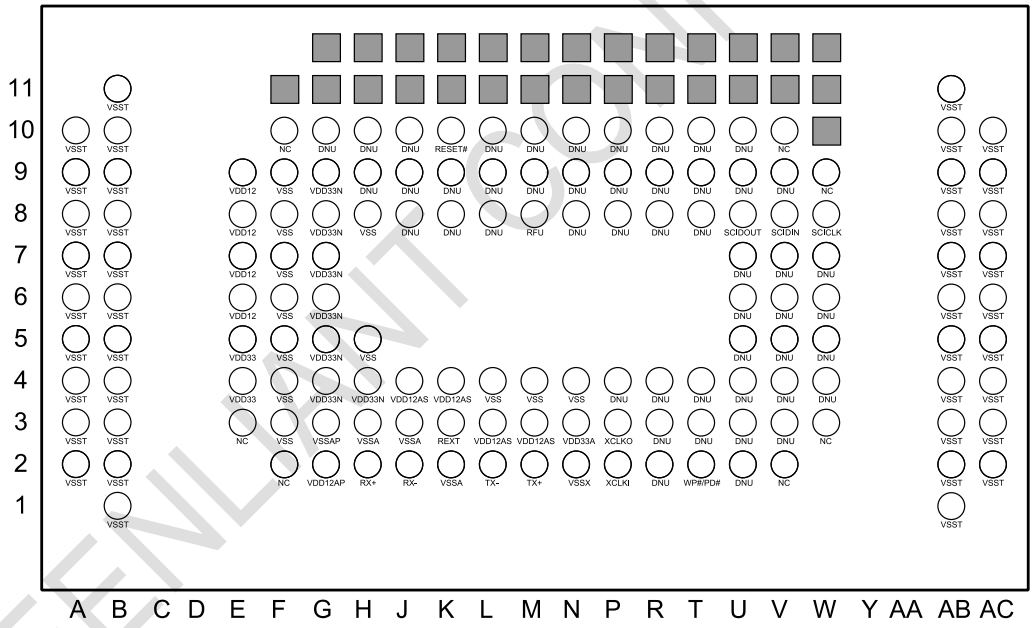

Figure 12-3: Locations of Solder Balls and Test Pads (balls facing down)

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12.5 Reference Documents

Table 12-4: Reference Documents

Document Number	Title
S72097	SATA NANDrive Application Design Guide
S72111	Serial Communication Interface (SCI)
S72099	NANDrive Special Function Zone Specification
S72084	NANDrive SMART Specification
S72091	NANDrive Protection Zone Specification
S72092	NANDrive Security Erase Feature / Purge Command Specification
S74025	Windows PT2 User Guide
S72089	NANDrive Power Interrupt Protection Design Considerations
S72098	PATA / SATA NANDrive Specification for Manufacturer Interface Command
S72090	SATA / PATA NANDrive Firmware Update Specification

12.6 Revision History

Table 12-5: Revision History

Revision	Description	Date
00.001	Initial draft as Advance Information for GLS85LS10016P/1032P	December 07, 2013
01.000	Release as Advance Information for GLS85LS10016P/1032P Added Section 9.0 and footnote in Table 11-8 Updated Tables 4-2, 10-5 and 11-2, and Section 10.4.1	January 18, 2013
01.100	Updated Section 11.1 and Table 12-1 Placed Valid Combinations into table format in Section 12.2	February 25, 2013
01.200	Added footnote 5 in Table 3-1 and footnote 21 in Section 11.1 Updated Tables 4-2, 11-6 and footnote 16	March 29, 2013
01.300	Official Release; Updated Section 10.4.1	August 29, 2013
01.400	Updated Power Specifications on first page Added information for part numbers GLS85LS1016P-S-I-FZJE-ND104 and GLS85LS1032P-S-I-FZJE-ND104	November 21, 2013
01.410	Updated Sections 10.4.1 and 11.4	February 25, 2014
01.500	Added Section 12.4.; Updated Sections 1.1.3 and 9.0	May 09, 2014
01.600	Updated Section 12.4	August 26, 2015

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