| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B1 | VREFB1N0 | VCCD_PLL3 | | | F6 | J9 | | | | | | |
| B1 | VREFB1N0 | GNDA3 | | | F5 | H9 | | | | | | |
| B1 | VREFB1N0 | VCCA3 | | | G6 | J8 | | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_L1p | | H7 | D3 | | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_L1n | | G3 | C2 | | | | DQ2L | DQ1L | DQ1L |
| B1 | VREFB1N0 | IO | DIFFIO_L2p | | B2 | D2 | DQ2L | DQ1L | DQ1L | DQ2L | DQ1L | DQ1L |
| B1 | VREFB1N0 | IO | DIFFIO_L2n | | B1 | D1 | DQ2L | DQ1L | DQ1L | DQ2L | DQ1L | DQ1L |
| B1 | VREFB1N0 | IO | VREFB1N0 | | G5 | H7 | | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_L3p | nRESET | E4 | G6 | DQ2L | DQ1L | DQ1L | DQ2L | DQ1L | DQ1L |
| B1 | VREFB1N0 | IO | DIFFIO_L3n | | E3 | G5 | DQ2L | DQ1L | DQ1L | DQ2L | DQ1L | DQ1L |
| B1 | VREFB1N0 | IO | DIFFIO_L4p | | C2 | E3 | DQS2L/CQ3L, CDPCLK0 | DQS2L/CQ3L, CDPCLK0 | DQS2L/CQ3L, CDPCLK0 | DQS2L/CQ3L, CDPCLK0 | DQS2L/CQ3L, CDPCLK0 | DQS2L/CQ3L, CDPCLK0 |
| B1 | VREFB1N0 | IO | DIFFIO_L4n | | C1 | F3 | DQ2L | DQ1L | DQ1L | DQ2L | DQ1L | DQ1L |
| B1 | VREFB1N0 | IO | DIFFIO_L5p | | D2 | F5 | DQ2L | DQ1L | DQ1L | DQ2L | DQ1L | DQ1L |
| B1 | VREFB1N0 | IO | DIFFIO_L5n | DATA1, ASDO | D1 | F4 | | | | | | |
| B1 | VREFB1N0 | IO | | | | H6 | | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_L6p | | H6 | G4 | DQ2L | DQ1L | DQ1L | DQ2L | DQ1L | DQ1L |
| B1 | VREFB1N0 | IO | DIFFIO_L6n | | J6 | G3 | DQ2L | DQ1L | DQ1L | | | |
| B1 | VREFB1N0 | IO | DIFFIO_L7p | | | H4 | | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_L7n | | H3 | H3 | | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_L8p | FLASH_nCE, nCSO | E2 | E2 | | | | | | |
| B1 | VREFB1N0 | IO | DIFFIO_L8n | | E1 | E1 | | DQ1L | DQ1L | | DQ1L | DQ1L |
| B1 | VREFB1N1 | IO | DIFFIO_L9p | | F2 | F2 | DM2L | DM1L0/BWS#1L0 | DM1L0/BWS#1L0 | DM2L | DM1L0/BWS#1L0 | DM1L0/BWS#1L0 |
| B1 | VREFB1N1 | IO | DIFFIO_L9n | | F1 | F1 | DQ0L | DQ1L | DQ1L | DQ0L | DQ1L | DQ1L |
| B1 | VREFB1N1 | IO | | | H4 | H5 | | | | | | |
| B1 | VREFB1N1 | IO | VREFB1N1 | | H5 | L5 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L10p | | | J4 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L10n | | | J3 | | | | DQ0L | DQ1L | DQ1L |
| B1 | VREFB1N1 | nSTATUS | | nSTATUS | K6 | M6 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L11p | | | G2 | | | | DQ0L | DQ1L | DQ1L |
| B1 | VREFB1N1 | IO | DIFFIO_L11n | | | G1 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L12p | | J4 | K2 | DQS0L/CQ1L, DPCLK0 | DQS0L/CQ1L, DPCLK0 | DQS0L/CQ1L, DPCLK0 | DQS0L/CQ1L, DPCLK0 | DQS0L/CQ1L, DPCLK0 | DQS0L/CQ1L, DPCLK0 |
| B1 | VREFB1N1 | IO | DIFFIO_L12n | | | K1 | | | | DQ0L | DQ1L | DQ1L |
| B1 | VREFB1N1 | IO | DIFFIO_L13p | | H2 | K4 | DQ0L | DQ1L | DQ1L | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L13n | | H1 | K3 | DQ0L | DQ1L | DQ1L | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L14p | | | L4 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L14n | | | L3 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L15p | | | M4 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L15n | | | M3 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L16p | | | J6 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L16n | | | J5 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L17p | | | J7 | | | | | | |
| B1 | VREFB1N1 | IO | DIFFIO_L17n | | | K7 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L18p | | | K8 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L18n | | | L8 | | | | | | |
| B1 | VREFB1N2 | IO | VREFB1N2 | | J3 | M5 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L19p | | | L7 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L19n | | | L6 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L20p | | | N4 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L20n | | | N3 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L21p | | | M8 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L21n | | | M7 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B1 | VREFB1N2 | IO | DIFFIO_L22p | | | L2 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L22n | | | L1 | | | | DQ0L | DQ1L | DQ1L |
| B1 | VREFB1N2 | IO | DIFFIO_L23p | | J2 | M2 | DQ0L | DQ1L | DQ1L | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L23n | | J1 | M1 | DQ0L | DQ1L | DQ1L | DQ0L | DQ1L | DQ1L |
| B1 | VREFB1N2 | IO | DIFFIO_L24p | | | P2 | | | | | | |
| B1 | VREFB1N2 | IO | DIFFIO_L24n | | | P1 | | | | DQ0L | DQ1L | DQ1L |
| B1 | VREFB1N2 | IO | | | | N8 | | | | | | |
| B1 | VREFB1N2 | DCLK | | DCLK | K2 | P3 | | | | | | |
| B1 | VREFB1N2 | IO | | DATA0 | K1 | N7 | | | | | | |
| B1 | VREFB1N2 | nCONFIG | | nCONFIG | K5 | P4 | | | | | | |
| B1 | VREFB1N2 | TDI | | TDI | L5 | P7 | | | | | | |
| B1 | VREFB1N2 | TCK | | TCK | L2 | P5 | | | | | | |
| B1 | VREFB1N2 | TMS | | TMS | L1 | P8 | | | | | | |
| B1 | VREFB1N2 | TDO | | TDO | L4 | P6 | | | | | | |
| B1 | VREFB1N2 | nCE | | nCE | L3 | R8 | | | | | | |
| B1 | VREFB1N2 | CLK0 | DIFFCLK_0p | | G2 | J2 | | | | | | |
| B1 | VREFB1N2 | CLK1 | DIFFCLK_0n | | G1 | J1 | | | | | | |
| B2 | VREFB2N0 | CLK2 | DIFFCLK_1p | | T2 | Y2 | | | | | | |
| B2 | VREFB2N0 | CLK3 | DIFFCLK_1n | | T1 | Y1 | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_L25p | | L6 | R2 | DQ0L | DQ1L | DQ1L | DQ0L | DQ1L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L25n | | M6 | R1 | DQ0L | DQ1L | DQ1L | | DQ1L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L26p | | | R7 | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_L26n | | | R6 | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_L27p | | M2 | U3 | DQ0L | DQ1L | DQ1L | DM0L | DM1L1/BWS#1L1 | DM1L1/BWS#1L1 |
| B2 | VREFB2N0 | IO | DIFFIO_L27n | | M1 | U4 | | DQ1L | DQ1L | | | |
| B2 | VREFB2N0 | IO | DIFFIO_L28p | | M4 | R3 | DM0L | DM1L1/BWS#1L1 | DM1L1/BWS#1L1 | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L28n | | M3 | R4 | DQ1L | DQ3L | DQ1L | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L29p | | N2 | T4 | DQ1L | DQ3L | DQ1L | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L29n | | N1 | T3 | DQ1L | DQ3L | DQ1L | | | |
| B2 | VREFB2N0 | IO | | | | R5 | | | | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N0 | IO | VREFB2N0 | | M5 | T7 | | | | | | |
| B2 | VREFB2N0 | IO | DIFFIO_L30p | | P2 | U2 | DQ1L | DQ3L | DQ1L | | | |
| B2 | VREFB2N0 | IO | DIFFIO_L30n | | P1 | U1 | DQ1L | DQ3L | DQ1L | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L31p | | R2 | V4 | DQ1L | DQ3L | DQ1L | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L31n | | R1 | V3 | DQ1L | DQ3L | DQ1L | | | |
| B2 | VREFB2N0 | IO | DIFFIO_L32p | | | V2 | | | | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L32n | | N5 | V1 | DQ1L | DQ3L | DQ1L | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N0 | IO | DIFFIO_L33p | | P4 | AB2 | DQS1L/CQ1L#, DPCLK1 | DQS1L/CQ1L#, DPCLK1 | DQS1L/CQ1L#, DPCLK1 | DQS1L/CQ1L#, DPCLK1 | DQS1L/CQ1L#, DPCLK1 | DQS1L/CQ1L#, DPCLK1 |
| B2 | VREFB2N0 | IO | DIFFIO_L33n | | P3 | AB1 | DQ1L | DQ3L | DQ1L | | | |
| B2 | VREFB2N0 | IO | DIFFIO_L34p | | U2 | W2 | DM1L/BWS#1L | DM3L0/BWS#3L0 | DM1L2/BWS#1L2 | DQ1L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L34n | | U1 | W1 | DQ3L | DQ3L | DQ1L | DM1L/BWS#1L | DM3L0/BWS#3L0 | DM1L2/BWS#1L2 |
| B2 | VREFB2N1 | IO | DIFFIO_L35p | | V2 | U6 | DQ3L | DQ3L | DQ1L | DQ3L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L35n | | V1 | U5 | DQ3L | DQ3L | DQ1L | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L36p | | P5 | Y4 | | | | DQ3L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L36n | | N6 | Y3 | DQ3L | DQ3L | DQ1L | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L37p | | R4 | AC2 | | | | DQ3L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L37n | | R3 | AC1 | | | | DQ3L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L38p | | W2 | AC3 | DQ3L | DQ3L | DQ1L | DQ3L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L38n | | W1 | AD3 | DQ3L | DQ3L | DQ1L | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L39p | | Y2 | AD2 | DQ3L | DQ3L | DQ1L | DQ3L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L39n | | Y1 | AD1 | DQ3L | DQ3L | DQ1L | | | |
| B2 | VREFB2N1 | IO | | | | AB3 | | | | DQ3L | DQ3L | DQ1L |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B2 | VREFB2N1 | IO | VREFB2N1 | | T3 | T8 | | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L40p | | AA2 | AA4 | | | | DQ3L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L40n | | AA1 | AA3 | DQ3L | DQ3L | DQ1L | | | |
| B2 | VREFB2N1 | IO | RUP1 | | V4 | U7 | | | | | | |
| B2 | VREFB2N1 | IO | RDN1 | | V3 | U8 | | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L41p | | | AE2 | | | | DQ3L | DQ3L | DQ1L |
| B2 | VREFB2N1 | IO | DIFFIO_L41n | | | AE1 | | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L42p | | | V6 | | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L42n | | | V5 | | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L43p | | | V8 | | | | | | |
| B2 | VREFB2N1 | IO | DIFFIO_L43n | | | V7 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L44p | | | W4 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L44n | | | W3 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L45p | | | Y6 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L45n | | | Y5 | | | | | | |
| B2 | VREFB2N2 | IO | | | | W7 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L46p | | | W8 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L46n | | | Y7 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L47p | | | AA6 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L47n | | | AA5 | | | | | | |
| B2 | VREFB2N2 | IO | | | | AA7 | | | | | | |
| B2 | VREFB2N2 | IO | VREFB2N2 | | R5 | AB4 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L48p | | T4 | AE3 | DQS3L/CQ3L#, CDPCLK1 | DQS3L/CQ3L#, CDPCLK1 | DQS3L/CQ3L#, CDPCLK1 | DQS3L/CQ3L#, CDPCLK1 | DQS3L/CQ3L#, CDPCLK1 | DQS3L/CQ3L#, CDPCLK1 |
| B2 | VREFB2N2 | IO | DIFFIO_L48n | | T5 | AF2 | DM3L/BWS#3L | DM3L1/BWS#3L1 | DM1L3/BWS#1L3 | DM3L/BWS#3L | DM3L1/BWS#3L1 | DM1L3/BWS#1L3 |
| B2 | VREFB2N2 | IO | DIFFIO_L49p | | | AC5 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L49n | | | AC4 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L50p | | | AB6 | | | | | | |
| B2 | VREFB2N2 | IO | DIFFIO_L50n | | | AB5 | | | | | | |
| B2 | VREFB2N2 | VCCA1 | | | T6 | Y8 | | | | | | |
| B2 | VREFB2N2 | GNDA1 | | | U5 | AA9 | | | | | | |
| B2 | VREFB2N2 | VCCD_PLL1 | | | U6 | Y9 | | | | | | |
| B3 | VREFB3N2 | IO | DIFFIO_B1p | | | AD5 | | | | | | |
| B3 | VREFB3N2 | IO | DIFFIO_B1n | | V5 | AE6 | DM3B/BWS#3B | DM3B1/BWS#3B1 | DM5B3/BWS#5B3 | DM1B | | |
| B3 | VREFB3N2 | IO | DIFFIO_B2p | | | AD4 | | | | | | |
| B3 | VREFB3N2 | IO | DIFFIO_B2n | | | AF4 | | | | DQ1B | | |
| B3 | VREFB3N2 | IO | DIFFIO_B3p | | Y4 | AE4 | | | | | | |
| B3 | VREFB3N2 | IO | DIFFIO_B3n | | Y3 | AG3 | DQ3B | DQ3B | DQ5B | DQ1B | | |
| B3 | VREFB3N2 | IO | | | Y6 | AD7 | DQS1B/CQ1B#, CDPCLK2 | DQS1B/CQ1B#, CDPCLK2 | DQS1B/CQ1B#, CDPCLK2 | DQS1B/CQ1B#, CDPCLK2 | DQS1B/CQ1B#, CDPCLK2 | DQS1B/CQ1B#, CDPCLK2 |
| B3 | VREFB3N2 | IO | PLL1_CLKOUTp | | AA3 | AE5 | | | | | | |
| B3 | VREFB3N2 | IO | PLL1_CLKOUTn | | AB3 | AF5 | | | | | | |
| B3 | VREFB3N2 | IO | DIFFIO_B4p | | W6 | AH3 | DQ3B | DQ3B | DQ5B | DQ1B | | |
| B3 | VREFB3N2 | IO | DIFFIO_B4n | | | AF3 | | | | | | |
| B3 | VREFB3N2 | IO | | | AA4 | AF6 | DQ3B | DQ3B | DQ5B | DQ1B | | |
| B3 | VREFB3N2 | IO | VREFB3N2 | | AB4 | Y10 | | | | | | |
| B3 | VREFB3N2 | IO | DIFFIO_B5p | | AA5 | AG4 | DQ3B | DQ3B | DQ5B | | | |
| B3 | VREFB3N2 | IO | DIFFIO_B5n | | | AH4 | | | | DQ1B | | |
| B3 | VREFB3N2 | IO | DIFFIO_B6p | | | AD8 | | | | DQ1B | | |
| B3 | VREFB3N2 | IO | DIFFIO_B6n | | | AC7 | | | | | | |
| B3 | VREFB3N2 | IO | DIFFIO_B7p | | | AG6 | | | | DQ1B | | |
| B3 | VREFB3N2 | IO | DIFFIO_B7n | | AA6 | AH6 | | | | DQ1B | | |
| B3 | VREFB3N2 | IO | DIFFIO_B8p | | AB6 | AB9 | | | | DM3B/BWS#3B | DM3B1/BWS#3B1 | DM5B3/BWS#5B3 |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B3 | VREFB3N2 | IO | DIFFIO_B8n | | AB5 | AB8 | | | | | | |
| B3 | VREFB3N2 | IO | | | | AD10 | | | | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N2 | IO | DIFFIO_B9p | | W7 | AG7 | DQ3B | DQ3B | DQ5B | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B9n | | Y7 | AH7 | DQ3B | DQ3B | DQ5B | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B10p | | | AB7 | | | | | | |
| B3 | VREFB3N1 | IO | DIFFIO_B10n | | | AC8 | | | | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B11p | | | AA8 | | | | | | |
| B3 | VREFB3N1 | IO | DIFFIO_B11n | | | AA10 | | | | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B12p | | | AG8 | | | | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B12n | | U9 | AH8 | DQ3B | DQ3B | DQ5B | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B13p | | V8 | AE7 | DQ3B | DQ3B | DQ5B | | | |
| B3 | VREFB3N1 | IO | DIFFIO_B13n | | W8 | AF7 | DQ3B | DQ3B | DQ5B | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | | | | AF9 | | | | DQ3B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B14p | | AA7 | AE8 | DM5B/BWS#5B | DM3B0/BWS#3B0 | DM5B2/BWS#5B2 | | | |
| B3 | VREFB3N1 | IO | DIFFIO_B14n | | AB7 | AF8 | DQ5B | DQ3B | DQ5B | DM5B/BWS#5B | DM3B0/BWS#3B0 | DM5B2/BWS#5B2 |
| B3 | VREFB3N1 | IO | | | Y8 | AE9 | DQ5B | DQ3B | DQ5B | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | VREFB3N1 | | V9 | AB11 | | | | | | |
| B3 | VREFB3N1 | IO | DIFFIO_B15p | | V10 | AE10 | DQS3B/CQ3B#, DPCLK2 | DQS3B/CQ3B#, DPCLK2 | DQS3B/CQ3B#, DPCLK2 | DQS3B/CQ3B#, DPCLK2 | DQS3B/CQ3B#, DPCLK2 | DQS3B/CQ3B#, DPCLK2 |
| B3 | VREFB3N1 | IO | DIFFIO_B15n | | U10 | AF10 | DQ5B | DQ3B | DQ5B | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B16p | | | AG10 | | | | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B16n | | | AH10 | | | | | | |
| B3 | VREFB3N1 | IO | DIFFIO_B17p | | AA8 | AE12 | DQ5B | DQ3B | DQ5B | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B17n | | AB8 | AF12 | DQ5B | DQ3B | DQ5B | | | |
| B3 | VREFB3N1 | IO | DIFFIO_B18p | | AA9 | AE11 | DQ5B | DQ3B | DQ5B | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N1 | IO | DIFFIO_B18n | | AB9 | AF11 | DQS5B/CQ5B#, DPCLK3 | DQS5B/CQ5B#, DPCLK3 | DQS5B/CQ5B#, DPCLK3 | DQS5B/CQ5B#, DPCLK3 | DQS5B/CQ5B#, DPCLK3 | DQS5B/CQ5B#, DPCLK3 |
| B3 | VREFB3N1 | IO | DIFFIO_B19p | | | AB10 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B19n | | | AC10 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B20p | | | AG11 | | | | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N0 | IO | DIFFIO_B20n | | | AH11 | | | | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N0 | IO | DIFFIO_B21p | | | AE13 | | | | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N0 | IO | DIFFIO_B21n | | | AF13 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B22p | | | AC12 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B22n | | | AB12 | | | | | | |
| B3 | VREFB3N0 | IO | VREFB3N0 | | U11 | AB13 | | | | | | |
| B3 | VREFB3N0 | IO | | | V11 | AD12 | DQ5B | DQ3B | DQ5B | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B23p | | W10 | AE14 | DQ5B | DQ3B | DQ5B | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B23n | | Y10 | AF14 | DQ5B | DQ3B | DQ5B | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B24p | | AA10 | AC11 | DM4B | DM5B1/BWS#5B1 | DM5B1/BWS#5B1 | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B24n | | AB10 | AD11 | | DQ5B | DQ5B | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B25p | | | Y12 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B25n | | | AA12 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B26p | | | Y13 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B26n | | | AA13 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B27p | | | AA14 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B27n | | | AB14 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B28p | | | AG12 | | | | DQ5B | DQ3B | DQ5B |
| B3 | VREFB3N0 | IO | DIFFIO_B28n | | | AH12 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B29p | | | AC14 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B29n | | | AD14 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B30p | | | Y14 | | | | | | |
| B3 | VREFB3N0 | IO | DIFFIO_B30n | | | Y15 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B3 | VREFB3N0 | CLK15 | DIFFCLK_6p | | AA11 | AG14 | | | | | | |
| B3 | VREFB3N0 | CLK14 | DIFFCLK_6n | | AB11 | AH14 | | | | | | |
| B4 | VREFB4N2 | CLK13 | DIFFCLK_7p | | AA12 | AG15 | | | | | | |
| B4 | VREFB4N2 | CLK12 | DIFFCLK_7n | | AB12 | AH15 | | | | | | |
| B4 | VREFB4N2 | IO | DIFFIO_B31p | | | AC15 | | | | DM4B | DM5B1/BWS#5B1 | DM5B1/BWS#5B1 |
| B4 | VREFB4N2 | IO | DIFFIO_B31n | | | AD15 | | | | | | |
| B4 | VREFB4N2 | IO | DIFFIO_B32p | | AA13 | AE15 | DQ4B | DQ5B | DQ5B | | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B32n | | AB13 | AF15 | DQ4B | DQ5B | DQ5B | DQ4B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B33p | | | AG17 | | | | DQ4B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B33n | | | AH17 | | | | DQ4B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B34p | | | AE16 | | | | | | |
| B4 | VREFB4N2 | IO | DIFFIO_B34n | | | AF16 | | | | DQ4B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B35p | | AA14 | AA16 | DQ4B | DQ5B | DQ5B | | | |
| B4 | VREFB4N2 | IO | DIFFIO_B35n | | AB14 | AB16 | DQ4B | DQ5B | DQ5B | DQ4B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | VREFB4N2 | | V12 | AA15 | | | | | | |
| B4 | VREFB4N2 | IO | | | | AB15 | | | | | | |
| B4 | VREFB4N2 | IO | DIFFIO_B36p | | W13 | AE17 | DQ4B | DQ5B | DQ5B | DQ4B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B36n | | Y13 | AF17 | DQS4B/CQ5B, DPCLK4 | DQS4B/CQ5B, DPCLK4 | DQS4B/CQ5B, DPCLK4 | DQS4B/CQ5B, DPCLK4 | DQS4B/CQ5B, DPCLK4 | DQS4B/CQ5B, DPCLK4 |
| B4 | VREFB4N2 | IO | DIFFIO_B37p | | AA15 | AG18 | DQ4B | DQ5B | DQ5B | DQ4B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B37n | | AB15 | AH18 | DQ4B | DQ5B | DQ5B | DQ4B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B38p | | U12 | AG19 | DQ4B | DQ5B | DQ5B | | | |
| B4 | VREFB4N2 | IO | DIFFIO_B38n | | | AH19 | | | | DM2B | DM5B0/BWS#5B0 | DM5B0/BWS#5B0 |
| B4 | VREFB4N2 | IO | DIFFIO_B39p | | Y14 | AC17 | | | | | | |
| B4 | VREFB4N2 | IO | DIFFIO_B39n | | Y15 | AD17 | | | | DQ2B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B40p | | AA16 | AG21 | DM2B | DM5B0/BWS#5B0 | DM5B0/BWS#5B0 | DQ2B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B40n | | AB16 | AH21 | DQ2B | DQ5B | DQ5B | DQ2B | DQ5B | DQ5B |
| B4 | VREFB4N2 | IO | DIFFIO_B41p | | V13 | AE18 | DQS2B/CQ3B, DPCLK5 | DQS2B/CQ3B, DPCLK5 | DQS2B/CQ3B, DPCLK5 | DQS2B/CQ3B, DPCLK5 | DQS2B/CQ3B, DPCLK5 | DQS2B/CQ3B, DPCLK5 |
| B4 | VREFB4N1 | IO | DIFFIO_B41n | | W14 | AF18 | | | | | | |
| B4 | VREFB4N1 | IO | DIFFIO_B42p | | | AG22 | | | | DQ2B | DQ5B | DQ5B |
| B4 | VREFB4N1 | IO | DIFFIO_B42n | | | AH22 | | | | DQ2B | DQ5B | DQ5B |
| B4 | VREFB4N1 | IO | DIFFIO_B43p | | V14 | AG23 | DQ2B | DQ5B | DQ5B | | | |
| B4 | VREFB4N1 | IO | DIFFIO_B43n | | | AH23 | | | | DQ2B | DQ5B | DQ5B |
| B4 | VREFB4N1 | IO | DIFFIO_B44p | | U14 | AE19 | | | | DQ2B | DQ5B | DQ5B |
| B4 | VREFB4N1 | IO | DIFFIO_B44n | | V15 | AF19 | DQ2B | DQ5B | DQ5B | | | |
| B4 | VREFB4N1 | IO | DIFFIO_B45p | | W15 | AF24 | DQ2B | DQ5B | DQ5B | DQ2B | DQ5B | DQ5B |
| B4 | VREFB4N1 | IO | DIFFIO_B45n | | | AF25 | | | | DM0B | DQ5B | DQ5B |
| B4 | VREFB4N1 | IO | DIFFIO_B46p | | | AE20 | | | | | | |
| B4 | VREFB4N1 | IO | DIFFIO_B46n | | T15 | AF20 | DQ2B | DQ5B | DQ5B | DQ0B | | |
| B4 | VREFB4N1 | IO | | | AB18 | AD18 | DQ2B | DQ5B | DQ5B | DQ0B | | |
| B4 | VREFB4N1 | IO | DIFFIO_B47p | | AA17 | AE21 | | | | DQ0B | | |
| B4 | VREFB4N1 | IO | DIFFIO_B47n | | AB17 | AF21 | | | | | | |
| B4 | VREFB4N1 | IO | VREFB4N1 | | AA18 | AC18 | | | | | | |
| B4 | VREFB4N1 | IO | RUP2 | | AA19 | AA17 | | | | | | |
| B4 | VREFB4N1 | IO | RDN2 | | AB19 | AB17 | | | | | | |
| B4 | VREFB4N1 | IO | DIFFIO_B48p | | W17 | AE25 | DQ2B | DQ5B | DQ5B | DQ0B | | |
| B4 | VREFB4N1 | IO | DIFFIO_B48n | | Y17 | AF26 | DQS0B/CQ1B, CDPCLK3 | DQS0B/CQ1B, CDPCLK3 | DQS0B/CQ1B, CDPCLK3 | DQS0B/CQ1B, CDPCLK3 | DQS0B/CQ1B, CDPCLK3 | DQS0B/CQ1B, CDPCLK3 |
| B4 | VREFB4N1 | IO | DIFFIO_B49p | | AA20 | AG25 | | DQ5B | DQ5B | | | |
| B4 | VREFB4N1 | IO | DIFFIO_B49n | | AB20 | AH25 | DQ2B | DQ5B | DQ5B | DQ0B | | |
| B4 | VREFB4N0 | IO | DIFFIO_B50p | | | AC19 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B50n | | | AD19 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B4 | VREFB4N0 | IO | DIFFIO_B51p | | | Y17 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B51n | | | Y16 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B52p | | | AE22 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B52n | | | AF22 | | | | DQ0B | | |
| B4 | VREFB4N0 | IO | DIFFIO_B53p | | | AB19 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B53n | | | AB18 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B54p | | | AD25 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B54n | | | AE24 | | | | DQ0B | | |
| B4 | VREFB4N0 | IO | VREFB4N0 | | V16 | AB20 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B55p | | | AC21 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B55n | | | AD21 | | | | | | |
| B4 | VREFB4N0 | IO | | | | AD24 | | | | | | |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTp | | T16 | AE23 | | | | | | |
| B4 | VREFB4N0 | IO | PLL4_CLKOUTn | | R16 | AF23 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B56p | | | Y19 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B56n | | | AA19 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B57p | | | AB22 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B57n | | | AB21 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B58p | | | AC22 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B58n | | | AD22 | | | | | | |
| B4 | VREFB4N0 | IO | | | | AA21 | | | | | | |
| B4 | VREFB4N0 | IO | DIFFIO_B59p | | | AG26 | | | | DQ0B | | |
| B4 | VREFB4N0 | IO | DIFFIO_B59n | | | AH26 | | | | | | |
| B5 | VREFB5N2 | VCCD_PLL4 | | | V17 | Y20 | | | | | | |
| B5 | VREFB5N2 | GNDA4 | | | V18 | AA20 | | | | | | |
| B5 | VREFB5N2 | VCCA4 | | | U18 | Y21 | | | | | | |
| B5 | VREFB5N2 | IO | DIFFIO_R51n | | AA22 | AC25 | | | | | | |
| B5 | VREFB5N2 | IO | DIFFIO_R51p | | AA21 | AC24 | DM3R/BWS#3R | DM3R1/BWS#3R1 | DM1R3/BWS#1R3 | | | |
| B5 | VREFB5N2 | IO | | | | AB24 | | | | DM3R/BWS#3R | DM3R1/BWS#3R1 | DM1R3/BWS#1R3 |
| B5 | VREFB5N2 | IO | RUP3 | | T17 | AA22 | | | | | | |
| B5 | VREFB5N2 | IO | RDN3 | | T18 | AB23 | | | | | | |
| B5 | VREFB5N2 | IO | DIFFIO_R50n | | W20 | AF27 | DQS3R/CQ3R#, CDPCLK4 | DQS3R/CQ3R#, CDPCLK4 | DQS3R/CQ3R#, CDPCLK4 | DQS3R/CQ3R#, CDPCLK4 | DQS3R/CQ3R#, CDPCLK4 | DQS3R/CQ3R#, CDPCLK4 |
| B5 | VREFB5N2 | IO | DIFFIO_R50p | | | AE26 | | | | | | |
| B5 | VREFB5N2 | IO | VREFB5N2 | | W19 | AA24 | | | | | | |
| B5 | VREFB5N2 | IO | | | | AA23 | | | | | | |
| B5 | VREFB5N2 | IO | DIFFIO_R49n | | Y22 | AD26 | DQ3R | DQ3R | DQ1R | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N2 | IO | DIFFIO_R49p | | R17 | AC26 | | | | | | |
| B5 | VREFB5N2 | IO | DIFFIO_R48n | | U20 | AE28 | DQ3R | DQ3R | DQ1R | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N2 | IO | DIFFIO_R48p | | M16 | AE27 | | | | | | |
| B5 | VREFB5N2 | IO | DIFFIO_R47n | | | AD28 | | | | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N2 | IO | DIFFIO_R47p | | | AD27 | | | | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N2 | IO | DIFFIO_R46n | | W22 | Y24 | DQ3R | DQ3R | DQ1R | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N2 | IO | DIFFIO_R46p | | W21 | Y23 | DQ3R | DQ3R | DQ1R | | | |
| B5 | VREFB5N2 | IO | DIFFIO_R45n | | T20 | AC28 | | | | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N2 | IO | DIFFIO_R45p | | T19 | AC27 | | | | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R44n | | | AB26 | | | | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R44p | | | AB25 | | | | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R43n | | V22 | AA26 | DQ3R | DQ3R | DQ1R | DQ3R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R43p | | V21 | AA25 | DQ3R | DQ3R | DQ1R | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R42n | | R20 | AB28 | DQ3R | DQ3R | DQ1R | DM1R/BWS#1R | DM3R0/BWS#3R0 | DM1R2/BWS#1R2 |
| B5 | VREFB5N1 | IO | DIFFIO_R42p | | | AB27 | | | | DQ1R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R41n | | U22 | Y26 | DQ3R | DQ3R | DQ1R | DQ1R | DQ3R | DQ1R |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B5 | VREFB5N1 | IO | DIFFIO_R41p | | U21 | Y25 | DQ3R | DQ3R | DQ1R | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R40n | | | W26 | | | | DQ1R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R40p | | R19 | W25 | DM1R/BWS#1R | DM3R0/BWS#3R0 | DM1R2/BWS#1R2 | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R39n | | | W27 | | | | DQ1R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R39p | | | W28 | | | | DQ1R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R38n | | R22 | V28 | DQ1R | DQ3R | DQ1R | DQ1R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R38p | | R21 | V27 | DQ1R | DQ3R | DQ1R | | | |
| B5 | VREFB5N1 | IO | VREFB5N1 | | P20 | U23 | | | | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R37n | | | V26 | | | | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R37p | | | V25 | | | | DQ1R | DQ3R | DQ1R |
| B5 | VREFB5N1 | IO | DIFFIO_R36n | | P22 | V24 | DQ1R | DQ3R | DQ1R | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R36p | | P21 | V23 | DQ1R | DQ3R | DQ1R | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R35n | | | W21 | | | | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R35p | | | V21 | | | | | | |
| B5 | VREFB5N1 | IO | DIFFIO_R34n | | | V22 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R34p | | | U22 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R33n | | N20 | U26 | DQ1R | DQ3R | DQ1R | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R33p | | | U25 | | | | | | |
| B5 | VREFB5N0 | IO | VREFB5N0 | | N19 | U24 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R32n | | | U28 | | | | DQ1R | DQ3R | DQ1R |
| B5 | VREFB5N0 | IO | DIFFIO_R32p | | | U27 | | | | | | |
| B5 | VREFB5N0 | IO | | | | U21 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R31n | | | Y22 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R31p | | | W22 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R30n | | | T26 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R30p | | N18 | T25 | DQS1R/CQ1R#, DPCLK6 | DQS1R/CQ1R#, DPCLK6 | DQS1R/CQ1R#, DPCLK6 | DQS1R/CQ1R#, DPCLK6 | DQS1R/CQ1R#, DPCLK6 | DQS1R/CQ1R#, DPCLK6 |
| B5 | VREFB5N0 | IO | DIFFIO_R29n | DEV_OE | N22 | T22 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R29p | DEV_CLRn | N21 | T21 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R28n | | M22 | R26 | DQ1R | DQ3R | DQ1R | DQ1R | DQ3R | DQ1R |
| B5 | VREFB5N0 | IO | DIFFIO_R28p | | M21 | R25 | DQ1R | DQ3R | DQ1R | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R27n | | M20 | R28 | DQ1R | DQ3R | DQ1R | DM0R | DM1R1/BWS#1R1 | DM1R1/BWS#1R1 |
| B5 | VREFB5N0 | IO | DIFFIO_R27p | | M19 | R27 | DQ1R | DQ3R | DQ1R | | DQ1R | DQ1R |
| B5 | VREFB5N0 | IO | | | | R24 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R26n | | | R23 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R26p | | | R22 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R25n | | | R21 | | | | | | |
| B5 | VREFB5N0 | IO | DIFFIO_R25p | | | P21 | | | | | | |
| B5 | VREFB5N0 | CLK7 | DIFFCLK_3n | | T22 | Y28 | | | | | | |
| B5 | VREFB5N0 | CLK6 | DIFFCLK_3p | | T21 | Y27 | | | | | | |
| B6 | VREFB6N2 | CLK5 | DIFFCLK_2n | | G22 | J28 | | | | | | |
| B6 | VREFB6N2 | CLK4 | DIFFCLK_2p | | G21 | J27 | | | | | | |
| B6 | VREFB6N2 | CONF_DONE | | CONF_DONE | M18 | P24 | | | | | | |
| B6 | VREFB6N2 | MSEL0 | | MSEL0 | M17 | N22 | | | | | | |
| B6 | VREFB6N2 | MSEL1 | | MSEL1 | L18 | P23 | | | | | | |
| B6 | VREFB6N2 | MSEL2 | | MSEL2 | L17 | M22 | | | | | | |
| B6 | VREFB6N2 | MSEL3 | | MSEL3 | K20 | P22 | | | | | | |
| B6 | VREFB6N2 | IO | | | | M23 | | | | | | |
| B6 | VREFB6N2 | IO | DIFFIO_R24n | INIT_DONE | L22 | P26 | | | | | | |
| B6 | VREFB6N2 | IO | DIFFIO_R24p | CRC_ERROR | L21 | P25 | | | | | | |
| B6 | VREFB6N2 | IO | | | | M24 | | | | | | |
| B6 | VREFB6N2 | IO | VREFB6N2 | | K19 | N21 | | | | | | |
| B6 | VREFB6N2 | IO | DIFFIO_R23n | nCEO | K22 | P28 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B6 | VREFB6N2 | IO | DIFFIO_R23p | CLKUSR | K21 | P27 | | | | | | |
| B6 | VREFB6N2 | IO | DIFFIO_R22n | | J22 | N26 | DQS0R/CQ1R, DPCLK7 | DQS0R/CQ1R, DPCLK7 | DQS0R/CQ1R, DPCLK7 | DQS0R/CQ1R, DPCLK7 | DQS0R/CQ1R, DPCLK7 | DQS0R/CQ1R, DPCLK7 |
| B6 | VREFB6N2 | IO | DIFFIO_R22p | | J21 | N25 | DM0R | DM1R1/BWS#1R1 | DM1R1/BWS#1R1 | | | |
| B6 | VREFB6N2 | IO | DIFFIO_R21n | | H22 | M28 | DQ0R | DQ1R | DQ1R | DQ0R | DQ1R | DQ1R |
| B6 | VREFB6N2 | IO | DIFFIO_R21p | | H21 | M27 | DQ0R | DQ1R | DQ1R | DQ0R | DQ1R | DQ1R |
| B6 | VREFB6N2 | IO | DIFFIO_R20n | | K18 | M26 | DQ0R | DQ1R | DQ1R | DQ0R | DQ1R | DQ1R |
| B6 | VREFB6N2 | IO | DIFFIO_R20p | | J18 | M25 | | | | | | |
| B6 | VREFB6N2 | IO | DIFFIO_R19n | | | L28 | | | | DQ0R | DQ1R | DQ1R |
| B6 | VREFB6N2 | IO | DIFFIO_R19p | | | L27 | | | | DQ0R | DQ1R | DQ1R |
| B6 | VREFB6N2 | IO | DIFFIO_R18n | | F22 | L24 | DQ0R | DQ1R | DQ1R | DQ0R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | DIFFIO_R18p | | F21 | L23 | DQ0R | DQ1R | DQ1R | | | |
| B6 | VREFB6N1 | IO | DIFFIO_R17n | | J20 | K28 | | | | DQ0R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | DIFFIO_R17p | | | K27 | | | | DQ0R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | | | | L26 | | | | DM2R | DM1R0/BWS#1R0 | DM1R0/BWS#1R0 |
| B6 | VREFB6N1 | IO | DIFFIO_R16n | | H20 | J26 | DQ0R | DQ1R | DQ1R | | | |
| B6 | VREFB6N1 | IO | DIFFIO_R16p | | H19 | J25 | DQ0R | DQ1R | DQ1R | | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | DIFFIO_R15n | nWE | E22 | G28 | DQ0R | DQ1R | DQ1R | DQ2R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | DIFFIO_R15p | nOE | E21 | G27 | | DQ1R | DQ1R | DQ2R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | VREFB6N1 | | H18 | M21 | | | | | | |
| B6 | VREFB6N1 | IO | | | | L25 | | | | | | |
| B6 | VREFB6N1 | IO | DIFFIO_R14n | | D22 | K26 | DM2R | DM1R0/BWS#1R0 | DM1R0/BWS#1R0 | DQ2R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | DIFFIO_R14p | | D21 | K25 | | DQ1R | DQ1R | | | |
| B6 | VREFB6N1 | IO | DIFFIO_R13n | nAVD | F20 | F28 | DQ2R | DQ1R | DQ1R | DQ2R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | DIFFIO_R13p | | F19 | F27 | DQ2R | DQ1R | DQ1R | | | |
| B6 | VREFB6N1 | IO | DIFFIO_R12n | PADD23 | G18 | E28 | DQ2R | DQ1R | DQ1R | DQ2R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | DIFFIO_R12p | | | E27 | | | | DQ2R | DQ1R | DQ1R |
| B6 | VREFB6N1 | IO | DIFFIO_R11n | | | H26 | | | | | | |
| B6 | VREFB6N1 | IO | DIFFIO_R11p | | | H25 | | | | | | |
| B6 | VREFB6N1 | IO | DIFFIO_R10n | | C22 | E26 | DQ2R | DQ1R | DQ1R | | | |
| B6 | VREFB6N1 | IO | DIFFIO_R10p | | C21 | F26 | DQ2R | DQ1R | DQ1R | DQ2R | DQ1R | DQ1R |
| B6 | VREFB6N0 | IO | DIFFIO_R9n | PADD22 | B22 | D28 | DQ2R | DQ1R | DQ1R | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R9p | PADD21 | B21 | D27 | DQ2R | DQ1R | DQ1R | DQ2R | DQ1R | DQ1R |
| B6 | VREFB6N0 | IO | DIFFIO_R8n | PADD20 | C20 | C27 | DQS2R/CQ3R, CDPCLK5 | DQS2R/CQ3R, CDPCLK5 | DQS2R/CQ3R, CDPCLK5 | DQS2R/CQ3R, CDPCLK5 | DQS2R/CQ3R, CDPCLK5 | DQS2R/CQ3R, CDPCLK5 |
| B6 | VREFB6N0 | IO | DIFFIO_R8p | | | D26 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R7n | | | L22 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R7p | | | L21 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R6n | | | J24 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R6p | | | J23 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R5n | | | K22 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R5p | | | K21 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R4n | | | H24 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R4p | | | H23 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R3n | | | G26 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R3p | | | G25 | | | | | | |
| B6 | VREFB6N0 | IO | VREFB6N0 | | D20 | J22 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R2n | | F17 | F25 | DQ2R | DQ1R | DQ1R | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R2p | | | F24 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R1n | | | G24 | | | | | | |
| B6 | VREFB6N0 | IO | DIFFIO_R1p | | | G23 | | | | | | |
| B6 | VREFB6N0 | IO | | | | H22 | | | | | | |
| B6 | VREFB6N0 | VCCA2 | | | F18 | J21 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B6 | VREFB6N0 | GNDA2 | | | E18 | H20 | | | | | | |
| B6 | VREFB6N0 | VCCD_PLL2 | | | E17 | J20 | | | | | | |
| B7 | VREFB7N0 | IO | DIFFIO_T61n | | | C26 | | | | | | |
| B7 | VREFB7N0 | IO | DIFFIO_T61p | | | B26 | | | | DQ0T | | |
| B7 | VREFB7N0 | IO | DIFFIO_T60n | | E16 | D22 | DQ2T | DQ5T | DQ5T | DQ0T | | |
| B7 | VREFB7N0 | IO | DIFFIO_T60p | | F15 | E22 | DQ2T | DQ5T | DQ5T | DQ0T | | |
| B7 | VREFB7N0 | IO | DIFFIO_T59n | | | A26 | | | | DQ0T | | |
| B7 | VREFB7N0 | IO | DIFFIO_T59p | | F14 | A25 | DQS0T/CQ1T, CDPCLK6 | DQS0T/CQ1T, CDPCLK6 | DQS0T/CQ1T, CDPCLK6 | DQS0T/CQ1T, CDPCLK6 | DQS0T/CQ1T, CDPCLK6 | DQS0T/CQ1T, CDPCLK6 |
| B7 | VREFB7N0 | IO | | | | B25 | | | | DQ0T | | |
| B7 | VREFB7N0 | IO | DIFFIO_T58n | | C18 | E21 | | | | | | |
| B7 | VREFB7N0 | IO | DIFFIO_T58p | | D18 | F21 | | | | DQ0T | | |
| B7 | VREFB7N0 | IO | VREFB7N0 | | D17 | F22 | | | | | | |
| B7 | VREFB7N0 | IO | DIFFIO_T57n | | | D25 | | | | | | |
| B7 | VREFB7N0 | IO | DIFFIO_T57p | | | C25 | | | | DQ0T | | |
| B7 | VREFB7N0 | IO | DIFFIO_T56n | | C19 | A23 | DQ2T | DQ5T | DQ5T | DQ0T | | |
| B7 | VREFB7N0 | IO | DIFFIO_T56p | | D19 | B23 | DQ2T | DQ5T | DQ5T | DM0T | | |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTp | | B20 | D23 | | | | | | |
| B7 | VREFB7N0 | IO | PLL2_CLKOUTn | | A20 | C23 | | | | | | |
| B7 | VREFB7N0 | IO | DIFFIO_T55n | | | C24 | | | | DQ2T | DQ5T | DQ5T |
| B7 | VREFB7N0 | IO | DIFFIO_T55p | | | D24 | | | | | | |
| B7 | VREFB7N0 | IO | DIFFIO_T54n | | | C22 | | | | DQ2T | DQ5T | DQ5T |
| B7 | VREFB7N0 | IO | DIFFIO_T54p | | C17 | D21 | DQ2T | DQ5T | DQ5T | DQ2T | DQ5T | DQ5T |
| B7 | VREFB7N0 | IO | RUP4 | | B19 | F19 | | | | | | |
| B7 | VREFB7N0 | IO | RDN4 | | A19 | E19 | | | | | | |
| B7 | VREFB7N0 | IO | | | | C21 | | | | DQ2T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T53n | | A18 | A22 | DQ2T | DQ5T | DQ5T | DQ2T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T53p | PADD0 | B18 | B22 | | | | | | |
| B7 | VREFB7N1 | IO | DIFFIO_T52n | | D15 | A21 | | | | DQ2T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T52p | | E15 | B21 | DQ2T | DQ5T | DQ5T | DQ2T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T51n | | | E18 | | | | DQ2T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T51p | | | F18 | | | | | | |
| B7 | VREFB7N1 | IO | DIFFIO_T50n | PADD1 | A17 | C18 | DQ2T | DQ5T | DQ5T | | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T50p | PADD2 | B17 | D18 | | DQ5T | DQ5T | | | |
| B7 | VREFB7N1 | IO | DIFFIO_T49n | | A16 | C20 | DM2T | DM5T0/BWS#5T0 | DM5T0/BWS#5T0 | DM2T | DM5T0/BWS#5T0 | DM5T0/BWS#5T0 |
| B7 | VREFB7N1 | IO | DIFFIO_T49p | | B16 | D20 | DQ4T | DQ5T | DQ5T | DQ4T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T48n | | | E24 | | | | | | |
| B7 | VREFB7N1 | IO | DIFFIO_T48p | | | E25 | | | | | | |
| B7 | VREFB7N1 | IO | DIFFIO_T47n | | | C19 | | | | DQ4T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T47p | | | D19 | | | | | | |
| B7 | VREFB7N1 | IO | VREFB7N1 | | C15 | G17 | | | | | | |
| B7 | VREFB7N1 | IO | DIFFIO_T46n | PADD3 | E14 | C17 | DQ4T | DQ5T | DQ5T | DQ4T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T46p | PADD4 | F13 | D17 | DQS2T/CQ3T, DPCLK8 | DQS2T/CQ3T, DPCLK8 | DQS2T/CQ3T, DPCLK8 | DQS2T/CQ3T, DPCLK8 | DQS2T/CQ3T, DPCLK8 | DQS2T/CQ3T, DPCLK8 |
| B7 | VREFB7N1 | IO | DIFFIO_T45n | PADD5 | A15 | A19 | DQ4T | DQ5T | DQ5T | DQ4T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T45p | PADD6 | B15 | B19 | DQ4T | DQ5T | DQ5T | DQ4T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T44n | PADD7 | C13 | A18 | | | | | | |
| B7 | VREFB7N1 | IO | DIFFIO_T44p | PADD8 | D13 | B18 | DQ4T | DQ5T | DQ5T | DQ4T | DQ5T | DQ5T |
| B7 | VREFB7N1 | IO | DIFFIO_T43n | | | G20 | | | | | | |
| B7 | VREFB7N1 | IO | DIFFIO_T43p | | | G21 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T42n | | | H19 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T42p | | | J19 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T41n | | | H21 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B7 | VREFB7N2 | IO | DIFFIO_T41p | | | G22 | | | | | | |
| B7 | VREFB7N2 | IO | | | | J17 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T40n | | | G19 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T40p | | | G18 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T39n | | | G16 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T39p | | | H17 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T38n | | | F17 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T38p | | | E17 | | | | DQ4T | DQ5T | DQ5T |
| B7 | VREFB7N2 | IO | VREFB7N2 | | E13 | G15 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T37n | | | J16 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T37p | | | H16 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T36n | PADD9 | A14 | C16 | DQ4T | DQ5T | DQ5T | DQ4T | DQ5T | DQ5T |
| B7 | VREFB7N2 | IO | DIFFIO_T36p | PADD10 | B14 | D16 | DQ4T | DQ5T | DQ5T | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T35n | PADD11 | A13 | A17 | DQ4T | DQ5T | DQ5T | | DQ5T | DQ5T |
| B7 | VREFB7N2 | IO | DIFFIO_T35p | PADD12 | B13 | B17 | DQS4T/CQ5T, DPCLK9 | DQS4T/CQ5T, DPCLK9 | DQS4T/CQ5T, DPCLK9 | DQS4T/CQ5T, DPCLK9 | DQS4T/CQ5T, DPCLK9 | DQS4T/CQ5T, DPCLK9 |
| B7 | VREFB7N2 | IO | DIFFIO_T34n | | | H15 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T34p | | | J15 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T33n | | | F15 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T33p | | E12 | E15 | | DQ5T | DQ5T | DM4T | DM5T1/BWS#5T1 | DM5T1/BWS#5T1 |
| B7 | VREFB7N2 | IO | DIFFIO_T32n | PADD13 | E11 | C15 | | | | | | |
| B7 | VREFB7N2 | IO | DIFFIO_T32p | PADD14 | F11 | D15 | DM4T | DM5T1/BWS#5T1 | DM5T1/BWS#5T1 | DQ5T | DQ3T | DQ5T |
| B7 | VREFB7N2 | CLK8 | DIFFCLK_5n | | A12 | A15 | | | | | | |
| B7 | VREFB7N2 | CLK9 | DIFFCLK_5p | | B12 | B15 | | | | | | |
| B8 | VREFB8N0 | CLK10 | DIFFCLK_4n | | A11 | A14 | | | | | | |
| B8 | VREFB8N0 | CLK11 | DIFFCLK_4p | | B11 | B14 | | | | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T31n | | D10 | C13 | DQ5T | DQ3T | DQ5T | DQ5T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T31p | | | D13 | | | | DQ5T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T30n | | A10 | C14 | DQ5T | DQ3T | DQ5T | DQ5T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T30p | PADD15 | B10 | D14 | | | | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T29n | PADD16 | A9 | C12 | DQ5T | DQ3T | DQ5T | DQ5T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T29p | PADD17 | B9 | D12 | DQS5T/CQ5T#, DPCLK10 | DQS5T/CQ5T#, DPCLK10 | DQS5T/CQ5T#, DPCLK10 | DQS5T/CQ5T#, DPCLK10 | DQS5T/CQ5T#, DPCLK10 | DQS5T/CQ5T#, DPCLK10 |
| B8 | VREFB8N0 | IO | DIFFIO_T28n | | | H14 | | | | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T28p | | | J14 | | | | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T27n | | | A12 | | | | DQ5T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T27p | | | B12 | | | | | | |
| B8 | VREFB8N0 | IO | VREFB8N0 | | C10 | G14 | | | | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T26n | | | F14 | | | | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T26p | | | E14 | | | | DQ5T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T25n | DATA2 | A8 | A11 | DQ5T | DQ3T | DQ5T | DQ5T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T25p | DATA3 | B8 | B11 | DQ5T | DQ3T | DQ5T | DQ5T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T24n | | | J13 | | | | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T24p | | | J12 | | | | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T23n | PADD18 | A7 | A10 | DQ5T | DQ3T | DQ5T | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T23p | DATA4 | B7 | B10 | DQ5T | DQ3T | DQ5T | DM5T/BWS#5T | DM3T0/BWS#3T0 | DM5T2/BWS#5T2 |
| B8 | VREFB8N0 | IO | DIFFIO_T22n | PADD19 | A6 | G13 | DQ5T | DQ3T | DQ5T | | | |
| B8 | VREFB8N0 | IO | DIFFIO_T22p | DATA15 | B6 | H13 | DQ5T | DQ3T | DQ5T | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N0 | IO | DIFFIO_T21n | | E9 | C10 | | | | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N1 | IO | DIFFIO_T21p | | | D10 | | | | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N1 | IO | DIFFIO_T20n | DATA14 | C8 | E12 | DQS3T/CQ3T#, DPCLK11 | DQS3T/CQ3T#, DPCLK11 | DQS3T/CQ3T#, DPCLK11 | DQS3T/CQ3T#, DPCLK11 | DQS3T/CQ3T#, DPCLK11 | DQS3T/CQ3T#, DPCLK11 |
| B8 | VREFB8N1 | IO | DIFFIO_T20p | DATA13 | C7 | F12 | DM5T/BWS#5T | DM3T0/BWS#3T0 | DM5T2/BWS#5T2 | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| B8 | VREFB8N1 | IO | DIFFIO_T19n | | D8 | E11 | | | | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N1 | IO | DIFFIO_T19p | | E8 | F11 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T18n | | | A7 | | | | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N1 | IO | DIFFIO_T18p | DATA5 | A5 | B7 | DQ3T | DQ3T | DQ5T | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N1 | IO | VREFB8N1 | | B5 | G12 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T17n | | | A6 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T17p | DATA6 | F10 | B6 | DQ3T | DQ3T | DQ5T | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N1 | IO | DIFFIO_T16n | | | G11 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T16p | | | H12 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T15n | DATA7 | C6 | C11 | DQ3T | DQ3T | DQ5T | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N1 | IO | DIFFIO_T15p | | D7 | D11 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T14n | | A4 | C9 | DQ3T | DQ3T | DQ5T | DQ3T | DQ3T | DQ5T |
| B8 | VREFB8N1 | IO | DIFFIO_T14p | DATA8 | B4 | D9 | DQ3T | DQ3T | DQ5T | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T13n | | | F10 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T13p | | | G10 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T12n | | | H10 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T12p | | | J10 | | | | | | |
| B8 | VREFB8N1 | IO | | | | E10 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T11n | DATA9 | F8 | A8 | DQ3T | DQ3T | DQ5T | DM3T/BWS#3T | DM3T1/BWS#3T1 | DM5T3/BWS#5T3 |
| B8 | VREFB8N1 | IO | DIFFIO_T11p | | | B8 | | | | | | |
| B8 | VREFB8N1 | IO | DIFFIO_T10n | | | C8 | | | | DQ1T | | |
| B8 | VREFB8N2 | IO | DIFFIO_T10p | | | D8 | | | | DQ1T | | |
| B8 | VREFB8N2 | IO | DIFFIO_T9n | DATA10 | A3 | C7 | DQ3T | DQ3T | DQ5T | DQ1T | | |
| B8 | VREFB8N2 | IO | DIFFIO_T9p | DATA11 | B3 | D7 | DQ3T | DQ3T | DQ5T | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T8n | | | E7 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T8p | | | D6 | | | | DQ1T | | |
| B8 | VREFB8N2 | IO | VREFB8N2 | | D6 | G9 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T7n | | E7 | E8 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T7p | | | F8 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T6n | | | G8 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T6p | | | H8 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T5n | | | G7 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T5p | | | F7 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T4n | | C3 | A4 | DQ3T | DQ3T | DQ5T | DQ1T | | |
| B8 | VREFB8N2 | IO | DIFFIO_T4p | DATA12 | C4 | B4 | DQS1T/CQ1T#, CDPCLK7 | DQS1T/CQ1T#, CDPCLK7 | DQS1T/CQ1T#, CDPCLK7 | DQS1T/CQ1T#, CDPCLK7 | DQS1T/CQ1T#, CDPCLK7 | DQS1T/CQ1T#, CDPCLK7 |
| B8 | VREFB8N2 | IO | DIFFIO_T3n | | F7 | B3 | DM3T/BWS#3T | DM3T1/BWS#3T1 | DM5T3/BWS#5T3 | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T3p | | | A3 | | | | DQ1T | | |
| B8 | VREFB8N2 | IO | | | F9 | C6 | | | | DQ1T | | |
| B8 | VREFB8N2 | IO | PLL3_CLKOUTp | | E5 | D5 | | | | | | |
| B8 | VREFB8N2 | IO | PLL3_CLKOUTn | | E6 | C5 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T2n | | | C4 | | | | DQ1T | | |
| B8 | VREFB8N2 | IO | DIFFIO_T2p | | | D4 | | | | DM1T | | |
| B8 | VREFB8N2 | IO | DIFFIO_T1n | | | E4 | | | | | | |
| B8 | VREFB8N2 | IO | DIFFIO_T1p | | | E5 | | | | | | |
| B8 | VREFB8N2 | IO | | | | C3 | | | | | | |
| | | VCCINT | | | J11 | K9 | | | | | | |
| | | VCCINT | | | J12 | K11 | | | | | | |
| | | VCCINT | | | L14 | K13 | | | | | | |
| | | VCCINT | | | M14 | K15 | | | | | | |
| | | VCCINT | | | P11 | K17 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | VCCINT | | | P12 | K19 | | | | | | |
| | | VCCINT | | | L9 | L10 | | | | | | |
| | | VCCINT | | | M9 | L12 | | | | | | |
| | | VCCINT | | | J13 | L14 | | | | | | |
| | | VCCINT | | | J14 | L16 | | | | | | |
| | | VCCINT | | | K14 | L18 | | | | | | |
| | | VCCINT | | | J10 | L20 | | | | | | |
| | | VCCINT | | | K9 | M9 | | | | | | |
| | | VCCINT | | | N9 | M11 | | | | | | |
| | | VCCINT | | | P9 | M13 | | | | | | |
| | | VCCINT | | | P10 | M15 | | | | | | |
| | | VCCINT | | | P13 | M17 | | | | | | |
| | | VCCINT | | | P14 | M19 | | | | | | |
| | | VCCINT | | | N14 | N10 | | | | | | |
| | | VCCINT | | | J16 | N12 | | | | | | |
| | | VCCINT | | | K15 | N14 | | | | | | |
| | | VCCINT | | | L16 | N16 | | | | | | |
| | | VCCINT | | | M15 | N18 | | | | | | |
| | | VCCINT | | | R12 | N20 | | | | | | |
| | | VCCINT | | | R10 | P9 | | | | | | |
| | | VCCINT | | | R8 | P11 | | | | | | |
| | | VCCINT | | | H9 | P13 | | | | | | |
| | | VCCINT | | | G12 | P15 | | | | | | |
| | | VCCINT | | | J8 | P17 | | | | | | |
| | | VCCINT | | | M8 | P19 | | | | | | |
| | | VCCINT | | | T7 | R10 | | | | | | |
| | | VCCINT | | | T9 | R12 | | | | | | |
| | | VCCINT | | | T13 | R14 | | | | | | |
| | | VCCINT | | | P15 | R16 | | | | | | |
| | | VCCINT | | | H15 | R18 | | | | | | |
| | | VCCINT | | | H11 | R20 | | | | | | |
| | | VCCINT | | | K8 | T9 | | | | | | |
| | | VCCINT | | | P17 | T11 | | | | | | |
| | | VCCINT | | | L7 | T13 | | | | | | |
| | | VCCINT | | | N16 | T15 | | | | | | |
| | | VCCINT | | | K17 | T17 | | | | | | |
| | | VCCINT | | | J17 | T19 | | | | | | |
| | | VCCINT | | | G16 | U10 | | | | | | |
| | | VCCINT | | | G14 | U12 | | | | | | |
| | | VCCINT | | | G10 | U14 | | | | | | |
| | | VCCINT | | | G8 | U16 | | | | | | |
| | | VCCINT | | | J7 | U18 | | | | | | |
| | | VCCINT | | | N7 | U20 | | | | | | |
| | | VCCINT | | | P7 | V9 | | | | | | |
| | | VCCINT | | | R6 | V11 | | | | | | |
| | | VCCINT | | | U8 | V13 | | | | | | |
| | | VCCINT | | | V7 | V15 | | | | | | |
| | | VCCINT | | | T11 | V17 | | | | | | |
| | | VCCINT | | | R15 | V19 | | | | | | |
| | | VCCINT | | | G4 | W10 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | VCCINT | | | H17 | W12 | | | | | | |
| | | VCCINT | | | U17 | W14 | | | | | | |
| | | VCCINT | | | U16 | W16 | | | | | | |
| | | VCCINT | | | U15 | W18 | | | | | | |
| | | VCCINT | | | R14 | W20 | | | | | | |
| | | VCCIO1 | | | D4 | B1 | | | | | | |
| | | VCCIO1 | | | F4 | H1 | | | | | | |
| | | VCCIO1 | | | K4 | K5 | | | | | | |
| | | VCCIO1 | | | | N1 | | | | | | |
| | | VCCIO1 | | | | N5 | | | | | | |
| | | VCCIO2 | | | N4 | AA1 | | | | | | |
| | | VCCIO2 | | | U4 | AG1 | | | | | | |
| | | VCCIO2 | | | W4 | T1 | | | | | | |
| | | VCCIO2 | | | | T5 | | | | | | |
| | | VCCIO2 | | | | W5 | | | | | | |
| | | VCCIO3 | | | AB2 | AA11 | | | | | | |
| | | VCCIO3 | | | W5 | AD6 | | | | | | |
| | | VCCIO3 | | | W9 | AD9 | | | | | | |
| | | VCCIO3 | | | W11 | AD13 | | | | | | |
| | | VCCIO3 | | | | AH2 | | | | | | |
| | | VCCIO3 | | | | AH5 | | | | | | |
| | | VCCIO3 | | | | AH9 | | | | | | |
| | | VCCIO3 | | | | AH13 | | | | | | |
| | | VCCIO4 | | | AB21 | AA18 | | | | | | |
| | | VCCIO4 | | | W12 | AD16 | | | | | | |
| | | VCCIO4 | | | W16 | AD20 | | | | | | |
| | | VCCIO4 | | | W18 | AD23 | | | | | | |
| | | VCCIO4 | | | | AH16 | | | | | | |
| | | VCCIO4 | | | | AH20 | | | | | | |
| | | VCCIO4 | | | | AH24 | | | | | | |
| | | VCCIO4 | | | | AH27 | | | | | | |
| | | VCCIO5 | | | P18 | AA28 | | | | | | |
| | | VCCIO5 | | | V19 | AG28 | | | | | | |
| | | VCCIO5 | | | Y19 | T24 | | | | | | |
| | | VCCIO5 | | | | T28 | | | | | | |
| | | VCCIO5 | | | | W24 | | | | | | |
| | | VCCIO6 | | | E19 | B28 | | | | | | |
| | | VCCIO6 | | | G19 | H28 | | | | | | |
| | | VCCIO6 | | | L19 | K24 | | | | | | |
| | | VCCIO6 | | | | N24 | | | | | | |
| | | VCCIO6 | | | | N28 | | | | | | |
| | | VCCIO7 | | | A21 | A16 | | | | | | |
| | | VCCIO7 | | | D12 | A20 | | | | | | |
| | | VCCIO7 | | | D14 | A24 | | | | | | |
| | | VCCIO7 | | | D16 | A27 | | | | | | |
| | | VCCIO7 | | | | E16 | | | | | | |
| | | VCCIO7 | | | | E20 | | | | | | |
| | | VCCIO7 | | | | E23 | | | | | | |
| | | VCCIO7 | | | | H18 | | | | | | |
| | | VCCIO8 | | | A2 | A2 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | VCCIO8 | | | D5 | A5 | | | | | | |
| | | VCCIO8 | | | D9 | A9 | | | | | | |
| | | VCCIO8 | | | D11 | A13 | | | | | | |
| | | VCCIO8 | | | | E6 | | | | | | |
| | | VCCIO8 | | | | E9 | | | | | | |
| | | VCCIO8 | | | | E13 | | | | | | |
| | | VCCIO8 | | | | H11 | | | | | | |
| | | GND | | | L10 | K10 | | | | | | |
| | | GND | | | L11 | K12 | | | | | | |
| | | GND | | | M10 | K14 | | | | | | |
| | | GND | | | M11 | K16 | | | | | | |
| | | GND | | | L12 | K18 | | | | | | |
| | | GND | | | L13 | K20 | | | | | | |
| | | GND | | | M12 | L9 | | | | | | |
| | | GND | | | M13 | L11 | | | | | | |
| | | GND | | | N11 | L13 | | | | | | |
| | | GND | | | K11 | L15 | | | | | | |
| | | GND | | | N12 | L17 | | | | | | |
| | | GND | | | K12 | L19 | | | | | | |
| | | GND | | | K13 | M10 | | | | | | |
| | | GND | | | N13 | M12 | | | | | | |
| | | GND | | | N10 | M14 | | | | | | |
| | | GND | | | K10 | M16 | | | | | | |
| | | GND | | | J9 | M18 | | | | | | |
| | | GND | | | F12 | M20 | | | | | | |
| | | GND | | | H12 | N9 | | | | | | |
| | | GND | | | H13 | N11 | | | | | | |
| | | GND | | | J15 | N13 | | | | | | |
| | | GND | | | K16 | N15 | | | | | | |
| | | GND | | | L15 | N17 | | | | | | |
| | | GND | | | N15 | N19 | | | | | | |
| | | GND | | | R13 | P10 | | | | | | |
| | | GND | | | R11 | P12 | | | | | | |
| | | GND | | | R9 | P14 | | | | | | |
| | | GND | | | P8 | P16 | | | | | | |
| | | GND | | | H14 | P18 | | | | | | |
| | | GND | | | H10 | P20 | | | | | | |
| | | GND | | | H8 | R9 | | | | | | |
| | | GND | | | N8 | R11 | | | | | | |
| | | GND | | | R7 | R13 | | | | | | |
| | | GND | | | T8 | R15 | | | | | | |
| | | GND | | | T12 | R17 | | | | | | |
| | | GND | | | P16 | R19 | | | | | | |
| | | GND | | | L8 | T10 | | | | | | |
| | | GND | | | G17 | T12 | | | | | | |
| | | GND | | | M7 | T14 | | | | | | |
| | | GND | | | F16 | T16 | | | | | | |
| | | GND | | | H16 | T18 | | | | | | |
| | | GND | | | G15 | T20 | | | | | | |
| | | GND | | | G13 | U9 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | GND | | | G11 | U11 | | | | | | |
| | | GND | | | E10 | U13 | | | | | | |
| | | GND | | | G9 | U15 | | | | | | |
| | | GND | | | K7 | U17 | | | | | | |
| | | GND | | | P6 | U19 | | | | | | |
| | | GND | | | U7 | V10 | | | | | | |
| | | GND | | | V6 | V12 | | | | | | |
| | | GND | | | T10 | V14 | | | | | | |
| | | GND | | | U13 | V16 | | | | | | |
| | | GND | | | T14 | V18 | | | | | | |
| | | GND | | | N17 | V20 | | | | | | |
| | | GND | | | G7 | W9 | | | | | | |
| | | GND | | | U19 | W11 | | | | | | |
| | | GND | | | Y21 | W13 | | | | | | |
| | | GND | | | R18 | W15 | | | | | | |
| | | GND | | | J5 | W17 | | | | | | |
| | | GND | | | J19 | W19 | | | | | | |
| | | GND | | | A1 | AA2 | | | | | | |
| | | GND | | | C5 | AA27 | | | | | | |
| | | GND | | | C9 | AC6 | | | | | | |
| | | GND | | | C11 | AC9 | | | | | | |
| | | GND | | | C12 | AC13 | | | | | | |
| | | GND | | | C14 | AC16 | | | | | | |
| | | GND | | | C16 | AC20 | | | | | | |
| | | GND | | | A22 | AC23 | | | | | | |
| | | GND | | | E20 | AF1 | | | | | | |
| | | GND | | | G20 | AF28 | | | | | | |
| | | GND | | | L20 | AG2 | | | | | | |
| | | GND | | | P19 | AG5 | | | | | | |
| | | GND | | | V20 | AG9 | | | | | | |
| | | GND | | | Y20 | AG13 | | | | | | |
| | | GND | | | AB22 | AG16 | | | | | | |
| | | GND | | | Y18 | AG20 | | | | | | |
| | | GND | | | Y16 | AG24 | | | | | | |
| | | GND | | | Y12 | AG27 | | | | | | |
| | | GND | | | Y11 | B2 | | | | | | |
| | | GND | | | Y9 | B5 | | | | | | |
| | | GND | | | Y5 | B9 | | | | | | |
| | | GND | | | AB1 | B13 | | | | | | |
| | | GND | | | N3 | B16 | | | | | | |
| | | GND | | | U3 | B20 | | | | | | |
| | | GND | | | W3 | B24 | | | | | | |
| | | GND | | | D3 | B27 | | | | | | |
| | | GND | | | F3 | C1 | | | | | | |
| | | GND | | | K3 | C28 | | | | | | |
| | | GND | | | | F6 | | | | | | |
| | | GND | | | | F9 | | | | | | |
| | | GND | | | | F13 | | | | | | |
| | | GND | | | | F16 | | | | | | |
| | | GND | | | | F20 | | | | | | |

| Bank Number | VREFB Group | Pin Name / Function | Optional Function(s) | Configuration Function | F484 | F780 | DQS for X8/X9 in 484 FBGA | DQS for X16/X18 in 484 FBGA | DQS for X32/X36 in 484 FBGA | DQS for X8/X9 in 780 FBGA | DQS for X16/X18 in 780 FBGA | DQS for X32/X36 in 780 FBGA |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | GND | | | | F23 | | | | | | |
| | | GND | | | | H2 | | | | | | |
| | | GND | | | | H27 | | | | | | |
| | | GND | | | | J11 | | | | | | |
| | | GND | | | | J18 | | | | | | |
| | | GND | | | | K6 | | | | | | |
| | | GND | | | | K23 | | | | | | |
| | | GND | | | | N2 | | | | | | |
| | | GND | | | | N6 | | | | | | |
| | | GND | | | | N23 | | | | | | |
| | | GND | | | | N27 | | | | | | |
| | | GND | | | | T2 | | | | | | |
| | | GND | | | | T6 | | | | | | |
| | | GND | | | | T23 | | | | | | |
| | | GND | | | | T27 | | | | | | |
| | | GND | | | | W6 | | | | | | |
| | | GND | | | | W23 | | | | | | |
| | | GND | | | | Y11 | | | | | | |
| | | GND | | | | Y18 | | | | | | |

**Notes:**
(1) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
(2) For DQS pins that do not have the associated DQ pins, the particular DQS is not supported.

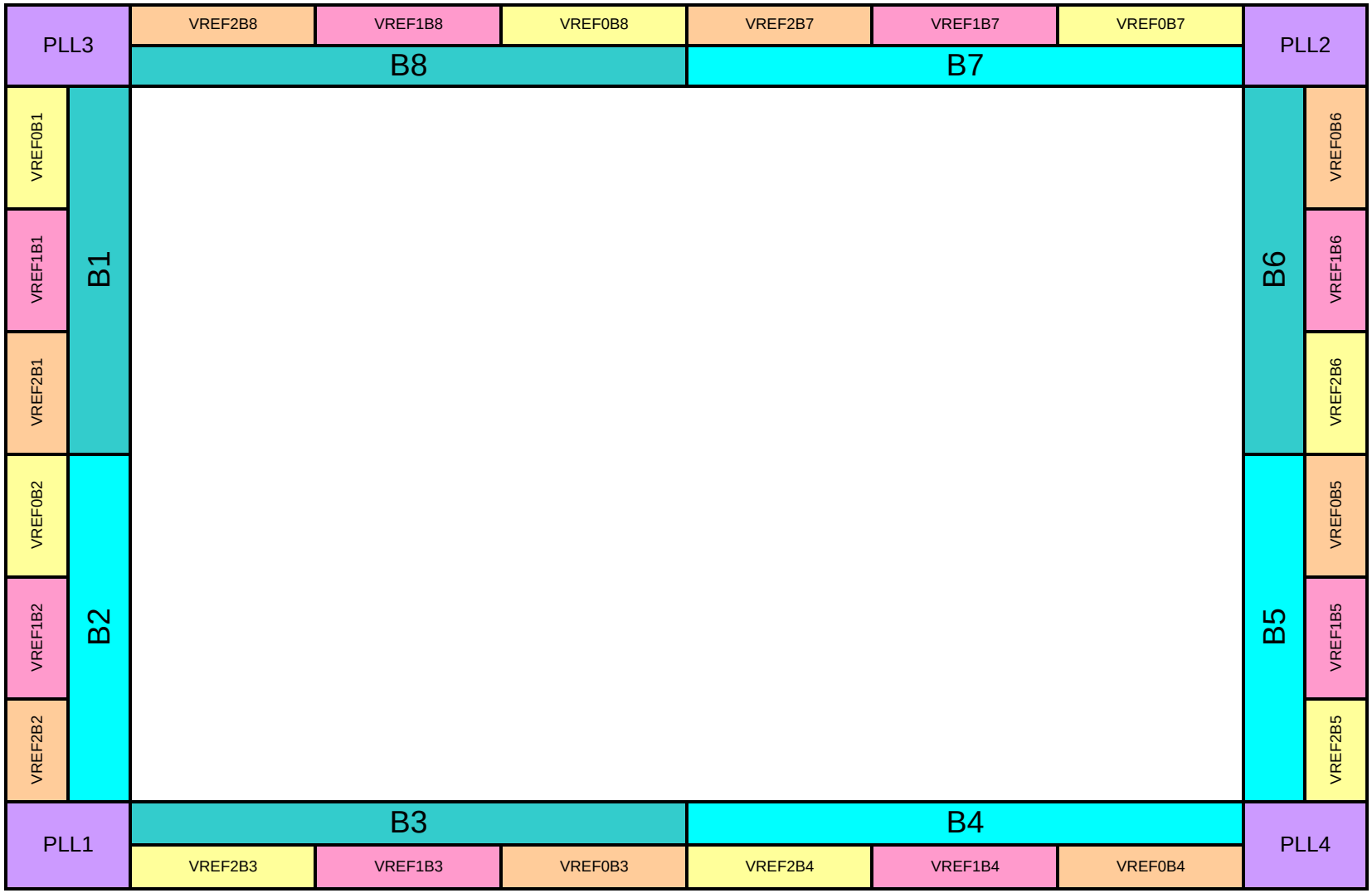
| Pin Name | Pin Type (1st, 2nd, and 3rd Function) | Pin Description |
|---|---|---|
| | | ***Supply and Reference Pins*** |
| VCCINT | Power | These are internal logic array voltage supply pins. |
| VCCIO[1..8] | Power | These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards. VCCIO powers up the JTAG pins (TCK, TMS, TDI, and TDO) and the following configuration pins: nCONFIG, DCLK, DATA[15..0], nCE, nCEO, nWE, nRESET, nOE, FLASH_nCE,nCSO and CLKUSR. |
| GND | Ground | Device ground pins. All GND pins should be connected to the board GND plane. |
| VREFB[1..8]N[0..2] | I/O | Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for the bank. If voltage-referenced I/O standards are not used in the bank, the VREF pins are available as user I/O pins. |
| VCCA[1..4] | Power | Supply (analog) voltage for PLLs[1..4] and other analog circuits in the device. |
| VCCD_PLL[1..4] | Power | Supply (digital) voltage for PLLs[1..4]. |
| RUP[1..4] | I/O, Input | Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor Rup must be connected to the designated RUP pin within the same bank. If not required, this pin is a regular I/O pin. |
| RDN[1..4] | I/O, Input | Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5, and 7. The external precision resistor Rdn must be connected to the designated RDN pin within the same bank. If not required, this pin is a regular I/O pin. |
| GNDA[1..4] | Ground | Ground for PLL[1..4]. You can connect these pins to GND plane on the board. |
| NC | No Connect | Do not drive signals into these pins. |
| | | ***Dedicated Configuration/JTAG Pins*** |
| DATA0 | Input (PS, FPP, AS) Bidirectional open drain (AP) | Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After AS configuration, DATA0 is a dedicated input pin with optional user control. After PS or PP configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA0 is a dedicated bidirectional pin with optional user control. |
| MSEL[3..0] | Input | Configuration input pins that set the Cyclone III device configuration scheme. These pins must be hardwired to VCCA or GND. Some of the smaller devices or package options do not support the AP flash programming and do not have the MSEL[3] pin. |
| nCE | Input | Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. |
| nCONFIG | Input | Dedicated configuration control input. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.The input buffer on this pin supports hysteresis using Schmitt trigger circuitry. |
| CONF_DONE | Bidirectional (open-drain) | This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. |
| nSTATUS | Bidirectional (open-drain) | This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. |
| TCK | Input | Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND. |
| TMS | Input | Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC. |
| TDI | Input | Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC. |
| TDO | Output | Dedicated JTAG output pin. |
| | | ***Clock and PLL Pins*** |
| CLK[0,2,4,6,9,11,13,15], DIFFCLK_[0..7]p | Clock, Input | Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins. |
| CLK[1,3,5,7,8,10,12,14], DIFFCLK_[0..7]n | Clock, Input | Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins. |
| PLL[1..4]_CLKOUT[p,n] | I/O, Output | I/O pins that be used as two single-ended clock output pins or one differential clock output pair.These pins can only use the differential I/O standard if it is being fed by a PLL output. |

| Pin Name | Pin Type (1st, 2nd, and 3rd Function) | Pin Description |
|---|---|---|
| | ***Optional/Dual-Purpose Configuration Pins*** | |
| DCLK | Input (PS, FPP)<br>I/O, Output (AS, AP) | Configuration clock pin. In PS and PP configuration modes, DCLK is used to clock configuration data from an external source into the Cyclone III device. In AS and AP modes, DCLK is an output from the Cyclone III device that provides timing for the configuration interface. After AS or AP configuration, this pin is available as a user I/O pin with optional user control. |
| nCEO | I/O, Output | Output that drives low when device configuration is complete. |
| FLASH_nCE, nCSO | I/O, Output | This pin functions as FLASH_nCE in AP mode, and nCSO in AS mode. This pin has an internal pull-up resistor that is always active.<br><br>nCSO: Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device.<br><br>FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash. |
| DATA1, ASDO | Input (FPP)<br>Output (AS)<br>Bidirectional open-drain (AP) | This pin functions as DATA1 in PS, FPP, and AP modes, and as ASDO in AS mode.<br><br>DATA1: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively.<br>In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated.<br>After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings.<br>After AP configuration, DATA1 is a dedicated bidirectional pin with optional user control.<br><br>ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control. |
| DATA[7..2] | Input (FPP)<br>Bidirectional open-drain (AP) | Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively.<br>In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.<br>After FPP configuration, DATA[7..2] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.<br>After AP configuration, DATA[7..2] are dedicated bidirectional pins with optional user control. |
| DATA[15..8] | Bidirectional open-drain (AP) | Data inputs. Btye-wide or word-wide configuration data is presented to the target device on DATA[15..0].<br>In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated.<br>After AP configuration, DATA[15..8] are dedicated bidirectional pins with optional user control. |
| PADD[23..0] | I/O, Output (AP) | 24-bit address bus from the Cyclone III device to the parallel flash in AP mode. |
| nRESET | I/O, Output (AP) | Active-low reset output. Driving the nRESET pin low resets the parallel flash. |
| nAVD | I/O, Output (AP) | Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[23..0] address bus. |
| nOE | I/O, Output (AP) | Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[15..0]). |
| nWE | I/O, Output (AP) | Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[15..0] bus is valid. |
| CRC_ERROR | I/O, Output | Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.This pin can be set in Quartus II software to support open-drain output. |
| DEV_CLRn | I/O (when option off),<br>Input (when option on) | Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software. |
| DEV_OE | I/O (when option off),<br>Input (when option on) | Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software. |

| Pin Name | Pin Type (1st, 2nd, and 3rd Function) | Pin Description |
|---|---|---|
| INIT_DONE | I/O, Output (open-drain) | This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software. |
| CLKUSR | I/O, Input | Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software. |
| ***Dual-Purpose Differential and External Memory Interface Pins*** | | |
| DIFFIO_[L,R,T,B][0..61][n,p] | I/O, TX/RX channel | Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. |
| DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCLK[0..11] | I/O, DQS/CQ, DPCLK | Dual-purpose DPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data. |
| DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPCLK[0..7] | I/O, DQS/CQ, CDPCLK | Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before being driven into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data. |
| DQ[0..5][L,R,T,B] | I/O, DQ | Optional data signal for use in external memory interfaces. |
| DM[0..5][L,R,B,T][0..1]/BWS#[0..5][L,R,T,B] | I/O, DM/BWS# | The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals. |

**Note:**

(1) The pin definitions are prepared based on the device with the largest density, EP3C120. Refer to the pin list for the availability of pins in each density.




**Notes:**

1. This is a top view of the silicon die.
2. This is only a pictorial representation to provide an idea of placement on the device.
   Refer to the pin list and the Quartus® II software for exact locations.

# Pin Information for the Cyclone® III EP3C120 Device
# Version 1.3

| Version Number | Changes Made | Date |
|---|---|---|
| 1.0 | Initial release. | 5/18/2007 |
| 1.1 | Updated Note(1) in Pin List. | 1/4/2008 |
| 1.2 | Updated pin function for CRC_ERROR pin. | 5/23/2008 |
| | Updated pin function for PLL[1..4]_CLKOUT[p,n] pin. | |
| | Remove RDY from pin list and pin definitions. | |
| | Incorporated pin connection guideline into Pin Definitions worksheet. | |
| | Incorporated VCCA and VCCD Decoupling recommendations. | |
| 1.3 | Removed Pin Connection Guideline from Pin Definitions worksheet. | 10/7/2009 |
| | Removed VCCA and VCCD Decoupling recommendations. | |
| | Removed PKG notes from Pin List Worksheet. | |
| | Updated pin function for DCLK pin. | |
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