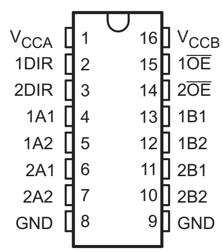
4-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

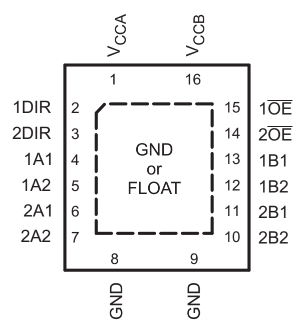
FEATURES

- **Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage**
- **Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range**
- **I/Os Are 4.6-V Tolerant**
- **I_{off} Supports Partial Power-Down-Mode Operation**
- **Maximim Data Rates**
  - **380 Mbps (1.8-V to 3.3-V Translation)**
  - **200 Mbps (<1.8-V to 3.3-V Translation)**
  - **200 Mbps (Translate to 2.5 V or 1.8 V)**
  - **150 Mbps (Translate to 1.5 V)**
  - **100 Mbps (Translate to 1.2 V)**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
  - **8000-V Human-Body Model (A114-A)**
  - **150-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

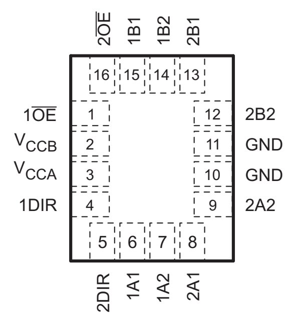
D, DGV, OR PW PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



RSV PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

This 4-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. The SN74AVC4T245 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVC4T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ}.

The SN74AVC4T245 is designed so that the control pins (1DIR, 2DIR, 1$\overline{OE}$, and 2$\overline{OE}$) are supplied by V_{CCA}.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RGY	Tape and reel	SN74AVC4T245RGYR	WT245
	QFN – RSV	Tape and reel	SN74AVC4T245RSVR	ZWU
	SOIC – D	Tube	SN74AVC4T245D	AVC4T245
		Tape and reel	SN74AVC4T245DR	
	TSSOP – PW	Tube	SN74AVC4T245PW	WT245
		Tape and reel	SN74AVC4T245PWR	
	TVSOP – DGV	Tape and reel	SN74AVC4T245DGVR	WT245

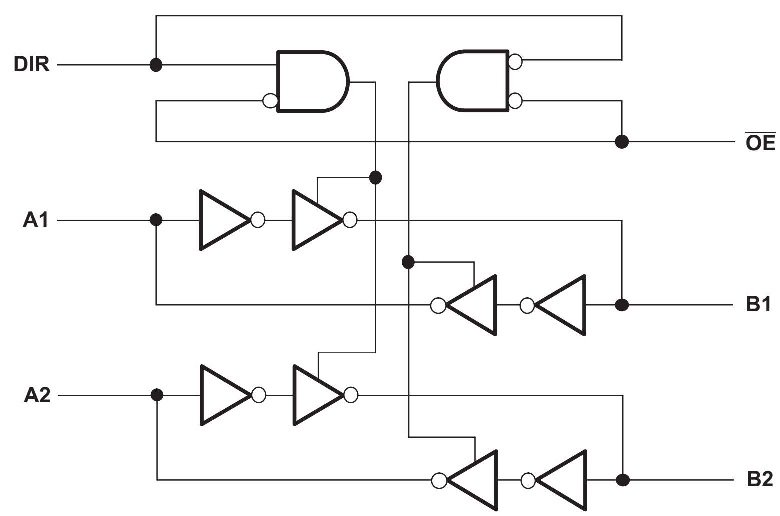
(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. FUNCTION TABLE(1) (each 2-bit section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

LOGIC DIAGRAM (POSITIVE LOGIC) FOR 1/2 OF AVC4T245



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range[2]	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state[2]	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state[2] [3]	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
$θ_{JA}$	Package thermal impedance	D package[4]		73	°C/W
		DB package[4]		82	
		DGV package[4]		120	
		PW package[4]		108	
		RGY package[5]		39	
		RSV package		184	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.
(5) The package thermal impedance is calculated in accordance with JESD 51-5.

RECOMMENDED OPERATING CONDITIONS(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.2 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.2 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})(5)	1.2 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})(5)	1.2 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.1 V to 1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V

ELECTRICAL CHARACTERISTICS[1] [2]

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –100 μA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} – 0.2		V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = –12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 μA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.25				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	μA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±0.1	±1		±5	μA
				0 V to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6 V	3.6 V		±0.5	±2.5		±5	μA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					8	μA
				0 V	0 V to 3.6 V					–2	
				0 V to 3.6 V	0 V					8	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					8	μA
				0 V	0 V to 3.6 V					8	
				0 V to 3.6 V	0 V					–2	
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, I_O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V					16	μA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		3.5			4.5	pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		6			7	pF

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.2 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V	V_{CCB} = 1.8 V ± 0.15 V	V_{CCB} = 2.5 V ± 0.2 V	V_{CCB} = 3.3 V ± 0.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.4	2.9	2.7	2.6	2.8	ns
t_{PHL}			3.4	2.9	2.7	2.6	2.8	
t_{PLH}	B	A	3.6	3.1	2.8	2.6	2.6	ns
t_{PHL}			3.6	3.1	2.8	2.6	2.6	
t_{PZH}	$\overline{OE}$	A	5.6	4.7	4.3	3.9	3.7	ns
t_{PZL}			5.6	4.7	4.3	3.9	3.7	
t_{PZH}	$\overline{OE}$	B	5	4.3	3.9	3.6	3.6	ns
t_{PZL}			5	4.3	3.9	3.6	3.6	
t_{PHZ}	$\overline{OE}$	A	6.2	5.2	5.2	4.3	4.8	ns
t_{PLZ}			6.2	5.2	5.2	4.3	4.8	
t_{PHZ}	$\overline{OE}$	B	5.9	5.1	5	4.7	5.5	ns
t_{PLZ}			5.9	5.1	5	4.7	5.5	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.2	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
t_{PHL}			3.2	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	
t_{PLH}	B	A	3.3	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	ns
t_{PHL}			3.3	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
t_{PZH}	$\overline{OE}$	A	4.9	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	ns
t_{PZL}			4.9	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
t_{PZH}	$\overline{OE}$	B	4.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
t_{PZL}			4.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
t_{PHZ}	$\overline{OE}$	A	5.6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
t_{PLZ}			5.6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
t_{PHZ}	$\overline{OE}$	B	5.2	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns
t_{PLZ}			5.2	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.9	0.1	6	0.1	4.9	0.1	3.9	0.3	3.9	ns
t_{PHL}			2.9	0.1	6	0.1	4.9	0.1	3.9	0.3	3.9	
t_{PLH}	B	A	3	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	ns
t_{PHL}			3	0.6	5.3	0.5	4.9	0.3	4.6	0.3	4.5	
t_{PZH}	$\overline{OE}$	A	4.4	1	7.4	1	7.3	0.6	7.3	0.4	7.2	ns
t_{PZL}			4.4	1	7.4	1	7.3	0.6	7.3	0.4	7.2	
t_{PZH}	$\overline{OE}$	B	4.1	1.2	9.2	1	7.4	0.8	5.3	0.8	4.6	ns
t_{PZL}			4.1	1.2	9.2	1	7.4	0.8	5.3	0.8	4.6	
t_{PHZ}	$\overline{OE}$	A	5.4	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7	ns
t_{PLZ}			5.4	1.6	8.6	1.8	8.7	1.3	8.7	1.6	8.7	
t_{PHZ}	$\overline{OE}$	B	5	1.7	9.9	1.6	8.7	1.2	6.9	1	6.9	ns
t_{PLZ}			5	1.7	9.9	1.6	8.7	1.2	6.9	1	6.9	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.8	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
t_{PHL}			2.8	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	
t_{PLH}	B	A	2.7	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
t_{PHL}			2.7	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	
t_{PZH}	$\overline{OE}$	A	4	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	ns
t_{PZL}			4	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	
t_{PZH}	$\overline{OE}$	B	3.8	0.9	8.8	0.8	7	0.6	4.8	0.6	4	ns
t_{PZL}			3.8	0.9	8.8	0.8	7	0.6	4.8	0.6	4	
t_{PHZ}	$\overline{OE}$	A	4.7	1	8.4	1	8.4	1	6.2	1	6.6	ns
t_{PLZ}			4.7	1	8.4	1	8.4	1	6.2	1	6.6	
t_{PHZ}	$\overline{OE}$	B	4.5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	ns
t_{PLZ}			4.5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
t_{PHL}			2.9	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	
t_{PLH}	B	A	2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	ns
t_{PHL}			2.6	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	
t_{PZH}	$\overline{OE}$	A	3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	ns
t_{PZL}			3.8	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	
t_{PZH}	$\overline{OE}$	B	3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns
t_{PZL}			3.7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	
t_{PHZ}	$\overline{OE}$	A	4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	ns
t_{PLZ}			4.8	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	
t_{PHZ}	$\overline{OE}$	B	5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	ns
t_{PLZ}			5.3	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	

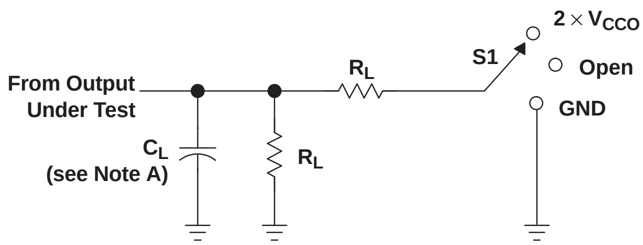
OPERATING CHARACTERISTICS

T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	1	1	1	1.5	2	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		12	12.5	13	14	15	
		Outputs disabled		1	1	1	1	1	
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	12	12.5	13	14	15	pF
		Outputs disabled		1	1	1	1	1	
	B to A	Outputs enabled		1	1	1	1	2	
		Outputs disabled		1	1	1	1	1	

(1) Power dissipation capacitance per transceiver

PARAMETER MEASUREMENT INFORMATION

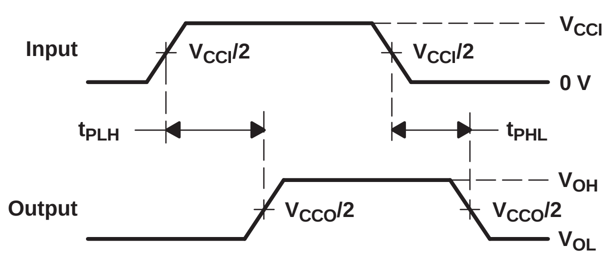


LOAD CIRCUIT

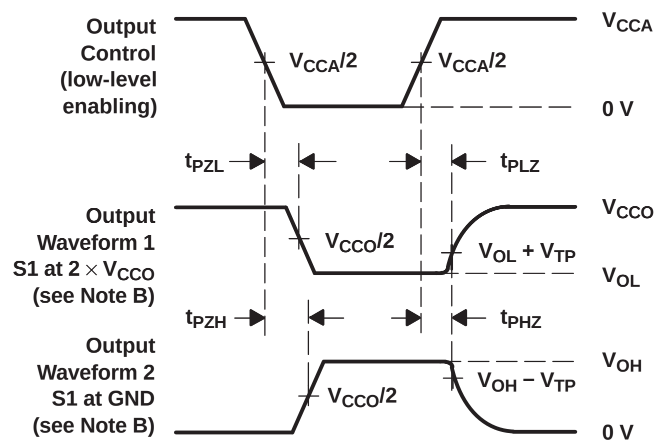
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V

VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 1. Load and Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision D (September 2007) to Revision E	Page
• Fixed t_{PZL} V_{CCB} = 3.3 V parameter typographical error from 36.6 to 3.6.	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
74AVC4T245DGVRE4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
74AVC4T245DGVRG4	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
74AVC4T245RGYRG4	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT245	Samples
74AVC4T245RSVRG4	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU	Samples
SN74AVC4T245D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245DBR	PREVIEW	SSOP	DB	16	2000	TBD	Call TI	Call TI	-40 to 85		
SN74AVC4T245DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245DGVR	ACTIVE	TVSOP	DGV	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245DT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245DTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245DTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AVC4T245	Samples
SN74AVC4T245PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
SN74AVC4T245PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245PWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT245	Samples
SN74AVC4T245RGYR	ACTIVE	VQFN	RGY	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT245	Samples
SN74AVC4T245RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWU	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] Only one of markings shown within the brackets will appear on the physical device.

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OTHER QUALIFIED VERSIONS OF SN74AVC4T245 :

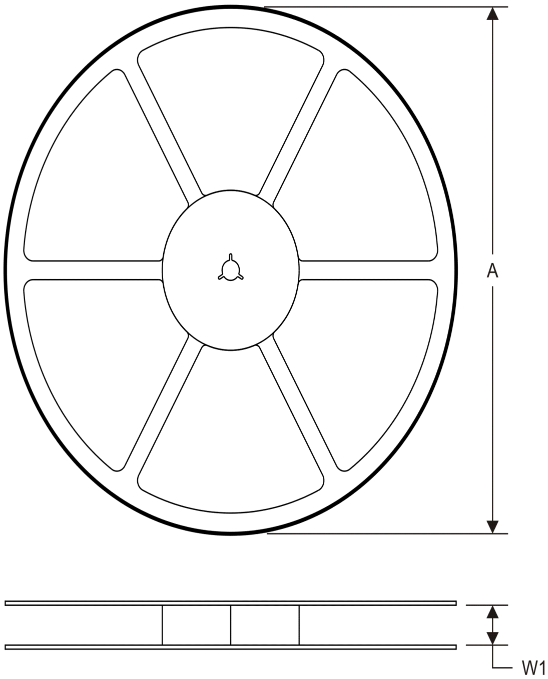
- Automotive: SN74AVC4T245-Q1

NOTE: Qualified Version Definitions:

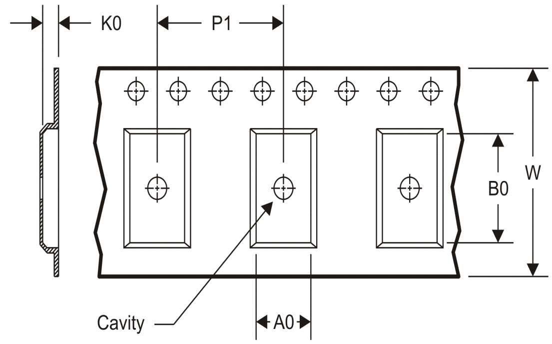
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



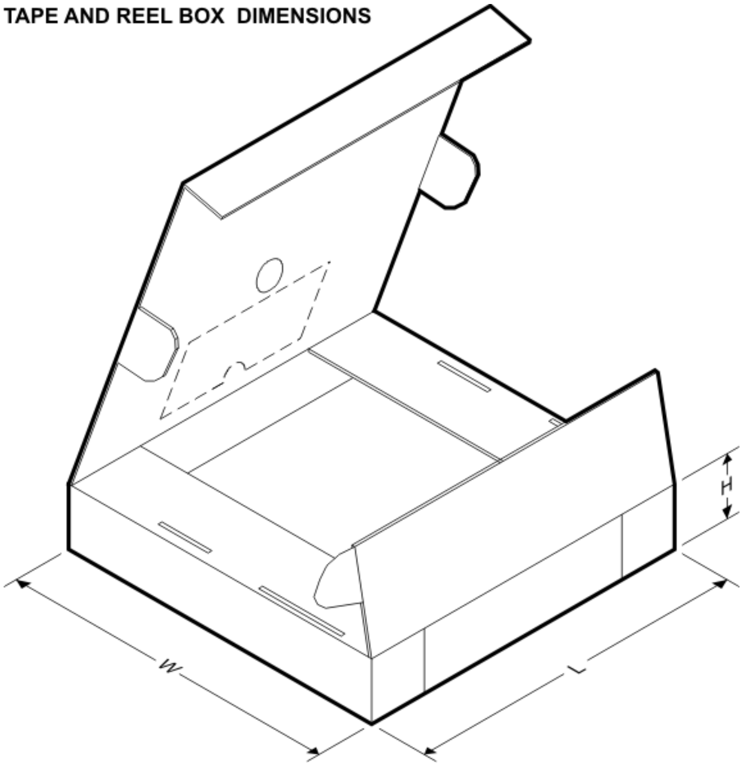
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC4T245DGVR	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AVC4T245DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AVC4T245PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T245PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T245RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T245RSVR	UQFN	RSV	16	3000	180.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

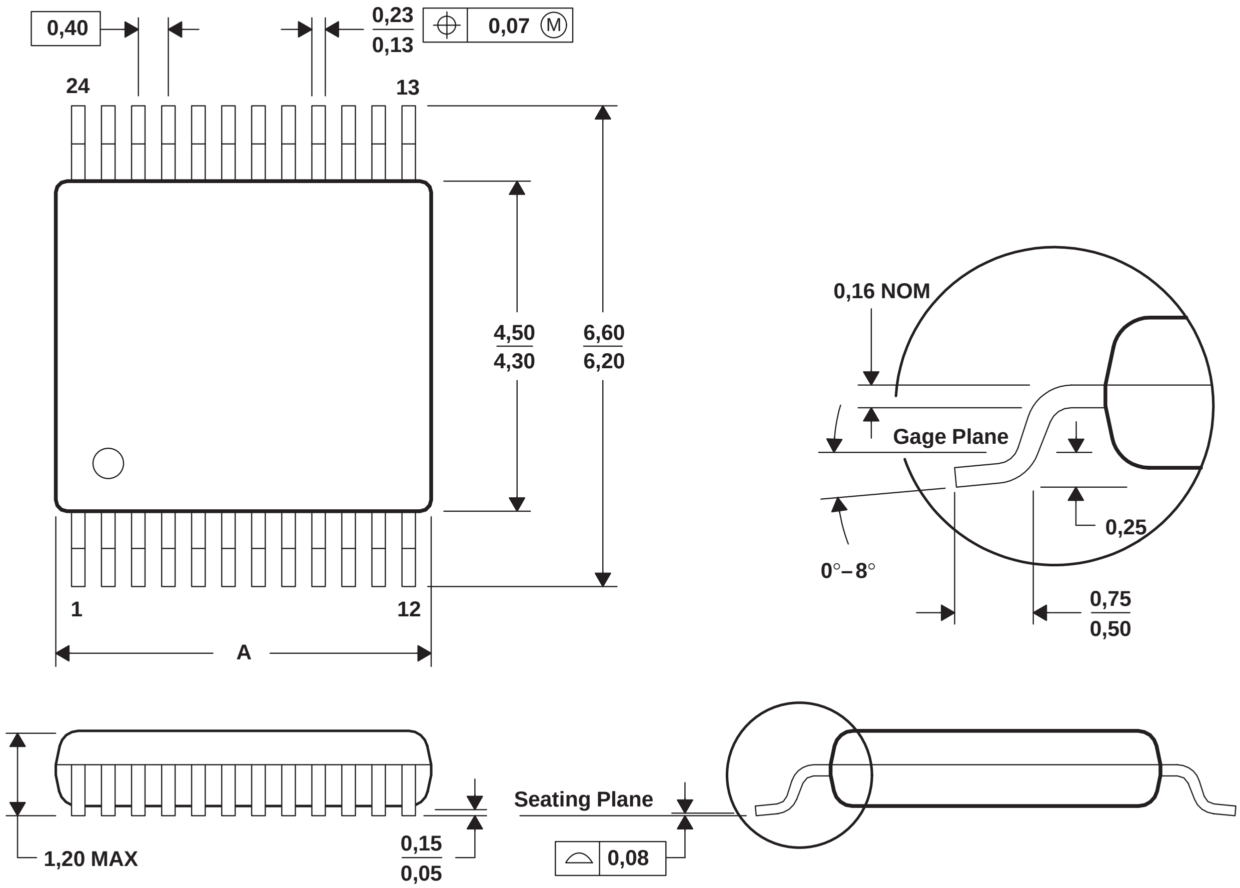


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC4T245DGVR	TVSOP	DGV	16	2000	367.0	367.0	35.0
SN74AVC4T245DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AVC4T245PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
SN74AVC4T245PWT	TSSOP	PW	16	250	367.0	367.0	35.0
SN74AVC4T245RGYR	VQFN	RGY	16	3000	367.0	367.0	35.0
SN74AVC4T245RSVR	UQFN	RSV	16	3000	203.0	203.0	35.0

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

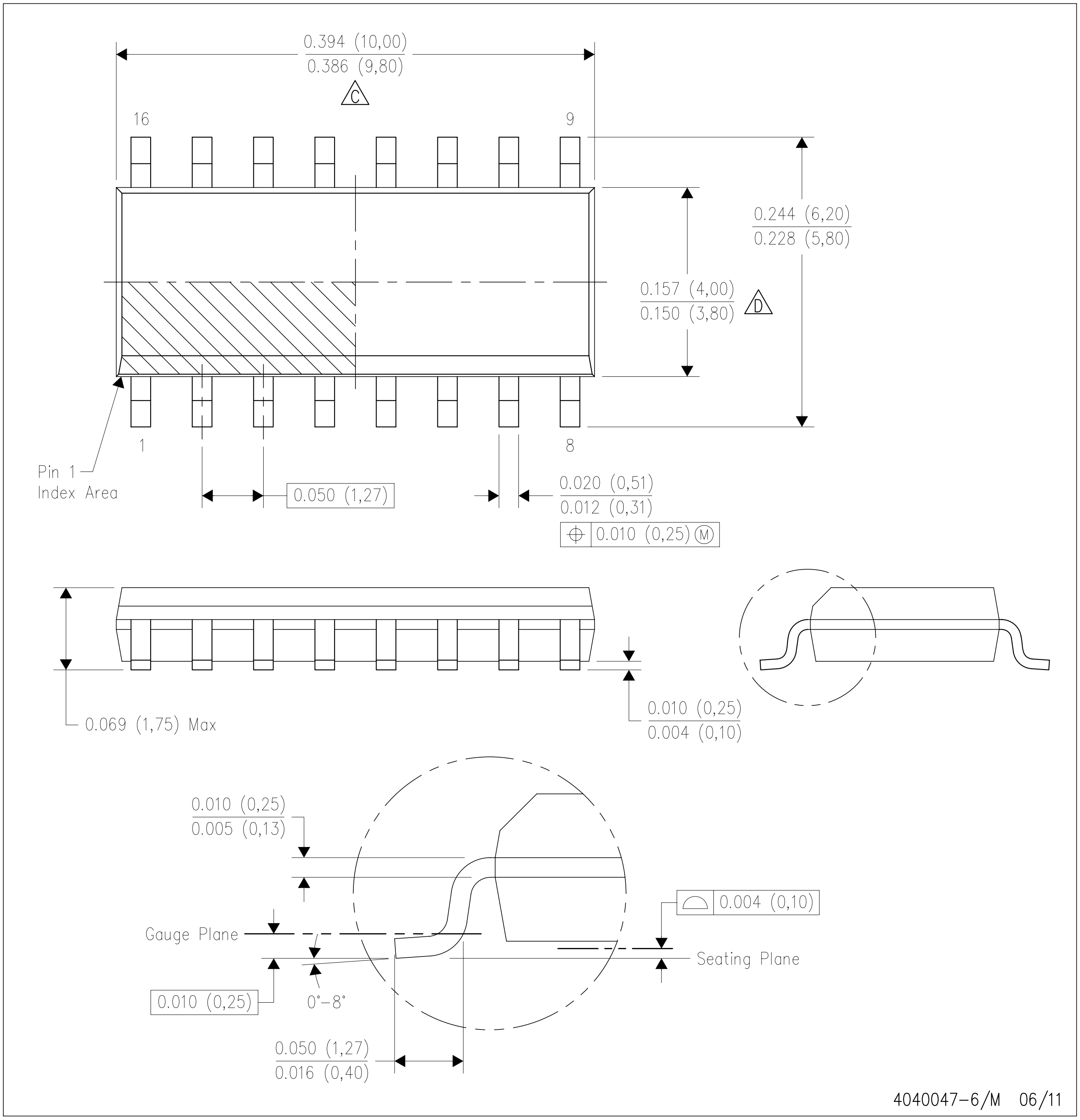


PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

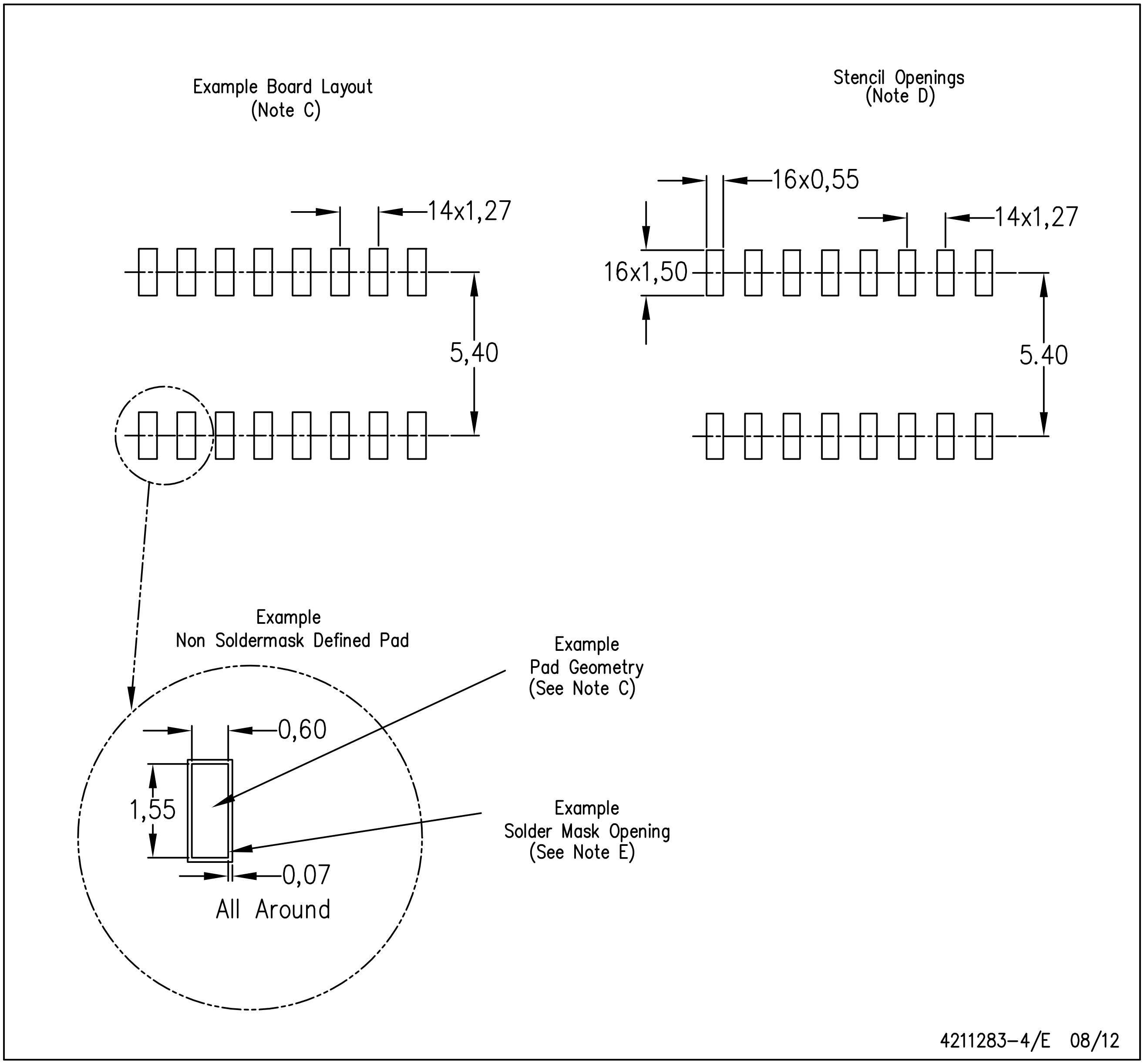
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R-PDSO-G16) PLASTIC SMALL OUTLINE



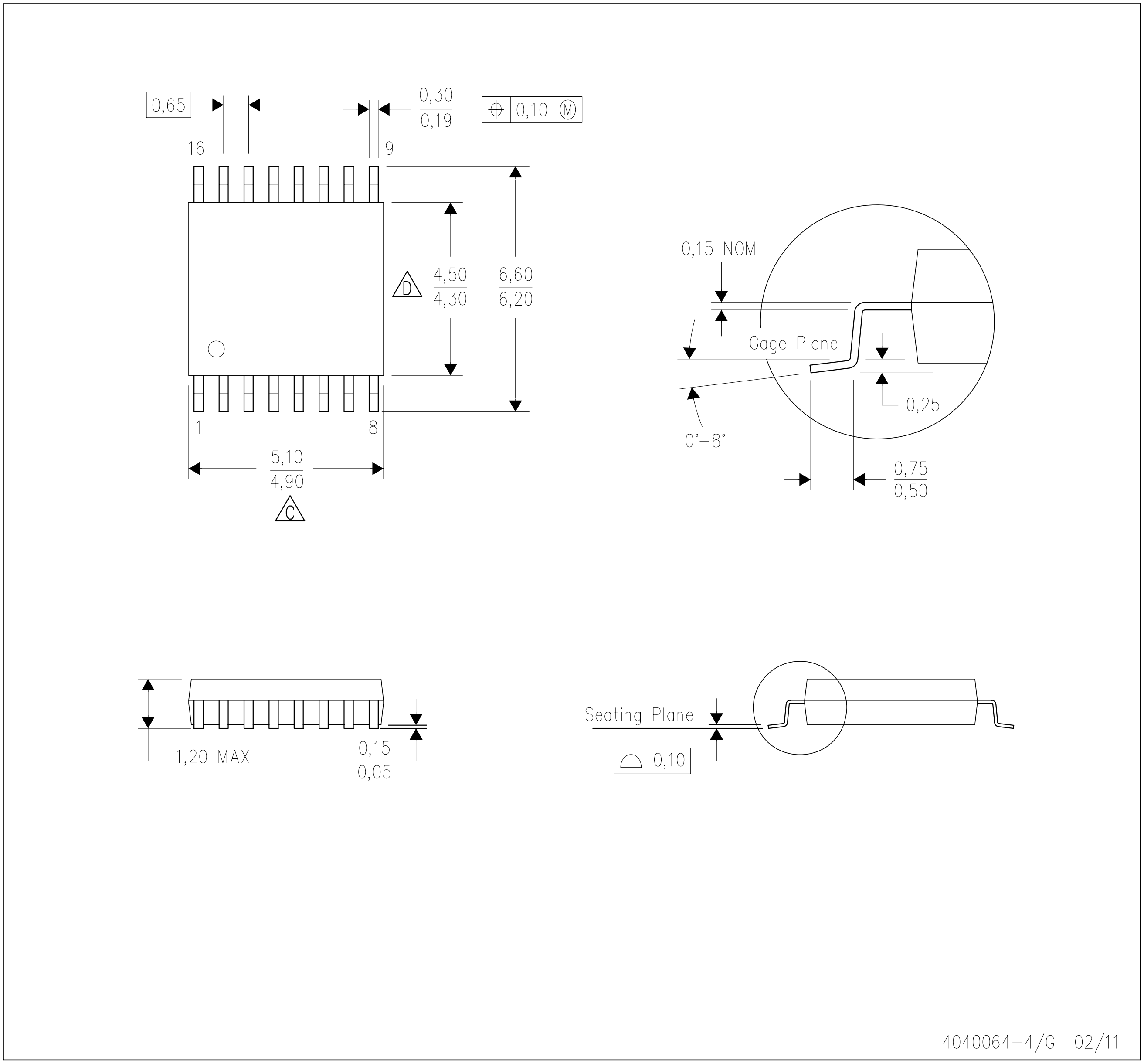
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



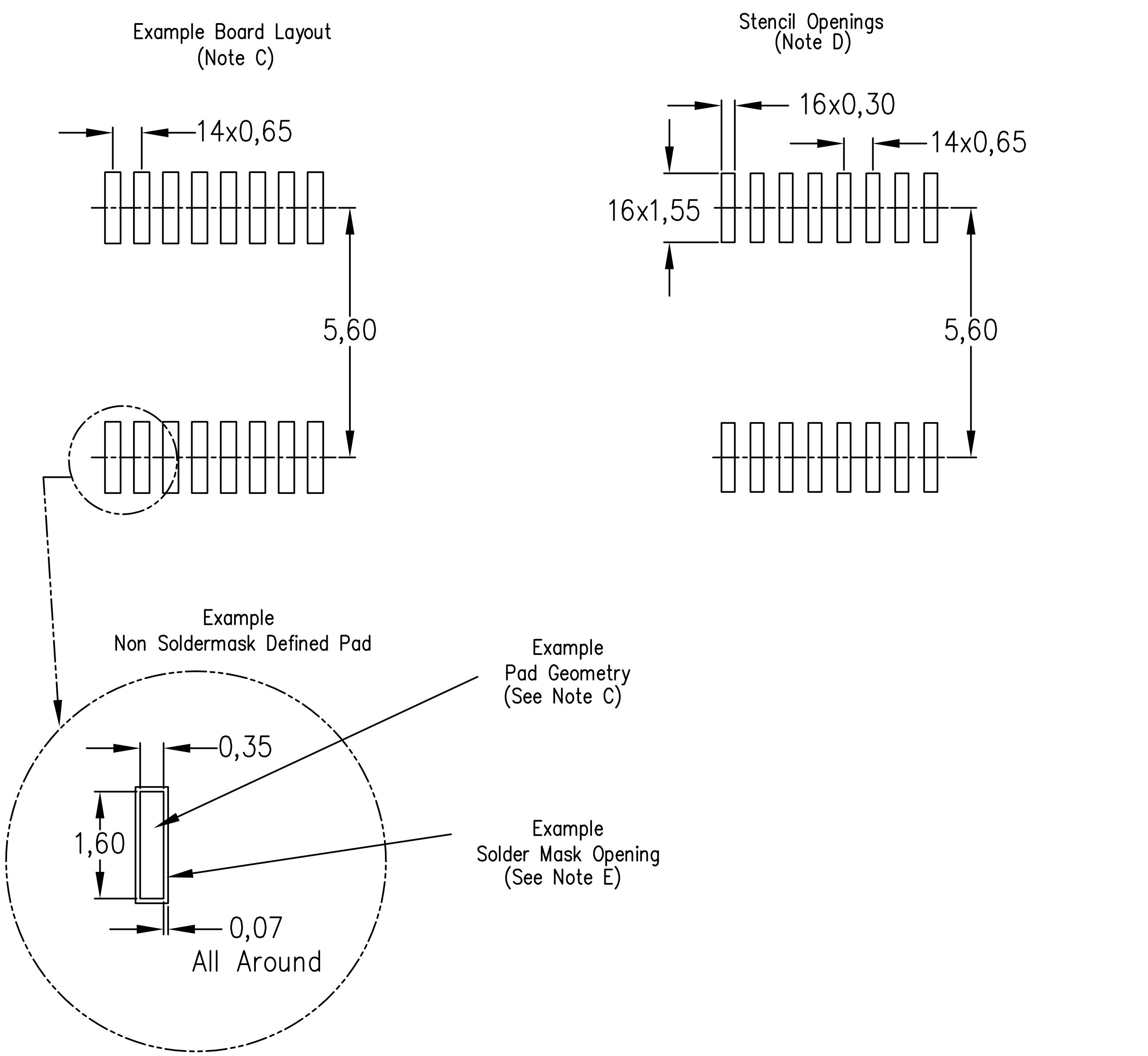
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO-153

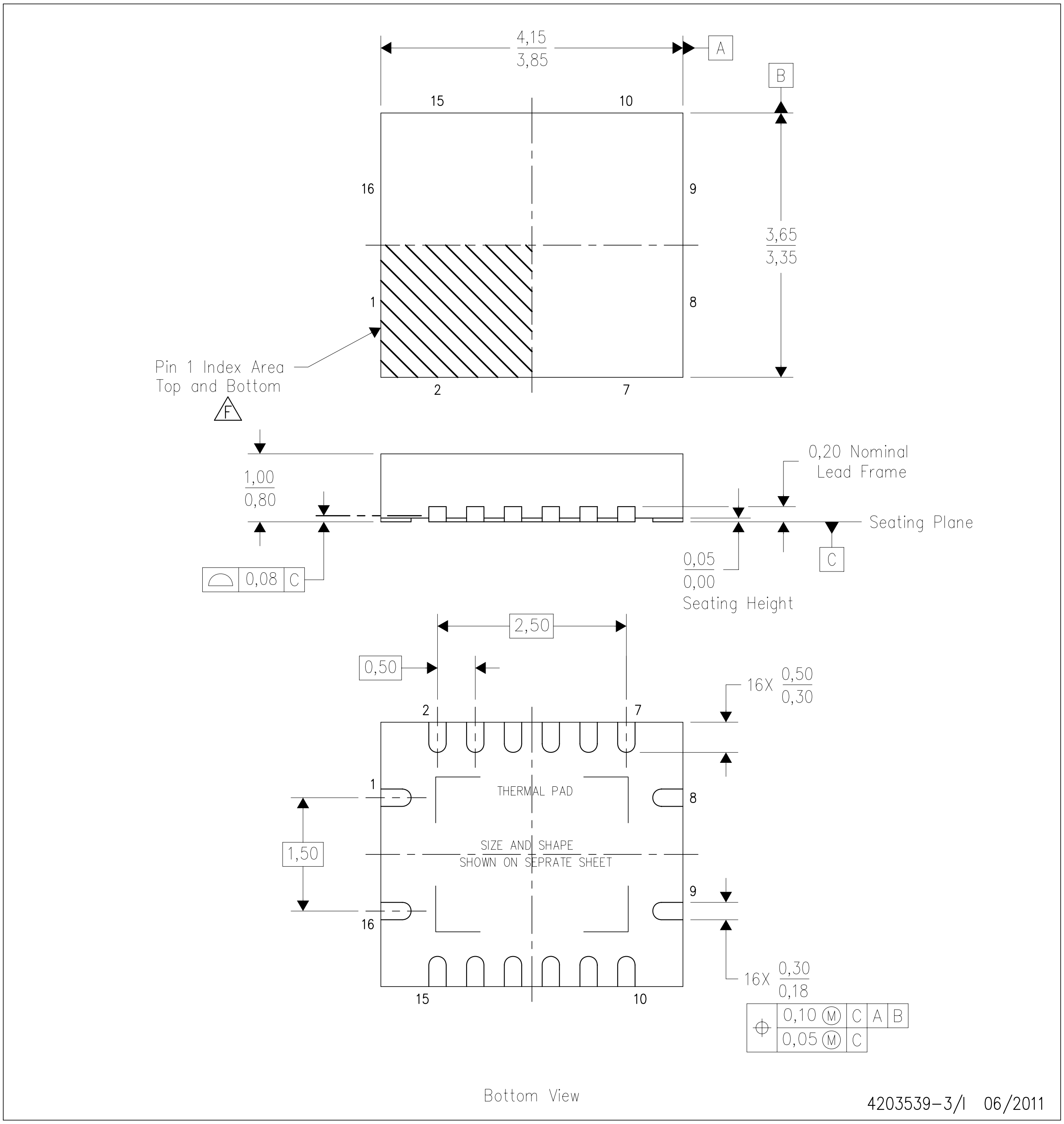
PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



4211284–3/F 12/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO–241 variation BA.

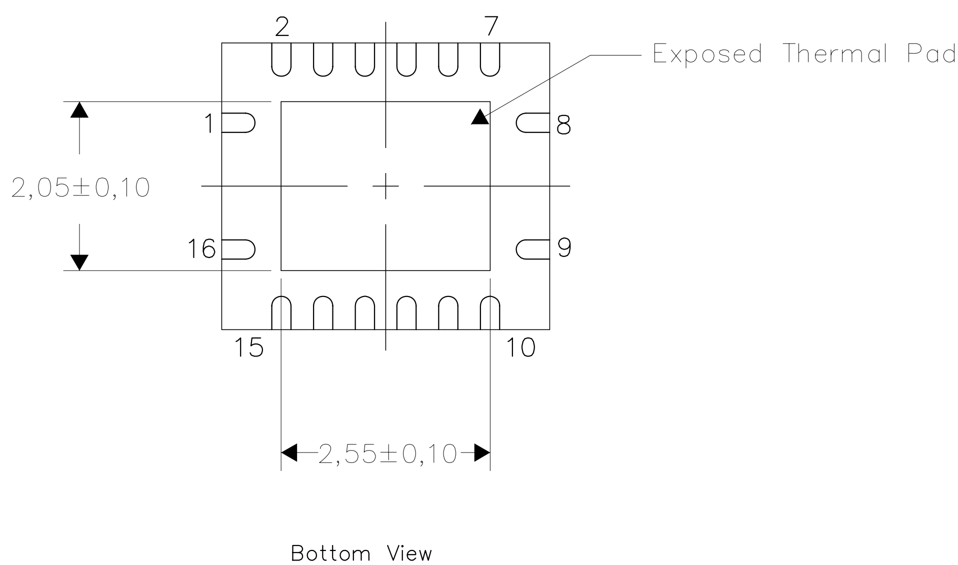
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

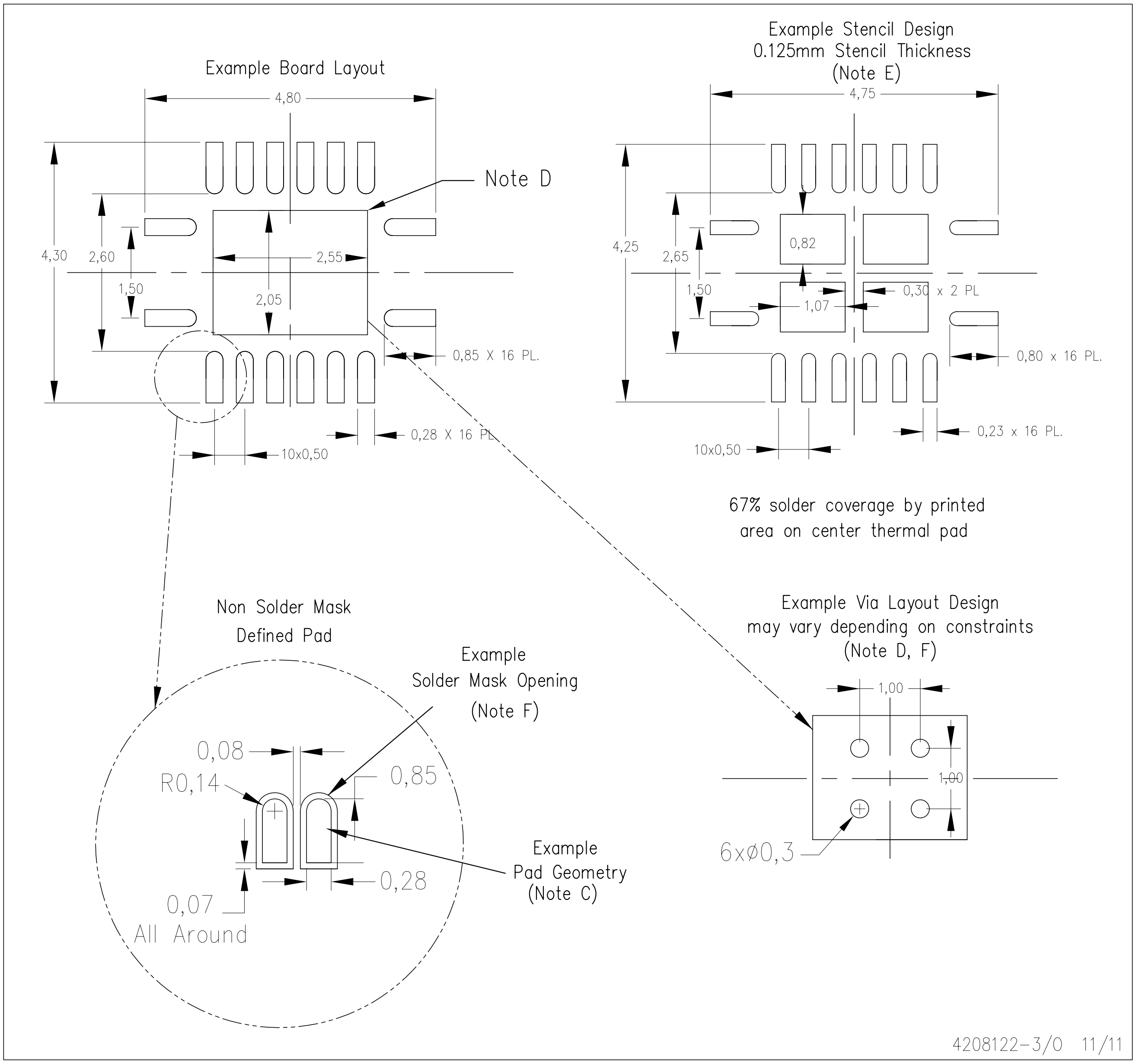


Exposed Thermal Pad Dimensions

4206353–3/0 11/11

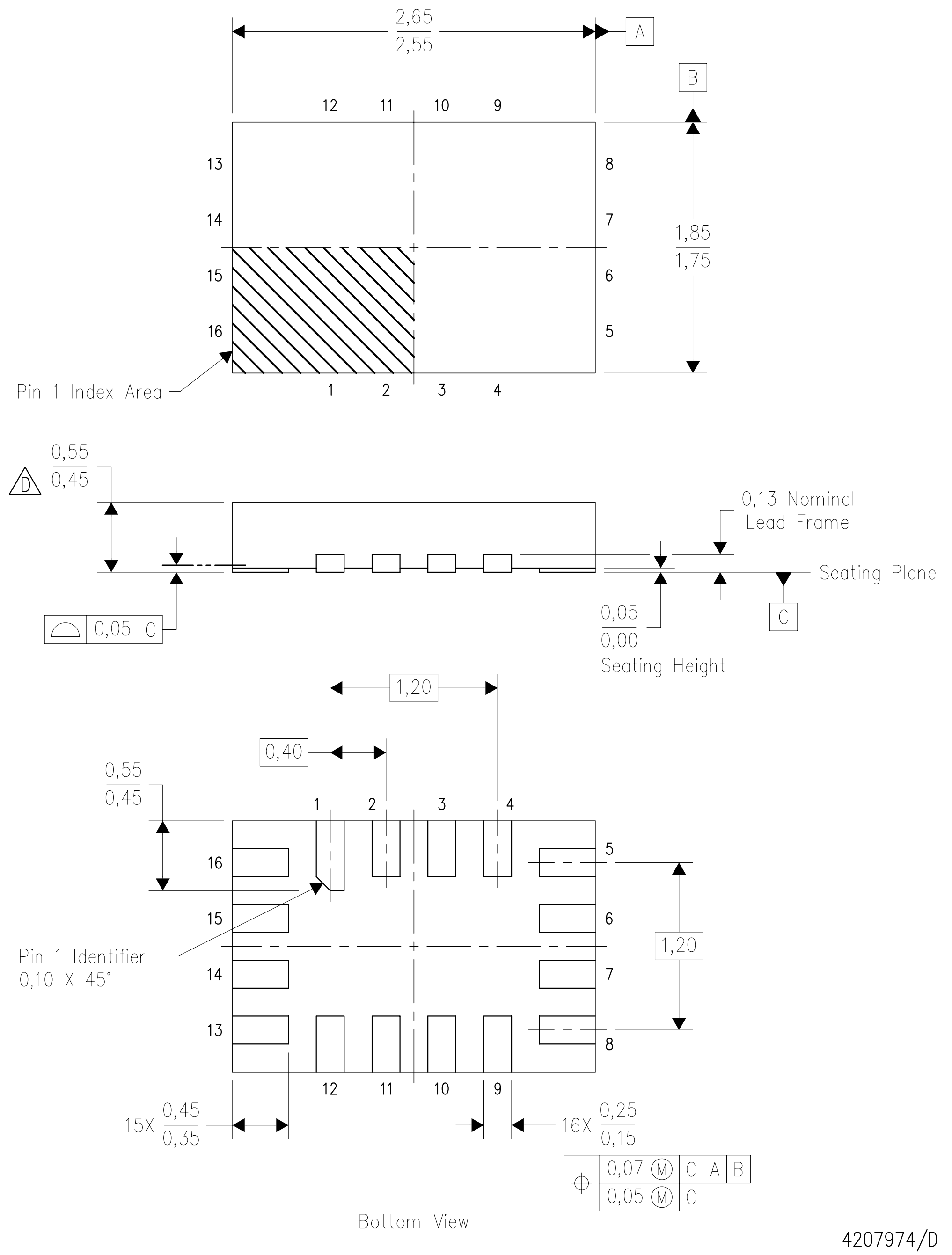
NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RSV (R-PUQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD

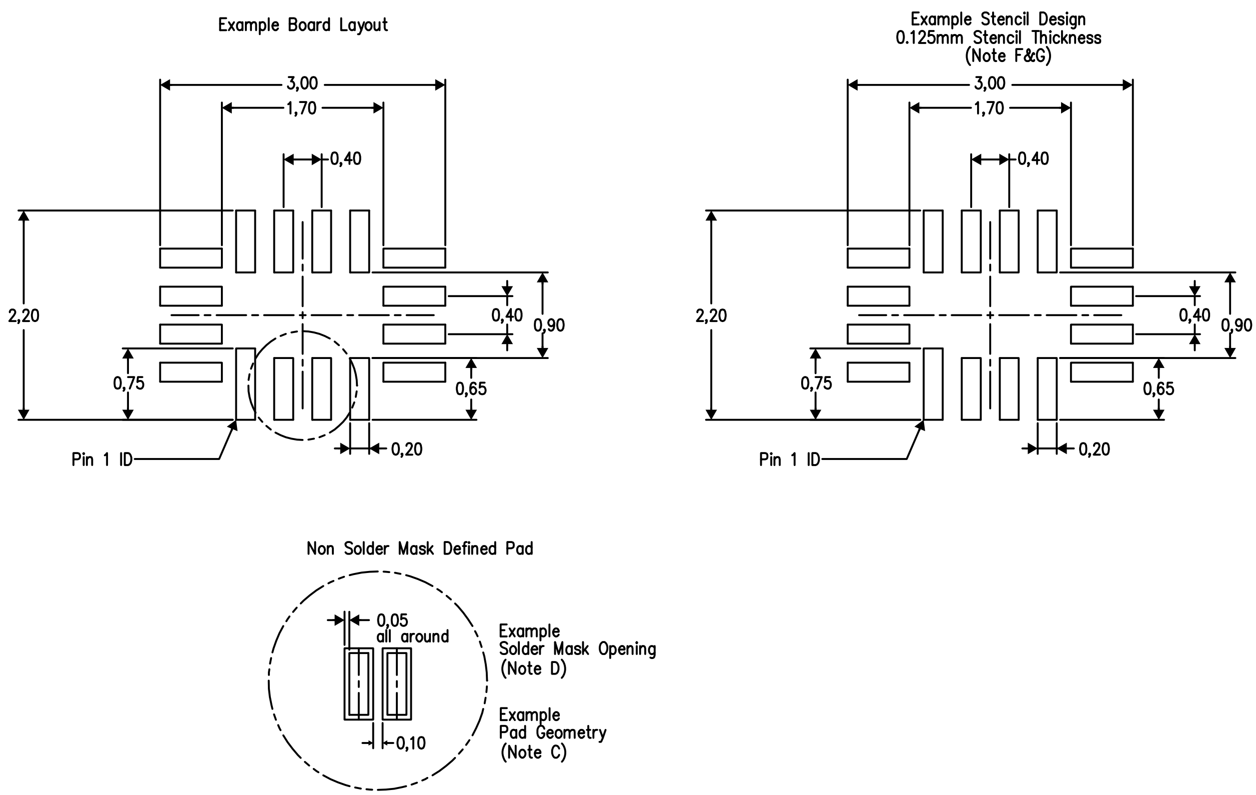


4207974/D 12/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

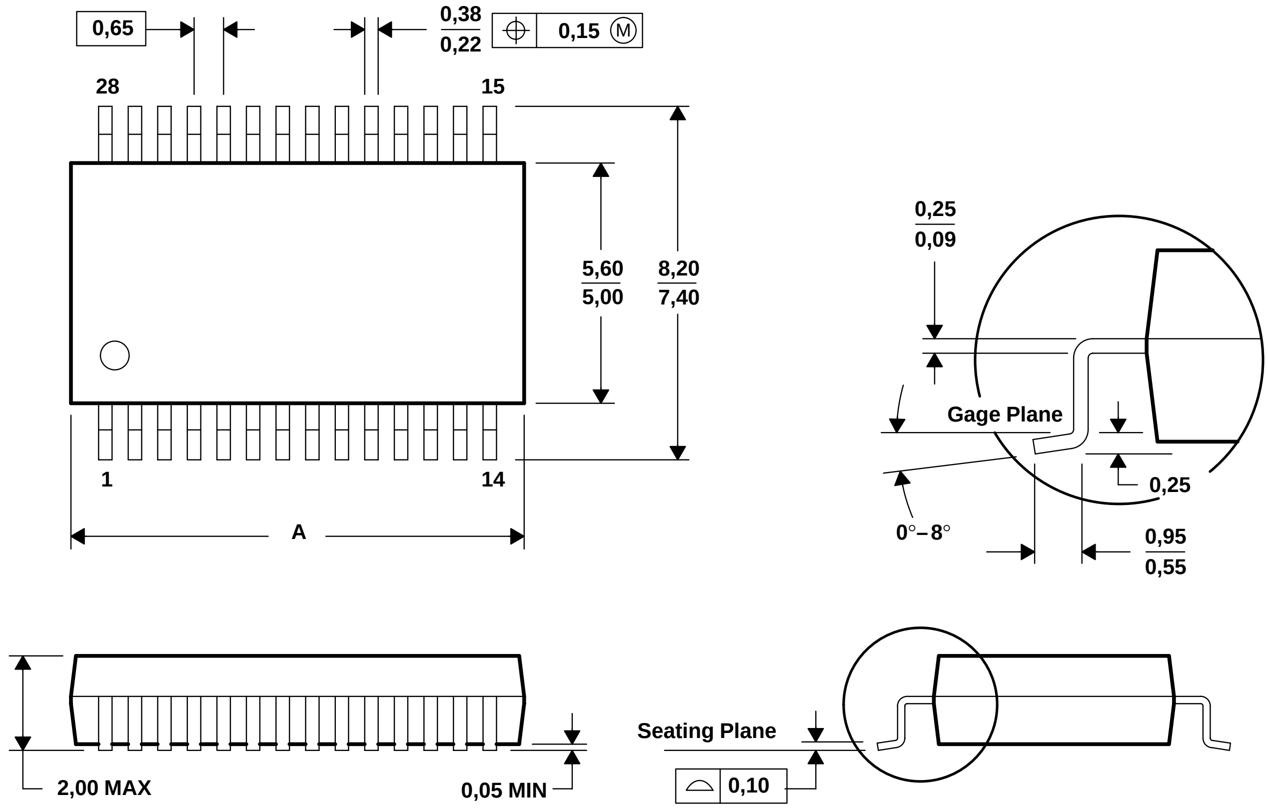


4208244/C 02/13

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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