Cyclone IV GX FPGA Features

View device ordering codes on **page 40**.

		Maximum Resource Count for Cyclone IV GX FPGAs (1.2 V)						
		EP4CGX15	**EP4CGX22**	**EP4CGX30**	**EP4CGX50**	**EP4CGX75**	**EP4CGX110**	**EP4CGX150**
Resources	LEs (K)	14	21	29	50	74	109	150
	M9K memory blocks	60	84	120	278	462	666	720
	Embedded memory (Kb)	540	756	1,080	2,502	4,158	5,490	6,480
	18 x 18 multipliers	0	40	80	140	198	280	360
Architectural Features	Global clock networks	20	20	20	30	30	30	30
	PLLs	3	4	4	8	8	8	8
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3						
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12						
	Emulated LVDS channels	9	40	40	73	73	139	139
	LVDS channels, 840 Mbps (receive/transmit)	7/7	14/14	14/14	49/49	49/49	59/59	59/59
	Transceiver count[1] (2.5 Gbps/3.125 Gbps)	2/0	2, 0 / 4, 0	4, 0 / 0, 4[2]	0, 8	0, 8	0, 8	0, 8
	PCIe hard IP blocks (Gen1)	1						
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR						

Notes:
1. Transceiver performance varies by product line and package offering.
2. EP4CGX30 supports 3.125 Gbps transceivers only in F484 package option.

Cyclone IV E FPGA Features

View device ordering codes on **page 40**.

		Maximum Resource Count for Cyclone IV E FPGAs								
		EP4CE6	**EP4CE10**	**EP4CE15**	**EP4CE22**	**EP4CE30**	**EP4CE40**	**EP4CE55**	**EP4CE75**	**EP4CE115**
Resources	LEs (K)	6	10	15	22	29	40	56	75	114
	M9K memory blocks	30	46	56	66	66	126	260	305	432
	Embedded memory (Kb)	270	414	504	594	594	1,134	2,340	2,745	3,888
	18 x 18 multipliers	15	23	56	66	66	116	154	200	266
Architectural Features	Global clock networks	10	10	20	20	20	20	20	20	20
	PLLs	2	2	4	4	4	4	4	4	4
I/O Features	I/O voltage levels supported (V)	1.2, 1.5, 1.8, 2.5, 3.3								
	I/O standards supported	LVTTL, LVCMOS, PCI, PCI-X, LVDS, mini-LVDS, RSDS, LVPECL, SSTL-18 (1 and II), SSTL-15 (I and II), SSTL-2 (I and II), HSTL-18 (I and II), HSTL-15 (I and II), HSTL-12 (I and II), Differential SSTL-18 (I and II), Differential SSTL-15 (I and II), Differential SSTL-2 (I and II), Differential HSTL-18 (I and II), Differential HSTL-15 (I and II), Differential HSTL-12 (I and II), Differential HSUL-12								
	LVDS channels	66	66	137	52	224	224	160	178	230
External Memory Interfaces	Memory devices supported	DDR2, DDR, SDR								

Cyclone IV GX and E FPGA Series Package and I/O Matrices

View device ordering codes on **page 40**.

	Cyclone IV GX FPGAs (1.2 V)					
	QFN (N)[1]	FBGA (F)				
	148 pin 11 x 11 (mm) 0.5 mm pitch	**169 pin** 14 x 14 (mm) 1.0 mm pitch	**324 pin** 19 x 19 (mm) 1.0 mm pitch	**484 pin** 23 x 23 (mm) 1.0 mm pitch	**672 pin** 27 x 27 (mm) 1.0 mm pitch	**896 pin** 31 x 31 (mm) 1.0 mm pitch
EP4CGX15	72 2	72 2				
EP4CGX22		72 2	150 4			
EP4CGX30		72 2	150 4	290 4		
EP4CGX50				290 4	310 8	
EP4CGX75				290 4	310 8	
EP4CGX110				270 4	393 8	475 8
EP4CGX150				270 4	393 8	475 8

Notes:

1. Quad flat pack, no lead.

636 / 12 — Values on top indicate available user I/O pins; values at the bottom indicate the 2.5 Gbps or 3.125 Gbps transceiver count.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.

	Cyclone IV E FPGAs (1.0 V and 1.2 V)							
	EQFP (E)[1]	FBGA (F)				MBGA (M)	UBGA (U)	
	144 pin 22 x 22 (mm) 0.5 mm pitch	**256 pin** 17 x 17 (mm) 1.0 mm pitch	**324 pin** 19 x 19 (mm) 1.0 mm pitch	**484 pin** 23 x 23 (mm) 1.0 mm pitch	**780 pin** 29 x 29 (mm) 1.0 mm pitch	**164 pin** 8 x 8 (mm) 0.5 mm pitch	**256 pin** 14 x 14 (mm) 0.8 mm pitch	**484 pin** 19 x 19 (mm) 0.8 mm pitch
EP4CE6	91	179					179	
EP4CE10	91	179					179	
EP4CE15	81	165		343		74	165	
EP4CE22	79	153					153	
EP4CE30			193	328	532			
EP4CE40			193	328	532			328
EP4CE55				324	374			324
EP4CE75				292	426			292
EP4CE115				280	528			

Notes:

1. Enhanced thin quad flat pack.

636 — Number indicates available user I/O pins.

Vertical migration (same V_{cc}, GND, ISP, and input pins). For vertical migration, the number of user I/O pins may be less than the number stated in the table.