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POWERING INNOVATION

Fundamentals of DDR3 for QorIQ Processors

FTF-NET-F0686

Mazyar Razzaz
Applications Engineer

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Agenda

- Introduction and Industry Trends
- Memory Organization and Operation
- Features and Capabilities
- Initialization and Register Configurations

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Introduction

- Many customers are deploying and expect DDR3 support on their new product offerings, especially since the price cross-over point occurred in Q1 of 2010
- Since 2008, almost all Freescale networking devices offer DDR3 support
- Many of the QorIQ devices offer DDR3L support
- Freescale devices with DDR3/DDR3L support provide customers with higher performance memories at lower power-consumptions levels
- Industry initial release of DDR4 is expected in 2013

DDR3 – Major Vendors

- Supported by all major memory vendors

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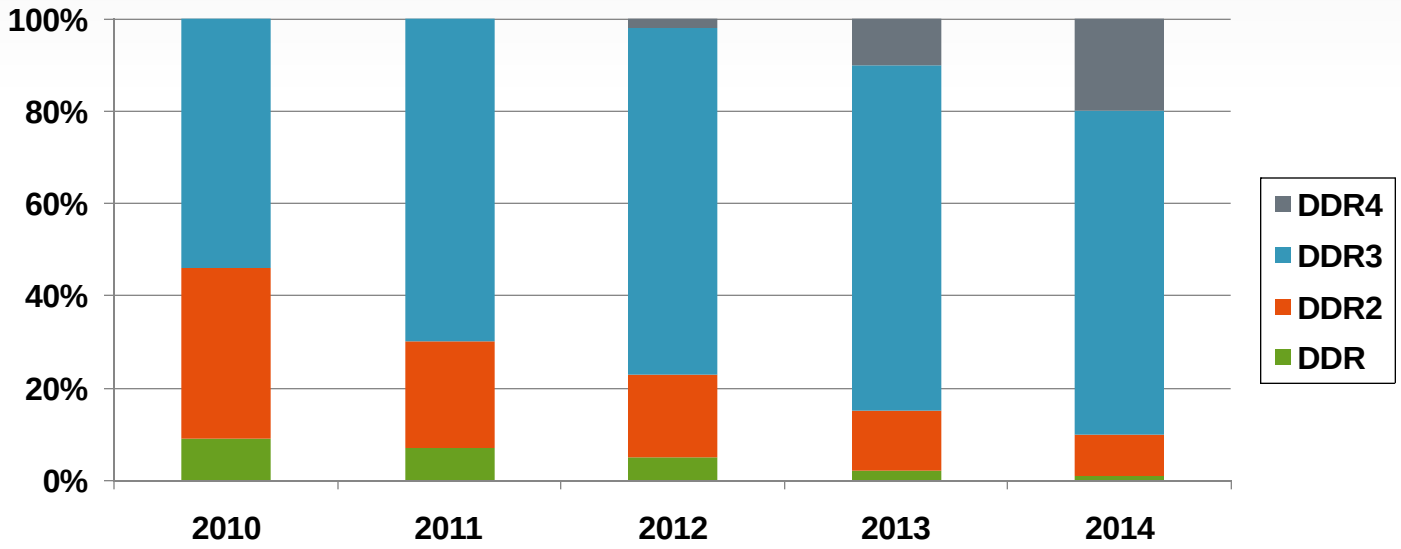
DRAM Migration Roadmap



	2010	2011	2012	2013	2014
DDR	9%	7%	5%	2%	1%
DDR2	37%	23%	18%	13%	9%
DDR3	54%	70%	75%	75%	70%
DDR4	0%	0%	2%	10%	20%

DDR SDRAM Highlights and Comparison

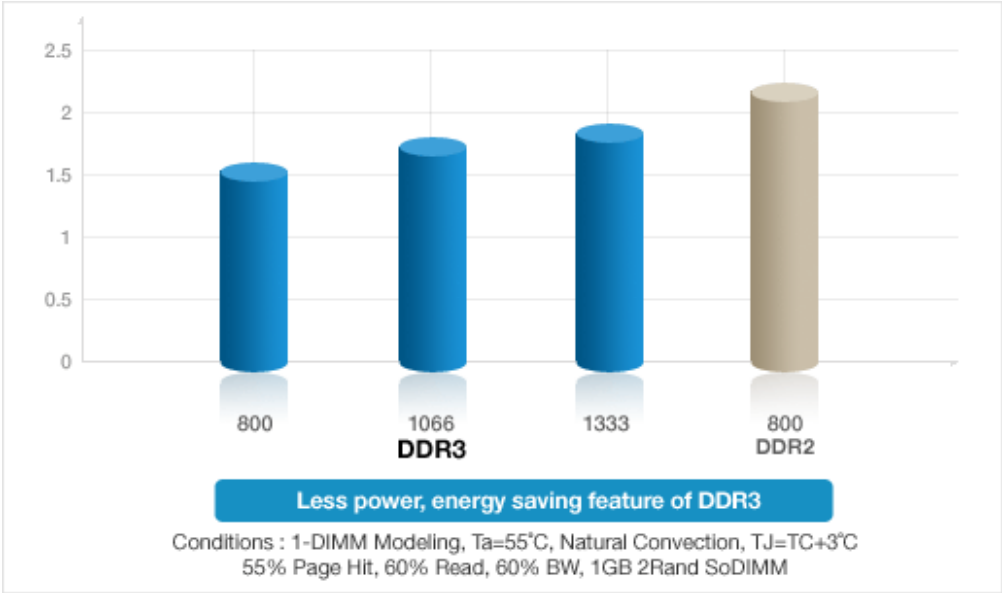
Feature/Category	DDR1	DDR2	DDR3
Package	TSOP	BGA only	BGA only
Densities	128Mb -1Gb	256Mb - 4Gb	512Mb -8Gb
Voltage	2.5V Core 2.5V I/O	1.8V Core 1.8V I/O	1.5V Core 1.5V I/O
I/O Signaling	SSTL_2	SSTL_18	SSTL_15
Internal Memory Banks	4	4 to 8	8
Data Rate	200-400 Mbps	400–800 Mbps	800–1600 Mbps
Termination	Motherboard termination to V_{TT} for all signals	On-die termination for data group. V_{TT} termination for address, command, and control	On-die termination for data group. V_{TT} termination for address, command, and control
Data Strobes	Single Ended	Differential or single	Differential

DDR SDRAM Highlights and Comparison (continued)

Feature/Category	DDR1	DDR2	DDR3
Burst Length	BL= 2, 4, 8 (2-bit prefetch)	BL= 4, 8 (4-bit prefetch)	BL= 8 (Burst chop 4) (8-bit prefetch)
CL/tRCD/tRP	15 ns each	15 ns each	12 ns each
Master Reset	No	No	Yes
ODT (On-die termination)	No	Yes	Yes
Driver Calibration	No	Off-Chip (OCD)	On-Chip with ZQ pin (ZQ cal)
Write Leveling	No	No	Yes

DDR3/DDR3L Power Saving

- DDR3 DRAM provides 25% power savings over DDR2
- DDR3L DRAM provides 15% power saving over DDR3 and 40% over DDR2
- DDR3 vs. DDR2 provides overall memory interface power saving of 35%
- DDR3L vs. DDR2 provides overall memory interface power saving of 50%



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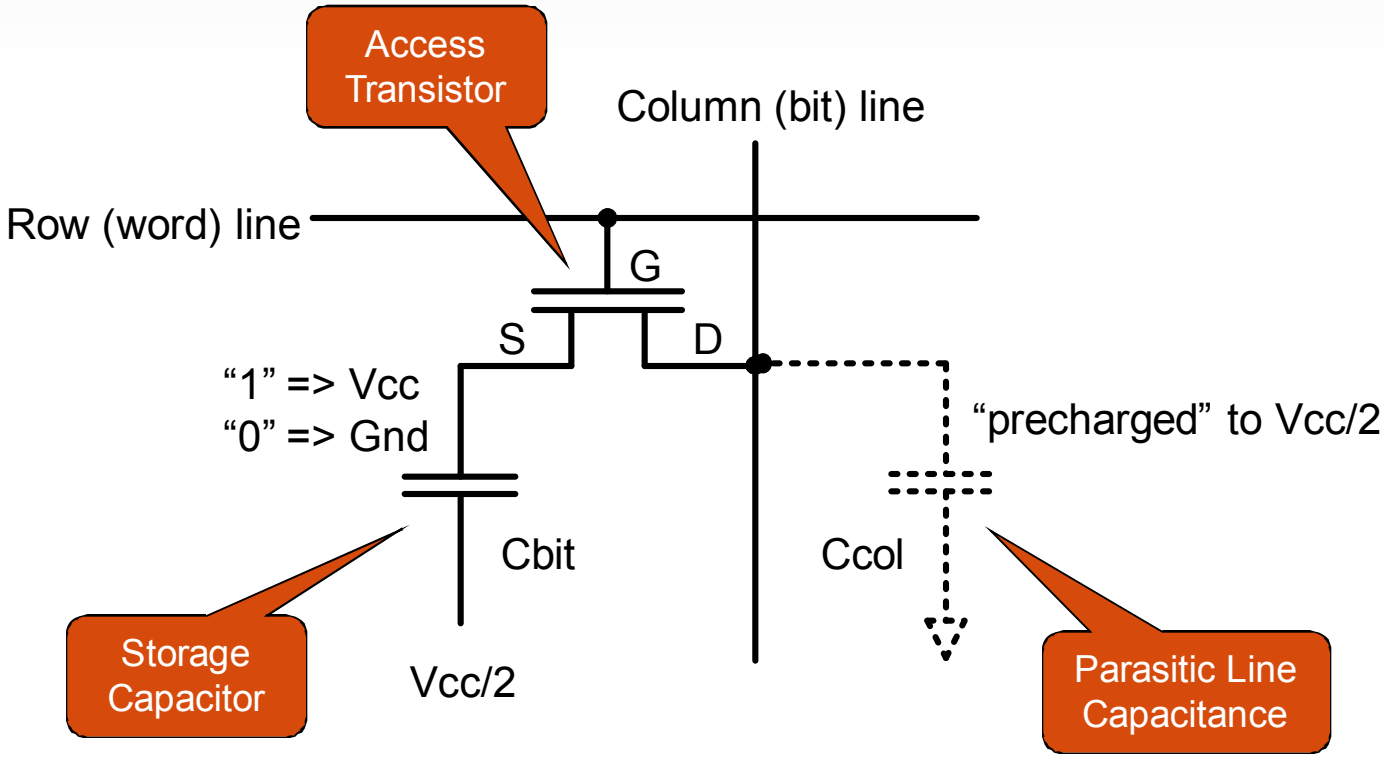
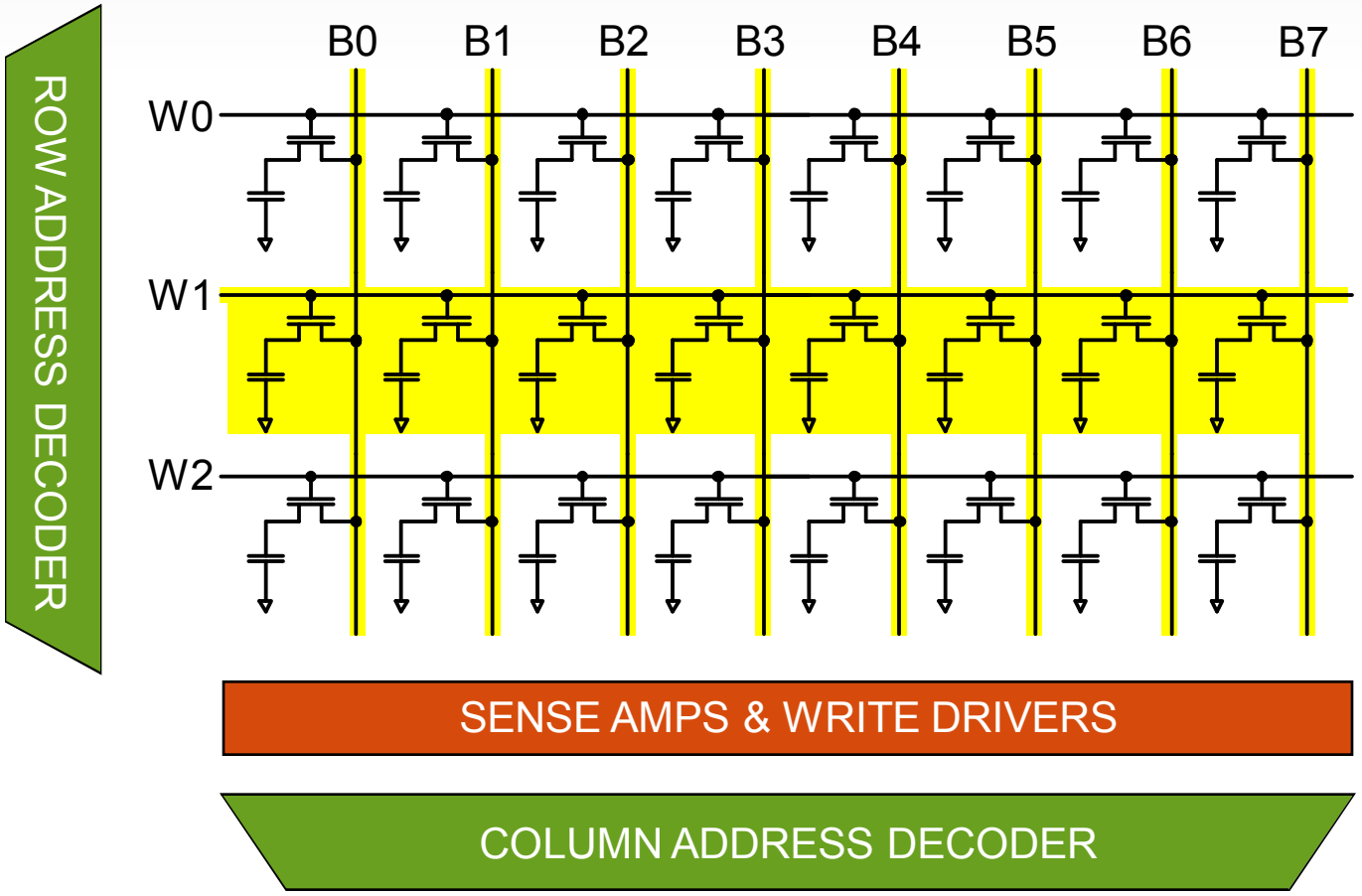
Basic DDR SDRAM

- Memory Organization and Operation

Single Transistor Memory Cell

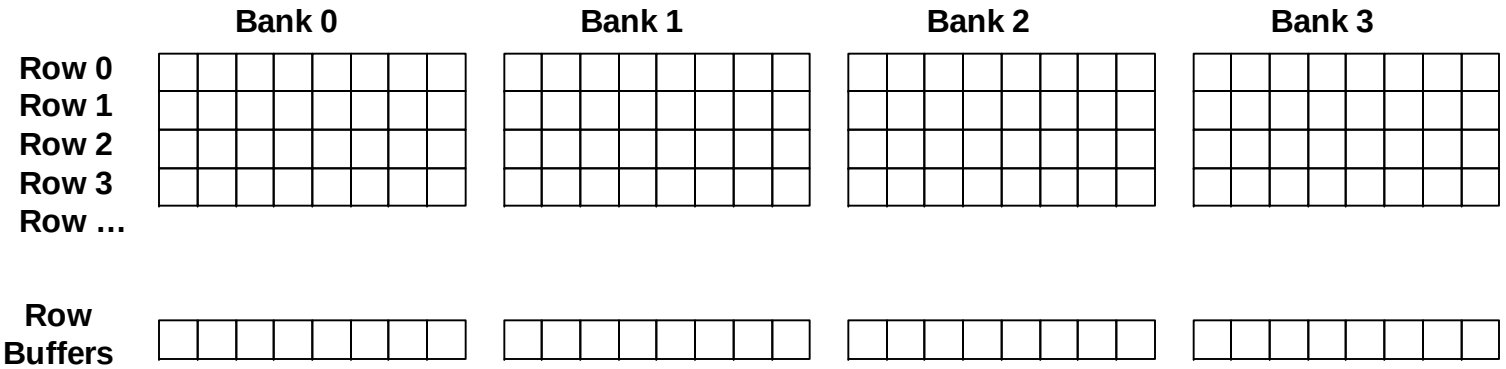


Memory Arrays



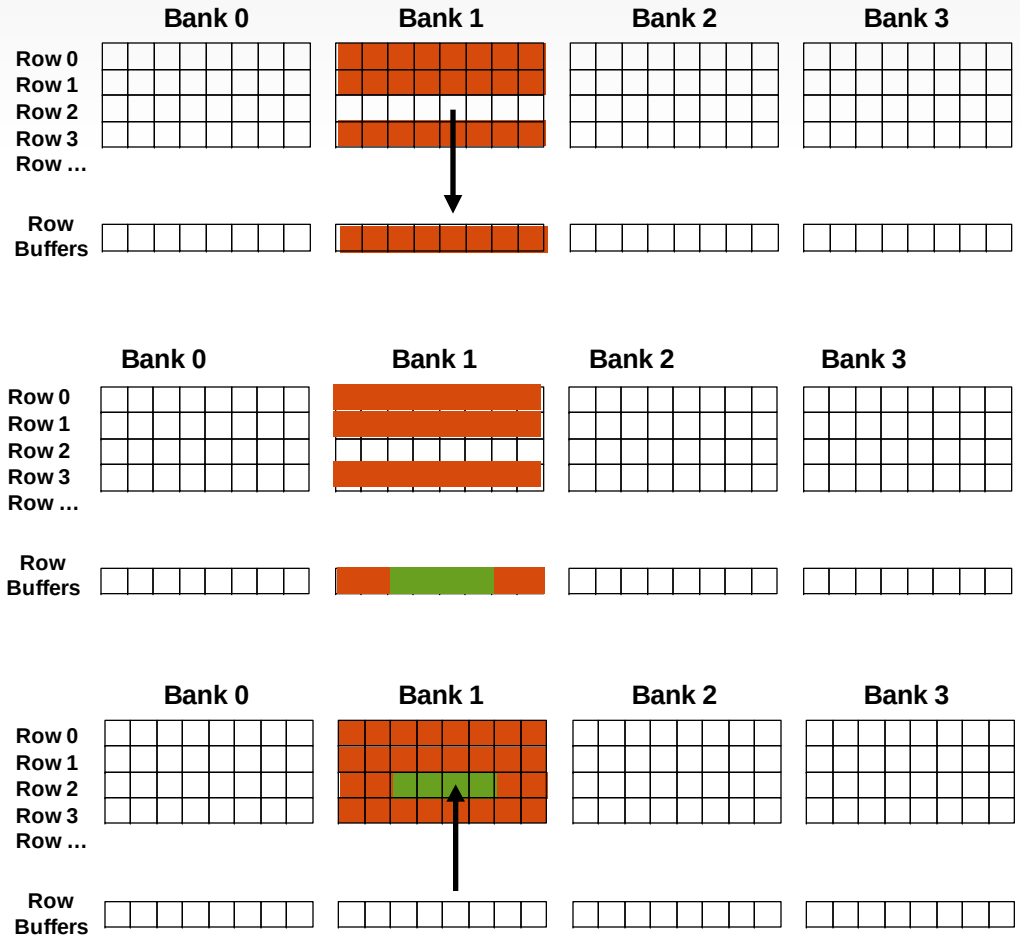
Internal Memory Banks

- Multiple arrays organized into banks
- Multiple banks per memory device
  - DDR1 – 4 banks, 2 bank address (BA) bits
  - DDR2 & DDR3 – 4 or 8 banks, 2 or 3 bank address (BA) bits
  - Can have one active row in each bank at any given time
- Concurrency
  - Can be opening or precharging a row in one bank while accessing another bank
- May be referred to as “internal”, “logical” or “sub-” banks

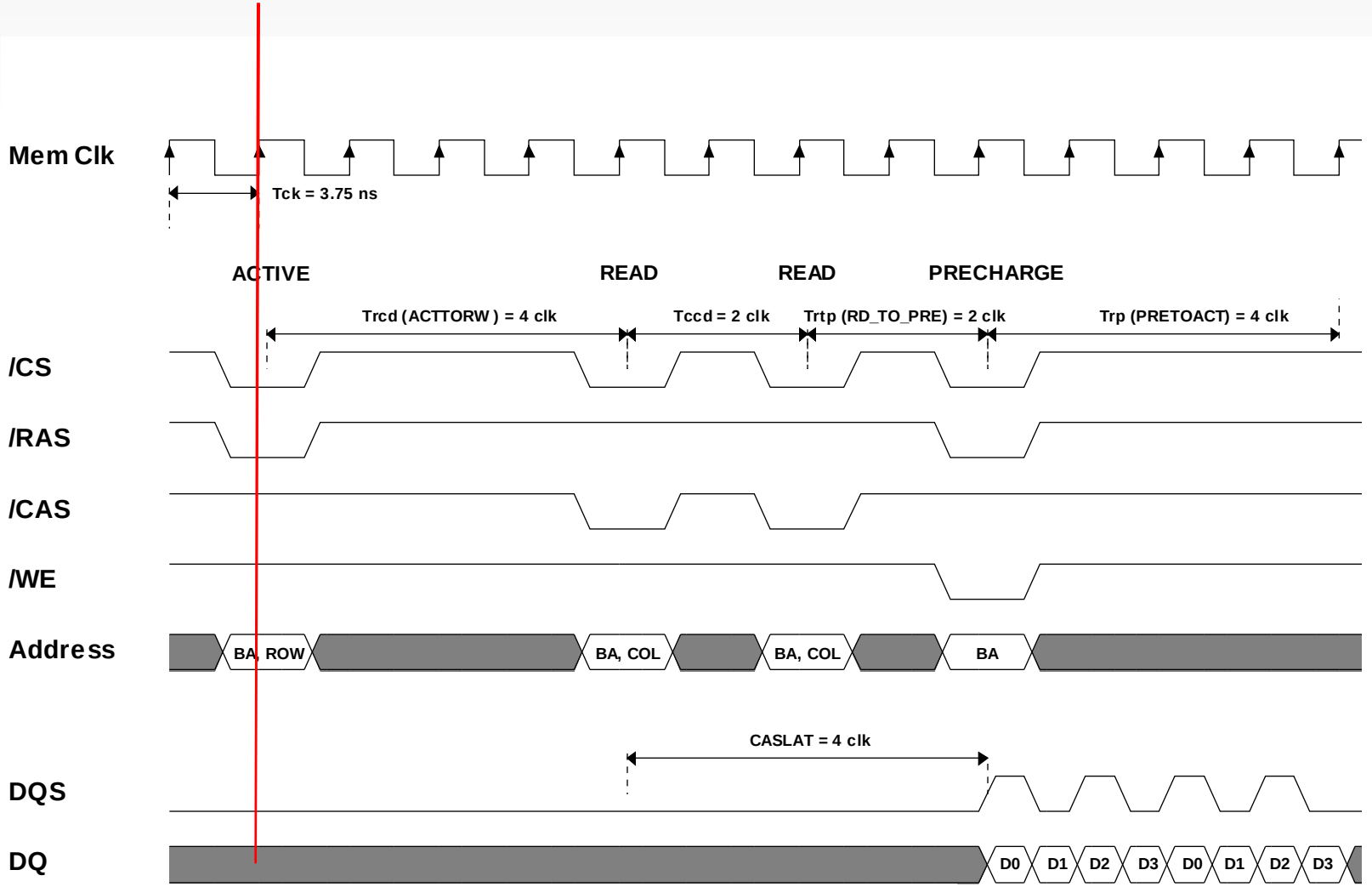


Memory Access

- A requested row is **ACTIVATED** and made accessible through the bank's row buffer
- **READ** and/or **WRITE** are issued to the active row
- The row is **PRECHARGED** and is no longer accessible through the bank's row buffer

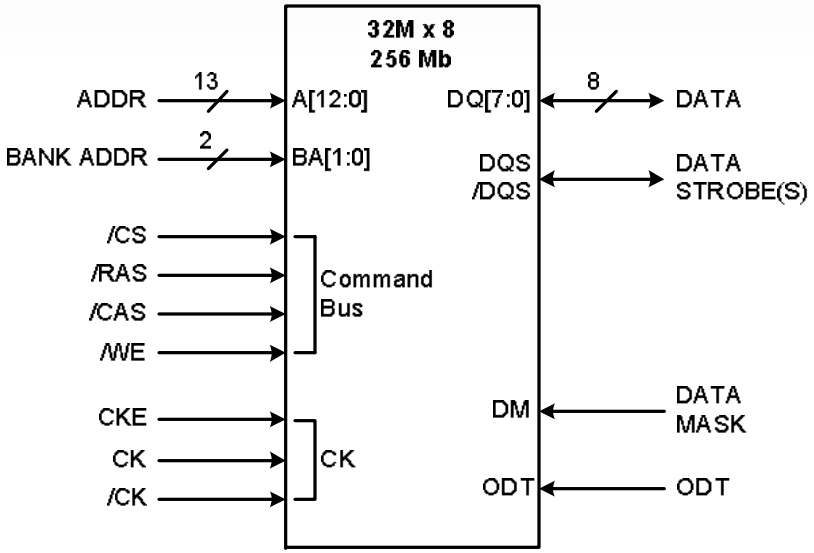


DDR2-533 Read Timing Example



Example – DDR2/3 SDRAM

- Micron MT47H32M8
- 32M x 8 (8M x 8 x 4 banks)
- 256 Mb total
- 13-bit row address
  - 8K rows
- 10-bit column address
  - 1K bits/row (8K total when you take into account the x8 width)
- 2-bit bank address
- Data bus: DQ, DQS, /DQS, DM
- ADD bus: A, BA, /CS, /RAS, /CAS, /WE, ODT, CKE, CK, /CK

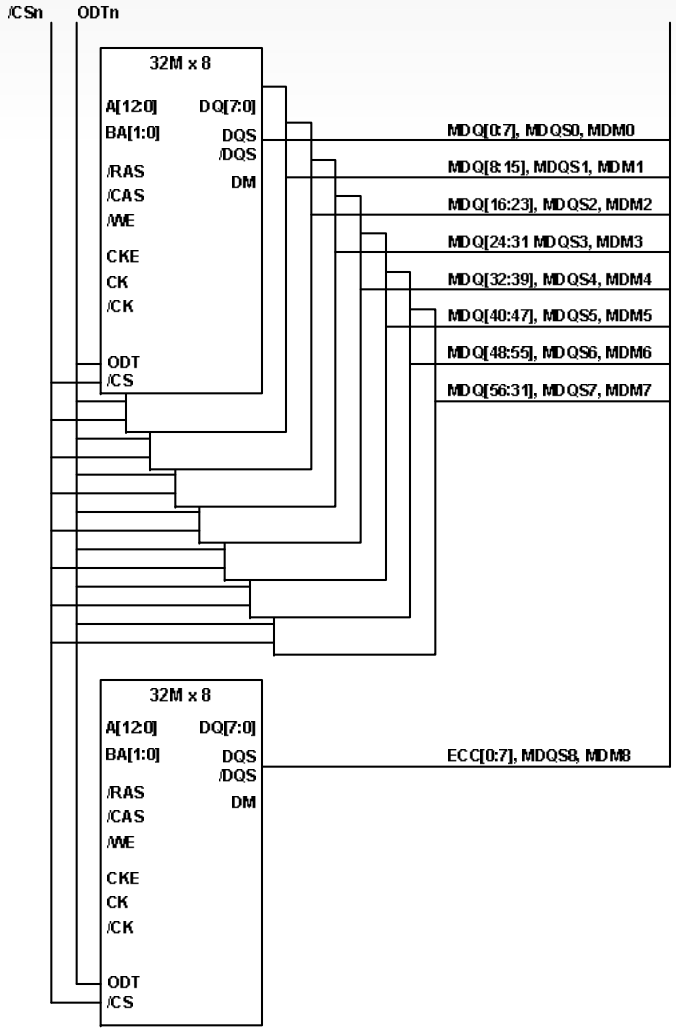


Example – DDR2/3 DIMM

- Micron MT9HTF3272A
- 9 each 32M x 8 memory devices
- 32M x 72 overall
- 256 MB total, single “rank”
- 9 “byte lanes”

Two Signal Bus

- 1- Address, command, control, and clock signals are shared among all 9 DRAM devices
- 2- Data, strobe, data mask not shared



DRAM Module Type

UDIMM: Unbuffered Desktop standard

SODIMM: Notebook standard

MiniDIMM:
Computing and Networking

VLP MiniDIMM:
Computing and Networking

RDIMM: Registered Server standard

VLP RDIMM: Very Low Profile
Computing and Networking

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PowerQUICC DDR Controllers

- Features and Capabilities

DDR1/DDR2/DDR3/DDR3L Controller Features

- Supports most JEDEC standard x8, x16, x32 DDR1 & 2 & 3 devices
- Memory device densities from 64Mb – through 4Gb
- Data rates up to: 333 Mb/s for DDR1, 800 Mb/s for DDR2 and DDR3
- Devices with 12-16 row address bits, 8-11 column address bits, 2-3 logical bank address bits
- Data mask signals for sub-doubleword writes
- Up to four physical banks (chip selects)
- Physical bank sizes up to 4GB, total memory up to 16GB per controller
- Physical bank interleaving between 2 or 4 chip selects
- Memory controller interleaving when more than 2 controllers are available
- Unbuffered or registered DIMMs

DDR1/DDR2/DDR3/DDR3L Controller Features (continued)

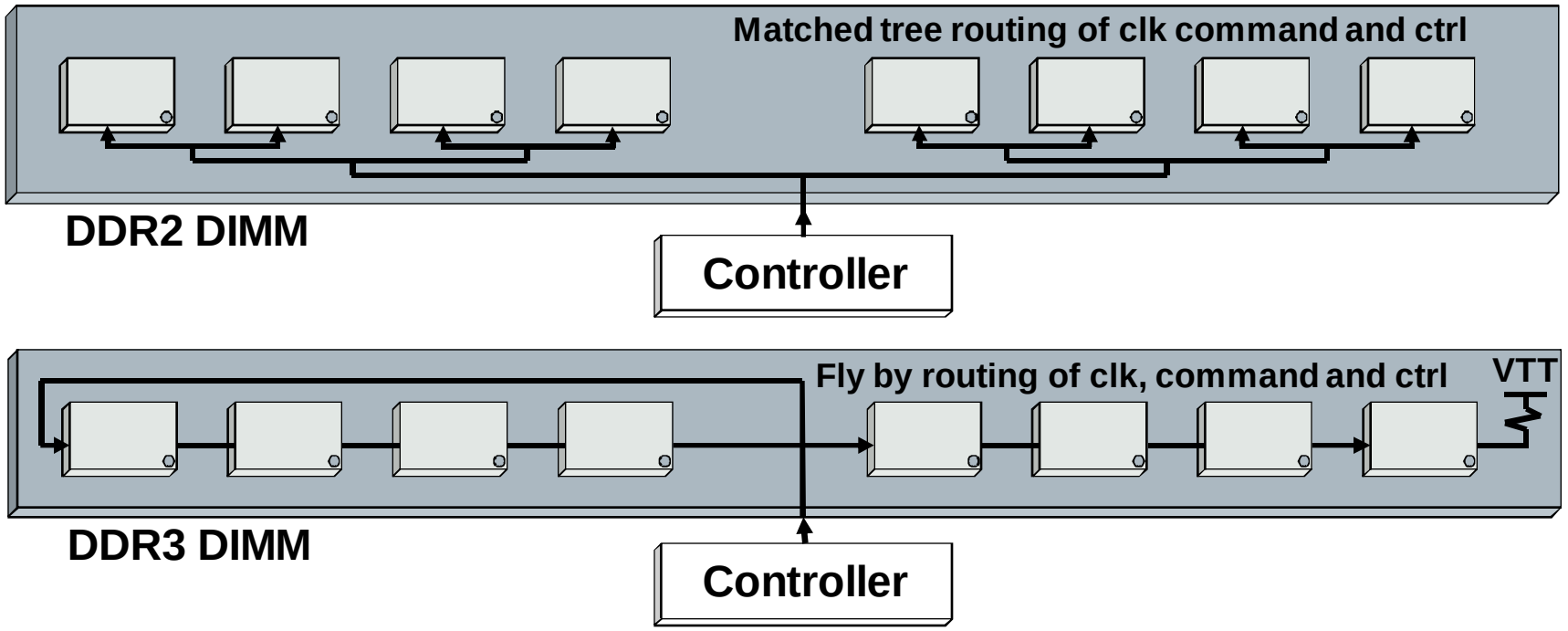
- Up to 32 open pages
  - Open row table
  - Amount of time rows stay open is programmable
- Auto-precharge, globally or by chip select
- Self-refresh
- Up to 8 posted refreshes
- Automatic or software-controlled memory device initialization
- ECC: 1-bit error correction, 2-bit error detection, detection of all errors within a nibble
- ECC error injection
- Read-modify-write for sub-doubleword writes when using ECC
- Automatic data initialization for ECC
- Dynamic power management

DDR2/DDR3/DDR3L Controller Additional Features

- Partial array self refresh
- Address and command parity for Registered DIMM
- Independent driver impedance setting for data, address/command, and clock
- Synchronous and Asynchronous clock-in option
- Write-leveling for DDR3
- Automatic CPO (operational)
- Asynchronous RESET for DDR3
- Automatic ZQ calibration for DDR3
- Fixed or On-the-Fly burst chop mode for DDR3
- Mirrored DIMM supported
- Many QorIQ devices offer full DDR3L support

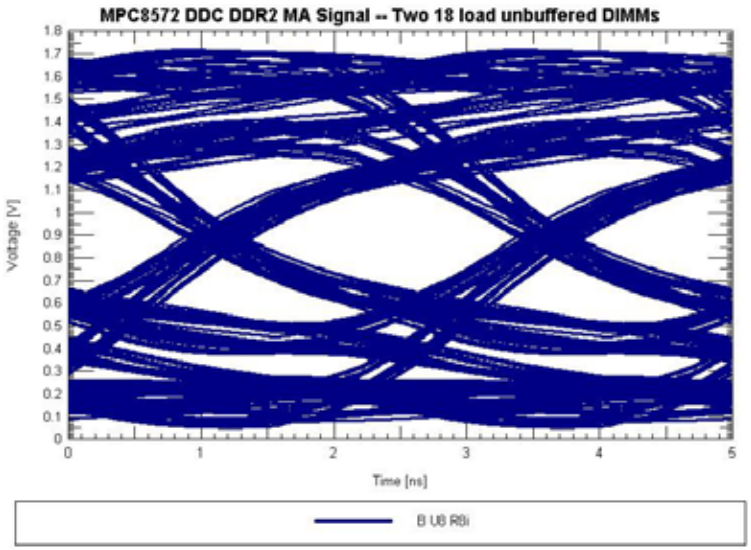
Fly-By Routing Topology

- Introduction of “fly-by” architecture
  - Address, command, control & clocks
  - Improved signal integrity…enabling higher speeds
  - On module termination

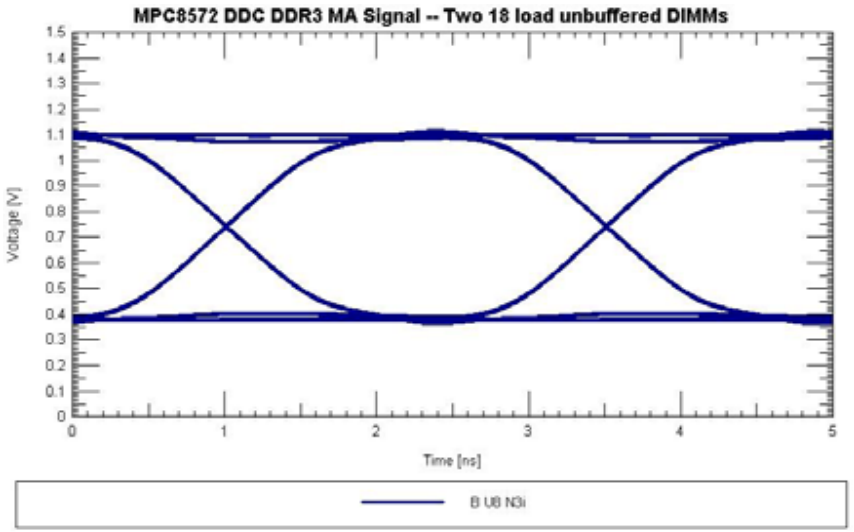


Fly-By Routing Improved SI

DDR2 Matched Tree Routing

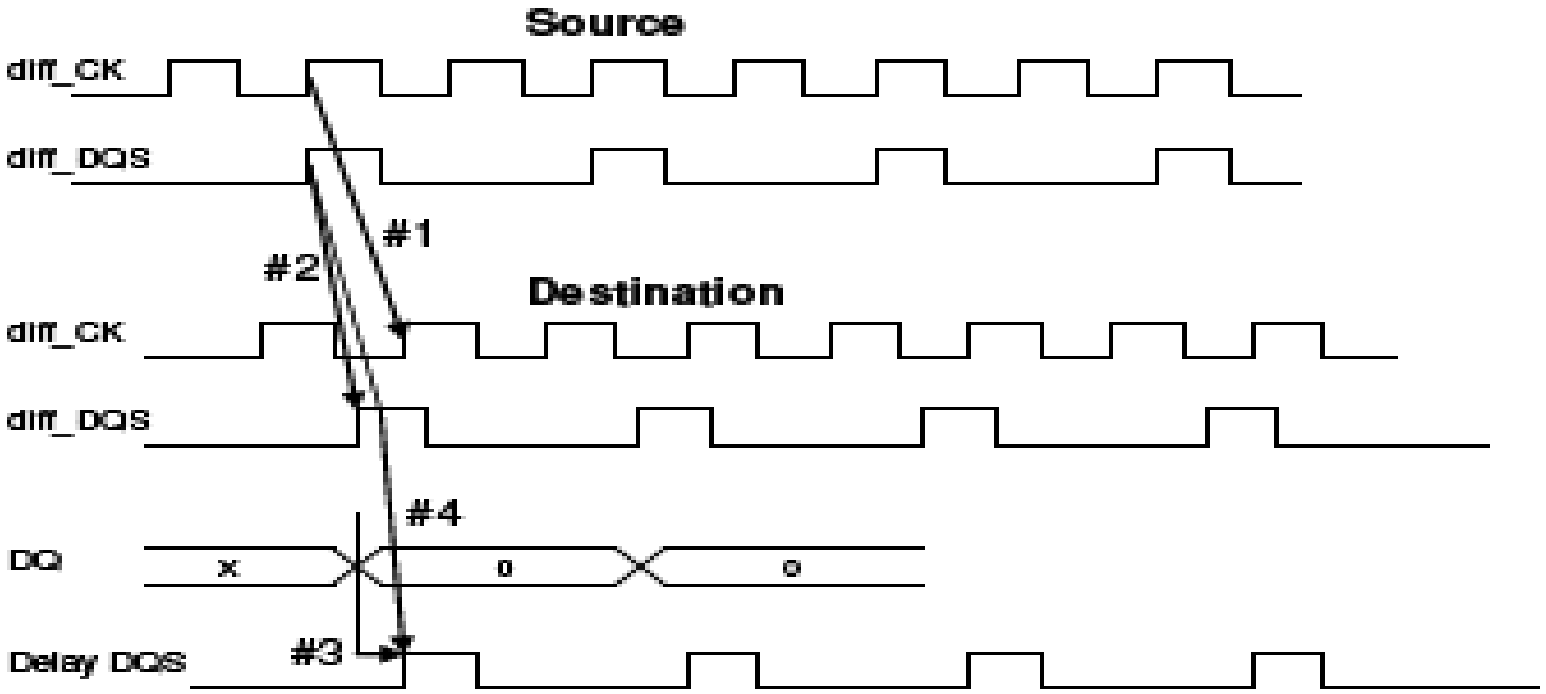


DDR3 Fly By Routing



What Is Write Leveling

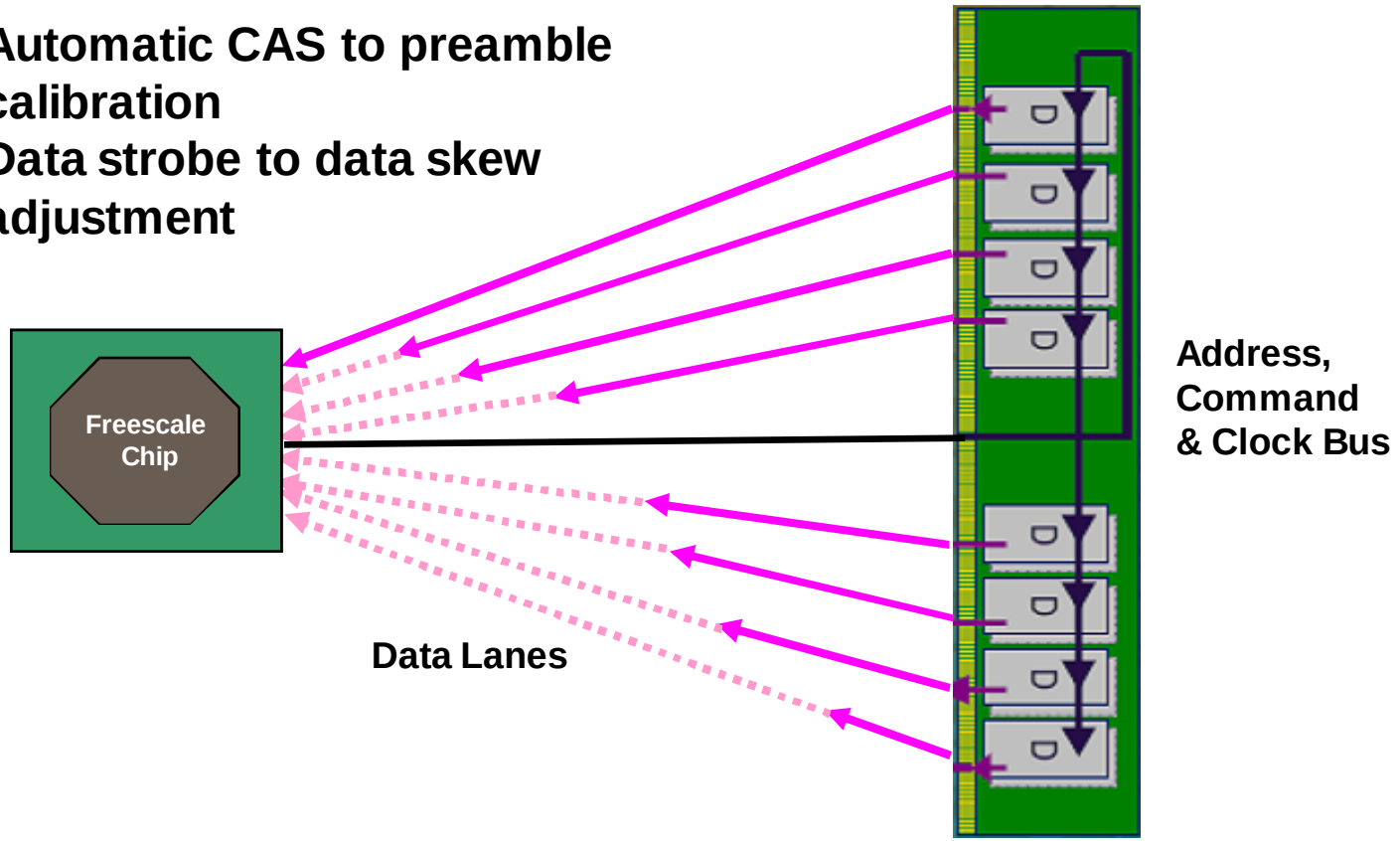
- During a write cycle, the skew between the clock and strobes is increased due to the fly-by topology. The write leveling will delay the strobe (and the corresponding data lanes) for each byte lane to reduce/compensate for this delay



Read Adjustment

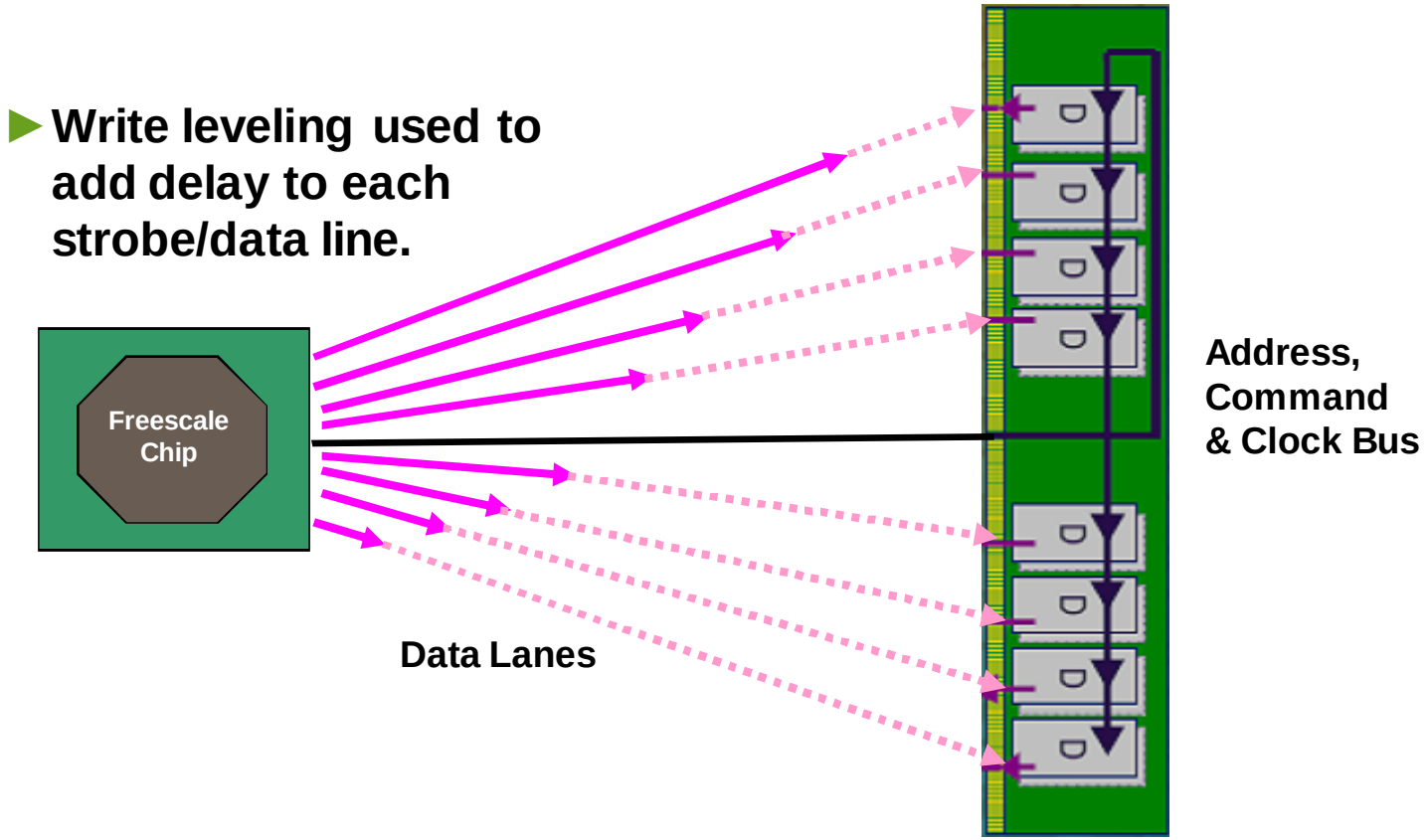
- Instead of JEDEC's MPR method, Freescale controllers use a proprietary method of read adjust method. Auto CPO will provide the expected arrival time of preamble for each strobe line of each byte lane during the read cycle to adjust for the delays cased by the fly-by topology

  - **Automatic CAS to preamble calibration**
  - **Data strobe to data skew adjustment**



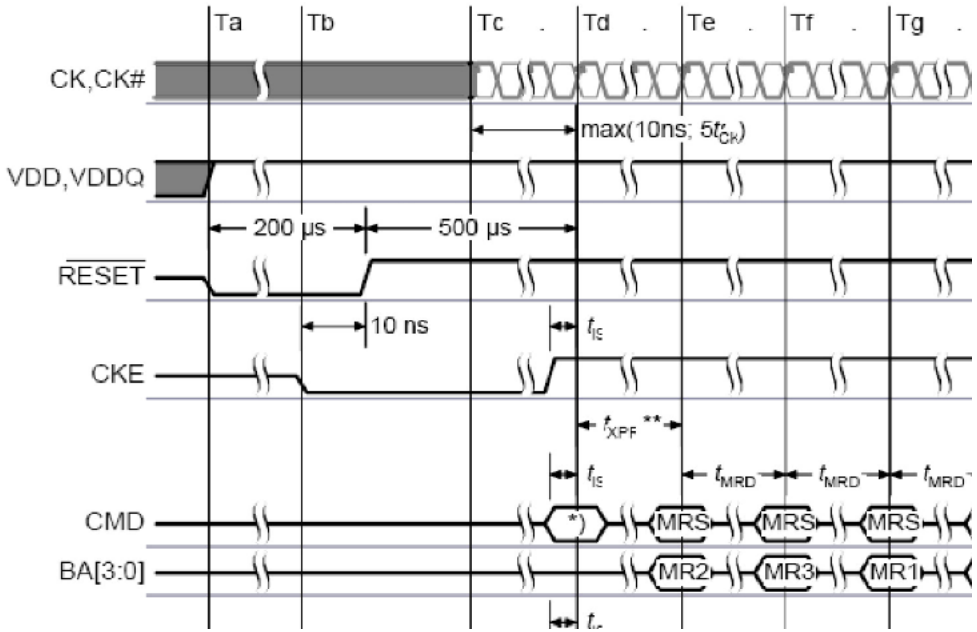
Write Adjustment

- Write leveling sequence during the initialization process will determine the appropriate delays to each strobe/data byte lane and add this delay for every write cycle



DDR3/DDR3L RESET Pin

- An asynchronous RESET# pin is available in all DDR3/DDR3L DRAM
  - Prevent illegal commands and/or unwanted states
  - Resets all state information
  - No power-down required
  - Destructive to data content
  - Independent of memory controller



DDR3/DDR3L ZQ Calibration Pin

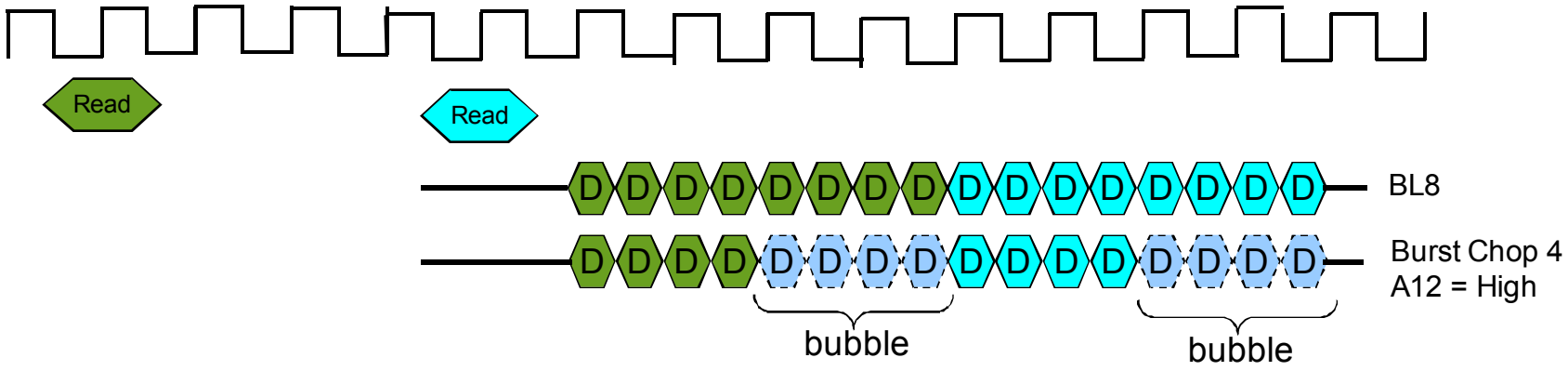
- The RZQ resistor is connected between the DDR3 memory and ground
  - Value = 240 Ohm +/- 1%
  - Permits driver and ODT calibration
- Easier and more accepted than DDR2's (optional) OCD method
- Freescale controllers support both ZQ calibration commands
  - ZQCL – used during initialization (..takes longer)
  - ZQCS – used during normal operation (…periodic and takes less time)

Table 9-26. DDR_ZQ_CNTL Field Descriptions

Bits	Name	Description
0	ZQ_EN	ZQ Calibration Enable. This bit determines if ZQ calibrating will be used. This bit should only be set if DDR3 memory is used (DDR_SDRAM_CFG[SDRAM_TYPE] = 3'b111). 0 ZQ Calibration will not be used. 1 ZQ Calibration will be used. A ZQCL command will be issued by the DDR controller after POR and anytime the DDR controller is exiting self refresh. A ZQCS command will be issued every 32 refresh sequences to account for VT variations.

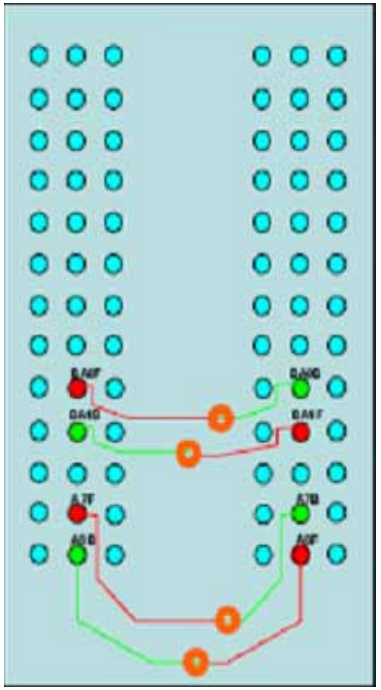
Burst Length Selection

- DDR3 always issues Burst Length of 8
  - Burst length of 8 is default
- DDR3 also supports pseudo Burst Length of 4
  - Fixed burst chop 4 (BC4)
  - On-the-fly burst chop (OTF BC4/8)
  - For P4080 use 8BL, for other devices use BC4 or OTF BC

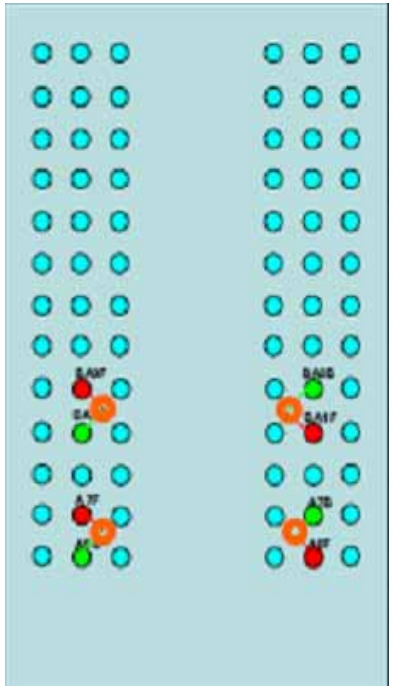


DIMM Mirroring…

- Freescale DDR3 memory controller supports address mirroring



Non-Mirrored



Mirrored

Edge Connector Signal	SDRAM Pin, Standard	SDRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
…	…	…
A15	A15	A15
BA0	BA0	BA1
BA1	BA1	BA0
BA2	BA2	BA2

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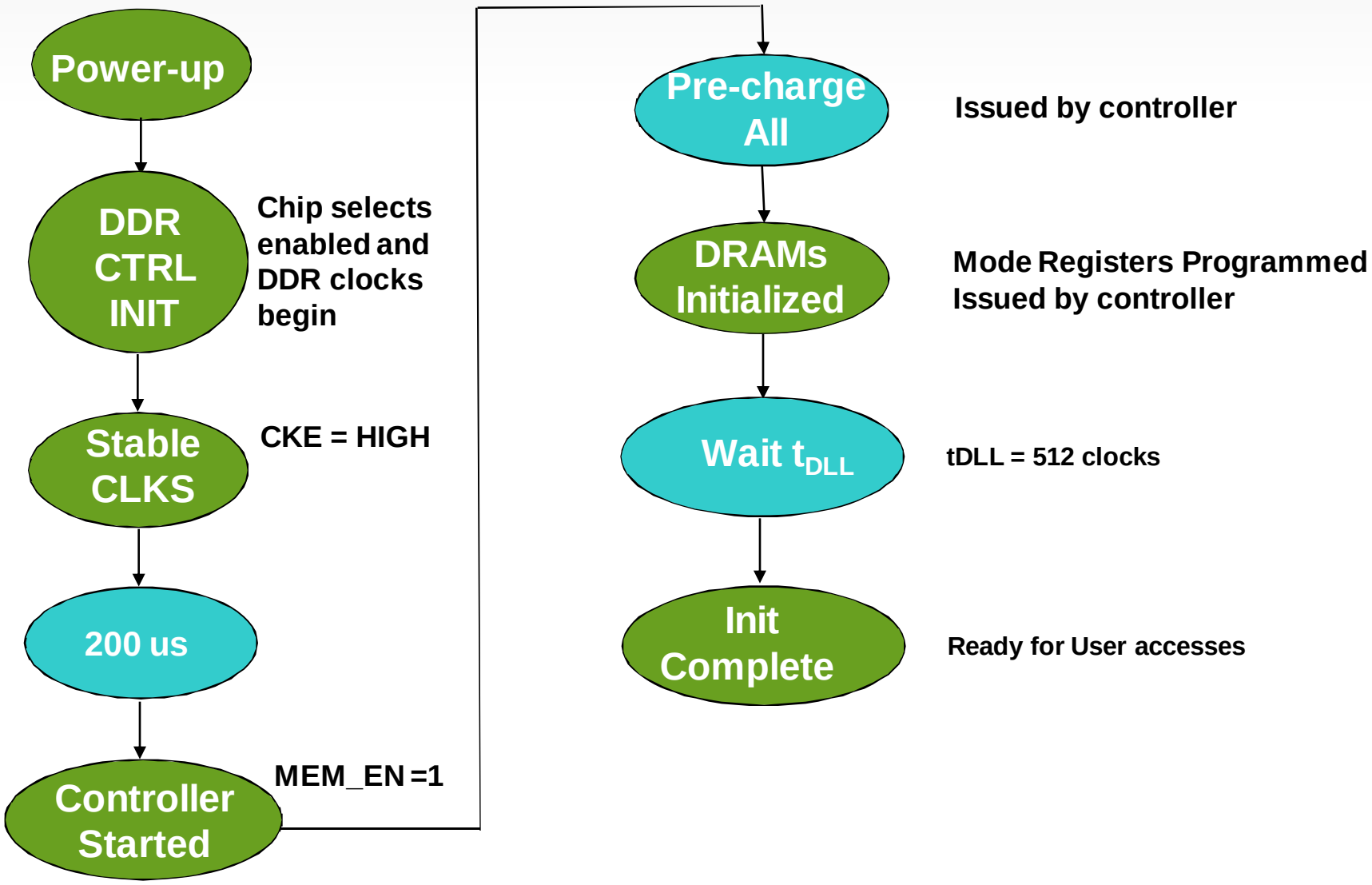
DDR3L support

- DDR3L (1.35V) is a low voltage version of the DDR3 (1.5V)
- DDR3L meets the exact same functional and timing specifications of DDR3
- VIH/VIL differences are compensated by corresponding derating values to Vref resulting in no change in AC timing, and timing budget calculation
- The main considerations for using DDR3L are:
  - Memory controller needs to support DDR3L
    - P1023, P1017, P1010, P1014, P2040, P3041, P5020
  - The supply voltage needs to be at 1.35V
  - Using DDR3L SDRAM

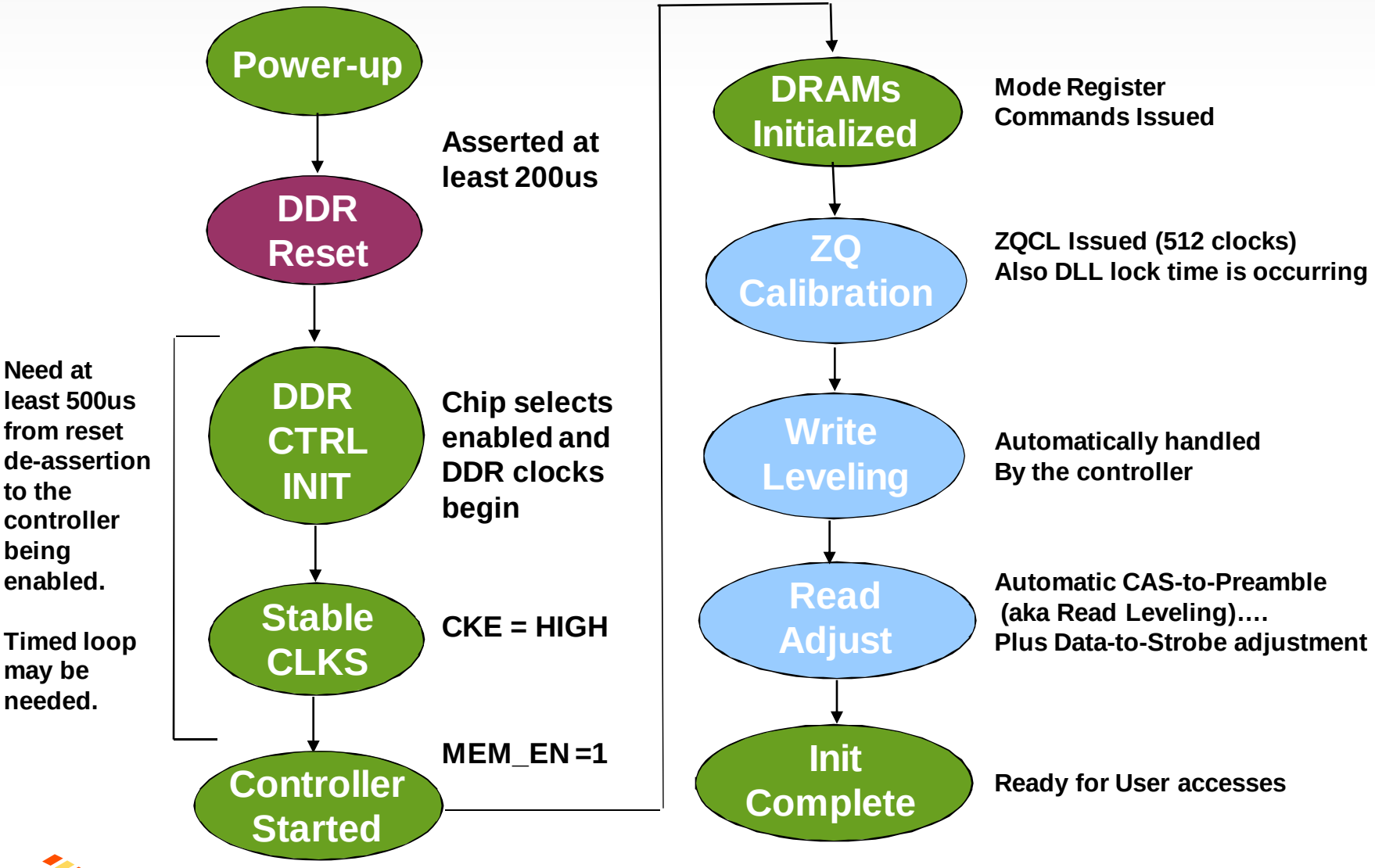
PowerQUICC DDR Controllers

- Initialization and Register Configurations

DDR2 Initialization Flow



DDR3 Initialization Flow



Register Configuration

- Two general type of registers to be configured in the memory controller
- First register type is set to the DRAM related parameter values that are provided via SPD or DRAM datasheet
- Second register type is the non-SPD values that are set based on customer's application. For example:
  - On-die-termination (ODT) settings for DRAM and controller
  - Driver impedance setting for DRAM and controller
  - Clock adjust, write data delay, Cast to preamble override (CPO)
  - 2T or 3T timing
  - Burst type selection (fixed or on-the-fly burst chop mode)
  - Write-leveling start value (WRLVL_START)
- Register configuration tools are available for FAEs to generate or analyze customer DDR register configuration

Summary

- DDR3 is mainstream now
- DDR4 is expected to start entering the market by 2013
- All QorIQ devices support DDR3
- All features of DDR3, such as write leveling, ZQ calibration, ODT, Mirrored DIMM, … are supported by the memory controller in QorIQ devices
- Follow JEDEC recommended topologies for discrete parts
- Configuration and initialization of memory controller is easily achieved
- For additional information go to Useful References page

Session materials will be posted @
www.freescale.com/FTF
Look for announcements in the FTF Group on LinkedIn or follow Freescale on Twitter

Useful References

- Books:
  - DRAM Circuit Design: A Tutorial, Brent Keeth and R. Jacob Baker, IEEE Press, 2001
- Freescale AppNotes:
  - AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces
  - AN2910 Hardware and Layout Design Considerations for DDR2 Memory Interfaces
  - AN2583 Programming the PowerQUICCIII / PowerQUICCII Pro DDR SDRAM Controller
  - AN3369 PowerQUICC DDR2 SDRAM Controller Register Setting Considerations
  - AN3939 PQ & QorIQ Interleaving
  - AN3940 Layout Design Considerations for DDR3 Memory Interface
  - AN4039 PowerQUICC DDR3 SDRAM Controller Register Setting Considerations
- Micron AppNotes:
  - TN-46-05 General DDR SDRAM Functionality
  - TN-47-02 DDR2 Offers New Features and Functionality
  - TN-47-01 DDR2 Design Guide
  - TN-41-07 DDR3 Power-Up, Initialization, and Reset
  - TN-41-08 DDR3 Design Guide
- JEDEC Specs:
  - JESD79E Double Data Rate (DDR) SDRAM Specification
  - JESD79-2F DDR2 SDRAM Specification
  - JESD79-3D DDR3 SDRAM Specification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