Application Note

MB86298 ‘Ruby’
EMI Optimization using SSCG

History

Date	Author	Version	Comment
22.06.2009	AvT	1.00	Draft version
24.08.2011	AvT	1.10	Removed 666MHz PLL clock references and related descriptions.
25.08.2011	AvT	1.20	Minor corrections (typo page 5, addition to diagram)

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1 Spread-Spectrum Clocking Introduction

Spread-spectrum clocking has become more popular in portable electronics devices because of faster clock speeds and the increasing integration of high-resolution LCD displays in smaller and smaller devices. As these devices are designed to be lightweight and inexpensive, passive EMI reduction measures such as capacitors or metal shielding are not a viable option. This document briefly describes the functionality and use of the Spread-Spectrum Clock Generation (SSCG) unit of the MB86298 'Ruby' display controller device.

A configurable spread-spectrum clock generator unit is integrated in MB86298 'Ruby' in order to be able to provide a modulated clock signal (as an alternative, parallel to the output of the internal PLL unit), for use by the GDC's internal units. Actually, this means that a modulated clock signal can be generated seperately for:

- the internal circuitry
- the output display controllers (also seperately for each)

The purpose of the SSCG is to spread the electromagnetic energy generated in a particluar bandwidth over a frequency domain, resulting in a wider bandwidth, reducing the spectral density of the EMI produced by the device. The radiated energy itself is not reduced, but simply distributed in a frequency domain.

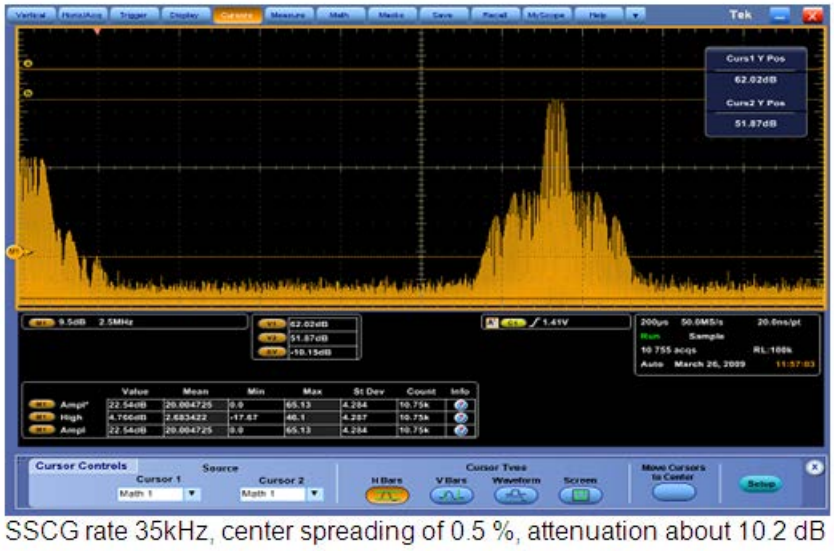


Figure 1 Screenshot of EMI analysis using SSCG

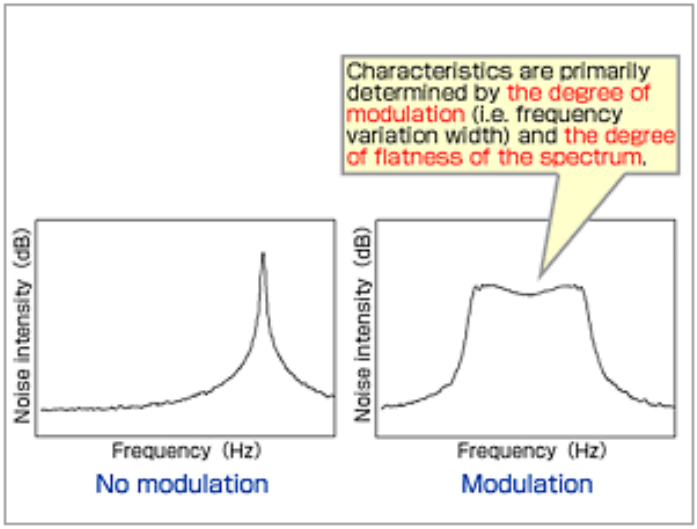


Figure 2 EMI improvement using SSCG

2 The SSCG unit in MB86298 'Ruby'

The SSCG unit plays an essential role in the MB86298 'Ruby' GDC providing the 'heartbeat' of the digital units in the device. Whereas the internal PLL provides a non-modulated clock to the internal units via the Clock/Reset Distribution unit, the SSCG can be configured and then activated to provide a modulated clock signal.

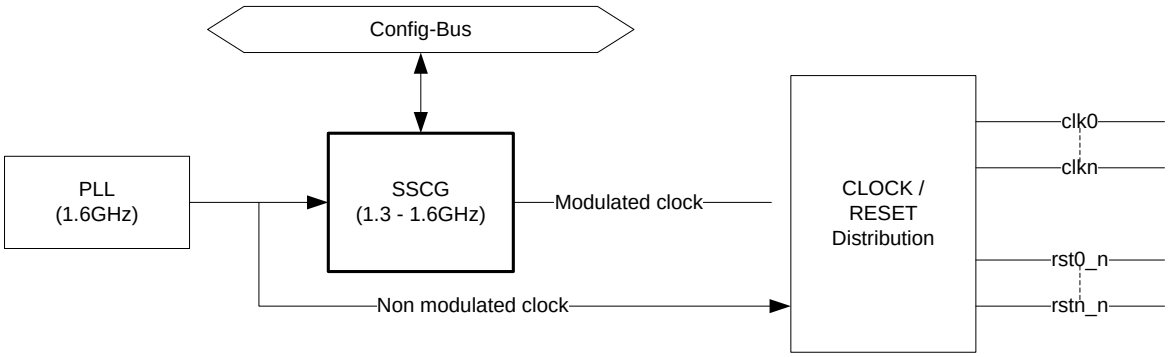


Figure 3 SSCG Location

2.1 Operating Frequency Ranges

The SSCG unit can be operated in the following input frequency range:

- Ruby SSCG unit: 1.3 GHz – 1.6 GHz

2.2 Modulation Parameters

2.2.1 Modulation Period

The SSCG unit can produce a modulated clock signal whose period (or wavelength) is variable in the range of:

- 1/1,048,320 to 1/256

of the (input) PLL clock.

Example
With a PLL input clock of 1.6 GHz, this means the period of the modulated signal can be theoretically in a range between 1,5 KHz (1.6 GHz * [1/1,048,320]) and 6,25 MHz (1.6 GHz * [1/256])

Recommend period range 15 kHz-35 kHz
(0xB4 <= SSCG_PERIOD <= 0x1A4)

2.2.2 Modulation Period Delta (Jitter)

The 'Modulation Period Delta' is the amount by which the period of the modulated output signal is intentionally 'jittered', i.e. alternately shifted up and down in the frequency spectrum.

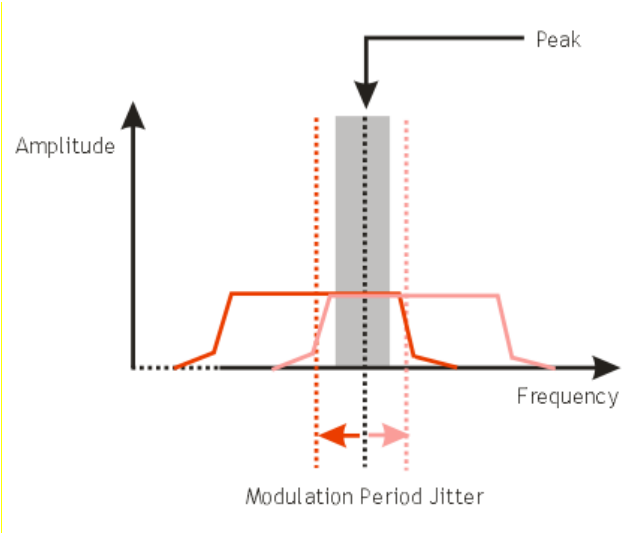


Figure 4 Modulation Period Jitter

2.2.3 Modulation Type

The term 'Modulation Type' refers to the direction in which the frequency spectrum of the modulated output signal is spread. The following modulation types can be selected:

- Non-modulated
  i.e. the SSCG is bypassed and the PLL signal is used.
- Downspread
  The frequency spread offset is shifted downwards (to the left) of the frequency spectrum.
  This modulation applies to all internal bus clocks and the memory clock domains. It could be used for the Display Clock signals, but then you must pay very careful attention to the resulting video timing (whether this causes display driving problems).
- Upspread **(not useable with MB86298 'Ruby'!)**
  The frequency spread offset is shifted upwards (to the right) of the frequency spectrum
- Center spread (default). The frequency spread offset is centered on the PLL frequency (x-axis of the frequency spectrum), DC offset = 0.
  This modulation type applies to the Display Clock signal only (not useable for the internal bus clocks and the memory clock domains).

Note:
The upspread option is not used with MB86298 'Ruby'.

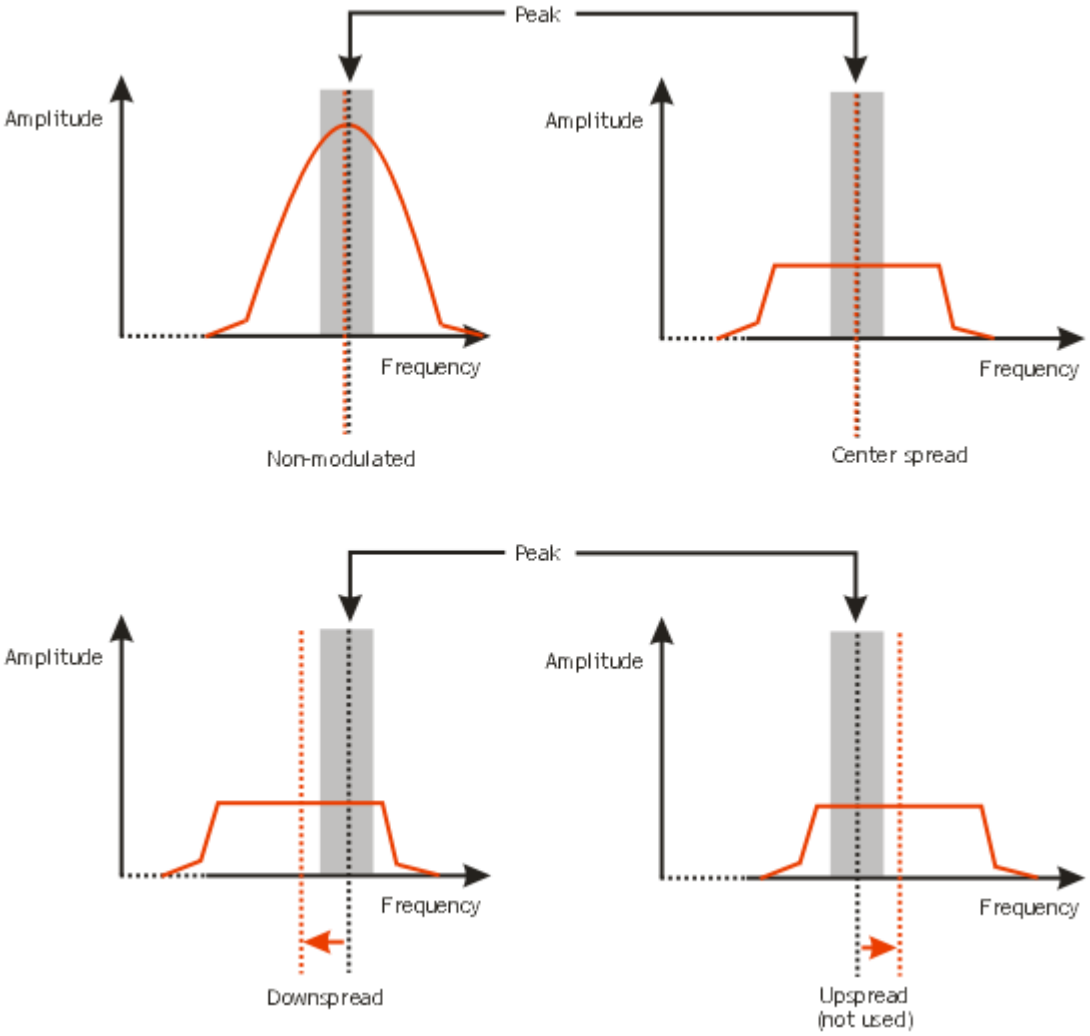


Figure 5 Modulation Types

2.2.4 Modulation Peak

The Modulation Peak (set using the SSCG_PEAK_FREQUENCY register) has two settings:

- SSCG_PEAK_FREQUENCY = 0
  Varies the Modulation Peak from 0 to ±3% (recommended value due to the latency of internal calculations)
- SSCG_PEAK_FREQUENCY = 1
  Varies the Modulation Peak from 0 to ±6%

For signal stability reasons, the 'Modulation Peak', i.e. maximum or minimum modulation frequency value of the modulated output signal is restricted to a specific value range. The values are as follows:

- Default: ±1.0%
- Downspread: 0 to -1.56%
- Center spread: -1.56% to +1.56%

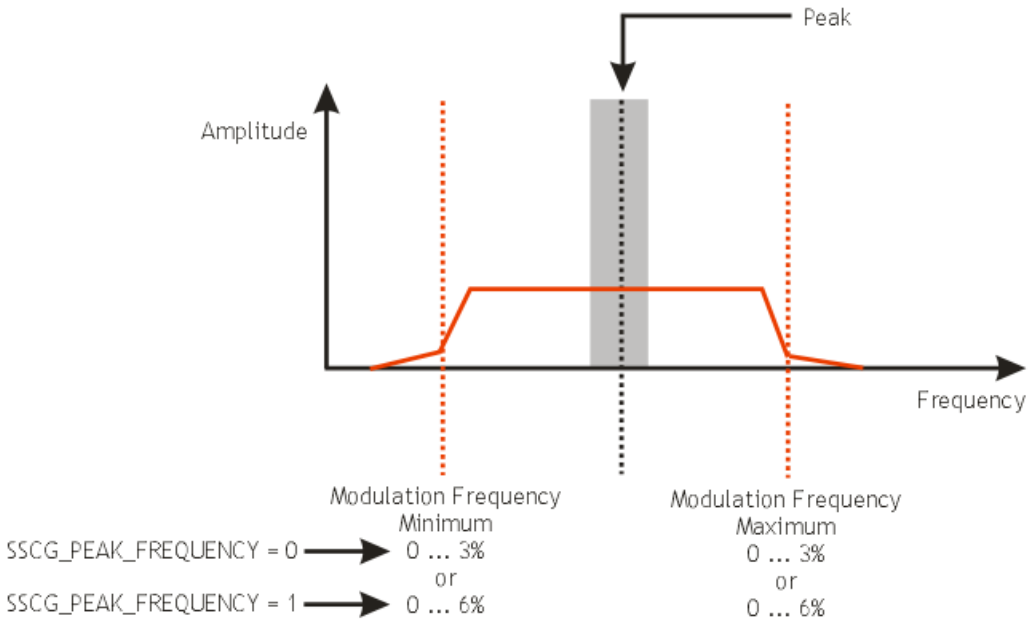
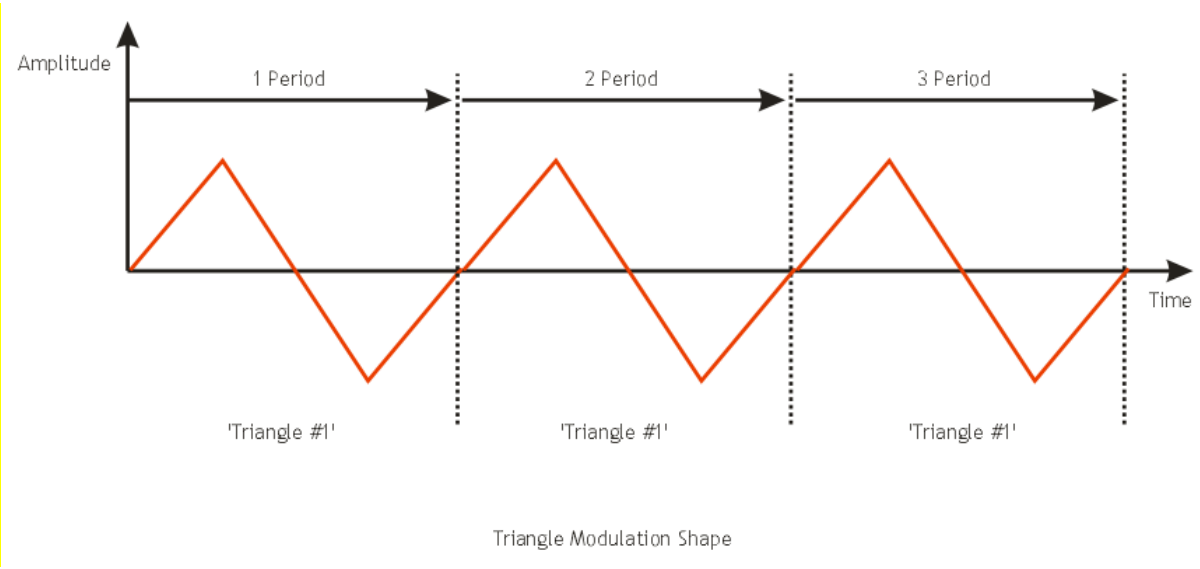


Figure 6 SSCG Modulation Peak

2.2.5 Modulation Shape

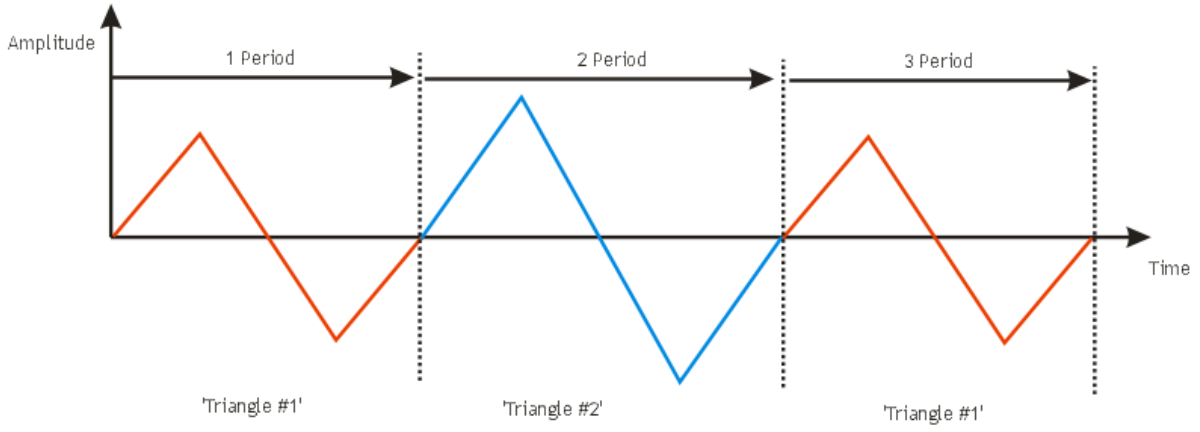
The 'Modulation Shape' is the form of signal which is used to modulate the main output clock signal. There are two shapes:

- Triangle
  A single triangular shape with a constant period is used for modulation.



Triangle Modulation Shape

- 'Dual Triangle'
  This shape is used when the duty cycle of the working period of the modulated output signal is intentionally 'jittered' or modified (using the SSCG_PERIOD_JITTER register) to level out small peaks in the frequency spectrum of the modulated clock signal. The amplitude of the 'second triangle shape' is also slightly higher than that of the first. The final modulation shape is essentially the result of continuously alternating between two different triangle shapes.



Dual Triangle Modulation Shape

2.3 Frequency Offset (DC Offset)

A frequency (DC) offset is an amount by which the average value of the periodic function is not centered around the x-axis.
A periodic signal has a DC offset component if it is not centered about the x-axis. In general, the DC value is the amount that must be subtracted from the signal to center it on the x-axis. by definition:

$$A_0 = \int_{-T/2}^{T/2} f(x)dx$$

With A0 being the DC offset. If A0 = 0, the function is centered and has no offset.
This parameter is set using the SSCG_FOFFSET register.

3 Selecting the SSCG Operating Frequency

This depends on the physical application (your design).
We recommend an SSCG operating frequency of 20 kHz.

4 How to configure the SSCG Unit

4.1 SSCG Unit Default Values

The SSCG unit has the following default settings:

SSCG_PERIOD = 35 kHz
SSCG_PERIOD_JITTER = 0x90. Note the recommended value for use is 0x70!

SSCG_CTRL.SSCG_TYPE = 0x11 (Center spread)
Modulation Peak = +/- 1.5%
SSCG_FOFFSET = 0x0
SSCG_IEN = 0

4.2 Configuring the SSCG Registers

Using the Hardware Manual, select one of the tables which list the settings of the various SSCG registers (Chapter 4, tables 4-2, 4-3, 4-4).

Example
An operating frequency of 15 kHz is required for the SSCG and the PLL clock is running at 1.6 GHz. In the current Hardware manual, the relevant table is:

- Table 4-7 SSCG speed of 15KHz (refer to 1.6GHz PLL clock) – see below

Given that you have decided (for signal stability reasons) to use a Modulation Peak of 0 to ±3% and the default value for SSCG_PERIOD_JITTER (0x90), then read the following table this way:

SSCG_PEAK_FREQUENCY				0	1
SSCG_TYPE	SSCG_PERIOD	SSCG_PERIOD_DELTA	Modulation Peak %	SSCG_STEP	SSCG_STEP
3 Center Spread	0x1A0	0x14D	0.5	0x2DD4	0x16EA
			1.0	0x5BA8	0x2DD4
			1.5	0x897C	0x44BE
			2.0	0xB750	0x5BA8
			2.5	0xE524	0x7292
			3.0	0x1 12F8	0x897C
2 Upspread **Not used with Ruby!**	0x1A0	0x14D	0.5	0x16EA	0x0B75
			1.0	0x2DD4	0x16EA
			1.5	0x44BE	0x225F
			2.0	0x5BA8	0x2DD4
			2.5	0x7292	0x3949
			3.0	0x897C	0x44BE
1 Downspread	0x1A0	0x14D	0.5	0x16EA	0x0B75
			1.0	0x2DD4	0x16EA
			1.5	0x44BE	0x225F
			2.0	0x5BA8	0x2DD4
			2.5	0x7292	0x3949
			3.0	0x897C	0x44BE

For a center spread type and a Modulation Peak of 2.0%, use the following settings:

SSCG_TYPE = 0x11
SSCG_PERIOD = 0x1A0
SSCG_PERIOD_DELTA = 0x14D
SSCG_STEP = 0xB750
Please take note of the limitations listed in the Hardware Manual.

5 Enabling the SSCG Unit

It is important to follow an specific scheme to enable the SSCG unit in order to avoid causing a spike on the clock signal of the effected clock domains.

1. Switch the internal clock domains to the non-SSCG modulated clock domain, reset the SSCG and switch the display clocks to the non-SSCG modulated clock domain:
   SSCG_CLKEN <0x3002_0004> = 0x00000000
2. Set the SSCG to Bypass mode and power down the SSCG:
   SSCG_CTRL <0x3002_0028> = 0x80000133
3. Power up the SSCG and set to Bypass mode:
   SSCG_CTRL <0x3002_0028> = 0x00000133
4. Configure the SSCG and wait for 1000 clock cycles before starting the SSCG
5. Disable the Bypass mode (enabling the SSCG unit):
   SSCG_CTRL <0x3002_0028> = 0x00010133
6. Release the SSCG reset (digital part) using global control and switch the internal clock domains to the SSCG modulated clock domain:
   SSCG_CLKEN <0x3002_0004> = 0x0000000C
7. Switch the display clock domains to the SSCG modulated clock domain:
   SSCG_CLKEN <0x3002_0004> = 0x0000000F
8. Enable the SSCG:
   SSCG_ENABLE <0x3002_002C> = 0x00000001
9. Wait for 1 millisecond
10. Reset the 'Frequency Limit' Interrupt:
    SSCG_IEN.IEn_Frequency_Limit <0x3002_001C> = 0x00000001
11. Check that SSCG_STATUS.STS_FREQUENCY_LIMIT = 0

Note:
The SSCG parameter configuration can be done in steps 4 .. 7; otherwise the SSCG will run with the default settings of <0x3002_0004> = the content of address 0x3002_0004.

A more detailled flow is described in the Hardware Manual.

6 Checking the SSCG Unit is Operating

You can check that the SSCG unit is operating by reading the SSCG_CNTOUTFREQ register. It will return a value that is not '0' if the SSCG is running.

7 Important Notes during operation

Note that not every receiver can handle a modulated output signal. If problems (screen artefacts etc.) are experienced with a display, try reducing the degree of modulation to attain a range that the receiver can accept.

Make sure that the SSCG configuration is a valid one (i.e. the constraints of the Hardware Manual are taken into consideration). Failure to do this – i.e. an illegal configuration - may generate a flood of interrupts from the SSCG unit.

Do not reconfigure the SSCG unit while it is being used!

8 Disabling the SSCG Unit

It is important to follow an specific scheme to disable the SSCG unit in order to avoid causing a spike on the clock signal of the effected clock domains. Use the following programming sequence: (example)

1. Disable the SSCG:
   SSCG_ENABLE <0x3002_002C> = 0x00000000
2. Set the SSCG to Bypass mode:
   SSCG_ENABLE <0x3002_0028> = 0x00000133
3. Switch the internal clock domains to the non-SSCG modulated clock domain:
   SSCG_CLKEN <0x3002_0004> = 0x00000007
4. Switch the display clock domains to the non-SSCG modulated clock domain:
   SSCG_CLKEN <0x3002_0004> = 0x00000004
5. Set the SSCG to Bypass mode and power down the SSCG:
   SSCG_CTRL <0x3002_0028> = 0x80000133
6. Reset the SSCG :
   SSCG_CLKEN <0x3002_0004> = 0x00000000

A more detailled flow is described in the Hardware Manual.