This guide is based on using the Allegro Free Physical Viewer to review an Allegro PCB layout file (.brd). Allegro Free Physical Viewer software can be downloaded from the Cadence Website.

Physical Viewer Checks

1. First examine the stack up of the PCB.

   Click the "Visibility" on (right) side bar to highlight layers. The focal point is on high speed differential signal traces. You can sample a couple of lanes (one lane = a pair of differential traces) to read their length skew. Click Display>Element, read the total etch length number; then read the complementary trace. The lengths difference should be no more than 5 mil (0.13mm) for add-in card and 10 mil (0.25mm) for system board[i]. Then check the length delta between lanes. Spec requires no more than 2 inches (50mm) and 7 inches (180mm) difference for PCIe add-in card and system board[ii]. In practice, every layout should be much better than this.

2. Next step is to confirm impedance control for the high speed traces.

   Impedance controlled traces have two types, Microstrip and Stripline. Microstrip is on top and bottom layers which are exposed to ambient. Microstrip traces have ground (optional power) layer coupled underneath through dielectric material. Make sure there is continuous ground plane along the route of traces. Traces running over broken reference planes should populate a 100nF capacitor within ¼ inch of reference planes discontinued place. Stripline traces are sandwiched between ground/power layers. The distance to upper and lower ground layers can be same (symmetric) or different (asymmetric). Likewise, all of the reference ground/power plane coupled with traces must have copper filled along traces. In other cases customers might use an asymmetric Stripline configuration (two Stripline layers adjacent to each other). In this case, traces should run perpendicular between layers to avoid cross-talk – note, not a preferred method of routing. As in most cases, customer should be responsible for SI simulations. Lastly, avoid 90 degree angle (trace bends?) when routing trace. All AC coupling capacitors should be placed symmetrically within their (P/N) paring and on the same side and same location along the traces. Signal caps should be placed near the TX output.

   Trace impedance can be calculated by Zcalc.exe (or other calculator found from Internet). All the needed parameters (except stack up thickness) can be read from Allegro Viewer. Click Display>Constrain; from the table you will get trace width and spacing info. In most case you'll also see Net Class which has name hints for the differential impedance (e.g. D85, 85OHM, D100, 100OHM etc.). If you see this info from Net Class, that means the impedance is taken care of -- simply verify if they are the correct impedance value. The trace width is usually no less than 5 mil (0.13mm). (Note, thinner traces result in more signal losses. Hence, longer routes are encouraged to use trace width in the range of 5-7mils). The spacing between is usually 1X to 2X

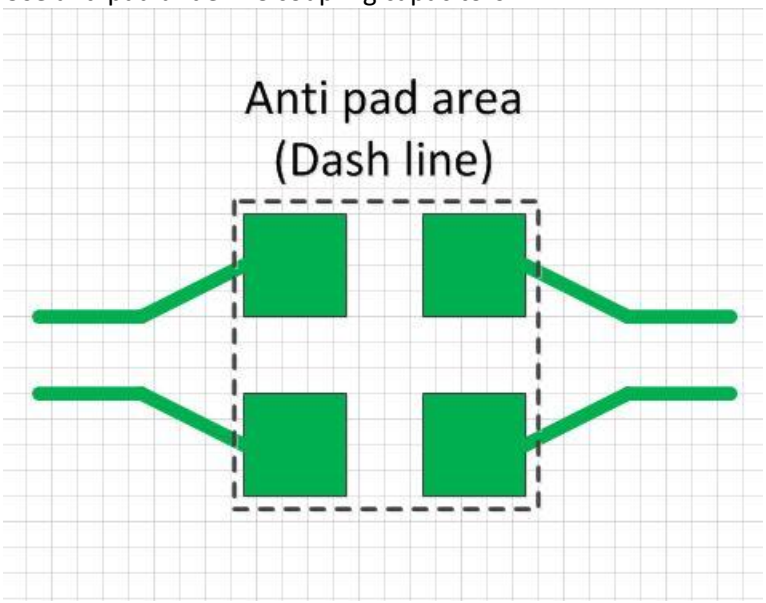
of trace width. The dielectric thickness is the parameter PCB fabrication and can adjust to match desired impedance. Most often, the layout designer leaves this final adjustment to the PCB manufacturer to ensure the proper impedance. The PCI Express specification specified the differential trace impedance should be within 68-105Ω. Since PCIe edge connector's character impedance is 85Ω, the traces between the connector and IC should be 85Ω -- the rest is usually set to 100Ω. Single ended traces impedance control is less important in review perspective.

3. Next step is to check the via count of each single trace. This can be read from Display>Element.

   The via count should be no more than three. There are some cases that Microstrip and Stripline are mixed in one signal pair. This should not be done. The different propagation delays of Microstrip and Stripline are hard to control and can introduce excessive skew and high frequency common mode noise. Lastly, the total propagation delay for PCIe add-in card is specified as no longer than 750pS[iii]. That roughly translated to 5.35 inches (135mm) and 4.26 inches (105mm) for Microstrip and Stripline, respectively. (This pertains to transport delay, but is typically not an issue)

Summary of trace review:

- Differential trace skew (one lane): < 5mil and 10 mil for PCIe add-in card and system board, respectively.
- Lane skew: <2000mil and 7000mil, PCIe add-in card and system board, respectively.
- Via count ≤3?
- AC coupling capacitors on TX? Placed on same side same spot?
- Use anti pad under AC coupling capacitors.



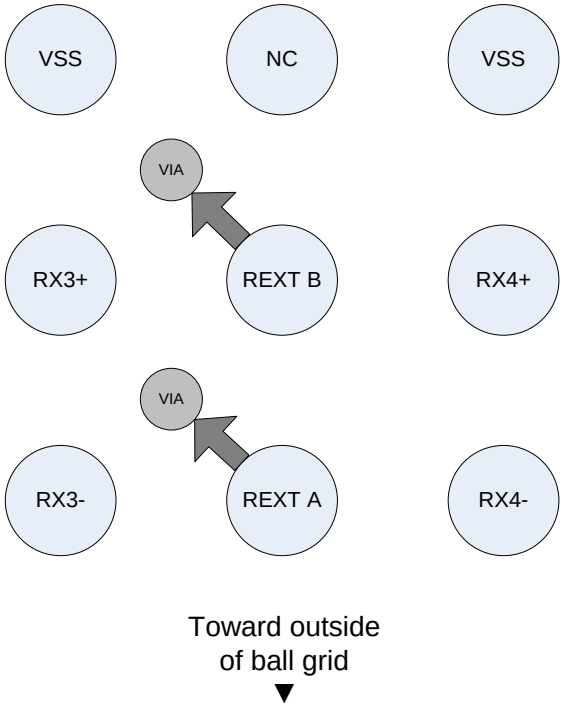
- Differential traces are Microstrip, Stripline or mixed?

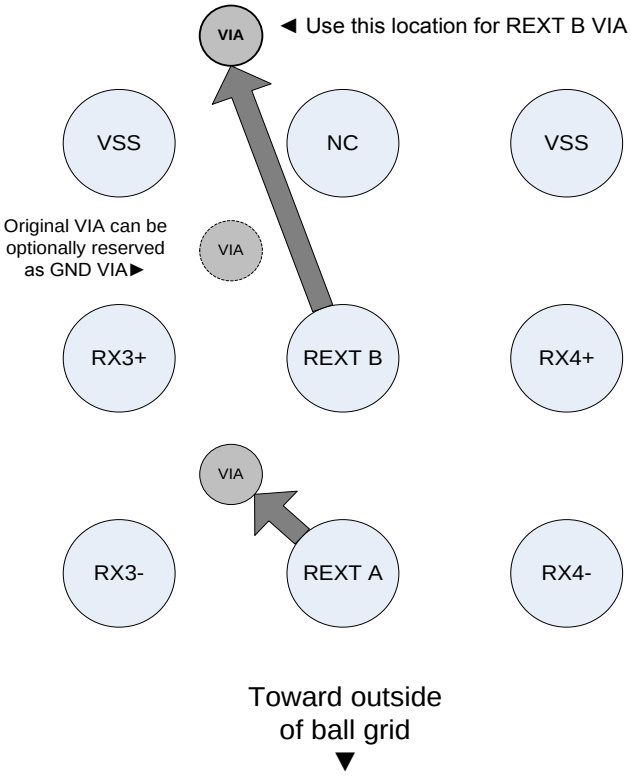
- If asymmetric Stripline, are the traces on different layers running in perpendicular?
- On PCIe add-in card: Are Microstrip and Stripline traces longer than 5.35 (135mm) and 4.26 inches (105mm), respectively?
- Any 90° angle trace routing?
- For PCIe add-in card, any layer under edge finger area should be removed. Including ground and power layers.

Component Placement

Major components should be placed such that routing of high-speed signal and clocks are as short as possible. Check that PLX IC decoupling capacitors are right in the ball grid of power and ground balls are on bottom layer. The stubs to/from capacitors should be short. Bulk capacitors are placed the surrounding area of the IC.

All the REXT resistors should be placed right next to the PLX IC. For PCIe Gen2 Switch, treat the traces connected to REXT as differential signal. i.e. the + and - trace running on the same layer and have the same width, minimum loop creation (note it is not necessary to make controlled impedance). No Test Points. Route them away from noise sources. Do not place different REXTs close to each other. For Gen2 devices, we recommend the placement of a small capacitor near the REXT(-) pin to ground, where possible. For Gen 2 devices whose REXT_A and REXT_B ball out matches the pattern as diagram below, there is a suggestion to REXT_B via. See the drawing below. Left one is what PCB layout engineers usually do to place the via's for REXT A and REXT B. Due to REXT B's sensitiveness to noise, PLX suggests to utilizing the empty space next to NC pad for REXT B via (As seen in right drawing). The original location for REXT B via can be optionally reserved as a GND via. This will limit potential noise injection into the switch bias circuit, if present.





Summary of placement review:

- Does placement minimize the routing of the high speed traces?
- Are the system clocks routed away from noise sources (such as switching supplies, single-ended logic signals, etc)
- Are REXT placement and trace routing OK?
- For Gen 2 devices whose REXT_A and REXT_B ball out matches the pattern as diagram above, did via's for REXT B follow PLX's suggestion?

Decoupling and Bulk Capacitance

Decoupling and bulk capacitors: Ideally we'd like to see at least one capacitor for each power ball. To fulfill this goal, customers might have to use 0201 footprint capacitor. In addition to placing caps under BGA, some caps can also be placed surrounding the IC. The lower decade caps should be placed closer to IC and so on. In some cases the cost of the board is first priority, a customer may reduce the quantity of capacitor to minimum. What minimum is has to be

verified by power simulation, and customers need advanced capability to do that (PLX does not have this capability).

Another way to create more decoupling capacitance is to utilize the power and ground layer closely coupled together. If this is not seen in the design, make recommendation.

Bulk capacitors are usually placed slightly farther (farther than highest decade decoupling caps) away from IC. Ideally you'd like to see them evenly distributed surrounding the IC.

Summary of decoupling and bulk capacitor placement review:

- The ideal design is to have as many decoupling caps as possible.
- The stubs of capacitors (one to power the other to ground) should be as short as possible.
- Are bulk capacitors evenly placed around the IC?
- Is power/ground layer buried capacitance utilized?

PCIe Add-in Connector considerations

If you're reviewing a PCIe add-in card, there is one more thing to review. The power and ground layer underneath the PCIe connector finger area should be removed[iv].

Footnotes:

[i] 4.6.6 in PCI Express CEM Rev 2.0.
[ii] Table 4-6, 4.6.5 in PCI Express CEM Rev 2.0.
[iii] 4.6.9 in PCI Express CEM Rev 2.0.
[iv] 5.3.2 in PCI Express CEM Rev 2.0.