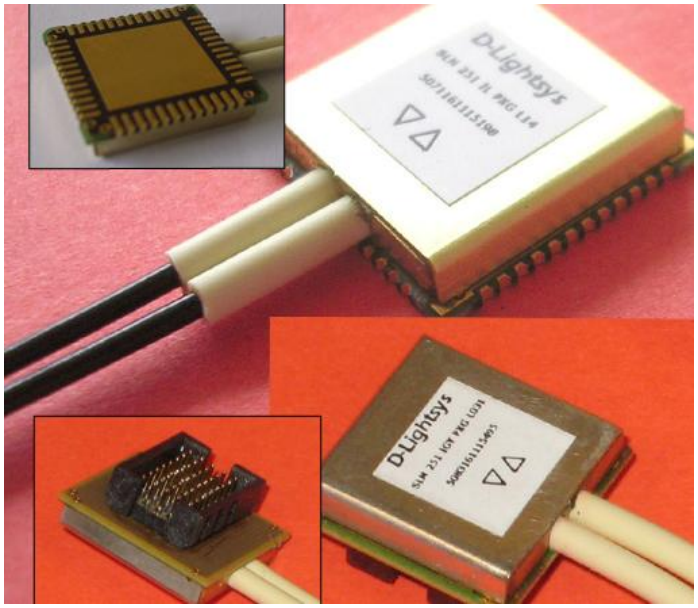
S-Light SLM-251-Ix-Pyz-Lvv
2.5 Gbps 850 nm optoelectronic Mil/Aero transceiver

Features

- Up to 4.25 Gbps
- Uses 850 nm VCSEL
- Complies with IEEE Std. 802.3z Gigabit Ethernet 1000 Base-Sx PMD and ARINC 804 requirements
- Controls and monitors compliant with SFF-8472 standard
- Qualified over the industrial temperature range [-40;+90°C] and functional over [-55:+125°C].
- Monitoring of the optical power over the temperature range
- Standard electrical SMT interface or solderless interface option
- Pigtailed optical connectics
- Low power consumpt° (<250 mW)



Applications

- Severe environment interconnects
- Sensors interconnects
- Numerical video transmission
- Board-to-board communications
- Datacommunications (LAN, SAN)
- On-board communications

Product Description

S-Light SLM-251-Ix-Pyz-Lvv optoelectronic modules are enhanced performances full duplex transceivers optimized for short distance high data rate optical communications. They are protocol independent and can be applied to Gigabit Ethernet, Fibre Channel, Infiniband or any specific communication application. The S-Light family is optimized for severe environment applications and complies with AEEC / ARINC 804 transceiver specifications.

SLM-251-Ix-Pyz-Lvv modules integrate state-of-the art 850-nm AlGaAs VCSEL and PIN photodiode chips and low power consumption CMOS electronics to comply with the SFF-8472 monitor and controls register map. SLM-251-IQ-Pyz optical interfaces consist of either 50/125 or 62.5/125 µm multimode optical cable pigtails terminated by the end-user specified optical terminus or connector. Both solderless and SMT package options are provided.

Ordering Information

Several versions of S-Light optoelectronic transceivers are currently available.

SLM- 251-Ix-Pyz-Lvv

- vv : Pigtail Length
  - Length in cm
- z : Optical cable
  - N ↔ Nexans 132574
  - G ↔ Gore CSG-13-824422-00
  - *Other cable options are available – contact sales*
- y : Pigtail termini
  - X ↔ 2 LuxCis Termini (ARINC801)
  - E ↔ 2 Elio Termini
  - T ↔ 2 ST connectors
  - L ↔ 2 LC connectors
  - *Other connectors are available (MC5, 29504…) – contact sales*
- x : Packaging option
  - L ↔ 48-Pin LCC package
  - GY ↔8x5 YFT-08-05-H-05-SB socket
  - *Other options upon request (QFN QFP…)*

D-Lightsys – 101 Rue Philibert Hoffmann – 93116 Rosny Sous Bois - Phone:+33(0)-149353953 - Fax:+33(0)-149353953

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Description

General

The SLM-251-Ix-Pyz-Lvv is an enhanced version of the SLM-250-Ix-Pyz-Lvv transceiver. This new version integrates SFF-8472 compliant control and monitor signals accessible through a 2-wire serial interface. The transmitter and the receiver parts of the transceiver are optimized for high speed DC-coupled serial links: the standard bit rate is 2.5Gbps (although the module operates up to 4.5 Gbps with decreased optical sensitivity). The module is 3.3 Volts single supplied for low power consumption.
The module mechanical dimensions 16.4×16.4×3.2 mm for the LCC package and 16.4x16.4x7.9mm for the socketed IGY one.

All the transmitter and receiver part of the module could be fully monitored and/or controlled through the 2-wire serial interface. Several features allow a large range of applications:

- Average and modulation currents of the VCSEL laser are both digitally programmable trough a 2-wire serial interface.
- A versatile input stage allows 100 Ω differential or 50 Ω to ground termination resistors to comply with CML or LVDS signaling levels.
- Analog outputs (RSSI, V_{avg} and V_{mod} control pins) permit the monitoring of the module state and performance.

Transmitter description

The transmitter side of S-Light modules is based on high speed 850nm AlGaAs Vertical Cavity Surface Emitting Lasers (VCSEL) and high performance BiCMOS laser driver. The transmitter is divided in three parts: The high speed circuit compatible with data rate running from DC to 4.25 Gbps ; the biasing and control circuit to control and monitor the laser and transmitter according to the application ; and the optical sub assembly, integrating all the optoelectronic and optical elements.

Receiver description

The receiver part of the S-Light module is based on high speed GaAs photodiode and high performances BiCMOS transimpedance (TIA) and limiting (LA) amplifiers. The signal path is AC-coupled and allows 2R (reshape and reclock) recovery.

Transceiver controls

The following input/output pins permit a complete monitoring of the transceiver:

- Serial interface (WP, SDA and SCL pins) : the 2-wire interface can be used to monitor in real-time the module status. It provides access to the following features: internal temperature, module operating modes, average input photocurrent, etc..
  Note that the 2-wire bidirectional bus interface is used during fabrication to program average and modulation currents to drive the VCSEL laser (for optimization of average power, extinction ratio, jitter…).
- DC/low-frequency Output RSSI : the DC / low-frequency output RSSI provides a voltage proportional to the average photocurrent generated by the photodiode.
- Received Signal Detect and/or Interrupt pin have been added to alert the user of a status change in the module operating mode.
- Alert signal: Alert is the VCSEL voltage supervisor output indicating whenever the VCSEL voltage drops below or exceeds in-fab predefined threshold voltages.
- TxEnable/Disable: The laser could be disabled or turned off through a dedicated pin or through the 2-wire serial interface.
- V_{avg} and V_{mod} outputs: these 2 pins deliver 2 voltages proportional to the average and modulation currents delivered to the VCSEL laser.

A Windows© PC-Based software is available for complete module monitoring and control. (Ref: SW-SLM/02 v1.0). Refer to the Application Note (Ref: AN-SLM/02) and to the Evaluation Board specifications (Ref: EVB-SLM/01) or contact sales for more information on programming and computing the feedback coefficients.

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Absolute Maximum Ratings

Stress beyond the values stated below may cause permanent damage to the device.

Parameter	Symbol	Min	Max	Unit	Notes
Storage temperature	T_{st}	-55	+125	°C	-
Soldering temperature	T_{sol}	-	230	°C	-
Soldering time	t_{sol}	-	60	s	-
Supply voltage	V_{CCTx}, V_{CCRx}	-0.3	+4.0	V	-
Signal pins voltage range	V_{pin}	V_{EEx}-0.3	V_{CCx}+0.3	V	-
Differential input voltage	ΔV_{in}	-	1.2	V	-
Junction temperature	T_j	-	130	°C	-
ESD resistance voltage	ESD	-	1	KV	-

Module specifications – General

VCC_x =3.3V, VEE=GND= 0V

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{CCTx}, V_{CCRx}	3.0	3.3	3.6	V	-
Supply voltage noise	N_{VCCx}	-	-	100	mV	-
Supply current (Tx + Rx)	I_{CC}	-	60	75	mA	1
Power consumption(Tx + Rx)	P	-	200	250	mW	1
Data rate	B	0.1	2.5	4.25	Gbps	-
Qualified operating temperature	T_{op}	-40	-	+90	°C	-
Functional operating temperature	T_{func}	-55	-	+125	°C	3

Notes:

1. Power consumption with Tx and Rx operating at full speed over the temperature range. Maximum power consumption occurs at 90°C.
2. Module operates within the functional operating temperature with decreased performances.

Module specifications – Electrical

B = 2.5Gbps, VCC_x =3.3V, VEE=GND= 0V, Temp = [-40;+90°C]

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Transmitter							
Input voltage range		V_{IN}	V_{EE}+ 0.825		V_{cc}+ 0.2	V	
Differential input voltage		V_{INpp}	100	-	950	mV	-
Input impedance		Z_{in}	80	100	120	Ω	-
Input capacitance (each input)		C_{in}	1.0	1.3	1.6	pF	-
Digital inputs	High	V_{high}	0.7xVcc	-	V_{CC} + 0.3	V	
	Low	V_{low}	V_{EE} - 0.3		0.3xVcc	V	
Tx supply current		I_{ccTx}	-	30	40	mA	-
Receiver							
Differential output voltage		V_{OUTdif}	200	400	700	mV	-
Output impedance		Z_{out}	80	100	120	Ω	-
Output CML drive current		I_o	-	12	-	mA	
Average proportional photocurrent output		I_{avg}	0	-	200	µA	1, 2, 3
Total jitter receiver		T_{JRx}	-	60	150	ps	-
Rise/Fall time		$\tau_{R\ Rx}$, $\tau_{F\ Rx}$	-	80	150	ps	4
Rx supply current		I_{ccRx}	-	30	35	mA	-

Notes:

1. DC / Low frequency output current proportional to the photocurrent generated by the photodiode.
2. Iavg is internally loaded with a 10kΩ resistor to provide RSSI voltage
3. RSSI voltage linearity is valid for RSSI<2V.
4. Measured at 20% / 80% levels.

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Module specifications - Optical

B = 2.5Gbps, VCCx=3.3V, VEE= 0V, Temp = [-40;+90°C]

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Emitter						
Center wavelength	λ_C	840	850	860	nm	-
Spectral width – rms	$\Delta\lambda$	-	-	0.85	nm	-
Core diameter of the Tx optical fiber pigtail	D_C	50	-	62.5	µm	-
Optical output power (average)	P_{out}	-4	-	-0.7	dBm	1,2,3
Optical output power variation over the specified temperature range	ΔP_{out}	-	-	1	dB	3, 4
Optical modulation amplitude	OMA_{Tx}	650	-	-	µW	-
Optical extinction ratio	E_R	7.5	9.0	-	dB	-
Relative Intensity Noise	RIN	-	-	-117	dB/Hz	-
Total jitter	T_{JTx}	-	60	150	ps	-
Rise/Fall time	τ_R, τ_F	-	80	150	ps	5
Receiver						
Center wavelength	λ_C	760	850	860	nm	-
Spectral width – rms	$\Delta\lambda$	-	-	1	nm	-
Core diameter of the Rx optical fiber pigtail	D_C	50	-	62.5	µm	-
Optical sensitivity	P_{in}	-23	-20	-17	dBm	6
Optical modulation amplitude	OMA_{Rx}	-	-	-	µW	-
Optical return loss	ORL	-30	-	-	dB	-

Notes:

1. SLM-251-Ix-Pyz transceivers are Class IM laser products according to IEC 60825-1 standard : average optical power is kept below –0.67dBm. A higher average optical power regulation is available upon request.
2. The output optical power is regulated over the temperature range. The optical power can be adjusted by the user through a 2-Wire serial interface.
3. Over specified operating temperature range (c.f. graph below).
4. The module is compliant with ARINC 804 long term temperature tests.
5. Measured at 20% / 80% levels.
6. For BER=10^{-12} measured at 2.5 Gbps with a 2^7-1 PRBS signal

Functional block diagrams

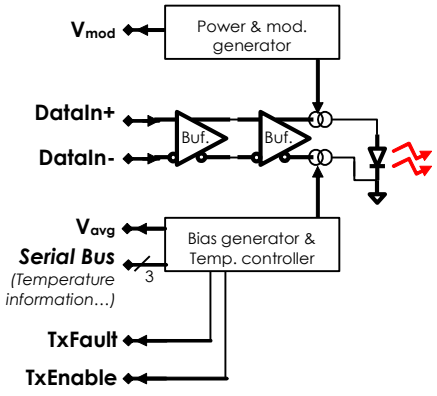

Figure 1 - Transmitter side (Tx)

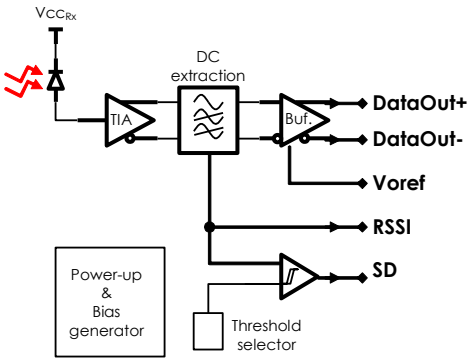

Figure 2 - Receiver side (Rx)

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Detailed description

General

The transmitter and the receiver parts of the transceiver are optimized for high speed DC-coupled serial links: the maximum bit rate is up to 4.25Gbits/s/ch. The module is 3.3 Volts single supplied for low power consumption.

Several features allow a large range of applications:

- Average and modulation currents are both digitally programmable trough a 2-wire serial interface (refer to the Control and Monitoring section and the Application Note AN-SLM/02).
- The transmitter could be disabled through the 2-wire interface as the TxEnable pin.
- Transmitter status is summarized through the dedicated pin TxFault as through the Alarm and Status register accessible via the 2-wire serial interface.
- A versatile input stage allows 100 Ω differential or 50 Ω to ground termination resistors to comply with CML or LVDS signaling levels.
- Analog outputs (I_{avg}, V_{avg} and V_{mod} control pins) permit the monitoring of the module state and performance.
- A digital Signal Detect pin (SD) indicates if the receiver status is ok or is the incident optical power is above the threshold.

The transceiver electronic is fabricated using state of the art AMS BYE 0.8µm SiGe BiCMOS technology.

Transmitter description

The transmitter side of S-Light modules is based on high speed 850nm AlGaAs Vertical Cavity Surface Emitting Lasers (VCSEL) and high performance BiCMOS laser driver. The transmitter is divided in three parts:

- The high speed circuit compatible with data rate running from DC to 4.25 Gbps,
- The biasing and control circuit to control and monitor the laser and transmitter according to the application,
- And the optical sub assembly, integrating all the opto-electronic and optical elements.

Power supply and biasing

The module is 3.3 Volts single power supply and includes internal decoupling components. Supply filtering is recommended, with roll-off frequency at 10 MHz or lower (see applications hints for details).

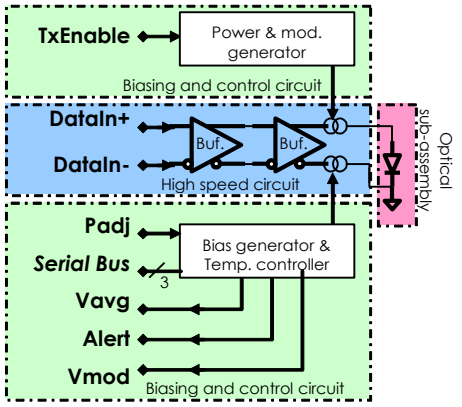

Figure 3 - Transmitter block diagram

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Data Input stage

The input stage is a versatile differential amplifier with large common-mode range compatible with various signaling levels such as CML, LVDS or ECL/PECL. This stage is internally biased and therefore suitable for AC-coupled operations and complies with standard IEEE 1596.3 "Reduced Range Link".

- Two on-chip termination resistors R_A of 50 Ω define the input impedance. Logical High (True) if *V*(DataIn+ > *V*(DataIn-).
- Handle up to 10mA of input current

For Differential CML : Internal bias (Vref) allows straight connection of the two incoming 50 Ω impedance lines to DataIn+ and DataIn-.
For Differential ECL 10k/100k/PECL: Separate load resistors are needed to draw bias current off the emitter follower outputs. And for LVDS: Internal bias unconnected providing 100 Ω differential input impedance.

Contact sales for input stage compliant mode (LVDS or CML) configurations.

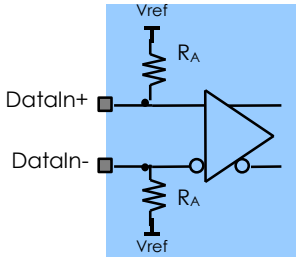

Figure 4 - Input stage

Driver stage

The current driver operates in inverted mode: it "steals" a current from the anode (p-side: Lp) of the laser. The complementary current is fed through an on-chip dummy diode to the common-n node, thus avoiding any net signal currents on the supply rails (Figure 5 -).

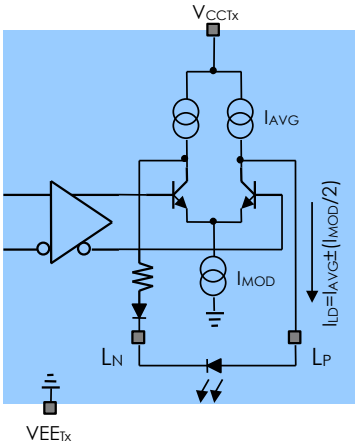

Figure 5 - Output stage

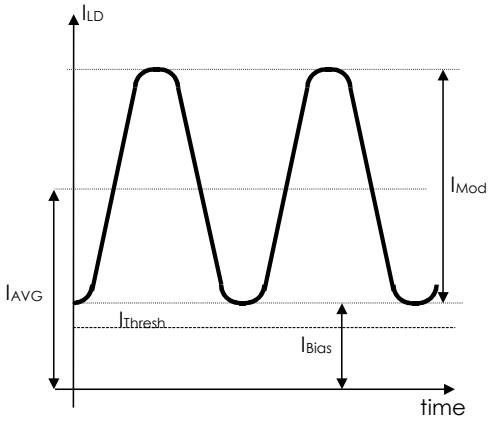

Figure 6 - Laser diode current

- In the logical High (True) state, the light is turned on : $I_H=I_{AVG}+I_{MOD}/2$
- In the logical Low (False) state, the light is turned off : $I_L=I_{AVG}-I_{MOD}/2$

The driver output stage is modeled by a current source and a capacitance C_{LP}. The VCSEL and its assembly are modeled by a bond-wire inductance L_L and a serie resistance r_s. An extrinsic capacitance C_{Ext}. See application notes for more information on the equivalent circuit.

Drive Current Control/Programming

Average and modulation current levels are preset by internal voltages V_{AVG} and V_{MOD} *(Figure 7 -)* according to the following equations:

$$I_{AVG} = V_{AVG} \cdot g_{AVG} \cdot N_{AVG}$$
$$I_{MOD} = V_{MOD} \cdot g_{MOD} \cdot M_{MOD}$$

These voltages are controlled/programmed using two digital potentiometers which can be addressed by means of a 2-wire serial interface (See the following section for further details on the 2-wire serial interface modes and operations). They can are accessible (and externally forced) by the user on the Vmod and Vavg pins. Therefore the previous equations are modified as follow:

$$V_{AVG} = R_{AVG} \cdot I_{SourceC} \Rightarrow I_{AVG} = R_{AVG} \cdot I_{SourceC} \cdot g_{AVG} \cdot N_{AVG}$$
$$V_{MOD} = R_{MOD} \cdot I_{SourceC} \Rightarrow I_{MOD} = R_{MOD} \cdot I_{SourceC} \cdot g_{MOD} \cdot M_{MOD}$$

$I_{sourceC}$, average and modulation gain and coefficient (g_x and N_x) are given in table 1.

Non-volatile Look-Up Table (LUT) with in-fabric programmed parameters are used to save and monitor the VCSEL current and voltage behavior over the functional temperature range. This specific design allows the optical power of the module as the extinction ration to remain respectively within 1dB and 2dB variation over the functional temperature range.

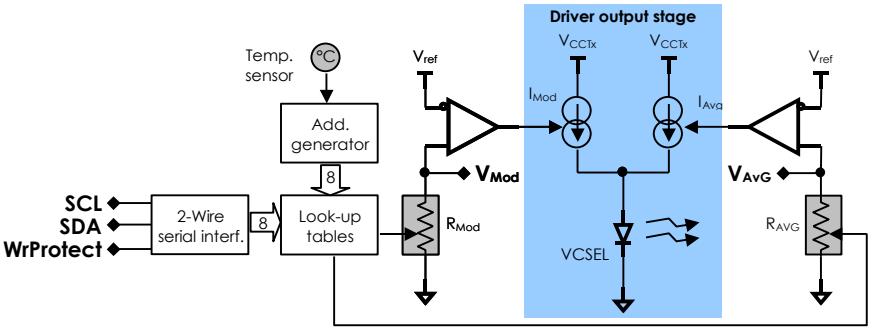

Figure 7 - Average and modulation current control circuit

The V_{MOD} and V_{AVG} voltages can be modified by the user to adapt the output optical power according to the applications requirements. The value of each variable resistor is determined by a temperature-addressed look-up table, which can assign a unique value (00h to FFh) to each resistor for every 2°C increment over the -40°C to +102°C range (-40°C correspond to LUT address 80h, and +102°C to address C7h, address increment corresponds to a 2°C step). See the *Temperature Conversion* section for more information. The variable resistors can also be used in manual mode. If the TEN bit equals 0 (refer to following paragraphs to TEN bit details), then the resistors are in manual mode and the temperature indexing is disabled. The user sets the resistors in manual mode by writing to addresses 82h and 83h in Table 01 to control resistors 0 and 1, respectively.

A Windows© PC-Based software is available for average and modulation current programming (Ref: SW-SLM/02 v1.0). Refer to the Application Note (Ref: AN-SLM/02) and the Evaluation Board specifications (Ref: EVB-SLM/01) or contact sales for more information on programming and computing the feedback coefficients.

Parameter	Symbol	Min.	Typ.	Max.
Average current transadmittance	g_{AVG}	0.8 mA/V	1.0 mA/V	1.25 mA/V
Modulation current transadmittance	g_{MOD}	0.8 mA/V	1.0 mA/V	1.25 mA/V
Transadmittance uniformity	σ_1	-	-	2%
N_{AVG} Factor	N_{AVG}	-	6	-
N_{MOD} Factor	N_{MOD}	-	4	-
Current preset	$I_{SourceC}$	80 µA	100 µA	120 µA
Thermal voltage slope	δV_{THERM}	-	9 mV/°C	-
Thermal voltage @ 50°C	V_{THERM}(50°C)	-	1.5V	-

Table 1 – Transceiver Internal gain and parameters for average and modulation programming

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Transmitter controls

The transmitter is provided with several input/output pins and/or dedicated registers accessible through the 2-wire serial interface, which permit a complete monitoring of the component:

- TxFault - *Pin 4 and bit 2 @ 6Eh in main device memory map (table 00h)*: provides a VCSEL voltage supervisor output indicating whenever the VCSEL voltage drops below or exceeds in-fab predefined threshold voltages. This active high supervisor signal is also accessible through the 2-wire serial interface. The VCSEL voltage and driver current supervisor detects both a high voltage level V_{VH}, and a low voltage level V_{VL}. These two signals are processed differently:
  - **V_{VH}** is only active when transmitter is powered-up. The threshold voltage is typically 2.3V. This signal does not power down the data channel.
  - **V_{VL}** is only active when transmitter is powered-up. The threshold voltage is typically 1.3V. The V_{VL} signal provides diagnostic information.
  - V_{VH} and V_{VL} signals are OR'ed to from the TxFault output signal.

- TxEnable - *Pin 3 and bit 1 @ 6Eh in table 00h*: the transmitter side of the SLM-251-xy-PzN module can be disabled by pulling high the TxEnable input pin or by setting the appropriate bit in the register map (see section below). Average and modulation currents are therefore set to 0mA and the VCSEL is shut-off. When TxEnable is low the data inputs modulate the output.

- Driver Temperature dependent voltage: 2 specific registers @ *60-61h in table 00h* indicates the module internal temperature on a 12 bit value (see next section for temperature computation).

- Average Optical Power - *Pin 5 and register 82h in table 01h*: The Pin 5 give a voltage proportional to the average optical power emitted by the VCSEL. The equivalent average laser current value is given by the previous equations with R_{AVG}= Decimal value x 50kΩ/256.

- Optical Modulation Amplitude - *Pin 8 and register 82h in table 01h*: The Pin 5 give a voltage proportional to the optical modulation amplitude of the laser. The equivalent OMA current value is given by the previous equations with R_{MOD}= Decimal value x 50kΩ/256.

- Transmitter power supply monitor – *Bit 0 @ 6Eh in table 00h*: this Status bit indicates if the transmitter power supply is ok or not.

Receiver description

The receiver part of the SLM-251-Ix-Pyz module is based on high speed GaAs photodiode and high performances BiCMOS transimpedance (TIA) and limiting (LA) amplifiers. Some input and output signals have been added to the design for complete controlling of the module (in particular a link monitor with a threshold selector has been added to comply with standard specifications SDH STM-16).

The signal path is AC-coupled and allows 2R (reshape and reclock) recovery. The minimum lower cut-off frequency is dependent on the pattern spreading but can be as low as 100KHz. This circuit is therefore compatible with data rates ranging from 100Mbps to 4.25 Gbps.

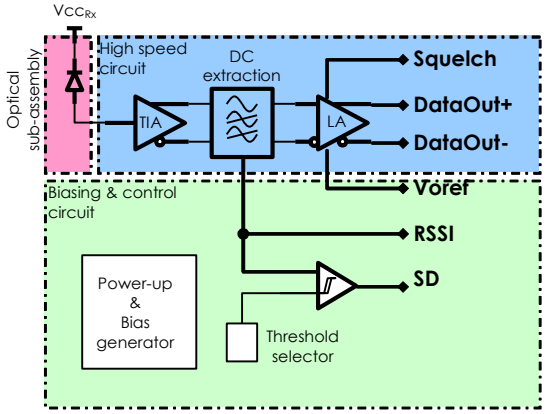

Figure 8 - Receiver bloc diagram

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Photodiode input stage

The photodiode input stage is a differential transimpedance amplifier with high sensitivity that operates with input current as low as 4 μA_{pp}. Typical photodiode sensitivity at 850nm is 0.6A/W : the optical sensitivity is therefore as low as –22dBm. The amplifier incorporates a compensation capacitor.

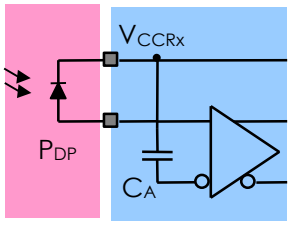

Figure 9 - Photodiode input stage

Data Output stage

The output stage is a differential current-mode-logic (CML) driver (Figure 10 -). The pull-up resistors are tied to a separated supply pin V_{OREF} which, according to the applied voltage, allows the stage to be compatible with LVDS level. The general characteristics of the output stage are the following (See application note for usage):

- Switched current I_0 of 9mA,
- pull-ups R_{OL} 2x100Ω to V_{OREF}.
- Free choice of V_{OREF} and 50Ω load resistor connection, as long as operating conditions are fulfilled.
- Only a small amount of noise is generated on V_{OREF} and V_{EERx}.

For differential DC-coupled termination with negative power supply (V_{CCRx} and V_{OREF} should be connected to ground and V_{EERx} to the negative supply): The outputs are then connected to 50Ω tracks, terminated by two 50Ω loads to ground, or a floating 100Ω load.
For single-ended AC-coupled : both outputs should see equal load impedances.
For LVDS-level compatibility : V_{OREF} should be tied to VEE_{Rx}+2.4V. The resulting levels are then compatible with an IEEE P1596.3 LVDS input stage.

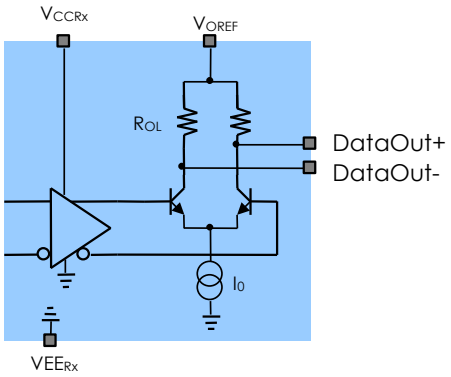

Figure 10 - Data output stage

Receiver controls

The receiver is provided with several input/output pins and/or dedicated registers accessible through the 2-wire serial interface, which permit a complete monitoring of the component:

- RSSI (Receiver Signal Strength Indicator) - *Pin 24 and register 64-65h in table 00h*: the DC/low-frequency output I_{AVG} sources a current proportional to the average input photocurrent. The Iavg source is internally loaded by a 10KΩ resistor. This resistor could be over driven by an external one attached to the RSSI pin and GND. The resulting voltage at the RSSI output pin should be kept below 2.0 V to maintain linearity. This output can be used to monitor the optical power incident on the photodiode. It may be left open if not used. The upper corner frequency of the output RSSI is equal to the roll-on frequency f_{Low} of the high-speed data path (Figure 11 - & Receiver characteristics table).
- Signal Detect (SD) – *Pin 30 and bit 2 @ 70h in table 00h*: this Status bit indicates if the receiver optical power is below threshold or not. If this status bit is asserted is the RSSI value is below a predefined threshold one.
- Receiver Saturation – *Bit 3 @ 70h in table 00h*: this Status bit indicates if the receiver optical power is above the receiver saturation.
- Receiver power supply monitor – *Bit 1 @ 70h in table 00h*: this Status bit indicates if the receiver power supply is ok or not.

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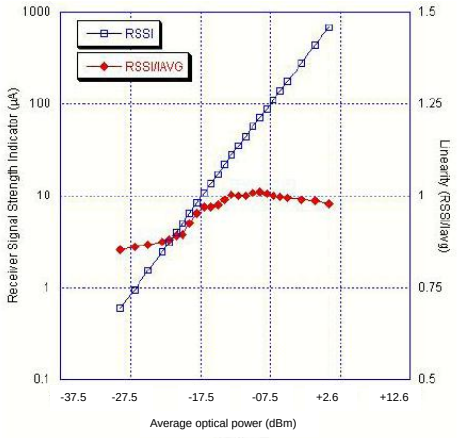

Figure 11 - Average monitor current and RSSI voltage

Receiver incident optical power computations

The voltage at RSSI output pin (in µV) is proportional to the input optical power of the receiver thought the following equation:

$$RSSI = \frac{1}{k} \cdot \frac{R_{ext} \times 10000}{R_{ext} + 10000} \cdot P_{opt} \text{ (µV)} \rightarrow Popt = k \cdot RSSI. \frac{R_{ext} + 10000}{R_{ext} \times 10000} \text{ (µW)}$$

Where R_{ext} is the resistor attached to RSSI pin, k an internal coefficient and P_{opt} the incident receiver optical power in µW. Note that linearity is maintained for RSSI ≤ 2.0V. RSSI accuracy is depending to the accuracy value of the internal k coefficient.

	Symbol	Min.	Typ.	Max.
Internal coefficient for RSSI	k	-20%	2	+20%

Power supply noise rejection

Even though bypass capacitors are integrated inside the module, additional filtering can reduce the noise penalty above 10 MHz. For a supply noise V_{PSN} = 100 mV_{PP} a 0.5 dB sensitivity penalty can be reached over the whole frequency range by using a first order low-pass filter with f_c = 10 MHz on the power supply (See application note for additional information).

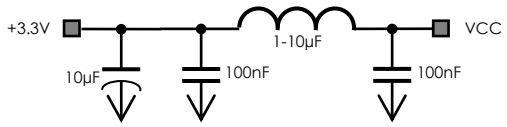

Figure 12 - Typical power supply filtering

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Control and Monitors Signals memory mapping

The following driver and receiver control or monitor signals are accessible by the 2-wire interface:

Control	Table	Address	Description
SD/LOSS	00h	6Eh bit 2	**Receiver Loss Of Signal/interupt indicator** : This status bit indicates if the module status according to MINT bit. It could be use as Signal Detect or Loss Of Signal indicator
TxDisable	00h	6Eh bit 1	**Transmitter Disable indicator** : This status bit indicates if the transmitter has been disabled externally or internally (refer to text and module datasheet for polarity and asserting)
TxVCC	00h	6Eh bit 0	**Transmitter power supply monitor bit**: this status bit indicates if the transmitter power supply is ok or not.
TxAvg	01h	82h	**Transmitter Average Resistor value**: Value(dec) x 50kΩ/256
TxMod	01h	83h	**Transmitter Modulation Resistor value**: Value(dec) x 50kΩ/256
Temp	00h	60-61h	**Module temperature**: 12 bit temperature value.
TempHi	00h	70h bit 7	**Module temperature upper limit:** Indicates if the current temperature is higher than 90°C.
TempLow	00h	70h bit 6	**Module temperature lower limit:** Indicates if the current temperature is below than -40°C.
RxRSSI	00h	64-65h	**Receiver Signal Strength Indicator:** This 12 bit value indicates the receiver incident average optical power. (Refer to datasheet)
TxFault	00h	64-65h	**Transmitter Fault indicator:** This 12 bit value indicates the transmitter TxFault pin voltage. (See text and refer to datasheet)
RxLOS	00h	70h bit 2	**Receiver Loss Of Signal:** this status bit indicates if the receiver incident optical power is sufficient for normal operations (@ BER)
RxSAT	00h	70h bit 3	**Receiver Saturation**: this status bit indicates if the receiver incident optical power is higher than the saturation point.
RxVCC	00h	70h bit 1	**Receiver power supply monitor bit** : this status bit indicates if the receiver power supply is below 2.5V.

Several other status and control bits are accessible to user. Refer to the application note AN-SLM/02 for a detailed memory mapping and following paragraphs for details operations.

Calculating Signal values

Each monitored signal (TxVCC, RSSI, RxVCC, TxFault and temperature) is available as a 16-bit value with 12-bit accuracy (left-justified) over the serial bus. Format is unsigned for all signals expect temperature. **The four LSBs should be masked when calculating the value**. The signals are updated every frame rate (t_{frame}) in a round-robin fashion. The comparison of all five signals with the high and low user-defined values is done automatically. The corresponding flags are set to 1 within a specified time of the occurrence of an out-of-limit condition.

The LSB = 100µV for TxVCC, 76.294µV for RxVCC and the LSB = 38.147µV for the other signals except temperature.

Monitor/TxVCC bit weights

MSB	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}
LSB	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

To calculate the value of VCC, convert the unsigned 16-bit value to decimal and multiply by **100µV for TxVCC** value and by **76.294µV for the RxVCC**. To calculate the value of RSSI, or TxFault convert the unsigned 16-bit value to decimal and multiply by 38.147µV (maximum value is 2.5V). *Note that TxFault is an open drain output. The user should program the threshold voltage according to the voltage drop in the load.*

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Monitor conversion examples

MSB (BIN)	LSB (BIN)	Voltage (V)
11000000	00000000	1.875
10000000	10000000	1.255

TxVCC conversion examples

MSB (BIN)	LSB (BIN)	Voltage (V)
10000000	10000000	3.29
11000000	11111000	4.94

Temperature Conversion and Look-up Table corresponding address

To calculate the value of the temperature, treat the two's complement value binary number as an unsigned binary number, then convert to decimal and divide by 256. If the result is greater than or equal to 128, then subtract 256 from the result.

Temperature bit weights

S	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}

Temperature:
High byte: -128°C to +127°C signed;
Low byte: 1/256°C.

Temperature conversion examples

MSB (BIN)	LSB (BIN)	Temperature (°C)
01000000	00000000	64
01000000	00001111	64.059
01011111	00000000	95
11110110	00000000	-10

LUT Address for corresponding Temperature values

Temperature	Corresp. Address
<-40°C	80h
-40°C	80h
-38°C	81h
-36°C	82h
-34°C	83h
—	—
-98°C	C5h
+100°C	C6h
+102°C	C7h
>+102°C	C7h

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Internal register map and description

The digital potentiometer is divided in two main parts: The main memory and the auxiliary memory. The main memory is dedicated to the control and monitoring the Transmitter and/or Receiver part of the D-Lightsys modules. The auxiliary memory is dedicated to the user; 128 bytes could be used to as Non-volatile independent memory.

Memory description

Main and auxiliary memories can be accessed by two separate device addresses. The Main Device address is A2h (or value in Table 01 byte 8Ch, when ADFIX = 1) and the Auxiliary Device address is A0h. A user option is provided to respond to one or two device addresses. This feature can be used to save component count in SFF applications (Main Device address can be used) or other applications where both GBIC (Auxiliary Device address can be used) and monitoring functions are implemented and two device addresses are needed.
The memory blocks are enabled with the corresponding device address. Memory space from 80h and up is accessible only through the Main Device address. This memory is organized as three tables; the desired table can be selected by the contents of memory location 7Fh in the Main Device. The Auxiliary Device address has no access to the tables, but the Auxiliary Device address can be mapped into the Main Device's memory space as a fourth table. Device addresses are programmable with two control bits in EEPROM:

- ADEN configures memory access to respond to different device addresses (see Tables 4 and 5). The default device address for EEPROM-generated addresses is A2h. If the ADEN bit is 1, additional 128 bytes of EEPROM are accessible through the Main Device, selected as Table 00h (see Figure 3). In this configuration, the Auxiliary Device is not accessible. APEN controls the protection of Table 00h regardless of the setting of ADEN.
- ADFIX (address fixed) determines whether the Main Device address is determined by an EEPROM byte (Table 01h, byte 8Ch, when ADFIX =1). There can be up to 128 devices sharing a common 2-wire bus, with each device having its own unique device address.

Memory Protection

Memory access from either device address can be either read/write or read only. Write protection is accomplished by a combination of control bits in EEPROM (APEN and MPEN in configuration register 89h) and a write-protect enable (WPEN) pin. The WPEN pin is not accessible from outside the module, in order to prevent accidental writes in the LUT by the end user.

Separate write protection is provided for the Auxiliary and Main Device address through distinct bits APEN and MPEN. APEN and MPEN are bits from configuration register 89h, Table 01h. Due to the location, the APEN and MPEN bits can only be written through the Main Device address. The control of write privileges through the Auxiliary Device address is dependent on the value of APEN.

Main Device address space 60h to 7Fh is SRAM and is not write protected by APEN, MPEN, or WPEN. For example, the user may reset flags set by the device. Bytes designated as "Reserved" may be used as scratchpad, but they will not be stored in a power cycle because of their volatility. These bytes are reserved for added functionality in future versions of this device. Note that in single device mode (ADEN bit = 1), APEN determines the protection level of Table 00, independent of WPEN. The write-protect operation, for both Main and Auxiliary Devices, is summarized in the following tables.

Main Device write protection mode

WPEN	MPEN	PROTECT MAIN
0	X	No
X	0	No
1	1	Yes

Auxiliary Device write protection mode

APEN	WPEN	PROTECT AUXILIARY
0	X	No
1	X	Yes

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Register Map

A description of the registers is below. The registers are read only (R) or read/write (R/W). The R/W registers are writable only if write protect has not been asserted (see the *Memory Description* section).

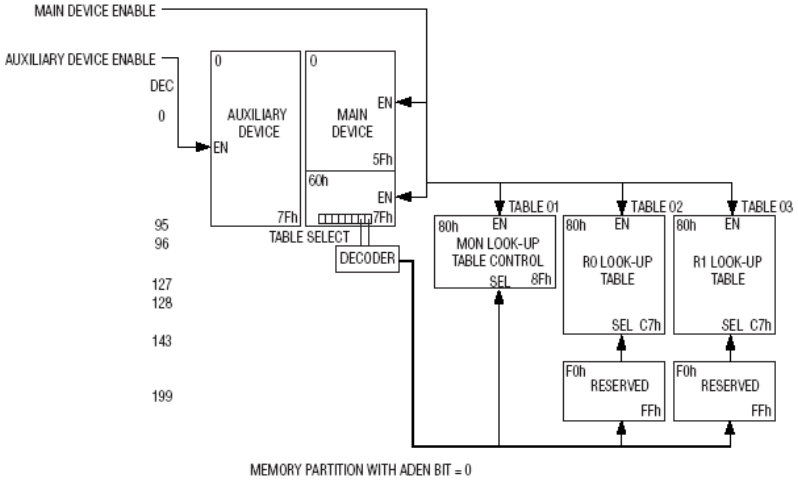

Figure 13 - Memory organization for ADEN bit set to 0

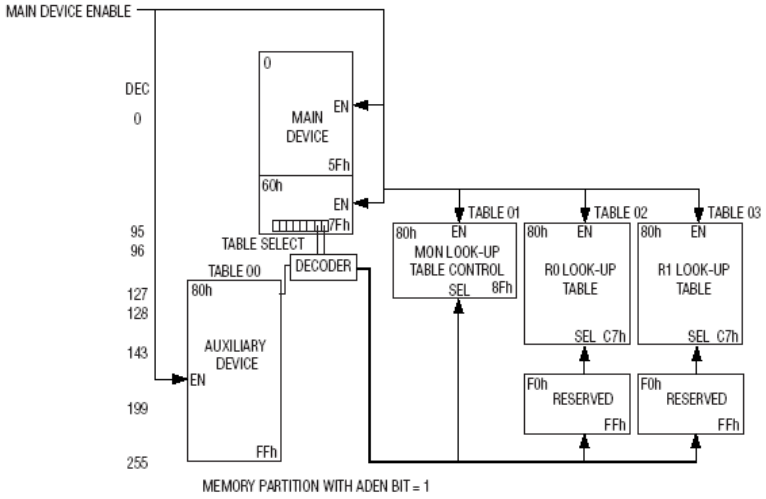

Figure 14 - Memory organization for ADEN bit set to 1

Auxiliary Device

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
00 to 7F	EEPROM	R/W	00	Standards Data	—

Main Device

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
01 to 5F	EEPROM	R	00	Reserved	Memory location reserved for D-Lightsys Hi and Low setup limits and Threshold for controlled parameters

Note: *SRAM defaults are power-on defaults. EEPROM defaults are factory defaults.*

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Main Device (Continued)

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
60 to 61	SRAM	R	—	Measured Temp (MSB to LSB)	Digitized measured value for temperature. See text.
62 to 63	SRAM	R	—	Measured TxVCC (MSB to LSB)	Digitized measured value for Transmitter VCC. See text.
64 to 65	SRAM	R	—	Measured RxRSSI (MSB to LSB)	Digitized measured value for the Receiver Signal Strength Indicator. See text.
66 to 67	SRAM	R	—	Measured RxVCC (MSB to LSB)	Digitized measured value for Receiver VCC. See text.
68 to 69	SRAM	R	—	Measured TxFault (MSB to LSB)	Digitized measured value for TxFault pin voltage. See text.
6A to 6D	SRAM	R	—	Reserved	—
6E	**SRAM**	**—**	**—**	**Status Register**	**—**
Bit 7	—	R	X	HIZSTA	Resistor status bit. A high indicates that both resistors are in high-impedance mode. A low indicates that both resistors are operating normally.
6	—	R/W	0	HIZCO	Resistor control bit. Setting this bit high causes both resistors to go into a high-impedance state.
5	—	—	X	X	—
4	—	—	X	X	—
2	—	R	X	SD	This status bit is high when SD bit is high: SD = MINT + POLARITY.
3	—	—	X	X	—
1	—	R	X	TxDisable	This status bit is high when TxDisable bit is high.
0	—	R	X	RDYB	This status bit goes high when TxVCC has fallen below the POA level.
6F	**SRAM**	**—**	**—**	**Conversion updates**	**—**
Bit 7	—	R/W	0	TAU	This bit goes high after a temperature and address update has occurred for the corresponding measurement in bytes 60h to 61h.
6	—	R/W	0	TxVCCU	Goes high after a VCC update has occurred for the corresponding measurement in bytes 62h to 63h.
5	—	R/W	0	RxRSSIU	Goes high after a RxRSSI update has occurred for the corresponding measurement in bytes 64h to 65h.
4	—	R/W	0	RxVCC2U	Goes high after a RxVCC update has occurred for the corresponding measurement in bytes 66h to 67h.
4	—	R/W	0	TxFaultU	Goes high after a TxFault update has occurred for the corresponding measurement in bytes 68h to 69h.
3	—	—	0	X	—
2	—	—	0	0	—
1	—	—	0	X	—
0	—	—	0	X	—

Note: The conversion update bits can be written to a 0 by the user and monitored to verify that a conversion has occurred.

Main Device (Continued)

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
70	**SRAM**	**R**		**Alarm flags #1**	**—**
Bit 7	—	—	—	Temphi	This alarm flag goes high when the upper limit of the temperature setting is violated. TempHi= 90°C
6	—	—	—	Templo	This alarm flag goes high when the lower limit of the temperature setting is violated. TempHi= -40°C
5	—	—	—	TxVCChi	This alarm flag goes high when the upper limit of the TxVCC setting is violated i.e. TxVCC>3.6.
4	—	—	—	TxVCClo	This alarm flag goes high when the lower limit of the TxVCC setting is violated i.e. TxVCC<3.0
3	—	—	—	RxSAT	This alarm flag goes high when the upper limit of the RSSI setting is violated. Corresponding to the Receiver saturation
2	—	—	—	RxLOS	This alarm flag goes high when the lower limit of the RSSI setting is violated i.e. Used MINT bit to configure the SD pin as a Loss Of Signal indicator (LOS).
1	—	—	—	RxVCChi	Goes high when the upper limit of the RxVCC setting is violated.
0	—	—	—	RxVCClo	Goes high when the lower limit of the RxVCC setting is violated.
71	**SRAM**	**R**	**—**	**Alarm flags #2**	**—**
Bit 7	—	—	—	TxFaulthi	Goes high when the upper limit of the TxFault setting is violated.
6	—	—	—	TxFaultlo	Goes high when the lower limit of the TxFault setting is violated.
5	—	—	—	X	—
4	—	—	—	X	—
3	—	—	—	X	—
2	—	—	—	X	—
1	—	—	—	X	—
0	—	—	—	MINT	A mask of all flags located in Table 01 byte 88h determines the value of MINT. MINT is maskable to 0 if no interrupt is desired by setting Table 01 byte 88h to 0.
72 to 7E	SRAM	R	00	Reserved	—
7F	SRAM	R/W	—	Table select	—
Bit 7	—	—	0	X	—
6	—	—	0	X	—
5	—	—	0	X	—
4	—	—	0	X	—
3	—	—	0	X	—
2	—	—	0	X	—
1	—	—	0	Table select bits	Set bits = 00 to select Table 00, Set bits = 01 to select Table 01, Set bits = 10 to select Table 02, Set bits = 11 to select Table 03.
0	—	—	0		

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Table 01h

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
80	**SRAM**	**R/W**		**Mode**	**—**
Bit 7	—	—	0	X	—
6	—	—	0	X	—
5	—	—	0	X	—
4	—	—	0	X	—
3	—	—	0	X	—
2	—	—	0	X	—
1	—	—	1	TEN	If TEN = 0, the temperature conversions update and the resistors can be controlled manually. The user sets the resistor in manual mode by writing to addresses 82h and 83h in Table 01 to control resistors 0 and 1, respectively.
0	—	—	1	AEN	AEN = 0 provides manual control of the temperature index.
81	SRAM	R	—	Temp index	This byte is the temperature-calculated index used to select the address of resistor settings in the look-up tables.
82	SRAM	R/W	00	Bias Resistor	Bias Resistor 0 position values.
83	SRAM	R/W	00	Modulation Resistor	Modulation Resistor 1 position values
84 to 87	SRAM	—	00	Reserved	—
88	**EEPROM**	**R/W**		**Interrupt enable**	
Bit 7	—	—	1	TMP	This byte configures a maskable interrupt, determining which event asserts a buffer 1 output (MINT set to 1, see register 89h in Table 01). If any combination of temperature, TxVCC, LOS/SD or RxVCC is desired to generate an interrupt (SD Pin), the corresponding bits are set to 1. To ignore interrupt set all bits to 0.
6	—	—	1	TxVCC	
5	—	—	1	RSSI	
4	—	—	1	RxVCC	
3	—	—	1	X	
2	—	—	0	X	
1	—	—	0	X	
0	—	—	0	X	
89	**EEPROM**	**R/W**		**Configuration**	**—**
Bit 7	—	—	0	X	—
6	—	—	0	X	
5	—	—	0	ADEN	Controls if the device responds to one or two device addresses (see the *Memory Description* section).
4	—	—	0	ADFIX	Controls the means by which Main and Auxiliary Device addresses are set (see the *Memory Description* section).
3	—	—	0	APEN	Controls auxiliary write protect. See the *Memory Description* section.
2	—	—	0	MPEN	Controls main write protect. See the *Memory Description* section.
1	—	—	0	POLARITY	Configures Polarity for SD pin: SD = MINT + POLARITY. (SD=LOS)
0	—	—	0	TxDisable	Transmitter Enable/Disable bit: If set to "one" the Transmitter is disabled.

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Table 01h (continued)

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
8A to 8B	EEPROM	—	00	Reserved	
8C	EEPROM	R/W	A2	Device address	Contains Main Device address if the bit ADFIX = 1. If ADFIX = 0, then address A2h is used.
8D to 8F	EEPROM	—	—	Reserved	—

Table 02h

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
80 to C7	EEPROM	R/W	FF	Bias Resistor Temperature LUT	Look-up table for Bias Resistor.
F0 to FF	EEPROM	R	FF	Reserved	—

Table 03h

Memory Location (hex)	EEPROM/SRAM	R/W	Default Setting (hex)	Name of Location	Function
80 to C7	EEPROM	R/W	FF	Modulation Resistor Temperature LUT	Look-up table for Modulation Resistor.
F0 to FF	EEPROM	R	FF	Reserved	—

Temperature conversion

The direct-to-digital temperature sensor measures temperature through the use of an on-chip temperature measurement technique with an operating range from -40°C to +102°C. Temperature conversions are initiated upon power-up, and the most recent conversion is stored in memory locations 60h and 61h of the Main Device, which are updated every t_{frame}. Temperature conversions do not occur during an active read or write to memory.

The value of each resistor is determined by the temperature-addressed look-up table. The look-up table assigns a unique value to each resistor for every 2°C increment with a 1°C hysteresis at a temperature transition over the operating temperature range.

Power-up and Low-Voltage operation

During power-up, the device is inactive until TxVCC exceeds the digital power-on-reset voltage (POD). At this voltage, the digital circuitry, which includes the 2-wire interface, becomes functional. However, EEPROM backed registers/settings cannot be internally read (recalled into shadow SRAM) until TxVCC exceeds the analog power-on-reset voltage (POA) at which time the remainder of the device becomes fully functional. Once TxVCC exceeds POA, the RDYB bit in byte 6Eh of the Main Device memory is timed to go from a 1 to a 0 and indicates when analog to digital conversions begin. If TxVCC ever dips below POA, the RDYB bit will read as a 1 again. Once a device exceeds POA and the EEPROM is recalled, the values remain active (recalled) until VCC falls below POD.

For 2-wire device addresses sourced from EEPROM (ADFIX = 1), the device address defaults to A2h until TxVCC exceeds POA and the EEPROM values are recalled. The Auxiliary Device (A0h) is always available within this voltage window (between POD and the EEPROM recall) regardless of the programmed state of ADEN. Furthermore, as the device powers-up, the TxVCCIo alarm flag (bit 4 of 70h in Main Device) will default to a 1 until the first TxVCC analog-to-digital conversion occurs and sets or clears the flag accordingly.

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2-Wire data transfer operation — Refer to AN-SLM/02

Description

The 2-wire serial port interface supports a bi-directional data transmission protocol with device addressing. This 2-wire interface is an **I²C compliant serial port.**

A device that sends data on the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a "master." The devices that are controlled by the master are "slaves." The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The S-Light or D-Light modules operate as slaves on the 2-wire bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL (4.7KΩ pull-up resistors should be added externally to the chip).

Clock and Data Transitions:

The SDA pin is normally pulled high with an external resistor or device. Data on the SDA pin may only change during SCL-low time periods. Data changes during SCL-high periods will indicate a start or stop condition depending on the conditions discussed below. See the timing diagrams in Figures 4 and 5 for further details.

Refer to AN-SLM/02 for detailed operation on the 2-wire serial interface.

2-Wire data transfer protocol and chronograms

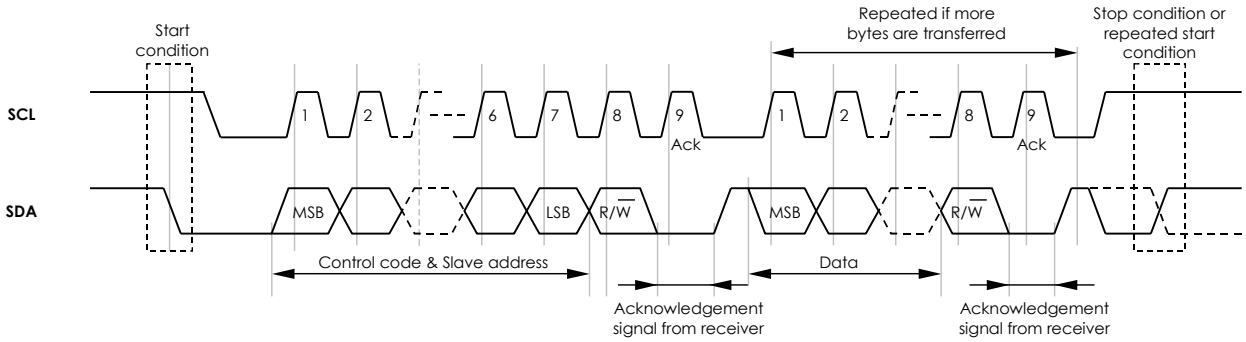

Figure 15 - 2-wire data transfer chronograms

2-Wire AC Characteristics and timing

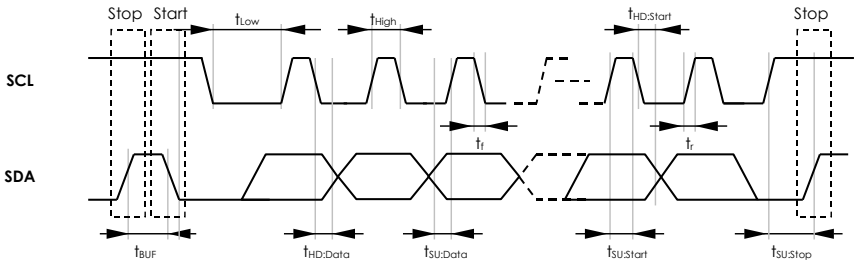

Figure 16 - 2-wire data transfer chronograms

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Timing table (-40°C to +90°C, V_{CC} = 3.3V)

Parameter	Symbol	Condition	Min.	Max.	Unit	Note
Serial clock frequency	F_{SCL}	Fast mode	0	400	kHz	1
		Standard mode	0	100		
Bus free time between STOP and START	t_{BUF}	Fast mode	1.3		µs	1
		Standard mode	4.7			
Hold time for START condition	$t_{HD:Start}$	Fast mode	0.6		µs	1,2
		Standard mode	4.0			
Low period of SCL clock	t_{Low}	Fast mode	1.3		µs	1
		Standard mode	4.7			
High period of SCL clock	t_{High}	Fast mode	0.6		µs	1
		Standard mode	4.0			
Data set-up time	$t_{SU:Data}$	Fast mode	0	0.9	µs	1
		Standard mode	0	0.9		
Data hold time	$t_{HD:Data}$	Fast mode	0	0.9	µs	1,3,4
		Standard mode	0	0.9		
Set-up time for STOP and START conditions	$t_{SU:Stop}$	Fast mode	0.6		µs	1
		Standard mode	4.0			
Rise time	t_r	Fast mode	80	300	ns	
		Standard mode	100	1000		
Fall time	t_f	Fast mode	80	300	ns	
		Standard mode	100	1000		
EEPROM write time	t_w	-	5	20	ms	5

Notes:

1. A fast mode device can be used in a standard mode system, but the requirement $t_{SU:DAT}$ > 250ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{RMAX} + $t_{SU:DAT}$ = 1000ns + 250ns = 1250ns before the SCL line is released.
2. After this period, the first clock pulse is generated.
3. The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.
5. EEPROM write begins after a STOP condition occurs.

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Typical Tx optical power and Rx sensitivity variations over temperature

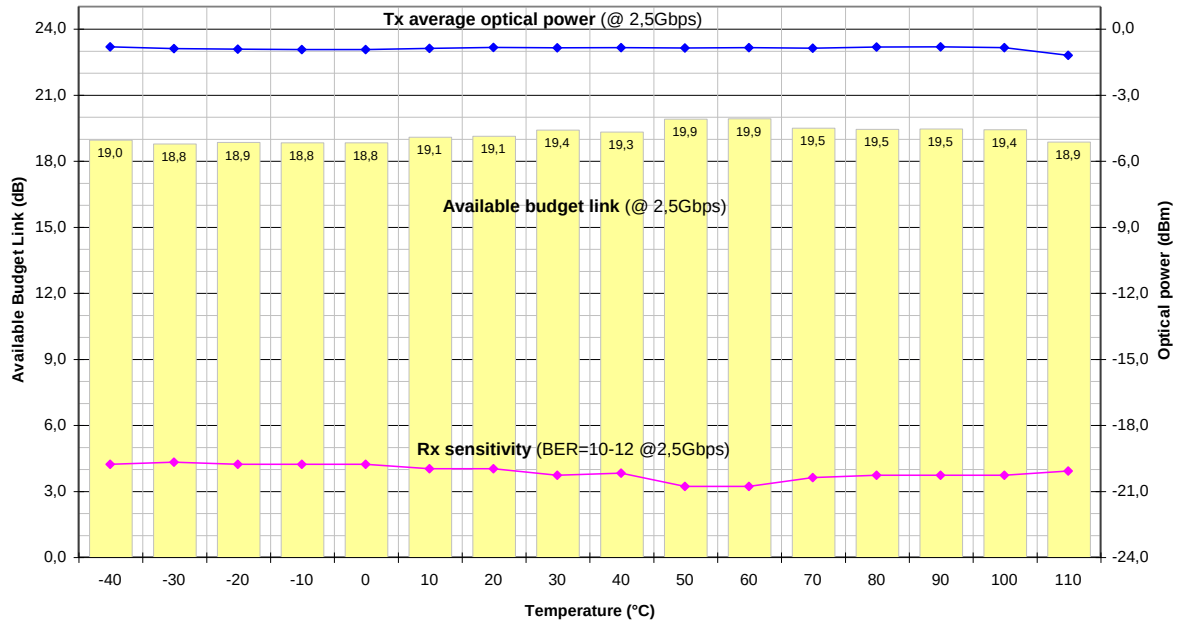

Figure 17 - Typical Tx optical power, Rx optical sensitivity and corresponding available budget link as a function of temperature at 2,5 Gbps.

Typical Eye diagrams

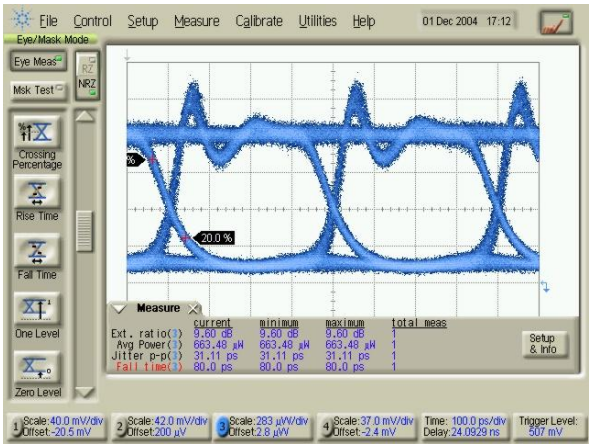

Figure 18 - 2.5GBps Tx optical eye diagram. 90°C external temperature.
ER = 9.6 dB, Pavg = 826µW
(Note that the optical eye is not filtered on this picture and that the optical power measurement at the scope is not calibrated).

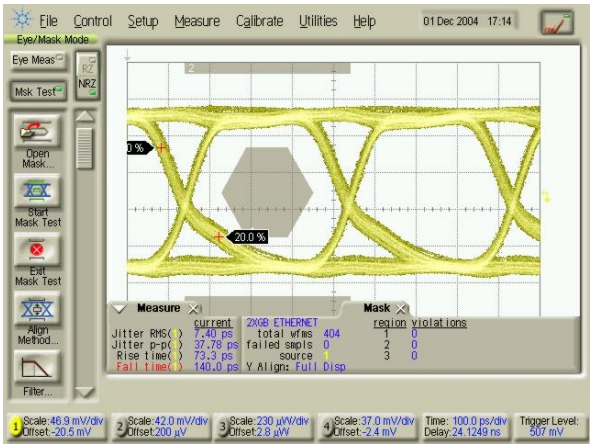

Figure 19 - 2.5GBps Rx electrical eye diagram. 90°C external temperature.
J_{rms} = 7ps, J_{p-p} = 38ps, T_r = 73ps, T_f = 140ps.

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5x8 socket package mechanical drawings

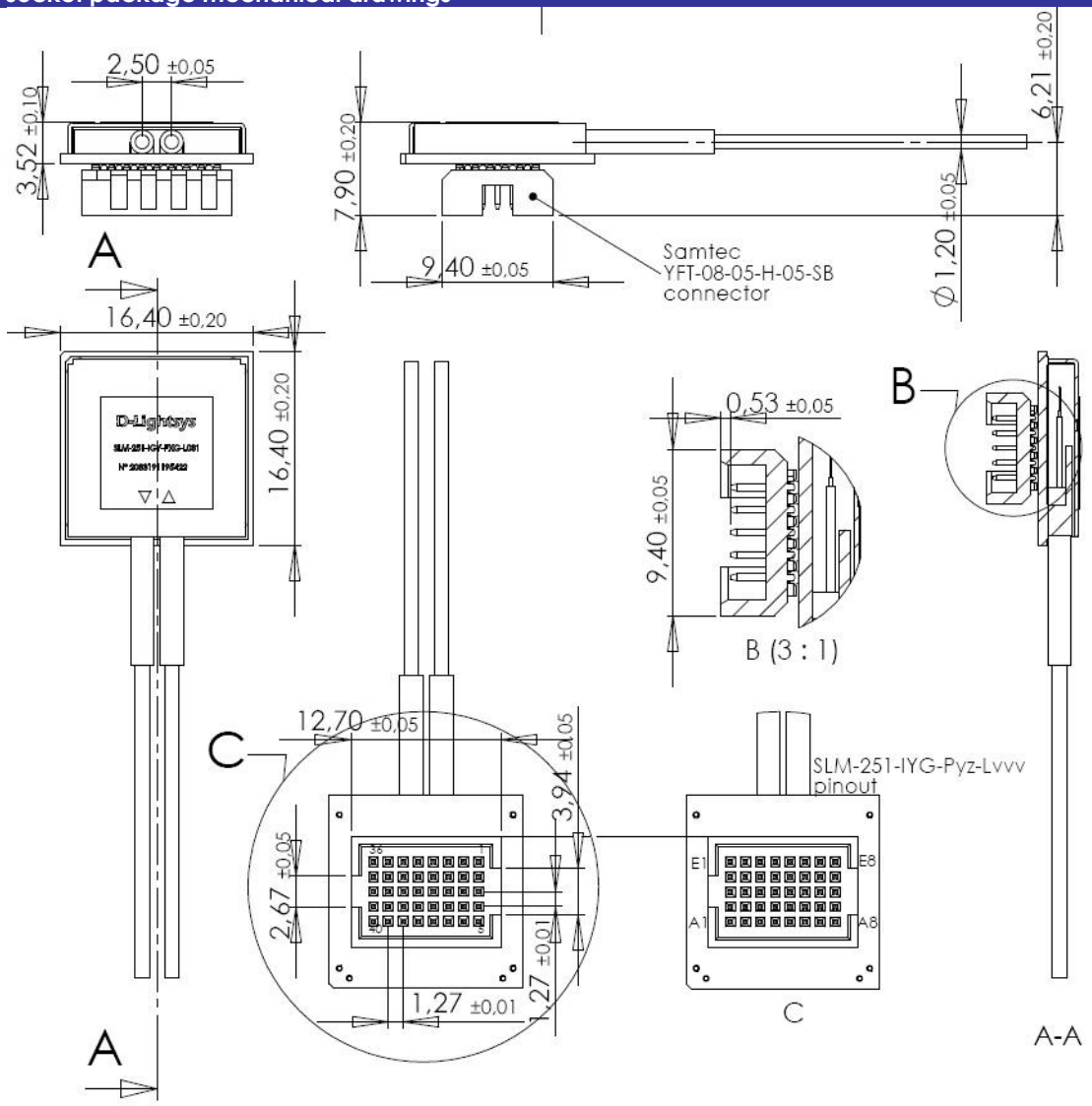

Figure 20 - YFT package mechanical dimensions (Ref: SLM-251-IGY–Pyz-Lvv)

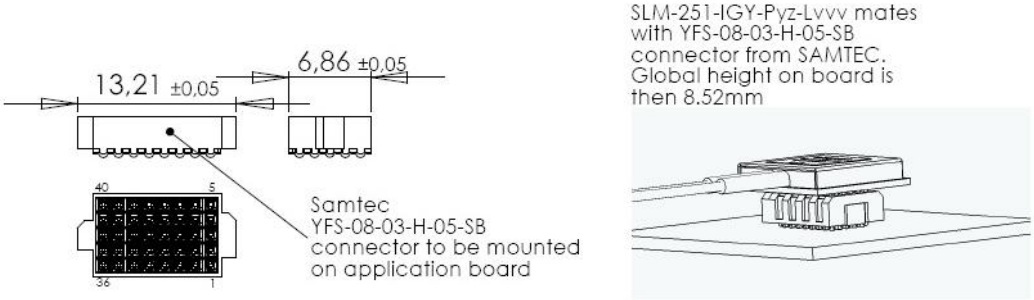

Figure 21 - YFS receptacle mechanical dimensions

SAMTEC Ordering P/N for the YFS-08-03-H-05-SB socket **is ASP-11046904**

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YFT package pin out description

Pins	1	2	3	4	5	6	7	8
A	GND	DIN+	DIN-	GND	GND	DOUT+	DOUT-	GND
B	GND	GND	GND	GND	GND	GND	GND	GND
C	TxEnable	VCCTx	VCCTx	GND	GND	VCCRx	VCCRx	SD
D	TxFault	V_{AVG}	V_{MOD}	GND	GND	NC	NC	RSSI
E	SDA	SCL	WP	GND	GND	NC	NC	NC

LCC Package mechanical drawings

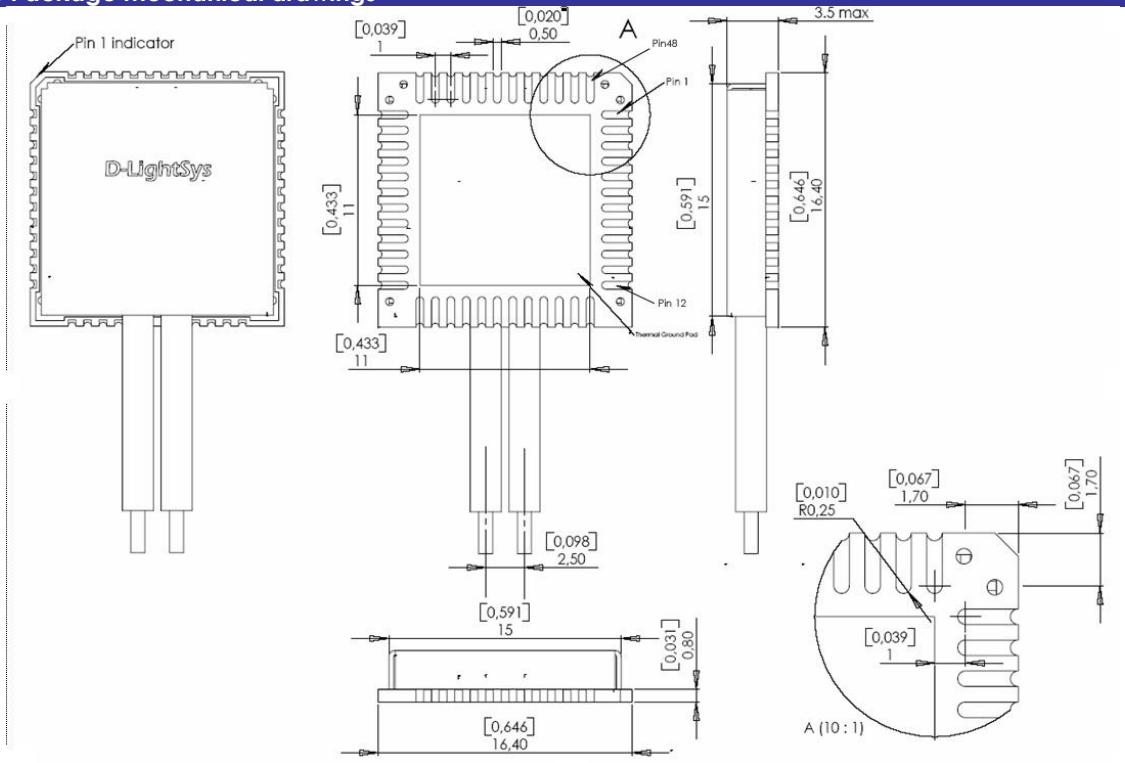
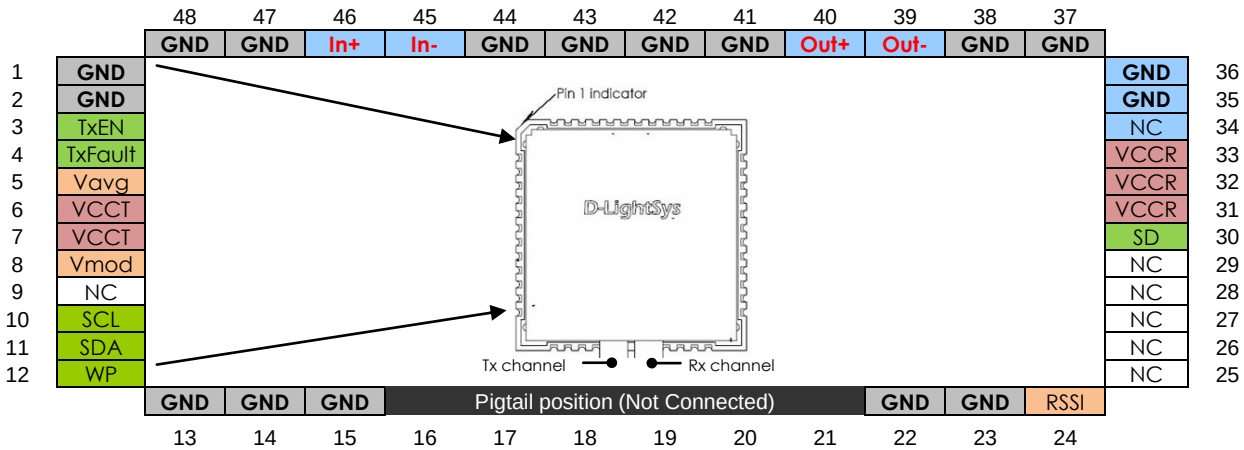


Figure 22 - LCC package mechanical dimensions (Ref: SLM-251-IL–Pyz-Lvv)

LCC Package Pin Layout (DLM-xx-251-IL option)



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Pin out description

Signal	Pin number		Type	Description
	LCC	YFT		
DataIn-	45	A3	HS[1] Input	**Negative Data input:** LVDS/CML negative high speed input
DataIn+	46	A2	HS[1] Input	**Positive Data input:** LVDS/CML positive high speed input
TxEnable	3	C1	Digital Input	**Transmitter Enable/Disable:** This pin allows the user to disable the laser. When this pin is high no current is pulled from the VCSEL. When low the data inputs modulate the output.
TxFault	4	D1	Digital Output	**Transmitter Fault:** A VCSEL Voltage Supervisor signal that provides a digital output high when the driver output leaves a specific range between V_{VVH} (VCSEL voltage high) and V_{VVL} (VCSEL voltage low). This is an active high output.
V_{AVG}	5	D2	Analog output	**Average Voltage Control:** Voltage proportional to the bias current flowing into the VCSEL
V_{MOD}	8	D3	Analog output	**Modulation Voltage Control :** Voltage proportional to the modulation current flowing into the VCSEL
SCL	10	E2	Digital Input	**2-Wire serial Clock input:** The serial clock input is used to clock data (SDA pin) into the module on rising edges and clock data out on falling edges. Connected to V_{EETx} if not used.1
SDA	11	E1	Digital Input/ Output	**2-Wire serial data interface:** The serial data pin is for serial data transfer to and from the module. The pin is open drain and may be wire-ORed with other open drain or open collector interfaces. Connected to V_{EETx} if not used.
WrProtect	12	E3	Digital Input	**Write protect:** If open or set to logic 1, all memory, control registers, and Look-up tables are write protected. If set to a logic 0, the device is not write protected and can be written to. The WP pin is pulled high internally.
V_{CCTx}	6, 7	C2, C3	Power	**Positive supply:** +3.3Volts positive power supply for the transmitter.
DataOut-	39	A7	HS[1] Output	**Negative Data Output:** CML negative high speed output.
DataOut+	40	A6	HS[1] Output	**Positive Data Output:** CML positive high speed output.
RSSI	24	D8	Analog output	**Receiver Signal Strength Indicator (Average optical power):** This Analog output pin allows the user to monitor the average incident optical power**.** The voltage on this pin is proportional to the input optical power. *See detailed description.*
SD	30	C8	Digital output	**SD / Int :** Signal detect/interrupt pin is a fully programmable pin, throught the I2C interface, that is asserted/desasserted according the violation of internal threshold registers/values. This pin is programmed by default to act as an active low signal detect (SD) function.
V_{CCRx}	31, 32, 33	C6, C7	Power	**Positive supply:** +3.3Volts positive power supply for the receiver.
VEE	1-2, 13-23, 35-38, 41-44, 47-48	A1, A4, A5, A8, B1-B8, C4, C5, D4, D5, E4, E5	Power	**Negative supply:** negative power supply tied to GND (0 Volt) for the transmitter and receiver
NC		D6, D7, E6, E7, E8	-	**Non Connected Pins:** Unconnected pin. Do not connect.

Notes:

1. HS pin type: High Speed inputs / output pins.

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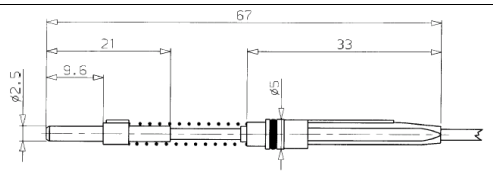
Pigtail mechanical drawing

Pigtail length can be adjusted to fit the customer's requirements.

The following pigtail termini/connectors are available.

▪ **E option :** Elio contacts from Souriau (based on 2.5 mm ferrule).	
▪ **X option :** LuxCis termini from Radiall (based on 1.25 mm ferrule).	
▪ **Other options available**	

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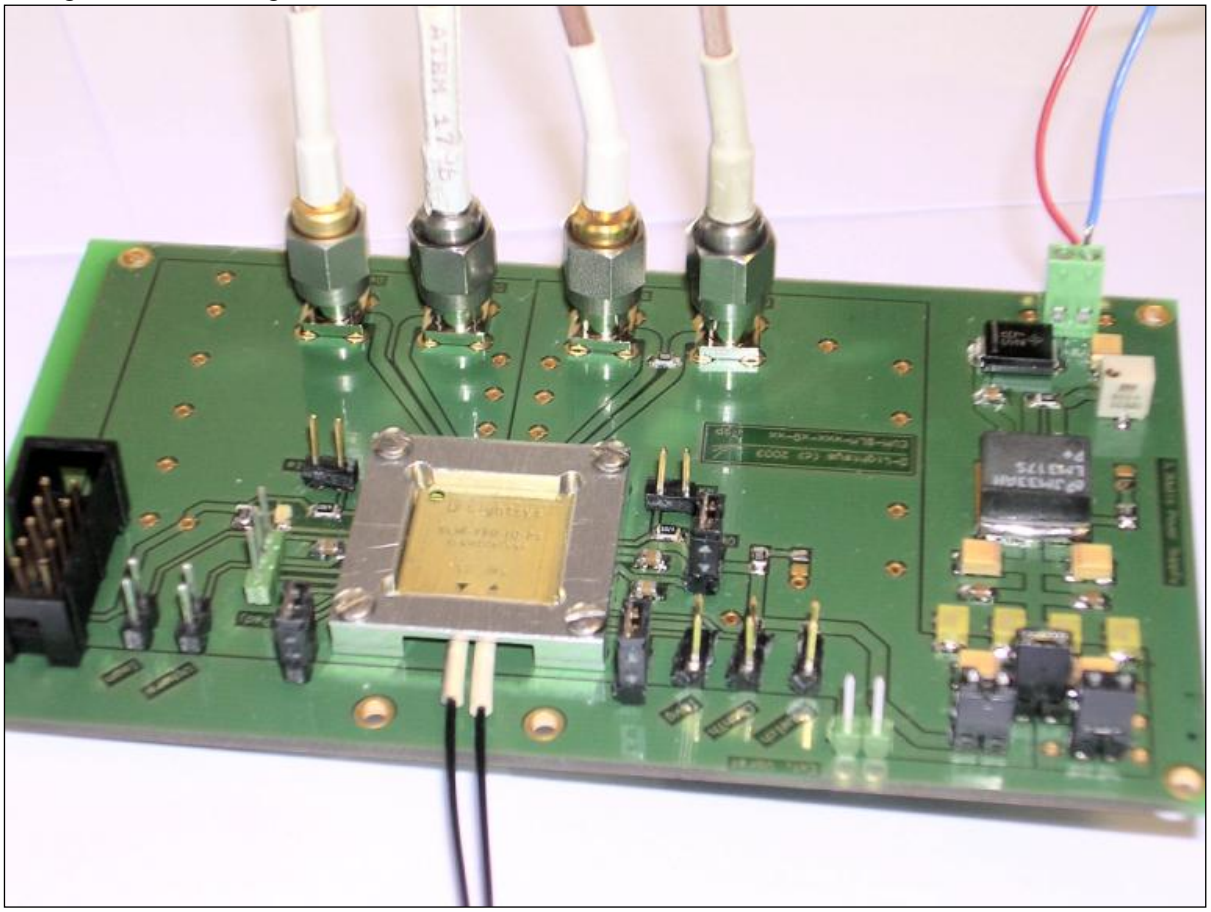
Evaluation board

An evaluation board is available for module testing. The picture below shows an LCC/QFN module evaluation board (Ref. EVB-SLM/02-A) with SMA connectors. A module holding tool permits module testing without soldering.



Related literature (distributed under Non-Disclosure Agreement)

Specification & Datasheet:

Application Notes:

Ref: AN-SLM/01 "*S-Light transceiver usages*"
Ref: AN-SLM/02 "*S-Light & D-Light family 2-wire serial interface usage*"
Ref: AN-SLM/03 "*S-Light & D-Light family input/output stage modeling*"
Ref: AN-SLM/05 "*S-Light & D-Light family Surface mount reflow process*"
Ref: AN-SLM/06 "*S-Light & D-Light family Surface bonding process*"
Ref: AN-SLM/07 "*S-Light & D-Light family thermal modeling*"

Evaluation board & Software materials:

Ref: EVB-SLM/02 " *SLM-vvv-wx-Pyz* Evaluation board documentation"
Ref: SOF-SLM/01 "Windows Based S-Light family module programming software user's guide"

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