GLS85LP0512P / 1002P / 1004P / 1008P
Industrial Grade PATA NANDrive™

Fact Sheet 02.000
June 2012

Features

- **Industry Standard ATA / IDE Bus Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-6 [1)]
  - Supports up to Multi-Word DMA Mode-4 [2)]
  - Supports up to Ultra DMA Mode-6
- **Performance**
  - Sustained sequential data read - Up to 50 MByte/sec
  - Sustained sequential data write - Up to 39 MByte/sec
- **Power Management**
  - 3.3V power supply
  - Immediate disabling of unused circuitry without Host intervention
  - Zero wake-up latency
- **Power Specification**
  - Active mode
    110mA typical (GLS85LP1008P)
    80mA typical (GLS85LP1004P)
    60mA typical (GLS85LP1002P/0512P)
  - Sleep mode
    500µA typical
- **Expanded Data Protection**
  - WP#/PD# pin configurable by firmware for prevention of data overwrites
  - Data security through user-selectable protection zones
  - Security Erase feature
- **20-Byte Unique ID for Enhanced Security**
  - Factory pre-programmed 10-Byte unique ID
  - User-programmable 10-Byte ID
- **Integrated Voltage Detector**
  - Prevents inadvertent Write operations due to unexpected power-down or brownout
- **Pre-programmed Embedded Firmware**
  - Executes industry standard ATA/IDE commands
  - Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
- **Robust Built-in ECC**
- **Industrial Temperature Range**
  - -40°C to 85°C
- **91-ball BGA and LBGA Packages**
  - 14mm x 24mm x 1.90mm (GLS85LP1002P/1004P/1008P)
  - 12mm x 24mm x 1.40mm (GLS85LP0512P)
- **All Devices are RoHS Compliant**

Product Description

The GLS85LP0512P / 1002P / 1004P / 1008P Industrial Grade PATA NANDrive™ devices (referred to as "PATA NANDrive" in this datasheet) are high-performance, fully-integrated, embedded flash solid state drives. They combine an integrated ATA Controller and 512 MByte, 2 GByte, 4 GByte or 8 GByte of NAND flash memory in a multi-chip package. These products are ideal for embedded and portable applications that require smaller form factor and more reliable data storage.

ATA-based solid state mass storage technology is widely used in GPS and telematics, in-vehicle infotainment, portable and industrial computers, handheld data collection scanners, point-of-sale terminals, networking and telecommunications equipment, robotics, audio and video recorders, monitoring devices and set-top boxes.

The PATA NANDrive supports standard ATA/IDE protocol with up to PIO Mode-6[1)], Multi-Word DMA Mode-4[2)] and Ultra DMA Mode-6 interface. The PATA NANDrive device provides complete IDE hard disk drive functionality and compatibility in a 14mm x 24mm BGA package or a 12mm x 24mm LBGA package for easy, space-saving mounting to a system motherboard. These products surpass traditional storage in their small size, security, reliability, ruggedness and low power consumption.

The integrated NAND flash controller with built-in advanced NAND management firmware communicates with the Host through the standard ATA protocol. It does not require any additional or proprietary software such as the Flash File System (FFS) and Memory Technology Driver (MTD).

The PATA NANDrive provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites. The PATA NANDrive is pre-programmed with a 10-Byte unique serial ID and has the option of programming an additional 10-Byte serial ID for even greater system security.

The PATA NANDrive's advanced NAND management technology enhances data security, improves endurance and accurately predicts the remaining lifespan of the NAND flash devices. This innovative technology combines robust error correction capabilities with advanced wear-leveling algorithms and bad block management to significantly extend the life of the product.

1) PATA NANDrive is capable of supporting PIO Mode-6, but Identify-Drive information report will show PIO Mode-4
2) PATA NANDrive is capable of supporting Multi-Word DMA Mode-4, but Identify-Drive information report will show MWDMA Mode-2

1.0 GENERAL DESCRIPTION

Each PATA NANDrive contains an integrated PATA NAND flash memory controller and NAND flash die in a BGA or LBGA package. Refer to Figure 2-1 for the Industrial Grade PATA NANDrive block diagram.

1.1 Optimized PATA NANDrive

The heart of the PATA NANDrive is the PATA NAND flash memory controller, which translates standard PATA signals into flash media data and control signals. The following components contribute to the PATA NANDrive's operation.

1.1.1 Microcontroller Unit (MCU)

The MCU transfers the ATA/IDE commands into data and control signals required for flash media operation.

1.1.2 Internal Direct Memory Access (DMA)

The PATA NANDrive uses internal DMA allowing instant data transfer from/to buffer to/from flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The PMU controls the power consumption of the PATA NANDrive. The PMU dramatically reduces the power consumption of the PATA NANDrive by putting the part of the circuitry that is not in operation into sleep mode.

The Flash File System handles inadvertent power interrupts and has auto-recovery capability to ensure the PATA NANDrive's data integrity. For regular power management, the Host must send an IDLE_IMMEDIATE command and wait for command ready before powering down the PATA NANDrive.

1.1.4 Embedded Flash File System

The embedded flash file system is an integral part of the PATA NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads
2. Provides flash media wear leveling to spread the flash writes across all memory address space to increase the longevity of flash media
3. Keeps track of data file structures
4. Manages system security for the selected protection zones
5. Stores the data in flash media upon completion of a Write command (The PATA NANDrive does not perform Post-Write operations, except for when the write cache is enabled)

1.1.5 Error Correction Code (ECC)

High performance is achieved through optimized hardware error detection and correction.

1.1.6 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed for manufacturing error reporting. During the design process, always provide access to the SCI port in the PCB design to aid in design validation.

1.1.7 Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing concurrent Read, Program and Erase operations to multiple flash media.

1.2 SMT Reflow Consideration

The PATA NANDrive family utilizes standard NAND flash for data storage. Because the high temperature in a surface-mount soldering reflow process can alter the content on NAND flash, do not program the PATA NANDrive before the reflow process.

1.3 Advanced NAND Management

The PATA NANDrive's integrated controller uses advanced wear-leveling algorithms to substantially increase the longevity of NAND flash media. Wear caused by data writes is evenly distributed in all or select blocks in the device that prevents "hot spots" in locations that are programmed and erased extensively. This effective wear-leveling technique results in optimized device endurance, enhanced data retention and higher reliability required by long-life applications.

2.0 FUNCTIONAL BLOCKS

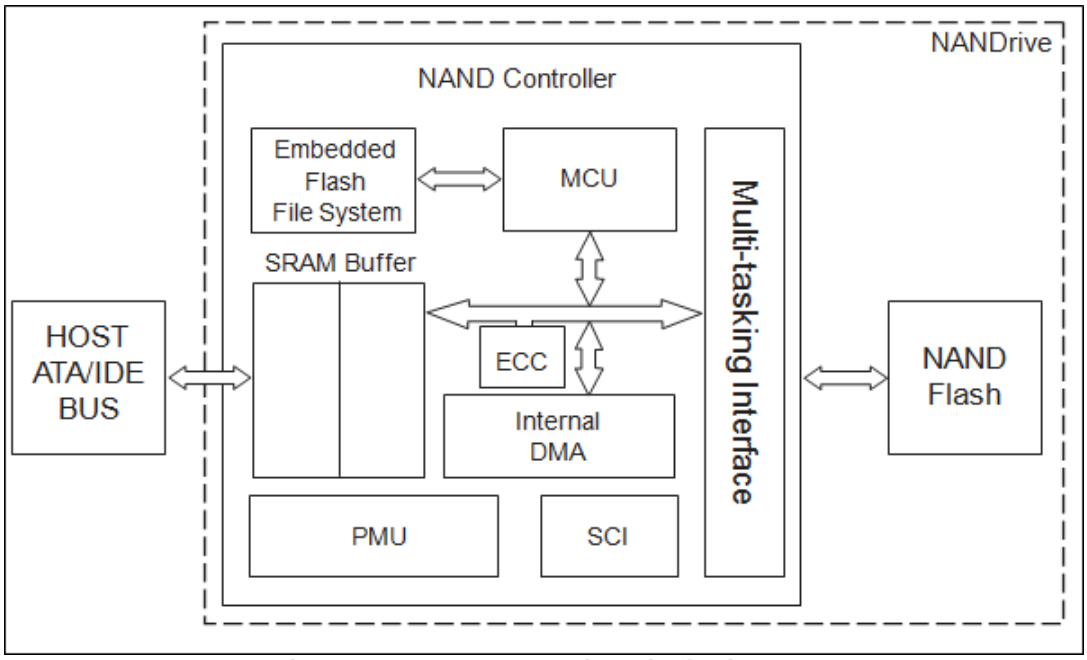


Figure 2-1: PATA NANDrive Block Diagram

3.0 PIN ASSIGNMENT

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output or Input/Output. Signals that the Host sources are designated as inputs, while signals that the PATA NANDrive sources are outputs.

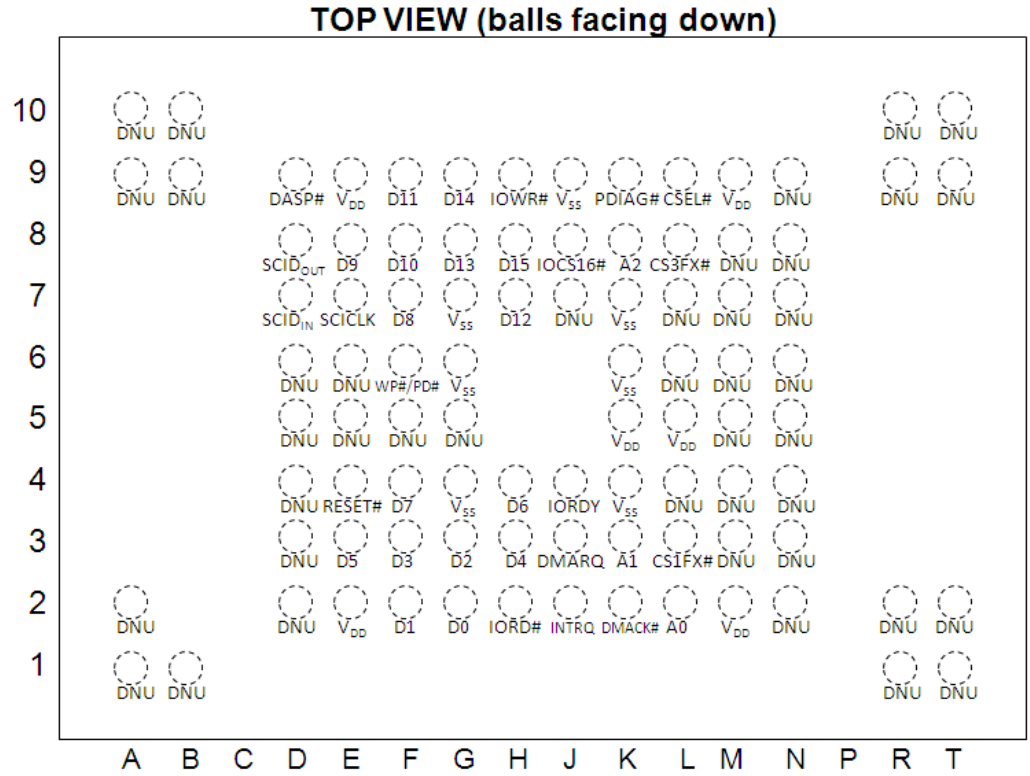


Figure 3-1: Pin Assignments for 91-Ball BGA / LBGA

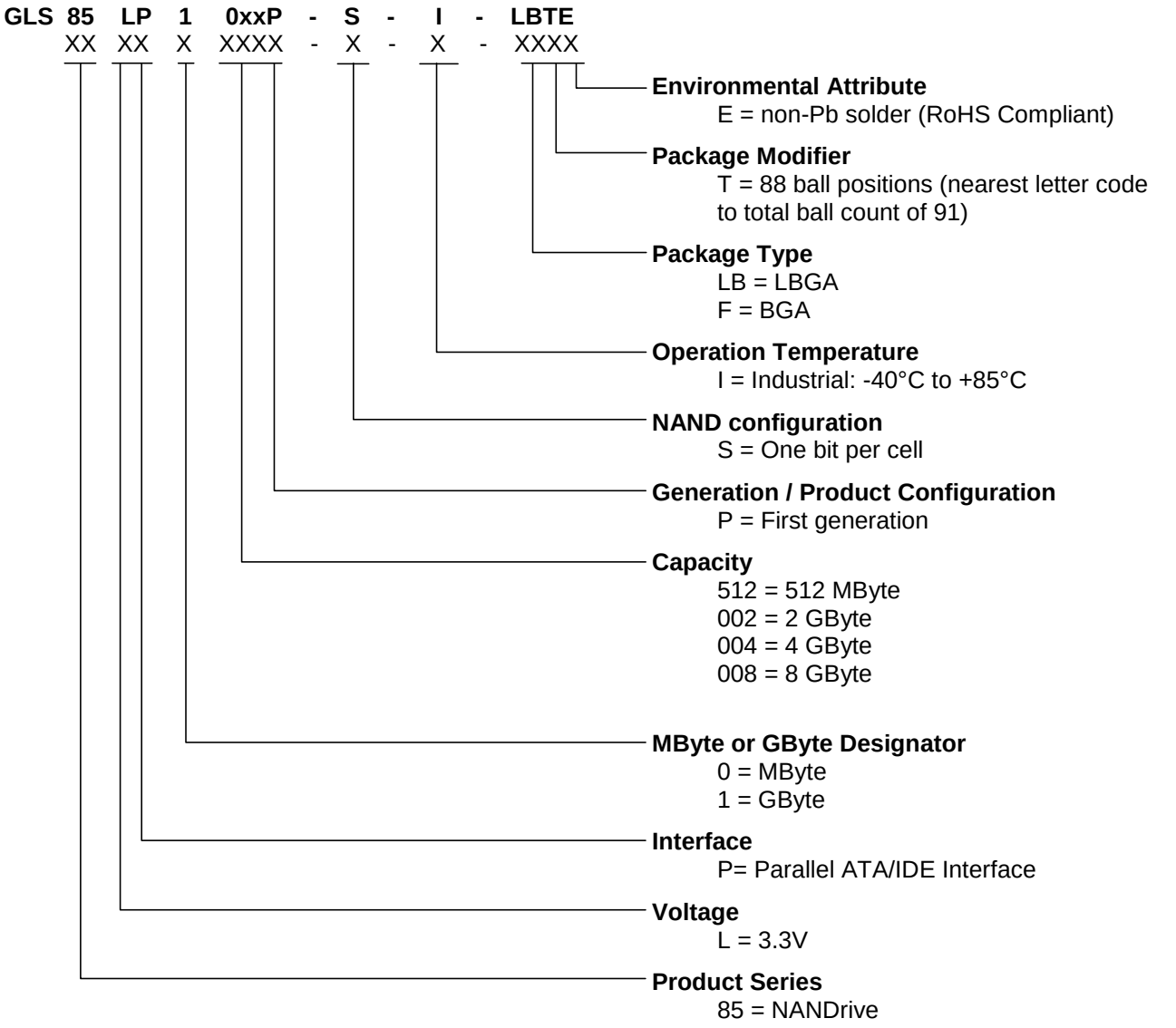
Table 3-1: Pin Assignments (1 of 2)

Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
Host Side Interface				
A2	K8	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	K3			
A0	L2			
D15	H8	I/O	I1Z/O2	D[15:0] Data bus
D14	G9			
D13	G8			
D12	H7			
D11	F9			
D10	F8			
D9	E8			
D8	F7			
D7	F4			
D6	H4			
D5	E3			
D4	H3			
D3	F3			
D2	G3			
D1	F2			
D0	G2			
DMACK#	K2	I	I2U	DMA Acknowledge - input from Host
DMARQ	J3	O	O2	DMA Request to Host
CS1FX#	L3	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	L8			CS3FX# is used to select the alternate status register and the Device Control register.
CSEL	L9	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	H2	I	I2Z	IORD#: This is an I/O Read Strobe generated by the Host. When Ultra DMA mode is not active, this signal gates I/O data from the device. (This pin supports three functions)
				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the Host to indicate that the Host is ready to receive Ultra DMA data-in bursts. The Host may negate HDMARDY# to pause an Ultra DMA transfer.
				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the Host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The Host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
IOWR#	H9	I	I2Z	IOWR#: This is an I/O Write Strobe generated by the Host. When Ultra DMA mode is not active, this signal is used to clock I/O data into the device. (This pin supports two functions)
				STOP: When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst

Table 3-1: Pin Assignments (2 of 2)

Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
IORDY	J4	O	O2	IORDY: When in PIO mode, the device is not ready to respond to a data transfer request. This signal is negated to extend the Host transfer cycle from the assertion of IORD# or IOWR#. However, it is never negated by this controller. (This pin supports three functions) DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the device to indicate that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer. DSTROBE: When Ultra DMA mode DMA Read is active, this signal is the data-in strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the Host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.
IOCS16#	J8	O	O3	This output signal is asserted low when the device is indicating a Word data transfer cycle.
INTRQ	J2	O	O2	This signal is the active high Interrupt Request to the Host.
PDIAG#	K9	I/O	I1U/O2	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	D9	I/O	I1U/O4	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	E4	I	I2U	This input pin is the active low hardware reset from the Host.
Serial Communication Interface (SCI)				
SCIDOUT	D8	O	O2	SCI data output. No external pull-up or pull-down resistor should connect to this signal.
SCIDIN	D7	I	I1U	SCI data input
SCICLK	E7	I	I1D	SCI clock
Miscellaneous				
WP#/PD#	F6	I	I2U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting.
V_{SS}	G4, G6, G7, K4, K6, K7, J9	PWR		Ground
V_{DD}	E2, E9, K5, L5, M2, M9	PWR		VDD (3.3V)
DNU	A1, A2, A9, A10, B1, B9, B10, D2, D3, D4, D5, D6, E5, E6, F5, G5, J7, L4, L6, L7, M3, M4, M5, M6, M7, M8, N2, N3, N4, N5, N6, N7, N8, N9, R1, R2, R9, R10, T1, T2, T9, T10			Do not use. All these pins should not be connected.

4.0 Product Ordering Information



Valid Combinations

PATA NANDrive Product

GLS85LP0512P-S-I-LBTE, GLS85LP1002P-S-I-FTE, GLS85LP1004P-S-I-FTE
GLS85LP1008P-S-I-FTE,

PATA NANDrive Evaluation Board (xxCN: xx-pin ATA Interface EVB, K: Kit)

GLS85LP0512P-S-I-40CN-K, GLS85LP0512P-S-I-44CN-K
GLS85LP1002P-S-I-40CN-K, GLS85LP1002P-S-I-44CN-K
GLS85LP1004P-S-I-40CN-K, GLS85LP1004P-S-I-44CN-K
GLS85LP1008P-S-I-40CN-K, GLS85LP1008P-S-I-44CN-K

Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid combinations and to determine availability of new product combinations.

4.1 Package Diagrams

4.1.1 FTE Package

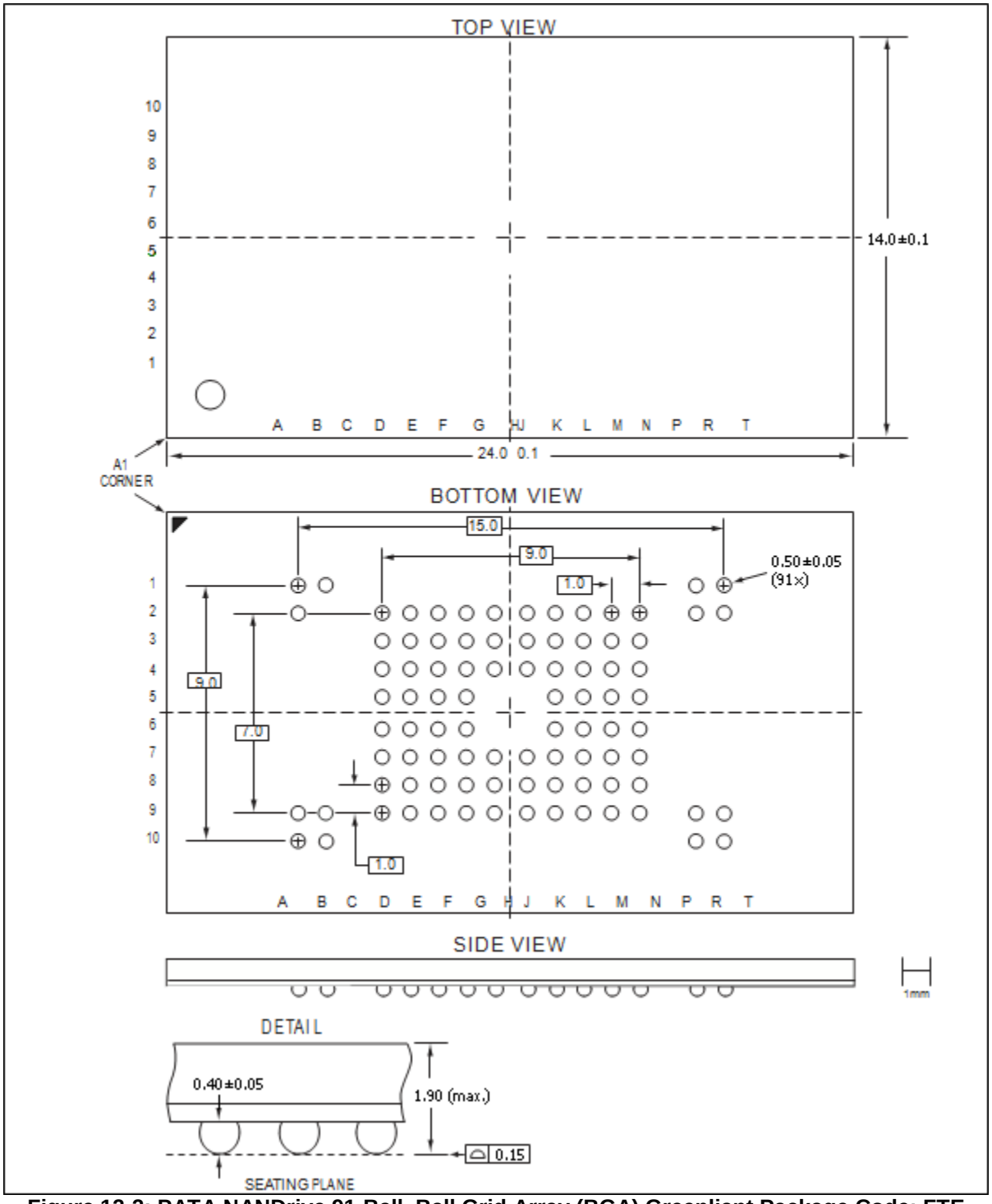


Figure 12-2: PATA NANDrive 91-Ball, Ball Grid Array (BGA) Greenliant Package Code: FTE

Note: All linear dimensions are in millimeters.
Un-tolerance dimensions are nominal target values.
Co-planarity: 0.15 mm.
Ball opening size is 0.40 mm (± 0.05 mm).

4.1.2 LBTE Package

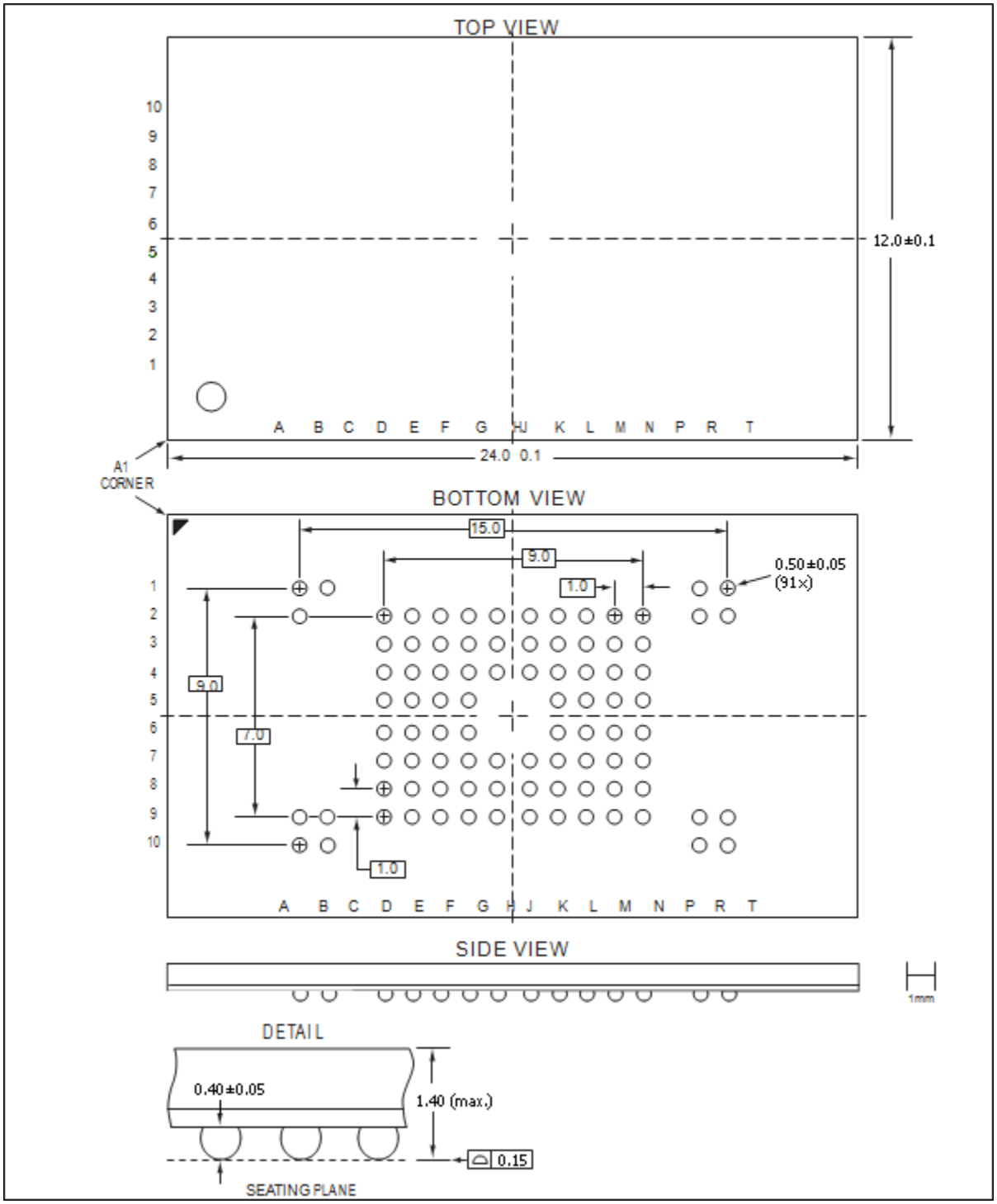


Figure 12-3: PATA NANDrive 91-Ball, Ball Grid Array (LBGA) Greenliant Package Code: LBTE

Note: All linear dimensions are in millimeters.
Un-tolerance dimensions are nominal target values.
Co-planarity: 0.15 mm.
Ball opening size is 0.40 mm (± 0.05 mm).

4.2 Reference Documents

Table 12-1: Reference Documents

Title	Revision	Date
Industrial Grade 512MB/2GB/4GB/8GB NANDrive Migration Guide v01.02	01.020	January 24, 2011
NANDrive SMART Specification	02.000	February 10, 2011
NANDrive Protection Zone Specification	01.000	February 10, 2011
NANDrive Security Erase Feature/ Purge Command	01.100	February 10, 2011
WindowsPT2 User Guide	02.000	March 1, 2011
NANDrive on Memory Bus	01.000	March 10, 2011
NANDrive Special Function Zone	01.000	August 16, 2011

4.3 Revision History

Table 12-2: Revision History

Number	Description	Date
01.000	Initial release of datasheet	June 15, 2011
02.000	Added Total program/erase cycle count Updated Power specification, Initialization time and Purge time	June 1, 2012