PEX 8619BA Base Board RDK
Hardware Reference Manual

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PREFACE

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ABOUT THIS MANUAL

This document describes the PLX PEX 8619BA-Base Board RDK, a Rapid Development Kit, from a hardware perspective. It contains a description of all major functional circuit blocks on the board and also is a reference for the creation of software for this product. This manual also includes complete schematics and bill of materials.

REVISION HISTORY

Date	Version	Comments
April 2009	1.0	Initial Release

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FIGURES

TABLES

1. General Information

The PLX PEX 8619BA Base Board RDK is a Rapid Development Kit based on the PEX 8619, a 16-lane, 16-port PCI Express switch based in the PCI Express Specification rev 2.0 with SerDes capable of running at 5 GT/s. The PEX 8619BA Base Board RDK provides a complete hardware and software development platform that facilitates getting designs up and running quickly, lowering risk and reducing time-to-market. This RDK consists a base board containing three hardware configuration Modules, a PCI Express cable adapter board that plugs into the host system, and up to two x4 PCI Express cables that used to connect the RDK to the cable adapter. This manual primarily focuses on the PEX 8619BA Base Board RDK, and its use with other parts to demonstrate the various functions of PEX 8619 chip. Figure 1 provides a top view (component side) of the PEX 8619BA Base Board RDK.

1.1 PEX 8619 Features

- 16-lane, 16-port PCI Express Gen 2 switch with integrated on-chip SerDes
- 160 GT/s aggregate bandwidth (5.0 GT/s/Lane x 16 Lanes x 2 (full duplex))
- 19mm^2 324-ball Plastic Ball Grid Array (PBGA) package
- Typical Power – 2.2W
- Cut-Thru packet latency of less than 160ns
- Low power SerDes (under 90mW per lane)
- Fully non-blocking switch architecture
- Flexible port configuration
    - 16 flexible and configurable ports (x1,x4 or x8), x2 is also supported
- Flexible device configuration
    - Configurable via serial EEPROM, I^{2}C, hardware strapping, or by the host
- Maximum packet payload size of 2,048 bytes
- Designate any Port as the *Upstream Port* (Port 0 is recommended)
- Dynamic Buffer Pool Architecture
- Read Pacing (allows user to throttle Read requests from Downstream Ports to allow for more efficient performance)
- Dual-Casting (enhances performance by sending date from one ingress port to two egress ports)
- Integrated Direct Memory Access (DMA) engine
- Dynamic speed (2.5 GT/s or 5.0 GT/s) negotiation
- Dynamic link-width negotiation (automatically negotiates down to optimal link-width based on traffic density)
- Lane and polarity reversal
- Non-Transparent Bridging support
    - Enables Dual-Host, Host-Failover applications
- Conventional PCI-compatible Link Power Management states – L0, L0s, L1, L2/L3 Ready, and L3 **(**with Vaux not supported)
- Conventional PCI-compatible Device Power Management states – D0 and D3hot
- Active State Power Management
- Spread-Spectrum Clock Isolation (Dual-clock Domain)
- Quality of Service (QoS)
    - Two Virtual Channels (VC0 and VC1) and Eight Traffic classes (TC)
    - Weighted Round-Robin Port and Virtual Channel arbitration
- Reliability, Availability, Serviceability (RAS) features
    - All ports are Hot-Plug capable through I^{2}C (Serial Hot-Plug Controller on every port)
    - Advanced Error Reporting capability
    - Performance Monitoring
        - Per-Port Payload and Header Counters
        - Per-traffic type (write, Read, Completion) Counters
    - JTAG AC/DC boundary scan
    - 16 Lane status balls (PEX_LANE_GOOD[15:0]#)
    - 32 GPIO balls (GPIO[31:0]

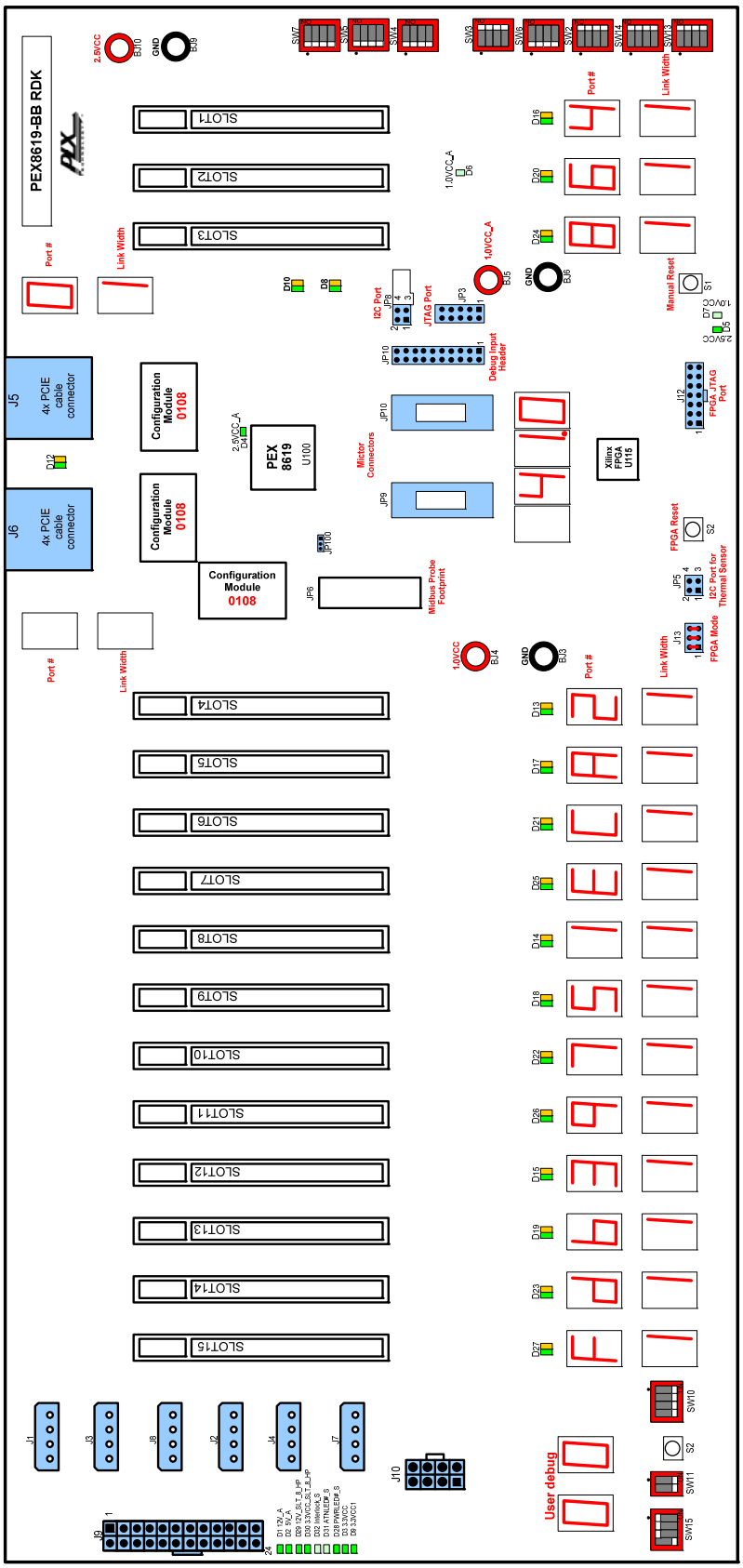


Figure 1. PEX 8619BA Base Board RDK Front View

- INTA# (PEX_INTA#) and FATAL ERROR (FATAL_ERR#) (Conventional PCI SERR# equivalent) ball support
- Compliant to the following specifications:
  - *PCI Local Bus Specification, Revision 3.0 (PCI r3.0)*
  - *PCI Bus Power Management Interface Specification, Revision 1.2 (PCI Power Mgmt. r1.2)*
  - *PCI to PCI Bridge Architecture Specification, Revision 1.2 (PCI-to-PCI Bridge r1.2)*
  - *PCI Express Base Specification, Revision 1.1 (PCI Express Base r1.1)*
  - *PCI Express Base Specification, Revision 2.0 (PCI Express Base r2.0)*
  - *IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture, 1990 (IEEE Standard 1149.1-1990)*
  - *IEEE Standard 1149.1a-1993, IEEE Standard Test Access Port and Boundary-Scan Architecture*
  - *IEEE Standard 1149.1-1994, Specifications for Vendor-Specific Extensions*
  - *IEEE Standard 1149.6-2003, IEEE Standard Test Access Port and Boundary-Scan Architecture Extensions (IEEE Standard 1149.6-2003)*
  - *The I^2C-Bus Specification, Version 2.1 (I^2C Bus v2.1)*

1.2 PEX 8619BA-BB RDK Features

- PLX PEX 8619 PCI Express switch in a 324-ball Plastic BGA package
- Based on PCI Express Card Electromechanical (CEM) Specification 2.0 and PCI Express External Cabling Specification 1.0
- Supports up to 6 different port configurations with x4 PCI Express cable connection(s) to the upstream PC
- Non-Transparent Bridging support
- One x8 Gen 2 Midbus probe footprint for upper 8 lanes of PCI Express signal probing for the chip
- PCI Express RefClk Circuits supports Spread-Spectrum Clock Isolation
- Serial Hot-Plug circuits on one PCI Express card edge connector
- In system programmable Serial EEPROM (2.5V)
- A standard 2x2 header provides the I^2C interface to an I^2C master
- DIP switches for port configuration, upstream port or NT port select and I^2C address settings
- Manual push-button PERST# capability
- Up to sixteen dual color LEDs for visual inspection of link speed and status
- 7-Segment displays for port numbers and link width
- Up to 3-digit display for junction temperature of PEX 8619
- Voltage level monitoring circuit for 1.0V and 2.5V power to the PEX 8619

2. System Architecture

The PEX 8619BA-Base Board RDK is a 21” x 10” bench top board for silicon evaluation and design reference for the PEX 8619 PCI Express Gen 2 switch. This RDK consists of three main hardware components: the base board, the PCI Express External Cable Adapter and PCI Express Cable assembly. Figure 1 represents the placement of major component blocks on the RDK base board. Figure 2 and Figure 3 provide diagrams of the RDK being used in a PC. The RDK provides up to 15 PCI Express slots for add-in cards and visual indicators for port, link status and speed information. The RDK is designed to be powered up with an ATX power supply.

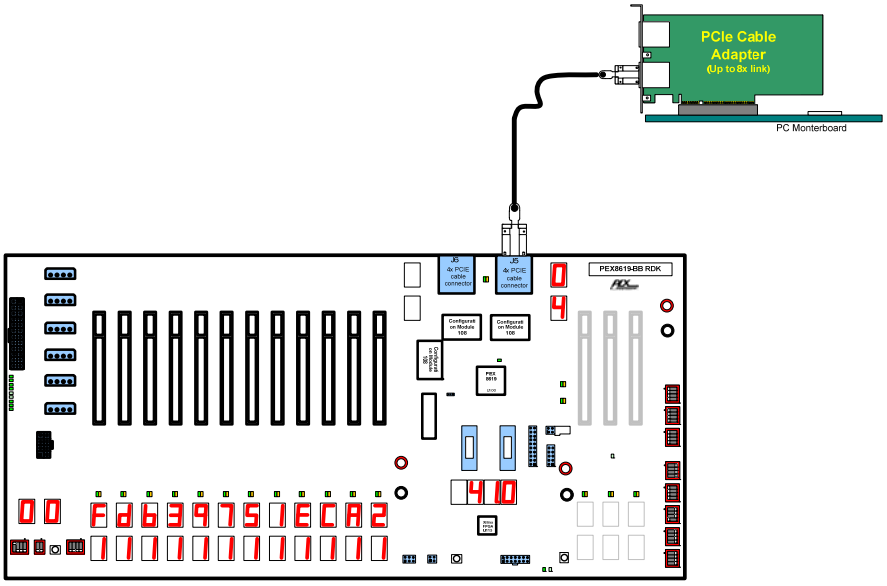


Figure 2. Connecting The RDK to a PC with x1 or x4 link

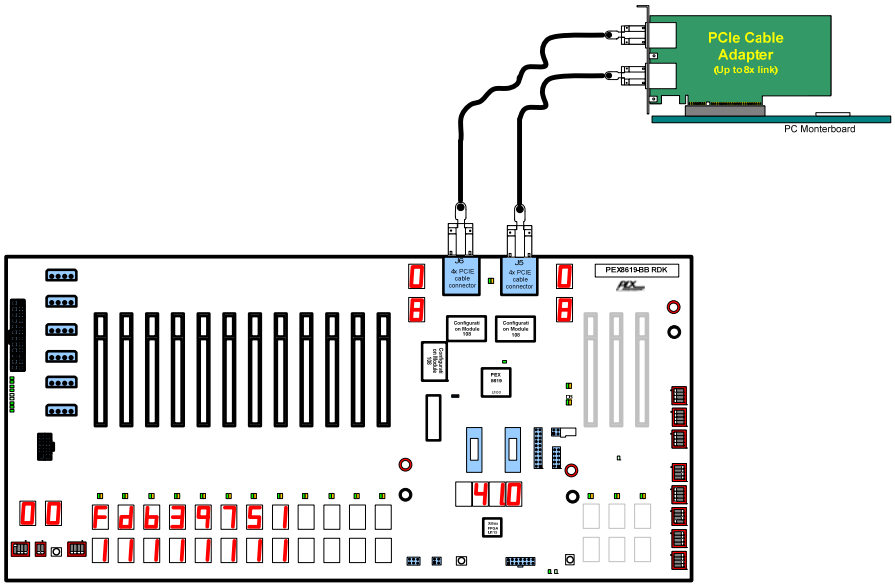


Figure 3. Connecting the RDK to a PC with x8 link

3. Hardware Architecture

The PEX 8619BA Base Board RDK is designed around the PEX 8619, a 16-port, 16-lane Gen 2 switch, and based on the PCI Express CEM 2.0 Specification. The RDK offers PCI Express interfaces to 15 PCI Express Edge Card Connectors, two x4 PCI Express External cable connectors, and three configuration modules. The RDK is designed to support 6 different port configurations (see Table 1 for details) and to connect to its upstream PC through its PCI Express Cable Connectors. The RDK relies on the PC connected to its PCI Express Cable Connector J5 to obtain it primary PCI Express reference clock and reset to support the RDK normal functions. Also, the RDK provides visual indications for power, link speed, port status, port number, and link width.

3.1 PEX 8619

The PEX 8619 is a 16-lane, 16-port PCI Express Gen 2 (5.0GT/s) switch. It is in 19mmx19mm package and it. It supports 9 different types of port configurations. Each with any port in the PEX 8619 can be designated as the upstream port or NT port. The PEX 8619 supports two clock domains which allows the support of Spread - Spectrum Clocking (SSC) isolation. The PEX 8519 also provides 16 lane status drivers and 32 GPIOs

3.2 PCI Express Interfaces

The RDK provides 15 PCI Express connectors and two x4 PCI Express External Cable Connectors for PCI Express connections of PEX 8619. The RDK supports 6 different port configurations of PEX 8619. With the correct port configuration STRAP pin settings and the right Configuration Modules are installed, the RDK can demonstrate up to 16 ports and a up to x8 link upstream connection PCI Express Gen 2 switch. Table 1 shows all port configurations supported by the RDK while sections 3.2.1 to 3.2.5 describe the Configuration Modules and hardware configurations of grouped of each four PCI Express lanes in details.

Table 1. Port Configurations Supported by the RDK

Strap pin Settings STRAP_PORTCFG[3:0]	**Port Configurations**	**Configuration Modules Used ***
0000	x1x1x1x1x1x1x1x1x1x1x1x1x1x1x1x1	0108 at U74;0108 at U75; and 0108 at U76
0001	x4x1x1x1x1x1x1x1x1x1x1x1	0107 at U74;0108 at U75; and 0108 at U76
0010	x4x4x1x1x1x1x1x1x1	0107 at U74;0108 at U75; and 0107 at U76
0011	x4x4x41x1x1x1	0107 at U74;0107 at U75; and 0107 at U76
0101	x8x1x1x1x1x1x1x1	0107 at U74;0109 at U75; and 0108 at U76
0110	x8x41x1x1x1	0107 at U74;0109 at U75; and 0107 at U76

*Note: * Three Configuration Modules may use for the RDK. They are "configuration Module 0107-0109"; U74, U75 and U76 are receptacles on the RDK for Configuration Modules to be installed*

3.2.1 RDK Configuration Modules and Their Receptacles

Each Configuration Module is a plug of a 200-pin board-to-board Mezzanine Connector assembled on a PCB. For the RDK, it is used to connect x4 link of PCI Express signals from PEX 8619 to one particular hardware connections. Only three Configuration Modules may be used on the PEX 8619BA base board RDK. These modules are labeled on their PCB silk screen as:

- Configuration Module 0107
- Configuration Module 0108
- Configuration Module 0109

On the RDK side, three receptacles of same Mezzanine Connectors are placed at U74, U75 and U76 where the Configuration Modules can be manually plugged in to complete the RDK PCI Express hardware configurations.

3.2.2 PCI Express Lane 0 to Lane 3

PCI Express lanes 0 - 3 of PEX 8619 are routed to the receptacle U74 as shown in Figure 4. When Configuration Module 0108 is plugged into U74 at Case (a), lanes 0-3 will be separately connected with a single line going to the following: PCI Express cable connector J5, PCI Express SLOT 1, PCI Express SLOT 2 and PCI Express SLOT 3. This results in x1 links to form port 0, 4, 6, and 8. When Configuration Module 0107 is plugged into U74 at Case (b), all four lanes will be connected to x4 PCI Express cable connector J5 to form a x4 link at port 0. Note that the PCIe signals to PCIe Cable Connector J5 can be an independent x4 port or the lower lanes of a x8 port.

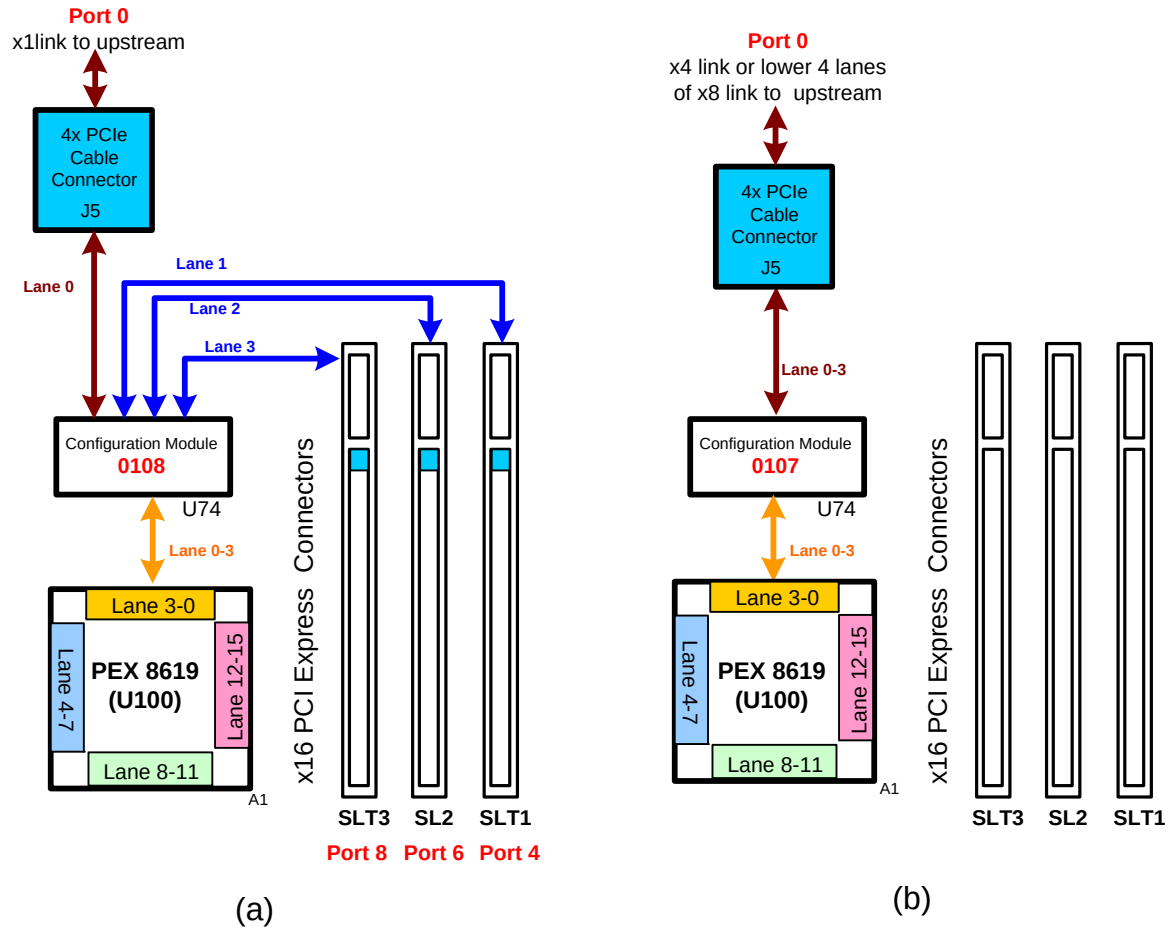


Figure 4. Lanes 0-3 Hardware Connections on the RDK

3.2.3 PCI Express Lane 4 to Lane 7

PCI Express lanes 4-7 of PEX 8619 are routed to the receptacle U75 as shown in Figure 5. When Configuration Module 0108 is plugged into U75 at Case (a), lanes 4-7 will be separately connected to PCI Express SLOT 4 to SLOT 7 with x1 link each to form ports 2, 10, 12, and 14. When Configuration Module 0107 is plugged into U75 at Case (b), four lanes will be connected to SLOT 4 to form a x4 link (port 4). When Configuration Module 0109 is plugged into U75 lane 4-7 will be connected to PCI Express cable connector J6 to form the upper four lanes of port 0 when port 0 is configured as a x8 port.

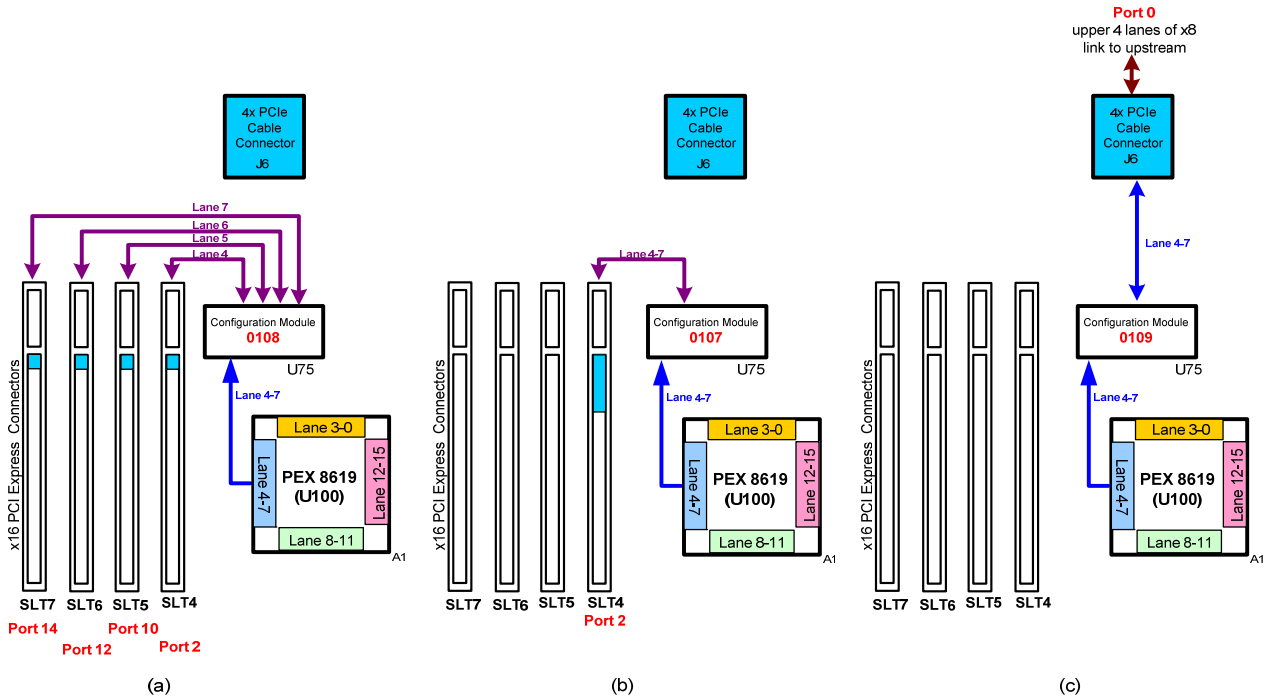


Figure 5. Lanes 4-7 Hardware Connections on the RDK

3.2.4 PCI Express Lane 8 to Lane 11

PCI Express lanes 8-11 of PEX 8619 are routed to the receptacle U76 as shown in Figure 6. When Configuration Module 0108 is plugged into U76 at Case (a), lanes 8-11 will be separately connected to PCI Express SLOT 8 to SLOT 11 with x1 link each to form ports 1, 5, 7, and 9. When Configuration Module 0107 is plugged into U76 at Case (b), four lanes will be connected to SLOT 8 to form a x4 link (port 1).

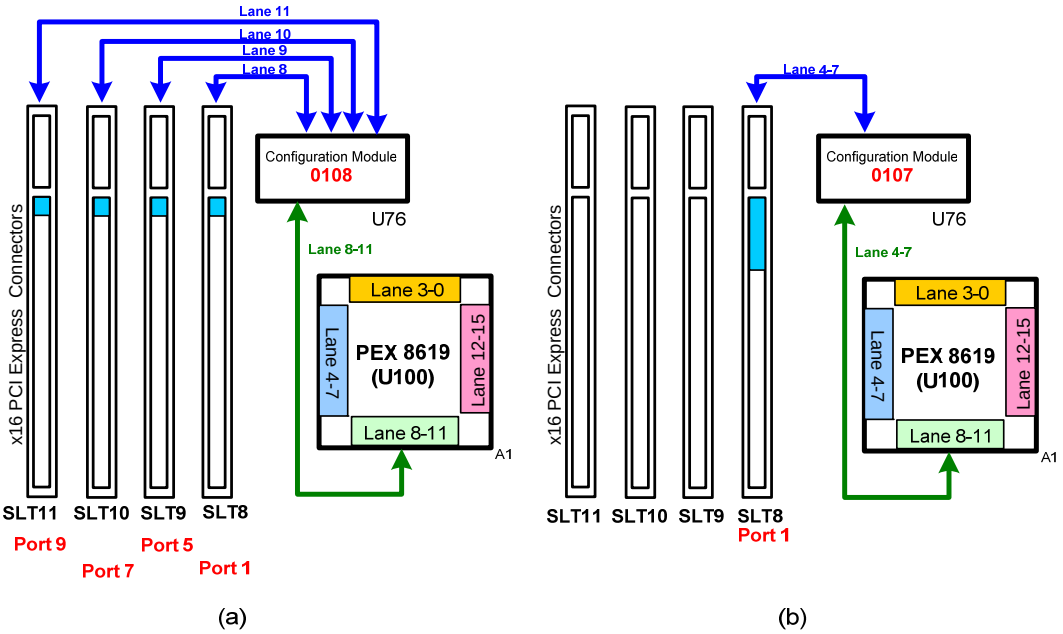


Figure 6. Lanes 8-11 Hardware Connections on the RDK

3.2.5 PCI Express lane 12 to lane 15

PCI Express lanes 12-15 of PEX 8619 are directly routed to PCI Express SLOT 12 to SLOT 15 with x1 link each to form ports 3, 11, 13 and 15, as shown in Figure 7, and a Configuration Module is not required.

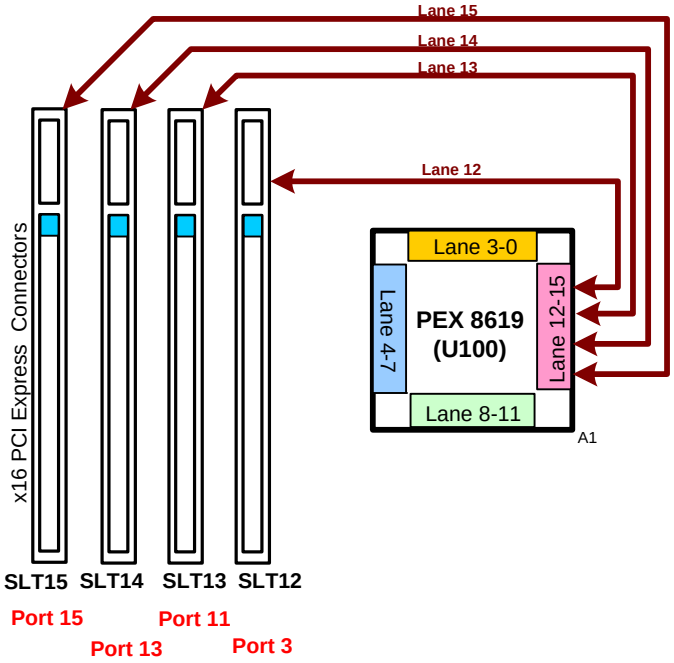


Figure 7. Lanes 12 – 15 Hardware Connections on the RDK

3.3 Reference Clock Circuits

The RDK reference clock circuits contain one crystal-to HCSL clock generator (U108) from On Semiconductor (NB3N5573), two one-to-four differential clock fan out buffer (U28 and U61) from SpectraLinear (CY28400-2), two 1-to-10 differential clock drivers (U113-U114) from On Semiconductor (MC100LVEP111), AC coupling capacitors, and resistors for source terminations and voltage dividers. The clock circuits are designed to perform two major clock functions: reference clock fan out and Spread-Spectrum Clock Isolation. Refer to Figure 8, the PCI Express clock (CREFCLKp and CREFCLKn) from x4 PCI Express External Cable Connector J5 feeds into 1-to-4 fan out buffer U28. The outputs from U28 support the primary REFCLK of the PEX 8619 and connect to the inputs of clock drivers U113 and U114. The Constant frequency output from the clock generator (U108) is connected to a 1-to-4 fan out buffer U61. The outputs from U61 support the input to CFC_REFCK on the PEX 8619 as well as inputs to U113 and U114. When Spread Spectrum Clocking Crossing is enabled, the PEX 8619 can be made part of two clock domains. Port 0 is part of the SSC domain while all on-board PCI Express SLOT 1 to SLOT 15 are part of the constant frequency domain. Add-in cards connected to SLOT1 – SLOT15 will operate in a constant frequency clock. The SSC isolation feature can be enabled with a pull-down resistor on STRAP_SSC_ISO_ENABLE# pin. On the RDK, this can be done in Dipswitch SW6 position 1 set to ‘ON’. This feature is disabled on the RDK by default.

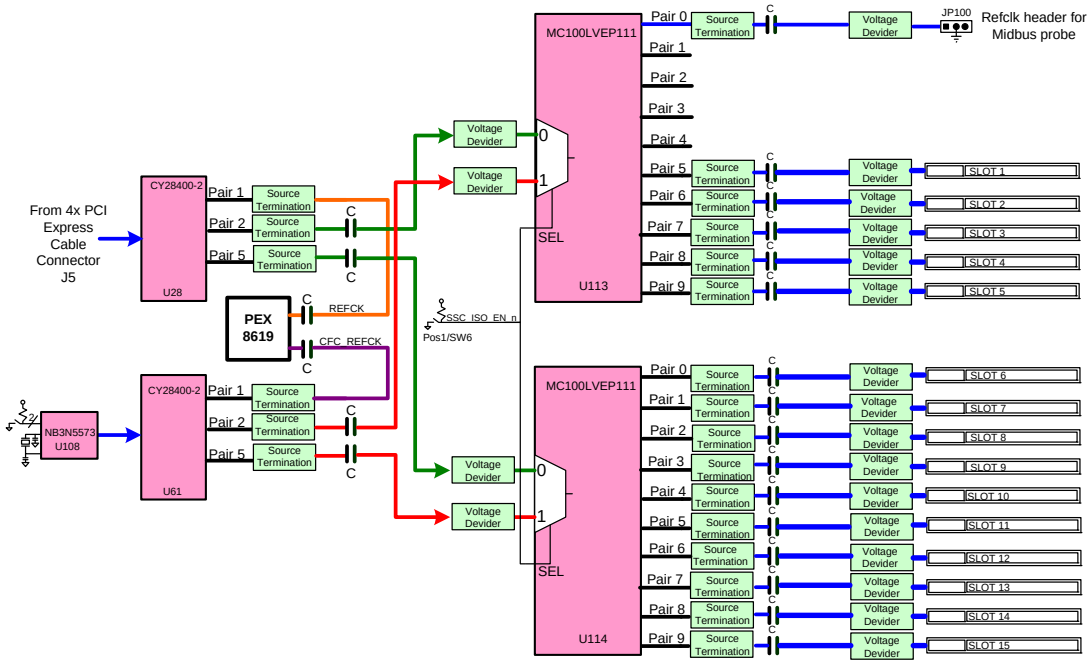


Figure 8. RDK Reference Clock Circuits

3.4 Reset Circuits

Refer to Figure 9, the RDK reset circuits include two National NC7S08 2-input AND gate (U17&U21), two Maxim MAX6420 reset controllers (U18 and U20), one Xilinx FPGA (U115), a Serial Hot-Plug controller, momentary switches (S1 and S3), resistors and capacitors.

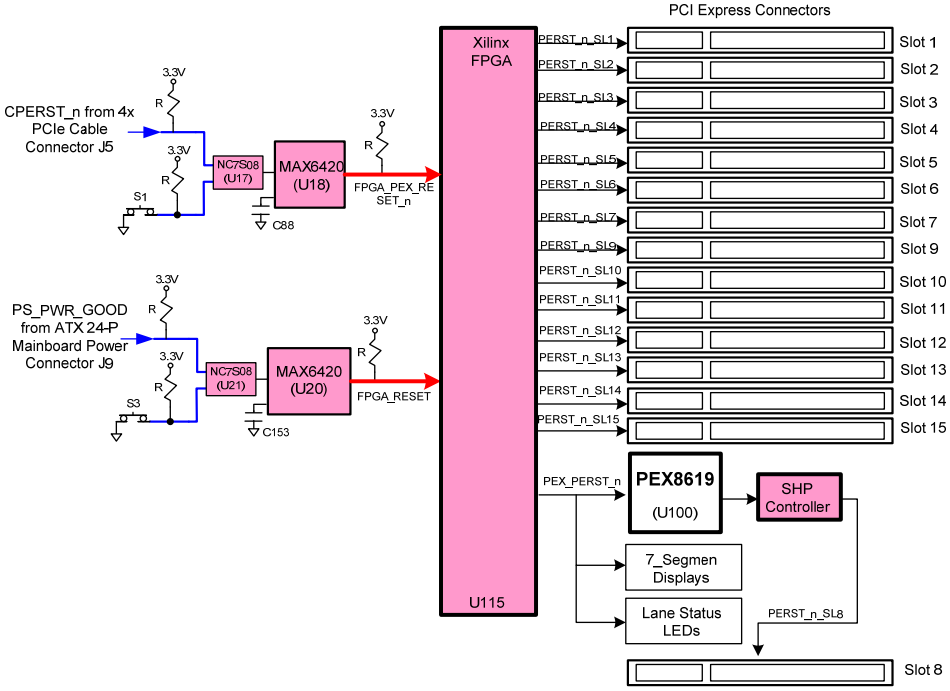


Figure 9. RDK Reset Circuits

The Reset Circuits contains two independent circuits: (a) the circuits reset the FPGA; (b) the circuits reset PEX 8619 and sends resets to 15 PCI Express connectors. The first one detect the power good signal, PS_PWR_GOOD, from the ATX 24-pin Main Power Connector and reset from momentary switch S3 to generate reset, FPGA_RESET, to the FPGA U115. The second detect the reset input, CPERST_n from the PCI Express Cable Connector J5 and the reset from momentary switch S1 input them to the FPGA that fans out the resets, PERST_n_SL[15:9, 7:1] , to 14 PCI Express slots, PEX_PERST_n to reset the PEX 8619, and PERST_n_SL8 to reset the PIC Express SLOT 8 through the Serial Hot-Plug Controller (see Figure 9 an Figure 10 for details)

3.5 Serial Hot-Plug (SHP) Controller Circuits

With external IO expenders and Hot-Plug controllers, PEX 8619 supports up to 16 PCI Express Serial Hot-Plug ports/ SLOTs. The RDK implements a serial Hot-Plug controller circuitry to PCI Express SLOT 8 for the SHP function demonstration. By default, the serial Hot-Plug circuit is enabled.

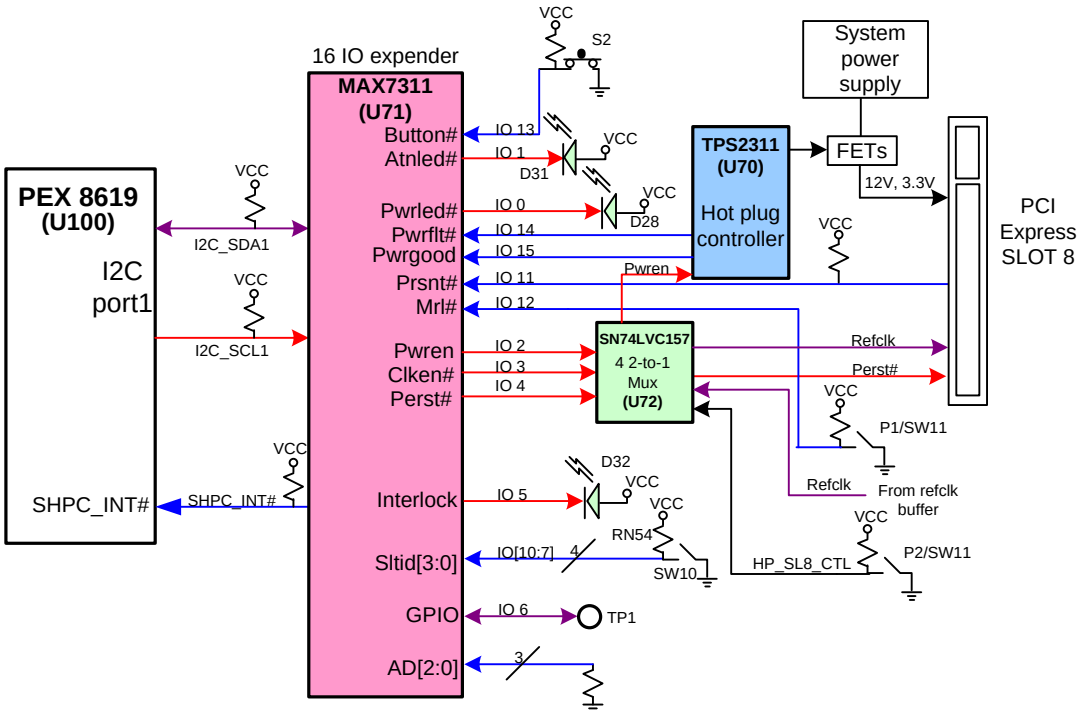


Figure 10. SERIAL HOT-PLUG Circuits

Refer to Figure 10 above, the serial Hot-Plug controller consists of MAX7311 I/O expander (U71), a TI TPS2311 dual hot–swap power controller (U70), a quad TI SN74LVC157 2-to-1 multiplexer (U72), two power MOSFET IRF7470 (Q1 and Q2), LEDs, manual switch, dipswitches and resistors. The PEX 8619 master I^2C interface is designed for the specific control use of the serial Hot-Plug controller. The master I^2C interface connected to the I/O expander and the interrupt output from the I/O expander connects to the SHP_INT# of the PEX 8619. When power is applied to the PEX 8619, the master I^2C interface will scan the bus and attempts to detect the presence of the I/O expander. If an I/O expander is detected, the I^2C master will program it as a “remote parallel Hot-Plug controller” and assign an available serial Hot-Plug port to the I/O expander. The IO expender then generates PWREN, CLKEN#, and PERST# outputs to control the power enable, clock enable# and reset# of the SHP SLOT8 and drives the LEDs at PWRLED#, ATNLED# and INTERLOCK# outputs. Also, it accepts BUTTON#, PWRFLT#, PWRGOOD, PRSNT# and MRL# inputs and generates interrupts to PEX 8619 for SHP status changes.

The RDK also provides dip switch (SW10) for setting the SLOTID [3:0]for the SLOT 8, and another dipswitch (SW11) to control the Serial Hot-Plug controller functions (enable/disable it), a test point for access the GPIO pin, and three pull-down resistors to set ADD [2:0] of the I/O expander U71. The LEDs D29 and D32 are 12V and 3.3V power indicators when power reaches PCI Express connector SLOT 82.

3.6 Serial EEPROM

The PEX 8619BA Base Board RDK contains a blank surface mount Atmel AT25256A 32-Kbit serial EEPROM (U19) which is directly interfaced to the PEX 8619. When programmed correctly, the serial EEPROM can be used to change the default configuration and internal register values of the PEX 8619. A blank EEPROM results in the default register values set in the PEX 8619. Refer to the Software Development Kit (SDK) documentation for more information of how to program the serial EEPROM.

3.7 I^2C Interface

The PEX 8619 implements an I^2C slave interface (I^2C port 0), which allows an external I^2C master to read and write device registers through an out-of-band mechanism. The PEX 8619 I^2C interface is accessible via a 7-bit address, at data rates from 100 Kbps up to 3.4 Mbps. The RDK provides a 2x2, 0.1" pitch header (JP8), which interface to the PEX 8619's I^2C port. This allows using standard ribbon cable, and/or connecting to an I^2C master such as Total Phase Aardvark I^2C controller. (See 4.3.10 for pin assignment of JP8.)

3.8 Power Distribution Circuits

To support the power of the RDK and the power of the PCI Express add-in cards plug into up to 15 PCI Express Edge Card connectors, an external ATX power supply is required. Refer to Figure 11, the RDK has 8 different ATX power connectors for power connections. These include one 24-pin ATX Main Power Connector J9, six 4-pin Peripheral Power Connectors J1- J4 & J7 - J8, and one 8-pin +12 V Power Connector.

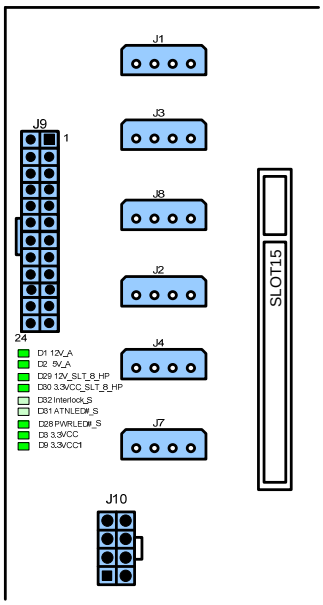


Figure 11. RDK ATX Power Connectors

The 24-pin ATX Power Connector should be connected to J9 and two or three 4-pin ATX Peripheral Power Connectors should be connected to either J1-J4 or J7-J8 depending on the power consumption requirements of the PCI Express add-in cards plugging into the PCI Express slots of the RDK.

Note Some 600 watt power supplies in the market such as the NSpire model PSH600V-D 600 Watt power supply requires a minimum power consumption at +12V output to stabilize its +5V outputs. Without 0.8A loading at +12V outputs, the NSpire 600 watt power supply will drop its +5V output to near 3.9V-4.2V levels. The RDK only uses +5V output from the ATX power supply to generated lower DC voltages to support the PEX 8619 chip and the on board FPGA and other circuits. This particular power supply does not operate correctly unless there is enough loading on the +12V supply. An Nvidia Geforce 8800GT high power graphic card can be plugged into one of PCI Express slots on the RDK in order to provide enough loading on the +12V supply.

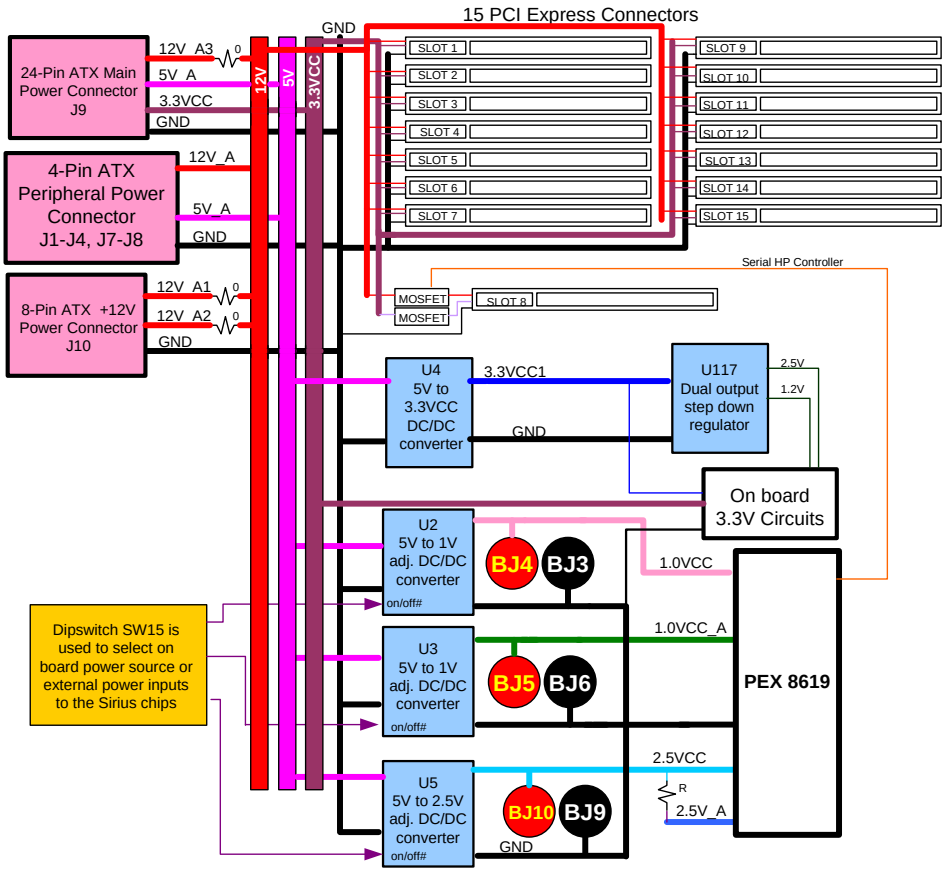


Figure 12. RDK Power Distribution Circuits

Refer to Figure 12, 15 PCI Express slots including the Serial Hot-Plug controlled SLOT 8 get 3.3 volt and 12 volt power from 24-pin ATX Main Power Connector, 4-pin ATX Peripheral Power Connectors and the +12V Power Connector. The RDK on board circuits and the PEX 8619 get their power from the +5V input from the ATX power supply. DC/DC converter U4 uses 5V input generates 3.3VCC1 to the on board circuit. The 3.3VCC1 further steps down by voltage regulator U117 to generate 2.5V and 1.2V for Xilinx FPGA (U115). Three dc/dc converters U2, U3 and U5 use 5V input to generate 1.0VCC, 1.0VCC_A and 2.5VCC for PEX 8619. Dip switch SW15 can be set to turn off these dc/dc converters for external power margin tests for PLX use only.

3.9 FPGA Interface

The RDK contains a Xilinx Spartan-3 FPGA which is used to perform 6 major functions (see Figure 13 for details):

- Connects to GPIOs, lane and chip status and spare pins of PEX 8619 (for PLX use only)
- Controls the 7-segment displays for port numbers and link width for PCI Express Cable Connectors J5 and J6 and PCI Express connectors SLOT 1 to SLOT15
- Decodes lane status and converts them to link speed and status LED display
- Communicates with the thermal sensor and displays the junction temperature of PEX 8619 in 4 digits
- Connects to users defined Dipswitches
- Fans out reset signals to PEX 8619 and PCI Express slots

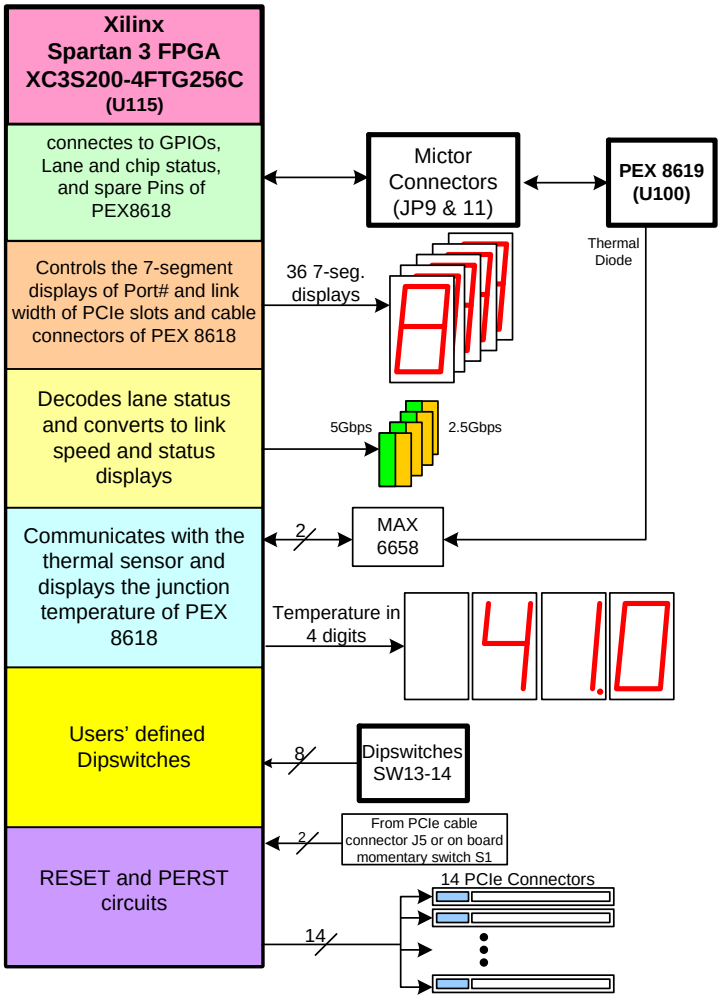


Figure 13. FPGA Interface on RDK

3.10 LED and 7-Segment Displays

The RDK provides 31 LEDs and forty 7-segment displays for power indicators, Hot-Plug output indicators, link speed/status, port numbers and link width of each port.

3.10.1 LED Indicators

All LED indicators and their associated functions are described in the Table 2 below.

Table 2. RDK LED Indicator descriptions

Indicator Type	Locations	LED Functions
Power LEDs/green color	D1	On: 12V_A is applied to the RDK from the ATX power supply
	D2	On: 5V_A is applied to the RDK from the ATX power supply
	D3	On: 3.3VCC is applied to the RDK from the ATX power supply
	D9	On: 3.3VCC1 from dc/dc converter U4
	D4	On: 2.5VCC_A is applied to PEX 8619
	D5	On: 2.5VCC is applied to PEX 8619
	D6	Power LED for 1.0VCC_A (did not work)
	D7	Power LED for 1.0VCC (did not work)

Indicator Type	Locations	LED Functions
Power LEDs/dual color: green and red	D8	Green LED on: 2.5VCC to PEX 8619 is within 10% range Red LED on: 2.5VCC to PEX 8619 is out of 10% range
	D10	Green LED on: 1.0VCC to PEX 8619 is within 10% range Red LED on: 1.0VCC to PEX 8619 is out of 10% range
SERIAL HOT-PLUG (SHP) LEDs/green color	D28	On: SHP power LED output active at SLOT 8
	D29	On: 12V is applied to PCI Express SLOT 8
	D30	On: 3.3V is applied to PCI Express SLOT 8
	D31	On: SHP Attention LED output active at SLOT 8
	D32	On: SHP Interlock LED output active at SLOT 8
Port Link Status and Speed LEDs / Dual color: green and yellow	D12	Green LED on: port 0 link up with GEN 2 speed (5Gbps) at connector J5 Yellow LED on: port 0 link up with GEN 1 speed (2.5Gbps) at connector J5 Both LED off: port 0 link down or no connected or no configured
	D16	Same function as D12 for port 4 at SLOT1
	D20	Same function as D12 for port 6 at SLOT2
	D24	Same function as D12 for port 8 at SLOT3
	D13	Same function as D12 for port 2 at SLOT4
	D17	Same function as D12 for port 10 at SLOT5
	D21	Same function as D12 for port 12 at SLOT6
	D25	Same function as D12 for port 14 at SLOT7
	D14	Same function as D12 for port 1 at SLOT8
	D18	Same function as D12 for port 5 at SLOT9
	D22	Same function as D12 for port 7 at SLOT10
	D26	Same function as D12 for port 9 at SLOT11
	D15	Same function as D12 for port 3 at SLOT12
	D19	Same function as D12 for port 6 at SLOT13
	D23	Same function as D12 for port 13 at SLOT14
	D27	Same function as D12 for port 15 at SLOT15

3.10.2 7-Segment Displays

The RDK has forty 7-segment displays. Thrity-four of them are used for port number and link width indicators of each PCI Express SLOTs, two are user defined 7-segment displays, and four of them are used for junction temperature display. (See Table 3 for details).

Table 3. RDK 7-Segment Display Functions

Location of Display	7-Segment Display Functions
DS37	For port 0 at cable connector J5, When enabled, LED display is 0
DS39	Link Width of port0, LED display is 1, 4 or 8 depending on the port configuration
DS33	Copy DS37 if cable connector J6 is used. Otherwise it would be off
DS35	Copy DS39 if cable connector J6 is used. Otherwise it would be off
DS2	For port 4 at SLOT1, When enabled, LED display is 4
DS6	Link Width of port 4, When enabled, LED display is 1
DS9	For port 6 at SLOT2, When enabled, LED display is 6
DS13	Link Width of port 6, When enabled, LED display is 1
DS1	For port 8 at SLOT3, When enabled, LED display is 8
DS5	Link Width of port 8, When enabled, LED display is 1

Location of Display	7-Segment Display Functions
DS12	For port 2 at SLOT4, When enabled, LED display is 2
DS16	Link Width of port 2, LED display is 1 or 4 depending on the port configuration
DS4	For port 10 at SLOT5, When enabled, LED display is A
DS8	Link Width of port 10, When enabled, LED display is 1
DS11	For port 12 at SLOT6, When enabled, LED display is C
DS15	Link Width of port 12, When enabled, LED display is 1
DS3	For port 14 at SLOT7, When enabled, LED display is E
DS7	Link Width of port 14, When enabled, LED display is 1
DS26	For port 1 at SLOT8, When enabled, LED display is 1
DS30	Link Width of port 1, LED display is 1 or 4 depending on the port configuration
DS18	For port 5 at SLOT9, When enabled, LED display is 5
DS22	Link Width of port 5, When enabled, LED display is 1
DS25	For port 7 at SLOT10, When enabled, LED display is 7
DS29	Link Width of port 7, When enabled, LED display is 1
DS17	For port 9 at SLOT11, When enabled, LED display is 9
DS21	Link Width of port 9, When enabled, LED display is 1
DS28	For port 3 at SLOT12, When enabled, LED display is 3
DS32	Link Width of port 3, When enabled, LED display is 1
DS20	For port 6 at SLOT13, When enabled, LED display is 6
DS24	Link Width of port 6, When enabled, LED display is 1
DS27	For port 13 at SLOT14, When enabled, LED display is 13
DS31	Link Width of port 13, When enabled, LED display is 1
DS19	For port 15 at SLOT15, When enabled, LED display is F
DS23	Link Width of port 15, When enabled, LED display is 1
DS10 and DS14	Users' defined 7-segment displays
DS34, DS36, DS38, DS40	Used to display junction temperature of PEX 8619BA in degree C

3.11 GPIO Pins

The PEX 8619 has thirty-two GPIO pins. Depends on the TEST MODE pin settings, 16 of them, GPIO[15:0], can be configured to perform Serial Hot-Plug reset output functions (PERSTx#).

3.12 Reserved Pins

The PEX 8619 has 2 STRAP_RESERVED pins. They are factory use only and should be set to know logic states. Table 4 shows the list of these reserved pins and their connections in the RDK.

Table 4. Strap_Reserved Pin Connections

Name	Pin Location	Connections on PEX 8619BA Base Board RDK
STRAP_RESERVED16	D14	Pull-down with a 1K ohm resistor
STRAP_RESERVED17#	F1	Pull-up with a 4.7K ohm resistor

4. On-Board Connectors, Switches, and Jumpers

4.1 DIP Switches

The PEX 8619BA Base Board RDK contains eleven DIP switches for various functions. Refer to Figure 14; they can be divided into three groups. The Group1 contains three dip switches and is located at the lower left corner of the RDK, Group2 contains three dip switches and is located at the middle of right edge, and the last group contains five dip switches and is located at the lower right hand corner of the RDK

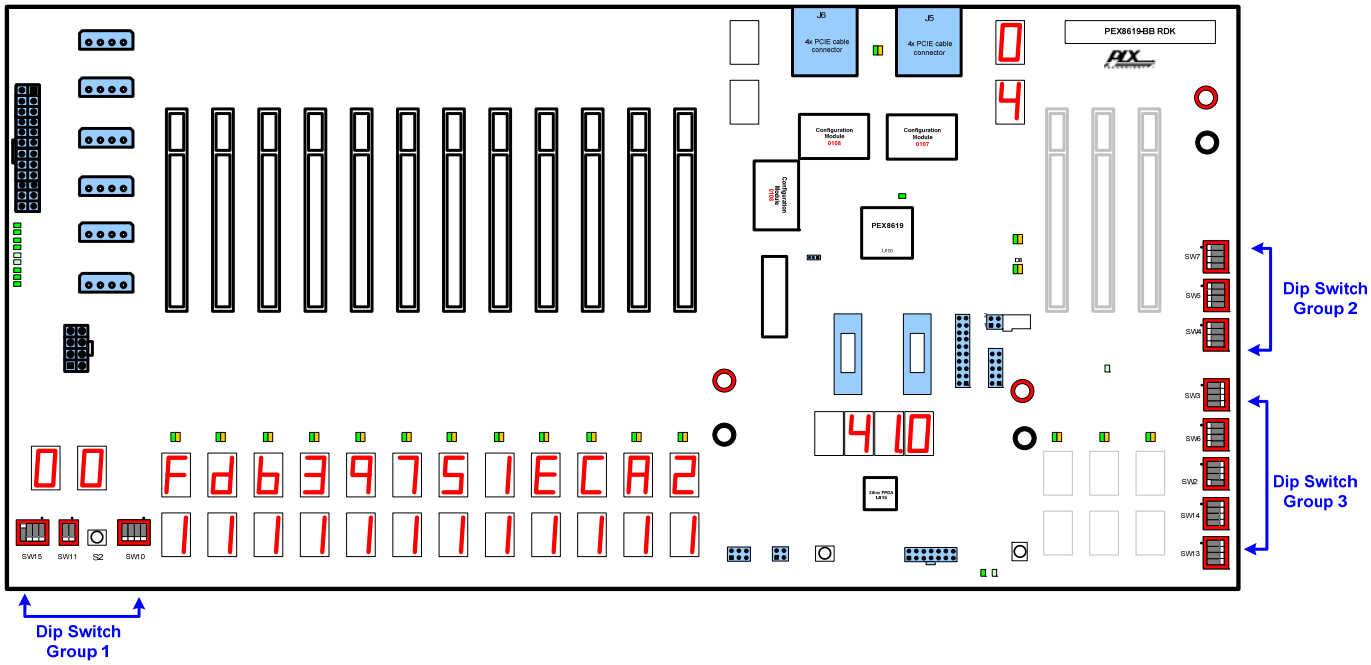


Figure 14. RDK Dip Switch Groups

4.1.1 Dip Switch Group 1

This group includes three dipswitches, SW10, SW11 and SW15. Figure 15 shows the default settings of these dipswitches and Table 5 describes the functions of each dipswitches

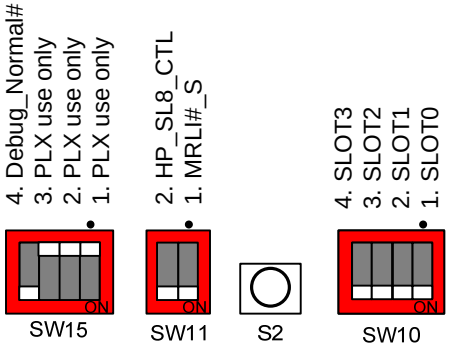


Figure 15. Group1 of Switches

Table 5. Functional Description of Group 1 Dip Switches

Name	Function	Settings
SW10	Slot number of Serial Hot-Plug port PCIe connectro SPLT8	Default: on, on, on, on (0000) 4: SLOT 3 3: SLOT 2 2: SLOT 1 1: SLOT 0
SW11	Serial Hot-Plug Port input and control	2. HP_SL8_CTL : on: enable Serial Hot-Plug (SHP) control outputs—PWREN_S, PERST#_S and CLKEN#_S; off: bypass above SHP control ouputs 1. MRLI#_S: on: enable SHP MRL# input; off: disable it Default: on,on (enable SHP functions at SLOT 8)
SW15	Debug function and dc/dc converter controls	4: Debug_normal_#: on : for normal operation; off: for debug us 3-1: for PLX use only Default: on, off,off,off

4.1.2 Dip Switch Group 2

This group includes three dipswitches, SW4, SW5 and SW7. Figure 16 shows the default settings of these dipswitches and Table 6 describes the functions of each dipswitches

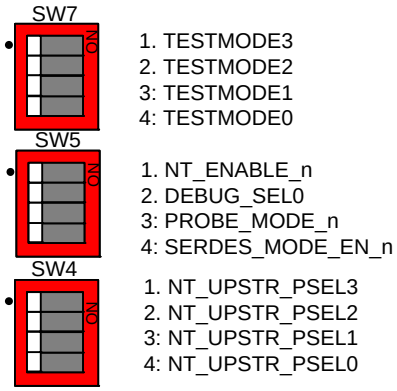


Figure 16. Group 2 of Dipswitches

Table 6. Functional Description of Group 2 Dip Switches

<table>
<tr><th>Name</th><th>Function</th><th>Settings</th></tr>
<tr><td>SW4</td><td>NT Upstream Port Selects</td><td>
<table>
<tr><th>NT_UPSTR_PSEL[3:0]</th><th>Port #</th></tr>
<tr><td>on,on,on,on</td><td>0</td></tr>
<tr><td>on,on,on,off</td><td>1</td></tr>
<tr><td>on,on,off,on</td><td>2</td></tr>
<tr><td>on,on,off,off</td><td>3</td></tr>
<tr><td>on,off,on,on</td><td>4</td></tr>
<tr><td>on,off,on,off</td><td>5</td></tr>
<tr><td>on,off,off,on</td><td>6</td></tr>
<tr><td>on,off,off,off</td><td>7</td></tr>
<tr><td>off,on,on,on</td><td>8</td></tr>
<tr><td>off,on,on,off</td><td>9</td></tr>
<tr><td>off,on,off,on</td><td>10</td></tr>
<tr><td>off,on,off,off</td><td>11</td></tr>
<tr><td>off,off,on,on</td><td>12</td></tr>
<tr><td>off,off,on,off</td><td>13</td></tr>
<tr><td>off,off,off,on</td><td>14</td></tr>
<tr><td>off,off,off,off</td><td>15</td></tr>
</table>
</td></tr>
<tr><td>SW5</td><td>NT port and debug mode enables</td><td>1. NT_ENABLE_n : on: enable NT mode, off: disable NT mode, default disable NT mode
2. DEBUG_SEL0: for PLX use only
3: PROBE_MODE_n: for PLX use only
4. SERDES_MODE_EN_n: for PLX use only

Default: 1-4: off,off,off,off</td></tr>
<tr><td>SW7</td><td>Test Mode selects</td><td>1. TESTMODE3: for PLX use only
2: TESTMODE2: for PLX use only
3. TESTMODE1: for PLX use only
4: TESTMODE0: for PLX use only

Default: 1-4: off,off,off,off</td></tr>
</table>

4.1.3 Dip Switch Group 3

This group includes five dipswitches, SW2, SW3, SW6, SW13 and SW14. Figure 17 shows the default settings of these dipswitches. Table 7 and Table 8 describe the functions of them.

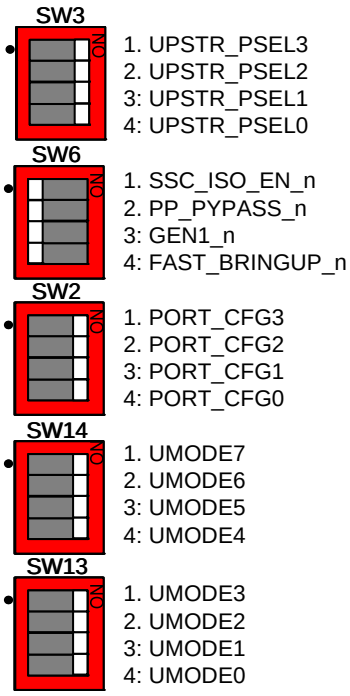


Figure 17. Group 3 of Dip Switches

Table 7. Port Configurations use Dipswitch SW2

Dipswitch Settings for STRAP_PORTCFG[3:0]	**Port Configurations**
ON,ON,ON,ON (0000)	x1x1x1x1x1x1x1x1x1x1x1x1x1x1x1
ON,ON,ON,OFF (0001)	x41x1x1x1x1x1x1x1x1x1x1x1
ON,ON,OFF,ON (0010)	x4x41x1x1x1x1x1x1x1
ON,ON,OFF,OFF (0011)	x4x4x41x1x1x1
ON, OFF,ON,OFF (0101)	x8x1x1x1x1x1x1x1x1
ON,OFF,OFF,ON (0110)	x8xx41x1x1x1

Table 8. Functional Descriptions of SW3, SW6, SW13-SW14

<table>
<tr><th>Name</th><th>Function</th><th>Settings</th></tr>
<tr><td>SW3</td><td>Upstream Port Selects</td><td>
<table>
<tr><th>UPSTR_PSEL[3:0]</th><th>Port #</th></tr>
<tr><td>on,on,on,on</td><td>0</td></tr>
<tr><td>on,on,on,off</td><td>1</td></tr>
<tr><td>on,on,off,on</td><td>2</td></tr>
<tr><td>on,on,off,off</td><td>3</td></tr>
<tr><td>on,off,on,on</td><td>4</td></tr>
<tr><td>on,off,on,off</td><td>5</td></tr>
<tr><td>on,off,off,on</td><td>6</td></tr>
<tr><td>on,off,off,off</td><td>7</td></tr>
<tr><td>off,on,on,on</td><td>8</td></tr>
<tr><td>off,on,on,off</td><td>9</td></tr>
<tr><td>off,on,off,on</td><td>10</td></tr>
<tr><td>off,on,off,off</td><td>11</td></tr>
<tr><td>off,off,on,on</td><td>12</td></tr>
<tr><td>off,off,on,off</td><td>13</td></tr>
<tr><td>off,off,off,on</td><td>14</td></tr>
<tr><td>off,off,off,off</td><td>15</td></tr>
</table>
</td></tr>
<tr><td>SW6</td><td>Other Mode Selects</td><td>1. SSC_ISO_EN_n : on: enable the Spread Spectrum Clocking (SSC) crossing, off: disable it, default is disable SSC crossing function
2. PP_PYPASS_n: for PLX use only
3: GEN 1_N: for PLX use only
4. FAST_BRINGUP_n: for PLX use only

Default: 1-4: off,off,off,off</td></tr>
<tr><td>SW13</td><td>Users Define Mode Switches</td><td>1. UMODE3
2: UMODE2
3. UMODE1
4: UMODE0

Default: 1-4: off,off,off,off</td></tr>
<tr><td>SW14</td><td>Users Define Mode Switches</td><td>1. UMODE7
2: UMODE6
3. UMODE5
4: UMODE4

Default: 1-4: off,off,off,off</td></tr>
</table>

4.2 Push-Button Switches

4.2.1 Manual Reset# (S1)

The RDK provides a manual switch (S1) for manual PERST# capability. Note that manual PERST# will only apply warm reset to the PEX 8619 as well as PCI Express SLOT 1 to SLOT 15.

4.2.2 FPGA Manual Reset# (S2)

This momentary switch (S2) provides manual reset to the FPGA (U115) on the RDK.

4.2.3 Serial Hot-Plug Controller Attention Button (S3)

The RDK provides a manual switch (S3) for attention button to the Serial Hot-Plug circuit. When pushed and released, the switch generates an active low pulse to the Attention Button Input to the IO Expender U71 which will generate interrupt signal, INT#, to the PEX 8619 for attention (see section 3.5 for details).

4.3 Connectors and Headers

4.3.1 ATX Peripheral Power Connectors (J1-J4 & J7-J8)

The RDK has six ATX Peripheral Power Connectors.

Table 9. Signal Names of J1-J4 & J7-J8

Pin #	Signal Name
1	12V
2	GND
3	GND
4	5V

4.3.2 x4 PCI Express External Cable Connectors (J5 & J6)

The RDK has two x4 PCI Express External Cable Connectors.

Table 10. Signal Names of J5 and J6

Pin #	Signal Name	Pin #	Signal Name
A1	GND	B1	GND
A2	PETp0	B2	PERp0
A3	PETn0	B3	PERn0
A4	GND	B4	GND
A5	GND	B5	PERp1
A6	PETp1	B6	PERn1
A7	PETn1	B7	GND
A8	GND	B8	PERp2
A9	PETp2	B9	PERn2
A10	PETn2	B10	GND
A11	GND	B11	PERp3
A12	PETp3	B12	PERn3
A13	PETn3	B13	GND
A14	GND	B14	PWR
A15	CREFCLKp	B15	PWR
A16	CREFCLKn	B16	PWR_RTN
A17	GND	B17	PWR_RTN
A18	SB_RTN	B18	CWAKE#
A19	CPWRON	B19	CPERST#

4.3.3 ATX Main Power Connector (J9)

Table 11. Signal Names of J9

Pin #	Signal Name	Pin #	Signal Name
1	+3.3VDC	13	+3.3VDC
2	+3.3VDC	14	-12VDC
3	COM	15	COM
4	+5VDC	16	PS_ON#
5	COM	17	COM
6	+5VDC	18	COM
7	COM	19	COM
8	PWR_OK	20	-5VDC
9	+5VSB	21	+5VDC
10	+12VDC	22	+5VDC
11	+12VDC	23	+5VDC
12	+3.3VDC	24	COM

4.3.4 ATX +12V Power Connector(J10)

Table 12. Signal Names of J10

Pin #	Signal Name	Pin #	Signal Name
1	COM	13	+12VDC
2	COM	14	+12VDC
3	COM	15	+12VDC
4	COM	16	+12VDC

4.3.5 Xilinx JTAG Connector (J12)

Table 13. Signal Names of J12

Pin #	Signal Name	Pin #	Signal Name
1	VREF to 2.5V	2	GND
3	SS_PROG_TMS	4	GND
5	SCLK_CCLK_TCK	6	GND
7	MISO_DONE_TDO	8	GND
9	MOSI_DIN_TDI	10	GND
11	NC	12	GND
13	NC_INIT_NC	14	DNG

4.3.6 Xilinx Mode Setting Header (J13)

Table 14. Signal Names of J13

Pin #	Signal Name	Pin #	Signal Name
1	GND	2	M0
3	GND	4	M1
5	GND	6	M2

4.3.7 PEX 8619 JTAG Header (JP3)

The 2x5 header JP3 provides a direct connection to the PEX 8619 JTAG interface. The 10-pin connector is designed to allow a direct interface to 3rd party JTAG controllers, such as the Corelis USB-1149.1/E controller. The pin assignment for the JTAG header (JP3) is listed at Table 15.

Table 15. Pin assignment of JP3

Pin #	Signal Name	Pin #	Signal Name
1	JTAG_TRST	2	GND
3	JTAG_TDI	4	GND
5	JTAG_TDO	6	GND
7	JTAG_TMS	8	GND
9	JTAG_TCK	10	GND

4.3.8 SMBus Header (JP5)

This header is for PLX use only

Table 16. Signal Names of JP5

Pin #	Signal Name	Pin #	Signal Name
1	SMBCLK	2	GND
3	SMBDATA	4	NC

4.3.9 PCI Express x8 Midbus Probe Footprint (JP6)

Table 17. Signal Names of JP6

Pin #	Signal Name	Pin #	Signal Name
		G1	GND
2	GND	1	C0p-Upstream
4	C0p-Downstream	3	C0n-Upstream
6	C0n-Downstream	5	GND
8	GND	7	C1p-Upstream
10	C1p-Downstream	9	C1n-Upstream
12	C1n-Downstream	11	GND
14	GND	13	C2p-Upstream
16	C2p-Downstream	15	C2n-Upstream

Pin #	Signal Name	Pin #	Signal Name
18	C2n-Downstream	17	GND
20	GND	19	C3p-Upstream
22	C3p-Downstream	21	C3n-Upstream
24	C3n-Downstream	23	GND
26	GND	25	C4p-Upstream
28	C4p-Downstream	27	C4n-Upstream
30	C4n-Downstream	29	GND
32	GND	31	C5p-Upstream
34	C5p-Downstream	33	C5n-Upstream
36	C5n-Downstream	35	GND
38	GND	37	C6p-Upstream
40	C6p-Downstream	39	C6n-Upstream
42	C6n-Downstream	41	GND
44	GND	43	C7p-Upstream
46	C7p-Downstream	45	C7n-Upstream
48	C7n-Downstream	47	
G2	GND		

4.3.10 PEX 8619 I²C Port (JP8)

Table 18. Pin assignment of JP8

Pin Number	Signal Name
1	I2C_SCL0
2	GND
3	I2C_SDA0
4	NC

4.3.11 Debug Signal Header (JP9 & JP11)

This is for PLX use only.

Table 19. Pin assignment of JP9 & JP11

Pin #	Signal Name at JP9	Signal Name at JP11
1	-	-
3	GND	GND
5	-	NC
7	GPIO16	DEBUG_SEL0
9	GPIO17	STRAP_UPCFG_TIMER_EN#
11	GPIO18	STRAP_SMBUS_EN#
13	GPIO19	STRAP_SPARE0#
15	GPIO20	UPSTRM_PSEL3
17	GPIO21	GPIO29
19	GPIO22	GPIO30

Pin #	Signal Name at JP9	Signal Name at JP11
21	GPIO23	I2C_ADDR2
23	GPIO24	STRAP_SPARE5#
25	GPIO25	GPIO6
27	GND	GPIO7
29	-	GPIO8
31	-	GPIO26
33	-	GPIO27
35	-	STRAP_NT_P2P_EN#
37	-	GND
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND
2	-	-
4	-	-
6	-	-
8	LN_GOOD_00_n	GPIO0
10	LN_GOOD_01_n	GPIO1
12	LN_GOOD_02_n	GPIO2
14	LN_GOOD_03_n	GPIO3
16	LN_GOOD_04_n	GPIO4
18	LN_GOOD_05_n	GPIO5
20	LN_GOOD_06_n	I2C_ADDR0
22	LN_GOOD_07_n	I2C_ADDR1
24	LN_GOOD_08_n	STRAP_SPARE1#
26	LN_GOOD_09_n	GPIO9
28	LN_GOOD_10_n	GPIO10
30	LN_GOOD_11_n	GPIO11
32	LN_GOOD_12_n	GPIO12
34	LN_GOOD_13_n	GPIO13
36	LN_GOOD_14_n	GPIO14
38	LN_GOOD_15_n	GPIO15

4.3.12 Debug Input Header (JP10)

This is for PLX use only.

Table 20. Pin assignment of JP10

Pin #	Signal Name	Pin #	Signal Name
1	GND	2	STRAP_SPARE1#
3	I2C_ADDR2	4	I2C_ADDR1
5	GPIO30	6	I2C_ADDR0
7	GPIO29	8	GND
9	UPSTRM_PSEL3	10	GPIO5
11	STRAP_SPARE0#	12	GPIO4
13	GND	14	GPIO3
15	STRAP_SMBUS_EN#	16	GPIO2
17	STRAP_UPCFG_TIMER_EN#	18	GPIO1
19	DEBUG_SEL0	20	GPIO0

4.3.13 Reference Clock Header (JP100)

Table 21. Pin assignment of JP100

Pin Number	Signal Name
1	LAI_Refclk_p
2	GND
3	LAI_Refclk_n

5. RDK Port Configurations

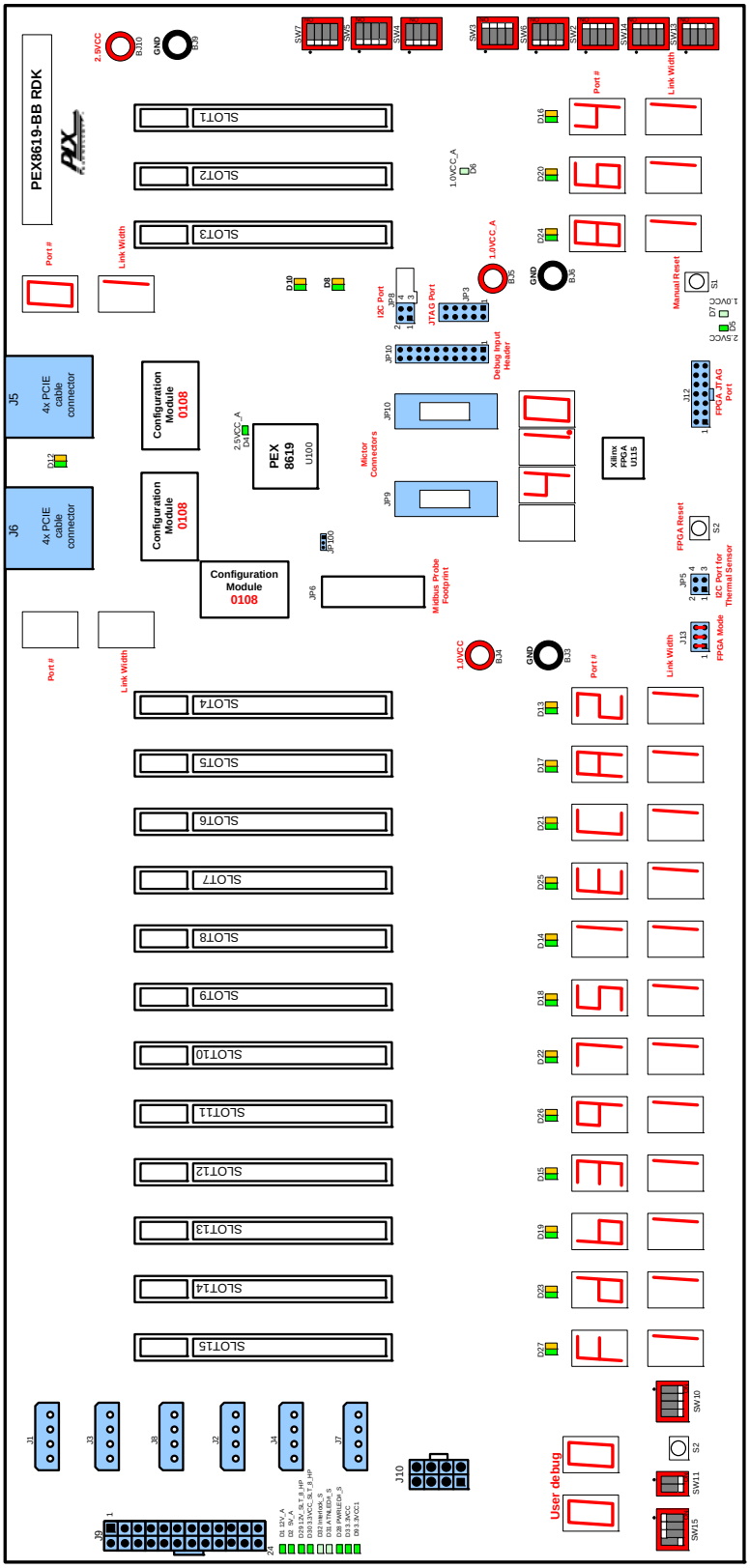


Figure 18. x1 upstream and 15x1 downstream (PCFG=0000)

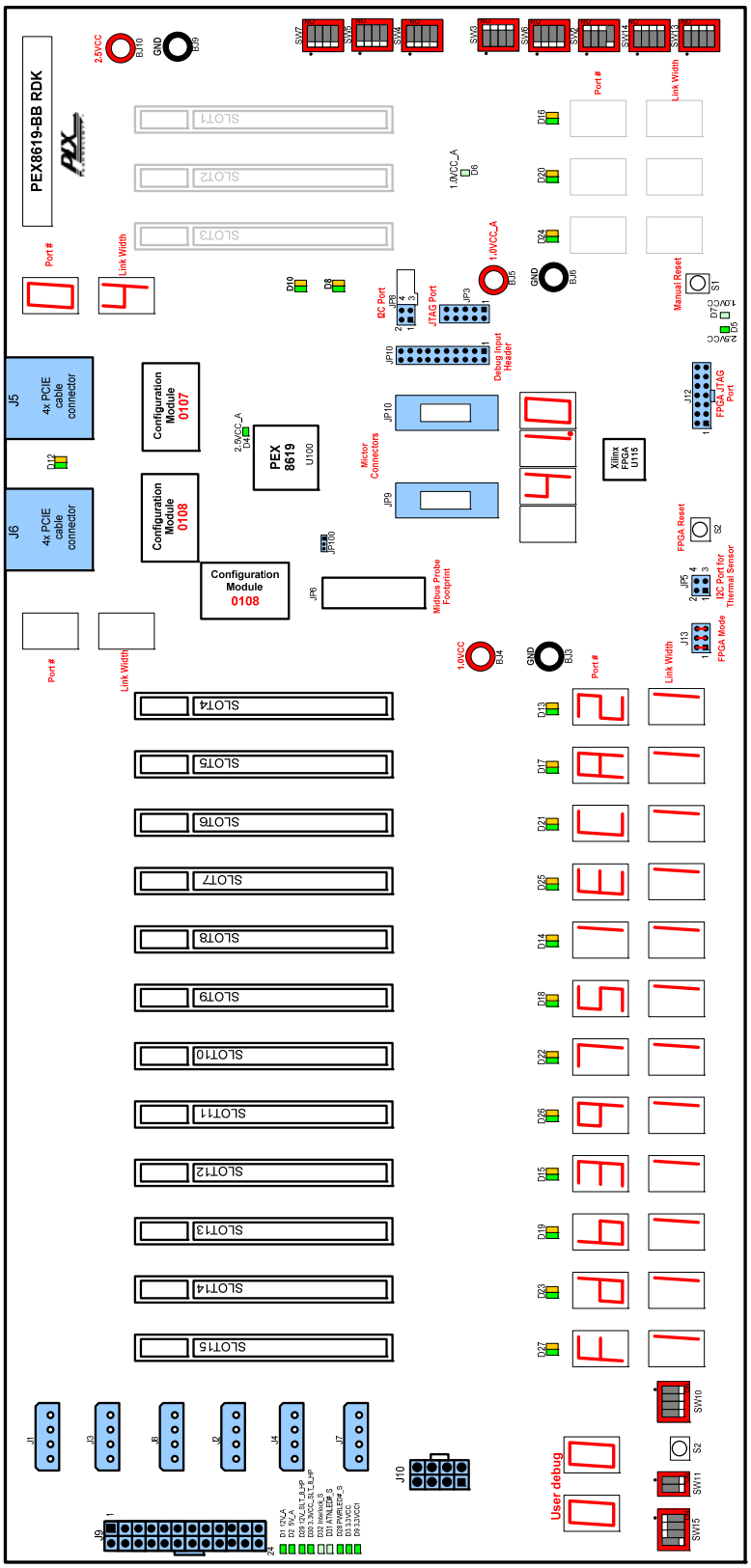


Figure 19. x4 upstream 12x1 downstream (PCFG=0001)

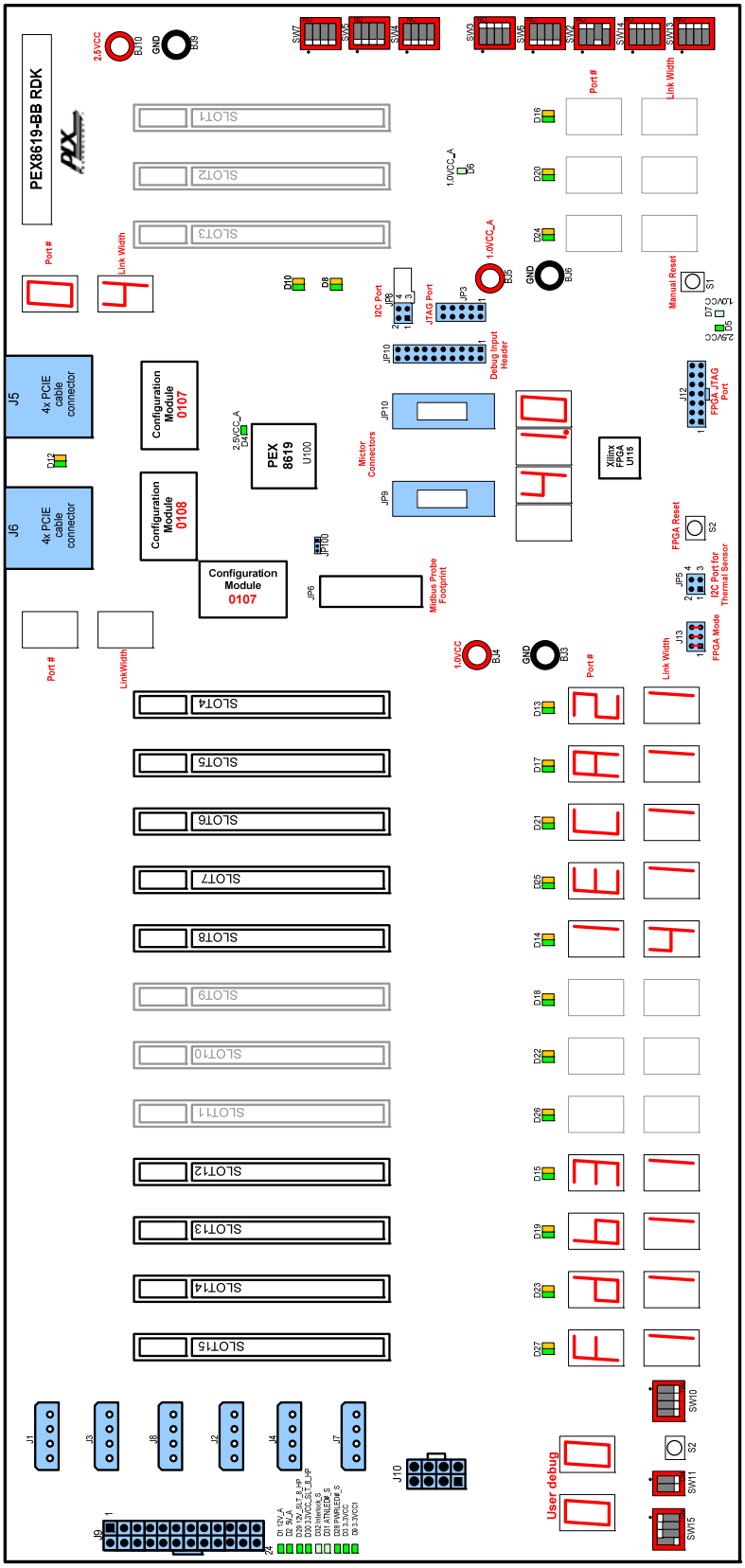


Figure 20. x4 upstream, 1x4 and 8x1 downstream (PCFG=0010)

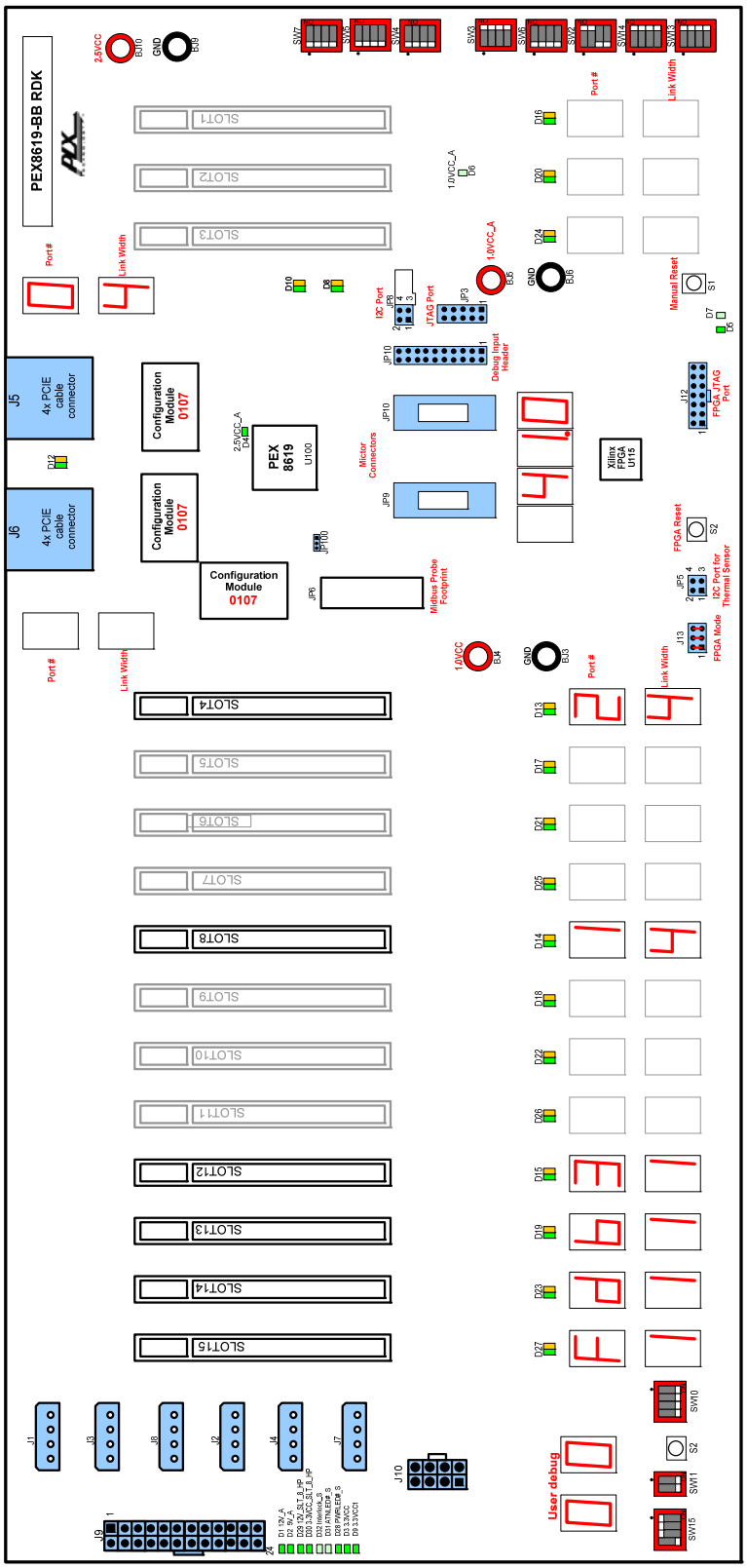


Figure 21. x4 upstream, 2x4 and 4x1 downstream (PCFG=0011)

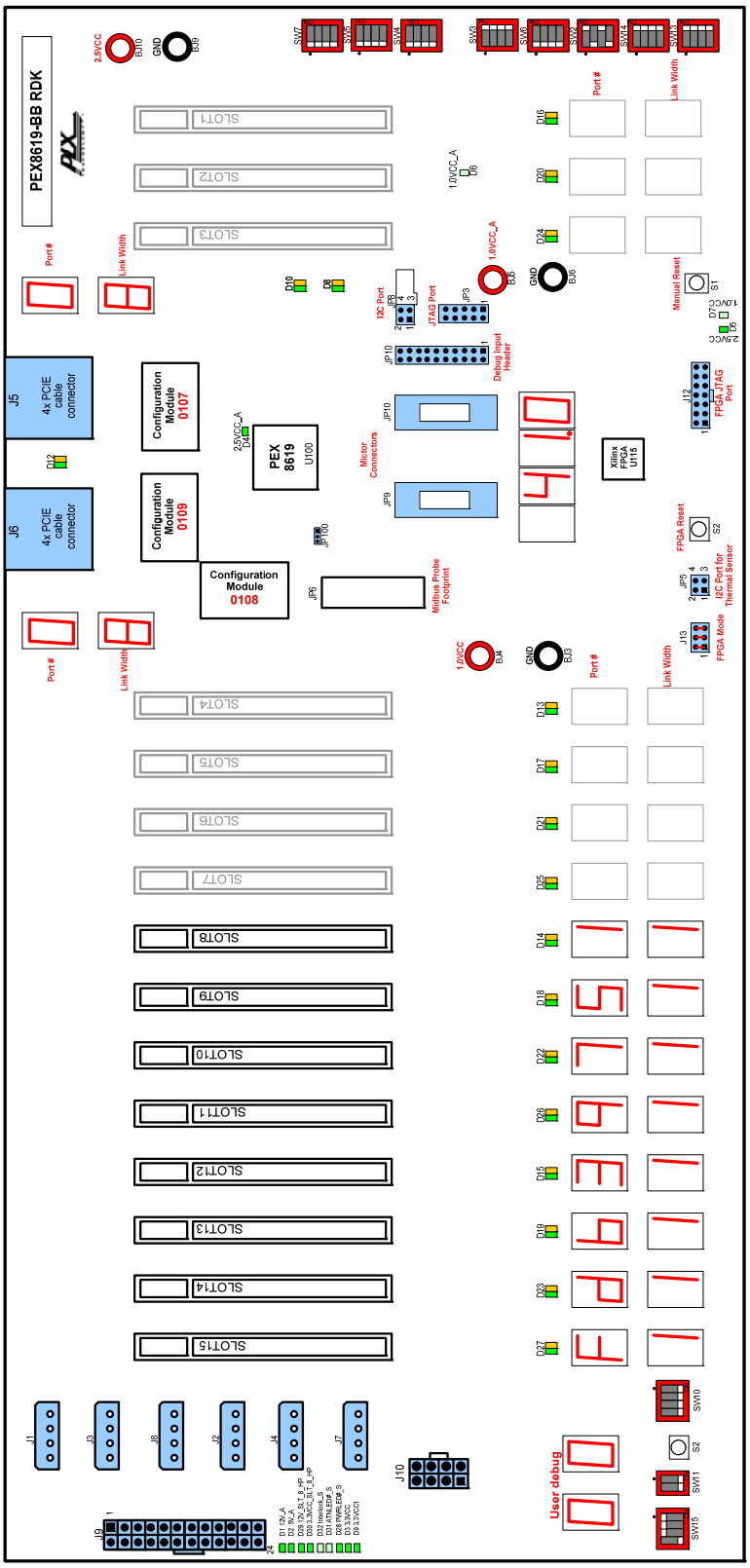


Figure 22. x8 upstream, 8x1 downstream (PCFG=0101)

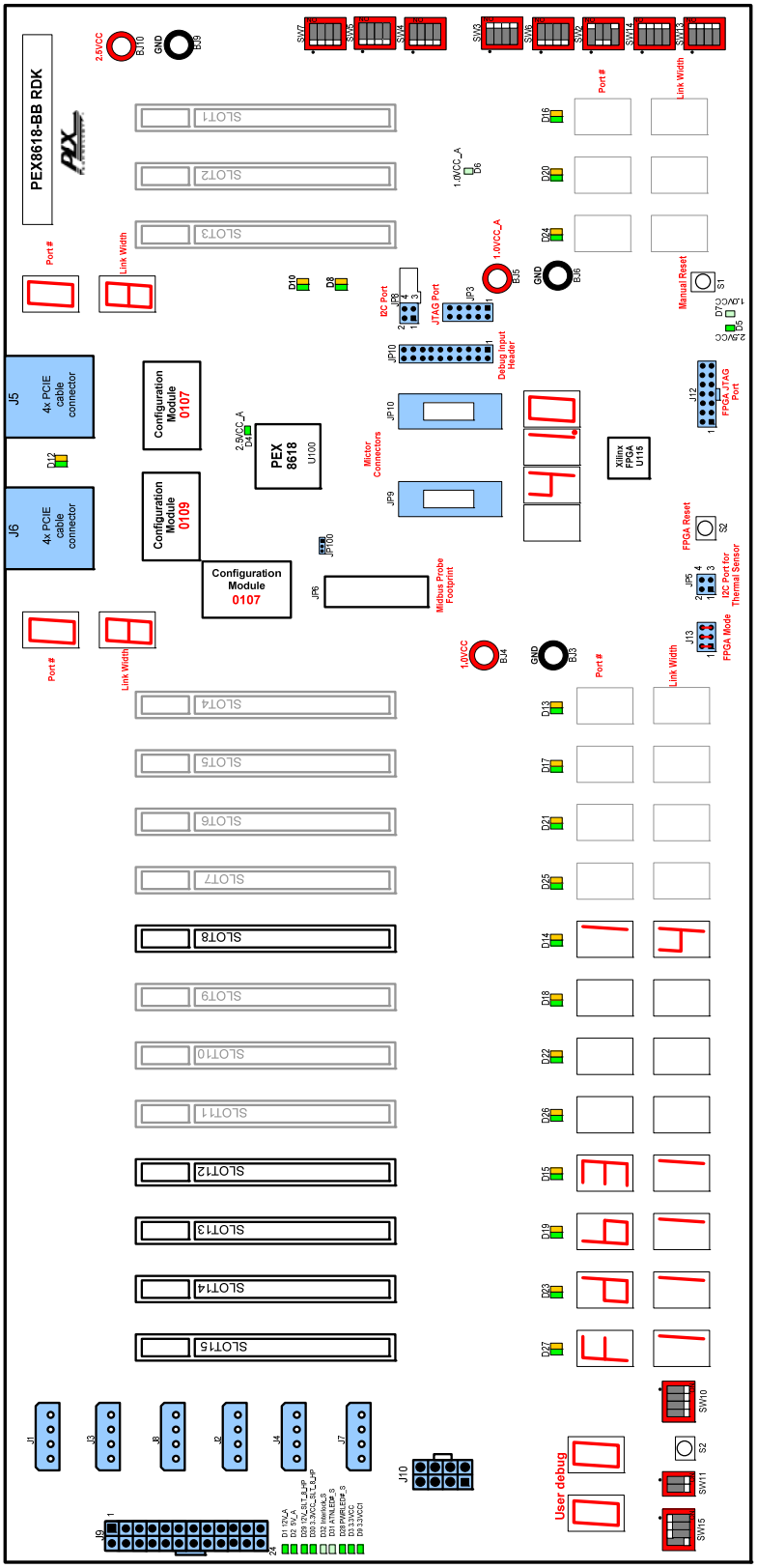


Figure 23. x8 upstream, 1x4 and 4x1 downstream (PCFG=0110)

6. Bill of Materials/ Schematics

Item #	Qty	Man.	Man. Part #	Description	Package Type	Component Designator(s)
SURFACE MOUNT COMPONENTS						
1	1	PLX	PEX8619-BA50BC G	IC, 16 lane 16 port PCIe gen2 switch with DMA, 19x19mm	BGA, 324-pin, full matrix, 1mm ball pitch	U100
2	4	BEL	S7AH-08E1A0.	Non-iso DC/DC converter, 5Vin/0.9-3.3Vout @8A	SMT, 7-pin	U2, U3, U4, U5
3	1	Intersil	ISL6132IR	IC, multiple voltage monitor	SMT, QFN-24	U16
4	2	National	NC7S08M5X	IC, 2-input AND gate	SMT, SOT23-5	U17, U21
5	2	MAXIM	MAX6420UK16-T	IC, Reset controller, Adj. reset timeout	SMT, SOT23-5	U18, U20
6	1	ATMEL	AT25256AN-10SU-2.7	IC, SPI Serial EEPROM	SMT, SO-8	U19
7	2	SpectralLinear/Cypress	CY28400OXC-2	IC, 100MHz Differential Clock Buffer	SMT, SSOP-28	U28, U61
8	44	Fairchild	MM74HC164MX	IC, 8-bit serial in/parallel-out shift register	SMT, SO14	U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U62, U63, U64, U65, U66, U67, U68, U69, U83, U84, U88, U89
9	1	MAXIM	MAX7311AUG	IC, 2-wire-interface 16-bit I/O Port Expander with Interrupt	SMT, TSSOP-24	U71
10	1	Texas	TPS2311IPW	IC, dual hot-swap power controller	SMT, TSSOP-20	U70
11	1	Texas	SN74LVC157APW	IC, Quad 2-to-1 data selector/multiplexer	SMT, TSSOP-16	U72
12	1	MAXIM	MAX6658MSA	IC, SMBus-compatible temperature sensor	SMT, SO-8	U78
13	5	NXP SEMI	SN74LVC04AD	IC, hex inverter	SMT, SO-14	U80, U85, U87, U91, U92
14	1	On Semiconductor	NB3N5573DTG	IC, crystal to HCSL clock generator, 3.3V	SMT TSSOP-16	U108
15	2	On Semiconductor	MC100LVEP111FAG	IC, 1:10 differential ECL/PECL/HSTL clock driver, 2.5/3.3V	SMT, QFP-32	U113, U114
16	1	Xilinx	XC3S200-4FTG256C	IC, Spartan-3 FPGA, 4ns, 173 I/Os, 256-pin, 1mm pitch,	SMT, 256-pin BGA	U115
17	1	Xilinx	XCF01SVOG20C	IC, 1Mbit platform flash PROM	SMT, TSSOP-20	U116
18	1	Maxim	MAX8833ETJ+	IC, dual 3A step-down regulator	SMT, QFN-32	U117
19	2	International Rectifier	IRF7470PBF	IC, N-channel MOSFET, 40V/10A 13mohm	SMT, SO-8	Q1, Q2
20	11	Lumex	SML-LXT0805GW-TR	LED, green color	SMT, 0805	D1, D2, D3, D4, D5, D9, D28, D29, D30, D31, D32
21	2	CML Innovative Technologies	7016X1/5	LED, dual color, green/red	SMT, 4-pin	D8, D10
22	16	CML Innovative Technologies	7016X5/7	LED, dual color, genn/yelow	SMT, 4-pin	D12, D13, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D27
23	1	Citizen	HCM49 25.000MABJ-UT	CRYSTAL, 25.000 MHz, 18pF load capacitor	SMT	Y2
24	1	ECS Inc	ECS-3953M-1000-AU	OSC, 100.000 MHZ 3.3V SMD	SMT	Y4
25	2	Panasonic	ELL-6SH1R0M	Inductor, 1.0UH 20% 3.4A,	SMT	L2, L3
26						
27	3	FCI	84517-101LF	Connector, 10x20, Receptacle	SMT	U74, U75, U76
28	2	Molex	75586-0011	Connector, receptacle, right angle receptacle, 0.8mm pitch for PCIE 4x cable,	SMT 38-pin connector	J5, J6

Item #	Qty	Man.	Man. Part #	Description	Package Type	Component Designator(s)
30	15	CTS	742C083472JTR	Resistor Network, 4.7K ohm 4R isolated	SMT, 8-pin	RN1, RN4, RN5, RN6, RN7, RN8, RN9, RN10, RN11, RN13, RN54, RN55, RN58, RN59, RN60
31	40	Panasonic	EXB-2HV221JV	Resistor Network, 220 ohm 8R isolated	SMT, 16-pin	RN14, RN15, RN16, RN17, RN18, RN19, RN20, RN21, RN22, RN23, RN24, RN25, RN26, RN27, RN28, RN29, RN30, RN31, RN32, RN33, RN34, RN35, RN36, RN37, RN38, RN39, RN40, RN41, RN42, RN43, RN44, RN45, RN46, RN47, RN48, RN49, RN50, RN51, RN52, RN53
32	1	CTS	742C083103JTR	Resistor Network 10K ohm 4R isolated	SMT, 8-pin	RN56
33	1	CTS	742C083102JTR	Resistor Network, 1K ohm 4R isolated	SMT, 8-pin	RN3
34	5	ROHM	MCR10EZHJ000	RES. 0.0 OHM 5%	SMT, 0805	R10, R59, R61, R62, R269
35	2	Panasonic	ERJ-6ENF2001V	RES. 2.00K OHM 1%	SMT, 0805	R262, R263
36	1	Panasonic	ERJ-6ENF2002V	RES. 20.0K OHM 1%	SMT, 0805	R251
37	3	Yageo	RC0805FR-07374RL	RES. 374 OHM 1%	SMT, 0805	R29, R30, R34
38	1	Panasonic	ERJ-6ENF4701V	RES. 4.70K OHM 1%	SMT, 0805	R268
39	12	Panosonic	ERJ-3GEY0R00V	RES. ZERO OHM 5%	SMT, 0603	R277, R285, R286, R287, R311, R314, R315, R339, R340, R344, R407, R408
40	40	Panasonic	ERJ-3GEYJ102V	RES. 1K OHM 5%	SMT, 0603	R434, R435, R436, R437, R438, R439, R440, R441, R442, R443, R444, R445, R446, R447, R448, R505, R506, R507, R508, R509, R511, R512, R513, R514, R515, R516, R517, R518, R519, R520, R521, R522, R523, R524, R525, R526, R527, R528, R529, R510
42	40	Panasonic	ERJ-3GEYJ121V	RES. 120 OHM 5%	SMT, 0805	R530, R531, R532, R533, R534, R535, R536, R537, R538, R539, R540, R541, R542, R543, R544, R545, R546, R547, R548, R549, R550, R551, R552, R553, R554, R555, R556, R557, R558, R559, R560, R561, R562, R563, R564, R565, R566, R567, R568, R569
43	2	Panasonic	ERJ-3GEYJ4R7V	RES. 4.7 OHM 5%	SMT, 0603	R293, R320
44	12	Panasonic	ERJ-3GEYJ512V	RES. 5.1K OHM 5%	SMT, 0603	R307, R308, R309, R310, R312, R313, R334, R335, R336, R337, R338, R374
45	48	Panasonic	ERJ-3GEYJ103V	RES 10K OHM 1%	SMT, 0603	R449, R454, R455, R456, R457, R458, R459, R460, R465, R466, R467, R468, R469, R470, R471, R472, R473, R474, R475, R476, R477, R478, R479, R480, R481, R482, R483, R484, R485, R486, R487, R488, R489, R490, R491, R492, R493, R494, R495, R496, R497, R498, R499, R500, R501, R502, R503, R504
46	4	Panasonic	ERJ-3EKF1431V	RES 1.43K OHM 1%	SMT, 0603	R281, R282, R283, R284
47	1	Panasonic	ERJ-3EKF2000V	RES 200 OHM 1%	SMT, 0603	R278
48	2	Panasonic	ERJ-3EKF2261V	RES 2.26K OHM 1%	SMT, 0603	R42, R44
49	3	Panasonic	ERJ-3EKF4750V	RES 475 OHM 1%	SMT, 0603	R79, R292, R319
50	1	Panasonic	ERJ-3EKF4990V	RES 499 OHM 1%	SMT, 0603	R28
51	9	Yageo	RC0603FR-075K1L	RES 5.10K OHM 1%	SMT, 0603	R60, R64, R70, R71, R72, R77, R78, R80, R81

Item #	Qty	Man.	Man. Part #	Description	Package Type	Component Designator(s)
52	8	Panasonic	ERJ-3EKF7321V	RES 7.32K OHM 1%	SMT, 0603	R450, R451, R452, R453, R461, R462, R463, R464
53	36	Panasonic	ERJ-S02F3900X	RES 390 OHM **5%**	SMT, 0402	R49, R50, R53, R54, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R232, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247
54	27	Panasonic	ERJ-2GEJ472X	RES 4.7K OHM 5%	SMT, 0402	R9, R33, R35, R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R259, R260, R265, R266, R270, R271, R272, R273, R274
55	3	Panasonic	ERJ-2RKF1001X	RES 1.00K OHM 1%	SMT, 0402	R254, R257, R258
56	1	Yageo	RM04F1001CTLF	RES 1K 1%	SMT, 0402	R350
57	3	Panasonic	ERJ-2RKF1002X	RES 10.0K OHM 1%	SMT, 0402	R58, R67, R351
58	3	Yageo	RM04F1002CTLF	RES 10K 1%	SMT, 0402	R348, R349, R359
59	1	Panasonic	ERJ-2RKF1003X	RES 100K OHM 1%	SMT, 0402	R248
60	1	Yageo	RM04F10R0CTLF	RES 10.0 OHM 1%	SMT, 0402	R346
61	1	Panasonic	ERJ-2RKF1181X	RES 1.18K OHM 1%	SMT, 0402	R41
62	3	Panasonic	ERJ-2RKF1201X	RES 1.21K OHM 1%	SMT, 0402	R1, R12, R252
63	1	Panasonic	ERJ-2RKF1242X	RES 12.4K OHM 1%	SMT, 0402	R249
64	1	Panasonic	ERJ-2RKF1372X	RES 13.7K OHM 1%	SMT, 0402	R250
65	3	Panasonic	ERJ-2RKF1500X	RES 150 OHM 1%	SMT, 0402	R253, R255, R256
66	1	Yageo	RM04F2000CTLF	RES 200 OHM 1%	SMT, 0402	R347
67	1	Yageo	RM04F2001CTLF	RES 2K OHM 1%	SMT, 0402	R14
68	4	Yageo	RM04F2002CTLF	RES 20K 1%	SMT, 0402	R352, R355, R356, R357
69	1	Panasonic	ERJ-2RKF2321X	RES 2.32K OHM 1%	SMT, 0402	R47
70	1	Panasonic	ERJ-2RKF3091X	RES 3.09K OHM 1%	SMT, 0402	R37
71	1	Panasonic	ERJ-2RKF3161X	RES 3.16K OHM 1%	SMT, 0402	R358
72	21	Yageo	RC0402FR-0733RL	RES 33.0 OHM 1%	SMT, 0402	R63, R65, R289, R291, R297, R299, R300, R301, R302, R306, R316, R318, R324, R326, R327, R328, R329, R333, R341, R342, R353
73	1	Yageo	RT0402FRE07360RL	RES 360 OHM 1%	SMT, 0402	R2
74	2	Panasonic	ERJ-2RKF3652X	RES 36.5K OHM 1%	SMT, 0402	R7, R11
75	1	Panasonic	ERJ-2RKF4640X	RES 464 OHM 1%	SMT, 0402	R43
76	1	Yageo	ERJ-2RKF4991X	RES 4.99K 1%	SMT, 0402	R354
77	18	Panasonic	ERJ-2RKF49R9X	RES 49.9 OHM 1%	SMT, 0402	R73, R74, R290, R294, R295, R296, R298, R303, R304, R305, R317, R321, R322, R323, R325, R330, R331, R332

Item #	Qty	Man.	Man. Part #	Description	Package Type	Component Designator(s)
78	2	Panasonic	ERJ-2GEJ513X	RES 51K OHM **1%**	SMT, 0402	R57, R66
79	1	Yageo	RT0402FRE0751RL	RES 51.1 OHM 1%	SMT, 0402	R267
80	1	Panasonic	ERJ-2RKF5761X	RES 5.76K OHM 1%	SMT, 0402	R45
81	1	Panasonic	ERJ-2RKF7321X	RES 7.32K OHM 1%	SMT, 0402	R38,
82	2	Panasonic	ERJ-M1WSF20MU	RES 0.02 OHM 1W 1%	SMT, 2512	R261, R264
83	1	Yageo	9C06031A7321FKHFT	Res. 7.32K ohm, 1/10W 1%	SMT, 0603	R343
84	1	Yageo	9C06031A1001FKHFT	Res. 1.0K ohm 1/10W 1%	SMT, 0603	R345
85	2	Panasonic	ERJ-2GEJ203X	Res. 20K ohm 1/16W 5%	SMT, 0402	R360-R361
90	11	Panasonic	ECJ3YB1C106M	CAP 10uF 16V 20% X5R	SMT, 1206	C42, C45, C47, C64, C67, C315, C319, C320, C326, C336, C339
91	1	CALCHIP	ECJ-2VC1H151J	CAP 150pf 50V 5% NPO	SMT, 0805	C160
92	1	CALCHIP	ECJ-2VC1H331J	CAP 330pf 50V 5% NPO	SMT, 0805	C80
93	2	Panasonic	ECJ-2VB1H102K	CAP 1000pf 50V 10% X7R	SMT, 0805	C79, C82
94	8	Kemet	GMC21X7R104K50NT	CAP 0.1 uf 50V 10% X7R	SMT, 0805	C72, C73, C74, C76, C78, C83, C86, C157
95	32	CALCHIP	GMC21X7R105K16NT-LF	CAP 1UF10% 16V X5R	SMT, 0805	C1, C2, C6, C8, C10, C12, C13, C16, C19, C20, C21, C24, C25, C26, C27, C28, C44, C46, C48, C63, C65, C71, C161, C257, C296, C298, C301, C302, C305, C306, C308, C310
96	2	Kemet	GMC21X5R106M6R3NT	CAP 10uf 6.3V 20% X5R	SMT, 0805	C75, C84
97	1	CALCHIP	08055C223KAT2A	CAP 0.022uf 50V 10% X7R	SMT, 0805	C163
98	1	CALCHIP	GMC21X5R226M6R3NT	CAP 22uf 6.3V 20% X5R	SMT, 0805	C156
99	1	AVX	06033A180GAT2A	CAP 18PF 25V NP0	SMT, 0603	C327
100	1	AVX	0603YA220JAT2A	CAP 22PF 16V NP0	SMT, 0603	C328
101	24	Kemet	C0603C105K8PACTU	CAP 1.0UF 10V 10% X5R	SMT, 0603	C89, C90, C91, C92, C93, C94, C95, C98, C121, C122, C123, C124, C125, C126, C127, C128, C389, C391, C392, C393, C395, C396, C412, C423
102	47	AVX	04026C102KAT2A	CAP 1000PF 50V X7R	SMT, 0402	C88, C153, C105, C108, C109, C110, C116, C117, C118, C120, C141, C145, C146, C148, C151, C259, C260, C334, C378, C379, C380, C381, C382, C383, C394, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C415, C416, C417, C418, C419, C420, C421, C422
103	72	Panasonic	ECJ-0EB1C103K	CAP 0.01uf 16V 10% X7R	SMT, 0402	C101, C102, C106, C107, C133, C137, C158, C159, C316, C317, C318, C321, C324, C325, C337, C338, C340, C341, C211, C212, C213, C214, C215, C216, C217, C218, C219, C220, C221, C222, C223, C224, C225, C226, C227, C228, C229, C230, C231, C232, C233, C234, C235, C236, C237, C238, C239, C240, C241, C242, C243, C244, C245, C246, C247, C248, C249, C250, C311, C312, C313, C314, C384, C385, C386, C387, C388, C390, C411, C413, C414, C424

Item #	Qty	Man.	Man. Part #	Description	Package Type	Component Designator(s)
104	97	Kemet	C0402C104K8PACTU	CAP 0.1UF 10V X5R	SMT, 0402	C85, C87, C154, C251, C252, C255, C256, C258, C261, C263, C264, C265, C266, C267, C268, C269, C270, C271, C272, C273, C274, C275, C276, C277, C278, C279, C280, C281, C282, C283, C284, C285, C286, C287, C288, C289, C290, C291, C292, C293, C294, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499
105	1	AVX	04023C222JAT2A	CAP 2200PF 25V X7R	SMT, 0402	C262
106	54	AVX	TAJC226K020R	CAP 22UF 20V 10% Tantalum	SMT, C Case	C3, C4, C5, C7, C9, C11, C14, C15, C17, C18, C22, C23, C29, C30, C31, C32, C181, C182, C183, C184, C185, C186, C187, C188, C189, C190, C191, C192, C193, C194, C195, C196, C197, C198, C199, C200, C201, C202, C203, C204, C205, C206, C207, C208, C209, C210, C295, C297, C299, C300, C303, C304, C307, C309
107	10	AVX	0201ZD103KAT2A	CAP 0.01UF 10% 10V X5R	SMT, 0201	C96, C97, C99, C100, C129, C130, C134, C135, C136, C138
108	20	Panasonic	ECJ-ZEB1E102K	CAP 1000PF 25V X7R	SMT, 0201	C103, C104, C111, C112, C113, C114, C115, C119, C131, C132, C139, C140, C142, C143, C144, C147, C149, C150, C152, C155
109	3	Vishay	594D187X0016R2T	CAP, 180UF 16V 20% Tantalum	SMT, D Case	C34, C35, C36
THROUGH-HOLE COMPONENTS						
200	40	Lumex	LDS-A516RI	7-SEGMENT display, red, common anode, 0.75"x0.48"	10-pin DIP	DS1, DS2, DS3, DS4, DS5, DS6, DS7, DS8, DS9, DS10, DS11, DS12, DS13, DS14, DS15, DS16, DS17, DS18, DS19, DS20, DS21, DS22, DS23, DS24, DS25, DS26, DS27, DS28, DS29, DS30, DS31, DS32, DS33, DS34, DS35, DS36, DS37, DS38, DS39, DS40
201	10	CK-Components	BD04	Switch, dipswitch, 4-POS Top Slide	8-pin TH	SW2, SW3, SW4, SW5, SW6, SW7, SW10, SW13, SW14, SW15
202	1	CK-Components	BD02	Switch, dipswitch, 2-POS Top Slide	4-pin TH	SW11
203	3	E Switch	TL1105F100Q	Switch, momentary E-switch, 6mm SQ,	4-pin TH	S1, S2, S3
204	1	Samtec	TMS-103-02-S-S	micro therninal strip, 1x3, Centerline:.050"	1x3 TH	JP100
205	6	Molex	15-24-4449	Connector, 4-pos straight ATX peripherial power connector	4-pin TH	J1, J2, J3, J4, J7, J8
206	2	Molex	74540-0400	Guide house, for 4x link PCIe external cable connector	TH	CAGE1 and CAGE2 for J5, J6
207	1	SULLINS	PBC05DAAN	HEADER, 5X2, 100mil	TH, 10-pin	JP3
208	2	SULLINS	PBC02DAAN	HEADER, 2X2, 100mil	TH, 4-pin	JP5, JP8
209	1	Sullins	PBC10DAAN	HEADER, 2X10, 100mil	TH, 20-pin	JP10
210	1	Sullins	PBC03DAAN	HEADER, 2X3, 100mil	TH, 6-pin	J13

Item #	Qty	Man.	Man. Part #	Description	Package Type	Component Designator(s)
211	1	Molex	39-28-1083	CONN, 2 X 4 straight locking 12V ATX power connector	TH, 8-pin	J10
212	1	Molex	44206-0001	Conn, ATX 24-pin Mainboard Power Connector	TH, 24-pin	J9
213	1	Molex	87831-1420	CONN, 2 X 7 straight shrouded, 2mm pitch	TH, 14-pin	J12
214	15	FCI	10018783-10003TLF	Conn. X16 PCIe card edge connector Vertical , 164-pin 1mm pitch	TH, 164-pin	SLOT1, SLOT2, SLOT3, SLOT4, SLOT5, SLOT6, SLOT7, SLOT8, SLOT9, SLOT10, SLOT11, SLOT12, SLOT13, SLOT14, SLOT15
MANUALLY INSERTED COMPONENTS						
300	3	Amp/Tyco	382811-6	Jumpers		JP13 (1-2,3-4,5-6)
MISCELLANEOUS COMPONENTS						
400	8	Olander	.2C5PPMS	Screw, M2 X 5MM PHIL PAN SST		XCAGE1, XCAGE2
401	12	3M	SJ5009(BLACK)	RUBBER BUMPER, .40 X .88 BLACK		Install at the bottom side of each board
402	1	PLX Technology	90-0104-000A	PCB, PEX8619 Base Board RDK		
PART THAT SHOULD NOT BE ASSEMBLED						
500	0	Concord Electronics	09-9127-1-0210	CONN, banana jack, black color	TH	BJ3, BJ6, BJ9
501	0	Concord Electronics	09-9127-1-0212	CONN, banana jack, red color	TH	BJ4, BJ5, BJ10
502	0	Agilent	E5387-68701	Midbus LAI 48-pin header shroud	TH	JP6
503	0	TBD	TBD	RES.	SMT, 2512	R15, R18, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R36, R39, R40, R46, R48, R51, R52, R55
504	0	Maxium	DS4100H+	IC, HCSL, OSC, 100MHz	SMT, 10-pin LCCC	U98
505	0	TBD	TBD	RES.	SMT, 0805	R4, R5, R13, R16
506	0	TBD	TBD	CAP.	SMT 0603	C253, C254
507	0	TBD	TBD	RES.	SMT, 0402	R75, R76
20	0	Lumex	SML-LXT0805GW-TR	LED, green color	SMT, 0805	D6, D7
65	0	Panasonic	ERJ-2RKF1500X	RES 150 OHM 1%	SMT, 0402	R31, R32
26	0	AMP	767054-1	Connector, 38-pin Mictor connector, vertical	SMT, vertical	JP9, JP11

NOTES

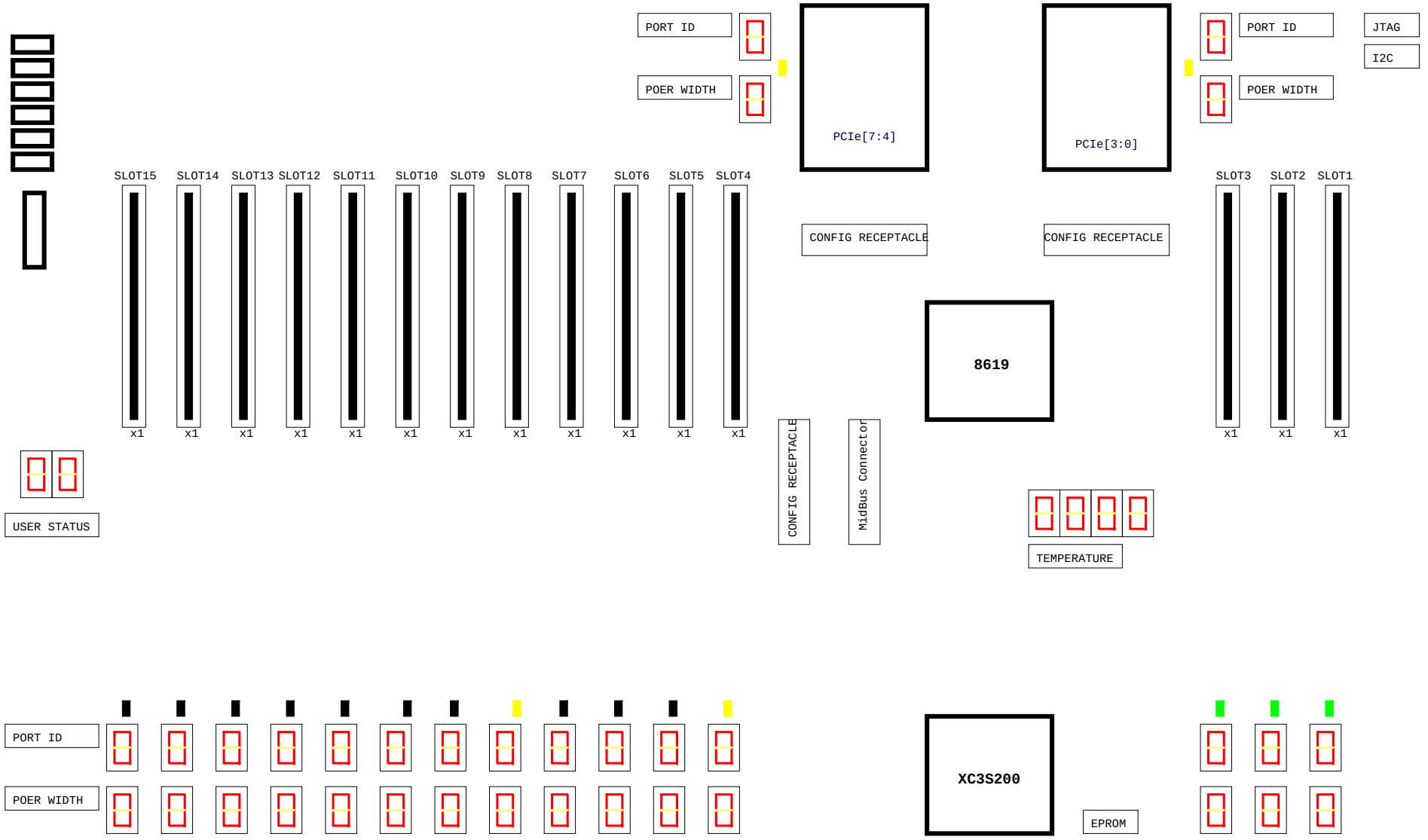
A. R277, R314, R315, R407and R408 are placed at pad 1 and 3

B. Header JP13 jump 1-2,3-4 and 5-6

C. 2"x1/4" labes with two different wordings depends the Kit to order 1."PEX8619BA-BB8U1D RDK" 2."PEX8619BA-BB4U1D RDK"

D. The label should be placed at upper right hand corner in the box

E. R343, R345, R360 and R361 are used for rework the board (see assembly instructions for details)



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RELEASE NOTES:

Initial Release: Apr 18, 2008

Release 0.1: May 15, 2008

- changed the RefClock Fanout Buffer to MC100LVEP111
- Chnaged the Xilinx FPGA part from XCS40XL to XC3S200 and the associated prom
- Added the Multioutput Voltage regulator for the new Xilin FPGA
- Updated the JTAG interface to USB to conform to latest Xilinx Tools

Release 0.2: March 9, 2009

- changed the R510 from 120 ohm to 1K ohm on page 6

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RELEASE NOTES:

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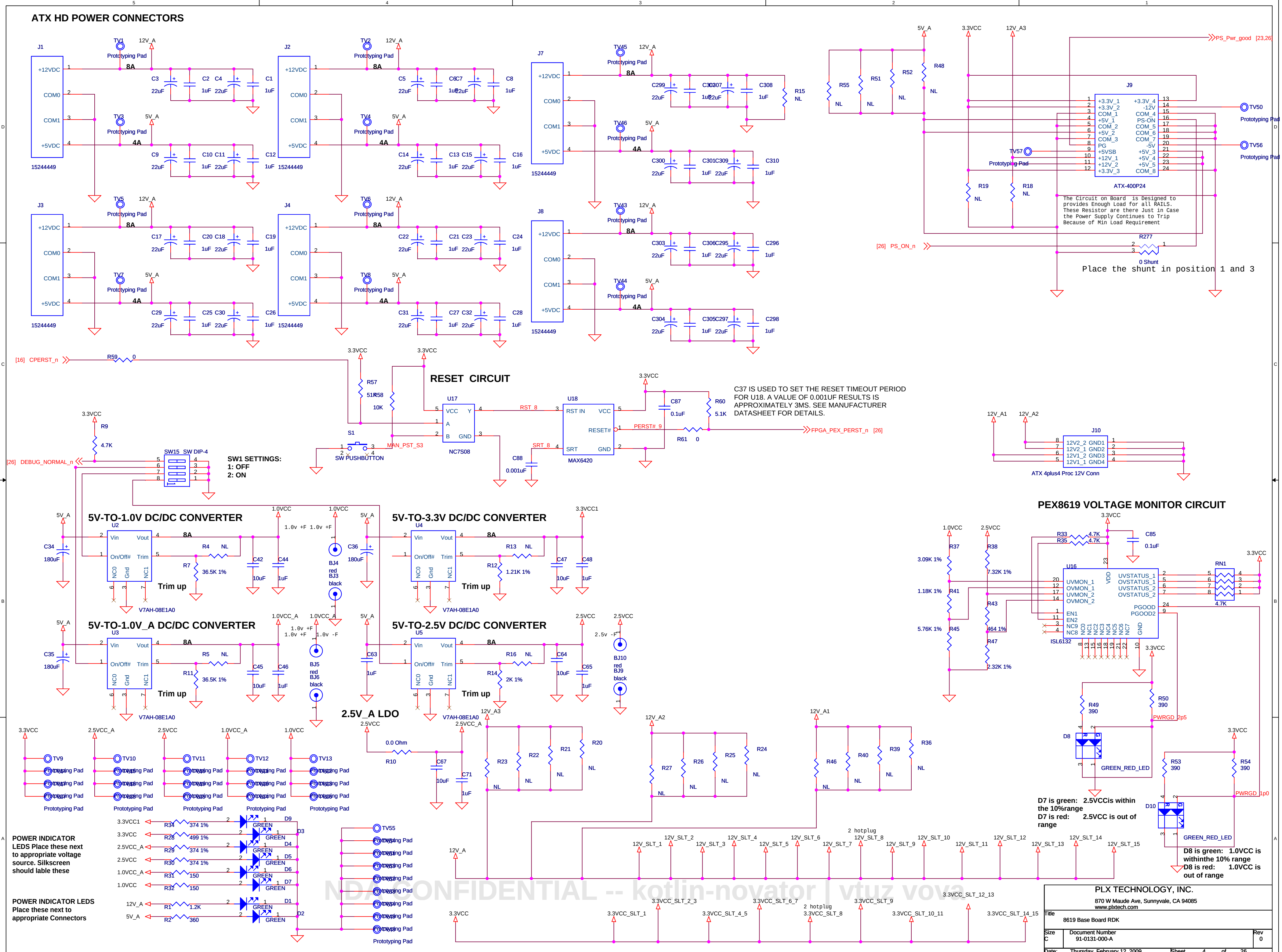

ATX HD POWER CONNECTORS
J1
J2
J3
J4
J7
J8
+12VDC
COM0
COM1
+5VDC
15244449
Prototyping Pad
12V_A
5V_A
8A
4A
22uF
1uF
J9
ATX-400P24
PS_Pwr_good [23,26]
The Circuit on Board is Designed to provides Enough Load for all RAILS. These Resistor are there Just in Case the Power Supply Continues to Trip Because of Min Load Requirement
[26] PS_ON_n
R277
0 Shunt
Place the shunt in position 1 and 3
[16] CPERST_n
RESET CIRCUIT
U17
NC7S08
U18
MAX6420
RST_8
PERST#_9
SRT_8
MAN_PST_S3
FPGA_PEX_PERST_n [26]
C37 IS USED TO SET THE RESET TIMEOUT PERIOD FOR U18. A VALUE OF 0.001UF RESULTS IS APPROXIMATELY 3MS. SEE MANUFACTURER DATASHEET FOR DETAILS.
S1
SW PUSHBUTTON
SW15 SW DIP-4
[26] DEBUG_NORMAL_n
SW1 SETTINGS:
1: OFF
2: ON
ATX 4plus4 Proc 12V Conn
5V-TO-1.0V DC/DC CONVERTER
5V-TO-3.3V DC/DC CONVERTER
5V-TO-1.0V_A DC/DC CONVERTER
5V-TO-2.5V DC/DC CONVERTER
V7AH-08E1A0
Trim up
2.5V_A LDO
PEX8619 VOLTAGE MONITOR CIRCUIT
U16
ISL6132
RN1
PWRGD_2p5
PWRGD_1p0
GREEN_RED_LED
D7 is green: 2.5VCCis within the 10%range
D7 is red: 2.5VCC is out of range
D8 is green: 1.0VCC is withinthe 10% range
D8 is red: 1.0VCC is out of range
POWER INDICATOR LEDS Place these next to appropriate voltage source. Silkscreen should lable these
POWER INDICATOR LEDS Place these next to appropriate Connectors
GREEN
12V_SLT_1
12V_SLT_2
12V_SLT_3
12V_SLT_4
12V_SLT_5
12V_SLT_6
12V_SLT_7
12V_SLT_8
12V_SLT_9
12V_SLT_10
12V_SLT_11
12V_SLT_12
12V_SLT_13
12V_SLT_14
12V_SLT_15
2 hotplug
3.3VCC_SLT_1
3.3VCC_SLT_2_3
3.3VCC_SLT_4_5
3.3VCC_SLT_6_7
3.3VCC_SLT_8
3.3VCC_SLT_9
3.3VCC_SLT_10_11
3.3VCC_SLT_12_13
3.3VCC_SLT_14_15
NDA CONFIDENTIAL -- kotlin-novator | vtuz vova
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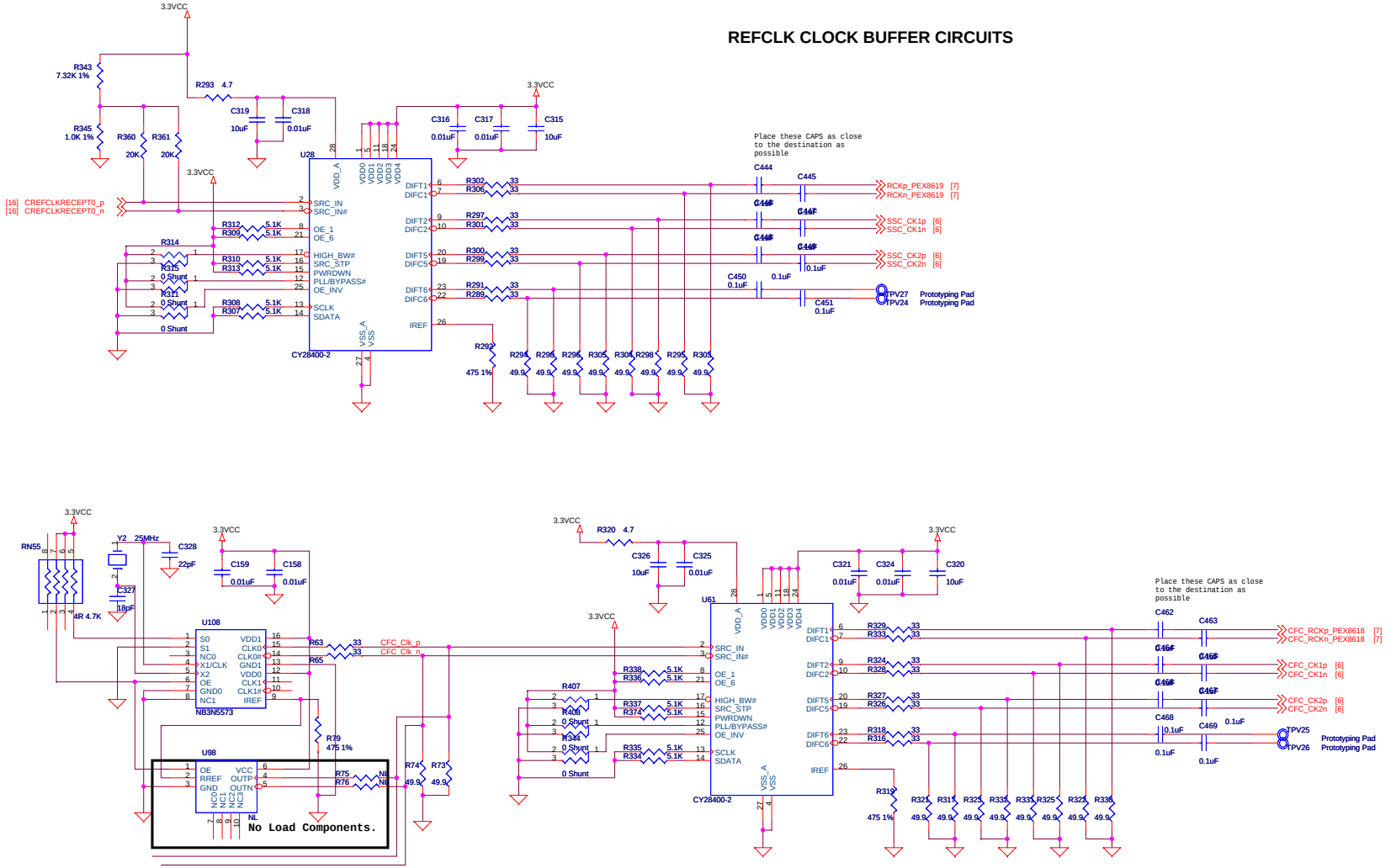
REFCLK CLOCK BUFFER CIRCUITS



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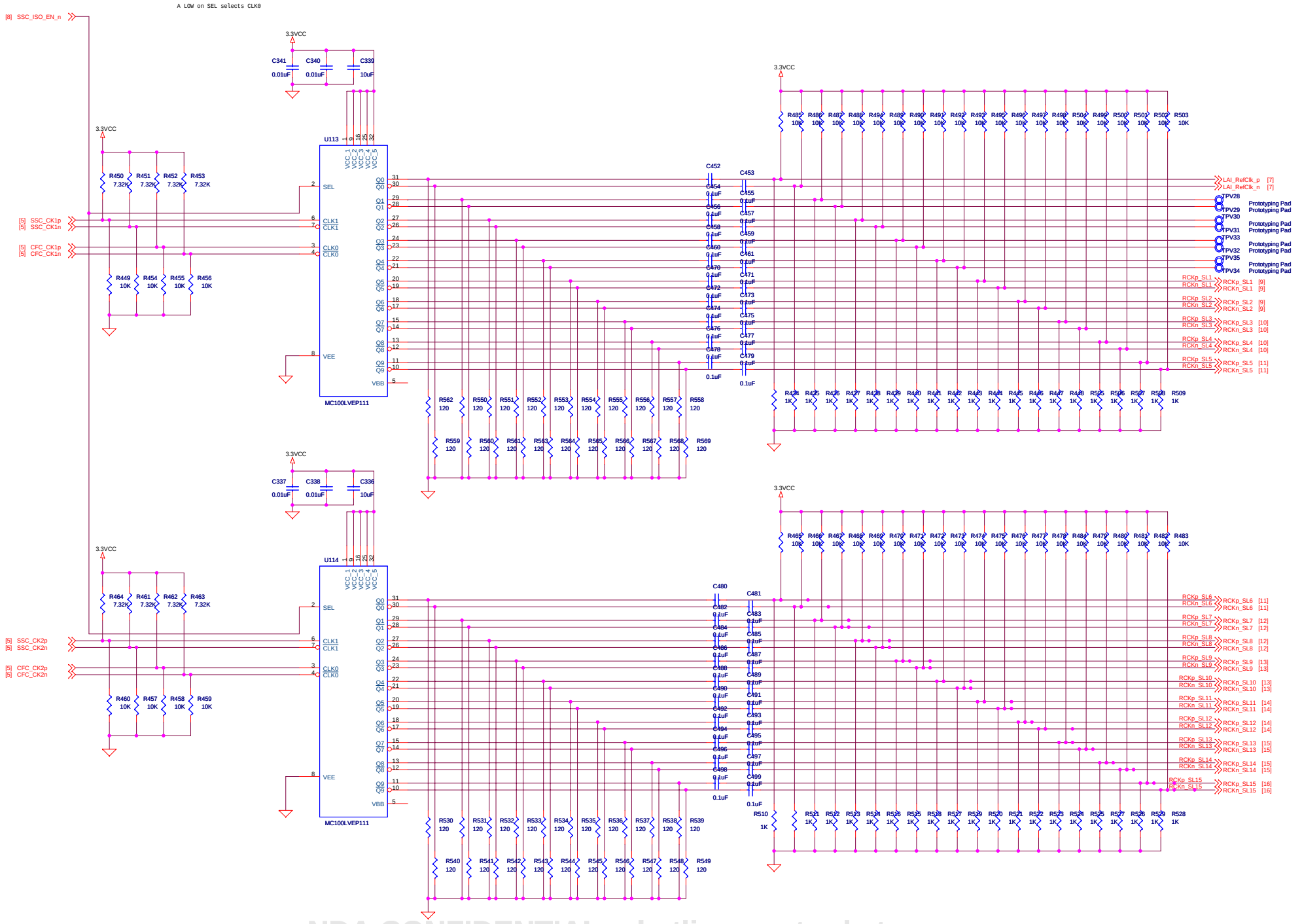

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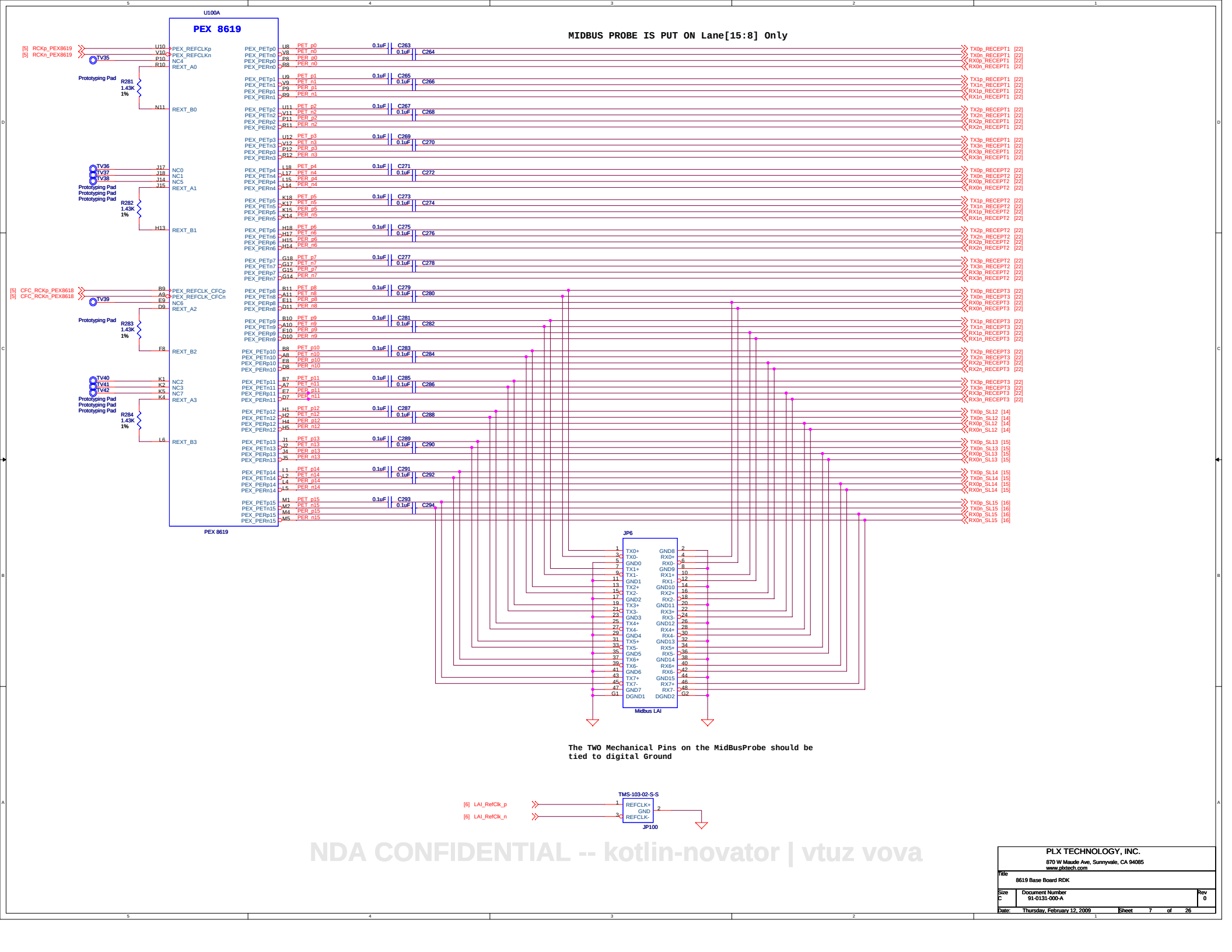
U100A
PEX 8619
MIDBUS PROBE IS PUT ON Lane[15:8] Only
[5] RCKp_PEX8619
[5] RCKn_PEX8619
TV35
Prototyping Pad
R281
1.43K
1%
TV36
TV37
TV38
Prototyping Pad
Prototyping Pad
Prototyping Pad
R282
1.43K
1%
[5] CFC_RCKp_PEX8618
[5] CFC_RCKn_PEX8618
TV39
R283
1.43K
1%
TV40
TV41
TV42
R284
1.43K
1%
PEX_REFCLKp
PEX_REFCLKn
PEX_REFCLK_CFCp
PEX_REFCLK_CFCn
REXT_A0
REXT_B0
REXT_A1
REXT_B1
REXT_A2
REXT_B2
REXT_A3
REXT_B3
0.1uF
JP6
Midbus LAI
The TWO Mechanical Pins on the MidBusProbe should be tied to digital Ground
TMS-103-02-S-S
JP100
[6] LAI_RefClk_p
[6] LAI_RefClk_n
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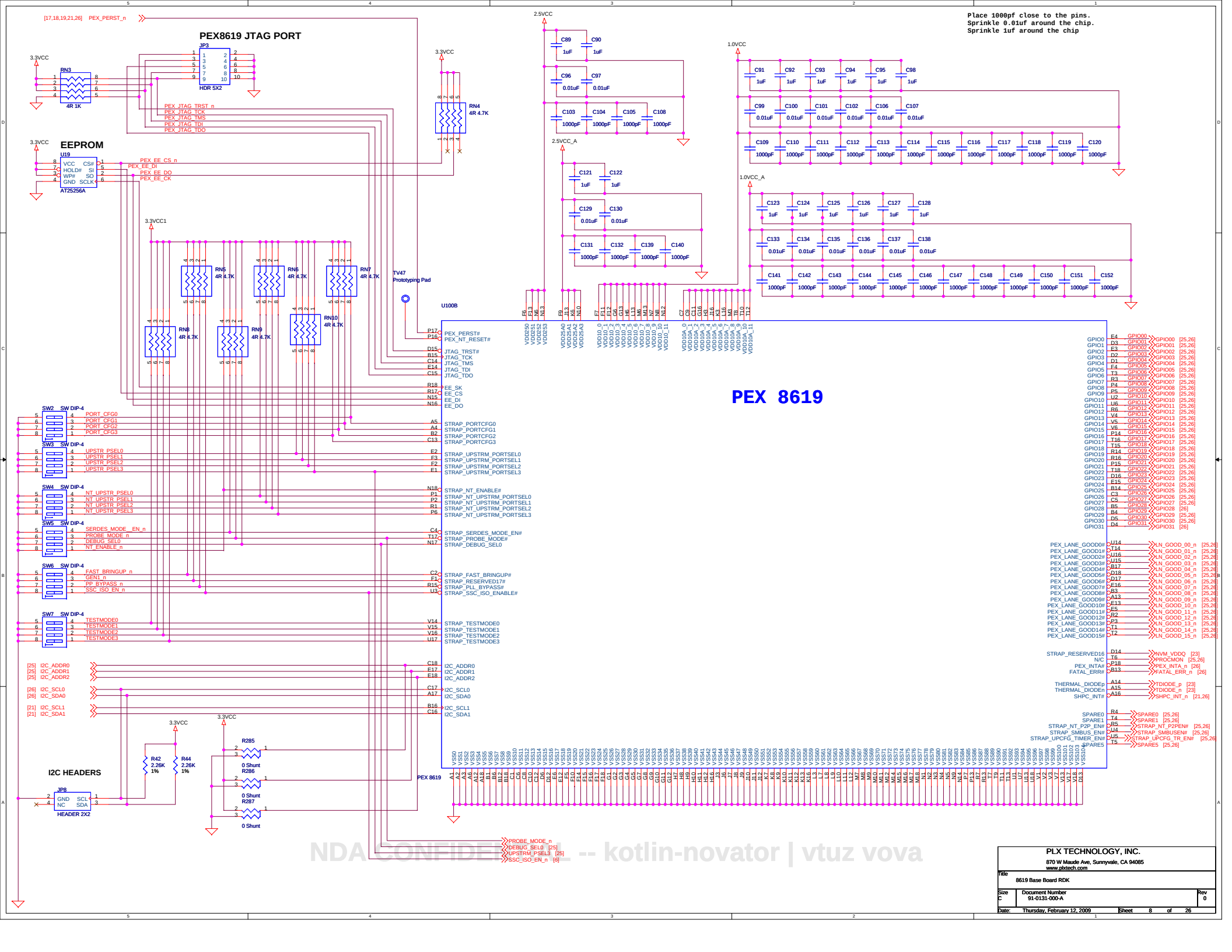

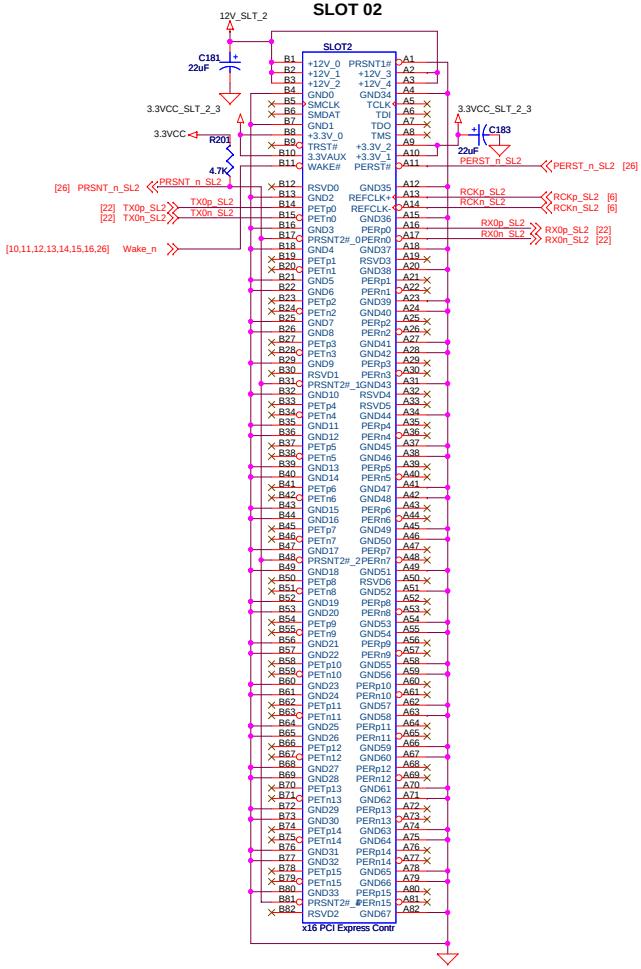

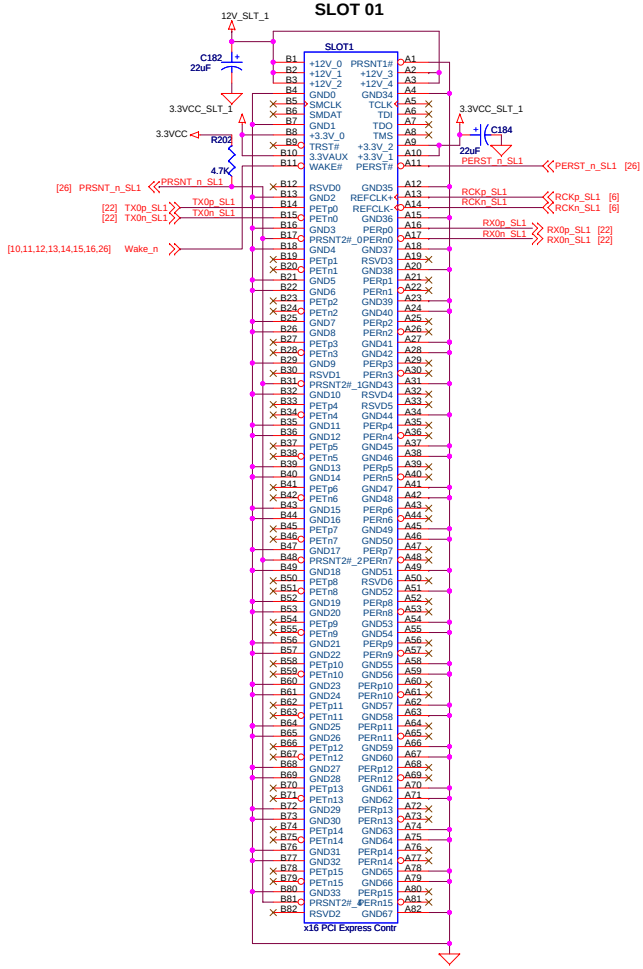

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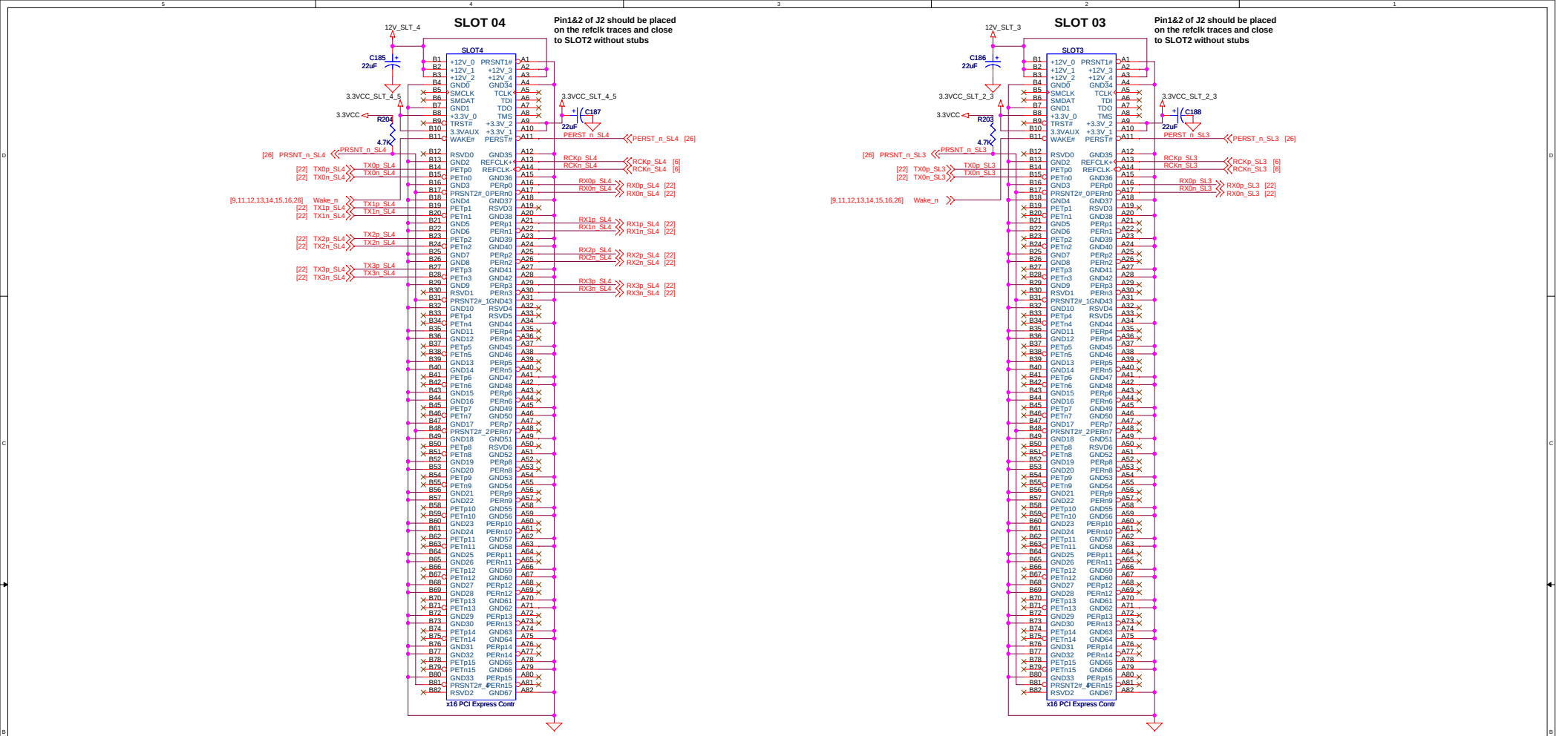

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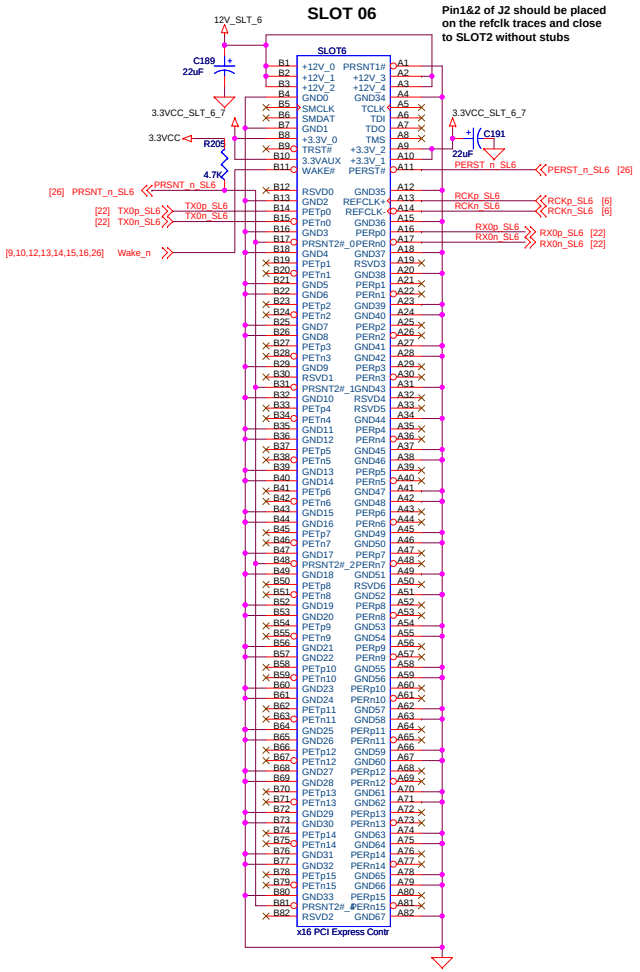

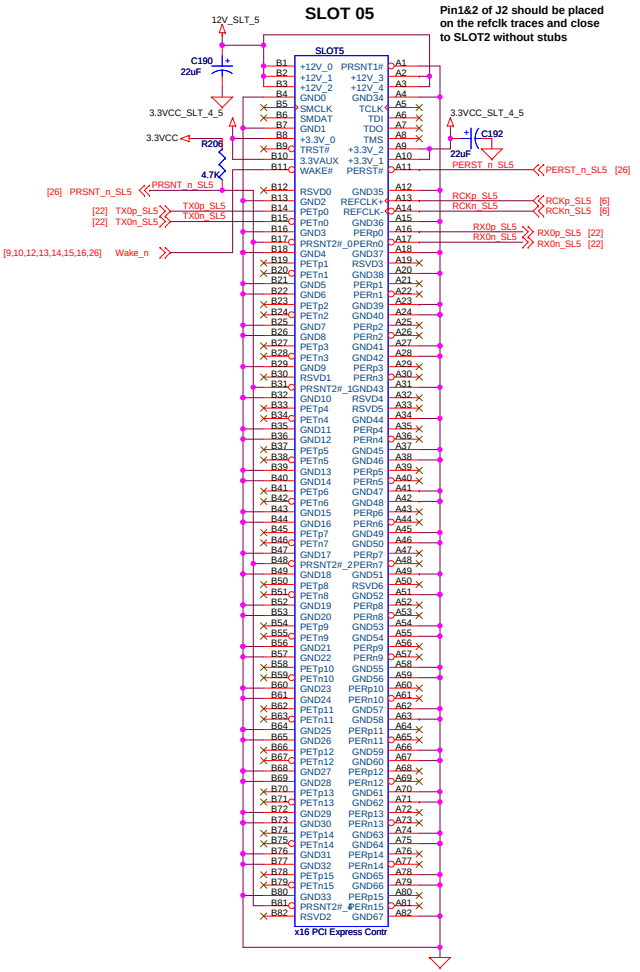

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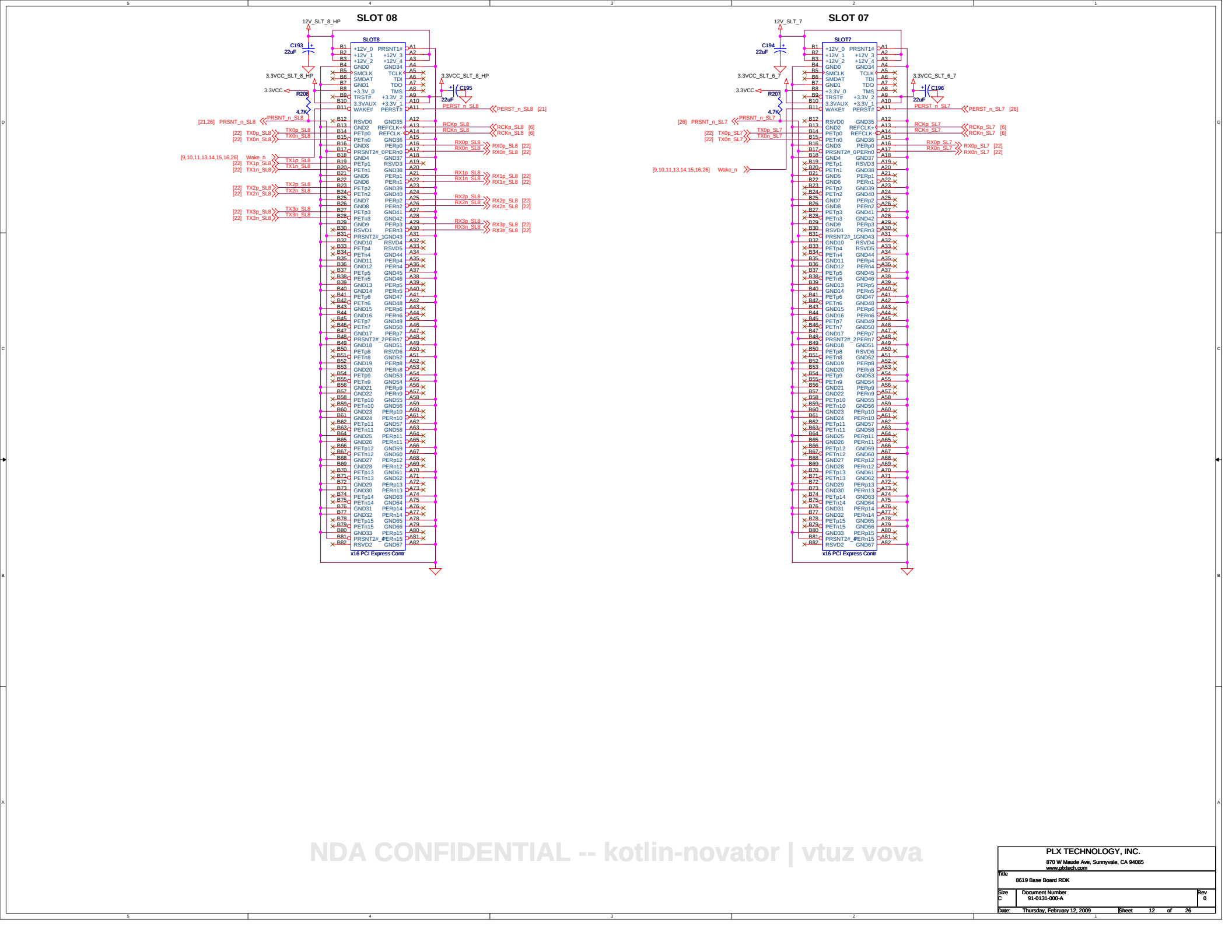

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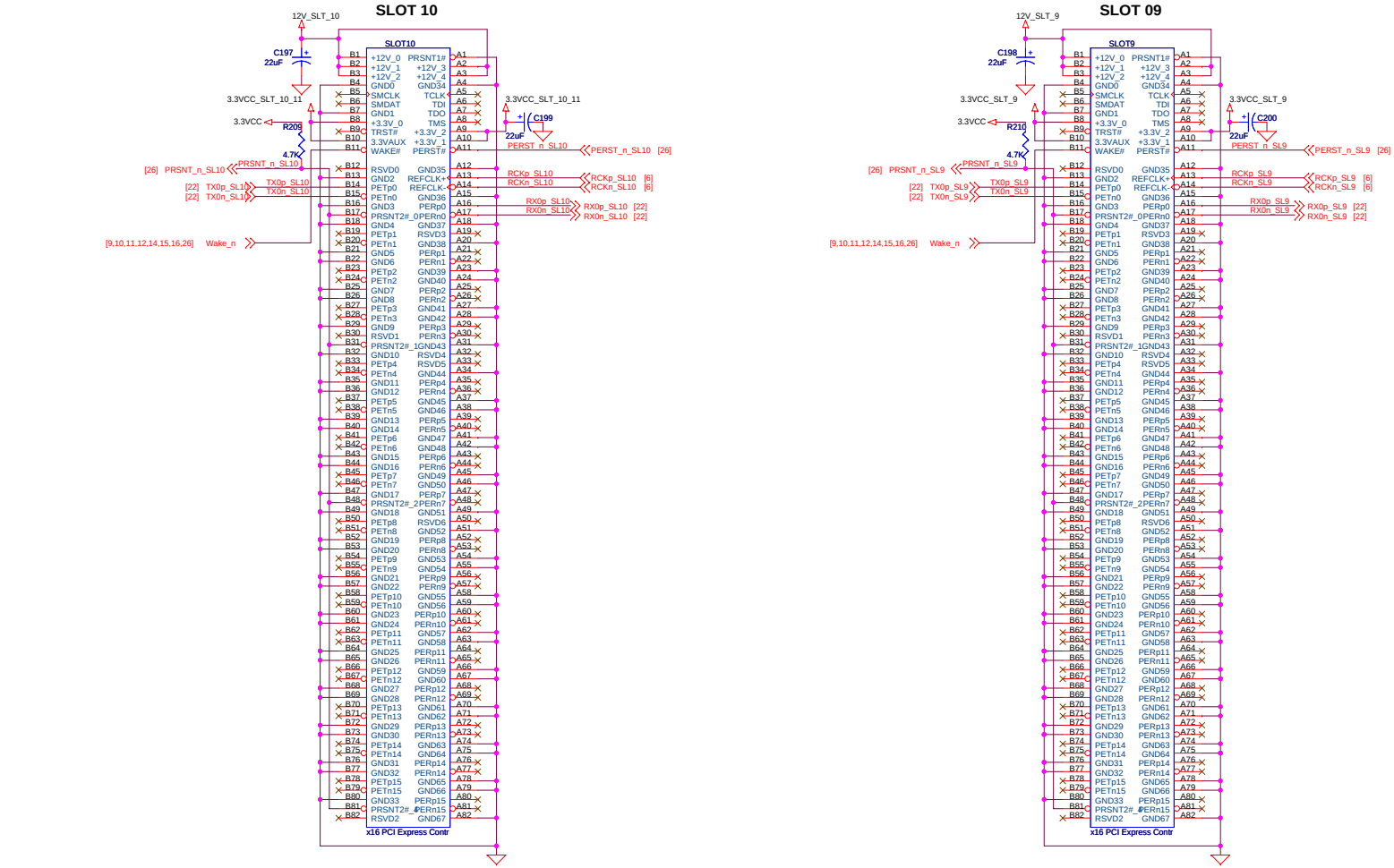

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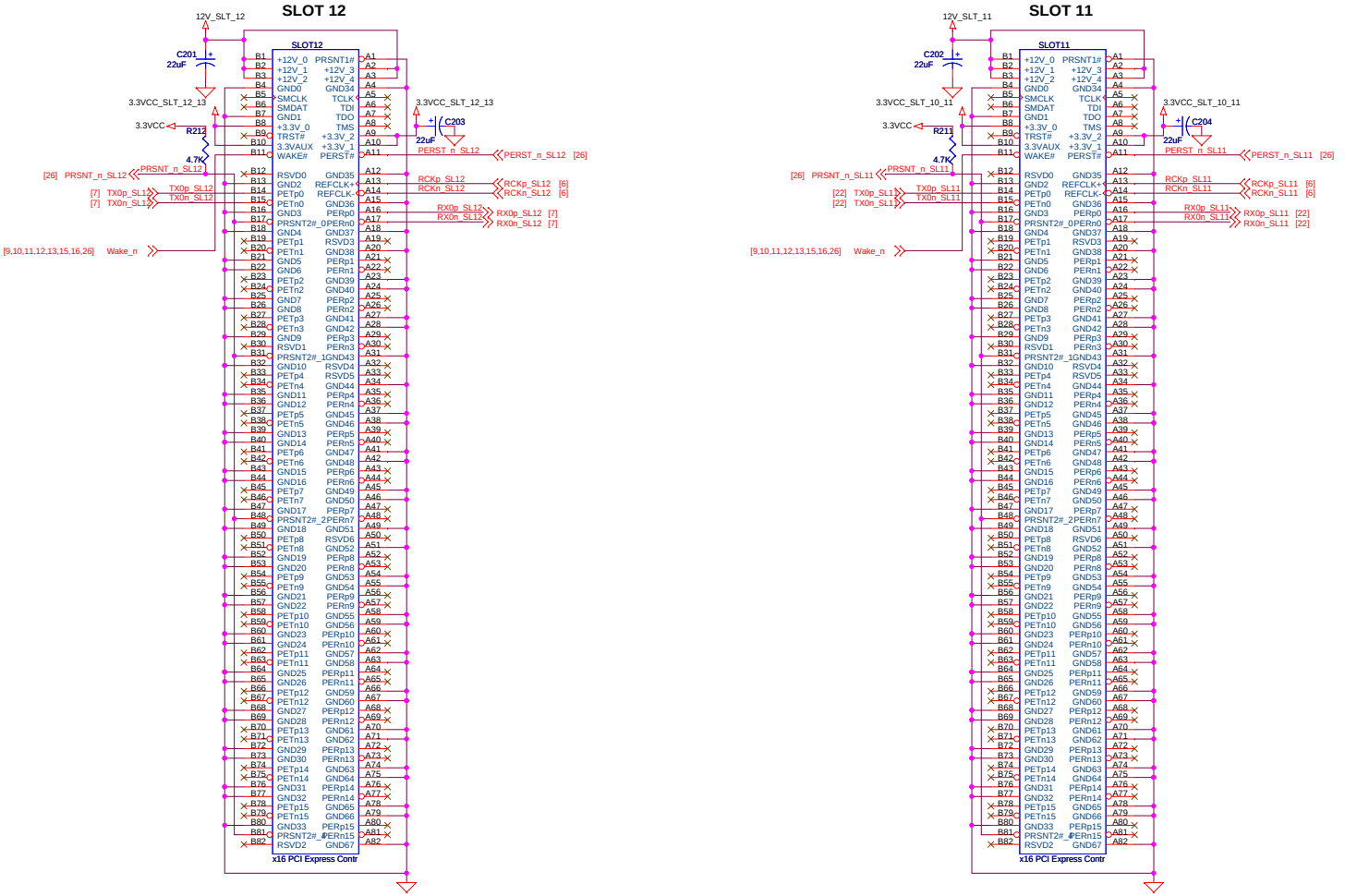

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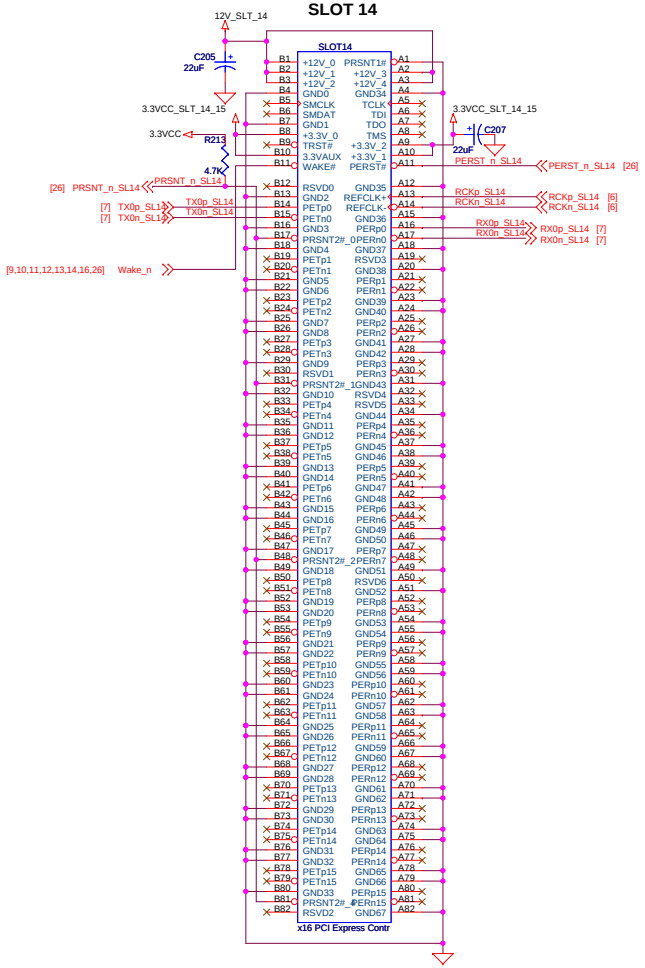

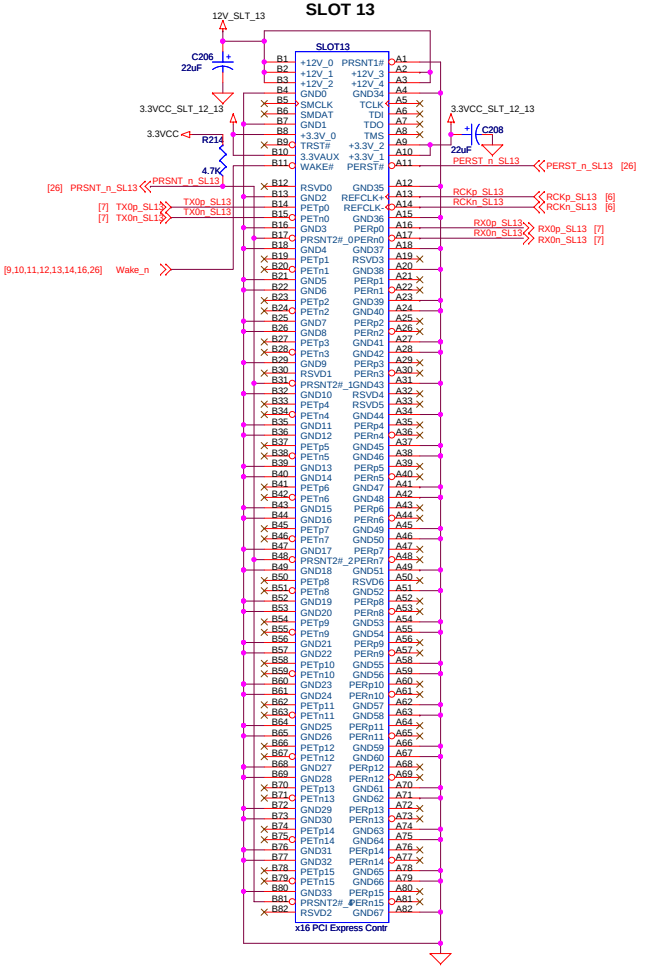

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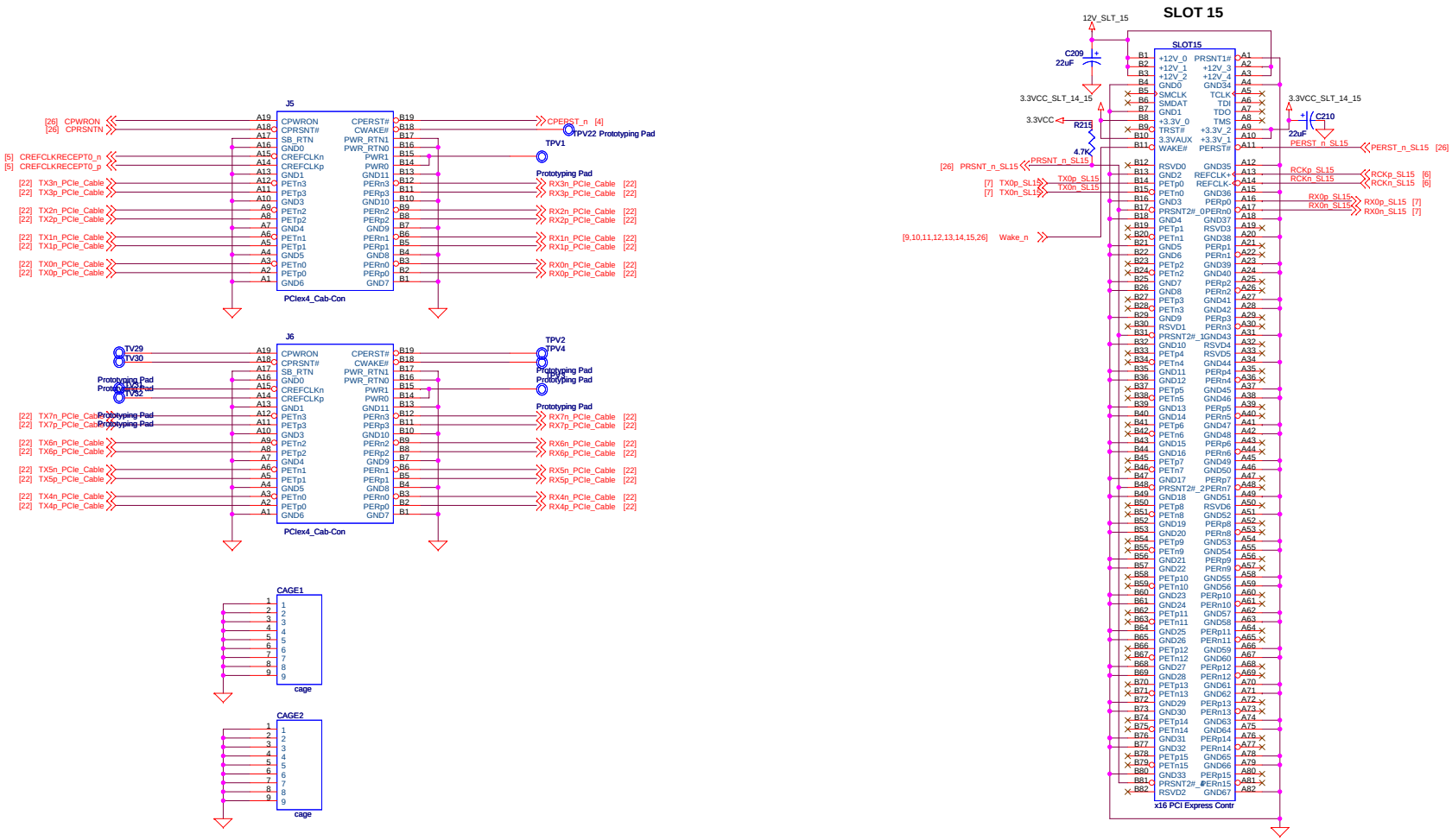

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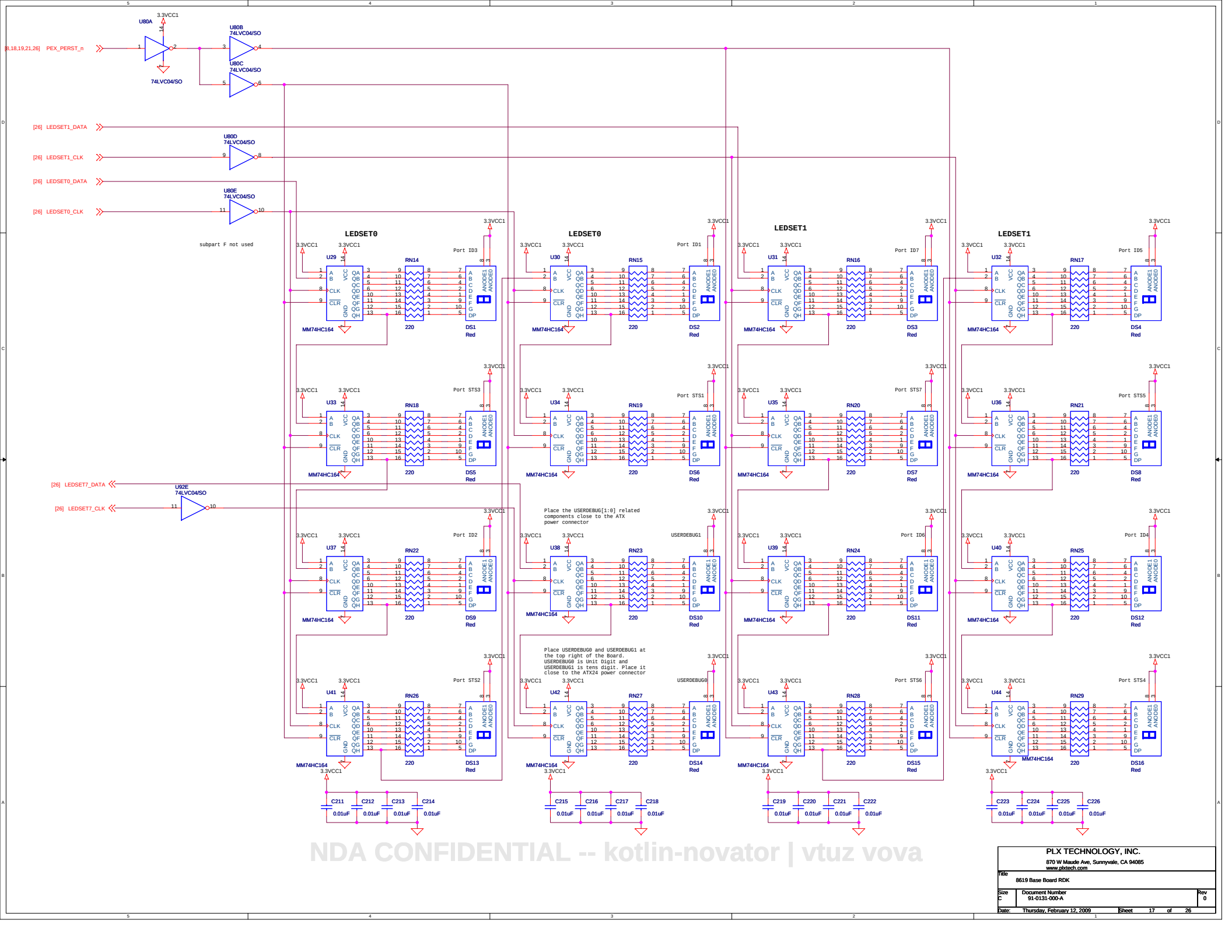
[8,18,19,21,26] PEX_PERST_n
U80A
U80B 74LVC04/SO
U80C 74LVC04/SO
74LVC04/SO
[26] LEDSET1_DATA
[26] LEDSET1_CLK
[26] LEDSET0_DATA
[26] LEDSET0_CLK
U80D 74LVC04/SO
U80E 74LVC04/SO
subpart F not used
[26] LEDSET7_DATA
[26] LEDSET7_CLK
U92E 74LVC04/SO
LEDSET0
LEDSET1
3.3VCC1
MM74HC164
220
Red
Port ID3
Port ID1
Port ID7
Port ID5
Port STS3
Port STS1
Port STS7
Port STS5
Port ID2
Port ID6
Port ID4
Port STS2
Port STS6
Port STS4
USERDEBUG1
USERDEBUG0
Place the USERDEBUG[1:0] related components close to the ATX power connector
Place USERDEBUG0 and USERDEBUG1 at the top right of the Board. USERDEBUG0 is Unit Digit and USERDEBUG1 is tens digit. Place it close to the ATX24 power connector
C211 C212 C213 C214 C215 C216 C217 C218 C219 C220 C221 C222 C223 C224 C225 C226
0.01uF
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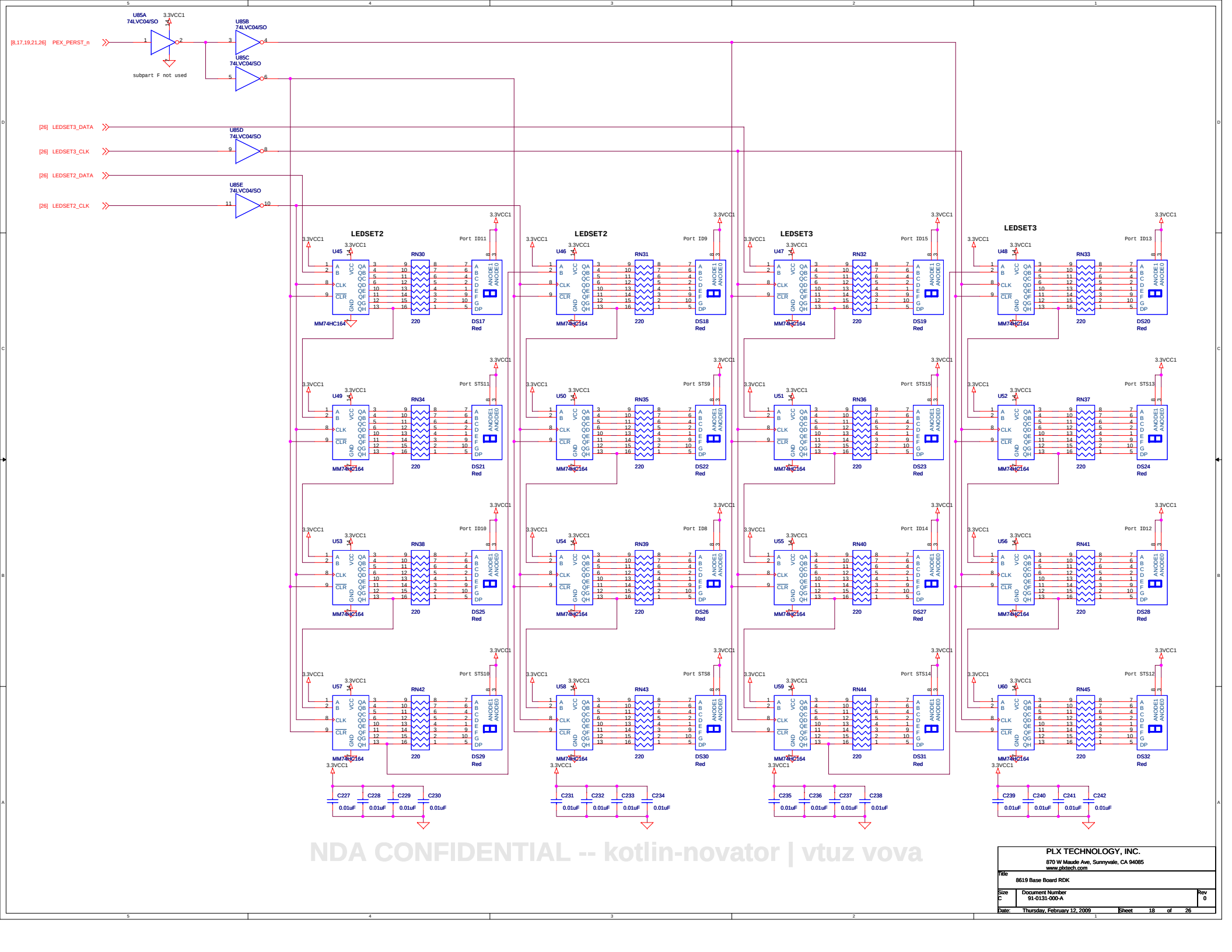

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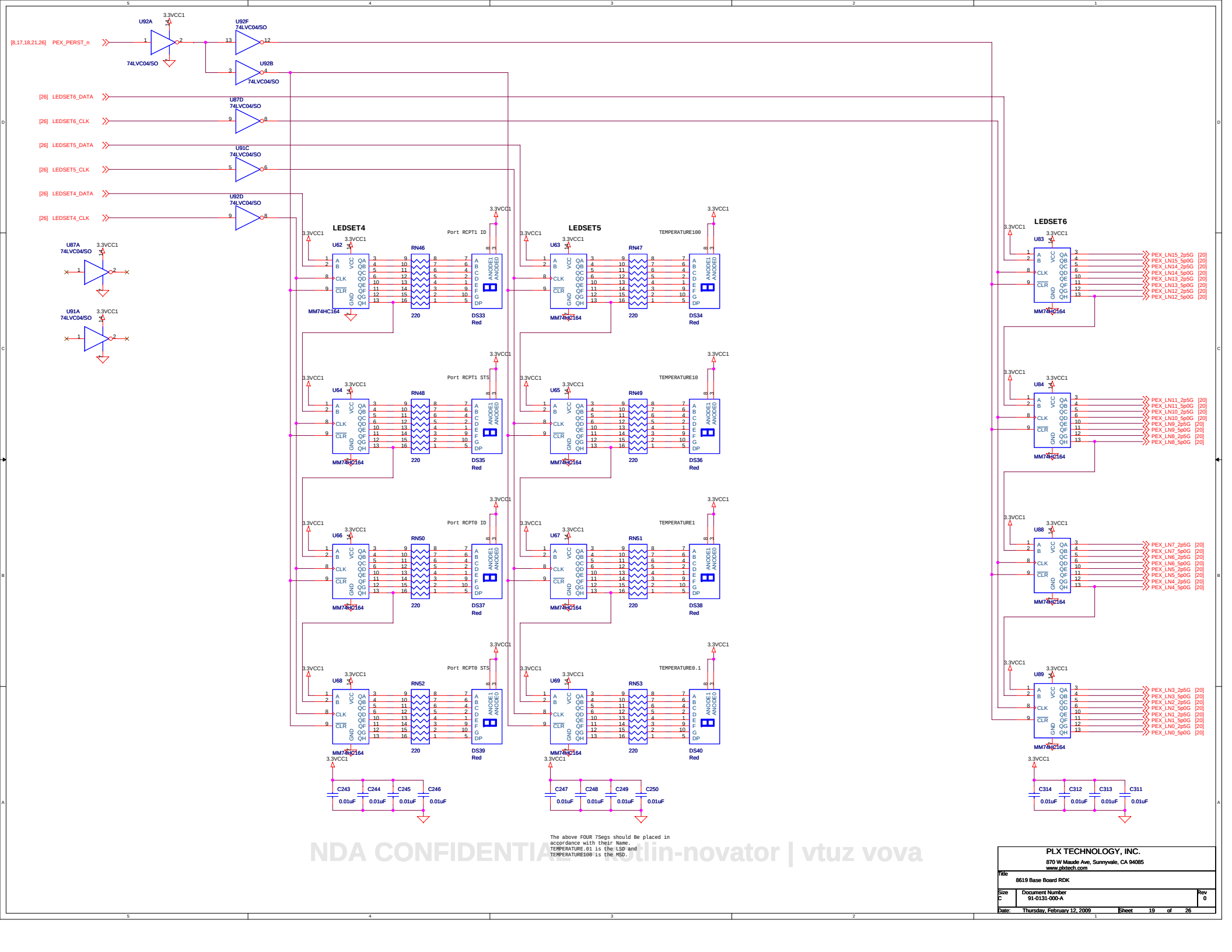

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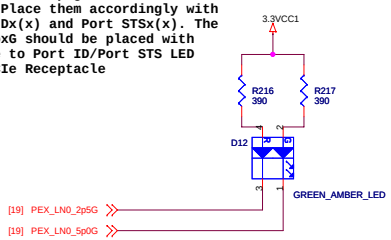
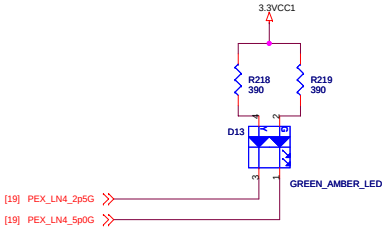
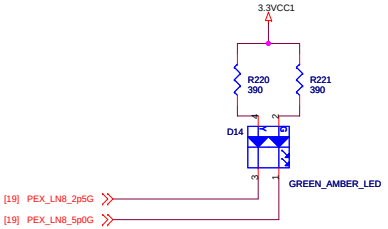
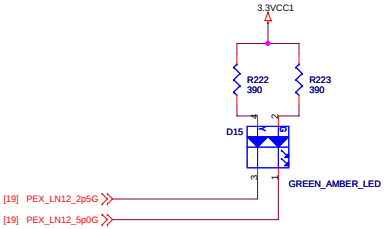
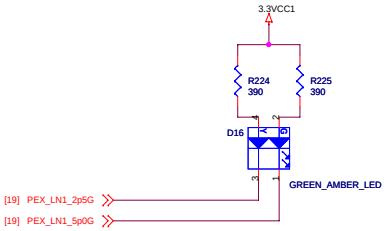
Except for PEX_LN0_xpxG LED all of the LEDs on this page are associated to slots. Place them accordingly with the Port IDx(x) and Port STSx(x). The PEX_LN0_XpxG should be placed with the close to Port ID/Port STS LED for the PCIe Receptacle

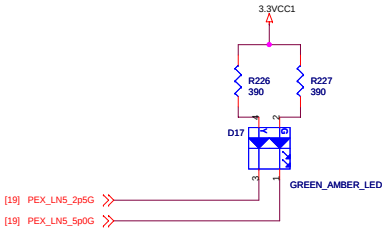


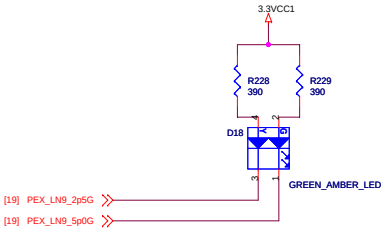


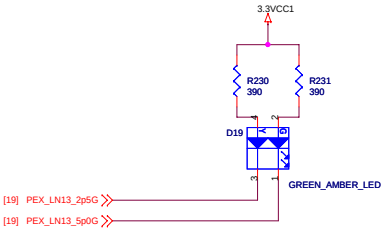


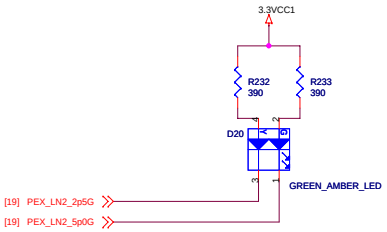


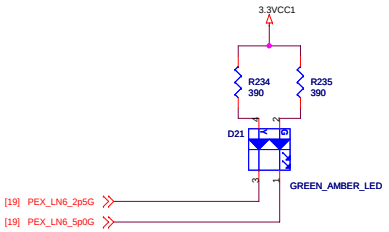


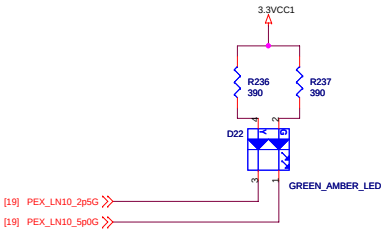


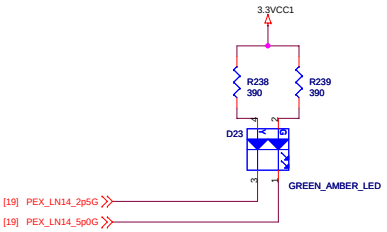


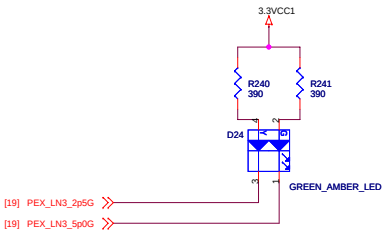


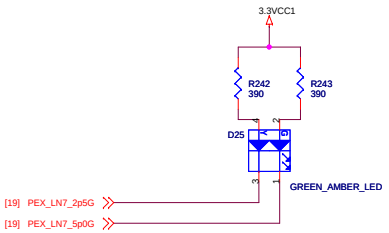


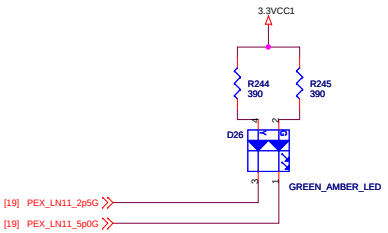


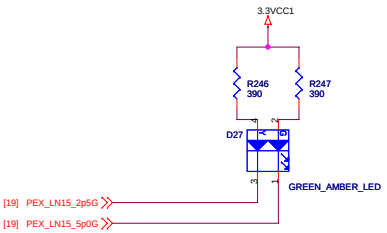












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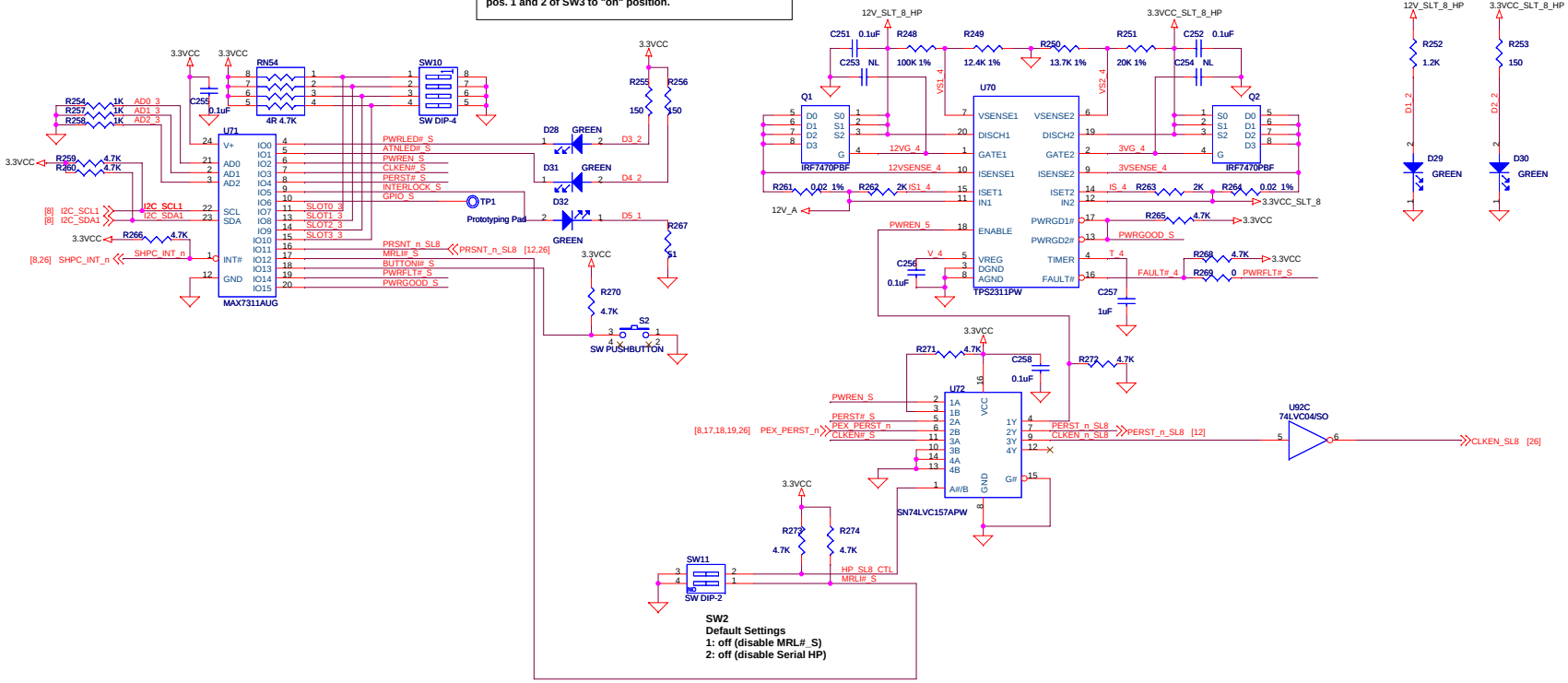
SERIAL HOT PLUG CIRCUIT FOR SLOT 8

To demonstrate the serial hot plug function of PEX 8618 requires the chip to boot with EEPROM and sets both pos. 1 and 2 of SW3 to "on" position.



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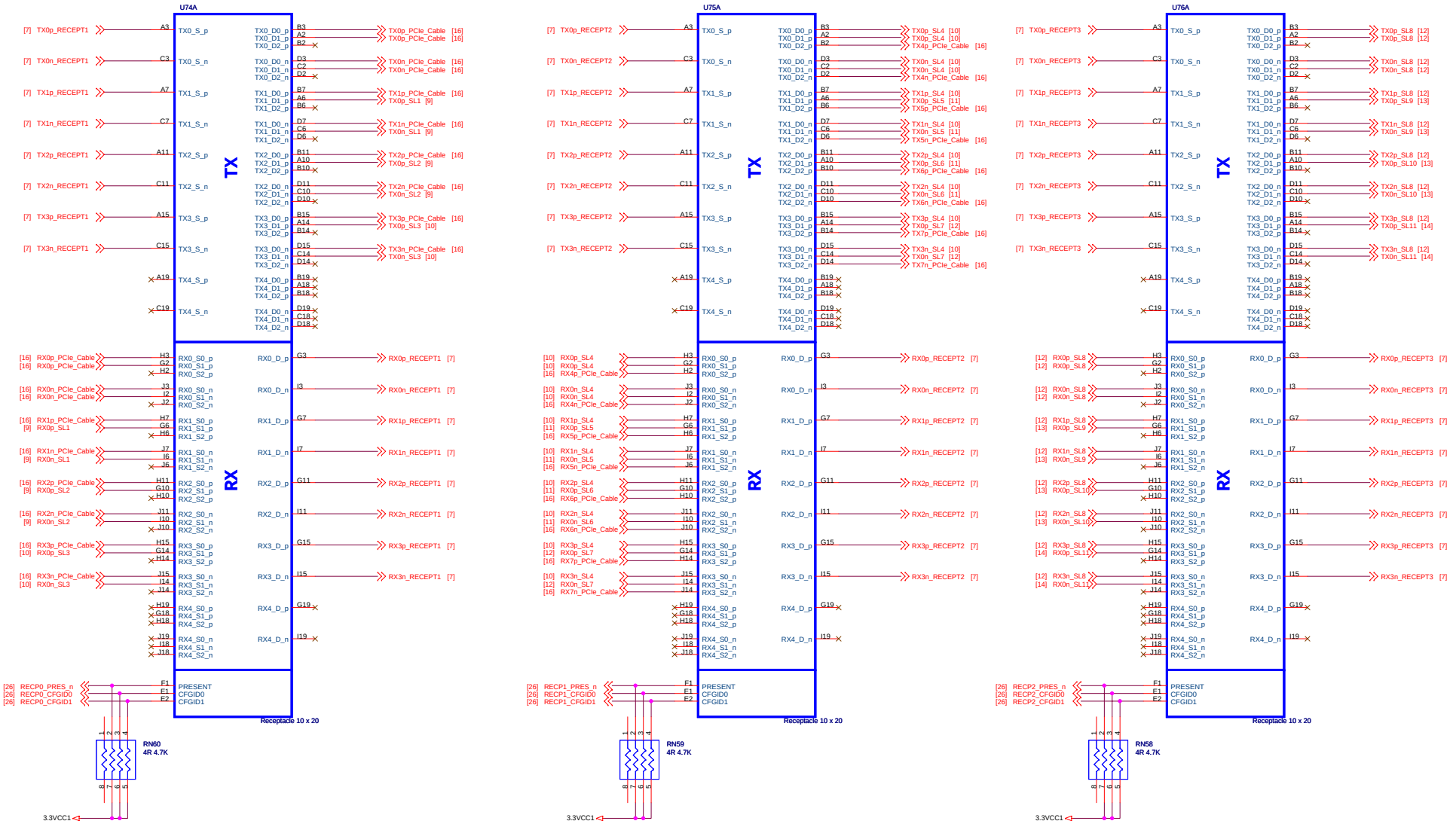

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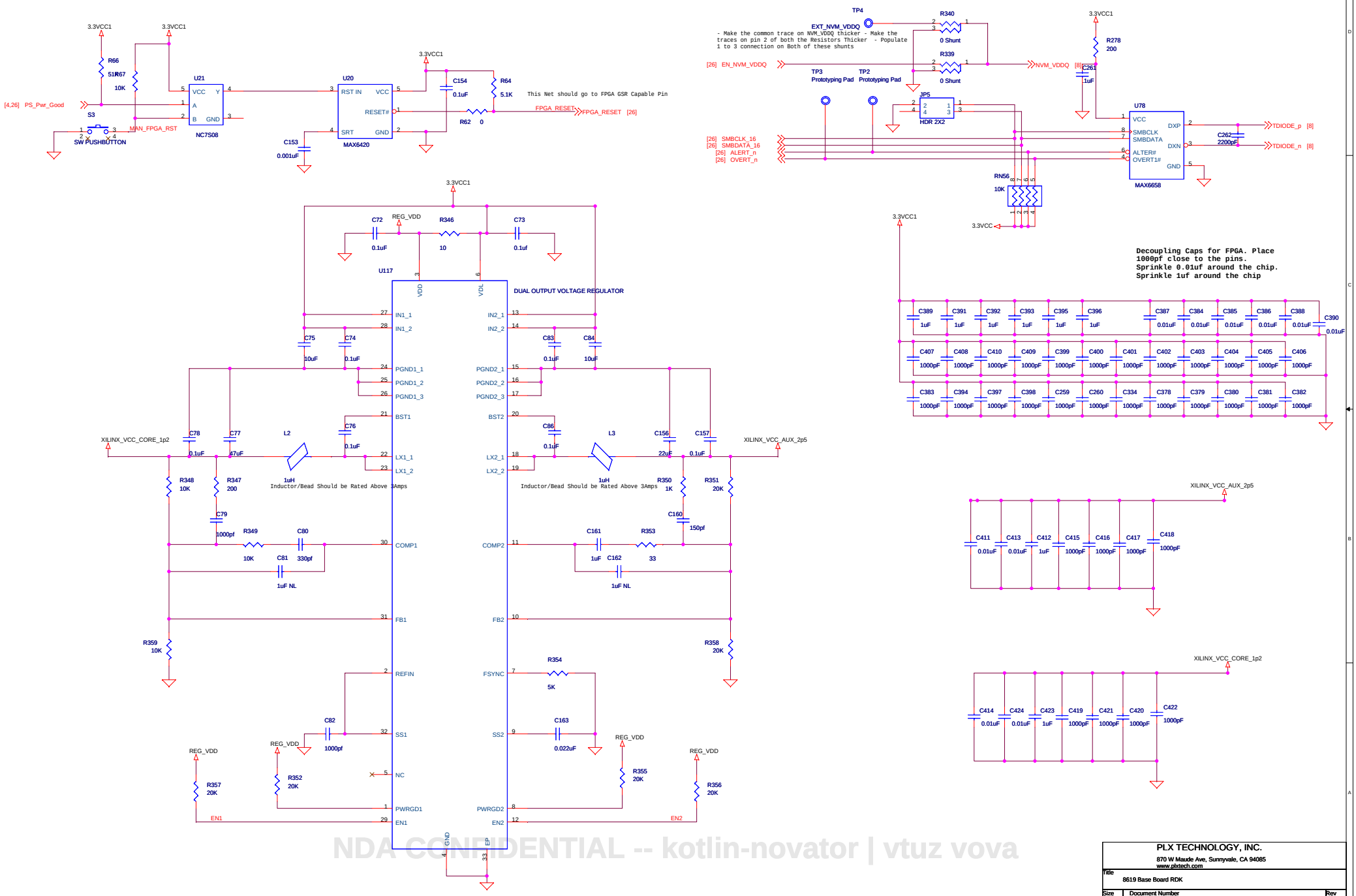

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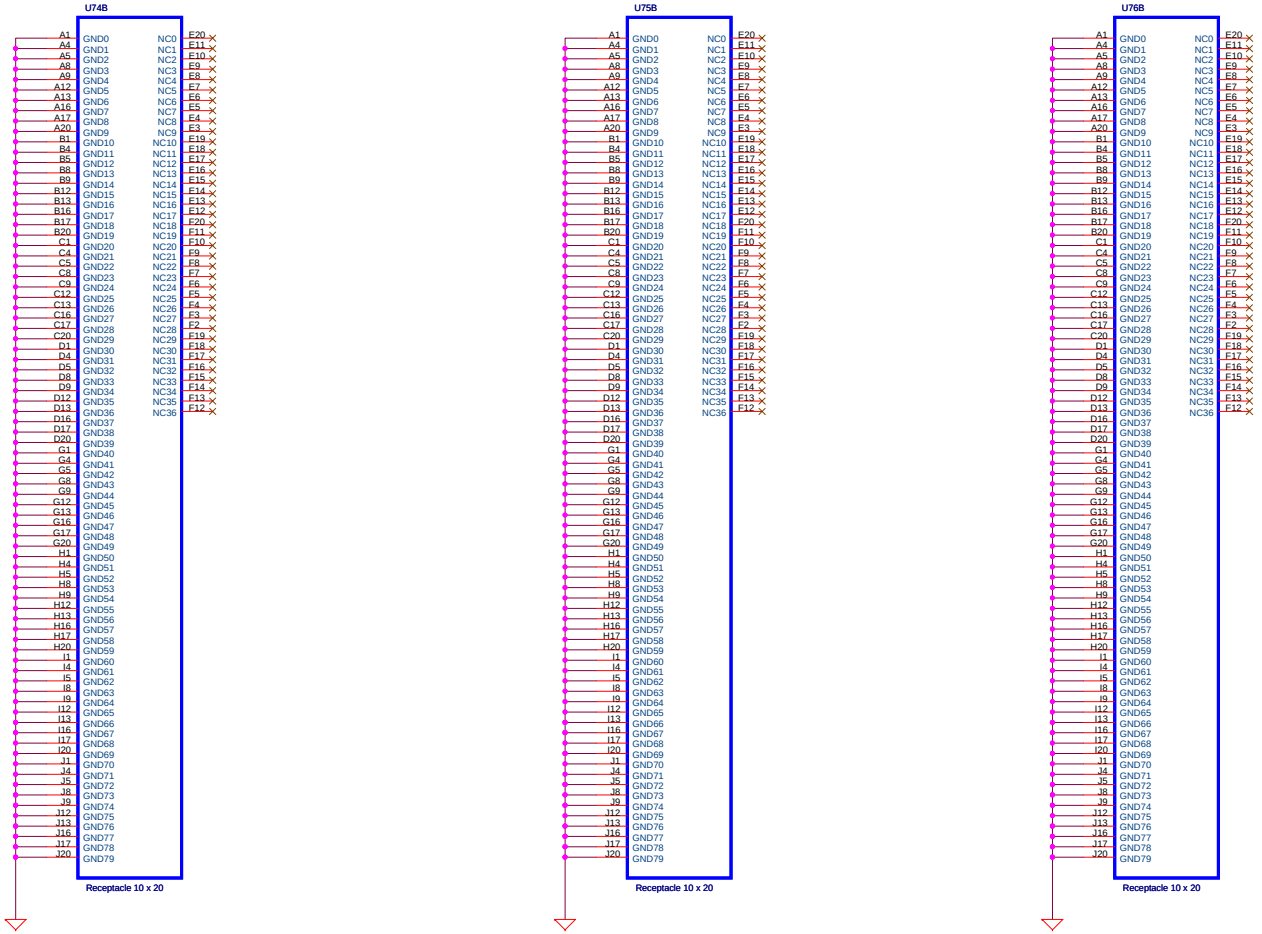

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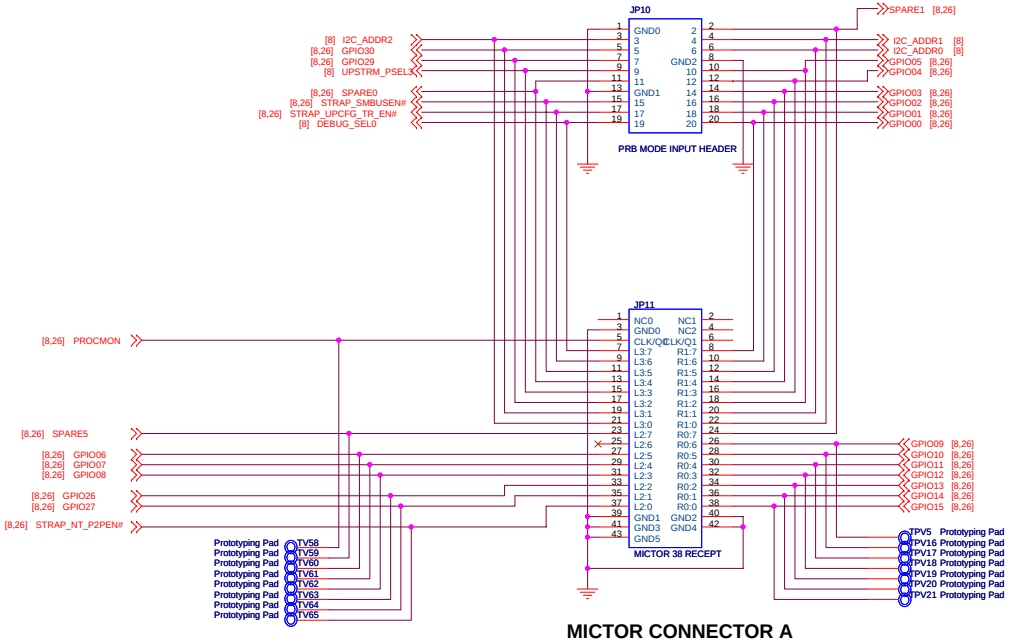
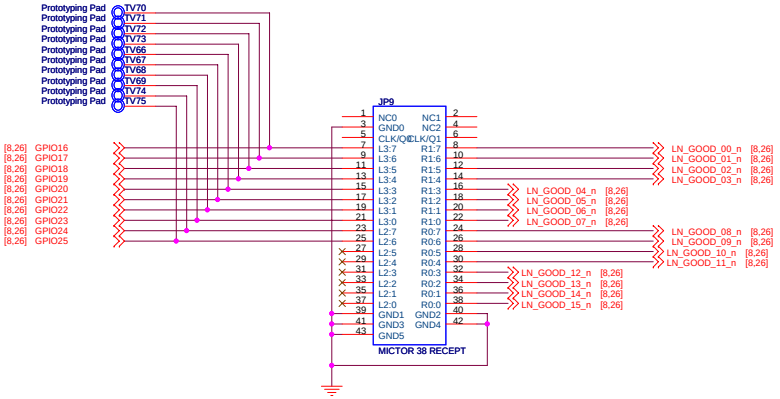
Note: The debug Circuit on this page is for PLX use only



MICTOR CONNECTOR A



MICTOR CONNECTOR C

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