BGT80

Transceiver Chipset for E-band Backhaul Applications from 81 to 86 GHz

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Datasheet

Revision: Rev. 1.0

2014-04-30

RF and Protection Devices

Specification

Date of Rev. History: 2013-04-30

Previous Revision: Target Specification Rev. 2.2

Page	Subjects (major changes since last revision)

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1 Product Features

1.1 Major Features of BGT80 Transceiver Chipset

- BGT80 covers the frequency range from 81 to 86 GHz
- Fabricated with silicon-germanium (SiGe) Infineon process technology
- Housed in a **e**mbedded **W**afer **L**evel **B**all Grid Array (eWLB) package of Infineon technology
- BGT80 can be programmed via SPI interface to work either in transmit (Tx) or/and receive (Rx) mode
- Zero IF – differential I/Q interface – direct conversion architecture
- Differential RF transmit output signaling
- Differential RF receive input signaling
- Differential intermediate frequency I/Q signaling
- Peak detector at Modulator output on the transmit path
- Peak detector at PA output on the transmit path
- Built-in temperature sensor
- SPI interface
- BITE (Built in test equipment) for EOL test in production at Infineon to verify RF performance
- Can be used in TDD or FDD systems

Product Name	Package	Marking
BGT80	PG-WFWLB-119-1, MSL1	BGT80 TR11

1.2 Applications

Intended for E-Band, 81 to 86GHz, FDD or TDD systems for telecommunication applications.

1.3 Description

The connection to the basestation was so far planned for lower data rates (few 100MBit/s) and needs now increased capacity. To do so, the backhaul technology comes into place. A solution using wireless backhaul in the E-Band (71 to 76GHz and 81 to 86GHz) will open up more than 10GHz frequency range. This enables datarates higher than 1Gbit/s for video and data service, sufficient to support LTE/4G mobile communication. Infineon business approach will enable such Gigabit service with the latest E-Band chipsets. With Infineon´s advanced SiGe (Silicon Germanium) technology with a transit frequency of 200GHz, it is possible to integrate all RF (Radio Frequency) building blocks, like Power Amplifier (PA), Low Noise Amplifier (LNA), Mixer, Voltage Gain Amplifier (VGA), Voltage Controlled Oscillator (VCO) and more into a single chip. This technology is proven and fully qualified for other Infineon Millimeter- and Microwave chipsets already. Furthermore, Infineon is the leading company to house these single chipsets into a plastic embedded Wafer Level Ball Grid Array (eWLB) package which can be processed in standard SMT flow. With the Infineon packaged chipsets, customer can reduce production cost and time-to-market significantly.

1.4 Block Diagram of BGT80 Transceiver Chipset

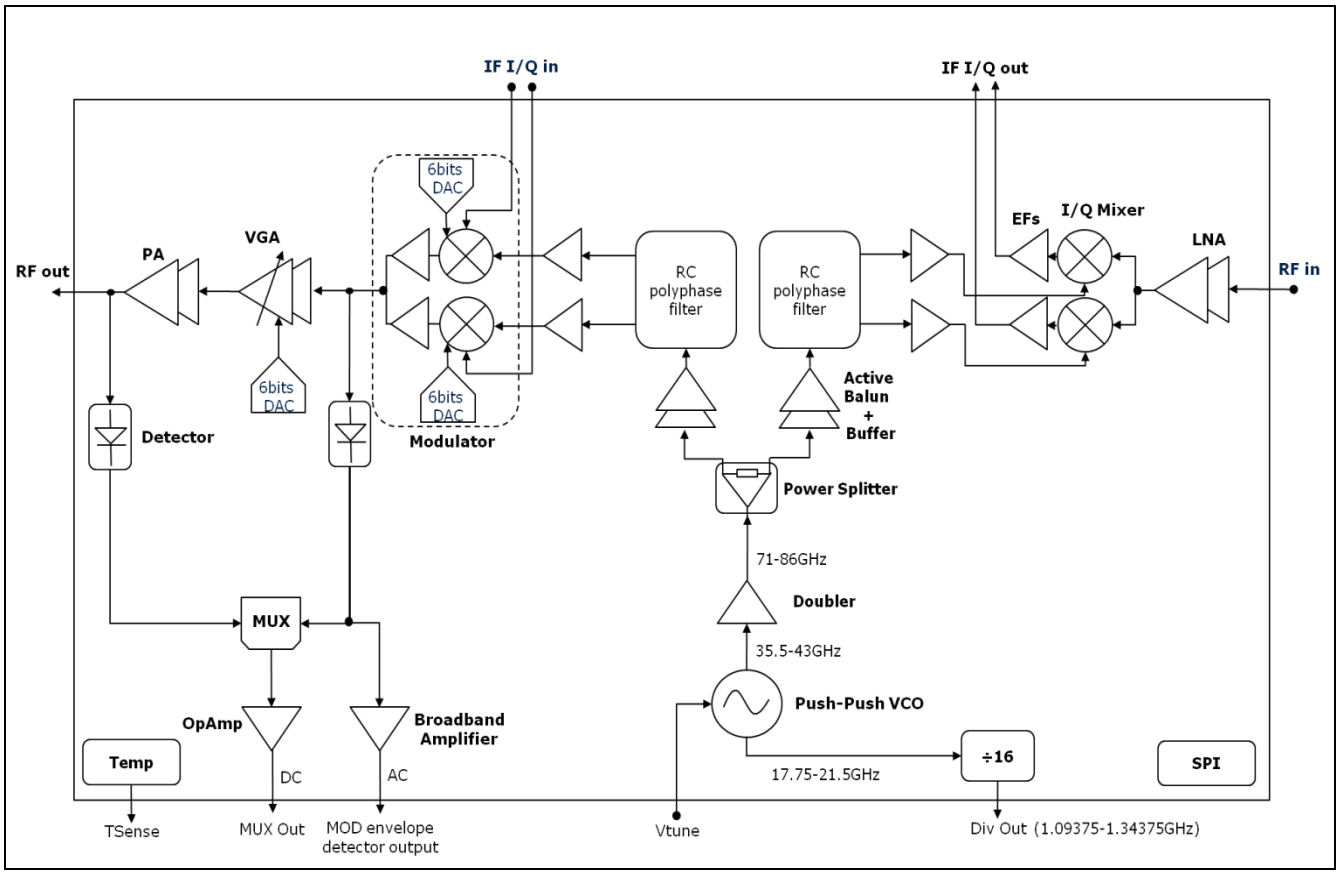


Figure 1 Block Diagram of BGT80 Transceiver Chipset

1.5 Pin Definition and Function

Figure 2 shows the bottom view of BGT80 package eWLB PG-WFWLB-119-1 with the pin number assignment.

The function of each pin is described in **Table 1** below.

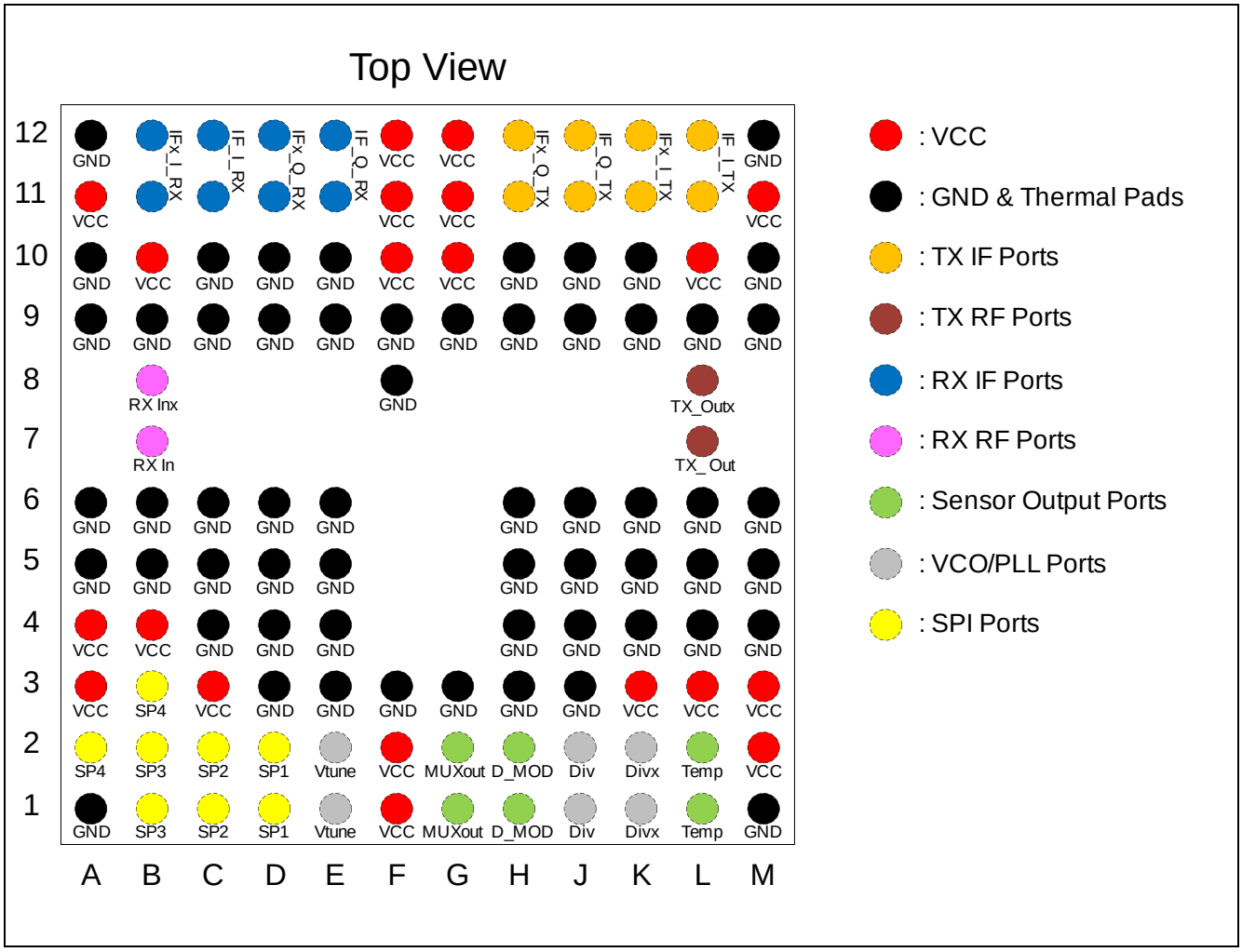


Figure 2 Pin Number Assignment of BGT80 package eWLB PG-WFWLB-119-1 (Top View)

Table 1 Pin Definition and Function

Pin No.	Name	Function
A3, A4, A11, B4, B10, C3, F10, F11, F12, G10, G11, G12, L10,	Vcc	DC supply for the transceiver chip – 3.3V

Table 1 Pin Definition and Function

Pin No.	Name	Function
M11		
K3, L3, M2, M3	Vcc_Temp	Supply voltage for the temperature sensor – 3.3V
F1, F2	Vcc_VCO	Supply voltage for the VCO – 3.3V
E1, E2	Vtune	VCO tuning voltage
D1, D2	SP1	SPI Enable - chip select
C1, C2	SP2	SPI Dataout - SPI data sequence (device → control board)
B1, B2	SP3	SPI clock
A2, B3	SP4	SPI Data - SPI data sequence (control board → device)
G1, G2	MUXout	MUX output (PPD_PA or PPD_MOD DC level output)
H1, H2	D_MOD	Modulator detector output
L1, L2	Temp	Temperature sensor output – DC voltage
J1, J2	Div	Frequency divider output
K1, K2	DivX	Complementary frequency divider output
B7	Rx_In	RF input of receiver
B8	Rx_Inx	Complementary RF input of receiver
B11, B12	IFx_I_Rx	Complementary inphase IF output of receiver
C11, C12	IF_I_Rx	Inphase IF output of receiver
D11, D12	IFx_Q_Rx	Complementary Quadrature IF output of receiver
E11, E12	IF_Q_Rx	Quadrature IF output of receiver
L7	Tx_Out	RF output of transmitter
L8	Tx_OuTx	Complementary RF output of transmitter
L11, L12	IF_I_Tx	Inphase IF input of transmitter
K11, K12	IFx_I_Tx	Complementary inphase IF input of transmitter
J11, J12	IF_Q_Tx	Quadrature IF input of transmitter
H11, H12	IFx_Q_Tx	Complementary Quadrature IF input of transmitter
A5, A6, A9, A10, B5, B6, B9, C4, C5, C6, C9, C10, D3, D4, D5, D6, D9, D10, E3, E4, E5, E6, E9, E10, F3, F8, F9, G3, G9, H3, H4, H5, H6, H9, H10, J3, J4, J5, J6, J9, J10, K4, K5, K6, K9, K10, L4, L5, L6, L9, M4, M5, M6, M9, M10, A1, A12, M1, M12	GND	Ground and thermal pads A1, A12, M1, M12 not connected to the RDL layer

Note: all pins described in the same line need to be connected on the PCB.

2 General Product Characteristic

The reference for all specified data is the Infineon application board (EVB) defined in chapter 5.

2.1 Absolute Maximum Ratings

Table 2 **Absolute Maximum Ratings T_b=-40 °C to 125 °C,** ambient temperature not below -40 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified). Parameters not subject to production test

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Supply Voltage	Vcc	V	-0.3		3.63	
DC Voltage at RF Pins	VDC_{RF}	V			0	Chip provides short to GND at the Tx and Rx RF pins
DC Voltage at all I/O Pins	$V_{I/O}$	V	-0.3		Vcc+0.3	Not exceeding 3.63V
DC Voltage at Tuning Port	V_{tune}	V	-0.3		6	
RF Input Power Level	P_{RF}	dBm			0	At the Rx input-port
IF_Tx Input Power Level	P_{IF_Tx}	dBm			0	At the IF_Tx input-port
Junction Temperature	T_j	°C	-40		170	
Storage Temperature	T_{stg}	°C	-40		150	

Attention: Stresses exceeding the max values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.2 Range of Functionality

Table 3 **Range of Functionality**

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Supply Voltage	Vcc	V	3.135	3.300	3.465	
Chip Silicon Backside Temperature Range	T_b	°C	-40		85	Measured with the on chip temperature sensor
Frequency Range	f_{RF}	GHz	81		86	

2.3 Current Consumption

Table 4 Current Consumption, Vcc= 3.135V to 3.465 and T_b= -40 to +85°C

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
- IC powered on, Tx off, Rx off [1]	ICoff	mA	200	270	340	
- Tx on, Rx off [1, 2]	ICTx	mA	400	480	560	@ max power
- Tx off, Rx on [1, 3]	ICRx	mA	280	350	420	
- Tx on, Rx on [1]	ICTRx	mA	460	560	660	@ max power

1) It includes the VCO and temperature sensor current consumption; typ Icc_VCO= 38mA (50mA Max); Icc_Tsense= 1.2mA Max

2) SPI register settings for Tx mode operation: register VGA= FF_H, register TX_MOD_I= 40_H, register TX_MOD_Q= 40_H, register General= BC_H, register MUX= 1_H

3) SPI register settings for Rx mode operation: register VGA= 0_H, register TX_MOD_I= 0_H, register TX_MOD_Q= 0_H, register General= 3_H, register MUX= 4_H

2.4 ESD Integrity

Table 5 ESD Integrity

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
ESD robustness, HBM	$V_{ESD-HBM}$	kV	-1		1	According to JESD22-A114, Equivalent Circuit: R=1k5, C=100pF,
ESD robustness, CDM	$V_{ESD-CDM}$	V	-250		250	According to JESD22-C101

2.5 Thermal Resistance

Table 6 Thermal Resistance, no heat sink applied on top of the package

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Package Rth	R_{th}	K/W		13		Chip backside to landing pad

3 Electrical Characteristic

3.1 LO Generation

Table 7 **Specifications for LO Generation,** min and max values cover the specified frequency range, f_{RF}= 81 to 86GHz, temperature range, T_b=-40 to +85°C, and voltage supply range, Vcc= 3.135 to 3.465V (unless otherwise specified)

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
LO Generation						
Tunable Frequency Range	f_{LO}	GHz	81.25		85.75	
VCO Tuning Voltage Range	V_{tune}	V	0		5.5 (5.8 opt.)	Single tuning port
Kvco	K_{vco}	GHz/V	0.5		5	@ Tx output
Phase Noise						
@100kHz Offset	$PN_{ssb100k}$	dBc/Hz		-80	-77	@ Tx output
@1MHz Offset	PN_{ssb1M}	dBc/Hz		-100	-97	@ Tx output
@10MHz Offset	PN_{ssb10M}	dBc/Hz		-120	-117	@ Tx output
Divider Chain						
Output Signaling						Differential
Divider Ratio	N_{DIV}			64		Referred to Tx output frequency
Divider Output Power	$PDIV_{out}$	dBm	-10	-7	-4	In 100 Ω differential load
Divider Output Coupling on Board	DIV_{AC}	nF		1		
Divider Output Load Impedance	DIV_{load}	Ω		100		

3.2 Transmitter Chain

Table 8 **Specifications for Transmit Chain *(RF performance at the landing pad on EVB board)*** , min and max values cover the specified frequency range, f_{RF}= 81 to 86GHz, temperature range, T_b=-40 to +85°C, and voltage supply range, Vcc= 3.135 to 3.465V (unless otherwise specified)

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Tx Output						
Output Signaling						Differential
Output Referred P-1dB	$OP\text{-}1dB_{Tx}$	dBm	2	8		Differential in 100 Ω

Table 8 **Specifications for Transmit Chain *(RF performance at the landing pad on EVB board)*** , min and max values cover the specified frequency range, f_{RF}= 81 to 86GHz, temperature range, T_b=-40 to +85°C, and voltage supply range, Vcc= 3.135 to 3.465V (unless otherwise specified)

Spec	Symbol	Unit	Value			Condition
						load; this value includes the 2dB loss of the eWLB package
Output Referred IP3	$OIP3_{Tx}$	dBm	8	14		VGA setting $3F_H$
Saturated Power	P_{sat}	dBm	4	10		Differential in 100 Ω load; this value includes the 2dB loss of the eWLB package
Power Amplifier (PA) Control Step (related to P_ctrl_d definition)	P_ctrl_s	dB	0.1	1	2	Above -10dBm output power, 6bits DAC VGA
PA Control Dynamic Range	P_ctrl_d	dB	15			-10dBm at each IF_Tx
Tx Chain Gain (over Frequency) @T_b=25°C	G_{Tx}	dB	17	22	26	Referred to a single-ended IF input, VGA setting $3F_H$
Tx Chain Gain Variation over Temperature	$G_{Tx, Temp}$	dB	+8		-10	T_b= -40 to +85°C
Noise Density at Tx Output	NF_{Tx}	dBm/ Hz	-145	-135	-125	Typ: VGA set to $3F_H$ Min: VGA set to F_H Max: VGA set to $3F_H$
LO feed-through level	LO_s	dBm		-30	-20	After calibration
Sideband Rejection	SB_R	dB		20		Before calibration
Tx-Port Output Impedance	Tx_{out}	Ω		100		Differential
IF Interface to Tx Chain						
Input Signaling						Differential
IF Bandwidth	IF_Tx_{BW}	MHz		500	1000	For each channel
IF Input Impedance	IF_Tx_{imp}	Ω	70		100	Differential
IF Coupling on Board	IF_Tx_c			AC		
Additional Features Specification						
Load Impedance for MUX Output	$Rmux_{load}$	MΩ		1		Capacitive load ≤20pF

Table 8 **Specifications for Transmit Chain *(RF performance at the landing pad on EVB board)*** , min and max values cover the specified frequency range, f_{RF}= 81 to 86GHz, temperature range, T_b=-40 to +85°C, and voltage supply range, Vcc= 3.135 to 3.465V (unless otherwise specified)

Spec	Symbol	Unit	Value			Condition
PA Peak Detector Accuracy	PPD_PA_{acc}	dB	-2		+2	
PA Peak Detector Dynamic Range	PPD_PA_{Dr}	dBm	-5		18	Min. 10Bits ADC
Output Power Vs PA Peak Detector Readout Relation	Pout PPD_PA (MUX out)	dBm V	$Pout = t_1 * \ln(\frac{PPD\_PA - y_0}{A_1})$ $y_0 = 0.9212$ $A_1 = 0.16147$ $t_1 = 6.98401$			PPD_PA selected via MUXout; this provides the output power at the landing pad
Modulator Detector Bandwidth	D_MOD_{BW}	MHz		250	350	-3dB Bandwidth

3.3 Receiver Chain

Table 9 **Specifications for Receive Chain *(RF performance at the landing pad on EVB board)*,** min and max values cover the specified frequency range, f_{RF}= 81 to 86GHz, temperature range, T_b=-40 to+85°C, and voltage supply range, Vcc= 3.135 to 3.465V (unless otherwise specified)

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Rx Chain						
Input Signaling						Differential
Conversion Gain (over Frequency)	CG_{diff}	dB	17	20	23	Differential in **400Ω** load at IF Ports; this value includes the 2dB loss of the eWLB package
Conversion Gain Variation over Temperature	$CG_{diff, Temp}$	dB	+3		-9	T_b= -40 to +85°C
Double-Side-Band Noise Figure	NFdsb	dB	7	9	16	This value includes the 2dB loss of the eWLB package
Input Referred P-1dB	$IP\text{-}1dB_{Rx}$	dBm	-18	-15		
Input Referred IP3	$IIP3_{Rx}$	dBm	-10	-7		
Input Referred IP2 (related to 2nd Harmonic)	$IIP2_{Rx}$	dBm	+30	+35		

Table 9 **Specifications for Receive Chain *(RF performance at the landing pad on EVB board)*,** min and max values cover the specified frequency range, f_{RF}= 81 to 86GHz, temperature range, T_b=-40 to+85°C, and voltage supply range, Vcc= 3.135 to 3.465V (unless otherwise specified)

Spec	Symbol	Unit	Value			Condition
LO Residual Power at the Rx Input	LO_{res}	dBm		-50	-45	
RF-Port Input Impedance	RF_{In}	Ω		100		Differential
Rx Chain to IF Interface						
Output Signaling						Differential
IF Bandwidth	IF_Rx_{BW}	MHz		500	1000	For each channel
IF Load Impedance	IF_Rx_{load}	Ω	400			Differential; Load the IF buffer can drive
IF Coupling on Board	IF_Rx_c			AC		
I/Q Amplitude Imbalance	IQ_{AI}	dB			1	
Absolute I/Q Phase Imbalance	$IQ_{\Delta\phi}$	deg		7	10	@ typ Vcc T_b, IF_Rx_{BW}, and f_{LO}= 83.5GHz
Relative I/Q Phase Imbalance	$IQ_{\Delta\phi R}$	deg	-3	0	3	Deviation of $IQ_{\Delta\phi}$ over Vcc, T_b, IF_Rx_{BW}, and f_{LO}

3.4 Temperature Sensor

Table 10 **Specifications for Temperature Sensor,** min and max values cover the specified voltage supply range, Vcc= 3.135 to 3.465V (unless otherwise specified)

Spec	Symbol	Unit	Value			Condition
Parameter			min	typ	max	
Temperature Range	T_b	°C	-40		+125	
Temperature Sensor Output Voltage Range	Tsense	V	1.135		2.01	
Chip Backside Temperature (Temp) Vs Temperature Sensor Readout (Tsense) Relation	Temp Tsense	°C V	$Temp = \frac{Tsense - a}{b};$ $a = 1.36;$ $b = 0.005$			See also Tsense_off and Tsense_sl
Temperature Sensor Offset (*a*)	Tsense_off	V	1.335	1.36	1.385	
Temperature Sensor Slope (*b*)	Tsense_sl	mV/K		5		
Load Impedance for Tsense Output	$Rsens_{load}$	MΩ		1		Capacitive load ≤20pF

4 Digital Control Interface

4.1 SPI (Serial Peripheral Interface)

The BGT80 is configured using a 4-wire SPI slave interface. The interface is always enabled and works autonomous; therefore no registers are required to control the SPI interface. It is used to configure the internal modules of the BGT80 chip via registers. The main tasks are to set the mode of operation of the Tx and/or Rx chain. Communication with an external micro controller is done via the four dedicated pins DATAOUT, DATA, CLK and ENABLE.

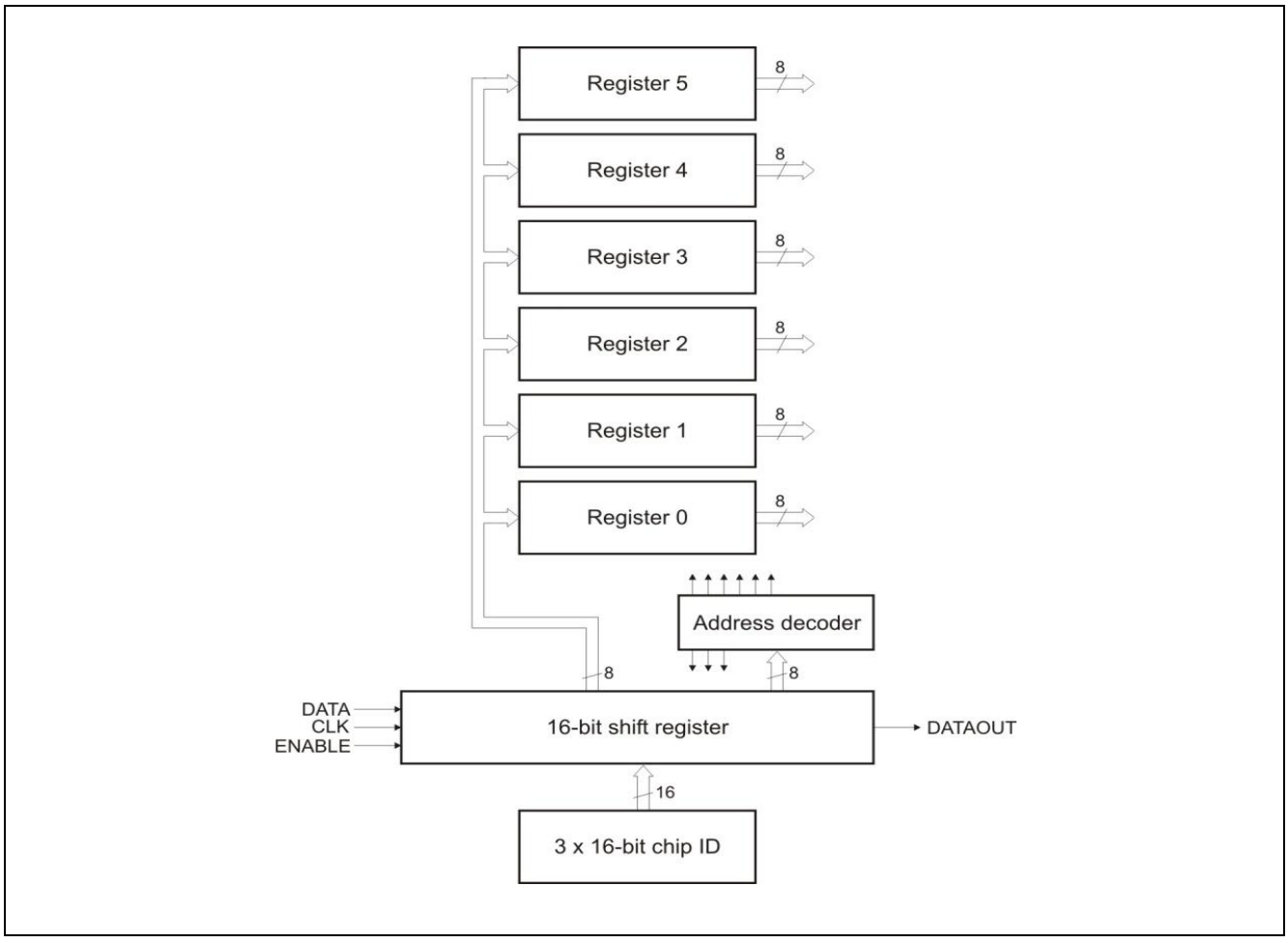


Figure 3 SPI Block Diagram

The SPI interface consists of a 16-bit shift register and six 8-bit registers (**Figure 3**). The interface is programmed by a 16-bit sequence consisting of a control (CMD)/address (ADDR) byte and a data byte (DATA).

The transceiver circuit is configured by writing configuration data into the six 8-bit registers (Register 0 to Register 5). The chip ID (set by 48 ID fuses) can be read back by applying a read chip-ID command.

4.2 Module Description

The SPI interface is programmed by a 16bit sequence consisting of two mode bits CMD, 6 address bits ADDR and 8 data bits DATA. This sequence is described in **Figure 4** and **Table 11**. The mode CMD is used to choose between read and write access.

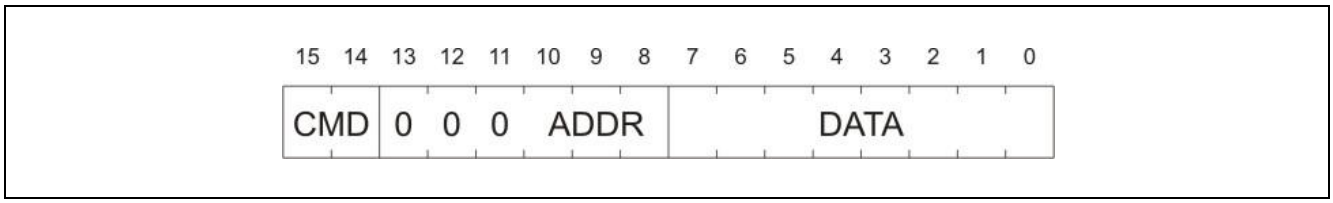


Figure 4 SPI Protocol

Table 11 SPI – Protocol Field Description

Field	Bit position	Description
CMD	15:14	Mode bit: 11_B – **write** 10_B – **read** 01_B – not used 00_B – **read out chip ID**
ADDR	13:11 10:8	000_B – reserved **Register address**
DATA	7:0	**Data**

4.3 Timing

The signal ENABLE acts as chip select and is low-active. The transmission of the serial data provided to the serial data input DATA is started by a negative edge on the enable input ENABLE. Data at the serial input DATA is then read at the falling edge of the clock input CLK. The most significant bit (MSB) is read first (**Figure 5** and **Figure 6**).

The serial output DATAOUT is high impedance while ENABLE remains inactive (logic high). Output data is clocked out at the rising edge of the clock input CLK with the MSB first. The timing parameters specified in **Table 12** have to be considered.

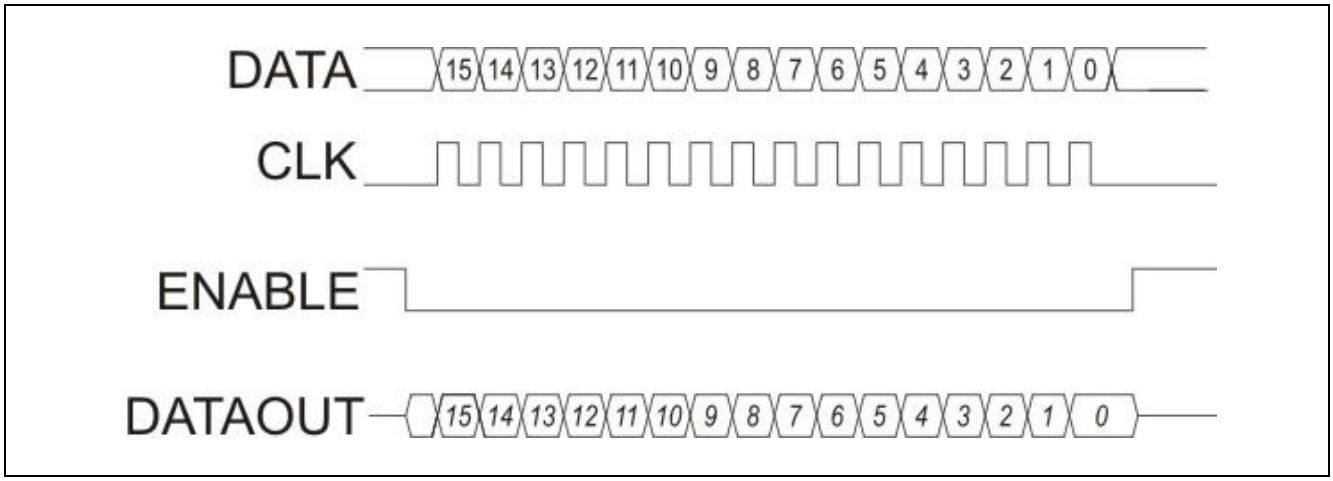


Figure 5 4-wire SPI Interface Transmission Scheme.

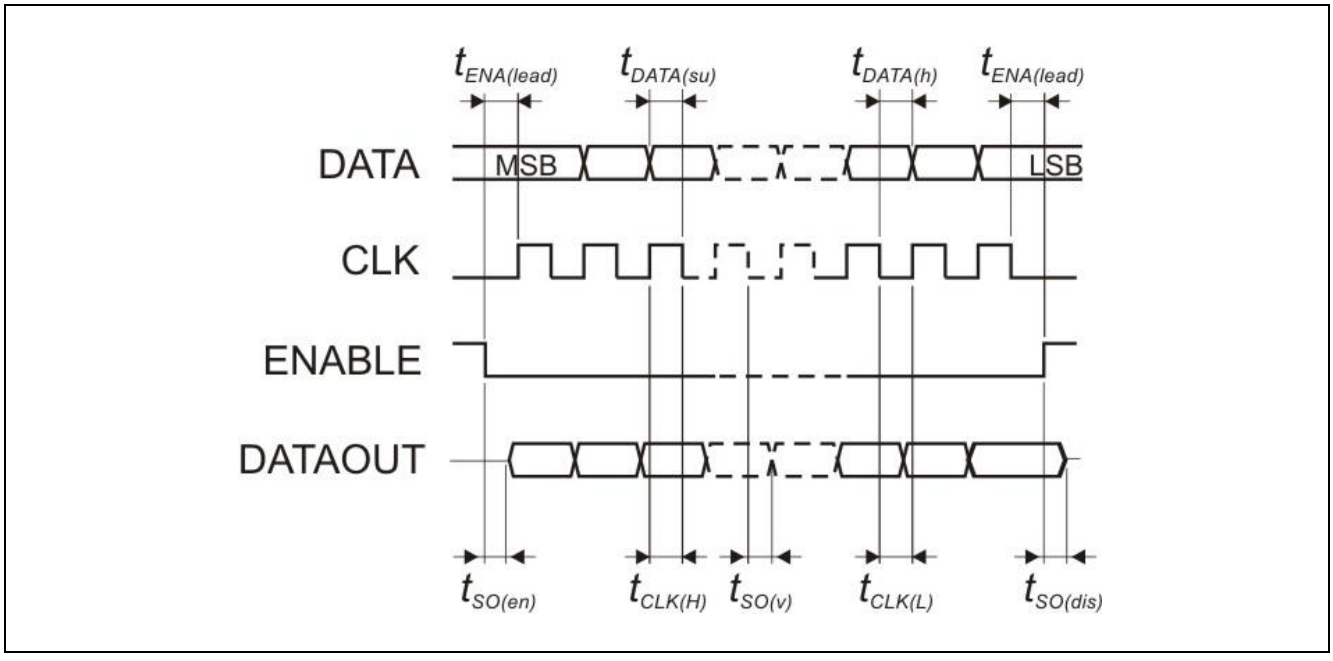


Figure 6 4-wire SPI interface timing diagram

Table 12 **Timing Characteristics**, Vcc= 3.135 to 3.465V, T_b=-40 °C to 85 °C, ambient temperature not below -40 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Limit Values			Unit
		Min.	Typ.	Max.	
Serial clock frequency	f_{CLK}			50	MHz
Serial clock high time	$t_{CLK(H)}$	10			ns
Serial clock low time	$t_{CLK(L)}$	10			ns
Enable lead time	$t_{ENA(lead)}$	20			ns
Enable select lag time	$t_{ENA(lag)}$	20			ns
Data setup time	$t_{DATA(su)}$	10			ns
Data hold time	$t_{DATA(h)}$	10			ns
Clock to serial output valid time (Load capacitance ≤20pF)	$t_{SO(v)}$			20	ns
Enable to serial output active time	$t_{SO(en)}$			100	ns
Enable to serial output high impedance time	$t_{SO(dis)}$			100	ns

4.4 Logic Levels

The digital inputs are designed to be compatible with standard CMOS / TTL levels (reported in **Table 13**). Unconnected input pins are at HIGH level. I/O interface is shown in **Figure 7 to Figure 10.**

Table 13 **Logic levels for pins DATA, DATAOUT, CLK, and ENABLE**, Vcc= 3.135 to 3.465V, T_b=-40 °C to 85 °C, ambient temperature not below -40 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified).

Parameter	Symbol	Limit Values	Unit		
		Min.	Typ.	Max.	
LOW level / input (DATA, CLK, ENABLE)	$V_{IN(L)}$	0		0.8	V
HIGH level / input (DATA, CLK, ENABLE)	$V_{IN(H)}$	2.0		Vcc	V
Input current (0V ≤ V_{IN} ≤ Vcc)	I_{IN}	-150		150	µA
LOW level / output (DATAOUT)	$V_{OUT(L)}$	0		0.66	V
HIGH level / output (DATAOUT)	$V_{OUT(H)}$	Vcc – 0.66		Vcc	V
Output current (LOW)	$I_{OUT(L)}$	-1.5			mA
Output current (HIGH)	$I_{OUT(H)}$	1.5			mA

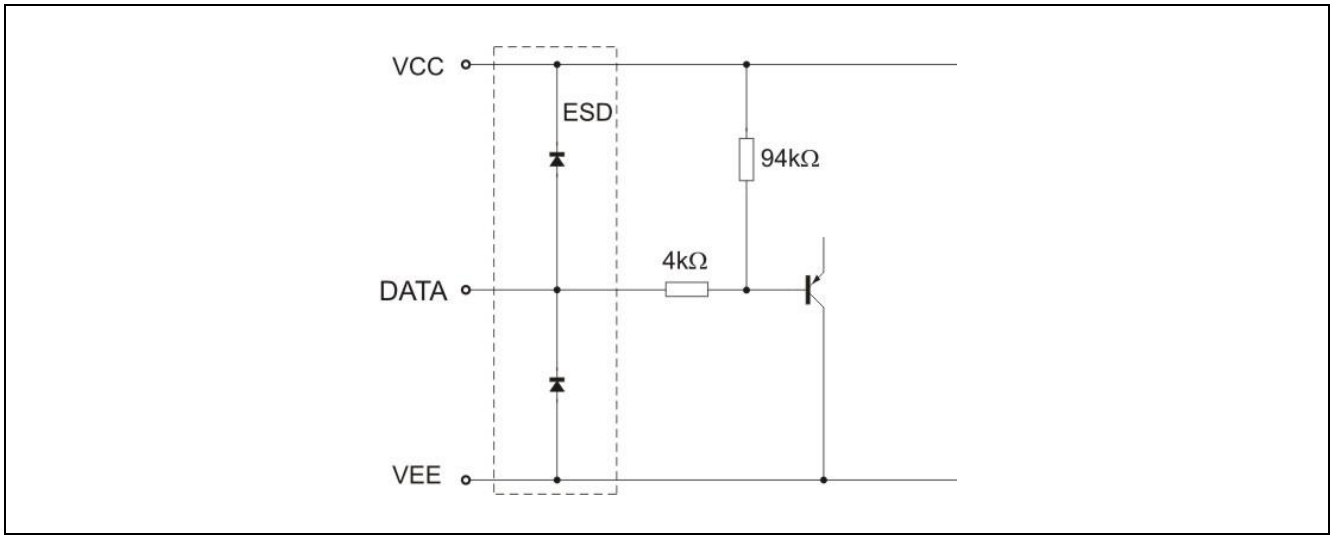


Figure 7 Data Input DATA

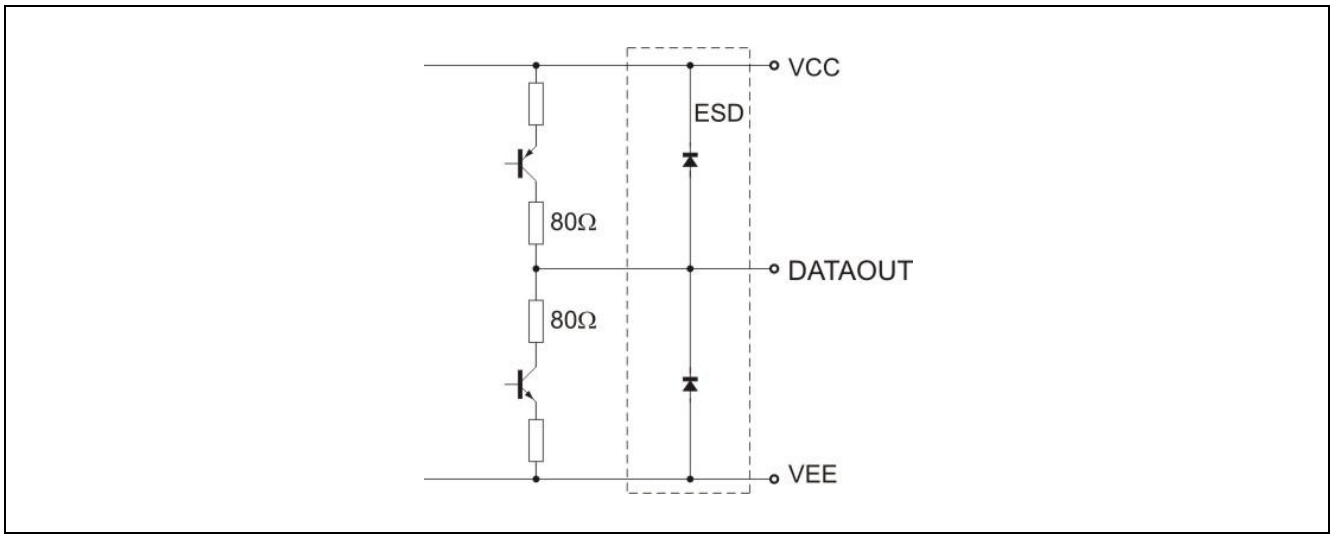


Figure 8 Data Output DATAOUT

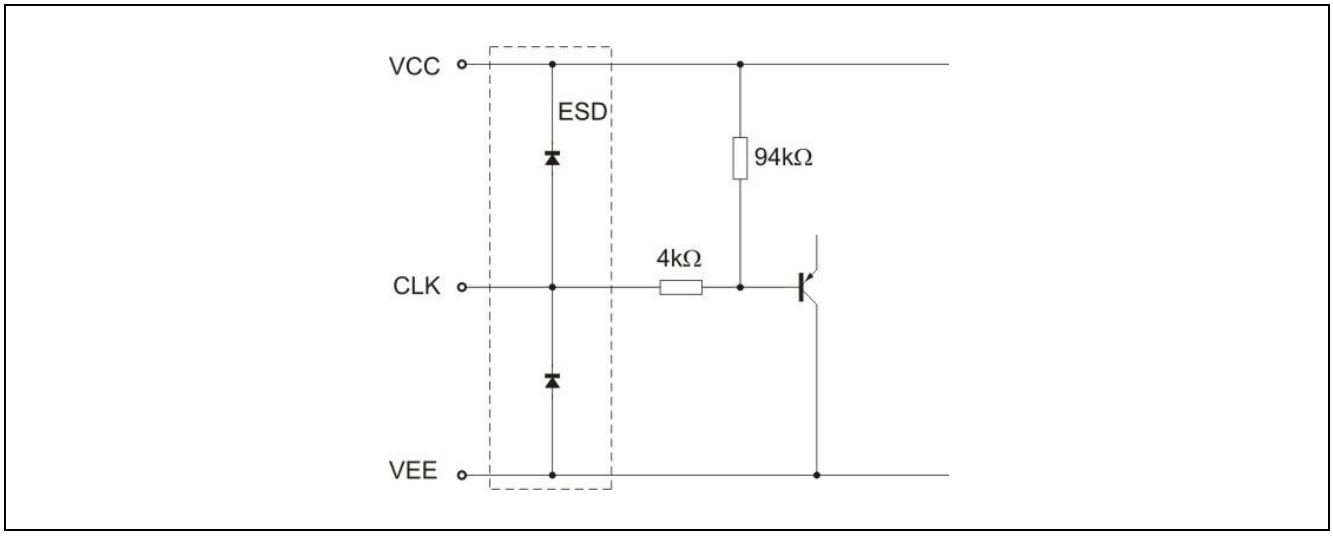


Figure 9 Clock Input CLK

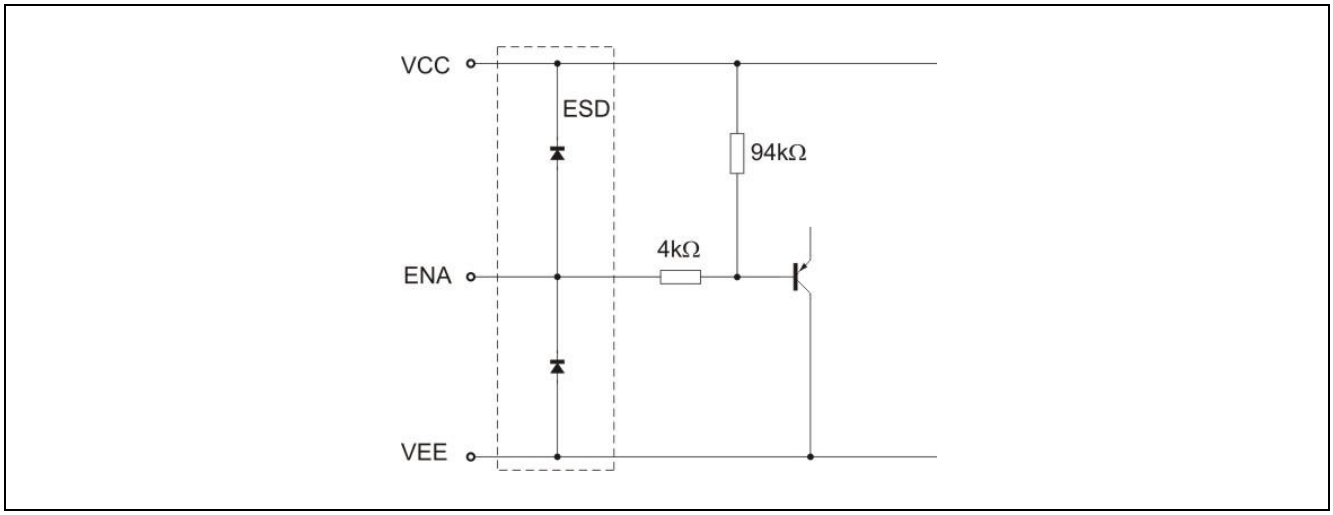


Figure 10 Enable Input ENABLE

4.5 Read Mode

Figure 11 shows a read command. The two most significant bits are set to 10_B to select the read mode, followed by three 0_Bs and three address bits (A2, A1 and A0) to select one of the six registers. The read sequence consists of two parts. In a first step, a read command is sent to the interface. The first most significant bit is set to 1_B followed by four bit set to 0_B, 10000_B, followed by three address bits (A2, A1 and A0) and eight data bits which may contain any arbitrary value. During the second part of the read sequence the selected 8-bit section is provided at DATAOUT. The command/address/data bits at DATA may contain any value.

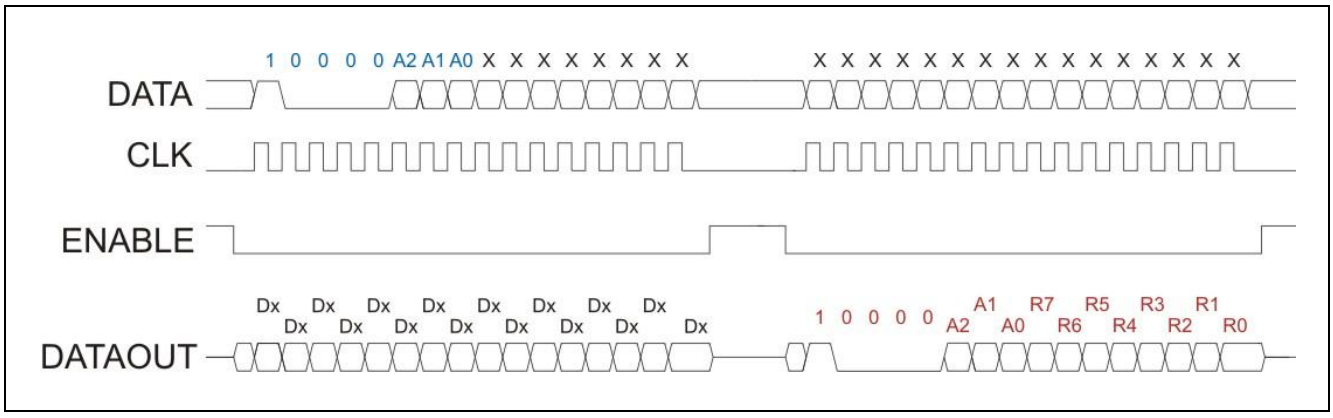


Figure 11 Read Mode Timing

4.6 Write Mode

Figure 12 shows a write command. The two most significant bits are 1_B to select the write mode, followed by three 0_Bs and three address bits (A2, A1 and A0) to select one of the six registers. The programming sequence is completed by eight data bits. While the 16-bit sequence consisting of

command/address and data is clocked into the interface, 16 bits are shifted out at DATAOUT. The content of these bits depends on the previous command. The content of these bits depends on the previous command. If the previous command was a ”Read chip-ID” the bits correspond to the selected 16-bit section of the chip ID (see section 4.7). If the previous command was a “Read” command then the content of the 8 lower bits corresponds to the content of the register that has been read. In all other cases the 16 bits at DATAOUT correspond to the previous command/address/data sequence.

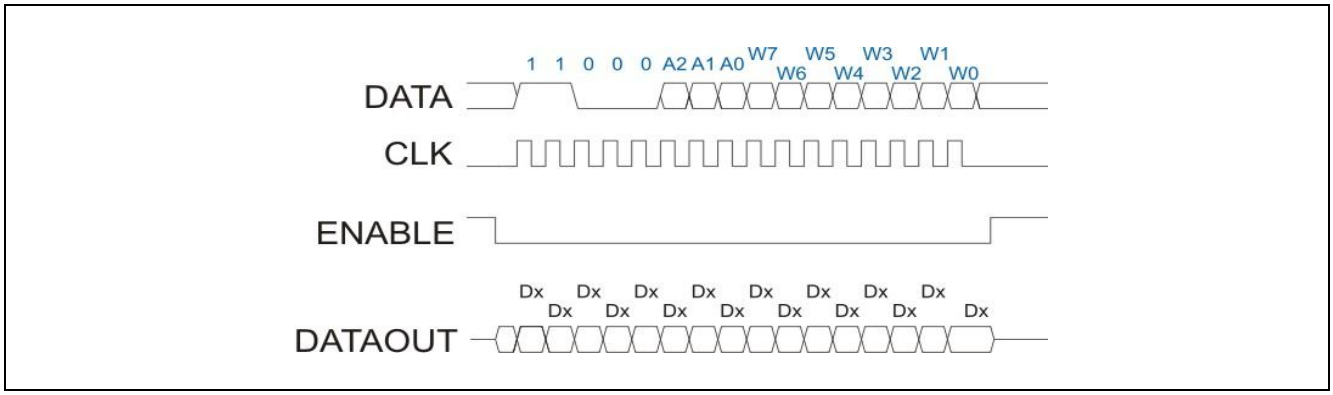


Figure 12 Write Mode Timing

4.7 Read Chip-ID Mode

Figure 13 shows a chip-ID read sequence. The chip-ID consists of 48 bits. It is read in three 16-bit sections, the section to be read is selected by two address bits (A1, A0). Valid addresses are 0_H to 2_H. The read sequence consists of two parts. In a first step, a read command is sent to the interface. The six most significant bits are 0_B, followed by two address bits (A1, A0) and eight data bits which may contain any arbitrary value. During the second part of the read chip-ID sequence the selected 16-bit section of the chip-ID is provided at DATAOUT. During the second part of the read chip-ID sequence the command/address/data bits at DATA may contain any value, as well as a further “Read chip-ID” command (next 16bits sequence), “Read” or “Write” command.

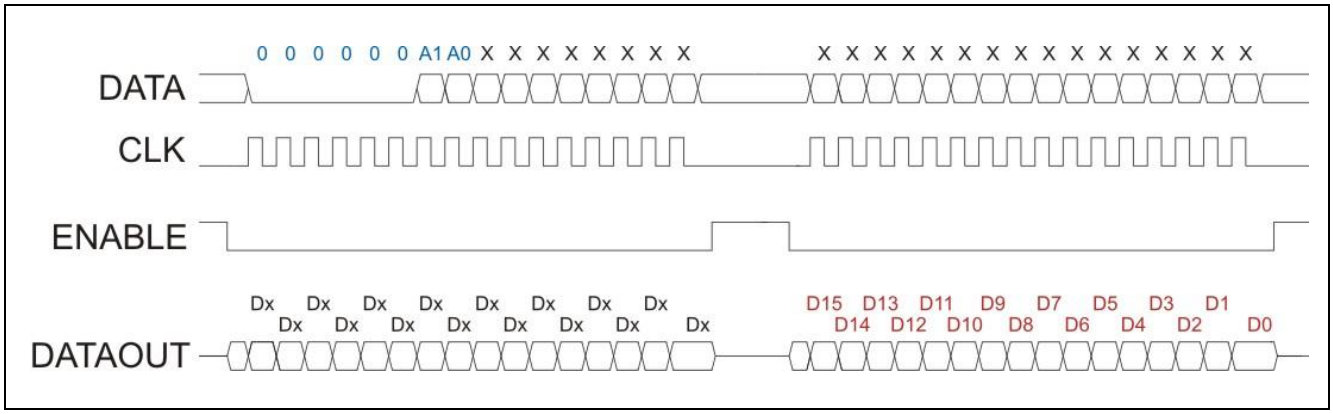


Figure 13 Read Chip-ID Mode Timing

BGT70 and BGT80 are identified by the bit 7 of the second (CMD 1_H) 16bits string of the Chip-ID read sequence. This bit is set to 0_B for BGT70 and 1_B for BGT80.

4.8 Register Map

In **table 4** an overview of the registers is presented.

Table 14 Register Map

Register	Register Address	Register Short Name	Function	Description
0	000000_B	VGA	VGA control	See section 4.8.1
1	000001_B	Tx_MOD_I	DAC channel I control	See section 4.8.2
2	000010_B	Tx_MOD_Q	DAC channel I control	See section 4.8.3
3	000011_B	General	Tx chain, Rx chain control	See section 4.8.4
4	000100_B	MUX	MUX control, Buffer PPD_MOD	See section 4.8.5
5	000101_B	not used		

4.8.1 Register VGA

The register is used to control the VGA in the transmitter chain.

7	6	5	4	3	2	1	0
sw_Buff_VGA	sw_DAC_VGA	DAC_VGA					

Table 15 Register VGA

Field	Bit	Type	Description	Reset Value
sw_Buff_VGA	7	rw	Enable/disable the buffer which drives the power amplifier 1_B enabled 0_B disabled	0_B
sw_DAC_VGA	6	rw	Enable/disable the DAC which sets the VGA 1_B enabled 0_B disabled	0_B
DAC_VGA	5:0	rw	Variable gain amplifier control / output power control 111111_B highest output power 000000_B lowest output power sw_Buff_VGA	000000_B

4.8.2 Register Tx_MOD_I

The register is used to control the DAC which is used to calibrate the channel I of the I/Q modulator in the transmitter chain.

7	6	5	4	3	2	1	0
n.u.	sw_DAC_I	DAC_MOD_I					

Table 16 Register Tx_MOD_I

Field	Bit	Type	Description	Reset Value
n.u.	7	rw	Not used	0_B
sw_DAC_I	6	rw	Enable/disable the DAC which calibrates the channel I of the Tx modulator. 1_B enabled 0_B disabled	0_B
DAC_MOD_I	5:0	rw	DAC_I current for modulator calibration 111111_B highest added current 000000_B lowest subtracted current	000000_B

4.8.3 Register Tx_MOD_Q

The register is used to control the DAC which is used to calibrate the channel Q of the I/Q modulator in the transmitter chain.

7	6	5	4	3	2	1	0
n.u.	sw_DAC_Q	DAC_MOD_Q					

Table 17 Register Tx_MOD_Q

Field	Bit	Type	Description	Reset Value
n.u.	7	rw	Not used	0_B
sw_DAC_Q	6	rw	Enable/disable the DAC which calibrates the channel Q of the Tx modulator. 1_B enabled 0_B disabled	0_B
DAC_MOD_Q	5:0	rw	DAC_Q current for modulator calibration 111111_B highest added current 000000_B lowest subtracted current	000000_B

4.8.4 Register General

The register is used to activate/deactivate several blocks in the transmitter chain as well in the receiver chain. The last bit is used to enable the PA.

7	6	5	4	3	2	1	0
sw_PA	n.u.	sw_Buff_Mod	MOD_I	MOD_Q	sw_LO_TX	sw_LO_RX	RX_SPI

Table 18 Register General

Field	Bit	Type	Description	Reset Value
sw_PA	7	rw	Enable/disable the power amplifier 1_B enabled 0_B disabled	0_B
n.u.	6	rw	Not used	0_B
sw_Buff_Mod	5	rw	Enable/disable the channel I of the transmitter I/Q modulator. 1_B enabled 0_B disabled	0_B
MOD_I	4	rw	Enable/disable the channel I of the transmitter I/Q modulator. 1_B enabled 0_B disabled	0_B
MOD_Q	3	rw	Enable/disable the channel Q of the transmitter I/Q modulator. 1_B enabled 0_B disabled	0_B
sw_LO_TX	2	rw	Enable/disable the blocks of the local oscillator distribution network which drives the Tx chain. 1_B enabled 0_B disabled	0_B
sw_LO_RX	1	rw	Enable/disable the blocks of the local oscillator distribution network which drives the Rx chain. 1_B enabled 0_B disabled	0_B
RX_SP	0	rw	Enable/disable the Rx chain. 1_B enabled 0_B disabled	0_B

4.8.5 Register MUX

The register is used to mux the outputs of the two peak detectors in the power amplifier chain. This register is also use to activate/deactivate the wideband buffer connected directly at the output of the modulator peak detector.

7	6	5	4	3	2	1	0
n.u.	n.u.	n.u.	n.u.	n.u.	SPI_buf_dec	MUX	MUX

Table 19 Register MUX

Field	Bit	Type	Description	Reset Value
n.u.	7	rw	Not used	0_B
n.u.	6	rw	Not used	0_B
n.u.	5	rw	Not used	0_B
n.u.	4	rw	Not used	0_B
n.u.	3	rw	Not used	0_B
D_MOD	2	rw	Enable/disable the broadband output buffer of the modulator envelope detector (AC out) 0_B enabled 1_B disabled	1_B
MUX out	1:0	rw	Select output either from PPD PA or from PPD buffer MOD 00_B PPD_MOD output enabled 01_B PPD_PA output enabled	00_B

5 Application Board

Figure 14 shows the top view of the layout of the application board for BGT80. For specific info about the BGT80 board design please refer to the Infineon application note *AN338* and to the reccomendation for eWLB assembly included in the document: *Recommendations for Printed Circuit Board Assembly of Infineon xWLy Packages*.

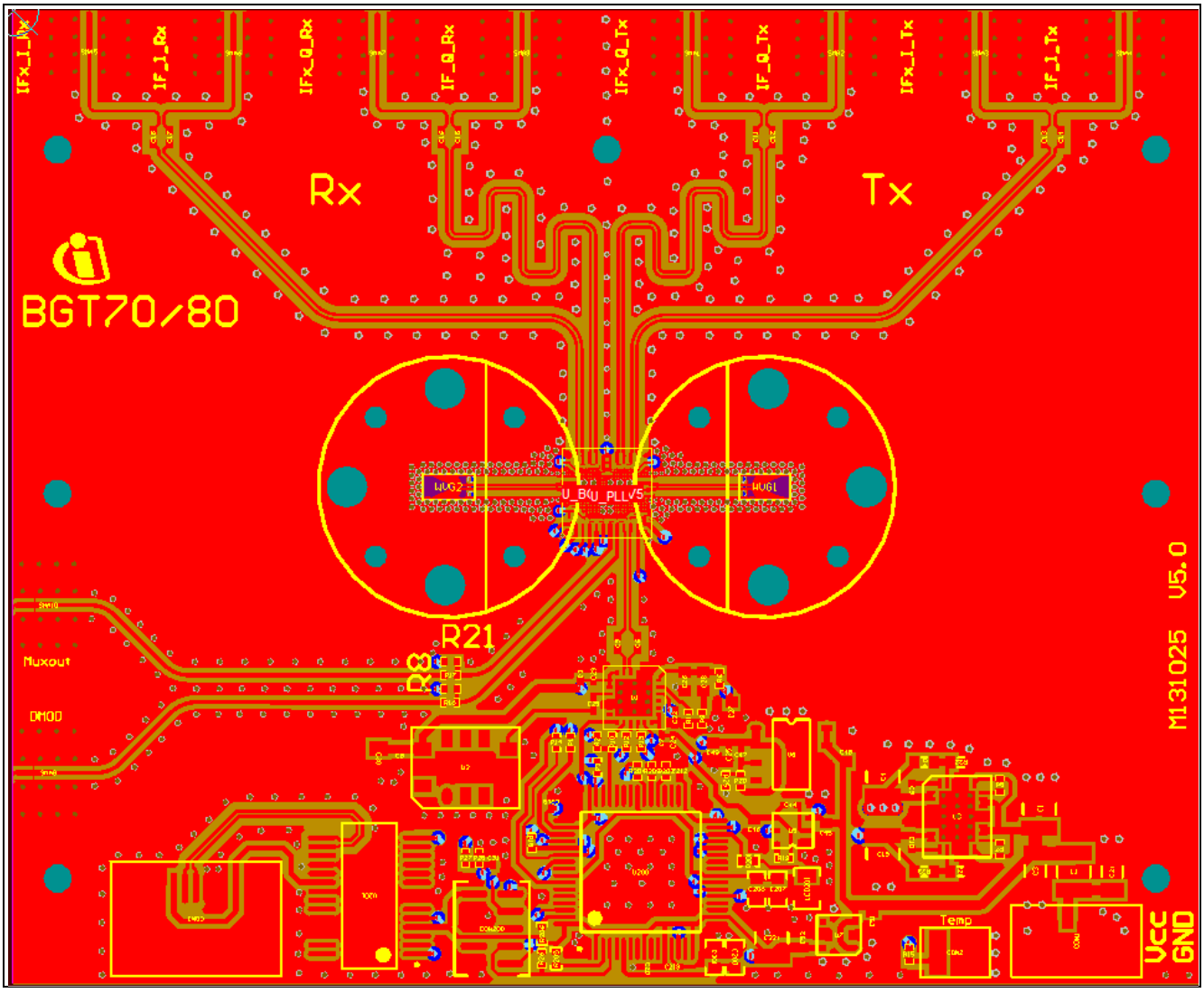


Figure 14 Top view of the Application Board BGT80

Figure 15 shows the top view picture of BGT80 after assembly. IF interface can be connected via the SMA ports (upper side). On-Board mode conversion circuits (differential <-> single mode) are implemented for the RF Tx and Rx ports. The Tx port is on the middle right side and Rx port on the middle left side. They can be connected with WR-12 waveguides. Down left side are the sense pins while the DC supply pins are on the bottom right corner. **Figure 16** presents the schematic of the application circuit while **Figure 17** the schematic of the PLL circuit implemented on the EVB.

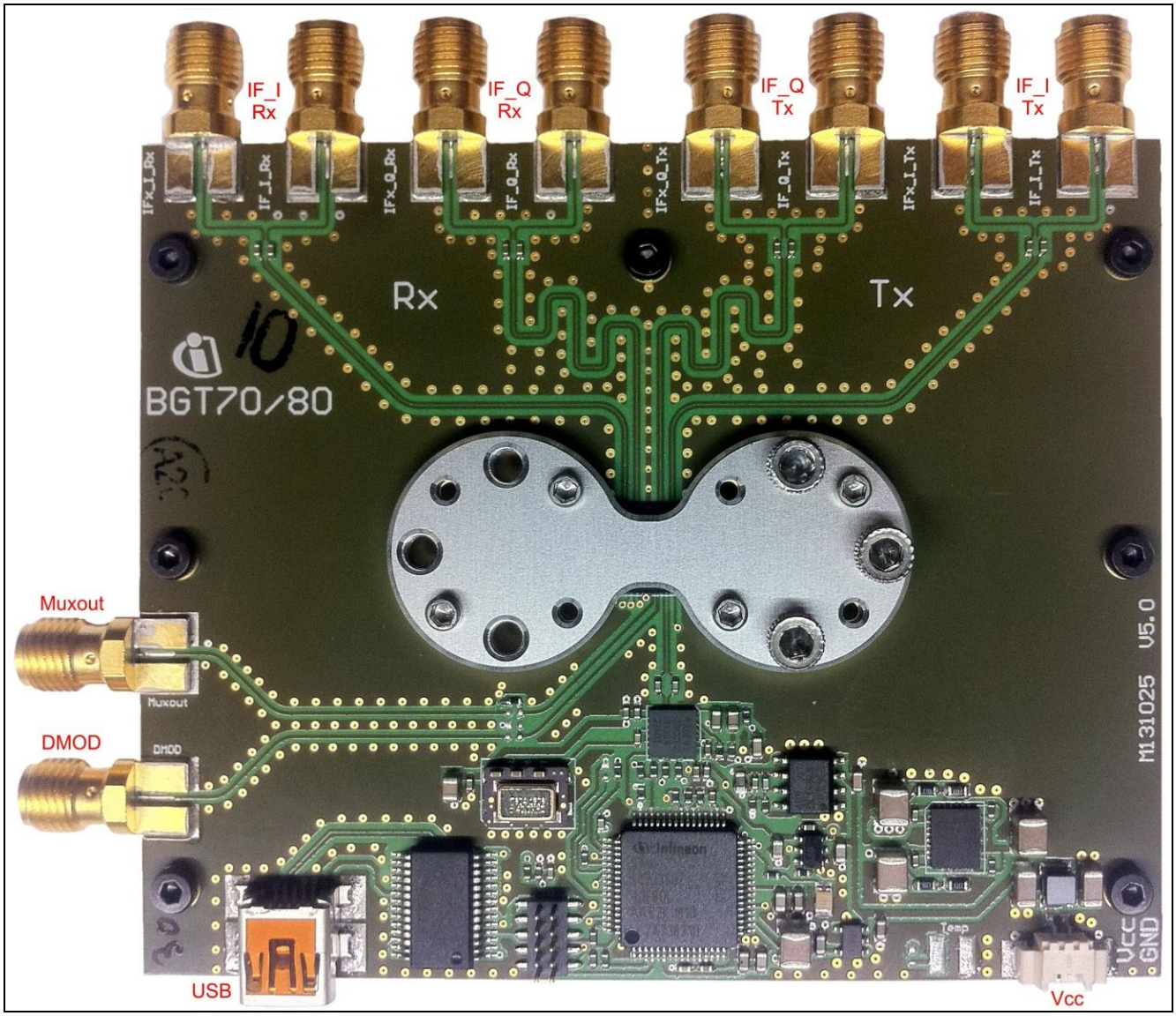


Figure 15 Picture of Application Board for BGT80 after Assembly

Table 20 Control Interface Description of BGT80 Application Board

Pin	Function	Description
DC Header		
Vcc	DC supply	6 V
Muxout	DC output	PPD_PA or PPD_MOD
DMOD	Broadband, 250MHz, AC output	PPD_MOD
IF_I_Rx/IF_Q_Rx	AC output	IF differential IQ Rx signals
IF_I_Tx/IF_Q_Tx	AC input	IF differential IQ Tx signals

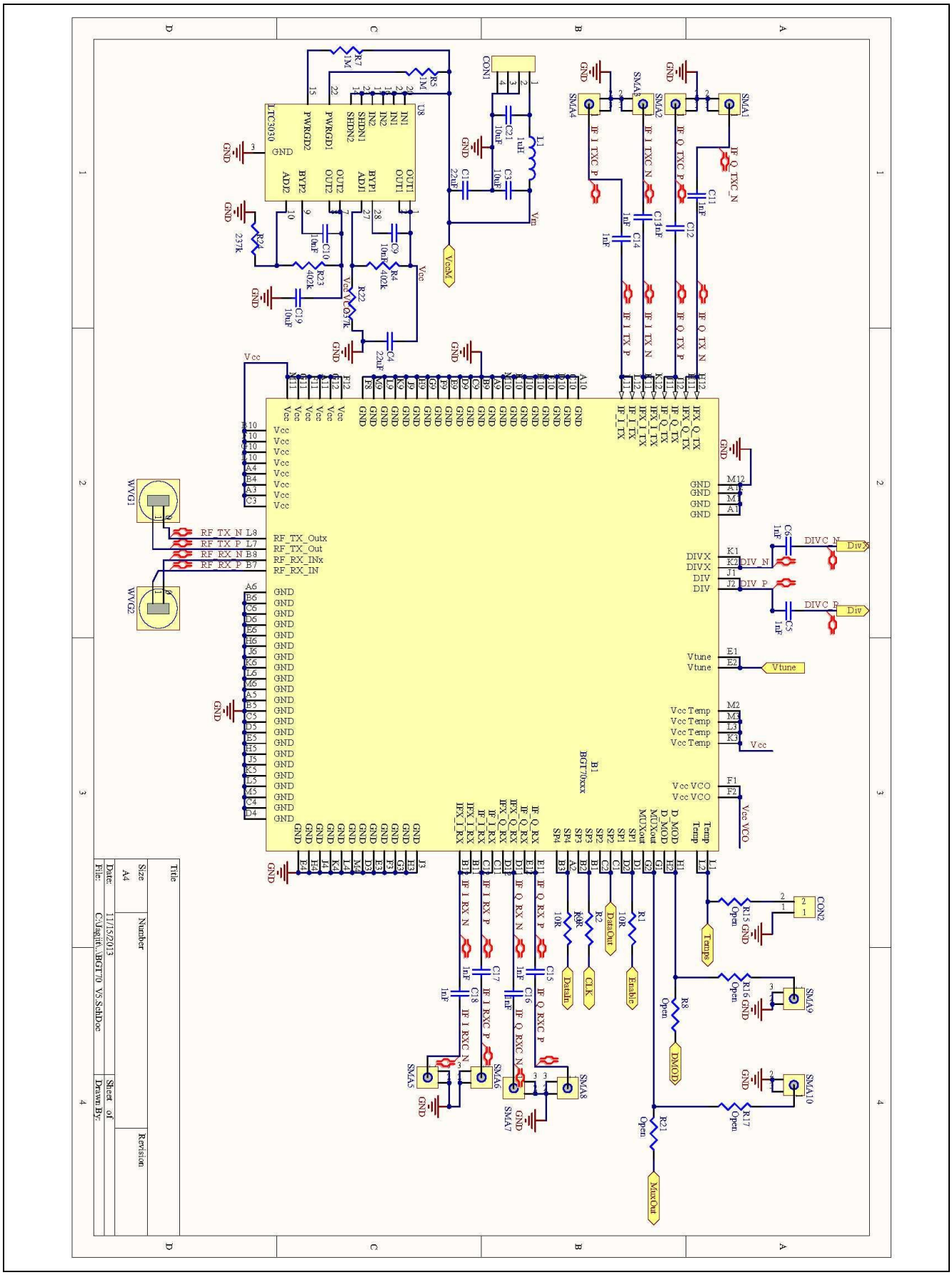


Figure 16 Schematic of BGT80 Application Circuit

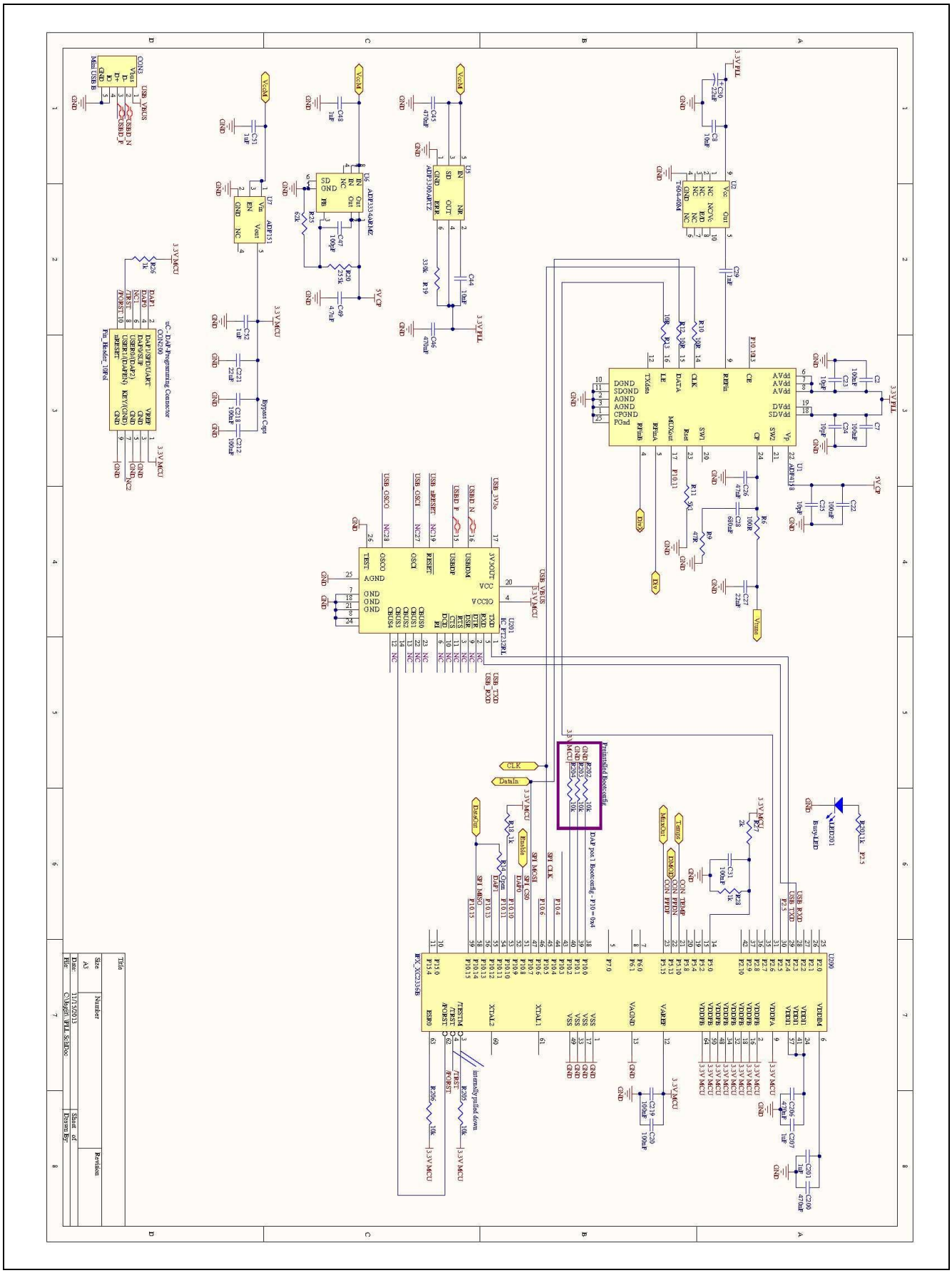


Figure 17 PLL Schematic used on BGT80 Evaluation Board

5.1 Bill-of-Materials

Table 10 below shows the Bill-of-Material for application board BGT80.

Designator	Part Number	Package	Quantity
U1	ADF4158	LFCSP	1
U7	ADP151AUJZ-3.3-R7	TSOT-5	1
U5	ADP3300ARTZ-3.3RL7	SOT-23	1
U6	ADP3334ARMZ	SOIC-8	1
B1		BGT70	1
C200, C206	470nF	0603	2
C201, C207	1uF	0603	2
C30	22uF	0805	1
C1, C4, C221	22uF	1210	3
C19	10uF	1210	1
C2, C7, C20, C22, C212, C218, C219	100nF	0402	7
C23, C24, C25	10pF	0402	3
C26	47nF	0603	1
C27	22nF	0603	1
C28	680nF	0603	1
C29	1nF	0402	1
C3, C21	10uF	1206	2
C31	100nF	0402	1
C45, C46	470nF	0603	2
C47	100pF	0402	1
C48	1uF	0603	1
C49	4.7uF	0603	1
C5, C6, C11, C12, C13, C14, C15, C16, C17, C18	1nF	0402	10
C51, C52	1uF	0603	2
C8, C9, C10, C44	10nF	0402	4
CON2		2x1 connector	1
SMA1, SMA2, SMA3, SMA4, SMA5, SMA6, SMA7, SMA8	SMA	Edge Launch SMA	8
SMA9, SMA10		Edge Launch SMA	2
U201	FT232RL	SSOP-28	1
U200	SAK-XC2336B-40F80L AA	QFP127P600-8N	1
L1	1uH (1210)	1210	1
LED201	LED	0805	1
U8	LT3030EUFD#PBF	LT3030	1
CON3		Mini USB	1
CON1	Molex	Molex 2 Pin	1
CON200	DAP_CON	DAP_CON	1
R1, R2, R3, R10, R12, R13	10R	0402	6
R11	5k1	0402	1
R18, R26, R28, R201	1k	0402	4
R19	330k	0402	1
R20	255k	0402	1
R202, R203, R204, R205, R206	10k	0402	5
R22, R24	237k	0603	2
R25	62k	0402	1
R27	2k	0402	1
R4, R23	402k	0603	2
R5, R7	1M	0402	2
R6	100R	0402	1
R8, R14, R15, R16, R17, R21	Open	0402	6
R9	47R	0402	1
U2	T604-040.0M	T604-40M	1

6 Package

The BGT80 chipset is in eWLB type package PG-WFWLB-119-1 with bump balls of diameter of 300 µm and height of 150 µm. According to IPC/JEDEC's J-STD-20, the moisture sensitivity level, MSL, is 1. **Figure 18** shows the BGT80 package. **Figure 19** shows the physical dimension of it. The package size is 6.0 x 6.0 x 0.8 mm³ with pitch of 500 µm.

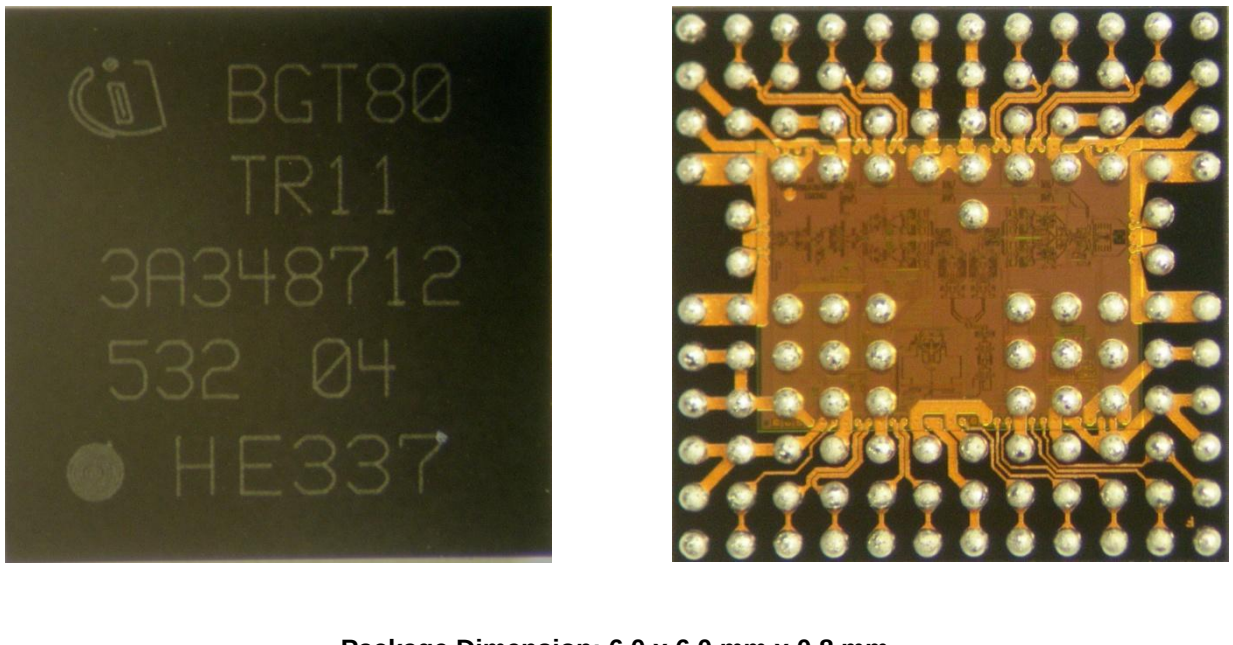


Figure 18 Top View (left), Bottom View (right) of BGT80 in eWLB Package

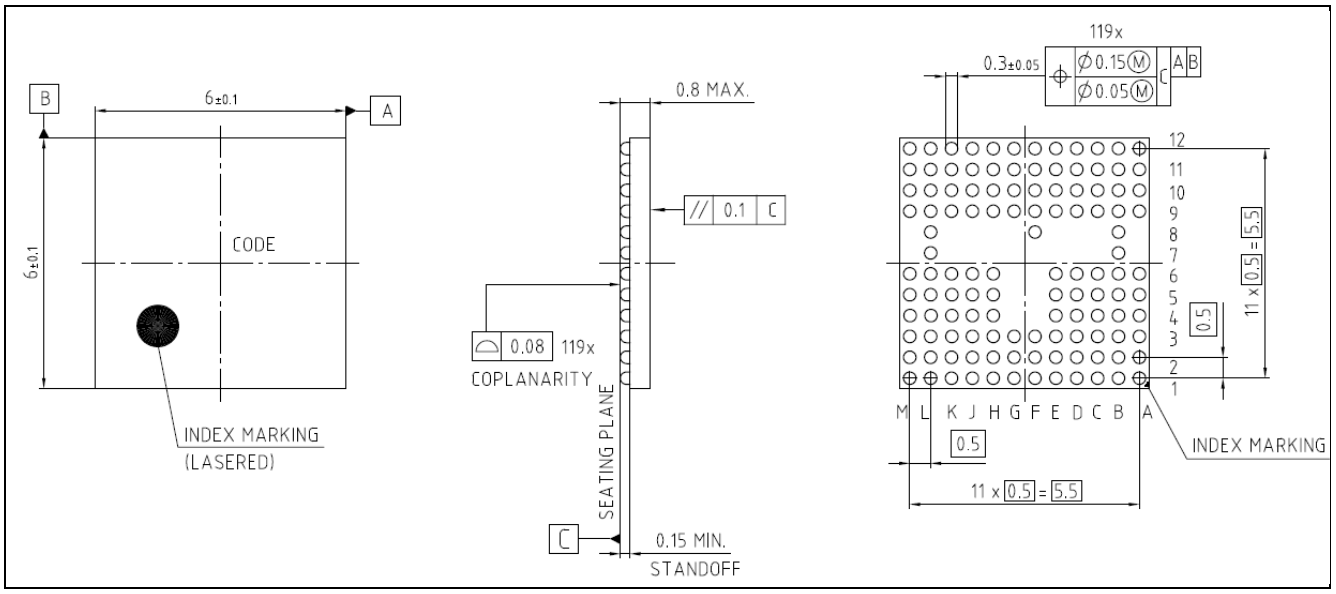
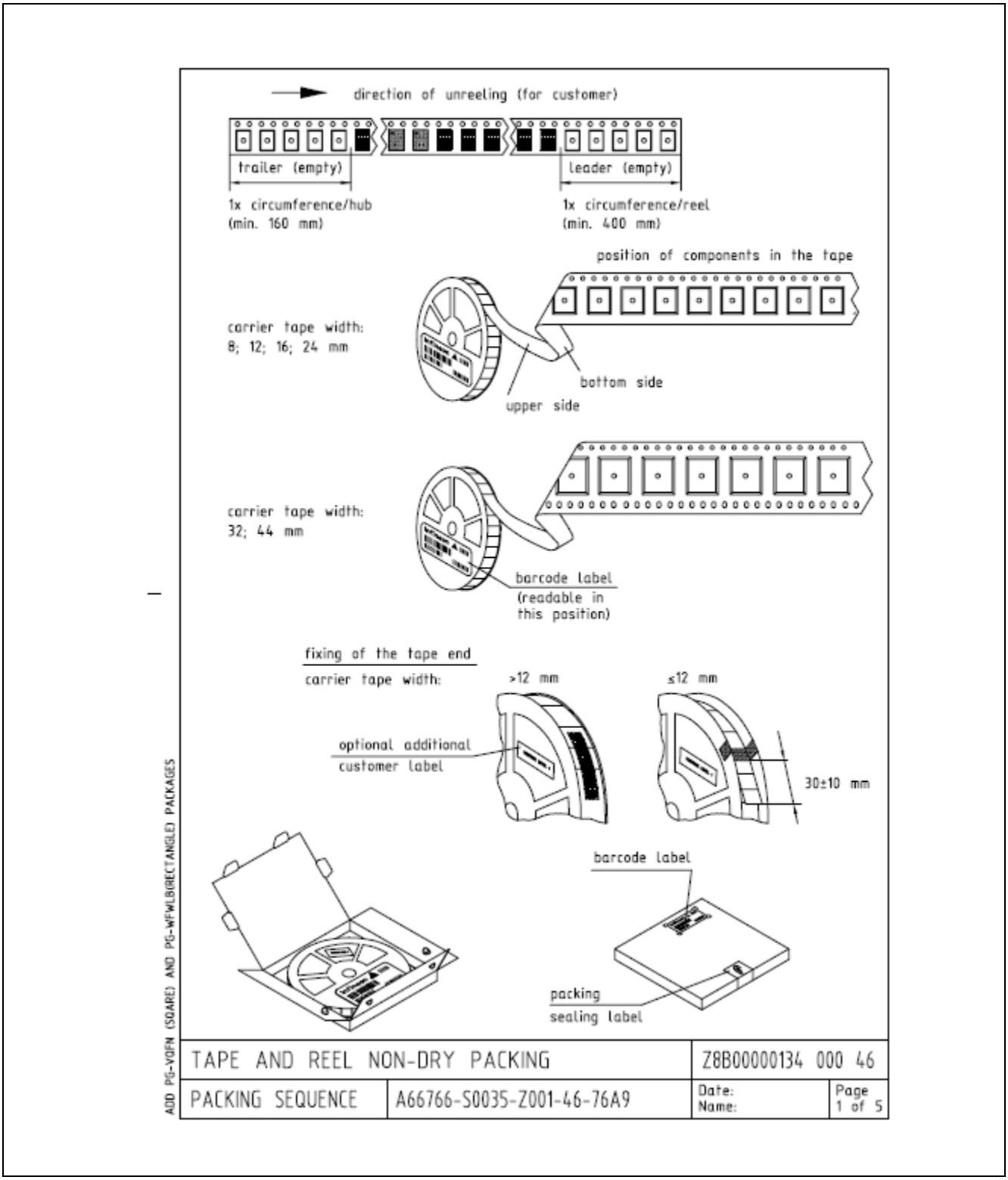


Figure 19 Dimension of eWLB Package PG-WFWLB-119-1 for BGT80 (left: top view; center: side view; right: bottom view)

Tape and reel information:

- Solder balls at bottom side, marking at top side
- 3000 pcs per reel



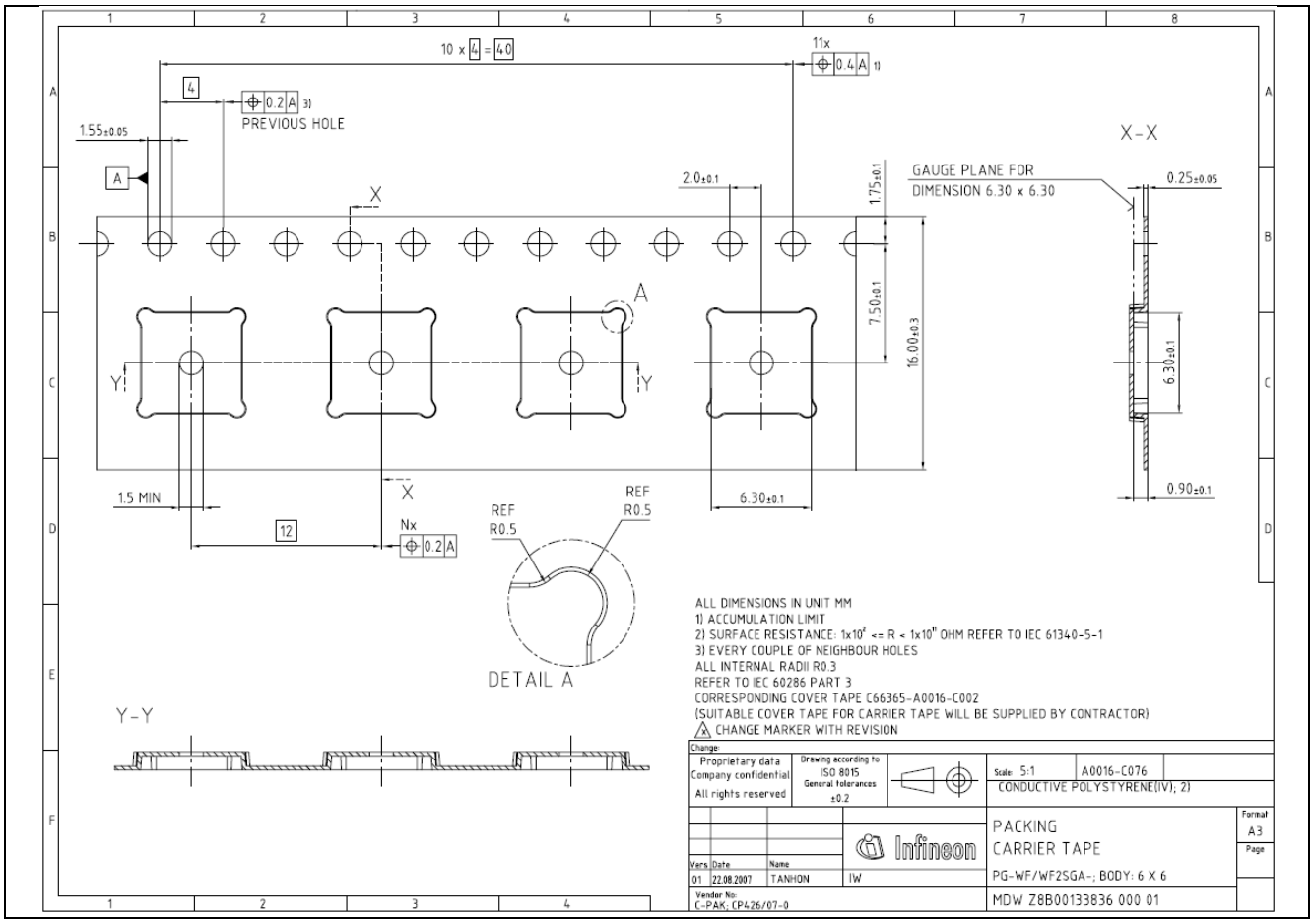


Figure 20 Tape and Reel Information of BGT80 in eWLB Package

w w w . i n f i n e o n . c o m

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