2-Gbps DIFFERENTIAL SWITCH 8-Bit, 1:2 MULTIPLEXER/DEMULTIPLEXER WITH 3-SIDE BAND SIGNALS

Check for Samples: TS3DV20812

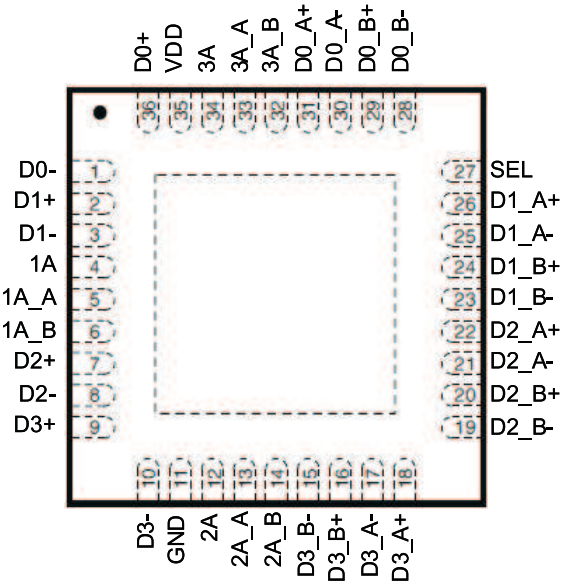
FEATURES

- Four High-Speed Bidirectional Differential Pair Channel MUX/DEMUX
- Supports up to 2 Gbps Data Rate
- V_{DD} Operating Range 2.5 V or 3.3
  - -0 V to 3.3 V Rail To Rail at 2.5 V
  - -0 V to 5 V Rail To Rail at 3.3V
- I_{OFF} partial Powerdown and Back-Drive Protection.
- 5-V Input Tolerant on Control Pin
- Supports Both AC- and DC-Coupled Signals
- Low Crosstalk: -38 dB at 825 MHz, 2.5 V or 3.3 V
- Insertion Loss: -1.5 dB at 825 MHz, 2.5 V or 3.3 V
- Off Isolation -24.67 dB at 825 MHz
- Low Bit-to-Bit Skew within Pair 5 ps Maximum
- Channel-to-Channel Skew: 30 ps Maximum
- Propagation Delay Times: 250 ps Maximum
- ESD Performance Tested per JESD 22
  - 2000-V Human Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

APPLICATIONS

- HDMI/DVI Video MUX
- Panel LVDS Bus MUX
- LVDS, LVPECL, CML
- Analog Signals VGA
- Gigabit LAN Signal MUX
- Serial Backplane Signal MUX
- Optical Module
- Central Office Telecommunication
- Wireless Base Station
- High-Speed Logic Data I/O MUX

RHH PACKAGE
(TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

TS3DV20812 is a High Speed Data Rate up to 2Gbps for Differential Signal Passive bi-directional Multiplexer and De-multiplexer for I/O rails up to 5V Level with Low Crosstalk and Insertion Loss.

TS3DV20812 can be used in either HDMI/DVI sink side or source side with 4-differential pair supporting the high speed and control pins.

The Ioff and back drive protection allowing to connect the external cable and prevent the back flow current when the Vcc is into 0V.

The 3 side band signals can be used in DDC (SDAL, SCL) and CEC Signal MUX.

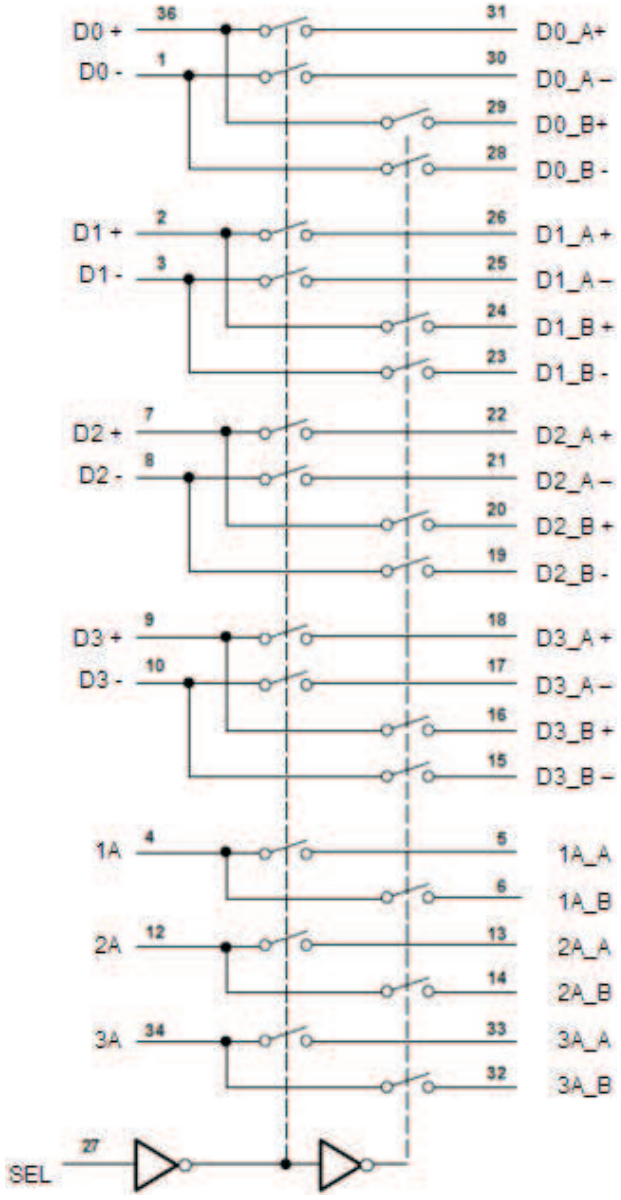
TS3DS20812 is characterized for operation from -40C to 85C.

Table 1. ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN – RHH	Tape and reel	TS3DV20812RHH	TBD

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

LOGIC DIAGRAM



FUNCTION TABLE

INPUT SEL	DIFFERENTIAL SIGNAL I/Os	FUNCTIONS	
		A-PORT	B-PORT
L	Dn (±), nA (AUX (±), HPD, CAD/CEC)	DnA (±), nA_A	High-impedance mode
H		High-impedance mode	DnB (±), nA_B

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range		–0.5	4.6	V
V_{IN}	Control input voltage range(2)(3)	SEL	–0.5	7	V
		I/O	–0.5	7	V
V_{IO}	Switch I/O voltage range (all three I/O ports)(4)	D0-D3, Aux, HPD, CAD/CEC	–0.5	V_{CC} + 0.5	V
		A port and B port	–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_{IN} < 0		–50	mA
$I_{I/OK}$	I/O port clamp current	V_O < 0		–50	mA
I_{IO}	Continuous output current(5)	ON-state switch		±128	mA
	Continuous current through VDD or GND			±100	mA
Θ_{JA}	Package thermal impedance(6)	RHH package		31.8	°C/W
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) V_I and V_O are used to denote specific conditions for V_{IO}.
(5) I_I and I_O are used to denote specific conditions for I_{IO}.
(6) The package thermal impedance is calculated in accordance with JESD 51-7.

RECOMMENDED OPERATING CONDITIONS

			MIN	MAX	UNIT
V_{DD}	Supply voltage		2.25	3. 6	V
V_{IH}	High-level control input voltage	SEL	2	5.5	V
V_{IL}	Low-level control input voltage	SEL	0	0.8	V
$V_{I/O}$	Input/output voltage	All ports	0	5.5	V
V_{ANALOG}	Analog signal range	Differential signal range	0	V_{DD}	V
V_I	Input tolerant	SEL	0	5.5	V
T_A	Operating free-air temperature		–40	85	°C

ELECTRICAL CHARACTERISTICS

for high-frequency switching over recommended operating free-air temperature range V_{DD} = 3.3 V ± 0.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{DD} = 3.6 V,	I_{IN} = –18 mA			–0.7	–1.2	V
I_{IH}	SEL	V_{DD} = 3.6 V,	V_{IN} = V_{DD}				±1	µA
I_{IL}	SEL	V_{DD} = 3.6 V,	V_{IN} = GND				±1	µA
I_{OFF}		V_{DD} = 06 V,	V_O = 0 to 3.6 V ,	V_I = 0 , V_{IN} = 0			1	µA
I_{CC}		V_{DD} = 3.6 V,	I_{IO} = 0	Switch ON or OFF		250	500	µA
C_{IN}	SEL	f = 10 MHz ,	V_{IN} = 0			2	2.5	pF
C_{OFF}	3-Port	f = 10 MHz ,	V_{IN} = 0 ,	Output is Open, Switch is OFF		2.5	4	pF
C_{ON}	3-Port	f = 10 MHz ,	V_{IN} = 0 ,	Output is Open, Switch is ON		8		pF
r_{ON}		V_{DD} = 3.6 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		4	6	Ω
$r_{ON(flat)}$ (3)		V_{DD} = 3.6 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		0.5		Ω
Δ r_{ON} (4)		V_{DD} = 3.6 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		0.4	1	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 3.3 V (unless otherwise noted), T_A = 25°.
(3) r_{ON}(flat) is the difference of r_{ON} in a given channel at specified voltages.
(4) Δr_{ON} is the difference of r_{ON} from center (D0 to Dn) ports to any other port.

ELECTRICAL CHARACTERISTICS

for high-frequency switching over recommended operating free-air temperature range V_{DD} = 2.5 V ± 0.25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)			MIN	TYP(2)	MAX	UNIT
V_{IK}	SEL	V_{DD} = 2.5 V ,	I_{IN} = –18 mA			–0.7	–1.2	V
I_{IH}	SEL	V_{DD} = 2.5 V ,	V_{IN} = V_{DD}				±1	µA
I_{IL}	SEL	V_{DD} = 2.5 V ,	V_{IN} = GND				±1	µA
I_{OFF}		V_{DD} = 06 V,	V_O = 0 to 2.5 V ,	V_I = 0 , V_{IN} = 0			1	µA
I_{CC}		V_{DD} = 2.5 V ,	I_{IO} = 0	Switch ON or OFF		250	500	µA
C_{IN}	SEL	f = 10 MHz ,	V_{IN} = 0			2	2.5	pF
C_{OFF}	3-Port	f = 10 MHz ,	V_{IN} = 0 ,	Output is Open, Switch is OFF		2.5	4	pF
C_{ON}	3-Port	f = 10 MHz ,	V_{IN} = 0 ,	Output is Open, Switch is ON		8		pF
r_{ON}		V_{DD} = 2.5 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		4	6	Ω
$r_{ON(flat)}$ (3)		V_{DD} = 2.5 V	V_I = 1.5 V and V_{DD},	I_O = –40 mA		0.5		Ω
Δ r_{ON} (4)		V_{DD} = 2.5 V	1.5 V ≤ V_I ≤ V_{DD},	I_O = –40 mA		0.4	1	Ω

(1) V_I, V_O, I_I, and I_O refer to I/O pins, V_{IN} refers to the control inputs.
(2) All typical values are at V_{DD} = 2.5 V (unless otherwise noted), T_A = 25°.
(3) r_{ON}(flat) is the difference of r_{ON} in a given channel at specified voltages.
(4) Δr_{ON} is the difference of r_{ON} from center (D0 to Dn) ports to any other port.

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figure 9 and Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	Dn	D_A or D_B		149		ps
t_{PZH}, t_{PZL}	SEL	D_A or D_B	0.5		15	ns
t_{PHZ}, t_{PLZ}	SEL	D_A or D_B	0.9		12	ns
SEL to switch turn on time		D_A or D_B		9	14	ns
SEL to switch turn off time		D_A or D_B		5	11	ns
$t_{sk(o)}$ (3)	Dn (+)(-), DA(+)(-), DB(+)(-)			22	28	ps
$t_{sk(o)}$	Dn (all), DnA(all), DnB(All)			19	25	ps
$t_{sk(p)}$(4)				22	31	ps

(1) All typical values are at V_{DD} = 2.5 V (unless otherwise noted), T_A = 25°.
(2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port to any other port.
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 2.5V ± 0.25 V, R_L = 200 Ω, C_L = 10 pF (unless otherwise noted) (see Figure 9 and Figure 10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP(1)	MAX	UNIT
t_{pd}(2)	Dn	D_A or D_B		149		ps
t_{PZH}, t_{PZL}	SEL	D_A or D_B	0.5		14	ns
t_{PHZ}, t_{PLZ}	SEL	D_A or D_B	0.9		15	ns
SEL to switch turn on time		D_A or D_B		9	17	ns
SEL to switch turn off time	D_A or D_B	D_A or D_B		5	18	ns
$t_{sk(o)}$ (3)	Dn (+)(-), DA(+)(-), DB(+)(-)			22	31	ps
$t_{sk(o)}$	Dn (all), DnA(all), DnB(All)			19	23	ps
$t_{sk(p)}$(4)				22	33	ps

(1) All typical values are at V_{DD} = 2.5 V (unless otherwise noted), T_A = 25°.
(2) The propagation delay is the calculated RC time constant of the typical ON-State resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(3) Output skew between center port to any other port.
(4) Skew between opposite transitions of the same output in a given device $|t_{PHL} - t_{PLH}|$

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 3.3 V ± 0.3 V, R_L = 50 Ω, C_L = 10 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
X_{TALK}	Differential crosstalk	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 11	-34.67	dB
O_{IRR}	Differential OFF isolation	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 12	-19.09	dB
I_{LOSS}	Differential insertion loss	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, seeFigure 13	-2.84	dB
I_{RETURN}	Differential return loss	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 13	-9.43	dB
DR	Data rate		2.20	Gbps
BW	Differential bandwidth		1.10	Ghz

DYNAMIC CHARACTERISTICS

over recommended operating free-air temperature range, V_{DD} = 2.5 V ± 0.25 V, R_L = 50 Ω, C_L = 10 pF (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
X_{TALK}	Differential crosstalk	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 7	-34.94	dB
O_{IRR}	Differential OFF isolation	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 8	-18.39	dB
I_{LOSS}	Differential insertion loss	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 9	-3.07	dB
I_{RETURN}	Differential return loss	825 MHz, 1.65Gbps, R_L = 50 Ω, C_L = 10 pF, see Figure 9	-9.56	dB
DR	Data rate		2.20	Gbps
BW	Differential bandwidth		1.10	Ghz

TYPICAL PERFORMANCE

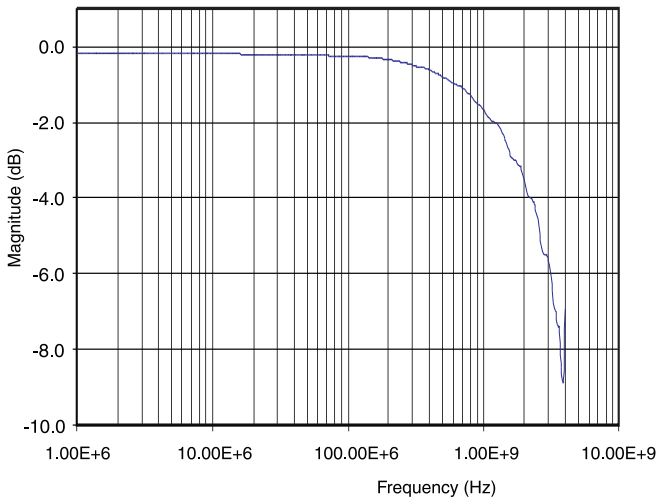


Figure 1. Differential Gain vs Frequency

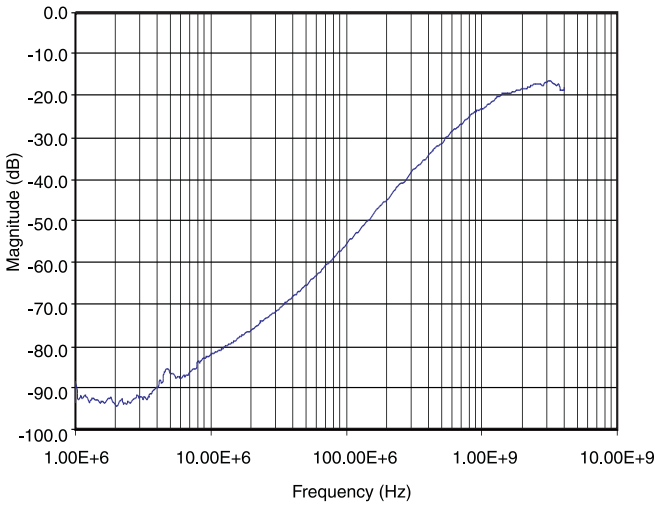


Figure 2. Differential Off Isolation vs Frequency

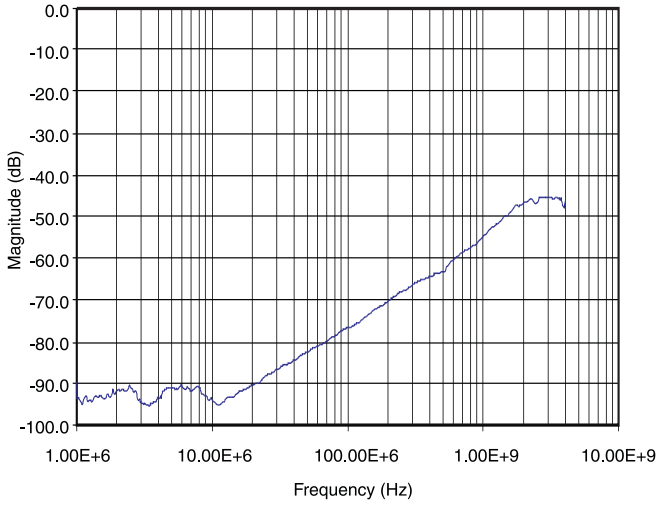


Figure 3. Differential Crosstalk vs Frequency

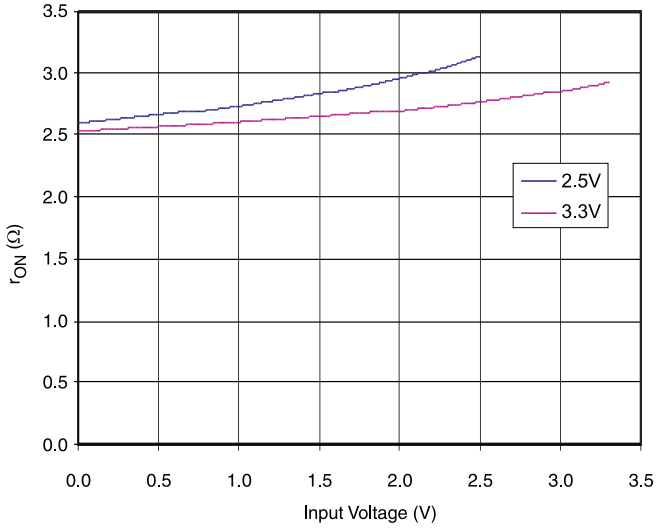


Figure 4. r_{ON} vs V_{COM} (Differential Switch)

APPLICATION INFORMATION

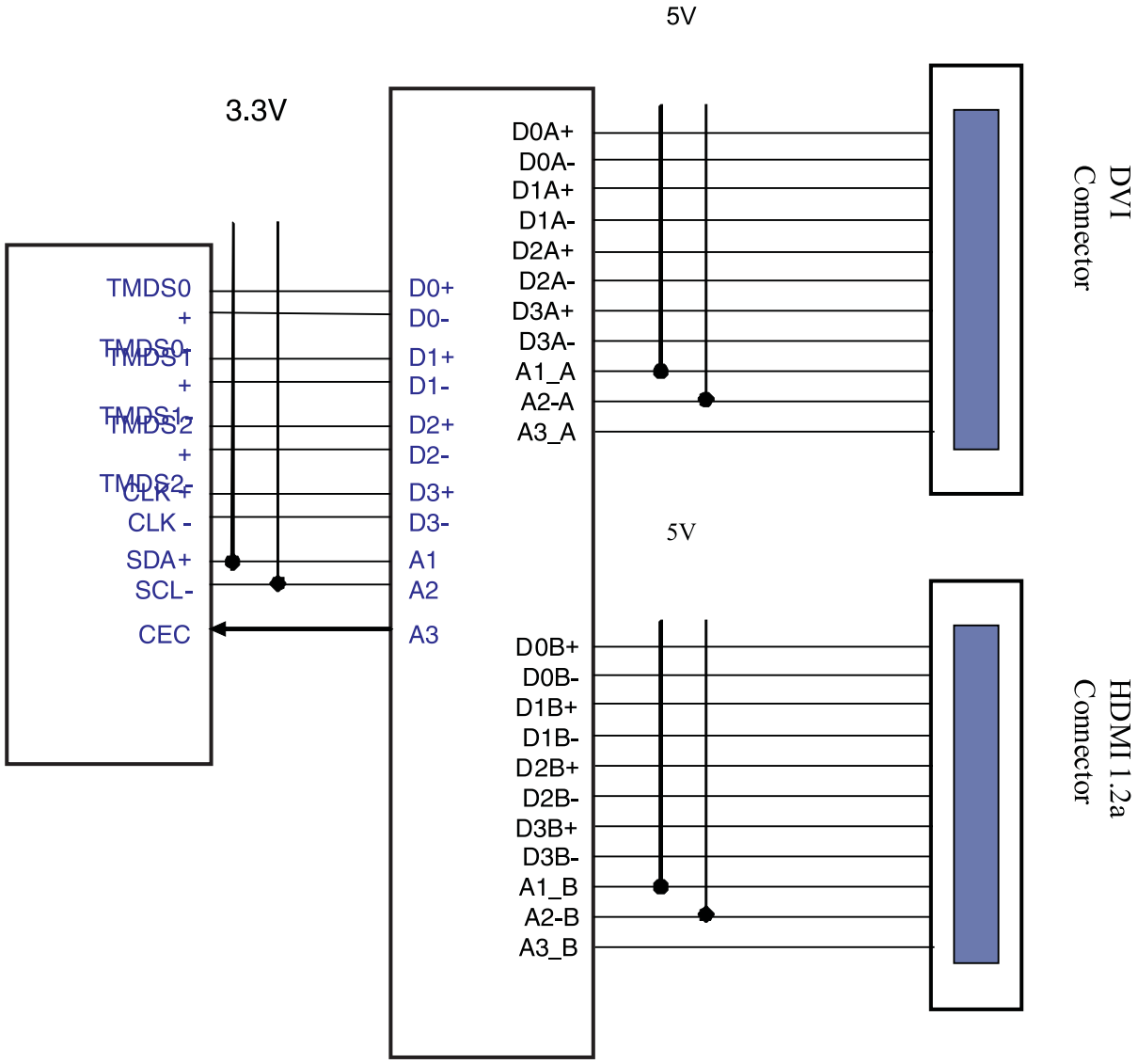


Figure 5. Typical Application Switching HDMI 1.2a and DVI

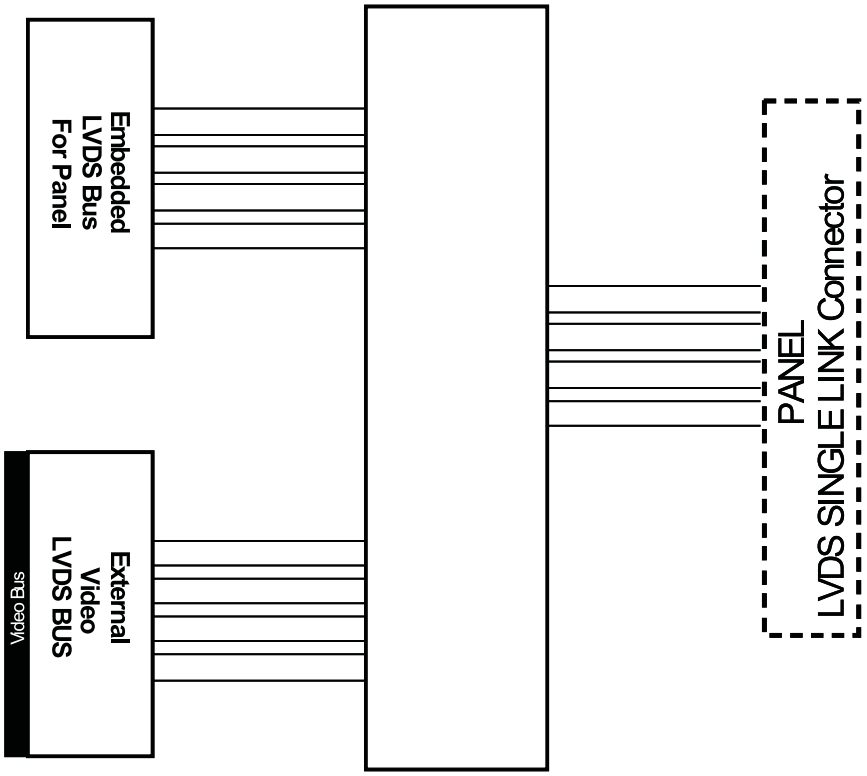
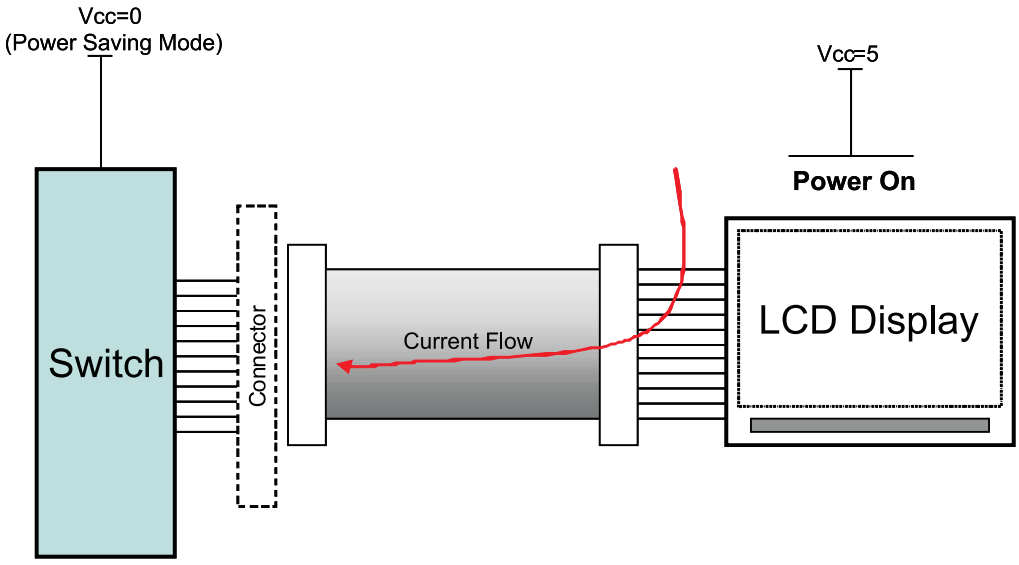


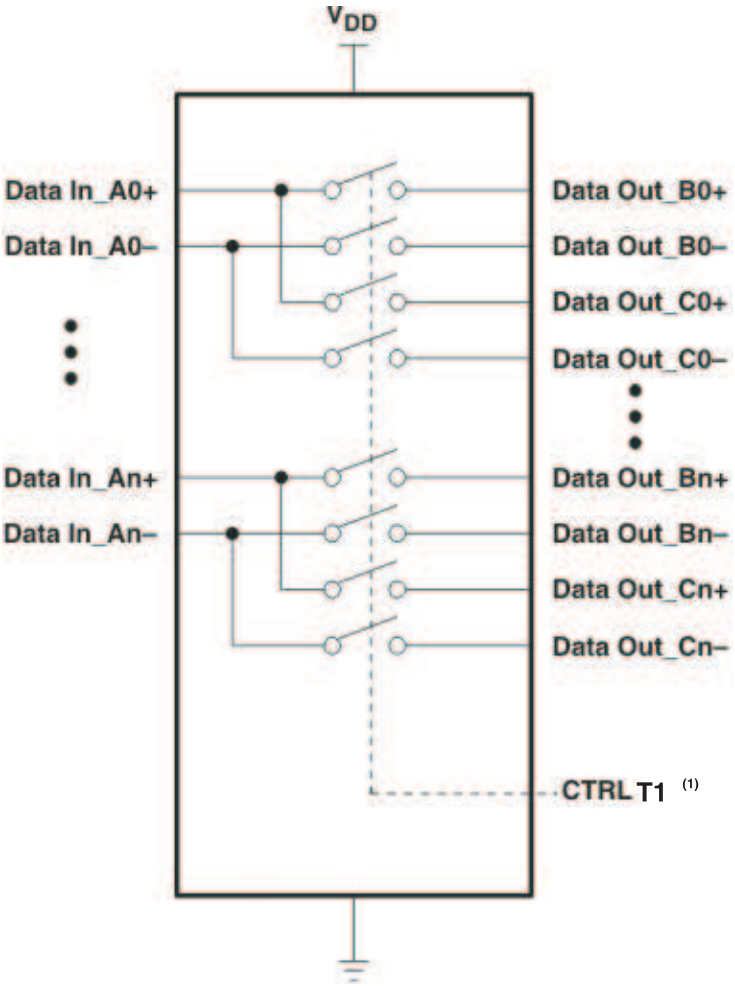
Figure 6. Typical Application for Dual LVDS



A. The switch already has I_{OFF} circuit and it will reduce the current flow leakage limit to 10 μA maximum and it will prevent the damage from back drive current flow from the power-on circuit.

Figure 7. I_{OFF} (Back Drive Protection)

PARAMETER MEASUREMENT INFORMATION

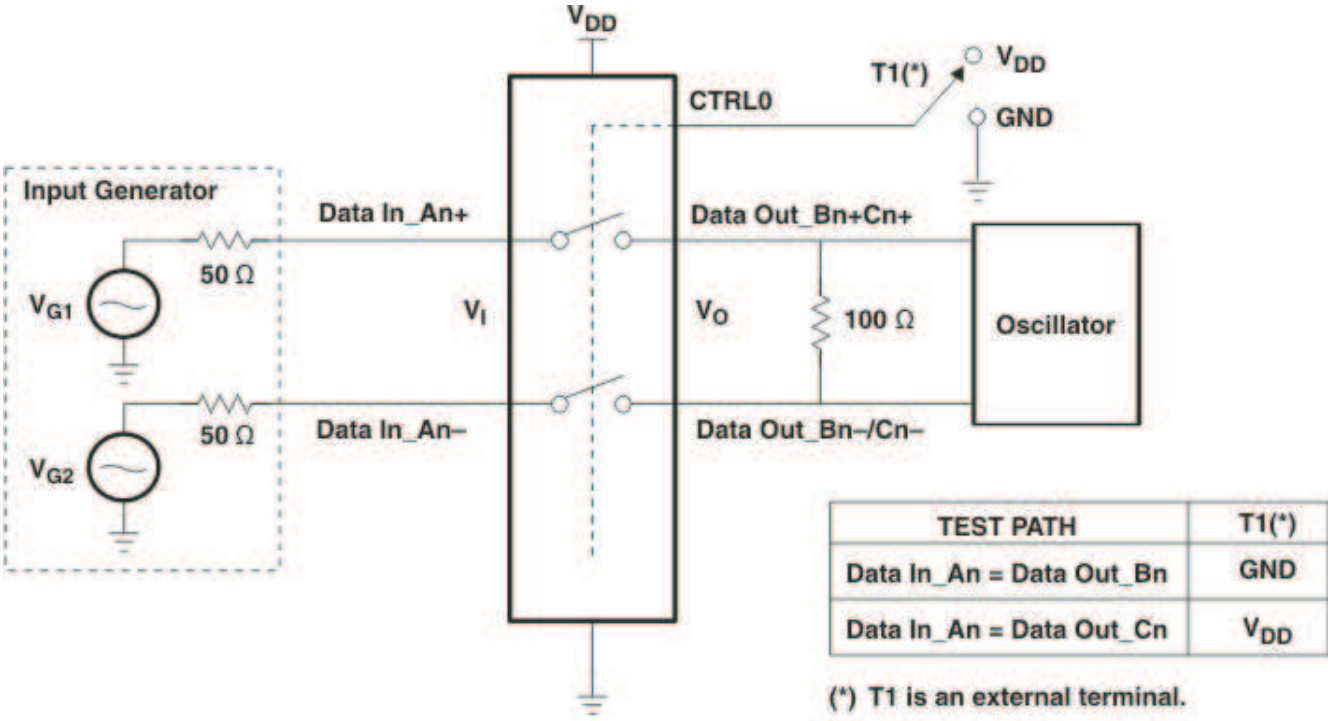


TEST PATH	T1(1)
Data In_An=Data Out_Bn	GND
Data In_An=Data Out_Cn	V_{DD}

(1) T1 is an external terminal.

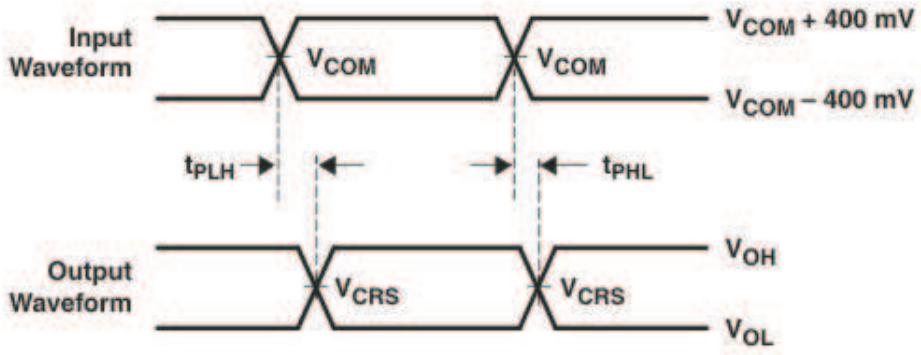
Figure 8. Differential Signaling Device

PARAMETER MEASUREMENT INFORMATION (continued)



TEST PATH	T1(*)
Data In_An = Data Out_Bn	GND
Data In_An = Data Out_Cn	V_{DD}

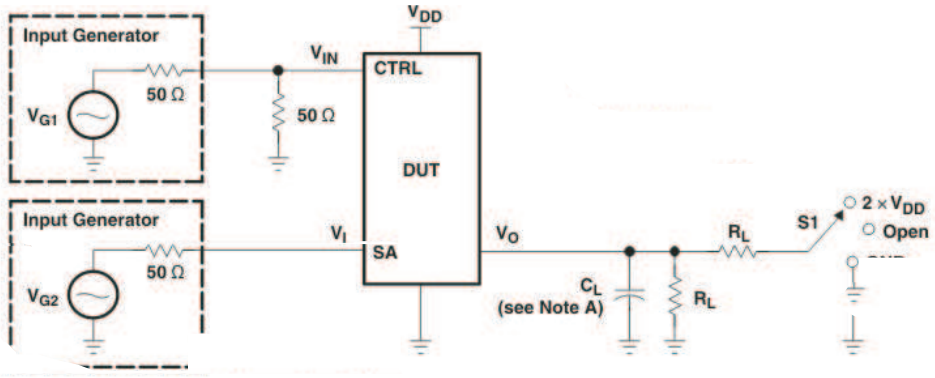
(*) T1 is an external terminal.



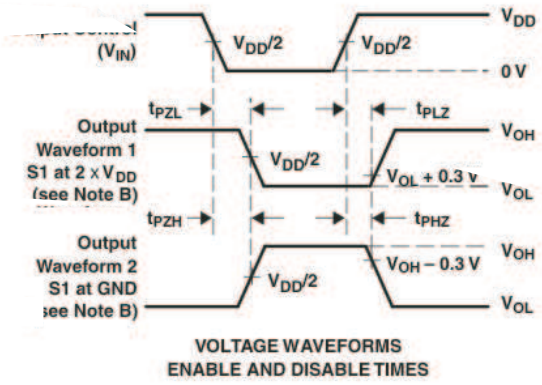
V_{COM} = 1.5 V
V_{CRS} is the cross-point of the differential signal.
$t_{sk} = |t_{PLHn} - t_{PHLn}|$

Figure 9. Test Circuit for Propagation Delay and Intra-Pair Skew

PARAMETER MEASUREMENT INFORMATION (continued)



TEST	V_{DD}	S1	R_L	V_I	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V ±300 mV	2 × V_{DD}	100 Ω	GND	No load	0.3 V
t_{PHZ}/t_{PZH}	3.3 V ±300 mV	GND	100 Ω	V_{DD}	No load	0.3 V

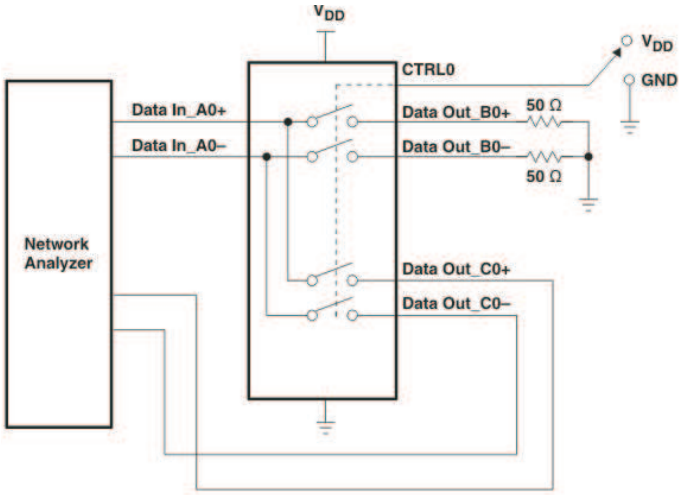


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

A. CL includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, ZO = 50 ohm, tr ≤ 2.5 ns, tf ≤ 2.5 ns
D. The outputs are measured one at a time, with one transition per measurement.
E. tPLZ and tPHZ are the same as tdis.
F. tPZL and tPZH are the same as ten.

Figure 10. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



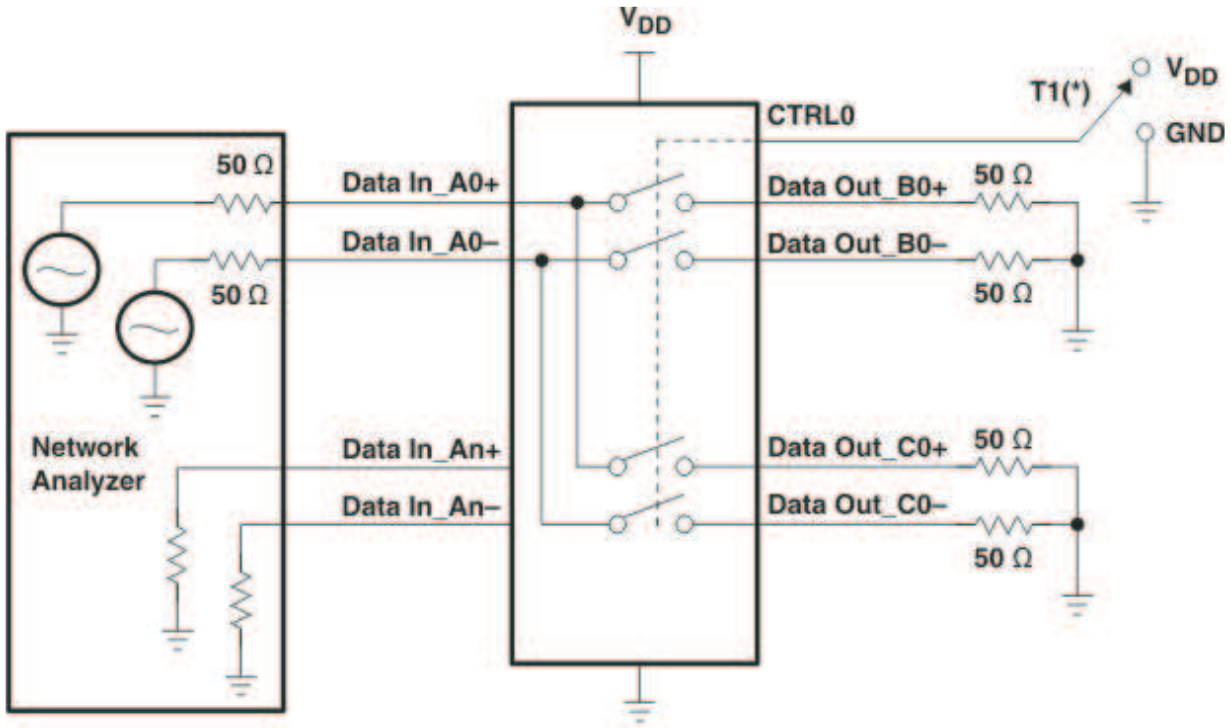
TEST	VNA MEASUREMENT
Differential insertion loss	S_{21}
Differential return loss	S_{11}
Common-mode insertion loss	S_{21}

TEST PATH	T1(1)
Data In_An=Data Out_Bn	GND
Data In_An=Data Out_Cn	V_{DD}

(1) T1 is an external terminal.

Figure 11. Differential Crosstalk Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



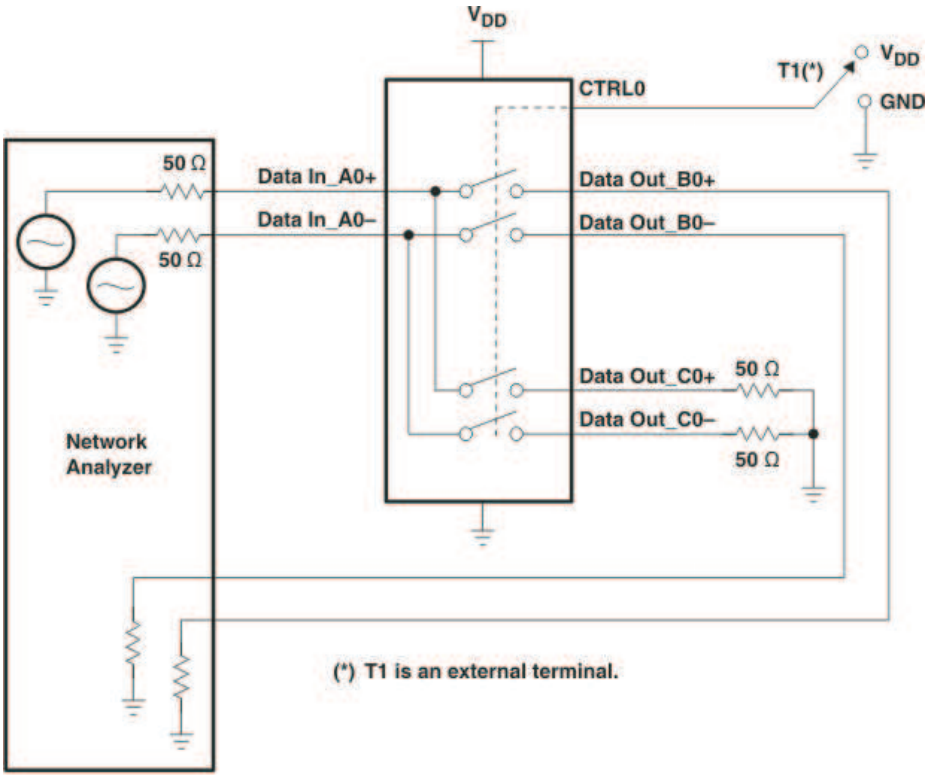
(*) T1 is an external terminal.

TEST PATH	T1(1)
Data In_An=Data Out_Bn	GND
Data In_An=Data Out_Cn	V_{DD}

(1) T1 is an external terminal.

Figure 12. Differential OFF Isolation Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)



TEST PATH	T1(1)
Data In_An=Data Out_Bn	GND
Data In_An=Data Out_Cn	V_{DD}

(1) T1 is an external terminal.

Figure 13. Differential Insertion Loss, Return Loss, and Common-Mode Insertion Loss Test Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TS3DV20812RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples

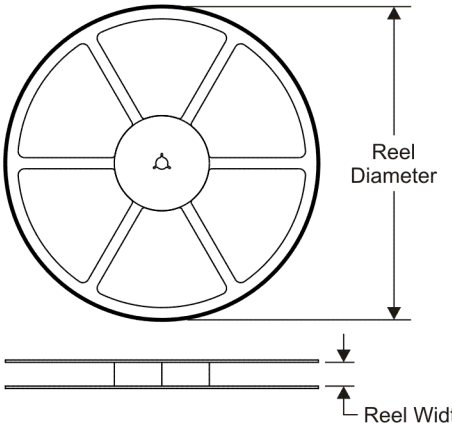
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

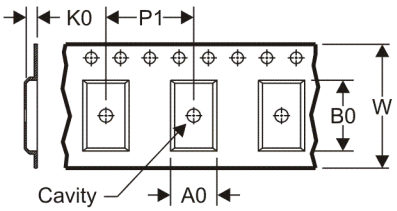
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

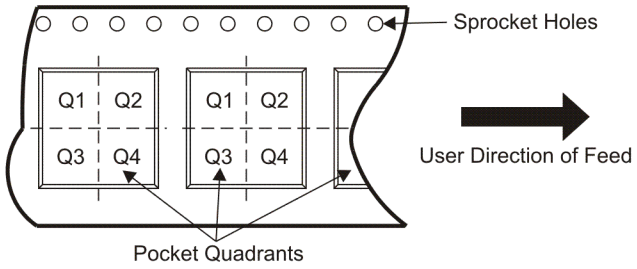


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

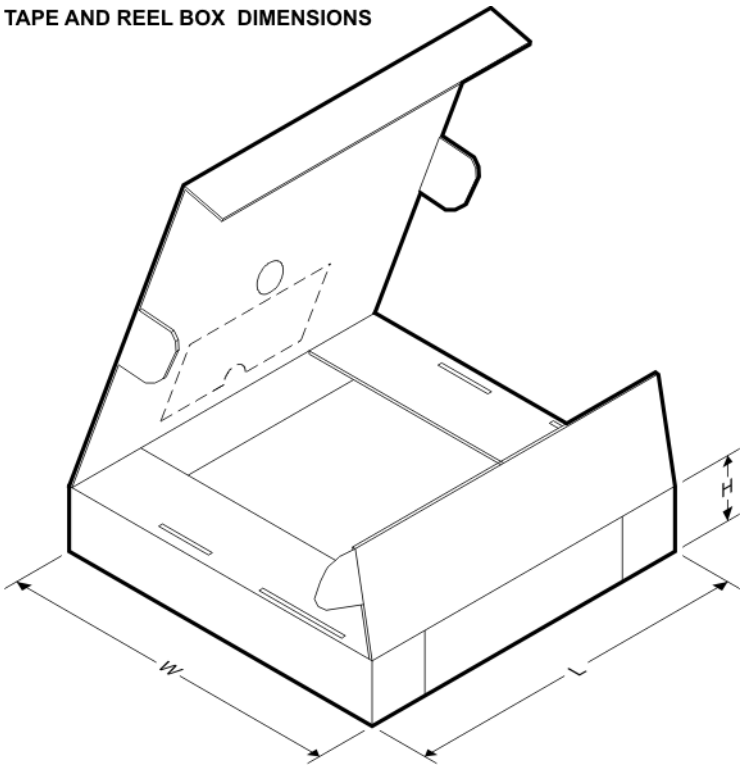
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3DV20812RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2

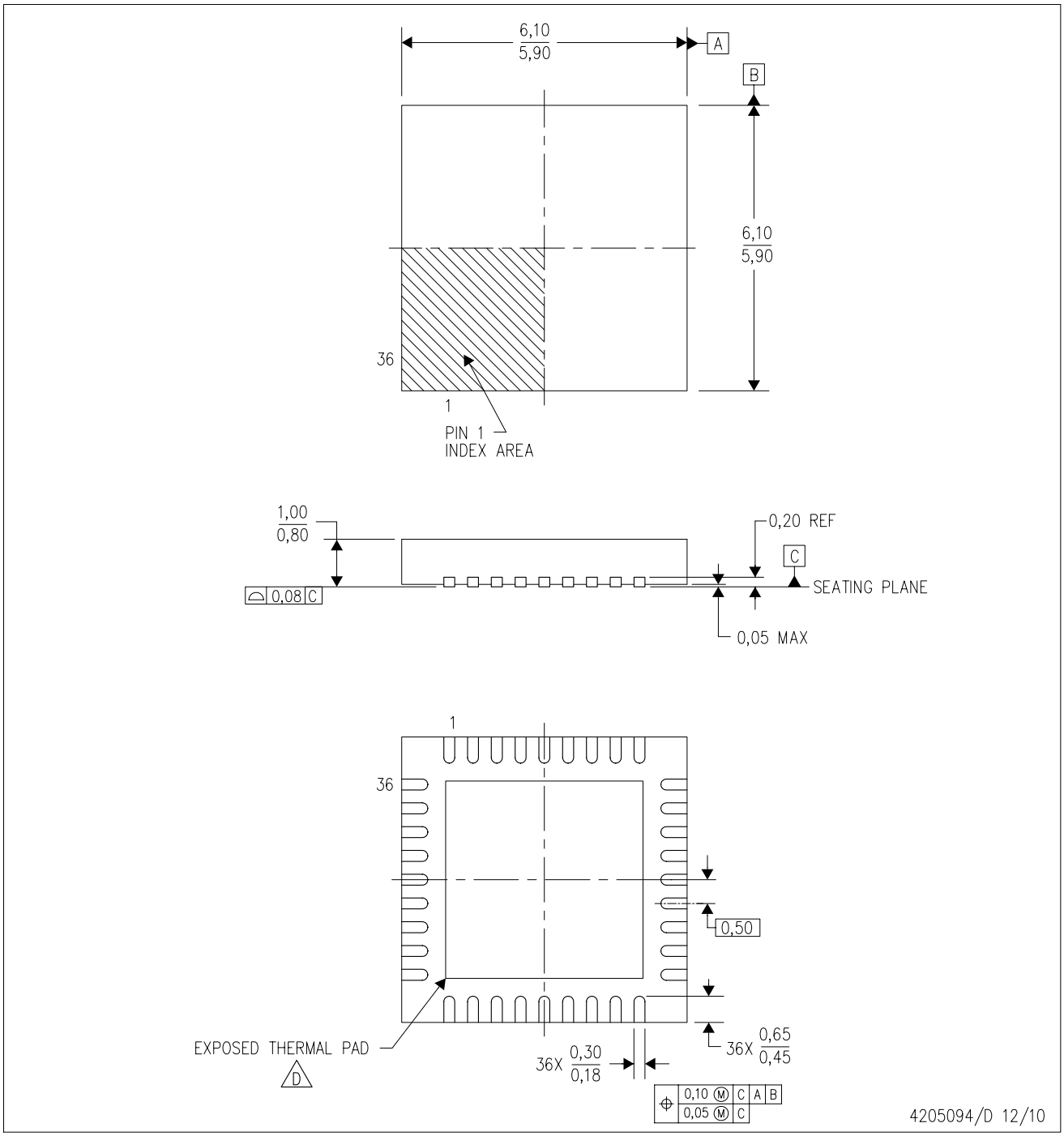
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3DV20812RHHR	VQFN	RHH	36	2500	346.0	346.0	33.0

RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

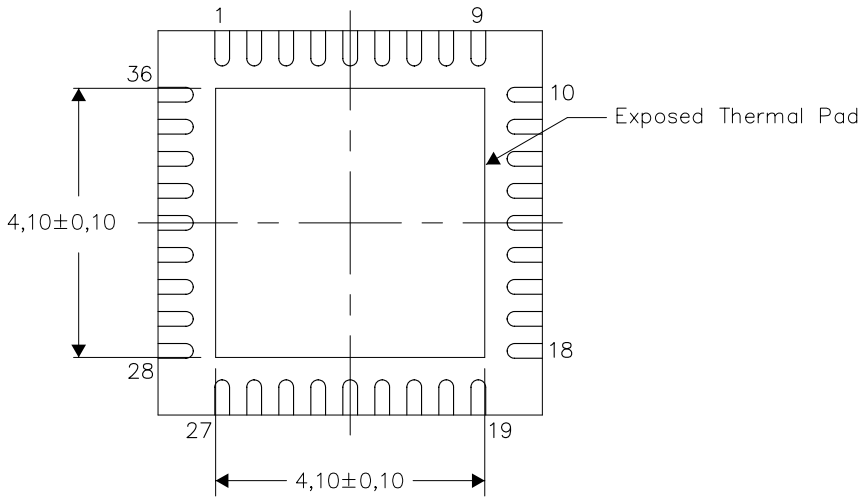
RHH (S–PVQFN–N36) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



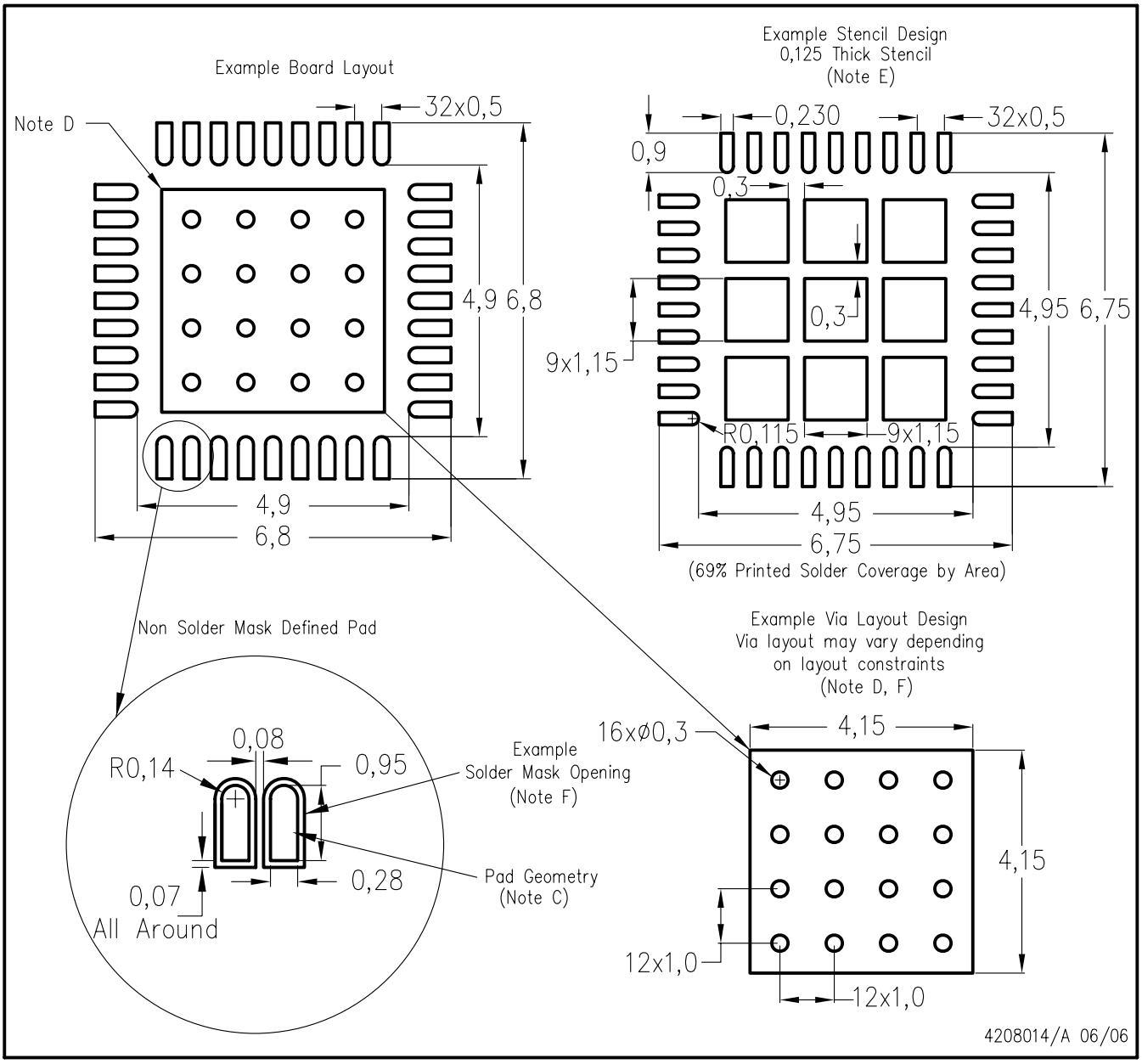
Bottom View

Exposed Thermal Pad Dimensions

4206362–3/H 09/10

NOTE: A. All linear dimensions are in millimeters

RHH (S–PQFP–N36)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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