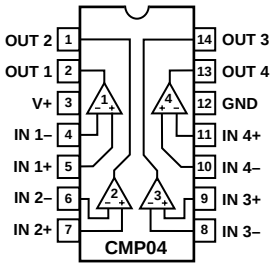
Quad Low Power, Precision Comparator

CMP04

FEATURES
- **High Gain: 200 V/mV typ**
- **Single or Dual Supply Operation**
- **Input Voltage Range Includes Ground**
- **Low Power Consumption (1.5 mW/Comparator)**
- **Low Input Bias Current: 100 nA max**
- **Low Input Offset Current: 10 nA max**
- **Low Offset Voltage: 1 mV max**
- **Low Output Saturation Voltage: 250 mV @ 4 mA**
- **Logic Output Compatible with TTL, DTL, ECL, MOS and CMOS**
- **Directly Replaces LM139/239/339 Comparators**
- **Available in Die Form**

PIN CONNECTIONS

14-Lead Cerdip
14-Lead Plastic DIP
14-Lead SOIC



GENERAL DESCRIPTION

Four precision independent comparators comprise the CMP04. Performance highlights include a very low offset voltage, low output saturation voltage and high gain in a single supply design. The input voltage range includes ground for single supply operation and V– for split supplies. A low power supply current of 2 mA, which is independent of supply voltage, makes this the preferred comparator for precision applications requiring minimal power consumption. Maximum logic interface flexibility is offered by the open-collector TTL output.

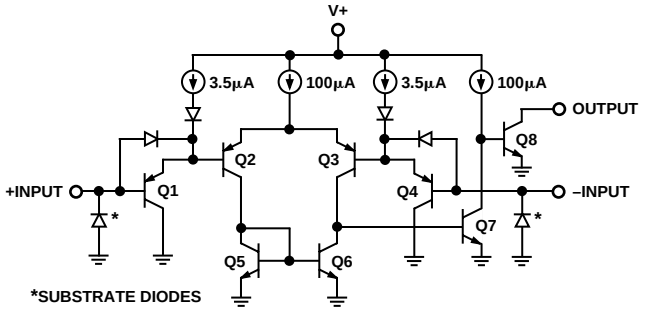


Figure 1. Simplified Schematic (1/4 CMP04)

TYPICAL INTERFACE

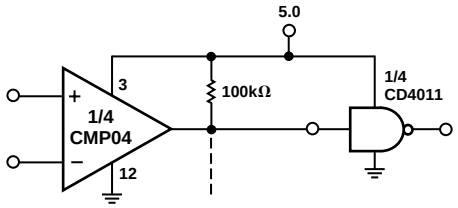


Figure 2a. Driving CMOS

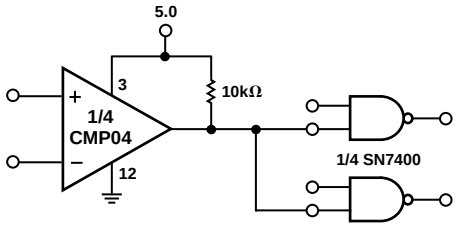


Figure 2b. Driving TTL

REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703

CMP04–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V+ = +5 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	R_S = 0 Ω, R_L = 5.1 kΩ, V_O = 1.4 V[1]		0.4	1	mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$, R_L = 5.1 kΩ, V_O = 1.4 V		2	10	nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$		25	100	nA
Voltage Gain	A_V	$R_L \geq 15$ kΩ, V+ = 15 V[2]	80	200		V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V[3]				
		V_{RL} = 5 V, R_L = 5.1 kΩ		300		ns
Small-Signal Response Time	t_r	V_{IN} = 100 mV Step[3], 5 mV Overdrive				
		V_{RL} = 5 V, R_L = 5.1 kΩ		1.3		µs
Input Voltage Range	CMVR	(Note 4)	0		V+ –1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 2, 5)	80	100		dB
Power Supply Rejection Ratio	PSRR	V+ = +5 V to +18 V[2]	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+) = 0$, $I_{SINK} \leq 4$ mA		250	400	mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+) = 0$, $V_O \leq 1.5$ V	6	16		mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1$ V, $V_{IN}(-) = 0$, V_O = 30 V		0.1	100	nA
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30 V		0.8	2.0	mA

NOTES
[1]At output switch point, V_O = 1.4 V, R_S = 0 Ω with V+ from 5 V; and over the full input common-mode range (0 V to V+ –1.5 V).
[2]Guaranteed by design.
[3]Sample tested.
[4]The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ –1.5 V, but either or both inputs can go to +30 V without damage.
[5]$R_L \geq 15$ kΩ, V+ = 15 V, V_{CM} = 1.5 V to 13.5 V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 36 V or ±18 V
Differential Input Voltage . . . . . 36 V dc
Input Voltage . . . . . –0.3 V to +36 V
Operating Temperature Range
  CMP04BY . . . . . –55°C to +125°C
  CMP04FP, FS . . . . . –40°C to +85°C
Junction Temperature (T_J) . . . . . –65°C to +150°C
Storage Temperature Range . . . . . –65°C to +150°C
  (P Suffix) . . . . . –65°C to +125°C
Input Current (V_{IN} < –3.0 V) . . . . . 50 mA
Output Short-Circuit to GND . . . . . Continuous
Lead Temperature (Soldering, 60 sec) . . . . . +300°C

Package Type	θ_{JA}[2]	θ_{JC}	Units
14-Lead Hermetic DIP (Y)	94	10	°C/W
14-Lead Plastic DIP (P)	83	39	°C/W
14-Lead SOIC	120	36	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for cerdip and plastic DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.

ORDERING GUIDE

Model	T_A = +25°C V_{OS}	Temperature Ranges	Package Descriptions	Package Options
CMP04BY/883C	1 mV	–55°C to +125°C	14-Lead Cerdip	Q-14
CMP04FP	1 mV	–40°C to +85°C	14-Lead Plastic DIP	N-14
CMP04FS	1 mV	–40°C to +85°C	14-Lead SOIC	R-14/SO-14

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the CMP04 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ELECTRICAL CHARACTERISTICS

(@ V+ = +5 V, –55°C ≤ T_A ≤ +125°C for CMP04BY, –40°C ≤ T_A ≤ +85°C for CMP04FP/FS, unless otherwise noted)

Parameter	Symbol	Conditions	CMP04B/F[1] Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	R_S = 0 Ω, R_L = 5.1 kΩ V_O = 1.4 V[2]		1 1	2 2	mV mV
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1 kΩ V_O = 1.4 V		4 4 4	20 20 20	nA nA nA
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$		40	200	nA
Voltage Gain	A_V	$R_L \geq 15$ kΩ, V+ = 15 V[3]	70	125		V/mV
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4 V[4] V_{RL} = 5 V, R_L = 5.1 kΩ		300 300 300		ns ns ns
Small-Signal Response Time	t_r	V_{IN} = 100 mV Step[4] 5 mV Overdrive V_{RL} = 5 V, R_L = 5.1 kΩ		1.3 1.3 1.3		µs µs µs
Input Voltage Range	CMVR	(Note 5)	0		V+ –1.5	V
Common-Mode Rejection Ratio	CMRR	(Notes 1, 3)	60	100		dB
Power Supply Rejection Ratio	PSRR	V+ = +5 V to +18 V	80	100		dB
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+)$ = 0, $I_{SINK} \leq 4$ mA		250 250	700 700	mV mV
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+)$ = 0, $V_O \leq 1.5$ V	5 5	16 16		mA mA
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1$ V, $V_{IN}(-)$ = 0, V_O = 30 V		0.1 0.1	200 200	nA nA
Supply Current	I+	R_L = ∞, All Comps V+ = 30 V		1.2 1.2	3.0 3.0	mA mA

NOTES
[1]$R_L \geq 15$ kΩ, V+ = 15 V, V_{CM} = 1.5 V to 13.5 V.
[2]At output switch point, V_O = 1.4 V, R_S = 0 Ω with V+ from 5 V; and over the full input common-mode range (0 V to V+ –1.5 V).
[3]Guaranteed by design.
[4]Sample tested.
[5]The input common-mode voltage or input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ –1.5 V, but either or both inputs can go to +30 V without damage.

Specifications subject to change without notice.

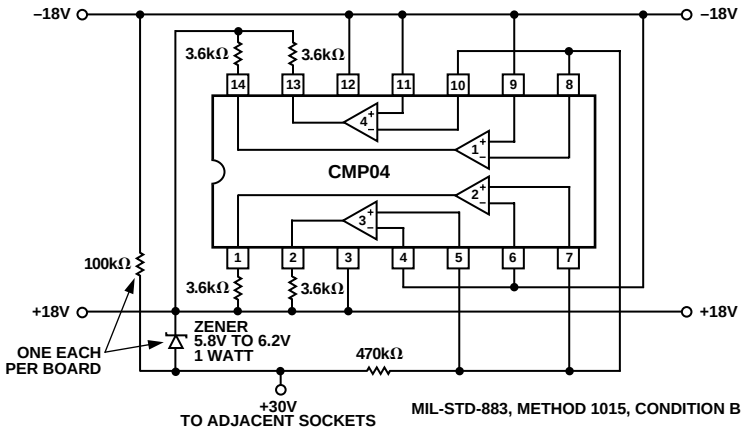
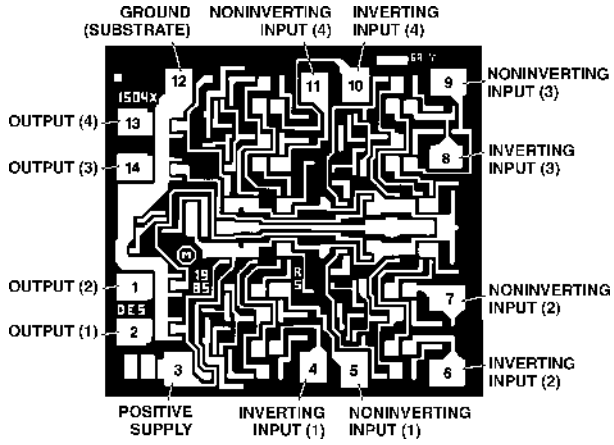


Figure 3. Burn-In Circuit

DICE CHARACTERISTICS



DIE SIZE 0.058 × 0.055 inch, 3190 sq. mils
(1.47 × 1.40 mm, 2.058 sq. mm)

WAFER TEST LIMITS (@ V+ = +5 V, T_A = +25°C, unless otherwise noted)

Parameter	Symbol	Conditions	CMP04N Limit	CMP04G Limit	Units
Input Offset Voltage	V_{OS}	R_S = 0 Ω, R_L = 5.1 kΩ V_O = 1.4 V[1]	1	2	mV max
Input Offset Current	I_{OS}	$I_{IN}(+) - I_{IN}(-)$ R_L = 5.1 kΩ V_O = 1.4 V	10	25	nA max
Input Bias Current	I_B	$I_{IN}(+)$ or $I_{IN}(-)$[1]	100	100	nA max
Voltage Gain	A_V	$R_L \geq 15$ kΩ, V+ = 15 V[3]	80	50	V/mV min
Input Voltage Range	CMVR	(Notes 2, 3)	V+ –1.5	V+ –1.5	V max
Common-Mode Rejection Ratio	CMRR	(Note 4)	80	80	dB min
Power Supply Rejection Ratio	PSRR	V+ = +5 V to +18 V	80	80	dB min
Saturation Voltage	V_{OL}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+)$ = 0, $I_{SINK} \leq 4$ mA	400	400	mV max
Output Sink Current	I_{SINK}	$V_{IN}(-) \geq 1$ V, $V_{IN}(+)$ = 0, $V_O \leq 1.5$ V	6	6	mA min
Output Leakage Current	I_{LEAK}	$V_{IN}(+) \geq 1$ V, $V_{IN}(-)$ = 0, V_O = 30 V	100	100	nA max
Supply Current	I+	$R_L = \infty$, All Comps V+ = 30 V	2	2	mA max

NOTES
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS (@ V+ = +5 V, unless otherwise noted)

Parameter	Symbol	Conditions	CMP04N Typical	CMP04G Typical	Units
Large-Signal Response Time	t_r	V_{IN} = TTL Logic Swing V_{REF} = 1.4 V[5] V_{RL} = 5 V, R_L = 5.1 kΩ	600	600	ns
Small-Signal Response Time	t_r	V_{IN} = 100 mV Step[5] 5 mV Overdrive V_{RL} = 5 V, R_L = 5.1 kΩ	1.3	1.3	µs

NOTES
[1]At output switch point, V_O = 1.4 V, R_S = 0 Ω with V+ from 5 V; and over the full input common-mode range (0 V to V+ –1.5 V).
[2]The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V+ –1.5 V, but either or both inputs can go to +30 V without damage.
[3]Guaranteed by design.
[4]$R_L \geq 15$ kΩ. V_{CM} = 1.5 V to 13.5 V.
[5]Sample tested.

Specifications subject to change without notice.

Typical Performance Characteristics

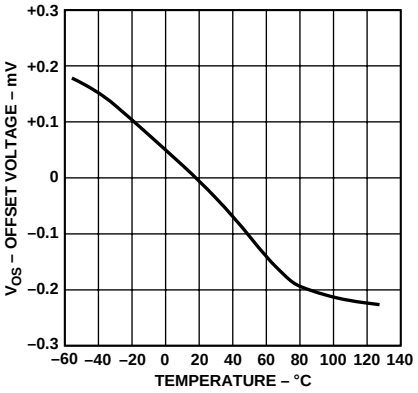


Figure 4. Offset Voltage vs. Temperature

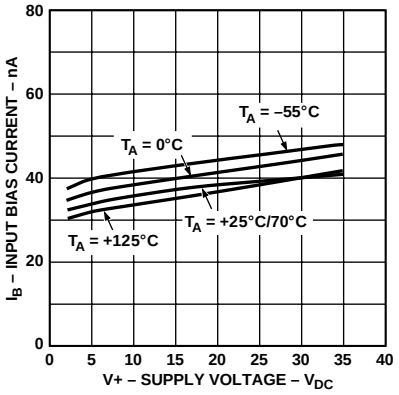


Figure 5. Input Bias Current vs. V+ and Temperature

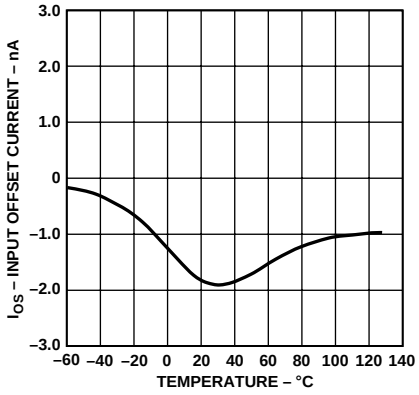


Figure 6. Input Offset Current vs. Temperature

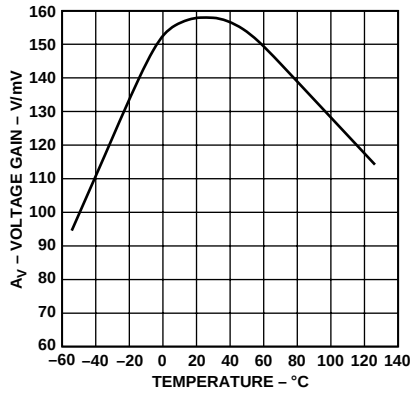


Figure 7. Voltage Gain vs. Temperature

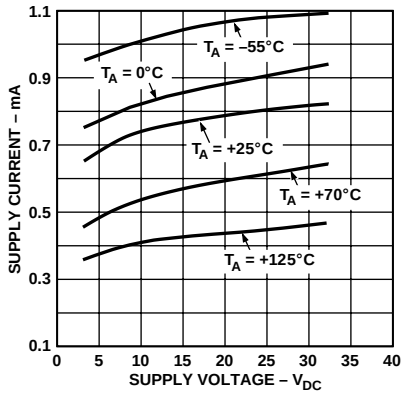


Figure 8. Supply Current vs. Supply Voltage

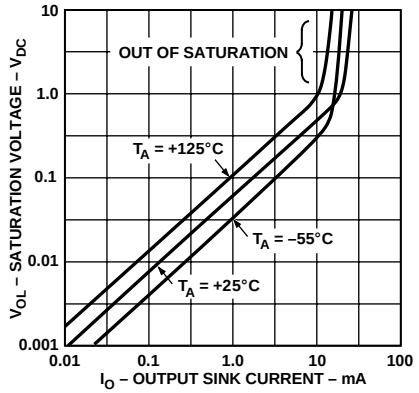


Figure 9. Output Voltage vs. Output Current and Temperature

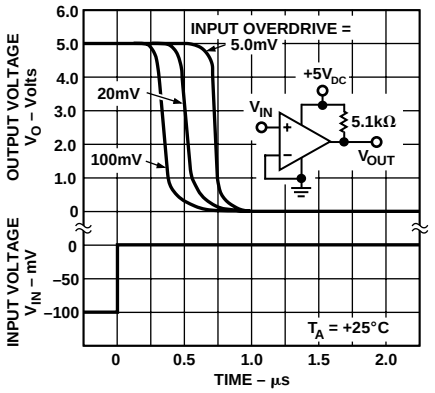


Figure 10. Response Time for Various Input Overdrives—Negative Transition

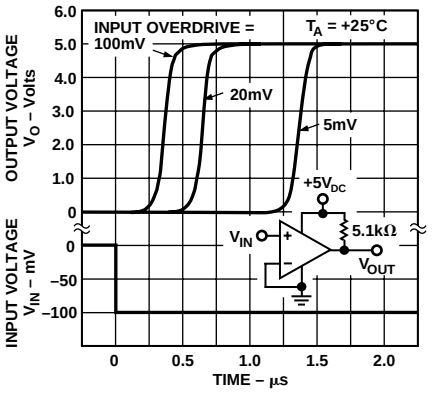


Figure 11. Response Time for Various Input Overdrives—Positive Transition

TYPICAL APPLICATIONS

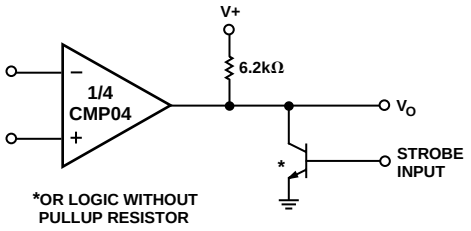


Figure 12. Output Strobing

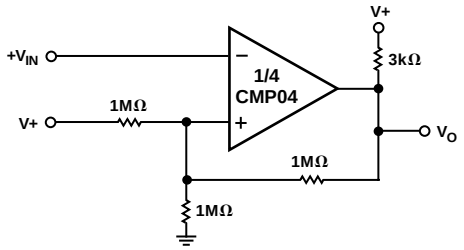


Figure 15. Inverting Comparator with Hysteresis

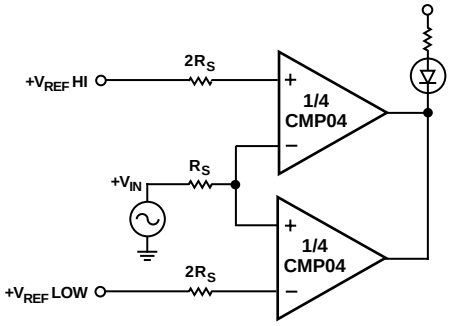


Figure 13. Limit Comparator

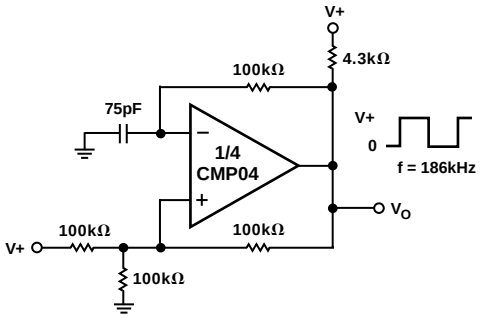


Figure 16. Square Wave Oscillator

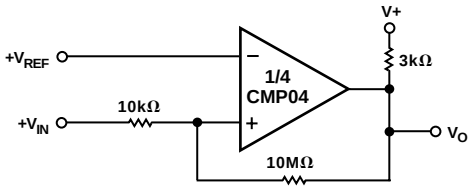


Figure 14. Noninverting Comparator with Hysteresis

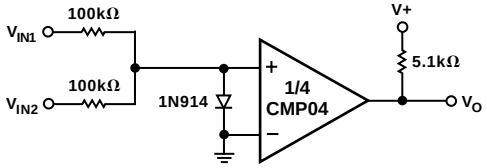


Figure 17. Comparing Input Voltages of Opposite Polarity

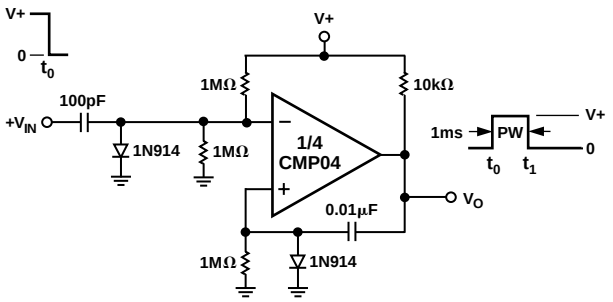


Figure 18. One-Shot Multivibrator

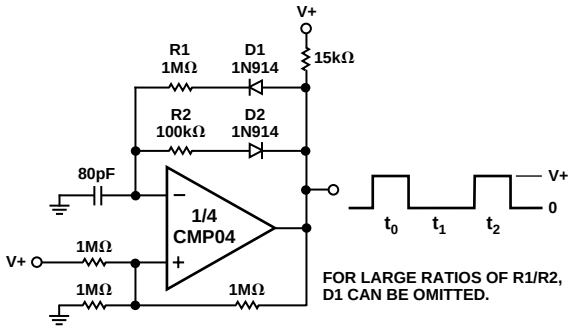


Figure 20. Pulse Generator

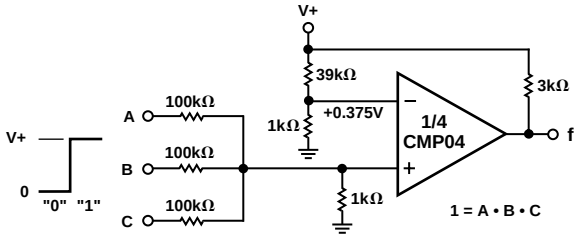


Figure 19. AND Gate

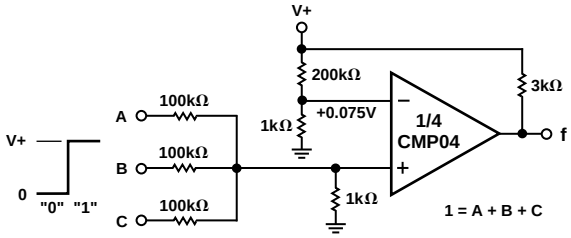


Figure 21. OR Gate

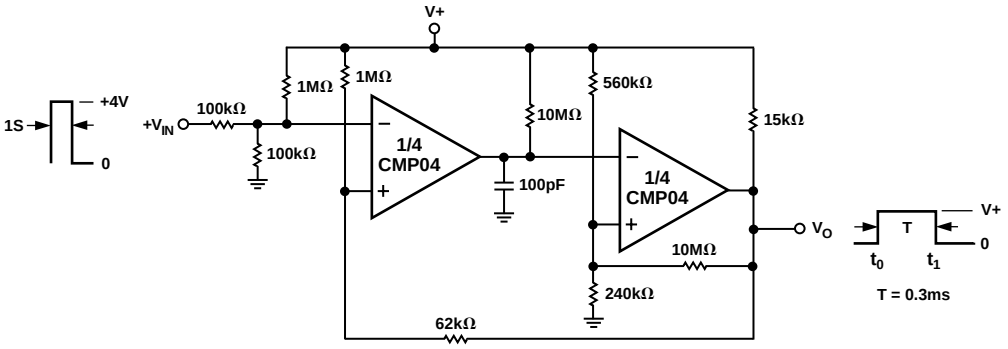


Figure 22. One-Shot Multivibrator with Input Lockout

TYPICAL APPLICATIONS

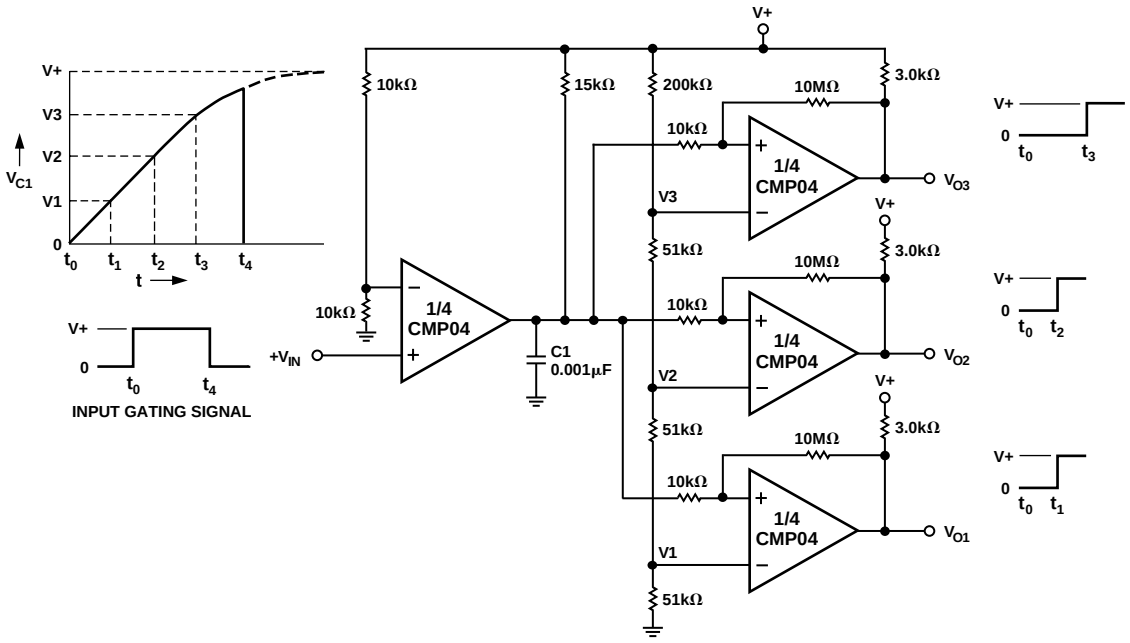


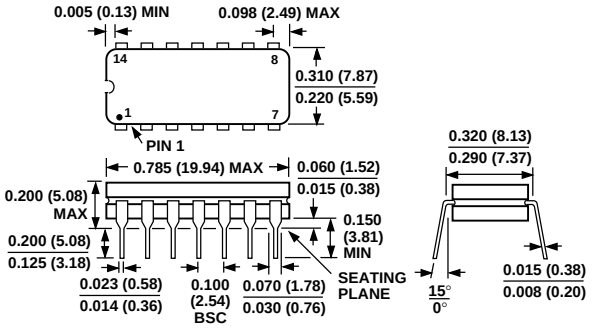
Figure 23. Time Delay Generator

C3107a–0–7/98

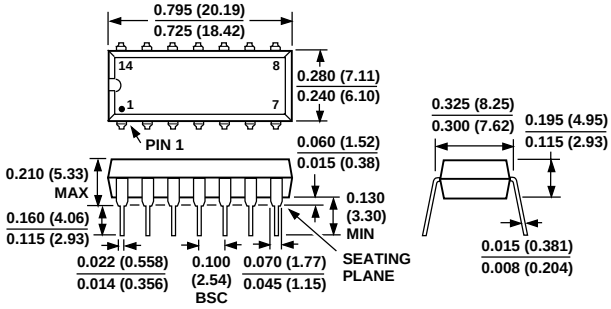
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

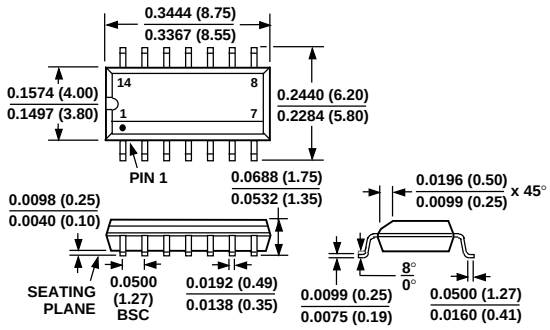
14-Lead Cerdip (Q-14)



14-Lead Plastic DIP (N-14)



14-Lead SOIC (R-14)



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