TEXAS INSTRUMENTS

ISO7760-Q1, ISO7761-Q1
ISO7762-Q1, ISO7763-Q1

SLLSEU7A – NOVEMBER 2018 – REVISED MARCH 2019

ISO776x-Q1 High-speed, robust EMC, reinforced six-channel digital isolators

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient temperature range
  - Device HBM ESD classification level 3A
  - Device CDM ESD classification level C6
- 100 Mbps data rate
- Robust isolation barrier:
  - >100-Year projected lifetime
  - Up to 5000 V_{RMS} isolation rating
  - Up to 12.8 kV surge capability
  - ±100 kV/μs Typical CMTI
- Wide supply range: 2.25 V to 5.5 V
- 2.25-V to 5.5-V Level translation
- Default output *high* (ISO776x) and *low* (ISO776xF) Options
- Low power consumption, typical 1.4 mA per channel at 1 Mbps
- Low propagation delay: 11 ns typical at 5 V
- Robust Electromagnetic Compatibility (EMC):
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 Contact discharge protection across isolation barrier
  - Low emissions
- Wide-SOIC (DW-16) and SSOP (DBQ-16) package options
- Safety-related certifications:
  - Reinforced insulation per DIN V VDE V 0884-11:2017-01
  - UL 1577 component recognition program
  - CSA Certification per IEC 60950-1, IEC 62368-1, and IEC 60601-1
  - CQC Certification per GB4943.1-2011
  - TUV Certification according to EN 60950-1 and EN 61010-1

2 Applications

- Hybrid, electric and power train system (EV/HEV)
  - Battery management system (BMS)
  - On-board charger
  - Traction inverter
  - DC/DC converter
  - Starter/generator

3 Description

The ISO776x-Q1 devices are high-performance, six-channel digital isolators with 5000-V_{RMS} (DW package) and 3000-V_{RMS} (DBQ package) isolation ratings per UL 1577. This family of devices is also certified according to VDE, CSA, TUV and CQC.

The ISO776x-Q1 family of devices provides high-electromagnetic immunity and low emissions at low-power consumption, while isolating CMOS or LVCMOS digital I/Os. Each isolation channel has a logic-input and logic-output buffer separated by a double capacitive silicon dioxide (SiO_2) insulation barrier. The ISO776x-Q1 family of devices is available in all possible pin configurations such that all six channels are in the same direction, or one, two, or three channels are in reverse direction while the remaining channels are in forward direction. If the input power or signal is lost, the default output is *high* for devices without suffix F and *low* for devices with suffix F. See the *Device Functional Modes* section for further details.

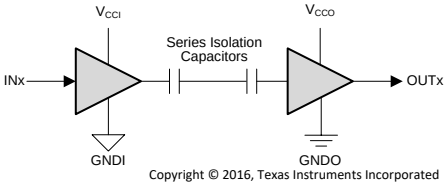
Used in conjunction with isolated power supplies, this family of devices helps prevent noise currents on data buses, such as CAN and LIN, or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. Through innovative chip design and layout techniques, electromagnetic compatibility of the ISO776x-Q1 family of devices has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance. The ISO776x-Q1 family of devices is available in 16-pin SOIC and SSOP packages.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7760-Q1	SOIC (16)	10.30 mm × 7.50 mm
ISO7761-Q1 ISO7762-Q1 IOS7763-Q1	SSOP (16)	4.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



V_{CCI}=Input V_{CC}, V_{CCO}=Output V_{CC}

GNDI=Input ground, GNDO=Output ground

Table of Contents

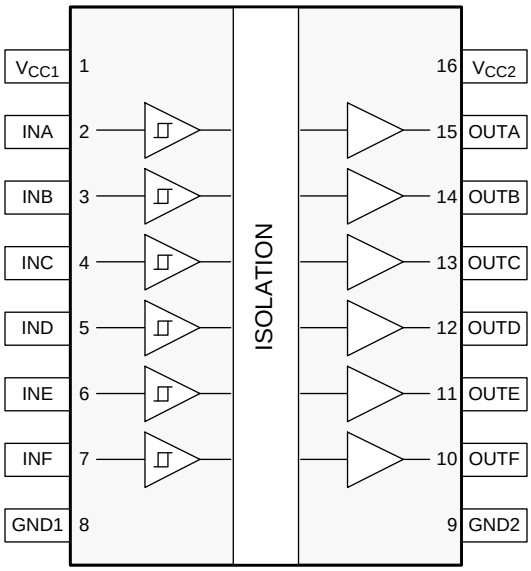
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

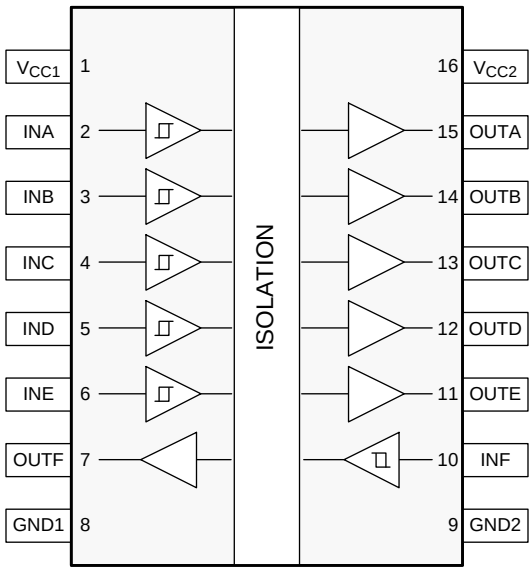
Changes from Original (November 2018) to Revision A	Page
• Changed CPG parameter description From: "External clearance" To: "External creepage" in Insulation Specifications table	7

5 Pin Configuration and Functions

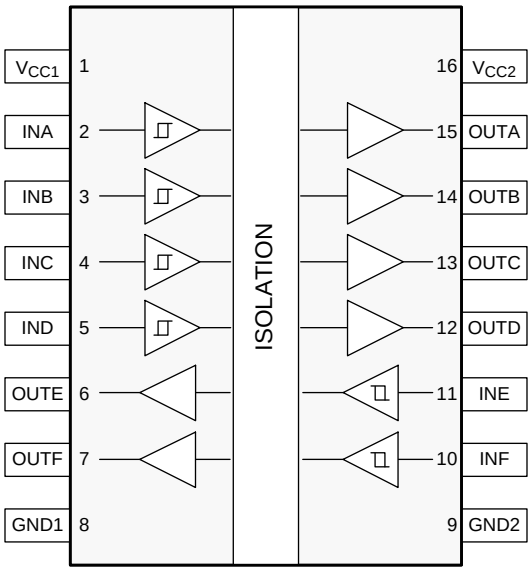
ISO7760-Q1 DW and DBQ Packages
16-Pin SOIC and SSOP
Top View



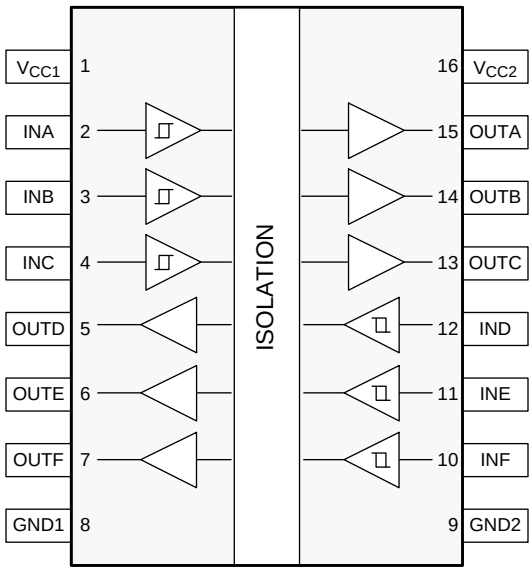
ISO7761-Q1 DW and DBQ Packages
16-Pin SOIC and SSOP
Top View



ISO7762-Q1 DW and DBQ Packages
16-Pin SOIC and SSOP
Top View



ISO7763-Q1 DW and DBQ Packages
16-Pin SOIC and SSOP
Top View



Pin Functions

PIN					I/O	DESCRIPTION
NAME	NO.					
	ISO7760-Q1	ISO7761-Q1	ISO7762-Q1	ISO7763-Q1		
GND1	8	8	8	8	—	Ground connection for V_{CC1}
GND2	9	9	9	9	—	Ground connection for V_{CC2}
INA	2	2	2	2	I	Input, channel A
INB	3	3	3	3	I	Input, channel B
INC	4	4	4	4	I	Input, channel C
IND	5	5	5	12	I	Input, channel D
INE	6	6	11	11	I	Input, channel E
INF	7	10	10	10	I	Input, channel F
OUTA	15	15	15	15	O	Output, channel A
OUTB	14	14	14	14	O	Output, channel B
OUTC	13	13	13	13	O	Output, channel C
OUTD	12	12	12	5	O	Output, channel D
OUTE	11	11	6	6	O	Output, channel E
OUTF	10	7	7	7	O	Output, channel F
V_{CC1}	1	1	1	1	—	Power supply, side 1
V_{CC2}	16	16	16	16	—	Power supply, side 2

6 Specifications

6.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage (2)	–0.5	6	V
V	Voltage at INx, OUTx	–0.5	V_{CCX} + 0.5 (3)	V
I_O	Output current	–15	15	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.
(3) Maximum voltage must not exceed 6 V

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±6000	V
		Charged-device model (CDM), per AEC Q100-011	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test (2) (3)	±8000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
(3) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage		2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising			2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling		1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis		100	200		mV
I_{OH}	High-level output current	V_{CCO} (1) = 5 V	–4			mA
		V_{CCO} = 3.3 V	–2			
		V_{CCO} = 2.5 V	–1			
I_{OL}	Low-level output current	V_{CCO} = 5 V			4	mA
		V_{CCO} = 3.3 V			2	
		V_{CCO} = 2.5 V			1	
V_{IH}	High-level input voltage		0.7 × V_{CCI} (1)		V_{CCI}	V
V_{IL}	Low-level input voltage		0		0.3 × V_{CCI}	V
DR (2)	Data rate		0		100	Mbps
T_A	Ambient temperature		-40	25	125	°C

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

6.4 Thermal Information

THERMAL METRIC[1]		ISO776x-Q1		UNIT
		DW (SOIC)	DBQ (SSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.3	86.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	24.0	26.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.3	36.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	28.7	36.1	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISO7760-Q1						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			292	mW
P_{D1}	Maximum power dissipation (side 1)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			50	mW
P_{D2}	Maximum power dissipation (side 2)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			242	mW
ISO7761-Q1						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			292	mW
P_{D1}	Maximum power dissipation (side 1)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			83	mW
P_{D2}	Maximum power dissipation (side 2)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			209	mW
ISO7762-Q1						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			292	mW
P_{D1}	Maximum power dissipation (side 1)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			116	mW
P_{D2}	Maximum power dissipation (side 2)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			176	mW
ISO7763-Q1						
P_D	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			292	mW
P_{D1}	Maximum power dissipation (side 1)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			146	mW
P_{D2}	Maximum power dissipation (side 2)	$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$°C, $C_L = 15$ pF, input a 50-MHz 50% duty cycle square wave			146	mW

6.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	DBQ-16	
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	>8	>3.7	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	>8	>3.7	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>21	>21	µm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I–IV	I–IV	
		Rated mains voltage ≤ 300 V_{RMS}	I–IV	I–III	
		Rated mains voltage ≤ 600 V_{RMS}	I–IV	n/a	
		Rated mains voltage ≤ 1000 V_{RMS}	I–III	n/a	
DIN V VDE V 0884-11:2017-01(2)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	566	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage; Time dependent dielectric breakdown (TDDB) test; see Figure 30	1500	400	V_{RMS}
		DC voltage	2121	566	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	8000	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM}$ (qualification)	8000	4000	V_{PK}
q_{pd}	Apparent charge(4)	Method a, After Input/Output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	≤5	
		Method b1; At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	≤5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~1.1	~0.9	pF
R_{IO}	Isolation resistance(5)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V, T_S = 150°C	$>10^9$	$>10^9$	
	Pollution degree		2	2	
	Climatic category		55/125/21	55/125/21	
UL 1577					
V_{ISO}	Withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for safe *electrical insulation only* within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device.

6.7 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB 4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013
Reinforced Insulation; Maximum transient isolation voltage, 8000 V_{PK} (DW-16) and 4242 V_{PK} (DBQ-16); Maximum repetitive peak isolation voltage, 2121 V_{PK} (DW-16) and 566 V_{PK} (DBQ-16); Maximum surge isolation voltage, 8000 V_{PK} (DW-16) and 4000 V_{PK} (DBQ-16)	Reinforced insulation per CSA 60950-1-07+A1+A2, IEC 60950-1 2nd Ed.+A1+A2, CSA 62368-1-14 and IEC 62368-1:2014 800 V_{RMS} (DW-16) and 370 V_{RMS} (DBQ-16) maximum working voltage (pollution degree 2, material group I); **DW-16:** 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 and IEC 60601-1 Ed. 3.1, 250 V_{RMS} maximum working voltage	**DW-16:** Single protection, 5000 V_{RMS} ; **DBQ-16:** Single protection, 3000 V_{RMS}	**DW-16:** Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V_{RMS} maximum working voltage; **DBQ-16:** Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage	5000 V_{RMS} Reinforced insulation per EN 61010-1:2010 (3rd Ed) up to working voltage of 600 V_{RMS} (DW-16) and 300 V_{RMS} (DBQ-16) 5000 V_{RMS} Reinforced insulation per EN 60950-1:2006/A2:2013 up to working voltage of 800 V_{RMS} (DW-16) and 370 V_{RMS} (DBQ-16)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate number: CQC15001121716 (DW) Certificate number: CQC18001199097 (DBQ)	Client ID number: 77311

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DW-16 PACKAGE						
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 60.3 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 1			377	mA
		$R_{\theta JA}$ = 60.3 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 1			576	
		$R_{\theta JA}$ = 60.3 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 1			754	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 60.3 °C/W, T_J = 150°C, T_A = 25°C, see Figure 3			2073	mW
T_S	Maximum safety temperature(1)				150	°C
DBQ-16 PACKAGE						
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 86.5 °C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C, see Figure 2			263	mA
		$R_{\theta JA}$ = 86.5 °C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C, see Figure 2			401	
		$R_{\theta JA}$ = 86.5 °C/W, V_I = 2.75 V, T_J = 150°C, T_A = 25°C, see Figure 2			525	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 86.5 °C/W, T_J = 150°C, T_A = 25°C, see Figure 4			1445	mW
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.

The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.

$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

6.9 Electrical Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 18	V_{CCO} (1) – 0.4	4.8		V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 18		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see Figure 20	85	100		kV/µs
C_I	Input capacitance (2)	V_I = V_{CC} / 2 + 0.4 × sin (2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.
(2) Measured from input pin to ground.

6.10 Supply Current Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7760-Q1							
Supply current - DC signal	V_I = V_{CC1} (ISO7760-Q1); V_I = 0 V (ISO7760-Q1 with F suffix)		I_{CC1}		1.6	2.3	mA
			I_{CC2}		3	4.9	
	V_I = 0 V (ISO7760-Q1); V_I = V_{CC1} (ISO7760-Q1 with F suffix)		I_{CC1}		8	11.3	
			I_{CC2}		3.3	5.3	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		5	6.4	mA
			I_{CC2}		3.5	5.6	
		10 Mbps	I_{CC1}		5.2	6.7	
			I_{CC2}		6.4	9	
		100 Mbps	I_{CC1}		7	9	
			I_{CC2}		35	44	
ISO7761-Q1							
Supply current - DC signal	V_I = V_{CCI} (1)(ISO7761-Q1); V_I = 0 V (ISO7761-Q1 with F suffix)		I_{CC1}		1.9	2.7	mA
			I_{CC2}		2.9	4.7	
	V_I = 0 V (ISO7761-Q1); V_I = V_{CCI} (ISO7761-Q1 with F suffix)		I_{CC1}		7.3	10.6	
			I_{CC2}		4.2	6.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.7	6.4	mA
			I_{CC2}		3.8	5.9	
		10 Mbps	I_{CC1}		5.3	7.2	
			I_{CC2}		6.3	8.8	
		100 Mbps	I_{CC1}		11.5	15	
			I_{CC2}		30.5	38	
ISO7762-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7762-Q1); V_I = 0 V (ISO7762-Q1 with F suffix)		I_{CC1}		2.1	3.2	mA
			I_{CC2}		2.6	4.2	
	V_I = 0 V (ISO7762-Q1); V_I = V_{CCI} (ISO7762-Q1 with F suffix)		I_{CC1}		6.5	9.3	
			I_{CC2}		5	7.5	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.5	6.3	mA
			I_{CC2}		4	6.1	
		10 Mbps	I_{CC1}		5.6	7.6	
			I_{CC2}		6	8.4	
		100 Mbps	I_{CC1}		16.5	21	
			I_{CC2}		25.7	32	
ISO7763-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7763-Q1); V_I = 0 V (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.4	3.7	mA
	V_I = 0 V (ISO7763-Q1); V_I = V_{CCI} (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		5.7	8.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.2	6.1	mA
		10 Mbps	I_{CC1}, I_{CC2}		5.8	8	
		100 Mbps	I_{CC1}, I_{CC2}		21	26.5	

(1) V_{CCI} = Input-side V_{CC}

6.11 Electrical Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –2 mA; see Figure 18	V_{CCO} (1) – 0.3	3.2		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA; see Figure 18		0.1	0.3	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{CCIIH} = V (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see Figure 20	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.12 Supply Current Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7760-Q1							
Supply current - DC signal	V_I = V_{CC1} (ISO7760-Q1); V_I = 0 V (ISO7760-Q1 with F suffix)		I_{CC1}		1.6	2.2	mA
			I_{CC2}		3	4.8	
	V_I = 0 V (ISO7760-Q1); V_I = V_{CC1} (ISO7760-Q1 with F suffix)		I_{CC1}		8	11.4	
			I_{CC2}		3.3	5.3	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.9	6.6	mA
			I_{CC2}		3.4	5.3	
		10 Mbps	I_{CC1}		5	6.7	
			I_{CC2}		5.5	7.8	
		100 Mbps	I_{CC1}		6.3	8.2	
			I_{CC2}		26	33	
ISO7761-Q1							
Supply current - DC signal	V_I = V_{CCI} (1) (ISO7761-Q1); V_I = 0 V (ISO7761-Q1 with F suffix)		I_{CC1}		1.8	2.7	mA
			I_{CC2}		2.9	4.7	
	V_I = 0 V (ISO7761-Q1); V_I = V_{CCI} (ISO7761-Q1 with F suffix)		I_{CC1}		7.2	10.3	
			I_{CC2}		4.2	6.6	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.6	6.5	mA
			I_{CC2}		3.7	5.7	
		10 Mbps	I_{CC1}		5.1	7	
			I_{CC2}		5.5	7.8	
		100 Mbps	I_{CC1}		9.4	12	
			I_{CC2}		22.8	29	
ISO7762-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7762-Q1); V_I = 0 V (ISO7762-Q1 with F suffix)		I_{CC1}		2.1	3.2	mA
			I_{CC2}		2.5	4.2	
	V_I = 0 V (ISO7762-Q1); V_I = V_{CCI} (ISO7762-Q1 with F suffix)		I_{CC1}		6.5	9.4	
			I_{CC2}		5	7.5	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.4	6.2	mA
			I_{CC2}		3.9	5.8	
		10 Mbps	I_{CC1}		5.2	7.1	
			I_{CC2}		5.4	7.5	
		100 Mbps	I_{CC1}		12.9	16.5	
			I_{CC2}		19.5	25	
ISO7763-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7763-Q1); V_I = 0 V (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.4	3.7	mA
	V_I = 0 V (ISO7763-Q1); V_I = V_{CCI} (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		5.7	8.4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.2	6.2	mA
		10 Mbps	I_{CC1}, I_{CC2}		5.2	7.5	
		100 Mbps	I_{CC1}, I_{CC2}		16	20.5	

(1) V_{CCI} = Input-side V_{CC}

6.13 Electrical Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA; see Figure 18	V_{CCO} (1) – 0.2	2.45		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA; see Figure 18		0.05	0.2	V
$V_{IT+(IN)}$	Rising input threshold voltage			0.6 x V_{CCI}	0.7 x V_{CCI}	V
$V_{IT-(IN)}$	Falling input threshold voltage		0.3 x V_{CCI}	0.4 x V_{CCI}		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		0.1 × V_{CCI}	0.2 x V_{CCI}		V
I_{IH}	High-level input current	V_{IH} = V_{CCI} (1) at INx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx	–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V; see Figure 20	85	100		kV/µs

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}.

6.14 Supply Current Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted).

PARAMETER	TEST CONDITIONS		SUPPLY CURRENT	MIN	TYP	MAX	UNIT
ISO7760-Q1							
Supply current - DC signal	V_I = V_{CC1} (ISO7760-Q1); V_I = 0 V (ISO7760-Q1 with F suffix)		I_{CC1}		1.6	2.2	mA
			I_{CC2}		3	4.8	
	V_I = 0 V (ISO7760-Q1); V_I = V_{CC1} (ISO7760-Q1 with F suffix)		I_{CC1}		8	11.6	
			I_{CC2}		3.3	5.3	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.9	6.8	mA
			I_{CC2}		3.4	5.3	
		10 Mbps	I_{CC1}		5	7	
			I_{CC2}		4.9	7.2	
		100 Mbps	I_{CC1}		6	8	
			I_{CC2}		20.3	26	
ISO7761-Q1							
Supply current - DC signal	V_I = V_{CCI} (1) (ISO7761-Q1); V_I = 0 V (ISO7761-Q1 with F suffix)		I_{CC1}		1.8	2.7	mA
			I_{CC2}		2.9	4.6	
	V_I = 0 V (ISO7761-Q1); V_I = V_{CCI} (ISO7761-Q1 with F suffix)		I_{CC1}		7.2	10.3	
			I_{CC2}		4.2	6.5	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.6	6.7	mA
			I_{CC2}		3.7	5.8	
		10 Mbps	I_{CC1}		4.9	7.1	
			I_{CC2}		5	7.3	
		100 Mbps	I_{CC1}		8.3	10.7	
			I_{CC2}		18.1	24	
ISO7762-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7762-Q1); V_I = 0 V (ISO7762-Q1 with F suffix)		I_{CC1}		2.1	3.2	mA
			I_{CC2}		2.6	4.1	
	V_I = 0 V (ISO7762-Q1); V_I = V_{CCI} (ISO7762-Q1 with F suffix)		I_{CC1}		6.5	9.6	
			I_{CC2}		4.9	7.5	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}		4.4	6.4	mA
			I_{CC2}		3.9	5.8	
		10 Mbps	I_{CC1}		5	7.1	
			I_{CC2}		5	7.1	
		100 Mbps	I_{CC1}		10.9	14.1	
			I_{CC2}		15.6	20.1	
ISO7763-Q1							
Supply current - DC signal	V_I = V_{CCI} (ISO7763-Q1); V_I = 0 V (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		2.3	3.7	mA
	V_I = 0 V (ISO7763-Q1); V_I = V_{CCI} (ISO7763-Q1 with F suffix)		I_{CC1}, I_{CC2}		5.7	8.4	
Supply current - AC signal	All channels switching with square wave clock input; C_L = 15 pF	1 Mbps	I_{CC1}, I_{CC2}		4.1	6.1	mA
		10 Mbps	I_{CC1}, I_{CC2}		4.9	7.1	
		100 Mbps	I_{CC1}, I_{CC2}		13	17	

(1) V_{CCI} = Input-side V_{CC}

6.15 Switching Characteristics—5-V Supply

V_{CC1} = V_{CC2} = 5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 18	6	11	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.4	4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 18		1.1	3.9	ns
t_f	Output signal fall time			1.4	3.9	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 19		0.2	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1.3		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.16 Switching Characteristics—3.3-V Supply

V_{CC1} = V_{CC2} = 3.3 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 18	6	12	16	ns
PWD	Pulse width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	5	ns
$t_{sk(o)}$	Channel-to-channel output skew time(2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time(3)				4.5	ns
t_r	Output signal rise time	See Figure 18		1	3	ns
t_f	Output signal fall time			1	3	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 19		0.2	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1.3		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.17 Switching Characteristics—2.5-V Supply

V_{CC1} = V_{CC2} = 2.5 V ±10% (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 18	7.5	13	18.5	ns
PWD	Pulse width distortion (1) $\lvert t_{PHL} - t_{PLH} \rvert$			0.6	5.1	ns
$t_{sk(o)}$	Channel-to-channel output skew time (2)	Same-direction channels			4.1	ns
$t_{sk(pp)}$	Part-to-part skew time (3)				4.6	ns
t_r	Output signal rise time	See Figure 18		1	3.5	ns
t_f	Output signal fall time			1	3.5	ns
t_{DO}	Default output delay time from input power loss	Measured from the time V_{CC} goes below 1.7 V. See Figure 19		0.1	0.3	µs
t_{ie}	Time interval error	2^{16} – 1 PRBS data at 100 Mbps		1.3		ns

(1) Also known as pulse skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

6.18 Insulation Characteristics Curves

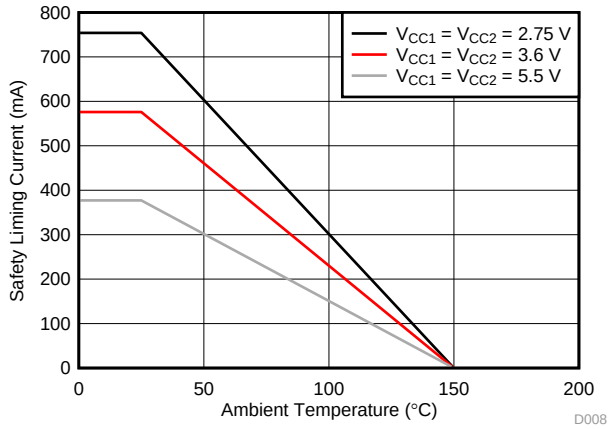


Figure 1. Thermal Derating Curve for Limiting Current per VDE for DW-16 Package

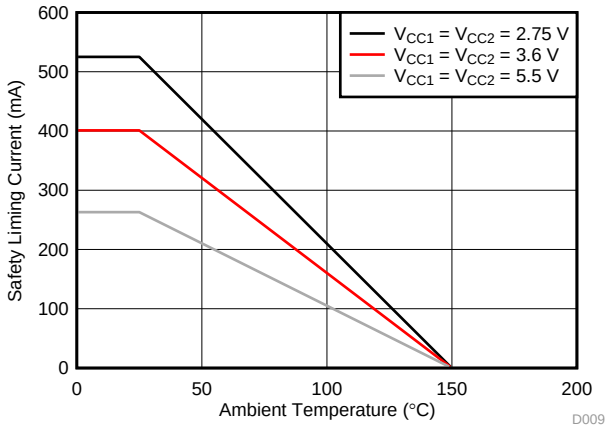


Figure 2. Thermal Derating Curve for Limiting Current per VDE for DBQ-16 Package

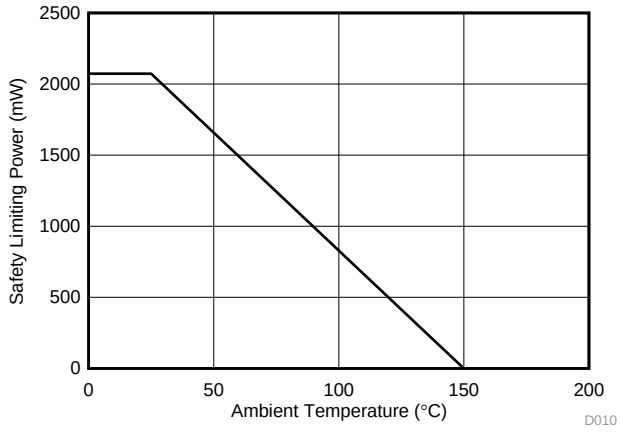


Figure 3. Thermal Derating Curve for Limiting Power per VDE for DW-16 Package

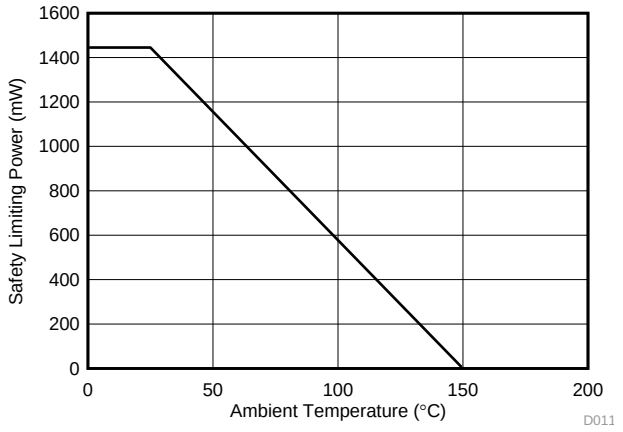
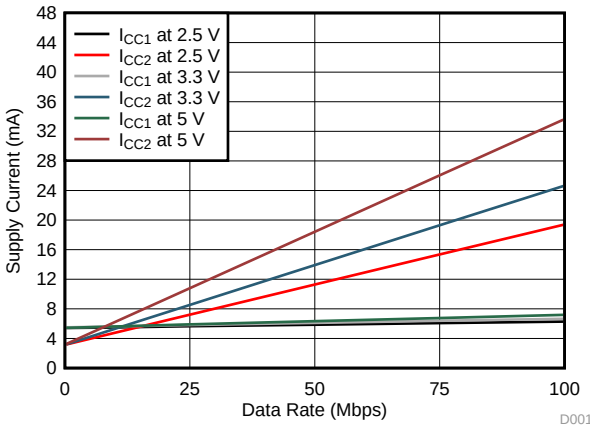


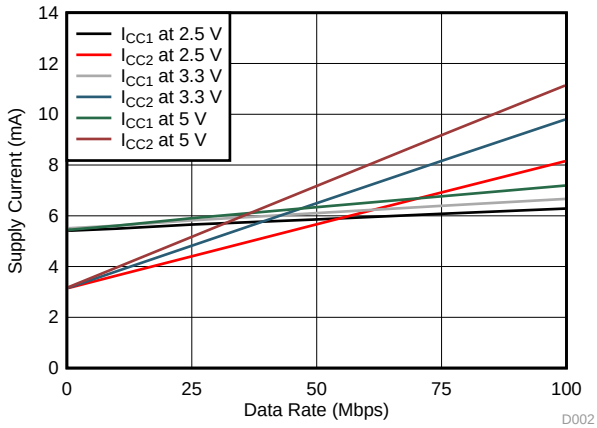
Figure 4. Thermal Derating Curve for Limiting Power per VDE for DBQ-16 Package

6.19 Typical Characteristics



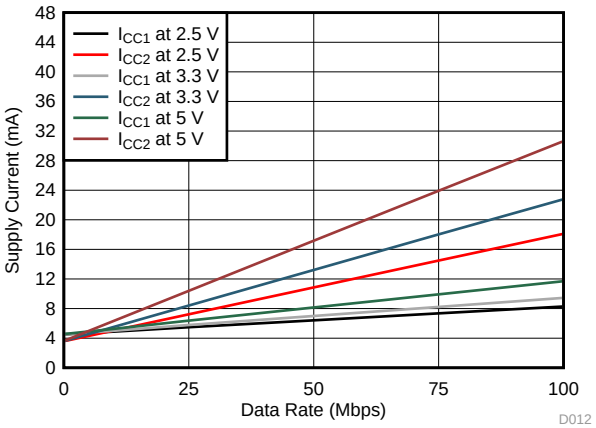
T_A = 25°C C_L = 15 pF

Figure 5. ISO7760-Q1 Supply Current vs Data Rate (With 15-pF Load)



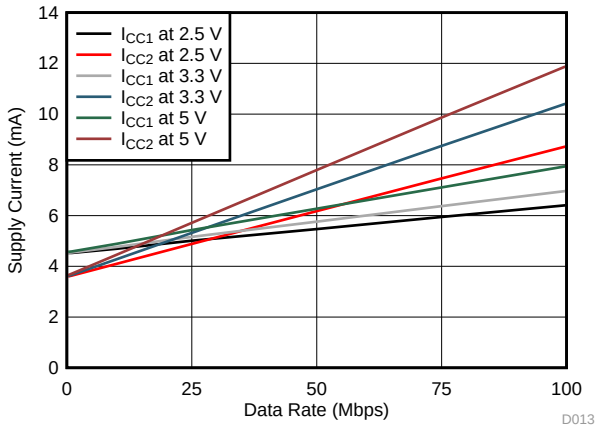
T_A = 25°C C_L = No Load

Figure 6. ISO7760-Q1 Supply Current vs Data Rate (With No Load)



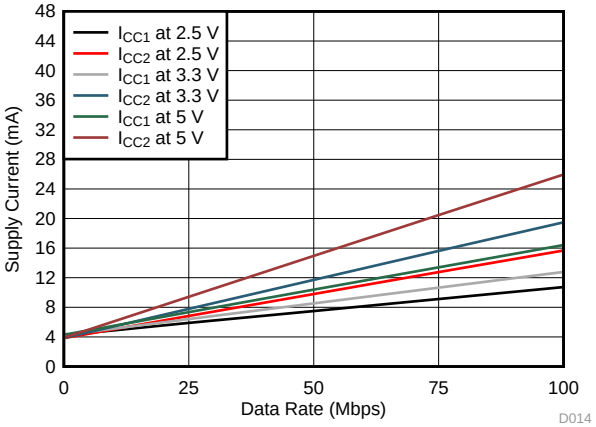
T_A = 25°C C_L = 15 pF

Figure 7. ISO7761-Q1 Supply Current vs Data Rate (With 15-pF Load)



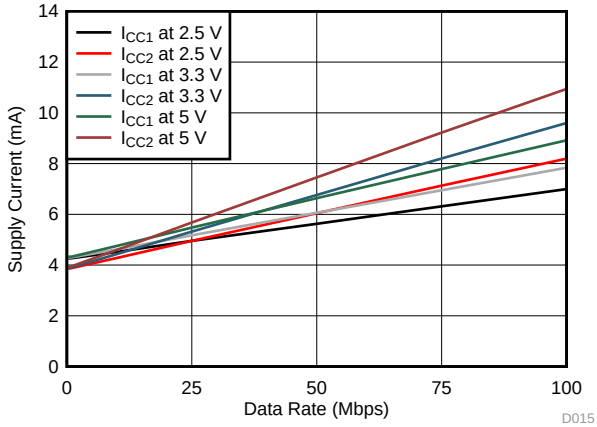
T_A = 25°C C_L = No Load

Figure 8. ISO7761-Q1 Supply Current vs Data Rate (With No Load)



T_A = 25°C C_L = 15 pF

Figure 9. ISO7762-Q1 Supply Current vs Data Rate (With 15-pF Load)



T_A = 25°C C_L = No Load

Figure 10. ISO7762-Q1 Supply Current vs Data Rate (With No Load)

Typical Characteristics (continued)

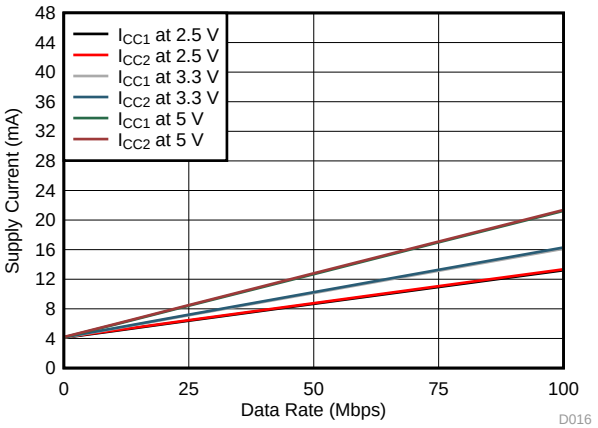


Figure 11. ISO7763-Q1 Supply Current vs Data Rate (With 15-pF Load)

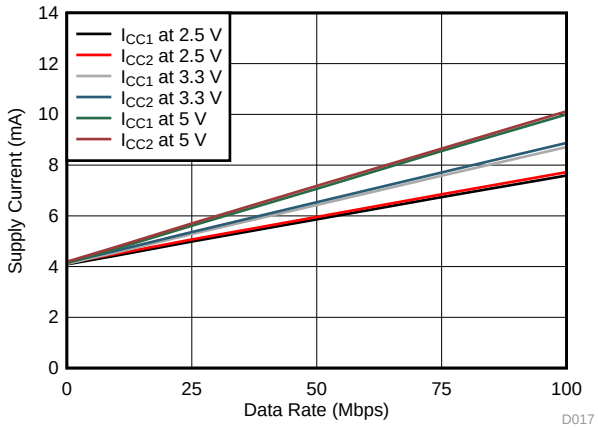


Figure 12. ISO7763-Q1 Supply Current vs Data Rate (With No Load)

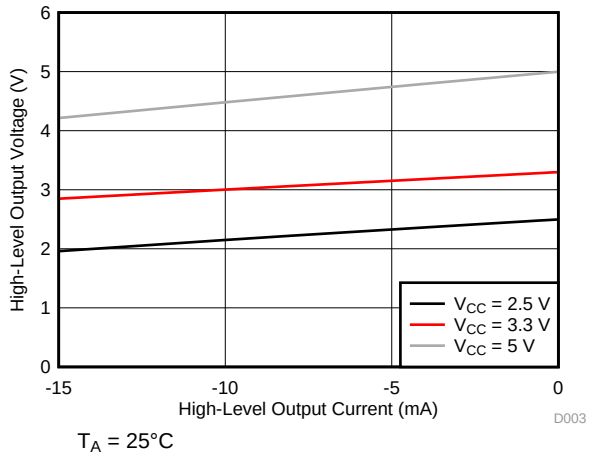


Figure 13. High-Level Output Voltage vs High-Level Output Current

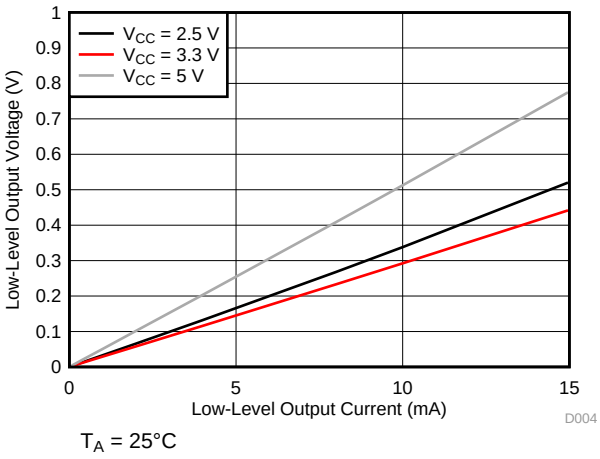


Figure 14. Low-Level Output Voltage vs Low-Level Output Current

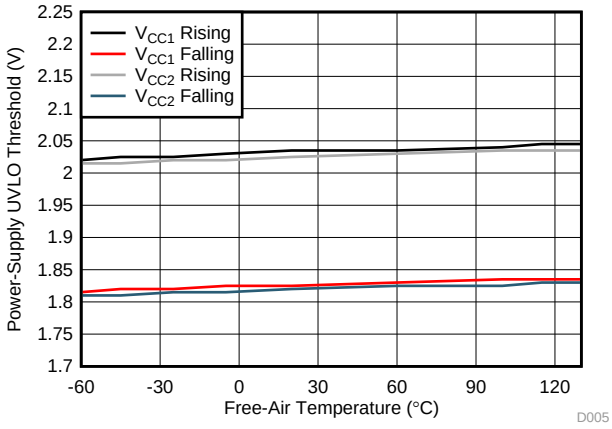


Figure 15. Power Supply Undervoltage Threshold vs Free-Air Temperature

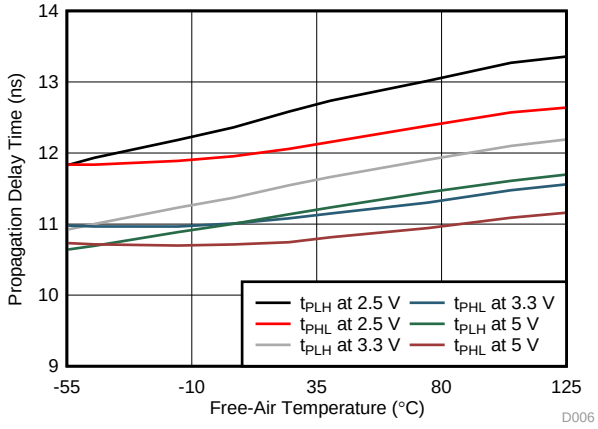
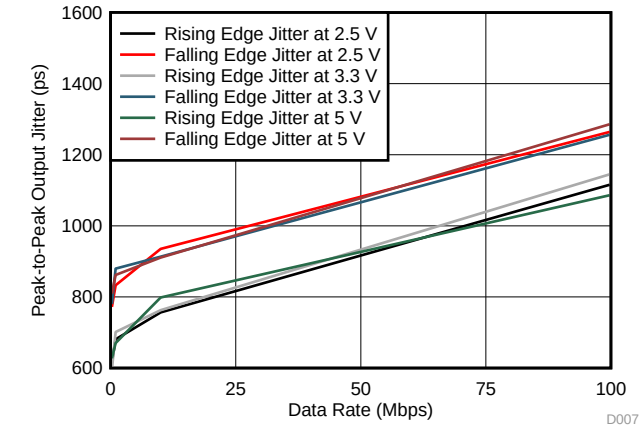


Figure 16. Propagation Delay Time vs Free-Air Temperature

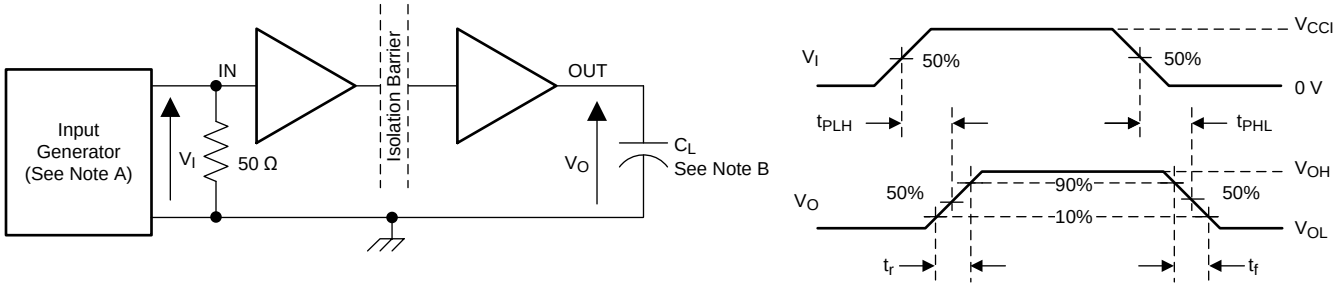
Typical Characteristics (continued)



T_A = 25°C

Figure 17. Peak-to-Peak Output Jitter vs Data Rate

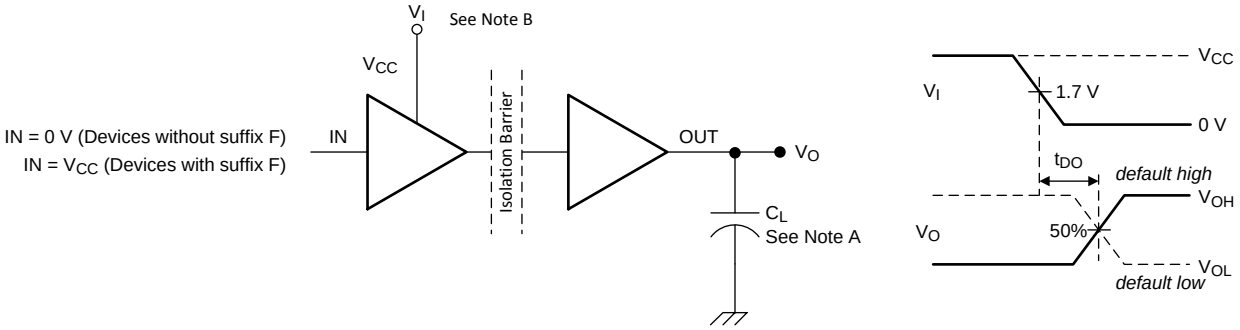
7 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

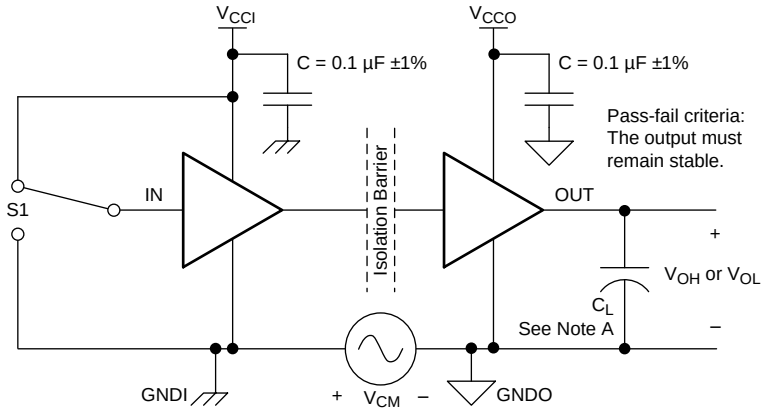
Figure 18. Switching Characteristics Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. Power-supply ramp rate = 10 mV/ns

Figure 19. Default Output Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 20. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO776x-Q1 family of devices uses an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The ISO776x-Q1 family of devices also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions because of the high-frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, Figure 21, shows a functional block diagram of a typical channel. Figure 22 shows a conceptual detail of how the ON-OFF keying scheme works.

8.2 Functional Block Diagram

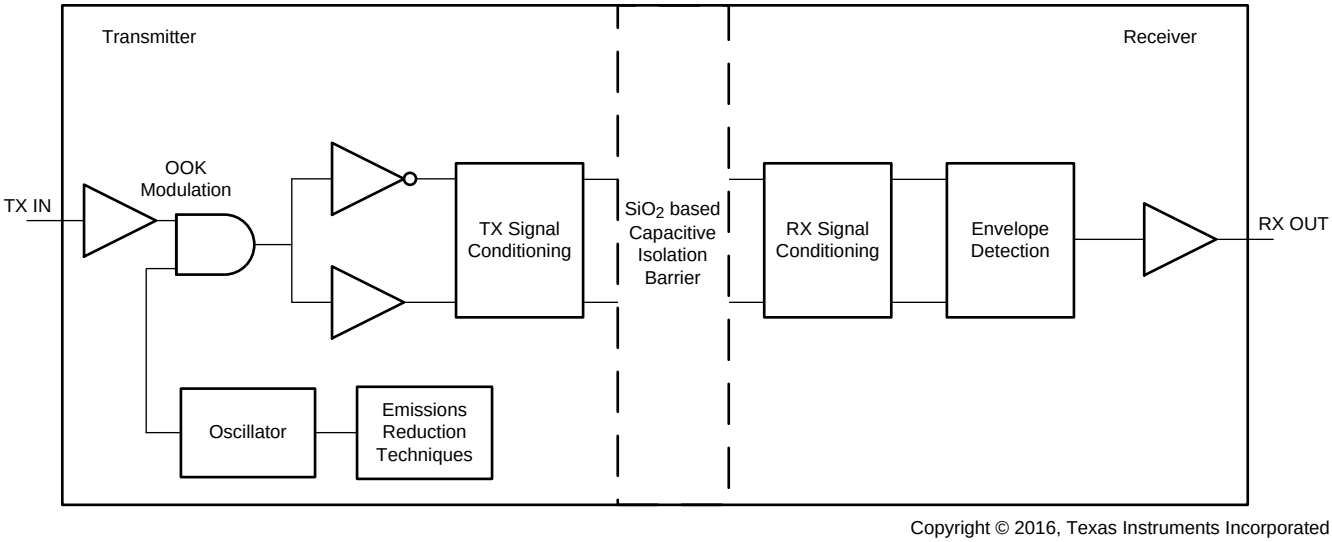


Figure 21. Conceptual Block Diagram of a Digital Capacitive Isolator

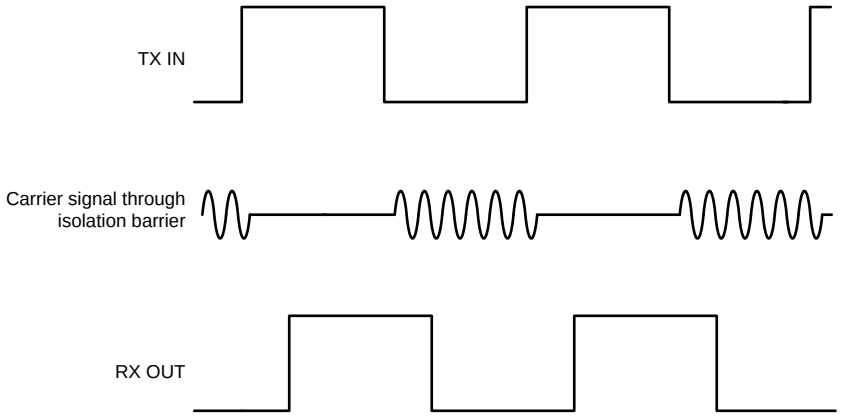


Figure 22. ON-OFF Keying (OOK) Based Modulation Scheme

8.3 Feature Description

Table 1 lists the device features.

Table 1. Device Features

PART NUMBER	CHANNEL DIRECTION	MAXIMUM DATA RATE	DEFAULT OUTPUT	PACKAGE	RATED ISOLATION(1)
ISO7760-Q1	6 Forward, 0 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7760-Q1 with F suffix	6 Forward, 0 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7761-Q1	5 Forward, 1 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7761-Q1 with F suffix	5 Forward, 1 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7762-Q1	4 Forward, 2 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7762-Q1 with F suffix	4 Forward, 2 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7763-Q1	3 Forward, 3 Reverse	100 Mbps	High	DW-16	5000 V_{RMS} / 8000V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}
ISO7763-Q1 with F suffix	3 Forward, 3 Reverse	100 Mbps	Low	DW-16	5000 V_{RMS} / 8000 V_{PK}
				DBQ-16	3000 V_{RMS} / 4242 V_{PK}

(1) See *Safety-Related Certifications* for detailed isolation ratings.

8.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO776x-Q1 family of devices incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by ensuring purely differential internal operation.

8.4 Device Functional Modes

Table 2 lists the functional modes for the ISO776x-Q1.

Table 2. Function Table(1)

V_{CCI}	V_{CCO}	INPUT (INx)(2)	OUTPUT (OUTx)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When INx is open, the corresponding channel output goes to its default logic state. Default is *High* for ISO776x-Q1 and *Low* for ISO776x-Q1 with F suffix.
PD	PU	X	Default	Default mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on the selected default option. Default is *High* for ISO776x-Q1 and *Low* for ISO776x-Q1 with F suffix. When V_{CCI} transitions from unpowered to powered-up, a channel output assumes the logic state of its input. When V_{CCI} transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When V_{CCO} is unpowered, a channel output is undetermined (3). When V_{CCO} transitions from unpowered to powered-up, a channel output assumes the logic state of the input

(1) V_{CCI} = Input-side V_{CC}; V_{CCO} = Output-side V_{CC}; PU = Powered up (V_{CC} ≥ 2.25 V); PD = Powered down (V_{CC} ≤ 1.7 V); X = Irrelevant; H = High level; L = Low level
(2) A strongly driven input signal can weakly power the floating V_{CC} via an internal protection diode and cause undetermined output.
(3) The outputs are in undetermined state when 1.7 V < V_{CCI}, V_{CCO} < 2.25 V.

8.4.1 Device I/O Schematics

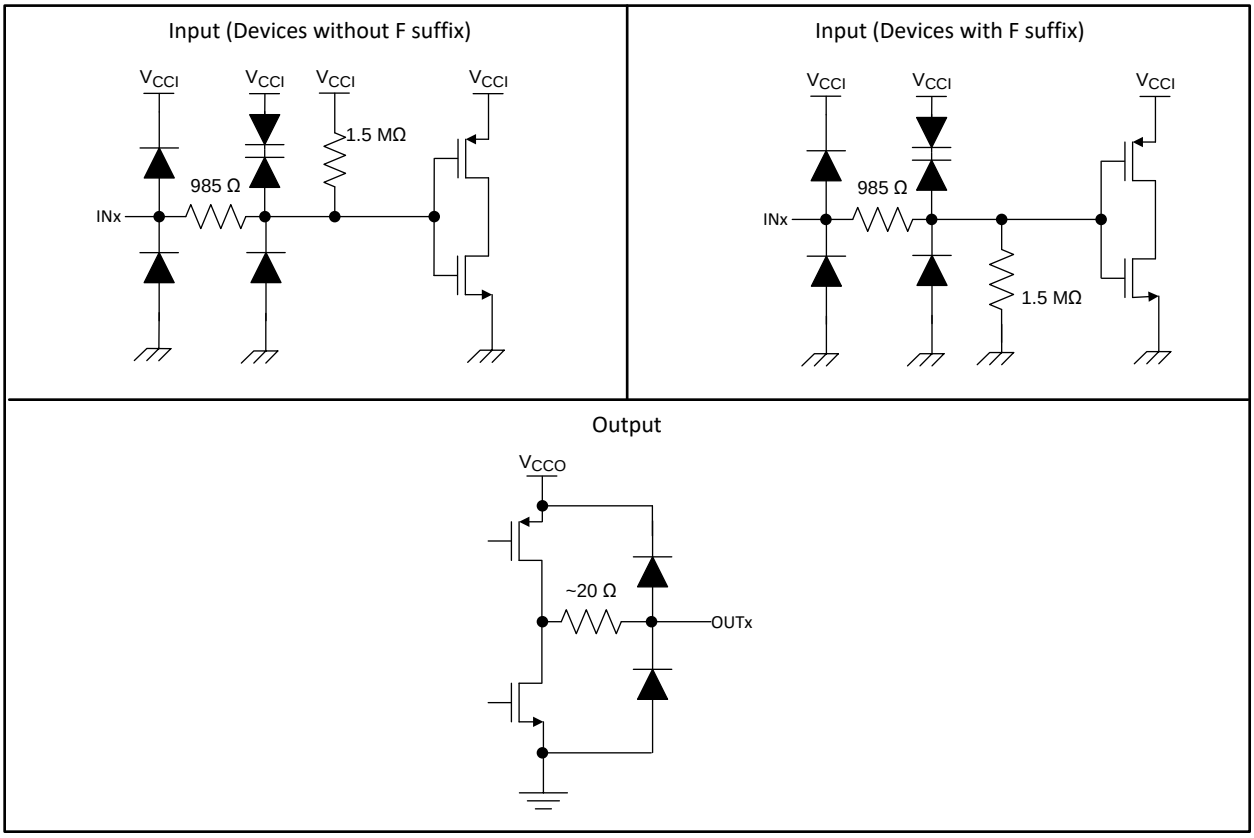


Figure 23. Device I/O Schematics

9 Application and Implementation

NOTE

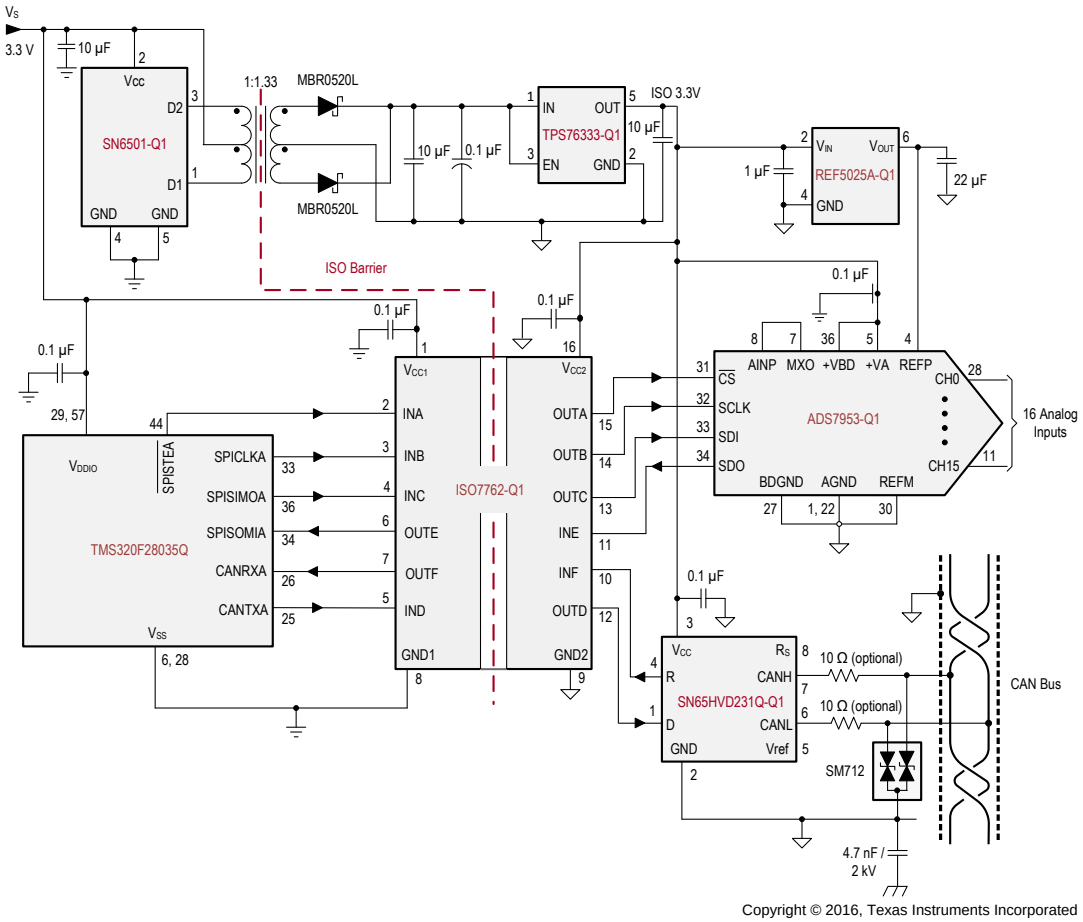
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO776x-Q1 family of devices is a high-performance, six-channel digital isolators. The ISO776x-Q1 family of devices uses single-ended CMOS-logic switching technology. The voltage range is from 2.25 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, μC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

Figure 24 shows the isolated serial-peripheral interface (SPI) and controller-area network (CAN) interface implementation.



NOTE: Multiple pins and discrete components omitted for clarity purpose.

Figure 24. Isolated SPI and CAN Interface

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 3.

Table 3. Design Parameters

PARAMETER	VALUE
Supply voltage, V_{CC1} and V_{CC2}	2.25 to 5.5 V
Decoupling capacitor between V_{CC1} and GND1	0.1 µF
Decoupling capacitor from V_{CC2} and GND2	0.1 µF

9.2.2 Detailed Design Procedure

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO776x-Q1 family of devices only requires two external bypass capacitors to operate.

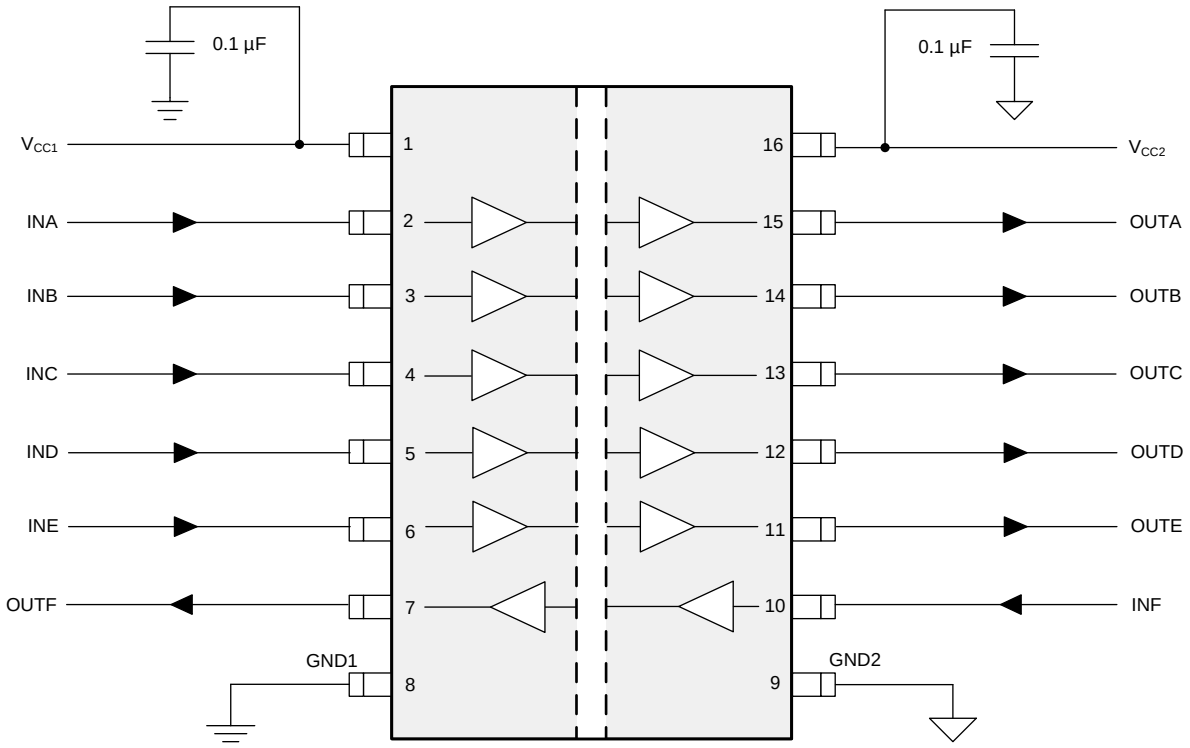


Figure 25. Typical ISO7761-Q1 Circuit Hook-up

9.2.3 Application Curves

The typical eye diagram of the ISO776x-Q1 family of devices indicates low jitter and a wide open eye at the maximum data rate of 100 Mbps.

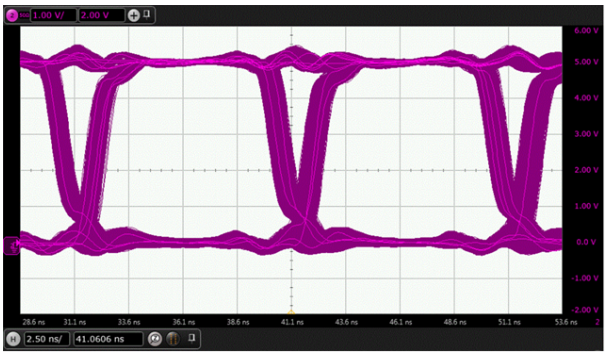


Figure 26. Eye Diagram at 100 Mbps PRBS 2^{16} – 1 Data, 5 V and 25°C

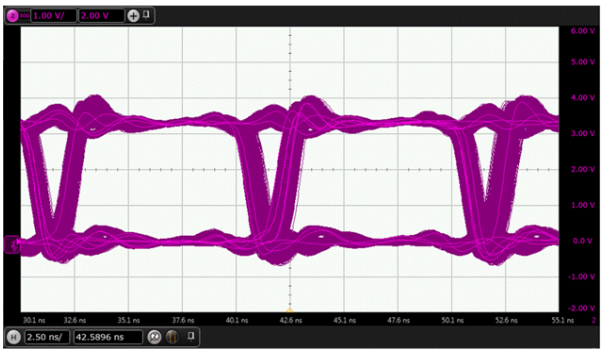


Figure 27. Eye Diagram at 100 Mbps PRBS 2^{16} – 1 Data, 3.3 V and 25°C

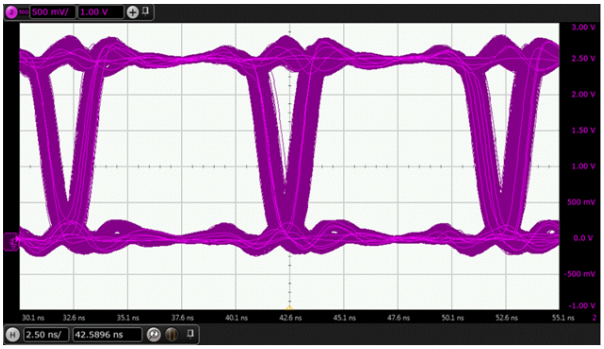


Figure 28. Eye Diagram at 100 Mbps PRBS 2^{16} – 1 Data, 2.5 V and 25°C

9.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See Figure 29 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

Figure 30 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V_{RMS} with a lifetime of 135 years. Other factors, such as package size, pollution degree, material group, etc. can further limit the working voltage of the component. The working voltage of DW-16 package is specified upto 1500 V_{RMS} and DBQ-16 package up to 400 V_{RMS}. At the lower working voltages, the corresponding insulation lifetime is much longer than 135 years.

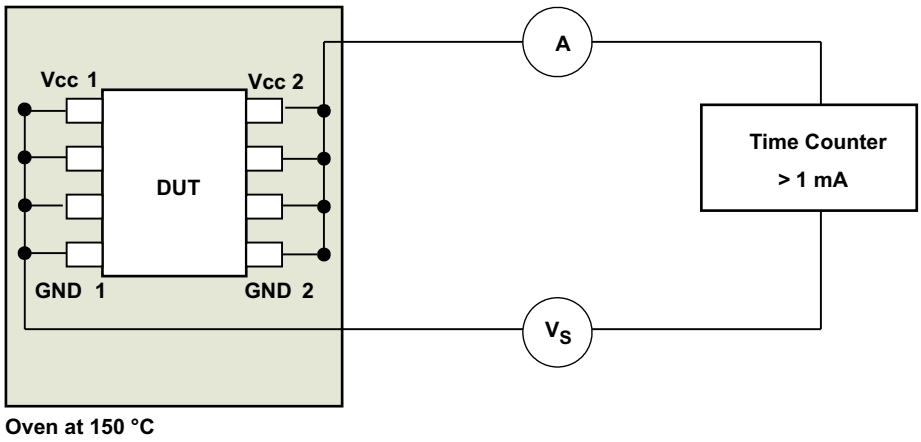


Figure 29. Test Setup for Insulation Lifetime Measurement

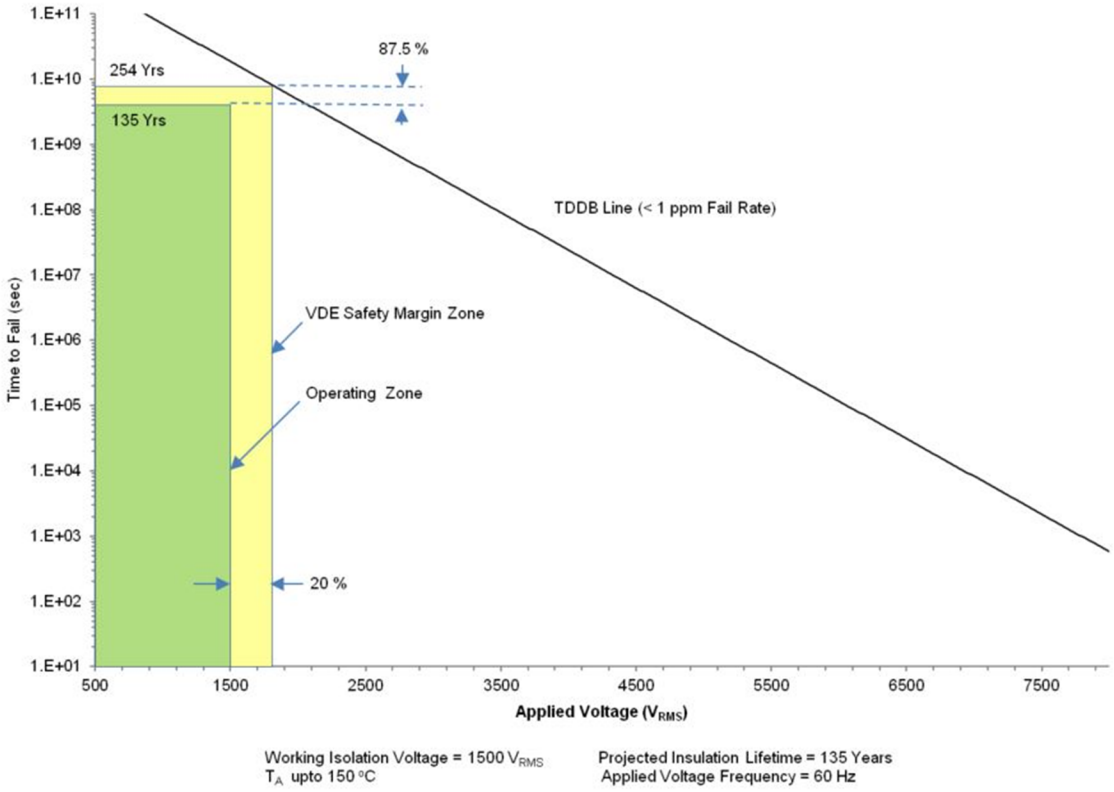


Figure 30. Insulation Lifetime Projection Data

10 Power Supply Recommendations

To help ensure reliable operation at data rates and supply voltages, a 0.1-μF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505. For such applications, detailed power supply design and transformer selection recommendations are available in the *SN6501 Transformer Driver for Isolated Power Supplies* data sheet or the *SN6505 Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 31). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/inch^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see the *Digital Isolator Design Guide* application report.

11.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11.2 Layout Example

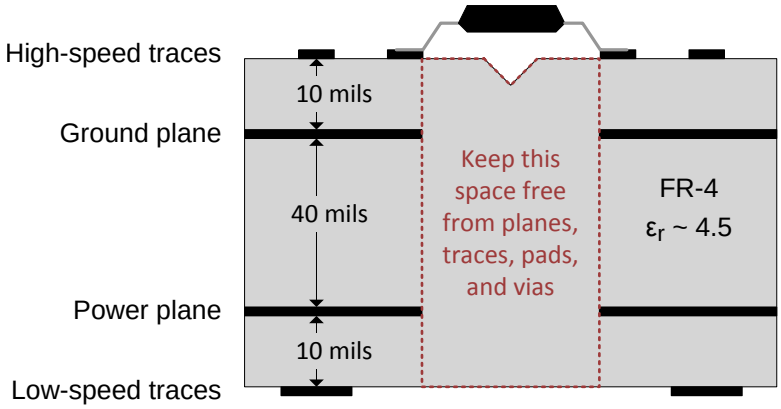


Figure 31. Layout Example Schematic

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide* application report
- Texas Instruments, *How to use isolation to improve ESD, EFT and Surge immunity in industrial systems* application report
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers* data sheet
- Texas Instruments, *ADS7953-Q1 Automotive 12-Bit, 1MSPS, 16-Channel Single-Ended Micropower, Serial Interface ADC* data sheet
- Texas Instruments, *REF50xxA-Q1 Low-Noise, Very Low Drift, Precision Voltage Reference* data sheet
- Texas Instruments, *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *SN65HVD231Q-Q1 3.3-V CAN Transceiver* data sheet
- Texas Instruments, *TPS76333-Q1 Low-Power 150-mA Low-Dropout Linear Regulators* data sheet

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7760-Q1	Click here	Click here	Click here	Click here	Click here
ISO7761-Q1	Click here	Click here	Click here	Click here	Click here
ISO7762-Q1	Click here	Click here	Click here	Click here	Click here
ISO7763-Q1	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

Piccolo, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

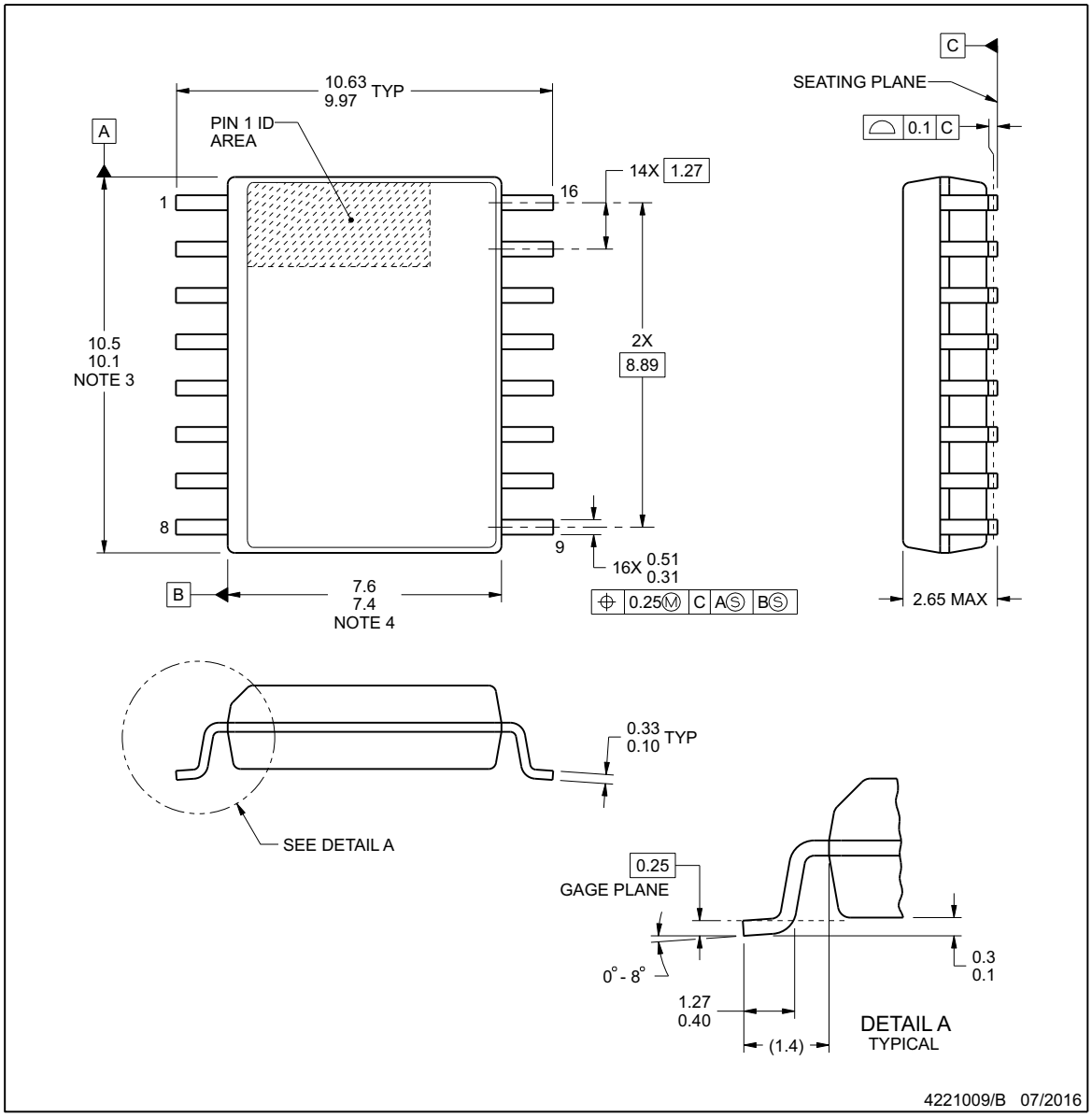
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES:

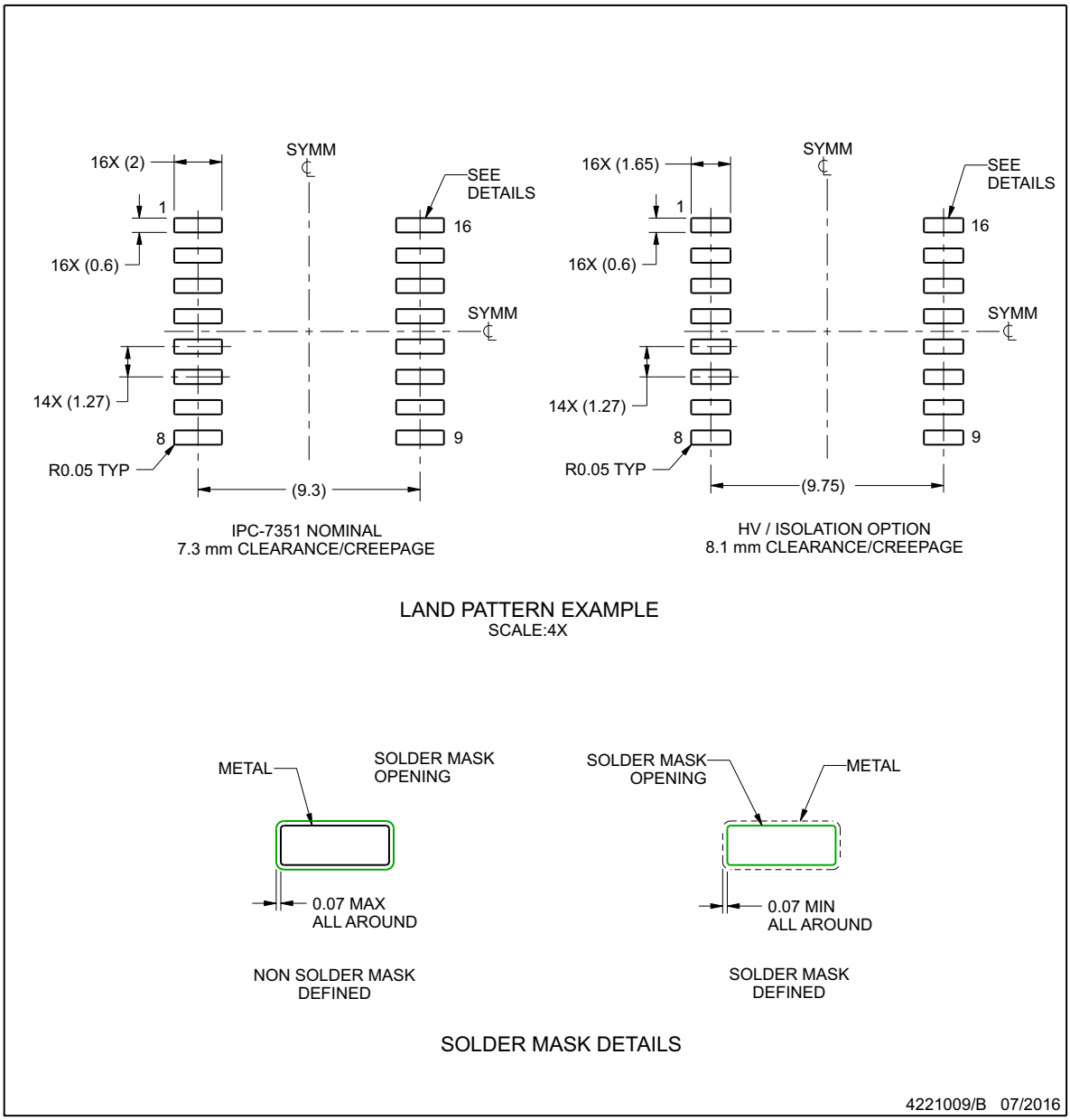
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

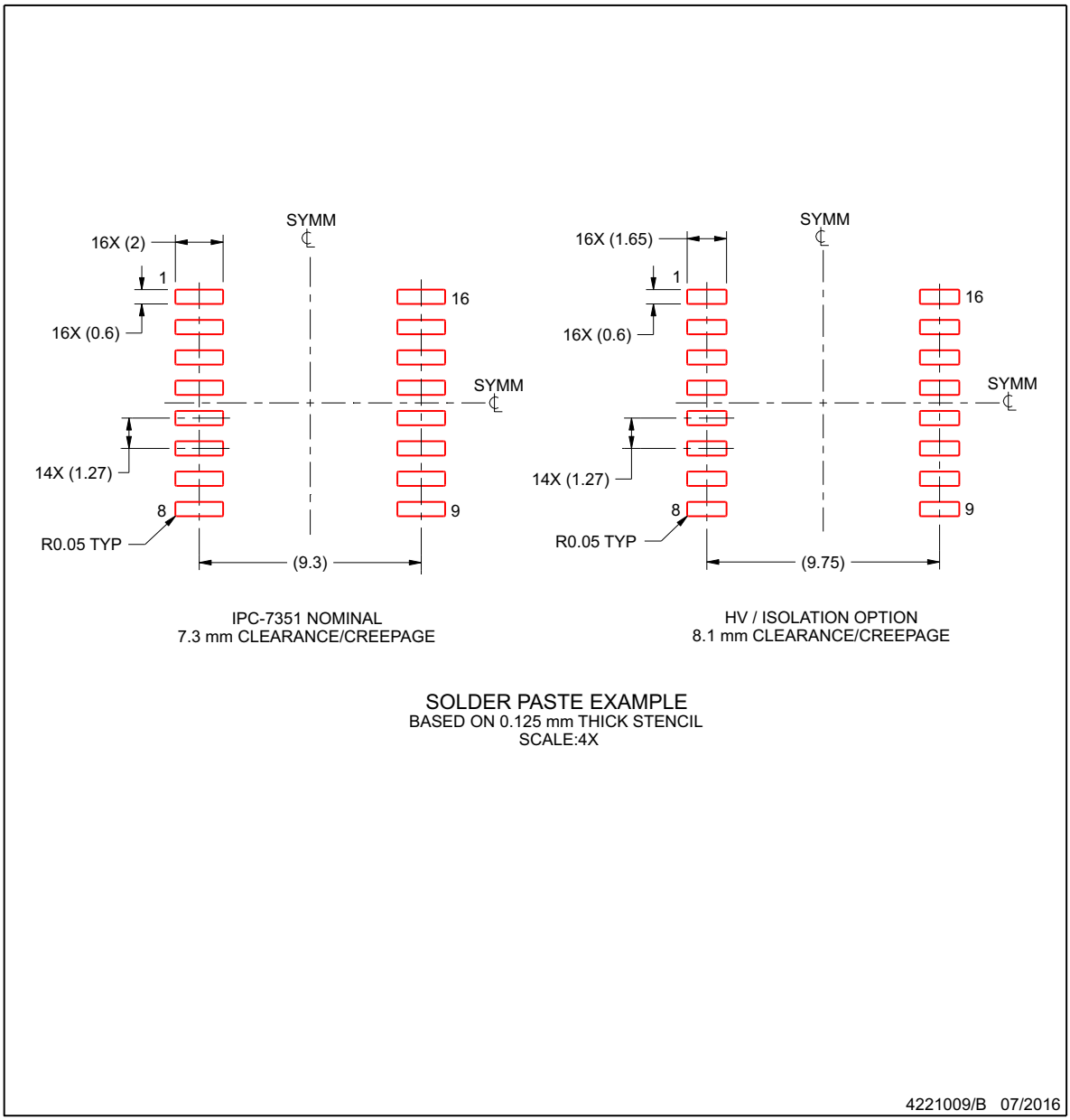
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7760FQDBQQ1	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7760FQ	Samples
ISO7760FQDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7760FQ	Samples
ISO7760FQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7760FQ	Samples
ISO7760FQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7760FQ	Samples
ISO7760QDBQQ1	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7760Q	Samples
ISO7760QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7760Q	Samples
ISO7760QDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7760Q	Samples
ISO7760QDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7760Q	Samples
ISO7761FQDBQQ1	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7761FQ	Samples
ISO7761FQDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7761FQ	Samples
ISO7761FQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7761FQ	Samples
ISO7761FQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7761FQ	Samples
ISO7761QDBQQ1	ACTIVE	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7761Q	Samples
ISO7761QDBQRQ1	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7761Q	Samples
ISO7761QDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7761Q	Samples
ISO7761QDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7761Q	Samples
ISO7762FQDBQQ1	PREVIEW	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7762FQ	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7762FQDBQRQ1	PREVIEW	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7762FQ	
ISO7762FQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7762FQ	Samples
ISO7762FQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7762FQ	Samples
ISO7762QDBQQ1	PREVIEW	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7762Q	
ISO7762QDBQRQ1	PREVIEW	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	Call TI	Level-2-260C-1 YEAR	-40 to 125	7762Q	
ISO7762QDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7762Q	Samples
ISO7762QDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7762Q	Samples
ISO7763FQDBQQ1	PREVIEW	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7763FQ	
ISO7763FQDBQRQ1	PREVIEW	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7763FQ	
ISO7763FQDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7763FQ	Samples
ISO7763FQDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7763FQ	Samples
ISO7763QDBQQ1	PREVIEW	SSOP	DBQ	16	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7763Q	
ISO7763QDBQRQ1	PREVIEW	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7763Q	
ISO7763QDWQ1	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7763Q	Samples
ISO7763QDWRQ1	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO7763Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF ISO7760-Q1, ISO7761-Q1, ISO7762-Q1, ISO7763-Q1 :

- Catalog: ISO7760, ISO7761, ISO7762, ISO7763

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

GENERIC PACKAGE VIEW

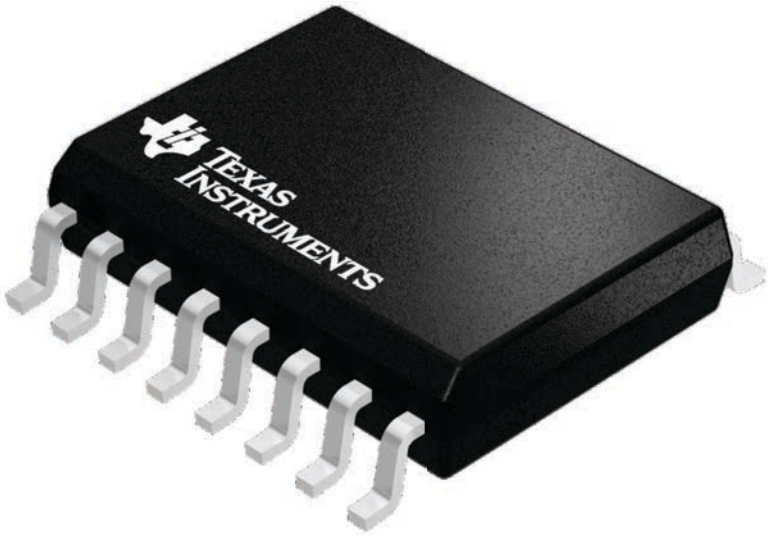
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

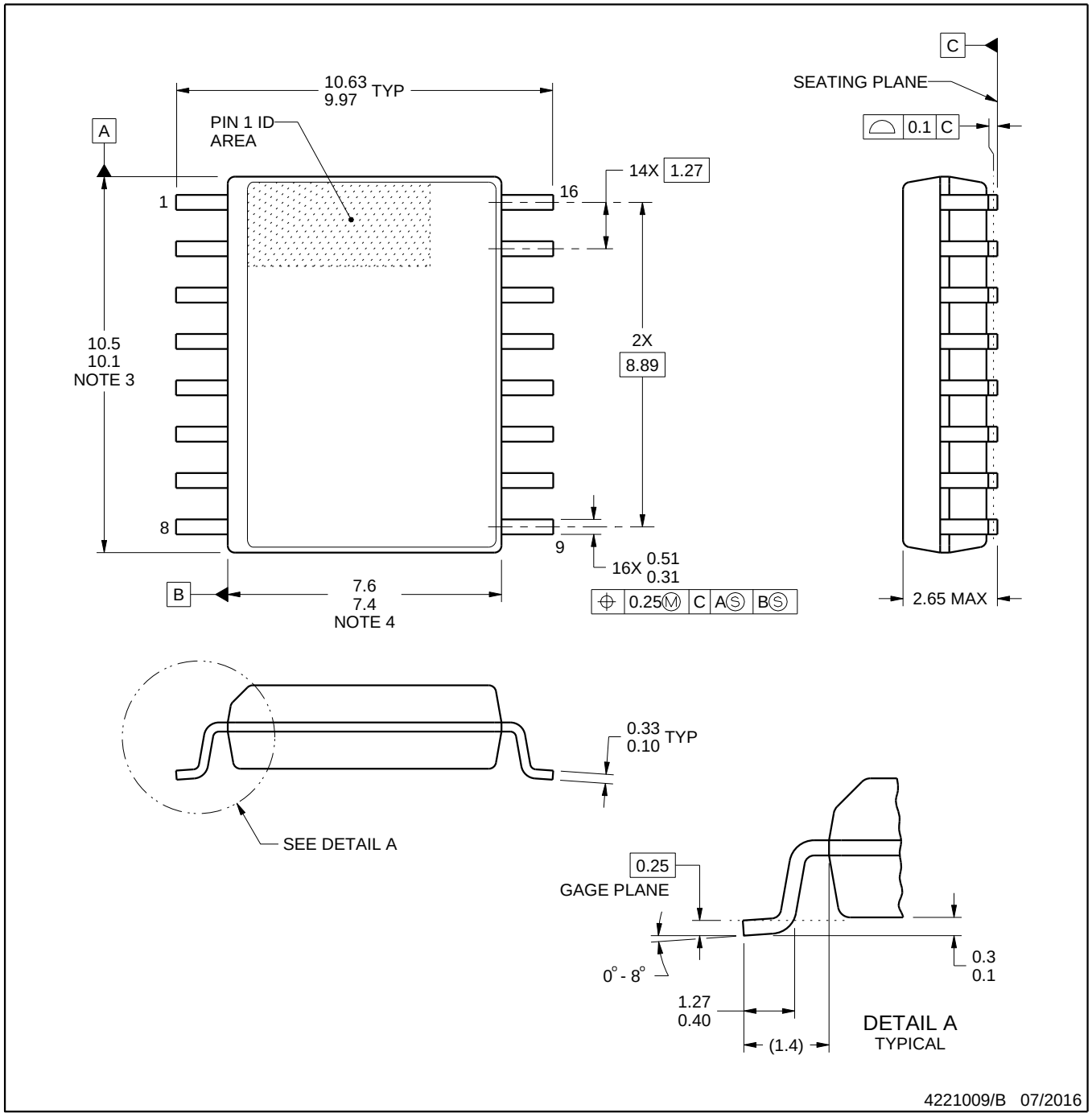
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



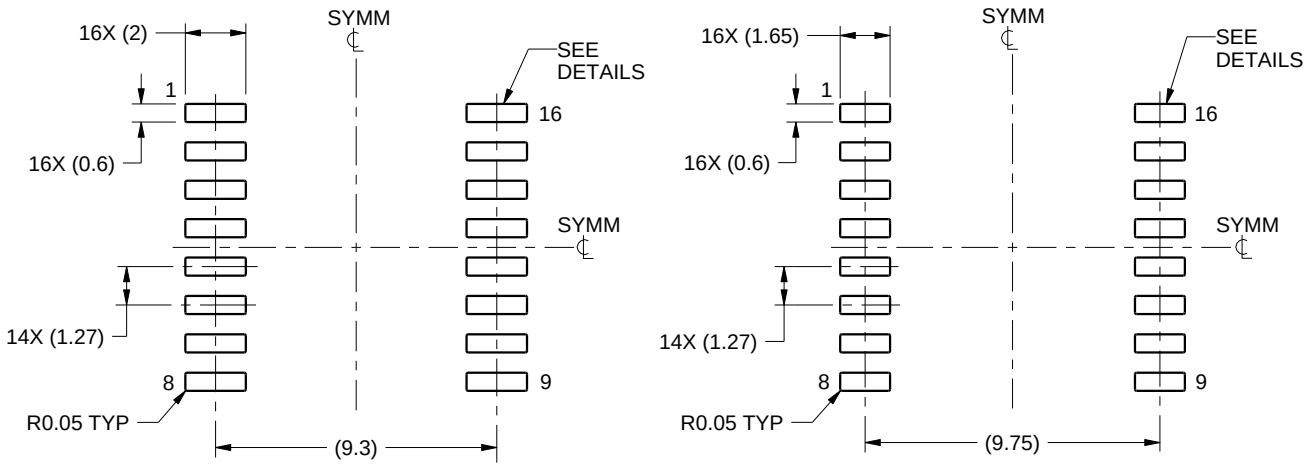
4224780/A

SOIC



NOTES:

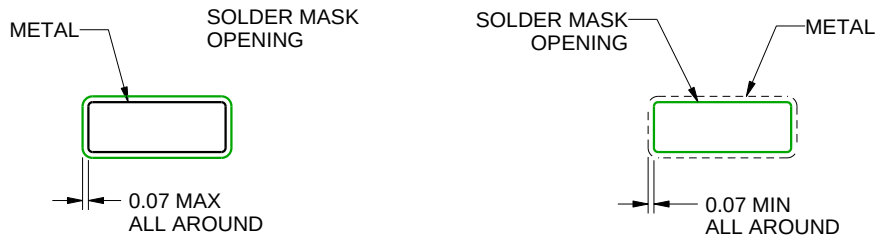
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

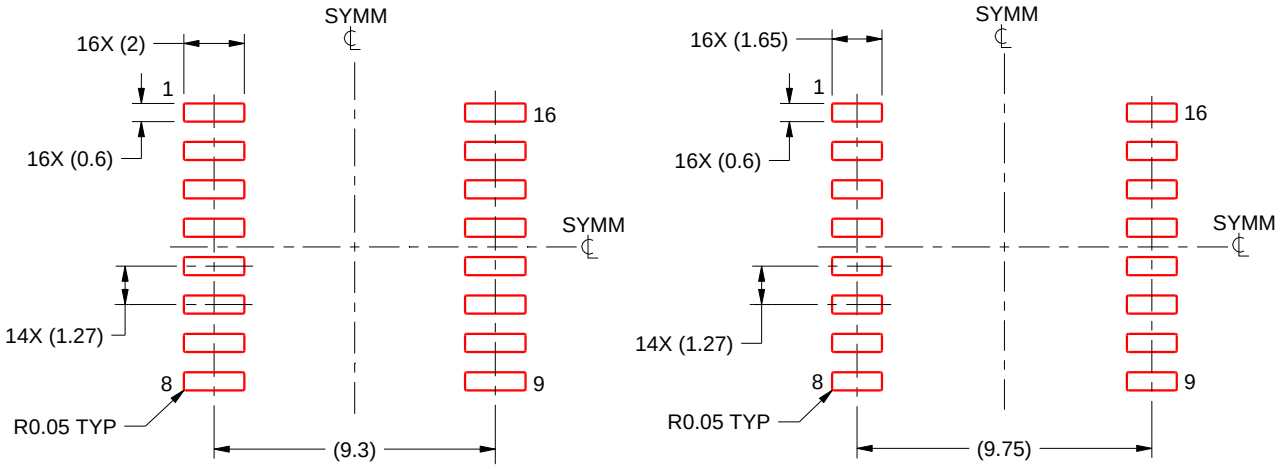
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

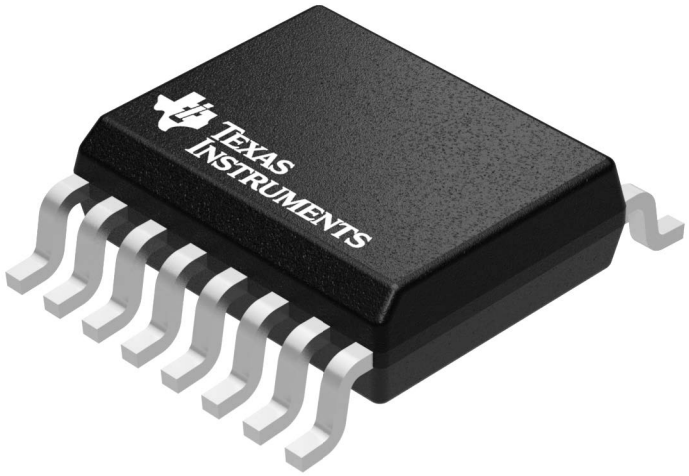
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

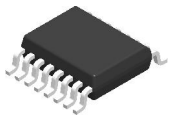
GENERIC PACKAGE VIEW

DBQ 16 SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

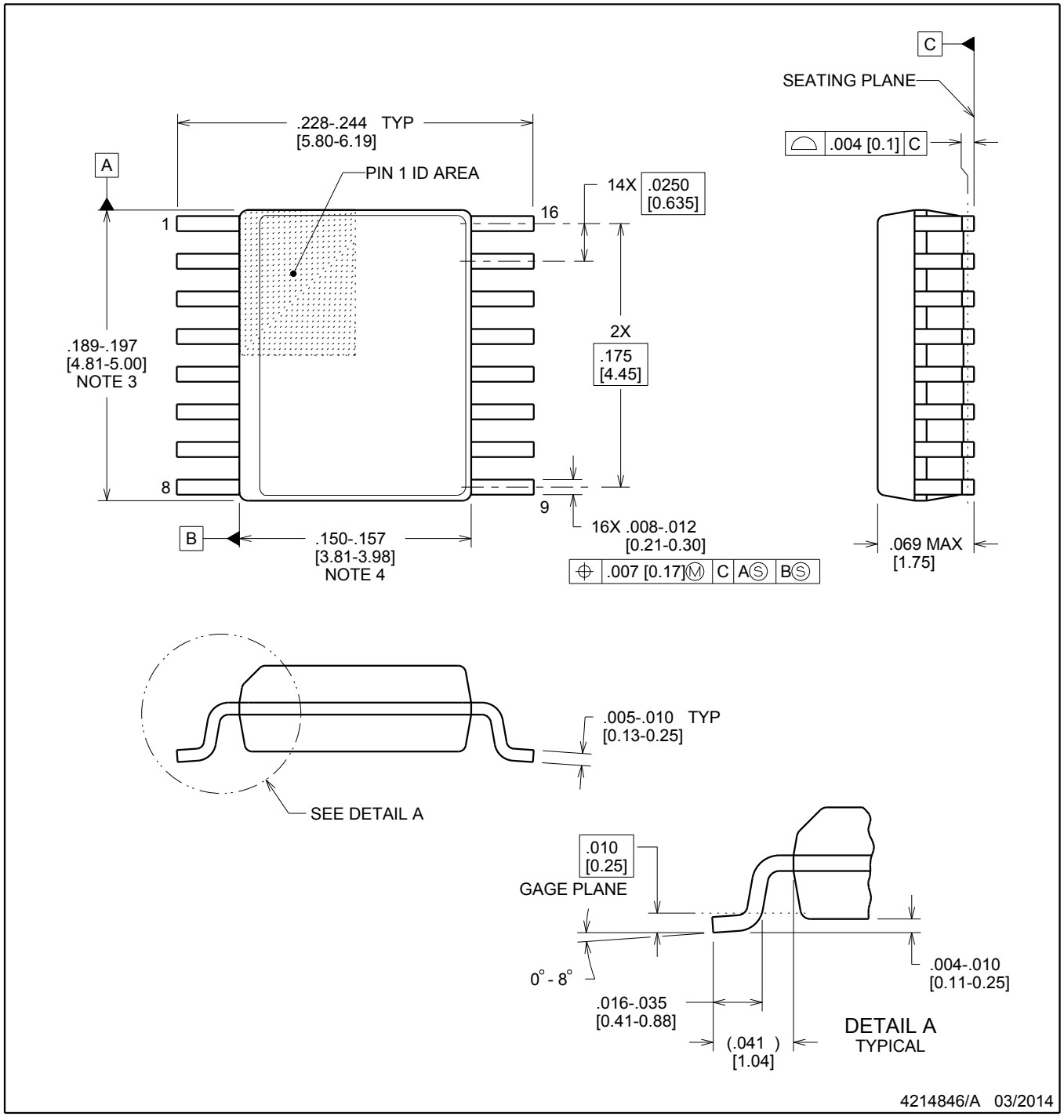


PACKAGE OUTLINE

DBQ0016A

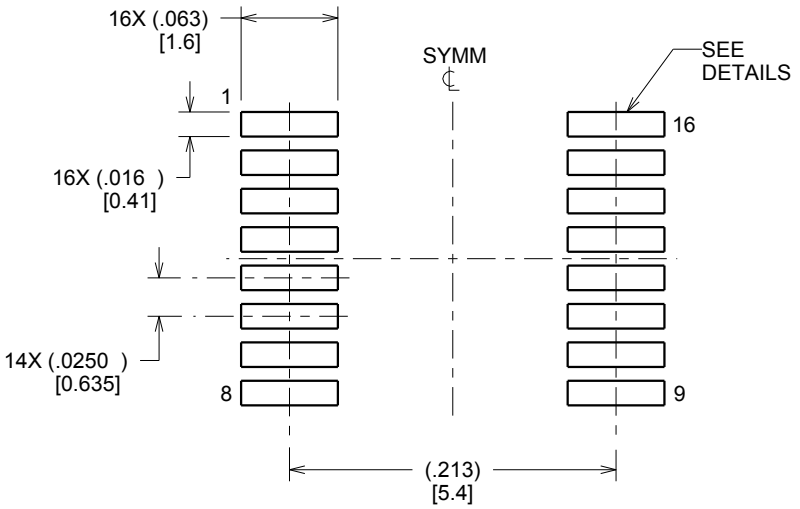
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

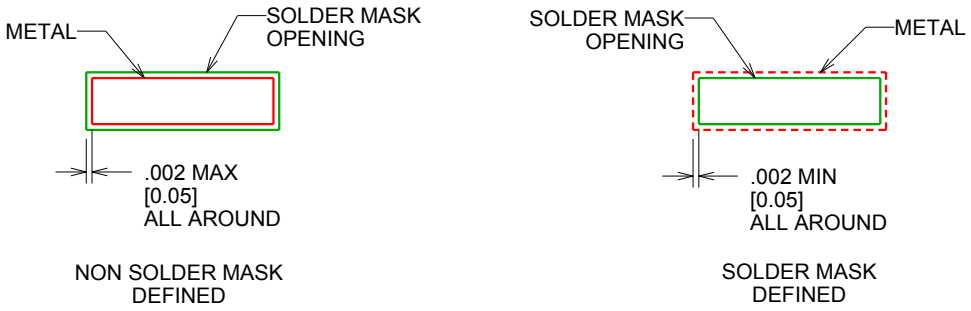


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

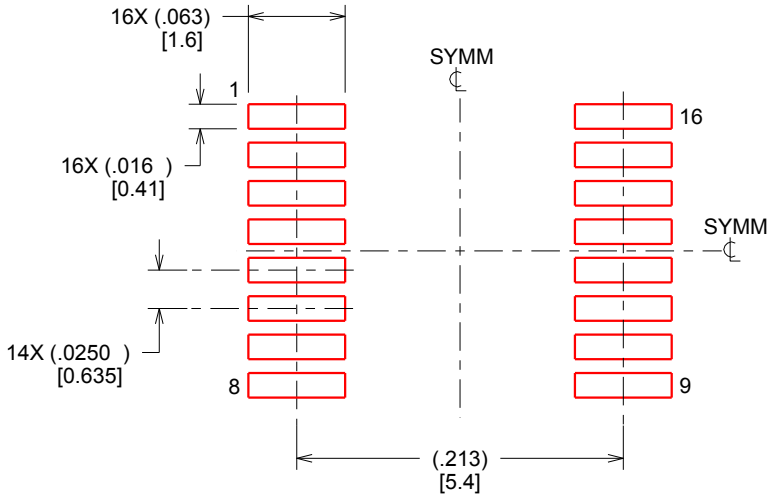
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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