Introduction

The PCI Express interconnect technology is analogous to high performance. We have seen many usage models where PCI Express is used in high performance applications. Graphics, Servers and Storage are a few that we can relate to which have high bandwidth requirements. Such systems make use of multiple PCIe ports each with at least x4 link widths for up to 16Gbps throughput at Gen 2 (5.0 GT/s) speeds. A bandwidth bridge usage model exploits the performance benefits of Gen 2 in slower Gen 1 (2.5 GT/s) systems.

The Need for a PCIe Switch

Because a point-to-point technology provides a direct connection between two devices, the approach for providing expansion to three or more devices requires the use of a PCIe switch. A PCIe switch provides many connections known as PCIe ports. Each PCIe port provides a point-to-point connection to another PCIe device. An 8-port PCIe switch, for example, provides connectivity to seven PCIe devices.

PCIe has a lot to offer

There are many advantages for PCIe over PCI; the primary being the increased bandwidth. The PCI Express Base Specification rev1.0a/1.1 has defined the physical interface speed to 2.5GT/s per differential pair. That is a single differential TX pair can transmit up to 250MB/s and up to 1GB/s when aggregating four (referred to as a x4 link). Furthermore, as more PCIe devices/applications became more bandwidth intensive , a new revision of the PCIe specification was drafted and ratified. The PCI Express Base Specification rev2.0 made critical improvements over the rev1.0a/1.1 specification. One such improvement was the potential for increased speed of the PCIe physical layer from 2.5GT/s to 5.0 GT/s effectively doubling the bandwidth of a given port. This speed increase however, is an optional implementation for the rev 2.0 specification. That is, a PCIe device compliant to the rev 2.0 specification is not required to support the higher speeds of 5.0 GT/s.

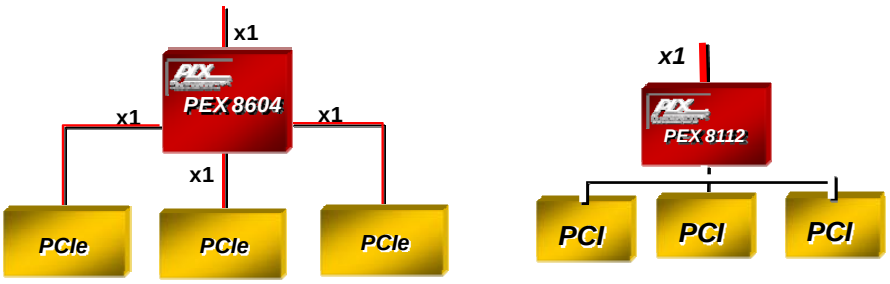

Figure 1. Point-to-Point PCIe connection versus PCI Bus

The function of a bridge

By definition, the term bridge in the context of interconnect makes reference to a device which has the capability to translate between two different protocols. For example, a PCI-to-PCIe bridge converts transactions which originate on the PCI bus to conform to the PCIe protocol on the other side.

Bandwidth bridge

A bandwidth bridge does not translate between two protocols. Instead, the term bandwidth bridge refers to a device which is able to match the speeds and bandwidth requirements between two devices of the same protocol with different speed implementations at the physical layer, such as is the case with PCIe. At the physical layer, PCIe rev 2.0 can support two different speed configurations; 2.5GT/s (required) and 5.0GT/s (optional).

PCIe Gen1 vs PCIe Gen 2

Those familiar with PCIe have certainly heard the terms "Gen1" and "Gen 2". It is common to refer to a device which is based on the PCIe Spec rev1.1 with 2.5GT/s SerDes as a Gen 1 device. It is also not uncommon to refer to a PCIe device with Gen 2 SerDes as a Gen 2 device. Similarly, it is not uncommon to assume that a PCIe device which is compliant to the PCI Express Base Specification rev2.0 supports 5.0 GT/s SerDes. However, this is not always the case. It is not mandatory for a PCIe device compliant to the rev 2.0 specification to support 5.0 GT/s SerDes. As a matter of fact, the rev2.0 specification mandates that all compliant devices support 2.5GT/s but 5.0GT/s support on the PCIe lanes is left as optional.
In fact, there are devices out in the market today which are compliant to the rev 2.0 but operate at a maximum of 2.5GT/s. Moreover, such devices are in some cases an important part of the system difficult to replace due to other functionality integral to the system. The lower speeds on its PCIe interface can create performance limitations with other PCIe devices. For example, consider a USB 3.0 bridge with a single PCIe lane running at 5.0 GT/s. When this USB device is connected to another PCIe device, the physical interface will be limited to the lower capable device. In our case, the PCIe interface on the USB device will be downgraded to 2.5GT/s. As a result, the bandwidth capabilities of the USB device are limited to half its capability.

A PCIe switch as a Bandwidth Bridge

In the example above, it was determined that the PCIe device connecting to the USB device is integral and cannot be replaced. However, sacrificing the performance is not a valid option either. In this case, a PCIe switch can be used as a bandwidth bridge. Consider the PEX 8604- a 4-lane; 2-port PCIe switch with 5.0 GT/s SerDes. Each port implements two PCIe lanes. The PCIe switch can be used to match the bandwidth between both devices by connecting two lanes from one switch port to two 2.5GT/s lanes from the one device and a single lane on the second interface to the USB device. The bandwidth for the single 5.0GT/s lane is matched by the aggregate bandwidth of the dual 2.5GT/s lanes.

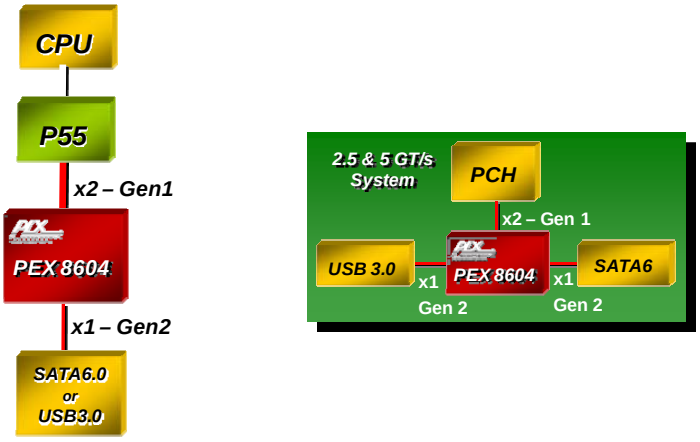

Figure 2. PEX 8604 used in a Bandwidth Bridge application

Conclusion

PCIe switches are typically used in fan-out applications where IO expansion is desired. However, flexibility in the configuration of PCIe switches available from PLX Technology allow system vendors to overcome bandwidth limitations introduced by other components in the system. When the PCIe switch is used as a bandwidth bridge, system designers can take advantage of the full performance capabilities of all the PCIe devices.