Application Report

How to Configure DP838xx for Ethernet Compliance Testing

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ABSTRACT

This application report covers how to setup and configure the DP838xx PHY (using the customer EVM) for Ethernet Physical Layer Compliance (IEEE 802.3) testing as the device under test (DUT). This application note primarily uses DP83867 as an example, but any DP838xx can use these procedures for compliance testing.

Refer to *DP83822 IEEE 802.3u Compliance and Debug* (SNLA266) for a DP83822 specific Ethernet compliance procedure.

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Trademarks

1 Standards and System Requirements

1.1 Standards

The following standards serve as references for the tests described in this document.

- Subclause 14.3.1 of IEEE standard 802.3-2002
- Subclause 40.6 IEEE standard 802.3-2002
- ANSI X3.263-1995

1.2 Test Equipment Suppliers

The different test equipment used to perform the various procedures described in this document can be procured from the following suppliers. Obtaining some of this equipment may require going through an agent.

- Tektronix
- Spirent
- Agilent (Keysight)
- Rohde and Schwarz
- Teledyne LeCroy

1.3 Test System Requirements

For testing an Ethernet PHY for both MII and MDI transmission, the following hardware and software are required:

- Oscilloscope with Ethernet physical layer compliance software (for example, Tektronix TDSET3)
- Ethernet compliance test fixture
- Link partner or packet generator (for example, Spirent SmartBits/Test Center)*
- TI USB-2-MDIO tool with PC (for alternative MDIO access)*
- DC power supply
- Necessary cables and probes
- Thermal stream or oven*
- * [*Not required for all tests or test setups.*]

1.4 Software Setup and Installation

Consult the test equipment OEM's Ethernet compliance software manual for help with compliance software installation.

For alternative MDIO access through MSP430 Launchpad, see the USB-2-MDIO User's Guide. Link to USB-2-MDIO tool page: http://www.ti.com/tool/USB-2-MDIO

2 Ethernet Physical Layer Compliance Testing

2.1 Standard Test Setup and Procedures

For Ethernet physical layer compliance testing, the PHY is managed through the serial management interface (SMI – also know as MDIO interface) to determine the test mode. The testing results are determined and recorded by the oscilloscope's Ethernet compliance software (for example, Tektronix's TDSET3).

The variation between Ethernet physical layer compliance tests is primarily the test mode of the PHY (configured by setting the internal PHY registers through SMI) and the connection on the test fixture (see Appendix A).

1. Connect the EVM to the 5-V DC jack (2.1-mm barrel plug) DC supply. For other external power supply options, see the *DP83867EVM User's Guide* (SNLU176) or *DP83867ERGZ EVM User's Guide* (SNLU190).
2. Connect the EVM to the test fixture according to setup outlined in the test fixture or software manual (see Figure 2-1). Identify if a link partner (packet generator) is needed for the test, and connect accordingly.
3. Set the thermal stream or oven to desired temperature (if applicable).
4. Configure the PHY's MDIO registers for the specific test. The SMI (MDIO interface) can be managed with TI's USB-2-MDIO tool through an MSP430 Launchpad (see the USB-2-MDIO tool for more info). The register configuration is outlined in Appendix B.
5. Start and configure the oscilloscope's Ethernet testing software (see the software user's manual).
6. Run the test and store the results (using the Ethernet compliance testing software).
7. Determine if the test has passed or failed according to IEEE standards.
8. Change test parameters or test channel and repeat.

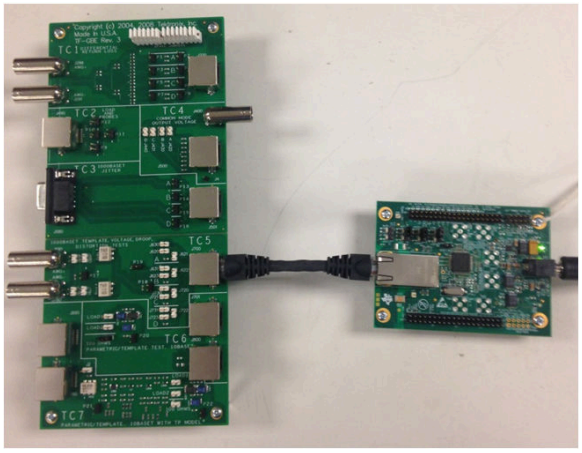

Figure 2-1. DP83867 EVM Connected to Testing Fixture Through CAT5 Cable

2.2 1000 BASE-T

Refer to Appendix B for 1000 BASE-T register writes.

Refer to Appendix C for Test Mode waveform oscilloscope captures.

2.2.1 Template (Test Mode 1)

Purpose: To ensure that the PHY transmit waveforms fit into the IEEE-defined templates.

Pass Condition: Voltage output waveforms fit into IEEE-defined templates with PHY in Test Mode 1 after normalization.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 1 by setting MDIO registers according to *1000 Base Test Mode 1* in Appendix B. Note that some Ethernet compliance software can run Template and Peak Voltage Tests simultaneously.

2.2.2 Peak Voltage (Test Mode 1)

Purpose: To ensure correct PHY transmitter output voltage levels.

Pass Condition: Voltage Levels are to be within:

|Peak Voltage B| – |Peak Voltage A| < 1%

|Peak Voltage C| < 2% of 0.5 × (|Peak Voltage B| + |Peak Voltage A|) / 2

|Peak Voltage D| < 2% of 0.5 × (|Peak Voltage B| + |Peak Voltage A|) / 2

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 1 by setting MDIO registers according to *1000 Base Test Mode 1* in Appendix B. Note that some Ethernet compliance software can run Template and Peak Voltage Tests simultaneously.

2.2.3 Droop (Test Mode 1)

Purpose: To ensure that the transmitter output voltage does not decay faster than specified in IEEE 802.3.

Pass Condition: The magnitude of the voltage at 500 ns after point F and H should greater than 73.1% of the magnitude of points F and H, respectively.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 1 by setting MDIO registers according to *1000 Base Test Mode 1* in Appendix B.

2.2.4 Jitter Master Unfiltered (Test Mode 2)

Purpose: To ensure that the PHY TX_TCLK Jitter with respect to an unjittered reference is within the specified bounds.

Pass Condition: The peak-to-peak value of the jittered waveform with respect to the unjittered reference should be less than 1.4 ns.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 2 by setting MDIO registers according to *1000 Base Test Mode 2* in Appendix B.

Note

For DP83867 TX_TCLK access, connect to pins 29 and 30 (TX_TCLK and GND) on the EVM as seen Figure 2-2, and use *1000 Base Test Mode 2 with TX_TCLK* in Appendix B (see Figure C-7 for TX_TCLK waveform).

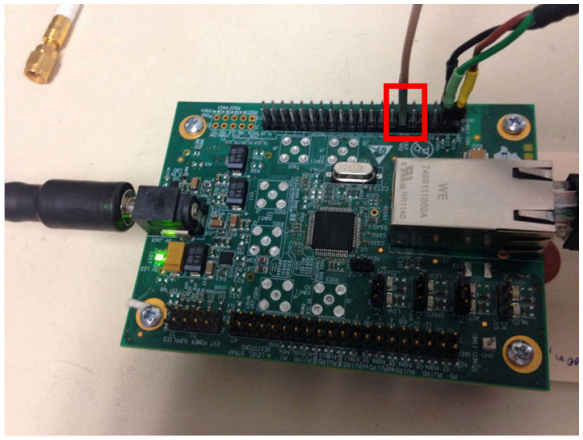

Figure 2-2. DP83867 EVM With CLK_OUT Pins Marked for TX_TCLK Access

2.2.5 Jitter Slave Unfiltered (Test Mode 2 and 3)

Purpose: To ensure that the PHY TX_TCLK Jitter with respect to an unjittered reference is within the specified bounds.

Pass Condition: The peak-to-peak value of the jittered waveform with respect to the unjittered reference should be less than 1.4 ns.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 2 and then Test Mode 3 by setting MDIO registers according to *1000 Base Test Mode 2* and then *1000 Base Test Mode 3* in Appendix B.

Note

For DP83867 TX_TCLK access, connect to pins 29 and 30 (TX_TCLK and GND) on the EVM as seen Figure 2-2, and use *1000 Base Test Mode 3 with TX_TCLK* in Appendix B (see Figure C-7 for TX_TCLK waveform).

2.2.6 Distortion (Test Mode 4)

Purpose: To ensure that the peak distortion is within the specified bounds.

Pass Condition: The peak distortion of the output differential signal should be less than 10 mV when sampled with TX_TCLK for at least 60% of the Unit Interval (UI) for 2047 consecutive samples at an arbitrary phase.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 4 by setting MDIO registers according to *1000 Base Test Mode 4* in Appendix B.

A disturbing signal of 2.7 Vpp at 20.8 MHz is required to pass Distortion test (please see Ethernet Compliance Software's Manual for setup).

Also, verify that the Ethernet Compliance software is adhering to the "at least 60% of Unit Interval (UI) for 10 mV", not 100% (for example, TDSET uses 100% of UI, so failures are seen even with compliant parts).

2.2.7 Common-Mode Voltage (Test Mode 4)

Purpose: To ensure that the Common-Mode Voltage is within the specified bounds.

Pass Condition: The magnitude of the Common-Mode Voltage should be within 50 mVpp.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 4 by setting MDIO registers according to *1000 Base Test Mode 4* in Appendix B.

Connect the DUT ground to test fixture ground for proper measurements (as outlined in IEEE 802.3 in Figure 2-3).

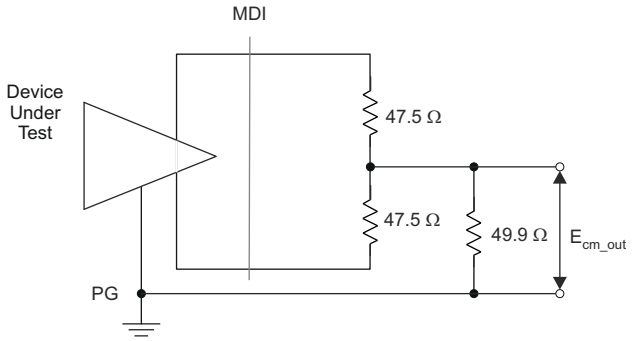

Figure 2-3. IEEE-Defined CM Voltage Test Setup

2.2.8 Return Loss (Test Mode 4)

Purpose: To ensure that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated:

≥16 dB over the frequency range of 1.0 MHz to 40 MHz

≥10 – 20log 10 (f /80) dB over the frequency range 40 MHz to 100 MHz (f in MHz)

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 4 by setting MDIO registers according to *1000 Base Test Mode 4* in Appendix B.

Note

A spectrum analyzer may be needed depending on Ethernet Compliance Software.

2.2.9 Common-Mode Noise Rejection

Purpose: Verify that the PHY's common-mode rejection ratio is within the specified bounds.

Pass Condition: See IEEE 802.3 40.6.1.3.3

Specific Test Setup: Special Testing setup is required for high voltage injection. Refer to the high voltage injection testing procedures (not included in this application note).

2.3 100 BASE-TX

Refer to Appendix B for 100 BASE-TX register writes. Use both MDI and MDIX configurations for all tests.

2.3.1 Template (Active Output Interface)

Purpose: To ensure that the output fits the transmit template.

Pass Condition: Fit into the specified ANSI Active Output Interface template.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B.

2.3.2 Differential Output Voltage

Purpose: To ensure the differential output voltage is within the specified bounds.

Pass Condition: The differential output voltage should be within a positive or negative 950–1050 mV.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B.

2.3.3 Signal Amplitude Symmetry

Purpose: To ensure the Signal Amplitude Symmetry is within the specified bounds.

Pass Condition: The ratio of the positive peak to negative peak amplitudes should be within 2% or 0.98 ≤ $|+V_{OUT}| / |–V_{OUT}| \leq 1.02$

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B.

2.3.4 Rise and Fall Time

Purpose: To ensure that the device rise and fall time are within the specified bounds.

Pass Condition: The rise and fall time (between 10% and 90% voltage levels for both positive and negative) should be between 3 ns and 5 ns. The maximum and minimum rise and fall times should be within 0.5 ns.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B.

2.3.5 Waveform Overshoot

Purpose: To ensure that the waveform overshoot is below the specified bound.

Pass Condition: The overshoot (both positive and negative maximum voltage level on transition) should not exceed 5% over the steady state voltage level (V_{OUT}).

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B.

2.3.6 Jitter

Purpose: To ensure that the transmit output jitter is within the specified bounds.

Pass Condition: The transmit output jitter should be less than 1.4 ns.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B.

2.3.7 Duty Cycle Distortion

Purpose: To ensure that the duty cycle distortion is below the specified bound.

Pass Condition: The duty cycle distortion (defined as above and below 50% of Vout) should not exceed ±0.25 ns.

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B.

2.3.8 Return Loss

Purpose: To ensure that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated:

≥16 dB over the frequency range of 2 MHz to 30 MHz

≥10 – 20log 10 (f /30) dB over the frequency range 30 MHz to 60 MHz (f in MHz)

≥10 dB over the frequency range 60 MHz to 80 MHz

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B. Note: A spectrum analyzer may be needed depending on Ethernet Compliance Software.

2.3.9 Common-Mode Rejection

Purpose: Verify that the PHY's common mode rejection ratio is within the specified bounds.

Pass Condition: See ANSI X3-263-1995 9.2.3

Specific Test Setup: Verify the correct test fixture connections. Configure PHY to output Test Mode 5 by setting MDIO registers according to *100 Base Standard MDI* and *100 Base Standard MDIX* in Appendix B.

Note

Some Ethernet compliance software does not include Common-Mode Rejection testing.

2.4 10 BASE-T/10 BASE-Te

Refer to Appendix B for 10 BASE-T/10 BASE-Te register writes.

The DP83867 supports only 10 BASE-Te mode of operation. Verify the DUT supports the standard, and is operating in the proper mode, when performing compliance testing.

2.4.1 Link Pulse

Purpose: To ensure that the link pulse waveform is within the specified bounds.

Pass Condition: The link pulse must fit into the IEEE-defined template.

Specific Test Setup: Verify the test fixture connections. Set MDIO registers according to *10 Base Link Pulse* in Appendix B.

2.4.2 TP_IDL

Purpose: To ensure that the transmitter functions properly after transitioning to an idle state.

Pass Condition: The transmitter TP_IDL pulse must fit within the template for Load 1, 2, and 3 with and without the twisted pair model (TPM).

Specific Test Setup: Verify the test fixture connections including the packet generator as a link partner (generating random packets). Configure the PHY to be in reverse loopback mode by setting MDIO registers according to *10 Base Standard* in Appendix B.

2.4.3 MAU, Internal

Purpose: To ensure that the transmitter output equalization is within the specified bounds.

Pass Condition: The transmitter waveform should fit within the IEEE-defined template for all data sequences when terminated with a 100-Ω resistor.

Specific Test Setup: Verify the test fixture connections including the packet generator as a link partner (generating random packets). Configure the PHY to be in reverse loopback mode by setting MDIO registers according to *10 Base Standard* in Appendix B. See Figure 2-4 for DP83867 10 BASE-Te test bench configuration.

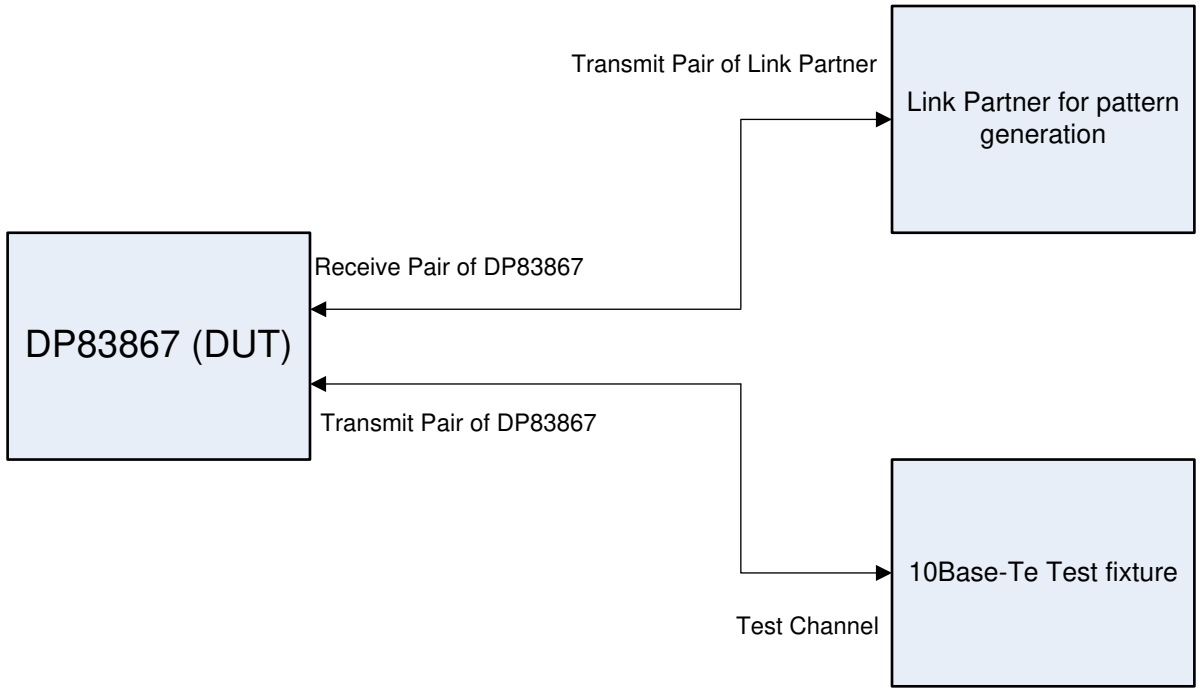

Figure 2-4. DP83867 10 BASE-Te Configuration

2.4.4 Jitter With TPM

Purpose: To ensure that the jitter is within the specified bounds.

Pass Condition: The transmitter output jitter should be less than ±5.5 ns. Note: Failure with TPM does not necessarily mean noncompliance.

Specific Test Setup: Verify the test fixture connections including the packet generator as a link partner (generating random packets). Configure the PHY to be in reverse loopback mode by setting MDIO registers according to *10 Base Standard* in Appendix B. See Figure 2-4 for DP83867 10 BASE-Te test bench configuration.

2.4.5 Jitter Without TPM

Purpose: To ensure that the jitter is within the specified bounds.

Pass Condition: The transmitter output jitter should be less than ±8.0 ns.

Specific Test Setup: Verify the test fixture connections including the packet generator as a link partner (generating random packets). Configure the PHY to be in reverse loopback mode by setting MDIO registers according to *10 Base Standard* in Appendix B. See Figure 2-4 for DP83867 10 BASE-Te test bench configuration.

2.4.6 Differential Voltage

Purpose: To ensure that the differential voltage is within the specified bounds.

Pass Condition: The peak differential voltage should be between 2.2 V and 2.8 V when terminated with 100-Ω resistor for 10BASE-T. The peak differential voltage should be between 1.54 V and 1.96 V when terminated with 100-Ω resistor for 10BASE-Te.

Specific Test Setup: Verify the test fixture connections including the packet generator as a link partner (generating random packets). Configure the PHY to be in reverse loopback mode by setting MDIO registers according to *10 Base Standard* in Appendix B. See Figure 2-4 for DP83867 10 BASE-Te test bench configuration.

2.4.7 Harmonic Content

Purpose: To ensure the harmonic content of the PHY is within the specified bounds.

Pass Condition: The Data Out circuit must drive all ones. All subsequent harmonics must be 27-dB below the fundamental.

Specific Test Setup: Verify the test fixture connections including the packet generator as a link partner (generating random packets). Configure the PHY to be in reverse loopback mode by setting MDIO registers according to *10 Base Standard* in Appendix B. See Figure 2-4 for DP83867 10 BASE-Te test bench configuration.

2.4.8 Common-Mode Voltage

Purpose: To ensure the common-mode voltage is within the specified bounds.

Pass Condition: The magnitude of the common-mode voltage should be less than 50-mV peak.

Specific Test Setup: Verify the test fixture connections including the packet generator as a link partner (generating random packets). Configure the PHY to be in reverse loopback mode by setting MDIO registers according to *10 Base Standard* in Appendix B. See Figure 2-4 for DP83867 10 BASE-Te test bench configuration.

2.4.9 Return Loss

Purpose: To ensure that the return loss is above the specified attenuation.

Pass Condition: The reflection of any incident signal to the PHY must be attenuated:

≥ 15 dB over the frequency range of 5.0 MHz to 10 MHz

Specific Test Setup: Two waveform inputs may be necessary depending on testing setup. Verify the test fixture connections including the packet generator as a link partner (generating random packets). Configure the PHY to be in reverse loopback mode by setting MDIO registers according to *10 Base Standard* in Appendix B. See Figure 2-4 for DP83867 10 BASE-Te test bench configuration.

2.4.10 Common-Mode Rejection

Purpose: Verify that the PHY's common-mode rejection ratio is within the specified bounds.

Pass Condition: See IEEE 802.3 14.3.1.2.6

Specific Test Setup: Refer to the high voltage injection testing procedures (not included in this app note). Set MDIO registers according to *10 Base Standard* in Appendix B.

3 References

TDSET3 Manual
http://www.tek.com/manual/tdset3-ethernet-test-compliance-software-printed-help-document

IEEE 802.3

ANSI X3.263-1995

DP83867E/IS/CS Robust, High Immunity, Small Form Factor 10/100/1000 Ethernet Phy (SNLS504)

DP83867IR/CR High Immunity 10/100/1000 Ethernet Physical Layer Transceiver (SNLS484)

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2017) to Revision B (May 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

Changes from Revision * (November 2015) to Revision A (January 2017)	Page
• Added data sheet links to *References*	10
• Updated registers in Appendix B	13

A Outline of Ethernet Compliance Tests for DP83867

Table A-1 lists the Ethernet compliance tests for DP83867.

Table A-1. Outline of Ethernet Compliance Tests for DP83867

TEST	TEST MODE	REGISTER CONFIGURATION (IN Appendix B)
1000 BASE-T		
Template	Test Mode 1	1000 Base Test Mode 1
Peak Voltage	Test Mode 1	1000 Base Test Mode 1
Droop	Test Mode 1	1000 Base Test Mode 1
Jitter Master Unfiltered	Test Mode 2	1000 Base Test Mode 2
Jitter Slave Unfiltered	Test Mode 2 and 3	1000 Base Test Mode 2/3
Distortion	Test Mode 4	1000 Base Test Mode 4
Common Mode Voltage	Test Mode 4	1000 Base Test Mode 4
Return Loss	Test Mode 4	1000 Base Test Mode 4
Common Mode Rejection	(Test Mode 4)	1000 Base Test Mode 4
100 BASE-TX		
Template	Test Mode 5	100 Base Standard MDI/MDIX
Differential Output Voltage	Test Mode 5	100 Base Standard MDI/MDIX
Signal Amplitude Symmetry	Test Mode 5	100 Base Standard MDI/MDIX
Rise and Fall Time	Test Mode 5	100 Base Standard MDI/MDIX
Waveform Overshoot	Test Mode 5	100 Base Standard MDI/MDIX
Jitter	Test Mode 5	100 Base Standard MDI/MDIX
Duty Cycle Distortion	Test Mode 5	100 Base Standard MDI/MDIX
Return Loss	Test Mode 5	100 Base Standard MDI/MDIX
Common Mode Rejection	Test Mode 5	100 Base Standard MDI/MDIX
10 BASE-T		
Link Pulse	*See register writes*	10 Base Link Pulse
TP_IDL	*See register writes*	10 Base Standard
MAU, Internal	*See register writes*	10 Base Standard
Jitter with TPM	*See register writes*	10 Base Standard
Jitter without TPM	*See register writes*	10 Base Standard
Differential Voltage	*See register writes*	10 Base Standard
Harmonic Content	*See register writes*	10 Base Standard
Common Mode Voltage	*See register writes*	10 Base Standard
Return Loss	*See register writes*	10 Base Standard
Common Mode Rejection	*See register writes*	10 Base Standard

B Ethernet Compliance Testing MDIO Register Writes for DP83867

1000 Base Test Mode 1:	
Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x0140	//1000 Base-T Mode
Reg 0x0010 = 0x5008	//forced MDI Mode
Reg 0x0009 = 0x3B00	//Test Mode 1
Reg 0x0025 = 0x0480	//output test mode to all channels
Reg 0x01D5 = 0xF508	

1000 Base Test Mode 2:	
Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x0140	//1000 Base-T Mode
Reg 0x0010 = 0x5008	//forced MDI Mode
Reg 0x0009 = 0x5B00	//Test Mode 2
Reg 0x0025 = 0x0480	//output test mode to all channels

1000 Base Test Mode 2 with TX_TCLK:	
Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x0140	//1000 Base-T Mode
Reg 0x0010 = 0x5008	//forced MDI Mode
Reg 0x0009 = 0x5B00	//Test Mode 2
Reg 0x0025 = 0x0480	//output test mode to all channels
Reg 0x0170 = 0x81F	//output clk a
Reg 0x00C6 = 0x0010	//proprietary

1000 Base Test Mode 3:	
Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x0140	//1000 Base-T Mode
Reg 0x0010 = 0x5008	//forced MDI Mode
Reg 0x0009 = 0x7B00	//Test Mode 3
Reg 0x0025 = 0x0480	//output test mode to all channels

1000 Base Test Mode 3 with TX_TCLK:	
Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x0140	//1000 Base-T Mode
Reg 0x0010 = 0x5008	//forced MDI Mode
Reg 0x0009 = 0x7B00	//Test Mode 3
Reg 0x0025 = 0x0480	//output test mode to all channels
Reg 0x0170 = 0x81F	//output clk
Reg 0x00C6 = 0x0010	//proprietary

1000 Base Test Mode 4:	
Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x0140	//1000 Base-T Mode
Reg 0x0010 = 0x5008	//forced MDI Mode
Reg 0x0009 = 0x9B00	//Test Mode 4

Reg 0x0025 = 0x0400	//0400: Channel A //0420: Channel B //0440: Channel C //0460: Channel D

100 Base Standard MDI (Test Mode 5):

Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x2100	//programs DUT to 100Base-TX Mode
Reg 0x0010 = 0x5008	//programs DUT to Forced MDI Mode
Reg 0x0009 = 0xBB00	//Test Mode 5
Reg 0x0025 = 0x0480	//output test mode to all channels

100 Base Standard MDIX (Test Mode 5):

Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x2100	//programs DUT to 100Base-TX Mode
Reg 0x0010 = 0x5028	//programs DUT to Forced MDIX Mode
Reg 0x0009 = 0xBB00	//Test Mode 5
Reg 0x0025 = 0x0480	//output test mode to all channels

10 Base Link Pulse:

Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x0100	//programs DUT to 10Base-T/Te Mode
Reg 0x0010 = 0x5008	//programs DUT to Forced MDI Mode

10 Base Standard:

Reg 0x001F = 0x8000	//reset PHY
Reg 0x0000 = 0x0100	//programs DUT to 10Base-T/Te Mode
Reg 0x0010 = 0x5008	//programs DUT to Forced MDI Mode
Reg 0x0016 = 0x0020	//programs DUT to Phy Loop-Back

C PHY Test Mode Waveforms

This appendix illustrates the PHY test mode waveforms.

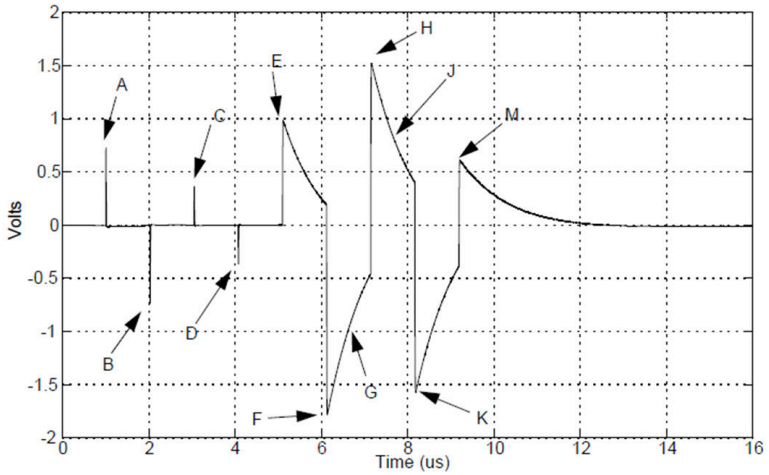

Figure C-1. IEEE Test Mode 1 per Standard

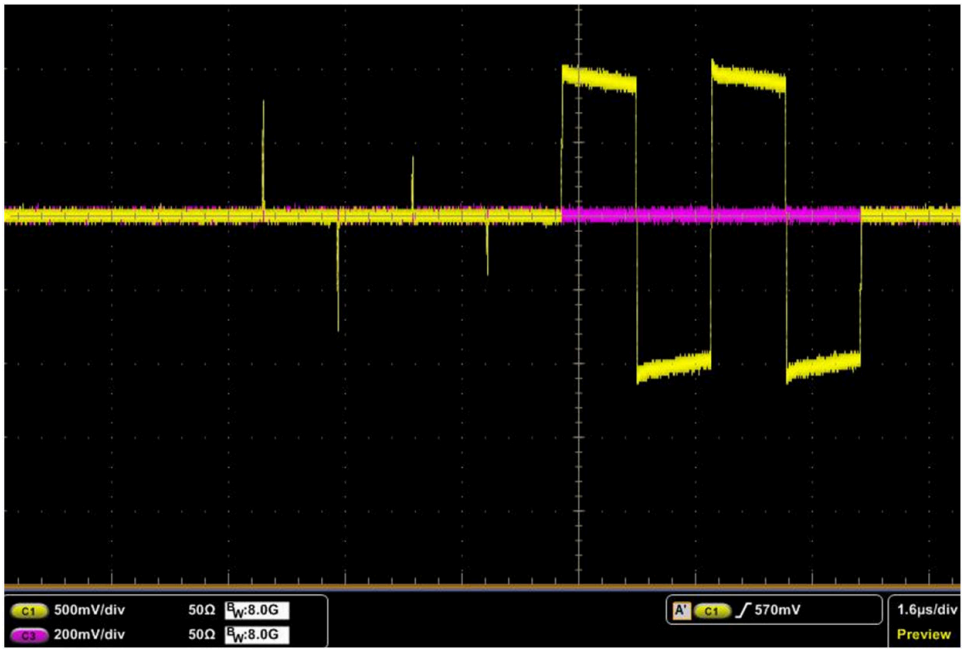

Figure C-2. DP83867 Test Mode 1 Output Waveform

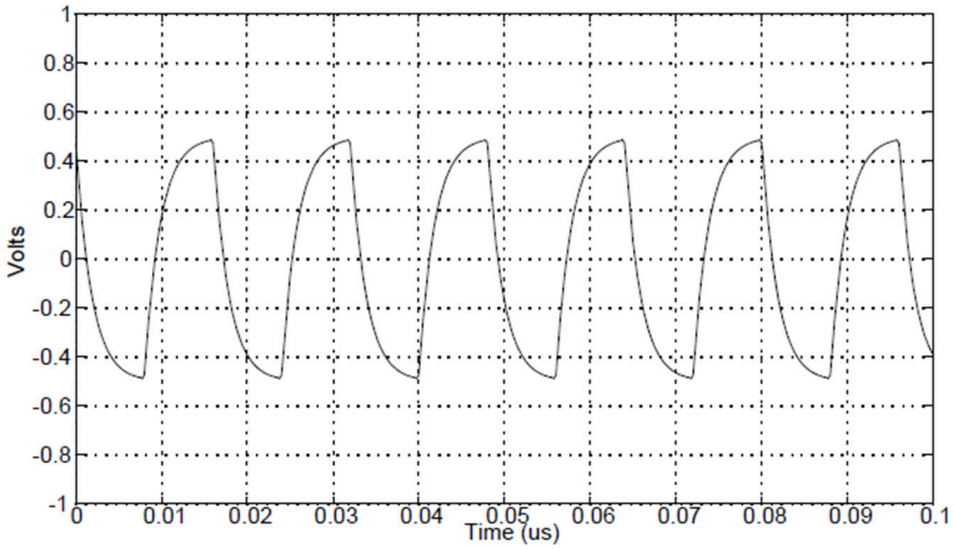

Figure C-3. IEEE Test Mode 2 and 3 per Standard

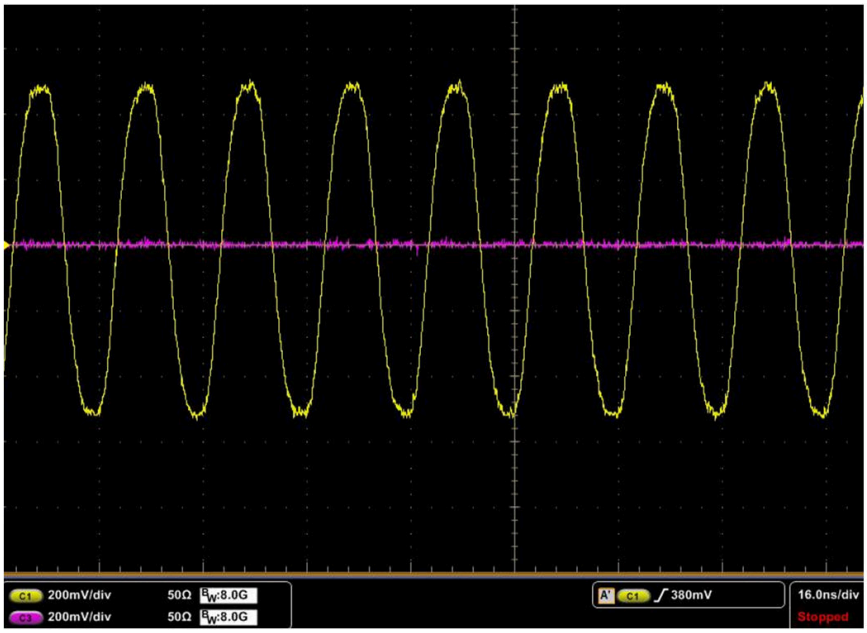

Figure C-4. DP83867 Test Mode 2 and 3 Output Waveform

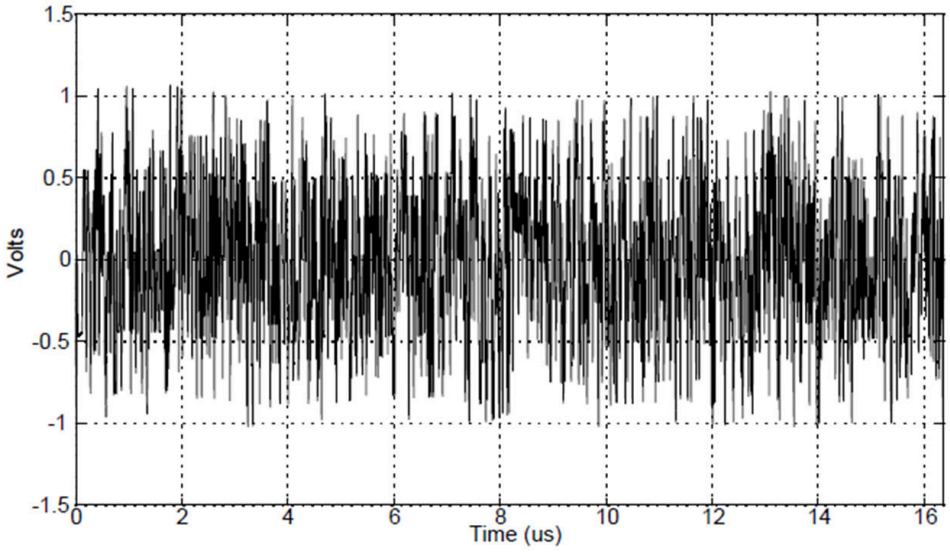

Figure C-5. IEEE Test Mode 4 per Standard

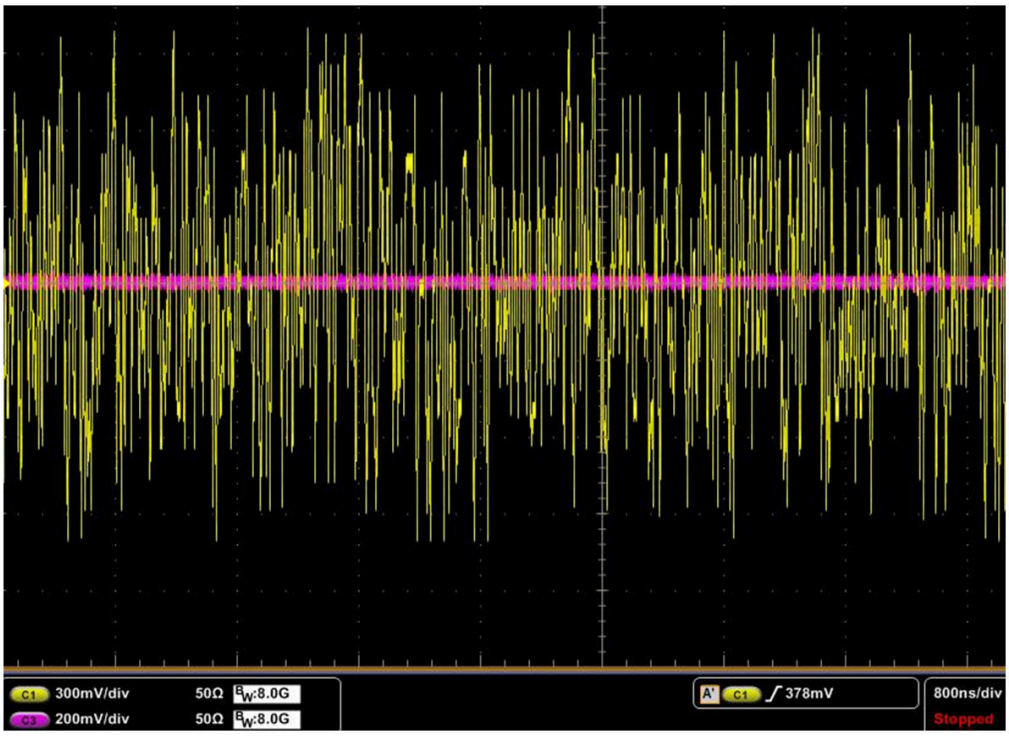

Figure C-6. DP83867 Test Mode 4 Output Waveform

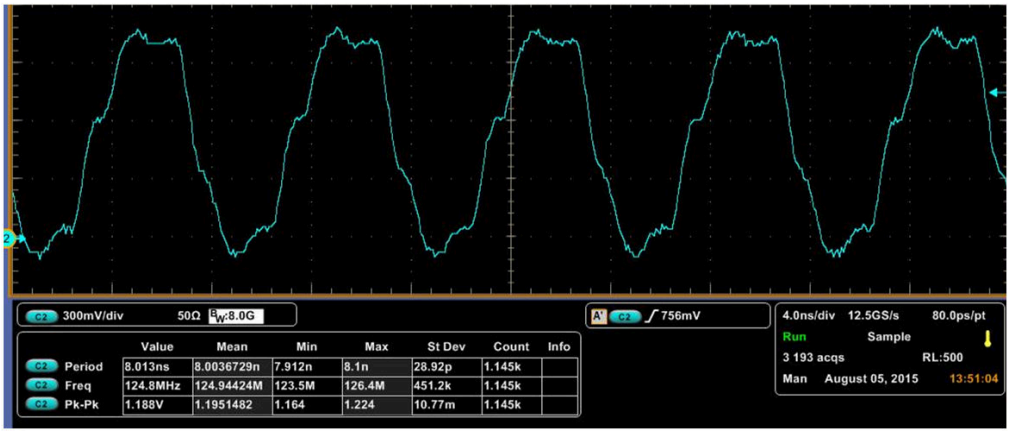

Figure C-7. DP83867 TX_TCLK Output Waveform (EVM Pin 29 to GND)

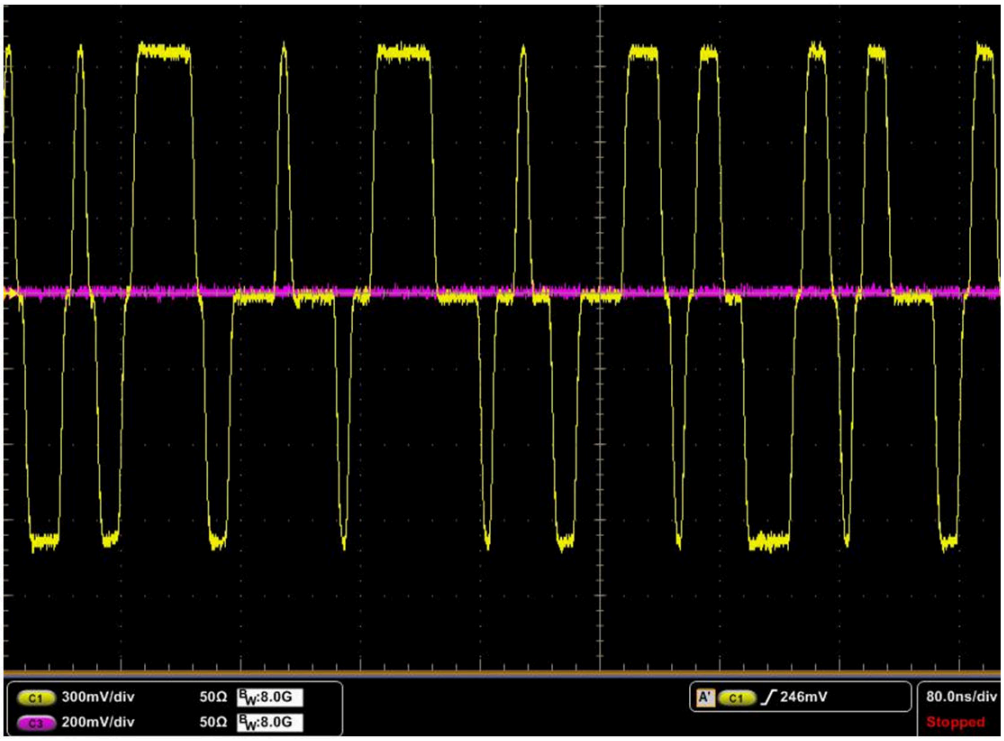

Figure C-8. DP83867 Scrambled Idles Output Waveform 100M (Test Mode 5)

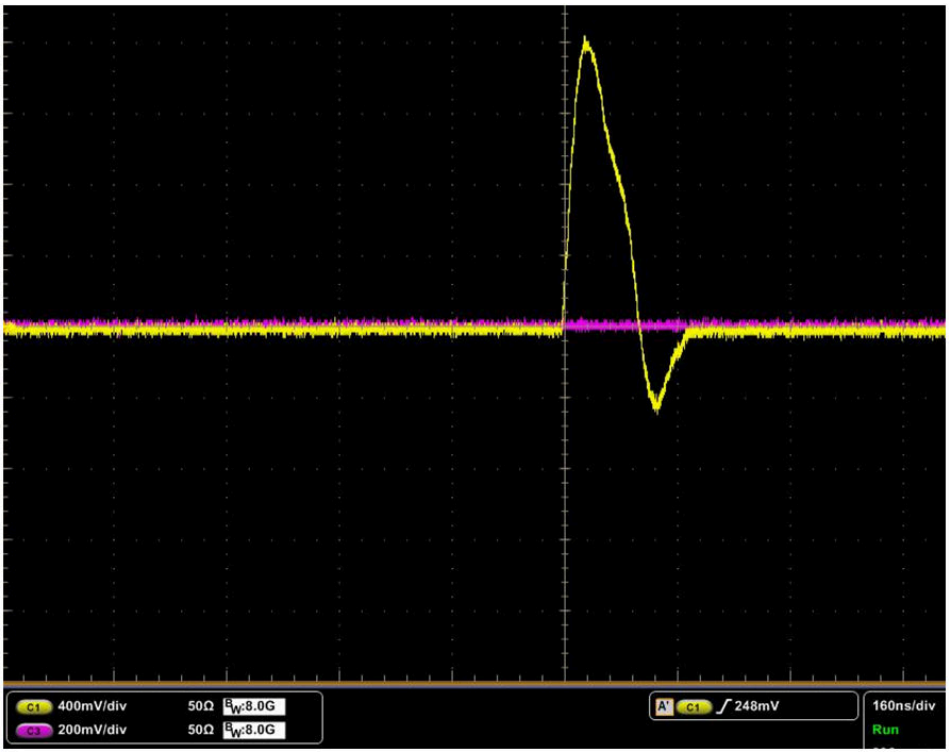

Figure C-9. DP83867 Link Pulse Output Waveform 10M

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