(intel) FPGA														Hard Processor Sy	ystem Pin Informa	ion for Intel® Arria® 10 De Versio
HPS Function	HPS Pin Mux Select 15	HPS Pin Mux Select 14	HPS Pin Mux Select 13	HPS Pin Mux Select 12	HPS Pin Mux Select 11	HPS Pin Mux Select 10	HPS Pin Mux Select 9	HPS Pin Mux Select 8	HPS Pin Mux Select 7	HPS Pin Mux Select 6	HPS Pin Mux Select 5	HPS Pin Mux Select 4	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
HPS_DIRECT_SHARED_Q4_12	GPIO1_IO23	NAND_ADQ15		Trace_D3				EMAC2_RXD3					SPIMO_SSO_N	SPIS1_MISO	EMACO_MDC	I2C_EMACO_SCL
HPS_DIRECT_SHARED_Q4_11 HPS_DIRECT_SHARED_Q4_10	GPIO1_IO22 GPIO1_IO21	NAND_ADQ14 NAND_ADQ13		Trace_D2 Trace D1				EMAC2_RXD2 EMAC2_TXD3				SDMMC DATA7	SPIM0_MISO SPIM0_MOSI	SPIS1_SS0_N SPIS1_MOSI	EMAC0_MDIO	I2C_EMAC0_SDA I2C_EMAC2_SCL
HPS_DIRECT_SHARED_Q4_10 HPS_DIRECT_SHARED_Q4_9	GPIO1_IO21 GPIO1_IO20	NAND_ADQ13 NAND_ADQ12	+	Trace_D1		+		EMAC2_TXD3 EMAC2_TXD2		+	+	SDMMC_DATA7	SPIMO_MOSI SPIMO CLK	SPIS1_MOSI SPIS1_CLK		I2C_EMAC2_SCL I2C_EMAC2_SDA
HPS_DIRECT_SHARED_Q4_8	GPIO1_IO20	NAND_ADQ11		Trace_CLK		+		EMAC2_RXD1				SDMMC DATA5	SPIMO SSO N	OI IOI_OLIX	EMAC1 MDC	I2C_EMAC1_SCL
HPS_DIRECT_SHARED_Q4_7	GPIO1_IO18	NAND_ADQ10						EMAC2_RXD0				SDMMC_DATA4	SPIM0_MISO		EMAC1_MDIO	I2C_EMAC1_SDA
HPS_DIRECT_SHARED_Q4_6	GPIO1_IO17	NAND_ADQ9	UART1_RTS_N	QSPI_SS3				EMAC2_TXD1				SDMMC_DATA3	SPIM0_SS1_N			
HPS_DIRECT_SHARED_Q4_5	GPIO1_IO16	NAND_ADQ8	UART1_CTS_N UART1_RX	QSPI_SS2				EMAC2_TXD0				SDMMC_DATA2 SDMMC_DATA1				
HPS_DIRECT_SHARED_Q4_4 HPS_DIRECT_SHARED_Q4_3	GPIO1_IO15 GPIO1_IO14	NAND_CE_N	UART1_KX UART1_TX	Trace_CLK		+		EMAC2_RX_CTL EMAC2_RX_CLK				SDMMC_DATA1				
HPS_DIRECT_SHARED_Q4_2	GPIO1_IO13	NAND_RB	OARTI_TX			+		EMAC2_TX_CTL				SDMMC_CMD				I2C1_SCL
HPS_DIRECT_SHARED_Q4_1	GPIO1_IO12	NAND_ALE						EMAC2_TX_CLK				SDMMC_DATA0				I2C1_SDA
HPS_DIRECT_SHARED_Q3_12	GPIO1_IO11	NAND_ADQ7						EMAC1_RXD3						SPIS0_MISO	EMAC0_MDC	I2C_EMACO_SCL
HPS_DIRECT_SHARED_Q3_11	GPIO1_IO10	NAND_ADQ6						EMAC1_RXD2						SPIS0_SS0_N	EMAC0_MDIO	I2C_EMAC0_SDA
HPS_DIRECT_SHARED_Q3_10 HPS_DIRECT_SHARED_Q3_9	GPIO1_IO9 GPIO1_IO8	NAND_ADQ5 NAND_ADQ4				+		EMAC1_TXD3			_			SPISO_MOSI	EMAC2_MDC EMAC2_MDIO	I2C_EMAC2_SCL I2C_EMAC2_SDA
HPS_DIRECT_SHARED_Q3_9 HPS_DIRECT_SHARED_Q3_8	GPI01_I08 GPI01_I07	NAND_ADQ4 NAND_CLE	UART1 RX					EMAC1_TXD2 EMAC1_RXD1						SPIS0_CLK SPIS1 MISO	EIVIAGZ_IVIDIO	I2C_EMAC2_SDA I2C1_SCL
HPS_DIRECT_SHARED_Q3_7	GPIO1_IO6	NAND_ADQ3	UART1_TX					EMAC1_RXD0	1		1	1		SPIS1_SS0_N		I2C1_SDA
HPS_DIRECT_SHARED_Q3_6	GPIO1_IO5	NAND_ADQ2	UART1_RTS_N					EMAC1_TXD1						SPIS1_MOSI		
HPS_DIRECT_SHARED_Q3_5	GPIO1_IO4	NAND_WP_N	UART1_CTS_N					EMAC1_TXD0					SPIM1_SS1_N	SPIS1_CLK		
HPS_DIRECT_SHARED_Q3_4	GPIO1_IO3	NAND_RE_N	UARTO_RX UARTO_TX					EMAC1_RX_CTL	-		1	+	SPIM1_SS0_N			I2C0_SCL
HPS_DIRECT_SHARED_Q3_3 HPS_DIRECT_SHARED_Q3_2	GPIO1_IO2 GPIO1_IO1	NAND_WE_N NAND_ADQ1	UARTO_TX UARTO_RTS_N	+	+	+		EMAC1_RX_CLK EMAC1_TX_CTL			+		SPIM1_MISO SPIM1_MOSI			I2C0_SDA
HPS_DIRECT_SHARED_Q3_1	GPI01_I01	NAND_ADQ0	UARTO_CTS_N			+		EMAC1_TX_CLK					SPIM1_MOSI			
HPS_DIRECT_SHARED_Q2_12	GPIO0_IO23	NAND_ADQ15	UART0_RX					USB1_DATA7				EMAC0_RXD3	SPIM1_SS0_N	SPIS0_MISO		I2C0_SCL
HPS_DIRECT_SHARED_Q2_11	GPIO0_IO22	NAND_ADQ14	UART0_TX					USB1_DATA6				EMAC0_RXD2	SPIM1_MISO	SPIS0_SS0_N		I2C0_SDA
HPS_DIRECT_SHARED_Q2_10	GPIO0_IO21	NAND_ADQ13	UARTO_RTS_N					USB1_DATA5				EMAC0_TXD3	SPIM1_MOSI	SPIS0_MOSI		I2C1_SCL
HPS_DIRECT_SHARED_Q2_9	GPIO0_IO20 GPIO0_IO19	NAND_ADQ12	UART0_CTS_N			+		USB1_DATA4				EMAC0_TXD2 EMAC0_RXD1	SPIM1_CLK	SPIS0_CLK		I2C1_SDA
HPS_DIRECT_SHARED_Q2_8 HPS_DIRECT_SHARED_Q2_7	GPI00_I019 GPI00_I018	NAND_ADQ11 NAND_ADQ10				+		USB1_DATA3 USB1_DATA2			+	EMACO_RXD1	SPIM1_SS1_N			
HPS DIRECT SHARED Q2 6	GPIO0_IO17	NAND_ADQ9						USB1_NXT				EMAC0_TXD1				
HPS_DIRECT_SHARED_Q2_5	GPIO0_IO16	NAND_ADQ8						USB1_DATA1				EMAC0_TXD0				
HPS_DIRECT_SHARED_Q2_4	GPI00_I015							USB1_DATA0				EMAC0_RX_CTL				
HPS_DIRECT_SHARED_Q2_3	GPIO0_IO14	NAND_CE_N						USB1_DIR				EMACO_RX_CLK				
HPS_DIRECT_SHARED_Q2_2 HPS_DIRECT_SHARED_Q2_1	GPIO0_IO13 GPIO0_IO12	NAND_RB NAND_ALE	+			+		USB1_STP USB1_CLK		+	+	EMAC0_TX_CTL EMAC0_TX_CLK				
HPS_DIRECT_SHARED_Q1_12	GPIO0_IO11	NAND_ADQ7				+		USB0 DATA7				LWAGO_TA_OLK	SPIM1_SS0_N	SPIS1_MISO	EMAC0_MDC	I2C_EMAC0_SCL
HPS_DIRECT_SHARED_Q1_11	GPIO0_IO10	NAND_ADQ6						USB0_DATA6					SPIM1_MISO	SPIS1_SS0_N	EMAC0_MDIO	I2C_EMAC0_SDA
HPS_DIRECT_SHARED_Q1_10	GPI00_I09	NAND_ADQ5						USB0_DATA5				SDMMC_DATA7	SPIM1_MOSI	SPIS1_MOSI	EMAC1_MDC	I2C_EMAC1_SCL
HPS_DIRECT_SHARED_Q1_9	GPIO0_IO8	NAND_ADQ4	LIADTA DV					USB0_DATA4				SDMMC_DATA6	SPIM1_CLK	SPIS1_CLK	EMAC1_MDIO	I2C_EMAC1_SDA
HPS_DIRECT_SHARED_Q1_8 HPS_DIRECT_SHARED_Q1_7	GPIO0_IO7 GPIO0_IO6	NAND_CLE NAND_ADQ3	UART1_RX UART1_TX			+		USB0_DATA3 USB0_DATA2				SDMMC_DATA5 SDMMC_DATA4	SPIM0_SS0_N SPIM0_MISO		EMAC2_MDC EMAC2_MDIO	I2C_EMAC2_SCL I2C_EMAC2_SDA
HPS_DIRECT_SHARED_Q1_6	GPI00_I05	NAND_ADQ3	UART1_TX UART1_RTS_N	QSPI_SS3		+		USB0_NXT				SDMMC_DATA3	SPIMO_MOSI		EIWAGZ_IWIDIO	I2C0_SCL
HPS_DIRECT_SHARED_Q1_5	GPIO0_IO4	NAND_WP_N	UART1_CTS_N	QSPI_SS2				USB0_DATA1				SDMMC_DATA2	SPIM0_CLK			I2C0_SDA
HPS_DIRECT_SHARED_Q1_4	GPIO0_IO3	NAND_RE_N	UART0_RX					USB0_DATA0				SDMMC_DATA1		SPIS0_MISO		I2C1_SCL
HPS_DIRECT_SHARED_Q1_3	GPIO0_IO2	NAND_WE_N	UARTO_TX			1		USB0_DIR				SDMMC_CCLK	00044 004 11	SPIS0_SS0_N		I2C1_SDA
HPS_DIRECT_SHARED_Q1_2 HPS_DIRECT_SHARED_Q1_1	GPIO0_IO1 GPIO0_IO0	NAND_ADQ1 NAND_ADQ0	UARTO_RTS_N UARTO_CTS_N		+	+		USB0_STP USB0_CLK				SDMMC_CMD SDMMC_DATA0	SPIM1_SS1_N SPIM0 SS1 N	SPIS0_MOSI SPIS0_CLK	+	
HPS_CLK1	GFIOU_IOU	ואַרואַר_אַרעע	OARTO_CTO_N			+		USBU_CLK			+	ODIVINIO_DATAU	OF HVIU_OO I_IV	OF IOU_OLIN		
HPS_nPOR			+		+	+			 		+	+	+			
HPS_nRST			+		+	+			 		+	+	+			
HPS_DEDICATED_4	GPIO2_IO0	NAND_ADQ0	1					SDMMC_DATA0			1	QSPI_CLK				
HPS DEDICATED 5	GPIO2 IO1	NAND ADQ1						SDMMC CMD				QSPI IO0				
BOOTSEL2/HPS_DEDICATED_6	GPIO2_IO2	NAND WE N						SDMMC CCLK				QSPI_SS0				
HPS_DEDICATED_7	GPIO2_IO3	NAND_RE_N						SDMMC_DATA1				QSPI_IO1				
HPS_DEDICATED_8	GPIO2_IO4	NAND_ADQ2						SDMMC_DATA2				QSPI_IO2_WPN				
HPS_DEDICATED_9	GPIO2_IO5	NAND_ADQ3	1					SDMMC_DATA3				QSPI_IO3_HOLD				
BOOTSEL1/HPS_DEDICATED_10	GPIO2_IO6	NAND_CLE						SDMMC_PWR_ENA					SPIMO_SS1_N	SPISO_MISO		
BOOTSELO/HPS_DEDICATED_11	GPIO2_IO7	NAND_ALE						QSPI_SS1				CM_PLL_CLK0	SPIMO_CLK			
HPS_DEDICATED_12	GPIO2_IO8	NAND_RB	UART1_TX					SDMMC_DATA4				CM_PLL_CLK1	SPIM0_MOSI		EMAC1_MDIO	I2C_EMAC1_SDA
HPS_DEDICATED_13	GPIO2_IO9	NAND_CE_N	UART1_RTS_N					SDMMC_DATA5				CM_PLL_CLK2	SPIMO_MISO		EMAC1_MDC	I2C_EMAC1_SCL
HPS_DEDICATED_14	GPIO2_IO10	NAND_ADQ4	UART1_CTS_N					SDMMC_DATA6				CM_PLL_CLK3	SPIMO_SSO_N		EMAC2_MDIO	I2C_EMAC2_SDA
HPS_DEDICATED_15	GPIO2_IO11	NAND_ADQ5	UART1_RX					SDMMC_DATA7				CM_PLL_CLK4		SPISO_CLK	EMAC2_MDC	I2C_EMAC2_SCL
HPS_DEDICATED_16	GPIO2_IO12	NAND_ADQ6	UART1_TX					QSPI_SS2				T		SPISO_MOSI	EMACO_MDIO	I2C_EMACO_SDA
HPS_DEDICATED_17	GPIO2_IO13	NAND_ADQ7	UART1_RX			1		QSPI_SS3						SPISO_SSO_N	EMACO MDC	I2C_EMACO_SCL



Hard Processor System Pin Information for Intel® Arria® 10 Devices Version 1.1

Version Number	Date	Changes Made					
1.0	9/26/2014	Initial release.					
1.1	3/24/2017	Rebranded as Intel.					