TECHNICAL BULLETIN

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

REVISION STATUS				
Revision	**SCR No.**	**Description**	**Initial**	**Date**
"-"	54714	Initial Release	Colleen Murphy	6/25/08
"A"	55031	Updated Min PWB information	Art Dellas	6/10/09
"B"	55938	Added New Figures 3, 4, and 5 Renumbered Subsequent Figures Revised Table of Contents	John Bailey	3/8/12

Amphenol Backplane Systems

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

TABLE OF CONTENTS

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

TABLE OF CONTENTS (CONTINUED)

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

1.0 SCOPE

1.1 Intent

1.1.1 The intent of this technical bulletin is to outline the standard signal trace widths, minimum spacing requirements and finish hole size requirements for the VIPER connector series when used in differential and single-ended signal applications. Furthermore, this bulletin provides specific design recommendations that will address layout, electrical performance, and manufacturability tradeoffs of the connector at the PCB level. The VIPER connector has a 1.8mm x 1.8mm backplane grid and a 1.8mm x 1.35mm mating daughtercard grid. These connectors are two-piece devices that connect two printed circuit boards. Daughtercard blade wafers and backplane receptacle connectors are through-hole-devices with eye-of-the-needle compliant pin contacts.

1.2 Efficient Routing

1.2.1 Efficient routing of signal traces between connector patterns improves yields and manufacturability. Spacing between trace/pad and trace/trace needs to be considered to allow for proper feature modifications needed for the inner layer fabrication process. Failure to allow for this may result in lower yields and higher PWB costs.

1.3 Finished Hole Sizes

1.3.1 All finished hole size requirements provided within this document are based on testing completed in FR-4 laminate.

2.0 DEFINITIONS

2.1 Fillets

2.1.1 An extension of the pad at the interface of the trace to the pad that will allow more pad area, in the event that the pad to hole registration compromises the interconnect area. See Figure 1 for details. For further information regarding these routing guidelines, please contact ABS Applications Engineering.

2.2 Foils/Copper Weights

2.2.1 Copper foil is measured in ounces (or weight) per square foot. Common copper weights are 0.5 ounces, 1 ounce, 1.5 ounces and 2 ounces (3 ounces up to 10 ounces are available for special order). 1 ounce = 0.0014", 1.5 ounces = 0.0021", 2 ounces = 0.0028".

2.3 Pads/Lands/Annular Ring

2.3.1 A pad is the support around a hole. If you see a specification calling out an annular ring of 0.005" (0.127mm), that will mean the amount of the pad left around the hole after processing.

2.4 Spacing

2.4.1 Spacing is the space between two electrical connections; it can be between two lines, two pads, a line and a pad etc.

2.5	Trace/Circuit/Line Width/Lines/Conductor
2.5.1	These are different terms for a connection. If you see the term 0.008" (0.203mm) lines, it means the electrical connection from one point to another will measure 0.008" (0.203mm) width.
2.6	Backplane
2.6.1	When used within this document refers to the PCB associated with the male connector half of the connector system mounted to a fixed PCB in a chassis.
2.7	Daughtercard
2.7.1	When used within this document refers to the PCB associated with the right-angle male connector half of the connector system mounted to a plug-in card in a chassis.
3.0	**ROUTING GUIDELINES**
3.1	Minimum Spacing
3.1.1	Minimum spacing, specific pad/trace, and trace/trace between all features should be 0.005" (0.127mm) to allow for manufacturing tolerances.
3.2	Impedance
3.2.1	Consider characteristic impedance (if applicable) when designing to ensure line widths will meet requirements. Please contact Amphenol Backplane Systems (ABS) Applications Engineering for impedance calculations.
3.3	Copper Weights
3.3.1	Consider copper weights when routing. Higher weights will impact minimum trace widths.
3.4	Fillets
3.4.1	Fillets at the interface (egress) of the trace to the pad are required to improve annular ring when the electrical design requires tight hole to pad configurations.
3.5	Trace Centering
3.5.1	Center all traces between holes to optimize spacing.
3.6	Non Functional Pads
3.6.1	For high speed applications, remove all non-functional pads. This is critical for multi-gigabit applications.
4.0	**DESIGN RULES AND MANUFACTURABILITY GUIDELINES**
4.1	General Design Rules
4.1.1	Drill
4.1.1.1	Backplane: ISO 0.65mm (0.0255") ±0.02mm.
4.1.1.2	Daughtercard Hole: ISO 0.55mm (0.0217") ±0.02mm.
4.1.2	Footprint
4.1.2.1	For specific connector footprint see Figures 1 and 2.
4.1.3	Drilled Hole and Copper Thickness
4.1.3.1	For copper wall thickness requirements and finish hole size reference, see Table 1, Figure 4 and Figure 5.

4.2	Daughtercard/ Backplane Manufacturability Guidelines
4.2.1	Line Widths, Pad Sizes and Spacing
4.2.1.1	Line widths, pad sizes and spacing applicable for 1/2 ounce and 1 ounce copper weights.
4.2.2	Filleting
4.2.2.1	Filleting of pads recommended (to be added by fabricator) for 0.000” annular ring (tangency), see Figure 3.
4.2.3	Minimum PCB Thickness
4.2.3.1	Recommended minimum daughtercard PCB thickness of 0.060” (1.525mm) and backplane PCB thickness of 0.073” (1.85mm).
4.2.4	Non-functional pads
4.2.4.1	Non-functional pads on signal should be removed for all multi-gigabit applications.
4.2.5	Plane Clearances
4.2.5.1	Plane clearances are applicable for copper weights up to 2 ounces. Please contact Amphenol Backplane Systems Applications Engineering for designs utilizing more than 2 ounces of copper per layer.
4.2.6	Surface Traces
4.2.6.1	Surface traces are not recommended. They tend to display more loss and are typically noisier. Surface microstrip traces will also generate forward crosstalk, whereas the forward crosstalk in internal stripline traces will be near zero.

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

5.0 ROUTING GUIDELINES

5.1 VIPER Signal Pad Sizes for Daughtercards and Backplanes

PCB Material Thickness in (mm)	Copper Weight (Ounces)	Process	Min. Pad Size 0.000 A/R, in (mm)	Min. Pad Size 0.001 A/R, in (mm)	Min. Pad Size 0.002 A/R,in (mm)
Daughtercards 0.060 to 0.150 (1.525 to 3.81)	0.5 (17μm)	Inner Layer	0.035 (0.89)	0.037 (0.94)	0.039 (0.99)
		Outer Layer	0.0375 (0.95)	0.0395 (1.00)	0.0415 (1.05)
Daughtercards 0.060 to 0.150 (1.525 to 3.81)	1.0 (35μm)	Inner Layer	0.036 (0.91)	0.038 (0.96)	0.040 (1.02)
		Outer Layer	0.0375 (0.95)	0.0395 (1.00)	0.0415 (1.05)
Backplanes 0.073 to 0.350 (1.85 to 8.89)	0.5 (17μm)	Inner Layer	0.039 (0.99)	0.041 (1.04)	0.043 (1.09)
		Outer Layer	0.0415 (1.05)	0.0435 (1.10)	0.0455 (1.15)
Backplanes 0.073 to 0.350 (1.85 to 8.89)	1.0 (35μm)	Inner Layer	0.040 (1.02)	0.042 (1.07)	0.044 (1.12)
		Outer Layer	0.0415 (1.05)	0.0435 (1.10)	0.0455 (1.15)

Table 1: Viper Minimum Pad Size vs. Copper Weight and Annular Ring ("A/R")

Notes for Table 1:

1. Outer layer pad sizes reflect a panel plating process.
2. Use inner layer pad sizes for outer layer pad sizes when pattern plating.
3. Values in parentheses are metric equivalents. For printed circuit board layout design, use metric units.
4. For plane clearances see Section 5.5, for all other plane clearances contact Amphenol Backplane Systems Applications Engineering.

5.2 Copper Thickness Requirement and Finished Thickness Reference

5.2.1 For Daughtercards:

Finish Type	Copper thickness, in Inches (mm) per side	Drill size, in inches (mm)	Typical Finish Thickness	Finished Hole Size, in Inches (mm)
Solder Finish (1)	0.0010 (0.0254) min 0.0025 (0.0635) max	0.0217 (0.55)	300-500 µinch (0.0076-0.0127)	0.018 ± 0.002 (0.46 ± 0.05)
Copper - OSP	0.0010 (0.0254) min 0.0025 (0.0635) max	0.0217 (0.55)	N/A	0.018 ± 0.002 (0.46 ± 0.05)
Nickel-Gold	0.0010 (0.0254) min 0.0025 (0.0635) max	0.0217 (0.55)	53-210µinch Ni-Au combined thickness (0.0013-0.0053)	0.018 ± 0.002 (0.46 ± 0.05)

Table 2: Copper Thickness Requirement and Finished Thickness Reference for Daughtercards

5.2.2 For Backplanes:

Finish Type	Copper thickness, in Inches (mm) per side	Drill size, in inches (mm)	Typical Finish Thickness	Finished Hole Size, in Inches (mm)
Solder Finish (1)	0.0010 (0.0254) min 0.0025 (0.0635) max	0.0256 (0.65)	300-500µinch (0.0076-0.0127)	0.022± 0.002(0.56 ±0.05)
Copper - OSP	0.0010 (0.0254) min 0.0030 (0.0762) max	0.0256 (0.65)	N/A	0.022± 0.002(0.56 ±0.05)
Nickel-Gold	0.0010 (0.0254) min 0.0025 (0.0635) max	0.0256 (0.65)	53-210µinch Ni-Au combined thickness (0.0013-0.0053)	0.0226± 0.002(0.575 ±0.05)

Table 3: Copper Thickness Requirement and Finished Thickness Reference for Backplanes

Note 1: Solder finish includes: Tin/lead reflowed (plated and reflowed) and HASL. Thickness measurement performed prior to fusing/ reflow process.

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

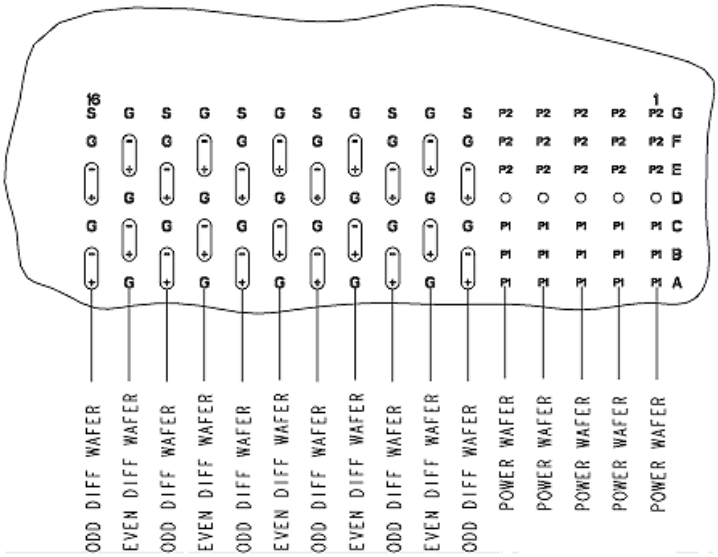

Figure 1. Daughtercard Connector Footprint

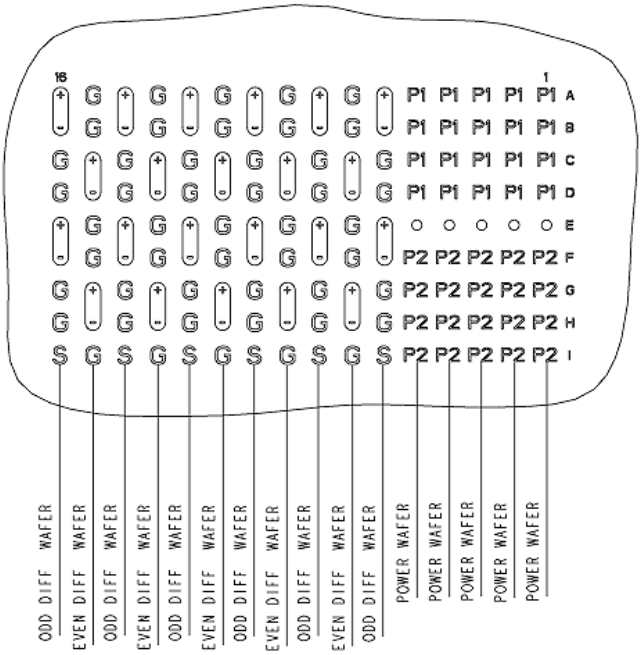

Figure 2. Backplane Footprint

Amphenol Backplane Systems

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

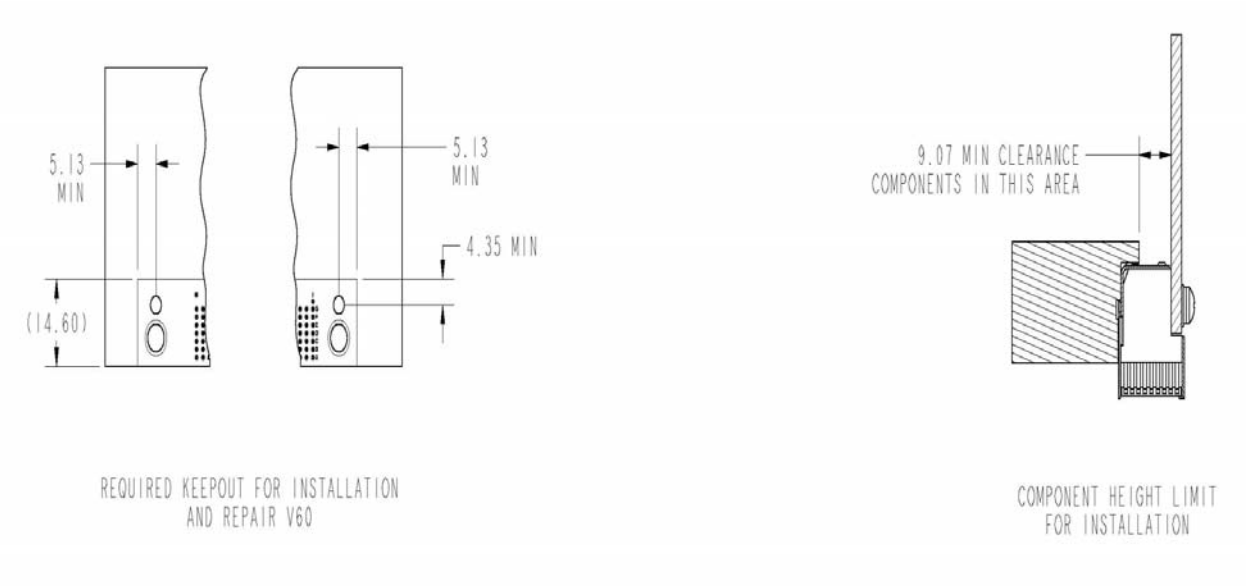

Figure 3. Daughtercard Component Keepout – Vita 60

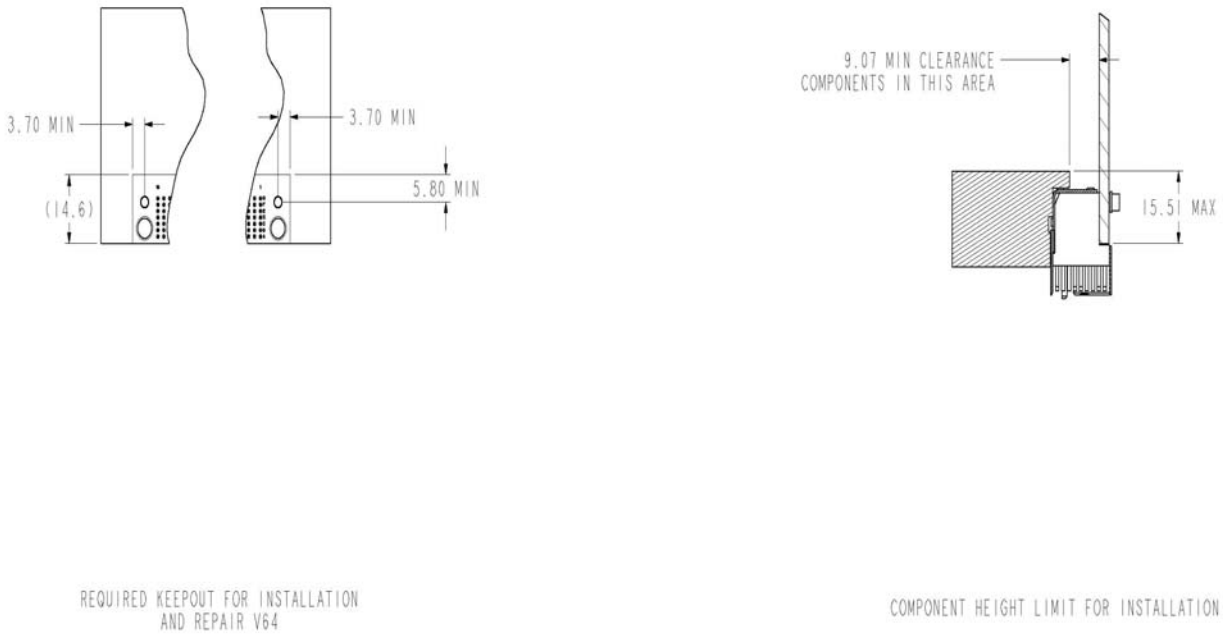

Figure 4. Daughtercard Component Keepout – Vita 64

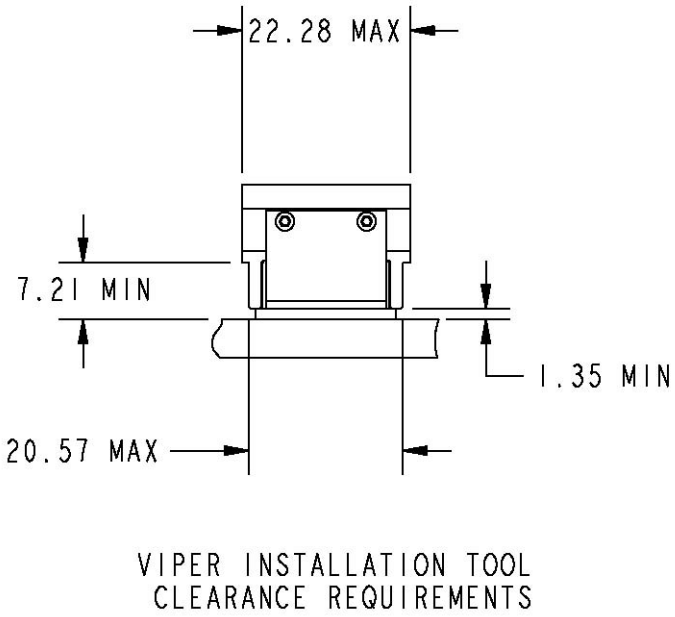

Figure 5. Backplane Component Keepout

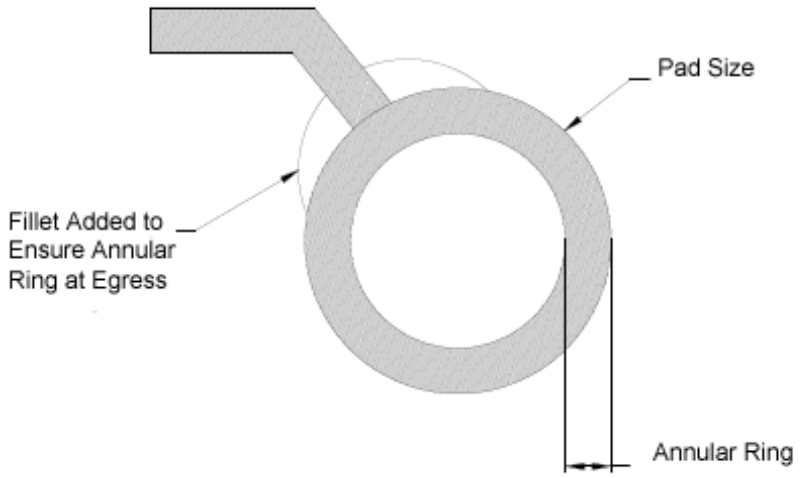

Figure 6: Preferred Fillet

5.2.3 Fillet Diameter equals one-half size of plated through hole pad diameter located on a line central to trace so that fillet size equals minimum annular ring plus 0.005 inches or (0.13mm).

5.3 Drill and Finished Hole Size

Daughter Card Hole Size

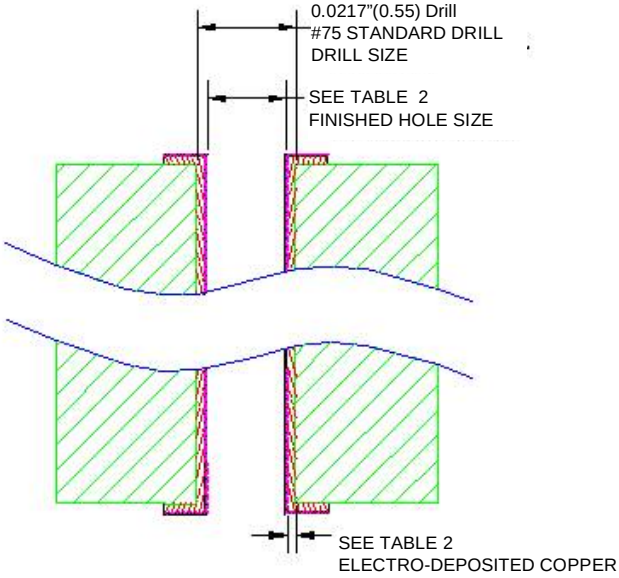

Figure 7. VIPER Drill and Finished Hole Size for Daughtercards

Backplane Hole Size

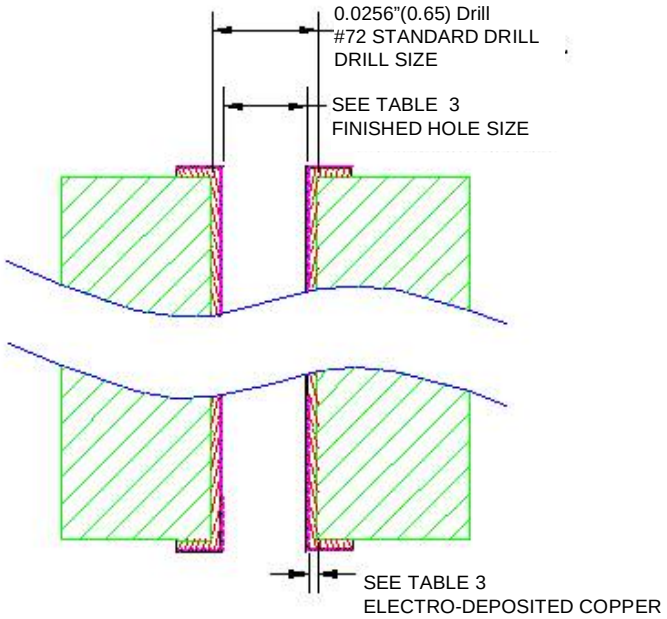

Figure 8. VIPER Drill and Finished Hole Size for Backplanes

5.4 Compliant Pin Critical Zone

5.4.1 The "Critical Working Zone" shown in the following figures is defined as the compliant working zone where the plated through hole requirements must meet the specifications defined within this document. In the "Non Critical Zone", the plated through hole is allowed to go below the minimum required finish hole size of 0.018" for daughter cards and 0.022" for backplanes in non-midplane applications.

5.4.2 Backdrilling is allowed in the "non critical zone" only. Backdrilling will be required for most high-speed applications on the backplane. The bottom of Figure 6 shows a non-backdrilled via to the left and a backdrilled via in the middle. The dual diameter via on the right is sometime used to reduce noise but is not very common. Removing a portion of the via barrel lowers via capacitance, improves noise characteristics and significantly improves the performance of the connector launch. Note that the pin is inserted after backdrilling so it doesn't matter how close you drill to the pin. The length of the pin determines the minimum stub length achievable, in this case 90 mils (2.28mm). It is important to discuss backdrilling with the specific board fabrication vendor to understand their tolerancing requirements and limitations.

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

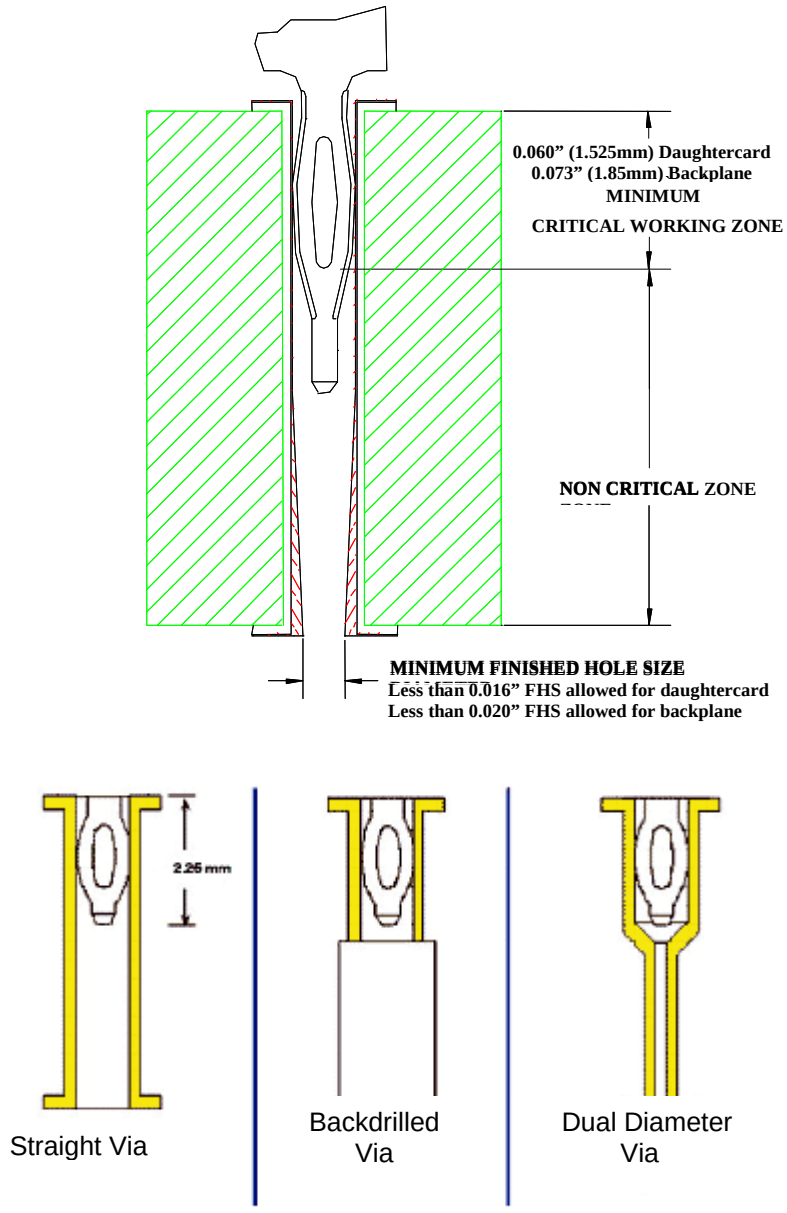

Figure 9. VIPER Compliant Pin Critical Zone and Backdrilling

5.5 Typical Anti-pad Geometry

5.5.1 The following describes recommended anti-pad design for VIPER. Variations to this design based on stack-up design and performance requirements are allowed. They should be characterized using 3D modeling techniques (e.g. HFSS or CST Microwave Studio). Recommended Differential anti-pad structures, such that a single anti-pad surrounds both signal pins, are shown in Figures 7 and 8 below. (This structure is patented by Amphenol). Note that the geometry leaves 10 mils (0.25mm) from edge of anti-pad to edge of ground hole to improve producability. Single-Ended anti-pad structures can be found in Figures 9 and 10.

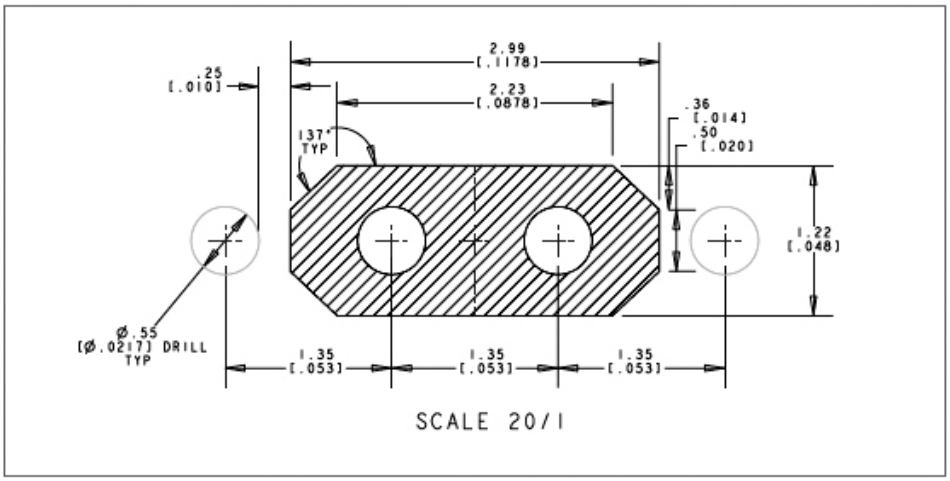

Figure 10. Anti-Pad Clearance for VIPER Daughtercard Differential

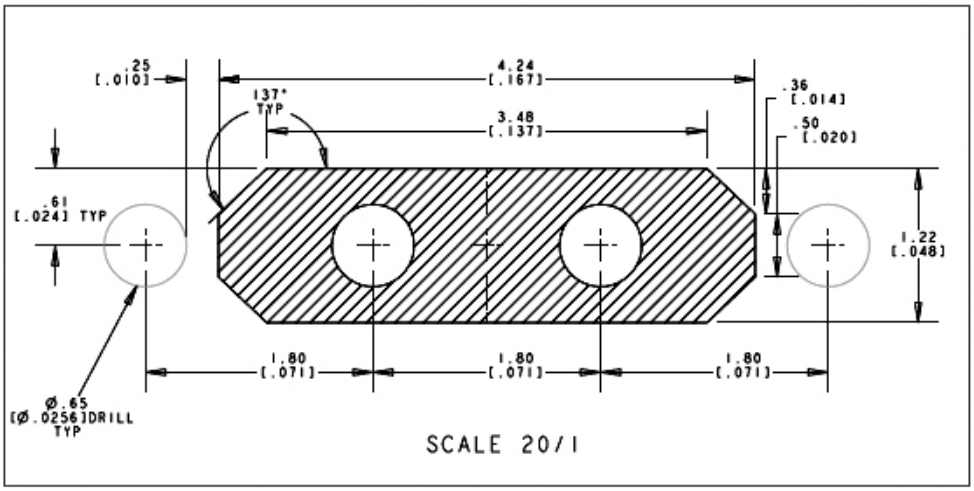

Figure 11. Anti-Pad Clearance for VIPER Backplane Differential

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

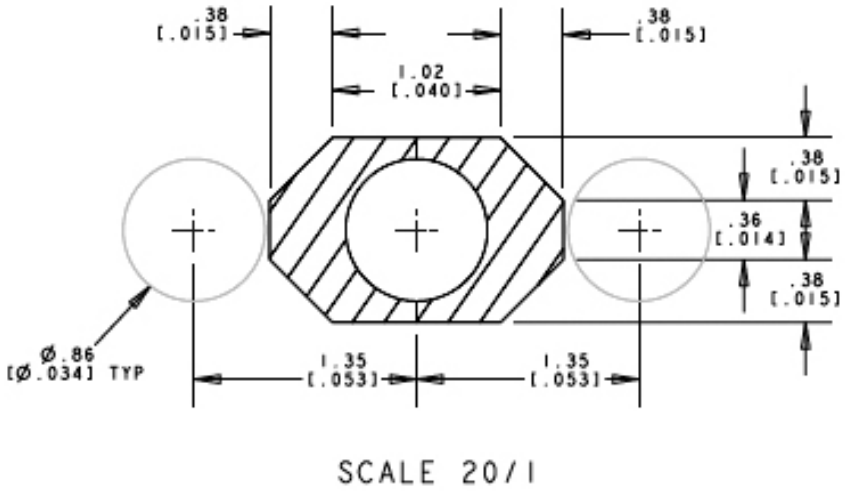

Figure 12. Anti-Pad Clearance – VIPER Daughtercard Single-Ended

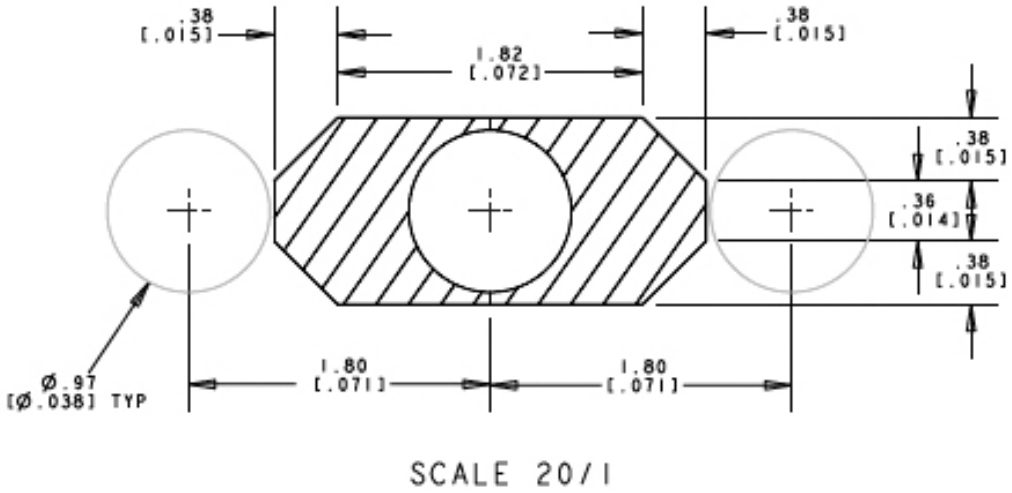

Figure 13. Anti-Pad Clearance – VIPER Backplane Single Ended

5.6 VIPER Typical High-Speed Differential Routing

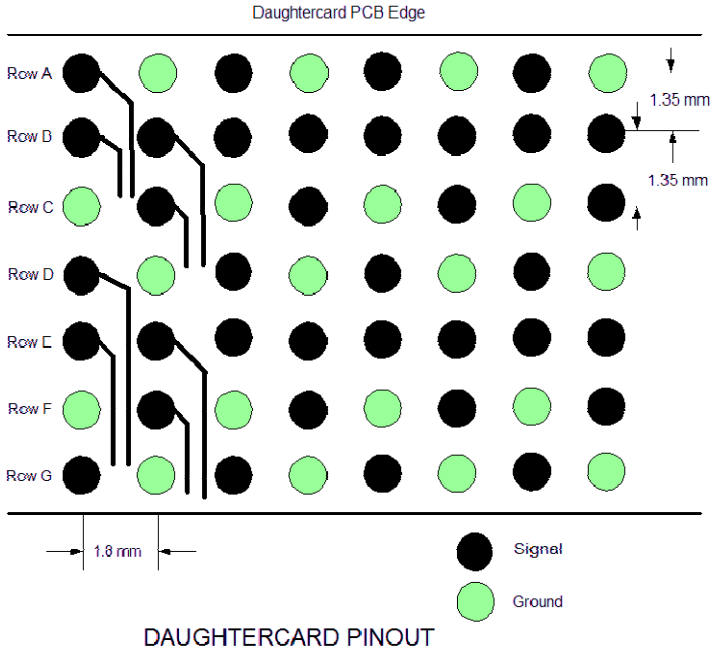

Figure 14. VIPER Daughtercard Hole Pattern – Differential

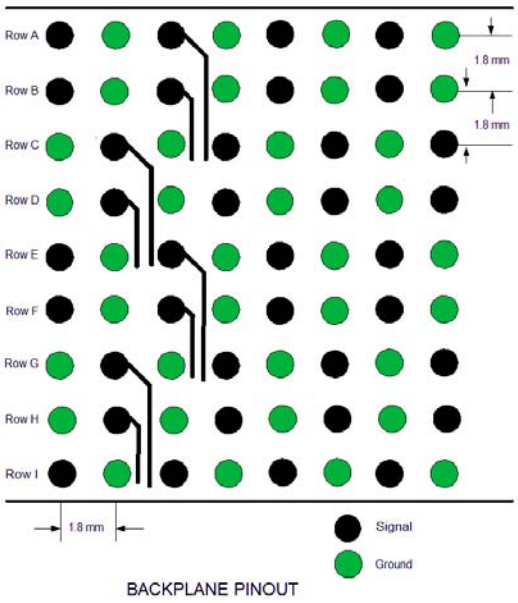

Figure 15. VIPER Backplane Hole Pattern – Differential

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

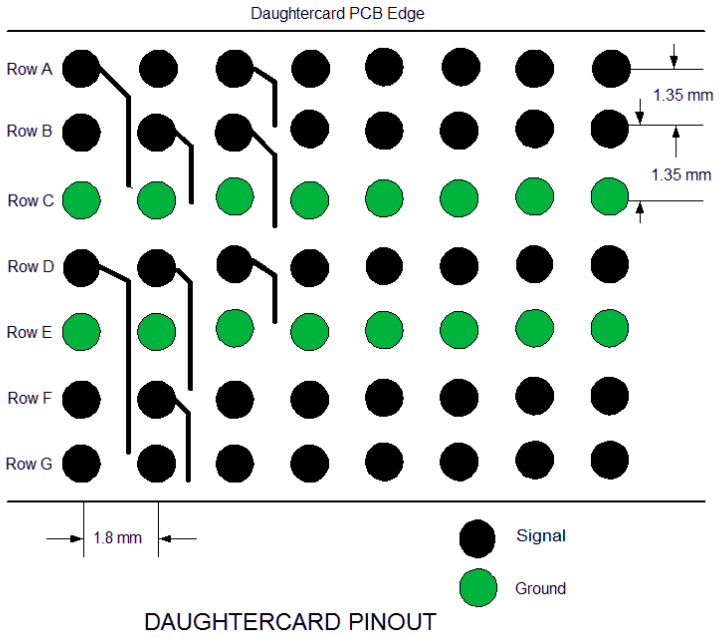

Figure 16. VIPER Daughtercard Hole Pattern – Single-Ended

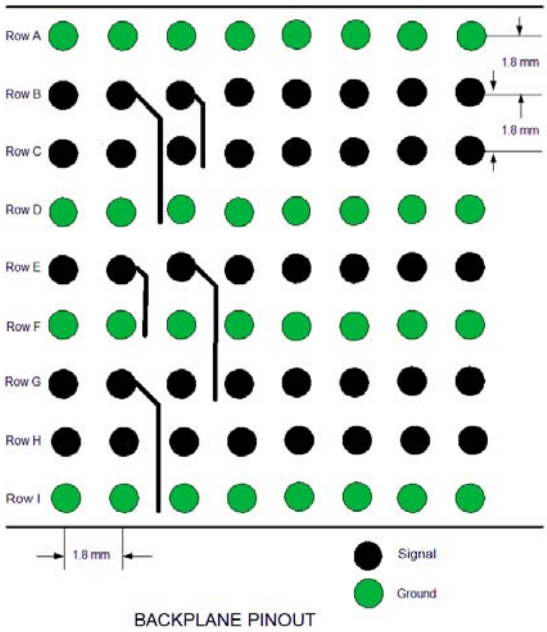

Figure 17. VIPER Backplane Hole Pattern – Single-Ended

5.6.1 Example - VIPER Daughtercard Routing

5.6.1.1 The available space for routing is determined by the distance between anti-pads. There is no secondary or vertical routing channel available on the daughtercard for differential pairs. Based on the VIPER 1.8mm (0.0709") spacing, this would leave a routing channel of 22.9 mils It is preferable to have a 3 or 4 mil edge-of-trace to edge-of-anti-pad space so that the pair is effectively referenced by the ground plane. This is shown below in Figure 15. Maintaining this 4 mil space on each side of the pair, the amount of space remaining for the differential trace pair itself would be 14.9 mils. Thus, a 5/6/5 pair (5 mil traces, 6 mil edge-to-edge space) would be a very reasonable design. Channel analysis and 3D modeling should be used to optimize link performance and anti-pad geometry for particular designs.

Center to Center	**0.0709" (1.80mm)**
Minus Anti-Pad Diameter	**0.048 (1.22)**
= Resulting Space for Traces	**0.0229 (0.582)**
Line Width	**0.005 (0.127)**
Space Between Lines	**0.006 (0.152)**
Resulting Ground Plane Web Overhang on Each Side	**0.00345 (0.0876)**

Table 4: Example VIPER Daughtercard Routing Channel Analysis

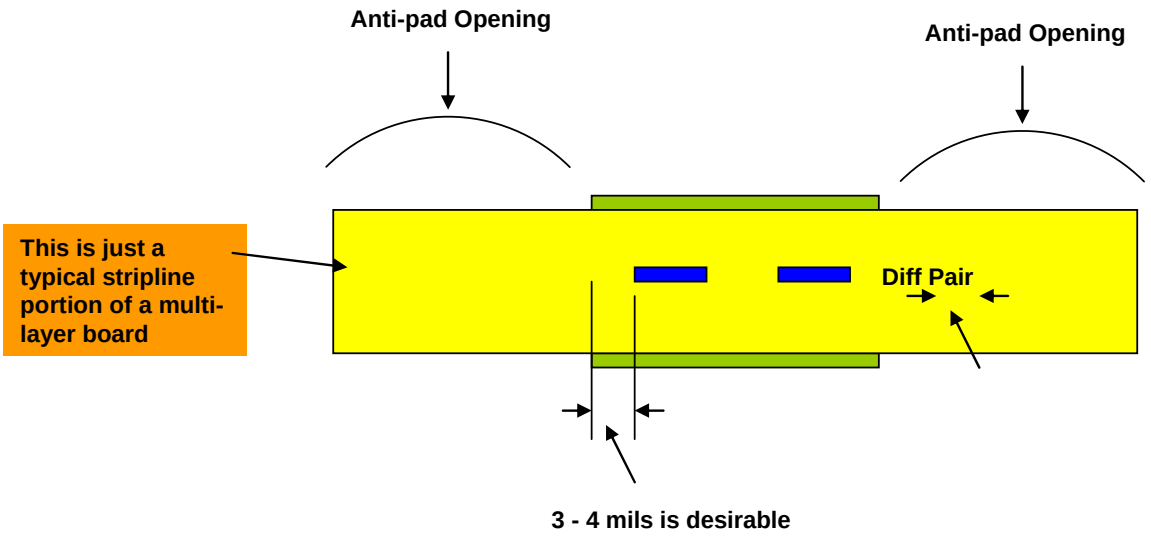

Figure 18. Example of VIPER Daughtercard High-Speed Differential Routing

5.6.2 Example - VIPER Backplane Routing

5.6.2.1 The available space for routing is determined by the distance between anti-pads. In this example, simulation has determined that the required backplane trace geometry is 8 mil traces with a 12 mil space. Since the backplane is on a 1.8mm x 1.8mm grid, it can be routed in both directions**.** Based on the VIPER 1.8mm (0.0709") spacing and reducing the anti-pad width to 38.9 mils, it would leave a routing channel of 32 mils. It is preferable to have a 3 or 4 mil edge-of-trace to edge-of-anti-pad space so that the pair is effectively referenced by the ground plane but in this case, a 2 mil overhang will result Table 5 and Figure 16. This is a tradeoff to keep the anti-pad as large as possible. Remember that the finished hole size for the backplane (22 mils) is larger than for the card (18 mils). Maintaining a 2 mil space on each side of the pair, the amount of space remaining for the differential trace pair itself would be 28 mils.

5.6.2.2 An alternative analysis is shown in Table 6 where a 3 mil space is maintained on each side of the pair with a routing channel of 22.9 mils. The amount of space remaining for the differential trace pair is 17 mils. Thus, a 6/5/6 pair (6 mil traces, 5 mil edge to edge space) would be a very reasonable design. Channel analysis and 3D modeling should be used to optimize link performance and anti-pad geometry for particular designs.

Center to Center	**0.0709" (1.80)**
Minus Anti-Pad Diameter	**0.0389 (0.988)**
= Resulting Space for Traces	**0.032 (0.813)**
Line Width	**0.008 (0.203)**
Space Between Lines	**0.0012 (0.305)**
Resulting Ground Plane Web Overhang on Each Side	**0.002 (0.051)**

Table 5: Example VIPER Backplane Routing Channel Analysis

Center to Center	**0.0709" (1.80mm)**
Minus Anti-Pad Diameter	**0.048 (1.22)**
= Resulting Space for Traces	**0.0229 (0.582)**
Line Width	**0.006 (0.152)**
Space Between Lines	**0.005 (0.127)**
Resulting Ground Plane Web Overhang on Each Side	**0.003 (0.074)**

Table 6: Example VIPER Backplane Routing Channel Analysis Alternative

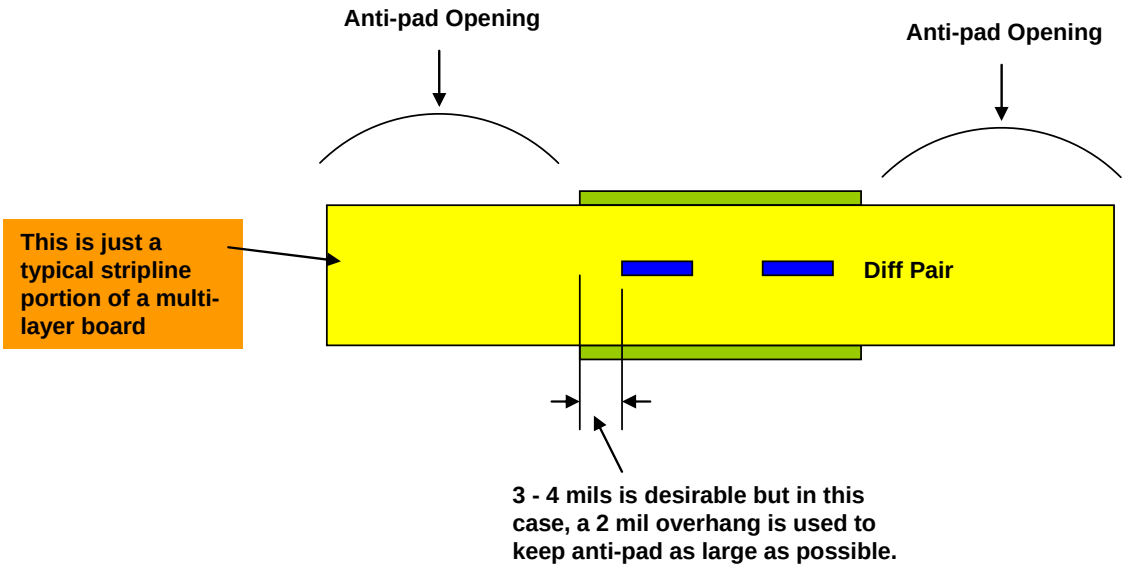

Figure 19: Example VIPER Backplane High Speed Differential Routing

6.0 **VIPER TX AND RX PIN ASSIGNMENTS**

6.1 In the VIPER connector, the worst-case noise generated is wafer-to-wafer. To minimize noise, keep TX pairs in the same rows and RX pairs in the same rows as shown below in Figure 17. With this strategy, TX generated noise is minimized on RX signals. Figures 18, 19,20 and 21 show the detailed pin mapping between the VIPER daughtercard and backplane.

6.2 Detailed Touchstone models are available for the VIPER connector and it is strongly recommended to perform the appropriate frequency domain channel analysis to quantify noise in the serial channels. This should include noise in the connector via footprints on both the Backplane and Daughtercards as well as noise in the connector itself. Additionally, any DC blocking cap launches should be optimized. Contact Amphenol Backplane Systems Applications Engineering for support on modeling.

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

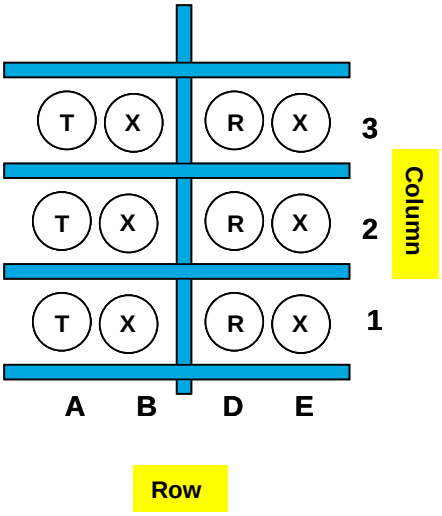

Figure 20: Optimal TX and RX pair assignment in VIPER

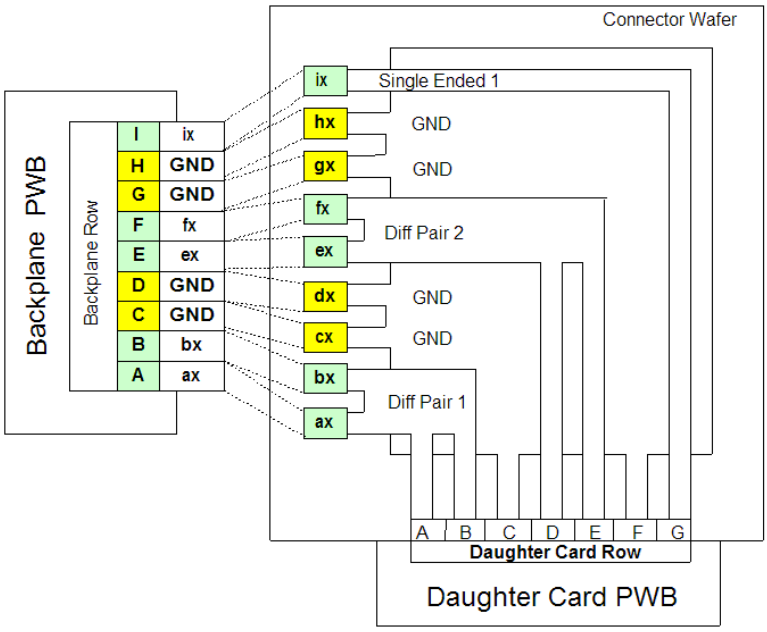

Figure 21. VIPER Pin Map of Daughtercard Wafer to Backplane Module – Differential A (Odd Mode)

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

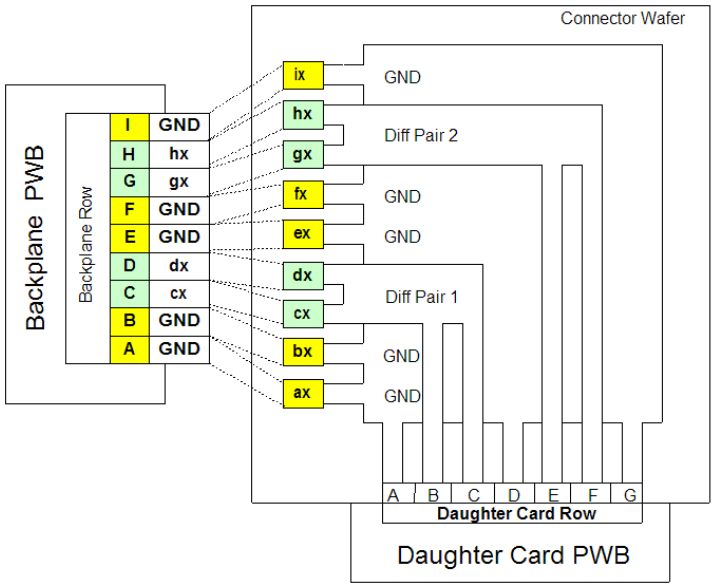

Figure 22. VIPER Pin Map of Daughtercard Wafer to Backplane Module - Differential B (Even Mode)

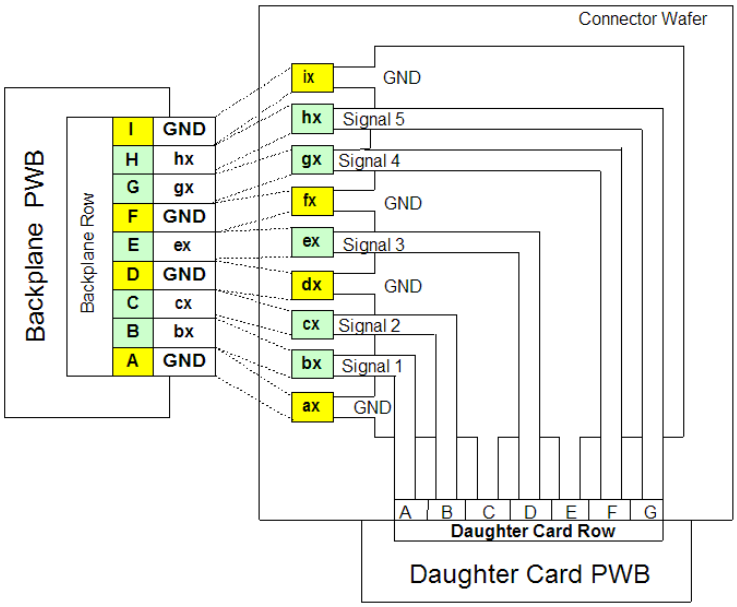

Figure 23. VIPER Pin Map of Daughtercard Wafer to Backplane Module – Single-Ended

VIPER™ SIGNAL TRACE ROUTING GUIDELINES FOR BACKPLANE AND DAUGHTERCARD CONNECTORS

TB-2097 **Revision "B" – 3/8/12**

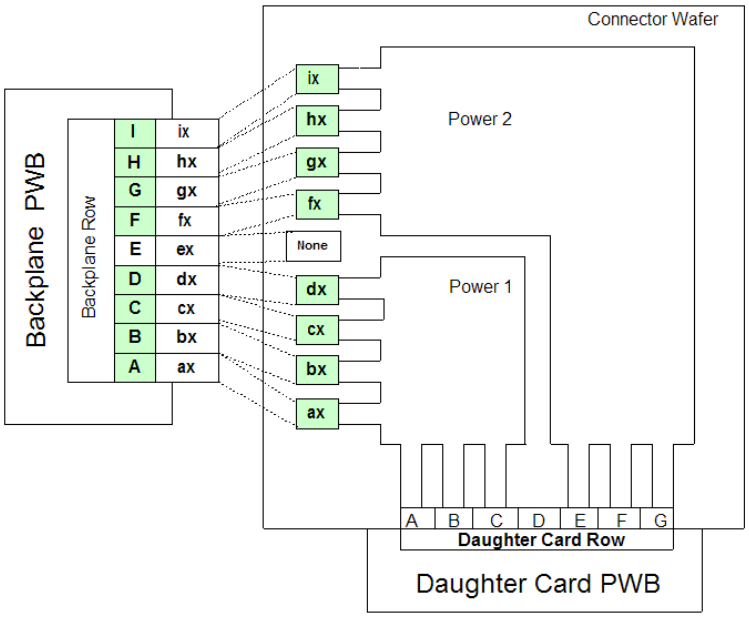

Figure 24. VIPER Pin Map of Daughtercard Wafer to Backplane Module – Power