82540EP/82541(PI/GI/EI) & 82562EZ(EX) Design Checklist v1.1

Project Name	
Fab Revision	
Date	
Designer	
Intel Contact	
Reviewer	

SECTION	CHECK ITEMS	REMARKS	√ DONE	COMMENTS
General	Have up-to-date product documentation and spec updates.	Documents are subject to frequent change.		
	Observe instructions for special pins needing pull-up or pull-down resistors.	Do not connect pull-up or pull-down resistors to any pins marked No Connect.		
82562EZ(EX) LCI Device Option	Connect LCI signals to corresponding signals on ICH device.			
	Each of the four control pins TESTEN, ISOL_TCK, ISOL_TI, and ISOL_EXEC should be connected to a LAN disable circuit through 100 Ω resistors.	Contact Intel for latest LAN disable circuit recommendations. If the LOM disable function is not used, connect Ball A13 to ground through a 3.3 K resistor.		
	Use a 93C46 EEPROM for non-alerting applications or a 93C66 EEPROM for ASF 1.0. **Note:** DO NOT use a Catalyst 93C46 Revision H.	EEPROM for 82562EZ(EX) attaches to ICH. Add decoupling capacitor. EEPROMs should be rated for at least 1 MHz.		
	Connect Ball B14 RBIAS10 to ground through a 619 Ω 1% resistor.	Recommended starting value. Meaure PCB's output amplitude and adjust as required to meet IEEE specification. See the 82540EP/82541(PI/GI/EI) & 82562EZ(EX) Dual Footprint Design Guide for more information.		
	Connect Ball B13 RBIAS100 to ground through a 649 Ω 1% resistor.	Recommended starting value. Meaure PCB's output amplitude and adjust as required to meet IEEE specification. See the 82540EP/82541(PI/GI/EI) & 82562EZ(EX) Dual Footprint Design Guide for more information.		

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82540EP/ 82541xx Controller Option	Connect 32-bit PCI interface pins to corresponding pins on system.			
	Connect Ball A9 LAN_PWR_GOOD to RSM_RST# or other voltage supervisor circuit.	Input should remain low until all power supplies are stable and for approximately 80ms. LAN_PWR_GOOD works like an auxiliary chip reset. It should be a clean, glitch-free signal. It is not intended for use as a LAN Disable. LAN_PWR_GOOD must be asserted during powerdown states to allow wakeup.		
	Connect Ball A6 PME# to system for wake up signaling.	Typical connection is PME# on ICH.		
	Connect Ball J12 AUX_PWR signals correctly.	AUX_PWR is a logic input denoting that auxiliary power is connected to the device. AUX_PWR = 1 is a requirement for wakeup.		
	Connect Ball B9 RST# to RST# on system.			
	For 82540EP, connect a 2.49 K Ω resistor from ball B14 PHYREF to ground.			
	Connect a 0.01 μF capacitor between Ball C2 M66EN and ground. M66EN should have a pull-up resistor somewhere in the system.	Capacitor per spec for signal integrity. This signal may be grounded anywhere on the segment for any PCI device incapable of 66 MHz operation.		
	Connect Ball G2 VIO to 5 V Standby or 3.3 V Standby to match PCI signaling voltage.	Use a 100 K Ω resistor as a current limiter and a 0.1 μF bypass capacitor.		
	For 82540EP only, attach a 33.2 Ω 1% pull-up resistor from ball H4 ZN_COMP to 3.3 V. Attach a 53.6 Ω 1% pull-down resistor from ball G4 ZP_COMP to ground.	Sets PCI bus drive strength.		
	If a LAN disable function is required, drive Ball P9 FLSH_SO /LAN_ DISABLE#. For 82551ER(IT), this is a no connect.	Use a Super IO general purpose (GP) port that retains its value during reset.		
	For the 82540EP only, use a 93C46 EEPROM for non-alerting applications or a 93C66 EEPROM for ASF1.0. **Note:** DO NOT use a Catalyst 93C46 Revision H.	For Microwire* EEPROMs, install a 100 Ω pull-down resistor on ball J4. Do not install a pull-down resistor on the EEDO pin. EEPROMs should be rated for at least 1 MHz.		
	For the 82541xx only, use a 93C46 EEPROM for non-alerting applications, an AT25040 for ASF1.0, or an AT25080 for ASF 2.0. **Note:** DO NOT use a Catalyst 93C46 Revision H.	For Microwire* EEPROMs, install a 1 K Ω pull-down resistor (for the 82541PI only, use a 100 Ω resistor) on ball C4 EEMODE. Do not install a pull-down resistor on the EEDO pin.		

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		For SPI* EEPROMs, install a 1K Ω pull-up resistor on ball J4 EEMODE, use a 3.3 K Ω pull-up resistor on write protect (WP#) and a 3.3 K Ω pull-up resistor on HOLD#. Microwire EEPROMs should be rated for at least 1 MHz and SPI* EEPROMs should be rated for at least 2 MHz.		
	Check reference schematic for connection of Software Defined Pins.	Intel driver software may expect to use Software Defined Pins for special functions.		
	Connect Ball A13 TEST to ground, using a 1 K Ω resistor for dual layout designs with 82562EZ(EX).			
	Provide a test point for IEEE PHY conformance testing. Depopulate the header for production.	For the 82540EP, this will be a header between ball M8 CLK_VIEW and ground (single-ended clock output). For the 82541xx, this will be a header between balls B14 and D14 (differential clock output).		
Clock Source	Use 25 MHz 30 ppm accuracy at 25 degrees C.	Parallel resonant crystals are preferred.		
	For the 82540EP, connect two 22 pF load caps to crystal. For the 82541GI(EI), connect two 18 pF load caps to crystal.	Capacitance affects accuracy of the frequency. Must be matched to crystal specs, including estimated trace capacitance in calculation. Use low ESR caps.		
EEPROM and FLASH Memory	Use decoupling capacitor.	Applies to EEPROM or FLASH devices.		
	EEPROM ORG ties to 3.3 V for x16 access.	For Microwire EEPROMs. Depends on EEPROM used.		
	Consider whether to use FLASH memory.	Most LOM systems with boot ROM place the image in the system FLASH.		
	If FLASH memory is used, select the appropriate device.	82540EP and 82541xx controllers use serial FLASH.		
SMBus (82540EP and 82541xx)	If SMBus is not used, connect pull-up resistors to SMBCLK, SMBDATA, and SMB_ALERT#.	4.7 K Ω pull-ups are reasonable values.		
	If SMBus is used, system should have pull-up resistors.	SMBus signals are open-drain.		
	For 82540EP/ 82541xx ASF applications, connect Ball B10 SMB_ALERT# to the system LAN_PWR_GOOD signal or to Vcc through a 3.3 K Ω pull-up resistor.	Use 3.3 V, not 3.3 V AUX. Alternatively, ball B10 can be configured as an SMB_ALERT# output.		

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Transmit and Receive Differential Pairs	82562EZ(EX) controllers use pairs of 54.9 Ω termination resistors.	Apply to both differential pairs.		
	82540EP/ 82541xx controllers use pairs of 49.9 Ω termination resistors with 0.01 μF capacitors attached between center nodes and ground.	Apply to all four differential pairs.		
Magnetics Module (10/100/1000 Base-T Applications)	Integrated magnetics modules/RJ-45 connectors are available to minimize space requirements.	Modules with pin compatibility from 10/100 to Gigabit are available, containing internal jumpers for the unused pairs. Multivendor pin compatibility is possible. Contact manufacturers.		
	Qualify magnetics module carefully for Return Loss, Insertion Loss, Open Circuit Inductance, Common Mode Rejection, and Crosstalk Isolation	Magnetics module is critical to passing IEEE PHY conformance tests and EMI test.		
	For 82562EZ(EX) devices use a 5-core model. For 82540EP and 82541xx controllers use a 12-core model.	Autotransformer models (10/100) provide better cable termination. All Gigabit models contain autotransformers.		
	For 82562EZ(EX) LCI devices, use 0.1 μF capacitor on receive center tap.	Improves bit error rate.		
	For 82562EZ(EX) LCI devices, do not use capacitor on transmit center tap.	For severe EMI problems, a capacitor up to 22 pF can be used. Larger values will diminish signal strength and fail IEEE PHY conformance.		
	For 82541xx controllers, supply 1.8 V to the transformer center taps and use 0.1 μF bypass capacitors. The 82540EP controller uses 2.5 V.	These voltages bias the controller's output buffers. Magnetics with four center tap pins may have better characteristics than those with one to two center tap pins. Use capacitors with low Equivalent Series Resistance (ESR). Decoupling capacitors should be placed as close as possible to the center tap pins.		

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Discrete Magnetics Module/RJ-45 Connector Option (10/100/1000 Base-T applications)	Bob Smith termination: use 4 x 75 Ω resistors for cable-side center taps and unused pins.	Terminates pair-to-pair common mode impedance of the CAT5 cable.		
	Bob Smith termination: use an EFT capacitor attached to the termination plane. Suggested values are 1500 pF/2KV or 1000 pF/3KV	Maintain greater than 25 mil spacing from capacitor to traces and components.		
	Connect signal pairs correctly to RJ-45 connector.	The differential pairs use pins 1-2 (Transmit in 10/100), 3-6 (Receive in 10/100), 4-5 (Gigabit only), and 7-8 (Gigabit only). Take care not to reverse the polarity.		
Power Supply and Signal Ground	For the 82541xx controller, connect external PNP transistors to the regulator control CTRL12 and CTRL18 outputs to supply 1.2 V and 1.8 V, respectively. The connections and transistor parameters are critical. (82540EP uses CTRL15 and CTRL18 to supply 1.5 V and 1.8 V, respectively.)	Alternatively, provide external regulators to generate these voltages. If the internal voltage regulator control circuit is not used, the CTRL pins may be left unconnected.		
	For the 82540EP and 82541xx controllers, consider using two 0.5 Ω resistors in parallel to the emitter path of the 1.2 V power supply PNP transistor for regulator power dissipation.			
	For the 82540EP/82541xx controllers or the 82562EZ(EX) device, provide a 3.3 V supply.	The 82562EZ(EX) component is a single-voltage device.		
	Design with power supplies that start up properly.	A good guideline is that all voltages should ramp to within their control bands in 20 ms. or less. It is desirable that voltages ramp in sequence and that the voltage rise be monotonic.		
	Use auxiliary power supplies.	Auxiliary power is necessary to support wake up from powerdown states.		
	Use decoupling and bulk capacitors generously.	Use approximately 12 bypass capacitors for the 82540EP/82541xx Ethernet silicon. Add approximately 20-30 µF of bulk capacitance per voltage rail, typically using 10 µF capacitors. If power is distributed on traces, bulk capacitors should be used at both ends. If power is distributed on cards, bulk capacitors should be used at the connector.		

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Chassis Ground (10/100/1000 Base-T applications)	If possible, provide a separate chassis ground to connect the shroud of the RJ-45 connector and to terminate the line side of the magnetics module.	This design improves EMI behavior.		
	Place pads for approximately four "stitching" capacitors to bridge the gap from chassis ground to signal ground.	Typical values range from 0.1μF to 4.7μF. Determine experimentally.		
Termination Plane	For designs with non-integrated magnetics modules, lay out Bob Smith termination plane. Term plane floats over chassis ground.	Splits in ground plane should be at least 50 mils to prevent arcing during hi-pot tests.		
LED Circuits	Basic recommendation is a single green LED for Activity and a dual (bi-color) LED for Speed. Many other configurations are possible.	Two LED configuration is compatible with integrated magnetics modules. For the Link/Activity LED, connect the anode to the ACTIVITY#/ACTLED# pin (ball C11) and the cathode to the LINK_UP#/LILED# pin (ball A12). For the bi-color speed LED pair, have the Link 100#/SPDLED# signal drive one end. The other end should be connected to 3.3 V for the 82562EZ(EX) device or to LINK1000# for the 82541xx device (use 0 Ω resistors for dual footprint designs.)		
	Connect LEDs to 3.3V as indicated in reference schematics.	Use 3.3V AUX for designs supporting wakeup. Consider adding 1-2 filtering capacitors per LED for extremely noisy situations. Suggested starting value 470 pF.		
	Connect LEDs to 3.3 V as indicated in reference schematics.	Use 3.3 V AUX for designs supporting wakeup. Consider adding filtering capacitors for extremely noisy situations. Suggested starting value 470 pF.		
	Add current limiting resistors to LED paths.	Typical current limiting resistors are 300 to 330 Ω when using a 3.3V supply. Current limiting resistors are typically included with integrated magnetics modules.		

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Mfg Test	82540EP and 82541xx controllers use a JTAG Test Access Port.	Place 1 K Ω pull-down resistors on ball L13 JTAG_TRST# and Ball L14 JTAG_TCK. (Use 100 Ω resistors for the 82541PI.) These connections hold the TAP controller in an inactive state. For 82562EZ(EX) LCI device option, depopulate the pull-down resistors.		