

November 1988 Revised November 1999

74AC08 • 74ACT08 Quad 2-Input AND Gate

General Description

The AC/ACT08 contains four, 2-input AND gates.

Features

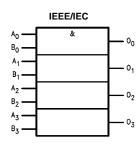
- I_{CC} reduced by 50% on 74AC only
- Outputs source/sink 24 mA

Ordering Code:

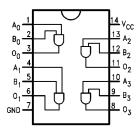
Order Number	Package Number	Package Description
74AC08SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74AC08SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC08PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT08SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body
74ACT08MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT08PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code. (PC not available in Tape and Reel.)

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A _n , B _n	Inputs
O _n	Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Absolute Maximum Ratings(Note 1)

 $\begin{array}{c} \text{V}_{I} = -0.5 \text{V} & -20 \text{ mA} \\ \text{V}_{I} = \text{V}_{CC} + 0.5 \text{V} & +20 \text{ mA} \\ \text{DC Input Voltage (V}_{I}) & -0.5 \text{V to V}_{CC} + 0.5 \text{V} \\ \text{DC Output Diode Current (I}_{OK}) & \end{array}$

 $V_{O} = -0.5V$ -20 mA $V_{O} = V_{CC} + 0.5V$ +20 mA

DC Output Voltage (V_O) $-0.5V \text{ to V}_{CC} + 0.5V$

DC Output Source

or Sink Current (I_O) $\pm 50 \text{ mA}$

DC V_{CC} or Ground Current

per Output Pin (I_{CC} or I_{GND}) ± 50 mA Storage Temperature (T_{STG}) $-65^{\circ}\mathrm{C}$ to $+150^{\circ}\mathrm{C}$

Junction Temperature (T_J)

PDIP 140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})

AC 2.0V to 6.0V

ACT 4.5V to 5.5V

Input Voltage (V₁) 0V to V_{CC}

Minimum Input Edge Rate (ΔV/Δt)

AC Devices

 $V_{\mbox{\footnotesize{IN}}}$ from 30% to 70% of $V_{\mbox{\footnotesize{CC}}}$

 $V_{CC} @ 3.3V, 4.5V, 5.5V$ 125 mV/ns

Minimum Input Edge Rate ($\Delta V/\Delta t$)

ACT Devices

 V_{IN} from 0.8V to 2.0V

V_{CC} @ 4.5V, 5.5V 125 mV

140°C Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V _{CC}	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
Symbol		(V)	Тур	Gu	aranteed Limits	Oilles	Conditions	
V _{IH}	Minimum HIGH Level	3.0	1.5	2.1	2.1		V _{OUT} = 0.1V	
	Input Voltage	4.5	2.25	3.15	3.15	V	or V _{CC} – 0.1V	
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum LOW Level	3.0	1.5	0.9	0.9		V _{OUT} = 0.1V	
	Input Voltage	4.5	2.25	1.35	1.35	V	or V _{CC} – 0.1V	
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum HIGH Level	3.0	2.99	2.9	2.9			
	Output Voltage	4.5	4.49	4.4	4.4	V	$I_{OUT} = -50 \mu A$	
		5.5	5.49	5.4	5.4			
							$V_{IN} = V_{IL}$ or V_{IH}	
		3.0		2.56	2.46		$I_{OH} = -12 \text{ mA}$	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76		I _{OH} = -24 mA (Note 2)	
V _{OL}	Maximum LOW Level	3.0	0.002	0.1	0.1			
	Output Voltage	4.5	0.001	0.1	0.1	V	$I_{OUT} = 50 \mu A$	
		5.5	0.001	0.1	0.1			
							$V_{IN} = V_{IL}$ or V_{IH}	
		3.0		0.36	0.44		$I_{OL} = 12 \text{ mA}$	
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$	
		5.5		0.36	0.44		I _{OL} = 24 mA (Note 2)	
I _{IN}	Maximum Input	5.5		±0.1	±1.0	μА	$V_1 = V_{CC}$, GND	
(Note 4)	Leakage Current	5.5		±0.1	11.0	μΛ	VI = VCC, GIVD	
I _{OLD}	Minimum Dynamic	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	Output Current (Note 3)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent	5.5		2.0	20.0	μА	$V_{IN} = V_{CC}$	
(Note 4)	Supply Current	5.5		2.0	20.0	μΛ	or GND	

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{IN} and $I_{\text{CC}} @ 3.0 \text{V}$ are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC} .

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC}	$T_A = +25^{\circ}C$		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	Units	Conditions	
Oyinboi		(V)	Тур	Gu	aranteed Limits	Oiiiis	Conditions	
V _{IH}	Minimum HIGH Level	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1V	
	Input Voltage	5.5	1.5	2.0	2.0	v	or V _{CC} – 0.1V	
V _{IL}	Maximum LOW Level	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1V	
	Input Voltage	5.5	1.5	0.8	0.8	· ·	or V _{CC} – 0.1V	
V _{OH}	Minimum HIGH Level	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
	Output Voltage	5.5	5.49	5.4	5.4	· ·	1007 = -30 μΑ	
							$V_{IN} = V_{IL}$ or V_{IH}	
		4.5		3.86	3.76	V	$I_{OH} = -24 \text{ mA}$	
		5.5		4.86	4.76	· ·	$I_{OH} = -24 \text{ mA (Note 5)}$	
V _{OL}	Maximum LOW Level	4.5	0.001	0.1	0.1	V	I 50 A	
	Output Voltage	5.5	0.001	0.1	0.1	· ·	I _{OUT} = 50 μA	
							$V_{IN} = V_{IL}$ or V_{IH}	
		4.5		0.36	0.44	V	$I_{OL} = 24 \text{ mA}$	
		5.5		0.36	0.44	•	I _{OL} = 24 mA (Note 5)	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}$, GND	
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5	mA	$V_I = V_{CC} - 2.1V$	
I _{OLD}	Minimum Dynamic Output Current	5.5			75	mA	V _{OLD} = 1.65V Max	
I _{OHD}	(Note 6)	5.5			-75	mA	V _{OHD} = 3.85V Min	
I _{CC}	Maximum Quiescent	5.5		4.0	40.0	μА	$V_{IN} = V_{CC}$	
	Supply Current	5.5		4.0	40.0	μΛ	or GND	

Note 5: All outputs loaded; thresholds on input associated with output under test.

AC Electrical Characteristics for AC

Symbol Parameter		V _{CC} (V)	$T_A = +25^{\circ}C$ $C_L = 50 \text{ pF}$		$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$		Units	
		(Note 7)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	3.3	1.5	7.5	9.5	1.0	10.0	ns
		5.0	1.5	5.5	7.5	1.0	8.5	115
t _{PHL}	Propagation Delay	3.3	1.5	7.0	8.5	1.0	9.0	ns
		5.0	1.5	5.5	7.0	1.0	7.5	115

Note 7: Voltage Range 3.3 is 3.3V ± 0.3V Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)				$T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $C_L = 50 \text{ pF}$		Units
		(Note 8)	Min	Тур	Max	Min	Max	
t _{PLH}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns
t _{PHL}	Propagation Delay	5.0	1.0	6.5	9.0	1.0	10.0	ns

Note 8: Voltage Range 5.0 is $5.0V \pm 0.5V$

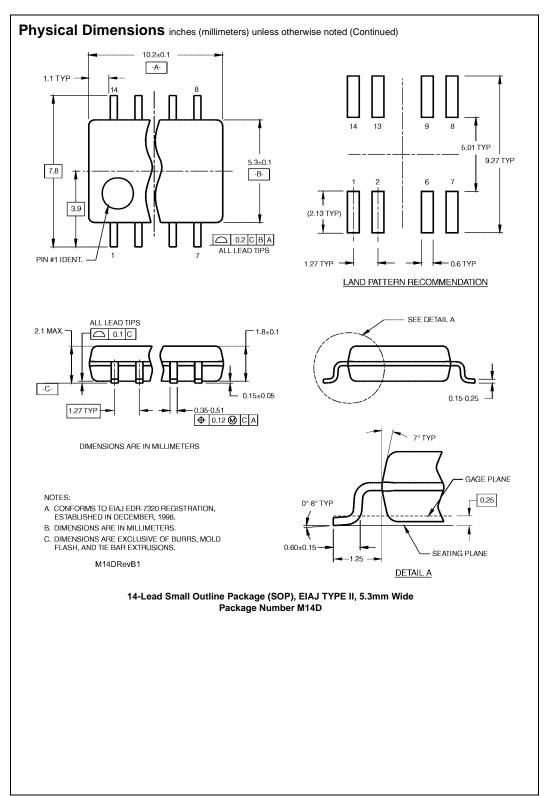
Capacitance

Symbol	Parameter	Тур	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	20.0	pF	V _{CC} = 5.0V

Note 6: Maximum test duration 2.0 ms, one output loaded at a time.

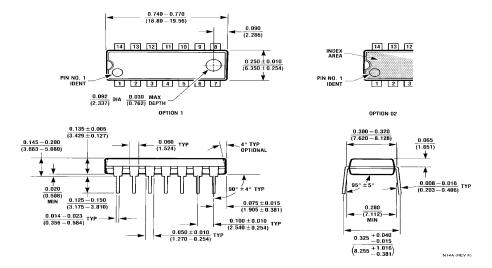
Physical Dimensions inches (millimeters) unless otherwise noted $\frac{0.335 - 0.344}{(8.509 - 8.738)}$ LEAD NO. 1 IDENT $\frac{0.150 - 0.157}{(3.810 - 3.988)}$ $\frac{0.053 - 0.069}{(1.346 - 1.753)}$ $\frac{0.010 - 0.020}{(0.254 - 0.508)}$ 8° MAX TYP ALL LEADS $\frac{0.004 - 0.010}{(0.102 - 0.254)}$ 0.014 0.008 - 0.010 (0.203 - 0.254) TYP ALL LEADS 0.050 (1.270) TYP $\frac{0.014 - 0.020}{(0.356 - 0.508)} \text{ TYP}$ 0.016 - 0.050 (0.406 - 1.270) TYP ALL LEADS 0.004 (0.102) ALL LEAD TIPS 0.008 (0.203) TYP M14A (REV h)

14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow Body Package Number M14A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 5.0±0.1 0.43 TYP -A-7.72 4.16 6.4 4.4±0.1 -B-3.2 0.2 C B A 0.65 ALL LEAD TIPS LAND PATTERN RECOMMENDATION PIN #1 IDENT. - SEE DETAIL A ALL LEAD TIPS 1.2 MAX ⊏ 0.90 ^{+0.15} 0.09-0.20 -C-L _{0.10±0.05} 0.65 0.19 - 0.30 **⊕** 0.13 **M** A B **C** -12.00° TOP & BOTTOM R0.09 MIN GAGE PLANE NOTES: 0.25 A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93. B. DIMENSIONS ARE IN MILLIMETERS. C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS. SEATING PLANE D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982. R0.09 MIN MTC14RevC3 DETAIL A 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N14A

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