VN5T006ASP-E

Single-channel high-side driver with analog current sense for 24 V automotive applications

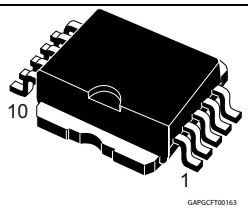
Datasheet – production data

Features

Max transient supply voltage	V_{CC}	58 V
Operating voltage range	V_{CC}	8 V to 36 V
Typ on-state resistance	R_{ON}	6 mΩ
Current limitation (typ)	I_{LIM}	115 A
Off-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected.

- General
  - Very low standby current
  - 3 V CMOS compatible input
  - Optimized electromagnetic emission
  - Very low electromagnetic susceptibility
  - Compliance with 2002/95/EC European directive
  - Fault reset standby pin (FR_Stby)
- Diagnostic functions
  - Proportional load current sense
  - Current sense precision for wide range currents
  - Off-state open-load detection
  - Output short to V_{CC} detection
  - Overload and short to ground latch-off
  - Thermal shutdown latch-off
  - Very low current sense leakage
- Protections
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Thermal shutdown
  - Reverse battery protected with self switch of the PowerMOS
  - Electrostatic discharge protection



PowerSO-10

Application

- All types of resistive, inductive and capacitive loads

Description

The VN5T006ASP-E is a device made using STMicroelectronics® VIPower®VN5T006ASP-E technology, intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes.

This device integrates an analog current sense which delivers a current proportional to the load current. Fault conditions such as overload, overtemperature or short to V_{CC} are reported via the current sense pin.

Output current limitation protects the device in overload condition. The device latches off in case of overload or thermal shutdown.

The device is reset by a low-level pass on the fault reset standby pin.

A permanent low level on the inputs and fault reset standby pin disables all outputs and sets the device in standby mode.

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Figure 1. Block diagram

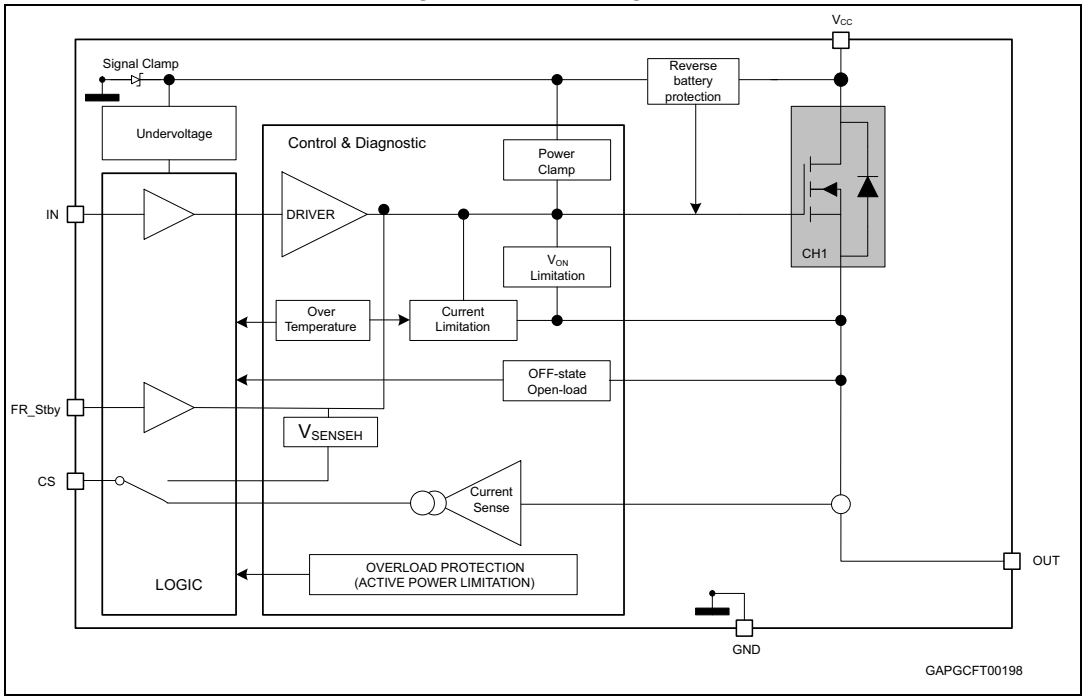


Table 1. Pin function

Name	Function
V_{CC}	Battery connection.
OUT	Power output.
GND	Ground connection.
IN	Voltage controlled input pin with hysteresis, CMOS compatible; it controls output switch state.
CS	Analog current sense pin; it delivers a current proportional to the load current.
FR_Stby	In case of latch-off for overtemperature /overcurrent condition, a low pulse on the FR_Stby pin is needed to reset the channel. The device enters in standby mode if all inputs and the FR_Stby pin are low.

Figure 2. Configuration diagram (top view)

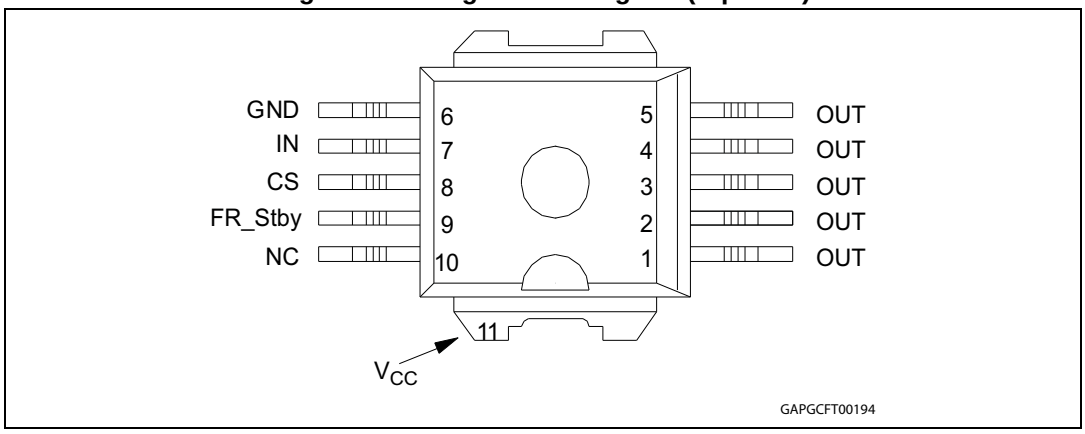


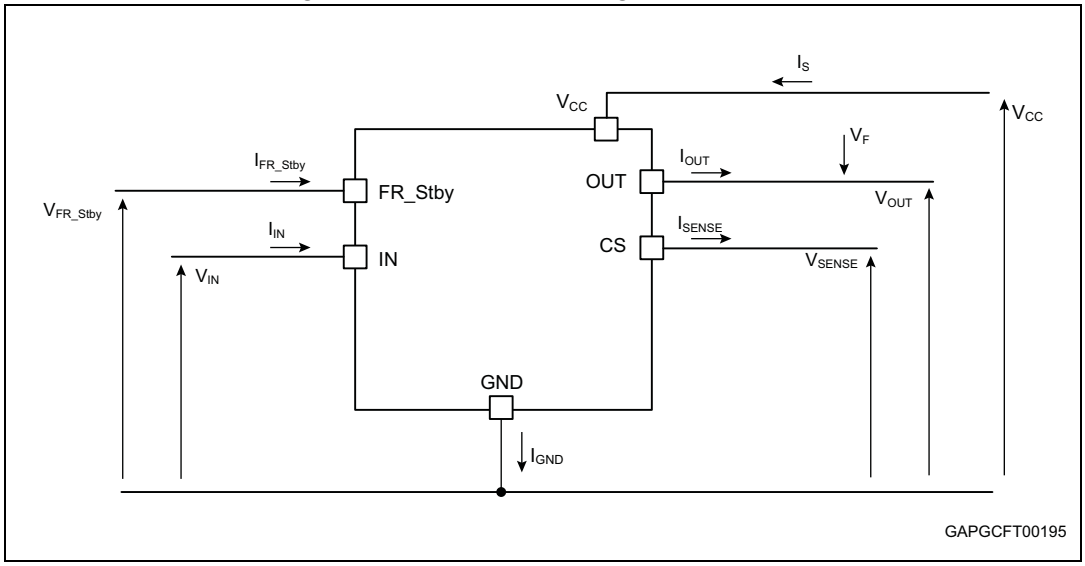
Table 2. Suggested connections for unused and not connected pins

Connection / pin	CS	N.C.	OUT	IN	FR_Stby
Floating	Not allowed	X(1)	X	X	X
To ground	Through 10 KΩ resistor	X	Not allowed	Through 10 KΩ resistor	Through 10 KΩ resistor

1. X: do not care.

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the ratings listed in *Table 3* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to the conditions reported in this section for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	58	V
$-V_{CC}$	Reverse DC supply voltage	-32	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	90	A
I_{IN}	DC input current	-1 to 10	mA
I_{FR_Stby}	Fault reset standby DC input current	-1 to 1.5	mA
V_{CSENSE}	Current sense maximum voltage	V_{CC} - 58 to +V_{CC}	V
E_{MAX}	Maximum switching energy (L = 10 mH; V_{bat} = 32 V; T_{jstart} = 150°C; I_{OUT} = 8.9 A)	880	mJ
L_{SMAX}	Maximum stray inductance in short circuit condition V_{bat} = 32 V; R_L = 300 mΩ; T_{jstart} = 150°C; I_{OUT} = I_{limH_max}	40	µH

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 KΩ; C = 100 pF) – IN – CS – FR_Stby – OUT – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case (max.) (with one channel on)	0.8	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient (max.)	See *Figure 27*	°C/W

2.3 Electrical characteristics

8 V < V_{CC} < 36 V; -40°C < T_j < 150°C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		8	24	36	V
V_{USD}	Undervoltage shutdown			3.5	5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	On-state resistance(2)	I_{OUT} = 10 A; T_j = 25°C; 8 V < V_{CC} < 36 V		6		mΩ
		I_{OUT} = 10 A; T_j = 150°C; 8 V < V_{CC} < 36 V			12	
$R_{ON\ REV}$	Reverse battery on-state resistance	V_{CC} = -24 V; I_{OUT} = -10 A; T_j = 25°C			6	mΩ
V_{clamp}	Clamp voltage	I_S = 20 mA	58	64	70	V
I_S	Supply current	Off-state: V_{CC} = 24 V; T_j = 25°C; V_{IN} = V_{OUT} = V_{SENSE} = 0 V		2(1)	5	µA
		On-state: V_{CC} = 24 V; V_{IN} = 5 V; I_{OUT} = 0 A		3	6	mA
$I_{L(off1)}$	Off-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 24 V; T_j = 25°C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 24 V; T_j = 125°C	0		5	

1. PowerMOS leakage included.

Table 6. Switching (V_{CC} = 24 V; T_j = 25°C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 2.4 Ω	—	32	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 2.4 Ω	—	67	—	µs
$dV_{OUT}/dt_{(on)}$	Turn-on voltage slope	R_L = 2.4 Ω		0.7		V/µs
$dV_{OUT}/dt_{(off)}$	Turn-off voltage slope	R_L = 2.4 Ω		0.46		V/µs
W_{ON}	Switching energy losses during t_{won}	R_L = 2.4 Ω	—	4.15	—	mJ
W_{OFF}	Switching energy losses during t_{woff}	R_L = 2.4 Ω	—	2.7	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
$V_{FR\_Stby\_L}$	Low-level fault-reset-standby voltage				0.9	V
$I_{FR\_Stby\_L}$	Low-level fault-reset-standby current	V_{FR_Stby} = 0.9 V	1			µA
$V_{FR\_Stby\_H}$	High-level fault-reset-standby voltage		2.1			V
$I_{FR\_Stby\_H}$	High-level fault-reset-standby current	V_{FR_Stby} = 2.1 V			10	µA
V_{FR_Stby} (hyst)	Fault-reset-standby hysteresis voltage		0.25			V
$V_{FR\_Stby\_CL}$	Fault-reset-standby clamp voltage	I_{FR_Stby} = 15 mA (10 ms)	11		15	V
		I_{FR_Stby} = -1 mA		-0.7		
t_{reset}	Overload latch-off reset time	See *Figure 4*	2		24	µs
t_{stby}	Standby delay	See *Figure 5*	120		1200	µs

Figure 4. T_{reset} definition

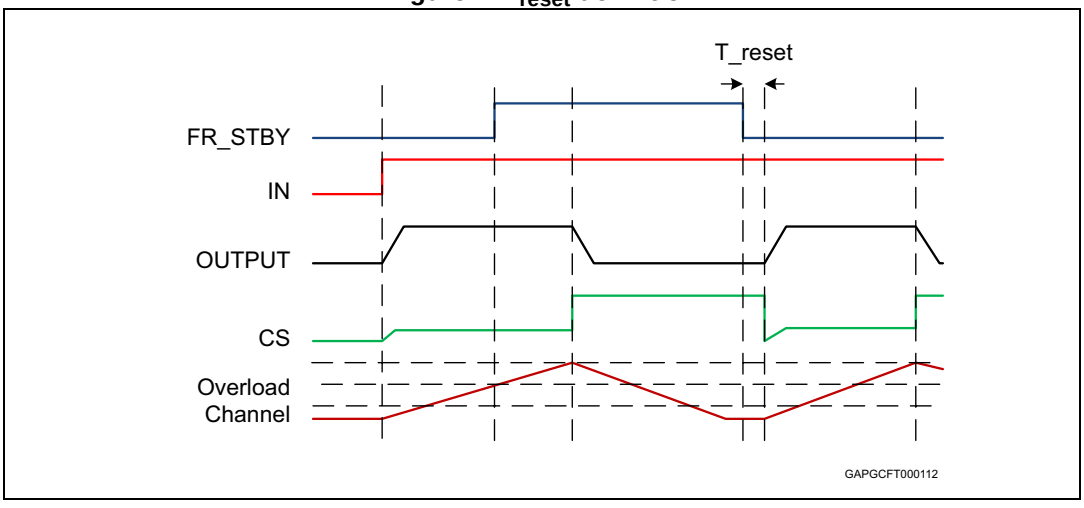


Figure 5. T_{stby} definition

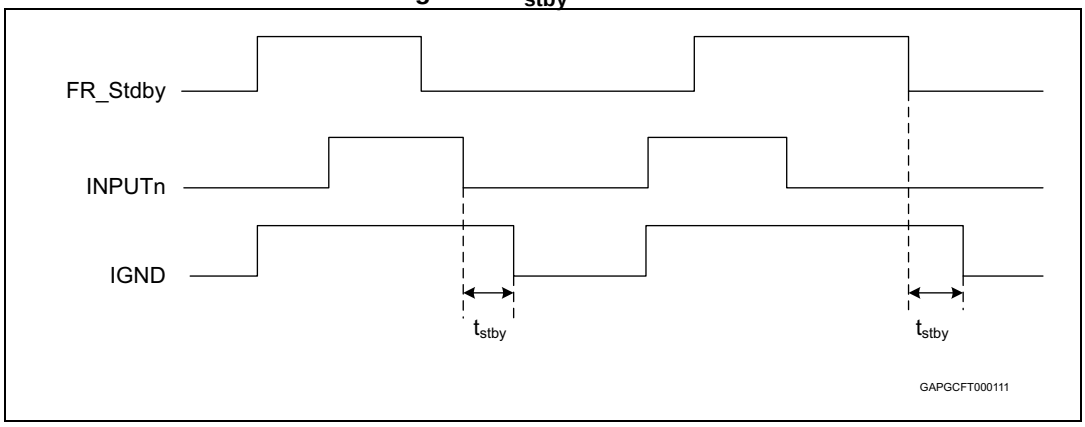


Table 8. Protections and diagnostics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	DC short-circuit current	V_{CC} = 24 V	81	115	162	A
		5 V < V_{CC} < 36 V			162	A
I_{limL}	Short-circuit current during thermal cycling	V_{CC} = 24 V; T_R < T_j < T_{TSD}		29		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 10 A; V_{IN} = 0 V; L = 6 mH	V_{CC} - 58	V_{CC} - 64	V_{CC} - 70	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 1 A; T_j = -40°C to 150°C		25		mV

Table 9. Current sense (8 V < V_{CC} < 36 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.6 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C T_j = 25°C to 150°C	3930 5035	11250	19850 17055	
dK_0/K_0(1)	Current sense ratio drift	I_{OUT} = 0.6 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	-30		30	%
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 1.6 A; V_{SENSE} = 1 V; T_j = -40°C to 150°C; T_j = 25°C to 150°C	5600 6215	10750	16940 14660	
dK_1/K_1(1)	Current sense ratio drift	I_{OUT} = 1.6 A; V_{SENSE} = 1 V; T_j = -40°C to 150°C	-28		25	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 2.4 A; V_{SENSE} = 1 V; T_j = -40°C to 150°C T_j = 25°C to 150°C	6030 6200	10370	15865 13635	
dK_2/K_2(1)	Current sense ratio drift	I_{OUT} = 2.4 A; V_{SENSE} = 1 V; T_j = -40°C to 150°C	-26		23	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 3 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C T_j = 25°C to 150°C	6040 6040	10070	15285 13090	
dK_3/K_3(1)	Current sense ratio drift	I_{OUT} = 3 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C	-25		22	%
K_4	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C T_j = 25°C to 150°C	5845 6000	8670	13630 10895	
dK_4/K_4(1)	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	-20		20	%
K_5	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C T_j = 25°C to 150°C	5920 6730	8400	11520 9765	
dK_5/K_5(1)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	-15		15	%
K_6	I_{OUT}/I_{SENSE}	I_{OUT} = 20 A; V_{SENSE} = 4 V; T_j = -40°C to 150°C	6960	8330	10090	
dK_6/K_6(1)	Current sense ratio drift	I_{OUT} = 3 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C	-8		8	%
dK/K_{BULB1}(1)	Current sense ratio drift	I_{OUT} = 0.6 A to 6 A; I_{CAL} = 3 A; V_{SENSE} = 0.5 V; T_j = -40°C to 150°C	-30		50	%
dK/K_{BULB2}(1)	Current sense ratio drift	I_{OUT} = 1.6 A to 4.2 A; I_{OUTCAL} = 3 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C	-30		26	%
dK/K_{BULB3}(1)	Current sense ratio drift	I_{OUT} = 0.6 A to 2.4 A; I_{OUTCAL} = 1.6 A; V_{SENSE} = 2 V; T_j = -40°C to 150°C	-27		25	%

Table 9. Current sense (8 V < V_{CC} < 36 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{IN} = 0 V; T_j = -40°C to 150°C	0		1	µA
		I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{IN} = 5 V; T_j = -40°C to 150°C	0		2	
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 40 A; R_{SENSE} = 3.9 KΩ	5			V
V_{SENSEH}	Analog sense output voltage in fault condition(2)	V_{CC} = 24 V; R_{SENSE} = 3.9 KΩ		8		V
I_{SENSEH}	Analog sense output current in fault condition (2)	V_{CC} = 24 V; V_{SENSE} = 5 V		9	12	mA
$t_{DSENSE2H}$	Delay response time from rising edge of IN pin	V_{SENSE} < 4 V; 1 A < I_{OUT} < 40 A; I_{SENSE} = 90% of $I_{SENSEMAX}$ (see *Figure 7*)		300	600	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4 V; I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} I_{OUTMAX} = 10 A (see *Figure 10*)			450	µs
$t_{DSENSE2L}$	Delay response time from falling edge of IN pin	V_{SENSE} < 4 V; 1 A < I_{OUT} < 40 A; I_{SENSE} = 10 % of $I_{SENSEMAX}$ (see *Figure 7*)		5	20	µs

1. Parameter guaranteed by design; it is not tested.
2. Fault condition includes: power limitation, overtemperature and open-load in OFF-state condition.

Table 10. Open-load detection (FR_Stby = 5 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load Off-state voltage detection threshold	V_{IN} = 0 V; 8 V < V_{CC} < 36 V	2		4	V
t_{DSTKON}	Output short-circuit to V_{CC} detection delay at turn-off	See *Figure 8*	180		1800	µs
$I_{L(off2)}$	Off-state output current at V_{OUT} = 4 V	V_{IN} = 0 V; V_{SENSE} = 0 V; V_{OUT} rising from 0 V to 4 V	-120		0	µA

Table 10. Open-load detection (FR_Stby = 5 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{OUT} = 4 V; V_{IN} = 0 V; V_{SENSE} = 90% of V_{SENSEH}			20	µs
t_{DFRSTK_ON}	Output short circuit to V_{CC} detection delay at FR_{STBY} activation	See *Figure 6*; $Input_{1,2}$ = low			50	µs

Figure 6. Output stuck to V_{CC} detection delay time at FR_{STBY} activation

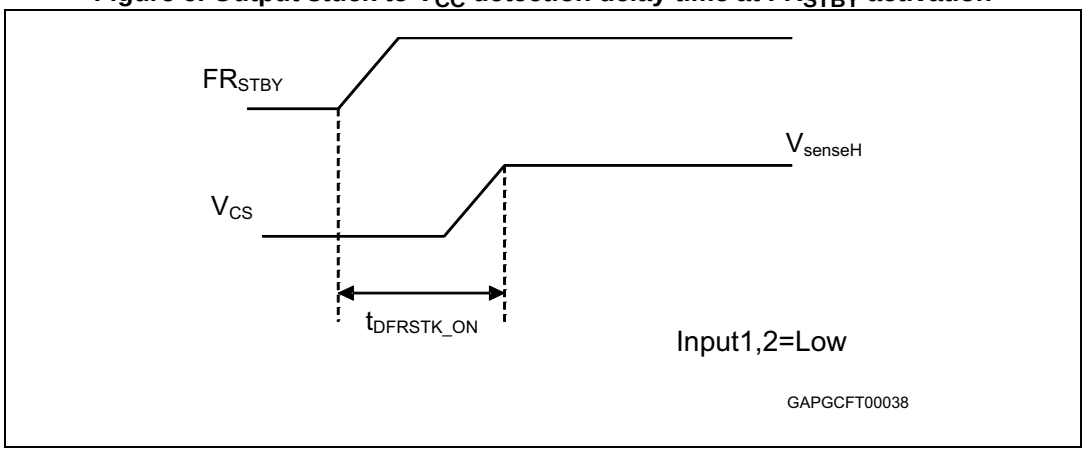


Figure 7. Current sense delay characteristics

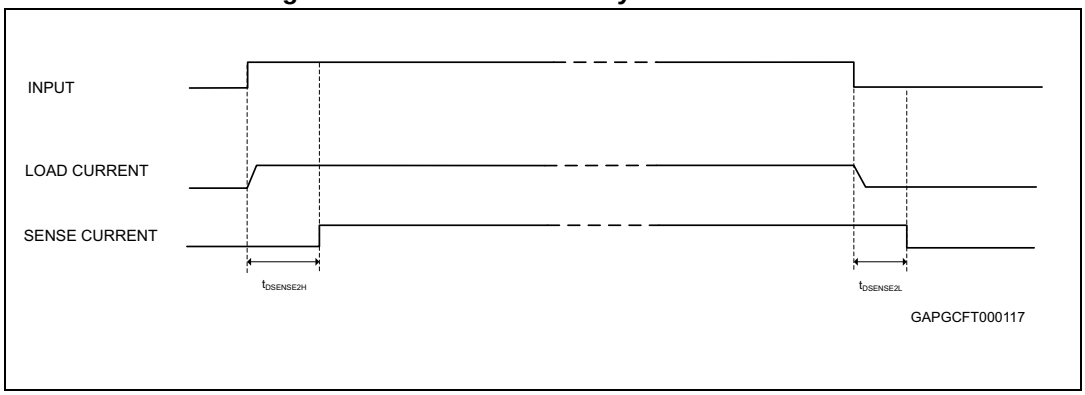


Figure 8. Open-load off-state delay timing

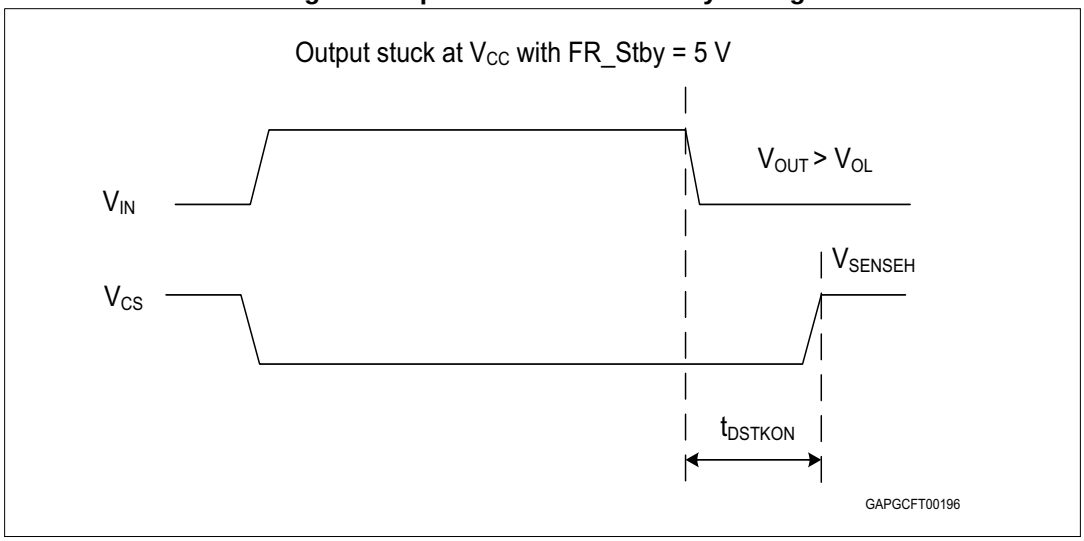


Figure 9. Switching characteristics

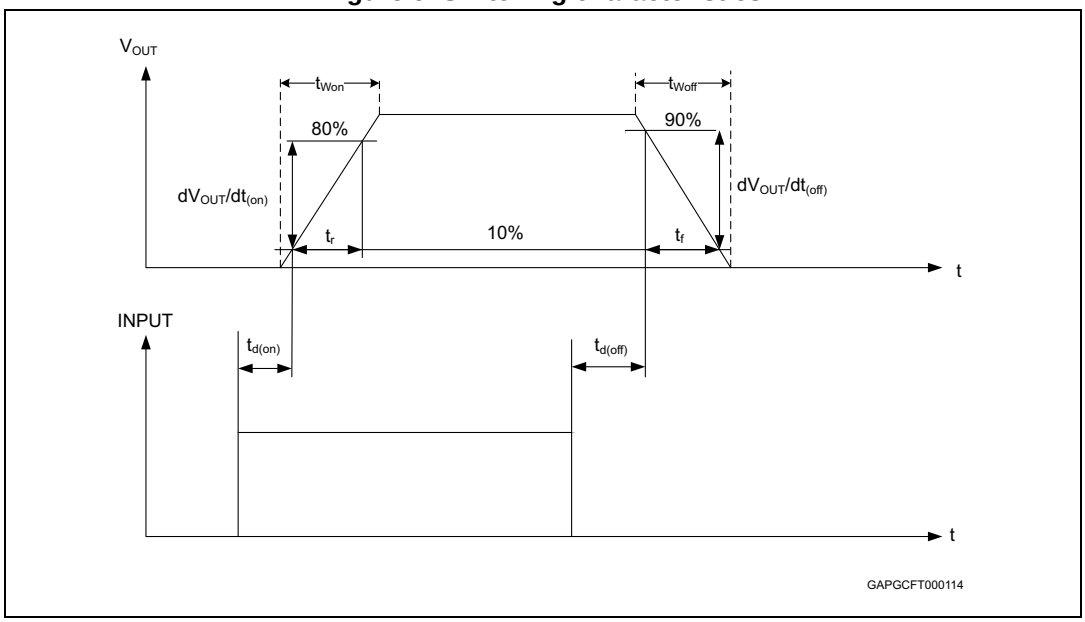


Figure 10. Delay response time between rising edge of output current and rising edge of current sense

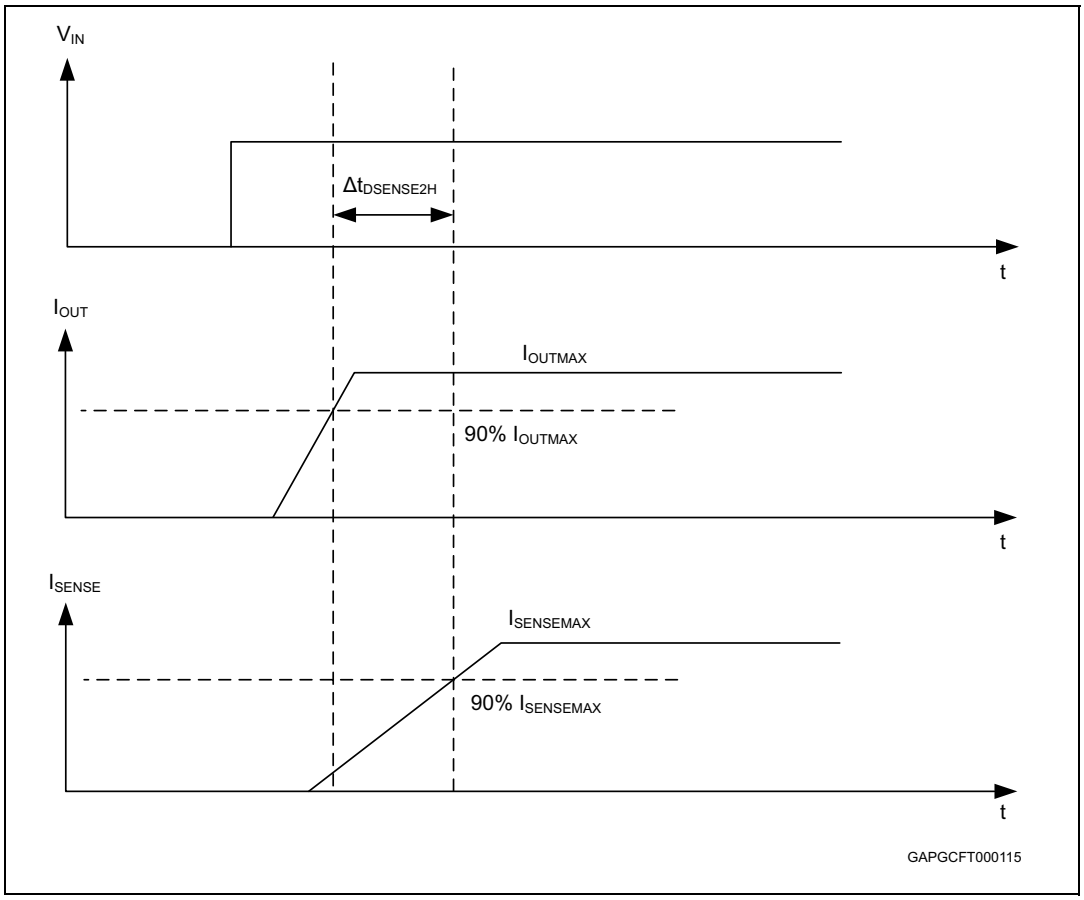


Figure 11. Output voltage drop limitation

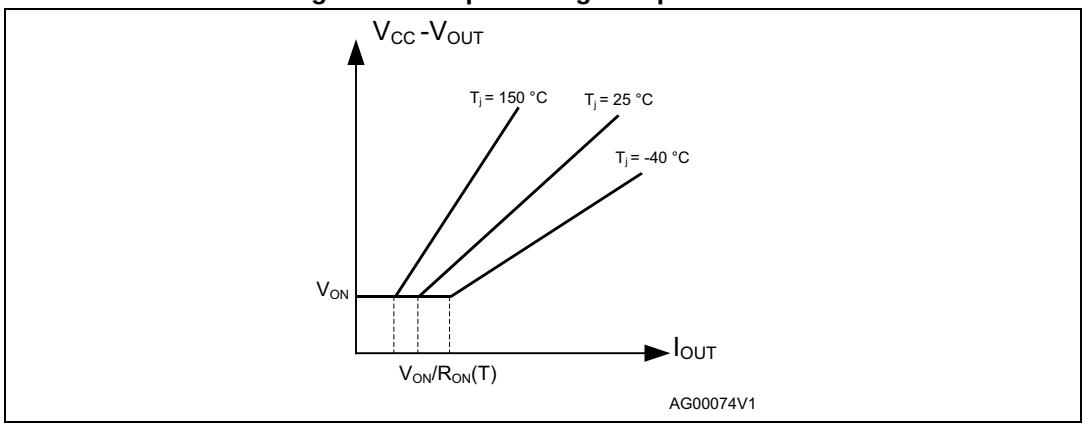
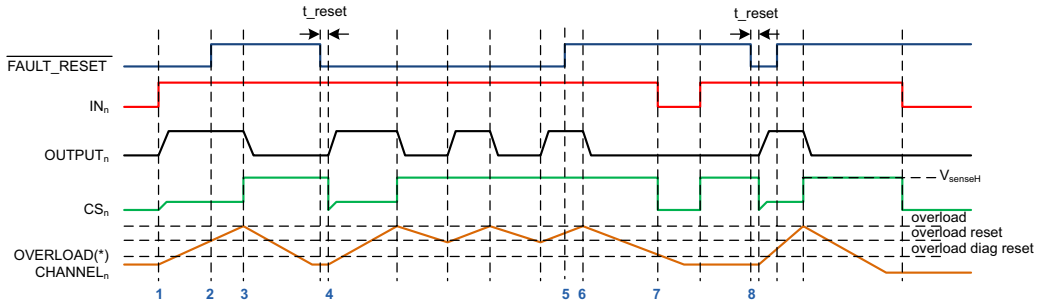


Figure 12. Device behavior in overload condition



1: $OUTPUT_n$ and CS_n controlled by INn
2: FAULT_RESET from '0' to '1' → no action on CS_n pin
3: overload latch-off. Inn high → CS_n high
4: FAULT_RESET low AND Temp channeln < overload_reset → overload latch reset after t_reset
4 to 5: FAULT_RESET low AND IN_n high → thermal cycling, CS_n high
5: FAULT_RESET high → latch-off reset disabled
6 to 7: overload event and FAULT_RESET high → latch-off, no thermal cycling
7 to 8: overload diagnostic disabled/enabled by the input
8: overload latch-off reset by FAULT_RESET

(*) OVERLOAD = thermal shutdown OR power limitation

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Table 11. Truth table

Conditions	Fault reset standby	Input	Output	Sense
Standby	L	L	X	0
Normal operation	X X	L H	L H	0 Nominal
Overload	X X	L H	L H	0 > Nominal
Overtemperature / short to ground	X L H	L H H	L Cycling Latched	0 V_{SENSEH} V_{SENSEH}
Undervoltage	X	X	L	0
Short to V_{BAT}	L H X	L L H	H H H	0 V_{SENSEH} < Nominal
Open-load Off-state (with pull-up)	L H X	L L H	H H H	0 V_{SENSEH} 0
Negative output voltage clamp	X	L	Negative	0

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels(1)		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and impedance
	III	IV				
1	- 450 V	- 600 V	5000 pulses	0.5 s	5 s	1 ms, 50 Ω
2a	+ 37 V	+ 50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	- 150 V	- 200 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+ 150 V	+ 200 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	- 12 V	- 16 V	1 pulse			100 ms, 0.01 Ω
5b(2)	+ 123 V	+ 174 V	1 pulse			350 ms, 1 Ω

1. The above test levels must be considered referred to V_{CC} = 24.5V except for pulse 5b
2. Valid in case of external load dump clamp: 58V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results	
	III	IV
1	C	C(1)
2a	C	C
3a	C	C
3b(2)	E	E
3b(3)	C	C
4	C	C
5b(4)	C	C

1. With R_{LOAD} < 24 Ω.
2. Without capacitor between V_{CC} and GND.
3. With 10 nF between V_{CC} and GND.
4. External load dump clamp: 58 V maximum, referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Electrical characteristics curves

Figure 13. Off-state output current

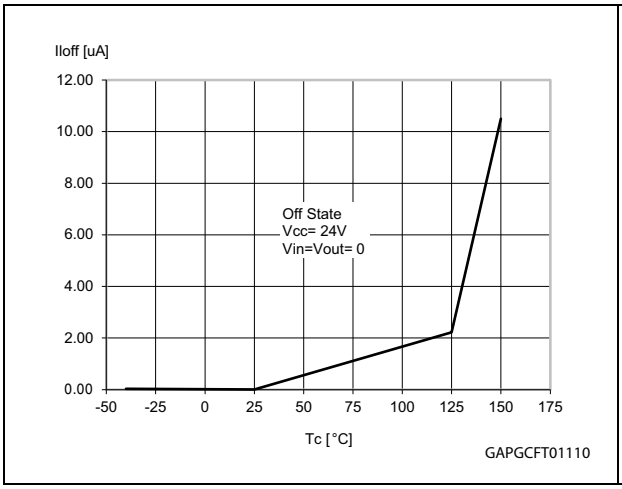


Figure 14. High level input current

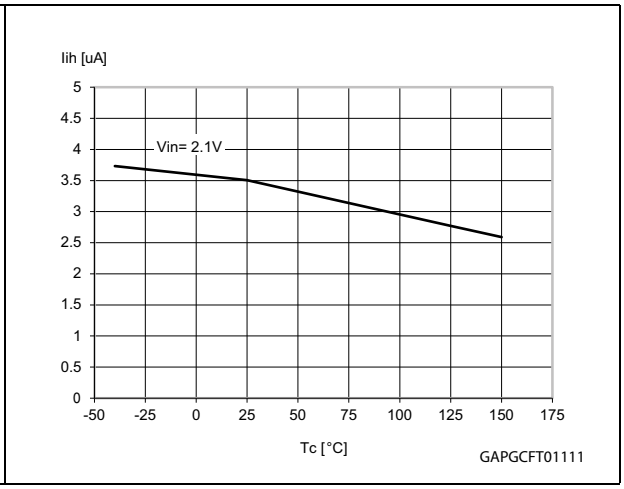


Figure 15. Input clamp voltage

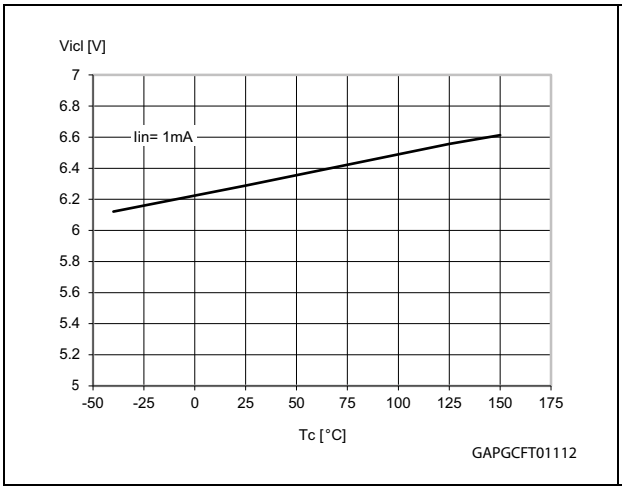


Figure 16. Input low level voltage

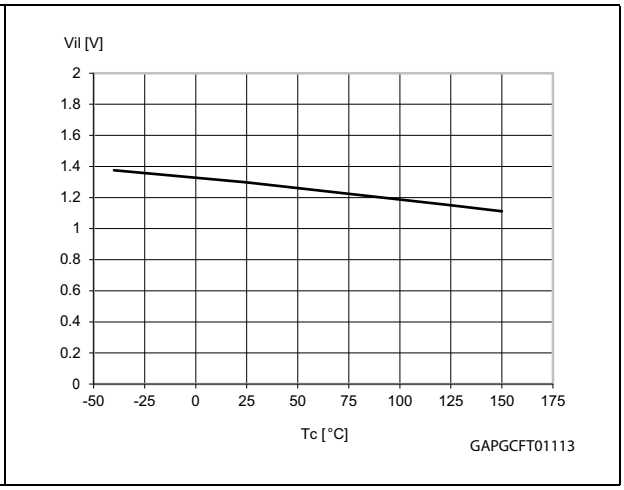


Figure 17. Input high level voltage

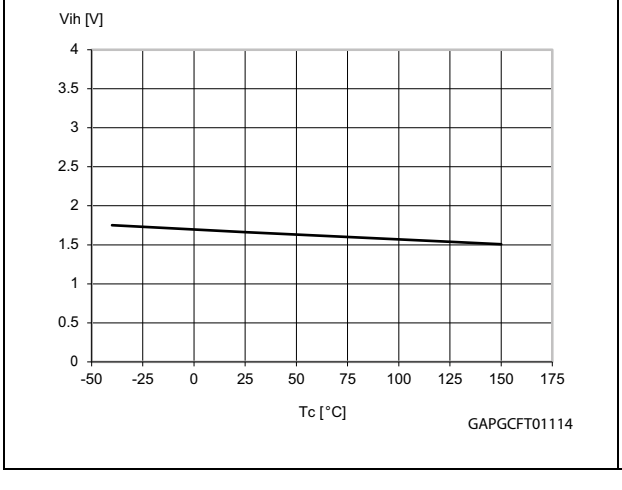


Figure 18. Input hysteresis voltage

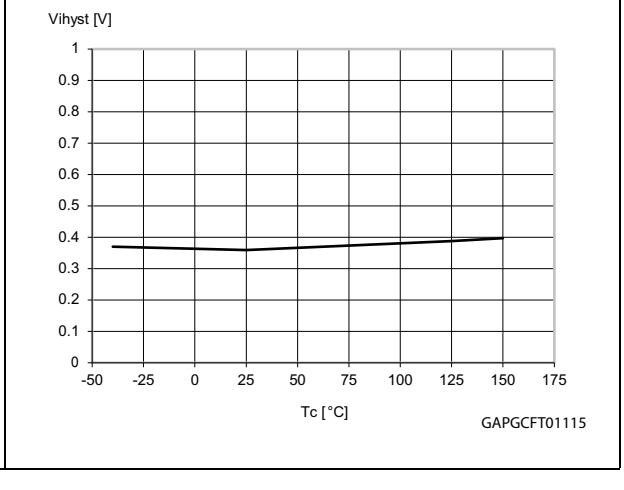


Figure 19. On state resistance vs T_{case}

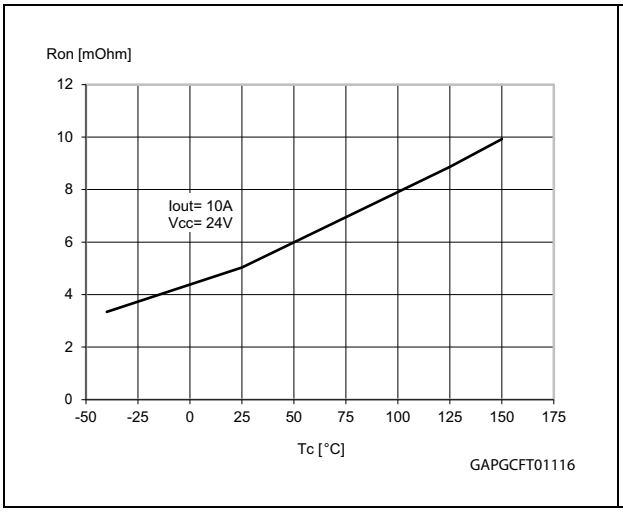


Figure 20. On state resistance vs V_{CC}

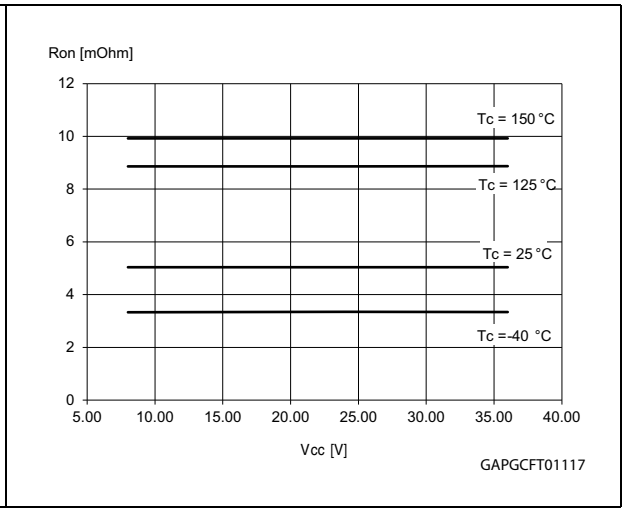


Figure 21. I_{LIMH} vs T_{case}

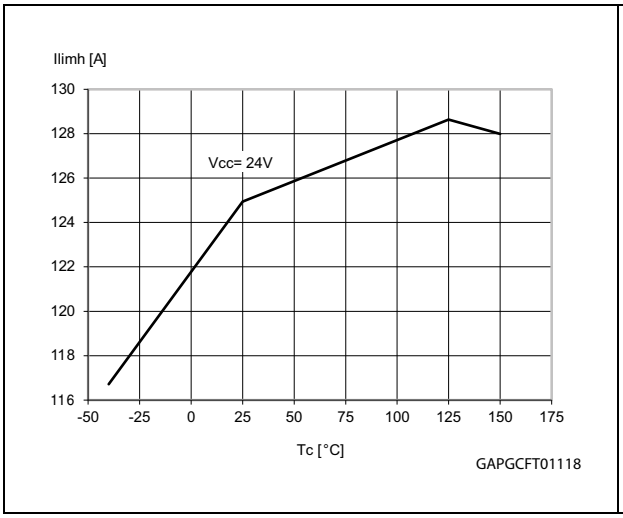


Figure 22. Turn-On voltage slope

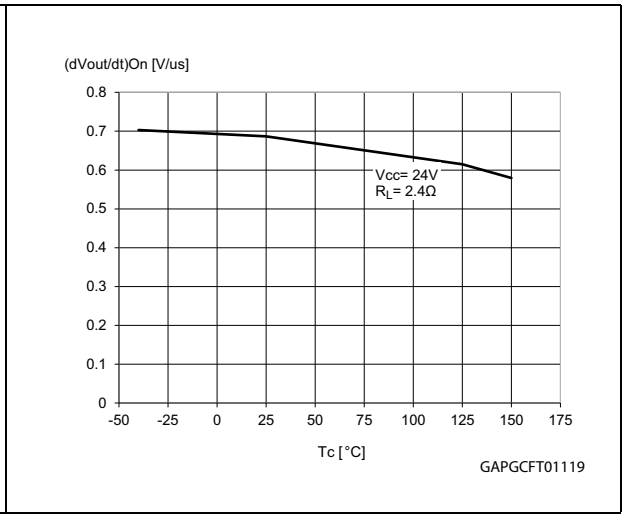
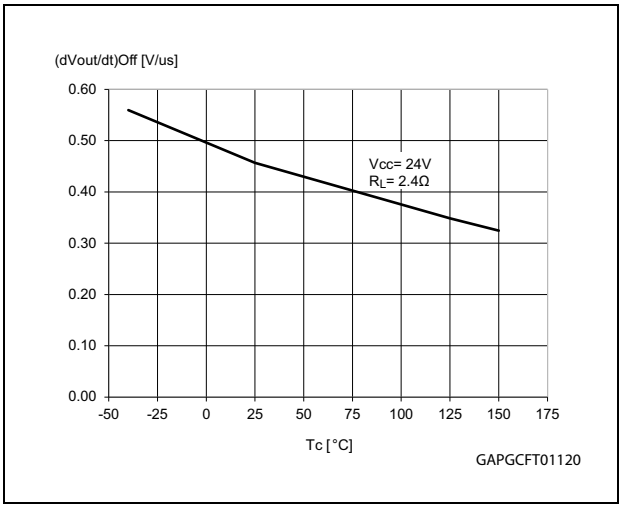
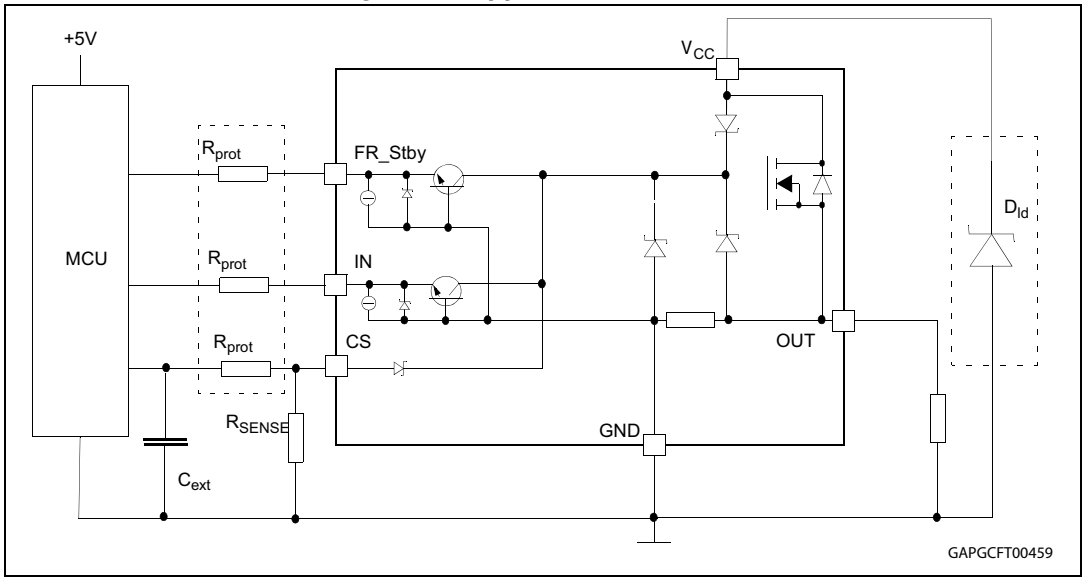


Figure 23. Turn-Off voltage slope



3 Application information

Figure 24. Application schematic



3.1 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2 2004 (E) table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins is pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/O pins from latching-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$-V_{CCpeak} / I_{latchup} \leq R_{prot} \leq (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

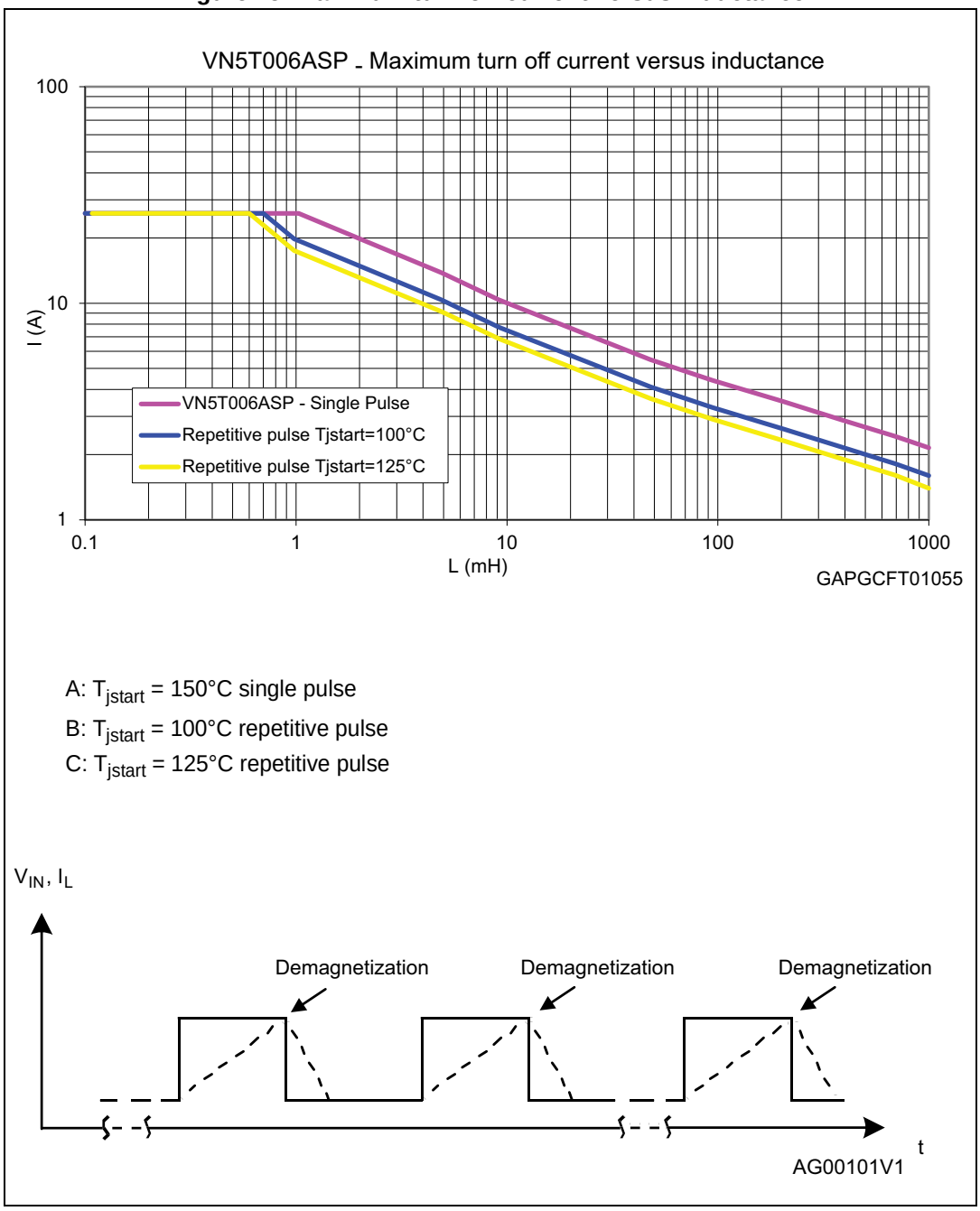
For V_{CCpeak} = -600 V and $I_{latchup} \geq$ 20 mA; $V_{OH\mu C} \geq$ 4.5 V

30 KΩ ≤ R_{prot} ≤ 190 kΩ.

Recommended value: R_{prot} = 56 kΩ

3.3 Maximum demagnetization energy (V_{CC} = 24 V)

Figure 25. Maximum turn-off current versus inductance

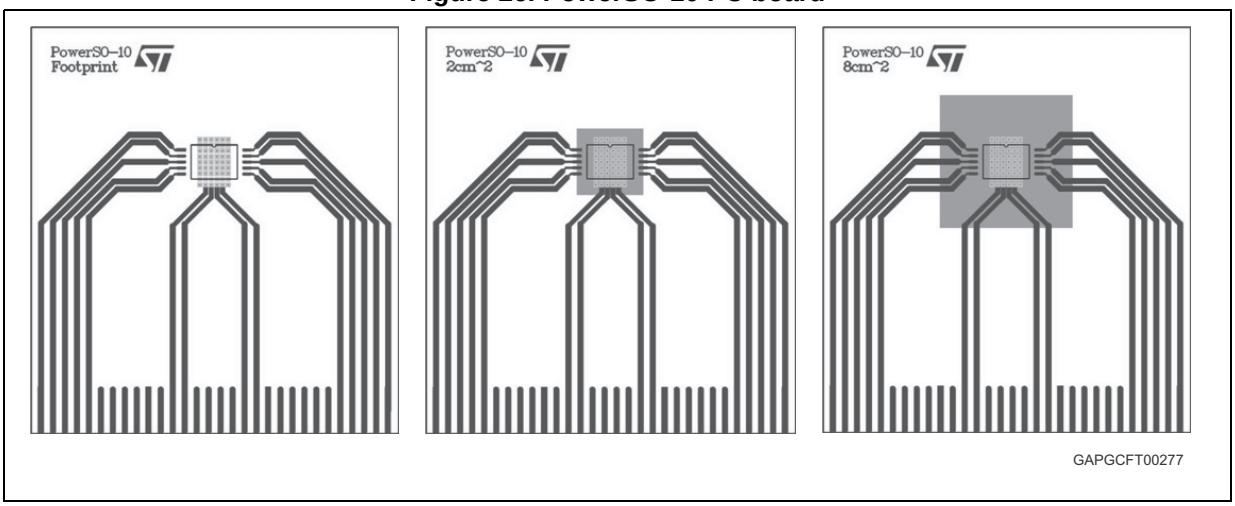


Note: Values are generated with R_L = 0 Ω
In case of repetitive pulses, T_{jstart} (at the beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PCB thermal data

4.1 PowerSO-10 thermal data

Figure 26. PowerSO-10 PC board



1. Layout condition of R_{th} and Z_{th} measurements (Board finish thickness 1.6 mm +/- 10%; Board double layer; Board dimension 77 x 86; Board Material FR4; Cu thickness 0.070 mm (front and back side); Thermal vias separation 1.2 mm; Thermal via diameter 0.3 mm +/- 0.08 mm; Cu thickness on vias 0.025 mm).

Figure 27. $R_{thj\text{-}amb}$ vs PCB copper area in open box free air condition (one channel on)

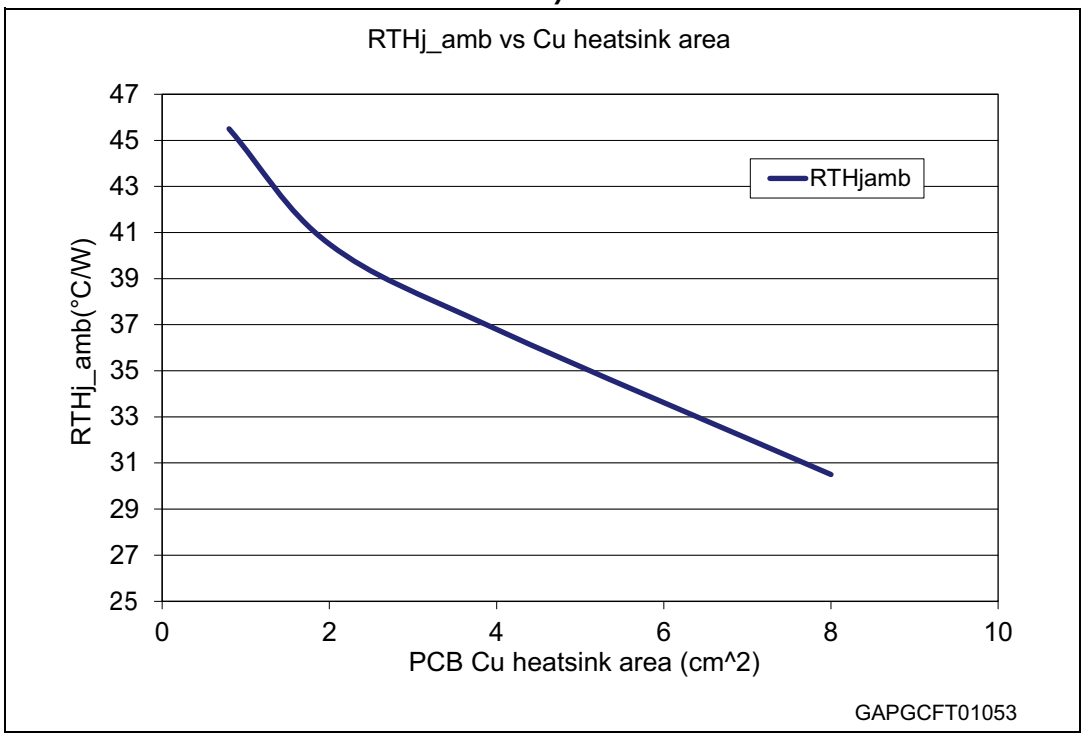


Figure 28. PowerSO-10 thermal impedance junction ambient single pulse (one channel on)

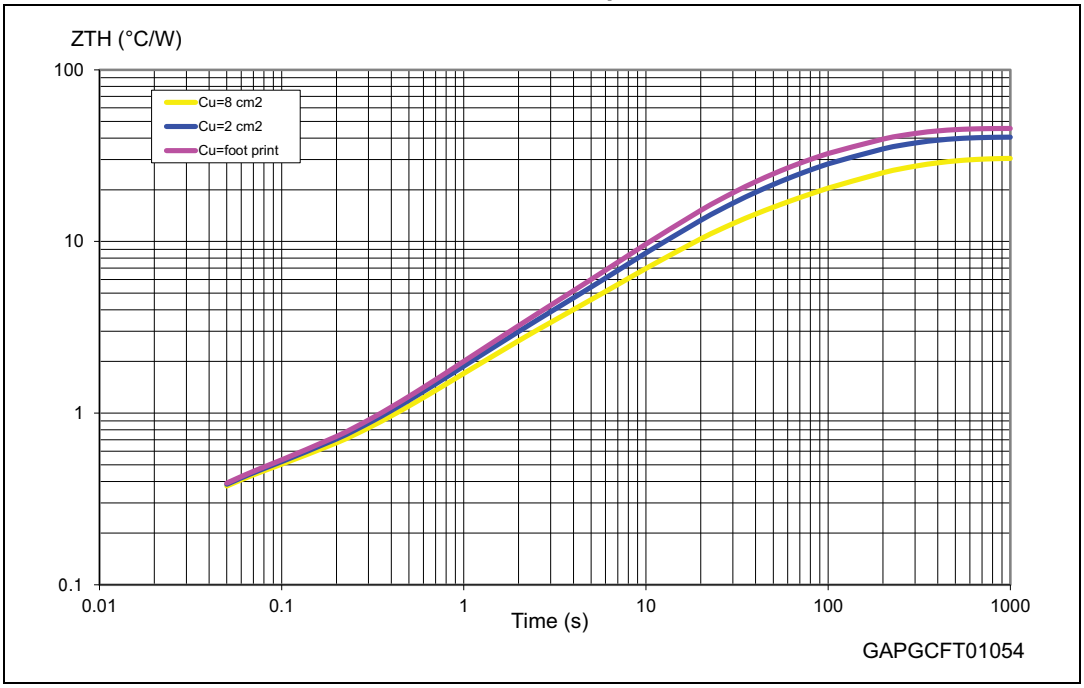
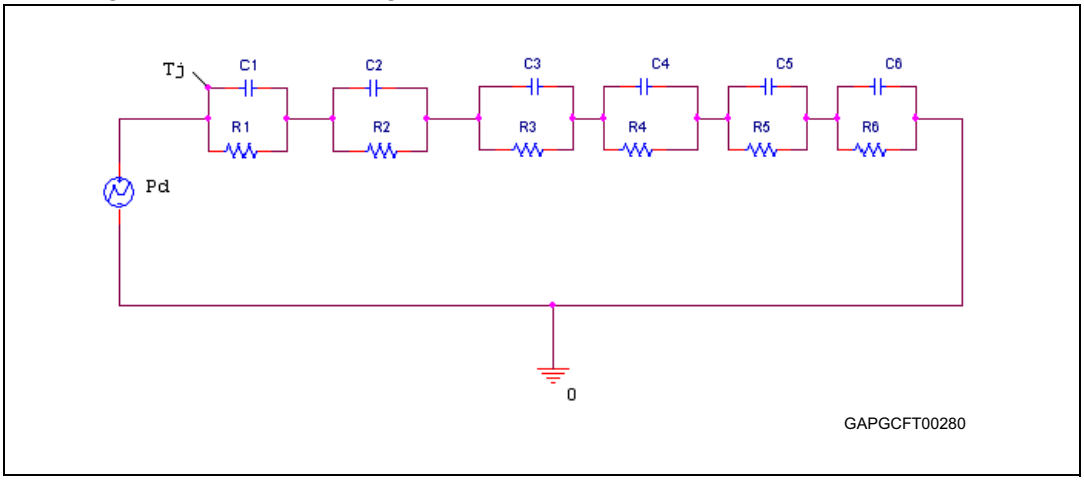


Figure 29. Thermal fitting model of a double channel HSD in PowerSO-10



1. The fitting model is a semplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 2: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1-\delta)$$

where $\delta = t_P/T$

Table 15. Thermal parameters

Area/island (cm^2)	Footprint	2	8
R1 (°C/W)	0.05		
R2 (°C/W)	0.3		
R3 (°C/W)	1.2		
R4 (°C/W)	7		
R5 (°C/W)	13	12	8
R6 (°C/W)	24	20	14
C1 (W.s/°C)	0.05		
C2 (W.s/°C)	0.1		
C3 (W.s/°C)	1		
C4 (W.s/°C)	2		
C5 (W.s/°C)	3	4	8
C6 (W.s/°C)	6	8	14

5 Package information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 PowerSO-10 mechanical data

Figure 30. PowerSO-10 package dimensions

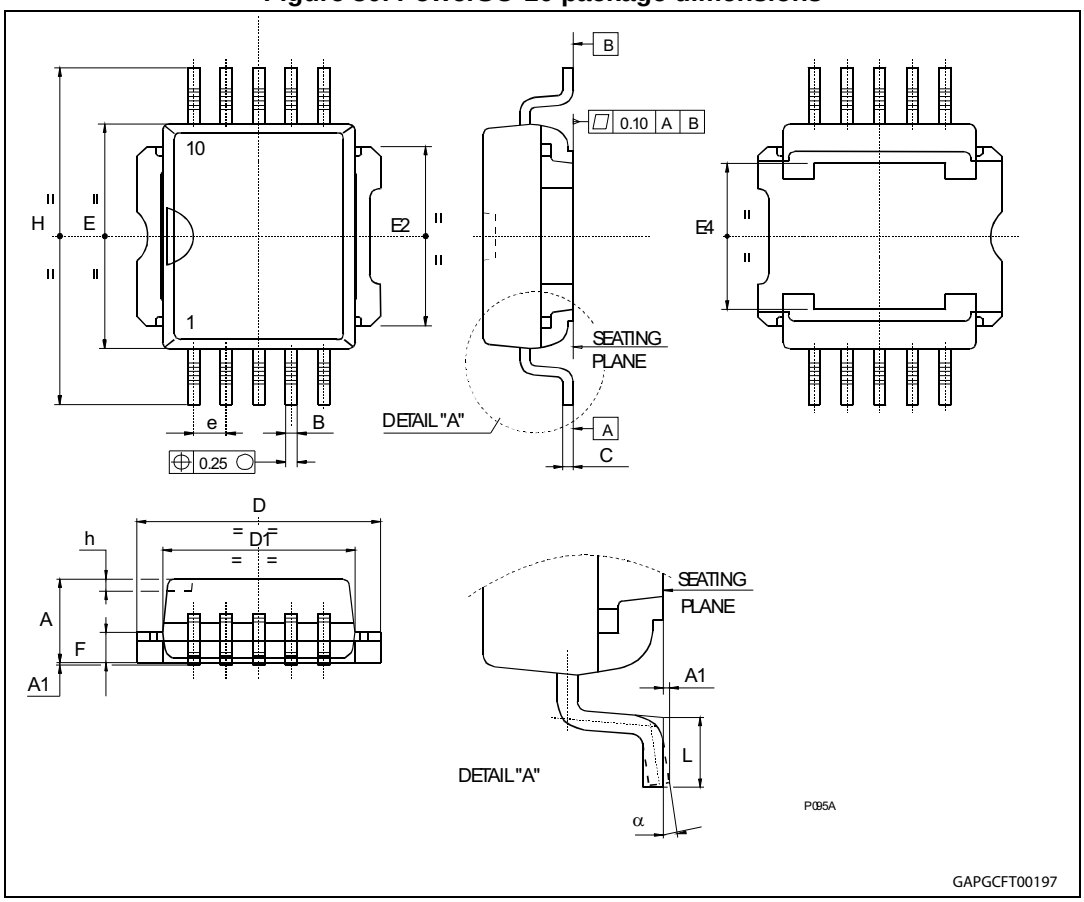


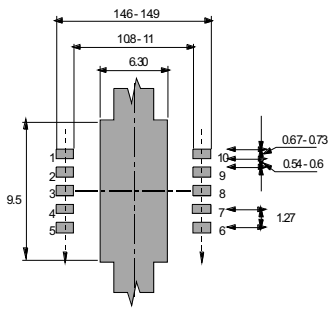
Table 16. PowerSO-10 mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	3.35		3.65
A(1)	3.4		3.6
A1	0.00		0.10
B	0.40		0.60
B(1)	0.37		0.53
C	0.35		0.55
C(1)	0.23		0.32
D	9.40		9.60
D1	7.40		7.60
E	9.30		9.50
E2	7.20		7.60
E2(1)	7.30		7.50
E4	5.90		6.10
E4(1)	5.90		6.30
e		1.27	
F	1.25		1.35
F(1)	1.20		1.40
H	13.80		14.40
H(1)	13.85		14.35
h		0.50	
L	1.20		1.80
L(1)	0.80		1.10
a	0º		8º
α(1)	2º		8º

1. Muar only POA P013P.

5.3 Packing information

Figure 31. PowerSO-10 suggested pad layout and tube shipment (no suffix)



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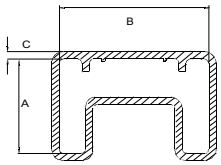
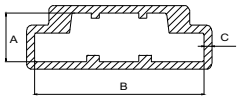


CASABLANCA



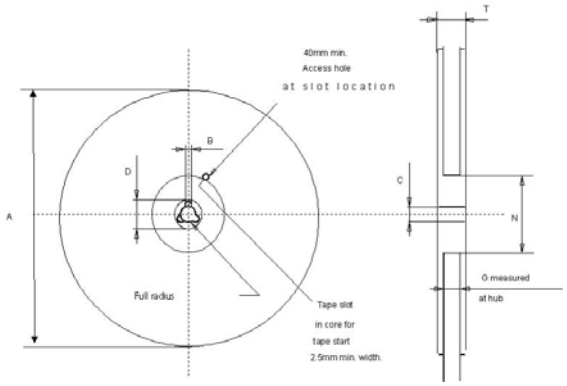
MUAR

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (± 0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

GAPGCFT00179

Figure 32. PowerSO-10 tape and reel shipment (suffix "TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

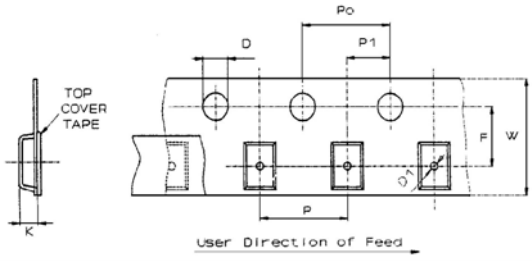
All dimensions are in mm.

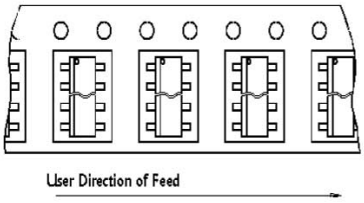
TAPE DIMENSIONS

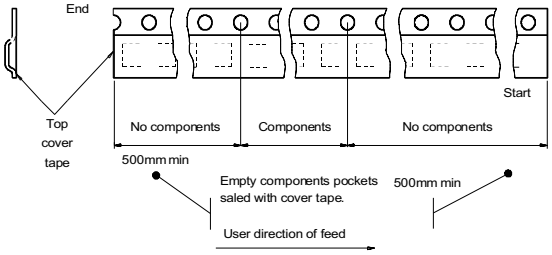
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (± 0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.







GAPGCFT00180

6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
PowerSO-10	VN5T006ASP-E	VN5T006ASPTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
19-Dec-2012	1	Initial release.
16-Jan-2013	2	Updated *Figure 3: Current and voltage conventions* *Table 6: Switching (VCC = 24 V; Tj = 25°C)*: – $dV_{OUT}/dt_{(on)}dV_{OUT}/dt_{(on)}$: updated values *Table 9: Current sense (8 V < V_{CC} < 36 V)*: – I_{OL}: removed row – dK/K_{BULB2}, dK/K_{BULB2}: updated test conditions Updated *Table 22: Turn-On voltage slope* and *Table 23: Turn-Off voltage slope*
16-Jun-2013	3	Changed document status from “preliminary data” to “production data”
17-Sep-2013	4	Updated disclaimer.

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