MADR-009269-000100

Single Driver for GaAs FET or PIN Diode Switches and Attenuators

Rev. V1

Features

- High Voltage CMOS Technology
- Complementary Outputs
- Positive Voltage Control
- CMOS device using TTL input levels
- Low Power Dissipation
- Low Cost Plastic SOIC-8 Package
- 100% Matte Tin Plating over Copper
- Halogen-Free “Green” Mold Compound
- 260°C Reflow Compatible

Description

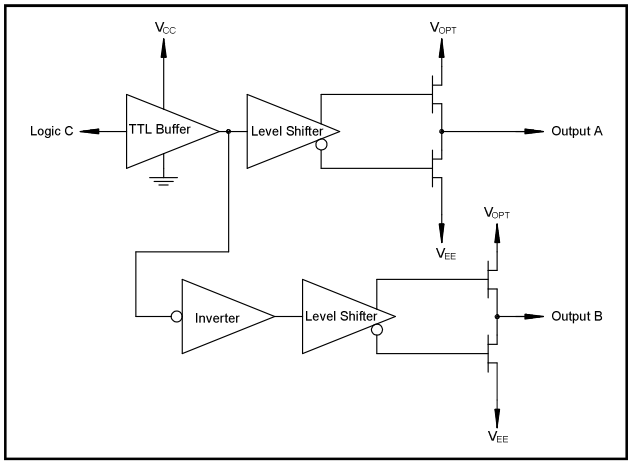
The MADR-009269-000100 is a single channel CMOS driver used to translate TTL control inputs into complementary gate control voltages for GaAs FET microwave switches and attenuators. High speed analog CMOS technology is utilized to achieve low power dissipation at moderate to high speeds, encompassing most microwave switching applications. The output HIGH level is optionally 0 to +2.0V (relative to GND) to optimize the intermodulation products of FET control devices at low frequencies. For driving PIN Diode circuits, the outputs are nominally switched between +5V & -5V.

Ordering Information[1]

Part Number	Package
MADR-009269-000100	Bulk Packaging
MADR-009269-000DIE	Die [2]
MADR-009269-0001TR	1000 piece reel

1. Reference Application Note M513 for reel size information.
2. Die sales are available in waffle packs in increments of 100 pieces.

Functional Schematic



Pin Configuration[3]

Pin No.	Function
1	Output A
2	GND
3	V_{CC}
4	C, Logic
5	V_{EE}
6	V_{OPT}
7	GND
8	Output B

3. The bottom of the die should be isolated for part number MADR-009269-000DIE.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Guaranteed Operating Ranges [4,5,8]

Symbol	Parameter	Unit	Min.	Typ.	Max.
V_{CC}	Positive DC Supply Voltage	V	4.5	5.0	5.5
V_{EE}	Negative DC Supply Voltage	V	-10.5	-5.0	-4.5
V_{OPT} [6,7]	Optional DC Output Supply Voltage	V	0	—	V_{CC}
V_{OPT} - V_{EE}	Negative Supply Voltage Range	V	4.5	Note 6,7	16.0
V_{CC} - V_{EE}	Positive to negative Supply Range	V	9.0	10.0	16.0
T_{OPER}	Operating Temperature	°C	-40	+25	+85
I_{OH}	DC Output Current - High	mA	-50	—	—
I_{OL}	DC Output Current - Low	mA	—	—	50
T_{rise}, T_{fall}	Maximum Input Rise or Fall Time	ns	—	—	500

4. Unused logic inputs must be tied to either GND or V_{CC}.
5. All voltages are relative to GND.
6. V_{OPT} is grounded in most cases when FETs are driven. To improve the intermodulation performance and the 1 dB compression point of GaAs control devices at low frequencies, V_{OPT} can be increased to between 1.0 and 2.0V. The nonlinear characteristics of the GaAs control devices will approximate performance at 500 MHz. It should be noted that the control current that is on the GaAs MMICs will increase when positive controls are applied.
7. When this driver is used to drive PIN diodes, V_{OPT} is often set to +5.0V, with V_{EE} set to -5.0V.
8. 0.01 uF decoupling capacitors are required on the power supply lines.

Truth Table

Input	Outputs	
C	A	B
Logic “0”	V_{EE}	V_{OPT}
Logic “1”	V_{OPT}	V_{EE}

Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Silicon Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

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DC Characteristics over Guaranteed Operating Range

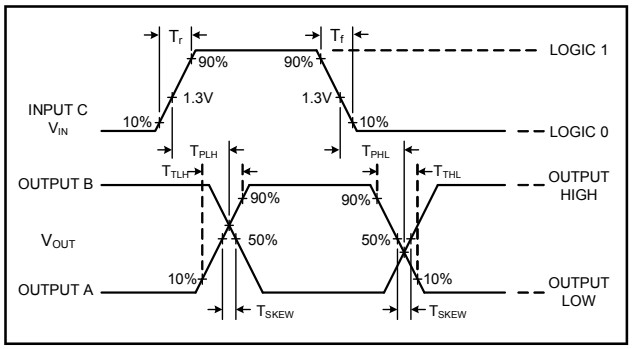
Symbol	Parameter	Test Conditions	Units	Min.	Typ.	Max.
V_{IH}	Input High Voltage	Guaranteed High Input Voltage	V	2.0	—	—
V_{IL}	Input Low Voltage	Guaranteed Low Input Voltage	V	—	—	0.8
V_{OH}	Output High Voltage	I_{OH} = -1 mA	V	V_{OPT} - 0.1	—	—
V_{OL}	Output Low Voltage	I_{OL} = 1 mA	V	—	—	V_{EE} + 0.1
I_{IN}	Input Leakage Current	V_{IN} = V_{CC} or GND, V_{EE} = min, V_{CC} = max, V_{OPT} = min or max	µA	-1	—	1
R_{NFET}	Output Resistance NFET On (to V_{EE})	V_{CC} = 5.0V, V_{EE} = -5.0V, V_{OPT} = 5.0V, V_{OUT} = -4.9V +25°C	Ω	—	30	—
R_{PFET}	Output Resistance PFET On (to V_{OPT})	V_{CC} = 5.0V, V_{EE} = -5.0V, V_{OPT} = 5.0V, V_{OUT} = 4.9V +25°C	Ω	—	30	—
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5V, V_{CC} = 5.5V, V_{OPT} = 5.5V, No Output Load	µA	—	1	—
ΔI_{CC}	Additional Supply Current (per TTL Input pin)	V_{CC}= max, V_{IN} = V_{CC} -2.1V	mA	—	1	—
I_{EE}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5V, V_{CC} = 5.5V, V_{OPT} = 5.5V, No Output Load	µA	—	1	—
I_{OPT}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, V_{EE} = -10.5V, V_{CC} = 5.5V, V_{OPT} = 5.5V, No Output Load	µA	—	1	—

AC Characteristics Over Guaranteed Operating Range[9]

		Typical performance			
Symbol	**Parameter**	**-40°C**	**+85°C**	**+85°C**	**Unit**
T_{PLH}	Propagation Delay	20	22	25	ns
T_{PHL}	Propagation Delay	20	22	25	ns
T_{TLH}	Output Transition Time (Rising Edge)	5	5	8	ns
T_{THL}	Output Transition Time (Falling Edge)	4	4	5	ns
T_{skew}	Delay Skew	2.5	2.5	2.5	ns
PRF (max)	50% Duty Cycle	DC	—	10	MHz
C_{IN}	Input Capacitance	5	5	5	pF

9. V_{CC} = +4.5V, V_{EE} = -4.5V, V_{OPT} = 0V or +4.5V, C_L = 25 pF, Trise, Tfall = 6 ns

Switching Waveforms

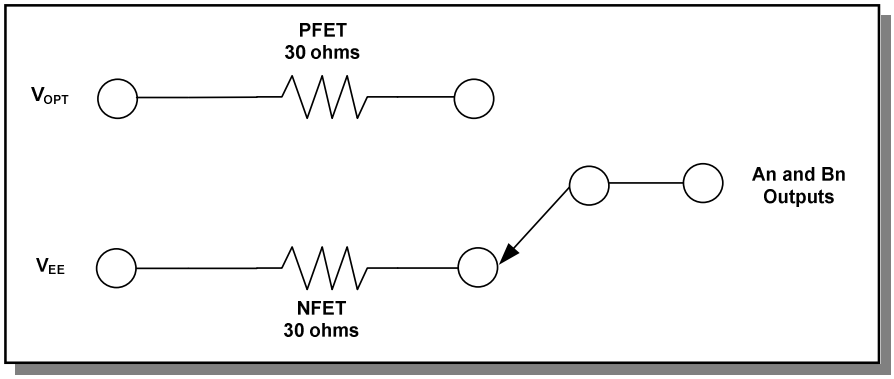


Absolute Maximum Ratings[11]

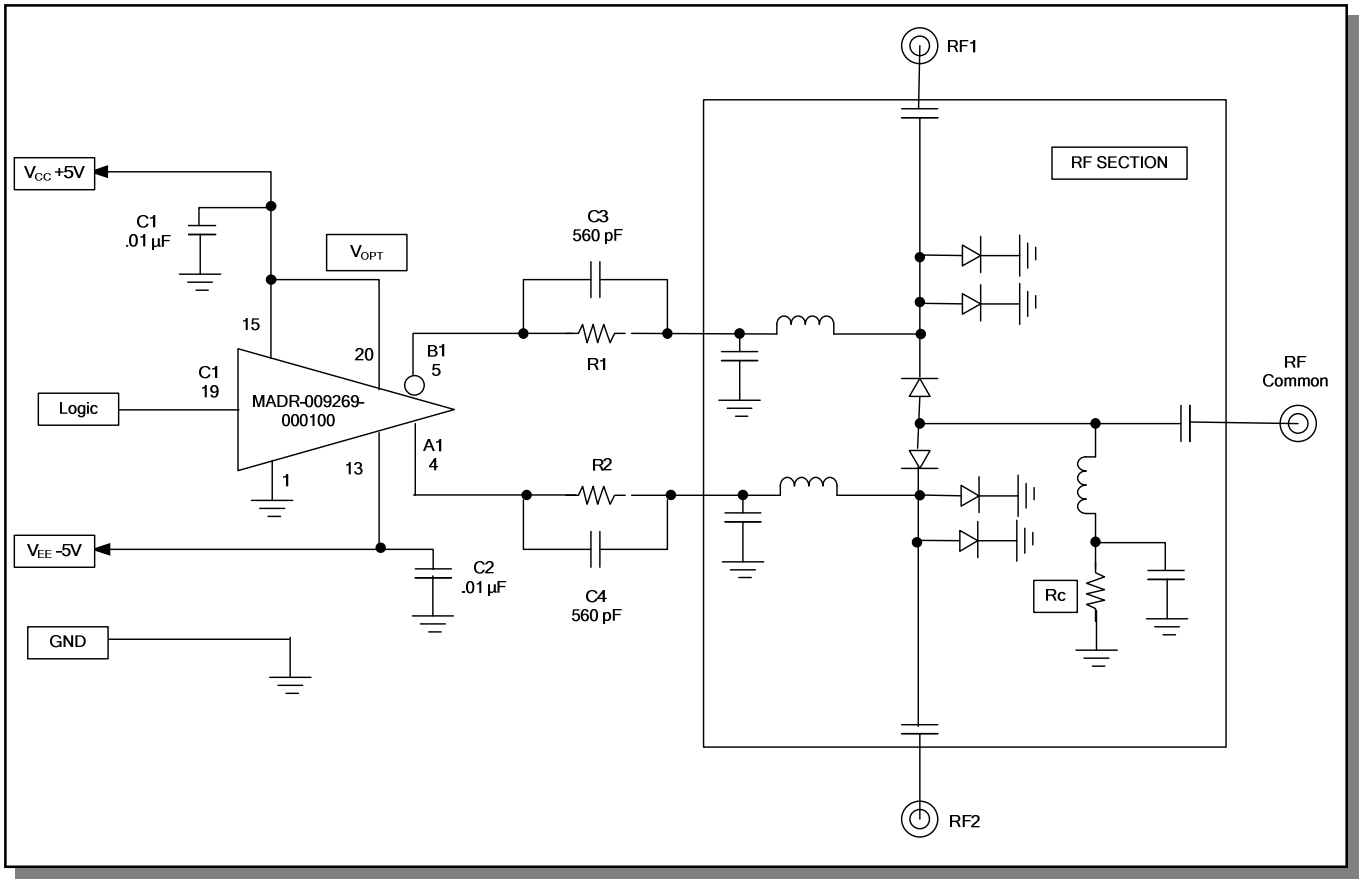
Symbol	Parameter	Min	Max	Unit
V_{CC}	Positive DC Supply Voltage	-0.5	7.0	V
I_{CC}	Positive DC Supply Current (-0.5V ≤ V_{IN} ≤ 0.8V; 2.0V ≤ V_{IN} ≤ V_{CC} + 0.5V; V_{CC} - V_{IN} ≤ 7.0V)	—	20	mA
V_{EE}	Negative DC Supply Voltage	-11.0	0.5	V
I_{EE}	Negative DC Supply Current (per Output) [12]	-60	—	mA
V_{OPT}	Optional DC Output Supply Voltage	-0.5	Note 13	V
I_{OPT}	Optional DC Output Supply Current (per Output) [12]	—	60	mA
V_{OPT} - V_{EE}	Output to Negative Supply Voltage Range	-0.5	18.0	V
V_{CC} - V_{EE}	Positive to Negative Supply Voltage Range	-0.5	18.0	V
V_{IN}	DC Input Voltage	-0.5 Note 14	V_{CC} +0.5	V
V_O	DC Output Voltage	V_{EE} – 0.5	V_{OPT} + 0.5	V
P_D[15]	Power Dissipation in Still Air	—	500	mW
T_{OPER}	Operating Temperature	-55	125	°C
T_{STG}	Storage Temperature	-65	150	°C
ESD	ESD Sensitivity	2.0	—	kV

11. All voltages are referenced to GND. All inputs and outputs incorporate latch-up protection structures.
12. The maximum I_{EE} and I_{OPT} are specified under the condition of V_{CC} = 5.5V, V_{EE} = -5.5V, V_{OPT} = 5.5V, and the total power dissipation is within 500 mW in still air.
13. The absolute maximum rating for V_{OPT} is V_{CC} + 0.5V, or +7.0V, whichever is less.
14. If V_{CC} ≥ 6.5V, then the minimum for V_{IN} is V_{CC} - 7.0V.
15. Derate -7 mW/°C from 65°C to 85°C.

Equivalent Output Circuit for A and B Outputs (50 mA load at 25°)



Typical Application for a SPDT Switch

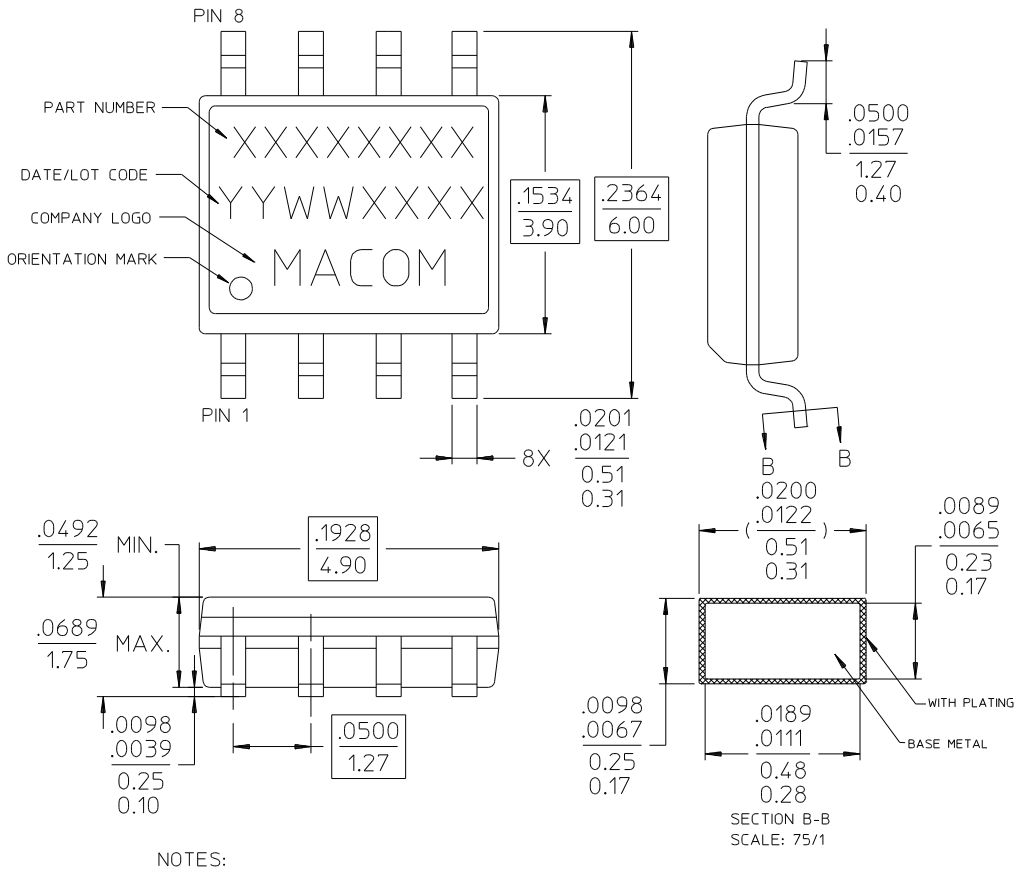


Description of Circuit

The MADR-009269-000100 provides a pair of complementary outputs that are each capable of driving a maximum of ± 50 mA into a load. In addition, with proper capacitor selection (C3 & C4) used in parallel with the current setting resistor (R1 & R2), additional spiking current can be achieved.

To achieve the Non-Inverting and Inverting complementary voltages, each output is switched between two internal FETs. The FETs are connected to V_{OPT} for the positive output and V_{EE} for the negative output. V_{OPT} and V_{EE} are adjustable for various configurations and have the following limitations: V_{EE} can be no more negative than –10.5 volts; V_{OPT} can be no more positive than +5.5 volts AND V_{OPT} must always be less than or equal to V_{CC}. Increasing V_{OPT} beyond V_{CC} will prevent the device from switching states when commanded to by the logic input. The most common configuration is to drive V_{EE} at –5.0 volts with V_{CC} and V_{OPT} tied together at +5.0 volts.

Lead-Free, SOIC-8†



NOTES:
1. REFERENCE JEDEC MS-012-AA, FOR ADDITIONAL DIMENSIONAL AND TOLERANCE INFORMATION.
2. REFERENCE M538 APPLICATON NOTE FOR FOOTPRINT INFORMATION.
3. ALL DIMENSIONS SHOWN AS INCHES/MM.

† Reference Application Note M538 for lead-free solder reflow recommendations.

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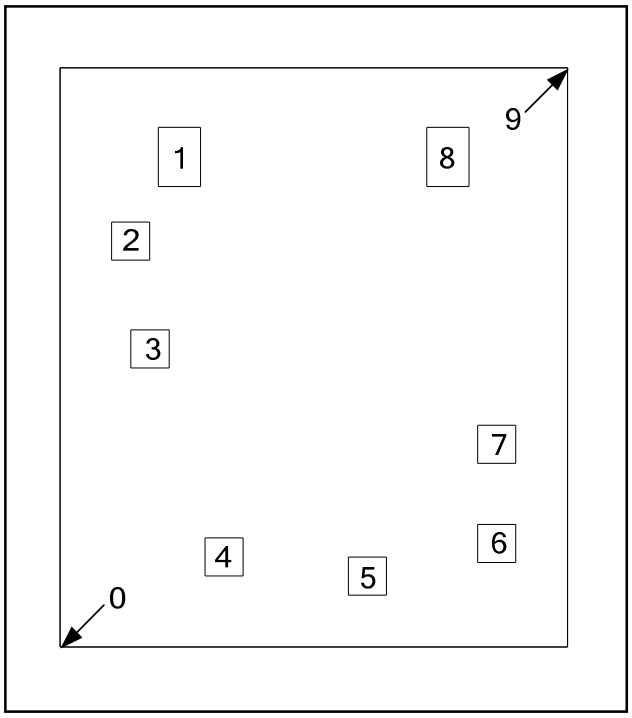
Die Outline



Pad Configuration[16,17]

Die Size: 1130 x 1290 µm (nominal)

Pad No.	X (µm) nominal	Y (µm) nominal	Pad Size (µm) X x Y
0	0	0	Lower left edge of die
1	266.40	1092.35	94 x 132
2	157.50	903.70	85 x 85
3	200.40	663.65	85 x 85
4	365.30	200.45	85 x 85
5	684.35	157.50	85 x 85
6	972.50	230.50	85 x 85
7	972.50	451.45	85 x 85
8	863.60	1092.35	94 x 132
9	1130	1290	Upper right edge of die

16. All X,Y dimensions are at bond pad center.
17. Die thickness is 8.0 mils.

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