NOTES:

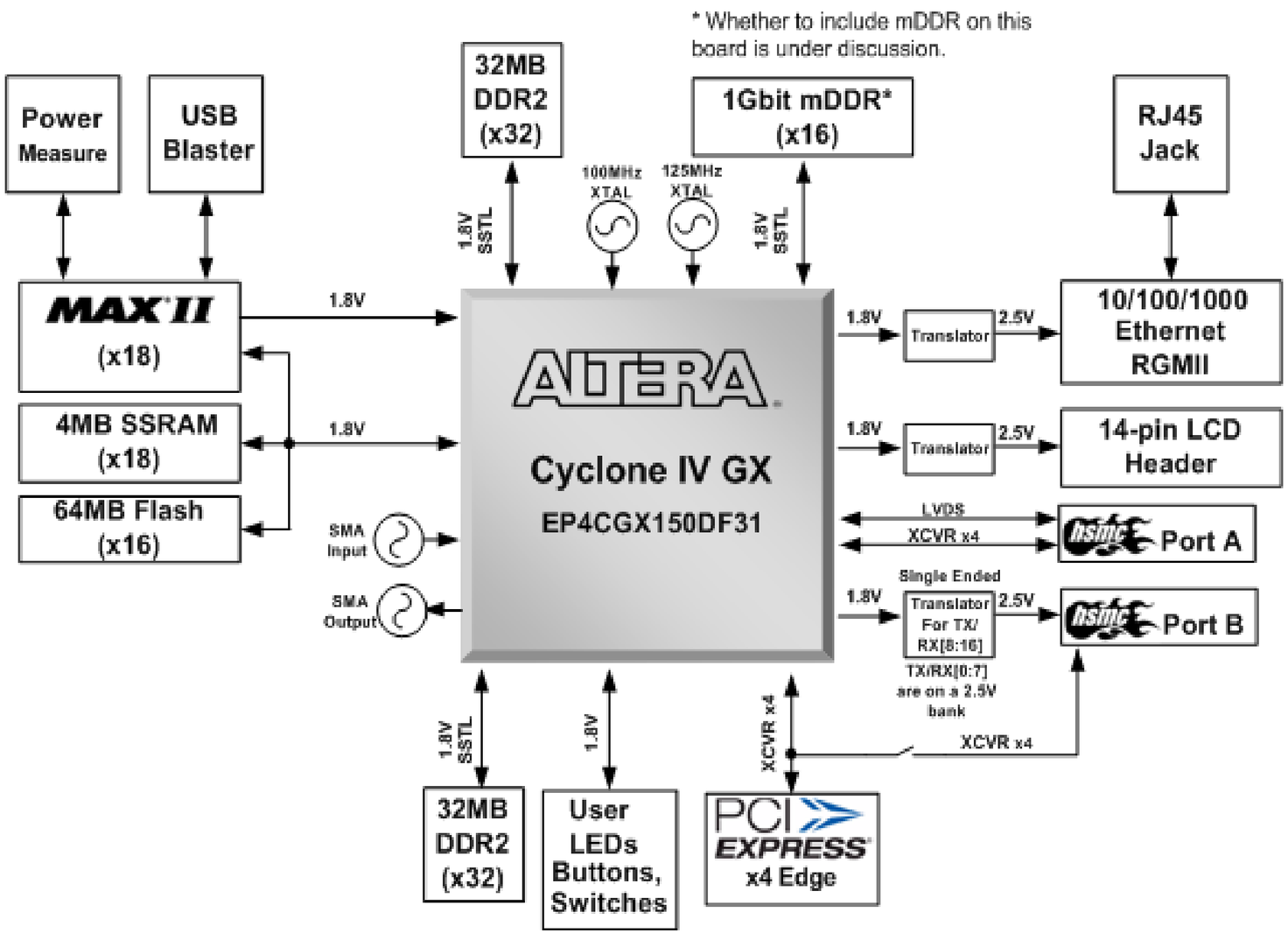
1. Project Drawing Numbers:

Raw PCB	100-0311003-A1
Gerber Files	110-0311003-A1
PCB Design Files	120-0311003-A1
Assembly Drawing	130-0311003-A1
Fab Drawing	140-0311003-A1
Schematic Drawing	150-0311003-A1
PCB Film	160-0311003-A1
Bill of Materials	170-0311003-A1
Schematic Design Files	180-0311003-A1
Functional Specification	210-0311003-A1
PCB Layout Guidelines	220-0311003-A1
Assembly Rework	320-0311003-A1

2. xx Parts, xx Library Parts, xx Nets, xx Pins

REV	DATE	PAGES	DESCRIPTION
A	5/15/2010	All	Initial Schematic

Cyclone IV GX FPGA Development Kit Board
Block Diagram



PAGE	DESCRIPTION
1	Title, Notes, Block Diagram, Revision History
2	C4GX FPGA Package Top
3	PCI Express Edge Connector x4
4	Cyclone IV GX Transceivers
5	Cyclone IV GX Banks 3 & 4
6	Cyclone IV GX Banks 5 & 6
7	Cyclone IV GX Banks 7 & 8
8	Cyclone IV GX Configuration
9	Cyclone IV GX Clocks
10	Clock Circuitry
11	DDR2 SDRAM x32 TOP
12	DDR2 SDRAM x32 BOTTOM
13	SSRAM & FLASH
14	MAX II
15	10/100/1000 Ethernet
16	HSM Connectors
17	User IO & Connector
18	Embedded USB Blaster
19	Power Monitor
20	Cyclone IV GX Power
21	Power 1
22	Power 2
23	Power 3
24	Decoupling
25	
26	
27	
28	
29	

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Cyclone IV GX FPGA Development Kit Board**

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Size	Document Number	Rev
B	150-0311003-B1 (6XX-43286R)	01

Date: Wednesday, December 08, 2010 Sheet 1 of 1

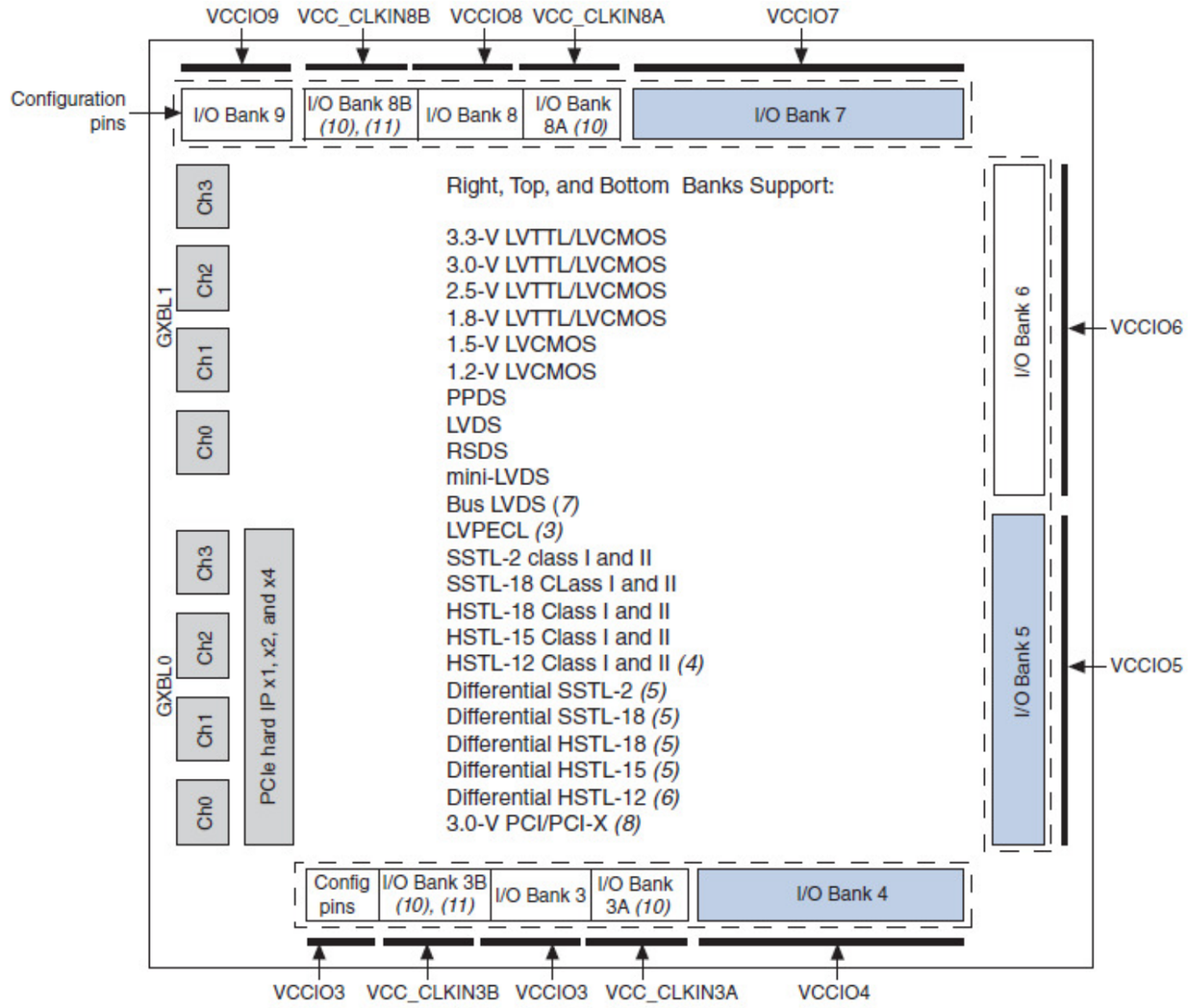
Notes:

1. FPGA Schematic Symbol Breakdown:
   - (A) Bank 3 - DDR2 SDRAM x32
   - (B) Bank 4 - DDR2 SDRAM x32, FLASH, SSRAM, SHARED FSM BUS
   - (C) Bank 5 - HSMC PORT B
   - (D) Bank 6 - HSMC PORT A
   - (E) Bank 7 - DDR2 SDRAM x32, ETHERNET
   - (F) Bank 8 - DDR2 SDRAM x32, mDDR SDRAM x16, LCD
   - (G) TRANSCEIVERS - PCIE x4/HSMB and HSMA XCVRs
   - (H) TRANSCEIVER POWER
   - (I) Some Clocks
   - (J) Configuration
   - (K) VCC, VCCD_PLL, VCCA, VCC_CLKIN
   - (L) VCCIO, VREF
   - (M) Ground
   - (N) Ground and NCs

Cyclone IV GX FPGA Package Top

BANK 8
VCCIO = 1.8V
DDR2 x32
GRAPHIC DISPLAY
HSMC PORT B

BANK 7
VCCIO = 1.8V
DDR2 x32
USER DIPSWITCH, PUSH BUTTONS
ETHERNET, HSMC PORT B



Transceiver Channels 4-7
HSMC XCVR PORT A

BANK 6
VCCIO = 2.5V/1.8V
HSMC PORT A

BANK 5
VCCIO = 2.5V
HSMC PORT A

Transceiver Channels 0-3
PCIE x4 or
HSMC XCVR PORT B

BANK 3
VCCIO = 1.8V
DDR2 x32
PCIE

BANKS 4
VCCIO = 1.8V
DDR2 x32
FLASH
SSRAM
SHARED FSM BUS

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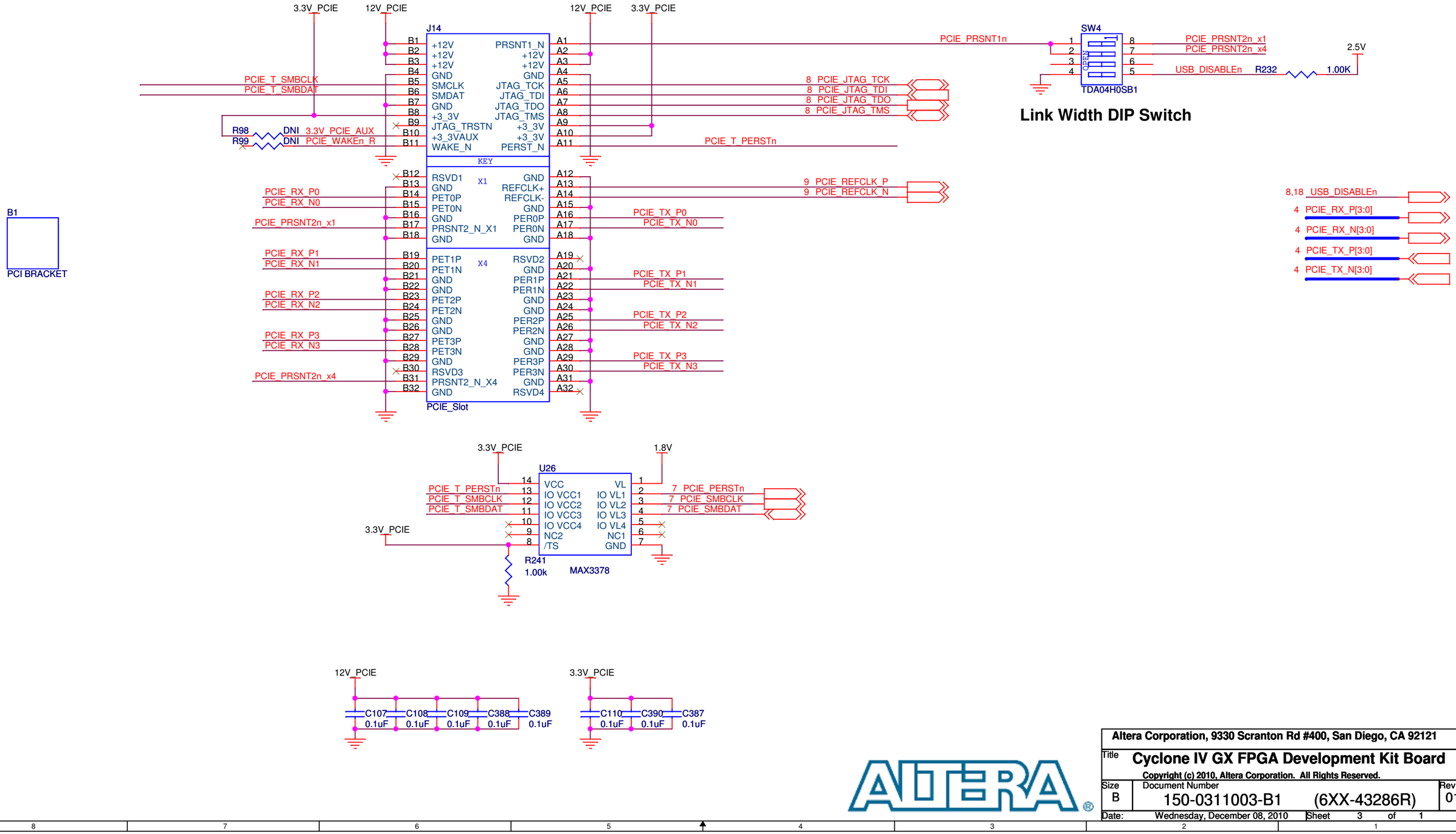
PCI Express Edge Connector



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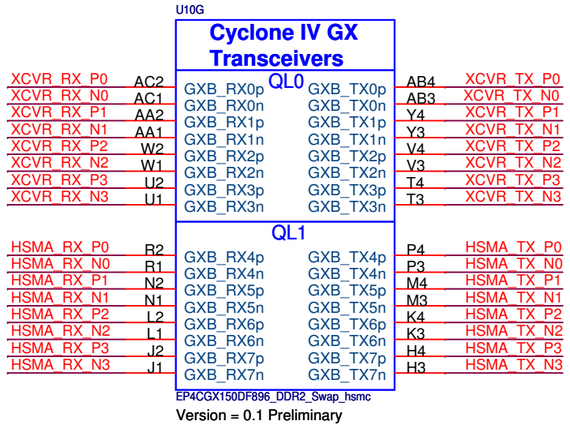
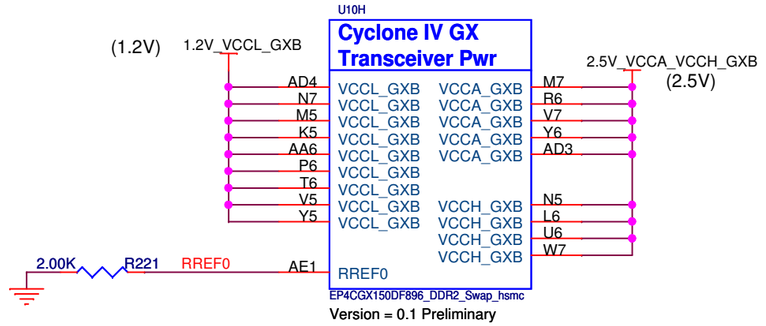
Cyclone IV GX Transceivers





16 HSMB_RX_P[3:0]
16 HSMB_RX_N[3:0]
16 HSMB_TX_P[3:0]
16 HSMB_TX_N[3:0]

16 HSMA_RX_P[3:0]
16 HSMA_RX_N[3:0]
16 HSMA_TX_P[3:0]
16 HSMA_TX_N[3:0]

3 PCIE_TX_P[3:0]
3 PCIE_TX_N[3:0]
3 PCIE_RX_P[3:0]
3 PCIE_RX_N[3:0]

XCVR_RX_P0	R84	0	PCIE_RX_P0	
	R86	DNI	HSMB_RX_P0	
XCVR_RX_N0	R85	0	PCIE_RX_N0	
	R87	DNI	HSMB_RX_N0	
XCVR_RX_P1	R88	0	PCIE_RX_P1	
	R89	DNI	HSMB_RX_P1	
XCVR_RX_N1	R90	0	PCIE_RX_N1	
	R91	DNI	HSMB_RX_N1	
XCVR_RX_P2	R92	0	PCIE_RX_P2	
	R94	DNI	HSMB_RX_P2	
XCVR_RX_N2	R93	0	PCIE_RX_N2	
	R95	DNI	HSMB_RX_N2	
XCVR_RX_P3	R96	0	PCIE_RX_P3	
	R97	DNI	HSMB_RX_P3	
XCVR_RX_N3	R100	0	PCIE_RX_N3	
	R101	DNI	HSMB_RX_N3	

XCVR_TX_P0	0.1uF	C324	PCIE_TX_P0	
	DNI	C323	HSMB_TX_P0	
XCVR_TX_N0	0.1uF	C341	PCIE_TX_N0	
	DNI	C340	HSMB_TX_N0	
XCVR_TX_P1	0.1uF	C326	PCIE_TX_P1	
	DNI	C325	HSMB_TX_P1	
XCVR_TX_N1	0.1uF	C343	PCIE_TX_N1	
	DNI	C342	HSMB_TX_N1	
XCVR_TX_P2	0.1uF	C328	PCIE_TX_P2	
	DNI	C327	HSMB_TX_P2	
XCVR_TX_N2	0.1uF	C345	PCIE_TX_N2	
	DNI	C344	HSMB_TX_N2	
XCVR_TX_P3	0.1uF	C330	PCIE_TX_P3	
	DNI	C329	HSMB_TX_P3	
XCVR_TX_N3	0.1uF	C347	PCIE_TX_N3	
	DNI	C346	HSMB_TX_N3	

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Size	Document Number	Rev
B	150-0311003-B1 (6XX-43286R)	01

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Cyclone IV GX Banks 3 & 4

70 pins of translation

1.8V_B3_B4

R166 49.9 RUP2
R165 49.9 RDN2

U10A

Cyclone IV GX Bank 3

DQ1B/DIFFIO_B5n
DQ1B/DIFFIO_B8p
DQ1B/DIFFIO_B8n
DQ1B/DIFFIO_B9n
DQ1B/DIFFIO_B10p
DQ1B/DIFFIO_B11n
DQ1B/DIFFIO_B12p
DQ1B/DIFFIO_B13p
DM1B/DIFFIO_B5p
DQS1B/CQ1Bn/DPCLK0/DIFFIO_B7p
DIFFIO_B9p
DIFFIO_B10n
DIFFIO_B11p
DIFFIO_B13n
DIFFIO_B7n
DIFFIO_B3n
DIFFIO_B4p
DIFFIO_B4n
DIFFIO_B6p
DIFFIO_B6n
DIFFIO_B20p
DIFFIO_B20n
DIFFIO_B24p
DIFFIO_B24n
DIFFIO_B26p
DIFFIO_B26n
DIFFIO_B29p
DIFFIO_B29n
DIFFIO_B34p
DIFFIO_B34n

DQ3B/DIFFIO_B14p
DQ3B/DIFFIO_B15p
DQ3B/DIFFIO_B16p
DQ3B/DIFFIO_B17p
DQ3B/DIFFIO_B18p
DQ3B/DIFFIO_B18n
DQ3B/DIFFIO_B19n
DQ3B/DIFFIO_B21p
DQ3B/DIFFIO_B22n
DM3B/BWSn3B/DIFFIO_B12n
DQS3B/CQ3Bn/DPCLK1/DIFFIO_B21n
DQ5B/DIFFIO_B25n
DQ5B/DIFFIO_B27p
DQ5B/DIFFIO_B28n
DQ5B/DIFFIO_B30p
DQ5B/DIFFIO_B31p
DQ5B/DIFFIO_B33p
DQ5B/DIFFIO_B35p
DQ5B/DIFFIO_B35n
DQ5B/DIFFIO_B36n
DM5B/BWSn5B/DIFFIO_B23n
DQS5B/CQ5Bn/DPCLK2/DIFFIO_B32p
DIFFIO_B14n
DIFFIO_B15n
DIFFIO_B16n
DIFFIO_B17n
DIFFIO_B19p
DIFFIO_B22p
DIFFIO_B25p
DIFFIO_B27n
DIFFIO_B28p
DIFFIO_B30n
DIFFIO_B31n
DIFFIO_B33n
DIFFIO_B36p
DIFFIO_B23p
DIFFIO_B32n

EP4CGX150DF896_DDR2_Swap_hsmc
Version = 0.1 Preliminary

DDR2B_DQ6	AF3	AE12	DDR2B_DQ14
DDR2B_DQ4	AH2	AG9	DDR2B_DQ9
DDR2B_DQ1	AJ3	AE13	DDR2B_DQ15
DDR2B_DQ3	AJ4	AG10	DDR2B_DQ12
DDR2B_DQ0	AG5	AH11	DDR2B_DQ11
DDR2B_DQ2	AK4	AJ10	DDR2B_DQ8
DDR2B_DQ5	AH6	AH12	DDR2B_DQ13
DDR2B_DQ7	AK5	AG13	DDR2B_DQ10
DDR2B_DM0	AE3	AH8	DDR2B_A10
DDR2B_DQS0	AD9	AJ6	DDR2B_DM1
		AH13	DDR2B_DQS1
FSM_A17	AH4	AB16	DDR2B_DQ23
FSM_A5	AH5	AJ7	DDR2B_DQ22
FSM_A18	AK3	AK8	DDR2B_DQ20
HSMB_TX_D_N15	AK6	AA15	DDR2B_DQ16
HSMB_RX_D_N13	AD10	AE14	DDR2B_DQ19
HSMB_TX_D_P13	AE10	AK11	DDR2B_DQ17
DDR2B_CLK_P	AF4	AH15	DDR2B_DQ18
DDR2B_CLK_N	AG4	AH16	DDR2B_DQ21
HSMB_RX_D_N15	AG3	AK14	FSM_D0
HSMB_RX_D_P14	AH3	AB13	DDR2B_DM2
		AF15	DDR2B_DQS2
DDR2B_BA0	AA12	AF12	FSM_A14
DDR2B_A12	AB11	AH9	FSM_A19
DDR2B_A9	AG7	AF13	DDR2B_ODT
DDR2B_A3	AH7	AH10	DDR2B_WEn
DDR2B_A0	AG14	AG12	DDR2B_RASn
DDR2B_A6	AH14	AG8	DDR2B_A7
DDR2B_A1	AK9	AA16	DDR2B_A8
DDR2B_CASn	AK10	AK7	DDR2B_A5
FSM_A7	AJ12	AJ9	DDR2B_BA1
HSMB_RX_D_P15	AK13	AB14	DDR2B_A2
		AE15	DDR2B_A11
		AK12	DDR2B_CSn
		AJ13	FSM_D15
		AA13	DDR2B_CKE
		AG15	DDR2B_A4

1.8V C138 0.1uF
1.8V C137 0.1uF

U10B

Cyclone IV GX Bank 4

DQ0B
DQ0B/DIFFIO_B67p
DQ0B/DIFFIO_B67n
DQ0B/DIFFIO_B69p
DQ0B/DIFFIO_B70n
DQ0B/DIFFIO_B72p
DQ0B/RUP2
DQ0B/RDN2
DM0B/DIFFIO_B64p
DQS0B/CQ1B/DPCLK5/DIFFIO_B69n
DIFFIO_B70p
DIFFIO_B72n
DIFFIO_B64n
DIFFIO_B38p
DIFFIO_B38n
DIFFIO_B40p
DIFFIO_B40n
DIFFIO_B41p
DIFFIO_B41n
DIFFIO_B44p
DIFFIO_B44n
DIFFIO_B49p
DIFFIO_B49n
DIFFIO_B45p
DIFFIO_B45n
DIFFIO_B48p
DIFFIO_B48n
DIFFIO_B50p
DIFFIO_B50n
DIFFIO_B51p
DIFFIO_B51n
DIFFIO_B52p
DIFFIO_B52n
DIFFIO_B53p
DIFFIO_B53n
DIFFIO_B56p
DIFFIO_B56n
DIFFIO_B57p
DIFFIO_B57n

DQ2B/DIFFIO_B54n
DQ2B/DIFFIO_B55n
DQ2B/DIFFIO_B59p
DQ2B/DIFFIO_B60p
DQ2B/DIFFIO_B61p
DQ2B/DIFFIO_B62p
DQ2B/DIFFIO_B63p
DM2B/DIFFIO_B46n
DQS2B/CQ3B/DPCLK4/DIFFIO_B58p
DQ4B/DIFFIO_B39p
DQ4B/DIFFIO_B39n
DQ4B/DIFFIO_B42p
DQ4B/DIFFIO_B42n
DQ4B/DIFFIO_B43p
DQ4B/DIFFIO_B43n
DQ4B/DIFFIO_B46p
DQ4B/DIFFIO_B47n
DQ4B/DIFFIO_B54p
DM4B/DIFFIO_B37p
DQS4B/CQ5B/DPCLK3/DIFFIO_B37n
DIFFIO_B55p
DIFFIO_B59n
DIFFIO_B60n
DIFFIO_B61n
DIFFIO_B62n
DIFFIO_B63n
DIFFIO_B47p
DIFFIO_B58n
DIFFIO_B65p
DIFFIO_B65n
DIFFIO_B66p
DIFFIO_B66n
DIFFIO_B68p
DIFFIO_B68n
DIFFIO_B71p
DIFFIO_B71n

EP4CGX150DF896_DDR2_Swap_hsmc
Version = 0.1 Preliminary

FSM_A4	AG25	AA20	HSMB_RX_D_N10
HSMB_RX_D_N8	Y20	AE21	FSM_A22
FLASH_CLK	Y21	AK23	FSM_A10
FSM_A3	AA21	AJ24	FSM_D9
FSM_A6	AH27	AG23	HSMB_RX_D_P7
HSMB_TX_D_P6	AG28	AK26	FSM_A16
RUP2	AD24	AH25	HSMB_TX_D_N16
RDN2	AE24		
HSMB_TX_D_N7	AJ27	AE19	HSMB_RX_D_N6
FSM_D7	AB22	AD22	HSMB_TX_D_P15
FSM_A15	AG27		
HSMB_TX_D_N6	AH28		
FSM_D4	AK28	AJ15	DDR2B_DQ30
		AK15	DDR2B_DQ28
FSM_A8	AE16	AK17	DDR2B_DQ25
HSMB_RX_D_P13	AG16	AK18	DDR2B_DQ27
HSMB_RX_D_N16	AD16	AH18	DDR2B_DQ24
HSMB_RX_D_P10	AE16	AJ18	DDR2B_DQ26
HSMB_RX_D_N9	AE17	AE18	DDR2B_DQ29
HSMB_RX_D_N14	AF18	AH19	DDR2B_DQ31
HSMB_RX_D_P11	AG17	Y19	FSM_D10
FSM_A11	AH17		
FSM_D14	Y18	Y17	DDR2B_DM3
FSM_A23	AA18	AA17	DDR2B_DQS3
HSMB_RX_D_P9	AJ19		
HSMB_RX_D_N11	AK19	AE20	HSMB_RX_D_P6
FSM_A13	AF19	AK24	HSMB_TX_D_P14
HSMB_CLK_OUT_P2	AG19	AK25	FSM_A21
HSMB_RX_D_P8	AK20	AH23	FSM_D11
HSMB_TX_D_P11	AK21	AK27	FSM_A24
		AJ25	HSMB_RX_D_N7
HSMB_TX_D_P9	AJ22	AG18	HSMB_RX_D_P12
FSM_D12	AK22		
HSMB_RX_D_N12	AG20	AE22	FSM_D8
FSM_A9	AH20		
HSMB_TX_D_N10	AH21	AG24	FSM_D6
HSMB_TX_D_N13	AJ21	AH24	FSM_D13
HSMB_CLK_IN_P2	AG22	AJ28	HSMB_TX_D_P7
HSMB_TX_D_N8	AH22	AK29	FSM_A2
		AG26	HSMB_TX_D_P8
FSM_A25	AF21	AH26	HSMB_TX_D_P10
HSMB_TX_D_N14	AF22	AD23	FSM_D5
		AE23	HSMB_TX_D_P12

12 DDR2B_DQ[31:0]
12 DDR2B_DQS[3:0]
12 DDR2B_DM[3:0]
12 DDR2B_A[12:0]
12 DDR2B_BA[1:0]
12 DDR2B_RASn
12 DDR2B_CASn
12 DDR2B_WEn
12 DDR2B_CSn
12 DDR2B_ODT
12 DDR2B_ODT
12 DDR2B_CLK_P
12 DDR2B_CLK_N
12 DDR2B_CKE

9 HSMB_TX_D_P16

SHARED BUS INTERFACE

FSM_D[15:0] FSM_D[15:0] 9,13,14,20
FSM_A[25:1] FSM_A[25:1] 8,9,13,14,20

USER INTERFACE

USER_LED[7:0] USER_LED[7:0] 7,8,9,14,17
USER_DIPSW[7:0] USER_DIPSW[7:0] 7,17,20

FLASH INTERFACE

FLASH_CLK FLASH_CLK 13,14
FLASH_OEn FLASH_OEn 9,13,14

MAX II INTERFACE

MAX_OEn MAX_OEn 9,14

HSMC PORT B

HSMB_RX_LED HSMB_RX_LED 7,17

HSMA INTERFACE

USER_DIPSW[7:0] USER_DIPSW[7:0] 7,17,20
3,7 PCIE_PERSTn
3,7 PCIE_SMBCLK
3,7 PCIE_SMBDAT

HSMB_RX_D_P7 HSMB_RX_D_P7
HSMB_RX_D_N8 HSMB_RX_D_N8
HSMB_RX_D_P8 HSMB_RX_D_P8
HSMB_RX_D_P9 HSMB_RX_D_P9
HSMB_RX_D_N9 HSMB_RX_D_N9
HSMB_TX_D_N16 HSMB_TX_D_N16

7 HSMB_TX_D_N15
HSMB_CLK_OUT_P2 HSMB_CLK_OUT_P2 9
HSMBT_CLK_IN_P2 HSMBT_CLK_IN_P2 16

1.8V C122 0.1uF
2.5V C121 0.1uF
1.8V C136 0.1uF
2.5V C135 0.1uF
2.5V C127 0.1uF
2.5V C120 0.1uF

U38 FXLA108

HSMB_RX_D_N14	1 VCCA	VCCB 20	16 HSMB_T_RX_D_N14
HSMB_RX_D_N12	2 A0	B0 19	16 HSMB_T_RX_D_N12
HSMB_RX_D_P6	3 A1	B1 18	16 HSMB_T_RX_D_P6
HSMB_RX_D_N6	4 A2	B2 17	16 HSMB_T_RX_D_N6
HSMB_RX_D_P7	5 A3	B3 16	16 HSMB_T_RX_D_P7
HSMB_RX_D_N10	6 A4	B4 15	16 HSMB_T_RX_D_N10
HSMB_RX_D_N8	7 A5	B5 14	16 HSMB_T_RX_D_N8
HSMB_RX_D_N7	8 A6	B6 13	16 HSMB_T_RX_D_N7
	9 A7 DAP	B7 12	
	10 GND	OEn 11	

U35 FXLA108

HSMB_TX_D_N13	1 VCCA	VCCB 20	16 HSMB_T_TX_D_N13
HSMB_TX_D_N10	2 A0	B0 19	16 HSMB_T_TX_D_N10
HSMB_TX_D_P9	3 A1	B1 18	16 HSMB_T_TX_D_P9
HSMB_TX_D_N14	4 A2	B2 17	16 HSMB_T_TX_D_N14
HSMB_TX_D_P15	5 A3	B3 16	16 HSMB_T_TX_D_P15
HSMB_TX_D_N8	6 A4	B4 15	16 HSMB_T_TX_D_N8
HSMB_TX_D_P14	7 A5	B5 14	16 HSMB_T_TX_D_P14
HSMB_TX_D_P16	8 A6	B6 13	HSMB_T_TX_D_P16
	9 A7 DAP	B7 12	
	10 GND	OEn 11	

U37 FXLA108

HSMB_RX_D_P11	1 VCCA	VCCB 20	16 HSMB_T_RX_D_P11
HSMB_RX_D_P10	2 A0	B0 19	16 HSMB_T_RX_D_P10
HSMB_RX_D_N9	3 A1	B1 18	16 HSMB_T_RX_D_N9
HSMB_RX_D_P9	4 A2	B2 17	16 HSMB_T_RX_D_P9
HSMB_RX_D_P8	5 A3	B3 16	16 HSMB_T_RX_D_P8
HSMB_RX_D_N11	6 A4	B4 15	16 HSMB_T_RX_D_N11
HSMB_RX_D_P12	7 A5	B5 14	16 HSMB_T_RX_D_P12
HSMB_RX_D_N16	8 A6	B6 13	16 HSMB_T_RX_D_N16
	9 A7 DAP	B7 12	
	10 GND	OEn 11	

U36 FXLA108

HSMB_TX_D_P12	1 VCCA	VCCB 20	16 HSMB_T_TX_D_P12
HSMB_TX_D_N16	2 A0	B0 19	16 HSMB_T_TX_D_N16
HSMB_TX_D_P10	3 A1	B1 18	16 HSMB_T_TX_D_P10
HSMB_TX_D_P8	4 A2	B2 17	16 HSMB_T_TX_D_P8
HSMB_TX_D_N7	5 A3	B3 16	16 HSMB_T_TX_D_N7
HSMB_TX_D_P7	6 A4	B4 15	16 HSMB_T_TX_D_P7
HSMB_TX_D_N6	7 A5	B5 14	16 HSMB_T_TX_D_N6
HSMB_TX_D_P6	8 A6	B6 13	16 HSMB_T_TX_D_P6
	9 A7 DAP	B7 12	
	10 GND	OEn 11	

1.8V C134 0.1uF
2.5V C133 0.1uF

U33 SN74AVC1T45

	1 VCCA	VCCB 6	2.5V
	2 GND	DIR 5	
HSMB_CLK_IN_P2	3 A	B 4	HSMBT_CLK_IN_P2

output
7,9 HSMB_TX_D_N12
7 HSMB_TX_D_P11
7,9 HSMB_TX_D_N11
7 HSMB_RX_D_N13
7 HSMB_RX_D_P13
7 HSMB_TX_D_P13
7 HSMB_RX_D_N15
7 HSMB_RX_D_P15
7 HSMB_TX_D_P14
7,9 HSMB_RX_D_P16

Input
7,16 HSMB_T_TX_D_P11
7,16 HSMB_T_TX_D_N11
7,16 HSMB_T_TX_D_N12
7,16 HSMB_T_TX_D_P13
7,16 HSMB_T_RX_D_P13
7,16 HSMB_T_RX_D_N13
7,16 HSMB_T_RX_D_P14
7,16 HSMB_T_RX_D_P15
7,16 HSMB_T_RX_D_N15
7,16 HSMB_T_RX_D_P16

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Title: Cyclone IV GX FPGA Development Kit Board

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Cyclone IV GX Banks 5 & 6

HSMB_CLK_IN_P1 — 100, 1% — R167 — HSMB_CLK_IN_N1

U10C

Cyclone IV GX Bank 5

HSMA_RX_D_P15	T23	DQ1R/DIFFIO_R34p		AB30	HSMB_RX_D_P0
HSMA_RX_D_N15	T24	DQ1R/DIFFIO_R34n	DQ3R/DIFFIO_R46n	AD30	HSMB_RX_D_N1
	V27	DQ1R/DIFFIO_R36p	DQ3R/DIFFIO_R47n	AB28	HSMB_TX_D_P0
HSMB_CLK_IN_N2	V28	DQ1R/DIFFIO_R36n	DQ3R/DIFFIO_R48n	AC28	HSMB_TX_D_P2
	W25	DQ1R/DIFFIO_R39p	DQ3R/DIFFIO_R49n	Y22	HSMB_RX_D_N5
HSMA_RX_D_P14	U25	DQ1R/DIFFIO_R40p	DQ3R/DIFFIO_R50n	AD27	HSMA_D3
HSMA_RX_D_N16	T21	DQ1R/DIFFIO_R42n	DQ3R/DIFFIO_R51p	AE29	HSMA_CLK_OUT0
	Y30	DQ1R/DIFFIO_R43n	DQ3R/DIFFIO_R52p	AE27	HSMB_TX_D_N4
			DQ3R/DIFFIO_R53p	AE28	HSMB_RX_D_P3
	AA29	DM1R/DIFFIO_R44n	DQ3R/DIFFIO_R53n		
	W27	DQS1R/CQ1Rn/DPCLK8/DIFFIO_R38p		AG30	HSMB_TX_D_P3
		DM3R/BWSn3R/DIFFIO_R54p		AA22	HSMB_CLK_OUT0
	W26	DIFFIO_R39n	DQS3R/CQ3Rn/DPCLK7/DIFFIO_R50p		
HSMA_RX_D_N14	T25	DIFFIO_R40n		Y25	HSMB_CLK_OUT_N2
HSMA_RX_D_P16	U21	DIFFIO_R42p	DQ5R	AF30	HSMA_D2
	AA30	DIFFIO_R43p	DQ5R/DIFFIO_R54n	AA27	HSMB_RX_D_P1
	AB29	DIFFIO_R44p	DQ5R/DIFFIO_R56p	Y27	HSMA_D1
	W28	DIFFIO_R38n	DQ5R/DIFFIO_R56n	AH29	HSMB_D0
			DQ5R/DIFFIO_R57p	AG29	HSMB_D3
			DQ5R/DIFFIO_R57n	AE26	HSMB_TX_D_P5
HSMA_RX_D_P13	T26		DQ5R/DIFFIO_R59n	AB25	HSMB_RX_D_N2
HSMA_RX_D_N13	T27	DIFFIO_R33p	DQ5R/DIFFIO_R60p	AA25	HSMB_CLK_OUT_P1
	U27	DIFFIO_R33n	DQ5R/DIFFIO_R60n		
	U28	DIFFIO_R35p		AB26	HSMB_TX_D_N2
HSMB_CLK_IN_N1	W29	DIFFIO_R35n		AC25	HSMB_RX_D_P4
HSMB_CLK_IN_P1	W30	DIFFIO_R37p	DM5R/BWSn5R/DIFFIO_R61n		
	V25	DIFFIO_R37n	DQS5R/CQ5Rn/DPCLK6/DIFFIO_R61p	AC30	HSMB_TX_D_N0
	V26	DIFFIO_R41p		AD29	HSMB_D2
HSMB_RX_D_N0	AA28	DIFFIO_R41n	DIFFIO_R46p	AB27	HSMB_RX_D_P2
HSMB_TX_D_P1	Y28	DIFFIO_R45p	DIFFIO_R47p	AC27	HSMA_D0
HSMB_RX_D_P5	AJ30	DIFFIO_R45n	DIFFIO_R48p	AD28	HSMB_TX_D_N9
HSMB_CLK_OUT_N1	AH30	DIFFIO_R58p	DIFFIO_R49p	AE30	HSMB_D1
		DIFFIO_R58n	DIFFIO_R51n	AE25	HSMB_TX_D_N5
			DIFFIO_R52n		
HSMB_RX_D_N4	AD25		DIFFIO_R59p		
HSMB_RX_D_N3	AD26	RUP3			
		RDN3			

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Version = 0.1 Preliminary

U10D

Cyclone IV GX Bank 6

HSMA_TX_D_N12	M28	DQ0R/DIFFIO_R21n		F26	HSMA_TX_D_P2
HSMA_RX_D_P6	M29	DQ0R/DIFFIO_R23p	DQ4R/DIFFIO_R1p	F27	HSMA_TX_D_N2
HSMA_RX_D_P3	N25	DQ0R/DIFFIO_R24p	DQ4R/DIFFIO_R1n	E27	HSMA_TX_D_P1
HSMA_RX_D_P5	N27	DQ0R/DIFFIO_R25p	DQ4R/DIFFIO_R3p	E28	HSMA_TX_D_N1
HSMA_RX_D_P4	R24	DQ0R/DIFFIO_R26p	DQ4R/DIFFIO_R3n	J27	HSMA_TX_D_P10
HSMA_RX_D_P10	R27	DQ0R/DIFFIO_R30p	DQ4R/DIFFIO_R5p	H27	HSMA_TX_D_N10
HSMA_RX_D_N10	R28	DQ0R/DIFFIO_R30n	DQ4R/DIFFIO_R5n	H25	HSMA_TX_D_N15
HSMA_RX_D_P11	T28	DQ0R/DIFFIO_R32p	DQ4R/DIFFIO_R6n	C29	HSMA_TX_D_P0
			DQ4R/DIFFIO_R7p		
HSMA_RX_D_N11	R29	DM0R/DIFFIO_R32n		C30	HSMA_TX_D_N0
HSMA_RX_D_N9	P30	DQS0R/CQ1R/DPCLK9/DIFFIO_R29n	DM4R/DIFFIO_R7n	G26	HSMA_RX_D_P1
			DQS4R/CQ5R/DPCLK11/DIFFIO_R2p		
HSMA_RX_D_P0	D29	DQ2R/DIFFIO_R9p	DIFFIO_R6p	J25	HSMA_TX_D_P15
HSMA_TX_D_P14	K25	DQ2R/DIFFIO_R10p	DIFFIO_R2n	G27	HSMA_RX_D_N1
HSMA_TX_D_P13	K26	DQ2R/DIFFIO_R11p			
HSMA_TX_D_N13	K27	DQ2R/DIFFIO_R11n	DIFFIO_R4p	F28	HSMA_TX_D_P4
HSMA_TX_D_P3	E30	DQ2R/DIFFIO_R13p	DIFFIO_R4n	F29	HSMA_TX_D_N4
HSMA_TX_D_N3	E30	DQ2R/DIFFIO_R13n	DIFFIO_R8p	J28	HSMA_TX_D_P9
HSMA_TX_D_P11	L27	DQ2R/DIFFIO_R15p	DIFFIO_R8n	H28	HSMA_TX_D_N9
HSMA_TX_D_P5	H30	DQ2R/DIFFIO_R19p	DIFFIO_R12p	G28	HSMA_TX_D_P6
			DIFFIO_R12n	G29	HSMA_TX_D_N6
HSMA_CLK_OUT_P1	P21	DM2R/DIFFIO_R16p	DIFFIO_R14p	M21	HSMA_TX_D_P16
HSMA_TX_D_N14	J26	DQS2R/CQ3R/DPCLK10/DIFFIO_R10n	DIFFIO_R14n	M22	HSMA_TX_D_N16
			DIFFIO_R17p	K28	HSMA_CLK_OUT_P2
HSMA_TX_D_P12	M27	DIFFIO_R21p	DIFFIO_R17n	K29	HSMA_CLK_OUT_N2
HSMA_RX_D_N6	M30	DIFFIO_R23n	DIFFIO_R18p	J29	HSMA_TX_D_P7
HSMA_RX_D_N3	M26	DIFFIO_R24n	DIFFIO_R18n	J30	HSMA_TX_D_N7
HSMA_RX_D_N5	N28	DIFFIO_R25n	DIFFIO_R20p	L30	HSMA_TX_D_P8
HSMA_RX_D_N4	P25	DIFFIO_R26n	DIFFIO_R20n	K30	HSMA_TX_D_N8
HSMA_RX_D_P9	R30	DIFFIO_R29p	DIFFIO_R22p	N24	HSMA_RX_D_P2
			DIFFIO_R22n	M25	HSMA_RX_D_N2
HSMA_RX_D_N0	D30	DIFFIO_R9n			
HSMA_TX_D_N11	L28	DIFFIO_R15n	DIFFIO_R27p	N29	HSMA_RX_D_P7
HSMA_TX_D_N5	G30	DIFFIO_R19n	DIFFIO_R27n	N30	HSMA_RX_D_N7
HSMA_CLK_OUT_N1	N21	DIFFIO_R16n	DIFFIO_R28p	P27	HSMA_RX_D_P8
			DIFFIO_R28n	P28	HSMA_RX_D_N8
			DIFFIO_R31p	R25	HSMA_RX_D_P12
			DIFFIO_R31n	R26	HSMA_RX_D_N12

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HSMA_RX_D_P0	DNI	R181	HSMA_RX_D_N0
HSMA_RX_D_P1	DNI	R190	HSMA_RX_D_N1
HSMA_RX_D_P2	DNI	R194	HSMA_RX_D_N2
HSMA_RX_D_P3	DNI	R189	HSMA_RX_D_N3
HSMA_RX_D_P4	DNI	R188	HSMA_RX_D_N4
HSMA_RX_D_P5	DNI	R179	HSMA_RX_D_N5
HSMA_RX_D_P6	DNI	R180	HSMA_RX_D_N6
HSMA_RX_D_P7	DNI	R178	HSMA_RX_D_N7
HSMA_RX_D_P8	DNI	R177	HSMA_RX_D_N8
HSMA_RX_D_P9	DNI	R169	HSMA_RX_D_N9
HSMA_RX_D_P10	DNI	R176	HSMA_RX_D_N10
HSMA_RX_D_P11	DNI	R175	HSMA_RX_D_N11
HSMA_RX_D_P12	DNI	R187	HSMA_RX_D_N12
HSMA_RX_D_P13	DNI	R186	HSMA_RX_D_N13
HSMA_RX_D_P14	DNI	R185	HSMA_RX_D_N14
HSMA_RX_D_P15	DNI	R191	HSMA_RX_D_N15
HSMA_RX_D_P16	DNI	R193	HSMA_RX_D_N16

HSMC PORT A

HSMA_TX_D_P[16:0] — HSMA_TX_D_P[16:0] 16

HSMA_TX_D_N[16:0] — HSMA_TX_D_N[16:0] 16

HSMA_RX_D_P[16:0] — HSMA_RX_D_P[16:0] 16

HSMA_RX_D_N[16:0] — HSMA_RX_D_N[16:0] 16

HSMA_CLK_IN_P[2:1] — HSMA_CLK_IN_P[2:1] 9,16

HSMA_CLK_IN_N[2:1] — HSMA_CLK_IN_N[2:1] 9,16

HSMA_CLK_OUT_P[2:1] — HSMA_CLK_OUT_P[2:1] 16

HSMA_CLK_OUT_N[2:1] — HSMA_CLK_OUT_N[2:1] 16

HSMA_CLK_OUT0 — HSMA_CLK_OUT0 16

HSMA_TX_D_P2 — HSMA_TX_D_P2 16

HSMA_TX_D_N2 — HSMA_TX_D_N2 16

HSMA_D[3:0] — HSMA_D[3:0] 16

HSMC PORT B

HSMB_CLK_OUT_P[2:1] — HSMB_CLK_OUT_P[2:1] 5,9,16

HSMB_CLK_OUT_N[2:1] — HSMB_CLK_OUT_N[2:1] 16

HSMB_CLK_IN_P1 — HSMB_CLK_IN_P1 16

HSMB_CLK_IN_N[2:1] — HSMB_CLK_IN_N[2:1] 16

HSMB_D[3:0] — HSMB_D[3:0] 16

HSMB_CLK_OUT0 — HSMB_CLK_OUT0 16

HSMB_TX_LED — HSMB_TX_LED 7,17

MAX INTERFACE

5,9 HSMB_TX_D_P16

5 HSMB_TX_D_N16

16 HSMB_TX_D_N9

8,16 HSMB_TX_D_P[5:0]

16,20 HSMB_TX_D_N[5:0]

16 HSMB_RX_D_P[5:0]

16 HSMB_RX_D_N[5:0]

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Cyclone IV GX Banks 7 & 8

1.8V_B7_B8

R170 49.9 RUP4
R171 49.9 RDN4

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Cyclone IV GX Bank 7

DDR2A_DQ7 F22
DDR2A_DQ6 B30
DDR2A_DQ0 G23
DDR2A_DQ5 F23
DDR2A_DQ4 H24
DDR2A_DQ2 G24
DDR2A_DQ1 D28
DDR2A_DQ3 C28

DDR2A_DM0 G22
DDR2A_DQS0 A29

DDR2A_A2 D17
DDR2A_ODT C17
DDR2A_A11 G18
DDR2A_A4 F18
DDR2A_RASn B18
DDR2A_CKE A19
DDR2A_BA1 B19
DDR2A_BA0 A20

DDR2A_CSn D20
DDR2A_A10 C20
DDR2A_A5 B21
DDR2A_A3 A21
DDR2A_A12 F21
DDR2A_A9 F20
DDR2A_CLK_P D23
DDR2A_CLK_N C23

HSMA_SCL B24
HSMA_RX_LED C24
ENET_MDC K21
HSMB_SCL K22

FLASH_CEn E25
FLASH_ADVn F24
DDR2A_A8 K17

RUP4 G25
RDN4 F25

DQ0T/DIFFIO_T64n
DQ0T/DIFFIO_T65p
DQ0T/DIFFIO_T66p
DQ0T/DIFFIO_T66n
DQ0T/DIFFIO_T68p
DQ0T/DIFFIO_T68n
DQ0T/DIFFIO_T69p
DQ0T/DIFFIO_T69n
DM0T/DIFFIO_T64p
DQS0T/CQ1T/DPCLK12/DIFFIO_T65n

DIFFIO_T38p
DIFFIO_T38n
DIFFIO_T40p
DIFFIO_T40n
DIFFIO_T42p
DIFFIO_T42n
DIFFIO_T44p
DIFFIO_T44n

DIFFIO_T46p
DIFFIO_T46n
DIFFIO_T48p
DIFFIO_T48n
DIFFIO_T50p
DIFFIO_T50n
DIFFIO_T52p
DIFFIO_T52n

DIFFIO_T53n
DIFFIO_T53p
DIFFIO_T67p
DIFFIO_T67n

IO1_B7
IO2_B7
IO3_B7

RUP4
RDN4

DQ2T/DIFFIO_T55n
DQ2T/DIFFIO_T56n
DQ2T/DIFFIO_T57n
DQ2T/DIFFIO_T59p
DQ2T/DIFFIO_T60p
DQ2T/DIFFIO_T61p
DQ2T/DIFFIO_T62p
DQ2T/DIFFIO_T63p
DM2T/DIFFIO_T54n
DQS2T/CQ3T/DPCLK13/DIFFIO_T47p
DIFFIO_T55p
DIFFIO_T56p
DIFFIO_T57p
DIFFIO_T59n
DIFFIO_T60n
DIFFIO_T61n
DIFFIO_T62n
DIFFIO_T63n
DIFFIO_T54p
DIFFIO_T47n

DQ4T/DIFFIO_T37n
DQ4T/DIFFIO_T39n
DQ4T/DIFFIO_T41n
DQ4T/DIFFIO_T43p
DQ4T/DIFFIO_T45p
DQ4T/DIFFIO_T45n
DQ4T/DIFFIO_T49p
DQ4T/DIFFIO_T51p
DM4T/DIFFIO_T36p
DQS4T/CQ5T/DPCLK14/DIFFIO_T37p
DIFFIO_T58p

DIFFIO_T39p
DIFFIO_T41p
DIFFIO_T43n
DIFFIO_T49n
DIFFIO_T51n
DIFFIO_T36n
DIFFIO_T58n

F19 DDR2A_DQ15
D21 DDR2A_DQ13
D22 DDR2A_DQ8
A26 DDR2A_DQ9
D26 DDR2A_DQ11
E24 DDR2A_DQ10
B27 DDR2A_DQ14
B28 DDR2A_DQ12

A24 DDR2A_DM1
G17 DDR2A_DQS1

G20 CPU_RESETn
E21 LCD_DATA3
E22 FSM_A1
A25 HSMA_PSNTn
C26 HSMB_PSNTn
D24 FSM_A20
A27 ENET_TX_EN
A28 FLASH_RESETn

B25 HSMA_TX_LED
F17 DDR2A_A6

K18 DDR2A_DQ23
A17 DDR2A_DQ19
C18 DDR2A_DQ18
D19 DDR2A_DQ17
E19 DDR2A_DQ16
E18 DDR2A_DQ21
C22 DDR2A_DQ22
A23 DDR2A_DQ20

B16 DDR2A_DM2
K19 DDR2A_DQS2
D25 HSMB_TX_LED

A18 DDR2A_WEn
D18 DDR2A_A0
C19 DDR2A_A1
B22 DDR2A_A7
A22

A16 DDR2A_CASn
C25 HSMA_SDA

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Cyclone IV GX Bank 8

LCD_DATA1 F9
ENET_GTX_CLK D9
FSM_D1 C9
LCD_DATA6 E10
ENET_TX_D2 D10
HSMB_RX_D_P16 D3
LCD_CSn C3
HSMB_SDA F10
LCD_WEn E6

ENET_TX_D0 G10

LCD_D_Cn D5
ENET_RESETn D6
USER_LED1 C7
CLKIN_SMA C5
USER_LED4 D4
SSRAM_CLK F11
USER_PB1 D11
USER_LED7 B6
ENET_RX_D1 B9

USER_DIPSW0 A5
LCD_DATA2 D7

USER_DIPSW2 E9
SSRAM_E1n C6
USER_DIPSW4 C4
PCIE_SMBDAT E12
C11
PCIE_PERSTn A7
MAX_WEn A9
A6
USER_DIPSW7 E7

USER_LED5 J9
ENET_RX_D0 F5
USER_PB2 F4
USER_LED0 E4
ENET_TX_D1 E3

HSMB_T_SCL
HSMB_T_SDA

DQ1T/DIFFIO_T5p
DQ1T/DIFFIO_T6p
DQ1T/DIFFIO_T6n
DQ1T/DIFFIO_T7p
DQ1T/DIFFIO_T7n
DQ1T/DIFFIO_T8p
DQ1T/DIFFIO_T8n
DQ1T/DIFFIO_T9n
DQ1T/DIFFIO_T10p
DQS1T/CQ1Tn/DPCLK17/DIFFIO_T9p
DQS5T/CQ5Tn/DPCLK15/DIFFIO_T34n

DQ3T/DIFFIO_T10n
DQ3T/DIFFIO_T11p
DQ3T/DIFFIO_T11n
DQ3T/DIFFIO_T12n
DQ3T/DIFFIO_T13p
DQ3T/DIFFIO_T14p
DQ3T/DIFFIO_T17p
DQ3T/DIFFIO_T18p
DQ3T/DIFFIO_T19p
DM3T/BWSn3T/DIFFIO_T16n
DQS3T/CQ3Tn/DPCLK16/DIFFIO_T15n

DIFFIO_T5n
DIFFIO_T12p
DIFFIO_T13n
DIFFIO_T14n
DIFFIO_T17n
DIFFIO_T18n
DIFFIO_T19n
DIFFIO_T16p
DIFFIO_T15p

DIFFIO_T1p
DIFFIO_T2p
DIFFIO_T2n
DIFFIO_T3p
DIFFIO_T3n

DM5T/DIFFIO_T20n
DQ5T/DIFFIO_T22n
DQ5T/DIFFIO_T24p
DQ5T/DIFFIO_T26n
DQ5T/DIFFIO_T28p
DQ5T/DIFFIO_T29n
DQ5T/DIFFIO_T32p
DQ5T/DIFFIO_T32n
DQ5T/DIFFIO_T34p
C16 DDR2A_DQS3

DIFFIO_T20p
DIFFIO_T22p
DIFFIO_T24n
DIFFIO_T26p
DIFFIO_T28n
DIFFIO_T29p

DIFFIO_T21n
DIFFIO_T21p
DIFFIO_T23p
DIFFIO_T23n

DIFFIO_T25p
DIFFIO_T25n
DIFFIO_T27p
DIFFIO_T27n

DIFFIO_T30p
DIFFIO_T30n
DIFFIO_T31p
DIFFIO_T31n
DIFFIO_T33p
DIFFIO_T33n
DIFFIO_T35p
DIFFIO_T35n

IO1_B8

A8 DDR2A_DM3
F12 DDR2A_DQ31
F13 DDR2A_DQ29
C14 DDR2A_DQ25
D15 DDR2A_DQ30
A12 DDR2A_DQ26
A14 DDR2A_DQ27
A13 DDR2A_DQ24
D16 DDR2A_DQ28

B7 FLASH_RDYBSYn
G12 USER_DIPSW6
E13 ENET_RX_D3
D14 PCIE_LED_X1
C15 LCD_DATA0
B12 MAX_CSn

C12 USER_PB0
D12 USER_LED6
C10 HSMB_RX_LED
B10 ENET_TX_D3

D13 SSRAM_BAn
C13 FLASH_WEn
A11 ENET_INTN
A10 PCIE_LED_X4

F14 USER_DIPSW5
E15 ENET_RX_DV
F15 PCIE_SMBCLK
F16
G14 ENET_RX_D2
G13 LCD_DATA5
G15 USER_DIPSW1
F16 LCD_DATA7

D8 USER_PB3

HSMB_RX_D_P7 5
HSMB_RX_D_N8 5
HSMB_RX_D_P8 5
HSMB_RX_D_P9 5
HSMB_RX_D_N9 5
HSMB_TX_D_N16 5

EP4CGX150DF896_DDR2_Swap_hsmc
Version = 0.1 Preliminary

HSMB_T_SCL 16
HSMB_T_SDA 16

1.8V C118 0.1uF
1.8V C119 0.1uF

1.8V C129 0.1uF
2.5V C130 0.1uF

U39 MAX3373
VL, TRI_STATE, VCC, VL_IO1, VL_IO2, VCCIO1, VCCIO2, GND

HSMB_SCL
HSMB_SDA
HSMB_T_SCL
HSMB_T_SDA

1.8V C319 0.1uF
1.8V C280 0.1uF

U29 FXLA108 21
VCCA, VCCB, A0, A1, A2, A3, A4, A5, A6, A7, GND, DAP, B0, B1, B2, B3, B4, B5, B6, B7, OEn

HSMB_RX_D_N13 5
HSMB_TX_D_P13 5
HSMB_TX_D_N12 9
HSMB_TX_D_N11 9
HSMB_TX_D_P11 5
HSMB_RX_D_P13 5

16 HSMB_T_RX_D_N13
16 HSMB_T_TX_D_P13
16 HSMB_T_TX_D_N12
16 HSMB_T_TX_D_N11
16 HSMB_T_TX_D_P11
16 HSMB_T_RX_D_P13

U28 FXLA108 21

HSMB_TX_D_N15 5
HSMB_RX_D_P16 9
HSMB_RX_D_N15 5
HSMB_RX_D_P15 5
HSMB_RX_D_P14 5

16 HSMB_T_TX_D_N15
16 HSMB_T_RX_D_P16
16 HSMB_T_RX_D_N15
16 HSMB_T_RX_D_P15
16 HSMB_T_RX_D_P14

2.5V C116 0.1uF
2.5V C115 0.1uF

U31 MAX3373
VL, TRI_STATE, VCC, VL_IO1, VL_IO2, VCCIO1, VCCIO2, GND

HSMA_SCL
HSMA_SDA
HSMA_T_SCL 16
HSMA_T_SDA 16

U49 FXLA108 21

ENET_TX_D0
ENET_RX_D3
ENET_RX_D2
ENET_RX_D1
ENET_RX_D0
ENET_RX_DV
ENET_TX_EN
ENET_GTX_CLK

ENET_T_TX_D0
ENET_T_RX_D3
ENET_T_RX_D2
ENET_T_RX_D1
ENET_T_RX_D0
ENET_T_RX_DV
ENET_T_TX_EN
ENET_T_GTX_CLK

U46 FXLA108 21

LCD_DATA7
LCD_DATA6
LCD_DATA5
LCD_DATA3
LCD_DATA2
ENET_TX_D3
ENET_TX_D2
ENET_TX_D1

LCD_T_DATA7
LCD_T_DATA6
LCD_T_DATA5
LCD_T_DATA3
LCD_T_DATA2
ENET_T_TX_D3
ENET_T_TX_D2
ENET_T_TX_D1

2.5V C320 0.1uF
2.5V C281 0.1uF

SHARED BUS INTERFACE

FSM_D1 FSM_D1 9,15
FSM_A1 FSM_A1 9,15
FSM_A20 FSM_A20 9,15
HSMB_RX_D_P16 HSMB_RX_D_P16 9,15

DDR2A x32 INTERFACE

MAX_CSn MAX_CSn 14
MAX_WEn MAX_WEn 14
11 DDR2A_DQ[31:0]
11 DDR2A_DQS[3:0]
11 DDR2A_DM[3:0]
11 DDR2A_A[12:0]
11 DDR2A_BA[1:0]

SSRAM_BAn SSRAM_BAn 13
SSRAM_BBn SSRAM_BBn 9,13
SSRAM_ADVn SSRAM_ADVn 13
SSRAM_ADSCn SSRAM_ADSCn 13
SSRAM_ADSPn SSRAM_ADSPn 13
SSRAM_E1n SSRAM_E1n 13
SSRAM_CLK SSRAM_CLK 13
SSRAM_BWn SSRAM_BWn 9,13
SSRAM_Gn SSRAM_Gn 9,13
SSRAM_GWn SSRAM_GWn 13,14

11 DDR2A_RASn
11 DDR2A_WEn
11 DDR2A_CSn
11 DDR2A_ODT
11 DDR2A_ODT
11 DDR2A_CLK_P
11 DDR2A_CLK_N
11 DDR2A_CKE
11 DDR2A_CASn

FLASH_RESETn FLASH_RESETn 13,14
FLASH_CEn FLASH_CEn 13,14
FLASH_ADVn FLASH_ADVn 13,14
FLASH_WEn FLASH_WEn 13,14

ENET_MDIO ENET_MDIO 9,15

HSMC INTERFACE

HSMB_RX_LED HSMB_RX_LED 17
HSMB_TX_LED HSMB_TX_LED 17
14,16 HSMB_PSNTn

ENET_RESETn ENET_RESETn 15
ENET_MDIO ENET_MDIO 9,15
ENET_INTN ENET_INTN 15
ENET_MDC ENET_MDC 15
HSMA_TX_LED HSMA_TX_LED 17
14,16 HSMA_PSNTn
HSMA_RX_LED HSMA_RX_LED 17

LCD DISPLAY INTERFACE

17 LCD_T_DATA[7:5]
17 LCD_T_DATA[3:2]
USER_PB[3:0] USER_PB[3:0] 17
17 LCD_D_Cn
USER_LED[7:0] USER_LED[7:0] 8,9,14,17

ETHERNET RGMII INTERFACE

CPU_RESETn CPU_RESETn 17
15 ENET_T_RX_D[3:0]
CLKIN_SMA CLKIN_SMA 9
PCIE_LED_X4 PCIE_LED_X4 17
PCIE_LED_X1 PCIE_LED_X1 17
9,15 ENET_T_RX_CLK
15 ENET_T_RX_DV
removed ENET_CRS
LCD_CSn LCD_CSn 17
LCD_WEn LCD_WEn 17
LCD_DATA0 LCD_DATA0 17
LCD_DATA1 LCD_DATA1 17
15 ENET_T_TX_D[3:0]
15 ENET_T_GTX_CLK
15 ENET_T_TX_EN

ETHERNET CONTROL INTERFACE

15 ENET_RESETn
15 ENET_INTn
9,15 ENET_MDIO
17,20 USER_DIPSW[7:0]

3 PCIE_PERSTn
3 PCIE_SMBCLK
3 PCIE_SMBDAT

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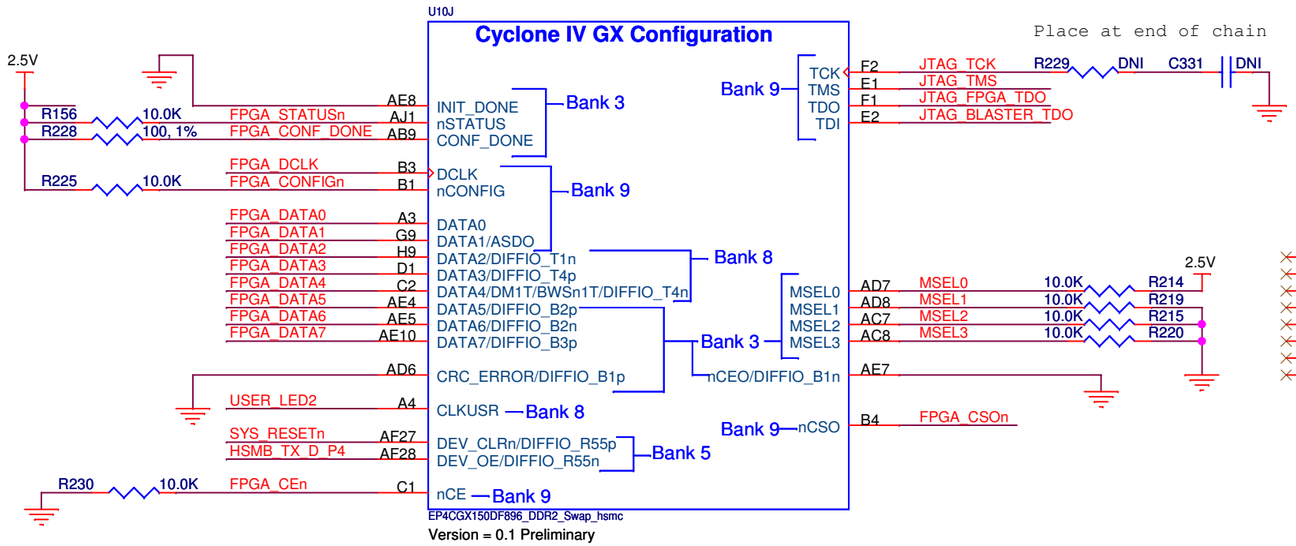
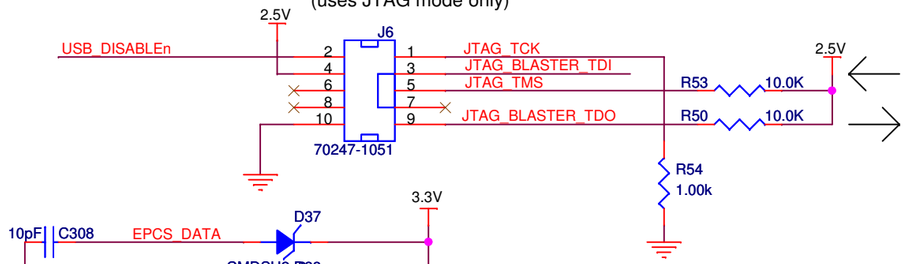
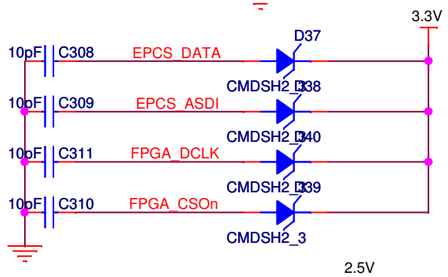
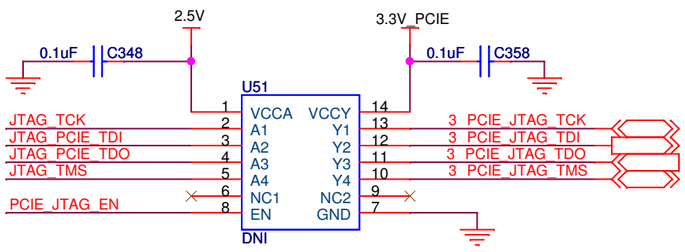
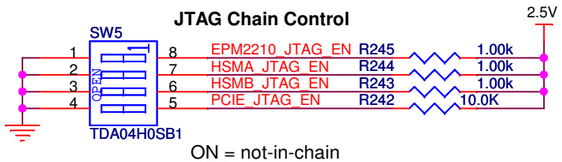
Cyclone IV GX Configuration

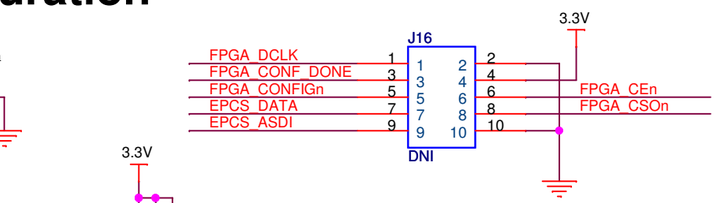


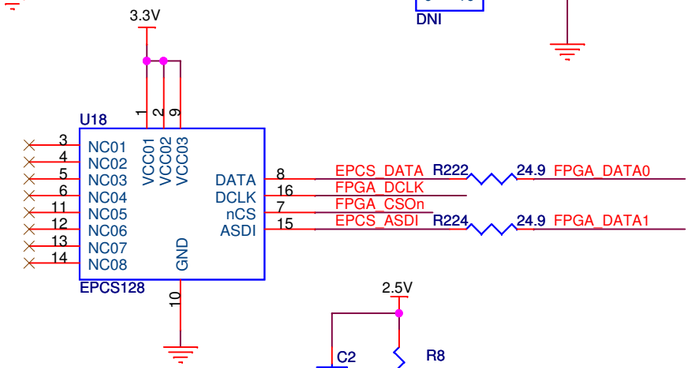


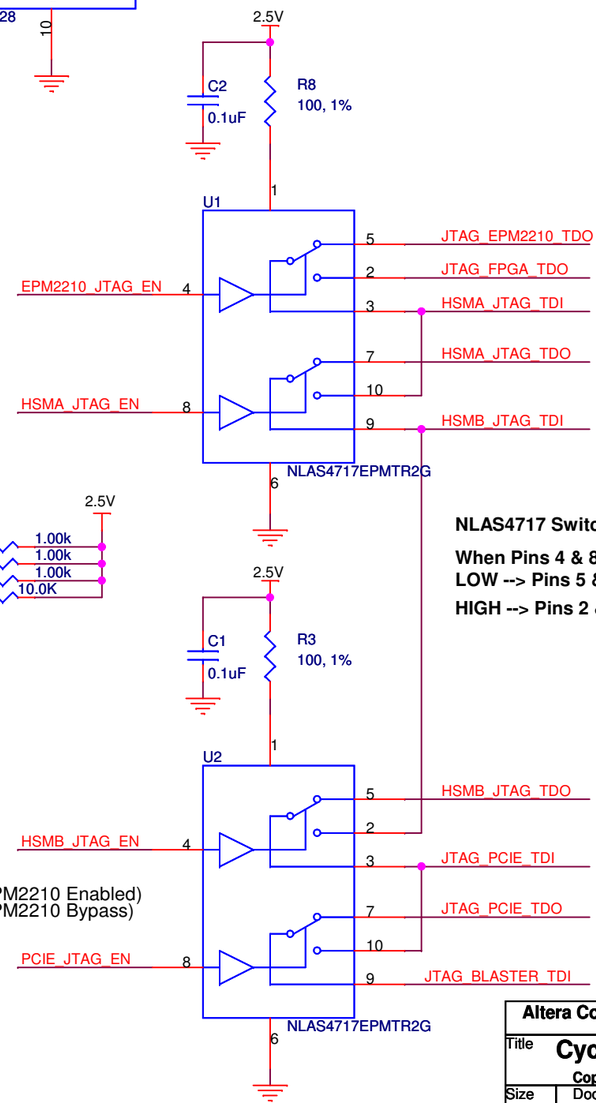












NLAS4717 Switch Functions

When Pins 4 & 8 are:
LOW --> Pins 5 & 7 = ON and Pins 2 & 10 = OFF
HIGH --> Pins 2 &10 = ON and Pins 5 & 7 = OFF

Logic 0 = pin 5 --> pin 3 (EPM2210 Enabled)
Logic 1 = pin 2 --> pin 3 (EPM2210 Bypass)

FPGA Not Installed Jumper

CONFIGURATION INTERFACE

14 FPGA_DATA[7:0]
14 FPGA_DCLK
14,17 FPGA_CONF_DONE
14,18 FPGA_STATUSn
14 FPGA_CONFIGn
14,17 SYS_RESETn
18 FPGA_CEn

JTAG

14,16,18 JTAG_TCK
14,16,18 JTAG_TMS
14 JTAG_FPGA_TDO
18 JTAG_BLASTER_TDO
16 HSMA_JTAG_TDI
16 HSMB_JTAG_TDI
18 JTAG_BLASTER_TDI
14 JTAG_EPM2210_TDO
16 HSMA_JTAG_TDO
16 HSMB_JTAG_TDO
3,18 USB_DISABLEn

USER_LED2 HSMB_TX_D_P4 → USER_LED2 14,17 HSMB_TX_D_P4 16

MSEL0 MSEL2 MSEL3 → MSEL0 14 MSEL2 14 MSEL3 14

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Cyclone IV GX FPGA Development Kit Board**

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Cyclone IV GX Clocks

HSMA_CLK_IN_P1 100, 1% R174 HSMA_CLK_IN_N1
HSMA_CLK_IN_P2 100, 1% R168 HSMA_CLK_IN_N2

PCIE_REFCLK_P R268 0 PCIE_REFCK_P
PCIE_REFCLK_N R267 0 PCIE_REFCK_N

C383 0.1uF
CLKA_IN_P0 — CLKA_IN_C_P0
R208 49.9
2.5V — R216 1.00k — N66134802
R210 1.00k
R209 49.9
C384 0.1uF
CLKA_IN_N0 — CLKA_IN_C_N0

C385 0.1uF
CLKA_IN_P1 — CLKA_IN_C_P1
R206 49.9
2.5V — R212 1.00k — N66160004
R207 1.00k
R205 49.9
C386 0.1uF
CLKA_IN_N1 — CLKA_IN_C_N1

C69 0.1uF
CLKIN_125M_P — CLKIN_C_125M_P
R197 49.9
2.5V — R195 1.00k — N66186150
R196 1.00k
R198 49.9
C70 0.1uF
CLKIN_125M_N — CLKIN_C_125M_N

U10I

Cyclone IV GX Clocks

PCIE_REFCK_P V15
PCIE_REFCK_N W15

CLKA_IN_C_P1 V11
CLKA_IN_C_N1 W11
V12
W12

HSMBT_CLK_IN0 AJ16
CLKIN_T_50 AK16

HSMA_CLK_IN_N2 V30
HSMA_CLK_IN_P2 V29

HSMA_CLK_IN_N1 T30
HSMA_CLK_IN_P1 T29

HSMAT_CLK_IN0 A15
ENET_RX_CLK B15

CLKIN_C_125M_N K15
CLKIN_C_125M_P L15

CLKA_IN_C_P0 L11
CLKA_IN_C_N0 K11
M10
L10

Bank 3A
REFCLK2p/CLKIO12/DIFFCLK_7p
REFCLK2n/CLKIO13/DIFFCLK_7n

Bank 3B
REFCLK0p/DIFFCLK_0p/CLKIO20
REFCLK0n/DIFFCLK_0n
REFCLK1p/DIFFCLK_1p/CLKIO22
REFCLK1n/DIFFCLK_1n

Bank 3
PLL1_CLKOUT9 AE6
PLL1_CLKOUTn AF6
PLL5_CLKOUTp AF7 HSMB_TX_D_N11
PLL5_CLKOUTn AG6
PLL6_CLKOUTp AE9 FSM_D3
PLL6_CLKOUTn AF9 HSMB_TX_D_N12

Bank 4
CLKIO14/DIFFCLK_6p PLL3_CLKOUTp AF24 CLKOUT_SMA
CLKIO15/DIFFCLK_6n PLL3_CLKOUTn AF25 HSMB_TX_D_P16

Bank 5
CLKIO4/DIFFCLK_2n
CLKIO5/DIFFCLK_2p

Bank 6
CLKIO6/DIFFCLK_3n PLL4_CLKOUTp D27 SSRAM_BBn
CLKIO7/DIFFCLK_3p PLL4_CLKOUTn C27 LCD_DATA4

Bank 7
CLKIO8/DIFFCLK_5n
CLKIO9/DIFFCLK_5p

Bank 8A
REFCLK3n/CLKIO10/DIFFCLK_4n
REFCLK3p/CLKIO11/DIFFCLK_4p

Bank 8B
REFCLK4p/DIFFCLK_8p/CLKIO17
REFCLK4n/DIFFCLK_8n
REFCLK5p/DIFFCLK_9p/CLKIO19
REFCLK5n/DIFFCLK_9n

Bank 8
PLL2_CLKOUTp G6 SSRAM_Gn
PLL2_CLKOUTn F6 USER_LED3
PLL7_CLKOUTp G7 ENET_MDIO
PLL7_CLKOUTn F7 FLASH_OEn
PLL8_CLKOUTp G8 MAX_OEn
PLL8_CLKOUTn F8 SSRAM_BWn

EP4CGX150DF896_DDR2_Swap_hsmc
Version = 0.1 Preliminary

SMA Connector

J9
1 CLKOUT_SMA
5 4 3 2

J10
1 CLKIN_SMA
5 4 3 2
R67 49.9
(external clock source)

USER_LED3 — USER_LED3 14,17

FSM_D3 — FSM_D3 13,14
SSRAM_BBn — SSRAM_BBn 13
LCD_DATA4 — LCD_DATA4 17

HSMB_TX_D_N11 — HSMB_TX_D_N11 7
HSMB_TX_D_N12 — HSMB_TX_D_N12 7
HSMB_TX_D_P16 — HSMB_TX_D_P16 5

HSMB_CLK_OUT_P2 — HSMB_CLK_OUT_P2 5
HSMB_T_CLK_OUT_P2 — HSMB_T_CLK_OUT_P2 16

HSMC PORT A
HSMA_TX_D_P[16:0] — HSMA_TX_D_P[16:0] 6,16
HSMA_TX_D_N[16:0] — HSMA_TX_D_N[16:0] 6,16
HSMA_CLK_IN_P[2:1] — HSMA_CLK_IN_P[2:1] 16
HSMA_CLK_IN_N[2:1] — HSMA_CLK_IN_N[2:1] 16
HSMA_CLK_OUT_P[2:1] — HSMA_CLK_OUT_P[2:1] 6,16
HSMA_CLK_OUT_N[2:1] — HSMA_CLK_OUT_N[2:1] 6,16
HSMA_TX_LED — HSMA_TX_LED 7,17
HSMA_CLK_IN0 — HSMA_CLK_IN0 16

HSMC PORT B
HSMB_CLK_IN_P1 — HSMB_CLK_IN_P1 6,16
HSMB_CLK_IN_N[2:1] — HSMB_CLK_IN_N[2:1] 6,16
HSMB_CLK_OUT_P[2:1] — HSMB_CLK_OUT_P[2:1] 5,6,16
HSMB_CLK_OUT_N[2:1] — HSMB_CLK_OUT_N[2:1] 6,16
HSMB_CLK_IN0 — HSMB_CLK_IN0 16

USER INTERFACE
USER_DIPSW[7:0] — USER_DIPSW[7:0] 7,17,20

3 PCIE_REFCLK_P
3 PCIE_REFCLK_N

CLOCK INTERFACE
10 CLKA_IN_P0
10 CLKA_IN_N0
10 CLKA_IN_P1
10 CLKA_IN_N1

10 CLKIN_125M_P
10 CLKIN_125M_N

10,14 CLKIN_50

SSRAM_Gn — SSRAM_Gn 13

FLASH_OEn — FLASH_OEn 13,14
MAX_OEn — MAX_OEn 14
SSRAM_BWn — SSRAM_BWn 13

ENET_MDIO — ENET_MDIO 15
CLKIN_SMA — CLKIN_SMA 7

U30 SN74AVC1T45: VCCA 1, GND 2, A 3, B 4, VCCB 6, DIR 5
1.8V — 0.1uF — 2.5V
HSMBT_CLK_IN0 (output) — HSMB_CLK_IN0 (Input)

U32 SN74AVC1T45: VCCA 1, GND 2, A 3, B 4, VCCB 6, DIR 5
1.8V — 2.5V
HSMAT_CLK_IN0 (output) — HSMA_CLK_IN0 (Input)

U22 SN74AVC1T45: VCCA 1, GND 2, A 3, B 4, VCCB 6, DIR 5
1.8V — 0.1uF — 2.5V
CLKIN_T_50 (output) — CLKIN_50 (Input)

U34 SN74AVC1T45: VCCA 1, GND 2, A 3, B 4, VCCB 6, DIR 5
2.5V — 1.8V
HSMB_T_CLK_OUT_P2 (output) — HSMB_CLK_OUT_P2 (Input)

U20 SN74AVC1T45: VCCA 1, GND 2, A 3, B 4, VCCB 6, DIR 5
1.8V — 2.5V
ENET_RX_CLK (output) — ENET_T_RX_CLK (Input)

ENET_T_RX_CLK 15

C125 0.1uF (2.5V) C126 0.1uF (1.8V)
C123 0.1uF (2.5V) C128 0.1uF (1.8V)
C117 0.1uF (2.5V) C132 0.1uF (1.8V)
C354 0.1uF (2.5V) C355 0.1uF (1.8V)
C86 0.1uF (2.5V) C85 0.1uF (1.8V)

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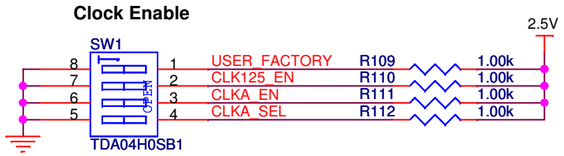
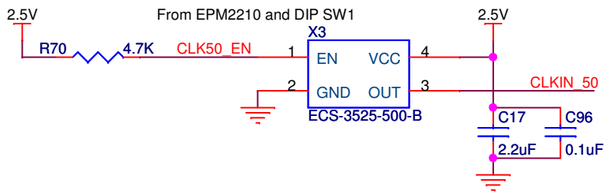
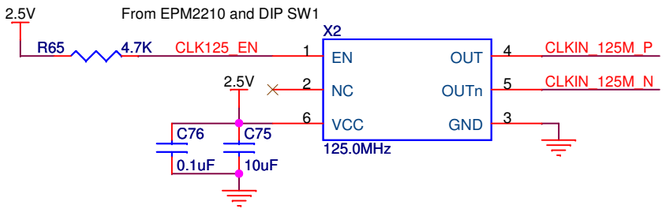
General Clock Circuitry

Clock Enable

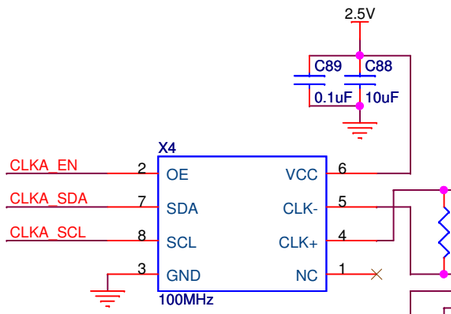


NIOS CPU Clock

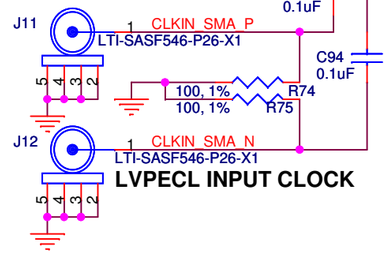


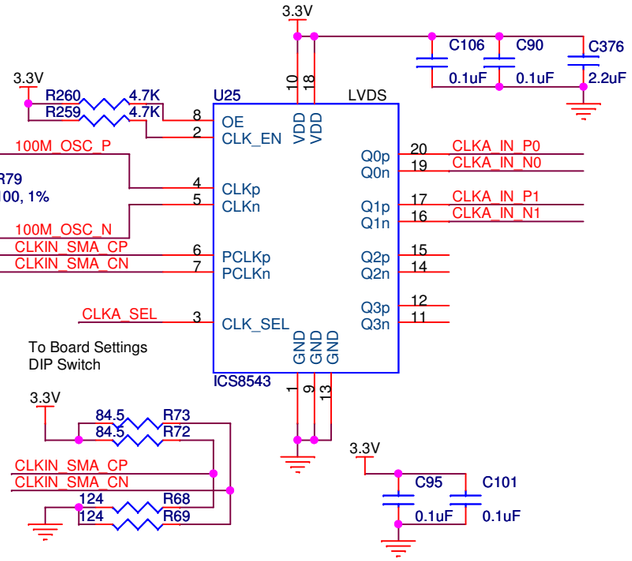


From EPM2210



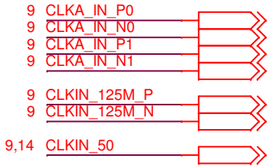
To FPGA and EPM2210





To Board Settings DIP Switch

CLOCK INTERFACE



From EPM2210

CLKA_SEL Settings:

Setting	SWx, DIP4
High	PCLKp/n
Low	CLKp/n

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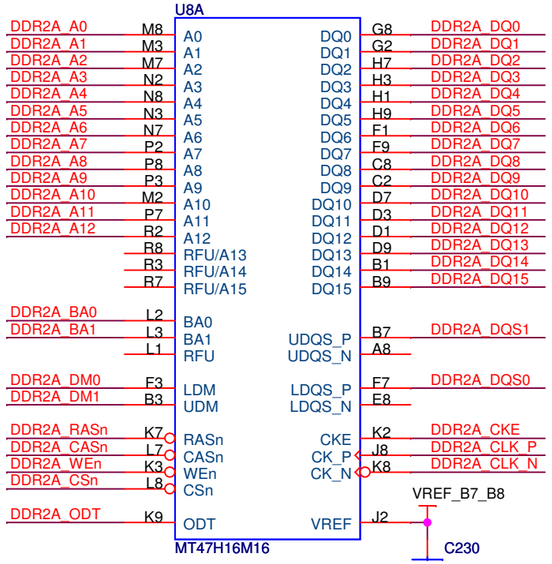
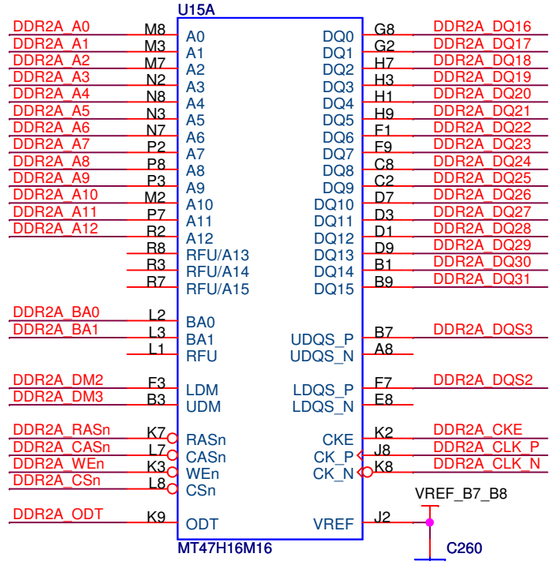
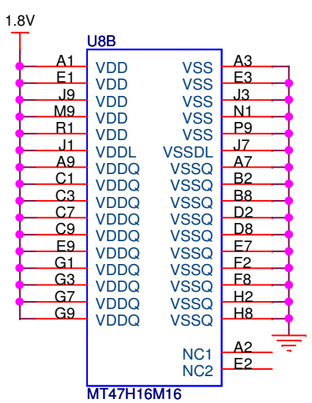
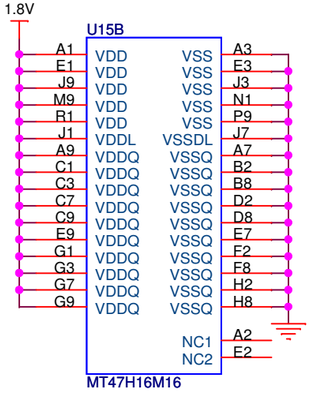
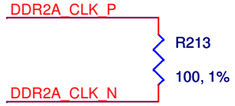
DDR2 SDRAM x32 TOP

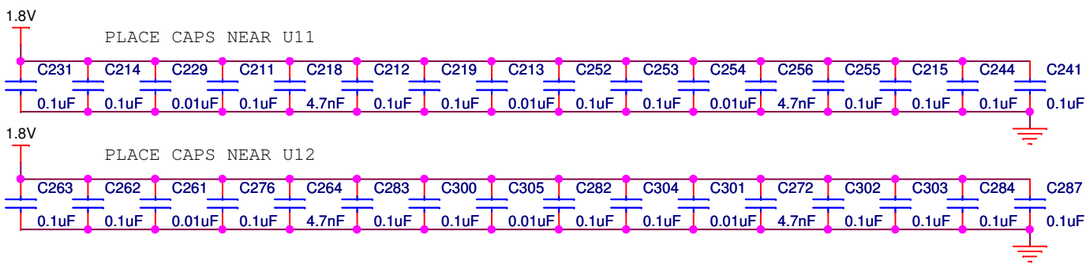


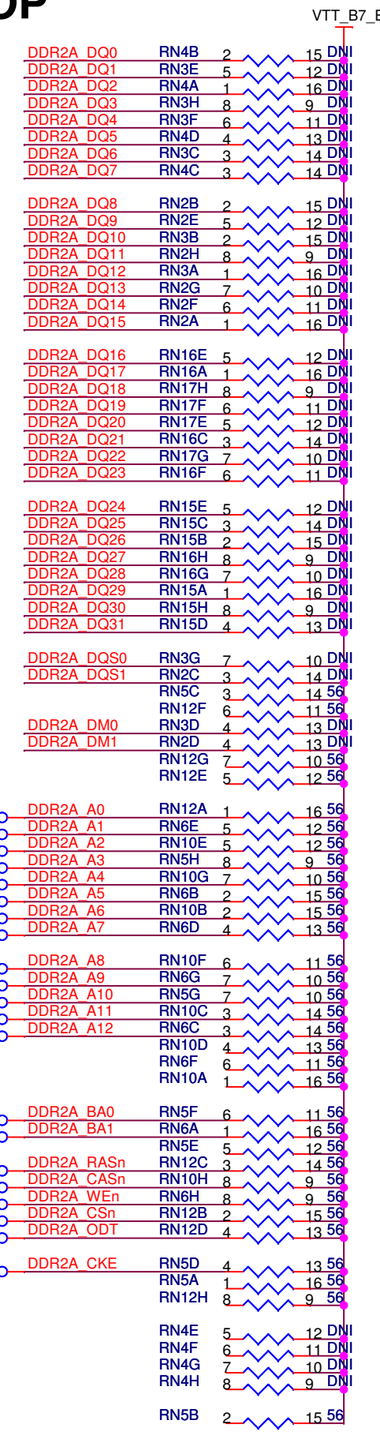


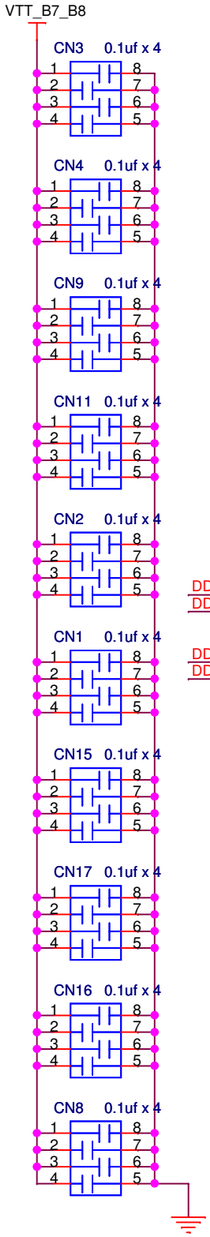




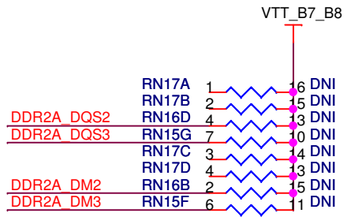








7 DDR2A_DQ[31:0]
7 DDR2A_DQS[3:0]
7 DDR2A_DM[3:0]
7 DDR2A_A[12:0]
7 DDR2A_BA[1:0]
7 DDR2A_RASn
7 DDR2A_CASn
7 DDR2A_WEn
7 DDR2A_CSn
7 DDR2A_ODT
7 DDR2A_CKE
7 DDR2A_CLK_P
7 DDR2A_CLK_N



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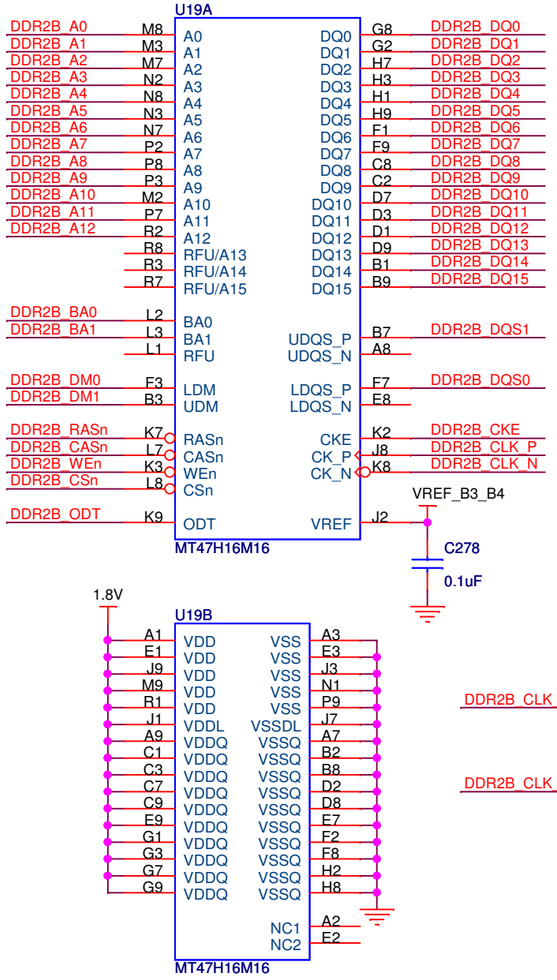
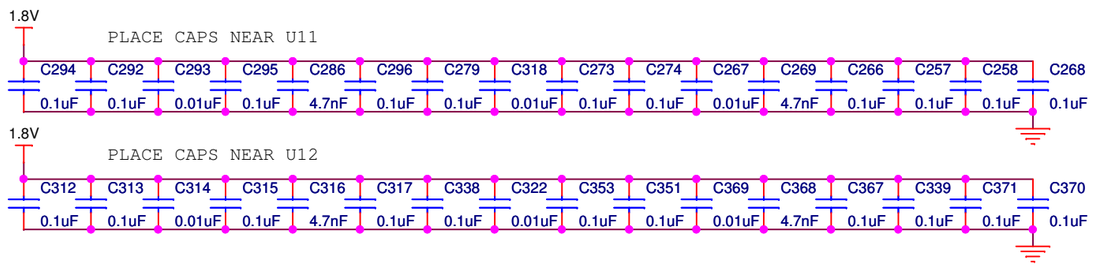
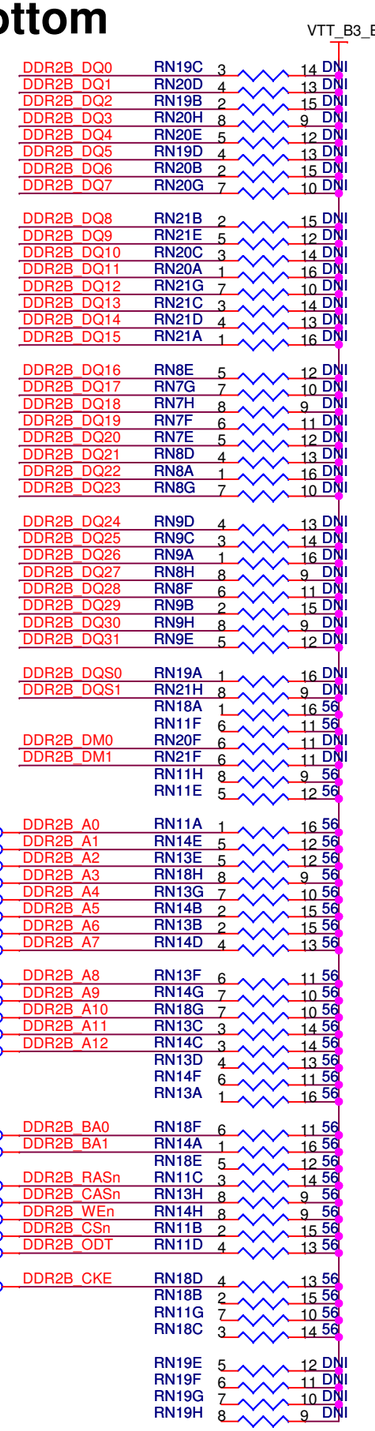
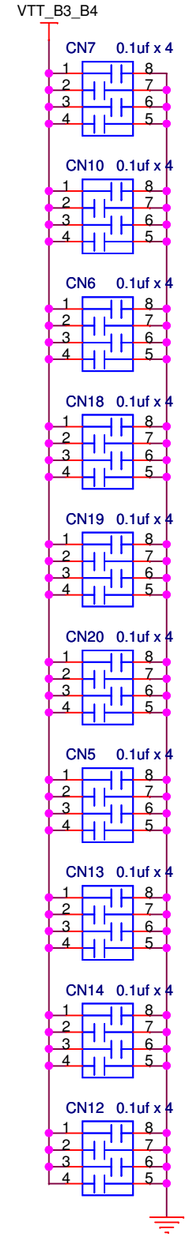
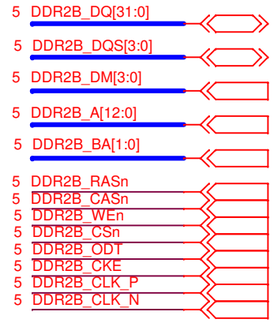
DDR2 SDRAM x32 Bottom

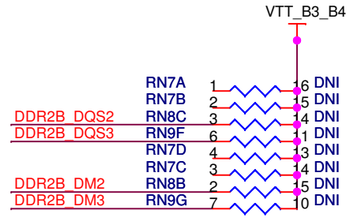












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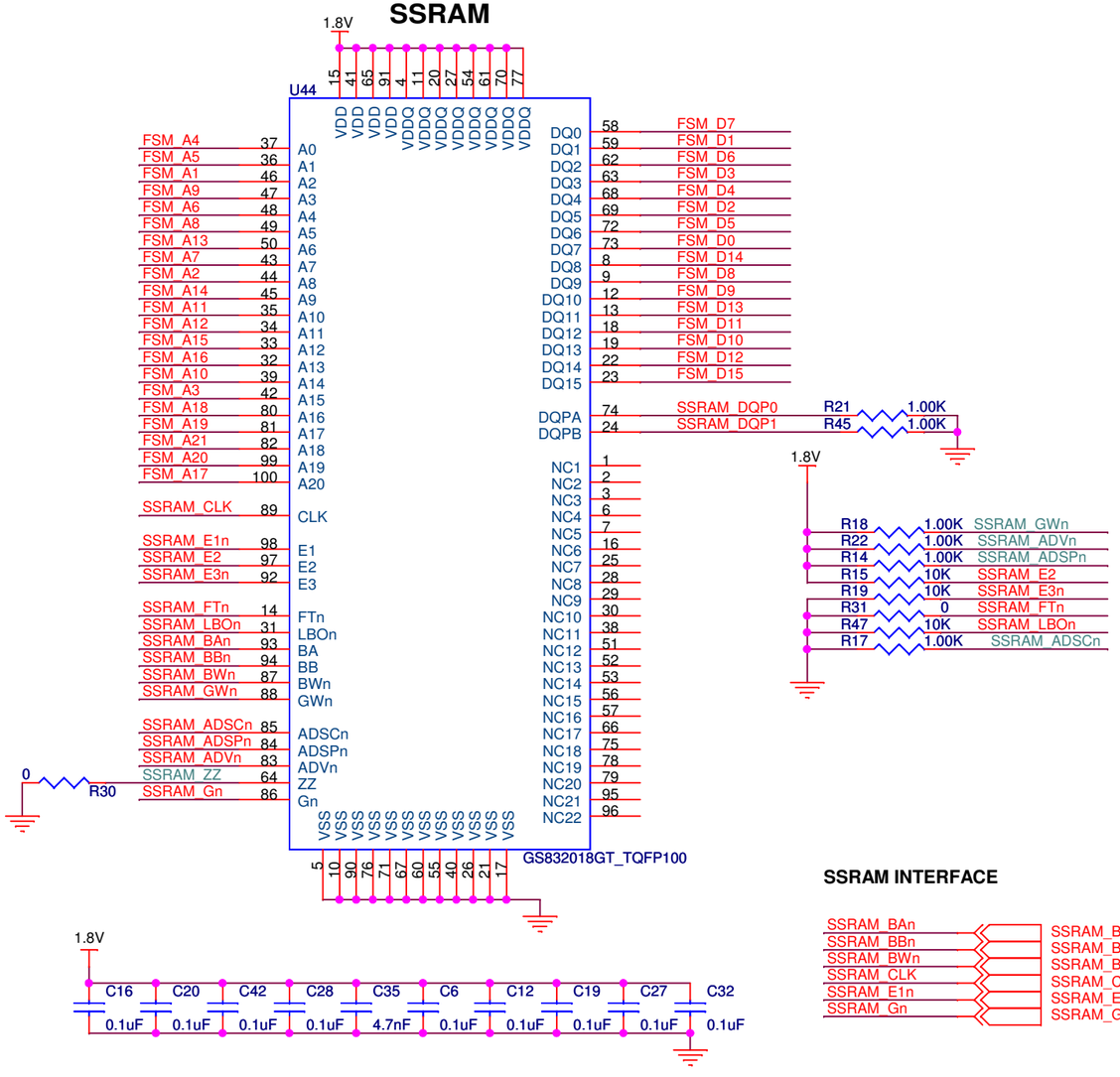
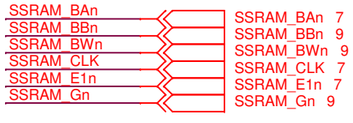
SSRAM & FLASH

SSRAM



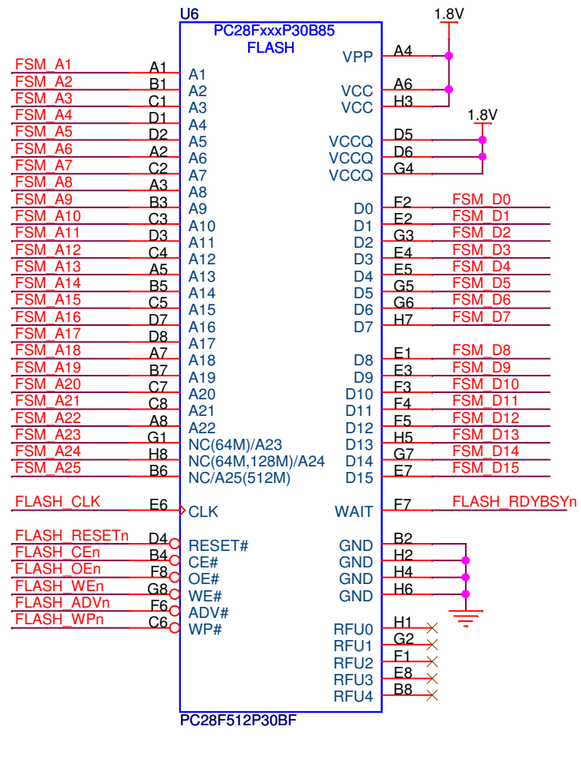
SSRAM INTERFACE



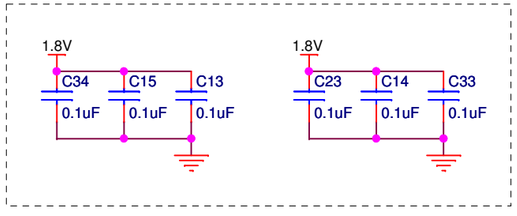

```
assign ssram_gwn = 1'b1; // HIGH Global Write Enable—Writes all bytes; active low
assign ssram_advn = 1'b1; // HIGH
assign ssram_adscn = 1'b0; // LOW
assign ssram_adspn = 1'b1; // HIGH
```

FLASH

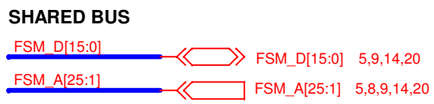
FLASH 512Mb (32M X 16)



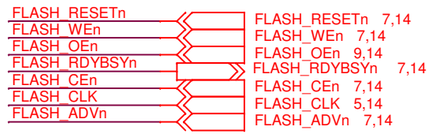
PLACE NEAR FLASH

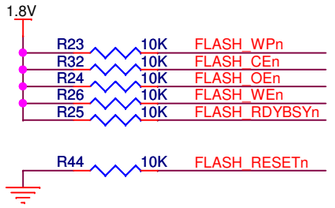


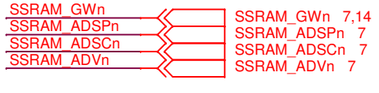
SHARED BUS



FLASH INTERFACE







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MAX II

U7A — MAX II BANK1

FPGA_DATA0	D3	IOB1_1	IOB1_25	H3	CLKA_EN
FPGA_DCLK	C2	IOB1_2	IOB1_26	J1	CLKA_SDA
FPGA_CONF_DONE	E3	IOB1_3	IOB1_27	H4	CLKA_SCL
FPGA_STATUSn	C3	IOB1_4	IOB1_28	J2	CLK125_EN
FPGA_CONFIGn	E4	IOB1_5	IOB1_29	J4	
	D2	IOB1_6	IOB1_30	K1	
	E5	IOB1_7	IOB1_31	J3	
	D1	IOB1_8	IOB1_32	K2	
	F3	IOB1_9			
SENSE_SDO	E2	IOB1_10	IOB1_34	L1	FPGA_DATA1
SENSE_SDI	F4	IOB1_11	IOB1_35	K5	
SENSE_SCK	E1	IOB1_12	IOB1_36	L2	MSEL0
SENSE_CSn	F5	IOB1_13	IOB1_37	K4	
	F2	IOB1_14	IOB1_38	M1	MSEL2
	F6	IOB1_15	IOB1_39	K3	
	F1	IOB1_16	IOB1_40	M2	MSEL3
17 MAX_EPCS	MAX_EPCS G3	IOB1_17	IOB1_41	L5	
	MAX_ERROR G2	IOB1_18	IOB1_42	M3	
	MAX_FACTORY G4	IOB1_19	IOB1_43	L4	
	MAX_USER G1	IOB1_20	IOB1_44	N1	USER_FACTORY
	HSMA_PSNTn G5	IOB1_21	IOB1_45	L3	
	HSMB_PSNTn H2	IOB1_22	IOB1_46	N2	
			IOB1_47	M4	
	H1	IOB1_24	IOB1_48	N3	
			IOB1_49	P2	FAN_CNTL
CLKIN_50	H5	IOB1/GCLK0	TCK	P3	JTAG_TCK
CLKIN_MAX_100	J5	IOB1/GCLK1	TDI	L6	JTAG_FPGA_TDO
			TDO	M5	JTAG_EPM2210_TDO
			TMS	N4	JTAG_TMS

EPM2210GF256FBGA

U7B — MAX II BANK2

C13	IOB2_50	IOB2_74	E9	FSM_D0
B16	IOB2_51	IOB2_75	A9	FSM_D1
C12	IOB2_52	IOB2_76	A8	FSM_D5
A15	IOB2_53	IOB2_77	B8	FSM_D9
D12	IOB2_54	IOB2_78	E8	FSM_D8
B14	IOB2_55	IOB2_79	A7	FSM_D12
C11	IOB2_56	IOB2_80	D8	FSM_D10
B13	IOB2_57	IOB2_81	B7	FSM_D3
D11	IOB2_58	IOB2_82	C8	FSM_D13
A13	IOB2_59	IOB2_83	A6	FSM_D4
E11	IOB2_60			
B12	IOB2_61	IOB2_85	B6	FSM_D7
C10	IOB2_62	IOB2_86	E7	FSM_D2
A12	IOB2_63	IOB2_87	A5	FSM_D15
D10	IOB2_64	IOB2_88	D7	FSM_D11
B11	IOB2_65	IOB2_89	B5	FSM_D14
E10	IOB2_66	IOB2_90	C7	FSM_D6
A11	IOB2_67	IOB2_91	A4	
		IOB2_92	E6	
B10	IOB2_69	IOB2_93	B4	
C9	IOB2_70	IOB2_94	D6	
A10	IOB2_71	IOB2_95	C4	
D9	IOB2_72	IOB2_96	C6	
B9	IOB2_73	IOB2_97	B3	
		IOB2_98	C5	
		IOB2_99	A2	
		IOB2_100	D5	
		IOB2_101	B1	MAX_FAN
		IOB2_102	D4	

EPM2210GF256FBGA

U7C — MAX II BANK3

USER_LED0	P14	IOB3_103	IOB3_127	J16	FPGA_DATA2
USER_LED1	N13	IOB3_104	IOB3_128	J13	FPGA_DATA3
USER_LED2	P15	IOB3_105	IOB3_129	H16	FPGA_DATA4
USER_LED3	M14	IOB3_106	IOB3_130	H13	FPGA_DATA5
USER_LED4	N14	IOB3_107	IOB3_131	H15	FPGA_DATA6
USER_LED5	M13	IOB3_108	IOB3_132	H14	FPGA_DATA7
USER_LED6	N15	IOB3_109	IOB3_133	G16	PGM_SEL
USER_LED7	L14	IOB3_110	IOB3_134	G12	PGM_LOAD
	N16	IOB3_111	IOB3_135	G15	
FLASH_ADVn	L13	IOB3_112			
FLASH_RESETn	M15	IOB3_113	IOB3_137	F16	
FLASH_WEn	L12	IOB3_114	IOB3_138	G13	
FLASH_OEn	M16	IOB3_115	IOB3_139	F15	
FLASH_RDYBSYn	L11	IOB3_116	IOB3_140	G14	
FLASH_CLK	L15	IOB3_117	IOB3_141	E16	
FLASH_CEn	K14	IOB3_118	IOB3_142	F11	
MAX_CSn	L16	IOB3_119	IOB3_143	E15	
MAX_OEn	K13	IOB3_120	IOB3_144	F12	
MAX_WEn	K15	IOB3_121	IOB3_145	D16	
	K12	IOB3_122	IOB3_146	F13	
	K16	IOB3_123	IOB3_147	D15	
			IOB3_148	F14	
SYS_RESETn	J15	IOB3_125	IOB3_149	D14	
	J14	IOB3_126	IOB3_150	E12	
			IOB3_151	C15	
			IOB3_152	E13	
			IOB3_153	C14	
	J12	IOB3/GLCK2	IOB3_154	E14	
	H12	IOB3/GCLK3	IOB3_155	D13	

EPM2210GF256FBGA

U7D — MAX II BANK4

FSM_A11	P4	IOB4_156	IOB4_180	N9
FSM_A19	R1	IOB4_157	IOB4_181	T8
FSM_A12	P5	IOB4_158	IOB4_182	T9
FSM_A21	T2	IOB4_159	IOB4_183	R9
FSM_A15	N5	IOB4_160	IOB4_184	P9
FSM_A5	R3	IOB4_161	IOB4_185	T10
FSM_A7	P6	IOB4_162		
FSM_A4	R4	IOB4_163	IOB4_187	R10
FSM_A10	N6	IOB4_164	IOB4_188	M10
FSM_A23	T4	IOB4_165	IOB4_189	T11
FSM_A16	M6	IOB4_166	IOB4_190	N10
FSM_A3	R5	IOB4_167	IOB4_191	R11
FSM_A1	P7	IOB4_168	IOB4_192	P10
FSM_A18	T5	IOB4_169	IOB4_193	T12
FSM_A17	N7	IOB4_170	IOB4_194	M11
FSM_A2	R6	IOB4_171	IOB4_195	R12
FSM_A20	M7	IOB4_172	IOB4_196	N11
FSM_A14	T6	IOB4_173	IOB4_197	T13
			IOB4_198	P11
FSM_A9	R7	IOB4_175	IOB4_199	R13
FSM_A8	P8	IOB4_176	IOB4_200	M12
FSM_A22	T7	IOB4_177	IOB4_201	R14
FSM_A13	N8	IOB4_178	IOB4_202	N12
FSM_A24	R8	IOB4_179	IOB4_203	T15
			IOB4_204	P12
FSM_A25	M9	IOB4/DEV_CLRn	IOB4_205	R16
FSM_A6	M8	IOB4/DEV_OE	IOB4_206	P13

EPM2210GF256FBGA

U7E — MAX II Power

H7	GNDINT	VCCINT	H8
H9	GNDINT	VCCINT	H10
J8	GNDINT	VCCINT	J7
J10	GNDINT	VCCINT	J9
G6	GNDINT	VCCINT	K6
F7	GNDINT	VCCINT	L7
K11	GNDINT	VCCINT	G11
L10	GNDINT	VCCINT	F10
A1	GNDIO	VCCIO1	C1
A16	GNDIO	VCCIO1	H6
B2	GNDIO	VCCIO1	J6
B15	GNDIO	VCCIO1	P1
G7	GNDIO		
G8	GNDIO	VCCIO2	A3
G9	GNDIO	VCCIO2	A14
G10	GNDIO	VCCIO2	F8
K7	GNDIO	VCCIO2	F9
K8	GNDIO		
K9	GNDIO	VCCIO3	C16
K10	GNDIO	VCCIO3	H11
R2	GNDIO	VCCIO3	J11
R15	GNDIO	VCCIO3	P16
T1	GNDIO		
T16	GNDIO	VCCIO4	L8
		VCCIO4	L9
		VCCIO4	T3
		VCCIO4	T14

EPM2210GF256FBGA

1.8V, 2.5V

Power

2.5V — R13 1.00K — C4 0.01uF

Y1 100MHz (EN, GND, VCC, OUT)

2.5V — L1 BLM15AG221SN1 — CLKIN_MAX_100 — C7 0.01uF — C8 4.7uF

MSEL0 MSEL2 MSEL3

MSEL0 8
MSEL2 8
MSEL3 8

USER INTERFACE

USER_LED[7:0] — USER_LED[7:0] 7,8,9,17

19 USER_FACTORY

SHARED BUS

5,9,13,20 FSM_D[15:0]
5,8,9,13,20 FSM_A[25:1]

FLASH INTERFACE

7,13 FLASH_RESETn
7,13 FLASH_WEn
9,13 FLASH_OEn
7,13 FLASH_RDYBSYn
5,13 FLASH_CLK
7,13 FLASH_CEn
7,13 FLASH_ADVn

CONFIGURATION INTERFACE

8,16,18 JTAG_TCK
8,16,18 JTAG_TMS
8 JTAG_EPM2210_TDO
8 JTAG_FPGA_TDO
8 FPGA_DATA[7:0]
8 FPGA_DCLK
8,17 FPGA_CONF_DONE
8,18 FPGA_STATUSn
8 FPGA_CONFIGn
7,16 HSMA_PSNTn
7,16 HSMB_PSNTn

CURRENT SENSE

19 SENSE_SDO
19 SENSE_SDI
19 SENSE_SCK
19 SENSE_CSn
19 FAN_CNTL

CLOCK INTERFACE

10 CLKA_SDA
10 CLKA_SCL
10 CLKA_EN
10 CLK50_EN
10 CLK125_EN
9,10 CLKIN_50
8 MAX_CLK

USER I/O's

17 PGM_LOAD
17 PGM_SEL
17 MAX_ERROR
17 MAX_FAN
17 MAX_FACTORY
17 MAX_USER
8,17 SYS_RESETn
19 FAN_CNTL
7 MAX_CSn
9 MAX_OEn
7 MAX_WEn

Place near MAX II

1.8V: C195 C206 C191 C164 C227 C165 C163 C226 C208 — 0.1uF

2.5V: C217 C175 C199 — 0.1uF

1.8V: C173 C216 C196 C197 C174 C207 C198 C204 — 0.1uF

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10/100/1000 Ethernet

RGMII Mode (default)

removed ENET_TX_CLK signal, Atached to ground

2.5V
R62 4.7K ENET_T_MDIO
R61 4.7K ENET_T_MDC
R63 4.7K ENET_T_INTN
R64 4.7K ENET_T_RESETn

C68 0.01uF R60 49.9 MDI_P0
C67 0.01uF R59 49.9 MDI_N0
C104 0.01uF R57 49.9 MDI_P1
C105 0.01uF R58 49.9 MDI_N1
R80 49.9 MDI_P2
R81 49.9 MDI_N2
R83 49.9 MDI_P3
R82 49.9 MDI_N3

J7 HFJ11-1G02E
VCC 9
TD0_P 1
TD0_N 2
TD1_P 3
TD1_N 6
TD2_P 4
TD2_N 5
TD3_P 7
TD3_N 8
GND 10
GND_TAB 12
GND_TAB 11

3.3V
R76 10.0K

X5 25MHz
EN 1
NC1 2
GND 3
OUT 4
NC2 5
VCC 6
ENET_XTAL_25MHZ
3.3V

R66 4.99K
R71 4.7K

U21A 88E1111

ENET_T_RESETn	28	RESET_N	
	27	COMA	
ENET_LED_RX	65	CONFIG0	
ENET_LED_LINK10	64	CONFIG1	
	63	CONFIG2	
ENET_LED_TX	61	CONFIG3	
	60	CONFIG4	
ENET_LED_LINK10	59	CONFIG5	
	58	CONFIG6	
MDI_P0	29	MDI0_P	MDI INTERFACE
MDI_N0	31	MDI0_N	
MDI_P1	33	MDI1_P	
MDI_N1	34	MDI1_N	
MDI_P2	39	MDI2_P	
MDI_N2	41	MDI2_N	
MDI_P3	42	MDI3_P	
MDI_N3	43	MDI3_N	
ENET_T_MDIO	24	MDIO	MGMT
ENET_T_MDC	25	MDC	
ENET_T_INTN	23	INT_N	
	37	HSDAC_P	TEST
	38	HSDAC_N	
ENET_RSET	30	RSET	
	56	SEL_FREQ	
ENET_XTAL_25MHZ	22	125CLK	
	55	XTAL1	
	54	XTAL2	
	53	VSSC	
	47	TRST_N	JTAG
	49	TCK	
	44	TDI	
	50	TDO	
	46	TMS	

GMII/MII/TBI INTERFACE

GTX_CLK	8	ENET_T_GTX_CLK
TX_CLK	4	
TX_EN	9	ENET_T_TX_EN
TX_ER	7	
TXD0	11	ENET_T_TX_D0
TXD1	12	ENET_T_TX_D1
TXD2	14	ENET_T_TX_D2
TXD3	16	ENET_T_TX_D3
TXD4	17	
TXD5	18	
TXD6	19	
TXD7	20	
RXCLK	2	ENET_T_RX_CLK
RX_DV	94	ENET_T_RX_DV
RX_ER	3	
RXD0	95	ENET_T_RX_D0
RXD1	92	ENET_T_RX_D1
RXD2	93	ENET_T_RX_D2
RXD3	91	ENET_T_RX_D3
RXD4	90	
RXD5	89	
RXD6	87	
RXD7	86	
CRS	84	
COL	83	

removed ENET_RX_CRS and ENET_RX_COL signals

SGMII INTERFACE

S_CLK_P	79	
S_CLK_N	80	
S_IN_P	82	
S_IN_N	81	
S_OUT_P	77	
S_OUT_N	75	
LED_TX	68	ENET_LED_TX
LED_RX	69	ENET_LED_RX
LED_DUPLEX	70	ENET_LED_DUPLEX
LED_LINK1000	73	ENET_LED_LINK1000
LED_LINK100	74	ENET_LED_LINK100
LED_LINK10	76	ENET_LED_LINK10

U21B 88E1111

26	VDDOX		
48	VDDOX		
5	VDDO		
21	VDDO		
88	VDDO		
96	VDDO		
72	VDDOH		
66	VDDOH		
52	VDDOH		
32	AVDD	DVDD	1
36	AVDD	DVDD	6
35	AVDD	DVDD	10
40	AVDD	DVDD	15
45	AVDD	DVDD	57
78	AVDD	DVDD	62
		DVDD	67
13	NC1	DVDD	71
51	NC2	DVDD	85
97	VSS		

1.1V

U9 MAX3373
1.8V
VL 3
TRI_STATE 6
VL_IO1 5
VL_IO2 4
VCC 7
VCCIO1 8
VCCIO2 1
GND 2
2.5V
ENET_INTN
ENET_RESETn
ENET_T_INTN
ENET_T_RESETn

U14 MAX3373
1.8V
VL 3
TRI_STATE 6
VL_IO1 5
VL_IO2 4
VCC 7
VCCIO1 8
VCCIO2 1
GND 2
2.5V
ENET_MDIO
ENET_MDC
ENET_T_MDIO
ENET_T_MDC

Place near PHY

1.1V
C382 0.1uF
C360 0.1uF
C98 0.1uF
C72 0.1uF
C74 0.1uF

2.5V
C97 0.1uF
C91 0.1uF
C361 0.1uF
C83 0.1uF
C73 0.1uF
C82 0.1uF
C87 0.1uF
C71 0.1uF

ETHERNET RGMII INTERFACE

7 ENET_T_RX_D[3:0]
9 ENET_T_RX_CLK
7 ENET_T_RX_DV

removed ENET_CRS

7 ENET_T_TX_D[3:0]
7 ENET_T_GTX_CLK
7 ENET_T_TX_EN

ETHERNET CONTROL INTERFACE

7 ENET_RESETn
7 ENET_INTn
7 ENET_MDC
9 ENET_MDIO

2.5V

ENET_LED_TX R266 220 D30 Green_LED
ENET_LED_RX R265 220 D31 Green_LED

removed ENET_LED_ACTIVITY with r445 and D6

ENET_LED_DUPLEX R261 220 D27 Green_LED
ENET_LED_LINK1000 R264 220 D24 Green_LED
ENET_LED_LINK100 R263 220 D25 Green_LED
ENET_LED_LINK10 R262 220 D26 Green_LED

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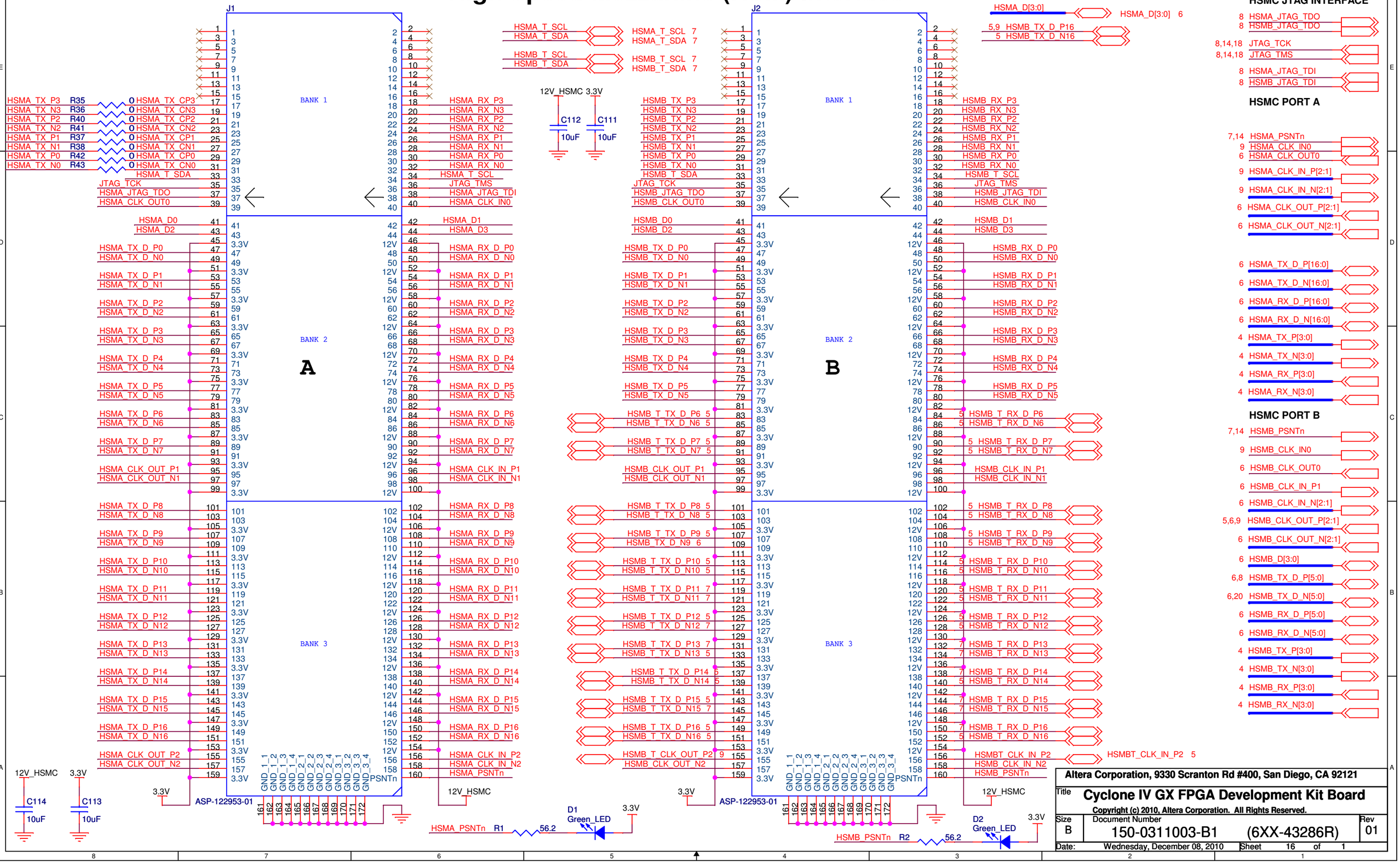
High Speed Mezzanine (HSM) Interface



HSMC JTAG INTERFACE

8 HSMA_JTAG_TDO
8 HSMB_JTAG_TDO
8,14,18 JTAG_TCK
8,14,18 JTAG_TMS
8 HSMA_JTAG_TDI
8 HSMB_JTAG_TDI

HSMC PORT A

7,14 HSMA_PSNTn
9 HSMA_CLK_IN0
6 HSMA_CLK_OUT0
9 HSMA_CLK_IN_P[2:1]
9 HSMA_CLK_IN_N[2:1]
6 HSMA_CLK_OUT_P[2:1]
6 HSMA_CLK_OUT_N[2:1]
6 HSMA_TX_D_P[16:0]
6 HSMA_TX_D_N[16:0]
6 HSMA_RX_D_P[16:0]
6 HSMA_RX_D_N[16:0]
4 HSMA_TX_P[3:0]
4 HSMA_TX_N[3:0]
4 HSMA_RX_P[3:0]
4 HSMA_RX_N[3:0]

HSMC PORT B

7,14 HSMB_PSNTn
9 HSMB_CLK_IN0
6 HSMB_CLK_OUT0
6 HSMB_CLK_IN_P1
6 HSMB_CLK_IN_N[2:1]
5,6,9 HSMB_CLK_OUT_P[2:1]
6 HSMB_CLK_OUT_N[2:1]
6 HSMB_D[3:0]
6,8 HSMB_TX_D_P[5:0]
6,20 HSMB_TX_D_N[5:0]
6 HSMB_RX_D_P[5:0]
6 HSMB_RX_D_N[5:0]
4 HSMB_TX_P[3:0]
4 HSMB_TX_N[3:0]
4 HSMB_RX_P[3:0]
4 HSMB_RX_N[3:0]

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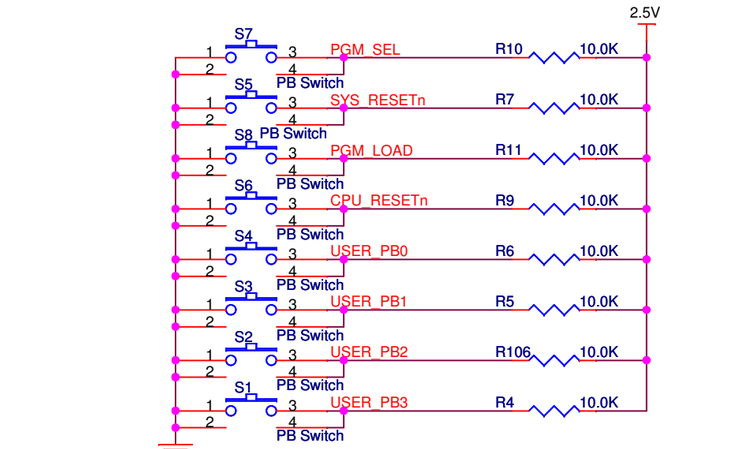
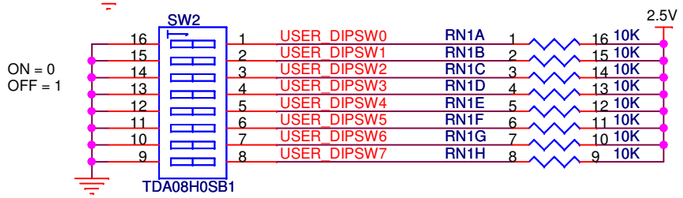
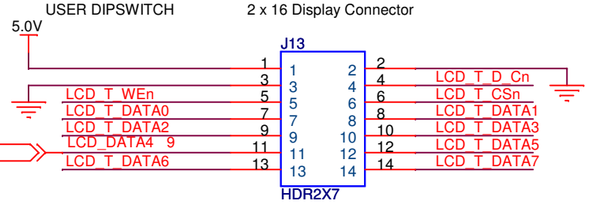
User IO & Connector

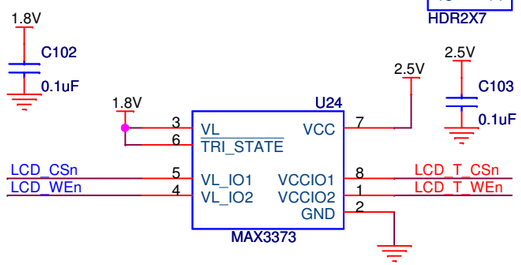


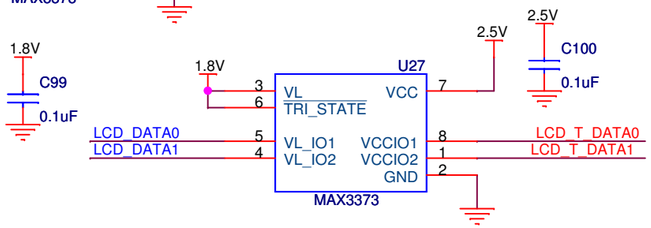


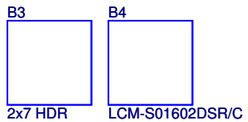
USER DIPSWITCH

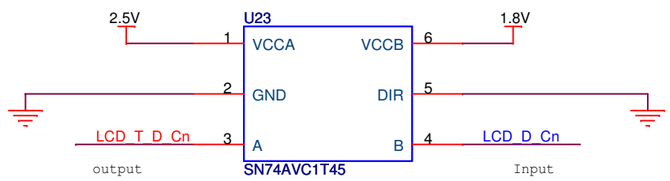
2 x 16 Display Connector

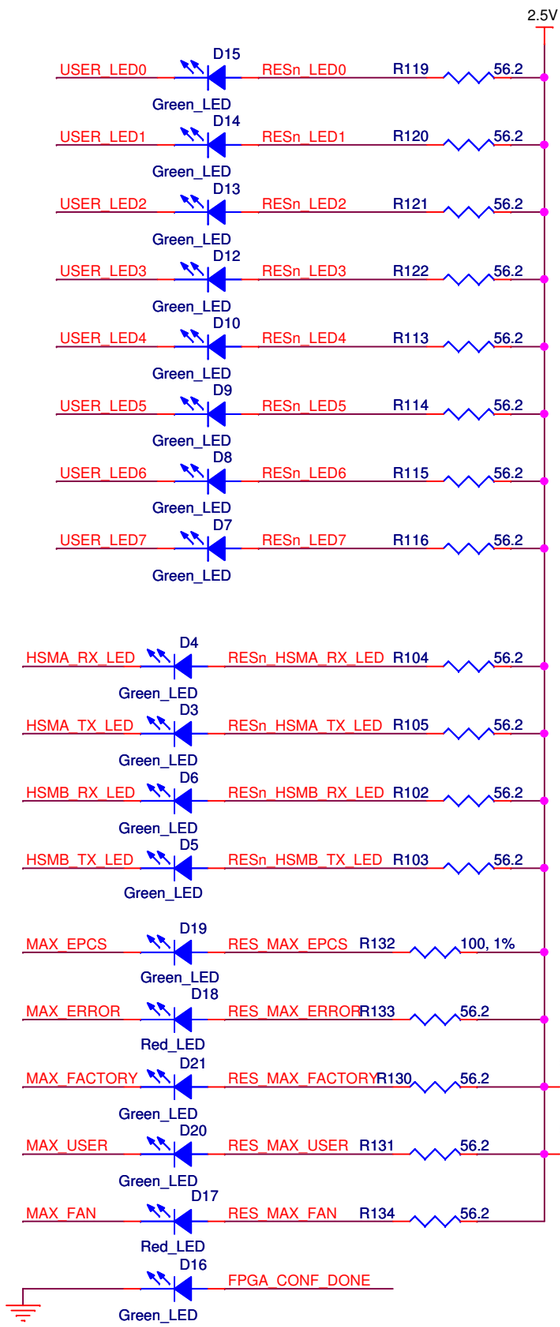


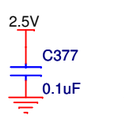


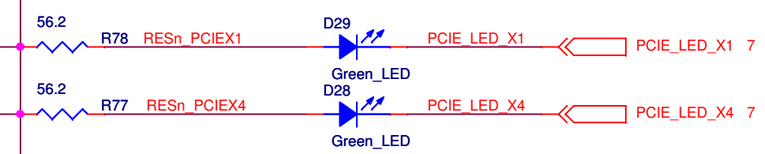




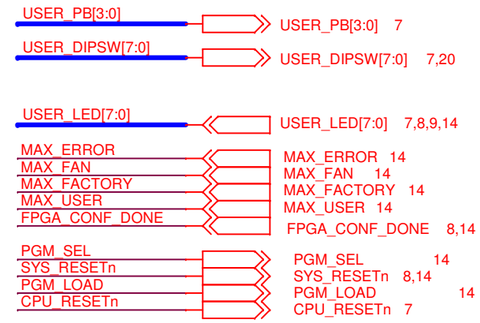




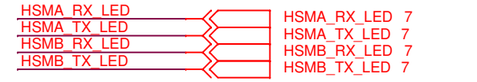




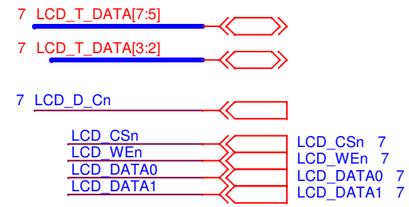
USER I/O's



HSMC INTERFACE



LCD DISPLAY INTERFACE



MAX_EPCS — MAX_EPCS 14

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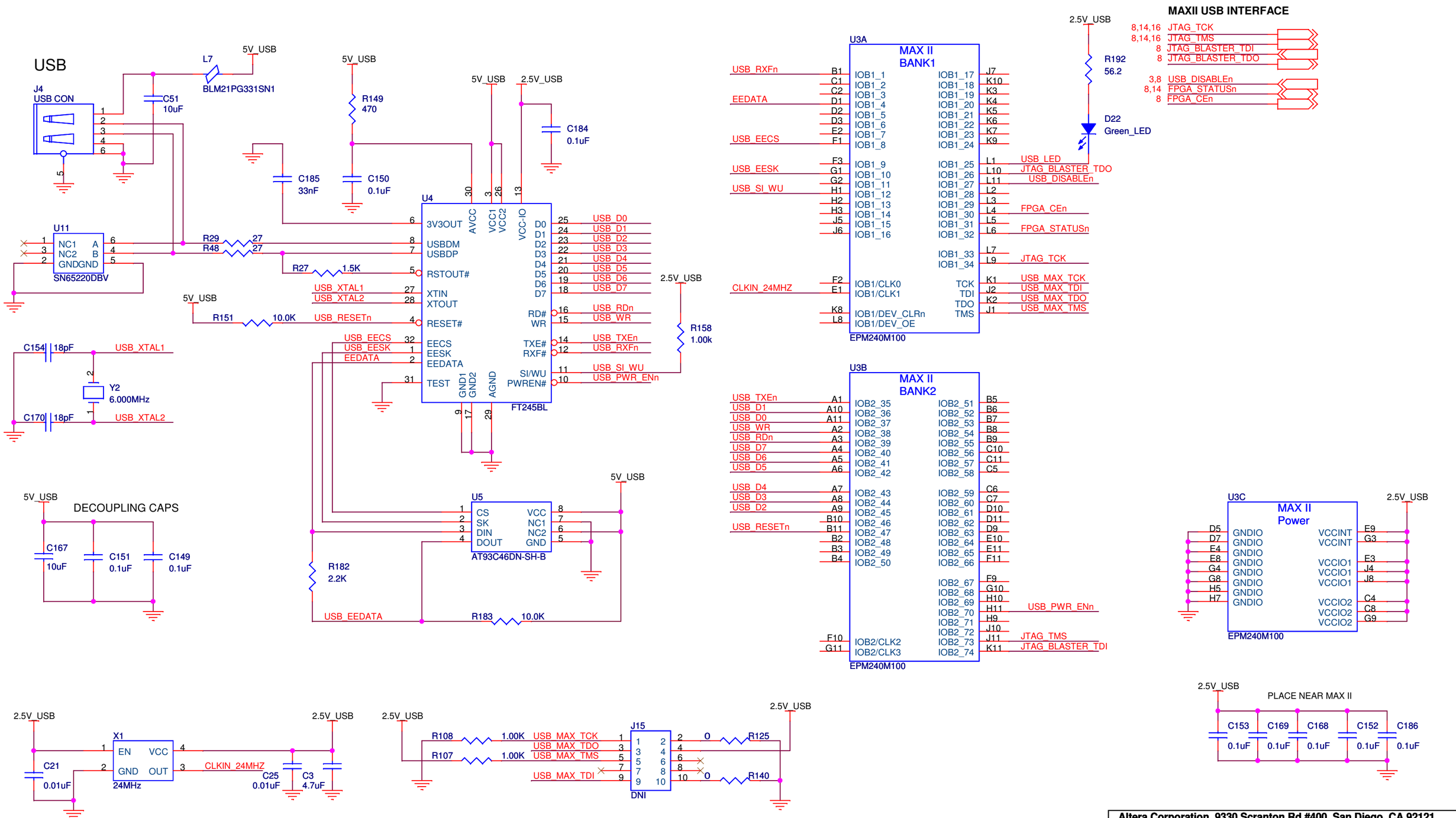
Embedded USB Blaster



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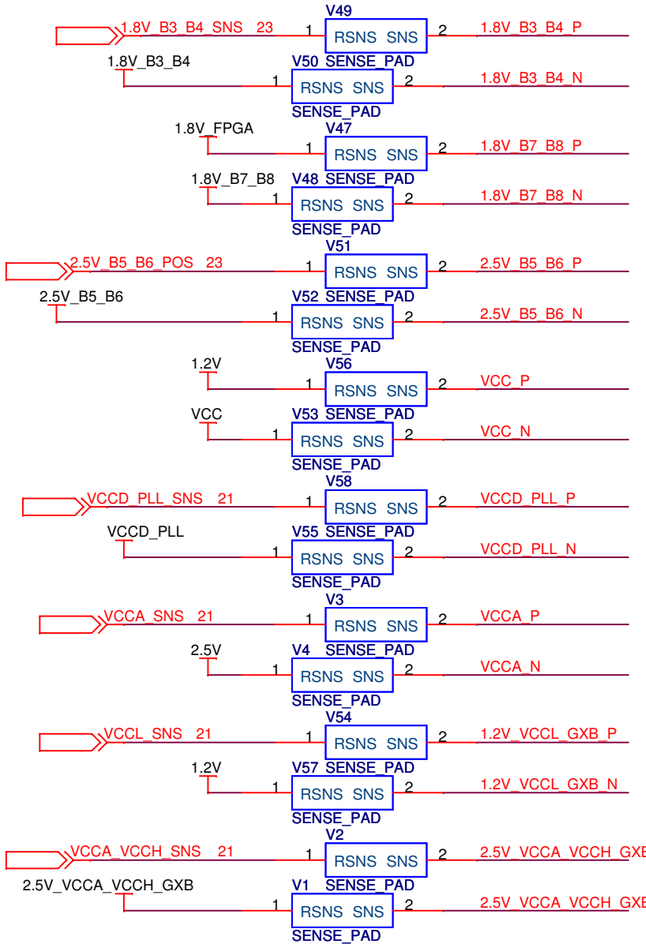
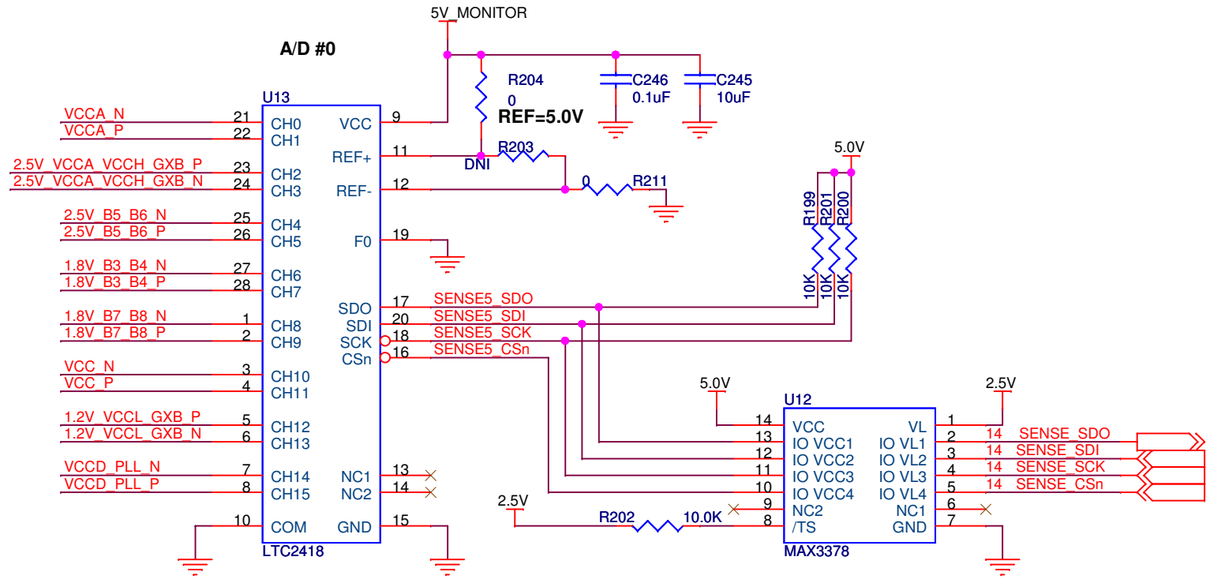
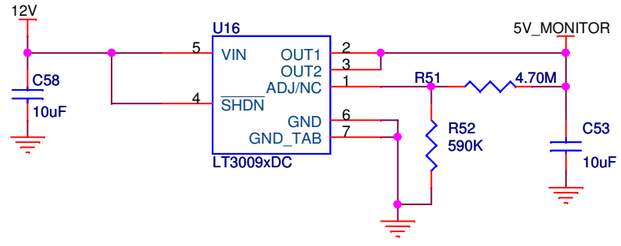
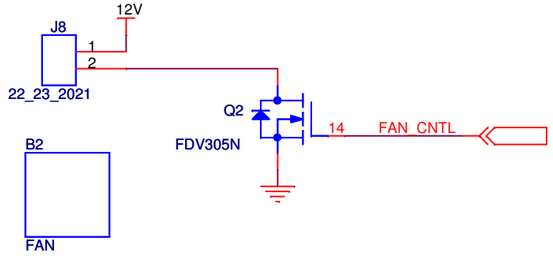
Power Monitor







Fan Power Header



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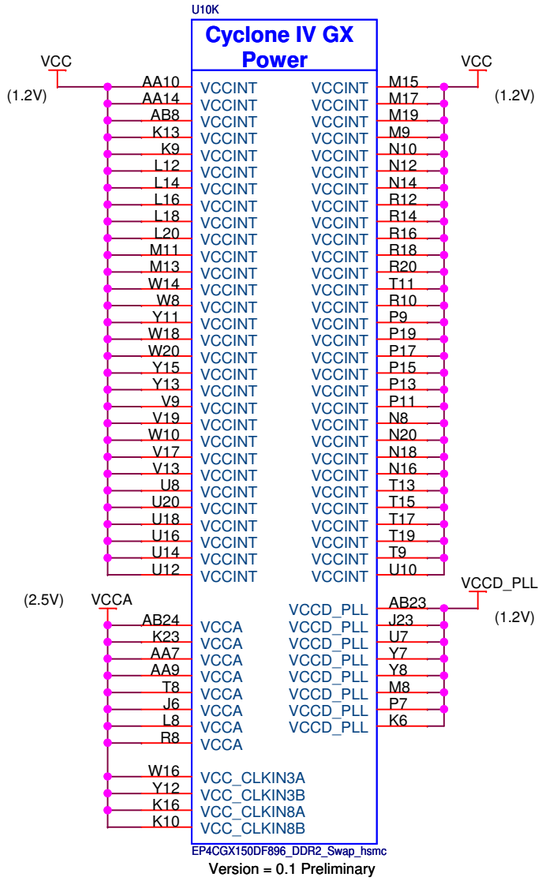
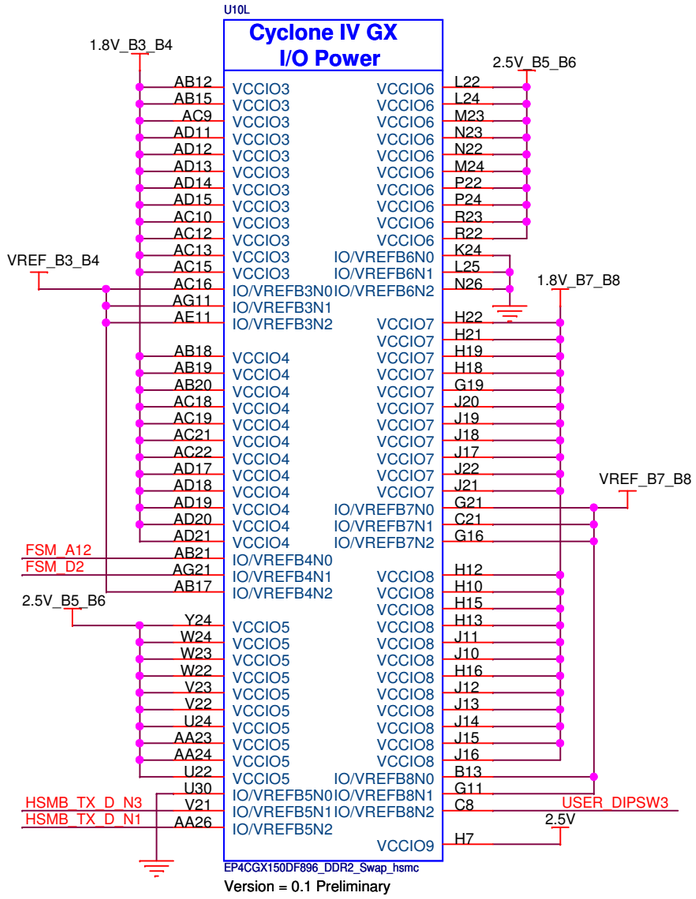
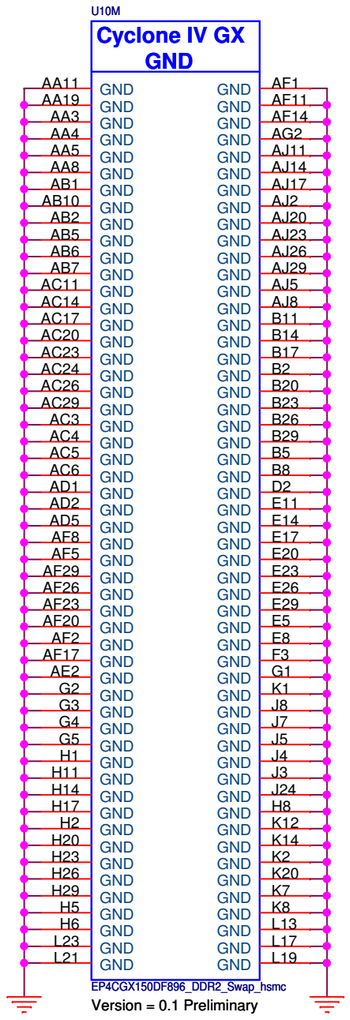
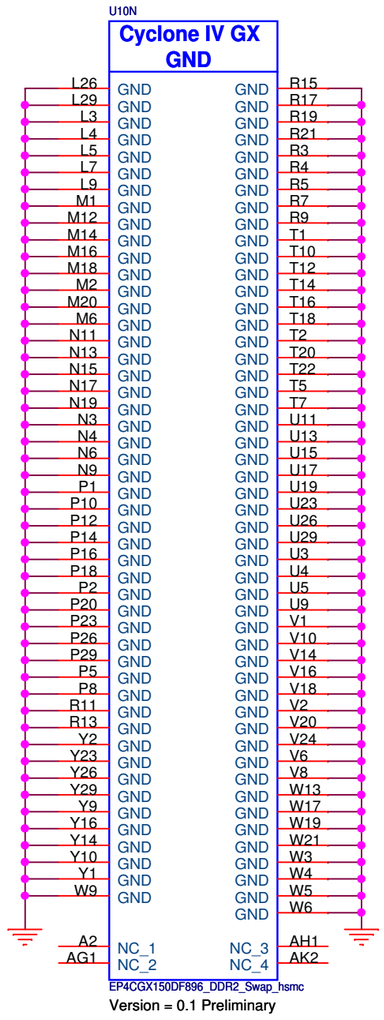
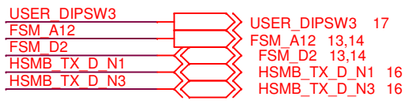
Cyclone IV GX Power



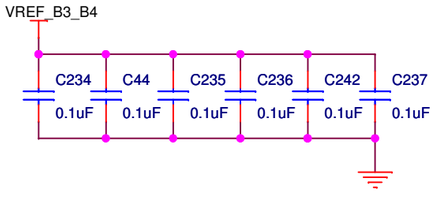


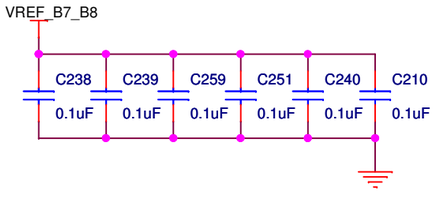


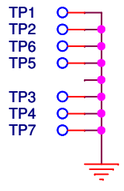




PLACE NEAR FPGA







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Power 1, (2.5V, 1.2V and 12V)

14V-20V DC INPUT

J5
RAPC712X
D23
FM540
DC_INPUT
Q1
FDS8880
12V
U48
LTC4357xDCB
A
SW3
EG2201A
R34
0
R20
68.1K
R16
11.5K
RUN_SW
12V_PCIE
Q3
FDS8880
U52
LTC4357xDCB
B

POWER LED
3.3V
R12
100, 1%
D11
Blue_Led

22,23 RUN_SW
19 VCCA_SNS
19 VCCA_VCCH_SNS
19 VCCL_SNS
19 VCCD_PLL_SNS

U43
LTC3853xUJ
TK/SS1
TK/SS2
TK/SS3
RUN1
RUN2
RUN3
ITH1
VFB1
ITH2
VFB2
ITH3
VFB3
MODE/PLLIN
ILIM
PGOOD3
PGOOD12
FREQ/PLLFLTR
SGND
EPAD_GND
EXTVCC
DRVCC12
INTVCC
VIN
BOOST1
TG1
SW1
BG1
BOOST2
TG2
SW2
BG2
BOOST3
TG3
SW3
BG3
SNSP1
SNSN1
SNSP2
SNSN2
SNSP3
SNSN3

R184 2.20
C43 10uF
C54 150uF
C203 2.2uF
C202 4.7uF
C205 0.1uF
INTVCC
12V

C172 0.1uF
C162 0.1uF
C161 0.1uF
330pF C144
R141 5.49K
C142 1500pF
2.5V
10pF C143
43.2K R129
20.0K R126
220pF C171
R161 10.0K
C188 680pF
1.2V
10pF C157
10.0K R153
20.0K R150
330pF C155
R152 43.2K
C156 470pF
12V_HSMC
10pF C189
140.0K R172
10.0K R173
0 R163
Forced Continuous
INTVCC
10.0K R154
DNI R162
100K R160
100K R159
R164 11.5K
Switching Freq = 450kHz
R155 3.24K
C190 0.01uF

D33 CMDSH2_3
D34 CMDSH2_3
D32 CMDSH2_3
Q6 SI4816BDY-T1
Q5 SI4816BDY-T1
Q4 SI4816BDY-T1
CH1
CH2
C194 0.1uF
C193 0.1uF
C192 0.1uF
C160 0.1uF
C159 0.1uF
C158 0.1uF
5.36K R144
1.62K R143
1.00M R142
2.61K R39
1.37K R49
4.32K R46
5.6uH L4
1.2uH L5
L6 8.2uH
C225 4.7uF
C224 0.1uF
C223 4.7uF
C222 0.1uF
C221 4.7uF
C220 0.1uF
SW1
SW2
SW3

2.5V
C39 10uF
C36 22uF
0.003 R33 VCCA_SNS
L3 BLM15AG221SN1
VCCA
2.5V_VCCA_VCCH_GXB
L2
VCCA_VCCH_SNS 0.003 R28
BLM15AG221SN1

1.2V
C37 10uF
C29 22uF
C187 330uF 4V Tantalum
0.003 R239 VCCL_SNS
L11 BLM15AG221SN1
1.2V_VCCL_GXB
L12
VCCD_PLL_SNS 0.003 R240
BLM15AG221SN1
VCCD_PLL
0.003 R238
VCC

12V_HSMC
C30 10uF
C24 220uF

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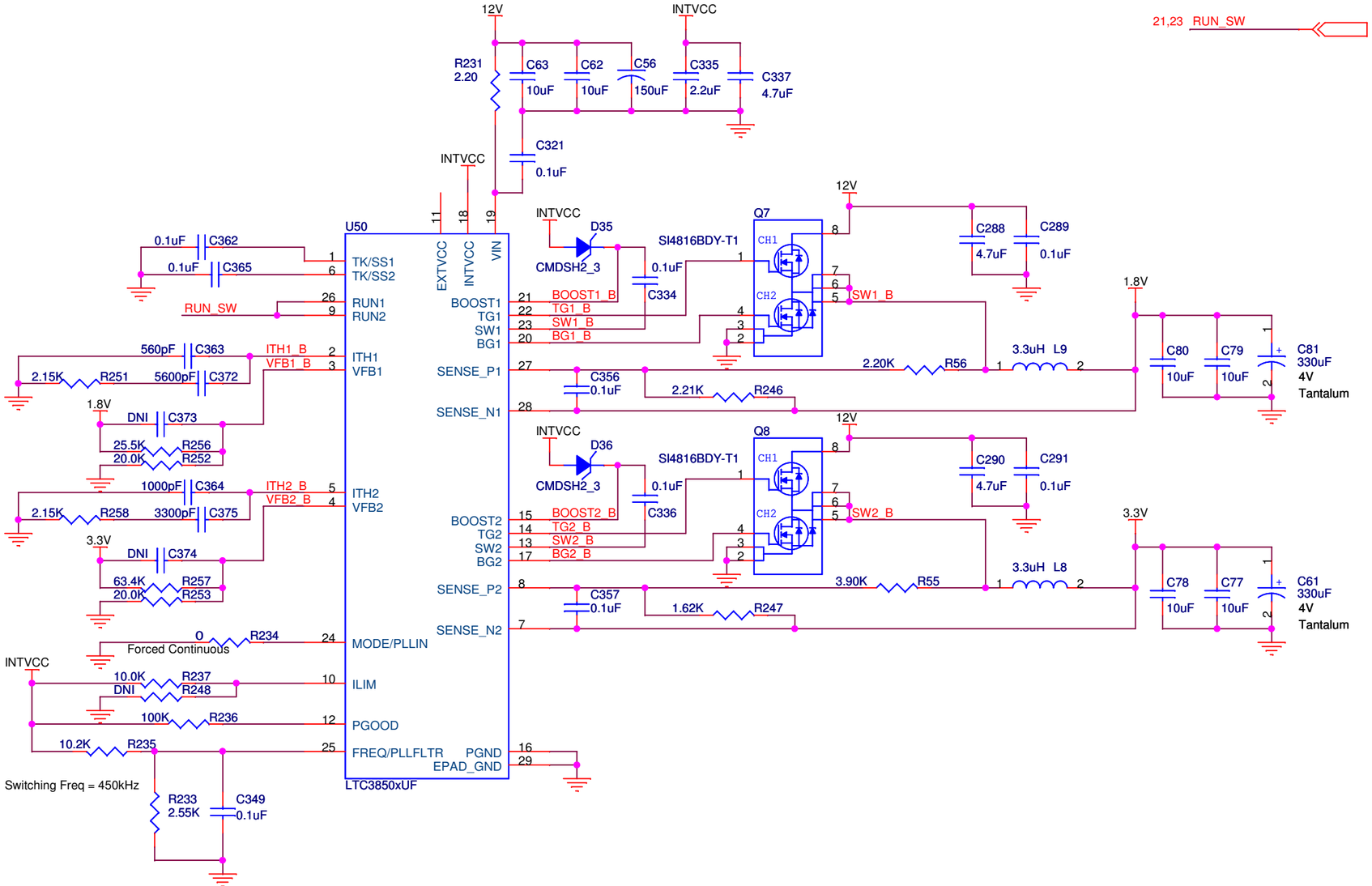
Power 2, (3.3V and 1.8V)



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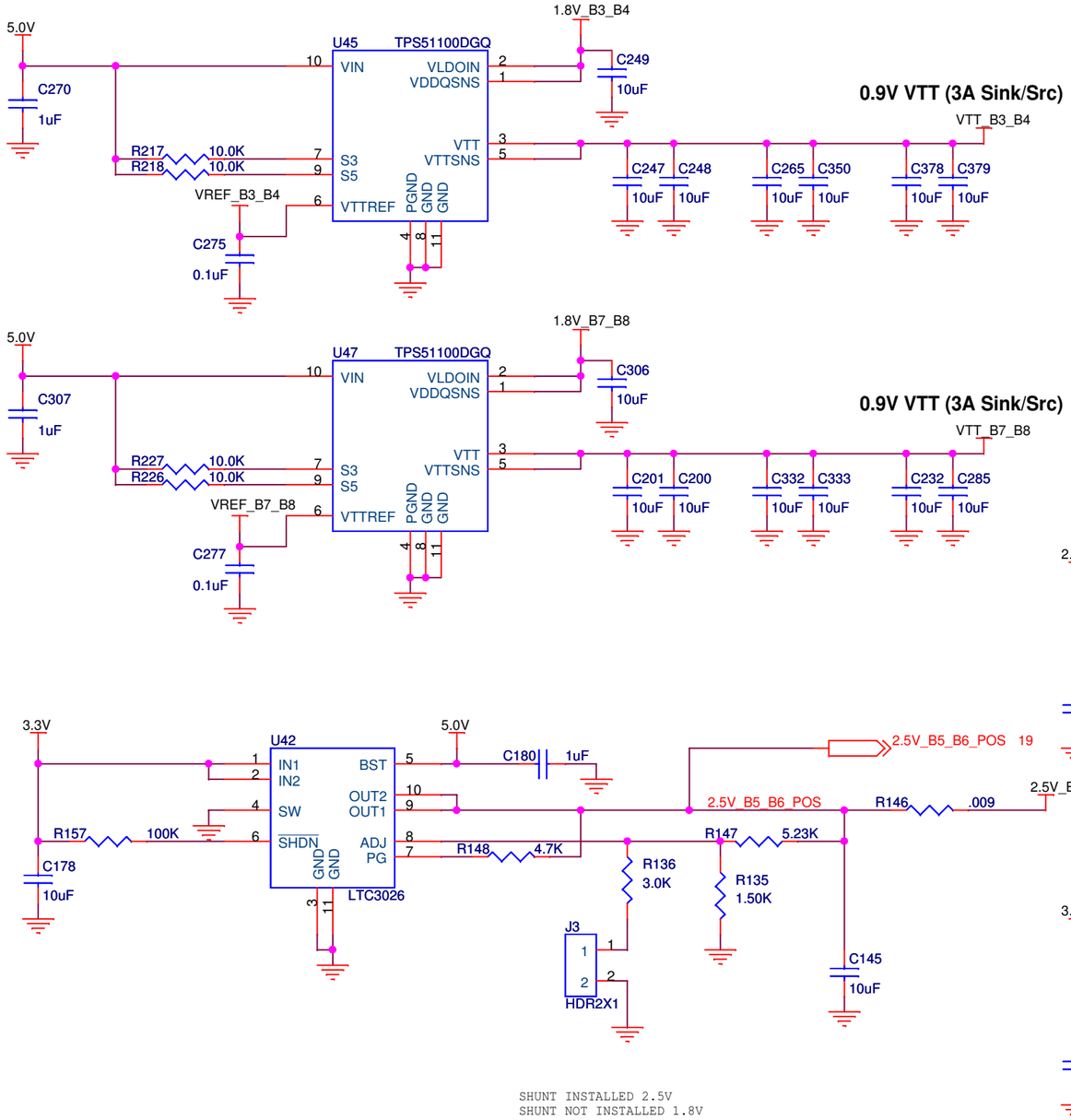
Power 3, (DDR2 (VREF/VTT), 5.0V, 1.8V FPGA VCCIO,1.1V Ethernet)



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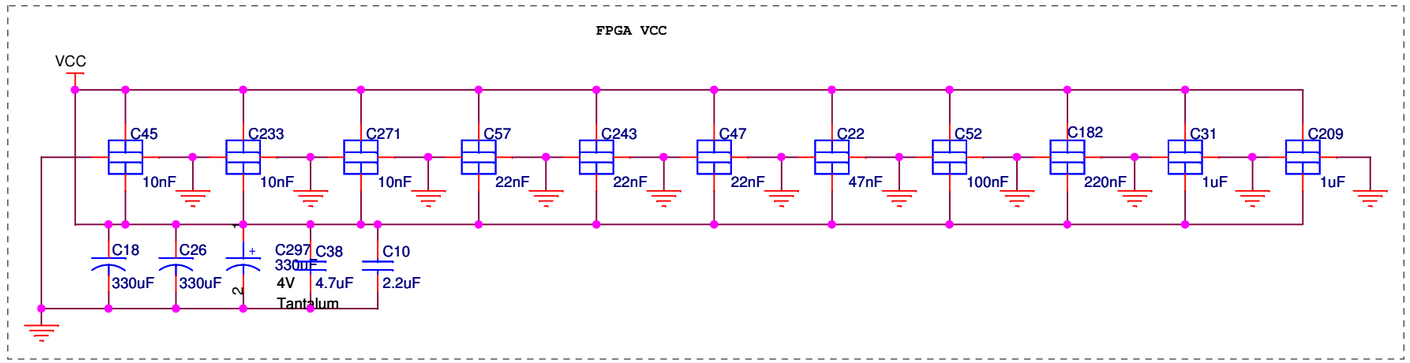
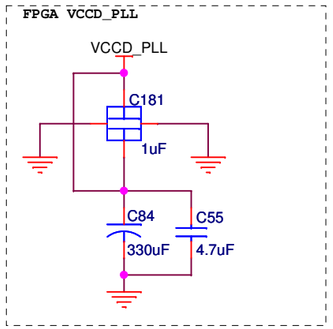
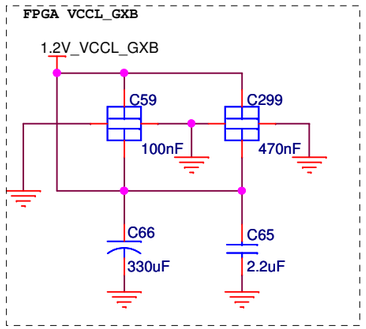
Place 6 vias minimum on each X2Y cap.

FPGA Decoupling

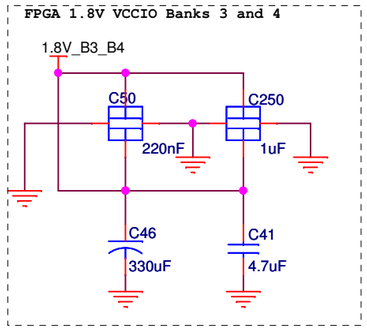


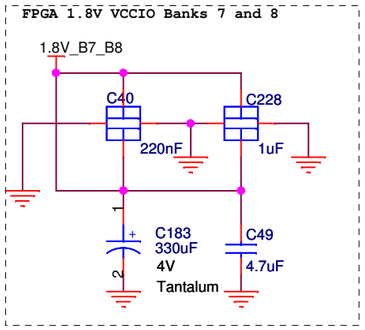


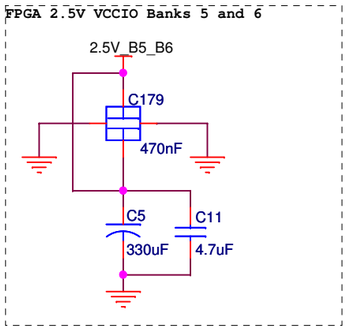


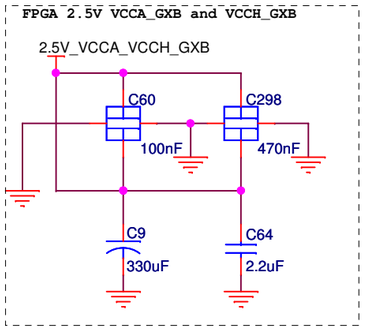
STANDOFF1
STANDOFF2
STANDOFF3
STANDOFF4
STANDOFF5

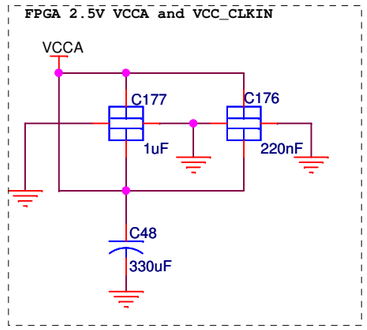
SCREW1
SCREW2
SCREW3
SCREW4
SCREW5











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