PEX 8619
Silicon Revisions and Errata List

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NDA REQUIRED

Version 1.10

May 2012

Website: www.plxtech.com
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A. Affected Silicon Revision

This document details Errata for the following silicon:

Product	Revision	Description	Status
PEX 8619	BA	16-Lane, 16-Port PCI Express Gen 2 Switch with DMA	Production

B. Device Documentation Version

The following documentation is the baseline functional description of the silicon:

Document	Version	Description	Publication Date
PEX 8619-BA Data Book	1.0	Data Book	July 2009

C. Errata Documentation Revision History

Revision	Publication Date	Description
0.1	March 2009	• Initial publication of the Errata list
0.2	April 2009	• Added Errata 5, 6, and 7
0.3	April 2009	• Added Errata 8 and 9
0.4	July 2009	• Added Errata 10, 11 and 12
1.0	August 2009	• Production Release • Updated Silicon status and Data book revision • Updated Errata 5
1.1	August 2009	• Added Caution i
1.2	November 2009	• Added Note to Errata 2 • Added Errata 13 and 14 • Added Caution ii
1.3	January 2010	• Corrected the affected silicon revision for Errata 14 and Caution i and ii
1.4	February 2010	• Added Caution iii
1.5	March 2010	• Added Errata 15
1.6	July 2010	• Added Errata 16
1.7	May 2011	• Added Errata 17 and 18 • Added Caution iv and v
1.8	July 2011	• Added Errata 19 • Added Caution vi, vii, and viii
1.9	March 2012	• Added Errata 20, and 21
1.10	May 2012	• Added Errata 22

D. Errata Summary

#	Description	Risk Category	Silicon Rev Affected
1	Correctable Error Status Bit Set When ASPM (L0s) is Enabled	Low	BA
2	Incorrect TCB Capture of Training Sets	Low	BA
3	Inverse Polarity on the THERMAL_DIODEn/p signals	Low	BA
4	Transaction Pending Bit on DMA Device is Not Reliable	Low	BA
5	The PHY Polling State Machine Can Get Stuck Under Noisy Links	Low	BA
6	Legacy Interrupts Cannot Be Generated in NT Mode if Hot Reset Propagation is Disabled	Low	BA
7	DMA Descriptor Invalidate Write-Back Does Not Update Associated Status Fields	Low	BA
8	Relaxed Ordering Bit and No Snoop Enable Bit are Read Only on the DMA Function PCIe Configuration Space	Low	BA
9	Inconsistent Default Value of Power Controller Control Register if MRL is Not Locked	Low	BA
10	AC JTAG Functionality in the PEX 8619 Does Not Work	Low	BA
11	NT Virtual Address Range Registers are Not Loaded Correctly in NT P2P Mode	Low	BA
12	I2C accesses to certain registers can receive incorrect responses when interleaved with DMA register accesses	Low	BA
13	PEX8619 DMA-initiated 64-bit Memory Writes traversing the NT-Virtual to NT-Link boundary have incorrect Requester-ID	Low	BA
14	Analog Loopback is Not Supported in Asynchronous Systems	Low	BA
15	Unreliable Port Disable/Re-enable when using 0x230[7:0] and 0x234[7:0]	Low	BA
16	A Gen2 port with x8 link-width may cause correctable errors on the link - under a heavy traffic scenario characterized by short TLPs	Low	BA
17	Both TX and RX in AC JTAG Functionality Does not Work	Low	BA
18	The upstream port LTSSM does not exit hot-reset until it receives TS1 with hot-reset TCB cleared	Low	BA
19	Link gets dropped when JTAG BYPASS is enabled	Low	BA

#	Description	Risk Category	Silicon Rev Affected
20	Interrupt Fencing Mode	Low	BA
21	Extended Tag Enable bit in DMA register	Low	BA
22	ECRC on DMA transfers needs to be consistently enabled or disabled between the PCIe devices involved in the DMA transfer	Low	BA

E. Caution Summary

#	Description	Risk Category	Silicon Rev Affected
i	The Surprise-Down Flag is Set When the Switch Transitions from L2/L3 READY to L0 Power Management States Without a Fundamental Reset	Low	BA
ii	A link will not come up if receivers are detected on a few lanes that do not exit Electrical Idle in polling	Low	BA
iii	Switch Initiated DMA Transfers Might Not Complete Over Noisy Links	Low	BA
iv	DMA transfers should not straddle the 4G boundary	Low	BA
v	Additional information for DMA MSI interrupt	Low	BA
vi	Data Book Erratum about I2C_ADDR[2:0] pins Description	Low	BA
vii	Serial Hot Plug Virtual Port Number Assignment	Low	BA
viii	Pin STRAP_NT_EN# has internal pull-up	Low	BA

1. Correctable Error Status Bit Set When ASPM (L0s) is Enabled

Risk Category: Low
Silicon Revisions Affected: BA

Description

When L0s ASPM is enabled, spurious receiver errors and/or bad TLP/DLLP counts could get logged which could result in ERR_CORR messages being received by the host.

Solution/Workaround

When L0s ASPM is enabled, set the Correctable Error Mast bit 0xFC8h[0,6,7]=1 to prevent the ERR_CORR message from being sent out due to receiver errors, bad TLPs and/or bad DLLPs respectively.

Impact

Spurious ERR_CORR messages could be received and the switch might set the Correctable Error Detected Bit (0x72[0]) when L0s ASPM is enabled.

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2. Incorrect TCB Capture of Training Sets

Risk Category: Low
Silicon Revisions Affected: BA

Description

In the case where excess noise exists on a link, the combination of a “COM” symbol followed by noise can result in the incorrect misinterpretation of Ordered Sets. The misinterpretation of said sequence might cause the LTSSM to remain in Loopback State until an assertion of hot reset or a fundamental Reset is detected.

Note: Due to what is required to create this condition, this problem has only manifested itself in asynchronous clocked systems where the reference clocks initially and abruptly deviate from the allowable tolerance for the reference clock (100 MHz ±300ppm) as defined in the PCI Express Base Specification.

Solution/Workaround

1. Assert hot reset or fundamental reset to the device
2. Set Register 0x23C[20] = 1 in order to mask Training Control Bits (TCB) in the training sets. *Note that setting this bit affects all ports in the switch and can cause the upstream port to ignore the hot reset TCB preventing the switch to be reset from such training set.*

3. Disable and then enable the failing port using corresponding register in 0x23Ch (even port) or 0x234h (odd port) to clear the LTSSM

Impact

The link might fail to achieve link-up status due to the noise on the link.

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3. Inverse Polarity on the THERMAL_DIODEn/p signals

Risk Category: Low
Silicon Revisions Affected: BA

Description

The polarity of the THERMAL_DIODEn/p is reversed on BA silicon with date codes of 905, 907, and 908.

Solution/Workaround

If using BA silicon with date codes of 905, 907 and 908, make sure to connect the THERMAL_DIODEn to the positive terminal and the THERMAL_DIONEp to the negative terminal of the measuring device. BA silicon with different date codes are not affected and should be connected normally.

Impact

Using the THERMAL_DIODEn/p as is can result in the incorrect temperature read of the device when using BA silicon with date codes of 905, 907 and 908. BA devices with different date codes are not affected.

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4. Transaction Pending Bit on DMA Device is Not Reliable

Risk Category: Low
Silicon Revisions Affected: BA

Description

The transaction pending bit (0x72[5]) on the DMA device (Function 1) of the switch is not reliable. A read to this register bit may not reflect the actual status of pending transactions for the DMA function.

Solution/Workaround

Use the per channel “DMA in progress” bit for the corresponding DMA channel (0x238[30], 0x338[30], 0x438[30] and 0x538[30] for DMA CH0, CH1, CH2 and CH3 respectively).

Impact

A configuration access to the transaction pending bit (0x72[5]) for the DMA function could return incorrect status. For accurate status update, use the “DMA in progress” bits instead.

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5. The PHY Polling State Machine Can Get Stuck Under Noisy Links

Risk Category: Low
Silicon Revisions Affected: BA

Description

The PHY state machine could get stuck in the Polling state when all the following conditions are met by the PEX 8619 PHY:

1. It times-out in the Polling.Active state (24ms) *AND*
2. Does not detect eight good training-sets on any lane during Polling.Active *AND*
3. all lanes of receiver are in electrical-idle at the Polling.Active timeout *AND*
4. detected an exit from electrical-idle on any lane at some point during Polling.Active *AND*
5. Target Link Speed is 5.0 GT/s

Solution/Workaround

Any one of the following two options can be a workaround to the above condition:

a. *setting* the electrical-idle mask bit on ANY lane of the port/link at PLX specific register offsets 200h/204h bits [15:8] using EEPROM, and optionally *clearing* once link is up.
b. Since the Target Link Speed has to be 5.0 GT/s for this problem to occur, *setting* the target-link speed bits in PCIe Link Control-2 register (offset 98h[3:0]) to train link in 2.5GT/s mode will prevent this issue for occurring. Once the link is up (i.e. L0 at 2.5 GT/s), change the target-link speed to 5.0 GT/s.

Impact

A **noisy** PCIe link that triggers Polling.Active state 24ms timeout could potentially get stuck.

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6. Legacy Interrupts Cannot Be Generated in NT Mode if Hot Reset Propagation is Disabled

Risk Category: Low
Silicon Revisions Affected: BA

Description

When Non-Transparent (NT) mode is enabled and the Upstream Port Reset Propagation bit is disabled (0x1DC[20]=1) allowing the upstream port to ignore a hot reset training sequence and preventing the device from resetting itself due to a DL_DOWN event, subsequent Doorbell Interrupts across the NT port to the Root Complex cannot be generated using the doorbell registers after a hot reset occurs on the upstream port. Furthermore, interrupts generated from the downstream ports will not be forwarded upstream.

Solution/Workaround

Implement one of the following:

- Do not set 0x1DC[20] but instead allow the device to be reset with a Hot Reset
- Use MSI in place of legacy interrupts when 0x1DC[20]=1
- Use the Training Control Bit (TCB) capture disable bit (0x228[5]) to disable the hot reset rather than the 0x1DC[20] bit.

Impact

There is no impact when the device is used in systems that do not use Hot Reset.
In systems where Hot Reset and legacy interrupts are used, the Upstream Port Reset Propagation bit (0x1DC[20]) cannot be disabled. A Hot Reset is required to reset the device or disabled using TCB bit 0x228[5].

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7. DMA Descriptor Invalidate Write-Back Does Not Update Associated Status Fields

Risk Category: Low
Silicon Revisions Affected: BA

Description

The DMA descriptor invalidate write-back mechanism does not update associated status fields in bits [30:28] and the transfer-count field in bits [26:0] of the descriptor write-back.

Solution/Workaround

If the bytes-transferred count is needed, software can do a memory-mapped read to the appropriate DMA channel current descriptor transfer-size field (device-offsets 228h/338h/438h/538h for channels 0/1/2/3 respectively) instead. For cases where the

descriptors are located in 64-bit address space, the write-back status fields [30:28] get updated correctly.

Impact

Descriptor write-back usage under 32-bit address space location of DMA descriptors cannot use the descriptor write-back feature. Instead, the user has to enable and rely on DMA interrupts to detect exceptions covered by the status fields.

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8. Relaxed Ordering Bit and No Snoop Enable Bit are Read Only on the DMA Function PCIe Configuration Space

Risk Category: Low
Silicon Revisions Affected: BA

Description

The Relaxed Ordering bit 0x70[4] and NoSnoop Enable bit 0x70[11] of the DMA function Device Control Register are read-only. These two bits should be read-writeable (R/W) instead.

Solution/Workaround

None. The DMA controller relies on the per-channel bits in the DMA control register to support Relaxed Ordering and No Snoop attributes for DMA TLPs. Applications that need these attributes should program the corresponding DMA channel offsets (0x238h, 0x248h, 0x258h, and 0x268h for channels 0, 1, 2, and 3 respectively).

Impact

For applications that use relaxed ordering or no snoop enable, programming of the per-channel DMA control register is required for this purpose. The value on bits 0x70[4] and 0x70[11] on the DMA device control register will not reflect this capability.

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9. Inconsistent Default Value of Power Controller Control Register if MRL is Not Locked

Risk Category: Low
Silicon Revisions Affected: BA

Description

For serial hot plug capable ports, if the MRL is not locked, the value (0 – Power ON) shown in the power controller control bit [10] of the Slot Control register (offset 80h) is incorrect. The port(s) is/are actually not powered on (HP_PWREN is low) which is the correct behavior despite the incorrect default register value. The port(s) can power ON and OFF normally.

Solution/Workaround

For serial hot plug capable ports, if the MRL is not locked, have the software ignore the value of the power controller control bit.

Impact

If the MRL is not locked, slight modifications to the software may be needed to ignore the value of the power controller control bit. The functionality associated with these registers is not affected. Power to the hot plug capable downstream ports can still be turned on and off normally.

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10. AC JTAG Functionality in the PEX 8619 Does Not Work

Risk Category: Low
Silicon Revisions Affected: BA

Description

The level output on the PEX 8619 RX pins used by the AC JTAG instructions is not stable and consequently it is not latched in the PEX 8619 by the boundary scan chain.

Solution/Workaround

There is no workaround for the RX pins.

Impact

The RX pins of the PEX 8619 cannot be used with AC JTAG instructions. The TX pins of the PEX 8619 are not affected and can be used with AC JTAG instructions.

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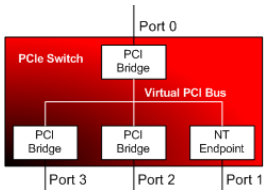
11. NT Virtual Address Range Registers are Not Loaded Correctly in NT P2P Mode

Risk Category: Low
Silicon Revisions Affected: BA

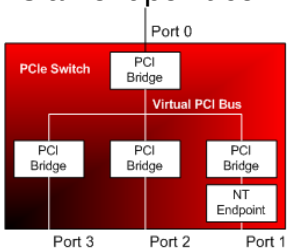
Description

The Non-Transparent (NT) feature in the Switch enables the NT device in one of two ways:

1. As an endpoint connected to the Virtual PCI Bus



2. As an endpoint connected to the secondary bus of a virtual PCI-to-PCI bridge



When asserted, the STRAP_NT_P2P_ENABLE# signal enables the second mode as described above, also referred to as the NT P2P mode.

In the NT P2P mode, configuring the NT Virtual address range registers with a serial EEPROM or through the I^2C interface result in the configuration data being loaded to non-existent register offsets instead.

Solution/Workaround

Follow the steps as listed in the order below for successfully programming the NT Virtual address range registers through a serial EEPROM or I^2C interface.

1. Disable the PCI Bridge between the NT endpoint and the Virtual PCI Bus by programming a “0” to register 0x1DC[6] of port 0.
2. Load the contents for the NT Virtual address range registers via the serial EEPROM or I^2C interface as required
3. Enable the virtual PCI Bridge between the NT endpoint and the Virtual PCI Bus by programming a "1" to register 0x1DC[6] of port

Impact

When using the NT P2P mode, EEPROM or I^2C based programming of NT virtual address range setup registers does not take effect. Memory Mapped programming accesses to the aforementioned registers are not impacted.

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12. I^2C accesses to certain registers can receive incorrect responses when interleaved with DMA register accesses

Risk Category: Low
Silicon Revisions Affected: BA

Description

When a register access to a shadow register is performed using the I^2C interface at the same time a software access to the DMA control registers (2C8h-324h, 348h-444h, 680h-7BCh, 980h-9FCh, E00h-E3Ch, F00h-F0Ch and F40h-F8Ch) occurs, the I^2C requests receive incorrect responses.

Solution/Workaround

4. Perform the I^2C access prior to the start of the DMA
5. If an I^2C access needs to occur after a DMA starts, ensure that a software register access to a non-DMA port precedes the I^2C access.

Impact

For a system using the internal DMA engine, register accesses using the I^2C interface are restricted in order to avoid incorrect responses

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13. PEX8619 DMA-initiated 64-bit Memory Writes traversing the NT-Virtual to NT-Link boundary have incorrect Requester-ID

Risk Category: Low
Silicon Revisions Affected: BA

Description

If a PEX8619 NT-Virtual port 64-bit BAR is enabled, PEX8619 DMA-initiated 64-bit Memory Write TLPs directed across the NT Port (from NT-Virtual to NT-Link domain) incorrectly contain (within the packet header) the Requester-ID of the initiating DMA endpoint (within the switch), instead of the translated Requester-ID (the Bus/Device Number of NT-Link port, captured from the last Config Write to the NT-Link port).

Solution/Workaround

. For Case 1 above using back-to-back NT-Link ports, program the second switch's NT-Link Requester-ID Lookup Table (offsets DB4h-DF0h), to include the Bus Number of the first PEX8619's DMA function.

2. For Case 2 above, ACS Source Validation should be disabled in the Port/Device that is connected to the PEX8619 NT-Link port.

3. For Case 3 above, software implementation should include handling of the incorrect Requester-ID value (of the PEX8619 DMA function) logged in the Header Log registers:

Impact

The MemWr TLP header Requester-ID field is not used for TLP routing. The following cases are the exceptions, with impact:

1. DMA through Back-to-Back (or cascaded) NT ports:
If a PEX8619 NT-Link port is connected to a second PEX8619 NT Port, and the second PEX8619 requires Requestor-ID translation, then the Requester-ID field within incoming PEX8619 DMA-initiated 64-bit MemWr TLPs will be incorrect and will not match the expected Requestor ID value in the second switch's NT port Requester-ID Lookup Table (LUT) register(s).

2. ACS Source Validation:
If a PEX8619 NT-Link port is connected to a PCIe device that implements ACS Source Validation, then PEX8619 DMA-initiated 64-bit MemWr TLPs directed across the NT Port (from NT-Virtual to NT-Link domain) could fail that device's ACS Source Validation check (unless the Bus Number value within the PEX8619 DMA MemWr Requester-ID field coincidentally happens to be within the range of other device's Secondary Bus Number and Subordinate Bus Number register values).

3. Error Logging:
If a PEX8619 DMA-initiated 64-bit MemWr TLP directed across the NT port (from NT-Virtual to NT-Link domain) encounters an Error, and the recipient Port/Device implements the optional PCIe Advanced Error Reporting Extended Capability, then the recipient Port/Device will log an incorrect Requestor-ID value within its Header Log registers.

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14. Analog Loopback is Not Supported in Asynchronous Systems

Risk Category: Low
Silicon Revisions Affected: BA

Description

Analog Loop Back Slave Mode does not work when enabled in systems with asynchronous clocks.

Solution/Workaround

For Asynchronous Systems use Line Side Loopback as follows, once switch device is placed in slave loopback ready condition using chosen method:

Use I^2C to program the following register bits: (all lanes in the group will be brought into a special “Line Side” loopback mode in parallel):
Note: The example below is for lanes 0-3 inclusive. Use 0xC04h for lanes 4-7, 0xC08h for lanes 8-11, and 0xC0Ch for lanes 12-15.

Bit	Description	Setting
0xC00[5]	Line Side Loopback Enable	1
0xC00[10]	AC Couple Mode Enable	1
0xC00[31]	Lane 0-3 Serdes Manual Control Override	1

All other bits can be left = 0
Enable the Master device's test pattern generator and receive pattern checker.

Impact

Systems using asynchronous clocks need to enable Line Analog Loopback Slave mode.

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15. Unreliable Port Disable/Re-enable when using 0x230[7:0] and 0x234[7:0]

Risk Category: Low
Silicon Revisions Affected: BA

Description

When the following bits *0x230[7:0]* and *0x234h[7:0]* are used to disable a particular port when the link is at Gen 2 speed, the link may not come up when the port is re-enabled by clearing these bits back to the default value.

Solution/Workaround

Note: Steps 1 and 2 below for disabling a port apply to transparent downstream ports only. Re-enabling of the ports for both transparent and non-transparent ports is described in step 3.

1. To bring a link down, set the link disable *bit 0x78[4]* and set the link retrain bit 0x78[5]
2. To disable a port, set detect.quiet wait selection at offset *0x228[11]* and/or *0x22Ch[11] = 1* then bring the target link speed to Gen1 by writing to *0x98[3:0]*. Follow with a write to 0x78[5]=1 to retrain the link. Finally, wait for 10 microseconds or more and then use port disable (*0x230[7:0]* and/or *0x234[7:0]*) to disable the port.
3. To enable the port, set detect.quiet wait selection at offset *0x228[11]* and/or *0x22C[11]=1*. Enable the port by clearing register 0x230[7:0] and/or *0x234[7:0]*. If the link does not come up, disable the port one more time and re-enable again.

Impact

At Gen 2 speed, customer cannot reliably use the port disable/re-enable functionality of registers *0x230[7:0]* and *0x234[7:0].*

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16. A Gen2 port with x8 link-width may cause correctable errors on the link - under a heavy traffic scenario characterized by short TLPs

Risk Category: Low
Silicon Revisions Affected: BA

Description

A port whose link-width is Gen2 x8 may experience a case, under a sequence of back-to-back 32-bit address MemRd TLPs followed by a MemWr TLP, where-in a correctable error can get injected into the transmitted data. The error manifests as an STP symbol in the middle of the transmitted MemWr TLP that would be NAK-ed by the connected device resulting in a re-send by the switch.

Solution/Workaround

Any of the following workarounds can be used to avoid the above behavior.

1. Enable ECRC in the system. This increases the 32-bit addressing MemRd TLP length from 3 DW to 4 DW and prevents this corner case issue.
2. Use 64-bit address space for Memory read TLP's, it also increases the MemRd TLP length from 3 DW to 4 DW.
3. Use credit throttling to prevent back to back reads going out of the switch by restricting the outstanding credits on the device connected to the switch.
4. Use read-pacing feature in the switch to prevent 3 back to back reads to go out of the Gen2 x8 port.

Impact

The connected device may experience correctable errors, setting associated bits in the PCIe error status registers.

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17. Both TX and RX in AC JTAG Functionality Does not Work

Risk Category: Low
Silicon Revisions Affected: BA

Description

The level output on the RX pins used by the AC JTAG instructions is not stable and consequently it is not latched by the boundary scan chain. The TX pins does not toggle

at the right cycle in AC JTAG mode. The statement about TX in erratum number 10 is incorrect.

Solution/Workaround

1. Bring up the links and check the widths using the PEX_LANE_GOOD# pins. The link width and speed can also be checked using I2C.
2. The external device can put the switch into loopback mode and then check the integrity of the link. The external device connected to the switch can also be put in loopback mode using the switch and the link integrity can be checked using PRBS or other user-programmable test patterns.

Impact

The RX/TX pins of the switch cannot be used with AC JTAG instructions.

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18. The upstream port LTSSM does not exit hot-reset until it receives TS1 with hot-reset TCB cleared

Risk Category: Low
Silicon Revisions Affected: BA

Description

The upstream device initiates the hot-reset sequence. The upstream port LTSSM transmits hot-reset TCB set. When the upstream device stops sending the TS with hot-reset set, the upstream port LTSSM should stay in hot-reset state for 2ms and transition to Detect state after 2ms timeout. But it is falsely looking for TS1 with hot-reset TCB clear from the upstream device to enable the 2ms timer

Solution/Workaround

There is no workaround

Impact

The LTSSM stays in hot-reset state until the upstream device go to Polling.Active state.

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19. Link gets dropped when JTAG BYPASS is enabled

Risk Category: Low
Silicon Revisions Affected: BA

Description

After functional bring up of PEX switch, if the BYPASS instruction is loaded into JTAG TAP the SerDes enters JTAG mode, the link drops

Solution/Workaround

There is no workaround

Impact

PEX switch does not maintain the link when BYPASS instruction is loaded into Test Access Port (TAP)

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20. Interrupt Fencing Mode

Risk Category: Low
Silicon Revisions Affected: BA

Description

The device only supports the basic mode-1 of interrupt fencing. Mode-2 (internal reset), Mode-3 (block packet transmission) and Mode-4 (block packet transmission and create surprise dl-down) are not supported.

Solution/Workaround

There is no workaround

Impact

The interrupt fencing is limited to the basic mode-1 consistent with behavior outlined in PCIe Base 2.0 specification.

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21. Extended Tag Enable bit in DMA register

Risk Category: Low
Silicon Revisions Affected: BA

Description

The description for the DMA function Type-0 space device control and status register 70h[8] “Extended Tag field enable” should state that “extended tags are supported and enabled when this bit is set”. The register’s attribute and default values specified in the data-book themselves are accurate. This is also consistent with the DMA function’s device capability offset 6Ch[5] that advertises extended-tag capability.

Solution/Workaround

There is no workaround

Impact

The description in datasheet is incorrect.

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22. ECRC on DMA transfers needs to be consistently enabled or disabled between the PCIe devices involved in the DMA transfer

Risk Category: Low
Silicon Revisions Affected: BA

Description

When ECRC is enabled on a PCIe device returning Completions in response to 8619 DMA reads but ECRC generation is not enabled on 8619 DMA function (function-1), there can be packet data corruption. Conversely, when ECRC is enabled on 8619 DMA function (function-1) but not enabled on the device returning Completions in response to

the DMA reads, there are cases where the packet data could get corrupted. The usage and programming of ECRC needs to be kept consistent between the 8619 DMA function-1 and its companion device sourcing/sinking PCIe requests or completions that serve the DMA transfer.

Solution/Workaround

1. ECRC generation, when used, needs to be enabled on both the source/destination of the DMA transfer as well as the 8619 DMA function, by setting offset 0xFCC[6] in function1.
2. ECRC when not used, needs to be kept disabled on both the source/destination and the 8619 DMA function (function-1).

Impact

If DMA is used in a system that has ECRC generation partially enabled, software needs to change to set ECRC generation enable bit for the DMA function 0xFCC[6] to be consistent with the companion PCIe devices involved in the transfer.

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i. The Surprise-Down Flag is Set When the Switch Transitions from L2/L3 READY to L0 Power Management States Without a Fundamental Reset

Risk Category: Low
Silicon Revisions Affected: BA

Description

In systems where the Switch is placed in L2/L3 READY power management state and then an attempt is made to exit that state without a fundamental reset (PERST#), the *PCIe Surprise Down Error Status bit* 0xFB8h[5] could get set on the downstream ports.

Solution/Workaround

Typical usage entails the use of a power cycle and/or fundamental reset after entry to L2/L3 READY state. However, any of the following workarounds can be used when that is not the case:

1. Prior to placing the switch in L2/L3 READY state, do a read-modify-write to the *HPC I/O Reload bit* 0x1E0[23] and *HPC Output Reload Value bit* 0x1E0[20]. This will prevent the surprise-down flag from getting set up on L2/L3 READY exit. Bits 0x1E0[23, 20] must be cleared upon return to L0 state.
2. Prior to placing the Switch in L2/L3 READY state, mask the surprise down status from generating a FATAL_ERR message by setting the *Surprise Down Error Mask bit* 0xFBC[5] = 1. Clear the *Surprise Down Error Status bit* 0xFB8[5] and *Surprise Down Error Mask bit* 0xFBC[5] bits in that order upon return to L0 state.

Impact

Applications that place the Switch in L2/L3 READY state could see a FATAL_ERR message upon exit to L0 state when a power cycle and/or fundamental reset is not used.

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ii. A link will not come up if receivers are detected on a few lanes that do not exit Electrical Idle in polling

Risk Category: Low
Silicon Revisions Affected: BA

Description

If unused lanes of a multilane link are terminated, the link will not come up. If a PEX8619 detects a receiver on some lanes but these lanes do not detect an exit from electrical idle in the Polling State, the link is supposed to negotiate out these non functioning lanes and still link up to a reduced link width. In case of PEX8619, the link will not come up. The inability of the PEX8619 to negotiate out these terminated but unused lanes is limited to LTSSM Polling State only. If lanes are found be terminated in Configuration or Recovery State, PEX8619 will negotiate out these lanes and will link up successfully to a reduced link width.

Solution/Workaround

1. Do not terminate unused lanes.
2. Use the “Never Detect Electrical Idle” bit if unused lanes are terminated.

Impact

Failure to link up in case of terminated unused lanes.

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iii. Switch Initiated DMA Transfers Might Not Complete Over Noisy Links

Risk Category: Low
Silicon Revisions Affected: BA

Description

The following scenario has been observed in the case where the link error rate is higher than that defined in the PCI Express Base Specification (BER higher than 10^{-12}). The high error rate on the link (noisy link) results in a high number of Bad TLP/DLLPs detected by the Switch. Consider the sequence of events below:

1. The integrated DMA controller in the Switch transmits TLP-A at time T1 at the same time, the replay timer for TLP-A starts. The link partner successfully receives TLP-A, and in return, it issues ACK-A1. However, due to the high error rate on that link, ACK-A1 gets dropped.
2. The integrated DMA controller in the Switch continues on to transmit TLP-B and TLP-C. The link partner successfully receives TLP-B and issues ACK-B1 to the Switch. The switch successfully receives ACK-B1 and at that exact time the replay timer for TLP-A expires.
3. The link partner sends ACK-C1 (in response to TLP-C), which is also dropped due to the noisy link. In this case, the replay timer, which should have started for TLP-C, does not start due to the condition resulting from Step 2.

In the above sequence, TLP-C will not get replayed on the link. Consequently, the DMA engine in the Switch will continue to wait for ACK-C1 from the link partner before it continues to the next DMA transfer preventing the DMA engine from reaching the done state (including interrupt done generation). If a non DMA TLP arrives and is transmitted out the noisy link after the replay timer for TLP-A expires, the DMA TLP and replay timer is restored allowing the DMA transfer to complete and generate the DMA Done interrupt to the host.

Solution/Workaround

If a DMA done interrupt is not seen within a pre-determined system time-frame, software should create a write or read transfer targeting the noisy link. The write or read will flush the egress port and allow the DMA transfer to complete and process the pending DMA done interrupt.

Impact

A switch initiated DMA transfer may not complete and fail to generate the DMA done interrupt when the target is on the other side of a link with a higher than BER 10^{-12} error rate.

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iv. DMA transfers should not straddle the 4G boundary

Risk Category: Low
Silicon Revisions Affected: BA

Description

DMA off-chip and on-chip descriptor modes should ensure source and destination transfer ranges do not straddle the 4G address boundary. The on-chip controller does not support such transfers. A given transfer can still target the >4G address region using the normal descriptor or extended-descriptor modes, as long as source and destination spaces of the transfer each reside on either side of the 4G boundary.

Solution/Workaround

There is no workaround.

Impact

DMA transfer should not straddle the 4G boundary.

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v. Additional information for DMA MSI interrupt

Risk Category: Low
Silicon Revisions Affected: BA

Description

In the section 8.1 DMA Features of datasheet, the “16 MSIs needed (four per channel)” should be removed. The “8 DMA interrupt vectors (two per channel)” is correct.

In the section 9.3.1 MSI Operation of datasheet, add additional information below to clarify the MSI in DMA Function.

If one MSI vector is enabled (default), all the DMA interrupt events are combined into a single vector.
If two MSI vectors are enabled,
Vector[0] – DMA normal interrupt events from all 4 channels
Vector[1] – DMA error interrupt events from all 4 channels
If four MSI vectors are enabled,
Vector[0] – DMA normal interrupt events from channel 0 and 1
Vector[1] – DMA normal interrupt events from channel 2 and 3
Vector[2] – DMA error interrupt events from channel 0 and 1
Vector[3] – DMA error interrupt events from channel 2 and 3
If eight MSI vectors are enabled,
Vector[0] – DMA normal interrupt events from channel 0
Vector[1] – DMA normal interrupt events from channel 1
Vector[2] – DMA normal interrupt events from channel 2
Vector[3] – DMA normal interrupt events from channel 3
Vector[4] – DMA error interrupt events from channel 0
Vector[5] – DMA error interrupt events from channel 1
Vector[6] – DMA error interrupt events from channel 2
Vector[7] – DMA error interrupt events from channel 3

The description of DMA MSI Capability Register (offset 48h)
Bit[19:17] Multiple Message Capable
000b = PEX 86xx DMA Function can request only one Message vector
001b = PEX 86xx DMA Function can request two Message vectors
010b = PEX 86xx DMA Function can request four Message vectors
011b through 111b = PEX 86xx DMA Function can request eight Message vectors
Bit[22:20] should make similar changes as bit[19:17]

DMA error interrupt is triggered when the bit [16] of DMA Interrupt Control/Status Register (csr_23C for ch_0) is set and the enable bit ([0]) is also set.

DMA normal interrupt is triggered when any of bit [21:17] of DMA Interrupt Control/Status Register (csr_23C for ch_0) is set and its corresponding enable bit ([5:1]) is also set.

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vi. Data Book Erratum about I2C_ADDR[2:0] pins Description

Risk Category: Low
Silicon Revisions Affected: BA

Description

In data book, the pins I2C_ADDR[2:0] description in Table 3-8 as

1. The internal pull-up resistors cause the I2C_ADDR[2:0] inputs to default to HHH(000b)
2. I2C_ADDR[2:0] require external pull-up or pull-down termination resistors. If I2C is not used, external termination is strongly recommended, to prevent possible input buffer oscillation

Also section 7.2.2 states “The default state for I2C_ADDR[2:0] inputs that are not externally connected High or Low is 111b, due to the internal pull-down resistors

The above description is incorrect, the correct description is

1. The internal pull-up resistors cause the I2C_ADDR[2:0] inputs to default to HHH(111b)
2. The “Type” column should be “PU” to indicate the internal pull-ups are present on the I2C_ADDR[2:0] pins.
3. No external termination is required if I2C is not used

Also section 7.2.2 should be corrected to state “The default state for I2C_ADDR[2:0] inputs that are not externally connected High or Low is 111b, due to the internal pull-up resistors

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vii. Serial Hot Plug Virtual Port Number Assignment

Risk Category: Low
Silicon Revisions Affected: BA

Description

The I/O Expander having the lowest I2C address is assigned to the lowest number clock-enabled downstream transparent port, and so on, even the Slot Implement bit in

the downstream port is cleared. Clock-enabled ports correspond to bits that are set in the Clock Enable register in port 0, offset 1D8h.

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viii. Pin STRAP_NT_EN# has internal pull-up

Risk Category: Low
Silicon Revisions Affected: BA

Description

The pin STRAP_NT_EN# has internal pull-up. The column type in data book for this pin should be PU.

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