TXB0304 4-Bit Bidirectional Level-Shifter/Voltage Translator with Automatic Direction Sensing

1 Features

- Fully Symmetric Supply Voltages, 0.9 V to 3.6 V on A Port and 0.9 V to 3.6 V
- V_{CC} Isolation Feature – If Either V_{CC} Input is at GND, all Outputs are in High-Impedance State
- OE Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 5 µA Max (I_{CCA} or I_{CCB})
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 8000-V Human-Body Model (A114-B)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecom

3 Description

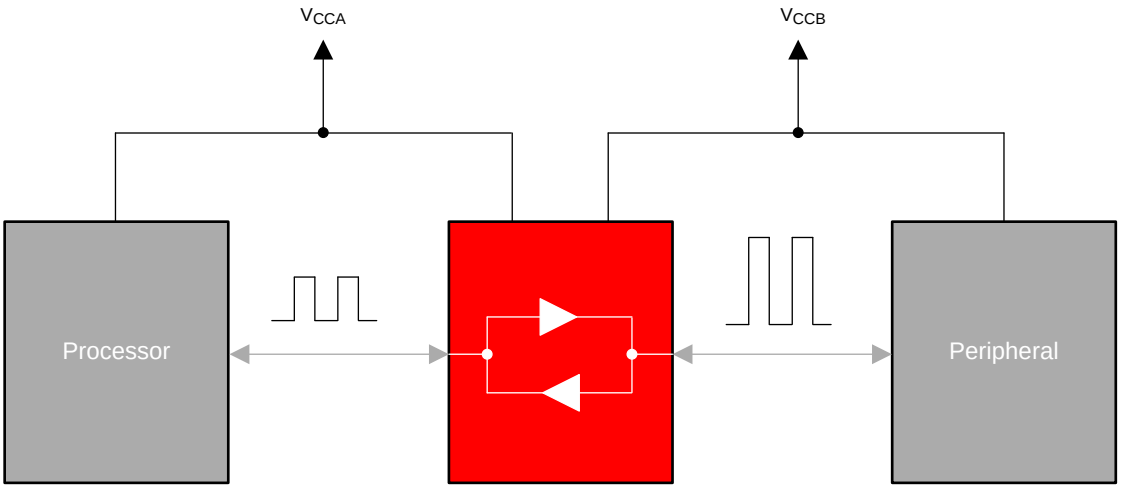
This 4-bit non-inverting translator uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 0.9 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 0.9 V to 3.6 V. This allows for low Voltage bidirectional translation between 1 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V voltage nodes. For the TXB0304, when the output-enable (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver. The OE device control pin input circuit is supplied by V_{CCA}. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The only difference between TXB0304 and TXBN0304 is the OE signal being active high and active low respectively.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXB0304	RUT UQFN (12)	2.00 mm × 1.70 mm
	RSV UQFN (16)	2.60 mm × 1.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Block Diagram for TXB0304



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2014) to Revision F — **Page**

- Made changes to *Description* section ... 1
- Made changes to *Absolute Maximum Ratings*, *Recommended Operating Conditions*[(1)(2)], *Switching Characteristics* and *Electrical Characteristics* tables ... 1

Changes from Revision D (October 2012) to Revision E — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Changed VCCA and VCCB in the ABS MAX table to V_{CCA} and V_{CCB} in 3 places ... 4
- Changed in ELEC CHARAC table the 0.9 x V_{CCA} and 0.9 x V_{CCB} from MAX column into the MIN column ... 5
- Changed in ELEC CHARAC table 0.2 (2 places) in the MIN column to the MAX ... 5

Changes from Revision C (May 2012) to Revision D — **Page**

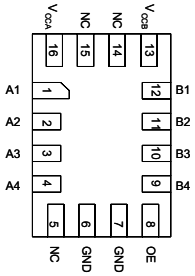
- Added *Application Information* section ... 12

Changes from Revision B (September 2011) to Revision C — **Page**

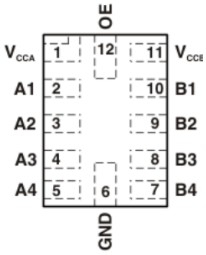
- Added package pin out diagram notes. ... 3

5 Pin Configuration and Functions

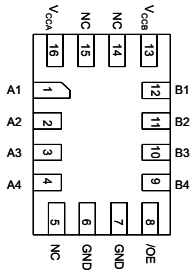
RSV Package
16-Pin UQFN
TXB0304 Top View



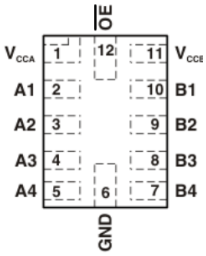
RUT Package
12-Pin UQFN
TXB0304 Top View



RSV Package
16-Pin UQFN
TXBN0304 Top View



RUT Package
12-Pin UQFN
TXBN0304 Top View



A. See *Layout Guidelines* for notes about package pin out diagrams.

Pin Functions

PIN					TYPE	DESCRIPTION	
NAME	TXB0304		TXBN0304				
	RSV	RUT	RSV	RUT			
A1	1	2	1	2	I/O	Input/output 1	Referenced to V_{CCA}
A2	2	3	2	3	I/O	Input/output 2	
A3	3	4	3	4	I/O	Input/output 3	
A4	4	5	4	5	I/O	Input/output 4	
B1	12	10	12	10	I/O	Input/output 4	Referenced to V_{CCB}
B2	11	9	11	9	I/O	Input/output 3	
B3	10	8	10	8	I/O	Input/output 2	
B4	9	7	9	7	I/O	Input/output 1	
GND	6, 7	6	6,7	6	GND	Ground	
NC	5, 14, 15	—	5, 14, 15	—	—	No connection; not internally connected	
OE	8	12	—	—	I	3-state output-mode enable. Pull OE (TXB0304) low to place all outputs in 3-state mode. Referenced to V_{CCA}.	
$\overline{OE}$	—	—	8	12	I	3-state output-mode enable. Pull $\overline{OE}$ (TXBN0304) high to place all outputs in 3-state mode. Referenced to V_{CCA}.	
V_{CCA}	16	1	16	1	—	A-port supply voltage 0.9 V ≤ V_{CCA} ≤ 3.6 V	
V_{CCB}	13	11	13	11	—	B-port supply voltage 0.9 V ≤ V_{CCB} ≤ 3.6 V	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage		–0.5	4.6	V
V_{CCB}			–0.5	4.6	
V_I	Input voltage	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state (2)	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C
T_J	Junction temperature		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions (1) (2)

			V_{CCA}	V_{CCB}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				0.9	3.6	V
V_{CCB}							
V_{IH}	High-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	V_{CCI} × 0.65	V_{CCI}	V
		OE/$\overline{OE}$	0.9 V to 3.6 V	0.9 V to 3.6 V	V_{CCA} × 0.65	3.6	
V_{IL}	Low-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	0	V_{CCI} × 0.35	V
		OE/$\overline{OE}$	0.9 V to 1.2 V	0.9 V to 3.6 V	0	V_{CCA} × 0.3	
			1.2 V to 3.6 V	0.9 V to 3.6 V	0	V_{CCA} × 0.35	
V_O	Voltage range applied to any output in the high-impedance or power-off state	A-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	V
		B-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	
Δt/Δv	Input transition rise or fall rate	A-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	ns/V
		B-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	
T_A	Operating free-air temperature				–40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, such as, both at V_{CCI} or both at GND.
(2) V_{CCI} is the supply voltage associated with the input port.

6.4 Thermal Information

THERMAL METRIC[1]		TXB0304		UNIT
		RUT (UQFN)	RSV (UQFN)	
		12 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	131.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.9	55.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.9	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
V_{OHA}	High-level output voltage	I_{OH} = –20 µA	T_A = 25°C	0.9 V to 3.6 V		0.9 x V_{CCA}			V
V_{OLA}	Low-level output voltage	I_{OL} = 20 µA	–40°C to 85°C	0.9 V to 3.6 V				0.2	V
V_{OHB}	High-level output voltage	I_{OH} = –20 µA	T_A = 25°C		0.9 V to 3.6 V	0.9 x V_{CCB}			V
V_{OLB}	Low-level output voltage	I_{OL} = 20 µA	–40°C to 85°C		0.9 V to 3.6 V			0.2	V
I_I	OE	V_I = V_{CCI} or GND	T_A = 25°C	0.9 V to 3.6 V	0.9 V to 3.6 V			±1	µA
			–40°C to 85°C					±2	
I_{off}	A port	V_I or V_O = 0 to 3.6 V	T_A = 25°C	0 V	0 V to 3.6 V			±1	µA
			–40°C to 85°C					±2	
	B port	V_I or V_O = 0 to 3.6 V	T_A = 25°C	0.9 V to 3.6 V	0 V			±1	
			–40°C to 85°C					±2	
I_{OZ}	A or B port	OE = GND	T_A = 25°C	0.9 V to 3.6 V	0.9 V to 3.6 V			±1	µA
			–40°C to 85°C					±2	
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			5	µA
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			5	µA
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			10	µA
I_{CCZA}	High-Z state supply current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			5	µA
I_{CCZB}	High-Z state supply current	V_I = V_{CCI} or GND, I_O = 0, OE = GND	–40°C to 85°C	0.9 V to 3.6 V	0.9 V to 3.6 V			5	µA
C_i	OE	T_A = 25°C		0.9 V to 3.6 V	0.9 V to 3.6 V		3		pF
C_{io}	A port	T_A = 25°C, OE = GND		0.9 V to 3.6 V	0.9 V to 3.6 V		6.7		pF
	B port						6.7		

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	LOAD	V_{CCA}	V_{CCB}	MIN	MAX	UNIT
Data rate	C_L = 15 pF	0.9 to 3.6 V	0.9 to 3.6 V		50	Mbps
	C_L = 15 pF	1.2 to 3.6 V	1.2 to 3.6 V		100	Mbps
	C_L = 15 pF	1.8 to 3.6 V	1.8 to 3.6 V		140	Mbps
	C_L = 30 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	C_L = 30 pF	1.2 to 3.6 V	1.2 to 3.6 V		90	Mbps
	C_L = 30 pF	1.8 to 3.6 V	1.8 to 3.6 V		130	Mbps
	C_L = 50 pF	1.2 to 3.6 V	1.2 to 3.6 V		80	Mbps
	C_L = 50 pF	1.8 to 3.6 V	1.8 to 3.6 V		120	Mbps
	C_L = 100 pF	1.2 to 3.6 V	1.2 to 3.6 V		70	Mbps
	C_L = 100 pF	1.8 to 3.6 V	1.8 to 3.6 V		100	Mbps

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted). (For parameter descriptions, see Figure 2 and Figure 3.)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V_{CCA}	V_{CCB}	MIN	TYP(1)	MAX	UNIT
t_{pd}	A	B	C_L = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	A	B	C_L = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	A	B	C_L = 15	1.8-3.6	1.8-3.6		3.7	4.8	
	A	B	C_L = 30	0.9-3.6	0.9-3.6		19.5	34	
	A	B	C_L = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	A	B	C_L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	A	B	C_L = 50	1.2-3.6	1.2-3.6		8	12.3	
	A	B	C_L = 50	1.8-3.6	1.8-3.6		4	5.4	
	A	B	C_L = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	A	B	C_L = 100	1.8-3.6	1.8-3.6		4.5	6	
	B	A	C_L = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	B	A	C_L = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	B	A	C_L = 15	1.8-3.6	1.8-3.6		3.7	5	
	B	A	C_L = 30	0.9-3.6	0.9-3.6		19.5	34	
	B	A	C_L = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	B	A	C_L = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	B	A	C_L = 50	1.2-3.6	1.2-3.6		8	12.3	
	B	A	C_L = 50	1.8-3.6	1.8-3.6		4	5.4	
	B	A	C_L = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	B	A	C_L = 100	1.8-3.6	1.8-3.6		4.5	6	
t_{en}	OE	A	C_L = 15	0.9-3.6	0.9-3.6			262	ns
				1.2-3.6	1.2-3.6			64	
				1.8-3.6	1.8-3.6			37	
		B	C_L = 15	0.9-3.6	0.9-3.6			332	
				1.2-3.6	1.2-3.6			76	
				1.8-3.6	1.8-3.6			41	
t_{dis}	OE	A	C_L = 15	0.9-3.6	0.9-3.6			172	ns
		B	C_L = 15	0.9-3.6	0.9-3.6			169	ns
t_{rB}, t_{fB}	B-port rise and fall times		C_L = 15	0.9-3.6	0.9-3.6		2.95		ns
t_{sA}, t_{sA}	A-port rise and fall times		C_L = 15	0.9-3.6	0.9-3.6		3.1		ns
$t_{SK(O)}$	Channel-to-channel skew		C_L = 15	0.9-3.6	0.9-3.6			0.15	ns

(1) T_A = 25°C

6.8 Operating Characteristics

C_{pd} - power dissipation capacitance measured at T_A = 25°C.

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = V_{CCA} (outputs enabled)	34	pF
	B-port input, A-port output		34	
C_{pdB}	A-port input, B-port output		34	pF
	B-port input, A-port output		34	
C_{pdA}	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns, OE = GND (outputs disabled)	0.01	pF
	B-port input, A-port output		0.01	
C_{pdB}	A-port input, B-port output		0.01	pF
	B-port input, A-port output		0.01	

(1) V_{CCA}, V_{CCB} 0.9 V to 3.6 V

6.9 Typical Characteristics

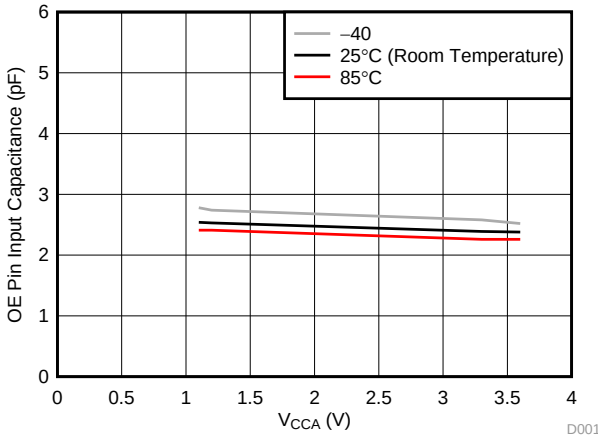
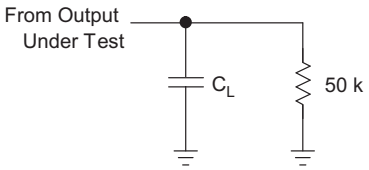
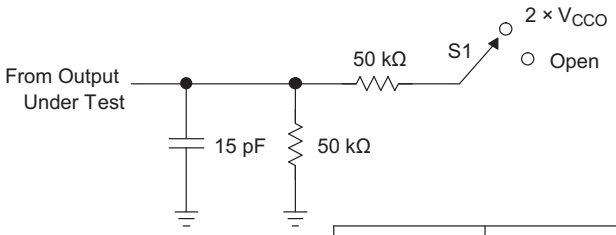


Figure 1. Input Capacitors for OE Pin (C_i) vs Power Supply (V_{CCA})

7 Parameter Measurement Information

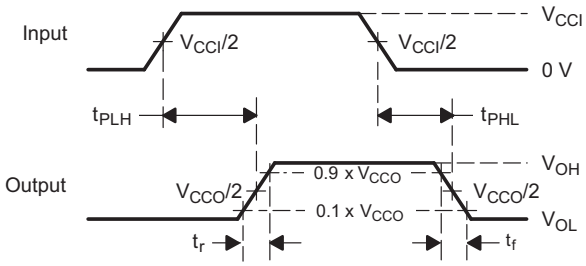


LOAD CIRCUIT FOR MAX DATA RATE, PULSE DURATION PROPAGATION DELAY OUTPUT RISE AND FALL TIME MEASUREMENT

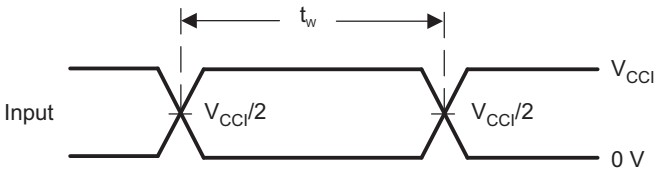


LOAD CIRCUIT FOR ENABLE/DISABLE TIME MEASUREMENT

TEST	S1
t_{PZL}/t_{PLZ} t_{PHZ}/t_{PZH}	2 × V_{CCO} Open



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION

A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. t_{PLH} and t_{PHL} are the same as t_{pd}.

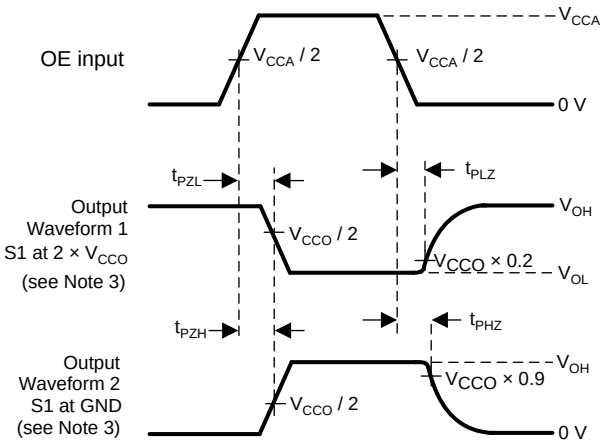
E. V_{CCI} is the V_{CC} associated with the input port.

F. V_{CCO} is the V_{CC} associated with output port.

G. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuits and Voltage Waveforms

Parameter Measurement Information (continued)



(1) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

(3) Waveform 1 is for an output with internal such that the output is high, except when OE is high. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

Figure 3. Enable and Disable Times

8 Detailed Description

8.1 Overview

The TXB0304 and TXBN0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

8.1.1 Architecture

The TXB0304 and TXBN0304 architecture (see Figure 4) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0304 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 30 Ω at V_{CCO} = 0.9 V to 1 V, 10 Ω at V_{CCO} = 1.1 V to 1.7 V, and 5 Ω at V_{CCO} = 1.8 V to 3.3 V.

8.2 Functional Block Diagram

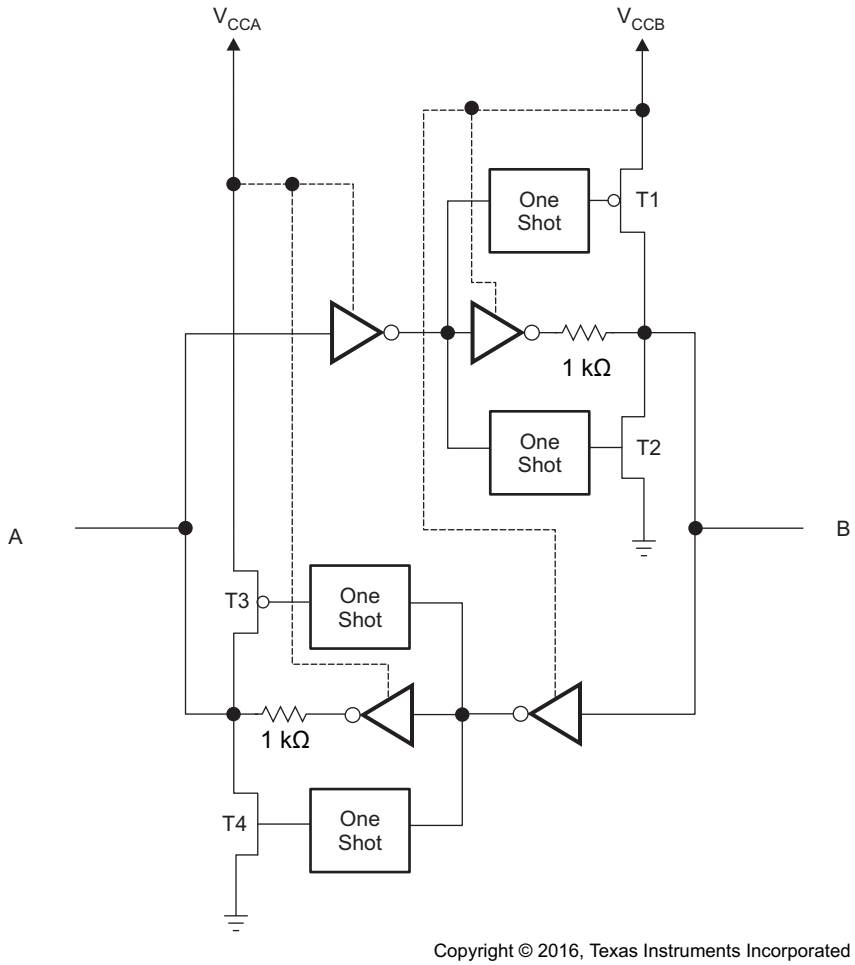
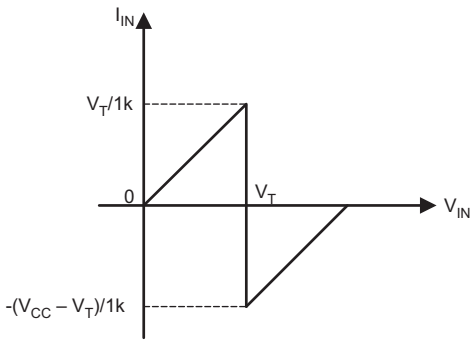


Figure 4. Architecture of TXB0304 I/O Cell

8.3 Feature Description

8.3.1 Input Driver Requirements

Typical I_{IN} vs V_{IN} characteristics of the TXB0304//TXBN0304 are shown in Figure 5. For proper operation, the device driving the data I/Os of the TXB0304 must have drive strength of at least ±3 mA.



(1) V_{CC} is power supply of TXB0304.

(2) V_T is the input threshold voltage of TXB0304 (typically it is $V_{CC}/2$).

Figure 5. Typical I_{IN} vs V_{IN} Curve

8.4 Device Functional Modes

8.4.1 Enable and Disable

The TXB0304 has an OE input that is used to disable the device by setting OE = low ($\overline{OE}$ = high for TXBN0304), which places all I/Os in the high-impedance (Hi-Z) state. The disable time (t_{dis}) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is high.

8.4.2 Pullup or Pulldown Resistor on I/O Lines

The TXB0304/TXBN0304 is designed to drive capacitive loads of up to 100 pF. The output drivers of the TXB0304 have low dc drive strength. If pull-up or pull-down resistors are connected externally to the data I/Os, their values must be kept higher than 20 kΩ to ensure that they do not contend with the output drivers of the TXB0304. but if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the V_{OH} and V_{OL} .

$$V_{ol} = V_{CCout} \times \frac{1.5k\Omega}{1.5k\Omega + R_{pu}} \quad (1)$$

$$V_{oh} = V_{CCout} \times \frac{R_{pd}}{1.5k\Omega + R_{pd}}$$

where

- V_{CCOUT} is the output port supply voltage on either V_{CCA} or V_{CCB}
- R_{PD} is the value of the external pull down resistor
- R_{PU} is the value of the external pull up resistor
- 1.5 kΩ is the counting the variation of the serial resistor 1kΩ in the I/O line. (2)

Because of this restriction on external resistors, the TXB0304 should not be used in applications such as I^2C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI TXS010X series of level translators.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TXB0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI TXS010X products. Any external pull-down or pull-up resistors are recommended larger than 20 kΩ.

9.2 Typical Application

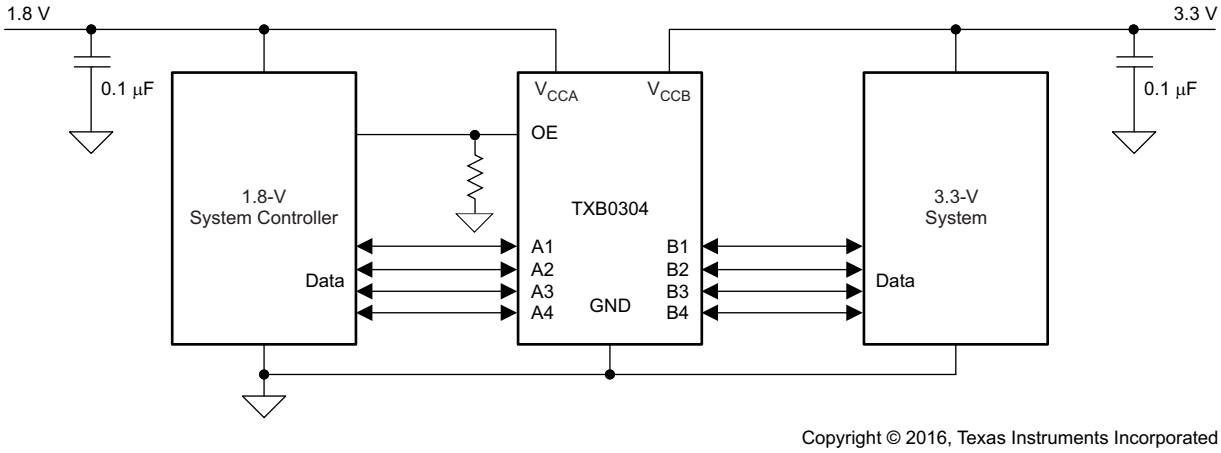


Figure 6. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.9 V to 3.6 V
Output voltage range	0.9 V to 3.6 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0304 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXB0304 device is driving to determine the output voltage range.
  - Don't recommend to have the external pull-up or pull-down resistors. If mandatory, it is recommended the value should be larger than 20 kΩ.

• An external pull-down or pull-up resistor decreases the output V_{OH} and V_{OL}. Use the below equations in section 8.5.2 to draft estimate the V_{OH} and V_{OL} as a result of an external pull-down and pull-up resistor.

9.2.3 Application Curve

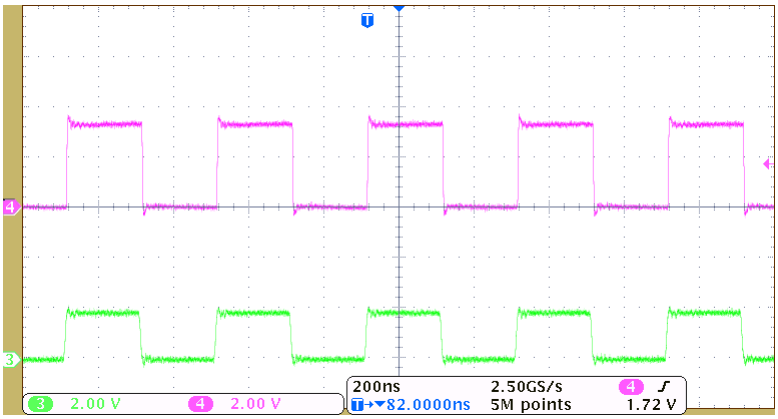


Figure 7. Level-Translation of a 2.5-MHz Signal

10 Power Supply Recommendations

There is no requirement for the power sequence. During operation, TXB0304 can work at both $V_{CCA} \leq V_{CCB}$ and $V_{CCA} \geq V_{CCB}$, During power-up sequencing, any power supply can be ramped up first. The TXB0304 has circuitry that disables all output ports when either V_{CC} is switched off ($V_{CCA/B}$ = 0 V).

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the V_{CCA}, V_{CCB} pin and GND pin
- Short trace-lengths should be used to avoid excessive loading.
- For long transmission lines, place a series resistor equivalent to the impedance of the transmission lines to avoid signal integrity issues
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.
- Pullup resistors are not required on both sides for Logic I/O.
- If pullup or pulldown resistors are needed, the resistor value must be over 20 kΩ.
- 20 kΩ is a safe recommended value, if the customer can accept higher Vol or lower Voh, smaller pull up or pull down resistor is allowed, the draft estimation is Vol = Vccout × 1.5k/(1.5k + Rpu) and Voh = Vccout × Rpd/(1.5k + Rpd).
- If pullup resistors are needed, please refer to the TXS0104 or contact TI.
- For detailed information, refer to application note SCEA043.

11.2 Layout Example

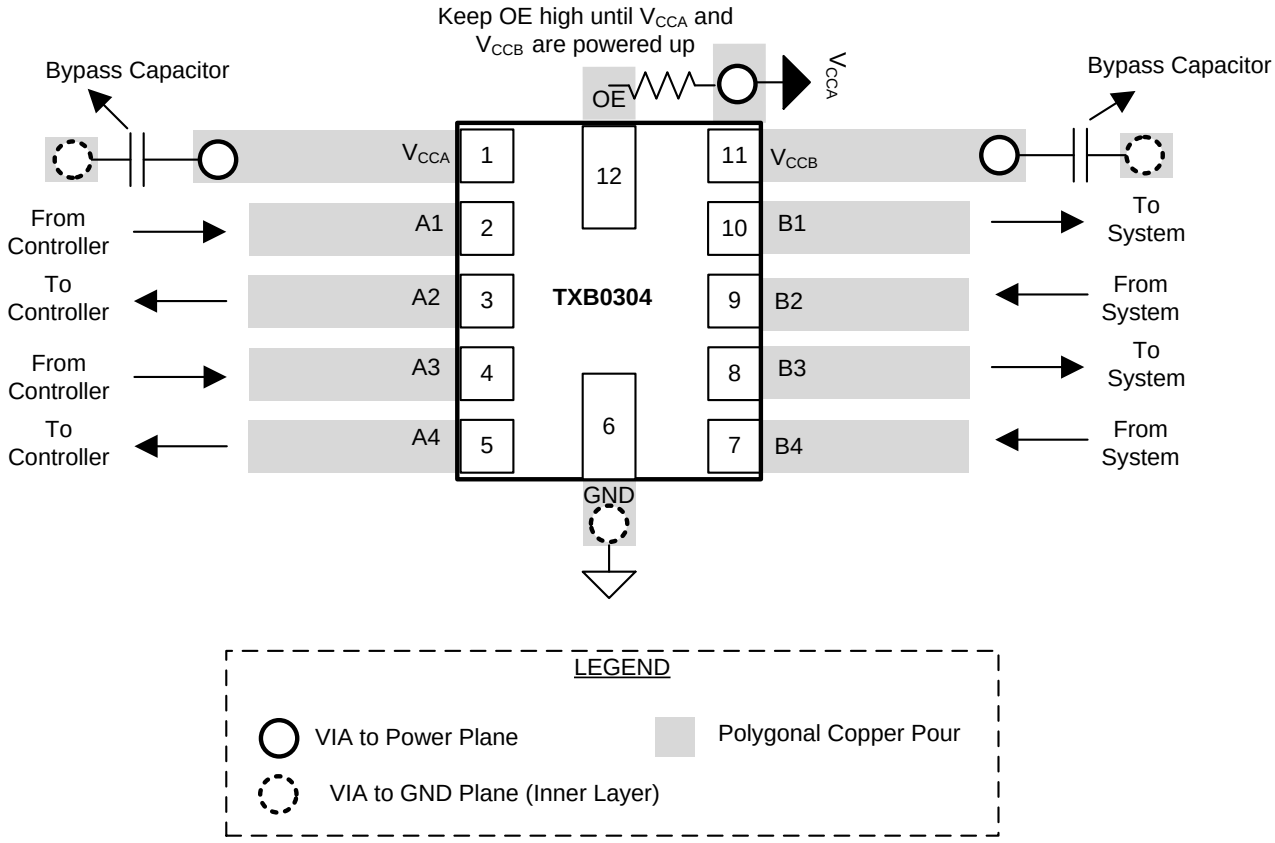


Figure 8. TXB0304 PCB Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

For TI TXS010X products, go to www.ti.com/product/txs0101.

For the TXB0304 IBIS Model, see SCEM544.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- Application Report, *A Guide to Voltage Translation With TXB-Type Translators,* SCEA043
- User's Guide, *TXB0304 Evaluation Module,* SCEU003

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0304RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTJ	Samples
TXB0304RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(737 ~ 73R ~ 73V)	Samples
TXBN0304RSVR	ACTIVE	UQFN	RSV	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTK	Samples
TXBN0304RUTR	ACTIVE	UQFN	RUT	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	74R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

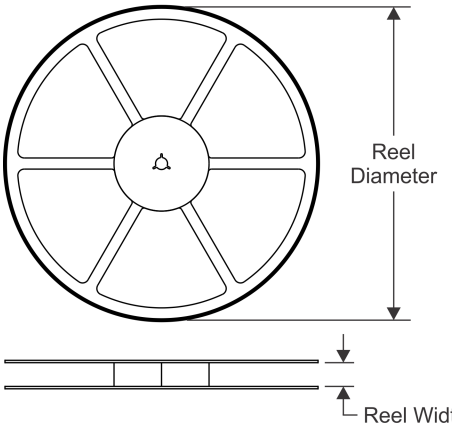
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

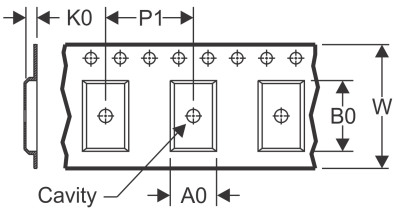
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

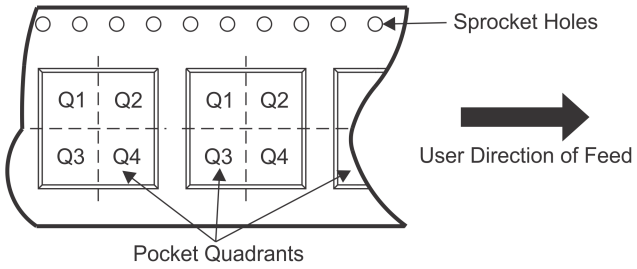


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

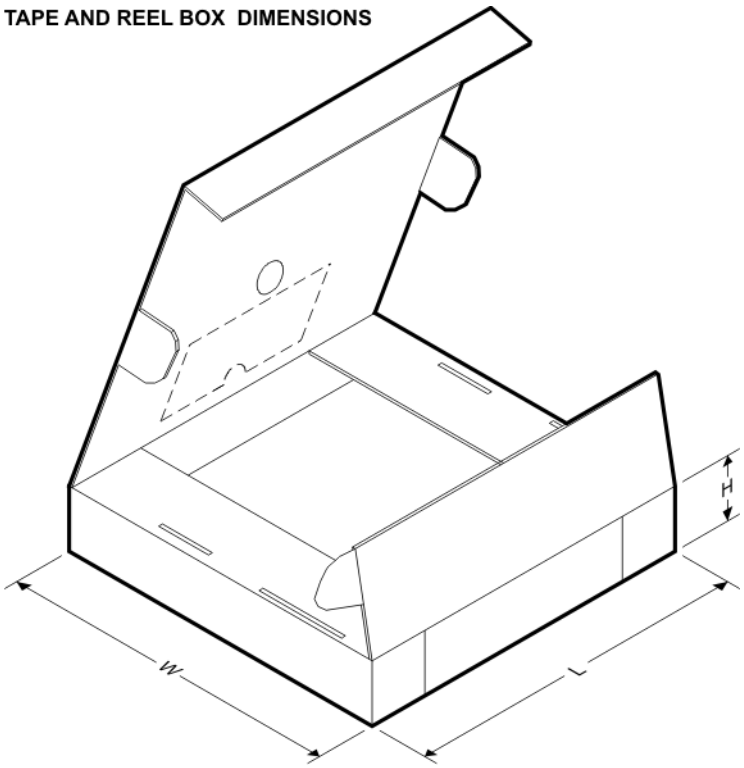
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXB0304RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	330.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1
TXBN0304RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

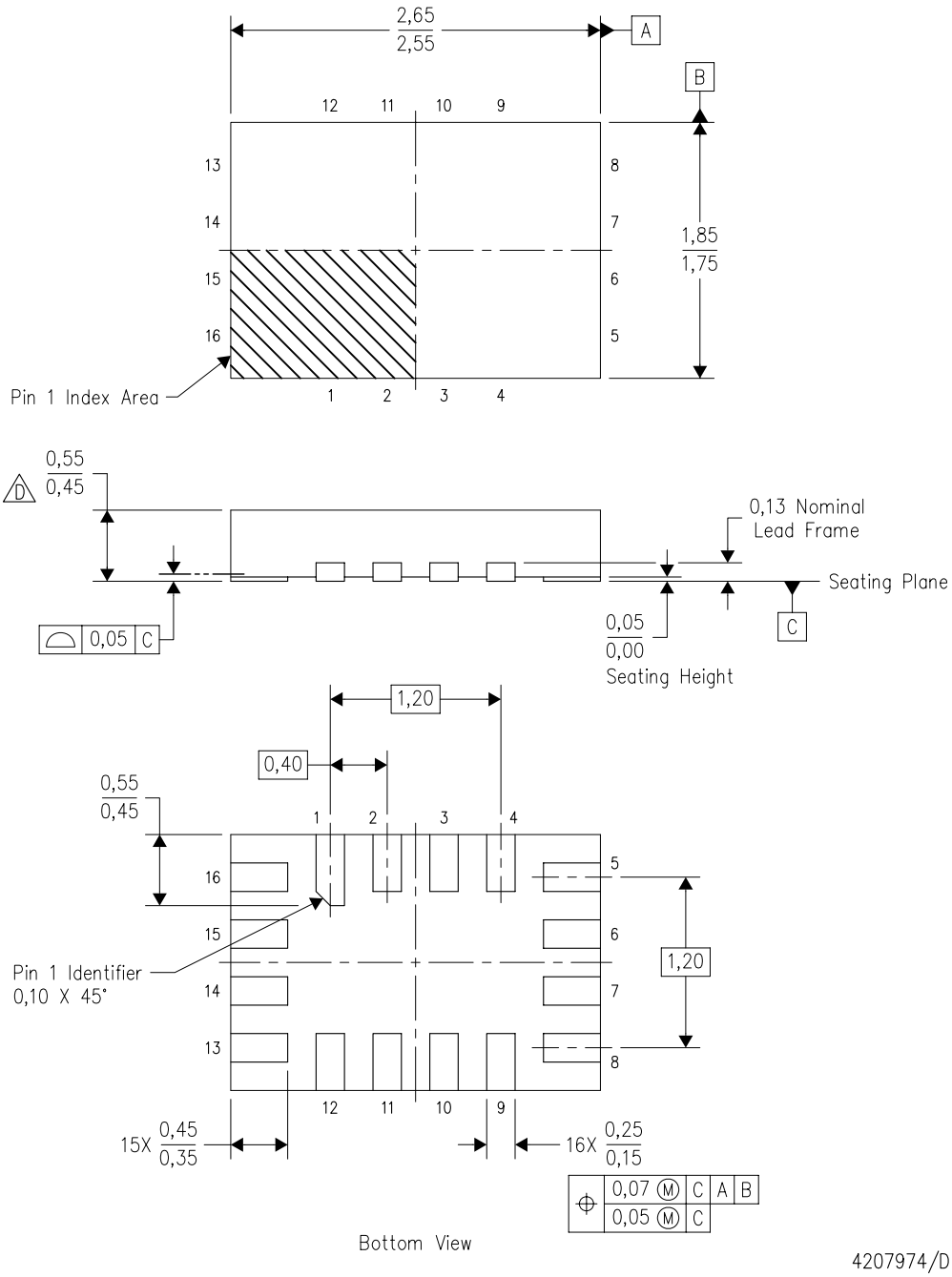
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

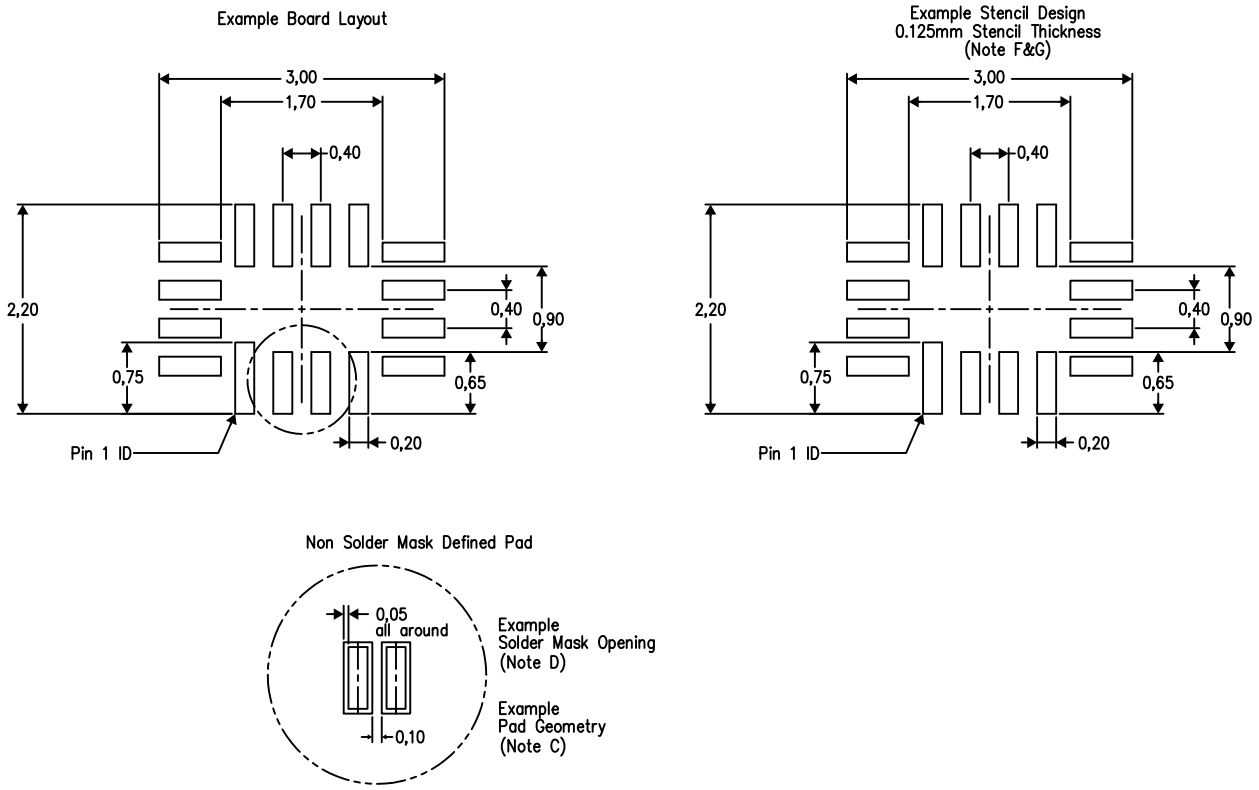
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXB0304RUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
TXBN0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXBN0304RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0
TXBN0304RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0

RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UFHE, except minimum package thickness.

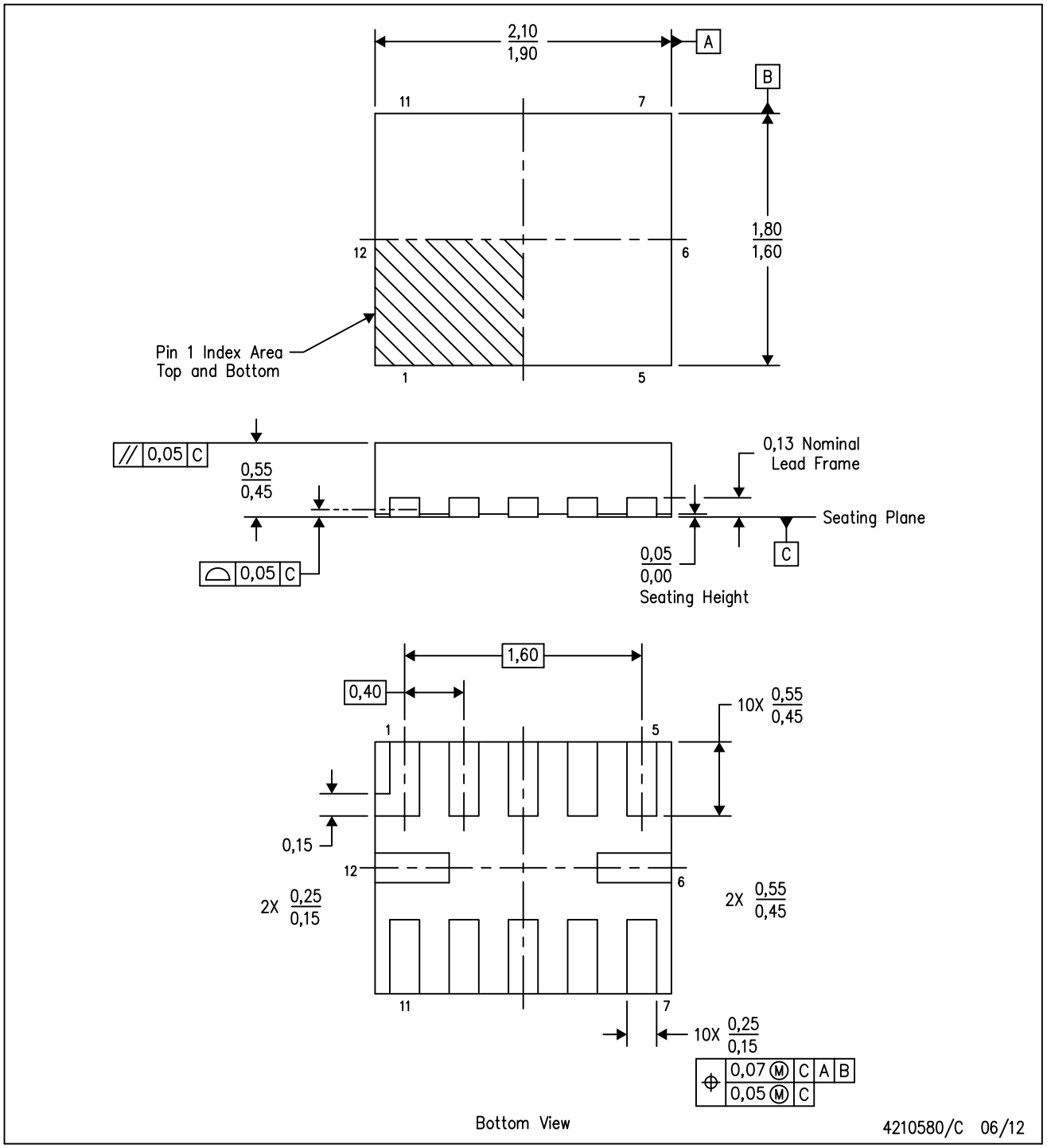
RSV (R–PUQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



4208244/C 02/13

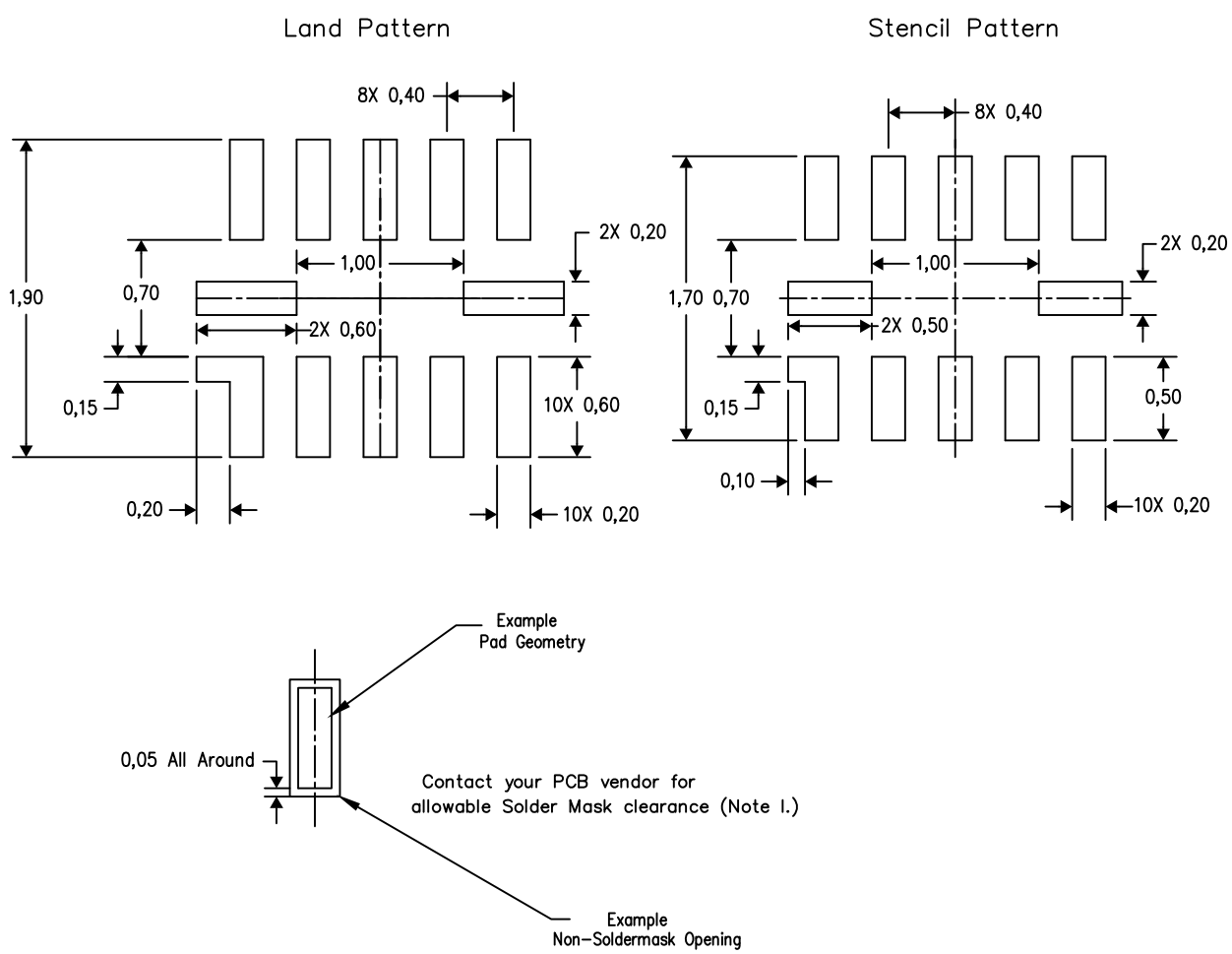
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.

RUT (R–PUQFN–N12) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,1016 mm (4 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Over–printing land for larger area ratio is not advised due to land width and bridging potential. Exersize extreme caution.
H. Suggest stencils cut with lasers such as Fiber Laser that produce the greatest positional accuracy.
I. Component placement force should be minimized to prevent excessive paste block deformation.

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RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

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