



Bank Number GXB_L1 GXB_L1 GXB_L1 GXB_L1		PinName/Function (2)	Optional Function(s)		Dedicated Tx/Rx	Emulated LVDS	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2
GXB_L1				Function	Channel	Output Channel					hard memory PHY (3)
GXB_L1		DNU					E33				FH1 (3)
GXB_L1		DNU					F33				
GXB_L1		RREF_TL					F34				
		REFCLK3Ln					R27				
GXB_L1		REFCLK3Lp GXB_TX_I1In					R26 G31				<u> </u>
GXB_L1		GXB_TX_L11n GXB_TX_L11p					G31 G32				
GXB_L1		GXB_RX_L11p,GXB_REFCLK_L11p					H34				
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					H33				
GXB_L1		GXB_TX_L10n					J31				
GXB_L1		GXB_TX_L10p					J32				
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p GXB_RX_L10n,GXB_REFCLK_L10n					K34				<u> </u>
GXB_L1 GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n GXB_TX_L9n					K33				-
GXB_L1		GXB_TX_L9p					L32				
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					M34				
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					M33				
GXB_L1		GXB_TX_L8n					N31				
GXB_L1		GXB_TX_L8p					N32				
GXB_L1		GXB_RX_L8p,GXB_REFCLK_L8p					P34				
GXB_L1 GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n GXB_TX_L7n					P33 R31				-
GXB_L1		GXB_TX_L7n					R32				†
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p		İ	İ	İ	T34		İ	İ	1
GXB L1		GXB RX L7n,GXB REFCLK L7n					T33				
GXB_L1		GXB_TX_L6n	<u> </u>				U31				
GXB_L1		GXB_TX_L6p					U32				
GXB_L1 GXB_L1		GXB_RX_L6p,GXB_REFCLK_L6p GXB_RX_L6n,GXB_REFCLK_L6n		1		1	V34 V33				
GXB_L1 GXB_L1		REFCLK2Ln					V33 U27				
GXB_L1		REFCLK2LD					U26				
GXB_L0		REFCLK1Ln					W27				
GXB_L0		REFCLK1Lp					W26				
GXB_L0		GXB_TX_L5n					W31				
GXB_L0		GXB_TX_L5p					W32				
GXB_L0		GXB_RX_L5p,GXB_REFCLK_L5p GXB_RX_L5n,GXB_REFCLK_L5n					Y34				ļ!
GXB_L0 GXB_L0		GXB_RX_L5n,GXB_REFCLK_L5n GXB_TX_L4n					Y33 AA31				
GXB_L0		GXB_TX_L4p					AA32				
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p					AB34				
GXB_L0		GXB RX L4n,GXB REFCLK L4n					AB33				
GXB_L0		GXB_TX_L3n					AC31				
GXB_L0		GXB_TX_L3p					AC32				
GXB_L0 GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p GXB_RX_L3n,GXB_REFCLK_L3n					AD34 AD33				
GXB_L0		GXB_TX_L2n					AE31				
GXB_L0		GXB TX L2p					AE32				
GXB_L0		GXB_RX_L2p,GXB_REFCLK_L2p					AF34				
GXB_L0		GXB_RX_L2n,GXB_REFCLK_L2n					AF33				
GXB_L0		GXB_TX_L1n					AG31				
GXB_L0		GXB_TX_L1p				-	AG32				ļ!
GXB_L0 GXB_L0		GXB_RX_L1p,GXB_REFCLK_L1p GXB_RX_L1n,GXB_REFCLK_L1n					AH34 AH33				
GXB_L0		GXB_TX_L0n					AJ31				
GXB_L0		GXB_TX_L0p		İ			AJ32				
GXB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AK34				
GXB L0		GXB RX L0n,GXB REFCLK L0n					AK33				
GXB_L0		REFCLK0Ln					AA28				
GXB_L0		REFCLK0Lp DNU				 	AA27 AL32				
34		TDO		TDO		 	AC28		 	 	
3A		TMS		TMS		 	AF30				
3A		TCK		TCK		1	AN32				
3A		TDI		TDI			AC29				
3A		DCLK		DCLK			AM32				
3A		nCSO		DATA4		L	AM34				
3A		AS_DATA3		DATA3		 	AM33	 			
3A 3A		AS_DATA2 AS_DATA1		DATA2 DATA1	1	t	AP33 AN33	1			
3A		AS_DATA1 AS_DATA0,ASDO		DATA1		 	AN34				
3A	VREFB3AN0	IO	RZQ_0		DIFFIO_TX_B1n	DIFFOUT_B1n	AL31				
3A	VREFB3AN0	10			DIFFIO_TX_B1p	DIFFOUT_B1p	AM31	DQ1B			
3A	VREFB3AN0		CLK0n		DIFFIO_RX_B2n	DIFFOUT_B2n	AP31	DQ1B			
	TITLE	10	CLK0p		DIFFIO_RX_B2p	DIFFOUT_B2p	AP32	DQ1B			
3A	VREFB3AN0	10		1	DIFFIO_TX_B3n	DIFFOUT_B3n	AD27	DOLD			
	VREFB3AN0 VREFB3AN0		CLK1n		DIFFIO_TX_B3p DIFFIO_RX_B4n	DIFFOUT_B3p DIFFOUT_B4n	AD26 AJ29	DQ1B DQSn1B/QK1B			
	VREFB3AN0 VREFB3AN0		CLK1p		DIFFIO_RX_B4n DIFFIO_RX_B4p	DIFFOUT_B4n	AK29	DQS1B/QR1B DQS1B/CQ1B/CQn1B/QKn1B	 	 	
	VREFB3AN0		FPLL BL CLKOUT1,FPLL BL CLKOUTn	1	DIFFIO_TX_B5n	DIFFOUT_B5n	AL30				1



Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0		DIFFIO_TX_B5p	DIFFOUT_B5p	AM30	DQ1B			
3A	VREFB3AN0	IO	FPLL_BL_CLKOUT3,FPLL_BL_FBn		DIFFIO_RX_B6n	DIFFOUT_B6n	AN30	DQ1B			
3A	VREFB3AN0	10	FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1		DIFFIO_RX_B6p	DIFFOUT_B6p	AP30	DQ1B			
3A	VREFB3AN0	10	VREFB3AN0				AE27		4		
3A	VREFB3AN0	10					AF28	DQ1B	4		
3A	VREFB3AN0	10	CLK2n		DIFFIO_RX_B7n	DIFFOUT_B7n	AH28	DQ1B			
3A	VREFB3ANO	10	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AJ28	DQ1B		-	00 // 04 4
3A 3A	VICE DOTTE	10			DIFFIO_TX_B8n	DIFFOUT_B8n	AL29	Doop	5045	-	CS#_3A_1
3A	VREFB3AN0 VREFB3AN0	io In	Cl K3n		DIFFIO_TX_B8p DIFFIO_RX_B9n	DIFFOUT_B8p DIFFOUT_B9n	AM29 AN29	DQ2B	DQ1B DQ1B	+	CS#_3A_0
3A	VREFB3AN0	10	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9n	AP29	DQ2B DQ2B	DQ1B	+	
3A		10	СЕКЗР		DIFFIO_RX_B9p	DIFFOUT_B9p	AE29	DQ2B	DQIB	+	ODT_3A_1
3A	VREFB3AN0	io			DIFFIO_TX_B10p	DIFFOUT_B10p	AF29	DQ2B	DQ1B	+	ODT_3A_0
3A	VREFB3AN0	10		_	DIFFIO_TX_B10p	DIFFOUT_B11n	AG27	DQSn2B/QK2B	DQ1B		WE#_3A
3A	VREFB3AN0	in			DIFFIO RX B11p	DIFFOUT_B11p	AH27	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B		CAS# 3A
3A	VREFB3AN0	10			DIFFIO TX B12n	DIFFOUT_B12n	AL28	DQGZB/CQZB/CQTIZB/QTTIZB	DQID		RAS#_3A
3A	VREFB3AN0	10			DIFFIO_TX_B12p	DIFFOUT_B12p	AM28	DQ2B	DQ1B		BA_3A_2
3A	VREFB3AN0	10			DIFFIO RX B13n	DIFFOUT B13n	AP27	DQ2B	DQ1B		BA 3A 1
3A	VREFB3AN0	10			DIFFIO_RX_B13p	DIFFOUT_B13p	AP28	DQ2B	DQ1B		BA_3A_0
3A	VREFB3AN0	10			DIFFIO TX B14n	DIFFOUT B14n	AG29				A 3A 15
3A	VREFB3AN0	10			DIFFIO_TX_B14p	DIFFOUT_B14p	AH29	DQ2B	DQ1B		A_3A_14
3A	VREFB3AN0	10			DIFFIO_RX_B15n	DIFFOUT_B15n	AK27	DQ2B	DQ1B		A_3A_13
3A	VREFB3AN0	10			DIFFIO_RX_B15p	DIFFOUT_B15p	AL27	DQ2B	DQ1B		A_3A_12
3A	VREFB3AN0	IO			DIFFIO_TX_B16n	DIFFOUT_B16n	AG26				A_3A_11
3A	VREFB3AN0	10			DIFFIO_TX_B16p	DIFFOUT_B16p	AH26	DQ3B	DQ1B		A_3A_10
3A	VREFB3AN0	IO			DIFFIO_RX_B17n	DIFFOUT_B17n	AJ26	DQ3B	DQ1B		A_3A_9
3A	VREFB3AN0	IO			DIFFIO_RX_B17p	DIFFOUT_B17p	AK26	DQ3B	DQ1B		A_3A_8
3A	VREFB3AN0	10			DIFFIO_TX_B18n	DIFFOUT_B18n	AD29				A_3A_7
011	VICE DOTTE	IO			DIFFIO_TX_B18p	DIFFOUT_B18p	AE28	DQ3B	DQ1B		A_3A_6
3A	VREFB3AN0	IO			DIFFIO_RX_B19n	DIFFOUT_B19n	AL26	DQSn3B/QK3B	DQSn1B/QK1B		A_3A_5
3A		IO			DIFFIO_RX_B19p	DIFFOUT_B19p	AM26	DQS3B/CQ3B/CQn3B/QKn3B	DQS1B/CQ1B/CQn1B/QKn1B		A_3A_4
3A	VREFB3AN0	10			DIFFIO_TX_B20n	DIFFOUT_B20n	AN27				A_3A_3
3A	VREFB3AN0	10			DIFFIO_TX_B20p	DIFFOUT_B20p	AN26	DQ3B	DQ1B		A_3A_2
3A	VREFB3AN0	10			DIFFIO_RX_B21n	DIFFOUT_B21n	AP25	DQ3B	DQ1B		A_3A_1
3A	VREFB3AN0	10			DIFFIO_RX_B21p	DIFFOUT_B21p	AP26	DQ3B	DQ1B		A_3A_0
3A	VREFB3AN0	10			DIFFIO_TX_B22n	DIFFOUT_B22n	AE26				CKE_3A_1
3A	VREFB3AN0	10			DIFFIO_TX_B22p	DIFFOUT_B22p	AF26	DQ3B	DQ1B		CKE_3A_0
3A	VREFB3AN0	10			DIFFIO_RX_B23n	DIFFOUT_B23n	AL25	DQ3B	DQ1B		CK#_3A
3A	VREFB3AN0	10			DIFFIO_RX_B23p	DIFFOUT_B23p	AM25	DQ3B	DQ1B		CK_3A
3B		10			DIFFIO_TX_B24n	DIFFOUT_B24n	AE23		.		RESET#_3A
3B	VREFB3BN0	10			DIFFIO TX B24p	DIFFOUT_B24p	AE24	DQ4B	DQ2B	DQ1B	DQ1_3B_8
3B	VREFB3BN0	10			DIFFIO_RX_B25n	DIFFOUT_B25n	AC24	DQ4B	DQ2B	DQ1B	DQ1_3B_7
3B	VREFB3BN0	10			DIFFIO_RX_B25p	DIFFOUT_B25p	AC25	DQ4B	DQ2B	DQ1B	DQ1_3B_6
3B	VREFB3BN0	10			DIFFIO_TX_B26n	DIFFOUT_B26n	AA25	DO 4D	Doop	DOLD	D144 0D
3B 3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_TX_B26p DIFFIO_RX_B27n	DIFFOUT_B26p DIFFOUT_B27n	AB25 AD24	DQ4B DQSn4B/QK4B	DQ2B DQ2B	DQ1B DQ1B	DM1_3B DQS#1_3B
		10									
3B 3B	VREFB3BN0 VREFB3BN0	10			DIFFIO_RX_B27p DIFFIO_TX_B28n	DIFFOUT_B27p DIFFOUT_B28n	AE25 AE25	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	DQ1B	DQS1_3B
3B	VREFB3BN0	10		+	DIFFIO_TX_B28p	DIFFOUT_B28p	AG24	DQ4B	DQ2B	DQ1B	DQ1_3B_5
3B	VREFB3BN0	10		+	DIFFIO_TX_B20p	DIFFOUT_B29n	AG24 AH24	DQ4B DQ4B	DQ2B	DQ1B	DQ1_3B_4
3B	VREFB3BN0	In .			DIFFIO_RX_B29p	DIFFOUT_B29p	AH25	DQ4B	DQ2B	DQ1B	DQ1_3B_4 DQ1_3B_3
3B	VREFB3BN0	in	VREFB3BN0		DII 1 IO_KX_D23p	Dii 1 OO1_D23p	Y23	DQ4B	DQZD	DQID	DQ1_3D_3
3B	VREFB3BN0	in	VICE BODING				AB24	DQ4B	DO2B	DQ1B	DQ1_3B_2
3B	VREFB3BN0	10		_	DIFFIO_RX_B30n	DIFFOUT_B30n	AJ25	DQ4B	DQ2B	DQ1B	DQ1_3B_1
3B	VREFB3BN0	io		+	DIFFIO_RX_B30p	DIFFOUT_B30p	AK24	DQ4B	DQ2B	DQ1B	DQ1_3B_0
3B	VREFB3BN0	10		1	DIFFIO_TX_B31n	DIFFOUT_B31n	AK23	1-3/-	1-3		
3B	VREFB3BN0	10		1	DIFFIO_TX_B31p	DIFFOUT_B31p	AL24	DQ5B	DQ2B	DQ1B	DQ2 3B 8
3B	VREFB3BN0	10		Ì	DIFFIO_RX_B32n	DIFFOUT_B32n	AF23	DQ5B	DQ2B	DQ1B	DQ2 3B 7
3B	VREFB3BN0	10		Ì	DIFFIO_RX_B32p	DIFFOUT_B32p	AG23	DQ5B	DQ2B	DQ1B	DQ2_3B_6
3B	VREFB3BN0	10		Ì	DIFFIO TX B33n	DIFFOUT B33n	AC23				
3B	VREFB3BN0	10			DIFFIO_TX_B33p	DIFFOUT_B33p	AD23	DQ5B	DQ2B	DQ1B	DM2_3B
3B	VREFB3BN0	10			DIFFIO_RX_B34n	DIFFOUT_B34n	AH23	DQSn5B/QK5B	DQSn2B/QK2B	DQ1B	DQS#2 3B
3B	VREFB3BN0	10			DIFFIO_RX_B34p	DIFFOUT_B34p	AJ23	DQS5B/CQ5B/CQn5B/QKn5B	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B	DQS2_3B
3B	VREFB3BN0	10			DIFFIO_TX_B35n	DIFFOUT_B35n	AL23				
3B	VREFB3BN0	10			DIFFIO_TX_B35p	DIFFOUT_B35p	AM23	DQ5B	DQ2B	DQ1B	DQ2_3B_5
3B	VREFB3BN0	10			DIFFIO_RX_B36n	DIFFOUT_B36n	AN23	DQ5B	DQ2B	DQ1B	DQ2_3B_4
3B	VREFB3BN0	IO			DIFFIO_RX_B36p	DIFFOUT_B36p	AN24	DQ5B	DQ2B	DQ1B	DQ2_3B_3
3B	VREFB3BN0	10			DIFFIO_TX_B37n	DIFFOUT_B37n	AA23				
3B		10			DIFFIO_TX_B37p	DIFFOUT_B37p	AB23	DQ5B	DQ2B	DQ1B	DQ2_3B_2
3B	VREFB3BN0	10			DIFFIO_RX_B38n	DIFFOUT_B38n	AP22	DQ5B	DQ2B	DQ1B	DQ2_3B_1
3B	VREFB3BN0	10			DIFFIO_RX_B38p	DIFFOUT_B38p	AP23	DQ5B	DQ2B	DQ1B	DQ2_3B_0
3C	VREFB3CN0	10			DIFFIO_TX_B39n	DIFFOUT_B39n	AE21		1		
3C	VREFB3CN0	IO			DIFFIO_TX_B39p	DIFFOUT_B39p	AE22	DQ6B	DQ3B	DQ1B	DQ3_3C_8
3C	VREFB3CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AL21	DQ6B	DQ3B	DQ1B	DQ3_3C_7
3C	VREFB3CN0	10			DIFFIO_RX_B40p	DIFFOUT_B40p	AL22	DQ6B	DQ3B	DQ1B	DQ3_3C_6
3C	VREFB3CN0	10			DIFFIO_TX_B41n	DIFFOUT_B41n	AB22				
3C	VREFB3CN0	10			DIFFIO_TX_B41p	DIFFOUT_B41p	AC22	DQ6B	DQ3B	DQ1B	DM3_3C
					DIFFIO_TX_B41p DIFFIO_RX_B42n DIFFIO_RX_B42p	DIFFOUT_B42n DIFFOUT_B42p	AC22 AH21 AH22	DQ6B DQSn6B/QK6B DQS6B/CQ6B/CQn6B/QKn6B	DQ3B DQ3B DQ3B	DQ1B DQSn1B/QK1B DQS1B/CQ1B/CQn1B/QKn1B	DM3_3C DQS#3_3C DQS3_3C



Number 3C 3C 3C											Note (1)
3C	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory
3C	VREFB3CN0	10			DIFFIO_TX_B43n	DIFFOUT_B43n	AF22				PHY (3)
3C	VREFB3CN0				DIFFIO_TX_B43II	DIFFOUT_B43n	AG21	DQ6B	DQ3B	DQ1B	DQ3_3C_5
	VREFB3CN0				DIFFIO RX B44n	DIFFOUT B44n	AJ22	DOGB	DO3B	DQ1B	DQ3_3C_4
_	VREFB3CN0				DIFFIO RX B44p	DIFFOUT_B44p	AK21	DQ6B	DQ3B	DQ1B	DQ3_3C_3
JU .	VREFB3CN0				DIFFIO_TX_B45n	DIFFOUT_B45n	AA21				
3C		10			DIFFIO_TX_B45p	DIFFOUT_B45p	AB21	DQ6B	DQ3B	DQ1B	DQ3_3C_2
3C		10			DIFFIO_RX_B46n	DIFFOUT_B46n	AM22	DQ6B	DQ3B	DQ1B	DQ3_3C_1
		10			DIFFIO_RX_B46p	DIFFOUT_B46p	AN21	DQ6B	DQ3B	DQ1B	DQ3_3C_0
3C	VREFB3CN0	10			DIFFIO_TX_B47n	DIFFOUT_B47n	AC21				
зC	VREFB3CN0	10			DIFFIO_TX_B47p	DIFFOUT_B47p	AD21	DQ7B	DQ3B	DQ1B	DQ4_3C_8
зC	VREFB3CN0	IO			DIFFIO_RX_B48n	DIFFOUT_B48n	AN20	DQ7B	DQ3B	DQ1B	DQ4_3C_7
зC		IO			DIFFIO_RX_B48p	DIFFOUT_B48p	AP20	DQ7B	DQ3B	DQ1B	DQ4_3C_6
зC	TITEL DOOLS	10			DIFFIO_TX_B49n	DIFFOUT_B49n	AA20				
зC	VREFB3CN0				DIFFIO_TX_B49p	DIFFOUT_B49p	AB20	DQ7B	DQ3B	DQ1B	DM4_3C
iC	VREFB3CN0	10			DIFFIO_RX_B50n	DIFFOUT_B50n	AL20	DQSn7B/QK7B	DQSn3B/QK3B	DQ1B	DQS#4_3C
iC	VREFB3CN0	10			DIFFIO_RX_B50p	DIFFOUT_B50p	AM20	DQS7B/CQ7B/CQn7B/QKn7B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B	DQS4_3C
iC		10			DIFFIO_TX_B51n	DIFFOUT_B51n	AJ20				
iC		10			DIFFIO_TX_B51p	DIFFOUT_B51p	AK20	DQ7B	DQ3B	DQ1B	DQ4_3C_5
iC	VREFB3CN0				DIFFIO_RX_B52n	DIFFOUT_B52n	AG20	DQ7B	DQ3B	DQ1B	DQ4_3C_4
iC .	VREFB3CN0	10	VIDEO COLO	-	DIFFIO_RX_B52p	DIFFOUT_B52p	AH20	DQ7B	DQ3B	DQ1B	DQ4_3C_3
<u></u>		10	VREFB3CN0	 		 	AC20	DO-TD	2002	DOLD	DO4 85 -
IC .		10 10		 	DIEERO DY DEG	DIFFOLIT DEG	AD20 AE20	DQ7B	DQ3B	DQ1B DQ1B	DQ4_3C_2 DQ4_3C_1
<u></u>		10		 	DIFFIO_RX_B53n	DIFFOUT_B53n		DQ7B	DQ3B	DQ1B	
ND.	VREFB3CN0			 	DIFFIO_RX_B53p	DIFFOUT_B53p	AF20	DQ7B	DQ3B	DQ1B	DQ4_3C_0
D D	VREFB3DN0	10			DIFFIO TX B70n	DIFFOUT B70n	AH19	DO®B	DO4B		1
ט	VREFB3DN0	10		+	DIFFIO_TX_B70p	DIFFOUT_B70p	AJ19	DQ8B	DQ4B	<u> </u>	+
3D 3D	VREFB3DN0 VREFB3DN0	10		+	DIFFIO_RX_B71n DIFFIO_RX_B71p	DIFFOUT_B71n DIFFOUT_B71p	AL19 AM19	DQ8B DQ8B	DQ4B DQ4B	<u> </u>	+
	VREFB3DN0 VREFB3DN0			+	DIFFIO_RX_B71p DIFFIO_TX_B72n	DIFFOUT_B72n	AM19 AB19	DQOD	D/M+D	<u> </u>	+
ND ND		10			DIFFIO_TX_B72p	DIFFOUT_B72p	AC19	DO8B	DQ4B		
<u>,D</u>	VREFB3DN0	10		-	DIFFIO_IX_B72p	DIFFOUT_B73n	AN18	DQSn8B/QK8B	DQ4B		+
SD.	VREFB3DN0	10			DIFFIO_RX_B73b	DIFFOUT_B73b	AP19	DOS8B/CO8B/COn8B/OKn8B	DQ4B		
.D		10			DIFFIO_TX_B74n	DIFFOUT_B74n	AE19	DQ36B/CQ6B/CQ16B/QK16B	DQ4B		
3D	VREFB3DN0	10			DIFFIO_TX_B74p	DIFFOUT_B74p	AF19	DQ8B	DQ4B		
3D	VREFB3DN0				DIFFIO_TX_B74p	DIFFOUT_B75n	AK18	DO8B	DO4B		
3D	VREFB3DN0	10			DIFFIO_RX_B75p	DIFFOUT_B75p	Al 18	DQ8B	DQ4B		
3D	VREFB3DN0	10	VREFB3DN0		DII 110_RX_D73p	DII 1 001_D/3p	AB18	DQOD	DQ+D		
3D	VREFB3DN0	10	VICE BODING				AA18	DO8B	DQ4B		+
3D	VREFB3DN0	IO	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AG18	DQ8B	DQ4B		
3D	VRFFB3DN0		CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AH18	DOSB	DQ4B		
∃D.	VREFB3DN0	IO			DIFFIO_TX_B77n	DIFFOUT_B77n	AN17				
3D	VREFB3DN0	10			DIFFIO_TX_B77p	DIFFOUT_B77p	AP17	DQ9B	DQ4B		
3D	VREFB3DN0	10	CLK5n		DIFFIO_RX_B78n	DIFFOUT_B78n	AG17	DQ9B	DQ4B		
3D	VREFB3DN0	10	CLK5p		DIFFIO_RX_B78p	DIFFOUT_B78p	AH17	DQ9B	DQ4B		
3D	VREFB3DN0	IO	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn		DIFFIO_TX_B79n	DIFFOUT_B79n	AA17				
3D	VREFB3DN0	10	FPLL_BC_CLKOUT0,FPLL_BC_CLKOUTp,FPLL_BC_FB0		DIFFIO_TX_B79p	DIFFOUT_B79p	AB17	DQ9B	DQ4B		
3D	VREFB3DN0	10	FPLL_BC_CLKOUT3,FPLL_BC_FBn		DIFFIO_RX_B80n	DIFFOUT_B80n	AJ17	DQSn9B/QK9B	DQSn4B/QK4B		
۶D	VREFB3DN0	IO	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B80p	DIFFOUT_B80p	AK17	DQS9B/CQ9B/CQn9B/QKn9B	DQS4B/CQ4B/CQn4B/QKn4B		
3D	VREFB3DN0				DIFFIO_TX_B81n	DIFFOUT_B81n	AL17				
۶D	VREFB3DN0				DIFFIO_TX_B81p	DIFFOUT_B81p	AM17	DQ9B	DQ4B		
iD		10	CLK6n	<u> </u>	DIFFIO_RX_B82n	DIFFOUT_B82n	AE17	DQ9B	DQ4B		<u> </u>
3D	VREFB3DN0		CLK6p		DIFFIO_RX_B82p	DIFFOUT_B82p	AF17	DQ9B	DQ4B		
iD		10		1	DIFFIO_TX_B83n	DIFFOUT_B83n	AC17				1
iD	VREFB3DN0	10			DIFFIO_TX_B83p	DIFFOUT_B83p	AC18	DQ9B	DQ4B		
iD	VREFB3DN0	10	CLK7n		DIFFIO_RX_B84n	DIFFOUT_B84n	AD17	DQ9B	DQ4B		ļ
iD	VREFB3DN0		CLK7p		DIFFIO_RX_B84p	DIFFOUT_B84p	AE18	DQ9B	DQ4B		
		VCCD_FPLL		-		1	Y17	 	ļ		1
		VCCA_FPLL		-		1	Y18	 	ļ		1
		DNU		-			AD18	 	ļ		
	VREFB4DN0			-	DIFFIO_TX_B93n	DIFFOUT_B93n	AP16				CS#_4D_1
D				1	DIFFIO_TX_B93p	DIFFOUT_B93p	AN15 AH16	DQ10B DQ10B	DQ5B		CS#_4D_0
	VREFB4DN0				DIEELO D:						1
4D	VREFB4DN0	10			DIFFIO_RX_B94n	DIFFOUT_B94n		D 0 10 D	DQ5B	†	A 4D :-
4D 4D	VREFB4DN0 VREFB4DN0	IO IO			DIFFIO_RX_B94p	DIFFOUT_B94p	AJ16	DQ10B	DQ5B		A_4D_15
4D 4D 4D	VREFB4DN0 VREFB4DN0 VREFB4DN0	10 10 10			DIFFIO_RX_B94p DIFFIO_TX_B95n	DIFFOUT_B94p DIFFOUT_B95n	AJ16 AE16	DQ10B	DQ5B		ODT_4D_1
4D 4D 4D 4D	VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0	IO IO IO IO			DIFFIO TX B95n DIFFIO TX B95p	DIFFOUT_B94p DIFFOUT_B95n DIFFOUT_B95p	AJ16 AE16 AF16	DQ10B DQ10B	DQ5B DQ5B		ODT_4D_1 ODT_4D_0
4D 4D 4D 4D 4D	VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0	10 10 10 10			DIFFIO_RX_B94p DIFFIO_TX_B95n DIFFIO_TX_B95p DIFFIO_RX_B96n	DIFFOUT_B94p DIFFOUT_B95n DIFFOUT_B95p DIFFOUT_B96n	AJ16 AE16 AF16 Y15	DQ10B DQ10B DQ10B DQSn10B/QK10B	DQ5B DQ5B DQ5B		ODT_4D_0 ODT_4D_0 WE#_4D
4D 4D 4D 4D 4D 4D	VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0	10 10 10 10 10 10			DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95p DIFFIO RX B96n DIFFIO RX B96p	DIFFOUT_B94p DIFFOUT_B95n DIFFOUT_B95p DIFFOUT_B96n DIFFOUT_B96p	AJ16 AE16 AF16 Y15 AA15	DQ10B DQ10B	DQ5B DQ5B		ODT_4D_0 ODT_4D_0 WE#_4D CAS#_4D
4D 4D 4D 4D 4D 4D 4D 4D	VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0 VREFB4DN0	10 10 10 10 10 10 10			DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95p DIFFIO RX B96n DIFFIO RX B96n DIFFIO RX B96p DIFFIO TX B97n	DIFFOUT B94p DIFFOUT B95n DIFFOUT B95p DIFFOUT B96n DIFFOUT B96p DIFFOUT B97n	AJ16 AE16 AF16 Y15 AA15 AB16	DQ10B DQ10B/DQSn10B/QK10B DQS10B/CQ10B/CQn10B/QKn10B	DQ5B DQ5B DQ5B DQ5B		ODT_4D_1 ODT_4D_0 WE#_4D CAS#_4D RAS#_4D
4D 4D 4D 4D 4D 4D 4D 4D 4D	VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO	10 10 10 10 10 10 10 10			DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95p DIFFIO RX B96n DIFFIO RX B96n DIFFIO RX B96p DIFFIO TX B97n DIFFIO TX B97p	DIFFOUT B95n DIFFOUT B95n DIFFOUT B96n DIFFOUT B96n DIFFOUT B96p DIFFOUT B97n DIFFOUT B97p	AJ16 AE16 AF16 Y15 AA15 AB16 AC16	DQ10B DQ10B DQ510B/CQ10B/CQn10B/QKn10B DQ510B/CQ10B/CQn10B/QKn10B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		ODT 4D 1 ODT 4D 0 WE# 4D CAS# 4D RAS#_4D BA_4D_2
4D 4D 4D 4D 4D 4D 4D 4D 4D 4D	VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO	10 10 10 10 10 10 10 10 10			DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95p DIFFIO RX B96n DIFFIO RX B96p DIFFIO TX B97n DIFFIO TX B97n DIFFIO TX B97n DIFFIO RX B98n	DIFFOUT B94p DIFFOUT B95n DIFFOUT B95p DIFFOUT B96n DIFFOUT B96p DIFFOUT B97n DIFFOUT B97p DIFFOUT B97p DIFFOUT B98n	AJ16 AE16 AF16 Y15 AA15 AB16 AC16 AL16	DQ10B DQ10B DQ510B/CQ1	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		ODT_4D_1 ODT_4D_0 WE#_4D CAS#_4D RAS#_4D BA_4D_2 BA_4D_1
4D 4D 4D 4D 4D 4D 4D 4D 4D 4D	VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO	10 10 10 10 10 10 10 10 10 10 10 10 10 1	I/DEEDATAMA		DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95p DIFFIO RX B96n DIFFIO RX B96n DIFFIO RX B96p DIFFIO TX B97n DIFFIO TX B97p	DIFFOUT B95n DIFFOUT B95n DIFFOUT B96n DIFFOUT B96n DIFFOUT B96p DIFFOUT B97n DIFFOUT B97p	AJ16 AE16 AF16 Y15 AA15 AB16 AC16 AL16 AM16	DQ10B DQ10B DQ510B/CQ10B/CQn10B/QKn10B DQ510B/CQ10B/CQn10B/QKn10B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		ODT 4D 1 ODT 4D 0 WE# 4D CAS# 4D RAS# 4D BA 4D 2
4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D	VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO	10 10 10 10 10 10 10 10 10 10 10 10 10 1	VREFB4DN0		DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95p DIFFIO RX B96n DIFFIO RX B96p DIFFIO TX B97n DIFFIO TX B97n DIFFIO TX B97n DIFFIO RX B98n	DIFFOUT B94p DIFFOUT B95n DIFFOUT B95p DIFFOUT B96n DIFFOUT B96p DIFFOUT B97n DIFFOUT B97p DIFFOUT B97p DIFFOUT B98n	AJ16 AE16 AF16 Y15 AA15 AB16 AC16 AL16 AM16 AJ14	DQ10B DQ10B DQ310B/QK10B DQ310B/QK10B DQ310B/CQ10B/CQn10B/QKn10B DQ10B DQ10B DQ10B DQ10B	DOSB DOSB DOSB DOSB DOSB DOSB DOSB DOSB		ODT_4D_1 ODT_4D_0 WE# 4D CAS# 4D RAS#_4D BA_4D_2 BA_4D_0
4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4	VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO VREFB4DNO	10 10 10 10 10 10 10 10 10 10 10 10 10 1	VREFB4DN0		DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95n DIFFIO TX B95p DIFFIO RX B96n DIFFIO RX B96p DIFFIO TX B97p DIFFIO RX B98n DIFFIO RX B98n DIFFIO RX B98p	DIFFOUT B94p DIFFOUT B95p DIFFOUT B95p DIFFOUT B96n DIFFOUT B96n DIFFOUT B97n DIFFOUT B97p DIFFOUT B97p DIFFOUT B98p	AJ16 AE16 AF16 Y15 AA15 AB16 AC16 AC16 AL16 AM16 AJ14 AK14	DQ10B DQ10B DQ510B/CQ10B/CQ110B/CQN10B/CQN10B/CQ10B DQ10B DQ10B DQ10B DQ10B DQ10B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		ODT_4D_1 ODT_4D_0 WE#_4D CAS#_4D RAS#_4D BA_4D_2 BA_4D_1 BA_4D_0 A_4D_14
4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4	VREFB4DNO VREFB4DNO	10 10 10 10 10 10 10 10 10 10 10 10 10 1	VREFB4DN0		DIFFIO RX B94p DIFFIO TX B95p DIFFIO TX B95p DIFFIO RX B96p DIFFIO RX B96p DIFFIO RX B96p DIFFIO RX B97p DIFFIO TX B97p DIFFIO RX B98p DIFFIO RX B98p DIFFIO RX B98p	DIFFOUT B94p DIFFOUT B95n DIFFOUT B95p DIFFOUT B95p DIFFOUT B96p DIFFOUT B97n DIFFOUT B97n DIFFOUT B98p DIFFOUT B98p DIFFOUT B98p	AJ16 AE16 AF16 Y15 AA15 AB16 AC16 AL16 AL16 AJ14 AK14 AL14	DQ10B DQ10B DQ310B/QK10B DQ310B/QK10B/CQn10B/QKn10B DQ10B DQ10B DQ10B DQ10B DQ10B DQ10B	DOSB DOSB DOSB DOSB DOSB DOSB DOSB DOSB		ODT_4D_1 ODT_4D_0 WE#_4D CAS#_4D RAS#_4D BA_4D_2 BA_4D_1 BA_4D_0 A_4D_13
4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4	VREFB4DNO VREFB4DNO	10 10 10 10 10 10 10 10 10 10 10 10 10 1	VREFB4DN0		DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95n DIFFIO RX B96n DIFFIO RX B96n DIFFIO RX B96n DIFFIO RX B97n DIFFIO TX B97n DIFFIO RX B98n DIFFIO RX B98p DIFFIO RX B98p DIFFIO RX B98p	DIFFOUT B94p DIFFOUT B95n DIFFOUT B95p DIFFOUT B95p DIFFOUT B96p DIFFOUT B97n DIFFOUT B97n DIFFOUT B97n DIFFOUT B98p DIFFOUT B98p DIFFOUT B98p	AJ16 AE16 AF16 Y15 AA15 AB16 AC16 AL16 AM16 AJ14 AK14 AM14	DQ10B DQ10B DQ510B/CQ10B/CQ110B/CQN10B/CQN10B/CQ10B DQ10B DQ10B DQ10B DQ10B DQ10B	DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B DQ5B		ODT 4D 1 ODT 4D 0 WE# 4D CAS# 4D RAS# 4D BA 4D 2 BA 4D 1 BA 4D 10 A 4D 14 A 4D 13 A 4D 12
4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4	VREFB4DNO VREFB4DNO	10	VREFB4DN0		DIFFIO RX B94p DIFFIO TX B95p DIFFIO TX B95p DIFFIO RX B96p DIFFIO RX B96p DIFFIO TX B97n DIFFIO TX B97n DIFFIO TX B97n DIFFIO TX B98p DIFFIO TX B98p DIFFIO RX B98p DIFFIO RX B98p DIFFIO RX B99p DIFFIO RX B99p DIFFIO RX B99p	DIFFOUT B94p DIFFOUT B95n DIFFOUT B95n DIFFOUT B95n DIFFOUT B96n DIFFOUT B96n DIFFOUT B97n DIFFOUT B97n DIFFOUT B98n DIFFOUT B98n DIFFOUT B98n DIFFOUT B99n DIFFOUT B99n DIFFOUT B99n DIFFOUT B99n DIFFOUT B99p	AJ16 AE16 AF16 AF16 AF15 AA15 AB16 AC16 AL16 AM16 AJ14 AK14 AL14 AM14 AA14	DQ10B DQ10B DQ5n10B/QK10B DQ510B/CQ10B/CQn10B/QKn10B DQ10B DQ10B DQ10B DQ10B DQ10B DQ10B DQ10B DQ10B DQ10B	DOSB DOSB DOSB DOSB DOSB DOSB DOSB DOSB		ODT 4D 1 ODT 4D 0 WE# 4D CAS# 4D RAS# 4D BA 4D 2 BA 4D 1 BA 4D 0 A 4D 14 A 4D 13 A 4D 12 A 4D 11
4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4D 4	VREFB4DNO VREFB4DNO	10	VREFB4DN0		DIFFIO RX B94p DIFFIO TX B95n DIFFIO TX B95n DIFFIO RX B96n DIFFIO RX B96n DIFFIO RX B96n DIFFIO RX B97n DIFFIO TX B97n DIFFIO RX B98n DIFFIO RX B98p DIFFIO RX B98p DIFFIO RX B98p	DIFFOUT B94p DIFFOUT B95n DIFFOUT B95p DIFFOUT B95p DIFFOUT B96p DIFFOUT B97n DIFFOUT B97n DIFFOUT B97n DIFFOUT B98p DIFFOUT B98p DIFFOUT B98p	AJ16 AE16 AF16 Y15 AA15 AB16 AC16 AL16 AM16 AJ14 AK14 AM14	DQ10B DQ10B DQ310B/QK10B DQ310B/QK10B/CQn10B/QKn10B DQ10B DQ10B DQ10B DQ10B DQ10B DQ10B	DOSB DOSB DOSB DOSB DOSB DOSB DOSB DOSB		ODT 4D 1 ODT 4D 0 WE# 4D CAS# 4D RAS# 4D BA 4D 2 BA 4D 1 BA 4D 0 A 4D 14 A 4D 13 A 4D 12



DDR3/DDR2 VRFF PinName/Function (2) ptional Function(s) Configuration Dedicated Tx/Rx Emulated LVDS F1152 DOS for X8/X9 DOS for X16/ X18 DOS for X32/ X36 Number Function Channel Output Channel hard memory PHY (3) DIFFOUT_B102n 4D VREFB4DN0 DIFFIO_TX_B102n AG14 A_4D_7 DIFFIO_TX_B102p DIFFOUT_B102p AH14 DQ11B DQ5B A 4D 6 VREFB4DN0 DIFFIO_RX_B103n DIFFOUT_B103r AG15 DQSn11B/QK11E DQSn5B/QK5E VREFB4DN0 IC DIFFIO_RX_B103p DIFFOUT_B103p AH15 DQS11B/CQ11B/CQn11B/QKn11B DQS5B/CQ5B/CQn5B/QKn5B A_4D_4 4D VREFB4DN0 IO DIFFIO_TX_B104n DIFFOUT_B104n AD15 A_4D_3 VREFB4DN0 IC DIFFIO_TX_B104p DIFFOUT_B104p AE15 DQ11B A 4D 2 DQ5B 4D VREFB4DN0 DIFFIO_RX_B105n DIFFOUT_B105n DQ11B DQ5B A_4D_1 VREFB4DN0 DIFFIO_RX_B105p DIFFOUT_B105p DQ5B A_4D_0 VREFB4DN0 IC DIFFIO TX B106n DIFFOUT B106n CKE 4D 1 VREFB4DN0 IO DIFFIO_TX_B106p DIFFOUT_B106p DQ11B DQ5B CKE_4D_0 4D VREFB4DN0 IC DIFFIO_RX_B107n DIFFOUT_B107n AC14 DQ11B DQ5B CK#_4D VREFB4DN0 DIFFIO RX B107p DIFFOUT B107p DQ5B CK_4D DIFFIO_TX_B108n DIFFOUT_B108r RESET#_4D VREFB4CN0 DIFFIO_TX_B108p DIFFOUT_B108p AC13 DQ6B DQ1_4C_8 DIFFIO_RX_B109n DIFFOUT_B109 AN14 VREFR4CN0 DIFFIO RX B109p DIFFOUT B109p AP14 DO12B DO6B DO2B DQ1 4C 6 VREEB4CN0 IC DIFFIO TX B110n DIFFOLIT B110n AN12 VREEB4CN0 IC DIFFIO TX B110p DIFFOUT B110p AP13 DO12B DO6B DO2B DM1 4C VRFFB4CN0 I DIFFIO_RX_B111n DIFFOUT_B111n Al 13 DQSn12B/QK12E DQ6B DQ2B DQS#1_4C VRFFB4CN0 DIFFIO RX B111p DIFFOUT B111p AM13 DQS12B/CQ12B/CQn12B/QKn12B DO6B DQ2B DOS1 4C VRFFB4CN0 DIFFIO TX B112n DIFFOUT B112n Y11 VRFFB4CN0 IC DIFFIO TX B112n DIFFOUT B112n AA12 DO6B DO2B DQ1 4C 5 VREFB4CN0 IC DIFFIO RX B113n DIFFOUT B113n AK12 DQ12B DQ6B DQ2B DQ1 4C 4 DIFFIO RX B113p DIFFOUT B113p DQ1 4C 3 VREFB4CN0 IC AL12 DQ12B DQ6B DQ2B VREFB4CN0 REFB4CN0 AK11 DQ12B DO6B DQ2B DQ1 4C 2 VRFFB4CN0 AI 11 DIFFIO_RX_B114n DIFFOUT_B114n DQ12B VRFFB4CN0 AH13 DO6B DO2B DQ1_4C_1 VRFFB4CN0 DIFFIO RX B114p DIFFOUT B114p A.J13 DQ12B DQ6B DO2B DQ1_4C_0 DIFFIO TX B115n DIFFOUT B115n VREFB4CN0 IO VREFB4CN0 IO DIFFIO_TX_B115p DIFFOUT_B115p AB12 DQ13B DQ6B DQ2B DQ2_4C_8 VREFB4CN0 IO DIFFIO_RX_B116n DIFFOUT_B116n AG12 DQ13B DQ2_4C_7 DQ6B DQ2B VREFB4CN0 IC DIFFIO_RX_B116p DIFFOUT_B116p AH12 DQ13B DQ2B DQ2 4C 6 DIFFIO_TX_B117n DIFFOUT_B117n VREFB4CN0 AH11 DIFFIO_TX_B117p DIFFOUT_B117p DIFFIO_RX_B118n DIFFOUT_B118n VREFB4CN0 DQSn13B/QK13B DQS#2_4C DQS6B/CQ6B/CQn6B/QKn6B VREFB4CN0 DIFFIO_RX_B118p DIFFOUT_B118p AF13 DQS13B/CQ13B/CQn13B/QKn13B DQS2_4C VREFB4CN0 DIFFIO_TX_B119n DIFFOUT_B119n VREFB4CN0 DIFFIO_TX_B119p DIFFOUT_B119p DQ2_4C_5 VREFB4CN0 DIFFIO_RX_B120n DIFFOUT_B120n AD12 DQ13B DQ6B DQ2B DQ2_4C_4 DIFFIO_RX_B120p DIFFOUT_B120p VREFB4CN0 DIFFIO TX B121n DIFFOUT B121 AD11 VREFR4CN0 IO DIFFIO TX B121p DIFFOUT B121p AF11 DO13B DO6B DO2B DO2 4C 2 VREERACNO IO DIFFIO RX B122n DIFFOLIT B122n AF11 DO13B DO6B DO2B DO2 4C 1 VREFR4CN0 IO DIFFIO RX B122p DIFFOUT B122p AG11 DO13B DO6B DO2B DO2 4C 0 VREFB4BN0 DIFFIO_TX_B123n DIFFOUT_B123n VREFB4BN0 DIFFIO_TX_B123p DIFFOUT_B123p AF9 DQ14B DQ7B DQ3 4B 8 VREFB4BN0 DIFFIO_RX_B124n DIFFOUT_B124n AM11 DQ14B DQ7B DQ2B DQ3_4B_7 DIFFIO RX B124p DIFFOUT B124p VREFB4BN0 AN11 DQ14B DQ7B DQ2B DQ3 4B 6 VREFRARNO I DIFFIO TX B125n DIFFOLIT B125n AI 10 DM3 4R VREERARNO IC DIFFIO TX B125n DIFFOLIT B125n AM10 DO14B DO7B DO2B VRFFB4BN0 IC DIFFIO RX B126n DIFFOUT B126n AP10 DQSn14B/QK14B DO7B DQSn2B/QK2B DOS#3 4B DQS14B/CQ14B/CQn14B/QKn14B DQS2B/CQ2B/CQn2B/QKn2B VRFFB4BN0 DIFFIO_RX_B126p DIFFOUT_B126p AP11 DQ7B DOS3 4B VRFFB4BN0 DIFFIO_TX_B127n DIFFOUT_B127n AA10 DQ3 4B 5 VRFFB4BN0 IO DIFFIO TX B127p DIFFOUT B127p AB10 DQ14B DQ7B DO2B DIFFIO_RX_B128n DIFFOUT_B128n AH10 DQ14B DQ2B DQ3_4B_4 VREFB4BN0 IO DQ7B DIFFIO RX B128p DIFFOUT B128p DQ14B DQ3_4B_3 VREFB4BN0 IO AJ10 DQ7B DQ2B DIFFIO TX B129n DIFFOUT B129n VREFB4BN0 IC AK9 DQ3_4B_2 VREFB4BN0 DIFFIO_TX_B129p DIFFOUT_B129p DQ14B DQ7B DIFFIO_RX_B130n DIFFOUT_B130n AN9 DQ14B DQ3_4B_1 VREFB4BN0 DQ7B DQ2B VREFB4BN0 DIFFIO RX B130p DIFFOUT B130p AN8 DQ14B DQ2B DQ3 4B 0 DIFFIO_TX_B131n DIFFOUT_B131n VREFB4BN0 VREFB4BN0 DIFFIO_TX_B131p DIFFOUT_B131p DQ7B DQ2B DQ4_4B_8 DIFFIO_RX_B132n DIFFOUT_B132n AG9 DQ15B DQ7B DQ2B DQ4_4B_7 VREFB4BN0 DIFFIO_RX_B132p DIFFOUT_B132p DQ15B DQ4_4B_6 VREFB4BN0 DIFFIO_TX_B133n DIFFOUT_B133n VREFB4BN0 DIFFIO_TX_B133p DIFFOUT_B133p DQ2B VREFR4RNO DIFFIO RX B134n DIFFOLIT B134r AI 8 DOSn15R/OK15R DOS#4 4B 4B VREFB4BN0 DIFFIO_RX_B134p DIFFOUT_B134p AMA DOS15B/CO15B/COn15B/OKn15B DQS7B/CQ7B/CQn7B/QKn7B DO2B DOS4 4B 4B VREFB4BN0 IO DIFFIO_TX_B135n DIFFOUT_B135n AC8 VREFB4BN0 DIFFIO_TX_B135p DIFFOUT_B135p DQ4_4B_5 VREFB4BN0 DIFFIO_RX_B136n DIFFOUT_B136n A.I8 DQ15B DQ2B DQ4_4B_4 VREFB4BN0 DIFFIO_RX_B136p DIFFOUT_B136p AK8 DQ15B 007B DQ2B DQ4 4B 3 V/PEEB/BNIO PEER/BNO VREERARNO IC AF8 DO15B DO7B DO2B DO4 4B 2 4R VREFRARNO IC DIFFIO RX B137n DIFFOLIT B137n AG8 DO15B DO7B DO2B DO4 4B 1 VREERARNO IO DIFFIO RX B137n DIFFOLIT B137n AHR DO15B DO7B DO2B DO4 4B 0 VRFFB4AN0 DATA10 DIFFIO_TX_B154n DIFFOUT_B154n AP8 VRFFB4AN0 DATA11 DIFFIO_TX_B154p DIFFOUT_B154p AP7 DQ16B DO8B 4A VRFFB4AN0 IC DATA5 DIFFIO_RX_B155n DIFFOUT_B155n Al 7 DQ16B DO8B



											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
4A	VREFB4AN0	Ю		DATA6	DIFFIO_RX_B155p	DIFFOUT_B155p	AM7	DQ16B	DQ8B		1111 (5)
4A		10		DATA12	DIFFIO_TX_B156n	DIFFOUT_B156n	AM6				
4A	VREFB4AN0			DATA13	DIFFIO_TX_B156p	DIFFOUT_B156p DIFFOUT_B157n	AN6	DQ16B DQSn16B/QK16B	DQ8B		
4A 4A	VREFB4AN0 VREFB4AN0	10		DATA7 DATA8	DIFFIO_RX_B157n DIFFIO_RX_B157p	DIFFOUT_B157p	AP6 AP5	DQSn16B/QK16B DQS16B/CQ16B/CQn16B/QKn16B	DQ8B DQ8B		+
4A	VREFB4AN0			DATA14	DIFFIO_TX_B158n	DIFFOUT_B158n	AF7	DQ316B/CQ16B/CQII16B/QKI116B	БООВ		+
4A	VREFB4AN0			DATA15	DIFFIO_TX_B158p	DIFFOUT_B158p	AF7	DQ16B	DQ8B		
4A	VREFB4AN0	10		DATA9	DIFFIO_RX_B159n	DIFFOUT_B159n	AM5	DQ16B	DQ8B		
4A	VREFB4AN0	10		CLKUSR	DIFFIO_RX_B159p	DIFFOUT_B159p	AN5	DQ16B	DQ8B		
4A 4A	VREFB4AN0 VREFB4AN0	10	VREFB4AN0				AK6 AL6	DQ16B	DQ8B		
4A 4A	VREFB4AN0 VREFB4AN0		CLK11n		DIFFIO_RX_B160n	DIFFOUT_B160n	AL6 AH7	DQ16B	DQ8B	<u> </u>	
4A	VREFB4AN0		CLK11p		DIFFIO RX B160p	DIFFOUT_B160p	AJ7	DQ16B	DQ8B		_
4A	VREFB4AN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B161n	DIFFOUT_B161n	AD6				
4A	VREFB4AN0		FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B161p	DIFFOUT_B161p	AE6	DQ17B	DQ8B		
4A 4A	VREFB4AN0 VREFB4AN0		FPLL_BR_CLKOUT3,FPLL_BR_FBn		DIFFIO_RX_B162n	DIFFOUT_B162n	AP3 AP4	DQ17B	DQ8B		
4A 4A	VREFB4AN0 VREFB4AN0	10	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B162p DIFFIO_TX_B163n	DIFFOUT_B162p DIFFOUT_B163n	AP4 AH6	DQ17B	DQ8B	+	+
4A	VREFB4AN0	10			DIFFIO_TX_B163p	DIFFOUT B163p	AJ6	DO17B	DO8B		+
4A	VREFB4AN0	10	CLK10n		DIFFIO_RX_B164n	DIFFOUT_B164n	AP2	DQSn17B/QK17B	DQSn8B/QK8B		1
4A	VREFB4AN0		CLK10p		DIFFIO_RX_B164p	DIFFOUT_B164p	AN3	DQS17B/CQ17B/CQn17B/QKn17B	DQS8B/CQ8B/CQn8B/QKn8B		
4A	VREFB4AN0			1	DIFFIO_TX_B165n	DIFFOUT_B165n	AC7	20172	2002	ļ	+
4A 4A	VREFB4AN0 VREFB4AN0		CLK9n	+	DIFFIO_TX_B165p DIFFIO_RX_B166n	DIFFOUT_B165p DIFFOUT_B166n	AC6 AL4	DQ17B DQ17B	DQ8B DQ8B		+
4A	VREFB4AN0 VREFB4AN0		CLK9n CLK9p	1	DIFFIO_RX_B166n DIFFIO_RX_B166p	DIFFOUT_B166n	AL4 AL5	DQ17B DQ17B	DQ8B	 	+
4A	VREFB4AN0		OE 10p		DIFFIO_TX_B167n	DIFFOUT_B167n	AM3	545	5405		1
4A	VREFB4AN0	10	RZQ_1		DIFFIO_TX_B167p	DIFFOUT_B167p	AM4	DQ17B	DQ8B		
4A	VREFB4AN0	10	CLK8n		DIFFIO_RX_B168n	DIFFOUT_B168n	AF6	DQ17B	DQ8B		
4A	VREFB4AN0		CLK8p		DIFFIO_RX_B168p	DIFFOUT_B168p	AG6	DQ17B	DQ8B		
		RREF_BR DNU					AM1 AM2				
		DNU					AN2	 		<u> </u>	+
GXB R0		REFCLK0Rp					AA8				+
GXB_R0		REFCLK0Rn					AA7				
GXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n					AK2				
GXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p					AK1				
GXB_R0 GXB_R0	+	GXB_TX_R0p GXB_TX_R0n					AJ3 AJ4				
GXB_R0		GXB_RX_R1n,GXB_REFCLK_R1n					AH2				
GXB_R0		GXB_RX_R1p,GXB_REFCLK_R1p					AH1				
GXB_R0		GXB_TX_R1p					AG3				
GXB_R0		GXB_TX_R1n					AG4				
GXB_R0 GXB_R0	+	GXB_RX_R2n,GXB_REFCLK_R2n GXB_RX_R2p,GXB_REFCLK_R2p					AF2 AF1				
GXB_R0	+	GXB_TX_R2p					AE3				+
GXB_R0		GXB_TX_R2n					AE4				1
GXB_R0		GXB_RX_R3n,GXB_REFCLK_R3n					AD2				
GXB_R0		GXB_RX_R3p,GXB_REFCLK_R3p					AD1				
GXB_R0 GXB_R0	+	GXB_TX_R3p GXB_TX_R3n					AC3 AC4				
GXB_R0		GXB RX R4n.GXB REFCLK R4n					AB2				+
GXB_R0		GXB_RX_R4p,GXB_REFCLK_R4p		1		1	AB1	<u> </u>		<u> </u>	
GXB_R0		GXB_TX_R4p					AA3				
GXB_R0	1	GXB_TX_R4n					AA4	-	1		
GXB_R0 GXB_R0	+	GXB_RX_R5n,GXB_REFCLK_R5n GXB_RX_R5p,GXB_REFCLK_R5p		+	+	1	Y2 Y1	+		 	+
GXB_R0	 	GXB_RX_R5p,GXB_REFCLK_R5p GXB_TX_R5p	<u> </u>	+	+	†	W3	1	1	1	+
GXB_R0		GXB_TX_R5n				İ	W4	<u> </u>	İ	<u> </u>	
GXB_R0		REFCLK1Rp					W9				
GXB R0		REFCLK1Rn		1	1		W8	ļ		ļ	+
GXB_R1		REFCLK2Rp		+	+	 	U9 U8			-	+
GXB_R1 GXB_R1	1	REFCLK2Rn GXB_RX_R6n,GXB_REFCLK_R6n		1	1	1	V2	1	1	 	+
GXB_R1	1	GXB_RX_R6p,GXB_REFCLK_R6p			1	1	V2 V1				1
GXB_R1		GXB_TX_R6p					U3				
GXB_R1	_	GXB_TX_R6n					U4				\bot
GXB_R1	+	GXB_RX_R7n,GXB_REFCLK_R7n	 	1	+	 	T2 T1	 	 	 	+
GXB_R1 GXB_R1	1	GXB_RX_R7p,GXB_REFCLK_R7p GXB_TX_R7p		1	1	1	R3	1	1	 	+
GXB_R1	1	GXB TX R7n				1	R4				1
GXB_R1		GXB_RX_R8n,GXB_REFCLK_R8n					P2				1
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					P1				
GXB_R1	1	GXB_TX_R8p					N3	-	1		+
GXB_R1 GXB_R1	 	GXB_TX_R8n GXB_RX_R9n,GXB_REFCLK_R9n		+	+	 	N4 M2				+
GXB_R1 GXB_R1	1	GXB_RX_R9n,GXB_REFCLK_R9n GXB_RX_R9p,GXB_REFCLK_R9p		1	1	1	M2 M1	1	1	 	+
GXB_R1	†	GXB_TX_R9p,GAB_REFCER_R9p			1	İ	L3	<u> </u>		 	
GXB_R1		GXB_TX_R9n					L4				
GXB_R1	1	GXB_RX_R10n,GXB_REFCLK_R10n				1	K2				



											Note (1
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
GXB_R1	1	GXB_RX_R10p,GXB_REFCLK_R10p					K1				FH1 (3)
GXB_R1	1	GXB_TX_R10p					.13				+
GXB_R1		GXB_TX_R10n					J4				_
GXB R1		GXB_RX_R11n,GXB_REFCLK_R11n					H2				_
GXB_R1		GXB RX R11p,GXB REFCLK R11p					H1			İ	+
GXB_R1		GXB_TX_R11p					G3				+
GXB_R1		GXB_TX_R11n					G4				+
GXB_R1		REFCLK3Rp					R9				+
GXB_R1	+	REFCLK3Rn					R8				+
GAB_RT	+	DNU					K5				+
7A		GND					H5				+
7.4	VREFB7AN0	IO	CLK12p		DIFFIO_RX_T1p	DIFFOUT_T1p	E3	DOAT	DQ1T		-
7A					DIFFIO_RX_11p		E4	DQ1T DQ1T	DQ1T	1	-
7A	VREFB7AN0 VREFB7AN0		CLK12n RZQ 5		DIFFIO_RX_11h	DIFFOUT_T1n DIFFOUT T2p	E4	DQ1T	DQ1T	-	+
/A			RZQ_5					DQ11	DQ11		_
7A	VREFB7AN0		0.11.0		DIFFIO_TX_T2n	DIFFOUT_T2n	F1				_
7A	VREFB7AN0		CLK13p		DIFFIO_RX_T3p	DIFFOUT_T3p	D1	DQ1T	DQ1T		_
7A	VREFB7AN0		CLK13n		DIFFIO_RX_T3n	DIFFOUT_T3n	E2	DQ1T	DQ1T		
7A	VREFB7AN0				DIFFIO_TX_T4p	DIFFOUT_T4p	G6	DQ1T	DQ1T		
7A	VREFB7AN0				DIFFIO_TX_T4n	DIFFOUT_T4n	H6				
7A	VREFB7AN0		CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	C1	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T		
7A	VREFB7AN0	10	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	C2	DQSn1T/QK1T	DQSn1T/QK1T		
7A	VREFB7AN0	Ю			DIFFIO_TX_T6p	DIFFOUT_T6p	E5	DQ1T	DQ1T	<u> </u>	
7A	VREFB7AN0				DIFFIO_TX_T6n	DIFFOUT_T6n	F6				
7A	VREFB7AN0	Ю	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p	DIFFOUT_T7p	C3	DQ1T	DQ1T		
7A	VREFB7AN0		FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO_RX_T7n	DIFFOUT_T7n	D3	DQ1T	DQ1T		
7A	VREFB7AN0	IO	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0		DIFFIO_TX_T8p	DIFFOUT_T8p	J6	DQ1T	DQ1T		
7A	VREFB7AN0	10	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn		DIFFIO_TX_T8n	DIFFOUT_T8n	K6				1
7A	VREFB7AN0		CLK15p		DIFFIO_RX_T9p	DIFFOUT_T9p	A3	DQ2T	DQ1T	İ	1
7A	VREFB7AN0		CLK15n		DIFFIO_RX_T9n	DIFFOUT_T9n	B3	DQ2T	DQ1T		+
7A	VREFB7AN0		OEI(13))		DII 110_IOX_1311	DII 1 001_1311	16	DO2T	DQ1T		+
74	TITLE BITTER	.0	VREFB7AN0		1	1	M7	DQZI	DQTT		+
7A	VREFB7AN0		VKEFB/ANU	DEV OF	DIFFIO_RX_T10p	DIFFOUT T10p	C6	DO2T	DO1T	1	-
/A				DE 1_0E				DOLL			
/A	VREFB7AN0			DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	D5	DQ2T	DQ1T		_
7A	VREFB7AN0			nPERSTR0	DIFFIO_TX_T11p	DIFFOUT_T11p	A2	DQ2T	DQ1T		
7A	VREFB7AN0			nPERSTL0	DIFFIO_TX_T11n	DIFFOUT_T11n	B2				
7A	VREFB7AN0			CvP_CONFDONE	DIFFIO_RX_T12p	DIFFOUT_T12p	B5	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T		
7A	VREFB7AN0			CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	C4	DQSn2T/QK2T	DQ1T		
7A	VREFB7AN0	10		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	A5	DQ2T	DQ1T		
7A	VREFB7AN0			PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	A4				
7A	VREFB7AN0	10		INIT_DONE	DIFFIO_RX_T14p	DIFFOUT_T14p	D6	DQ2T	DQ1T		
7A	VREFB7AN0	10		nCEO	DIFFIO_RX_T14n	DIFFOUT_T14n	E6	DQ2T	DQ1T		1
7A	VREFB7AN0	10		PR_ERROR	DIFFIO_TX_T15p	DIFFOUT_T15p	J7	DQ2T	DQ1T		1
7A	VREFB7AN0	10		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15n	K7				
7B	VREFB7BN0			_	DIFFIO_RX_T32p	DIFFOUT_T32p	K9	DQ3T	DQ2T	DQ1T	DQ4_7B_0
7B	VREFB7BN0	IO			DIFFIO_RX_T32n	DIFFOUT_T32n	K8	DQ3T	DQ2T	DQ1T	DQ4_7B_1
7B		IO					M10	DQ3T	DQ2T	DQ1T	DQ4_7B_2
7B	VREFB7BN0		VREFB7BN0				P11	Dato	10421	Dair	
7B	VREFB7BN0		VICEI BI BINO	+	DIFFIO_RX_T33p	DIFFOUT_T33p	C8	DQ3T	DQ2T	DQ1T	DQ4_7B_3
7B	VREFB7BN0				DIFFIO RX T33n	DIFFOUT T33n	D7	DOST	DQ2T	DO1T	DQ4_7B_3
70		10			DIFFIO_TX_T34p	DIFFOUT_T34p	E8	DQ3T	DQ2T	DQ1T	DQ4_7B_5
7B	VREFB7BN0				DIFFIO_TX_T34p	DIFFOUT_T34p	F7	DQ31	DQZI	DQTI	DQ4_7B_5
			 	+				DOCATIONATION - ATTOM- AT	DOCATICOATICO-ATION: AT	DOAT	DOC4 7D
7B	VREFB7BN0		 	+	DIFFIO_RX_T35p	DIFFOUT_T35p	N10	DQS3T/CQ3T/CQn3T/QKn3T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	DQS4_7B
7B	VREFB7BN0			+	DIFFIO_RX_T35n	DIFFOUT_T35n	N11	DQSn3T/QK3T	DQSn2T/QK2T	DQ1T	DQS#4_7B
/B	VREFB7BN0			1	DIFFIO_TX_T36p	DIFFOUT_T36p	G8	DQ3T	DQ2T	DQ1T	DM4_7B
/B				+	DIFFIO_TX_T36n	DIFFOUT_T36n	G7				
7B	VREFB7BN0	10			DIFFIO_RX_T37p	DIFFOUT_T37p	H8	DQ3T	DQ2T	DQ1T	DQ4_7B_6
7B	VREFB7BN0	10			DIFFIO_RX_T37n	DIFFOUT_T37n	J8	DQ3T	DQ2T	DQ1T	DQ4_7B_7
7B	VREFB7BN0			1	DIFFIO_TX_T38p	DIFFOUT_T38p	L9	DQ3T	DQ2T	DQ1T	DQ4_7B_8
7B	VREFB7BN0				DIFFIO_TX_T38n	DIFFOUT_T38n	M8			<u> </u>	
7B	VREFB7BN0				DIFFIO_RX_T39p	DIFFOUT_T39p	B6	DQ4T	DQ2T	DQ1T	DQ3_7B_0
7B	VREFB7BN0				DIFFIO_RX_T39n	DIFFOUT_T39n	C7	DQ4T	DQ2T	DQ1T	DQ3_7B_1
7B	VREFB7BN0	10			DIFFIO_TX_T40p	DIFFOUT_T40p	E9	DQ4T	DQ2T	DQ1T	DQ3_7B_2
7B	VREFB7BN0				DIFFIO_TX_T40n	DIFFOUT_T40n	F8				T
7B	VREFB7BN0				DIFFIO_RX_T41p	DIFFOUT_T41p	A7	DQ4T	DQ2T	DQ1T	DQ3_7B_3
7B	VREFB7BN0				DIFFIO_RX_T41n	DIFFOUT_T41n	A6	DQ4T	DQ2T	DQ1T	DQ3_7B_4
7B					DIFFIO TX T42p	DIFFOUT T42p	G9	DQ4T	DQ2T	DQ1T	DQ3 7B 5
7B	VREFB7BN0			1	DIFFIO_TX_T42n	DIFFOUT_T42n	H9			1-2	
7B	VREFB7BN0			1	DIFFIO_RX_T43p	DIFFOUT T43p	D8	DQS4T/CQ4T/CQn4T/QKn4T	DO2T	DQS1T/CQ1T/CQn1T/QKn1T	DQS3 7B
7B			 	+	DIFFIO_RX_T43p	DIFFOUT_T43n	D8	DOSn4T/QK4T	DQ2T	DQSn1T/QK1T	DQS3_7B DQS#3_7B
7D			 	+			D9 A8				
/ D	VREFB7BN0		 	+	DIFFIO_TX_T44p DIFFIO_TX_T44p	DIFFOUT_T44p	A8 B8	DQ4T	DQ2T	DQ1T	DM3_7B
D				+		DIFFOUT_T44n					
7B	VREFB7BN0				DIFFIO_RX_T45p	DIFFOUT_T45p	A10	DQ4T	DQ2T	DQ1T	DQ3_7B_6
'B	VREFB7BN0				DIFFIO RX T45n	DIFFOUT_T45n	B9	DQ4T	DQ2T	DQ1T	DQ3 7B 7
7B			ļ	1	DIFFIO_TX_T46p	DIFFOUT_T46p	J10	DQ4T	DQ2T	DQ1T	DQ3_7B_8
В	VREFB7BN0				DIFFIO_TX_T46n	DIFFOUT_T46n	K10			<u> </u>	
/C	VREFB7CN0	10			DIFFIO_RX_T47p	DIFFOUT_T47p	F10	DQ5T	DQ3T	DQ1T	DQ2_7C_0
/C	VREFB7CN0				DIFFIO_RX_T47n	DIFFOUT_T47n	G10	DQ5T	DQ3T	DQ1T	DQ2_7C_1
70	VREFB7CN0	10			DIFFIO_TX_T48p	DIFFOUT_T48p	J11	DQ5T	DQ3T	DQ1T	DQ2_7C_2
70							K11				



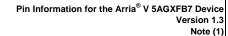
											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
70	VREFB7CN0	in			DIFFIO_RX_T49p	DIFFOUT_T49p	G11	DQ5T	DQ3T	DQ1T	DQ2_7C_3
7C	VREFB7CN0				DIFFIO RX T49n	DIFFOUT T49n	H11	DOST	DOST	DO1T	DQ2_7C_4
7C	VREFB7CN0				DIFFIO_TX_T50p	DIFFOUT_T50p	K12	DQ5T	DQ3T	DQ1T	DQ2_7C_5
7C	VREFB7CN0				DIFFIO_TX_T50n	DIFFOUT_T50n	111	5401	5401	Dair	
70	VREFB7CN0				DIFFIO_RX_T51p	DIFFOUT_T51p	E11	DQS5T/CQ5T/CQn5T/QKn5T	DQS3T/CQ3T/CQn3T/QKn3T	DQ1T	DQS2_7C
rc	VREFB7CN0				DIFFIO_RX_T51n	DIFFOUT_T51n	F11	DQSn5T/QK5T	DQSn3T/QK3T	DQ1T	DQS#2_7C
70		10			DIFFIO_TX_T52p	DIFFOUT_T52p	C10	DQ5T	DQ3T DQ3T	DQ1T	DM2_7C
70	VREFB7CN0				DIFFIO_TX_T52p	DIFFOUT_T52n	D10	DQSI	DQST	BQII	DIVIZ_7C
70	VREFB7CN0				DIFFIO_TX_T52n	DIFFOUT_T53p	G12	DOST	DQ3T	DO1T	DQ2_7C_6
70	VREFB7CN0				DIFFIO_RX_T53p	DIFFOUT_T53n	H12	DQ5T	DQ3T	DQ1T	DQ2_7C_0
70	VREFB7CN0				DIFFIO_TX_T54p	DIFFOUT_T54p	L12	DQ5T	DQ3T	DQ1T	DQ2_7C_8
70	VREFB7CN0				DIFFIO_TX_T54p	DIFFOUT_T54n	M12	DQSI	DQ31	DQTT	DQ2_7C_8
70	VREFB7CN0				DIFFIO_IX_T54fi	DIFFOUT_T55p	A11	DQ6T	DQ3T	DQ1T	DQ1_7C_0
70	VREFB7CN0				DIFFIO_RX_155p	DIFFOUT_155p	B11	DQ6T	DQ3T	DQ1T	DQ1_7C_0
70	VREFB7CN0				DIFFIO_RA_15511	DIFFOUT_155H	N13			DQ1T	
70	VREFB7CN0		VREFB7CN0				M13	DQ6T	DQ3T	DQ11	DQ1_7C_2
70			VREFB/GNU		DIFFIO DV TFO	DIFFOLIT TEO		DOST	DOOT	DOLT	DO4 70 0
<u>/C</u>	VREFB7CN0				DIFFIO_RX_T56p	DIFFOUT_T56p	C11	DQ6T	DQ3T	DQ1T	DQ1_7C_3
7C	VREFB7CN0				DIFFIO_RX_T56n	DIFFOUT_T56n	D11	DQ6T	DQ3T	DQ1T	DQ1_7C_4
7C	VREFB7CN0				DIFFIO_TX_T57p	DIFFOUT_T57p	J13	DQ6T	DQ3T	DQ1T	DQ1_7C_5
7C	VREFB7CN0				DIFFIO_TX_T57n	DIFFOUT_T57n	K13				
7C	VREFB7CN0		ļ	ļ	DIFFIO_RX_T58p	DIFFOUT_T58p	A13	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	DQ1T	DQS1_7C
7C		IO	ļ	ļ	DIFFIO_RX_T58n	DIFFOUT_T58n	B12	DQSn6T/QK6T	DQ3T	DQ1T	DQS#1_7C
7C	VREFB7CN0				DIFFIO_TX_T59p	DIFFOUT_T59p	D12	DQ6T	DQ3T	DQ1T	DM1_7C
7C	VREFB7CN0	10			DIFFIO_TX_T59n	DIFFOUT_T59n	E12				
7C	VREFB7CN0	10			DIFFIO_RX_T60p	DIFFOUT_T60p	F13	DQ6T	DQ3T	DQ1T	DQ1_7C_6
7C	VREFB7CN0	10			DIFFIO_RX_T60n	DIFFOUT_T60n	G13	DQ6T	DQ3T	DQ1T	DQ1_7C_7
7C	VREFB7CN0	IO			DIFFIO_TX_T61p	DIFFOUT_T61p	M11	DQ6T	DQ3T	DQ1T	DQ1_7C_8
7C	VREFB7CN0				DIFFIO TX T61n	DIFFOUT_T61n	N12				RESET# 7D
7D	VREFB7DN0				DIFFIO_RX_T62p	DIFFOUT_T62p	H14	DQ7T	DQ4T		CK_7D
7D	VRFFB7DN0				DIFFIO_RX_T62n	DIFFOUT T62n	J14	DOTT	DQ4T		CK# 7D
7D	VREFB7DN0	10			DIFFIO_TX_T63p	DIFFOUT_T63p	K14	DQ7T	DQ4T		CKE_7D_0
7D	VREFB7DN0				DIFFIO TX T63n	DIFFOUT T63n	114	DQTI	DQTI		CKE_7D_0
7D		10			DIFFIO_RX_T64p	DIFFOUT_T64p	F14	DQ7T	DQ4T		A_7D_0
7D	VREFB7DN0				DIFFIO_RX_T64n	DIFFOUT_T64n	G14	DQ7T	DQ4T		A_7D_1
7D	VREFB7DN0				DIFFIO_RX_164fi	DIFFOUT_164f1	M14	DO7T	DQ4T		A_7D_1 A_7D_2
70							M15	DQ/I	DQ41		
/D	VREFB7DN0				DIFFIO_TX_T65n	DIFFOUT_T65n					A_7D_3
7D	VREFB7DN0				DIFFIO_RX_T66p	DIFFOUT_T66p	G15	DQS7T/CQ7T/CQn7T/QKn7T	DQS4T/CQ4T/CQn4T/QKn4T		A_7D_4
7D	VREFB7DN0				DIFFIO_RX_T66n	DIFFOUT_T66n	H15	DQSn7T/QK7T	DQSn4T/QK4T		A_7D_5
7D	VREFB7DN0				DIFFIO_TX_T67p	DIFFOUT_T67p	C13	DQ7T	DQ4T		A_7D_6
7D	VREFB7DN0				DIFFIO_TX_T67n	DIFFOUT_T67n	D13				A_7D_7
7D	VREFB7DN0				DIFFIO_RX_T68p	DIFFOUT_T68p	D14	DQ7T	DQ4T		A 7D 8
7D	VREFB7DN0				DIFFIO_RX_T68n	DIFFOUT_T68n	E14	DQ7T	DQ4T		A_7D_9
7D	VREFB7DN0				DIFFIO_TX_T69p	DIFFOUT_T69p	K15	DQ7T	DQ4T		A_7D_10
7D	VREFB7DN0	10			DIFFIO_TX_T69n	DIFFOUT_T69n	L15				A_7D_11
7D	VREFB7DN0	10			DIFFIO_RX_T70p	DIFFOUT_T70p	B14	DQ8T	DQ4T		A_7D_12
7D		10			DIFFIO_RX_T70n	DIFFOUT_T70n	C14	DQ8T	DQ4T		A_7D_13
7D	VREFB7DN0	10					N15	DQ8T	DQ4T		A_7D_14
7D	VREFB7DN0	10	VREFB7DN0				N14				
7D	VREFB7DN0	10			DIFFIO_RX_T71p	DIFFOUT_T71p	A14	DQ8T	DQ4T		BA_7D_0
7D	VREFB7DN0	10			DIFFIO_RX_T71n	DIFFOUT_T71n	B15	DQ8T	DQ4T		BA_7D_1
7D	VREFB7DN0	10			DIFFIO_TX_T72p	DIFFOUT_T72p	D15	DQ8T	DQ4T		BA_7D_2
7D	VREFB7DN0	10			DIFFIO_TX_T72n	DIFFOUT_T72n	E15				RAS#_7D
7D	VREFB7DN0	10			DIFFIO_RX_T73p	DIFFOUT_T73p	F16	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T		CAS#_7D
7D	VREFB7DN0				DIFFIO RX T73n	DIFFOUT_T73n	G16	DQSn8T/QK8T	DQ4T	1	WE#_7D
7D	VREFB7DN0				DIFFIO_TX_T74p	DIFFOUT_T74p	J16	DQ8T	DQ4T		ODT_7D_0
7D	VREFB7DN0				DIFFIO_TX_T74n	DIFFOUT_T74n	K16	ĺ		1	ODT_7D_1
7D	VREFB7DN0	10			DIFFIO_RX_T75p	DIFFOUT_T75p	C16	DQ8T	DQ4T	İ	A 7D_15
7D	VREFB7DN0	10		Ì	DIFFIO RX T75n	DIFFOUT T75n	D16	DOST	DQ4T	1	
7D	VREFB7DN0				DIFFIO_TX_T76p	DIFFOUT_T76p	M16	DQ8T	DQ4T	1	CS#_7D_0
7D	VREFB7DN0			1	DIFFIO_TX_T76n	DIFFOUT_T76n	N16	<u> </u>		1	CS#_7D_1
	THE DIDING	VCCA FPLL			D 10_17_17011	5 001_17011	R17			1	
		VCCD_FPLL	 		1	+	R16	†		†	-
	1	DNU DNU	 	1	1	+	I 18	1	†	†	-
on .			CLK10n	 	DIEEIO DY TOS-	DIFFOUT_T85p		DOOT	DOST	1	-
BD BD	VREFB8DN0		CLK19p CLK19n	1	DIFFIO_RX_T85p		A16	DQ9T	DQ5T	1	-
שט	VREFB8DN0		CEN 1911	1	DIFFIO_RX_T85n	DIFFOUT_T85n	A17	DQ9T	DQ5T	+	
SU	TITEL BODITO	10			DIFFIO_TX_T86p	DIFFOUT_T86p	K17	DQ9T	DQ5T	ļ	
3D	VREFB8DN0		0.1112	ļ	DIFFIO_TX_T86n	DIFFOUT_T86n	L17			+	-
3D	VREFB8DN0		CLK18p	ļ	DIFFIO_RX_T87p	DIFFOUT_T87p	K18	DQ9T	DQ5T	ļ	
3D		10	CLK18n		DIFFIO_RX_T87n	DIFFOUT_T87n	K19	DQ9T	DQ5T		
BD.	VREFB8DN0		ļ	ļ	DIFFIO_TX_T88p	DIFFOUT_T88p	D17	DQ9T	DQ5T	Į.	
3D		IO			DIFFIO_TX_T88n	DIFFOUT_T88n	E17	1		1	
3D	VREFB8DN0		FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T89p	DIFFOUT_T89p	F17	DQS9T/CQ9T/CQn9T/QKn9T	DQS5T/CQ5T/CQn5T/QKn5T		
3D		Ю	FPLL_TC_CLKOUT3,FPLL_TC_FBn		DIFFIO_RX_T89n	DIFFOUT_T89n	G17	DQSn9T/QK9T	DQSn5T/QK5T	ļ	
BD	VREFB8DN0	10	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T90p	DIFFOUT_T90p	M17	DQ9T	DQ5T		
3D	VREFB8DN0	10	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn	1 -	DIFFIO_TX_T90n	DIFFOUT_T90n	N17	1			
3D	VREFB8DN0	10	CLK17p		DIFFIO_RX_T91p	DIFFOUT_T91p	H17	DQ9T	DQ5T		
8D	VREFB8DN0	10	CLK17n		DIFFIO_RX_T91n	DIFFOUT_T91n	J17	DQ9T	DQ5T		
					DIFFIG. TV. TOO	DIFFOUT_T92p	B17	DQ9T	DQ5T		
BD	VREFB8DN0	10			DIFFIO_TX_T92p	DIFFOUT_192p					



											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
8D	VREFB8DN0	10	CLK16p		DIFFIO_RX_T93p	DIFFOUT_T93p	A19	DQ10T	DQ5T	1	PHY (3)
8D	VREFB8DN0		CLK16p		DIFFIO_RX_193p	DIFFOUT_193p DIFFOUT_T93n	A19 A20	DQ10T	DQ5T DQ5T	1	+
8D	VREFB8DN0		CERTOII		DIFFIO_KA_193II	DIFFOUT_19311	M18	DQ10T	DQ5T	†	
8D	VREFB8DN0	10	VREFB8DN0				N18				
8D	VREFB8DN0	IO			DIFFIO_RX_T94p	DIFFOUT_T94p	C19	DQ10T	DQ5T		
8D	VREFB8DN0	10			DIFFIO_RX_T94n	DIFFOUT_T94n	B18	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T95p	DIFFOUT_T95p	G18	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T95n	DIFFOUT_T95n	G19				
8D	VREFB8DN0	10			DIFFIO_RX_T96p	DIFFOUT_T96p	H18	DQS10T/CQ10T/CQn10T/QKn10T	DQ5T		
8D	VREFB8DN0	10			DIFFIO_RX_T96n	DIFFOUT_T96n	J19	DQSn10T/QK10T	DQ5T		
8D	VREFB8DN0	10			DIFFIO_TX_T97p	DIFFOUT_T97p	M19	DQ10T	DQ5T		
8D	VREFB8DN0	IO			DIFFIO_TX_T97n	DIFFOUT_T97n	N19				
	VREFB8DN0	10			DIFFIO_RX_T98p	DIFFOUT_T98p	D19	DQ10T	DQ5T		
8D	VREFB8DN0	10			DIFFIO_RX_T98n	DIFFOUT_T98n	D18	DQ10T	DQ5T	!	
8D 8D	VREFB8DN0 VREFB8DN0				DIFFIO_TX_T99p DIFFIO_TX_T99p	DIFFOUT_T99p DIFFOUT_T99n	E18	DQ10T	DQ5T		+
8C	VREFB8CN0	10			DIFFIO_TX_T99II	DIFFOUT_T116p	K20	DQ11T	DQ6T	DQ2T	DQ4_8C_0
8C	VREFB8CN0	in			DIFFIO_RX_T116n	DIFFOUT_T116n	L20	DQ11T	DQ6T	DQ2T	DQ4_8C_1
8C	VREFB8CN0	10			DII 110_IOX_1110II	DII I GOI_II I I II	M20	DQ11T	DQ6T	DQ2T	DQ4_8C_2
8C	VREFB8CN0	10	VREFB8CN0				N20				
8C	VREFB8CN0	10			DIFFIO_RX_T117p	DIFFOUT_T117p	A22	DQ11T	DQ6T	DQ2T	DQ4 8C 3
8C	VREFB8CN0	10			DIFFIO_RX_T117n	DIFFOUT_T117n	B21	DQ11T	DQ6T	DQ2T	DQ4_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T118p	DIFFOUT_T118p	B20	DQ11T	DQ6T	DQ2T	DQ4_8C_5
8C	VREFB8CN0	10			DIFFIO_TX_T118n	DIFFOUT_T118n	C20				
8C	VREFB8CN0	10			DIFFIO_RX_T119p	DIFFOUT_T119p	D20	DQS11T/CQ11T/CQn11T/QKn11T	DQS6T/CQ6T/CQn6T/QKn6T	DQ2T	DQS4_8C
8C	VREFB8CN0	10			DIFFIO_RX_T119n	DIFFOUT_T119n	E20	DQSn11T/QK11T	DQSn6T/QK6T	DQ2T	DQS#4_8C
8C	VREFB8CN0	Ю			DIFFIO_TX_T120p	DIFFOUT_T120p	K21	DQ11T	DQ6T	DQ2T	DM4_8C
8C	VREFB8CN0	10			DIFFIO_TX_T120n	DIFFOUT_T120n	L21				
8C	VREFB8CN0	10			DIFFIO_RX_T121p	DIFFOUT_T121p	F20	DQ11T	DQ6T	DQ2T	DQ4_8C_6
8C	TITEL BOOKS	10			DIFFIO_RX_T121n	DIFFOUT_T121n	G20	DQ11T	DQ6T	DQ2T	DQ4_8C_7
8C	VREFB8CN0 VREFB8CN0	10			DIFFIO_TX_T122p DIFFIO_TX_T122n	DIFFOUT_T122p DIFFOUT_T122n	H20 J20	DQ11T	DQ6T	DQ2T	DQ4_8C_8
8C	VREFB8CN0	10			DIFFIO_TX_T122II	DIFFOUT_T123p	D21	DQ12T	DQ6T	DQ2T	DQ3_8C_0
8C	VREFB8CN0	io			DIFFIO_RX_T123p	DIFFOUT_T123p	E21	DQ12T	DQ6T	DQ2T	DQ3_8C_1
8C	VREFB8CN0	10			DIFFIO TX T124n	DIFFOUT T124n	M21	DQ12T	DOST	DQ2T	DQ3_8C_2
8C	VREFB8CN0	10			DIFFIO_TX_T124n	DIFFOUT_T124n	N21				
	VREFB8CN0	10			DIFFIO_RX_T125p	DIFFOUT_T125p	C22	DQ12T	DQ6T	DQ2T	DQ3 8C 3
8C	VREFB8CN0	10			DIFFIO_RX_T125n	DIFFOUT_T125n	D22	DQ12T	DQ6T	DQ2T	DQ3_8C_4
8C	VREFB8CN0	IO			DIFFIO_TX_T126p	DIFFOUT_T126p	G21	DQ12T	DQ6T	DQ2T	DQ3_8C_5
8C	VREFB8CN0	10			DIFFIO_TX_T126n	DIFFOUT_T126n	H21				
8C	VREFB8CN0	10			DIFFIO_RX_T127p	DIFFOUT_T127p	F22	DQS12T/CQ12T/CQn12T/QKn12T	DQ6T	DQS2T/CQ2T/CQn2T/QKn2T	DQS3_8C
8C	VREFB8CN0	Ю			DIFFIO_RX_T127n	DIFFOUT_T127n	G22	DQSn12T/QK12T	DQ6T	DQSn2T/QK2T	DQS#3_8C
8C	VREFB8CN0	10			DIFFIO_TX_T128p	DIFFOUT_T128p	M22	DQ12T	DQ6T	DQ2T	DM3_8C
8C	VREFB8CN0	10			DIFFIO_TX_T128n	DIFFOUT_T128n	N22	DOLOT	DOST	DOOT	200 00 0
8C	VREFB8CN0	10			DIFFIO_RX_T129p	DIFFOUT_T129p	A23	DQ12T	DQ6T	DQ2T DQ2T	DQ3_8C_6
8C 8C	VREFB8CN0 VREFB8CN0	10			DIFFIO_RX_T129n	DIFFOUT_T129n	B23	DQ12T	DQ6T		DQ3_8C_7
		10			DIFFIO TV T420-			DOMOT			DO2 0C 0
		Ю			DIFFIO_TX_T130p	DIFFOUT_T130p	J22	DQ12T	DQ6T	DQ2T	DQ3_8C_8
8C 8B	VREFB8CN0	IO IO			DIFFIO_TX_T130n	DIFFOUT_T130n	K22			DQ2T	
8B	VREFB8CN0 VREFB8BN0	Ю			DIFFIO_TX_T130n DIFFIO_RX_T131p	DIFFOUT_T130n DIFFOUT_T131p	K22 H23	DQ13T	DQ7T	DQ2T DQ2T	DQ2_8B_0
8B 8B	VREFB8CN0	10 10 10 10			DIFFIO_TX_T130n	DIFFOUT_T130n	K22			DQ2T	
8B 8B 8B	VREFB8CN0 VREFB8BN0 VREFB8BN0 VREFB8BN0	10 10 10 10			DIFFIO_TX_T130n DIFFIO_RX_T131p DIFFIO_RX_T131n DIFFIO_TX_T132p	DIFFOUT_T130n DIFFOUT_T131p DIFFOUT_T131n DIFFOUT_T132p	K22 H23 J23 K24	DQ13T DQ13T	DQ7T DQ7T	DQ2T DQ2T DQ2T	DQ2_8B_0 DQ2_8B_1
8B 8B 8B	VREFB8CN0 VREFB8BN0 VREFB8BN0	O			DIFFIO_TX_T130n DIFFIO_RX_T131p DIFFIO_RX_T131n	DIFFOUT_T130n DIFFOUT_T131p DIFFOUT_T131n	K22 H23 J23	DQ13T DQ13T	DQ7T DQ7T	DQ2T DQ2T DQ2T	DQ2_8B_0 DQ2_8B_1
8B 8B 8B 8B 8B 8B	VREFB8CN0 VREFB8BN0 VREFB8BN0 VREFB8BN0 VREFB8BN0 VREFB8BN0 VREFB8BN0 VREFB8BN0	O			DIFFIO_TX_T130n DIFFIO_RX_T131p DIFFIO_RX_T131n DIFFIO_TX_T132p DIFFIO_TX_T132n DIFFIO_RX_T133p DIFFIO_RX_T133p	DIFFOUT_T130n DIFFOUT_T131p DIFFOUT_T131n DIFFOUT_T132p DIFFOUT_T132p DIFFOUT_T132n DIFFOUT_T133p DIFFOUT_T133p	K22 H23 J23 K24 L24 B24 C23	DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T	DQ7T DQ7T DQ7T DQ7T	DQ2T DQ2T DQ2T DQ2T DQ2T DQ2T DQ2T	DQ2 8B 0 DQ2 8B 1 DQ2 8B 2 DQ2 8B 3 DQ2 8B 4
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8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8	VREFBBNO VREFBBNO	O	VREFB8BNO		DIFFIO TX T130n DIFFIO TX T131p DIFFIO RX T131p DIFFIO RX T131n DIFFIO TX T132n DIFFIO TX T132n DIFFIO TX T132n DIFFIO TX T132n DIFFIO RX T133n DIFFIO TX T133n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T140p DIFFIO TX T140p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n	DIFFOUT_T130n DIFFOUT_T131p DIFFOUT_T131p DIFFOUT_T131p DIFFOUT_T132p DIFFOUT_T132p DIFFOUT_T132p DIFFOUT_T132p DIFFOUT_T133n DIFFOUT_T133n DIFFOUT_T134p DIFFOUT_T134p DIFFOUT_T134p DIFFOUT_T135p DIFFOUT_T145p DIFFOUT_T140p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T143p	K22 H23 J23 K24 L24 B24 C23 D23 E23 D23 C23 C23 C23 C23 M23 C24 H24 K23 L23 C24 K23 C25 C25 C25 C25 C25 C25 C25 C25 C25 C25	DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ14T	DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T	DO2T	D02 8B 0 D02 8B 1 D02 8B 2 D02 8B 3 D02 8B 4 D02 8B 5 D032 8B 4 D02 8B 5 D032 8B D0382 8B D0382 8B D0382 8B D0382 8B D01 8B 6 D02 8B 6 D01 8B 1 D01 8B 2 D01 8B 3 D01 8B 4 D01 8B 3 D01 8B 4 D01 8B 3 D01 8B 4 D01 8B 3 D01 8B 4 D01 8B 5
8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8	VREFBBNO VREFBBNO	O	VREFB8BN0		DIFFIO TX T130n DIFFIO TX T131n DIFFIO RX T131n DIFFIO RX T131n DIFFIO TX T132n DIFFIO TX T132n DIFFIO TX T132n DIFFIO TX T132n DIFFIO RX T133n DIFFIO TX T132n DIFFIO TX T133n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T140p DIFFIO TX T1440p	DIFFOUT, T130n DIFFOUT, T131p DIFFOUT, T131p DIFFOUT, T131p DIFFOUT, T132p DIFFOUT, T132p DIFFOUT, T132p DIFFOUT, T132p DIFFOUT, T133p DIFFOUT, T133p DIFFOUT, T133p DIFFOUT, T134p DIFFOUT, T135p DIFFOUT, T135p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T136p DIFFOUT, T141p DIFFOUT, T141p DIFFOUT, T141p DIFFOUT, T144p	K22 H23 J23 J23 K24 L24 B24 C23 D23 F23 F23 F23 F23 F23 F23 F	D013T D014T D014T	DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T	DO2T	D02.8B 0 D02.8B 1 D02.8B 2 D02.8B 3 D02.8B 3 D02.8B 4 D02.8B 5 D02.8B 4 D02.8B 5 D03.8B 6 D03.8B 6 D04.8B 6 D04.8B 6 D04.8B 1 D01.8B 0 D01.8B 3 D01.8B 3 D01.8B 5 D01.8B 5 D01.8B 5 D01.8B 6 D01.8B 6 D01.8B 6 D01.8B 6 D01.8B 6 D01.8B 6
8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8B 8	VREFBBNO VREFBBNO	O	VREFBSBNO		DIFFIO TX T130n DIFFIO TX T131p DIFFIO RX T131p DIFFIO RX T131n DIFFIO TX T132n DIFFIO TX T132n DIFFIO TX T132n DIFFIO TX T132n DIFFIO RX T133n DIFFIO TX T133n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T134n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T135n DIFFIO TX T140p DIFFIO TX T140p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T141p DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n DIFFIO TX T142n	DIFFOUT_T130n DIFFOUT_T131p DIFFOUT_T131p DIFFOUT_T131p DIFFOUT_T132p DIFFOUT_T132p DIFFOUT_T132p DIFFOUT_T132p DIFFOUT_T133n DIFFOUT_T133n DIFFOUT_T134p DIFFOUT_T134p DIFFOUT_T134p DIFFOUT_T135p DIFFOUT_T145p DIFFOUT_T140p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T141p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T142p DIFFOUT_T143p	K22 H23 J23 K24 L24 B24 C23 D23 E23 D23 C23 C23 C23 C23 M23 C24 H24 K23 L23 C24 K23 C25 C25 C25 C25 C25 C25 C25 C25 C25 C25	DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ13T DQ31T DQ31T DQ13T DQ13T DQ13T DQ14T	DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T DQ7T	DO2T	D02 8B 0 D02 8B 1 D02 8B 2 D02 8B 3 D02 8B 4 D02 8B 5 D032 8B 4 D02 8B 5 D032 8B D0382 8B D0382 8B D0382 8B D0382 8B D01 8B 6 D02 8B 6 D01 8B 1 D01 8B 2 D01 8B 3 D01 8B 4 D01 8B 3 D01 8B 4 D01 8B 3 D01 8B 4 D01 8B 3 D01 8B 4 D01 8B 5

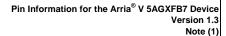


DDR3/DDR2 VREF PinName/Function (2) ptional Function(s) Configuration Dedicated Tx/Rx Emulated LVDS F1152 DOS for X8/X9 DOS for X16/ X18 DOS for X32/ X36 Number Function Channel Output Channel hard memory PHY (3) DIFFIO_TX_T145n DIFFOUT_T145n VREFB8BN0 K25 RESET# 8A DIFFIO_RX_T146p DIFFOUT_T146p DQ15T DQ8T CK_8A VREFB8AN0 E26 DIFFIO_RX_T146n DIFFOUT_T146n CK#_8A VREFB8AN0 DQ8T VREFB8AN0 IC DIFFIO_TX_T147p DIFFOUT_T147p K29 DQ15T DQ8T CKE_8A_0 VREFB8AN0 IO DIFFIO_TX_T147n DIFFOUT_T147n L29 CKE_8A_1 VREFB8AN0 IC DIFFIO_RX_T148p DIFFOUT_T148p DQ15T A 8A 0 DQ8T VREFB8AN0 DIFFIO_RX_T148n DIFFOUT_T148n DQ15T T8QC A_8A_1 VREFB8AN0 DIFFIO_TX_T149p DIFFOUT_T149p A_8A_2 DQ15T T8QC VREFB8AN0 I DIFFIO TX T149n DIFFOUT T149n A 8A 3 VREFB8AN0 IO DIFFIO_RX_T150p DIFFOUT_T150p DQS15T/CQ15T/CQn15T/QKn15T DQS8T/CQ8T/CQn8T/QKn8T A_8A_4 8A VREFB8AN0 DIFFIO_RX_T150n DIFFOUT_T150n H26 DQSn15T/QK15T DQSn8T/QK8T A_8A_5 VREFB8AN0 DIFFIO TX T151p DIFFOUT T151p DQ15T A 8A 6 DIFFIO_TX_T151n DIFFOUT_T151n A 8A 7 VREFB8AN0 DIFFIO_RX_T152p DIFFOUT_T152p DQ8T 8 A8 A VREFB8AN0 DIFFIO_RX_T152n DIFFOUT_T152n DQ8T A 8A 9 VREFR8ANO DIFFIO TX T153p DIFFOUT T153p DQ15T DOST A 8A 10 84 VREERSAND IC DIFFIO TX T153n DIFFOUT T153n D28 A 8A 11 VREERSAND IC DIFFIO RX T154p DIFFOUT T154p DO16T DOST A 8A 12 VRFFB8AN0 DIFFIO_RX_T154n DIFFOUT_T154n DQ16T DQ8T A 8A 13 VRFFB8AN0 DIFFIO_TX_T155p DIFFOUT_T155p DQ16T DOST A 8A 14 DIFFIO_TX_T155n DIFFOUT_T155n A 8A 15 VRFFB8AN0 BA 8A 0 VRFFB8AN0 DIFFIO RX T156p DIFFOUT T156p A29 DOST VREFB8AN0 IC DIFFIO RX T156n DIFFOUT T156n A28 DQ16T DQ8T BA 8A 1 DIFFIO TX T157p DIFFOUT T157p DQ16T BA 8A 2 VREFB8AN0 IC B29 DQ8T VREFB8AN0 DIFFIO TX T157n DIFFOUT T157n RAS# 8A DQS16T/CQ16T/CQn16T/QKn16T F28 DOST CAS# 8A VRFFB8AN0 DIFFIO RX T158p DIFFOUT T158p DIFFIO_RX_T158n DIFFOUT_T158n DOSn16T/QK16T WF# 8A VRFFB8AN0 F29 T8OC VRFFB8AN0 DIFFIO_TX_T159p DIFFOUT_T159p H27 DQ16T DO8T ODT 8A 0 DIFFIO_TX_T159n DIFFOUT_T159n ODT 8A 1 VREFB8AN0 IC VREFB8AN0 IO CLK23p DIFFIO_RX_T160p DIFFOUT_T160p D29 DQ16T DQ8T VREFB8AN0 IO DIFFIO_RX_T160n DIFFOUT_T160n DQ16T DQ8T CLK23n E29 VREFB8AN0 IO DIFFIO_TX_T161p DIFFOUT_T161p D30 DQ16T DQ8T CS#_8A_0 VREFB8AN0 CS#_8A_1 VREFB8AN0 LK22p VREFB8AN0 VREFB8AN0 DQ17T VREFB8AN0 REFB8AN0 VREFB8AN0 FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1 DIFFIO_RX_T163p DIFFOUT_T163p VREFB8AN0 FPLL_TL_CLKOUT3,FPLL_TL_FBn DIFFIO_RX_T163n DIFFOUT_T163n DQ17T VREFB8AN0 FPLL_TL_CLKOUT0,FPLL_TL_CLKOUTp,FPLL_TL_FB0 DIFFIO_TX_T164p DIFFOUT_T164p VREFB8AN0 FPLL TL CLKOUT1,FPLL TL CLKOUTn DIFFIO TX T164n DIFFOUT T164n 8A VREFRRAND IO CLK21p DIFFIO_RX_T165p DIFFOUT_T165p A32 DQS17T/CQ17T/CQn17T/QKn17T VREFRRAND IO CI K21n DIFFIO RX T165n DIFFOLIT T165n B32 DOSn17T/OK17T 84 VREFRRAND IO DIFFIO_TX_T166p DIFFOUT_T166p .128 DO17T VRFFB8AN0 DIFFIO_TX_T166n DIFFOUT_T166n VRFFB8AN0 LK20p VRFFB8AN0 LK20n DQ17T DQ17T VREFB8AN0 VREERSAND IC R70 6 DIFFIO TX T168n DIFFOLIT T168n F32 MSFI 0 MSEL 0 D34 MSFI 1 MSFI 1 H30 MSFL2 MSFL2 K30 MSFL3 MSFL3 M29 MSFL4 MSFL4 M30 CONF_DONE CONF_DONE C34 nSTATUS nSTATUS B34 nCE A33 nCE B33 GND AA26 AA33 GND AA34 GND AB27 AB28 GND AB29 GND AB30 AR31 GND AB32 GND AC30 GND AC34 GND AD31 CNID AD32 GND AF30 GND AF33 GND AF34 GND AF31 GND AF32 AG30





											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		GND					AG33				1111 137
		GND					AG34				
		GND					AH31				
		GND GND		-			AH32 AJ30				
		GND					AJ33				+
		GND					AJ34				1
		GND					AK31				
		GND GND					AK32				1
		GND					AL33 AL34				
		GND GND					AL34 E34				+
		GND					F31				1
		GND					F32				
		GND					G30				
		GND					G33				
		GND					G34 H31				+
		GND GND		-		-	H32				+
		GND					J30				+
		GND					J33				
		GND					J34				
	-	GND		1	1	1	K31 K32	+			+
	 	GND GND					K32 L30				+
		GND		—		—	L30	<u> </u>			+
		GND		İ	İ	İ	L34		İ		1
		GND					M31				
		GND					M32				1
		GND					N28				
		GND GND					N29 N33				+
		GND					N34				+
		GND					P27				+
		GND					P31				1
		GND					P32				
		GND					R28				
		GND GND					R30 R33				+
		GND					R34				+
		GND GND					T27				+
		GND					T29				
		GND					T31				ļ
		GND GND					T32 U28				+
		GND		-		-	U33				+
		GND					U34				1
		GND					V27				1
		GND					V31				
		GND					V32				
		GND GND		-			W28 W30				
		GND					W33				+
		GND		<u> </u>		<u> </u>	W34	<u> </u>			
		GND GND					W34 Y27				
		GND					Y29				
	1	GND GND		 	 	 	Y31 Y32	+	 	 	+
		GND		 	1	 	Y32 AA1	<u> </u>			+
		GND		 	1	 	AA2	 			+
		GND					AA9				1
		GND					AB3				
		GND GND				<u> </u>	AB4				4
	-	GND GND		_		_	AB5 AB7				+
		GND		 		 	AB7 AB8	1			+
		GND		—		—	AC1	<u> </u>			+
		GND					AC2				1
		GND					AC5				
		GND					AD3	 			4
		GND GND				_	AD4 AE1				+
		GND		 		 	AE1 AE2	1			+
		GND		1		1	AE5				1
		GND					AF3				1
		GND					AF4				
		GND					AG1	 			4
	 	GND GND				_	AG2 AG5				+
	l	UNU	1	1	l	1	AGO	I .	l .	l .	



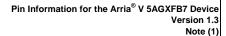


											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		GND					AH3				FH1 (3)
		GND				1	AH4				1
		GND					AJ1				1
		GND					AJ2				
		GND				ļ	AJ5				
		GND GND					AK3 AK4	 			+
		GND		-			AL1	 			+
		GND				†	AL2				†
		GND GND				1	AL2 AL3				1
		GND					AN1				
		GND					F3				
		GND					F4				
		GND				ļ	G1 G2				
		GND GND					G2 G5				+
		GND					H3	+			+
		GND				†	H4				†
		GND					J1				1
		GND					J2				
		GND					J5				
		GND					K3	 			4
		GND		1	1	 	K4 L1	 	ļ		+
		GND GND		-			L1 L2	 	 		+
		GND		t			L2 L5	 	 		+
	1	GND		†	1	1	M3	†			1
		GND		İ	İ		M4	1	İ		1
		GND					M5				1
		GND					N1				
		GND					N2				
		GND				ļ	N6				4
		GND GND		-			P3 P4	 			4
		GND					P8	 			+
		GND					R1				+
		GND					R2				+
		GND				1	R5				1
		GND					R7				
		GND					T3				
		GND					T4				
		GND					T6				4
		GND GND					T8 U1				+
		GND		-		-	U2	 			+
		GND					U7	1			+
		GND				†	V3				1
		GND					V4				
		GND					V8				
		GND					W1				
		GND		 	-		W2	 			+
	1	GND GND		 	1		W5 W7	+	 		+
	 	GND		 	 	 	W7 Y3	 	 		+
	i	GND GND		İ			Y4	1			1
		GND					Y6				1
		GND					Y8				
		VCCP					P18				4
		VCCP				ļ	R13				
		VCCP		1	1		R21	 	ļ		+
		VCCP		-			T10	 	 		+
	1	VCCP		 	1	+	U25 V10	+	1		+
		VCCP VCCP		t			W25	 	 		+
	i	VCCP		İ			Y12	1			1
		VCCP					Y19				
		VCCP					Y22				
		VCCA_FPLL			ļ		V26				1
		VCCA_FPLL			ļ	ļ	V9	 	ļ		4
		VCCA FPLL					T26	 			+
	-	VCCA_FPLL VCCBAT		 			T9 M28	 	 		+
		VCC_AUX		 	 		P12	 	 		+
		VCC_AUX		1			P24	1			1
		VCC AUX					W11				1
		VCC_AUX					Y24				
		VCCD_FPLL					Y26				
		VCCD_FPLL VCCD_FPLL					Y9 P26				



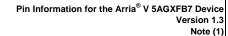


DDR3/DDR2 F1152 DQS for X8/X9 Optional Function(s) Dedicated Tx/Rx DQS for X16/ X18 PinName/Function (2) Configuration Emulated LVDS DQS for X32/ X36 Function Output Channel hard memory PHY (3) VCCD_FPLL VCCA_GXBL0 VCCA_GXBR0 Y28 VCCA_GXBL1 T28 VCCA_GXBR1 T7 VCCH GXBL0 V28 VCCH_GXBR0 VCCH_GXBL1 VCCH_GXBR1 VCCL_GXBL0 VCCL_GXBL0 V30 VCCL_GXBR0 VCCL_GXBR0 P29 VCCL_GXBL1 P30 P5 VCCL GXBR1 VCCL GXBR1 P6 VCCR GXBL AA29 VCCR GXBL
VCCR GXBL
VCCR GXBL
VCCR GXBL AA30 N30 U29 U30 VCCR GXBR AA5 VCCR GXBR AA6 VCCR GXBR N5 U5 VCCR_GXBR VCCR_GXBR VCCT_GXBL0 VCCT_GXBL0 W29 Y30 VCCT_GXBR0 W6 VCCT_GXBR0 VCCT_GXBL1 R29 VCCT_GXBL1 VCCT_GXBR1 VCCT_GXBR1 R14 R23 VCC T14 VCC T16 VCC T18 VCC T24 U11 1112 VCC VCC U13 U15 VCC VCC VCC U19 1120 VCC U21 VCC U22 U23 VCC V14 W13 VCC W19 VCC W21 VCC W23 V18 VCCIO3A AD30 VCCIO3A AF27 VCCIO3A AH30 VCCIO3A AJ27 VCCIO3A VCCIO3B AK30 AM27 AF24





Bank Number	PinName/Function (2) VCCIO3B VCCIO3B VCCIO3B VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C VCCIO4C VCCIO4C VCCIO4C	Optional Function(s)		Dedicated Tx/Rx Channel	Output Channel	F1152 AJ24 AM24 AP24 AF21 AJ21 AM21 AP21 AF18 AJ18 AM18 AP18 AD5 AF5	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
	VCCIO3B VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C					AM24 AP24 AF21 AJ21 AM21 AP21 AF18 AJ18 AM18 AP18 AD5				FIII (3)
	VCCIO3B VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C					AM24 AP24 AF21 AJ21 AM21 AP21 AF18 AJ18 AM18 AP18 AD5				
	VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3C VCCIO3D VCCIO3D VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C VCCIO4C VCCIO4C					AF21 AJ21 AM21 AP21 AF18 AJ18 AM18 AP18 AD5				
	VCCIO3C VCCIO3C VCCIO3C VCCIO3D VCCIO3B VCCIO3B VCCIO3B VCCIO3B VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C					AJ21 AM21 AP21 AF18 AJ18 AM18 AP18 AD5				
	VCCIO3C VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C					AM21 AP21 AF18 AJ18 AM18 AP18 AD5				
	VCCIO3C VCCIO3D VCCIO3D VCCIO3D VCCIO3B VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C					AP21 AF18 AJ18 AM18 AP18 AD5				
	VCCIO3D VCCIO3D VCCIO3D VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C					AF18 AJ18 AM18 AP18 AD5				
	VCCIO3D VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C VCCIO4C VCCIO4C					AJ18 AM18 AP18 AD5				
	VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C					AM18 AP18 AD5				
	VCCIO3D VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C					AP18 AD5				
	VCCIO4A VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C					AD5				
	VCCIO4A VCCIO4A VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C VCCIO4C					AF5				
	VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C						<u> </u>			T
	VCCIO4A VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C					AH5				+
	VCCIO4B VCCIO4B VCCIO4B VCCIO4C VCCIO4C VCCIO4C					AK5				1
	VCCIO4B VCCIO4B VCCIO4C VCCIO4C					AF9				1
	VCCIO4B VCCIO4B VCCIO4C VCCIO4C					AJ9				1
	VCCIO4B VCCIO4C VCCIO4C					AM9				1
	VCCIO4C VCCIO4C					AP9				
	VCCIO4C					AF12				
	VCCIOAC					AJ12				
						AM12				4
	VCCIO4C		ļ	-	 	AP12 AF15				+
	VCCIO4D VCCIO4D					AF15 AJ15				+
		 	1	1	1	AJ15 AM15				+
 	VCCIO4D VCCIO4D		 	 	 	AP15	 			+
-	VCCIO7A	<u> </u>				C5	 			+
	VCCIO7A					F2				+
	VCCIO7A					F5				1
	VCCIO7A					L7				1
	VCCIO7B					A9				1
	VCCIO7B					C9				1
	VCCIO7B					F9				
	VCCIO7B					J9				
	VCCIO7C					A12				
	VCCIO7C					C12				
	VCCIO7C					F12				
	VCCIO7C VCCIO7D					J12 A15				+
	VCCIO7D VCCIO7D					C15				+
	VCCIO7D VCCIO7D					F15				+
	VCCIO7D					J15				+
	VCCIO8A					C27				+
	VCCIOBA					C30				+
	VCCIO8A					F27				1
	VCCIO8A					F30				1
	VCCIO8A					J29				1
	VCCIO8A					M26				
	VCCIO8B					A24				
L	VCCIO8B					C24	ļ			4
	VCCIO8B					F24				4
	VCCIO8B					J24 A21				+
-	VCCIO8C VCCIO8C	 	1	1	1	A21 C21				+
-	VCCIO8C	<u> </u>				F21	 			+
	VCCIOSC VCCIOSC		1	1	1	J21				†
	VCCIO8C VCCIO8D					A18				1
	VCCIO8D					C18				1
	VCCIO8D					F18				
	VCCIO8D					J18				
	VCCPD3					AB26				
	VCCPD3		ļ	ļ	ļ	AC27				1
	VCCPD3					Y21				
	VCCPD3					Y25				
	VCCPD4A		ļ	-	 	AB6 AB9				+
-	VCCPD4A	 					 			+
-	VCCPD4BCD VCCPD4BCD	 				Y10 Y14	 			+
-	VCCPD4BCD VCCPD4BCD	 	1	1		Y14 Y16				+
-	VCCPD4BCD VCCPD7A	 				N8	†			+
	VCCPD7A		1	1		N9				†
	VCCPD7BCD					P14				1
	VCCPD7BCD					P16				1
	VCCPD7BCD					R11				1
	VCCPD8					N26				1
	VCCPD8					N27				
	VCCPD8					P20			<u> </u>	
	VCCPD8	<u> </u>				P22			<u> </u>	





											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		VCCPGM					M9				(0)
		VCCPGM					AC26				
		GND					AA11				<u> </u>
		GND					AA13				
		GND GND					AA16 AA19				+
		GND					AA19 AA22				1
		GND					AA24				
		GND					AD10				İ
		GND GND					AD10 AD13				
		GND					AD16				
		GND					AD19				<u> </u>
		GND					AD22				
		GND GND				-	AD25 AD28				<u> </u>
		GND					AD28 AD7				+
		GND					AG10				†
		GND					AG13				
		GND					AG16				
		GND					AG19				
		GND					AG22				
		GND					AG25				
		GND					AG28			1	
		GND		1	-	1	AG7	-	ļ	 	
		GND GND				 	AK10 AK13			1	+
		GND		 	-	† 	AK13 AK16	1	 	1	+
		GND					AK19				†
		GND					AK22				
		GND					AK25				
		GND					AK28				
		GND					AK7				
		GND					AN10				ļ
		GND					AN13				ļ
		GND				-	AN16				<u> </u>
		GND GND					AN19 AN22				
		GND					AN25			1	-
		GND					AN28				
		GND					AN31				
		GND					AN4	İ			1
		GND					AN7				
		GND					B1				
		GND					B10				
		GND					B13				
		GND GND				-	B16 B19				<u> </u>
		GND					B19 B22				
		GND					B25				
		GND					B28				
		GND					B31				
		GND					B4				
		GND					B7				
		GND GND					D2				
		GND		ļ	ļ		D4		ļ	1	
		GND				 	E10				
		GND GND	 	1	 	 	E13 E16		 	1	+
		GND					E19				
		GND					E22				t
		GND					E25			İ	
		GND					E28	_			
		CND					E31				
		GND					E7				ļ
		GND				L	H10			1	
		GND				 	H13				
		GND	 		-	 	H16 H19	1	 	1	
		GND GND				 	H19 H22			1	+
		GND				 	H25	1	 	1	+
		GND				 	H25 H28	1	<u> </u>	1	
		GND		1	1	†	H7				1
		GND				İ	L10			i	1
		GND		<u> </u>			L13				
		GND					L16	_			
		GND					L19				
		GND				1	L22			1	
		GND GND					L25 L28				



Pin Information for the Arria® V 5AGXFB7 Device Version 1.3 Note (1)

Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
	1	GND					L8				1111 (3)
	1	GND					M6				
		GND					N7				
		GND					P10				
		GND					P13			+	
	+	GND					P15				
		GND					P17			+	
	+	GND					P19				
		GND					P21				
		GND					P23				
	+	GND				+	P25				
	+	GND			+	+	R10 R12	+			
	+	GND			_	-		+			
	+	GND				-	R18	 			
		GND					R20				
		GND					R22				
		GND					R24				
		GND					T11				
		GND					T13				
		GND					T15				
		GND					T17				
		GND					T19				
		GND					T21				
		GND					T23				
		GND					T25				
		GND					U10				
		GND					U14				
		GND					U16				
		GND					U24				
		GND					V11				
		GND					V13				
	1	GND			1	1	V15	1			
	1	GND					V17	1		1	
	1	GND			1	1	V19	1			
	+	GND	+		+	+	V19 V21	†	+	- 	
	1	GND					V23	1			
	+	GND	+			1	V25	1	+	- 1	
	+	GND			+	-	W10	1	+	+	
	+	GND	<u> </u>			-	W12	1	+	- 	
					-	-	W14	1	+		
	+	GND			+	+		+			
	+	GND			+	+	W16	 			
	+	GND			_	-	W18	+			
		GND			_	-	W20	ļ			
		GND				<u> </u>	W22				
	1	GND					W24				
	1	GND			[U18			1	

Notes:
(1) For more information about pin definitions and pin connection guidelines, refer to the
Arria V Device Family Pin Connection Guidelines.
(2) GXB_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.
(3) RESET pin is only applicable for DDR3 device.



		□ 4.									Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
	1	DNU					A38				FH1 (3)
		DNU					B38				
		RREF_TL					B39				
GXB_L2		REFCLK5Ln					U32				
GXB_L2		REFCLK5Lp					U31				
GXB_L2		GXB_TX_L17n					C36				
GXB_L2		GXB_TX_L17p					C37				
GXB_L2 GXB L2	-	GXB_RX_L17p,GXB_REFCLK_L17p GXB_RX_L17n,GXB_REFCLK_L17n					D39 D38				1
GXB_L2		GXB_TX_L16n					E36				
GXB_L2		GXB_TX_L16p					E37				
GXB_L2		GXB_RX_L16p,GXB_REFCLK_L16p					F39				
GXB_L2		GXB RX L16n,GXB REFCLK L16n					F38				
GXB_L2		GXB_TX_L15n					G36				
GXB_L2		GXB_TX_L15p					G37				
GXB_L2		GXB_RX_L15p,GXB_REFCLK_L15p					H39				
GXB_L2		GXB_RX_L15n,GXB_REFCLK_L15n					H38				
GXB_L2		GXB_TX_L14n					J36				
GXB_L2 GXB_L2		GXB_TX_L14p GXB_RX_L14p,GXB_REFCLK_L14p					J37 K39				
GXB_L2 GXB_L2		GXB_RX_L14p,GXB_REFCLK_L14p					K38				
GXB_L2 GXB_L2	t	GXB_RX_L14n,GXB_REFCLK_L14n GXB_TX_L13n	 	†	+	 	1.36			 	1
GXB_L2 GXB_L2	1	GXB_TX_L13n	1	1	+		L37			<u> </u>	1
GXB_L2	1	GXB_RX_L13p,GXB_REFCLK_L13p		İ	İ		M39				i e
GXB_L2	1	GXB_RX_L13n,GXB_REFCLK_L13n		İ	İ		M38				i e
GXB_L2		GXB_TX_L12n					N36				
GXB_L2		GXB_TX_L12p					N37				
GXB_L2		GXB_RX_L12p,GXB_REFCLK_L12p					P39				
GXB_L2		GXB_RX_L12n,GXB_REFCLK_L12n					P38				
GXB_L2		REFCLK4Ln					W32				
GXB_L2		REFCLK4Lp					W31				
GXB_L1		REFCLK3Ln					AA32				
GXB_L1		REFCLK3Lp					AA31				
GXB_L1 GXB_L1	-	GXB_TX_L11n					R36 R37				1
GXB_L1		GXB_TX_L11p GXB_RX_L11p,GXB_REFCLK_L11p					T39				
GXB_L1		GXB_RX_L11n,GXB_REFCLK_L11n					T38				
GXB_L1	1	GXB_TX_L10n					U36				
GXB_L1		GXB_TX_L10p					U37				
GXB_L1		GXB_RX_L10p,GXB_REFCLK_L10p					V39				
GXB_L1		GXB_RX_L10n,GXB_REFCLK_L10n					V38				
GXB_L1		GXB_TX_L9n					W36				
GXB_L1		GXB_TX_L9p					W37				
GXB_L1		GXB_RX_L9p,GXB_REFCLK_L9p					Y39				
GXB_L1		GXB_RX_L9n,GXB_REFCLK_L9n					Y38				
GXB_L1 GXB_L1		GXB_TX_L8n GXB_TX_L8p					AA36 AA37				
GXB_L1 GXB_L1	-	GXB_RX_L8p,GXB_REFCLK_L8p					AB39				1
GXB_L1		GXB_RX_L8n,GXB_REFCLK_L8n					AB38				
GXB_L1		GXB TX L7n					AC36				
GXB_L1		GXB_TX_L7p					AC37				
GXB_L1		GXB_RX_L7p,GXB_REFCLK_L7p					AD39				
GXB_L1		GXB_RX_L7n,GXB_REFCLK_L7n					AD38				
GXB_L1		GXB_TX_L6n					AE36	-			
GXB_L1		GXB_TX_L6p		ļ	1		AE37				
GXB_L1	-	GXB_RX_L6p,GXB_REFCLK_L6p		ļ	+		AF39				.
GXB_L1	+	GXB_RX_L6n,GXB_REFCLK_L6n		1	+	-	AF38			ļ	
GXB_L1	 	REFCLK2Ln		 	 		AC32				
GXB_L1 GXB_L0	1	REFCLK2Lp REFCLK1Ln	+	1	+	 	AC31 AE32				1
GXB_L0 GXB_L0	+	REFCLK1Lp		†	+		AE32 AE31				1
GXB_L0	t	GXB_TX_L5n		t	†	†	AG36				1
GXB_L0	t	GXB_TX_L5p		t	†	†	AG37				1
GXB_L0	1	GXB_RX_L5p,GXB_REFCLK_L5p		1	1		AH39				
GXB_L0	1	GXB_RX_L5n,GXB_REFCLK_L5n		i e	1		AH38				İ
GXB_L0	İ.,	GXB_TX_L4n		<u> </u>			AJ36				<u>i </u>
GXB_L0		GXB_TX_L4p					AJ37				
GXB_L0		GXB_RX_L4p,GXB_REFCLK_L4p GXB_RX_L4n,GXB_REFCLK_L4n					AK39	-			
GXB_L0		GXB_RX_L4n,GXB_REFCLK_L4n					AK38	-			
GXB_L0	1	GXB_TX_L3n		ļ			AL36				
GXB_L0	1	GXB_TX_L3p		ļ	1		AL37				ļ
GXB_L0		GXB_RX_L3p,GXB_REFCLK_L3p		1	+	ļ	AM39			ļ	!
GXB_L0	+	GXB_RX_L3n,GXB_REFCLK_L3n		1	+	-	AM38			ļ	
GXB_L0 GXB_L0	 	GXB_TX_L2n GXB_TX_L2p		 	 		AN36 AN37				
	+		+	1	+	1				 	1
GXB_L0 GXB_L0	+	GXB_RX_L2p,GXB_REFCLK_L2p GXB_RX_L2n,GXB_REFCLK_L2n		1	+		AP39 AP38			-	
GAB_LU	+	GXB_TX_L1n		†	+		AP38 AR36				1
GXB I 0			The state of the s	1						-	
GXB_L0	-	GXR TX L1n					AR37				
GXB_L0 GXB_L0 GXB_L0		GXB_TX_L1p GXB_RX_L1p,GXB_REFCLK_L1p					AR37 AT39				



		D 4.									Note (1
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
XB_L0		GXB_TX_L0n					AU36				1 10/
XB_L0		GXB_TX_L0p					AU37				1
XB_L0		GXB_RX_L0p,GXB_REFCLK_L0p					AW37				1
XB_L0		GXB_RX_L0n,GXB_REFCLK_L0n					AW36				1
XB_L0		REFCLK0Ln					AG33				1
XB_L0		REFCLK0Lp					AG32				T
		DNU					AH31				1
A		TDO		TDO			AT34				1
A		TMS		TMS			AM35				1
BA .		TCK		TCK			AV34				
BA		TDI		TDI			AT33				
A		DCLK		DCLK			AW34				1
BA .		nCSO		DATA4			AR34				
3A		AS_DATA3		DATA3			AU34				
3A		AS_DATA2		DATA2			AR33				
3A		AS_DATA1		DATA1			AU33				
3A		AS_DATA0,ASDO		DATA0			AV33				1
3A	VREFB3AN0		RZQ 0		DIFFIO TX B1n	DIFFOUT B1n	AN33				1
34	VREFB3AN0	IO			DIFFIO_TX_B1p	DIFFOUT_B1p	AP33	DQ1B			1
3A	VRFFB3AN0	IO	CI K0n		DIFFIO RX B2n	DIFFOUT B2n	AN34	DQ1B			
3A	VREFB3AN0	10	CLK0p	1	DIFFIO_RX_B2p	DIFFOUT_B2p	AP34	DQ1B	i		1
3A	VREFB3AN0	10	The state of the s	1	DIFFIO TX B3n	DIFFOUT B3n	AK32		i		1
3A	VREFB3AN0	10	<u> </u>	+	DIFFIO_TX_B3p	DIFFOUT_B3p	AL32	DQ1B	†	 	1
3A	VREFB3AN0	lio	CLK1n	+	DIFFIO_TX_B3p	DIFFOUT_B3p	AJ34	DQSn1B/QK1B	†	 	+
34	VREFB3AN0	10	CLK11p	+	DIFFIO_RX_B4fi	DIFFOUT_B4n	AK34	DQS1B/QK1B DQS1B/CQ1B/CQn1B/QKn1B	1	<u>†</u>	+
3A	VREFB3AN0	10	FPLL BL CLKOUT1,FPLL BL CLKOUTn		DIFFIO_TX_B5n	DIFFOUT_B5n	AL34	DQ31B/CQ1B/CQIIIB/QRIIIB		1	+
9A	VREFB3AN0	10	FPLL_BL_CLKOUT0,FPLL_BL_CLKOUTp,FPLL_BL_FB0	+	DIFFIO_TX_B5p	DIFFOUT_B5p	AL34 AM34	DQ1B	1	<u>†</u>	+
3A	VREFB3AN0 VREFB3AN0	10	FPLL_BL_CLKOUTO,FPLL_BL_CLKOUTP,FPLL_BL_FBU FPLL_BL_CLKOUT3,FPLL_BL_FBn	+	DIFFIO_IX_B5p DIFFIO_RX_B6n	DIFFOUT_B5p	AM34 AJ33	DQ1B DQ1B	1	+	+
3M	VREFB3AN0 VREFB3AN0	10	FPLL_BL_CLKOUT3,FPLL_BL_FBn FPLL_BL_CLKOUT2,FPLL_BL_FBp,FPLL_BL_FB1	+	DIFFIO_RX_B6n DIFFIO_RX_B6p	DIFFOUT_B6n DIFFOUT B6p	AJ33 AK33		1	+	+
OM.		10		+	DIFFIU_KA_BOD	DIELOO1 Bob		DQ1B	1	+	+
JA	VREFB3AN0 VREFB3AN0	10	VREFB3AN0	+	+	 	AJ31	DOAD	+	+	+
3A		10					AK31	DQ1B			
3A	VREFB3AN0	10	CLK2n		DIFFIO RX B7n	DIFFOUT_B7n	AL33	DQ1B			
3A	VREFB3AN0	10	CLK2p		DIFFIO_RX_B7p	DIFFOUT_B7p	AM33	DQ1B			
3A	VREFB3AN0	10			DIFFIO_TX_B8n	DIFFOUT_B8n	AN32				CS#_3A_1
3A	VREFB3AN0	10			DIFFIO_TX_B8p	DIFFOUT_B8p	AP32	DQ2B	DQ1B		CS#_3A_0
3A	VREFB3AN0	10	CLK3n		DIFFIO_RX_B9n	DIFFOUT_B9n	AT32	DQ2B	DQ1B		
3A	VREFB3AN0	IO	CLK3p		DIFFIO_RX_B9p	DIFFOUT_B9p	AU32	DQ2B	DQ1B		
3A	VREFB3AN0	IO			DIFFIO_TX_B10n	DIFFOUT_B10n	AL31				ODT_3A_1
3A	VREFB3AN0	IO			DIFFIO_TX_B10p	DIFFOUT_B10p	AM31	DQ2B	DQ1B		ODT_3A_0
3A	VREFB3AN0	10			DIFFIO_RX_B11n	DIFFOUT_B11n	AW33	DQSn2B/QK2B	DQ1B		WE#_3A
3A	VREFB3AN0	10			DIFFIO_RX_B11p	DIFFOUT_B11p	AW32	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B		CAS#_3A
3A	VREFB3AN0	10			DIFFIO_TX_B12n	DIFFOUT_B12n	AN31				RAS#_3A
3A	VREFB3AN0	IO			DIFFIO_TX_B12p	DIFFOUT_B12p	AP31	DQ2B	DQ1B		BA_3A_2
3A	VREFB3AN0	10			DIFFIO_RX_B13n	DIFFOUT_B13n	AR31	DQ2B	DQ1B		BA_3A_1
3A	VREFB3AN0	10			DIFFIO_RX_B13p	DIFFOUT_B13p	AT31	DQ2B	DQ1B		BA_3A_0
3A	VREFB3AN0	10			DIFFIO_TX_B14n	DIFFOUT_B14n	AD29				A_3A_15
3A	VREFB3AN0	10			DIFFIO_TX_B14p	DIFFOUT_B14p	AE29	DQ2B	DQ1B		A_3A_14
3A	VREFB3AN0	10			DIFFIO RX B15n	DIFFOUT B15n	AG30	DQ2B	DQ1B		A 3A 13
3A	VREFB3AN0	10			DIFFIO_RX_B15p	DIFFOUT_B15p	AH30	DQ2B	DQ1B		A_3A_12
3A	VRFFB3AN0	IO			DIFFIO TX B16n	DIFFOUT B16n	AU31				A 3A 11
3A	VREFB3AN0	IO			DIFFIO_TX_B16p	DIFFOUT_B16p	AV31	DQ3B	DQ1B		A 3A 10
34	VREEB3ANO	10			DIFFIO RX B17n	DIFFOLIT B17n	AW30	DQ3B	DQ1B		A 3A 9
34	VREFB3AN0	10			DIFFIO_RX_B17p	DIFFOUT_B17p	AW31	DQ3B	DQ1B		A_3A_8
34	VREFB3AN0	lio	<u> </u>	+	DIFFIO_TX_B18n	DIFFOUT_B18n	AK30		F	 	A 3A 7
34	VREFB3AN0	lio	†	+	DIFFIO_TX_B18p	DIFFOUT_B18p	AL30	DQ3B	DQ1B	1	A_3A_7 A_3A_6
3A	VREFB3AN0	lio.	†	1	DIFFIO_IX_B10p	DIFFOUT_B18p	AR30	DOSn3B/OK3B	DOSn1B/OK1B	†	A_3A_5
34	VREFB3AN0	lio.	+	+	DIFFIO_RX_B19p	DIFFOUT_B19p	AT30	DQS3B/CQ3B/CQn3B/QKn3B	DQS1B/QQ1B/CQn1B/QKn1B	 	A_3A_4
3A	VREFB3AN0	10	+	+	DIFFIO_RX_B19p	DIFFOUT_B19p	AU30	DQGGB/CQGB/CQHGB/QNHGB	DQC1D/CQ1D/CQIIID/QRIIID	<u>†</u>	A_3A_4 A_3A_3
3A	VREFB3AN0	lio	+	+	DIFFIO_TX_B20p	DIFFOUT_B20p	AV30	DQ3B	DQ1B	<u>†</u>	A_3A_3 A_3A_2
2A	VREFB3AN0 VREFB3AN0	10	†	+	DIFFIO_IX_B20p DIFFIO_RX_B21n	DIFFOUT_B20p DIFFOUT_B21n	AV30 AT29	DQ3B DQ3B	DQ1B	+	A_3A_2 A_3A_1
3A 3A		10	+	+				DQ3B DQ3B	DQ1B DQ1B	+	A_3A_1 A 3A 0
0/1	VREFB3AN0	10	+	+	DIFFIO_RX_B21p	DIFFOUT_B21p	AU29	D/40D	DQ1D	+	
3A	VREFB3AN0	10	+	+	DIFFIO_TX_B22n	DIFFOUT_B22n	AN30	Door	2012	+	CKE_3A_1
3A	VREFB3AN0	10	+	+	DIFFIO_TX_B22p	DIFFOUT_B22p	AP30	DQ3B	DQ1B	+	CKE_3A_0
3A	VREFB3AN0	10			DIFFIO_RX_B23n	DIFFOUT_B23n	AN29	DQ3B	DQ1B		CK#_3A
3A	VREFB3AN0	IO	<u> </u>		DIFFIO_RX_B23p	DIFFOUT_B23p	AP29	DQ3B	DQ1B	 	CK_3A
3B	VREFB3BN0	IO	<u> </u>		DIFFIO_TX_B24n	DIFFOUT_B24n	AB29	l	L	 	RESET#_3A
3B	VREFB3BN0	IO	<u> </u>	1	DIFFIO_TX_B24p	DIFFOUT_B24p	AC29	DQ4B	DQ2B	DQ1B	DQ1_3B_8
3B	VREFB3BN0	10		1	DIFFIO_RX_B25n	DIFFOUT_B25n	AF28	DQ4B	DQ2B	DQ1B	DQ1_3B_7
3B	VREFB3BN0	IO		1	DIFFIO_RX_B25p	DIFFOUT_B25p	AG28	DQ4B	DQ2B	DQ1B	DQ1_3B_6
3B	VREFB3BN0	10			DIFFIO_TX_B26n	DIFFOUT_B26n	AK29				
3B	VREFB3BN0	10			DIFFIO_TX_B26p	DIFFOUT_B26p	AL29	DQ4B	DQ2B	DQ1B	DM1_3B
3B	VREFB3BN0	10			DIFFIO_RX_B27n	DIFFOUT_B27n	AH28	DQSn4B/QK4B	DQ2B	DQ1B	DQS#1_3B
3B	VREFB3BN0	10			DIFFIO_RX_B27p	DIFFOUT_B27p	AJ28	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	DQ1B	DQS1_3B
3B	VREFB3BN0	10			DIFFIO_TX_B28n	DIFFOUT_B28n	AD28				T
3B	VREFB3BN0	IO	1	1	DIFFIO_TX_B28p	DIFFOUT_B28p	AE28	DQ4B	DQ2B	DQ1B	DQ1_3B_5
3B	VREFB3BN0	10	1	1	DIFFIO_RX_B29n	DIFFOUT_B29n	AB27	DQ4B	DQ2B	DQ1B	DQ1_3B_4
	VREFB3BN0	10	1	1	DIFFIO_RX_B29p	DIFFOUT_B29p	AB28	DQ4B	DQ2B	DQ1B	DQ1_3B_3
3B			VREFB3BN0	1			AL 28				
3B 3B	VRFFB3BN0										
		10	VREFB3BNU				AM28	DO4B	DO2B	DO1B	DO1 3B 2
	VREFB3BN0 VREFB3BN0 VREFB3BN0	10 10	VNEFBSBNU		DIFFIO_RX_B30n	DIFFOUT_B30n	AM28 AC27	DQ4B DQ4B	DQ2B DQ2B	DQ1B DQ1B	DQ1_3B_2 DQ1_3B_1



											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
3B	VREFB3BN0	IO			DIFFIO_TX_B31n	DIFFOUT_B31n	AP28				1111 (3)
3B	VREFB3BN0	Ю			DIFFIO_TX_B31p	DIFFOUT_B31p	AR28	DQ5B	DQ2B	DQ1B	DQ2_3B_8
3B	VREFB3BN0	10			DIFFIO_RX_B32n	DIFFOUT_B32n	AU28	DQ5B	DQ2B	DQ1B	DQ2_3B_7
BB	VREFB3BN0	10			DIFFIO_RX_B32p	DIFFOUT_B32p	AV28	DQ5B	DQ2B	DQ1B	DQ2_3B_6
BB	VREFB3BN0 VREFB3BN0	10			DIFFIO_TX_B33n DIFFIO_TX_B33n	DIFFOUT_B33n DIFFOUT_B33n	AJ27 AK27	DO5B	DQ2B	DO1B	DM2_3B
3B	VREFB3BN0	10			DIFFIO_RX_B34n	DIFFOUT_B34n	AW29	DQSn5B/QK5B	DQSn2B/QK2B	DQ1B	DQS#2_3B
3B	VREFB3BN0	10			DIFFIO RX B34p	DIFFOUT B34p	AW28	DQS5B/CQ5B/CQn5B/QKn5B	DQS2B/CQ2B/CQn2B/QKn2B	DQ1B	DQS2 3B
3B	VREFB3BN0	10			DIFFIO_TX_B35n	DIFFOUT_B35n	AP27				
3B	VREFB3BN0	IO			DIFFIO_TX_B35p	DIFFOUT_B35p	AR27	DQ5B	DQ2B	DQ1B	DQ2_3B_5
3B	VREFB3BN0	10			DIFFIO_RX_B36n	DIFFOUT_B36n	AT27	DQ5B	DQ2B	DQ1B	DQ2_3B_4
3B	VREFB3BN0	10			DIFFIO_RX_B36p	DIFFOUT_B36p	AU27	DQ5B	DQ2B	DQ1B	DQ2_3B_3
3B	VREFB3BN0 VREFB3BN0	10			DIFFIO TX B37n	DIFFOUT_B37n DIFFOUT_B37p	AM27 AN27	DO5B	DQ2B	DO1B	DQ2_3B_2
3B	VREFB3BN0	10			DIFFIO_TX_B37p	DIFFOUT_B38n	AV27	DQ5B	DQ2B	DQ1B DQ1B	DQ2_3B_1
3B	VREFB3BN0	in			DIFFIO RX B38p	DIFFOUT B38p	AW27	DQ5B	DQ2B	DQ1B	DQ2_3B_0
3C	VREFB3CN0	10			DIFFIO_TX_B39n	DIFFOUT B39n	AG27	5405	Date	DQ1D	
3C	VREFB3CN0	10			DIFFIO_TX_B39p	DIFFOUT_B39p	AH27	DQ6B	DQ3B	DQ1B	DQ3_3C_8
3C	VREFB3CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B40n	AB25	DQ6B	DQ3B	DQ1B	DQ3_3C_7
3C	VREFB3CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B40p	AC25	DQ6B	DQ3B	DQ1B	DQ3_3C_6
3C	VREFB3CN0	10			DIFFIO_TX_B41n	DIFFOUT_B41n	AE27				
3C	VREFB3CN0	IIO		+	DIFFIO_TX_B41p	DIFFOUT_B41p	AF27	DQ6B	DQ3B	DQ1B	DM3_3C
3C	VREFB3CN0	IO		+	DIFFIO_RX_B42n	DIFFOUT_B42n	AE25	DQSn6B/QK6B	DQ3B	DQSn1B/QK1B	DQS#3_3C
3C	VREFB3CN0 VREFB3CN0	IO IO		 	DIFFIO_RX_B42p DIFFIO_TX_B43n	DIFFOUT_B42p DIFFOUT_B43n	AF25 AC24	DQS6B/CQ6B/CQn6B/QKn6B	DQ3B	DQS1B/CQ1B/CQn1B/QKn1B	DQS3_3C
3C	VREFB3CN0 VREFB3CN0	lio		†	DIFFIO_TX_B43n DIFFIO_TX_B43p	DIFFOUT_B43n DIFFOUT_B43p	AC24 AD25	DQ6B	DQ3B	DQ1B	DQ3_3C_5
3C	VREFB3CN0	10		1	DIFFIO_RX_B44n	DIFFOUT_B43p	AG26	DQ6B	DQ3B	DQ1B DQ1B	DQ3_3C_5
3C	VREFB3CN0	10		1	DIFFIO_RX_B44p	DIFFOUT_B44p	AH26	DQ6B	DQ3B	DQ1B	DQ3_3C_3
3C	VREFB3CN0	10			DIFFIO_TX_B45n	DIFFOUT_B45n	AD26				
3C	VREFB3CN0	IO			DIFFIO_TX_B45p	DIFFOUT_B45p	AE26	DQ6B	DQ3B	DQ1B	DQ3_3C_2
3C	VREFB3CN0	IO			DIFFIO_RX_B46n	DIFFOUT_B46n	AG25	DQ6B	DQ3B	DQ1B	DQ3_3C_1
3C	VREFB3CN0	10			DIFFIO_RX_B46p	DIFFOUT_B46p	AH25	DQ6B	DQ3B	DQ1B	DQ3_3C_0
3C	VREFB3CN0	10			DIFFIO_TX_B47n	DIFFOUT_B47n	AN26				
3C	VREFB3CN0	10			DIFFIO_TX_B47p DIFFIO_RX_B48n	DIFFOUT_B47p	AP26 AM25	DQ7B	DQ3B	DQ1B DQ1B	DQ4_3C_8
3C	VREFB3CN0 VREFB3CN0	10			DIFFIO_RX_B48n DIFFIO RX B48p	DIFFOUT_B48n DIFFOUT_B48p	AM25 AN25	DQ7B DQ7B	DQ3B DQ3B	DQ1B DQ1B	DQ4_3C_7 DQ4_3C_6
3C	VREFB3CN0	10			DIFFIO_RX_B46p	DIFFOUT_B46p	AIN25 AJ25	БQ/В	DQ3B	DQIB	DQ4_3C_6
3C	VREFB3CN0	in			DIFFIO TX B49p	DIFFOUT_B49p	AK25	DQ7B	DQ3B	DQ1B	DM4_3C
3C	VREFB3CN0	10			DIFFIO RX B50n	DIFFOUT B50n	AT26	DQSn7B/QK7B	DQSn3B/QK3B	DQ1B	DQS#4 3C
3C	VREFB3CN0	Ю			DIFFIO_RX_B50p	DIFFOUT_B50p	AU26	DQS7B/CQ7B/CQn7B/QKn7B	DQS3B/CQ3B/CQn3B/QKn3B	DQ1B	DQS4_3C
3C	VREFB3CN0	IO			DIFFIO_TX_B51n	DIFFOUT_B51n	AR25				
3C	VREFB3CN0	IO			DIFFIO_TX_B51p	DIFFOUT_B51p	AT25	DQ7B	DQ3B	DQ1B	DQ4_3C_5
3C	VREFB3CN0	10			DIFFIO_RX_B52n	DIFFOUT_B52n	AW25	DQ7B	DQ3B	DQ1B	DQ4_3C_4
3C	VREFB3CN0	10			DIFFIO_RX_B52p	DIFFOUT_B52p	AW26	DQ7B	DQ3B	DQ1B	DQ4_3C_3
3C	VREFB3CN0 VREFB3CN0	10	VREFB3CN0				AK26 AL26	DQ7B	DQ3B	DQ1B	DQ4_3C_2
3C	VREFB3CN0 VREFB3CN0	10			DIFFIO_RX_B53n	DIFFOUT_B53n	AV25	DQ7B	DQ3B	DQ1B	DQ4_3C_2 DQ4_3C_1
3C	VREFB3CN0	in			DIFFIO_RX_B53p	DIFFOUT B53p	AV24	DQ7B	DQ3B	DQ1B DQ1B	DQ4_3C_0
3C	VREFB3CN0	10			DIFFIO TX B54n	DIFFOUT_B54n	AD23	Dairo	5405	DQ1D	
3C	VREFB3CN0	IO			DIFFIO_TX_B54p	DIFFOUT_B54p	AD24	DQ8B	DQ4B	DQ2B	DQ5_3C_8
3C	VREFB3CN0	10			DIFFIO_RX_B55n	DIFFOUT_B55n	AT24	DQ8B	DQ4B	DQ2B	DQ5_3C_7
3C	VREFB3CN0	IO			DIFFIO_RX_B55p	DIFFOUT_B55p	AU24	DQ8B	DQ4B	DQ2B	DQ5_3C_6
3C	VREFB3CN0	10		1	DIFFIO_TX_B56n	DIFFOUT_B56n	AK24				
3C	VREFB3CN0	10		1	DIFFIO_TX_B56p	DIFFOUT_B56p	AL24	DQ8B	DQ4B	DQ2B	DM5_3C
3C	VREFB3CN0	IO		+	DIFFIO_RX_B57n	DIFFOUT_B57n	AE24	DQSn8B/QK8B	DQ4B	DQ2B	DQS#5_3C
3C	VREFB3CN0 VREFB3CN0	10		+	DIFFIO_RX_B57p DIFFIO_TX_B58n	DIFFOUT_B57p DIFFOUT_B58n	AF24 AG24	DQS8B/CQ8B/CQn8B/QKn8B	DQ4B	DQ2B	DQS5_3C
3C	VREFB3CN0	lio		+	DIFFIO_TX_B58n	DIFFOUT_B58n	AG24 AH24	DO8B	DO4B	DO2B	DO5 3C 5
3C	VREFB3CN0	lio		†	DIFFIO_TX_B56p	DIFFOUT_B56p	AH24 AW23	DQ8B	DQ4B	DQ2B	DQ5_3C_5 DQ5_3C_4
3C	VREFB3CN0	IO		1	DIFFIO_RX_B59p	DIFFOUT_B59p	AW24	DQ8B	DQ4B	DQ2B	DQ5_3C_3
3C	VREFB3CN0	10		1	DIFFIO_TX_B60n	DIFFOUT_B60n	AN24				1
3C	VREFB3CN0	10			DIFFIO_TX_B60p	DIFFOUT_B60p	AP24	DQ8B	DQ4B	DQ2B	DQ5_3C_2
3C	VREFB3CN0	Ю			DIFFIO_RX_B61n	DIFFOUT_B61n	AT23	DQ8B	DQ4B	DQ2B	DQ5_3C_1
3C	VREFB3CN0	10		1	DIFFIO_RX_B61p	DIFFOUT_B61p	AU23	DQ8B	DQ4B	DQ2B	DQ5_3C_0
3D	VREFB3DN0	10			DIFFIO_TX_B62n	DIFFOUT_B62n	AN23				+
3D	VREFB3DN0	IIO	1	+	DIFFIO_TX_B62p	DIFFOUT_B62p	AP23	DQ9B	DQ4B	DQ2B	4
3D	VREFB3DN0 VREFB3DN0	IO IO		 	DIFFIO_RX_B63n	DIFFOUT_B63n DIFFOUT_B63p	AD22 AE23	DQ9B DQ9B	DQ4B DQ4B	DQ2B	+
3D 3D	VREFB3DN0 VREFB3DN0	io		+	DIFFIO_RX_B63p DIFFIO_TX_B64n	DIFFOUT_B63p DIFFOUT_B64n	AE23 AK23	DOM	DUTE	DQ2B	+
		lio	 	t	DIFFIO_TX_B64b	DIFFOUT_B64n	AN23	DO9B	DO4B	DO2B	+
3D	VREER3DN0	P ^o			DIFFIO_RX_B65n	DIFFOUT_B65n	AT22	DQSn9B/QK9B	DQSn4B/QK4B	DQ2B	1
		10			DIFFIO RX B65n	DIFFOUT B65p	AU22	DQS9B/CQ9B/CQn9B/QKn9B	DQS4B/CQ4B/CQn4B/QKn4B	DQ2B	1
3D	VREFB3DN0 VREFB3DN0 VREFB3DN0	10			DIFFIO_RX_B65D						
3D 3D	VREFB3DN0	10 10			DIFFIO_RX_B66n	DIFFOUT_B66n	AV22				
3D 3D 3D 3D	VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0	10 10 10			DIFFIO_TX_B66n DIFFIO_TX_B66p	DIFFOUT_B66p	AW22	DQ9B	DQ4B	DQ2B	
3D 3D 3D 3D 3D 3D	VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0	10 10 10 10			DIFFIO_TX_B66n DIFFIO_TX_B66p DIFFIO_RX_B67n	DIFFOUT_B66p DIFFOUT_B67n	AW22 AV21	DQ9B	DQ4B	DQ2B	
3D 3D 3D 3D 3D 3D	VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0	O			DIFFIO_TX_B66n DIFFIO_TX_B66p DIFFIO_RX_B67n DIFFIO_RX_B67p	DIFFOUT_B66p DIFFOUT_B67n DIFFOUT_B67p	AW22 AV21 AW21				
3D 3D 3D 3D 3D 3D 3D 3D 3D	VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0	10 10 10 10 10 10			DIFFIO TX B66n DIFFIO TX B66p DIFFIO RX B67n DIFFIO RX B67p DIFFIO TX B68n	DIFFOUT_B66p DIFFOUT_B67n DIFFOUT_B67p DIFFOUT_B68n	AW22 AV21 AW21 AG23	DQ9B DQ9B	DQ4B DQ4B	DQ2B DQ2B	
3D 3D 3D 3D 3D 3D 3D 3D 3D	VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0	IO			DIFFIO TX B66n DIFFIO TX B66p DIFFIO RX B67n DIFFIO RX B67p DIFFIO TX B68n DIFFIO TX B68p	DIFFOUT_B66p DIFFOUT_B67n DIFFOUT_B67p DIFFOUT_B68n DIFFOUT_B68p	AW22 AV21 AW21 AG23 AH23	DQ9B DQ9B DQ9B	DQ4B DQ4B DQ4B	DQ2B DQ2B DQ2B	
3D 3D 3D 3D 3D 3D 3D 3D	VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0 VREFB3DN0	O			DIFFIO TX B66n DIFFIO TX B66p DIFFIO RX B67n DIFFIO RX B67p DIFFIO TX B68n	DIFFOUT_B66p DIFFOUT_B67n DIFFOUT_B67p DIFFOUT_B68n	AW22 AV21 AW21 AG23	DQ9B DQ9B	DQ4B DQ4B	DQ2B DQ2B	



	VDEE	Dishlama/Franchisa /01	Ontinent Frantise (a)	C	D-4: 'T 'D	Familiate d 11000	F4547	DOC 4 VOIVO	DOC 4 V4C/ V40	DOC 4 V20/ VCC	Note (
ank umber	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
	VREFB3DN0	10			DIFFIO_TX_B70p	DIFFOUT_B70p	AP22	DQ10B	DQ5B	DQ2B	
	VREFB3DN0	10			DIFFIO_RX_B71n	DIFFOUT_B71n	AW 19	DQ10B	DQ5B	DQ2B	
	VREFB3DN0	10			DIFFIO_RX_B71p	DIFFOUT B71p	AW 20	DQ10B	DQ5B	DQ2B	
	VREFB3DN0	IO			DIFFIO_TX_B72n	DIFFOUT_B72n	AK22				+
	VREEB3DN0	IO			DIFFIO_TX_B72p	DIFFOUT_B72p	AL22	DQ10B	DQ5B	DQ2B	+
	VREFB3DN0	in			DIFFIO RX B73n	DIFFOUT B73n	AR21	DQSn10B/QK10B	DQ5B	DQSn2B/QK2B	+
	VREFB3DN0	10			DIFFIO_RX_B73n	DIFFOUT B73n	AT21	DQS10B/CQ10B/CQn10B/QKn10B	DQ5B DQ5B	DQS12B/QR2B DQS2B/CQ2B/CQn2B/QKn2B	+
	= 0=	10						DQS10B/CQ10B/CQ110B/QK110B	DQSB	DQ52B/CQ2B/CQ112B/QK112B	
	VREFB3DN0	10			DIFFIO_TX_B74n DIFFIO_TX_B74n	DIFFOUT_B74n DIFFOUT_B74n	AG22 AH22	DQ10B	DQ5B	DQ2B	+
	VREFB3DN0	10									
	VREFB3DN0	10			DIFFIO_RX_B75n	DIFFOUT_B75n	AT20	DQ10B	DQ5B	DQ2B	
	VREFB3DN0	10			DIFFIO_RX_B75p	DIFFOUT_B75p	AU20	DQ10B	DQ5B	DQ2B	
	VREFB3DN0	10	VREFB3DN0				AJ21				
	VREFB3DN0	10					AK21	DQ10B	DQ5B	DQ2B	
	VREFB3DN0	10	CLK4n		DIFFIO_RX_B76n	DIFFOUT_B76n	AU19	DQ10B	DQ5B	DQ2B	
	VREFB3DN0	10	CLK4p		DIFFIO_RX_B76p	DIFFOUT_B76p	AV19	DQ10B	DQ5B	DQ2B	T
	VREFB3DN0	10			DIFFIO_TX_B77n	DIFFOUT_B77n	AM21				
	VREFB3DN0	IO			DIFFIO_TX_B77p	DIFFOUT_B77p	AN21	DQ11B	DQ5B	DQ2B	+
	VREFB3DN0	10	CI K5n		DIFFIO RX B78n	DIFFOUT B78n	AF21	DQ11B	DQ5B	DQ2B	-
	VREFB3DN0	10	CLK5p	+	DIFFIO_RX_B78p	DIFFOUT_B78p	AF21	DQ11B	DQ5B	DQ2B	+
		10						DQ11B	DQ5B	DQ2B	
	VREFB3DN0	10	FPLL_BC_CLKOUT1,FPLL_BC_CLKOUTn	+	DIFFIO_TX_B79n	DIFFOUT_B79n	AD21				+
	VREFB3DN0	10	FPLL BC CLKOUT0,FPLL BC CLKOUTp,FPLL BC FB0	1	DIFFIO_TX_B79p	DIFFOUT_B79p	AC22	DQ11B	DQ5B	DQ2B	
	VREFB3DN0	10	FPLL_BC_CLKOUT3,FPLL_BC_FBn	_[DIFFIO_RX_B80n	DIFFOUT_B80n	AG21	DQSn11B/QK11B	DQSn5B/QK5B	DQ2B	
	VREFB3DN0	10	FPLL_BC_CLKOUT2,FPLL_BC_FBp,FPLL_BC_FB1		DIFFIO_RX_B80p	DIFFOUT_B80p	AH21	DQS11B/CQ11B/CQn11B/QKn11B	DQS5B/CQ5B/CQn5B/QKn5B	DQ2B	
	VREFB3DN0	10			DIFFIO_TX_B81n	DIFFOUT_B81n	AN20				
	VREFB3DN0	10			DIFFIO_TX_B81p	DIFFOUT_B81p	AP20	DQ11B	DQ5B	DQ2B	1
	VREFB3DN0	10	CLK6n		DIFFIO_RX_B82n	DIFFOUT_B82n	AC21	DQ11B	DQ5B	DQ2B	1
	VREFB3DN0	in.	CLK6p	1	DIFFIO_RX_B82p	DIFFOUT_B82p	AD20	DQ11B	DQ5B	DQ2B	1
	VREFB3DN0	lio.	o E rop	+	DIFFIO_TX_B83n	DIFFOUT_B83n	AG20	540	5405		+
		10		+				DOMAR	DOED	DOOR	+
	VREFB3DN0	10		-	DIFFIO_TX_B83p	DIFFOUT_B83p	AH20	DQ11B	DQ5B	DQ2B	
	VREFB3DN0	10	CLK7n		DIFFIO_RX_B84n	DIFFOUT_B84n	AK20	DQ11B	DQ5B	DQ2B	
	VREFB3DN0	IO	CLK7p		DIFFIO_RX_B84p	DIFFOUT_B84p	AL20	DQ11B	DQ5B	DQ2B	
		VCCD_FPLL					AB20				
		VCCA_FPLL					AB21				T
		DNU					AE20				_
	VREFB4DN0				DIFFIO_TX_B85n	DIFFOUT_B85n	AV/18				+
	VREFB4DN0	10			DIFFIO_TX_B85p	DIFFOUT B85p	AW18	DQ12B			
	VREFB4DN0	10			DIFFIO_TX_B85p	DIFFOUT_B86n	AG19	DQ12B			
	= .=	10									
	VREFB4DN0	10			DIFFIO_RX_B86p	DIFFOUT_B86p	AH19	DQ12B			
	VREFB4DN0	10			DIFFIO_TX_B87n	DIFFOUT_B87n	AN19				
	VREFB4DN0	10			DIFFIO_TX_B87p	DIFFOUT_B87p	AP19	DQ12B			
	VREFB4DN0	10			DIFFIO_RX_B88n	DIFFOUT_B88n	AK19	DQSn12B/QK12B			
	VREFB4DN0	10			DIFFIO_RX_B88p	DIFFOUT_B88p	AL19	DQS12B/CQ12B/CQn12B/QKn12B			
	VRFFB4DN0	in.			DIFFIO TX B89n	DIFFOUT B89n	AH18				_
	VREFB4DN0	10			DIFFIO_TX_B89p	DIFFOUT_B89p	AJ18	DQ12B			_
	VREFB4DN0	10		+	DIFFIO_RX_B90n	DIFFOUT_B90n	AU18	DQ12B			
		10									
	VREFB4DN0	10			DIFFIO_RX_B90p	DIFFOUT_B90p	AT19	DQ12B			_
	VREFB4DN0	10			DIFFIO_TX_B91n	DIFFOUT_B91n	AE19				
	VREFB4DN0	IO			DIFFIO_TX_B91p	DIFFOUT_B91p	AF19	DQ12B			
	VREFB4DN0	10			DIFFIO_RX_B92n	DIFFOUT_B92n	AW 17	DQ12B			
	VREFB4DN0	10			DIFFIO RX B92p	DIFFOUT B92p	AW 16	DQ12B			
	VREFB4DN0	IO.			DIFFIO_TX_B93n	DIFFOUT_B93n	AK17				CS# 4D 1
	VREFB4DN0	in		1	DIFFIO_TX_B93p	DIFFOUT B93p	ΔΙ 17	DQ13B	DQ6B	1	CS# 4D 0
	VREFB4DN0	In	İ	1	DIFFIO RX B94n	DIFFOUT_B94n	AT17	DQ13B	DQ6B	1	1
		10	1	+	DIFFIO_RX_B94n	DIFFOUT_B94n	A117		DO6B	1	A 4D 15
	VREFB4DN0	IU		1				DQ13B	DUOD	+	
	VREFB4DN0	IU	1	+	DIFFIO_TX_B95n	DIFFOUT_B95n	AC19	ļ	1		ODT_4D_4
	VREFB4DN0	10		1	DIFFIO_TX_B95p	DIFFOUT_B95p	AD19	DQ13B	DQ6B	ļ	ODT_4D_0
	VREFB4DN0	10			DIFFIO_RX_B96n	DIFFOUT_B96n	AP18	DQSn13B/QK13B	DQ6B		WE#_4D
	VREFB4DN0	10	<u> </u>		DIFFIO_RX_B96p	DIFFOUT_B96p	AR18	DQS13B/CQ13B/CQn13B/QKn13B	DQ6B		CAS#_4D
	VREFB4DN0	10			DIFFIO_TX_B97n	DIFFOUT_B97n	AD17				RAS#_4D
	VREFB4DN0	10			DIFFIO TX B97p	DIFFOUT_B97p	AC18	DQ13B	DQ6B	1	BA 4D 2
	VREFB4DN0	io.		1	DIFFIO_RX_B98n	DIFFOUT_B98n	AD18	DQ13B	DQ6B	1	BA_4D_1
	VREFB4DN0 VREFB4DN0	10	 	1	DIFFIO_RX_B98p	DIFFOUT_B98p	AE18	DQ13B DQ13B	DQ6B	1	BA_4D_1
		IU	VDCCD (DV)	1	DIEFIO_KX_B98p	DILLOUI_RASD		DUISB	DUOD	+	BA_4D_0
	VREFB4DN0	IU	VREFB4DN0		-	ļ	AF18			ļ	
	VREFB4DN0	10		1			AG18	DQ13B	DQ6B	ļ	A_4D_14
	VREFB4DN0	10	<u> </u>		DIFFIO_RX_B99n	DIFFOUT_B99n	AL18	DQ13B	DQ6B	<u> </u>	A_4D_13
	VREFB4DN0	10	1		DIFFIO_RX_B99p	DIFFOUT_B99p	AM18	DQ13B	DQ6B		A_4D_12
	VREFB4DN0	10			DIFFIO_TX_B100n	DIFFOUT_B100n	AG17				A_4D_11
	VREFB4DN0	IO			DIFFIO_TX_B100p	DIFFOUT_B100p	AH17	DQ14B	DQ6B		A_4D_10
	VREFB4DN0	io.		1	DIFFIO RX B101n	DIFFOUT B101n	AN17	DQ14B	DQ6B	1	A 4D 9
		10	†	+	DIFFIO_RX_B101p		AP17			 	A_4D_9 A_4D_8
	VREFB4DN0	10		+		DIFFOUT_B101p		DQ14B	DQ6B	1	
	VREFB4DN0	IU	1	+	DIFFIO_TX_B102n	DIFFOUT_B102n	AR16	ļ	1		A_4D_7
	VREFB4DN0	10			DIFFIO_TX_B102p	DIFFOUT_B102p	AT16	DQ14B	DQ6B		A_4D_6
	VREFB4DN0	10	<u> </u>		DIFFIO_RX_B103n	DIFFOUT_B103n	AU16	DQSn14B/QK14B	DQSn6B/QK6B		A_4D_5
	VREFB4DN0	10			DIFFIO_RX_B103p	DIFFOUT_B103p	AV16	DQS14B/CQ14B/CQn14B/QKn14B	DQS6B/CQ6B/CQn6B/QKn6B		A_4D_4
	VREFB4DN0	IO			DIFFIO TX B104n	DIFFOUT_B104n	AJ16			1	A_4D_3
	VREFB4DN0	lin	İ	1	DIFFIO_TX_B104p	DIFFOUT_B104p	AK16	DQ14B	DQ6B	1	A_4D_2
		10		+						1	
	VREFB4DN0	IIO	1	+	DIFFIO_RX_B105n	DIFFOUT_B105n	AN16	DQ14B	DQ6B	 	A_4D_1
	VREFB4DN0	Ю		1	DIFFIO_RX_B105p	DIFFOUT_B105p	AP16	DQ14B	DQ6B		A_4D_0
_	VREFB4DN0	10	<u> </u>	<u> </u>	DIFFIO_TX_B106n	DIFFOUT_B106n	AL16	<u> </u>	<u> </u>	<u> </u>	CKE_4D_1
	VRFFB4DN0	IO			DIFFIO TX B106p	DIFFOUT_B106p	AM16	DQ14B	DQ6B		CKE 4D 0
	VKEFB4DN0										



											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
4D	VREFB4DN0	IO			DIFFIO_RX_B107p	DIFFOUT_B107p	AF16	DQ14B	DQ6B		CK_4D
4C	VREFB4CN0	10			DIFFIO_TX_B108n	DIFFOUT_B108n	AN15				RESET#_4D
4C	VREFB4CN0	Ю			DIFFIO_TX_B108p	DIFFOUT_B108p	AP15	DQ15B	DQ7B	DQ3B	DQ1_4C_8
4C	VREFB4CN0	IO			DIFFIO_RX_B109n	DIFFOUT_B109n	AW 14	DQ15B	DQ7B	DQ3B	DQ1_4C_7
4C	VREFB4CN0	10			DIFFIO_RX_B109p	DIFFOUT_B109p	AW 15	DQ15B	DQ7B	DQ3B	DQ1_4C_6
4C	VREFB4CN0	10			DIFFIO_TX_B110n	DIFFOUT_B110n	AC16	DOAFR	DO70	DOOR	DM4 40
4C	VREFB4CN0 VREFB4CN0	10			DIFFIO_TX_B110p DIFFIO_RX_B111n	DIFFOUT_B110p DIFFOUT_B111n	AD16 AG16	DQ15B DQSn15B/QK15B	DQ7B DQ7B	DQ3B DQ3B	DM1_4C DQS#1_4C
4C	VREFB4CN0	10			DIFFIO_RX_B111p	DIFFOUT_B111p	AH16	DQS15B/CQ15B/CQn15B/QKn15B	DQ7B	DQ3B	DQS#1_4C
4C	VREFB4CN0	10			DIFFIO TX B112n	DIFFOUT_B112n	AK15	DQ013B/0Q13B/0Q113B/QR113B	DQ/B	DGOD	DQ01_40
4C	VREFB4CN0	IO			DIFFIO_TX_B112p	DIFFOUT_B112p	AL15	DQ15B	DQ7B	DQ3B	DQ1_4C_5
4C	VREFB4CN0	10			DIFFIO RX B113n	DIFFOUT B113n	AV13	DQ15B	DQ7B	DQ3B	DQ1_4C_4
4C	VREFB4CN0	10			DIFFIO_RX_B113p	DIFFOUT_B113p	AW 13	DQ15B	DQ7B	DQ3B	DQ1_4C_3
4C	VREFB4CN0	10	VREFB4CN0				AG15				
4C	VREFB4CN0	10					AH15	DQ15B	DQ7B	DQ3B	DQ1_4C_2
4C	VREFB4CN0	10			DIFFIO_RX_B114n	DIFFOUT_B114n	AT15	DQ15B	DQ7B	DQ3B	DQ1_4C_1
4C	VREFB4CN0	10			DIFFIO_RX_B114p	DIFFOUT_B114p	AU15	DQ15B	DQ7B	DQ3B	DQ1_4C_0
4C	VREFB4CN0	10			DIFFIO_TX_B115n	DIFFOUT_B115n	AC15				
4C	VREFB4CN0	10			DIFFIO_TX_B115p	DIFFOUT_B115p	AD14	DQ16B	DQ7B	DQ3B	DQ2_4C_8
10	VREFB4CN0	10			DIFFIO_RX_B116n	DIFFOUT_B116n	AT14	DQ16B	DQ7B	DQ3B	DQ2_4C_7
10	VREFB4CN0 VREFB4CN0	10			DIFFIO RX B116p DIFFIO TX B117n	DIFFOUT_B116p DIFFOUT_B117n	AU14 AT13	DQ16B	DQ7B	DQ3B	DQ2 4C 6
1C	VREFB4CN0 VREFB4CN0	10	1	1	DIFFIO_TX_B117h	DIFFOUT_B117h	AU13	DQ16B	DQ7B	DQ3B	DM2_4C
ıc.	VREFB4CN0 VREFB4CN0	io.	 	+	DIFFIO_TX_B117p	DIFFOUT_B118n	AE16	DQSn16B/QK16B	DQSn7B/QK7B	DQ3B	DQS#2_4C
4C	VREFB4CN0	10			DIFFIO_RX_B118b	DIFFOUT B118p	AF15	DQS16B/CQ16B/CQn16B/QKn16B	DQS7B/CQ7B/CQn7B/QKn7B	DQ3B	DQS2_4C
4C	VREFB4CN0	IO			DIFFIO_TX_B119n	DIFFOUT_B119n	AK14				_ 402_10
4C	VREFB4CN0	IO			DIFFIO_TX_B119p	DIFFOUT_B119p	AL14	DQ16B	DQ7B	DQ3B	DQ2_4C_5
4C	VREFB4CN0	IO			DIFFIO_RX_B120n	DIFFOUT_B120n	AN14	DQ16B	DQ7B	DQ3B	DQ2_4C_4
4C	VREFB4CN0	10			DIFFIO_RX_B120p	DIFFOUT_B120p	AP14	DQ16B	DQ7B	DQ3B	DQ2_4C_3
4C	VREFB4CN0	10			DIFFIO_TX_B121n	DIFFOUT_B121n	AG14				
4C	VREFB4CN0	10			DIFFIO_TX_B121p	DIFFOUT_B121p	AH14	DQ16B	DQ7B	DQ3B	DQ2_4C_2
4C	VREFB4CN0	IO			DIFFIO_RX_B122n	DIFFOUT_B122n	AD15	DQ16B	DQ7B	DQ3B	DQ2_4C_1
4C	VREFB4CN0	10			DIFFIO_RX_B122p	DIFFOUT_B122p	AE15	DQ16B	DQ7B	DQ3B	DQ2_4C_0
4B	VREFB4BN0	10			DIFFIO_TX_B123n	DIFFOUT_B123n	AP13				
4B	VREFB4BN0	10			DIFFIO_TX_B123p	DIFFOUT_B123p	AR13	DQ17B	DQ8B	DQ3B	DQ3_4B_8
4B	VREFB4BN0	10			DIFFIO_RX_B124n	DIFFOUT_B124n DIFFOUT_B124n	AE14	DQ17B	DQ8B	DQ3B	DQ3_4B_7
4B	VREFB4BN0	10			DIFFIO_RX_B124p		AE13	DQ17B	DQ8B	DQ3B	DQ3_4B_6
4B	VREFB4BN0 VRFFB4BN0	10			DIFFIO_TX_B125n DIFFIO_TX_B125p	DIFFOUT_B125n DIFFOUT_B125p	AT12 AU12	DQ17B	DO8B	DO3B	DM3 4B
4D	VREFB4BN0	10			DIFFIO_TX_B125p	DIFFOUT B126n	AV12	DQSn17B/QK17B	DQ8B	DQSn3B/QK3B	DQS#3_4B
4B	VREFB4BN0	10			DIFFIO RX B126n	DIFFOUT B126n	AW 12	DQS17B/CQ17B/CQn17B/QKn17B	DQ8B	DQS3B/CQ3B/CQn3B/QKn3B	DQS3_4B
4B	VREFB4BN0	10			DIFFIO_TX_B127n	DIFFOUT_B127n	AL13	DQ017B/CQ17B/CQ117B/QR117B	DQOB	DQ03B/CQ3B/CQ13B/Q1113B	DQ03_4D
4B	VREFB4BN0	IO			DIFFIO_TX_B127p	DIFFOUT_B127p	AM13	DQ17B	DQ8B	DQ3B	DQ3 4B 5
4B	VREFB4BN0	10			DIFFIO_RX_B128n	DIFFOUT_B128n	AW 10	DQ17B	DQ8B	DQ3B	DQ3_4B_4
4B	VREFB4BN0	10			DIFFIO_RX_B128p	DIFFOUT_B128p	AW 11	DQ17B	DQ8B	DQ3B	DQ3_4B_3
4B	VREFB4BN0	10			DIFFIO_TX_B129n	DIFFOUT_B129n	AN12				
4B	VREFB4BN0	10			DIFFIO_TX_B129p	DIFFOUT_B129p	AP12	DQ17B	DQ8B	DQ3B	DQ3_4B_2
4B	VREFB4BN0	10			DIFFIO_RX_B130n	DIFFOUT_B130n	AH13	DQ17B	DQ8B	DQ3B	DQ3_4B_1
1B	VREFB4BN0	10			DIFFIO_RX_B130p	DIFFOUT_B130p	AJ13	DQ17B	DQ8B	DQ3B	DQ3_4B_0
4B	VREFB4BN0	IO			DIFFIO_TX_B131n	DIFFOUT_B131n	AH12				
4B	VREFB4BN0	10			DIFFIO_TX_B131p	DIFFOUT_B131p	AJ12	DQ18B	DQ8B	DQ3B	DQ4_4B_8
1B	VREFB4BN0 VREFB4BN0	10			DIFFIO_RX_B132n DIFFIO_RX_B132p	DIFFOUT_B132n DIFFOUT_B132p	AF13 AG13	DQ18B DQ18B	DQ8B DQ8B	DQ3B DQ3B	DQ4_4B_7 DQ4_4B_6
ib		10					AU10	DQ18B	DQ8B	DQ3B	DQ4_4B_6
4D	VREFB4BN0 VREFB4BN0	10			DIFFIO_TX_B133n DIFFIO_TX_B133p	DIFFOUT_B133n DIFFOUT_B133p	AV10	DO18B	DO8B	DQ3B	DM4_4B
IR	VREFB4BN0 VREFB4BN0	10	1	1	DIFFIO_TX_B133p	DIFFOUT_B133p	AV10 AT11	DQSn18B/QK18B	DQSn8B/QK8B	DQ3B DQ3B	DOS#4_4B
1B	VREFB4BN0	lio	1	1	DIFFIO_RX_B134n	DIFFOUT_B134p	AU11	DQS18B/CQ18B/CQn18B/QKn18B	DQS8B/CQ8B/CQn8B/QKn8B	DQ3B	DQS4_4B
1B			•							· · · · -	
	VREFB4BN0	IO			DIFFIO_TX_B135n	DIFFOUT_B135n	AK12				
1B	VREFB4BN0 VREFB4BN0	10			DIFFIO_TX_B135n DIFFIO_TX_B135p			DQ18B	DQ8B	DQ3B	DQ4_4B_5
4B 4B	VIKEI DIDITO	10 10 10			DILLIO_IX_DIGGII	DIFFOUT_B135n	AK12		DQ8B DQ8B	DQ3B DQ3B	DQ4_4B_4
1B 1B 1B	VREFB4BN0 VREFB4BN0 VREFB4BN0	10 10 10			DIFFIO_TX_B135p	DIFFOUT_B135n DIFFOUT_B135p	AK12 AL12 AC13 AD13	DQ18B			
4B 4B 4B	VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0	10 10 10	VREFB4BN0		DIFFIO_TX_B135p DIFFIO_RX_B136n	DIFFOUT_B135n DIFFOUT_B135p DIFFOUT_B136n	AK12 AL12 AC13 AD13 AN11	DQ18B DQ18B DQ18B	DQ8B DQ8B	DQ3B DQ3B	DQ4_4B_4 DQ4_4B_3
1B 1B 1B	VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0	10 10 10 10	VREFB48N0		DIFFIO_TX_B135p DIFFIO_RX_B136n DIFFIO_RX_B136p	DIFFOUT_B135n DIFFOUT_B135p DIFFOUT_B136n DIFFOUT_B136p	AK12 AL12 AC13 AD13 AN11 AP11	DQ18B DQ18B DQ18B DQ18B	DQ8B DQ8B DQ8B	DQ3B DQ3B DQ3B	DQ4_4B_4 DQ4_4B_3 DQ4_4B_2
1B 1B 1B	VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0	10 10 10 10	VREFB4BN0		DIFFIO_TX_B135p DIFFIO_RX_B136n DIFFIO_RX_B136p	DIFFOUT_B135n DIFFOUT_B135p DIFFOUT_B136n DIFFOUT_B136p DIFFOUT_B137n	AK12 AL12 AC13 AD13 AN11 AP11 AV9	DQ18B DQ18B DQ18B DQ18B DQ18B	DQ8B DQ8B DQ8B DQ8B	DQ3B DQ3B DQ3B DQ3B	DQ4_4B_4 DQ4_4B_3 DQ4_4B_2 DQ4_4B_1
18 18 18 18 18	VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0	IC	VREFB48N0		DIFFIO TX_B135p DIFFIO_RX_B136n DIFFIO_RX_B136p DIFFIO_RX_B137n DIFFIO_RX_B137n	DIFFOUT_B135n DIFFOUT_B135p DIFFOUT_B136n DIFFOUT_B136p DIFFOUT_B137n DIFFOUT_B137n	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9	DQ18B DQ18B DQ18B DQ18B	DQ8B DQ8B DQ8B	DQ3B DQ3B DQ3B	DQ4_4B_4 DQ4_4B_3 DQ4_4B_2
18 18 18 18 18	VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0	IC	VREFB4BN0		DIFFIO_TX_B135p DIFFIO_RX_B136n DIFFIO_RX_B136p DIFFIO_RX_B137n DIFFIO_RX_B137p DIFFIO_TX_B138n	DIFFOUT_B135n DIFFOUT_B135p DIFFOUT_B136n DIFFOUT_B136p DIFFOUT_B137n DIFFOUT_B137n DIFFOUT_B138n	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12	D018B D018B D018B D018B D018B D018B D018B	DQ8B DQ8B DQ8B DQ8B DQ8B	DQ3B DQ3B DQ3B DQ3B DQ3B	DQ4_4B_3 DQ4_4B_2 DQ4_4B_1 DQ4_4B_0
4B 4B 4B 4B 4B 4B 4B	VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0	IC	VREFB4BN0		DIFFIO_TX_B135p DIFFIO_RX_B136n DIFFIO_RX_B136p DIFFIO_RX_B137n DIFFIO_RX_B137p DIFFIO_RX_B137p DIFFIO_TX_B138n DIFFIO_TX_B138p	DIFFOUT_B135n DIFFOUT_B135p DIFFOUT_B136p DIFFOUT_B136p DIFFOUT_B137n DIFFOUT_B137n DIFFOUT_B138n DIFFOUT_B138n	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12 AD11	D0188 D0188 D0188 D0188 D0188 D0188 D0188 D0188	DQ8B DQ9B DQ8B DQ8B DQ8B DQ8B DQ8B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ4_4B_3 DQ4_4B_2 DQ4_4B_1 DQ4_4B_0 DQ5_4B_8
4B 4B 4B 4B 4B 4B 4B	VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0	IC	VREFB4BN0		DIFFIO_TX_B135p DIFFIO_RX_B136n DIFFIO_RX_B136n DIFFIO_RX_B136p DIFFIO_RX_B137n DIFFIO_RX_B137n DIFFIO_TX_B138n DIFFIO_TX_B138p DIFFIO_TX_B138p	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136p DIFFOUT B136p DIFFOUT B137n DIFFOUT B137n DIFFOUT B137p DIFFOUT B138n DIFFOUT B138n DIFFOUT B138p DIFFOUT B138p	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12 AD11 AF12	DQ18B DQ18B DQ18B DQ18B DQ18B DQ18B DQ18B DQ18B DQ18B DQ19B DQ19B	DQ8B DQ8B DQ8B DQ8B DQ8B DQ8B DQ9B DQ9B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B	DQ4_4B_3 DQ4_4B_2 DQ4_4B_1 DQ4_4B_0 DQ5_4B_8 DQ5_4B_7
4B 4B 4B 4B 4B 4B 4B	VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0 VREFB4BN0	IC	VREFB4BN0		DIFFIO TX B135p DIFFIO RX B136n DIFFIO RX B136n DIFFIO RX B137n DIFFIO RX B137n DIFFIO TX B138n DIFFIO TX B138n DIFFIO TX B138n DIFFIO RX B139n DIFFIO RX B139n	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136p DIFFOUT B136p DIFFOUT B137n DIFFOUT B137n DIFFOUT B137p DIFFOUT B138p DIFFOUT B138p DIFFOUT B138p DIFFOUT B139p DIFFOUT B139p	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12 AD11 AF12 AG12	D0188 D0188 D0188 D0188 D0188 D0188 D0188 D0188	DQ8B DQ9B DQ8B DQ8B DQ8B DQ8B DQ8B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B	DQ4_4B_3 DQ4_4B_2 DQ4_4B_1 DQ4_4B_0 DQ5_4B_8
4B 4B 4B 4B 4B 4B 4B	VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO	IC	VREFB4BN0		DIFFIO TX_B13Sp DIFFIO RX_B13Sn DIFFIO RX_B13Sn DIFFIO RX_B13Sn DIFFIO RX_B137n DIFFIO TX_B138n DIFFIO TX_B138n DIFFIO RX_B139n DIFFIO RX_B139n DIFFIO TX_B139p	DIFFOUT B135n DIFFOUT B135p DIFFOUT B135p DIFFOUT B136p DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B139n DIFFOUT B139n DIFFOUT B139n	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12 AD11 AF12 AG12 AT9	D0188 D0188 D0188 D0188 D0188 D0188 D0188 D0188 D0188 D0198 D0198	DQ8B DQ8B DQ8B DQ8B DQ8B DQ8B DQ9B DQ9B DQ9B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B	DQ4 4B 4 DQ4 4B 3 DQ4 4B 2 DQ4 4B 1 DQ4 4B 0 DQ5 4B 8 DQ5 4B 8 DQ5 4B 6
4B 4B 4B 4B 4B 4B 4B 4B 4B 4B	VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO VREFB4BNO	IC	VREFB4BN0		DIFFIO TX B13Sp DIFFIO RX B136n DIFFIO RX B136p DIFFIO RX B137n DIFFIO RX B137n DIFFIO RX B137n DIFFIO TX B138n DIFFIO TX B138n DIFFIO RX B139n DIFFIO RX B139n DIFFIO RX B139n DIFFIO TX B140n	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136p DIFFOUT B136p DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138p DIFFOUT B139n DIFFOUT B139n DIFFOUT B139n DIFFOUT B139n DIFFOUT B139n DIFFOUT B140n	AK12 AL12 AC13 AD13 AD11 AP11 AV9 AW9 AC12 AD11 AF12 AG12 AG12 AT9 AU9	D018B D018B D018B D018B D018B D018B D018B D018B D018B D019B D019B D019B D019B	OQ88 DQ8B DQ8B DQ8B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B DQ4B	DQ4_4B_4 DQ4_4B_2 DQ4_4B_1 DQ4_4B_1 DQ4_4B_0 DQ5_4B_8 DQ5_4B_7 DQ5_4B_6 DM5_4B
4B 4B 4B 4B 4B 4B 4B 4B 4B 4B	VREFB4BNO VREFB4BNO	IC	VREFB4BN0		DIFFIO TX, B13Sp DIFFIO, RX, B13Sn DIFFIO, RX, B13Sn DIFFIO, RX, B137n DIFFIO RX, B137n DIFFIO TX, B13Sn DIFFIO, TX, B13Sn DIFFIO, RX, B13Sn DIFFIO, RX, B13Sn DIFFIO, RX, B13Sn DIFFIO, RX, B13Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn DIFFIO, TX, B14Sn	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136p DIFFOUT B136p DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B139n DIFFOUT B139n DIFFOUT B140n DIFFOUT B140p DIFFOUT B140p DIFFOUT B140p	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12 AD11 AF12 AG12 AG12 AU9 AU9 AU9	D018B D018B D018B D018B D018B D018B D018B D018B D018B D019B D019B D019B D019B D019B D019B D019B	DQ8B DQ9B DQ8B DQ8B DQ8B DQ8B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B DQ4B DQ4B	DQ4_4B_4 DQ4_4B_2 DQ4_4B_1 DQ4_4B_0 DQ5_4B_8 DQ5_4B_8 DQ5_4B_7 DQ5_4B_6 DQ5_4B_6 DQ5_4B_6 DQ5_4B_6
18	VREFB4BNO VREFB4BNO	Color Colo	VREFB4BN0		DIFFIO TX B135p DIFFIO RX B136p DIFFIO RX B136p DIFFIO RX B137p DIFFIO RX B137p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B140p DIFFIO RX B140p DIFFIO RX B1410p DIFFIO RX B1410p DIFFIO RX B1410p	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136n DIFFOUT B136n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B139n DIFFOUT B149n DIFFOUT B149n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B141n DIFFOUT B141n	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12 AG11 AF12 AG12 AT9 AU9 AU9 AU9 AU9 AU9 AU9 AU9 AU	D018B D018B D018B D018B D018B D018B D018B D018B D018B D019B D019B D019B D019B	OQ88 DQ8B DQ8B DQ8B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B DQ4B	DQ4_4B_4 DQ4_4B_2 DQ4_4B_1 DQ4_4B_1 DQ4_4B_0 DQ5_4B_8 DQ5_4B_7 DQ5_4B_6 DM5_4B
18	VREFB4BNO VREFB4BNO	Color Colo	VREFB4BN0		DIFFIO TX B135p DIFFIO RX B136n DIFFIO RX B136n DIFFIO RX B136n DIFFIO RX B137n DIFFIO RX B137n DIFFIO TX B138n DIFFIO TX B138n DIFFIO TX B138n DIFFIO TX B138n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B140n DIFFIO TX B141n DIFFIO RX B141n DIFFIO RX B141n DIFFIO RX B141n DIFFIO RX B141n DIFFIO RX B141n DIFFIO RX B141n DIFFIO RX B141n DIFFIO RX B142n	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136p DIFFOUT B136p DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B139b DIFFOUT B139b DIFFOUT B140n DIFFOUT B140n DIFFOUT B141n DIFFOUT B141n	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AC12 AD11 AF12 AG12 AG12 AG11 AF12 AG11 AF12 AG11 AG11 AG11 AG11 AG11 AG11 AG11 AG	D0188 D0188 D0188 D0188 D0188 D0188 D0188 D0188 D0198 D0198 D0198 D0198 D0198 D0198 D0198 D0198 D0198	DQ88 DQ88 DQ88 DQ88 DQ88 DQ98 DQ98 DQ98	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B DQ4B DQ4B	DQ4 4B 4 DQ4 4B 3 DQ4 4B 1 DQ4 4B 1 DQ4 4B 1 DQ4 4B 0 DQ5 4B 7 DQ5 4B 6 DQ5 4B 6 DQ5 4B 6 DQ5 4B 6
18	VREFB4BNO VREFB4BNO	Color Colo	VREFB4BN0		DIFFIO TX B135p DIFFIO RX B136p DIFFIO RX B136p DIFFIO RX B137p DIFFIO RX B137p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B140p DIFFIO RX B140p DIFFIO RX B1410p DIFFIO RX B1410p DIFFIO RX B1410p	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136n DIFFOUT B136n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B139n DIFFOUT B149n DIFFOUT B149n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B141n DIFFOUT B141n	AK12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12 AG11 AF12 AG12 AT9 AU9 AU9 AU9 AU9 AU9 AU9 AU9 AU	D018B D018B D018B D018B D018B D018B D018B D018B D018B D019B D019B D019B D019B D019B D019B D019B	DQ8B DQ9B DQ8B DQ8B DQ8B DQ8B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9B	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4B	DQ4_4B_4 DQ4_4B_2 DQ4_4B_1 DQ4_4B_0 DQ5_4B_8 DQ5_4B_8 DQ5_4B_7 DQ5_4B_6 DQ5_4B_6 DQ5_4B_6 DQ5_4B_6
4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B	VREFB4BNO VREFB4BNO	Color Colo	VREFB4BN0		DIFFIO TX B135p DIFFIO RX B136p DIFFIO RX B136p DIFFIO RX B136p DIFFIO RX B137p DIFFIO RX B137p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO RX B139p DIFFIO RX B139p DIFFIO RX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B141p DIFFIO TX B141p DIFFIO TX B142p	DIFFOUT B135n DIFFOUT B135p DIFFOUT B135p DIFFOUT B136n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B139n DIFFOUT B149n DIFFOUT B149n DIFFOUT B140n DIFFOUT B140n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B142n DIFFOUT B142n	AK12 AL12 AC13 AC13 AN11 AP11 AV9 AC9 AC12 AD11 AF12 AG12 AG11 AF12 AG11 AH11 AH11 AH11 AH11 AH11 AH11 AH11	D018B D018B D018B D018B D018B D018B D018B D018B D018B D019B	DQ8B DQ8B DQ8B DQ8B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9B DQ9	DO3B DO3B DO3B DO3B DO3B DO3B DO3B DO4B DO4B DO4B DO4B DO4B DO4B DO4B DO4	DO4, 4B 4 DO4 4B 3 DO4, 4B 2 DO4, 4B 1 DO4, 4B 1 DO4, 4B 0 DO5, 4B 8 DO5, 4B 7 DO5, 4B 6 DOS, 4B 6 DOS, 4B 6 DOS, 4B 7 DOS, 4B 6 DOS, 4B 7 DOS, 4B 6 DOS, 4B 7 DOS, 4B 6
4B 4B 4B 4B 4B 4B 4B	VREFB4BNO VREFB4BNO	Color Colo	VREFB4BN0		DIFFIO TX B13Sp DIFFIO RX B13Sp DIFFIO RX B13Sp DIFFIO RX B13Fp DIFFIO RX B137n DIFFIO RX B137n DIFFIO RX B137n DIFFIO RX B137n DIFFIO TX B13Sp DIFFIO TX B13Sp DIFFIO TX B13Sp DIFFIO TX B140p DIFFIO TX B140p DIFFIO RX B141p DIFFIO RX B141p DIFFIO RX B141p DIFFIO RX B141p DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n DIFFIO TX B142n	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136p DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B139n DIFFOUT B149n DIFFOUT B149n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B140n DIFFOUT B141n DIFFOUT B141n DIFFOUT B142n DIFFOUT B142n DIFFOUT B1438n	AK12 AL12 AC13 AC13 AD13 AN11 AP11 AP11 AV9 AC12 AD11 AF12 AF12 AF12 AF14 AF14 AF14 AF15 AF15 AF17 AF17 AF17 AF17 AF17 AF17 AF17 AF17	D018B D018B D018B D018B D018B D018B D018B D018B D018B D018B D019B D019B D019B D039B D019B	OQ88 DQ88 DQ88 DQ88 DQ98 DQ98 DQ98 DQ98 D	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4	DO4 48 4 DO4 48 3 DO4 48 2 DO4 48 1 DO4 48 1 DO4 48 0 DO5 48 7 DO5 48 7 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6
4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B	VREFB4BNO VREFB4BNO	Color Colo	VREFB46N0		DIFFIO TX B135p DIFFIO RX B136p DIFFIO RX B136p DIFFIO RX B137n DIFFIO RX B137n DIFFIO RX B137p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO RX B138p DIFFIO RX B138p DIFFIO RX B138p DIFFIO RX B138p DIFFIO RX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO RX B141p DIFFIO RX B141p DIFFIO RX B141p DIFFIO RX B142p DIFFIO RX B143p DIFFIO RX B143p DIFFIO RX B143p DIFFIO RX B143p DIFFIO TX B143p DIFFIO TX B143p DIFFIO TX B143p DIFFIO TX B143p	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136p DIFFOUT B136p DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B139n DIFFOUT B140n DIFFOUT B140n DIFFOUT B141n DIFFOUT B141n DIFFOUT B141n DIFFOUT B142n DIFFOUT B142n DIFFOUT B142n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B143n DIFFOUT B144n	AK12 AL12 AL12 AL12 AC13 AD13 AN11 AP11 AV9 AW9 AC12 AD11 AF12 AG12 AG12 AT19 AU9 AU9 AU9 AU9 AU9 AU9 AU9 AU9 AU9 AU	D018B D018B D018B D018B D018B D018B D018B D018B D018B D018B D019B D019B D019B D039B D019B	OQ88 DQ88 DQ88 DQ88 DQ98 DQ98 DQ98 DQ98 D	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4	DO4 48 4 DQ4 48 3 DO4 48 2 DO4 48 1 DQ4 48 1 DQ4 48 0 DQ5 48 6 DQ5 48 7 DQ5 48 6 DM5
4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B 4B	VREFB4BNO VREFB4BNO	Color Colo	VREFB4BN0		DIFFIO TX B135p DIFFIO RX B136p DIFFIO RX B136p DIFFIO RX B137p DIFFIO RX B137p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO TX B138p DIFFIO RX B139p DIFFIO RX B139p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B140p DIFFIO TX B141p DIFFIO TX B142p DIFFIO TX B142p DIFFIO TX B143p DIFFIO TX B143p DIFFIO TX B143p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p DIFFIO TX B144p	DIFFOUT B135n DIFFOUT B135p DIFFOUT B136n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B137n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B138n DIFFOUT B140n	AK12 AL12 AL12 AC13 AD13 AN11 AP11 AP11 AP11 AF12 AG12 AG12 AG12 AT9 AU9 AG11 AH11 AH11 AH11 AH11 AH11 AF12 AF12 AF12 AF12 AF12 AF10 AK11 AK11 AK11 AK11	D018B D018B D018B D018B D018B D018B D018B D018B D018B D018B D019B D019B D019B D019B D019B D0519B/C019B/C019B/CM19B D0519B/C019B/CM19B D019B D019B D019B	DQ88 DQ88 DQ88 DQ88 DQ98 DQ98 DQ98 DQ98	DQ3B DQ3B DQ3B DQ3B DQ3B DQ3B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4B DQ4	DO4 48 4 DO4 48 2 DO4 48 2 DO4 48 1 DO4 48 1 DO5 48 1 DO5 48 7 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 6 DO5 48 5 DO5 48 5 DO5 48 5 DO5 48 5 DO5 48 3



											Note (1
lank lumber		PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
A	VREFB4AN0	10			DIFFIO_TX_B146n	DIFFOUT_B146n	AL9				
A	VREFB4AN0	Ю			DIFFIO_TX_B146p	DIFFOUT_B146p	AM9	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	IO			DIFFIO_RX_B147n	DIFFOUT_B147n	AW7	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	10			DIFFIO_RX_B147p	DIFFOUT_B147p	AW8	DQ20B	DQ9B	DQ4B	
	VREFB4AN0	IO			DIFFIO_TX_B148n	DIFFOUT_B148n	AV7				
A	VREFB4AN0	10			DIFFIO_TX_B148p	DIFFOUT_B148p	AV6	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	IO			DIFFIO_RX_B149n	DIFFOUT_B149n	AW6	DQSn20B/QK20B	DQSn9B/QK9B	DQ4B	
A	VREFB4AN0	IO			DIFFIO_RX_B149p	DIFFOUT_B149p	AW5	DQS20B/CQ20B/CQn20B/QKn20B	DQS9B/CQ9B/CQn9B/QKn9B	DQ4B	
A	VREFB4AN0	IO			DIFFIO_TX_B150n	DIFFOUT_B150n	AK9				
A	VREFB4AN0	10			DIFFIO_TX_B150p	DIFFOUT_B150p	AK10	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	10			DIFFIO_RX_B151n	DIFFOUT_B151n	AU7	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	10			DIFFIO_RX_B151p	DIFFOUT_B151p	AU8	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	IO			DIFFIO_TX_B152n	DIFFOUT_B152n	AN9				
	VREFB4AN0	10			DIFFIO_TX_B152p	DIFFOUT_B152p	AP9	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	10			DIFFIO_RX_B153n	DIFFOUT_B153n	AT8	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	10			DIFFIO_RX_B153p	DIFFOUT_B153p	AR9	DQ20B	DQ9B	DQ4B	
A	VREFB4AN0	10		DATA10	DIFFIO_TX_B154n	DIFFOUT_B154n	AH10				
A	VREFB4AN0	10		DATA11	DIFFIO_TX_B154p	DIFFOUT_B154p	AJ10	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	IO		DATA5	DIFFIO_RX_B155n	DIFFOUT_B155n	AF10	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	10		DATA6	DIFFIO_RX_B155p	DIFFOUT_B155p	AE11	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	IO		DATA12	DIFFIO_TX_B156n	DIFFOUT_B156n	AK6				
A	VREFB4AN0	IO		DATA13	DIFFIO_TX_B156p	DIFFOUT_B156p	AL6	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	IO		DATA7	DIFFIO_RX_B157n	DIFFOUT_B157n	AH6	DQSn21B/QK21B	DQ10B	DQSn4B/QK4B	
A	VREFB4AN0	IO		DATA8	DIFFIO_RX_B157p	DIFFOUT_B157p	AJ6	DQS21B/CQ21B/CQn21B/QKn21B	DQ10B	DQS4B/CQ4B/CQn4B/QKn4B	
A	VREFB4AN0	IO		DATA14	DIFFIO_TX_B158n	DIFFOUT_B158n	AH9				
A	VREFB4AN0	IO		DATA15	DIFFIO_TX_B158p	DIFFOUT_B158p	AJ9	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	IO		DATA9	DIFFIO_RX_B159n	DIFFOUT_B159n	AM6	DQ21B	DQ10B	DQ4B	
	VREFB4AN0	IO		CLKUSR	DIFFIO_RX_B159p	DIFFOUT_B159p	AN6	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	Ю	VREFB4AN0				AH7			<u> </u>	
A	VREFB4AN0	10					AH8	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	10	CLK11n		DIFFIO_RX_B160n	DIFFOUT_B160n	AJ7	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	10	CLK11p		DIFFIO_RX_B160p	DIFFOUT_B160p	AK7	DQ21B	DQ10B	DQ4B	
A	VREFB4AN0	10	FPLL_BR_CLKOUT1,FPLL_BR_CLKOUTn		DIFFIO_TX_B161n	DIFFOUT_B161n	AL7				
A	VREFB4AN0	10	FPLL_BR_CLKOUT0,FPLL_BR_CLKOUTp,FPLL_BR_FB0		DIFFIO_TX_B161p	DIFFOUT_B161p	AM7	DQ22B	DQ10B	DQ4B	
A	VREFB4AN0	10	FPLL BR CLKOUT3.FPLL BR FBn		DIFFIO RX B162n	DIFFOUT B162n	AN8	DQ22B	DQ10B	DQ4B	
A	VREFB4AN0	10	FPLL_BR_CLKOUT2,FPLL_BR_FBp,FPLL_BR_FB1		DIFFIO_RX_B162p	DIFFOUT B162p	AP8	DQ22B	DQ10B	DQ4B	-
A	VREFB4AN0	10			DIFFIO_TX_B163n	DIFFOUT B163n	AT6				-
A	VREFB4AN0	IO			DIFFIO_TX_B163p	DIFFOUT_B163p	AU6	DQ22B	DQ10B	DQ4B	+
A	VRFFB4AN0	10	CLK10n		DIFFIO_RX_B164n	DIFFOUT B164n	AR7	DQSn22B/QK22B	DQSn10B/QK10B	DQ4B	+
A	VREFB4AN0	IO	CLK10p		DIFFIO_RX_B164p	DIFFOUT_B164p	AT7	DQS22B/CQ22B/CQn22B/QKn22B	DQS10B/CQ10B/CQn10B/QKn10B	DQ4B	+
A	VRFFB4AN0	10			DIFFIO TX B165n	DIFFOUT B165n	AK8				-
A	VREFB4AN0	10			DIFFIO_TX_B165p	DIFFOUT_B165p	AL8	DQ22B	DQ10B	DQ4B	-
A	VREFB4AN0	IO.	CLK9n		DIFFIO RX B166n	DIFFOUT B166n	AV4	DQ22B	DQ10B	DQ4B	-
A	VREFB4AN0	10	CLK9p		DIFFIO_RX_B166p	DIFFOUT_B166p	AW4	DQ22B	DQ10B	DQ4B	+
A	VREFB4AN0	10			DIFFIO_TX_B167n	DIFFOUT_B167n	AN7				+
A	VREFB4AN0	IO.	RZQ_1		DIFFIO_TX_B167p	DIFFOUT_B167p	AP7	DQ22B	DQ10B	DQ4B	-
A	VREFB4AN0	10	CLK8n		DIFFIO_RX_B168n	DIFFOUT_B168n	AP6	DQ22B	DQ10B	DQ4B	+
A	VREFB4AN0	10	CLK8p		DIFFIO_RX_B168p	DIFFOUT_B168p	AR6	DQ22B	DQ10B	DQ4B	-
		RREF_BR					AW2				-
		DNU			_		AV3				-
		DNU			_		AW3				-
SXB_R0		REFCLK0Rp			T		AF8				
SXB_R0		REFCLK0Rn	1								
SXB R0							AF7				+
		GXB_RX_R0n,GXB_REFCLK_R0n									+
XB_R0		GXB_RX_R0n,GXB_REFCLK_R0n GXB_RX_R0p,GXB_REFCLK_R0p					AF7				
SXB_R0 SXB_R0		GXB_RX_R0n,GXB_REFCLK_R0n GXB_RX_R0p,GXB_REFCLK_R0p GXB_TX_R0p					AF7 AU2				
SXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p GXB_TX_R0p					AF7 AU2 AU1				
		GXB_RX_R0p,GXB_REFCLK_R0p					AF7 AU2 AU1 AT3				
SXB_R0 SXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p GXB_TX_R0p GXB_TX_R0n					AF7 AU2 AU1 AT3 AT4				
SXB_R0 SXB_R0 SXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p GXB_TX_R0p GXB_TX_R0n GXB_RX_R1n,GXB_REFCLK_R1n					AF7 AU2 AU1 AT3 AT4 AR2				
SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0		GXB_RX_R0p,GXB_REFCLK_R0p GXB_TX_R0p GXB_TX_R0n GXB_RX_R1n,GXB_REFCLK_R1n GXB_RX_R1p,GXB_REFCLK_R1p GXB_TX_R1p					AF7 AU2 AU1 AT3 AT4 AR2 AR1				
SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0		GXB RX R0p,GXB_REFCLK_R0p GXB_TX_R0p GXB_TX_R0n GXB_RX_R1n,GXB_REFCLK_R1n GXB_RX_R1p,GXB_REFCLK_R1p GXB_TX_R1p GXB_TX_R1p GXB_TX_R1n					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4				
SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX, R0p GXB TX, R0n GXB RX, R1n,GXB REFCLK, R1n GXB RX, R1n,GXB REFCLK, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1n GXB RX, R2n,GXB REFCLK, R2n					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3				
SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0		GMB RX R0p.GMB REFCLK R0p GMB TX R0p GMB TX R0p GMB RX R1n,GMB REFCLK R1n GMB RX R1n,GMB REFCLK R1n GMB TX R1p,GMB REFCLK R1p GMB TX, R1p GMB TX, R1n GMB RX, R2n,GMB REFCLK R2n GMB TX, R1n GMB RX, R2n,GMB REFCLK R2n GMB RX, R2n,GMB REFCLK R2n					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1				
SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R0p GXB RX R1n.GXB REFCLK R1n GXB RX R1p.GXB REFCLK R1p GXB TX R1p GXB TX R1p GXB TX R1n GXB TX R1n GXB RX R2p.GXB REFCLK R2p GXB TX R7 GXB TX R1P GXB RX R2p.GXB REFCLK R2p GXB TX R2p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2				
SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX, R0p GXB TX, R0p GXB RX, R1n,GXB REFCLK R1n GXB RX, R1n,GXB REFCLK R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB RX, R2n,GXB REFCLK R2n GXB RX, R2n,GXB REFCLK R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1 AM3				
SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0 SXB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R0n GXB RX R1n.GXB REFCLK R1n GXB RX R1p.GXB REFCLK R1p GXB TX, R1p GXB TX, R1p GXB TX, R1n GXB RX R2n.GXB REFCLK R2n GXB RX R2n.GXB REFCLK R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1 AM3 AM4				
6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0 6XB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX, R0p GXB TX, R0p GXB, TX, R0n GXB, RX, R1n,GXB, REFCLK, R1n GXB, RX, R1n,GXB, REFCLK, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB TX, R2n,GXB, REFCLK, R2n GXB, RX, R2p,GXB, REFCLK, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R3p GXB REFCLK, R3p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1 AM3 AM4 AL2 AL1				
SXB_R0 SXB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R0n GXB RX R1n.GXB REFCLK R1n GXB RX R1p.GXB REFCLK R1p GXB TX, R1p GXB TX, R1p GXB TX, R1n GXB RX R2n.GXB REFCLK R2n GXB RX R2n.GXB REFCLK R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1 AM3 AM4 AL2				
EXB_R0 EXB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX, R0p GXB TX, R0n GXB RX, R1n,GXB REFCLK, R1n GXB RX, R1n,GXB REFCLK, R1n GXB TX, R1n GXB TX, R1n GXB TX, R1n GXB TX, R1n GXB TX, R2n,GXB REFCLK, R2n GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2n GXB RX, R3n,GXB REFCLK, R3n GXB RX, R3n,GXB REFCLK, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1 AM4 AL2 AL1 AK3 AK4 AK4				
SXB_R0 SXB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB RX R1n,GXB REFCLK R1n GXB RX R1n,GXB REFCLK R1n GXB RX R1p.GXB REFCLK R1p GXB TX, R1p GXB RX R2n,GXB REFCLK R2n GXB TX, R1n GXB RX R2n,GXB REFCLK R2n GXB RX R2n,GXB REFCLK R2n GXB RX R2n,GXB REFCLK R2n GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB RX R3n,GXB REFCLK R3n GXB RX R3n,GXB REFCLK R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p					AF7 AU2 AU1 AT3 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1 AM3 AM4 AL2 AL1 AK3 AK4 AK3 AK4 AJ2				
EXB_R0 EXB_R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R0n GXB RX R1n.GXB REFCLK R1n GXB RX R1p.GXB REFCLK R1p GXB TX, R1p GXB TX, R1p GXB TX, R1n GXB RX R2n.GXB REFCLK R2n GXB TX, R1n GXB RX R2p.GXB REFCLK R2n GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R3p GXB RX R3p.GXB REFCLK R3n GXB RX R3p.GXB REFCLK R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3n GXB RX, R3n,GXB REFCLK R4n GXB RX, R3n,GXB REFCLK R4n GXB RX, R3n,GXB REFCLK R4n GXB RX, R3n,GXB REFCLK R4n GXB RX, R3n,GXB REFCLK R4n GXB RX, R3n,GXB REFCLK R4n GXB RX, R4n,GXB REFCLK R4n GXB RX, R4n,GXB REFCLK R4n					AF7 AU2 AU1 AU3 AT3 AT4 AR2 AR1 AR2 AR1 AP3 AP4 AN2 AN4 AN4 AN5 AM4 AM3 AM4 AL2 AL1 AK3 AK4 AJ2 AJ1				
EXB R0 EXB R0		GMB RX R0p.GMB REFCLK R0p GMB TX R0p GMB TX R0p GMB RX R1n,GMB REFCLK R1n GMB RX R1n,GMB REFCLK R1n GMB RX R1p,GMB REFCLK R1p GMB TX, R1p GMB RX, R2n,GMB REFCLK R2p GMB TX, R1n GMB RX, R2n,GMB REFCLK R2n GMB TX, R2n GMB TX, R2n GMB TX, R2n GMB TX, R2n GMB TX, R2n GMB TX, R3n,GMB REFCLK R3n GMB TX, R3n,GMB REFCLK R3n GMB TX, R3p GMB TX, R4p GMB RX, R4p,GMB REFCLK, R4p GMB TX, R4p GMB TX, R4p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AR9 AR4 AR9 AR4 AR9 AN1 AM3 AM4 AL2 AL1 AL1 AK3 AK4 AJ2 AJ1 AH3				
EXB R0 EX		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R0n GXB RX R1n,GXB REFCLK R1n GXB RX R1p.GXB REFCLK R1p GXB TX, R1p GXB TX, R1p GXB RX R2n,GXB REFCLK R2n GXB TX, R1n GXB RX R2n,GXB REFCLK R2n GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R3n,GXB REFCLK R3p GXB TX, R4p GXB TX, R4p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AR9 AP4 AN2 AN1 AN1 AM3 AM4 AL1 AK3 AK4 AJ2 AJ1 AH3 AH3 AH4				
EXB. R0 EXB. R		GMB RX R0p.GMB REFCLK R0p GMB TX R0p GMB TX R0p GMB TX R1p GMB RX R1p.GMB REFCLK R1p GMB RX R1p.GMB REFCLK R1p GMB TX R1p.GMB REFCLK R1p GMB TX R1p GMB TX R1p GMB RX R2p.GMB REFCLK R2p GMB TX R1p GMB RX R2p.GMB REFCLK R2p GMB TX R2p GMB TX R2p GMB TX R2p GMB TX R2p GMB TX R2p GMB TX R2p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R3p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p GMB TX R4p					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP4 AP4 AN2 AN1 AM3 AM4 AL2 AL1 AK3 AK4 AJ2 AJ1 AH3 AH4 AG2				
EXB R0 EXB R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R1p GXB RX R1n,GXB REFCLK R1n GXB RX R1p.GXB REFCLK R1p GXB RX R1p.GXB REFCLK R2p GXB TX, R1p GXB RX R2n,GXB REFCLK R2n GXB TX, R1p GXB RX R2n,GXB REFCLK R2n GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB RX R3p,GXB REFCLK R3p GXB RX R3p,GXB REFCLK R3p GXB RX R3p,GXB REFCLK R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R4n GXB RX R4p,GXB REFCLK R4p GXB TX, R					AF7 AU2 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1 AM3 AM4 AL1 AK3 AK4 AJ2 AJ1 AJ3 AH4 AG2				
EXB R0 EXB R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R0n GXB RX R1n.GXB REFCLK R1n GXB RX R1n.GXB REFCLK R1p GXB TX R1n GXB TX R1n GXB RX R2n.GXB REFCLK R2p GXB TX R1n GXB RX R2p.GXB REFCLK R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R2p GXB TX R3n GXB RX R3n.GXB REFCLK R3n GXB RX R3n.GXB REFCLK R3n GXB RX R3n.GXB REFCLK R3n GXB RX R3n.GXB REFCLK R3n GXB TX R3n GXB RX R3n.GXB REFCLK R4n GXB TX R3p GXB TX R3n GXB RX R4n.GXB REFCLK R4n GXB TX R4p GXB TX R5p.GXB REFCLK R5p					AF7 AU2 AU1 AT3 AU4 AT4 AR2 AR1 AP3 AP4 AN2 AN4 AN2 AN4 AN4 AN4 AN4 AN4 AL2 AL1 AL1 AL1 AL3 AK4 AJ1 AH3 AH4 AG2 AG1 AF3				
EXB R0 EXB R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R1p GXB RX R1n,GXB REFCLK R1n GXB RX R1p,GXB REFCLK R1p GXB TX, R1p GXB TX, R1p GXB RX R1p,GXB REFCLK R2p GXB TX, R1p GXB RX, R2p,GXB REFCLK R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R3p,GXB REFCLK R3p GXB TX, R3p,GXB REFCLK R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R4p GXB					AF7 AU2 AU1 AT3 AU1 AT3 AT4 AR2 AR1 AR9 AP3 AP4 AN1 AM3 AM4 AM4 AU2 AL1 AK3 AK4 AJ2 AL1 AH3 AH4 AH4 AG2 AG1 AF3 AF3 AF3 AF4				
EXB R0 EX		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R0n GXB RX R1n,GXB REFCLK R1n GXB RX R1p.GXB REFCLK R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB TX, R1p GXB RX R2n,GXB REFCLK R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R3p GXB REFCLK R3p GXB RX R3p,GXB REFCLK R3p GXB TX, R3p					AF7 AU2 AU1 AT3 AU1 AT3 AT4 AR2 AR1 AP3 AP4 AN2 AN1 AM3 AM4 AM4 AU2 AU1 AM3 AM4 AU1 AM3 AM4 AU2 AU1 AM3 AM4 AU2 AU1 AM4 AU2 AU1 AU2 AU1 AU3 AU4 AU4 AU4 AU5 AU4 AU4 AU6 AU6 AU7 AU7 AU7 AU7 AU7 AU7 AU7 AU7 AU7 AU7				
EXB R0 EXB R0		GXB RX R0p.GXB REFCLK R0p GXB TX R0p GXB TX R0p GXB TX R1p GXB RX R1n,GXB REFCLK R1n GXB RX R1p,GXB REFCLK R1p GXB TX, R1p GXB TX, R1p GXB RX R1p,GXB REFCLK R2p GXB TX, R1p GXB RX, R2p,GXB REFCLK R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R2p GXB TX, R3p,GXB REFCLK R3p GXB TX, R3p,GXB REFCLK R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R3p GXB TX, R4p GXB					AF7 AU2 AU1 AT3 AU1 AT3 AT4 AR2 AR1 AR9 AP3 AP4 AN1 AM3 AM4 AM4 AU2 AL1 AK3 AK4 AJ2 AL1 AH3 AH4 AH4 AG2 AG1 AF3 AF3 AF3 AF4				



											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
GXB_R1		GXB_RX_R6n,GXB_REFCLK_R6n					AE2			1	1111 (3)
GXB_R1		GXB RX R6p,GXB REFCLK R6p					AE1				
GXB_R1		GXB_TX_R6p					AD3				
GXB_R1		GXB_TX_R6n					AD4				
GXB_R1		GXB_RX_R7n,GXB_REFCLK_R7n					AC2			<u> </u>	<u> </u>
GXB_R1		GXB_RX_R7p,GXB_REFCLK_R7p					AC1			<u> </u>	
GXB_R1		GXB_TX_R7p					AB3			 	+
GXB_R1 GXB_R1	-	GXB_TX_R7n GXB_RX_R8n.GXB_REFCLK_R8n		+			AB4 AA2			+	+
GXB_R1		GXB_RX_R8p,GXB_REFCLK_R8p					AA1			 	+
GXB_R1		GXB_TX_R8p					Y3			-	+
GXB_R1		GXB_TX_R8n					Y4				1
GXB_R1		GXB_RX_R9n,GXB_REFCLK_R9n					W2				1
GXB_R1		GXB_RX_R9p,GXB_REFCLK_R9p					W1				1
GXB_R1		GXB_TX_R9p					V3				1
GXB_R1		GXB_TX_R9n					V4				
GXB_R1		GXB_RX_R10n,GXB_REFCLK_R10n					U2			<u> </u>	
GXB_R1		GXB_RX_R10p,GXB_REFCLK_R10p					U1				<u> </u>
GXB_R1		GXB_TX_R10p					T3			<u> </u>	
GXB_R1		GXB_TX_R10n					T4				
GXB_R1 GXB_R1	1	GXB_RX_R11n,GXB_REFCLK_R11n		1	 		R2 R1			+	+
GXB_R1 GXB_R1	1	GXB_RX_R11p,GXB_REFCLK_R11p GXB_TX_R11p		 	 		K1	 		 	+
GXB_R1	1	GXB_TX_R11n	1	†	 	l	P3	 		+	+
GXB_R1 GXB_R1		REFCLK3Rp	1	†	 	l	Y9	 		+	+
GXB_R1		REFCLK3Rn	1	1	1		19 Y8			 	+
GXB_R2		REFCLK4Rp			1		V9			1	1
GXB_R2		REFCLK4Rn			1		V8			1	1
GXB_R2		GXB_RX_R12n,GXB_REFCLK_R12n		İ	i e		N2				1
GXB_R2		GXB_RX_R12p,GXB_REFCLK_R12p					N1				
GXB_R2		GXB_TX_R12p					M3				
GXB_R2		GXB_TX_R12n					M4				1
GXB_R2		GXB_RX_R13n,GXB_REFCLK_R13n					L2				
GXB_R2		GXB_RX_R13p,GXB_REFCLK_R13p					L1				
GXB_R2		GXB_TX_R13p					K3				
GXB_R2		GXB_TX_R13n					K4			<u> </u>	<u> </u>
GXB_R2		GXB_RX_R14n,GXB_REFCLK_R14n					J2				
GXB_R2		GXB_RX_R14p,GXB_REFCLK_R14p					J1				4
GXB_R2		GXB_TX_R14p					H3				
GXB_R2 GXB_R2	-	GXB_TX_R14n GXB_RX_R15n,GXB_REFCLK_R15n		+			H4 G2			+	+
GXB_R2 GXB_R2	-	GXB_RX_R15n,GXB_REFCLK_R15n GXB_RX_R15p,GXB_REFCLK_R15p		+			G2 G1			+	+
GXB_R2		GXB_TX_R15p,GXB_REFCER_R15p					F3			 	+
GXB_R2		GXB_TX_R15n					F4			 	+
GXB_R2		GXB_RX_R16n,GXB_REFCLK_R16n					F2				+
GXB_R2		GXB_RX_R16p,GXB_REFCLK_R16p					E1				1
GXB_R2		GXB_TX_R16p					D3				1
GXB_R2		GXB_TX_R16n					D4				1
GXB_R2		GXB_RX_R17n,GXB_REFCLK_R17n GXB_RX_R17p,GXB_REFCLK_R17p					C2				1
GXB_R2		GXB_RX_R17p,GXB_REFCLK_R17p					C1				
GXB_R2		GXB_TX_R17p					B3				
GXB_R2	1	GXB_TX_R17n		ļ	ļ		B4	ļ			
GXB_R2		REFCLK5Rp		 	ļ		T9			<u> </u>	
GXB_R2		REFCLK5Rn	1	ļ	1	ļ	T8	ļ		 	↓
7.6	1	DNU		 	 	 	C5	 		 	+
7A 7A	VREFB7AN0	GND	CLK12p	1	DIFFIO_RX_T1p	DIFFOUT_T1p	N6 C6	DQ1T	DQ1T	DQ1T	+
7A 7A		io	CLK12p CLK12n	1	DIFFIO_RX_11p DIFFIO_RX_T1n			DQ1T	DQ1T	DQ1T DQ1T	+
7A 7A		IO	RZQ_5	 	DIFFIO_TX_T2p	DIFFOUT_T2p		DQ1T	DQ1T	DQ1T	+
7A	VREFB7AN0	IO	·	1	DIFFIO_TX_T2n	DIFFOUT_T2n	G6			 	1
7A	VREFB7AN0	10	CLK13p	1	DIFFIO_RX_T3p	DIFFOUT_T3p	A6	DQ1T	DQ1T	DQ1T	1
7A	VREFB7AN0	IO	CLK13n	İ	DIFFIO_RX_T3n	DIFFOUT_T3n	B6	DQ1T	DQ1T	DQ1T	1
7A	VREFB7AN0	IO		İ	DIFFIO_TX_T4p	DIFFOUT_T4p	F7	DQ1T	DQ1T	DQ1T	1
7A	VREFB7AN0	10		<u> </u>	DIFFIO_TX_T4n	DIFFOUT_T4n	G7				
7A	VREFB7AN0	IO	CLK14p		DIFFIO_RX_T5p	DIFFOUT_T5p	E6	DQS1T/CQ1T/CQn1T/QKn1T	DQS1T/CQ1T/CQn1T/QKn1T	DQ1T	
7A	VREFB7AN0	IO	CLK14n		DIFFIO_RX_T5n	DIFFOUT_T5n	E7	DQSn1T/QK1T	DQSn1T/QK1T	DQ1T	
/A	VREFB7AN0	IO			DIFFIO_TX_T6p	DIFFOUT_T6p		DQ1T	DQ1T	DQ1T	
/A	VREFB7AN0	IO		1	DIFFIO_TX_T6n	DIFFOUT_T6n	D7			<u> </u>	1
/A	VREFB7AN0	IO	FPLL_TR_CLKOUT2,FPLL_TR_FBp,FPLL_TR_FB1		DIFFIO_RX_T7p			DQ1T	DQ1T	DQ1T	
'A	VREFB7AN0	IO	FPLL_TR_CLKOUT3,FPLL_TR_FBn		DIFFIO RX T7n	DIFFOUT_T7n		DQ1T	DQ1T	DQ1T	
<u>'A</u>	VREFB7AN0	10	FPLL_TR_CLKOUT0,FPLL_TR_CLKOUTp,FPLL_TR_FB0	 	DIFFIO_TX_T8p	DIFFOUT_T8p	J8	DQ1T	DQ1T	DQ1T	
<u>A</u>	VREFB7AN0	IO	FPLL_TR_CLKOUT1,FPLL_TR_CLKOUTn	 	DIFFIO_TX_T8n	DIFFOUT_T8n	K8	DOOT	2017	10017	+
А	VREFB7AN0	IO	CLK15p	 	DIFFIO_RX_T9p	DIFFOUT_T9p	H6	DQ2T	DQ1T	DQ1T	+
7.6	VREFB7AN0 VREFB7AN0	10	CLK15n	_	DIFFIO_RX_T9n	DIFFOUT_T9n	Jb V7	DQ2T DQ2T	DQ1T DQ1T	DQ1T DQ1T	+
7A			VREFB7AN0	+	1		17	DUZI	DQTI	DQTI	+
7A 7A				1	1	l	J/				
7A 7A 'A	VREFB7AN0	10		DEV OF	DIEEIO PV T40s	DIEEOLIT T105				DO1T	
7A 7A 7A 7A	VREFB7AN0 VREFB7AN0	10 10		DEV_OE	DIFFIO_RX_T10p		K6	DQ2T DQ2T	DQ1T DO1T	DQ1T DQ1T	+
	VREFB7AN0 VREFB7AN0 VREFB7AN0	10 10 10		DEV_CLRn	DIFFIO_RX_T10n	DIFFOUT_T10n	L6	DQ2T	DQ1T	DQ1T	
	VREFB7AN0 VREFB7AN0 VREFB7AN0 VREFB7AN0	10 10 10 10				DIFFOUT_T10n DIFFOUT_T11p					



											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
7A	VREFB7AN0	IO		CRC_ERROR	DIFFIO_RX_T12n	DIFFOUT_T12n	P9	DQSn2T/QK2T	DQ1T	DQSn1T/QK1T	
7A	VREFB7AN0	Ю		PR_DONE	DIFFIO_TX_T13p	DIFFOUT_T13p	L7	DQ2T	DQ1T	DQ1T	
7A	VREFB7AN0	10		PR_REQUEST	DIFFIO_TX_T13n	DIFFOUT_T13n	M6		ļ		
7A	VICEI DITTE	IO		INIT_DONE	DIFFIO_RX_T14p		M7	DQ2T	DQ1T	DQ1T	
/A	VREFB7AN0 VREFB7AN0	10		nCEO PR FRROR	DIFFIO_RX_T14n DIFFIO_TX_T15n	DIFFOUT_T14n DIFFOUT_T15p	N7 I 10	DQ2T DQ2T	DQ1T DQ1T	DQ1T DQ1T	+
7A	VREFB7AN0	io		PR_READY	DIFFIO_TX_T15n	DIFFOUT_T15p	M10	DQ21	DQTI	DQTI	+
7A	VREFB7AN0	10		FR_READ1	DIFFIO_TX_T15H	DIFFOUT T16b	D9	DQ3T	DQ2T	DQ1T	+
7A	VREFB7AN0	10			DIFFIO_RX_T16n	DIFFOUT_T16n	E9	DQ3T	DQ2T	DQ1T	+
7A	VREFB7AN0	10			DIFFIO_TX_T17p	DIFFOUT_T17p	F9	DQ3T	DQ2T	DQ1T	1
7A	VREFB7AN0	10			DIFFIO_TX_T17n	DIFFOUT_T17n	G9				1
7A	VREFB7AN0	IO			DIFFIO_RX_T18p	DIFFOUT_T18p	C8	DQ3T	DQ2T	DQ1T	1
7A	VREFB7AN0	Ю			DIFFIO_RX_T18n	DIFFOUT_T18n	D8	DQ3T		DQ1T	
7A	VREFB7AN0	IO			DIFFIO_TX_T19p	DIFFOUT_T19p	K9	DQ3T	DQ2T	DQ1T	
7A	VREFB7AN0	10			DIFFIO_TX_T19n	DIFFOUT_T19n	L9		<u> </u>		4
7A	VREFB7AN0	10			DIFFIO_RX_T20p	DIFFOUT_T20p	A7	DQS3T/CQ3T/CQn3T/QKn3T	DQS2T/CQ2T/CQn2T/QKn2T	DQ1T	4
7A	VREFB7AN0	10			DIFFIO_RX_T20n	DIFFOUT_T20n	B7	DQSn3T/QK3T	DQSn2T/QK2T	DQ1T	4
7A	VREFB7AN0	10			DIFFIO_TX_T21p	DIFFOUT_T21p	B9 C9	DQ3T	DQ2T	DQ1T	+
7A 7A	VREFB7AN0 VREFB7AN0	10			DIFFIO_TX_T21n DIFFIO_RX_T22p	DIFFOUT_T21n DIFFOUT_T22p	A9	DQ3T	DQ2T	DQ1T	+
7A		10					A9 A8				+
7A	VREFB7AN0 VREFB7AN0	in .	 		DIFFIO_RX_T22n DIFFIO_TX_T23p	DIFFOUT_T22n DIFFOUT_T23p	H9	DQ3T DQ3T	DQ2T DQ2T	DQ1T DQ1T	+
7A	VREFB7AN0	IO	 		DIFFIO_TX_T23p	DIFFOUT_T23n	.19				+
7B	VREFB7BN0	IO		1	DIFFIO_RX_T24p	DIFFOUT_T24p	F10	DQ4T	DQ2T	DQ1T	DQ5_7B_0
7B		10		1	DIFFIO_RX_124p	DIFFOUT T24n	F10	DQ4T	DQ2T	DQ1T	DQ5_7B_0 DQ5_7B_1
7B	VREFB7BN0	10	İ		DIFFIO_TX_T25p	DIFFOUT_T25p	N10	DQ4T	DQ2T	DQ1T	DQ5_7B_2
7B	VREFB7BN0	10			DIFFIO_TX_T25n		M11				T
7B	VREFB7BN0	10		<u> </u>	DIFFIO_RX_T26p	DIFFOUT_T26p	B10	DQ4T	DQ2T	DQ1T	DQ5_7B_3
7B	VREFB7BN0	IO			DIFFIO_RX_T26n	DIFFOUT_T26n	C10	DQ4T	DQ2T	DQ1T	DQ5_7B_4
7B	VREFB7BN0	IO			DIFFIO_TX_T27p	DIFFOUT_T27p	H10	DQ4T	DQ2T	DQ1T	DQ5_7B_5
7B	VREFB7BN0	IO			DIFFIO_TX_T27n	DIFFOUT_T27n	J10				
7B	VREFB7BN0	IO			DIFFIO_RX_T28p	DIFFOUT_T28p	P12	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T	DQ1T	DQS5_7B
7B	VREFB7BN0	IO			DIFFIO_RX_T28n	DIFFOUT_T28n	R12	DQSn4T/QK4T	DQ2T	DQ1T	DQS#5_7B
7B	VREFB7BN0	10			DIFFIO_TX_T29p	DIFFOUT_T29p		DQ4T	DQ2T	DQ1T	DM5_7B
7B	VREFB7BN0	10			DIFFIO_TX_T29n	DIFFOUT_T29n	T11				
7B	VREFB7BN0	10			DIFFIO_RX_T30p			DQ4T		DQ1T	DQ5_7B_6
7B	VREFB7BN0	10			DIFFIO_RX_T30n	DIFFOUT_T30n	A10	DQ4T	DQ2T	DQ1T	DQ5_7B_7
7B	VREFB7BN0	10			DIFFIO_TX_T31p	DIFFOUT_T31p	J11	DQ4T	DQ2T	DQ1T	DQ5_7B_8
7B	VREFB7BN0	10			DIFFIO_TX_T31n		K11				
7B	VREFB7BN0 VREFB7BN0	10			DIFFIO_RX_T32p	DIFFOUT_T32p	M12 N12	DQ5T DQ5T	DQ3T DQ3T	DQ2T DQ2T	DQ4_7B_0
/B	VREFB7BN0 VREFB7BN0	10			DIFFIO_RX_T32n	DIFFOUT_T32n	N12 F11	DQ5T		DQ2T	DQ4_7B_1 DQ4_7B_2
7D	VREFB7BN0	10	VREFB7BN0				G11	DQST	DQ31	DQZI	DQ4_7B_2
7B	VREFB7BN0	io	VKEFB/BNU		DIFFIO_RX_T33p	DIFFOUT_T33p	C11	DQ5T	DQ3T	DQ2T	DQ4_7B_3
7B	VREFB7BN0	in			DIFFIO_RX_T33n	DIFFOUT_T33n	D11	DQ5T	DQ3T	DQ2T	DQ4_7B_4
7B	VREFB7BN0	in			DIFFIO_TX_T34p	DIFFOUT_T34p	K12	DQ5T		DQ2T	DQ4_7B_5
7B	VREFB7BN0	10			DIFFIO_TX_T34n	DIFFOUT_T34n	L12	Date	Bajor	DOL	DQ1_7D_0
7B	VREFB7BN0	10			DIFFIO_RX_T35p	DIFFOUT_T35p		DQS5T/CQ5T/CQn5T/QKn5T	DQS3T/CQ3T/CQn3T/QKn3T	DQ2T	DQS4 7B
7B	VREFB7BN0	10			DIFFIO_RX_T35n	DIFFOUT_T35n	E12	DQSn5T/QK5T	DQSn3T/QK3T	DQ2T	DQS#4_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T36p	DIFFOUT_T36p	F12	DQ5T	DQ3T	DQ2T	DM4_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T36n	DIFFOUT_T36n	G12				T
7B		10			DIFFIO_RX_T37p		P13	DQ5T		DQ2T	DQ4_7B_6
7B	VREFB7BN0	10			DIFFIO_RX_T37n	DIFFOUT_T37n	R13	DQ5T	DQ3T	DQ2T	DQ4_7B_7
7B	VREFB7BN0	IO			DIFFIO_TX_T38p	DIFFOUT_T38p	H12	DQ5T	DQ3T	DQ2T	DQ4_7B_8
7B	VREFB7BN0	10		ļ	DIFFIO_TX_T38n	DIFFOUT_T38n	J12		<u> </u>		\bot
/B	VICEI DI DI IO	IO	1	ļ	DIFFIO_RX_T39p	Dii 1 001_100p	B12	DQ6T		DQ2T	DQ3_7B_0
/B	VREFB7BN0	IO		ļ	DIFFIO_RX_T39n DIFFIO_TX_T40n	DIFFOUT_T39n	C12 M13	DQ6T	DQ3T	DQ2T DQ2T	DQ3_7B_1
/B	VREFB7BN0 VREFB7BN0	IO IO		-	DIFFIO_TX_T40p DIFFIO_TX_T40n	DII 1 001_110P	M13 N13	DQ6T	DQ3T	DQ21	DQ3_7B_2
7 D		io		1	DIFFIO_IX_I40n DIFFIO_RX_T41p		N13 A13	DQ6T	DQ3T	DQ2T	DO2 7D 2
7B	VREFB7BN0 VREFB7BN0	io		1	DIFFIO_RX_141p DIFFIO_RX_T41n	DIFFOUT_T41p DIFFOUT_T41n	A13 A12	DQ6T	DQ3T	DQ2T	DQ3_7B_3 DQ3_7B_4
7B	VREFB7BN0 VREFB7BN0	lio.	1	1	DIFFIO_RX_141n DIFFIO_TX_T42p		J13	DQ6T		DQ2T	DQ3_7B_4 DQ3_7B_5
7B	VREFB7BN0 VREFB7BN0	in .	1	1	DIFFIO_TX_T42p	DIFFOUT_T42p	J13 K13	DGUI	DQUI	DULE I	DU3_1B_3
7B		IO IO			DIFFIO_TX_T42II			DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	DQS2T/CQ2T/CQn2T/QKn2T	DOS3 7B
7B	VREFB7BN0	IO			DIFFIO_RX_T43n	DIFFOUT_T43n	E13	DQSn6T/QK6T	DQ3T	DQSn2T/QK2T	DQS#3_7B
7B	VREFB7BN0	IO			DIFFIO_TX_T44p			DQ6T		DQ2T	DM3_7B
7B	VREFB7BN0	10			DIFFIO_TX_T44n		B13				1 -
7B	VREFB7BN0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	C14	DQ6T	DQ3T	DQ2T	DQ3_7B_6
7B	VREFB7BN0	10			DIFFIO_RX_T45n	DIFFOUT_T45n	D14	DQ6T	DQ3T	DQ2T	DQ3_7B_7
7B	VREFB7BN0	Ю			DIFFIO_TX_T46p	DIFFOUT_T46p	G13	DQ6T	DQ3T	DQ2T	DQ3_7B_8
7B	VREFB7BN0	Ю			DIFFIO_TX_T46n	DIFFOUT_T46n	H13				
7C	VREFB7CN0	IO			DIFFIO_RX_T47p	DIFFOUT_T47p	R14	DQ7T	DQ4T	DQ2T	DQ2_7C_0
7C	VREFB7CN0	Ю			DIFFIO_RX_T47n	DIFFOUT_T47n	T14	DQ7T	DQ4T	DQ2T	DQ2_7C_1
7C	VREFB7CN0	IO			DIFFIO_TX_T48p	DIFFOUT_T48p		DQ7T	DQ4T	DQ2T	DQ2_7C_2
7C	VREFB7CN0	Ю			DIFFIO_TX_T48n	DIFFOUT_T48n	N14			1	
_	VREFB7CN0	10			DIFFIO_RX_T49p	DIFFOUT_T49p	F14	DQ7T	DQ4T	DQ2T	DQ2_7C_3
'C		10			DIFFIO_RX_T49n	DIFFOUT_T49n	G14	DQ7T	DQ4T	DQ2T	DQ2_7C_4
7C 7C	VREFB7CN0										
7C 7C	VREFB7CN0	IO			DIFFIO_TX_T50p	DIFFOUT_T50p	L15	DQ7T	DQ4T	DQ2T	DQ2_7C_5
7C 7C 7C	VREFB7CN0 VREFB7CN0	IO IO			DIFFIO_TX_T50n	DIFFOUT_T50n	M15				
7C 7C 7C 7C 7C	VREFB7CN0	10 10 10			DIFFIO_TX_T50n DIFFIO_RX_T51p	DIFFOUT_T50n DIFFOUT_T51p		DQ7T DQS7T/CQ7T/CQn7T/QKn7T DQSn7T/QK7T	DQS4T/CQ4T/CQn4T/QKn4T	DQ2T DQ2T DQ2T	DQ2_7C_5 DQS2_7C DQS#2_7C



											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
7C	VREFB7CN0	Ю			DIFFIO_TX_T52p	DIFFOUT_T52p	N15	DQ7T	DQ4T	DQ2T	DM2_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T52n	DIFFOUT_T52n	P15				
'C	VREFB7CN0	10			DIFFIO_RX_T53p	DIFFOUT_T53p	E15	DQ7T	DQ4T	DQ2T	DQ2_7C_6
C	VREFB7CN0	10			DIFFIO_RX_T53n	DIFFOUT_T53n	F15	DQ7T	DQ4T	DQ2T	DQ2_7C_7
7C	VREFB7CN0	10			DIFFIO_TX_T54p	DIFFOUT_T54p	J14	DQ7T	DQ4T	DQ2T	DQ2_7C_8
7C	VREFB7CN0	10		-	DIFFIO_TX_T54n	DIFFOUT_T54n	K14	DOOT	DOAT	DOOT	DO4 70 0
70	VREFB7CN0 VREFB7CN0	10		+	DIFFIO_RX_T55p DIFFIO_RX_T55n	DIFFOUT_T55p DIFFOUT_T55n	P16 R16	DQ8T DQ8T	DQ4T DQ4T	DQ2T DQ2T	DQ1_7C_0 DQ1_7C_1
7C	VREFB7CN0	10			DIFFIO_RX_155H	DIFFOUT_1550	C15	DQ8T	DQ4T	DQ2T	DQ1_7C_1
7C	VREFB7CN0	IO .	VREFB7CN0				D15	DQUI	DQ41	DQZI	DQ1_70_2
7C	VREFB7CN0	IO			DIFFIO_RX_T56p	DIFFOUT_T56p	M16	DQ8T	DQ4T	DQ2T	DQ1_7C_3
7C	VREFB7CN0	10			DIFFIO_RX_T56n	DIFFOUT_T56n	N16	DQ8T	DQ4T	DQ2T	DQ1_7C_4
7C	VREFB7CN0	IO			DIFFIO_TX_T57p	DIFFOUT_T57p	H15	DQ8T	DQ4T	DQ2T	DQ1_7C_5
7C	VREFB7CN0	10			DIFFIO_TX_T57n	DIFFOUT_T57n	J15				
7C	VREFB7CN0	Ю			DIFFIO_RX_T58p	DIFFOUT_T58p	G16	DQS8T/CQ8T/CQn8T/QKn8T	DQ4T	DQ2T	DQS1_7C
7C	VREFB7CN0	Ю			DIFFIO_RX_T58n	DIFFOUT_T58n	H16	DQSn8T/QK8T	DQ4T	DQ2T	DQS#1_7C
7C	VREFB7CN0	10			DIFFIO_TX_T59p	DIFFOUT_T59p	A15	DQ8T	DQ4T	DQ2T	DM1_7C
7C	VREFB7CN0	IO			DIFFIO_TX_T59n	DIFFOUT_T59n	B15				
7C	VREFB7CN0 VREFB7CN0	10			DIFFIO_RX_T60p DIFFIO_RX_T60n	DIFFOUT_T60p DIFFOUT_T60n	D16 E16	DQ8T DQ8T	DQ4T DQ4T	DQ2T DQ2T	DQ1_7C_6 DQ1_7C_7
70		10		+							
70	VREFB7CN0 VREFB7CN0	10	1	†	DIFFIO_TX_T61p DIFFIO_TX_T61n	DIFFOUT_T61p DIFFOUT_T61n	J16 K16	DQ8T	DQ4T	DQ2T	DQ1_7C_8 RESET#_7D
7D	VREFB7CN0	IO		<u> </u>	DIFFIO_TX_T61fi DIFFIO_RX_T62p	DIFFOUT_T62p	N18	DQ9T	DQ5T	†	CK 7D
7D	VREFB7DN0	IO			DIFFIO_RX_T62n	DIFFOUT_T62n	P18	DQ9T	DQ5T		CK#_7D
7D	VREFB7DN0	10			DIFFIO_TX_T63p	DIFFOUT_T63p	M17	DQ9T	DQ5T	i	CKE_7D_0
7D	VREFB7DN0	10			DIFFIO_TX_T63n	DIFFOUT_T63n	N17				CKE_7D_1
7D	VREFB7DN0	IO			DIFFIO_RX_T64p	DIFFOUT_T64p	B16	DQ9T	DQ5T		A_7D_0
7D	VREFB7DN0	10			DIFFIO_RX_T64n	DIFFOUT_T64n	C16	DQ9T	DQ5T		A_7D_1
7D	VREFB7DN0	Ю			DIFFIO_TX_T65p	DIFFOUT_T65p	J17	DQ9T	DQ5T		A_7D_2
7D	VREFB7DN0	10			DIFFIO_TX_T65n	DIFFOUT_T65n	K17				A_7D_3
7D	VREFB7DN0	10			DIFFIO_RX_T66p	DIFFOUT_T66p	F17	DQS9T/CQ9T/CQn9T/QKn9T	DQS5T/CQ5T/CQn5T/QKn5T		A_7D_4
7D	VREFB7DN0	10			DIFFIO_RX_T66n	DIFFOUT_T66n	G17	DQSn9T/QK9T	DQSn5T/QK5T		A_7D_5
7D	VREFB7DN0	10			DIFFIO_TX_T67p	DIFFOUT_T67p	R17	DQ9T	DQ5T		A_7D_6
7D	VREFB7DN0 VREFB7DN0	10			DIFFIO_TX_T67n	DIFFOUT_T67n DIFFOUT_T68p	T17 C17	DQ9T	DQ5T		A_7D_7
7D 7D	VREFB7DN0 VREFB7DN0	10		+	DIFFIO_RX_T68p DIFFIO_RX_T68n	DIFFOUT_168p	D17	DQ9T	DQ5T		A_7D_8 A_7D_9
7D	VREFB7DN0	io io		+	DIFFIO_KX_168n	DIFFOUT T69n	K18	DO9T	DOST		A_7D_9 A_7D_10
7D	VREFB7DN0	in			DIFFIO_TX_T69n	DIFFOUT_T69n	L18	DQST	DQST		A_7D_10 A_7D_11
7D	VREFB7DN0	IO .			DIFFIO_RX_T70p	DIFFOUT T70p	R19	DO10T	DOST		A_7D_11
7D	VREFB7DN0	IO			DIFFIO_RX_T70n	DIFFOUT_T70n	T19	DQ10T	DQ5T		A_7D_13
7D	VREFB7DN0	IO					R18	DQ10T	DQ5T		A_7D_14
7D	VREFB7DN0	IO	VREFB7DN0				T18				
7D	VREFB7DN0	10			DIFFIO_RX_T71p	DIFFOUT_T71p	E18	DQ10T	DQ5T		BA_7D_0
7D	VREFB7DN0	IO			DIFFIO_RX_T71n	DIFFOUT_T71n		DQ10T	DQ5T		BA_7D_1
7D	VREFB7DN0	Ю			DIFFIO_TX_T72p	DIFFOUT_T72p	H18	DQ10T	DQ5T		BA_7D_2
7D	VREFB7DN0	10			DIFFIO_TX_T72n	DIFFOUT_T72n	J18				RAS#_7D
7D	VREFB7DN0	10			DIFFIO_RX_T73p	DIFFOUT_T73p	N19	DQS10T/CQ10T/CQn10T/QKn10T	DQ5T		CAS#_7D
7D	VREFB7DN0	10			DIFFIO_RX_T73n	DIFFOUT_T73n		DQSn10T/QK10T	DQ5T		WE#_7D
7D 7D	VREFB7DN0 VREFB7DN0	10			DIFFIO_TX_T74p	DIFFOUT_T74p DIFFOUT_T74n	B18 C18	DQ10T	DQ5T		ODT_7D_0
7D	VREFB7DN0	10		+	DIFFIO_TX_T74n DIFFIO_RX_T75p	DIFFOUT_174n	A17	DQ10T	DQ5T		ODT_7D_1 A_7D_15
7D	VREFB7DN0	10		+	DIFFIO_RX_T75p	DIFFOUT_T75n		DQ10T	DQ5T		A_7D_15
7D	VREFB7DN0	IO .	 	 	DIFFIO_TX_T76p	DIFFOUT_T76p	L19	DQ10T	DQ5T	†	CS#_7D_0
7D	VREFB7DN0	IO .		1	DIFFIO_TX_T76n	DIFFOUT_T76n	M19			i e	CS#_7D_1
7D	VREFB7DN0	IO		1	DIFFIO_TX_T70p	DIFFOUT_T77p	F19	DQ11T		İ	35
7D	VREFB7DN0	10		İ	DIFFIO_RX_T77n	DIFFOUT_T77n	G19	DQ11T		İ	1
7D	VREFB7DN0	IO			DIFFIO_TX_T78p	DIFFOUT_T78p	J19	DQ11T			
7D	VREFB7DN0	IO			DIFFIO_TX_T78n	DIFFOUT_T78n	K19				
7D	VREFB7DN0	10			DIFFIO_RX_T79p	DIFFOUT_T79p		DQ11T			
7D	VREFB7DN0	Ю		1	DIFFIO_RX_T79n	DIFFOUT_T79n		DQ11T			4
7D	VREFB7DN0	10			DIFFIO_TX_T80p	DIFFOUT_T80p	J20	DQ11T			
7D	VREFB7DN0	10			DIFFIO_TX_T80n	DIFFOUT_T80n	K20			1	
7D	VREFB7DN0	10		 	DIFFIO_RX_T81p	DIFFOUT_T81p	A18	DQS11T/CQ11T/CQn11T/QKn11T		1	+
7D	VREFB7DN0	10		 	DIFFIO_RX_T81n	DIFFOUT_T81n		DQSn11T/QK11T		ļ	+
7D 7D	VREFB7DN0 VREFB7DN0	10		 	DIFFIO_TX_T82p	DIFFOUT_T82p	R20 T20	DQ11T		ļ	+
7D 7D	VREFB7DN0 VREFB7DN0	10		_	DIFFIO_TX_T82n DIFFIO_RX_T83p	DIFFOUT_T82n DIFFOUT_T83p	T20 F20	DQ11T		1	+
יט מי	VREFB7DN0 VREFB7DN0	10		<u> </u>	DIFFIO_RX_183p	DIFFOUT_183p	G20	DQ11T DQ11T		1	+
ח	VREFB7DN0 VREFB7DN0	10	1	†	DIFFIO_RX_183n DIFFIO_TX_T84p	DIFFOUT_T84p	M20	DQ11T DQ11T		 	+
מי	VREFB7DN0	in	 	 	DIFFIO_TX_T84n	DIFFOUT_T84n	N20			†	+
	VINEL BY DINU	VCCA_FPLL		1	D.I. I.IO_1A_104II	D 1 OO1_10#II	V20			i e	+
	1	VCCD_FPLL		1	1	1	V19			İ	1
		DNU	İ	İ	1		P21			İ	1 '
BD	VREFB8DN0		CLK19p		DIFFIO_RX_T85p	DIFFOUT_T85p	C20	DQ12T	DQ6T	DQ3T	1
BD	VREFB8DN0	10	CLK19n	İ	DIFFIO_RX_T85n	DIFFOUT_T85n	D20	DQ12T	DQ6T	DQ3T	1
BD	VREFB8DN0	10			DIFFIO_TX_T86p	DIFFOUT_T86p	M21	DQ12T	DQ6T	DQ3T	
BD	VREFB8DN0	10		<u> </u>	DIFFIO_TX_T86n	DIFFOUT_T86n	N21				
BD	VREFB8DN0	IO	CLK18p		DIFFIO_RX_T87p	DIFFOUT_T87p	G21	DQ12T	DQ6T	DQ3T	
BD.		10	CLK18n		DIFFIO_RX_T87n	DIFFOUT_T87n	H21	DQ12T	DQ6T	DQ3T	
BD	VREFB8DN0	10			DIFFIO_TX_T88p	DIFFOUT_T88p	D21	DQ12T	DQ6T	DQ3T	
BD.	VREFB8DN0				DIFFIO_TX_T88n	DIFFOUT_T88n	E21				



											Note (1
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
D	VREFB8DN0	IO	FPLL_TC_CLKOUT2,FPLL_TC_FBp,FPLL_TC_FB1		DIFFIO_RX_T89p	DIFFOUT_T89p	A20	DQS12T/CQ12T/CQn12T/QKn12T	DQS6T/CQ6T/CQn6T/QKn6T	DQ3T	1
BD.	VREFB8DN0	10	FPLL TC CLKOUT3,FPLL TC FBn		DIFFIO_RX_T89n	DIFFOUT_T89n	B21	DQSn12T/QK12T	DQSn6T/QK6T	DQ3T	1
D	VREFB8DN0	IO	FPLL_TC_CLKOUT0,FPLL_TC_CLKOUTp,FPLL_TC_FB0		DIFFIO_TX_T90p	DIFFOUT_T90p	J21	DQ12T	DQ6T	DQ3T	
D	VREFB8DN0	10	FPLL_TC_CLKOUT1,FPLL_TC_CLKOUTn		DIFFIO_TX_T90n	DIFFOUT_T90n	K21				
D	VREFB8DN0	10	CLK17p		DIFFIO_RX_T91p	DIFFOUT_T91p	A22	DQ12T	DQ6T	DQ3T	
D	VREFB8DN0	10	CLK17n		DIFFIO_RX_T91n	DIFFOUT_T91n	A21	DQ12T	DQ6T	DQ3T	
D D	VREFB8DN0 VREFB8DN0	10			DIFFIO_TX_T92p DIFFIO_TX_T92n	DIFFOUT_T92p DIFFOUT T92n	R21 T21	DQ12T	DQ6T	DQ3T	+
D D	VREFB8DN0	10	CLK16p		DIFFIO_TX_T92n DIFFIO_RX_T93p	DIFFOUT_T92n DIFFOUT_T93p	B22	DQ13T	DQ6T	DQ3T	+
D	VREFB8DN0	in	CLK16n		DIFFIO_RX_T93n	DIFFOUT_T93n	C22	DQ13T	DQ6T	DQ3T	+
BD	VREFB8DN0	10	OLIVIOII		BII TIO_IOX_TOON	Dii 1 001_100ii	J22	DQ13T	DQ6T	DQ3T	_
BD	VREFB8DN0	IO	VREFB8DN0				H22				
BD.	VREFB8DN0	10			DIFFIO_RX_T94p	DIFFOUT_T94p	E22	DQ13T	DQ6T	DQ3T	
BD.	VREFB8DN0	IO			DIFFIO_RX_T94n	DIFFOUT_T94n	F22	DQ13T	DQ6T	DQ3T	
BD	VREFB8DN0	IO			DIFFIO_TX_T95p	DIFFOUT_T95p	A23	DQ13T	DQ6T	DQ3T	
BD	VREFB8DN0	10			DIFFIO_TX_T95n	DIFFOUT_T95n	A24				
BD	VREFB8DN0	10			DIFFIO_RX_T96p	DIFFOUT_T96p	C23	DQS13T/CQ13T/CQn13T/QKn13T	DQ6T	DQS3T/CQ3T/CQn3T/QKn3T	
BD	VREFB8DN0	10			DIFFIO_RX_T96n	DIFFOUT_T96n	D23	DQSn13T/QK13T	DQ6T	DQSn3T/QK3T	
BD BD	VREFB8DN0 VREFB8DN0	10			DIFFIO_TX_T97p DIFFIO_TX_T97n	DIFFOUT_T97p DIFFOUT_T97n	L22 M22	DQ13T	DQ6T	DQ3T	
RD.		10		+				DO42T	DOCT	DOST	+
חס	VREFB8DN0 VREFB8DN0	10		+	DIFFIO_RX_T98p DIFFIO_RX_T98n	DIFFOUT_T98p DIFFOUT_T98n	N22 P22	DQ13T DQ13T	DQ6T DQ6T	DQ3T DQ3T	+
ID.	VREFB8DN0	lio		+	DIFFIO_TX_T99p	DIFFOUT_1980	R22	DQ13T	DQ6T	DQ3T	+
D .	VREFB8DN0	10		1	DIFFIO_TX_T99n	DIFFOUT_T99n	T22				+
BD	VREFB8DN0	10		1	DIFFIO_TX_199II	DIFFOUT T100p	F23	DQ14T	DQ7T	DQ3T	+
BD	VREFB8DN0	IO			DIFFIO_RX_T100p	DIFFOUT_T100p	G23	DQ14T	DQ7T	DQ3T	1
BD	VREFB8DN0	IO	İ	1	DIFFIO_TX_T101p	DIFFOUT_T101p	R23	DQ14T	DQ7T	DQ3T	1
BD	VREFB8DN0	IO	İ	1	DIFFIO_TX_T101n	DIFFOUT_T101n	T23	-			1
BD.	VREFB8DN0	Ю		1	DIFFIO_RX_T102p	DIFFOUT_T102p	B24	DQ14T	DQ7T	DQ3T	1
BD.	VREFB8DN0	10			DIFFIO_RX_T102n	DIFFOUT_T102n	C24	DQ14T	DQ7T	DQ3T	1
BD	VREFB8DN0	10			DIFFIO_TX_T103p	DIFFOUT_T103p	M23	DQ14T	DQ7T	DQ3T	
BD	VREFB8DN0	Ю			DIFFIO_TX_T103n	DIFFOUT_T103n	N23				
BD.	VREFB8DN0	IO			DIFFIO_RX_T104p	DIFFOUT_T104p	D24	DQS14T/CQ14T/CQn14T/QKn14T	DQS7T/CQ7T/CQn7T/QKn7T	DQ3T	
D	VREFB8DN0	IO			DIFFIO_RX_T104n	DIFFOUT_T104n	E24	DQSn14T/QK14T	DQSn7T/QK7T	DQ3T	
D	VREFB8DN0	IO			DIFFIO_TX_T105p	DIFFOUT_T105p	J23	DQ14T	DQ7T	DQ3T	
BD	VREFB8DN0	10			DIFFIO_TX_T105n	DIFFOUT_T105n	K23				
BD	VREFB8DN0	10			DIFFIO_RX_T106p	DIFFOUT_T106p	F24	DQ14T	DQ7T	DQ3T	
3D	VREFB8DN0	10			DIFFIO_RX_T106n	DIFFOUT_T106n	G24	DQ14T	DQ7T	DQ3T	
BD	VREFB8DN0	10			DIFFIO_TX_T107p	DIFFOUT_T107p	H24	DQ14T	DQ7T	DQ3T	
8D	VREFB8DN0	Ю			DIFFIO_TX_T107n	DIFFOUT_T107n	J24				
8C	VREFB8CN0	10			DIFFIO_RX_T108p	DIFFOUT_T108p	T26	DQ15T	DQ7T	DQ3T	DQ5_8C_0
BC .	VREFB8CN0 VREFB8CN0	10			DIFFIO_RX_T108n	DIFFOUT_T108n DIFFOUT T109p	T25 G25	DQ15T	DQ7T DQ7T	DQ3T DQ3T	DQ5_8C_1 DQ5_8C_2
BC BC		10						DQ15T	DQ71	DQ31	DQ5_8C_2
SC NC	VREFB8CN0 VREFB8CN0	10			DIFFIO_TX_T109n DIFFIO_RX_T110p	DIFFOUT_T109n DIFFOUT_T110p	H25 N24	DQ15T	DQ7T	DQ3T	DQ5_8C_3
00	VREFB8CN0	10		+	DIFFIO_RX_T110p	DIFFOUT_T110n	P24	DQ15T	DQ7T	DQ3T	DQ5_8C_4
SC	VREFB8CN0	10		+	DIFFIO_RX_T110f	DIFFOUT_T111p	R24	DQ15T	DQ7T	DQ3T	DQ5_8C_4
BC	VREFB8CN0	10		+	DIFFIO_TX_T111p	DIFFOUT_T111p	T24	DQISI	buri	DQ31	DQ3_8C_3
3C	VREFB8CN0	in .			DIFFIO_RX_T112p	DIFFOUT_T112p	A25	DQS15T/CQ15T/CQn15T/QKn15T	DQ7T	DO3T	DOS5 8C
BC	VREFB8CN0	10			DIFFIO_RX_T112n	DIFFOUT T112n	B25	DQSn15T/QK15T	DQ7T	DQ3T	DQS#5 8C
RC.	VRFFB8CN0	IO			DIFFIO TX T113p	DIFFOUT T113p	K24	DQ15T	DQ7T	DQ3T	DM5_8C
BC	VREFB8CN0	10			DIFFIO_TX_T113n	DIFFOUT T113n	L24				
BC	VREFB8CN0	10			DIFFIO_RX_T114p	DIFFOUT_T114p	D25	DQ15T	DQ7T	DQ3T	DQ5_8C_6
BC .	VREFB8CN0	10			DIFFIO_RX_T114n	DIFFOUT_T114n	E25	DQ15T	DQ7T	DQ3T	DQ5_8C_7
BC	VREFB8CN0	IO			DIFFIO_TX_T115p	DIFFOUT_T115p	P25	DQ15T	DQ7T	DQ3T	DQ5_8C_8
3C	VREFB8CN0	Ю			DIFFIO_TX_T115n	DIFFOUT_T115n	R25				
BC .	VREFB8CN0	IO			DIFFIO_RX_T116p	DIFFOUT_T116p	C26	DQ16T	DQ8T	DQ4T	DQ4_8C_0
BC	VREFB8CN0	10		<u> </u>	DIFFIO_RX_T116n	DIFFOUT_T116n	D26	DQ16T	DQ8T	DQ4T	DQ4_8C_1
BC .	VREFB8CN0	10		 			K25	DQ16T	DQ8T	DQ4T	DQ4_8C_2
BC .	VREFB8CN0	10	VREFB8CN0	 	L		L25				4
BC	VREFB8CN0	10			DIFFIO_RX_T117p	DIFFOUT_T117p	R26	DQ16T	DQ8T	DQ4T	DQ4_8C_3
3C	VREFB8CN0	IIO	1	1	DIFFIO_RX_T117n	DIFFOUT_T117n	T27	DQ16T	DQ8T	DQ4T	DQ4_8C_4
SC .	VREFB8CN0	IO		 	DIFFIO_TX_T118p DIFFIO_TX_T118n	DIFFOUT_T118p DIFFOUT_T118n	A26	DQ16T	DQ8T	DQ4T	DQ4_8C_5
)C	VREFB8CN0	IO IO		+			A27	DODACTIONACTION ACTION ACT	DOCOT/OCOT/OC-CT/O// CT	DOAT	D004 00
oc .	VREFB8CN0 VREFB8CN0	IO IO		+	DIFFIO_RX_T119p DIFFIO_RX_T119n	DIFFOUT_T119p DIFFOUT_T119n	M26 N26	DQS16T/CQ16T/CQn16T/QKn16T DQSn16T/QK16T	DQS8T/CQ8T/CQn8T/QKn8T DQSn8T/QK8T	DQ4T DQ4T	DQS4_8C DQS#4_8C
ec .	VREFB8CN0 VREFB8CN0	IO		+	DIFFIO_RX_I119n DIFFIO_TX_T120p	DIFFOUT_I119n DIFFOUT_T120p	N26 J26	DQSn161/QK161 DQ16T	DQSn81/QK81 DQ8T	DQ4T	DQS#4_8C DM4_8C
ic .	VREFB8CN0	lio.	1	1	DIFFIO_TX_T120p	DIFFOUT_T120p	J26 K26	DQ101	Date	DQT1	DIVI4_0C
iC.	VREFB8CN0 VREFB8CN0	lio	1	1	DIFFIO_IX_I120n	DIFFOUT_T120n	F26	DQ16T	DQ8T	DQ4T	DQ4_8C_6
ec ec	VREFB8CN0	lio.		+	DIFFIO_RX_T121p	DIFFOUT_T121p	G26	DO16T	DQ8T	DO4T	DQ4_8C_7
ic.	VREFB8CN0	lin		1	DIFFIO_RX_T121II	DIFFOUT_T122p	M25	DQ16T	DQ8T	DQ4T	DQ4_8C_8
BC	VREFB8CN0	lio	 	+	DIFFIO_TX_T122p	DIFFOUT_T122p	N25	24.01	540.	D 40,71	Jun-00_0
3C	VREFB8CN0	lin		1	DIFFIO_TX_T122II	DIFFOUT_T123p	P27	DQ17T	DQ8T	DQ4T	DQ3 8C 0
BC .	VREFB8CN0	IO		1	DIFFIO_RX_T123p	DIFFOUT T123p	R27	DQ17T	DQ8T	DQ4T	DQ3_8C_0
BC	VREFB8CN0	IO		1	DIFFIO_TX_T124p	DIFFOUT_T124p	H27	DQ17T	DQ8T	DQ4T	DQ3_8C_2
3C	VREFB8CN0	10		1	DIFFIO TX T124n	DIFFOUT T124n	J27				1
BC	VREFB8CN0	IO		1	DIFFIO_RX_T125p	DIFFOUT_T125p	B27	DQ17T	DQ8T	DQ4T	DQ3_8C_3
BC	VREFB8CN0	IO		1	DIFFIO_RX_T125n	DIFFOUT_T125p	C27	DQ17T	DQ8T	DQ4T	DQ3_8C_4
20	VREFB8CN0	10		İ	DIFFIO_TX_T126p	DIFFOUT_T126p	E27	DQ17T	DQ8T	DQ4T	DQ3_8C_5
				1					i		
BC	VREFB8CN0	10			DIFFIO_TX_T126n	DIFFOUT_T126n	F27				l l



ank		1						1	T		Note
umber		PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR hard memo PHY (3)
;	VREFB8CN0	10			DIFFIO_RX_T127n	DIFFOUT_T127n	T28	DQSn17T/QK17T	DQ8T	DQSn4T/QK4T	DQS#3_8C
	VREFB8CN0	10			DIFFIO_TX_T128p	DIFFOUT_T128p	K27	DQ17T	DQ8T	DQ4T	DM3_8C
	VREFB8CN0	10			DIFFIO_TX_T128n	DIFFOUT_T128n	L27				
	VREFB8CN0	10			DIFFIO_RX_T129p	DIFFOUT_T129p	M27	DQ17T	DQ8T	DQ4T	DQ3_8C_6
	VREFB8CN0	10			DIFFIO_RX_T129n	DIFFOUT_T129n	N27	DQ17T	DQ8T	DQ4T	DQ3_8C_7
	VREFB8CN0	10			DIFFIO TX T130p	DIFFOUT T130p	N28	DQ17T	DQ8T	DQ4T	DQ3_8C_8
	VREFB8CN0	10			DIFFIO TX T130n	DIFFOUT T130n	P28				
	VREFB8BN0	IO.			DIFFIO_RX_T131p	DIFFOUT_T131p	L28	DQ18T	DQ9T	DQ4T	DQ2_8B_0
	VREFB8BN0	in			DIFFIO RX T131n	DIFFOUT T131n	M28	DQ18T	DOST	DQ4T	DQ2_8B_1
	VREFB8BN0	10		_	DIFFIO_TX_T132p	DIFFOUT_T131II	H28	DQ18T	DQ9T	DQ4T	DQ2_8B_2
	VREFB8BN0	10			DIFFIO_TX_T132n	DIFFOUT_T132n	J28	DQ181	DQ91	DQ41	DQ2_66_2
		10						DOJOT	2007	2017	200 02 0
	VREFB8BN0	10			DIFFIO_RX_T133p	DIFFOUT_T133p	C28	DQ18T	DQ9T	DQ4T	DQ2_8B_3
	VREFB8BN0	10			DIFFIO_RX_T133n	DIFFOUT_T133n	D28	DQ18T	DQ9T	DQ4T	DQ2 8B 4
	VREFB8BN0	10			DIFFIO_TX_T134p	DIFFOUT_T134p	F28	DQ18T	DQ9T	DQ4T	DQ2_8B_5
	VREFB8BN0	10			DIFFIO_TX_T134n	DIFFOUT_T134n	G28				
	VREFB8BN0	IO			DIFFIO_RX_T135p	DIFFOUT_T135p	R29	DQS18T/CQ18T/CQn18T/QKn18T	DQS9T/CQ9T/CQn9T/QKn9T	DQ4T	DQS2_8B
	VREFB8BN0	10			DIFFIO_RX_T135n	DIFFOUT_T135n	T29	DQSn18T/QK18T	DQSn9T/QK9T	DQ4T	DQS#2_8E
	VREFB8BN0	10			DIFFIO_TX_T136p	DIFFOUT_T136p	J29	DQ18T	DQ9T	DQ4T	DM2_8B
	VREFB8BN0	10			DIFFIO_TX_T136n	DIFFOUT_T136n	K29				
	VRFFB8BN0	IO			DIFFIO RX T137p	DIFFOUT T137p	M29	DO18T	DOST	DO4T	DQ2 8B 6
	VREFB8BN0	in.			DIFFIO_RX_T137n	DIFFOUT_T137n	N29	DQ18T	DQ9T	DQ4T	DQ2_8B_7
	VREFB8BN0	lio		+	DIFFIO_RX_T13/II	DIFFOUT_T138n	F29	DO18T	DO9T	DQ4T	DQ2 8B 8
	VREFB8BN0	lio.	<u> </u>	+	DIFFIO_TX_T138p	DIFFOUT_T138n	G29	24.01	5401	DQ71	DQ2_0B_0
	VREFB8BN0	10		1	DIFFIO_TX_T138n	DIFFOUT_T138n	G29 B28	DQ19T	DQ9T	DQ4T	DQ1 8B (
		10	<u> </u>	+							
	VREFB8BN0	10		_	DIFFIO_RX_T139n	DIFFOUT_T139n	C29	DQ19T	DQ9T	DQ4T	DQ1_8B_
	VREFB8BN0	10				ļ	R30	DQ19T	DQ9T	DQ4T	DQ1_8B_2
	VREFB8BN0	IO	VREFB8BN0				R31				
	VREFB8BN0	10			DIFFIO_RX_T140p	DIFFOUT_T140p	A29	DQ19T	DQ9T	DQ4T	DQ1_8B_3
	VREFB8BN0	10			DIFFIO_RX_T140n	DIFFOUT_T140n	A28	DQ19T	DQ9T	DQ4T	DQ1_8B_4
	VREFB8BN0	10			DIFFIO_TX_T141p	DIFFOUT_T141p	L30	DQ19T	DQ9T	DQ4T	DQ1_8B_5
	VREFB8BN0	10			DIFFIO_TX_T141n	DIFFOUT T141n	M30		1	1	
	VREFB8BN0	10		_	DIFFIO_RX_T142p	DIFFOUT_T142p	N30	DQS19T/CQ19T/CQn19T/QKn19T	DQ9T	DQ4T	DQS1_8B
	VREFB8BN0	in		_	DIFFIO_RX_T142p	DIFFOUT_T142p	P30		DQ9T	DQ4T	DQS#1 8E
		10						DQSn19T/QK19T			
	VREFB8BN0	10			DIFFIO_TX_T143p	DIFFOUT_T143p	J30	DQ19T	DQ9T	DQ4T	DM1_8B
	VREFB8BN0	10			DIFFIO_TX_T143n	DIFFOUT_T143n	K30				
	VREFB8BN0	IO			DIFFIO_RX_T144p	DIFFOUT_T144p	D30	DQ19T	DQ9T	DQ4T	DQ1_8B_6
	VREFB8BN0	IO			DIFFIO_RX_T144n	DIFFOUT_T144n	D29	DQ19T	DQ9T	DQ4T	DQ1_8B_7
	VREFB8BN0	10			DIFFIO_TX_T145p	DIFFOUT_T145p	F30	DQ19T	DQ9T	DQ4T	DQ1_8B_8
	VREFB8BN0	10			DIFFIO TX T145n	DIFFOUT T145n	G30				RESET# 8
	VREFB8AN0	IO.			DIFFIO_RX_T146p	DIFFOUT_T146p	B30	DQ20T	DQ10T		CK_8A
	VREEB8AN0	10			DIFFIO RX T146n	DIFFOUT T146n	C30	DQ20T	DQ10T		CK# 8A
	VREFB8AN0	10		+	DIFFIO_TX_T147p	DIFFOUT_T147p	E31	DQ20T	DQ10T	+	CKE_8A_0
	VREFB8AN0	10		+	DIFFIO_TX_T147p	DIFFOUT T147p	E31	DQ201	DQ101	+	CKE_8A_0
		10								+	
	VREFB8AN0	10			DIFFIO_RX_T148p	DIFFOUT_T148p	B31	DQ20T	DQ10T		A_8A_0
	VREFB8AN0	10			DIFFIO_RX_T148n	DIFFOUT_T148n	A30	DQ20T	DQ10T		A_8A_1
	VREFB8AN0	IO			DIFFIO_TX_T149p	DIFFOUT_T149p	A31	DQ20T	DQ10T		A_8A_2
	VREFB8AN0	10			DIFFIO_TX_T149n	DIFFOUT_T149n	A32				A 8A 3
	VREFB8AN0	10			DIFFIO_RX_T150p	DIFFOUT_T150p	A33	DQS20T/CQ20T/CQn20T/QKn20T	DQS10T/CQ10T/CQn10T/QKn10T		A_8A_4
	VREFB8AN0	10			DIFFIO_RX_T150n	DIFFOUT_T150n	B33	DQSn20T/QK20T	DQSn10T/QK10T		A 8A 5
	VREEB8ANO	IO			DIFFIO TX T151p	DIFFOLIT T151n	H31	DO20T	DO10T		A 8A 6
	VREFB8AN0	10			DIFFIO_TX_T151n	DIFFOUT_T151n	J31				A 8A 7
	VREEBBAND	lio		+	DIFFIO_TX_T15111	DIFFOUT T152p	C31	DQ20T	DQ10T	†	A 8A 8
	VREFB8AN0 VREFB8AN0	10		1	DIFFIO_RX_1152p	DIFFOUT_T152p	001		DQ10T	+	71_071_0
	VREFB8ANO VREFB8ANO	10		+			D31	DQ20T	DQ101 DQ10T	+	A_8A_9 A_8A_10
		IU	<u> </u>		DIFFIO_TX_T153p	DIFFOUT_T153p	OOL	DQ20T	DQ101	1	
	VREFB8AN0	10			DIFFIO_TX_T153n	DIFFOUT_T153n	D32	1	1	+	A_8A_11
	VREFB8AN0	10			DIFFIO_RX_T154p	DIFFOUT_T154p	N31	DQ21T	DQ10T	4	A_8A_12
	VREFB8AN0	10			DIFFIO_RX_T154n	DIFFOUT_T154n	P31	DQ21T	DQ10T	<u> </u>	A_8A_13
	VREFB8AN0	10			DIFFIO_TX_T155p	DIFFOUT_T155p	J32	DQ21T	DQ10T		A_8A_14
	VREFB8AN0	10			DIFFIO_TX_T155n	DIFFOUT_T155n	K32				A_8A_15
	VREFB8AN0	10			DIFFIO_RX_T156p	DIFFOUT_T156p	M32	DQ21T	DQ10T		BA 8A 0
	VREFB8AN0	10			DIFFIO_RX_T156n	DIFFOUT T156n	N32	DQ21T	DQ10T	1	BA 8A 1
	VREFB8AN0	in			DIFFIO_TX_T157p	DIFFOUT_T157p	J34	DQ21T	DQ10T	1	BA 8A 2
	VREFB8AN0	lio.	<u> </u>	+	DIFFIO_TX_T157p	DIFFOUT_T157p	K34	I Superior	54,01	1	RAS# 8A
		10						DOCOATICOCATICO-CATION-CAT	DOJOT	+	
	VREFB8AN0	10	<u> </u>	+	DIFFIO_RX_T158p	DIFFOUT_T158p	L33	DQS21T/CQ21T/CQn21T/QKn21T	DQ10T	+	CAS#_8A
		IIO			DIFFIO_RX_T158n	DIFFOUT_T158n	M33	DQSn21T/QK21T	DQ10T	+	WE#_8A
	VREFB8AN0	10		1	DIFFIO_TX_T159p	DIFFOUT_T159p	L31	DQ21T	DQ10T	1	ODT_8A_
	VREFB8AN0	IO				DIFFOUT T159n	M31	1		1	ODT_8A_
	VREFB8AN0 VREFB8AN0	IO IO			DIFFIO_TX_T159n						
	VREFB8AN0 VREFB8AN0 VREFB8AN0	10 10 10	CLK23p		DIFFIO_TX_T159n DIFFIO_RX_T160p	DIFFOUT_T160p	N34	DQ21T	DQ10T		
	VREFB8AN0 VREFB8AN0 VREFB8AN0	10 10 10	CLK23p CLK23n				N34 N33	DQ21T DQ21T	DQ10T DQ10T		
	VREFB8AN0 VREFB8AN0 VREFB8AN0 VREFB8AN0	IO	CLK23p CLK23n		DIFFIO_RX_T160p DIFFIO_RX_T160n	DIFFOUT_T160p DIFFOUT_T160n	N33	DQ21T	DQ10T		CS# 8A
	VREFB8AN0 VREFB8AN0 VREFB8AN0 VREFB8AN0 VREFB8AN0	10 10 10 10 10	CLK23p CLK23n		DIFFIO_RX_T160p DIFFIO_RX_T160n DIFFIO_TX_T161p	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161p	N33 L34				
	VREFB8AN0 VREFB8AN0 VREFB8AN0 VREFB8AN0 VREFB8AN0 VREFB8AN0 VREFB8AN0	10 10 10 10 10	CLK23n		DIFFIO_RX_T160p DIFFIO_RX_T160n DIFFIO_TX_T161p DIFFIO_TX_T161n	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161p DIFFOUT_T161n	N33 L34 M34	DQ21T DQ21T	DQ10T		
	VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO	10 10 10 10 10 10	CLK23n CLK22p		DIFFIO RX T160p DIFFIO RX T160n DIFFIO TX T161p DIFFIO TX T161n DIFFIO RX T162p	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161p DIFFOUT_T161n DIFFOUT_T162p	N33 L34 M34 E34	DQ21T DQ21T DQ22T	DQ10T		
	VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO	O	CLK23n		DIFFIO_RX_T160p DIFFIO_RX_T160n DIFFIO_TX_T161p DIFFIO_TX_T161n	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161p DIFFOUT_T161n	N33 L34 M34 E34 F34	DQ21T DQ21T DQ22T DQ22T	DQ10T		
	VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO	10 10 10 10 10 10 10 10 10 10 10 10 10 1	CLK22p CLK22p CLK22p		DIFFIO RX T160p DIFFIO RX T160n DIFFIO TX T161p DIFFIO TX T161n DIFFIO RX T162p	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161p DIFFOUT_T161n DIFFOUT_T162p	N33 L34 M34 E34 F34 J33	DQ21T DQ21T DQ22T	DQ10T		
	VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO	O	CLK23n CLK22p		DIFFIO RX T160p DIFFIO RX T160n DIFFIO TX T161p DIFFIO TX T161n DIFFIO RX T162p	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161p DIFFOUT_T161n DIFFOUT_T162p	N33 L34 M34 E34 F34	DQ21T DQ21T DQ22T DQ22T	DQ10T		
	VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO	IO	CLK23n CLK22p CLK22b VREFB8AN0		DIFFIO RX T160p DIFFIO RX T160n DIFFIO TX T161p DIFFIO TX T161n DIFFIO RX T162p DIFFIO RX T162n	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161p DIFFOUT_T161n DIFFOUT_T162p DIFFOUT_T162n	N33 L34 M34 E34 F34 J33 H33	DQ21T DQ21T DQ22T DQ22T DQ22T DQ22T	DQ10T		
	VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO	O	CLK22p CLK22p CLK22h VREFB8ANO FPLL_TL_CLKOUT2,FPLL_TL_FBp,FPLL_TL_FB1		DIFFIO RX T160p DIFFIO RX T160n DIFFIO TX T161p DIFFIO TX T161p DIFFIO TX T161p DIFFIO RX T162p DIFFIO RX T162p DIFFIO RX T162n DIFFIO RX T163p	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161p DIFFOUT_T161p DIFFOUT_T162p DIFFOUT_T162n DIFFOUT_T162n	N33 L34 M34 E34 F34 J33 H33	DQ21T DQ21T DQ22T DQ22T DQ22T DQ22T DQ22T	DQ10T		
	VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO	10	CLK22h CLK22h VREFB8AN0 VRLFB8AN0 FPLL TL CLKOUT2,FPLL_TL_FB,FPLL_TL_FB1 FPLL TL CLKOUT3,FPLL_TL_FB		DIFFIO RX T160p DIFFIO RX T160n DIFFIO TX T161n DIFFIO TX T161n DIFFIO TX T161n DIFFIO RX T162p DIFFIO RX T162p DIFFIO RX T163p DIFFIO RX T163p	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161n DIFFOUT_T161n DIFFOUT_T162p DIFFOUT_T162n DIFFOUT_T163p DIFFOUT_T163p DIFFOUT_T163n	N33 L34 M34 E34 F34 J33 H33 B34 A35	D021T D021T D022T D022T D022T D022T D022T D022T	DQ10T		
	VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO VREFBBANO	O	CLK22p CLK22p VREFBBAN0 FPIL TL CLKOUT2.FPIL TL FBp,FPIL TL FB1 FPIL TL CLKOUT5.FPIL TL FBn FPIL TL CLKOUT5.FPIL TL FBn FPIL TL CLKOUT5.FPIL TL FBn		DIFFIO RX T160p DIFFIO RX T160n DIFFIO TX T161p DIFFIO TX T161p DIFFIO RX T162p DIFFIO RX T162p DIFFIO RX T162p DIFFIO RX T163p DIFFIO RX T163p DIFFIO RX T163n DIFFIO TX T164p	DIFFOUT_T160p DIFFOUT_T160p DIFFOUT_T161p DIFFOUT_T161f DIFFOUT_T161n DIFFOUT_T162p DIFFOUT_T162p DIFFOUT_T162n DIFFOUT_T163p DIFFOUT_T163p DIFFOUT_T163n DIFFOUT_T164p	N33 L34 M34 E34 F34 J33 H33 B34 A35 C33	DQ21T DQ21T DQ22T DQ22T DQ22T DQ22T DQ22T	DQ10T		
	VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO VREFB8ANO	O	CLK22h CLK22h VREFB8AN0 VRLFB8AN0 FPLL TL CLKOUT2,FPLL_TL_FB,FPLL_TL_FB1 FPLL TL CLKOUT3,FPLL_TL_FB		DIFFIO RX T160p DIFFIO RX T160n DIFFIO TX T161n DIFFIO TX T161n DIFFIO TX T161n DIFFIO RX T162p DIFFIO RX T162p DIFFIO RX T163p DIFFIO RX T163p	DIFFOUT_T160p DIFFOUT_T160n DIFFOUT_T161n DIFFOUT_T161n DIFFOUT_T162p DIFFOUT_T162n DIFFOUT_T163p DIFFOUT_T163p DIFFOUT_T163n	N33 L34 M34 E34 F34 J33 H33 B34 A35	D021T D021T D022T D022T D022T D022T D022T D022T	DQ10T		CS# 8A (CS# 8A 1

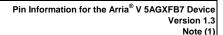


		□ 4.									Note (1
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
A	VREFB8AN0	IO			DIFFIO_TX_T166p	DIFFOUT_T166p	F32	DQ22T			1111 13/
A	VREFB8AN0	10			DIFFIO_TX_T166n	DIFFOUT_T166n	G32				T
A	VREFB8AN0	IO	CLK20p		DIFFIO_RX_T167p	DIFFOUT_T167p	C34	DQ22T			
A	VREFB8AN0	IO	CLK20n		DIFFIO_RX_T167n	DIFFOUT_T167n	D34	DQ22T			
A	VREFB8AN0				DIFFIO_TX_T168p	DIFFOUT_T168p	E33	DQ22T			↓
A	VREFB8AN0		RZQ_6		DIFFIO_TX_T168n	DIFFOUT_T168n	F33				
BA BA		MSEL0		MSEL0			H35				+
SA BA		MSEL1 MSEL2		MSEL1 MSEL2	1		A34 D35				+
BA .		MSEL3		MSEL3			A37				+
BA.		MSEL4		MSEL4			P34				+
BA .		CONF_DONE		CONF_DONE			K35				†
BA		nSTATUS		nSTATUS			F35				1
BA .		nCE		nCE			M35				
BA		nCONFIG		nCONFIG			A36				
BA		GND					P35				
		GND					AA33				
		GND					AA35				+
		GND GND					AA38 AA39				+
		GND					AB31				+
	i	GND GND		1			AB31 AB32		 	†	†
	i	GND		1	1	1	AB34			İ	1
		GND					AB36			İ	1
		GND		<u> </u>	<u> </u>		AB37				
		GND					AC33				
		GND		ļ	ļ	ļ	AC38				1
		GND					AC39			1	4
		GND					AD30				+
		GND					AD32				+
		GND GND					AD36 AD37				+
		GND					AE33				+
		GND					AE35				+
		GND					AE38				1
		GND					AE39				1
		GND					AF31				
		GND					AF32				
		GND			ļ		AF34				
		GND					AF36				
		GND					AF37				+
		GND GND					AG38 AG39				+
		GND					AH32				+
		GND					AH33				+
		GND					AH34				1
		GND					AH35				1
		GND					AH36				
		GND					AH37				
		GND			ļ		AJ35				
		GND					AJ38				+
		GND					AJ39				+
	1	GND GND		1	1	1	AK36 AK37	 	1	1	+
	l .	GND	1	 	 	 	AL35	 	 	 	+
	i	GND		1			AL35		 	†	†
	İ	GND	İ	İ	1		AL39			İ	1
		GND		<u> </u>	İ		AM36				
		GND					AM37				
		GND					AN35				1
		GND					AN38			1	
		GND					AN39			1	4
	1	GND	ļ	1	1	1	AP36		ļ	 	+
	-	GND GND		 	1		AP37 AR35	 	 	1	+
		GND		<u> </u>	<u> </u>		AR35 AR38			1	+
	1	GND		1	1	1	AR39				†
		GND					AT36				1
	İ	GND	İ	İ	1		AT37			İ	1
		GND					AU35				
		GND					AU38				
		GND					AU39				1
		GND		1	1		AV35				1
		GND					AV36				
		GND		 	1	ļ	AV37				+
		GND GND		_	_		AV38 AV39	-	-		+
	1	GND		+	+	1	AV39 AW35	 	 	1	+
		OND	l	1	1			ļ		I	4
		GND					VM 38				
		GND GND					AW38 B36				+





Mathematical Math												Note (1)
POC	Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	hard memory
COC												
			GND					C38				
			GND					D36				+
												1
150 150			GND					E35				
			GND					E38				
1												+
100 100			GND					F37				
			GND					G35				
			GND					H36				+
Main Main			GND					H37				1
SCO												
Second			GND					J38				+
Second												1
Oct			GND					K37				
Second			GND					L35				
GSC			GND			 						+
Second			GND			†		M36				+
			GND			<u> </u>		M37				1
COD			GND					N35				
OCC			GND					N38				
GOC GOC						1						+
DOC DOC			GND					P37				
QSC			GND									1
Dec												+
			GND					T32				+
OBD			GND					T36				1
			GND									1
OSD												+
OND OND			GND					U35				+
0.00			GND					U39				
OND OND			GND									
QND QND			GND					V34				
ONO WIS WIS WIS			GND									+
GND W39 W39			GND					W33				
SND			GND					W38				
GND												+
GND			GND					Y32				+
OND OND			GND					Y36				1
GND A3												
SND SND			GND					A2				
SND NAS <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td>A4</td> <td></td> <td></td> <td></td> <td>1</td>								A4				1
OND OND			GND					A5				1
SND SND			GND	<u> </u>	1	ļ		AA3	ļ	ļ		+
GND			GND			+		AA4 AA6				+
GND			GND		<u> </u>	<u> </u>			<u> </u>		<u> </u>	1
SAD SAT			GND					AB1				
SND			GND					AB2				
SAD			GND GND			1		AB7 AC3	 	 		+
SAD						†						+
SND SND			GND					AC8				1
SND SND			GND					AD1				
SND SND			GND			1			 	 		+
SND SND			GND			†		AD5				+
SND			GND					AD7				<u> </u>
GND			GND					AE3				
GND						 						+
GND			GND			†		AE6 AF8				+
GND			GND		<u> </u>	<u> </u>		AF1	<u> </u>		<u> </u>	
GND			GND					AF2				
GND AG4 GND AG5	-		GND					AF9				
GND AG5						+						+
			GND			†		AG5				+





		□ 4.									Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		GND					AG7				1 111 107
		GND					AG8				
		GND					AH1				
		GND					AH2				
		GND					AH5				
		GND			-		AJ3				1
		GND GND					AJ4 AK1				1
		GND					AK2				
		GND					AK5				1
		GND					AL3				
		GND					AL4				
		GND					AM1				
		GND					AM2				
		GND					AM5				
		GND					AN3				
		GND					AN4 AP1				
		GND GND					AP1 AP2				1
		GND					AP5				1
		GND					AR3				
		GND					AR4				
		GND	İ	İ	1		AT1				İ
		GND					AT2			<u> </u>	
		GND					AT5				
		GND			1		AU3				
	ļ	GND		ļ	1		AU4				<u> </u>
		GND	ļ	1	+		AV1			ļ	
		GND GND					AV2 B1				1
		GND					B1 B2				1
		GND					B5				
		GND					C3				
		GND					C4				
		GND					D1				
		GND					D2				
		GND					D5				
		GND					E3				
		GND					E4				
		GND					F1				
		GND					F2				
		GND GND					F5 G3				
		GND					G4				
		GND					H1				1
		GND					H2				
		GND					H5				1
		GND					J3				
		GND					J4				
		GND					K1				
		GND					K2				
	 	GND		 	1	-	K5				
	l	GND GND		1	+	1	L3 L4				1
	l	GND		1	+		L4 M1				1
	1	GND		1	+		M2			<u> </u>	1
		GND	İ	İ	1		M5				İ
		GND					N3				
		GND					N4				
		GND					N5				
		GND		ļ	1		P1				
		GND		ļ			P2				<u> </u>
	 	GND	ļ	1	+	1	P6			ļ	1
	 	GND		 	 		P7				
	 	GND GND		 	 		R3 R4				
		GND	1	 	†		R8			 	
	l	GND		1	†	1	T1				1
	i	GND		İ	İ		T10				i e
		GND		İ			T2				İ
		GND					T5				
		GND GND					T7				
		GND					U3				
		GND		1			U4				
	ļ	GND		ļ			U6				<u> </u>
	ļ	GND GND		ļ	_		U8				
	ļ	GND	1	ļ	-		V1				
	 	GND	ļ	1	+	1	V2			-	1
	 	GND		 	+	 	V7 W3				
		GND GND		 	+		W3 W4			-	-
	i	טאט		1		ı	vV 4	l .	l	l .	





											Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		GND					W8				1 111 (0)
		GND					Y1				
		GND GND					Y2 Y5				+
		GND					Y7				
		VCCP					AA21				
		VCCP					AA25				
		VCCP VCCP					AB15 U16				+
		VCCP					V13				
		VCCP					V22				
		VCCP					V25				
		VCCP VCCP					V27 Y13				-
		VCCP					Y27				
		VCCA_FPLL					AC30				
		VCCA_FPLL VCCA_FPLL					AC9 Y30				
		VCCA_FPLL VCCA_FPLL					AA9				-
		VCCA_FPLL					V31				
		VCCA_FPLL					U9				
		VCCBAT VCC_AUX			 		R33 AB14				
		VCC_AUX		1	†		AB14 AB26		1		
		VCC_AUX			<u> </u>		U14			<u> </u>	1
		VCC_AUX					U28				
		VCCD_FPLL VCCD_FPLL	<u> </u>	1	ļ		AD31 AE9	ļ	-		1
		VCCD_FPLL VCCD_FPLL		1	†		W30	<u> </u>			†
		VCCD_FPLL					W9				
		VCCD_FPLL					T31				
		VCCD_FPLL					R9				
		VCCA_GXBL0 VCCA_GXBR0					AF33 AE7				
		VCCA_GXBL1					AB33				
		VCCA_GXBR1					AA7				
		VCCA_GXBL2					V33				
		VCCA_GXBR2 VCCH_GXBL0					U7 AD33				
		VCCH_GXBE0					AC7				-
		VCCH_GXBL1					Y33				
		VCCH_GXBR1					W7				
		VCCH_GXBL2					T33 R7				
		VCCH_GXBR2 VCCL_GXBL0					AD34				
		VCCL_GXBL0					AD35				
		VCCL_GXBR0					AC5				
		VCCL_GXBR0					AC6				
		VCCL_GXBL1 VCCL_GXBL1					Y34 Y35				+
		VCCL_GXBR1					W5				
		VCCL_GXBR1					W6				
		VCCL_GXBL2					T34				1
		VCCL_GXBL2 VCCL_GXBR2		-	1		T35 R5	 			+
		VCCL_GXBR2 VCCL_GXBR2			İ		R6				†
		VCCR_GXBL					AC34				
		VCCR_GXBL					AC35				1
		VCCR_GXBL			 		AG34				
		VCCR_GXBL VCCR_GXBL		1	†		AG35 R35	<u> </u>			†
		VCCR_GXBL					W34				1
		VCCR_GXBL					W35				
		VCCR_GXBR					AB5				1
		VCCR_GXBR VCCR_GXBR			+		AB6 AF5				+
		VCCR_GXBR VCCR_GXBR			İ		AF6				†
		VCCR_GXBR					P5				
		VCCR_GXBR					V5				
		VCCR_GXBR VCCT_GXBL0			+		V6 AE34				+
		VCCT_GXBL0			1		AE34 AF35				1
		VCCT_GXBR0					AD6				
		VCCT_GXBR0					AE5				1
		VCCT_GXBL1	<u> </u>		 		AA34 AB35				+
		VCCT_GXBL1 VCCT_GXBR1		1	†		AB35 AA5				1
		VCCT_GXBR1		<u> </u>	<u> </u>		Y6	<u> </u>		<u> </u>	İ
		VCCT_GXBL2					U34				
		VCCT_GXBL2 VCCT_GXBR2					V35				
							T6	1	1	i	





		·									Note (1)
Bank Number	VREF	PinName/Function (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2 hard memory PHY (3)
		VCCT_GXBR2					U5				
		VCC					AA10				
		VCC					AA12				
		VCC					AA14				+
		vcc vcc					AA16 AA18				+
		VCC					AA20				1
		VCC					AA22				1
		VCC					AA24				
		VCC					AA26				
	-	VCC VCC					AB11 AB17				
		VCC					U10				+
		VCC					U12				1
		VCC					V11				1
		VCC					V15				
		VCC VCC					V17 V23				4
		VCC					V23 V29				+
		VCC					W10				†
		VCC					W12				1
		VCC					W14				
		VCC			ļ		W16				4
		VCC	<u> </u>	 	 		W18	 	 		+
	1	vcc vcc		1	}	-	W20 W22	 	 		+
	1	VCC		 	1		W24				+
		VCC		İ	<u> </u>		W26	<u> </u>			1
		VCC					W28				
		VCC					Y11				
		VCC					Y15				
		VCC					Y17 Y19				+
		VCC VCC					Y23				+
		vcc					Y25				+
		VCC					Y29				
		VCC					Y21				
		VCCIO3A					AH29				
		VCCIO3A					AJ30				
	1	VCCIO3A VCCIO3A					AK35 AM30				+
		VCCIOSA VCCIOSA					AP35				+
		VCCIO3A					AT35				1
		VCCIO3B					AK28				
		VCCIO3B					AL27				
		VCCIO3B					AN28				
		VCCIO3B VCCIO3C					AT28 AJ24				+
		VCCIOSC					AL25				+
		VCCIO3C					AM24				+
		VCCIO3C					AP25				
		VCCIO3C					AR24				
		VCCIO3C			ļ		AU25				
	-	VCCIO3D VCCIO3D			 		AJ22 AL21				+
		VCCIO3D VCCIO3D		1	1		AL21 AM22	1	1		+
		VCCIO3D			1		AP21				1
		VCCIO3D					AR22				
		VCCIO3D					AU21				
		VCCIO4A					AG10				
	1	VCCIO4A	<u> </u>	 	 		AJ5	 	 		+
	-	VCCIO4A VCCIO4A			-		AL5 AN5	-	 	-	+
		VCCIO4A VCCIO4A	 	 	 		AR5	 	 	 	+
		VCCIO4A			İ		AU5				1
		VCCIO4B					AK13				
		VCCIO4B					AM12				1
	-	VCCIO4B					AN10				4
	-	VCCIO4B VCCIO4B			 		AN13 AR12				+
		VCCIO4B VCCIO4B		1	1	 	AR12 AT10	 	1		+
		VCCIO4B VCCIO4C					AJ15				+
		VCCIO4C			Ì		AM15				1
		VCCIO4C					AR15				1
		VCCIO4C					AV15				
		VCCIO4D					AJ19				4
		VCCIO4D		ļ	ļ		AK18 AM19				+
		VCCIO4D VCCIO4D			-	-	AM19 AN18	 	 	 	+
	1	VCCIO4D VCCIO4D	1		†		AR19	1	1		+
		VCCIO4D	İ		İ		AT18				1
							_	-			





VREF PinName/Function (2) Optional Function(s) Configuration Dedicated Tx/Rx Emulated LVDS F1517 DQS for X8/X9 DQS for X16/ X18 DQS for X32/ X36 DDR3/DDR2 Function Channel Output Channel hard memory PHY (3) VCCIO7A VCCIO7A VCCIO7A VCCIO7A VCCIO7A VCCIO7A VCCIO7B VCCIO7B VCCIO7B VCCIO7B VCCIO7B K10 VCCIO7B I 13 VCCIO7C VCCIO7C G15 VCCIO7C K15 VCCIO7C I 16 VCCIO7D VCCIO7D VCCIO7D VCCIO7D VCCIO7D VCCIO7D VCCIO8A M18 VCCIO8A G31 VCCIO8A VCCIO8A G33 VCCIO8A K33 VCCIO8A VCCIO8B VCCIO8B VCCIO8B VCCIO8B VCCIO8C C25 VCCIO8C VCCIO8C VCCIO8C VCCIO8C VCCIO8C VCCIO8D M24 VCCIO8D VCCIO8D VCCIO8D G22 VCCIO8D K22 VCCIO8D VCCPD3 AA27 VCCPD3 AA28 VCCPD3 VCCPD3 AA29 AB22 VCCPD3 AB23 VCCPD3 AB24 VCCPD4A AC10 VCCPD4A AE10 VCCPD4BCD VCCPD4BCD AB12 AB13 VCCPD4BCD AB16 VCCPD4BCD VCCPD4BCD AB18 AB19 VCCPD7A VCCPD7A VCCPD7BCD VCCPD7BCD VCCPD7BCD VCCPD7BCD 1118 VCCPD7BCD 1119 VCCPD8 VCCPD8 T30 VCCPD8 U21 VCCPD8 VCCPD8 VCCPD8 VCCPD8 VCCPGM VCCPGM AG29 GND GND GND AA11 AA13 AA15 AA17 GND GND GND AA19 AA23





Dedicated Tx/Rx DDR3/DDR2 VREF PinName/Function (2) Optional Function(s) Configuration Emulated LVDS F1517 DQS for X8/X9 DQS for X16/ X18 DQS for X32/ X36 Function Channel Output Channel hard memory PHY (3) GND AB10 GND GND GND AC11 AC14 AC17 GND AC20 GND AC23 AC26 GND AC28 GND GND AE30 AF11 GND AF14 GND GND AF17 AF20 GND AF23 GND GND GND AF26 AF29 AF30 GND GND GND AG31 GND GND GND AJ17 A.120 GND AJ23 GND GND AJ26 AJ29 GND AJ32 GND GND AJ8 AM11 GND AM14 GND AM17 AM20 GND AM23 GND GND GND AM26 AM29 AM32 GND AM8 GND GND AR11 GND AR17 GND AR23 GND AR26 GND AR29 AR32 AR8 GND GND AV11 AV14 GND AV17 GND AV20 GND AV26 GND GND GND AV29 AV32 GND GND GND AV8 B11 B14 GND GND GND GND GND GND B32 GND GND E14 GND E17 GND GND GND GND GND GND GND GND GND H14 H17 GND GND GND



Pin Information for the Arria® V 5AGXFB7 Device Version 1.3

Note (1)

											Note (1)
Bank	VREF	PinName/Function (2)	Optional Function(s)	Configuration	Dedicated Tx/Rx	Emulated LVDS	F1517	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	DDR3/DDR2
Number		• • •	, , , , , , , , , , , , , , , , , , , ,	Function	Channel	Output Channel					hard memory
											PHY (3)
		GND					H32				
		GND					H8				
		GND					L11				
		GND					L14				
		GND					L17				
		GND					L20				
		GND					L23				
		GND					L26				
		GND					L29	İ			
		GND					L32	İ			
		GND					18	İ			
		GND					N8				
		GND					P11				
		GND					P14				
		GND					P17				
-		GND		1	†	1	P20	†		†	+
\vdash		GND		1	+	-	P20 P23			 	+
\vdash		GND		1	+	-	P23			 	+
H +		GND		1	1	ł	P29	1		 	+
\vdash				 	 		P29 P32	+		}	+
\vdash		GND GND		 	 		P32	+		}	+
\vdash				 	 			+		}	+
		GND					U13				
		GND					U15				
		GND					U17				
		GND					U20				
		GND					U23				
		GND					U25				
		GND					U27				
		GND					U30				
		GND					V10				
		GND					V12				
		GND					V14				
		GND					V16				
		GND					V18				
		GND					V21				
		GND					V24				
		GND					V26				
		GND					V28				
		GND					V30				
		GND					W11				
		GND					W13				
		GND		İ	İ		W15			İ	
		GND		İ	İ		W17			İ	
		GND			1		W19	<u> </u>		†	1
		GND			1		W23	<u> </u>		†	1
		GND			1		W25	<u> </u>		†	1
\vdash		GND		 	1		W27	†		†	+
\vdash		GND		 	1		W29	†		†	+
 		GND		+	1		Y10	<u> </u>		†	+
\vdash		GND		1	+	-	Y10 Y12			 	+
\vdash		GND		1	+	-	Y12 Y14			 	+
\vdash		GND GND		1	+	-	Y14 Y16			 	+
\vdash				 	 			+		}	+
\vdash		GND		ļ	+	-	Y18	+	 	 	+
\vdash		GND					Y20	ļ		ļ	-
\vdash		GND					Y22	ļ		ļ	1
\vdash		GND					Y24	ļ		ļ	1
\vdash		GND			<u> </u>		Y26			ļ	1
		GND			<u> </u>		Y28			ļ	1
		GND					W21	1			

Notes:

(1) For more information about pin definitions and pin connection guidelines, refer to the
Arria V Device Family Pin Connection Guidelines.

(2) GXB_REFCLK pin is not supported in current Cuartus II version, but will be supported in future Quartus II release version.

(3) RESET pin is only applicable for DDR3 device.



Pin Information for the Arria[®] V 5AGXFB7 Device Version 1.3

Version Number	Date	Changes Made
1.0	11/4/2011	Preliminary release.
1.1	1/3/2012	Split VCC to VCC and VCCP
1.2	5/11/2012	- Removed Preliminary - Rename the CQ pins in DQS and hard memory PHY columns
1.3	7/31/2015	Removed LPDDR2 hard memory PHY, RLDRAMII hard memory PHY, and QDRII hard memory PHY columns.