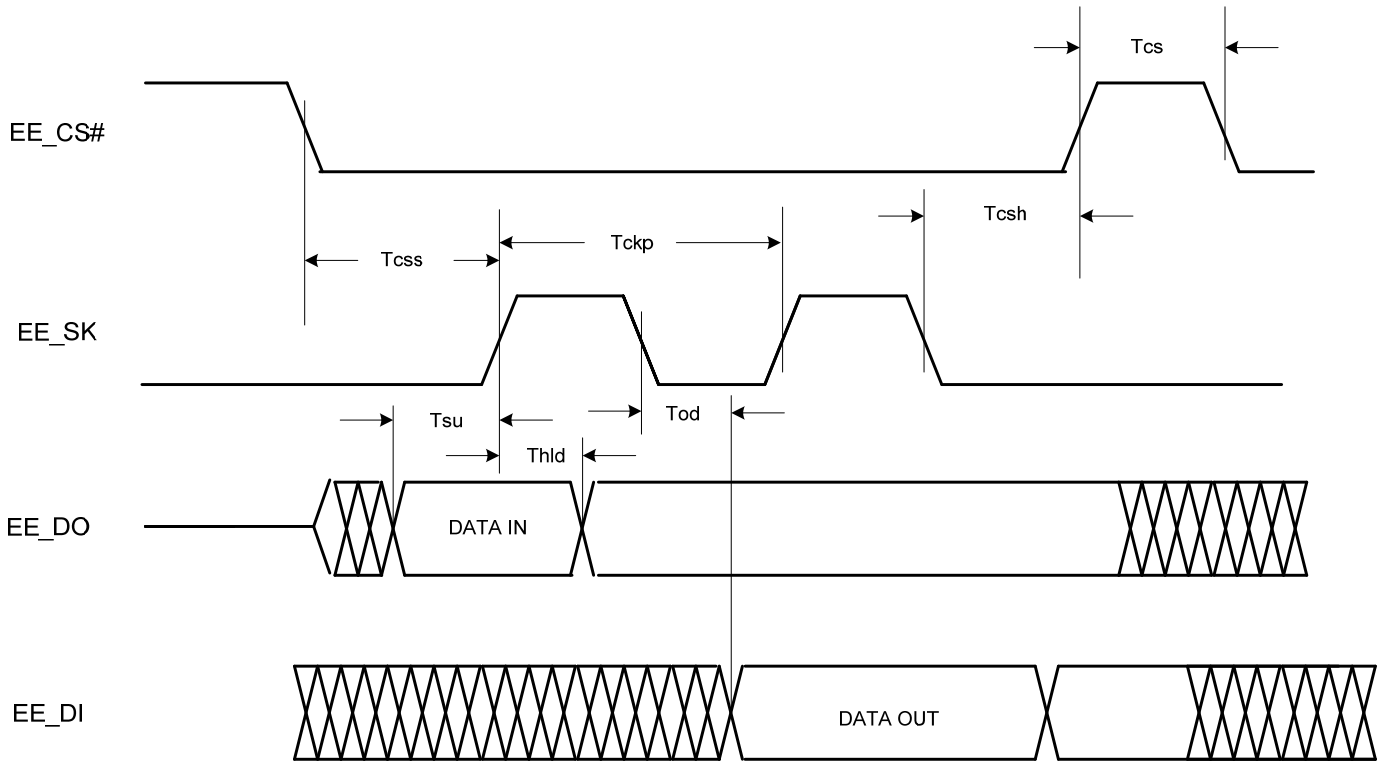
1 Disclaimer

This note is a compilation of timing specifications for the listed synchronous interfaces. Timing parameters are worse case extractions estimations from a gate-level design. These values are intended as general reference and as such, are not guaranteed specification nor measured as part silicon validation/verification. While these interfaces tend to have significant signal margin, it is advised the user stay within these guidelines.

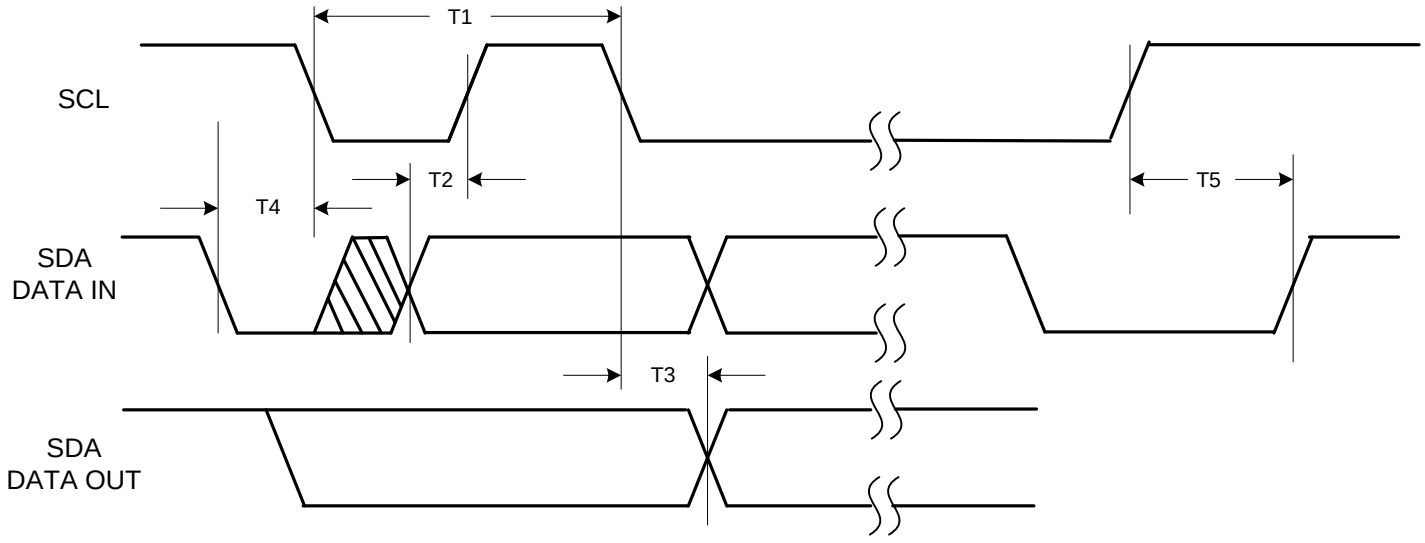
2 EEPROM Interface Timing Specifications

Parameter	Name	Min	Max	Units	Notes
EE_SK Clock Period	Tckp	56	1000	ns	Programmable to meet external device needs
EE_DO Data input to EE_SK setup time	Tsu	12		ns	
EE_SK Rising edge to EE_DO data input hold time	Thld	4		ns	
EE_SK Falling edge to EE_DI output data stable	Tod		12	ns	
EE_CS# falling edge to EE_SK rise edge	Tcss	(1/2*Tckp) -8		ns	This is programmable in increments of 1/2 Tckp
EE_SK falling edge to EE_CS# rising edge hold time	Tcsh	(1/2*Tckp) -8		ns	This is programmable in increments of 1/2 Tckp
EE_CS# high time	Tcs	(1/2*Tckp) -8		ns	This is programmable in increments of 1/2 Tckp



3 I2C Interface Timing Specifications

Parameter	Name	Min	Max	Units
Serial Clock Period	T1	10		us
Data In setup time to SCL high	T2	60		ns
Data Out Stable after SCL low	T3		80	ns
SDA low setup time to SCL low (Start Condition)	T4	100		ns
SDA Hold time after SCL high (Stop condition)	T5	60		ns



4 JTAG Interface Timing Specifications

Parameter	Name	Min	Max	Units
JTAG_TCK Clock Period	Tjcp	50		ns
JTAG_TMS/JTAG_TDI input to TCK setup time	Tjpsu	0.457		ns
JTAG_TMS/JTAG_TDI input to TCK hold time	Tjph	13.51		ns
JTAG_TDO high impedence to valid output from fall edge of JTAG_TCK (50 pf load)	Tjpzx		5.97	ns
JTAG_TCK falling edge to JTAG_TDO data valid	Tjpco		4.3	ns