The pin connection guidelines in the device pin-out are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification. The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B1	VREFB1N0	VCCD_PLL3			1	F5	F6	J9										
B1	VREFB1N0	GNDA3			2	E5	F5	H9										
B1	VREFB1N0	VCCA3			3	E4	G6	J8										
B1	VREFB1N0	IO	DIFFIO_L1p			B2	G4	D3		DQ1L	DQ1L							Adj.
B1	VREFB1N0	IO	DIFFIO_L1n			B1	G3	C2							DQ2L	DQ1L	DQ1L	Adj.
B1	VREFB1N0	VCCINT			4													
B1	VREFB1N0	GND			5													
B1	VREFB1N0	IO						M9										
B1	VREFB1N0	IO	DIFFIO_L2p				B2	D2				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Sep.
B1	VREFB1N0	IO	DIFFIO_L2n				B1	D1				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Sep.
B1	VREFB1N0	IO	VREFB1N0		6	C2	G5	H7										
B1	VREFB1N0	IO	DIFFIO_L3p					E5										Adj.
B1	VREFB1N0	IO	DIFFIO_L3n			C1		E4		DQ1L	DQ1L							Adj.
B1	VREFB1N0	IO	DIFFIO_L4p	nRESET		C3	E4	G6				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Adj.
B1	VREFB1N0	IO	DIFFIO_L4n				E3	G5				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Adj.
B1	VREFB1N0	IO	DIFFIO_L5p					H4										Adj.
B1	VREFB1N0	IO	DIFFIO_L5n					H3										Adj.
B1	VREFB1N0	IO	DIFFIO_L6p					J5										Sep.
B1	VREFB1N0	VCCIO1			7													
B1	VREFB1N0	IO	DIFFIO_L6n					G7										Sep.
B1	VREFB1N0	GND			8													
B1	VREFB1N1	IO	DIFFIO_L7p		9	D3	C2	E3	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	DQS2L/CQ3L, CDPCLK0	Sep.
B1	VREFB1N1	VCCINT			10													
B1	VREFB1N1	IO	DIFFIO_L7n				C1	F3				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Sep.
B1	VREFB1N1	GND			11													
B1	VREFB1N1	IO	DIFFIO_L8p			D2	D2	F5		DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Adj.
B1	VREFB1N1	IO	DIFFIO_L8n	DATA1, ASDO	12	D1	D1	F4										Adj.
B1	VREFB1N1	IO	VREFB1N1		13	F3	H7	L5										
B1	VREFB1N1	IO	DIFFIO_L9p				H6	G4				DQ2L	DQ1L	DQ1L	DQ2L	DQ1L	DQ1L	Adj.
B1	VREFB1N1	IO	DIFFIO_L9n				J6	G3				DQ2L	DQ1L	DQ1L				Adj.
B1	VREFB1N1	IO	DIFFIO_L10p	FLASH_nCE, nCSO	14	E2	E2	E2										Adj.
B1	VREFB1N1	IO	DIFFIO_L10n			E1	E1	J6		DQ1L	DQ1L		DQ1L	DQ1L				Adj.
B1	VREFB1N1	IO	DIFFIO_L11p					E1								DQ1L	DQ1L	Adj.
B1	VREFB1N1	IO	DIFFIO_L11n					J7										Adj.
B1	VREFB1N1	IO	DIFFIO_L12p				F2	F2				DM2L	DM1L0/BWS#1L0	DM1L0/BWS#1L0	DM2L	DM1L0/BWS#1L0	DM1L0/BWS#1L0	Sep.
B1	VREFB1N1	IO	DIFFIO_L12n				F1	F1				DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	Sep.
B1	VREFB1N1	IO	DIFFIO_L13p					K4										Adj.
B1	VREFB1N1	IO	DIFFIO_L13n					K3										Adj.
B1	VREFB1N1	IO	DIFFIO_L14p				H8	K7										Adj.
B1	VREFB1N1	IO	DIFFIO_L14n				J8	L6										Adj.
B1	VREFB1N1	IO	DIFFIO_L15p					L8										Adj.
B1	VREFB1N2	IO	DIFFIO_L15n					L7										Adj.
B1	VREFB1N2	IO	DIFFIO_L16p					M8										Adj.
B1	VREFB1N2	IO	DIFFIO_L16n					M7										Adj.
B1	VREFB1N2	VCCIO1			15													
B1	VREFB1N2	IO	DIFFIO_L17p					L4										Sep.
B1	VREFB1N2	GND			16													
B1	VREFB1N2	IO	DIFFIO_L17n					L3										Sep.
B1	VREFB1N2	IO	DIFFIO_L18p					H6										Adj.
B1	VREFB1N2	IO	DIFFIO_L18n				J5	H5										Adj.
B1	VREFB1N2	IO	DIFFIO_L19p					J4										Adj.
B1	VREFB1N2	IO	DIFFIO_L19n					J3							DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N2	nSTATUS		nSTATUS	17	G5	K6	M6										
B1	VREFB1N2	IO	VREFB1N2		18	H6	H5	N8										
B1	VREFB1N2	VCCINT			19													
B1	VREFB1N2	IO	DIFFIO_L20p			G2	L8	G2		DQ1L	DQ1L				DQ0L	DQ1L	DQ1L	Sep.
B1	VREFB1N2	GND			20													
B1	VREFB1N2	IO	DIFFIO_L20n			G1	K8	G1		DQ1L	DQ1L							Sep.
B1	VREFB1N2	IO	DIFFIO_L21p				J7	M3										Adj.
B1	VREFB1N2	IO	DIFFIO_L21n				K7	K1							DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N2	IO	DIFFIO_L22p					N4										Adj.
B1	VREFB1N2	IO	DIFFIO_L22n					N3										Adj.
B1	VREFB1N3	IO						M4										
B1	VREFB1N3	IO			21	H2	J4	K2	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	DQS0L/CQ1L, DPCLK0	

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B1	VREFB1N3	IO	DIFFIO_L23p				H2	L2				DQ0L	DQ1L	DQ1L				Adj.
B1	VREFB1N3	IO	DIFFIO_L23n				H1	L1				DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N3	IO	VREFB1N3		22	H1	J3	M5										
B1	VREFB1N3	IO	DIFFIO_L24p				J2	M2				DQ0L	DQ1L	DQ1L				Adj.
B1	VREFB1N3	IO	DIFFIO_L24n				J1	M1				DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N3	IO	DIFFIO_L25p					P2										Adj.
B1	VREFB1N3	IO	DIFFIO_L25n					P1							DQ0L	DQ1L	DQ1L	Adj.
B1	VREFB1N3	DCLK		DCLK	23	H4	K2	P3										
B1	VREFB1N3	IO		DATA0	24	H3	K1	N7										
B1	VREFB1N3	nCONFIG		nCONFIG	25	H5	K5	P4										
B1	VREFB1N3	TDI		TDI	26	J6	L5	P7										
B1	VREFB1N3	TCK		TCK	27	J1	L2	P5										
B1	VREFB1N3	TMS		TMS	28	J2	L1	P8										
B1	VREFB1N3	TDO		TDO	29	J5	L4	P6										
B1	VREFB1N3	nCE		nCE	30	K6	L3	R8										
B1	VREFB1N3	CLK0	DIFFCLK_0p		31	F2	G2	J2										
B1	VREFB1N3	CLK1	DIFFCLK_0n		32	F1	G1	J1										
B2	VREFB2N0	CLK2	DIFFCLK_1p		33	N2	T2	Y2										
B2	VREFB2N0	CLK3	DIFFCLK_1n		34	N1	T1	Y1										
B2	VREFB2N0	IO	DIFFIO_L26p			K2	L6	R2		DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	DQ0L	DQ1L	DQ1L	Sep.
B2	VREFB2N0	VCCIO2			35													
B2	VREFB2N0	IO	DIFFIO_L26n			K1	M6	R1		DQ1L	DQ1L	DQ0L	DQ1L	DQ1L		DQ1L	DQ1L	Sep.
B2	VREFB2N0	GND			36													
B2	VREFB2N0	IO	DIFFIO_L27p				M2	U3				DQ0L	DQ1L	DQ1L	DM0L	DM1L1/BWS#1L1	DM1L1/BWS#1L1	Adj.
B2	VREFB2N0	IO	DIFFIO_L27n				M1	U2					DQ1L	DQ1L				Adj.
B2	VREFB2N0	IO	DIFFIO_L28p		37	K5	M4	R3	DQ1L	DQ1L	DQ1L	DM0L	DM1L1/BWS#1L1	DM1L1/BWS#1L1	DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0	IO	DIFFIO_L28n		38	L5	M3	R6	DQ1L	DM1L/BWS#1L	DM1L0/BWS#1L0	DQ1L	DQ3L	DQ1L				Adj.
B2	VREFB2N0	IO	DIFFIO_L29p				N2	R4				DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0	IO	DIFFIO_L29n				N1	R7				DQ1L	DQ3L	DQ1L				Adj.
B2	VREFB2N0	IO	DIFFIO_L30p					T4							DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0	IO	DIFFIO_L30n				L7	T3										Adj.
B2	VREFB2N0	IO	VREFB2N0		39	L6	M5	T8										
B2	VREFB2N0	IO	DIFFIO_L31p					U4										Adj.
B2	VREFB2N0	IO	DIFFIO_L31n					R5							DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N0	VCCINT			40													
B2	VREFB2N0	IO	DIFFIO_L32p		41	L2	P2	U1	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	Sep.
B2	VREFB2N0	GND			42													
B2	VREFB2N0	IO	DIFFIO_L32n			L1	P1	V4		DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	Sep.
B2	VREFB2N0	IO	DIFFIO_L33p			L4	R2	V3		DQ3L	DQ1L	DQ1L	DQ3L	DQ1L				Adj.
B2	VREFB2N0	IO	DIFFIO_L33n		43	L3	R1	V2	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	DQ1L	DQ3L	DQ1L	Adj.
B2	VREFB2N1	IO					N5	V9				DQ1L	DQ3L	DQ1L				
B2	VREFB2N1	IO	DIFFIO_L34p		44	M2	P4	AB2	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	DQS1L/CQ1L#, DPCLK1	Adj.
B2	VREFB2N1	IO	DIFFIO_L34n		45	M1	P3	AB1	DQ1L			DQ1L	DQ3L	DQ1L				Adj.
B2	VREFB2N1	IO						V1							DQ1L	DQ3L	DQ1L	
B2	VREFB2N1	IO	DIFFIO_L35p				U2	W2				DM1L/BWS#1L	DM3L0/BWS#3L0	DM1L2/BWS#1L2	DQ1L	DQ3L	DQ1L	Sep.
B2	VREFB2N1	IO	DIFFIO_L35n				U1	W1				DQ3L	DQ3L	DQ1L	DM1L/BWS#1L	DM3L0/BWS#3L0	DM1L2/BWS#1L2	Sep.
B2	VREFB2N1	IO	DIFFIO_L36p					W3										Adj.
B2	VREFB2N1	IO	DIFFIO_L36n					W4										Adj.
B2	VREFB2N1	IO	DIFFIO_L37p					V6										Adj.
B2	VREFB2N1	IO	DIFFIO_L37n					U5										Adj.
B2	VREFB2N1	IO	DIFFIO_L38p				V2	Y5				DQ3L	DQ3L	DQ1L				Adj.
B2	VREFB2N1	IO	DIFFIO_L38n				V1	Y6				DQ3L	DQ3L	DQ1L				Adj.
B2	VREFB2N1	IO	DIFFIO_L39p					V5										Adj.
B2	VREFB2N1	IO	DIFFIO_L39n					U6							DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N1	IO	DIFFIO_L40p					AA7										Adj.
B2	VREFB2N1	IO	DIFFIO_L40n					AA6										Adj.
B2	VREFB2N1	IO	VREFB2N1		46	M3	P5	T7										
B2	VREFB2N1	IO	DIFFIO_L41p				N6	AA8				DQ3L	DQ3L	DQ1L				Adj.
B2	VREFB2N1	IO	DIFFIO_L41n				M7	Y7										Adj.
B2	VREFB2N1	VCCIO2			47													
B2	VREFB2N1	IO	DIFFIO_L42p				M8	Y4							DQ3L	DQ3L	DQ1L	Sep.
B2	VREFB2N1	GND			48													
B2	VREFB2N2	IO	DIFFIO_L42n				N8	Y3										Sep.
B2	VREFB2N2	IO	DIFFIO_L43p					T9										Adj.
B2	VREFB2N2	IO	DIFFIO_L43n					AC2							DQ3L	DQ3L	DQ1L	Adj.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B2	VREFB2N2	IO	DIFFIO_L44p		49	P2	W2	W8	DQ1L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L				Adj.
B2	VREFB2N2	IO	DIFFIO_L44n			P1	W1	AC1		DQ3L	DQ1L	DQ3L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N2	IO	DIFFIO_L45p			R2	Y2	V7		DQ3L	DQ1L	DQ3L	DQ3L	DQ1L				Adj.
B2	VREFB2N2	IO	DIFFIO_L45n				Y1	AC3				DQ3L	DQ3L	DQ1L	DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N2	IO	DIFFIO_L46p					AD2							DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N2	IO	DIFFIO_L46n					AD1										Adj.
B2	VREFB2N2	IO	DIFFIO_L47p					AB3							DQ3L	DQ3L	DQ1L	Sep.
B2	VREFB2N2	IO	DIFFIO_L47n					AA4							DQ3L	DQ3L	DQ1L	Sep.
B2	VREFB2N2	IO						W9										
B2	VREFB2N2	IO	DIFFIO_L48p					AB7										Adj.
B2	VREFB2N2	IO	DIFFIO_L48n					AC7										Adj.
B2	VREFB2N2	IO	VREFB2N2		50	R1	T3	V8										
B2	VREFB2N2	IO	DIFFIO_L49p				N7	AE1										Adj.
B2	VREFB2N2	IO	DIFFIO_L49n				P7	AE2							DQ3L	DQ3L	DQ1L	Adj.
B2	VREFB2N2	IO	DIFFIO_L50p				AA2	AA5										Adj.
B2	VREFB2N2	IO	DIFFIO_L50n				AA1	AF2				DQ3L	DQ3L	DQ1L	DM3L/BWS#3L	DM3L1/BWS#3L1	DM1L3/BWS#1L3	Adj.
B2	VREFB2N3	IO	DIFFIO_L51p					AB6										Adj.
B2	VREFB2N3	IO	DIFFIO_L51n					AB5										Adj.
B2	VREFB2N3	IO						AA3										
B2	VREFB2N3	IO	RUP1		51	T2	V4	U7	DQ1L									
B2	VREFB2N3	IO	RDN1		52	T1	V3	U8	DQ1L									
B2	VREFB2N3	IO	DIFFIO_L52p			T3	P6	AC4		DQ3L	DQ1L							Sep.
B2	VREFB2N3	VCCINT			53													
B2	VREFB2N3	IO	DIFFIO_L52n			R3		AD3		DQ3L	DQ1L							Sep.
B2	VREFB2N3	GND			54													
B2	VREFB2N3	IO					T5	AD4				DM3L/BWS#3L	DM3L1/BWS#3L1	DM1L3/BWS#1L3				
B2	VREFB2N3	IO			55	M5	T4	AE3	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	DQS3L/CQ3L#, CDPCLK1	
B2	VREFB2N3	IO	VREFB2N3		56	R5	R5	AB4										
B2	VREFB2N3	IO			57	R4	R6	AB8	DQ1L	DM3L/BWS#3L	DM1L1/BWS#1L1							
B2	VREFB2N3	IO	DIFFIO_L53p				R7	AC5										Adj.
B2	VREFB2N3	IO	DIFFIO_L53n				T7	AD5										Adj.
B2	VREFB2N3	IO	DIFFIO_L54p					AE4										Adj.
B2	VREFB2N3	IO	DIFFIO_L54n					AF3										Adj.
B2	VREFB2N3	VCCA1			58	N5	T6	Y8										
B2	VREFB2N3	GNDA1			59	P5	U5	AA9										
B2	VREFB2N3	VCCD_PLL1			60	P4	U6	Y9										
B3	VREFB3N3	VCCINT			61													
B3	VREFB3N3	IO	DIFFIO_B1p			U1	V6	AC11										Res.
B3	VREFB3N3	GND			62													
B3	VREFB3N3	IO	DIFFIO_B1n			V1	V5	AD11				DM3B/BWS#3B	DM3B1/BWS#3B1	DM5B3/BWS#5B3				Res.
B3	VREFB3N3	IO	DIFFIO_B2p					AD12										Res.
B3	VREFB3N3	IO	DIFFIO_B2n					AE6							DM1B			Res.
B3	VREFB3N3	IO	DIFFIO_B3p				U7	AF4							DQ1B			Res.
B3	VREFB3N3	IO	DIFFIO_B3n				U8	AB12										Res.
B3	VREFB3N3	IO	VREFB3N3		63	T4	Y4	Y10										
B3	VREFB3N3	IO	DIFFIO_B4p				Y3	AG4				DQ3B	DQ3B	DQ5B				Res.
B3	VREFB3N3	VCCINT			64													
B3	VREFB3N3	IO	DIFFIO_B4n					AG3							DQ1B			Res.
B3	VREFB3N3	GND			65													
B3	VREFB3N3	IO	DIFFIO_B5p					AE7										Res.
B3	VREFB3N3	VCCIO3			66													
B3	VREFB3N3	IO	DIFFIO_B5n					AE8										Res.
B3	VREFB3N3	GND			67													
B3	VREFB3N3	IO	DIFFIO_B6p		68	P6	Y6	AD7	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	DQS1B/CQ1B#, CDPCLK2	Res.
B3	VREFB3N3	IO	DIFFIO_B6n					Y12										Res.
B3	VREFB3N2	IO	PLL1_CLKOUTp		69	U2	AA3	AE5										
B3	VREFB3N2	IO	PLL1_CLKOUTn		70	V2	AB3	AF5										
B3	VREFB3N2	IO	DIFFIO_B7p				W6	AH3				DQ3B	DQ3B	DQ5B	DQ1B			Res.
B3	VREFB3N2	VCCINT			71													
B3	VREFB3N2	IO	DIFFIO_B7n				V7	W10										Res.
B3	VREFB3N2	GND			72													
B3	VREFB3N2	IO					AA4	AF6				DQ3B	DQ3B	DQ5B	DQ1B			
B3	VREFB3N2	IO	VREFB3N2		73	T6	AB4	AA12										
B3	VREFB3N2	IO	DIFFIO_B8p				AA5	AC12				DQ3B	DQ3B	DQ5B				Res.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B3	VREFB3N2	IO	DIFFIO_B8n				AB5	AH4							DQ1B			Res.
B3	VREFB3N2	IO	DIFFIO_B9p					AC10										Res.
B3	VREFB3N2	IO	DIFFIO_B9n					AD8							DQ1B			Res.
B3	VREFB3N2	IO	DIFFIO_B10p					AG6							DQ1B			Res.
B3	VREFB3N2	IO	DIFFIO_B10n					AB13										Res.
B3	VREFB3N2	IO	DIFFIO_B11p				T8	AH6							DQ1B			Res.
B3	VREFB3N2	IO	DIFFIO_B11n				T9	AA13										Res.
B3	VREFB3N2	IO	DIFFIO_B12p				W7	AB9				DQ3B	DQ3B	DQ5B	DM3B/BWS#3B	DM3B1/BWS#3B1	DM5B3/BWS#5B3	Res.
B3	VREFB3N2	VCCINT			74													
B3	VREFB3N2	IO	DIFFIO_B12n				Y7	AD10				DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B	Res.
B3	VREFB3N2	GND			75													
B3	VREFB3N2	IO	DIFFIO_B13p				U9	AG7				DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B	Res.
B3	VREFB3N2	IO	DIFFIO_B13n				V8	Y13				DQ3B	DQ3B	DQ5B				Res.
B3	VREFB3N2	IO					W8	AH7				DQ3B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B	
B3	VREFB3N1	IO	DIFFIO_B14p				AA7	AC8				DM5B/BWS#5B	DM3B0/BWS#3B0	DM5B2/BWS#5B2	DQ3B	DQ3B	DQ5B	Res.
B3	VREFB3N1	IO	DIFFIO_B14n				AB7	AA10				DQ5B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B	Res.
B3	VREFB3N1	IO					Y8	Y14				DQ5B	DQ3B	DQ5B				
B3	VREFB3N1	IO	DIFFIO_B15p				T10	AG8							DQ3B	DQ3B	DQ5B	Res.
B3	VREFB3N1	IO	DIFFIO_B15n				T11	Y15										Res.
B3	VREFB3N1	IO	VREFB3N1		76	P7	V9	AB11										
B3	VREFB3N1	VCCIO3			77													
B3	VREFB3N1	IO	DIFFIO_B16p		78	U3	V10	AE10	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	DQS3B/CQ3B#, DPCLK2	Res.
B3	VREFB3N1	GND			79													
B3	VREFB3N1	IO	DIFFIO_B16n			V3		AH8		DM3B/BWS#3B	DM5B1/BWS#5B1				DQ3B	DQ3B	DQ5B	Res.
B3	VREFB3N1	IO	DIFFIO_B17p			U4		AF7		DQ3B	DQ5B				DQ3B	DQ3B	DQ5B	Res.
B3	VREFB3N1	IO	DIFFIO_B17n		80	V4	U10	AH10	DM5B/BWS#5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B				Res.
B3	VREFB3N1	IO	DIFFIO_B18p		81	U5	AA8	AF9	DQ5B			DQ5B	DQ3B	DQ5B	DQ3B	DQ3B	DQ5B	Res.
B3	VREFB3N1	IO	DIFFIO_B18n		82	V5	AB8	AH12	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B				Res.
B3	VREFB3N1	IO	DIFFIO_B19p					AF8							DM5B/BWS#5B	DM3B0/BWS#3B0	DM5B2/BWS#5B2	Res.
B3	VREFB3N1	IO	DIFFIO_B19n					AF12										Res.
B3	VREFB3N1	IO	DIFFIO_B20p					AE9							DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N1	IO	DIFFIO_B20n					AF13										Res.
B3	VREFB3N1	IO	DIFFIO_B21p			R8	AA9	AF10		DQ3B	DQ5B	DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N1	IO	DIFFIO_B21n		83	T8	AB9	AF11	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	DQS5B/CQ5B#, DPCLK3	Res.
B3	VREFB3N0	IO	VREFB3N0		84	P8	U11	AA14										
B3	VREFB3N0	IO	DIFFIO_B22p					AG10							DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N0	IO	DIFFIO_B22n					AE12							DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N0	IO	DIFFIO_B23p					AE11							DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N0	VCCINT			85													
B3	VREFB3N0	IO	DIFFIO_B23n			P9		AG11		DQ3B	DQ5B				DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N0	GND			86													
B3	VREFB3N0	IO	DIFFIO_B24p			U6		AH11		DQ3B	DQ5B				DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N0	IO	DIFFIO_B24n			V6		AB14		DQ3B	DQ5B							Res.
B3	VREFB3N0	IO	DIFFIO_B25p					AE13							DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N0	IO	DIFFIO_B25n				V11	AC14				DQ5B	DQ3B	DQ5B				Res.
B3	VREFB3N0	IO	DIFFIO_B26p			U7	W10	AG12				DQ5B	DQ3B	DQ5B	DQ5B	DQ3B	DQ5B	Res.
B3	VREFB3N0	IO	DIFFIO_B26n			V7	Y10	AD14		DQ3B	DQ5B	DQ5B	DQ3B	DQ5B				Res.
B3	VREFB3N0	IO	DIFFIO_B27p		87	U8	AA10	AE14	DQ5B	DQ3B	DQ5B	DM4B	DM5B1/BWS#5B1	DM5B1/BWS#5B1				Res.
B3	VREFB3N0	IO	DIFFIO_B27n		88	V8	AB10	AF14	DQ5B	DM5B/BWS#5B	DM5B0/BWS#5B0		DQ5B	DQ5B				Res.
B3	VREFB3N0	CLK15	DIFFCLK_6p		89	U9	AA11	AG14										
B3	VREFB3N0	CLK14	DIFFCLK_6n		90	V9	AB11	AH14										
B4	VREFB4N3	CLK13	DIFFCLK_7p		91	U10	AA12	AG15										
B4	VREFB4N3	CLK12	DIFFCLK_7n		92	V10	AB12	AH15										
B4	VREFB4N3	IO	DIFFIO_B28p		93	U11	AA13	AB15	DQ5B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B				Res.
B4	VREFB4N3	IO	DIFFIO_B28n		94	V11	AB13	AC15	DQ5B			DQ4B	DQ5B	DQ5B	DM4B	DM5B1/BWS#5B1	DM5B1/BWS#5B1	Res.
B4	VREFB4N3	IO	DIFFIO_B29p			U12	AA14	AD15		DQ5B	DQ5B	DQ4B	DQ5B	DQ5B				Res.
B4	VREFB4N3	IO	DIFFIO_B29n				AB14	AE15				DQ4B	DQ5B	DQ5B		DQ5B	DQ5B	Res.
B4	VREFB4N3	IO						AA16										
B4	VREFB4N3	IO	VREFB4N3		95	V12	V12	AA15										
B4	VREFB4N3	IO	DIFFIO_B30p					AF15							DQ4B	DQ5B	DQ5B	Res.
B4	VREFB4N3	VCCIO4			96													
B4	VREFB4N3	IO	DIFFIO_B30n					AG17							DQ4B	DQ5B	DQ5B	Res.
B4	VREFB4N3	GND			97													
B4	VREFB4N3	IO	DIFFIO_B31p					AH17							DQ4B	DQ5B	DQ5B	Res.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B4	VREFB4N3	IO	DIFFIO_B31n					W16										Res.
B4	VREFB4N3	IO	DIFFIO_B32p		98	U13	W13	AF16	DQ5B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	Res.
B4	VREFB4N3	IO	DIFFIO_B32n		99	V13	Y13	AF17	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	DQS4B/CQ5B, DPCLK4	Res.
B4	VREFB4N3	IO	DIFFIO_B33p			P10	AA15	AB16		DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	Res.
B4	VREFB4N3	IO	DIFFIO_B33n			P11	AB15	AE16				DQ4B	DQ5B	DQ5B				Res.
B4	VREFB4N3	IO	DIFFIO_B34p		100	U14	U12	AE17	DQ5B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	DQ4B	DQ5B	DQ5B	Res.
B4	VREFB4N3	VCCINT			101													
B4	VREFB4N3	IO	DIFFIO_B34n			V14		AG18		DQ5B	DQ5B				DQ4B	DQ5B	DQ5B	Res.
B4	VREFB4N3	GND			102													
B4	VREFB4N2	IO	DIFFIO_B35p		103	U15	AA16	AH18	DQ5B			DM2B	DM5B0/BWS#5B0	DM5B0/BWS#5B0	DQ4B	DQ5B	DQ5B	Res.
B4	VREFB4N2	VCCIO4			104													
B4	VREFB4N2	IO	DIFFIO_B35n			V15	AB16	AH19		DQ5B	DQ5B	DQ2B	DQ5B	DQ5B	DM2B	DM5B0/BWS#5B0	DM5B0/BWS#5B0	Res.
B4	VREFB4N2	GND			105													
B4	VREFB4N2	IO	DIFFIO_B36p				T12	AD17							DQ2B	DQ5B	DQ5B	Res.
B4	VREFB4N2	IO	DIFFIO_B36n			R11	T13	AF18		DQ5B	DQ5B							Res.
B4	VREFB4N2	IO			106	P12	V13	AE18	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	DQS2B/CQ3B, DPCLK5	
B4	VREFB4N2	IO	VREFB4N2		107	T11	W14	Y17										
B4	VREFB4N2	IO	DIFFIO_B37p					AG21							DQ2B	DQ5B	DQ5B	Res.
B4	VREFB4N2	IO	DIFFIO_B37n					AC17										Res.
B4	VREFB4N2	IO	DIFFIO_B38p					AH21							DQ2B	DQ5B	DQ5B	Res.
B4	VREFB4N2	IO	DIFFIO_B38n				U13	AG22							DQ2B	DQ5B	DQ5B	Res.
B4	VREFB4N2	IO	DIFFIO_B39p				V14	AH22				DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B	Res.
B4	VREFB4N2	IO	DIFFIO_B39n				U14	AG19										Res.
B4	VREFB4N2	IO	DIFFIO_B40p				U15	AH23							DQ2B	DQ5B	DQ5B	Res.
B4	VREFB4N2	VCCINT			108													
B4	VREFB4N2	IO	DIFFIO_B40n				V15	AE19				DQ2B	DQ5B	DQ5B	DQ2B	DQ5B	DQ5B	Res.
B4	VREFB4N1	GND			109													
B4	VREFB4N1	IO	DIFFIO_B41p					AF24							DQ2B	DQ5B	DQ5B	Res.
B4	VREFB4N1	IO	DIFFIO_B41n				W15	AF19				DQ2B	DQ5B	DQ5B				Res.
B4	VREFB4N1	IO	DIFFIO_B42p				T14	AF25							DM0B	DQ5B	DQ5B	Res.
B4	VREFB4N1	IO	DIFFIO_B42n				T15	AF20				DQ2B	DQ5B	DQ5B	DQ0B			Res.
B4	VREFB4N1	IO					AB18	AD18				DQ2B	DQ5B	DQ5B	DQ0B			
B4	VREFB4N1	IO	DIFFIO_B43p				AA17	Y19										Res.
B4	VREFB4N1	IO	DIFFIO_B43n				AB17	AE21							DQ0B			Res.
B4	VREFB4N1	IO	VREFB4N1		110	U16	AA18	AC18										
B4	VREFB4N1	IO	DIFFIO_B44p					AB18										Res.
B4	VREFB4N1	IO	DIFFIO_B44n			V16		AA19		DQ5B	DQ5B							Res.
B4	VREFB4N1	IO	DIFFIO_B45p					AD19										Res.
B4	VREFB4N1	IO	DIFFIO_B45n					AE20										Res.
B4	VREFB4N1	IO	DIFFIO_B46p					AC19										Res.
B4	VREFB4N1	IO	DIFFIO_B46n					AB19										Res.
B4	VREFB4N1	IO	RUP2		111	T13	AA19	AA17										
B4	VREFB4N1	IO	RDN2		112	T14	AB19	AB17										
B4	VREFB4N1	IO						AD21										
B4	VREFB4N1	IO	DIFFIO_B47p			U17		AF21										Res.
B4	VREFB4N0	IO	DIFFIO_B47n			V17		AE25							DQ0B			Res.
B4	VREFB4N0	IO	DIFFIO_B48p				W17	AC21				DQ2B	DQ5B	DQ5B				Res.
B4	VREFB4N0	IO	DIFFIO_B48n		113	R13	Y17	AF26	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	DQS0B/CQ1B, CDPCLK3	Res.
B4	VREFB4N0	IO	DIFFIO_B49p				AA20	AG25					DQ5B	DQ5B				Res.
B4	VREFB4N0	IO	DIFFIO_B49n				AB20	AH25				DQ2B	DQ5B	DQ5B	DQ0B			Res.
B4	VREFB4N0	IO	VREFB4N0		114	P13	V16	AB20										
B4	VREFB4N0	IO	DIFFIO_B50p				U16	AG23										Res.
B4	VREFB4N0	VCCINT			115													
B4	VREFB4N0	IO	DIFFIO_B50n				U17	AF22							DQ0B			Res.
B4	VREFB4N0	GND			116													
B4	VREFB4N0	IO	DIFFIO_B51p					AE24							DQ0B			Res.
B4	VREFB4N0	IO	DIFFIO_B51n					AG26							DQ0B			Res.
B4	VREFB4N0	IO	PLL4_CLKOUTp		117	U18	T16	AE23										
B4	VREFB4N0	IO	PLL4_CLKOUTn		118	V18	R16	AF23										
B4	VREFB4N0	IO	DIFFIO_B52p				R14	AD22										Res.
B4	VREFB4N0	VCCINT			119													
B4	VREFB4N0	IO	DIFFIO_B52n				R15	AE22										Res.
B4	VREFB4N0	GND			120													

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B4	VREFB4N0	IO	DIFFIO_B53p					AB21										Res.
B4	VREFB4N0	IO	DIFFIO_B53n					AC22										Res.
B4	VREFB4N0	IO						AH26										
B5	VREFB5N3	VCCD_PLL4			121	P15	V17	Y20										
B5	VREFB5N3	GNDA4			122	P14	V18	AA20										
B5	VREFB5N3	VCCA4			123	N14	U18	Y21										
B5	VREFB5N3	IO	DIFFIO_R56n				AA22	AA21										Adj.
B5	VREFB5N3	IO	DIFFIO_R56p				AA21	AB22				DM3R/BWS#3R	DM3R1/BWS#3R1	DM1R3/BWS#1R3				Adj.
B5	VREFB5N3	VCCIO5			124													
B5	VREFB5N3	IO	DIFFIO_R55n					AB24							DM3R/BWS#3R	DM3R1/BWS#3R1	DM1R3/BWS#1R3	Sep.
B5	VREFB5N3	GND			125													
B5	VREFB5N3	IO	DIFFIO_R55p			N15		AC24		DM3R/BWS#3R	DM1R1/BWS#1R1							Sep.
B5	VREFB5N3	IO	RUP3		126	T16	T17	AA22	DQ1R	DQ3R	DQ1R							
B5	VREFB5N3	IO	RDN3		127	R16	T18	AB23	DQ1R									
B5	VREFB5N3	IO						AD25										
B5	VREFB5N3	IO			128	T18	W20	AF27	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	DQS3R/CQ3R#, CDPCLK4	
B5	VREFB5N3	VCCINT			129													
B5	VREFB5N3	IO	DIFFIO_R54n			T17		AE26		DQ3R	DQ1R							Sep.
B5	VREFB5N3	GND			130													
B5	VREFB5N3	IO	DIFFIO_R54p					AE27										Sep.
B5	VREFB5N3	IO	DIFFIO_R53n		131			Y22	DQ1R									Adj.
B5	VREFB5N3	IO	DIFFIO_R53p		132			AD24	DQ1R									Adj.
B5	VREFB5N3	IO	VREFB5N3		133	R18	W19	AA24										
B5	VREFB5N3	IO	DIFFIO_R52n					AC25										Sep.
B5	VREFB5N3	IO	DIFFIO_R52p					AD26							DQ3R	DQ3R	DQ1R	Sep.
B5	VREFB5N3	IO	DIFFIO_R51n		134		Y22	AE28	DQ1R			DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	IO	DIFFIO_R51p		135		Y21	AA23	DQ1R									Adj.
B5	VREFB5N2	IO	DIFFIO_R50n				U20	AD28				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	IO	DIFFIO_R50p				U19	Y23										Adj.
B5	VREFB5N2	IO	DIFFIO_R49n				W22	AD27				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	IO	DIFFIO_R49p				W21	AC26				DQ3R	DQ3R	DQ1R				Adj.
B5	VREFB5N2	IO	DIFFIO_R48n				Y24								DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	IO	DIFFIO_R48p					W22										Adj.
B5	VREFB5N2	IO	DIFFIO_R47n					AC28							DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	IO	DIFFIO_R47p					W21										Adj.
B5	VREFB5N2	IO	DIFFIO_R46n				P15	AC27							DQ3R	DQ3R	DQ1R	Sep.
B5	VREFB5N2	VCCIO5			136													
B5	VREFB5N2	IO	DIFFIO_R46p		137		P16	AB26	DQ1R						DQ3R	DQ3R	DQ1R	Sep.
B5	VREFB5N2	GND			138													
B5	VREFB5N2	IO						V26										
B5	VREFB5N2	IO	VREFB5N2		139	R17	R17	U24										
B5	VREFB5N2	IO					P17	V22										
B5	VREFB5N2	IO	DIFFIO_R45n				V22	AA26				DQ3R	DQ3R	DQ1R	DQ3R	DQ3R	DQ1R	Adj.
B5	VREFB5N2	IO	DIFFIO_R45p				V21	U26				DQ3R	DQ3R	DQ1R				Adj.
B5	VREFB5N2	VCCINT			140													
B5	VREFB5N2	IO	DIFFIO_R44n				R20	AB28				DQ3R	DQ3R	DQ1R	DM1R/BWS#1R	DM3R0/BWS#3R0	DM1R2/BWS#1R2	Sep.
B5	VREFB5N2	GND			141													
B5	VREFB5N2	IO	DIFFIO_R44p					AB27							DQ1R	DQ3R	DQ1R	Sep.
B5	VREFB5N2	IO	DIFFIO_R43n				U22	V21				DQ3R	DQ3R	DQ1R				Adj.
B5	VREFB5N1	IO	DIFFIO_R43p				U21	Y26				DQ3R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N1	IO	DIFFIO_R42n			P18	R18	U20		DQ3R	DQ1R							Adj.
B5	VREFB5N1	IO	DIFFIO_R42p			P17	R19	W26		DQ3R	DQ1R	DM1R/BWS#1R	DM3R0/BWS#3R0	DM1R2/BWS#1R2	DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N1	IO	DIFFIO_R41n					W27							DQ1R	DQ3R	DQ1R	Sep.
B5	VREFB5N1	IO	DIFFIO_R41p					W28							DQ1R	DQ3R	DQ1R	Sep.
B5	VREFB5N1	IO	DIFFIO_R40n					AB25										Adj.
B5	VREFB5N1	IO	DIFFIO_R40p				N16	V28							DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N1	IO	DIFFIO_R39n				R22	AA25				DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N1	IO	DIFFIO_R39p				R21	V27				DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N1	IO	VREFB5N1		142	N16	P20	U23										
B5	VREFB5N1	IO						W25										
B5	VREFB5N1	IO	DIFFIO_R38n			M14	P22	V25		DQ3R	DQ1R	DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N1	IO	DIFFIO_R38p			L13	P21	R22		DQ3R	DQ1R	DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N1	IO	DIFFIO_R37n					V24										Sep.
B5	VREFB5N1	IO	DIFFIO_R37p					U27										Sep.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B5	VREFB5N1	IO	DIFFIO_R36n			L15	N20	V23		DQ3R	DQ1R	DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N1	IO	DIFFIO_R36p			L14	N19	U28		DQ3R	DQ1R				DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N1	IO	DIFFIO_R35n					Y25										Adj.
B5	VREFB5N1	IO	DIFFIO_R35p					T26										Adj.
B5	VREFB5N0	IO	DIFFIO_R34n					W20										Adj.
B5	VREFB5N0	IO	DIFFIO_R34p					U22										Adj.
B5	VREFB5N0	IO	DIFFIO_R33n			M17	N17	V20		DQ3R	DQ1R							Adj.
B5	VREFB5N0	IO	DIFFIO_R33p		143	L16	N18	T25	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	DQS1R/CQ1R#, DPCLK6	Adj.
B5	VREFB5N0	IO	DIFFIO_R32n	DEV_OE	144	M18	N22	T22										Adj.
B5	VREFB5N0	IO	DIFFIO_R32p	DEV_CLRn	145	L17	N21	T21										Adj.
B5	VREFB5N0	IO	DIFFIO_R31n				M22	R26				DQ1R	DQ3R	DQ1R	DQ1R	DQ3R	DQ1R	Adj.
B5	VREFB5N0	IO	DIFFIO_R31p				M21	R25				DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N0	IO	DIFFIO_R30n				M20	R28				DQ1R	DQ3R	DQ1R	DM0R	DM1R1/BWS#1R1	DM1R1/BWS#1R1	Adj.
B5	VREFB5N0	IO	DIFFIO_R30p				M19	U25				DQ1R	DQ3R	DQ1R				Adj.
B5	VREFB5N0	IO	VREFB5N0		146	L18	M16	R24										
B5	VREFB5N0	IO						R27								DQ1R	DQ1R	
B5	VREFB5N0	VCCINT			147													
B5	VREFB5N0	IO	DIFFIO_R29n			K18		R23		DM1R/BWS#1R	DM1R0/BWS#1R0							Sep.
B5	VREFB5N0	GND			148													
B5	VREFB5N0	IO	DIFFIO_R29p			K17		R21		DQ1R	DQ1R							Sep.
B5	VREFB5N0	IO						P21										
B5	VREFB5N0	CLK7	DIFFCLK_3n		149	N18	T22	Y28										
B5	VREFB5N0	CLK6	DIFFCLK_3p		150	N17	T21	Y27										
B6	VREFB6N3	CLK5	DIFFCLK_2n		151	F18	G22	J28										
B6	VREFB6N3	CLK4	DIFFCLK_2p		152	F17	G21	J27										
B6	VREFB6N3	CONF_DONE		CONF_DONE	153	K14	M18	P24										
B6	VREFB6N3	VCCIO6			154													
B6	VREFB6N3	MSEL0		MSEL0	155	K13	M17	N22										
B6	VREFB6N3	GND			156													
B6	VREFB6N3	MSEL1		MSEL1	157	J18	L18	P23										
B6	VREFB6N3	MSEL2		MSEL2	158	J17	L17	M22										
B6	VREFB6N3	MSEL3		MSEL3 (1)		J14	K20	P22										
B6	VREFB6N3	IO	DIFFIO_R28n					K25										Adj.
B6	VREFB6N3	IO	DIFFIO_R28p			H17		M24		DQ1R	DQ1R							Adj.
B6	VREFB6N3	IO	DIFFIO_R27n	INIT_DONE	159	G18	L22	P26										Adj.
B6	VREFB6N3	IO	DIFFIO_R27p	CRC_ERROR	160	G17	L21	P25										Adj.
B6	VREFB6N3	IO	DIFFIO_R26n					H26										Adj.
B6	VREFB6N3	IO	DIFFIO_R26p	.				L25										Adj.
B6	VREFB6N3	IO	VREFB6N3		161	J13	K19	N21										
B6	VREFB6N3	IO	DIFFIO_R25n					N25										Adj.
B6	VREFB6N3	IO	DIFFIO_R25p					G24										Adj.
B6	VREFB6N3	IO	DIFFIO_R24n	nCEO	162	E18	K22	P28										Sep.
B6	VREFB6N3	VCCINT			163													
B6	VREFB6N3	IO	DIFFIO_R24p	CLKUSR	164	E17	K21	P27										Sep.
B6	VREFB6N3	GND			165													
B6	VREFB6N3	IO	DIFFIO_R23n		166	H16	J22	N26	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	DQS0R/CQ1R, DPCLK7	Adj.
B6	VREFB6N3	IO	DIFFIO_R23p				J21	L22				DM0R	DM1R1/BWS#1R1	DM1R1/BWS#1R1				Adj.
B6	VREFB6N3	IO	DIFFIO_R22n				H22	M28				DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R	Sep.
B6	VREFB6N2	IO	DIFFIO_R22p				H21	M23				DQ0R	DQ1R	DQ1R				Sep.
B6	VREFB6N2	IO						M27							DQ0R	DQ1R	DQ1R	
B6	VREFB6N2	IO	DIFFIO_R21n					L20										Adj.
B6	VREFB6N2	IO	DIFFIO_R21p					M26							DQ0R	DQ1R	DQ1R	Adj.
B6	VREFB6N2	IO	DIFFIO_R20n				K17	K22										Adj.
B6	VREFB6N2	IO	DIFFIO_R20p				K18	L23				DQ0R	DQ1R	DQ1R				Adj.
B6	VREFB6N2	VCCINT			167													
B6	VREFB6N2	IO						J26										
B6	VREFB6N2	GND			168													
B6	VREFB6N2	IO	DIFFIO_R19n					H25										Adj.
B6	VREFB6N2	IO	DIFFIO_R19p					K21										Adj.
B6	VREFB6N2	IO	VREFB6N2		169	H18	J18	M25										
B6	VREFB6N2	IO	DIFFIO_R18n				F22	J23				DQ0R	DQ1R	DQ1R				Adj.
B6	VREFB6N2	IO	DIFFIO_R18p				F21	L28				DQ0R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R	Adj.
B6	VREFB6N2	IO	DIFFIO_R17n					L27							DQ0R	DQ1R	DQ1R	Sep.
B6	VREFB6N2	IO	DIFFIO_R17p					L24							DQ0R	DQ1R	DQ1R	Sep.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B6	VREFB6N2	IO	DIFFIO_R16n					E25										Adj.
B6	VREFB6N2	IO	DIFFIO_R16p					K28							DQ0R	DQ1R	DQ1R	Adj.
B6	VREFB6N2	IO	DIFFIO_R15n					F24										Adj.
B6	VREFB6N1	IO	DIFFIO_R15p					K27							DQ0R	DQ1R	DQ1R	Adj.
B6	VREFB6N1	IO	DIFFIO_R14n					J24										Adj.
B6	VREFB6N1	IO	DIFFIO_R14p					L26							DM2R	DM1R0/BWS#1R0	DM1R0/BWS#1R0	Adj.
B6	VREFB6N1	IO	DIFFIO_R13n				H20	H23				DQ0R	DQ1R	DQ1R				Adj.
B6	VREFB6N1	IO	DIFFIO_R13p				H19	J25				DQ0R	DQ1R	DQ1R		DQ1R	DQ1R	Adj.
B6	VREFB6N1	VCCIO6			170													
B6	VREFB6N1	IO	DIFFIO_R12n	nWE	171	D18	E22	G28	DQ1R	DQ1R	DQ1R	DQ0R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Sep.
B6	VREFB6N1	GND			172													
B6	VREFB6N1	IO	DIFFIO_R12p	nOE		D17	E21	G27		DQ1R	DQ1R		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Sep.
B6	VREFB6N1	IO	DIFFIO_R11n					H22										Adj.
B6	VREFB6N1	IO	DIFFIO_R11p					H24										Adj.
B6	VREFB6N1	IO	VREFB6N1		173	H15	H18	M21										
B6	VREFB6N1	IO	DIFFIO_R10n				J17	G25										Adj.
B6	VREFB6N1	IO	DIFFIO_R10p				H16	K26							DQ2R	DQ1R	DQ1R	Adj.
B6	VREFB6N1	IO	DIFFIO_R9n				D22	G26				DM2R	DM1R0/BWS#1R0	DM1R0/BWS#1R0				Adj.
B6	VREFB6N1	IO	DIFFIO_R9p				D21	G23					DQ1R	DQ1R				Adj.
B6	VREFB6N1	IO	DIFFIO_R8n	nAVD		H14	F20	F28		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Sep.
B6	VREFB6N1	IO	DIFFIO_R8p			H13	F19	F27		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R				Sep.
B6	VREFB6N1	IO	DIFFIO_R7n	PADD23		G14	G18	E28		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Adj.
B6	VREFB6N1	IO	DIFFIO_R7p				H17	G22										Adj.
B6	VREFB6N1	IO	DIFFIO_R6n				C22	E27				DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Adj.
B6	VREFB6N0	IO	DIFFIO_R6p				C21	H21				DQ2R	DQ1R	DQ1R				Adj.
B6	VREFB6N0	IO						F26							DQ2R	DQ1R	DQ1R	
B6	VREFB6N0	VCCINT			174													
B6	VREFB6N0	IO	DIFFIO_R5n	PADD22		C18	B22	D28		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R				Sep.
B6	VREFB6N0	GND			175													
B6	VREFB6N0	IO	DIFFIO_R5p	PADD21		C17	B21	D27		DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	DQ2R	DQ1R	DQ1R	Sep.
B6	VREFB6N0	IO	DIFFIO_R4n	PADD20	176	B18	C20	C27	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	DQS2R/CQ3R, CDPCLK5	Adj.
B6	VREFB6N0	IO	DIFFIO_R4p					F25										Adj.
B6	VREFB6N0	IO	VREFB6N0		177	B17	D20	J22										
B6	VREFB6N0	IO	DIFFIO_R3n					E26										Adj.
B6	VREFB6N0	IO	DIFFIO_R3p					E24										Adj.
B6	VREFB6N0	IO	DIFFIO_R2n				F17	D25				DQ2R	DQ1R	DQ1R				Sep.
B6	VREFB6N0	IO	DIFFIO_R2p				G17	D24										Sep.
B6	VREFB6N0	IO	DIFFIO_R1n					D26										Adj.
B6	VREFB6N0	IO	DIFFIO_R1p					C26										Adj.
B6	VREFB6N0	VCCA2			178	F14	F18	J21										
B6	VREFB6N0	GNDA2			179	F15	E18	H20										
B6	VREFB6N0	VCCD_PLL2			180	E15	E17	J20										
B7	VREFB7N0	VCCINT			181													
B7	VREFB7N0	IO						G21										
B7	VREFB7N0	GND			182													
B7	VREFB7N0	IO	DIFFIO_T52n					B26							DQ0T			Res.
B7	VREFB7N0	IO	DIFFIO_T52p					D22							DQ0T			Res.
B7	VREFB7N0	IO	DIFFIO_T51n				F16	E22							DQ0T			Res.
B7	VREFB7N0	IO	DIFFIO_T51p				E16	J19				DQ2T	DQ5T	DQ5T				Res.
B7	VREFB7N0	IO	DIFFIO_T50n				F15	A26				DQ2T	DQ5T	DQ5T	DQ0T			Res.
B7	VREFB7N0	IO	DIFFIO_T50p				G16	G20										Res.
B7	VREFB7N0	IO						B25							DQ0T			
B7	VREFB7N0	IO	DIFFIO_T49n			C16	G15	G19										Res.
B7	VREFB7N0	IO	DIFFIO_T49p		183	D16	F14	A25	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	DQS0T/CQ1T, CDPCLK6	Res.
B7	VREFB7N0	IO	DIFFIO_T48n				H15	F21							DQ0T			Res.
B7	VREFB7N0	IO	DIFFIO_T48p			A18	H14	C25		DQ5T	DQ5T				DQ0T			Res.
B7	VREFB7N0	IO	VREFB7N0		184	A17	D17	F22										
B7	VREFB7N0	IO						A23							DQ0T			
B7	VREFB7N0	IO	DIFFIO_T47n				C19	H19				DQ2T	DQ5T	DQ5T				Res.
B7	VREFB7N0	IO	DIFFIO_T47p				D19	B23				DQ2T	DQ5T	DQ5T	DM0T			Res.
B7	VREFB7N0	IO	PLL2_CLKOUTn		185	C14	A20	C23										
B7	VREFB7N1	IO	PLL2_CLKOUTp		186	D14	B20	D23										
B7	VREFB7N1	IO	DIFFIO_T46n					C24							DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	IO	DIFFIO_T46p				C17	E21				DQ2T	DQ5T	DQ5T				Res.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B7	VREFB7N1	IO	RUP4		187	E14	B19	F19										
B7	VREFB7N1	IO	RDN4		188	E13	A19	E19										
B7	VREFB7N1	IO						C22							DQ2T	DQ5T	DQ5T	
B7	VREFB7N1	IO	DIFFIO_T45n				A18	D21				DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	IO	DIFFIO_T45p	PADD0		E12	B18	B22		DQ5T	DQ5T							Res.
B7	VREFB7N1	IO	VREFB7N1		189	D12	D15	F18										
B7	VREFB7N1	IO	DIFFIO_T44n				E15	C21				DQ2T	DQ5T	DQ5T	DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	IO	DIFFIO_T44p				G14	D19										Res.
B7	VREFB7N1	IO	DIFFIO_T43n					A22							DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	IO	DIFFIO_T43p					A21							DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	VCCINT			190													
B7	VREFB7N1	IO	DIFFIO_T42n				G13	B21							DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	GND			191													
B7	VREFB7N1	IO	DIFFIO_T42p					E18							DQ2T	DQ5T	DQ5T	Res.
B7	VREFB7N1	VCCIO7			192													
B7	VREFB7N1	IO	DIFFIO_T41n	PADD1		A16	A17	C18				DQ2T	DQ5T	DQ5T		DQ5T	DQ5T	Res.
B7	VREFB7N2	GND			193													
B7	VREFB7N2	IO	DIFFIO_T41p	PADD2	194	B16	B17	D18	DQ5T	DQ5T	DQ5T		DQ5T	DQ5T				Res.
B7	VREFB7N2	IO	DIFFIO_T40n				A16	C20				DM2T	DM5T0/BWS#5T0	DM5T0/BWS#5T0	DM2T	DM5T0/BWS#5T0	DM5T0/BWS#5T0	Res.
B7	VREFB7N2	IO	DIFFIO_T40p				B16	H17				DQ4T	DQ5T	DQ5T				Res.
B7	VREFB7N2	IO	VREFB7N2		195	C12	C15	G17										
B7	VREFB7N2	IO	DIFFIO_T39n					D20							DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N2	IO	DIFFIO_T39p					C19							DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N2	IO	DIFFIO_T38n	PADD3	196	A15	E14	C17		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N2	IO	DIFFIO_T38p		197			G18	DQ5T									Res.
B7	VREFB7N2	IO						H15										
B7	VREFB7N2	VCCINT			198													
B7	VREFB7N2	IO	DIFFIO_T37n					F17										Res.
B7	VREFB7N2	GND			199													
B7	VREFB7N2	IO	DIFFIO_T37p	PADD4	200	B15	F13	D17	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	DQS2T/CQ3T, DPCLK8	Res.
B7	VREFB7N2	IO	DIFFIO_T36n	PADD5	201	A14	A15	A19	DQ5T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	IO	DIFFIO_T36p	PADD6	202	B14	B15	B19	DQ5T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	IO	DIFFIO_T35n	PADD7		A13	C13	A18										Res.
B7	VREFB7N3	IO	DIFFIO_T35p	PADD8		B13	D13	B18		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	IO	DIFFIO_T34n					E17							DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	IO	DIFFIO_T34p					J16										Res.
B7	VREFB7N3	IO	DIFFIO_T33n					J17										Res.
B7	VREFB7N3	IO	DIFFIO_T33p					H16										Res.
B7	VREFB7N3	IO	DIFFIO_T32n					G16										Res.
B7	VREFB7N3	IO	DIFFIO_T32p					F15										Res.
B7	VREFB7N3	IO	VREFB7N3		203	E11	E13	G15										
B7	VREFB7N3	IO	DIFFIO_T31n	PADD9		A12	A14	C16		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	DQ4T	DQ5T	DQ5T	Res.
B7	VREFB7N3	VCCINT			204													
B7	VREFB7N3	IO	DIFFIO_T31p	PADD10		B12	B14	D16				DQ4T	DQ5T	DQ5T				Res.
B7	VREFB7N3	GND			205													
B7	VREFB7N3	IO	DIFFIO_T30n					H14										Res.
B7	VREFB7N3	IO	DIFFIO_T30p					K15										Res.
B7	VREFB7N3	IO	DIFFIO_T29n	PADD11		A11	A13	A17		DQ5T	DQ5T	DQ4T	DQ5T	DQ5T		DQ5T	DQ5T	Res.
B7	VREFB7N3	VCCIO7			206													
B7	VREFB7N3	IO	DIFFIO_T29p	PADD12	207	B11	B13	B17	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	DQS4T/CQ5T, DPCLK9	Res.
B7	VREFB7N3	GND			208													
B7	VREFB7N3	IO	DIFFIO_T28n					E15							DM4T	DM5T1/BWS#5T1	DM5T1/BWS#5T1	Res.
B7	VREFB7N3	IO	DIFFIO_T28p				E12	J14					DQ5T	DQ5T				Res.
B7	VREFB7N3	IO	DIFFIO_T27n	PADD13		C10	E11	C15		DM5T/BWS#5T	DM5T0/BWS#5T0							Res.
B7	VREFB7N3	IO	DIFFIO_T27p	PADD14		D10	F11	D15				DM4T	DM5T1/BWS#5T1	DM5T1/BWS#5T1	DQ5T	DQ3T	DQ5T	Res.
B7	VREFB7N3	CLK8	DIFFCLK_5n		209	A10	A12	A15										
B7	VREFB7N3	CLK9	DIFFCLK_5p		210	B10	B12	B15										
B8	VREFB8N0	CLK10	DIFFCLK_4n		211	A9	A11	A14										
B8	VREFB8N0	CLK11	DIFFCLK_4p		212	B9	B11	B14										
B8	VREFB8N0	IO	DIFFIO_T26n				D10	C13				DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	Res.
B8	VREFB8N0	IO	DIFFIO_T26p				E10	D13							DQ5T	DQ3T	DQ5T	Res.
B8	VREFB8N0	IO	DIFFIO_T25n				A10	C14				DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	Res.
B8	VREFB8N0	IO	DIFFIO_T25p	PADD15		E10	B10	D14										Res.
B8	VREFB8N0	IO	DIFFIO_T24n	PADD16		C9	A9	C12		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	Res.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B8	VREFB8N0	VCCIO8			213													
B8	VREFB8N0	IO	DIFFIO_T24p	PADD17	214	D9	B9	D12	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	DQS5T/CQ5T#, DPCLK10	Res.
B8	VREFB8N0	GND			215													
B8	VREFB8N0	IO	DIFFIO_T23n					A12							DQ5T	DQ3T	DQ5T	Res.
B8	VREFB8N0	IO	DIFFIO_T23p					B12										Res.
B8	VREFB8N0	IO	VREFB8N0		216	E9	C10	G14										
B8	VREFB8N0	IO	DIFFIO_T22n		217		G11	K13	DQ5T									Res.
B8	VREFB8N0	IO	DIFFIO_T22p					F14										Res.
B8	VREFB8N0	IO						E14							DQ5T	DQ3T	DQ5T	
B8	VREFB8N0	IO	DIFFIO_T21n					H12										Res.
B8	VREFB8N0	IO	DIFFIO_T21p					J12										Res.
B8	VREFB8N0	IO	DIFFIO_T20n	DATA2	218	A8	A8	A11		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	Res.
B8	VREFB8N1	IO	DIFFIO_T20p	DATA3	219	B8	B8	B11	DQ5T			DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	Res.
B8	VREFB8N1	IO	DIFFIO_T19n	PADD18		A7	A7	A10		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T				Res.
B8	VREFB8N1	VCCINT			220													
B8	VREFB8N1	IO	DIFFIO_T19p	DATA4	221	B7	B7	B10	DQ5T	DQ3T	DQ5T	DQ5T	DQ3T	DQ5T	DM5T/BWS#5T	DM3T0/BWS#3T0	DM5T2/BWS#5T2	Res.
B8	VREFB8N1	GND			222													
B8	VREFB8N1	IO	DIFFIO_T18n	PADD19		A6	A6	G13		DQ3T	DQ5T	DQ5T	DQ3T	DQ5T				Res.
B8	VREFB8N1	IO	DIFFIO_T18p	DATA15		B6	B6	H13				DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N1	IO	DIFFIO_T17n					B8										Res.
B8	VREFB8N1	IO	DIFFIO_T17p					C10							DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N1	IO						D11										
B8	VREFB8N1	IO	VREFB8N1		223	C7	E9	F11										
B8	VREFB8N1	IO	DIFFIO_T16n	DATA14	224	A5	C8	E12	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	DQS3T/CQ3T#, DPCLK11	Res.
B8	VREFB8N1	IO	DIFFIO_T16p	DATA13		B5	C7	F12				DM5T/BWS#5T	DM3T0/BWS#3T0	DM5T2/BWS#5T2				Res.
B8	VREFB8N1	IO	DIFFIO_T15n					D10							DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N1	IO	DIFFIO_T15p					F10										Res.
B8	VREFB8N1	IO	DIFFIO_T14n				H11	E11							DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N1	IO	DIFFIO_T14p				H10	E8										Res.
B8	VREFB8N1	IO	DIFFIO_T13n					E10										Res.
B8	VREFB8N2	IO	DIFFIO_T13p					E7										Res.
B8	VREFB8N2	IO	DIFFIO_T12n					A7							DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N2	IO	DIFFIO_T12p					G10										Res.
B8	VREFB8N2	IO	DIFFIO_T11n					G11										Res.
B8	VREFB8N2	VCCIO8			225													
B8	VREFB8N2	IO	DIFFIO_T11p	DATA5	226	C5	A5	B7	DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N2	GND			227													
B8	VREFB8N2	IO	DIFFIO_T10n					B3										Res.
B8	VREFB8N2	VCCINT			228													
B8	VREFB8N2	IO	DIFFIO_T10p					J10										Res.
B8	VREFB8N2	GND			229													
B8	VREFB8N2	IO	DIFFIO_T9n					F8										Res.
B8	VREFB8N2	IO	DIFFIO_T9p					F7										Res.
B8	VREFB8N2	IO	VREFB8N2		230	D7	B5	G12										
B8	VREFB8N2	IO	DIFFIO_T8n				G10	A6										Res.
B8	VREFB8N2	IO	DIFFIO_T8p	DATA6	231	E8	F10	B6	DQ5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N2	IO	DIFFIO_T7n	DATA7	232	A4	C6	C11	DM5T/BWS#5T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N2	IO	DIFFIO_T7p				D7	H10										Res.
B8	VREFB8N2	IO						G8										
B8	VREFB8N2	IO	DIFFIO_T6n				A4	C9				DQ3T	DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	Res.
B8	VREFB8N2	VCCINT			233													
B8	VREFB8N3	IO	DIFFIO_T6p	DATA8		B4	B4	D9				DQ3T	DQ3T	DQ5T				Res.
B8	VREFB8N3	GND			234													
B8	VREFB8N3	IO	DIFFIO_T5n	DATA9		E7	F8	A8		DQ3T	DQ5T	DQ3T	DQ3T	DQ5T	DM3T/BWS#3T	DM3T1/BWS#3T1	DM5T3/BWS#5T3	Res.
B8	VREFB8N3	IO	DIFFIO_T5p				G8	C8							DQ1T			Res.
B8	VREFB8N3	IO						D8							DQ1T			
B8	VREFB8N3	IO	DIFFIO_T4n	DATA10		A3	A3	C7		DM3T/BWS#3T	DM5T1/BWS#5T1	DQ3T	DQ3T	DQ5T	DQ1T			Res.
B8	VREFB8N3	IO	DIFFIO_T4p	DATA11		B3	B3	D7				DQ3T	DQ3T	DQ5T				Res.
B8	VREFB8N3	IO	VREFB8N3		235	E6	D6	G9										
B8	VREFB8N3	IO					E7	D6							DQ1T			
B8	VREFB8N3	IO	DIFFIO_T3n				C3	A4				DQ3T	DQ3T	DQ5T	DQ1T			Res.
B8	VREFB8N3	IO	DIFFIO_T3p	DATA12	236	D5	C4	B4	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	DQS1T/CQ1T#, CDPCLK7	Res.

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
B8	VREFB8N3	VCCINT			237													
B8	VREFB8N3	IO	DIFFIO_T2n					A3							DQ1T			Res.
B8	VREFB8N3	GND			238													
B8	VREFB8N3	IO	DIFFIO_T2p					C6							DQ1T			Res.
B8	VREFB8N3	IO	DIFFIO_T1n				F7	H8				DM3T/BWS#3T	DM3T1/BWS#3T1	DM5T3/BWS#5T3				Res.
B8	VREFB8N3	IO	DIFFIO_T1p				G7	C4							DQ1T			Res.
B8	VREFB8N3	IO					F9	D4							DM1T			
B8	VREFB8N3	IO	PLL3_CLKOUTn		239	A1	E6	C5										
B8	VREFB8N3	IO	PLL3_CLKOUTp		240	A2	E5	D5										
B8	VREFB8N3	IO					G9	C3										
		VCCINT				G7	J11	K9										
		VCCINT				G8	J12	K11										
		VCCINT				G10	L14	L16										
		VCCINT				G11	M14	K17										
		VCCINT				G12	P11	K19										
		VCCINT				H7	P12	L10										
		VCCINT				H12	L9	L12										
		VCCINT				J7	M9	L14										
		VCCINT				J12	J13	L18										
		VCCINT				K7	J14	N20										
		VCCINT				K12	K14	M11										
		VCCINT				L7	J10	M13										
		VCCINT				L12	K9	M15										
		VCCINT				M7	N9	M17										
		VCCINT				M8	P9	M19										
		VCCINT				M9	P10	N10										
		VCCINT				M11	P13	N12										
		VCCINT				M12	P14	N14										
		VCCINT				F10	N14	N16										
		VCCINT				F12	J16	N18										
		VCCINT				F6	K15	P9										
		VCCINT				F8	L16	P11										
		VCCINT				G13	M15	P13										
		VCCINT				M6	R12	P15										
		VCCINT				N11	R10	P17										
		VCCINT				N13	R8	P19										
		VCCINT				N7	H9	R10										
		VCCINT				N9	G12	R12										
		VCCINT						R14										
		VCCINT						R16										
		VCCINT						R18										
		VCCINT						R20										
		VCCINT						T11										
		VCCINT						T13										
		VCCINT						T15										
		VCCINT						T17										
		VCCINT						T19										
		VCCINT						U10										
		VCCINT						U12										
		VCCINT						U14										
		VCCINT						U16										
		VCCINT						U18										
		VCCINT						V11										
		VCCINT						V15										
		VCCINT						V17										
		VCCINT						V19										
		VCCINT						V13										
		VCCINT						W12										
		VCCINT						W14										
		VCCINT						W18										
		VCCIO1				F4	D4	B1										
		VCCIO1				G4	F4	H1										
		VCCIO1				J4	K4	K5										
		VCCIO1					H4	K8										
		VCCIO1						N1										

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
		VCCIO1						N5										
		VCCIO2				K4	N4	AA1										
		VCCIO2				M4	U4	AG1										
		VCCIO2				N4	W4	T1										
		VCCIO2					R4	T5										
		VCCIO2						W7										
		VCCIO2						W5										
		VCCIO3				R6	AB2	AA11										
		VCCIO3				R7	W5	AD6										
		VCCIO3				R9	W9	AD9										
		VCCIO3					W11	AD13										
		VCCIO3					AA6	AH2										
		VCCIO3						AH5										
		VCCIO3						AH9										
		VCCIO3						AH13										
		VCCIO3						AB10										
		VCCIO4				R10	AB21	AA18										
		VCCIO4				R12	W12	AD16										
		VCCIO4				R14	W16	AD20										
		VCCIO4					W18	AD23										
		VCCIO4					Y14	AH16										
		VCCIO4						AH20										
		VCCIO4						AH24										
		VCCIO4						AH27										
		VCCIO4						Y16										
		VCCIO5				K15	P18	AA28										
		VCCIO5				M15	V19	AG28										
		VCCIO5				R15	Y19	T24										
		VCCIO5					T19	T28										
		VCCIO5						U21										
		VCCIO5						W24										
		VCCIO6				F16	E19	B28										
		VCCIO6				G15	G19	H28										
		VCCIO6				J15	L19	K24										
		VCCIO6					J20	L21										
		VCCIO6						N24										
		VCCIO6						N28										
		VCCIO7				D11	A21	A16										
		VCCIO7				D13	D12	A20										
		VCCIO7				D15	D14	A24										
		VCCIO7					D16	A27										
		VCCIO7					D18	E16										
		VCCIO7						E20										
		VCCIO7						E23										
		VCCIO7						H18										
		VCCIO7						J15										
		VCCIO8				D4	A2	A2										
		VCCIO8				D6	D5	A5										
		VCCIO8				D8	D9	A9										
		VCCIO8					D11	A13										
		VCCIO8					E8	E6										
		VCCIO8						E9										
		VCCIO8						E13										
		VCCIO8						H11										
		VCCIO8						J13										
		GND				G9	L10	K10										
		GND				H9	L11	K12										
		GND				H8	M10	K14										
		GND				J8	M11	K18										
		GND				J9	L12	K20										
		GND				J10	L13	L11										
		GND				H10	M12	L15										
		GND				H11	M13	L17										
		GND				J11	N11	L19										
		GND				K11	K11	L9										

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
		GND				K10	N12	M10										
		GND				K9	K12	M12										
		GND				K8	K13	M14										
		GND				L8	N13	M16										
		GND				L9	N10	M18										
		GND				L10	K10	N11										
		GND				M10	J9	N13										
		GND				L11	F12	N15										
		GND				F11	H12	N17										
		GND				F13	H13	N19										
		GND				F7	J15	P10										
		GND				F9	K16	P12										
		GND				G6	L15	P14										
		GND				M13	N15	P16										
		GND				N10	R13	P18										
		GND				N12	R11	P20										
		GND				N6	R9	R11										
		GND				N8	P8	R13										
		GND						R15										
		GND						R17										
		GND						R19										
		GND						R9										
		GND						T10										
		GND						T12										
		GND						T14										
		GND						T16										
		GND						T18										
		GND						U11										
		GND						U13										
		GND						U15										
		GND						U17										
		GND						U19										
		GND						V10										
		GND						V12										
		GND						V14										
		GND						V18										
		GND						W11										
		GND						W15										
		GND						W17										
		GND						W19										
		GND				C15	A1	AA2										
		GND				C13	C5	AA27										
		GND				C11	C9	AC6										
		GND				C8	C11	AC9										
		GND				C6	C12	AC13										
		GND				C4	C14	AC16										
		GND				E3	C16	AC20										
		GND				G3	A22	AC23										
		GND				J3	E20	AF1										
		GND				K3	G20	AF28										
		GND				N3	L20	AG2										
		GND				P3	P19	AG5										
		GND				T5	V20	AG9										
		GND				T7	Y20	AG13										
		GND				T9	AB22	AG16										
		GND				T10	Y18	AG20										
		GND				T12	Y16	AG24										
		GND				T15	Y12	AG27										
		GND				P16	Y11	B2										
		GND				M16	Y9	B5										
		GND				J16	Y5	B9										
		GND				K16	AB1	B13										
		GND				G16	N3	B16										
		GND				E16	U3	B20										
		GND					W3	B24										

Bank Number	VREFB Group	Pin Name / Function	Optional Function(s)	Configuration Function	Q240	F324	F484 / U484	F780	DQS for X8/X9 in Q240	DQS for X8/X9 in F324	DQS for X16/X18 in F324	DQS for X8/X9 in F484/U484	DQS for X16/X18 in F484/U484	DQS for X32/X36 in F484/U484	DQS for X8/X9 in F780	DQS for X16/X18 in F780	DQS for X32/X36 in F780	PKG NOTES (4), (5), (6)
		GND					D3	B27										
		GND					F3	C1										
		GND					K3	C28										
		GND					H3	F6										
		GND					R3	F9										
		GND					AB6	F13										
		GND					Y15	F16										
		GND					T20	F20										
		GND					J19	F23										
		GND					C18	H2										
		GND					D8	H27										
		GND						J11										
		GND						J18										
		GND						K6										
		GND						K16										
		GND						K23										
		GND						L13										
		GND						M20										
		GND						N2										
		GND						N6										
		GND						N9										
		GND						N23										
		GND						N27										
		GND						T2										
		GND						T6										
		GND						T20										
		GND						T23										
		GND						T27										
		GND						U9										
		GND						V16										
		GND						W6										
		GND						W13										
		GND						W23										
		GND						Y11										
		GND						Y18										

Notes:
(1) Q240 in the EP3C40 device does not have the MSEL[3] pin and does not support the Active Parallel (AP) configuration mode.
(2) If the p pin or n pin is not available for the package, the particular differential pair is not supported.
(3) If dedicated CLK pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the core logic.
(4) "Adj." in PKG NOTE denotes the dedicated differential output drivers with p and n pins located adjacent to each other.
(5) "Sep." in PKG NOTE denotes the dedicated differential output drivers with p and n pins not located adjacent to each other.
(6) "Res." in PKG NOTE denotes differential output drivers that require external resistor network.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.			
		Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins.	All VCCINT pins must be connected to 1.2V supply. Decoupling depends on the design decoupling requirements of the specific board. See *Note (8)*
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards. VCCIO powers up the JTAG pins (TCK, TMS, TDI and TDO) and the following configuration pins: nCONFIG, DCLK, DATA[15..0], nCE, nCEO, nWE, nRESET, nOE, FLASH_nCE, nCSO and CLKUSR.	Decoupling depends on the design decoupling requirements of the specific board. See *Note (8)*
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.	All GND pins should be connected to the board GND plane.
VREFB[1..8]N[0..3] *(Note 2)*	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-referenced pins for the bank. If voltage-referenced I/O standards are not used in the bank, the VREF pins are available as user I/O pins.	If VREF pins are not used, the designer should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See *Note (8)*
VCCA[1..4] *(Note 3)*	Power	Supply (analog) voltage for PLLs[1..4] and other analog circuits in the device.	The designer must connect these pins to 2.5V, even if the PLL is not used. These pins must be powered up and powered down at the same time. Connect VCCA[1..4] pins together. VCCA supply to the chip should be isolated. See *Note(9)* for details. See *Note(10)* for recommended decoupling.
VCCD_PLL[1..4] *(Note 3)*	Power	Supply (digital) voltage for PLLs[1..4].	The designer must connect these pins to 1.2V, even if the PLL is not used.Connect VCCD_PLL[1..4] pins together. VCCD_PLL supply to the chip should be isolated. See *Note(9)* for details. See *Note (11)* for recommended decoupling.
RUP[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5 and 7. The external precision resistor Rup must be connected to the designated RUP pin within the same bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O, the pin can be connected to VCCIO of the bank in which the RUP pin resides or GND.
RDN[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5 and 7. The external precision resistor Rdn must be connected to the designated RDN pin within the same bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to GND.
GNDA[1..4] *(Note 3)*	Ground	Ground for PLL[1..4]. You can connect these pins to GND plane on the board.	The designer should connect these pins to an isolated analog ground plane on the board.
NC	No Connect	Do not drive signals into these pins.	Do not connect these pins to any signal.
		Dedicated Configuration/JTAG Pins	
DCLK	Input (PS, FPP) Output (AS, AP)	Dedicated configuration clock pin. In PS and PP configuration modes, DCLK is used to clock configuration data from an external source into the Cyclone III device. In AS and AP modes, DCLK is an output from the Cyclone III device that provides timing for the configuration interface.	DCLK should not be left floating. In JTAG configuration and schemes that use an external host, designer should drive it high or low, whichever is more convenient on the board. In AS and AP mode, the DCLK has an internal pull-up resistor(typically 25-kΩ) that is always active.
DATA0	Input (PS, FPP, AS) Bidirectional open drain (AP)	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA0 has an internal pull-up resistor that is always active. After AS configuration, DATA0 is a dedicated input pin with optional user control. After PS or PP configuration, DATA0 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA0 is a dedicated bidirectional pin with optional user control.	If you are using a serial configuration device in AS configuration mode, you must connect a 25- Ω series resistor at the near end of the serial configuration device for the DATA[0]. If DATA[0] is not used, it should be driven high or low, whichever is more convenient on the board.
MSEL[3..0]	Input	Configuration input pins that set the Cyclone III device configuration scheme. These pins must be hardwired to VCCA or GND. Some of the smaller devices or package options do not support the AP flash programming and do not have the MSEL[3] pin.	These pins are internally connected to 5-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used, these pins should be tied to VCCA or GND. Refer to Chapter 10 of Cyclone III Handbook: Configuring Cyclone III Devices. If only JTAG configuration is used, then connect these pins to GND.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE is tied low.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user mode causes the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.	If you are using PS configuration scheme with a download cable, connect this pin through a 10-k Ω resistor to VCCA. For other configuration schemes, if this pin is not used, this pin must be connected directly or through a 10-kΩ resistor to VCCIO.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode.	This pin is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-kΩ pull-up resistor.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization.	This pin is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-k Ω pull-up resistor.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.	Connect this pin to a 1-kΩ resistor to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.	When interfacing with 2.5V/3.0V/3.3V configuration voltage standards, connect this pin through a 1-k Ω resistor to VCCA. Otherwise, connect this pin through a 1-kΩ resistor to VCCIO. See *Note (4)* .
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.	When interfacing with 2.5V/3.0V/3.3V configuration voltage standards, connect this pin through a 1-k Ω resistor to VCCA. Otherwise, connect this pin through a 1-kΩ resistor to VCCIO. See *Note (4)* .
TDO	Output	Dedicated JTAG output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected.
		Clock and PLL Pins	
CLK[0,2,4,6,9,11,13,15], DIFFCLK_[0..7]p *(Note 5)*	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND. See *Note (12)* .

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
CLK[1,3,5,7,8,10,12,14], DIFFCLK_[0..7]n *(Note 5)*	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND. See *Note (12)* .
PLL[1..4]_CLKOUT[p,n] *(Note 3)*	I/O, Output	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.These pins can only use the differential I/O standard if it is being fed by a PLL output.	Connect unused pins to GND. See *Note (12)* .
Optional/Dual-Purpose Configuration Pins			
nCEO	I/O, Output	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds a subsequent device's nCE pin and must be pulled high to VCCIO by an external 10-kΩ pull-up resistor. During single device configuration and for the last device in multi-device configuration, this pin can be left floating or used as a user I/O after configuration.
FLASH_nCE, nCSO	I/O, Output	This pin functions as FLASH_nCE in AP mode, and nCSO in AS mode. This pin has an internal pull-up resistor that is always active. nCSO: Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device. FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash.	When not programming the device in AS mode, nCSO is not used. Similarly, FLASH_nCE is not used when not programming the device in AP mode. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
DATA1, ASDO	Input (FPP) Output (AS) Bidirectional open-drain (AP)	This pin functions as DATA1 in PS, FPP, and AP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA1 is a dedicated bidirectional pin with optional user control. ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.	When not programming the device in AS or AP mode, this pin is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
DATA[7..2]	Input (FPP) Bidirectional open-drain (AP)	Data inputs. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA[7..2] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings. After AP configuration, DATA[7..2] are dedicated bidirectional pins with optional user control.	When not programming the device in AP mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to leave these pins unconnected.
DATA[15..8]	Bidirectional open-drain (AP)	Data inputs. Btye-wide or word-wide configuration data is presented to the target device on DATA[15..0]. In PS, FPP, or AS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After AP configuration, DATA[15..8] are dedicated bidirectional pins with optional user control.	When not programming the device in AP mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to leave these pins unconnected.
PADD[23..0]	I/O, Output (AP)	24-bit address bus from the Cyclone III device to the parallel flash in AP mode.	When not programming the device in AP mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to leave these pins unconnected.
nRESET	I/O, Output (AP)	Active-low reset output. Driving the nRESET pin low resets the parallel flash.	When not programming the device in AP mode, nRESET is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nAVD	I/O, Output (AP)	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[23..0] address bus.	When not programming the device in AP mode, nRESET is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nOE	I/O, Output (AP)	Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[15..0] and RDY).	When not programming the device in AP mode, nOE is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nWE	I/O, Output (AP)	Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[15..0] bus is valid.	When not programming the device in AP mode, nWE is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
CRC_ERROR	I/O, Output	Active-high signal that indicates that the error-detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error-detection circuit is enabled.This pin can be set in Quartus ® II software to support open-drain output.	If open drain feature is used, connect this pin to VCCIO of Bank 1 through a 10-k Ω resistor.When the output for CRC_ERROR is not used and this pin is not used as an I/O then it is recommended to leave the pin unconnected.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus ® II software.	When the input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to VCCIO or GND

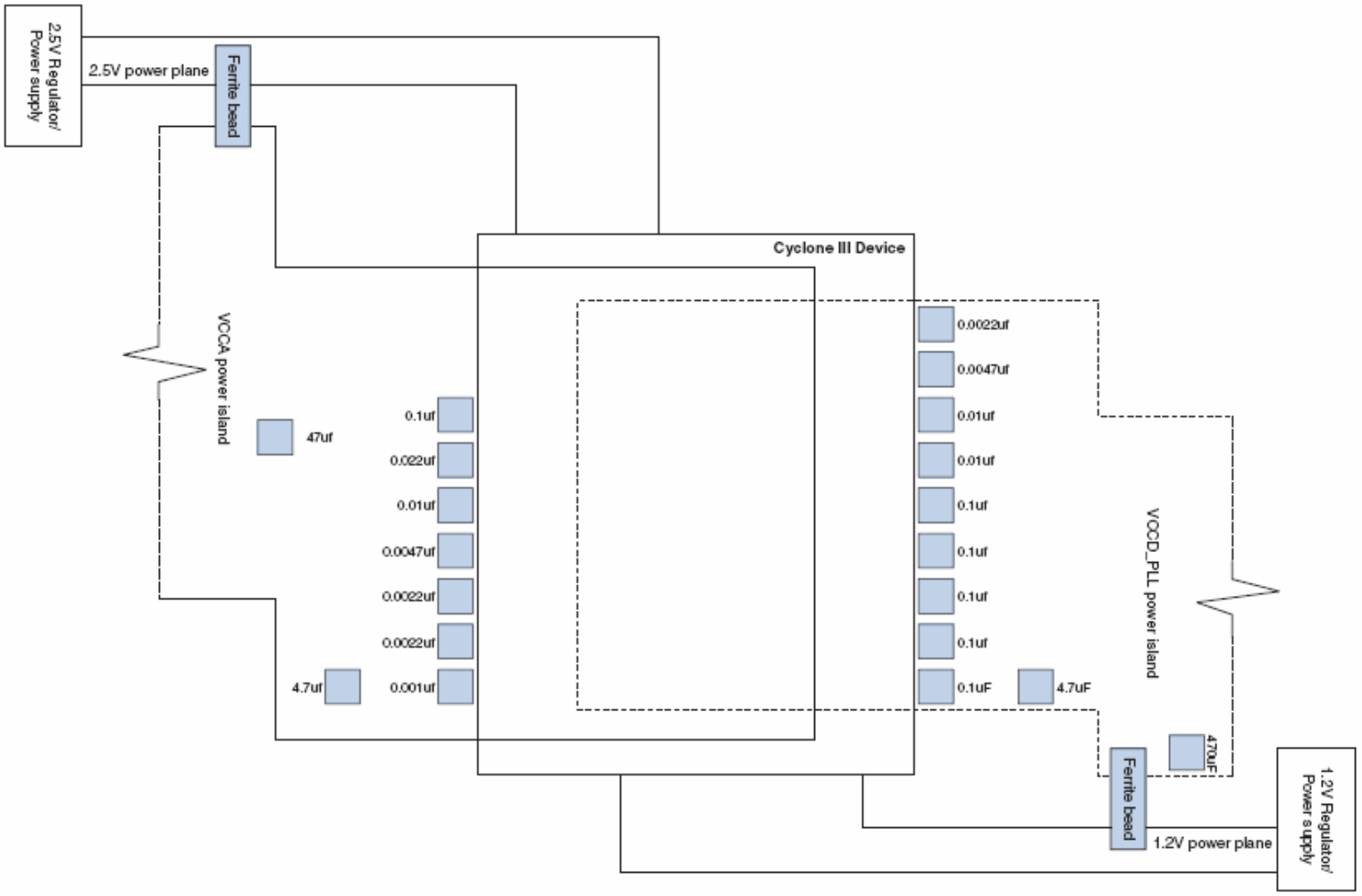
Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.	When the input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to VCCIO or GND.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.	Connect this pin to a 10-kΩ resistor to VCCIO.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to GND.
Dual-Purpose Differential and External Memory Interface Pins			
DIFFIO_[L,R,T,B][0..61][n,p] *(Note 6)*	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS-compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See *Note (12)* .
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCLK[0..11] *(Note 7)*	I/O, DQS/CQ, DPCLK	signals such as clocks, asynchronous clears, presets, and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See *Note (12)* .
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPCLK[0..7] *(Note 7)*	I/O, DQS/CQ, CDPCLK	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets, and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before being driven into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry, which allows for the fine tuning of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See *Note (12)* .
DQ[0..5][L,R,T,B] *(Note 7)*	I/O, DQ	Optional data signal for use in external memory interfaces.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).
DM[0..5][L,R,B,T][0..1]/BWS#[0..5][L,R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See *Note (12)* .

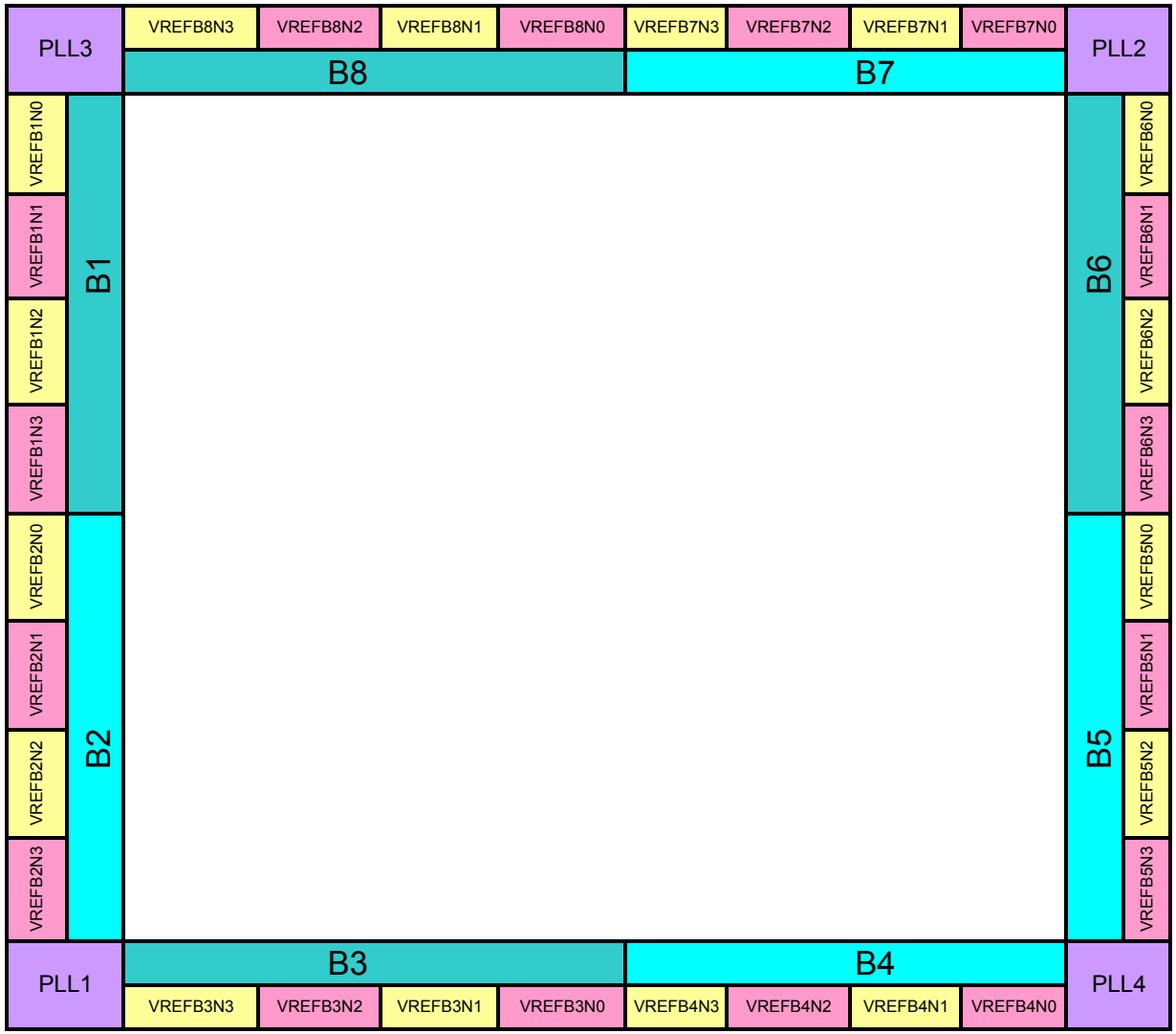
Notes:

(1) This pin connection guideline is created based on the largest Cyclone III device (EP3C120F780).
(2) EP3C5 and EP3C10 only have VREFB[1..8]N0.
(3) EP3C5 and EP3C10 only have PLL(1 & 2). EP3C16 and other larger densities have PLL (1,2,3 & 4).
(4) You must follow specific requirements when interfacing Cyclone III devices with 2.5V/3.0V/3.3V configuration voltage standards. All I/O inputs must maintain a maximum AC voltage of 4.1V. Refer to Configuration and JTAG Pin I/O Requirements of Chapter 10 in Cyclone III Handbook: Configuring Cyclone III Devices.
(5) The number of dedicated global clocks for each device density is different. EP3C5 and EP3C10 support four dedicated clock pins on the left and right sides of the device, that can drive a total of 10 global clock networks. EP3C16 and other larger densities support four dedicated clock pins on each side of the device that can drive a total of 20 global clock networks.
(6) The differential TX/RX channels for each device density and package is different. Please refer to the Cyclone III Handbook Chapter 8: High-Speed Differential Interfaces in Cyclone III Devices.
(7) For details on the DQ and DQS bus modes support in different device densities, refer to the Cyclone III Handbook Chapter 9: External Memory Interfaces in Cyclone III Devices.
(8) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling.
(9) Use a power island for VCCA and VCCD_PLL. PLL power supply may originate from another plane on the board but must be isolated using a ferrite bead or other equivalent methods. If using a ferrite bead, choose an 0402 package with low DC resistance, higher current rating than the maximum steady state current for the supply it is connected to (VCCA or VCCD_PLL) and high impedance at 100MHz.
(10) Decouple VCCA power island with a parallel combination of 1x47uF, 1x4.7uF, 1x0.1uF, 1x0.022uF, 1x0.01uF, 1x0.0047uF, 2x0.022uF, 1x0.001uF. Use 0402 package for 0.1uF and smaller capacitors for lower mounting inductance. Place 0.1uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20mV ripple voltage was used in the analysis for VCCA decoupling. Refer to the figure on "VCCA&VCCD Decoupling" worksheet for decoupling capacitor placement guidelines. The figure on "VCCA&VCCD Decoupling" worksheet depicts symbolic representation of decoupling scheme and not the exact layout.
(11) Decouple VCCD_PLL power island with a parallel combination of 1x470uF(low ESR Tantalum), 1x4.7uF, 5x0.1uF, 2x0.01uF, 1x0.0047uF, 1x0.0022uF. Use 0402 package for 0.1uF and smaller capacitors for lower mounting inductance. Place 0.1uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20mV ripple voltage was used in the analysis for VCCD_PLL decoupling.Refer to the figure on "VCCA&VCCD Decoupling" worksheet for decoupling capacitor placement guidelines.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines

The figure on "VCCA&VCCD Decoupling" worksheet depicts symbolic representation of decoupling scheme and not the exact layout.
(12) The unused pins must be connected as specified in the Quartus II software settings. The default Quartus II setting for unused pins is 'As inputs tri-stated with weak pull-up resistors'. To change the setting, go to 'Assignments', then 'Device'. Click on 'Device & Pin options' dialog box and go to 'Unused Pins' tab. You may choose the desired setting from the 'Reserve all unused pins' drop down list.





Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to get an idea of placement on the device.
   Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	9/7/2007	Initial release.
1.1	1/4/2008	Updated Note(2) in Pin List.
1.2	5/23/2008	▪ Updated pin function for CRC_ERROR pin. ▪ Updated DQ/DQS support for UBGA package. ▪ Updated pin function for PLL[1..4]_CLKOUT[p,n] pin. ▪ Remove RDY from pin list and pin definitions. ▪ Incorporated pin connection guideline into Pin Definitions worksheet. ▪ Incorporated VCCA and VCCD Decoupling recommendations.
1.3	5/7/2009	Changed VREFB[1..8]N[0..2] to VREFB[1..8]N[0..3] in Pin Definitions.