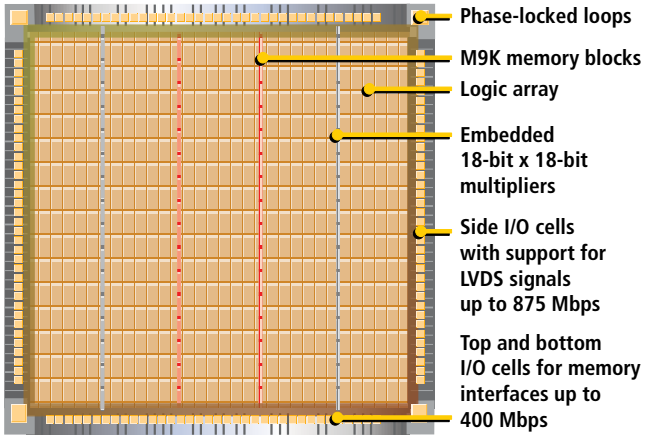
Cyclone III product specs

Altera® Cyclone® III FPGAs, the newest offering in the Cyclone series of low-cost devices, feature low power and high functionality to deliver more, sooner, and for less—especially for your most cost-sensitive high-volume applications. Built on TSMC's 65-nm low-power (LP) process technology, Cyclone III FPGAs were designed to provide customers with the flexibility and application-optimized features that enable the highest levels of design possibilities and productivity, while meeting the most stringent cost and power budgets in your applications. From video and image processing, to displays and wireless systems, and more, the opportunities for designers using Cyclone III devices are unlimited.

Visit **www.altera.com/devices** for information on the entire Cyclone series of low-cost FPGAs.

Cyclone III floorplan



Cyclone III family features summary

Cost-optimized architecture	Offers from 5,136 to 119,088 logic elements (LEs)—70 percent more than the Cyclone II FPGA family for enhanced system integration.
Low-power architecture	Altera's innovative power-saving features and TSMC's 65-nm LP process technology come together to minimize both standby and dynamic power consumption. Quartus® II design software provides a power-aware design flow to enable software optimization for minimal power usage. Compared to Cyclone II FPGAs, Cyclone III devices lower power consumption by up to 50 percent.
Embedded memory	Up to 4 Mbits of embedded memory for memory-intensive applications such as video line buffers.
Embedded multipliers	Up to 288 dedicated 18-bit x 18-bit multipliers with 260-MHz performance for high-bandwidth parallel processing applications.
External memory interfaces	Support for high-speed external memory interfaces including DDR, DDR2, SDR SDRAM, and QDR II SRAM at up to 400 megabits per second (Mbps). The autocalibrating external memory interface PHY feature eases timing closure and eliminates variations over process, voltage, and temperature (PVT).
Robust clock management	Up to 20 global clock networks and 4 phase-locked loops (PLLs) per device with 5 outputs per PLL. Supports dynamic reconfiguration for frequency and phase changes.
Differential signaling	Supports up to 875-Mbps receive and 840-Mbps transmit LVDS signaling. Ability to use reduced swing differential signaling (RSDS), LVDS, and point-to-point differential signaling (PPDS) without external resistors.
Commodity parallel configuration	Native support for commodity parallel flash devices to provide fast and low-cost configuration solutions.
Remote system upgrade	Allows storage of multiple configuration images in a single configuration device for field upgrades. Automatic error correction circuitry restores factory image if a configuration error is detected.
Hot socketing and power sequencing	Robust on-chip hot-socketing and power-sequencing support that ensures proper device operation independent of the power-up sequence.
IP MegaCore® library	Shorten design time using a broad portfolio of more than 200 Altera and partner IP cores. Altera IP can be evaluated in hardware before purchase.
Embedded soft-core processor	Nios® II embedded processors offer an ideal replacement for low-cost discrete microprocessors to reduce cost and increase flexibility. Nios II soft processor support for Cyclone III FPGAs offers over 100-DMIPS performance.
Free software support	The free, downloadable Quartus II Web Edition software supports the Cyclone III device, offering productivity and performance features including TimeQuest timing analysis, PowerPlay power optimization, and SOPC Builder, providing the fastest path to design completion for Cyclone III FPGAs.

Package Statistics[1]	EQFP[2]	PQFP		FBGA				UBGA	
Number of pins	144	208	240	256	324	484	780	256	484
Nominal length x width (mm)	22 x 22	31 x 31	35 x 35	17 x 17	19 x 19	23 x 23	29x29	14 x 14	19 x 19
Maximum surface area (mm)	493	952	1,215	296	369	538	841	196	369
Maximum height (mm)	1.6	4.1	4.1	1.55	2.6	2.6	2.6	2.2	2.2
Nominal lead pitch (mm)	0.5	0.5	0.5	1	1	1	1	0.8	0.8
Maximum lead width (mm)	0.27	0.27	0.27	0.7	0.7	0.7	0.7	0.6	0.6

[1] All Cyclone III FPGA packages use wirebond technology [2] EQFP is a TQFP with an exposed pad on the bottom to connect to ground

Cyclone III FPGA family package and I/O matrix

93 Number indicates available user I/O pins.

Vertical migration (Same V_{CC}, GND, ISP, and input pins). User I/O may be less than labelled for vertical migration.

Unless noted, all Cyclone series devices are offered in commercial and industrial temperatures and lead-free packages.

		Cyclone III (1.2V) Low cost, high volume							
		EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Enhanced thin quad flat pack (E)	144-pin EQFP	94	94	84	82				
Plastic quad flat pack (Q)	240-pin PQFP[1]			160	148	128			
FineLine BGA (F)	256-pin FBGA	182	182	168	156				
	324-pin FBGA				215	195			
	484-pin FBGA			346		331	327	295	283
	780-pin FBGA					535	377	429	531
Ultra FineLine BGA (U)	256-pin UFBGA	182	182	168	156				
	484-pin UFBGA			346		331	327	295	

[1] This package does not support industrial temperatures

Cyclone III FPGA features

		Cyclone III (1.2V) Low cost, high volume							
		EP3C5	EP3C10	EP3C16	EP3C25	EP3C40	EP3C55	EP3C80	EP3C120
Density and speed	LEs	5,136	10,320	15,408	24,624	39,600	55,856	81,264	119,088
	Total RAM (Kbits)	414	414	504	594	1,134	2,340	2,745	3,888
	M9K block (8 Kbits + 512 parity bits)[1]	46	46	56	66	126	260	305	432
	Speed grades (fastest to slowest)[2]	6, 7, 8	6, 7, 8	6, 7, 8	6, 7, 8	6, 7, 8	6, 7, 8	6, 7, 8	7, 8
Architectural features	Embedded processor available	Nios II							
	18-bit x 18-bit/9-bit x 9-bit multipliers	23/46	23/46	56/112	66/132	126/252	156/312	244/488	288/576
	True dual-port RAM	✓	✓	✓	✓	✓	✓	✓	✓
	Global clock networks	10	10	20	20	20	20	20	20
	PLLs/unique outputs	2/10	2/10	4/20	4/20	4/20	4/20	4/20	4/20
	Configuration file size (Mbits)	2.8	2.8	3.9	5.5	9.1	14.2	19	27.2
I/O features	I/O voltage levels supported	1.5, 1.8, 2.5, 3.0, 3.3							
	I/O standards supported	LVDS, RSDS, Mini-LVDS, LVPECL, Differential SSTL-18 (I and II), Differential SSTL-2 (I and II), 1.5V Differential HSTL (I and II), 1.8V Differential HSTL (I and II), SSTL-18 (I and II), SSTL-2 (I and II), 1.5V HSTL (I and II), PCI, PCI-X, PCI Express[3], LVTTL, LVCMOS, and PPDS							
	LVDS maximum data rate (Mbps) (receive/transmit)	875/840							
	LVDS channels	66	66	136	79	223	159	177	229
I/O features (continued)	RSDS maximum data rate (Mbps) (transmit)	360							
	Mini-LVDS maximum data rate (Mbps) (transmit)	400							
	Series on-chip termination	✓	✓	✓	✓	✓	✓	✓	✓
	Programmable drive strength	✓	✓	✓	✓	✓	✓	✓	✓
External memory interfaces	Memory device supported	QDR II, DDR2, DDR, SDR							
	MegaCore controller with clear text datapath	✓							
	System timing and analysis	✓							
	Board layout guideline	✓							

[1] Kbits = 1,024 bits [2] Not all packages are supported in all speed grades [3] Requires external PHY device

FOR MORE INFORMATION

Cyclone III FPGAs www.altera.com/cyclone3

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