Application Note
August 2011

SATA NANDrive™ Application Design Guide

Rev 01.002

Greenliant Systems
Proprietary and Confidential
08/10/2011

Application Note
August 2011

Disclaimer

By downloading and using these files, you agree:

1. The information delivered hereunder ("Information") is confidential to Greenliant Systems. You may use the Information only to generate or produce a reference PCB ("Product"), or a Modified Product, as defined below. The Information is delivered as is. Greenliant Systems makes no warranty express or implied, with respect to the use, merchantability, or fitness for purpose of the Information, the Product or the Modified Product. Further, Greenliant Systems disclaims any patent infringement liability arising out of, resulting from, or in connection with the use of the Information, the Product, or the Modified Product, or the use of the Information, the Product or the Modified Product, in combination with any other component, products or process. In no event shall Greenliant Systems be liable for any incidental or consequential damages with regard to the Information, the Product, or the Modified Product.

2. You will not sell or otherwise commercially exploit the Product. You will have the right to use the Information to generate or produce a reference PCB in which at least all references to Greenliant Systems markings, logos and part numbers are removed ("Modified Product"), and have the right to commercially exploit the Modified Product.

3. The unauthorized use, disclosure or duplication of the Information or the Product will result in irreparable harm to Greenliant Systems for which legal damages would be an inadequate remedy. Accordingly, in the event of unauthorized use, disclosure or duplication, Greenliant Systems will be entitled to injunctive relief in addition to any other rights or remedies it may have at law or equity.

4. All Intellectual Property rights residing or subsisting in the Information or the Product belongs to Greenliant Systems.

SATA NANDrive™ Application Design Guide

Application Note
August 2011

Table of Contents

SATA NANDrive™ Application Design Guide

Application Note
August 2011

Revision History

Revision	Description	Date
00.001	Initial Release	09/13/2010
01.000	Official Release	09/30/2010
01.001	Updated the format Corrected the typos	04/08/2011
01.002	Updated Figure 5 Update section 2.3	08/10/2011

SATA NANDrive™ Application Design Guide

Application Note
August 2011

1. Introduction

SATA NANDrive is the heart of a high-performance, flash media-based data storage system. The SATA NANDrive is a very flexible product that can work well in a number of different applications. Two easily overlooked features should be considered when designing with the SATA NANDrive:

- Serial Communication Interface (SCI) – The SCI provides trace information during debugging processes. To aid in validation, always implement SCI access in PCB design.
- WP#/PD# pin – The WP#/PD# pin can be used for either Write Protect mode or Power-down mode, but only one mode is active at any time. Through the WP#/PD# pin, the NAND controller can either provide write protection in the default mode, or power-down protection in the Power Down mode.

2. Power Supply Design

For high speed digital and analog PCB design, clean and stable power supply is desired for the best performance and reliability. Besides the signal integrity, Electro-Magnetic Interference will also come from poor system power supply design. This section provides general power supply design guidance for designing high speed PCBs using Greenliant SATA NANDrive.

2.1. Power-on Sequence

Most processors or controllers require to have core logic power comes up before the NAND interface. However, Greenliant SATA NANDrive provides design flexibility that allows different power sequences per design need.

1. 3.3V (VDD) comes up 10ms earlier before Digital 1.2V (D1V2) comes up, and then Analog 1.2V (A1V2) and PLL 1.2V. This is the default and recommended sequencing.
2. Digital 1.2V (D1V2) comes up before 3.3V (VDD) comes up, and then Analog 1.2V (A1V2) and PLL 1.2V.
3. 3.3V (VDD) and Digital 1.2V (D1V2) comes up at the same time, and then Analog 1.2V (A1V2) and PLL 1.2V.

2.2. Power Requirements

To assure the system provides enough power for the SATA NANDrive to operate at the peak, the power requirement for each power source should use the max current drawn in the highest demanding application for power budget calculation. For 85LS1032A, the 32GB SATA NANDrive, it requires peak current of 400mA for 3.3V (VDD), and the total peak current of 480mA for Digital 1.2V and Analog 1.2V, where the Analog 1.2V for SATA PHY requires 5% tolerance. The following parameters also need to be considered when choosing the power source according the system PCB:

- When using a switch power supply, make sure the coil can handle the max current output. The same apply to the ferrite bead in the “Pi” filter if used.
- When using LDO regulator, check the max current rating and make sure it can generate the current with 5-10% margin. Regulator efficiency needs to be factored in when doing the calculation.
- Bulk capacitors are required and should be spread out over the section of all components on PCB that are sharing the same power source.
- To prevent electrical and magnetic inference (EMI), all power components of the power circuitry should be placed away from sensitive signals such as high speed digital and analog signals.
- When using connectors to pass signals and power (including GND), make sure there are enough pins to allow the max current to pass through.

There might be other requirements from the power supply components for PCB design. Please check with manufacturers for additional design considerations in the schematic and layout.

2.3. The Power Source Design Guide

Power supply noise will impact SATA signals performance significantly. It is critical to design power source to eliminate noise penetrate into analog signals.

- SATA NANDrive power sources need to have “Pi filter” between the digital and analog 1.2V to filter power noise as shown in Figure 1. Ideally, using plane instead of trace for power and ground will achieve the best noise prevention and heat dissipation. If this practice is impossible due to PCB limitation, use as much power traces as possible for the best result. Multiple via is also required for power and ground signal transfer to different layers or power planes.

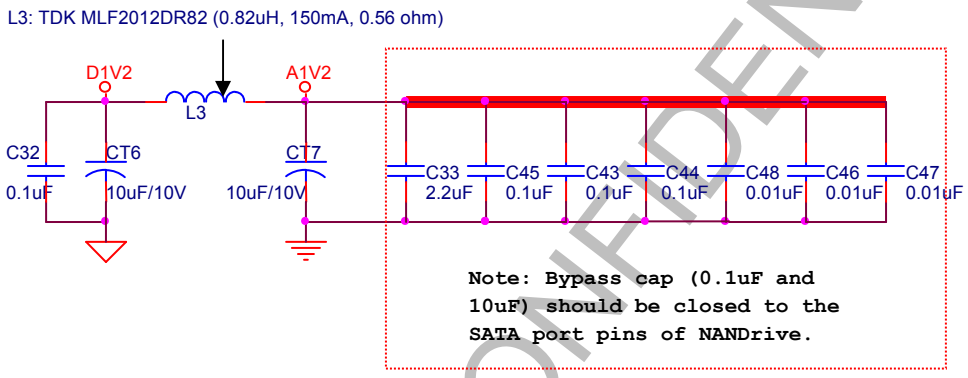

Figure 1: Recommended Pi Filter for Analog power

- PLL, as analog power source, also needs to have ”Pi filter” between the digital and analog 1.2V to filter power noise as shown in Figure 2. Use wider trace layout with multiple via placed is recommended. For better isolation from the high speed SATA signals, PLL power is recommended to come from A1V2.

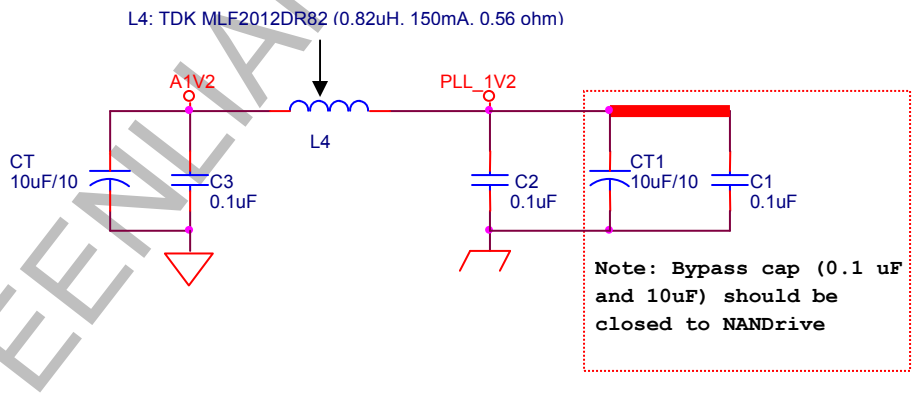

Figure 2: Recommended Pi Filter for System PLL power

2.4. Sleep Mode Recovery Guide

The power management unit (PMU) dramatically reduces the power consumption of the SATA NANDrive by putting the part of the circuitry that is not in operation into sleep mode. When host sends the standard ATA Sleep (E6h) command to SATA NANDrive, the device will set BSY, enter Sleep mode, clear BSY and generate an interrupt. However, the recovery from sleep mode is different from the ATA standard due to the SATA PHY. When SATA NANDrive is put in sleep mode, the SATA PHY will be turned off and it will not receive any command; thus, issuing any command from host will not recover the device from sleep mode. Hardware reset will be required for the recovery.

Therefore, if the application needs to achieve the maximum power reduction and needs SATA NANDrive to enter sleep mode, the host of the application must be capable to control the RESET# pin for sleep mode recovery.

3. SCI Interface for Debugging

SATA NANDrive has a Serial Communication Interface (SCI) that provides information during the system validation and debugging. This serial port is same as UART, and uses standard RS-232 protocol with baud rate 115,200. For information on the SCI connection, see Figure 8. There are three pins for SCI interface:

- SCIDIN: Input data pin to SATA NANDrive
- SCIOUT: Output data pin from SATA NANDrive
- SCICLK: Clock input for SCI. This requires an 11.0592 MHz 3.3V oscillator

These three pins are very critical during debugging stage. Greenliant recommends that you bring them to a multiple pin header or pads if space is limited.

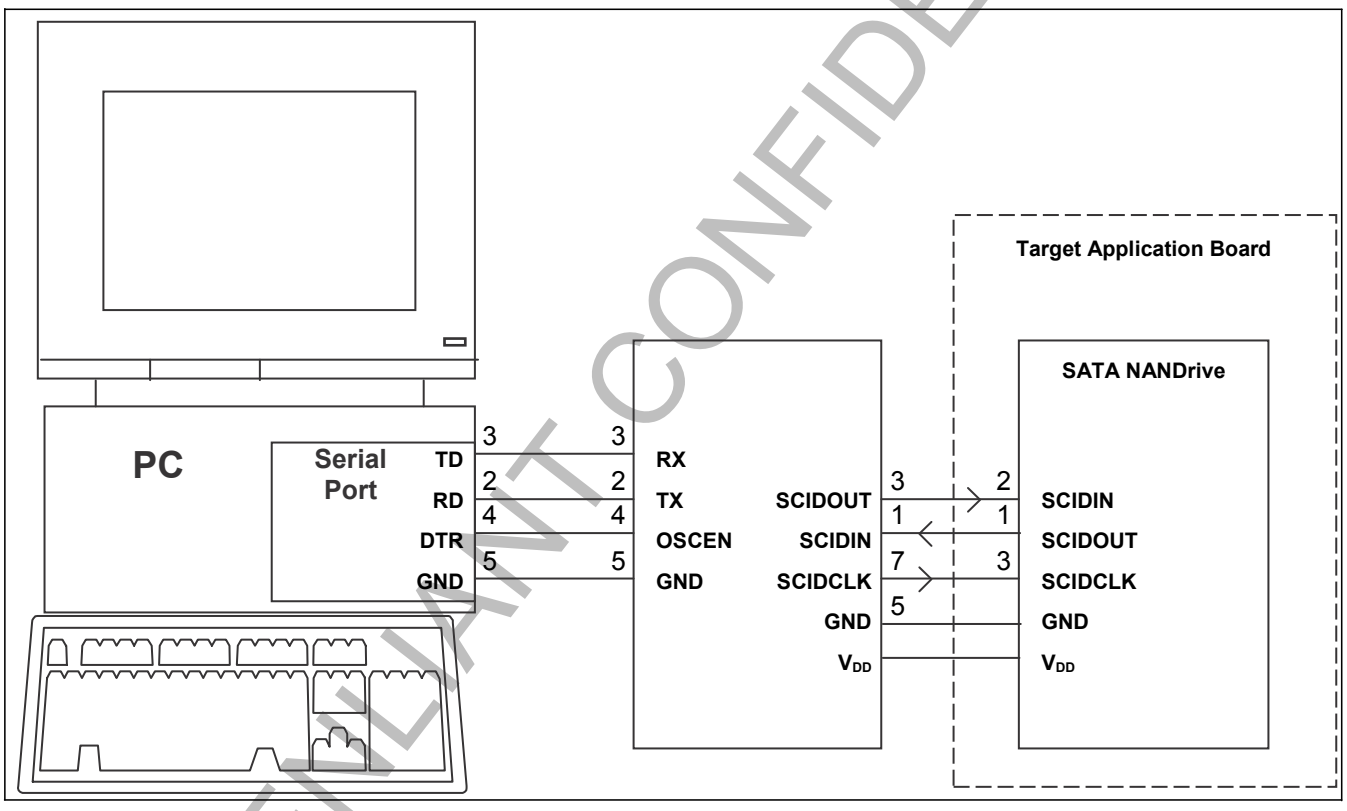

Figure 3: SCI Design Block Diagram

4. PCB Design Suggestions

Since the interface differential pair signals can go up to 1.5Gbps/3.0Gbps, without having good layout on these pairs at extra high frequency will result high Bit Error Rate (BER) due to noise and poor signal quality. Greenliant recommends the following practices:

- Use a characteristic impedance calculator to determine the traces' width and spacing that are required for the specific board stack-up, and the target is 100Ω ±15% differential impedance.
- Maintain parallelism between SATA differential signals with the needed trace spacing to achieve 100Ω ±15% differential impedance. Keep and maintain the overall SATA signals to have Z_{diff} 100-Ω ±15% and Z_{SE} 50-Ω ±10% distribution along all traces. However, deviations will normally occur due to package breakout and connector pins routing. In this case, minimize the deviations in trace length as much as possible.
- Keep SATA signals to be equal-length if possible to avoid mismatching happens, or keep the SATA signals length within 0.1mm difference.
- Keep SATA signals to travel to the exact same symmetric environment and to the same reference GND plane. If there are some SATA signals mismatching existed, keep all the mismatch elements at one end as shown in Figure 4, and let the remaining traces to keep the maximum matching condition.

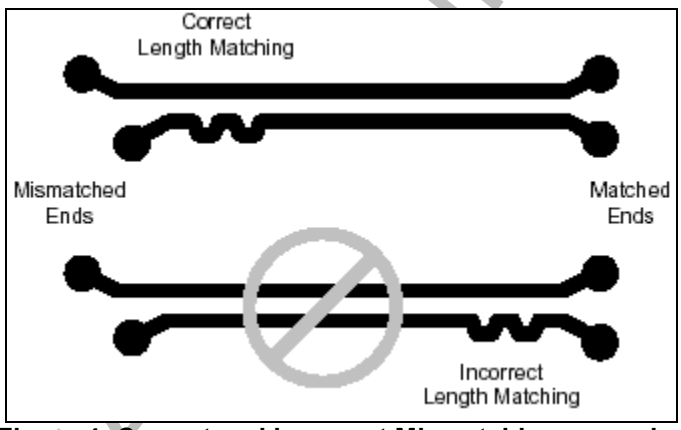

Figure 4: Correct and incorrect Mismatching examples

- Ensure that there is no open trace ends branched from a transmission line. These are also known as "stubs".
- Connect all bypass capacitors near the power pin of NANDrive.

Refer to the application note, *GLS85LSxxxxx PCB layout guide*, for more details regarding PCB design.

4.1. Reference Design Schematic

Figure 5 shows the information about the connection of the SATA bus to SATA NANDrive. The reference schematic is an example and should only be used as a guideline. The final design decision depends on the real application and configurations. When designing the final product, keep the following in mind:

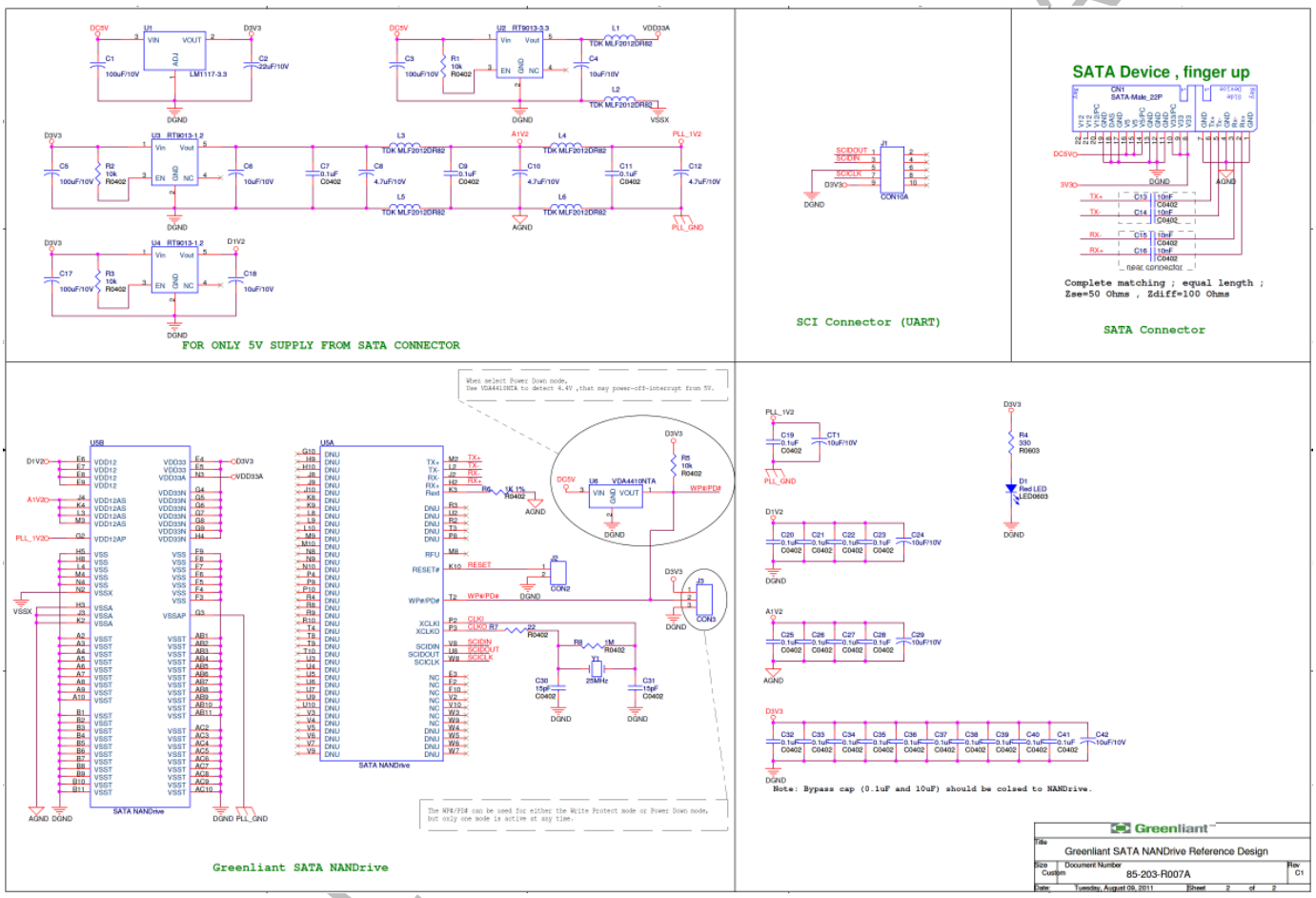

Figure 5: SATA NANDrive Reference Schematic

5. Manufacturing Testing

At its first power-up, the internal controller within SATA NANDrive will search and pair with the internal NAND, and then it executes a low-level format. This initialization time could be as long as minutes, depending on the density. The higher density devices will take longer time. This requirement is limited to the first time the device performs power-up; future power cycling takes less than two seconds.

When performing the manufacturing test, do not apply a reset or power cycle until the first power-up process has completed. If the first power-up process is interrupted, the initialization will repeat upon the next power up until it successfully completes.

When recovering from a power failure, SATA NANDrive will perform a recovery operation during the next power-up which will increase the power-up time before the device can be accessed.

6. Software Support

The SATA NANDrive complies with ATA/ATAPI-7 specification and supports the command set shown in Table 1.

Table 1: SATA NANDrive ATA Command Set

Command	Code	Command	Code
NOP	00h	Data Set Management	06h
Device Reset	08h	Read Sector(s)	20h
Read Sector(s) EXT	24h	Read DMA EXT	25h
Read Native Max Address EXT	27h	Read Multiple EXT	29h
Read Log EXT	2Fh	Write Sector(s)	30h
Write Sector(s) EXT	34h	Write DMA EXT	35h
Set Max Address EXT	37h	Write Multiple EXT	39h
Read Verify Sector(s)	40h	Read Verify Sector(s) EXT	42h
Execute Device Diagnostic	90h	Download Microcode	92h
Packet	A0h	SMART [1]	B0h
Read Multiple	C4h	Write Multiple	C5h
Set Multiple Mode	C6h	Read DMA	C8h
Write DMA	CAh	Get Media Status	DAh
Standby Immediate	E0h	Idle Immediate	E1h
Standby	E2h	Idle	E3h
Read Buffer	E4h	Check Power Mode	E5h
Set Sleep Mode	E6h	Flush Cache	E7h
Write Buffer	E8h	Flush Cache EXT	EAh
Identify Drive	ECh	Set Features	EFh
Security Set Password	F1h	Security Unlock	F2h
Security Erase Prepare	F3h	Security Erase Unit	F4h
Security Freeze Lock	F5h	Security Disable Password	F6h
Read Native Max Address	F8h		
Set Max Lock	F9h/02h	Set Max Set Password	F9h/01h
Set Max Freeze Lock	F9h/04h	Set Max Unlock	F9h/03h
Obsolete CMD by the ATA/ATAPI specifications			
Recalibrate	10h	Read Sectors Without Retry	21h
Write Sectors Without Retry	31h	Write Verify	3Ch
Read Verify Sectors Without Retry	41h	Seek	70h
Initialize Device Parameters	91h	Read DMA Without Retry	C9h
Write DMA Without Retry	CBh	Set Max Address	F9h/00h

1) Please ask your Greenliant contact for more detail.

7. PT2 Utility

PT2 is software tool that allows the user to read drive information, ATA command history, and some debug functions on a computer running the Windows operating system. PT2 provides the following functions:

- Drive information such as size, serial number, and firmware version
- Diagnostics and status
- Firmware upgrade
- Firmware parameters adjustments
- Monitor NAND flash age and bad block numbers
- Set and change passwords

8. Summary

The additional features provided by the SATA NANDrive make any application more reliable, durable and robust. To ensure the best implementation, follow the provided hardware and software design suggestions of Greenliant.

Additional documentation and support is available for many of the application design suggestions mentioned in this guide. The Greenliant Application team also can provide schematic and PCB layout review services to ensure the accuracy of designs. Contact Greenliant for further information about the documents and services available.

9. Reference Documents

Title	Revision	Date
GLS85LSxxxxx PCB Layout Guide	00.020	June 14, 2010
GLS85LSxxxxx Power Supply Design guide	01.010	June 18, 2010
NANDrive SMART Specification	01.200	Feb 10, 2011
NANDrive Security Erase Feature, Purge Command Specification	01.100	Feb 10, 2011
NANDrive Protection Zone Specification	01.000	Feb 10, 2011
WindowsPT2 User Guide	02.000	March 10, 2011
S74109 SATA_and_mini-SATA NANDrive Evaluation Board	01.001	April 5, 2011
Serial Communication Interface (SCI)	01.201	April 8, 2011