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/*
 * Device Tree for Zybo board
 * Partially generated by Device Tree Generator 1.1
 *
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 *
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 * Foundation, Inc., 59 Temple Place, Suite 330, Boston,
 * MA 02111-1307 USA
 */

/dts-v1/;
/ {
    #address-cells = <1>;
    #size-cells = <1>;
    compatible = "xlnx,zynq-7000";
    model = "Xilinx Zynq";
    aliases {
        ethernet0 = &ps7_ethernet_0;
        serial0 = &ps7_uart_1;
        spi0 = &ps7_qspi_0;
    };
    chosen {
        bootargs = "console=ttyPS0,115200 root=/dev/ram rw earlyprintk";
        linux,stdout-path = "/amba.script@0/serial@e0001000";
    };
    cpus {
        #address-cells = <1>;
        #size-cells = <0>;
        ps7_cortexa9_0: cpu@0 {
            bus-handle = <&ps7_axi_interconnect_0>;
            clock-latency = <1000>;
            clocks = <&clkc 3>;
            compatible = "arm,cortex-a9";
            device_type = "cpu";
            interrupt-handle = <&ps7_scugic_0>;
            operating-points = <666667 1000000 333334 1000000 222223 1000000>;
            reg = <0x0>;
        };
    };
};

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    };
    ps7_cortexa9_1: cpu@1 {
        bus-handle = <&ps7_axi_interconnect_0>;
        clocks = <&clk0 3>;
        compatible = "arm,cortex-a9";
        device_type = "cpu";
        interrupt-handle = <&ps7_scugic_0>;
        reg = <0x1>;
    };
};
pmu {
    compatible = "arm,cortex-a9-pmu";
    interrupt-parent = <&ps7_scugic_0>;
    interrupts = <0 5 4>, <0 6 4>;
    reg = <0xf8891000 0x1000>, <0xf8893000 0x1000>;
    reg-names = "cpu0", "cpu1";
};
ps7_ddr_0: memory@0 {
    device_type = "memory";
    reg = <0x0 0x20000000>;
};
ps7_axi_interconnect_0: amba@0 {
    #address-cells = <1>;
    #size-cells = <1>;
    compatible = "xlnx,ps7-axi-interconnect-1.00.a", "simple-bus";
    ranges;
    ps7_af1_0: ps7-afi@f8008000 {
        compatible = "xlnx,ps7-afi-1.00.a";
        reg = <0xf8008000 0x1000>;
    };
    ps7_af1_1: ps7-afi@f8009000 {
        compatible = "xlnx,ps7-afi-1.00.a";
        reg = <0xf8009000 0x1000>;
    };
    ps7_af1_2: ps7-afi@f800a000 {
        compatible = "xlnx,ps7-afi-1.00.a";
        reg = <0xf800a000 0x1000>;
    };
    ps7_af1_3: ps7-afi@f800b000 {
        compatible = "xlnx,ps7-afi-1.00.a";
        reg = <0xf800b000 0x1000>;
    };
    ps7_ddrc_0: ps7-ddrc@f8006000 {
        compatible = "xlnx,zynq-ddrc-1.0";
        reg = <0xf8006000 0x1000>;
        xlnx,has-ecc = <0x0>;
    };
    ps7_dev_cfg_0: ps7-dev-cfg@f8007000 {
        clock-names = "ref_clk", "fclk0", "fclk1", "fclk2", "fclk3";
        clocks = <&clk0 12>, <&clk0 15>, <&clk0 16>, <&clk0 17>, <&clk0 18>;
        compatible = "xlnx,zynq-devcfg-1.0";
        interrupt-parent = <&ps7_scugic_0>;
        interrupts = <0 8 4>;
        reg = <0xf8007000 0x100>;
    };
    ps7_dma_s: ps7-dma@f8003000 {

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        #dma-cells = <1>;
        #dma-channels = <8>;
        #dma-requests = <4>;
        clock-names = "apb_pclk";
        clocks = <&clk 27>;
        compatible = "arm,primecell", "arm,pl330";
        interrupt-names = "abort", "dma0", "dma1", "dma2", "dma3",
            "dma4", "dma5", "dma6", "dma7";
        interrupt-parent = <&ps7_scugic_0>;
interrupts = <0 13 4>, <0 14 4>, <0 15 4>, <0 16 4>, <0 17 4>, <0 40 4>, <0 41 4>, <0 42 4>, <0 43 4>;
        reg = <0xf8003000 0x1000>;
    } ;
    ps7_ethernet_0: ps7-ethernet@e000b000 {
        #address-cells = <1>;
        #size-cells = <0>;
        clock-names = "ref_clk", "aper_clk";
        clocks = <&clk 13>, <&clk 30>;
        compatible = "xlnx,ps7-ethernet-1.00.a";
        interrupt-parent = <&ps7_scugic_0>;
        interrupts = <0 22 4>;
        phy-handle = <&phy0>;
        phy-mode = "rgmii-id";
        reg = <0xe000b000 0x1000>;
        xlnx,eth-mode = <0x1>;
        xlnx,has-mdio = <0x1>;
        xlnx,ptp-enet-clock = <108333336>;
        mdio {
            #address-cells = <1>;
            #size-cells = <0>;
            phy0: phy@1 {
                compatible = "realtek,RTL8211E";
                device_type = "ethernet-phy";
                reg = <1>;
            } ;
        } ;
    } ;
    ps7_globaltimer_0: ps7-globaltimer@f8f00200 {
        clocks = <&clk 4>;
        compatible = "arm,cortex-a9-global-timer";
        interrupt-parent = <&ps7_scugic_0>;
        interrupts = <1 11 0x301>;
        reg = <0xf8f00200 0x100>;
    } ;
    ps7_gpio_0: ps7-gpio@e000a000 {
        #gpio-cells = <2>;
        clocks = <&clk 42>;
        compatible = "xlnx,zynq-gpio-1.0";
        emio-gpio-width = <64>;
        gpio-controller ;
        gpio-mask-high = <0xc0000>;
        gpio-mask-low = <0xfe81>;
        interrupt-parent = <&ps7_scugic_0>;
        interrupts = <0 20 4>;
        reg = <0xe000a000 0x1000>;
    } ;
    ps7_iop_bus_config_0: ps7-iop-bus-config@e0200000 {

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        compatible = "xlnx,ps7-iop-bus-config-1.00.a";
        reg = <0xe0200000 0x1000>;
    };
    ps7_ocmc_0: ps7-ocmc@f800c000 {
        compatible = "xlnx,zynq-ocmc-1.0";
        interrupt-parent = <&ps7_scugic_0>;
        interrupts = <0 3 4>;
        reg = <0xf800c000 0x1000>;
    };
    ps7_pl310_0: ps7-pl310@f8f02000 {
        arm,data-latency = <3 2 2>;
        arm,tag-latency = <2 2 2>;
        cache-level = <2>;
        cache-unified;
        compatible = "arm,pl310-cache";
        interrupt-parent = <&ps7_scugic_0>;
        interrupts = <0 2 4>;
        reg = <0xf8f02000 0x1000>;
    };
    ps7_qspi_0: ps7-qspi@e000d000 {
        clock-names = "ref_clk", "pclk";
        clocks = <&clkc 10>, <&clkc 43>;
        compatible = "xlnx,zynq-qspi-1.0";
        interrupt-parent = <&ps7_scugic_0>;
        interrupts = <0 19 4>;
        is-dual = <0>;
        num-cs = <1>;
        reg = <0xe000d000 0x1000>;
        xlnx,fb-clk = <0x1>;
        xlnx,qspi-mode = <0x0>;
        #address-cells = <1>;
        #size-cells = <0>;
        flash@0 {
            compatible = "s25fl128s1";
            reg = <0x0>;
            spi-tx-bus-width = <1>;
            spi-rx-bus-width = <4>;
            spi-max-frequency = <50000000>;
            #address-cells = <1>;
            #size-cells = <1>;
            partition@qspi-fsbl-uboot {
                label = "qspi-fsbl-uboot";
                reg = <0x0 0x400000>;
            };
            partition@qspi-linux {
                label = "qspi-linux";
                reg = <0x400000 0x500000>;
            };
            partition@qspi-device-tree {
                label = "qspi-device-tree";
                reg = <0x900000 0x20000>;
            };
            partition@qspi-user {
                label = "qspi-user";
                reg = <0x920000 0x6E0000>;
            };
        };
    };

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    };

};

ps7_qspi_linear_0: ps7-qspi-linear@fc000000 {
    clock-names = "ref_clk", "aper_clk";
    clocks = <&clkc 10>, <&clkc 43>;
    compatible = "xlnx,ps7-qspi-linear-1.00.a";
    reg = <0xfc000000 0x1000000>;
};

ps7_scugic_0: ps7-scugic@f8f01000 {
    #address-cells = <2>;
    #interrupt-cells = <3>;
    #size-cells = <1>;
    compatible = "arm,cortex-a9-gic", "arm,gic";
    interrupt-controller;
    num_cpus = <2>;
    num_interrupts = <96>;
    reg = <0xf8f01000 0x1000>, <0xf8f00100 0x100>;
};

ps7_scutimer_0: ps7-scutimer@f8f00600 {
    clocks = <&clkc 4>;
    compatible = "arm,cortex-a9-twd-timer";
    interrupt-parent = <&ps7_scugic_0>;
    interrupts = <1 13 0x301>;
    reg = <0xf8f00600 0x20>;
};

ps7_scuwdt_0: ps7-scuwdt@f8f00620 {
    clocks = <&clkc 4>;
    compatible = "xlnx,ps7-scuwdt-1.00.a";
    device_type = "watchdog";
    interrupt-parent = <&ps7_scugic_0>;
    interrupts = <1 14 0x301>;
    reg = <0xf8f00620 0xe0>;
};

ps7_sd_0: ps7-sdio@e0100000 {
    clock-frequency = <500000000>;
    clock-names = "clk_xin", "clk_ahb";
    clocks = <&clkc 21>, <&clkc 32>;
    compatible = "arasan,sdhci-8.9a";
    interrupt-parent = <&ps7_scugic_0>;
    interrupts = <0 24 4>;
    reg = <0xe0100000 0x1000>;
    xlnx,has-cd = <0x1>;
    xlnx,has-power = <0x0>;
    xlnx,has-wp = <0x1>;
};

ps7_slcr_0: ps7-slcr@f8000000 {
    #address-cells = <1>;
    #size-cells = <1>;
    compatible = "xlnx,zynq-slcr", "syscon";
    ranges;
    reg = <0xf8000000 0x1000>;
    clk: clkc@100 {
        #clock-cells = <1>;
        clock-output-names = "armpll", "ddrpll", "iopll", "cpu_6or4x", "cpu_3or2x",
            "cpu_2x", "cpu_1x", "ddr2x", "ddr3x", "dci",

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        "lqspi", "smc", "pcap", "gem0", "gem1",
        "fclk0", "fclk1", "fclk2", "fclk3", "can0",
        "can1", "sdio0", "sdio1", "uart0", "uart1",
        "spi0", "spi1", "dma", "usb0_aper", "usb1_aper",
        "gem0_aper", "gem1_aper", "sdio0_aper", "sdio1_aper", "spi0_aper",
        "spi1_aper", "can0_aper", "can1_aper", "i2c0_aper", "i2c1_aper",
        "uart0_aper", "uart1_aper", "gpio_aper", "lqspi_aper", "smc_aper",
        "swdt", "dbg_trc", "dbg_apb";
    compatible = "xlnx,ps7-clkc";
    fclk-enable = <0xf>;
    ps-clk-frequency = <50000000>;
    reg = <0x100 0x100>;
};

};
ps7_ttc_0: ps7-ttc@f8001000 {
    clocks = <&clkc 6>;
    compatible = "cdns,ttc";
    interrupt-names = "ttc0", "ttc1", "ttc2";
    interrupt-parent = <&ps7_scugic_0>;
    interrupts = <0 10 4>, <0 11 4>, <0 12 4>;
    reg = <0xf8001000 0x1000>;
};

ps7_uart_1: serial@e0001000 {
    clock-names = "uart_clk", "pclk";
    clocks = <&clkc 24>, <&clkc 41>;
    compatible = "xlnx,xuartps", "cdns,uart-r1p8";
    current-speed = <115200>;
    device_type = "serial";
    interrupt-parent = <&ps7_scugic_0>;
    interrupts = <0 50 4>;
    port-number = <0>;
    reg = <0xe0001000 0x1000>;
    xlnx,has-modem = <0x0>;
};

ps7_usb_0: ps7-usb@e0002000 {
    clocks = <&clkc 28>;
    compatible = "xlnx,ps7-usb-1.00.a", "xlnx,zynq-usb-1.00.a";
    dr_mode = "host";
    interrupt-parent = <&ps7_scugic_0>;
    interrupts = <0 21 4>;
    phy_type = "ulpi";
    reg = <0xe0002000 0x1000>;
    xlnx,usb-reset = "MIO 46";
};

ps7_xadc: ps7-xadc@f8007100 {
    clocks = <&clkc 12>;
    compatible = "xlnx,zynq-xadc-1.00.a";
    interrupt-parent = <&ps7_scugic_0>;
    interrupts = <0 7 4>;
    reg = <0xf8007100 0x20>;
};

};
};
};

```