

Name: \_\_\_\_\_ CM: \_\_\_\_\_ Start Date: Thursday, June 6, 2019

Name: \_\_\_\_\_ CM: \_\_\_\_\_ Due Date: Friday, June 8, 2019

## Software and Hardware Co-Design with Zybo, Spring 2019 HUST

### Lab #4 Block Design and IPs Creation on Zybo

This is an individual lab. Each student must perform it and demonstrate parts 1 and 2 of this lab to obtain credit for it. Late lab submission will be accepted with a grade reduction of 20% for each day that it is late.

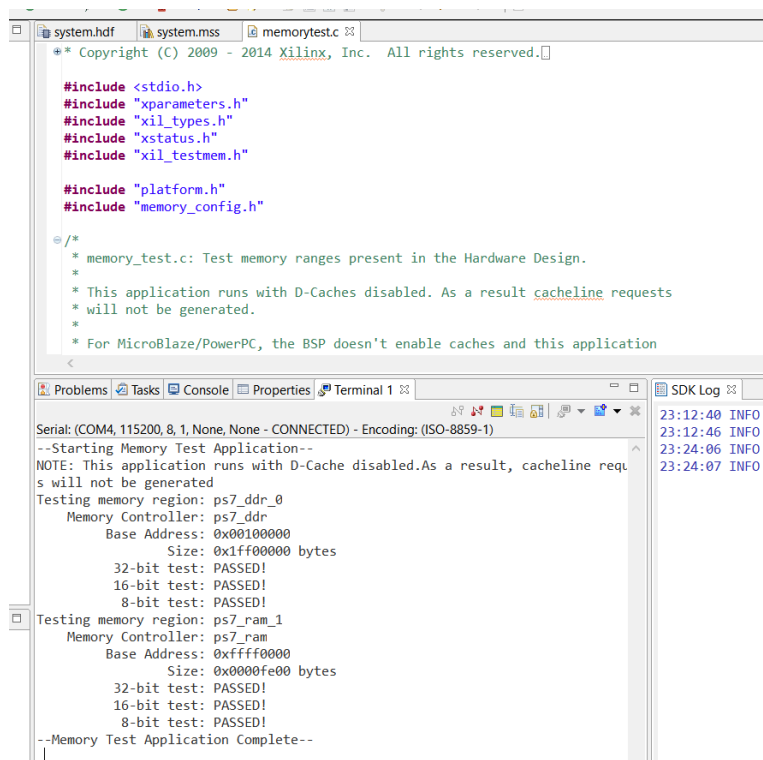
You will need to download the first five labs are under “Embedded System Design Flow on Zynq using Vivado” from the Xilinx University Program (XUP) Website. Go to [www.xilinx.com](http://www.xilinx.com). Choose **Support/University Program** and then **Resource/Workshops**. See the appendix of this lab for more details.

## I. Objectives

- Follow the first two labs from Xilinx University Program on Advanced Embedded System Design on Zynq using Vivado.
  - a. **Lab #4 Part 1: ZYNQ Lab 1** Use Vivado to Build Embedded Systems, pages ZYNQ1-1 to ZYNQ1-16.
  - b. **Lab #4 Part 2: ZYNQ Lab 2** Adding IP Cores in PL, pages ZYNQ2-1 to ZYNQ2-16.

## II. Deliverables

### II.1 Demonstrate Lab #4 Part 1 on memory test display on an SDK terminal.



```
system.hdf | system.mss | memorytest.c
/* Copyright (C) 2009 - 2014 Xilinx, Inc. All rights reserved.

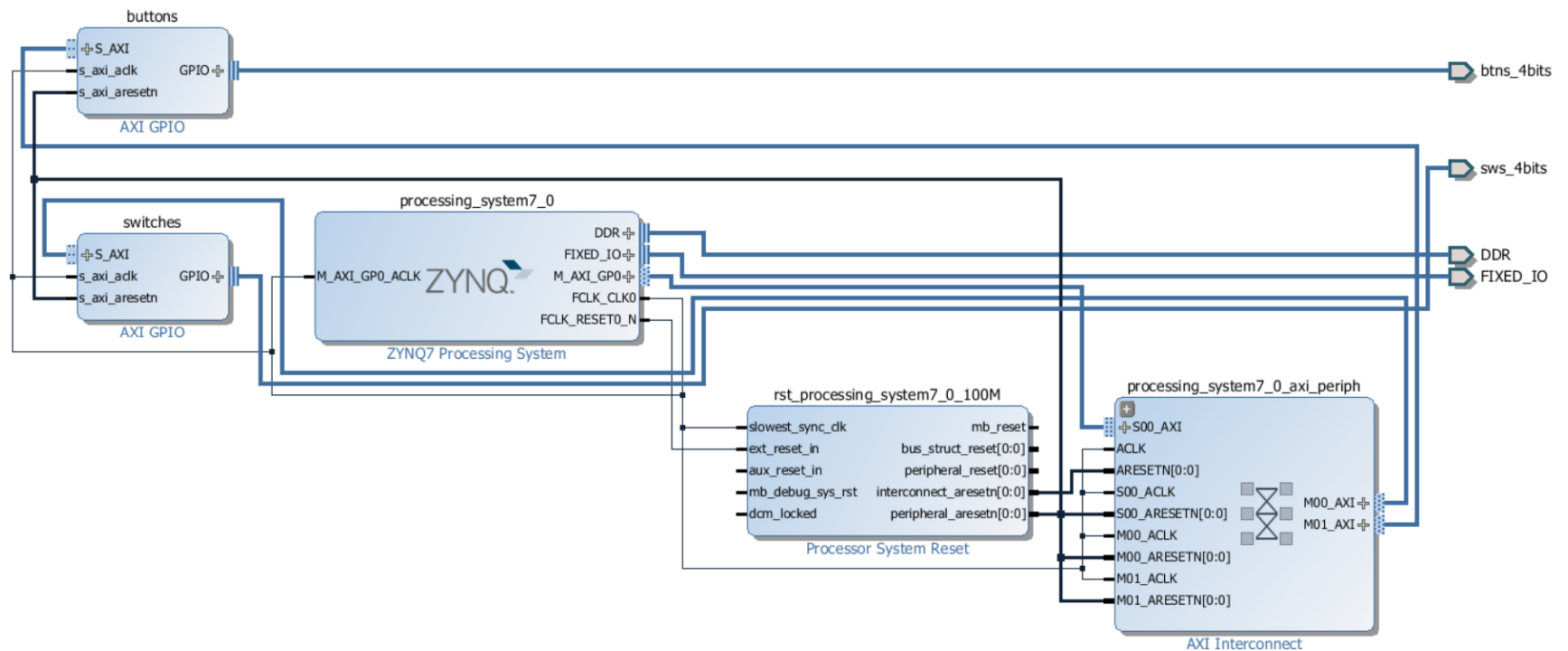
#include <stdio.h>
#include "xparameters.h"
#include "xil_types.h"
#include "xstatus.h"
#include "xil_testmem.h"

#include "platform.h"
#include "memory_config.h"

/*
 * memory_test.c: Test memory ranges present in the Hardware Design.
 *
 * This application runs with D-Caches disabled. As a result cacheline requests
 * will not be generated.
 *
 * For MicroBlaze/PowerPC, the BSP doesn't enable caches and this application
 */

Serial: (COM4, 115200, 8, 1, None, None - CONNECTED) - Encoding: (ISO-8859-1)
--Starting Memory Test Application--
NOTE: This application runs with D-Cache disabled.As a result, cacheline requests will not be generated
Testing memory region: ps7_ddr_0
Memory Controller: ps7_ddr
Base Address: 0x00100000
Size: 0x1fff0000 bytes
32-bit test: PASSED!
16-bit test: PASSED!
8-bit test: PASSED!
Testing memory region: ps7_ram_1
Memory Controller: ps7_ram
Base Address: 0xffff0000
Size: 0x0000fe00 bytes
32-bit test: PASSED!
16-bit test: PASSED!
8-bit test: PASSED!
--Memory Test Application Complete--
```

## II.1 Demonstrate Lab #4 Part 2 circuit to display status of push buttons and slide switches.



```

XGpio_Initialize(&push, XPAR_BUTTONS_DEVICE_ID);
XGpio_SetDataDirection(&push, 1, 0xffffffff);

while (1)
{
    psb_check = XGpio_DiscreteRead(&push, 1);
    xil_printf("Push Buttons Status %x\r\n", psb_check);
}
  
```

Serial: (COM4, 115200, 8, 1, None, None - CONNECTED) - Encoding: (ISO-8859-1)

```

DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
DIP Switch Status F
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DIP Switch Status F
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DIP Switch Status F
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Push Buttons Status 0
DIP Switch Status F
Push Buttons Status 0
  
```

### III. Appendix Download the first five labs from Xilinx U Program

#### III.1 Install files needed for the first five labs of Embedded Design Workshop

The first five labs are under “Embedded System Design Flow on Zynq using Vivado” from the Xilinx University Program (XUP) Website.

Go to [www.xilinx.com](http://www.xilinx.com). Choose **Support/University Program** and then **Resource/Workshops**.

Open **Embedded System Design Flow on Zynq**.

Find the relevant files under **2015x Workshop Material** as shown on the right.

Download the following three zipped files:

- (1) labdocs.zip which contains 2015\_2\_zynq\_labdocs\_pdf folder.
- (2) Lab Source File.zip, which contains 2015\_2\_zynq\_sources folder.
- (3) Zybo Board Files, which contains Zybo folder.

2014x Workshop Material ▾

Common to ZedBoard and ZYBO

- Labdocs (PDF)
- Lab Source File
- Labdocs and Presentation (docx and pptx)\*

ZedBoard

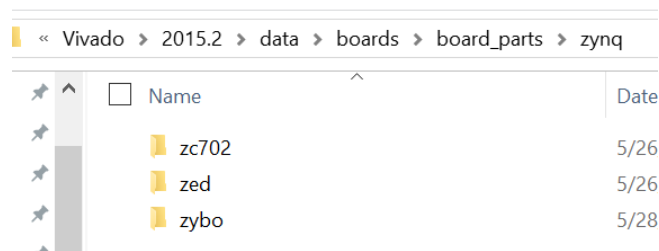
- README
- Labsolution\*

ZYBO

- README
- Board Files (required to do the labs)
- Labsolution\*

Your download folder should have the following zipped files.

- (a) Create a folder “c:\xup\embedded\” on your laptop PC’s hard drive. Upzip both 2015\_2\_zynq\_labdocs\_pdf.zip and 2015\_2\_zynq\_sources.zip into this “c:\xup\embedded\” folder.
- (b) Finally, unzip zybo.zip file to the following folder  
 C:\Xilinx\Vivado\2015.2\data\boards\board\_parts\zynq. This directory contains the board files for various boards, which has other default board files. Placing this “Zybo” file in the specified directory will allow you to select the Zybo board during the design. Vivado is not aware of the Zybo board without performing this step.



### III.2 Create a directory for folders and files of these labs

Create a directory “c:\xup\embedded\2015\_2\_zynq\_labs” as a folder to contain all five labs of “Embedded System Design Flow on Zynq using Vivado”.

