Name: _____ CM: _____ Start Date: Thursday, June 6, 2019

Due Date: Friday, June 7, 2019

Software and Hardware Co-Design with Zybo, Spring 2019 HUST
Lab #5 Add custom IP and write basic software

This is an individual lab. Each student must perform it and demonstrate parts 2 of this lab to obtain credit for it. Late lab submission will be accepted with a grade reduction of 10% for each day that it is late.

You will need to download the first five labs are under "Embedded System Design Flow on Zynq using Vivado" from the Xilinx University Program (XUP) Website. Go to www.xilinx.com. Choose **Support/University Program** and then **Resource/Workshops.** See the appendix of this lab for more details.

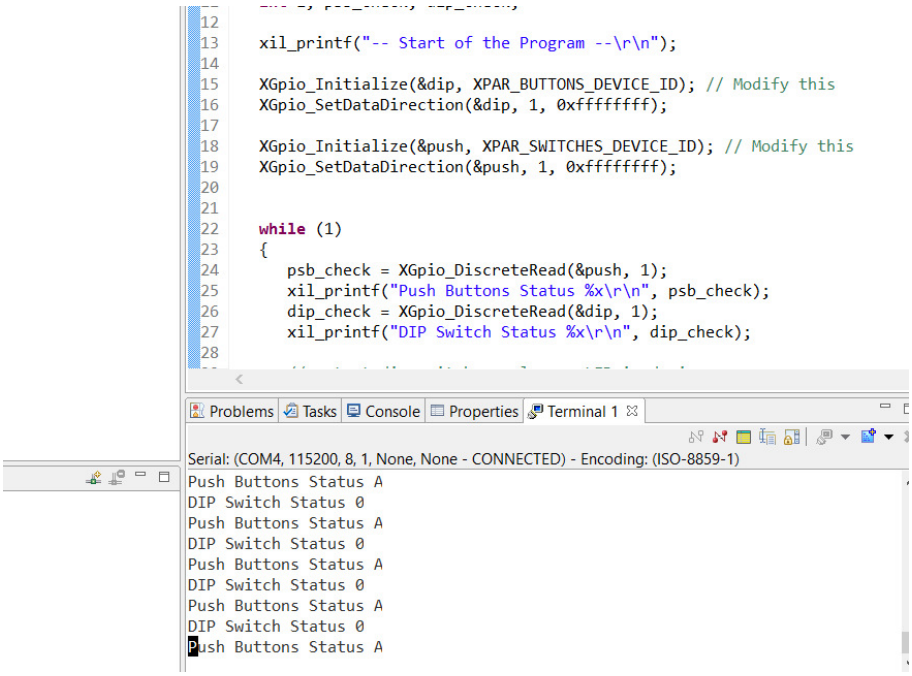
I. Objectives

- *Follow the second two labs from Xilinx University Program on Advanced Embedded System Design on Zynq using Vivado.*
  a. ***Lab #5 Part 1: ZYNQ Lab 3*** *Use Vivado to Build Embedded Systems, pages ZYNQ3-1 to ZYNQ3-16.*
  b. ***Lab #5 Part 2: ZYNQ Lab 4*** *Adding IP Cores in PL, pages ZYNQ2-1 to ZYNQ2-16. Demonstrate this part to get credit for this lab.*

II. Deliverables

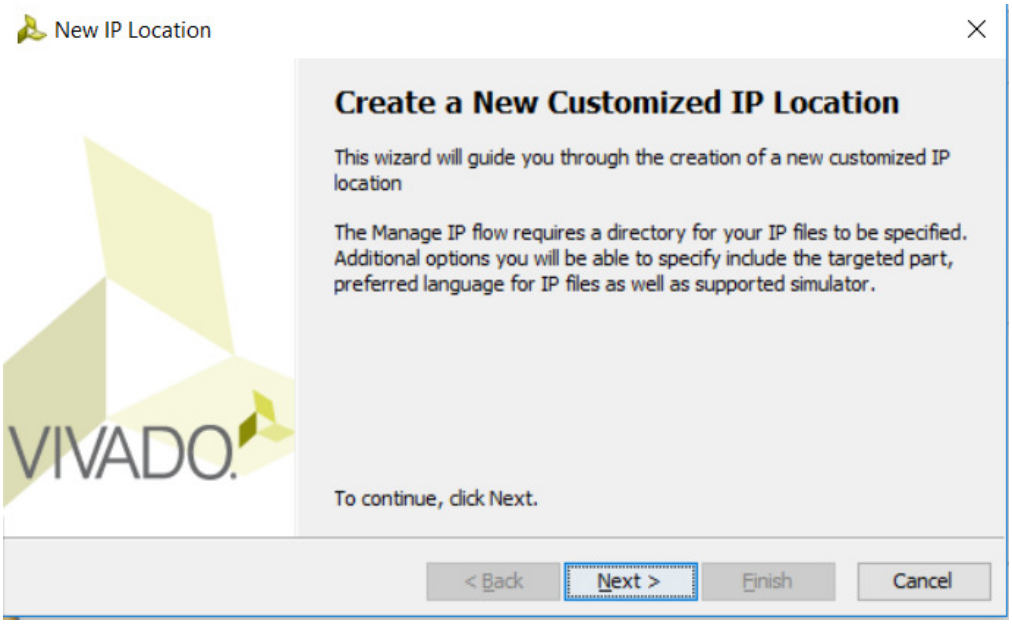
II.1 Demonstrate Lab #5 Part 2 to get credit for this lab.

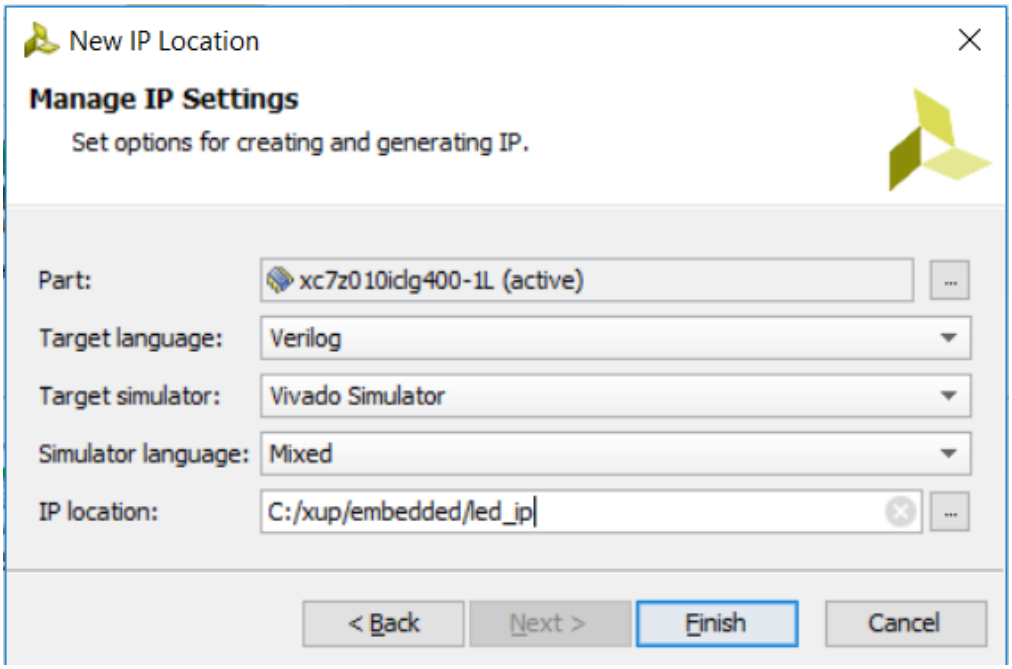
Demonstrate your Lab #5 Part 2 to get credit for Lab #5. Show your SDK terminal display of push button and slide switches. Demonstrate the states of LEDs as you press corresponding push buttons.



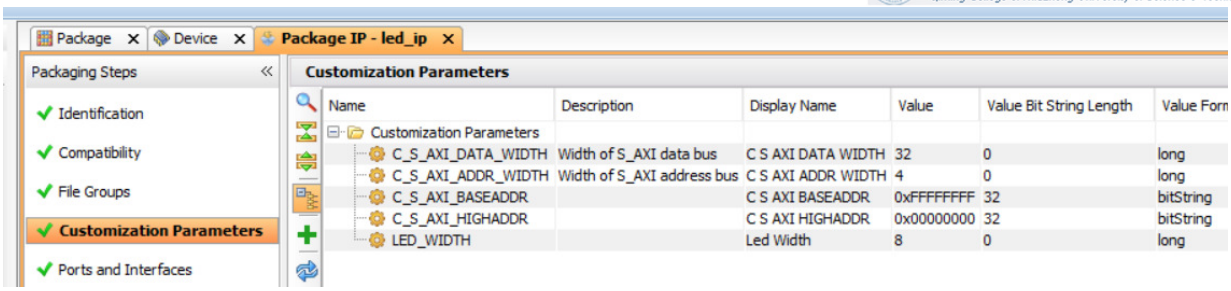
III. Lab #5 Part 1 Create a Custom IP, Part Number xc7z010iclg400-1L

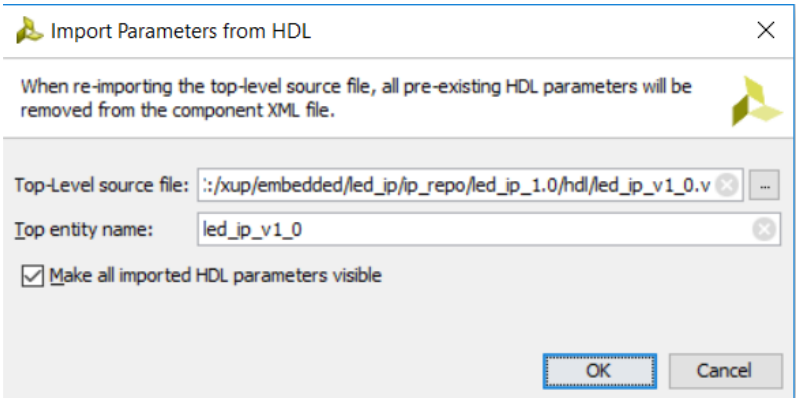
Follow Lab Workbook on Adding Custom IP to the System, pages ZYNQ3-1 to ZYNQ3-16 to create a new IP and add it to your block design. The new IP directory is C:/xup/embedded/led_ip. Click "Finish".



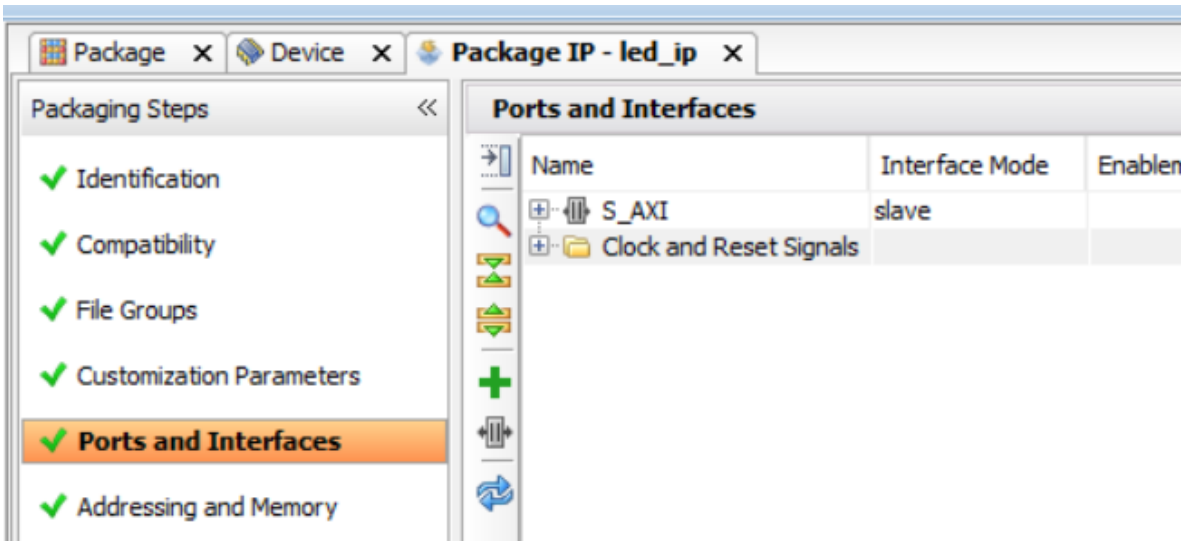


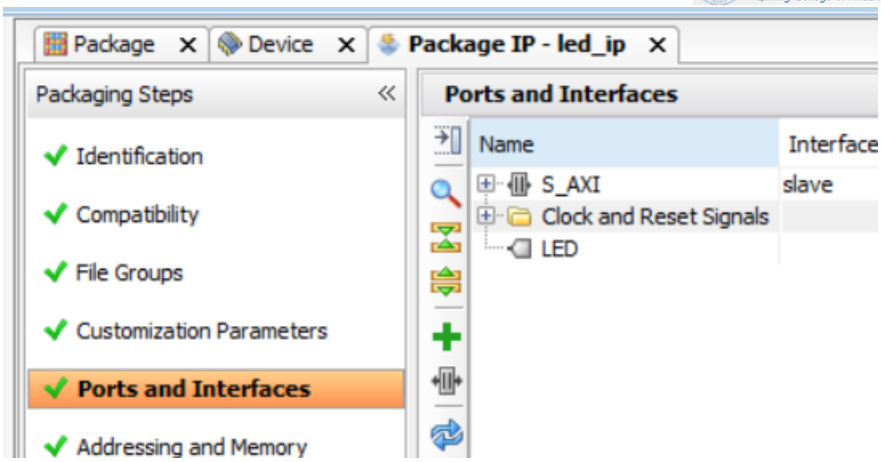
If you don't see LED_WIDTH parameter, right click on the Customization Parameters menu, choose "Import Parameters". Choose led_ip_v1_0 so that LED_WIDTH would show.





If you don't see LED port under Ports and Interfaces menu, right click on the ports window, choose "Import IP Ports".

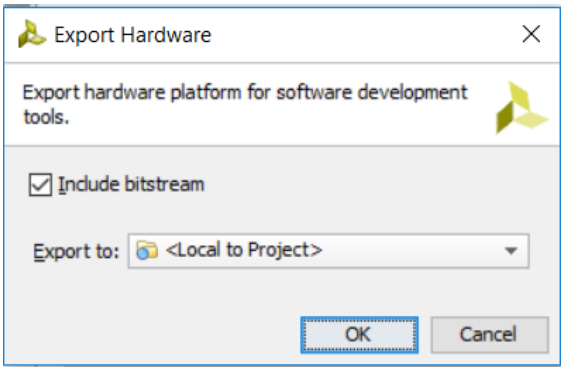




IV. Lab #5 Part 2

Save lab5part1SoC project as lab5part2SoC project. Follow XUP Lab #4 pages ZYNQ 4-1 to ZYNQ 4-11 to complete this part of Lab #5.

You do not need to do any hardware design. Just generate the bit stream file, open implemented design and export hardware.



And then start SDK.

V. Demonstrate your Lab #5 Part 2

V.1 Lab #5 Part 1 circuit with 4-bit LED IP.

Generate bit stream file for this block design. Make sure lab3_zybo.xdc file is attached to this design.