Q2. Pipelined CSGY6133

	Read		Writeback	
	Mem	EX	Mem	WB
sub $rd,\ rs$	/	$rd,\ rs$	/	rs
subm $rd,\ rs$	rd	$rs,\ Mem[rd]$	/	rs
st $rd,\ rs$	$rd,\ rs$	/	$Mem[rd]$	/

The above table shows how these three instructions access the registers in different states. As we known, the raw dependency only happens when the first instruction writes back to the same register/memoryblock that the second instruction reads. Therefore, we only have to consider about the rs of 'sub' and 'subm' in the first instruction. As to 'st' instruction, the writeback can always be done in Mem state before the next instruction comes. So 'st' won't cause raw dependency at all.

The table below shows all possiable pair that will cause the raw dependency.

1.	**sub** $1, $2	Raw Hazard	Resolving
2.	**sub** $2, $3	Yes	EX-EX forwarding
	sub $3, $2	Yes	EX-EX forwarding
	sub $2, $2	Yes	EX-EX forwarding
	subm $2, $3	Yes	Stalling before EX, EX-Mem forwarding
	subm $3, $2	Yes	EX-EX forwarding
	subm $2, $2	Yes	Stalling before EX, EX-Mem forwarding
	st $2, $3	Yes	Stalling before EX, EX-Mem forwarding
	st $3, $2	Yes	Stalling before EX, EX-Mem forwarding
	st $2, $2	Yes	Stalling before EX, EX-Mem forwarding

1.	**subm** $1, $2	Raw Hazard	Resolving
2.	**sub** $2, $3	Yes	EX-EX forwarding
	sub $3, $2	Yes	EX-EX forwarding
	sub $2, $2	Yes	EX-EX forwarding
	subm $2, $3	Yes	Stalling before EX, EX-Mem forwarding
	subm $3, $2	Yes	EX-EX forwarding
	subm $2, $2	Yes	Stalling before EX, EX-Mem forwarding
	st $2, $3	Yes	Stalling before EX, EX-Mem forwarding
	st $3, $2	Yes	Stalling before EX, EX-Mem forwarding
	st $2, $2	Yes	Stalling before EX, EX-Mem forwarding