Assignment #1

CS-GY 6133

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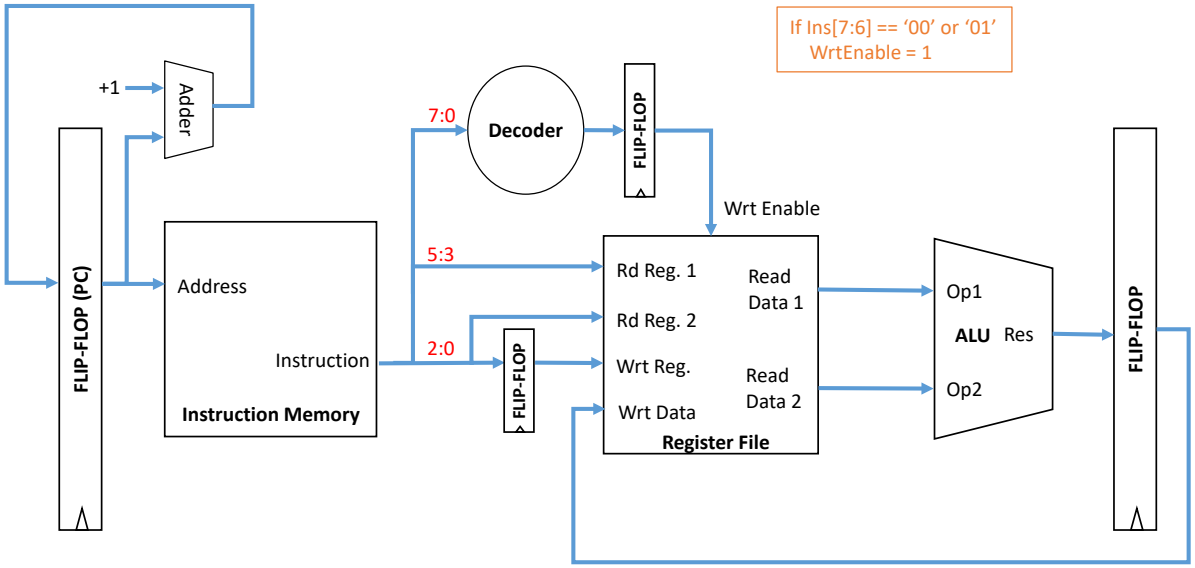
Q1. Single-cycle Processor Design

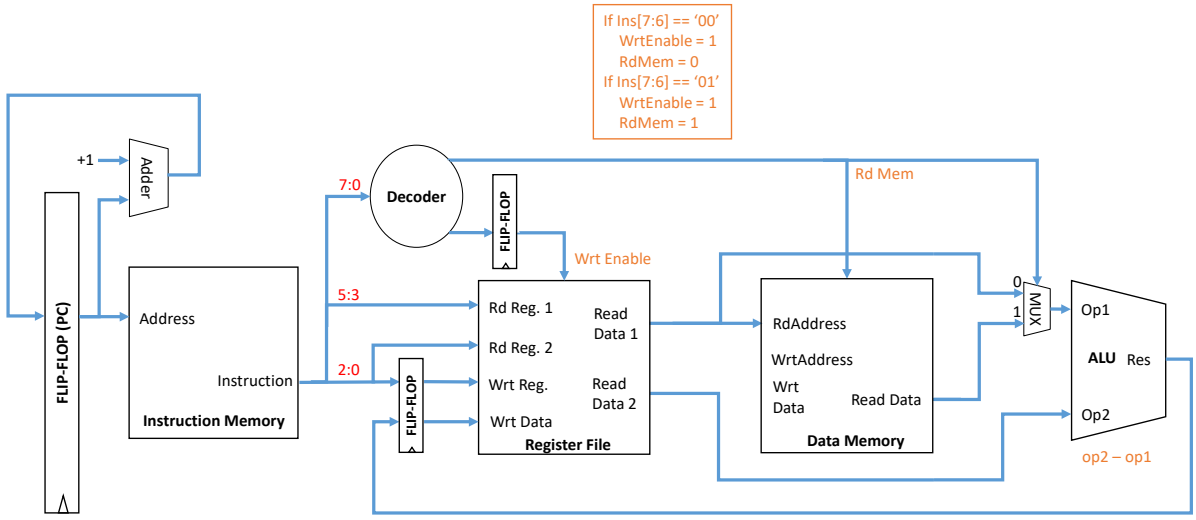
A1.1

Supporting 'sub' instruction



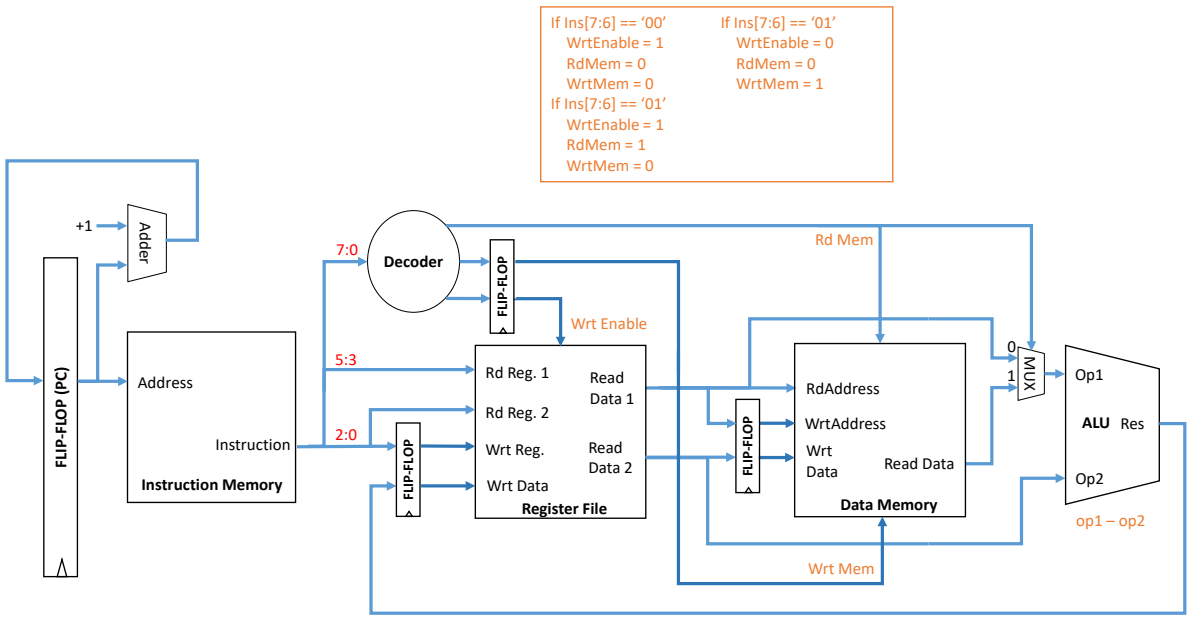
A1.2

Supporting 'sub', 'subm' instructions



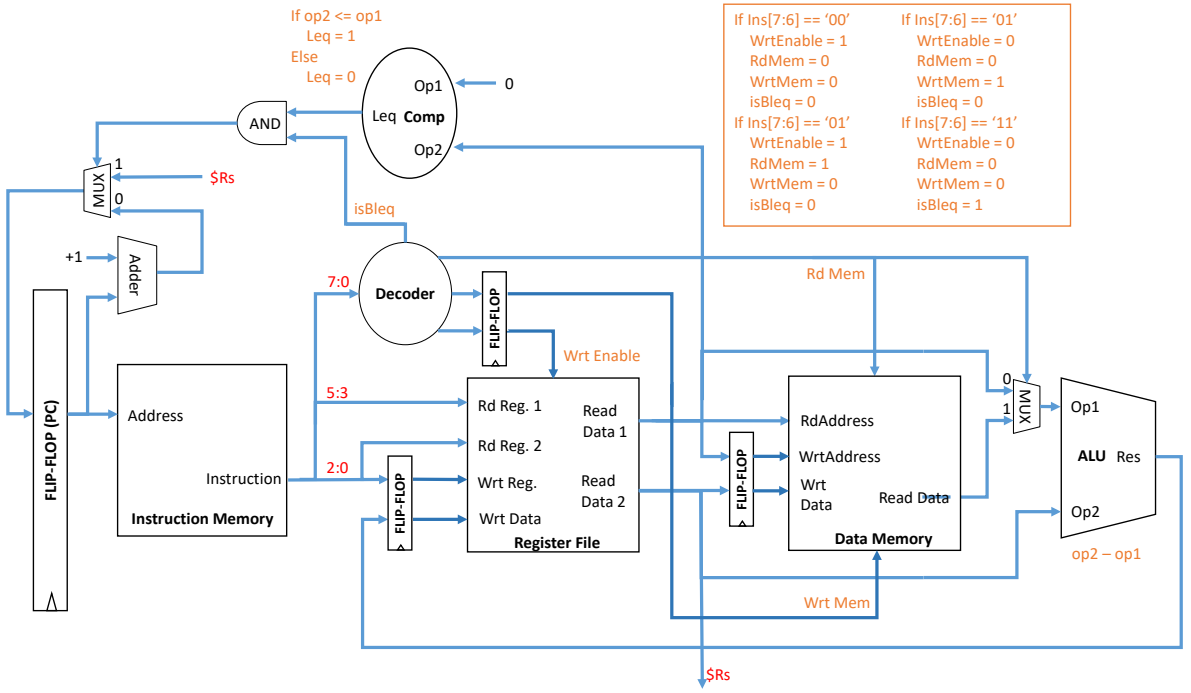
A1.3

Supporting 'sub', 'subm', 'st' instructions



A1.4

Supporting 'sub', 'subm', 'st', 'bleq' instructions



A1.5

The path 'IM-RF-DM-MUX-ALU' takes the longest time (4.5ns). So the maximum frequency is 222.2 MHz.

Q2. Pipelined CSGY6133

The table below shows how these three instructions access the registers in different states. As we known, the RAW hazard only happens when the first instruction writes back to the same register/memory-block that the second instruction reads. Therefore, we only have to consider about the rs of 'sub' and 'subm' in the first instruction. As to 'st' instruction, the data will be update immediately at next positive clock edges. So 'st' won't cause RAW hazard at all.

	Read		Writeback	
	Mem	EX	Mem	WB
sub $rd,\ rs$	/	$rd,\ rs$	/	rs
subm $rd,\ rs$	rd	$rs,\ Mem[rd]$	/	rs
st $rd,\ rs$	$rd,\ rs$	/	$Mem[rd]$	/

The table below shows all possible pairs that will cause the RAW hazard.

1.	**sub** \$1, \$2	RAW Hazard	Resolving
2.	**sub** \$2, \$3	Yes	EX-EX forwarding
	sub \$3, \$2	Yes	EX-EX forwarding
	sub \$2, \$2	Yes	EX-EX forwarding
	subm \$2, \$3	Yes	Stalling before EX, EX-Mem forwarding
	subm \$3, \$2	Yes	EX-EX forwarding
	subm \$2, \$2	Yes	Stalling before EX, EX-Mem forwarding[1]
	st \$2, \$3	Yes	Stalling before EX, EX-Mem forwarding
	st \$3, \$2	Yes	Stalling before EX, EX-Mem forwarding
	st \$2, \$2	Yes	Stalling before EX, EX-Mem forwarding

1.	**subm** $1, $2	RAW Hazard	Resolving
2.	**sub** $2, $3	Yes	EX-EX forwarding
	sub $3, $2	Yes	EX-EX forwarding
	sub $2, $2	Yes	EX-EX forwarding
	subm $2, $3	Yes	Stalling before EX, EX-Mem forwarding
	subm $3, $2	Yes	EX-EX forwarding
	subm $2, $2	Yes	Stalling before EX, EX-Mem forwarding[1]
	st $2, $3	Yes	Stalling before EX, EX-Mem forwarding
	st $3, $2	Yes	Stalling before EX, EX-Mem forwarding
	st $2, $2	Yes	Stalling before EX, EX-Mem forwarding

EX-EX Forwarding

Cycle	1	2	3	4	5	6
sub $1, $2	IF	RF/ID	Mem	EX	WB	
sub $2, $3		IF	RF/ID	Mem	EX	WB

EX-Mem Forwarding (with stalling)

Cycle	1	2	3	4	5	6	7
sub $1, $2	IF	RF/ID	Mem	EX	WB		
sub $2, $3		IF	RF/ID	Mem stalling	Mem	EX	WB