

Q4

4.1

1GB byte-addressable memory need 30 bits address.

- (a) 8KB cache with 1 byte blocks can contain 8192 blocks. $8192 = 2^{13}$ so we need 13 bits for index and 17 bits tag, 0 bit offset.
- (b) 8KB cache with 4 byte blocks can contain 2048 blocks. $2048 = 2^{11}$ so we need 11 bits for index and 2 bits offset. The rest 17 bits for tag.
- (c) 8 Byte blocks so offset is 3 bits. 2-way and 8 byte so $8 \times 1024 / (4 \times 2) = 1024 = 2^{10}$ blocks per way so we need 10 bits for index and $30 - 10 - 3 = 17$ bits for tag.
- (d) 16 Byte blocks so offset is 4 bits. 4-way and 16 byte so $8 \times 1024 / (16 \times 4) = 128 = 2^7$ blocks per way so we need 7 bits for index and $30 - 7 - 4 = 19$ bits for tag.
- (e) For Fully-associative cache, there are as many ways as blocks. 8KB cache with 8 byte blocks contains $8 \times 1024 / 8 = 1024$ blocks. So fully-associative cache has 1024-way set associative. 8 byte blocks so offset is 3 bits. One block per way so 0 bit for index and $30 - 3 = 27$ bits for tag.

To sum up:

Question	Offset bits	Index bits	Tag bits
(a)	0	13	17
(b)	2	11	17
(c)	3	10	17
(d)	4	7	19
(e)	3	0	27

4.2

Accessing Address	Hit or Miss State	Memory State after this access	
0	Compulsory Miss	0	1
1	Hit	Not Changed	
2	Compulsory Miss	0	1
		2	3
3	Hit	Not Changed	
4	Conflict Miss	4	5
		2	3
5	Hit	Not Changed	
6	Conflict Miss	4	5
		6	7

7	Hit	Not Changed	
8	Conflict Miss	8	9
		6	7
9	Hit	Not Changed	
0	Conflict Miss	0	1
		6	7
1	Hit	Not Changed	
...	Same as the previous same accessing address	Same as state after the previous same accessing address	

4.3

Accessing Address	Hit or Miss State	Memory State after this access		Victim Cache State	
0	Compulsory Miss	0	1		
1	Hit in main cache	Not Changed		Not Changed	
2	Compulsory Miss	0	1	Not Changed	
		2	3		
3	Hit in main cache	Not Changed		Not Changed	
4	Conflict Miss	4	5	0	1
		2	3		
5	Hit in main cache	Not Changed		Not Changed	
6	Conflict Miss	4	5	0	1
				2	3
		6	7		
7	Hit in main cache	Not Changed		Not Changed	
8	Conflict Miss	8	9	4	5
				2	3
		6	7		

9	Hit in main cache	Not Changed		Not Changed
0	Conflict Miss	0	1	4
				5
		6	7	8
				9
1	Hit in main cache	Not Changed		Not Changed
2	Conflict Miss	0	1	6
				7
		2	3	8
				9
3	Hit in main cache	Not Changed		Not Changed
4	Conflict Miss	4	5	6
				7
		2	3	0
				1
5	Hit in main cache	Not Changed		Not Changed
6	Hit in the victim cache	4	5	2
				3
		6	7	0
				1
7	Hit in main cache	Not Changed		Not Changed
8	Conflict Miss	8	9	2
				3
		6	7	4
				5
9	Hit in main cache	Not Changed		Not Changed