

Homework 3

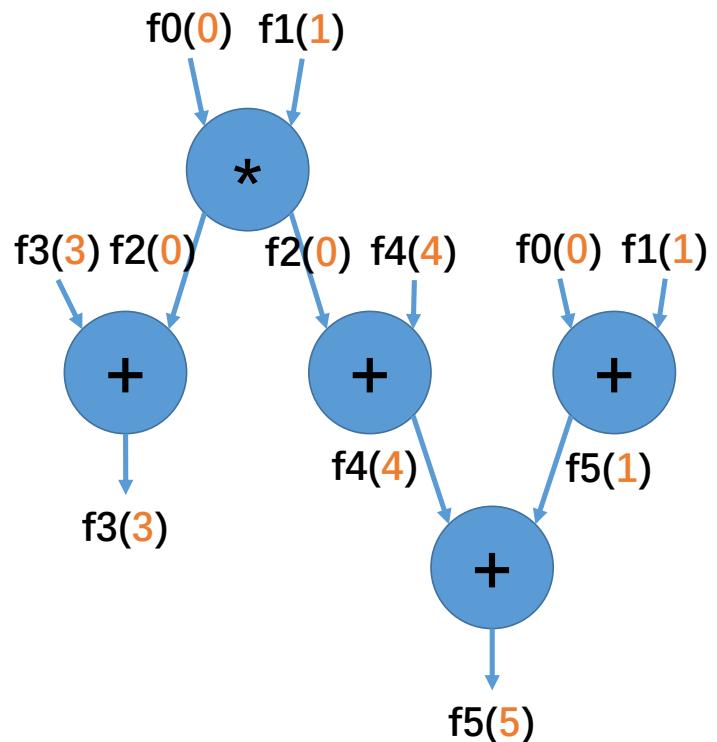
CS-GY 6133

Bo Yao, by677
Tianyu Gu, tg1553**Q1. Out-of-Order Execution Using Tomasulo's Algorithm****(a) Data-flow graph**

In our graph, $f_a(n)$ means that register a contains value n . After the code executes, the result should be:

$$R[f0]=0, R[f1]=1, R[f2]=0, R[f3]=3, R[f4]=4, R[f5]=5.$$

- T0:** muld $f0, f1, f2$
- T1:** addd $f0, f1, f5$
- T2:** addd $f2, f3, f3$
- T3:** addd $f2, f4, f4$
- T4:** addd $f4, f5, f5$

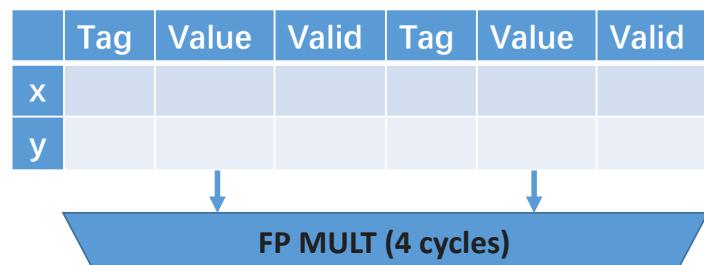


(b) Simulate cycle-by-cycle

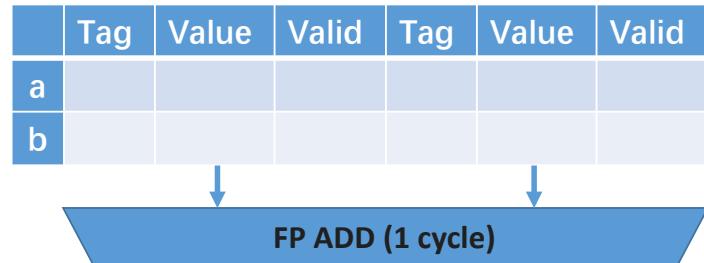
In the table below, '**wE**' means waiting to execute (RAW dependency, waiting in reservation stations); '**wD**' means waiting to decode/dispatch (reservation stations is full, instruction stalling).

	Tag	Value	Valid
f0		0	1
f1		1	1
f2		2	1
f3		3	1
f4		4	1
f5		5	1

Cycle 0

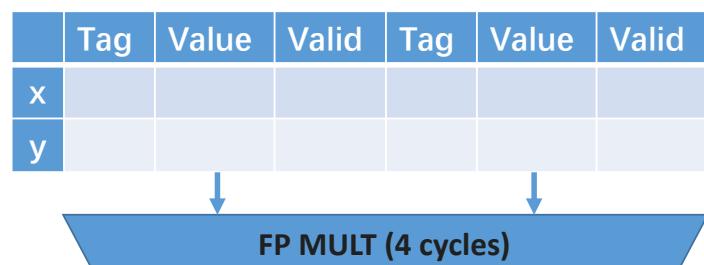


Instruction	Stage
muld f0, f1, f2	
addd f0, f1, f5	
addd f2, f3, f3	
addd f2, f4, f4	
addd f4, f5, f5	

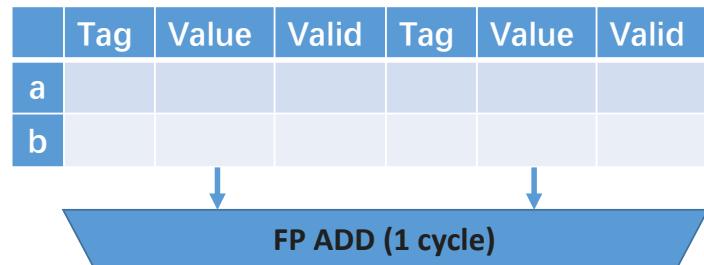


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		2	1
f3		3	1
f4		4	1
f5		5	1

Cycle 1

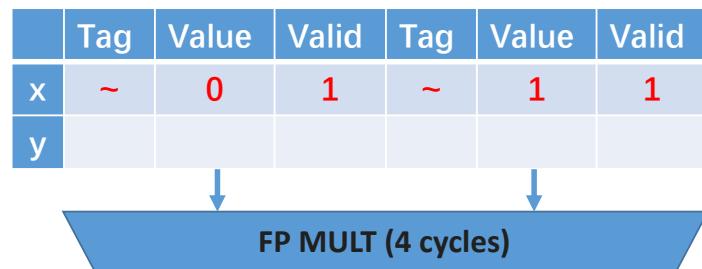


Instruction	Stage
muld f0, f1, f2	F
addd f0, f1, f5	
addd f2, f3, f3	
addd f2, f4, f4	
addd f4, f5, f5	

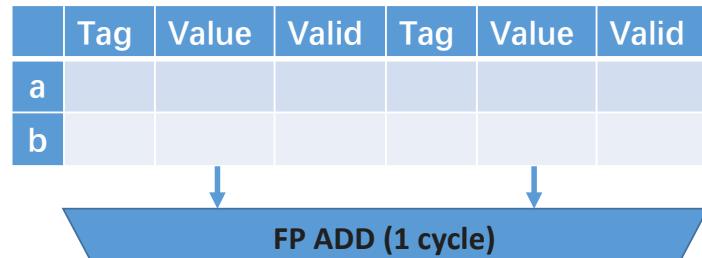


	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3		3	1
f4		4	1
f5		5	1

Cycle 2

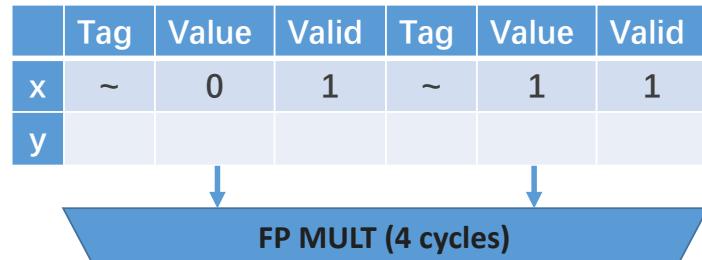


Instruction	Stage
muld f0, f1, f2	D
adddd f0, f1, f5	F
adddd f2, f3, f3	
adddd f2, f4, f4	
adddd f4, f5, f5	

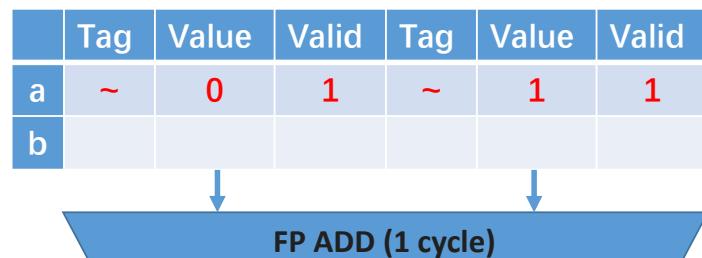


	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3		3	1
f4		4	1
f5	a	5	0

Cycle 3

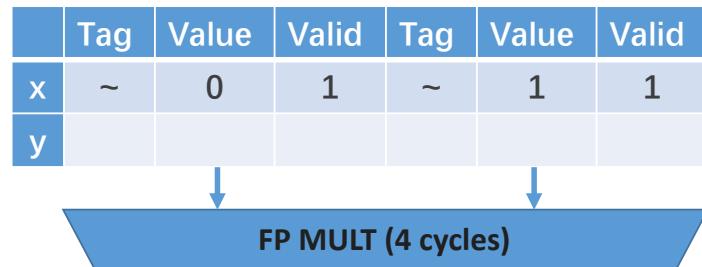


Instruction	Stage
muld f0, f1, f2	E1
adddd f0, f1, f5	D
adddd f2, f3, f3	F
adddd f2, f4, f4	
adddd f4, f5, f5	

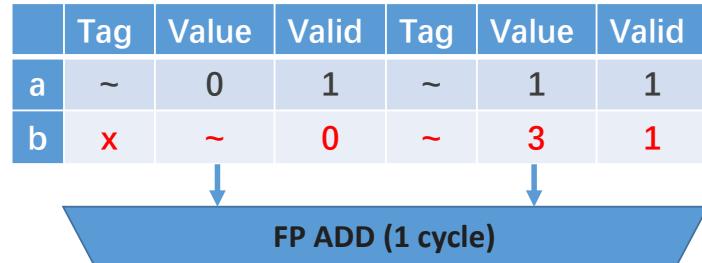


	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4		4	1
f5	a	5	0

Cycle 4

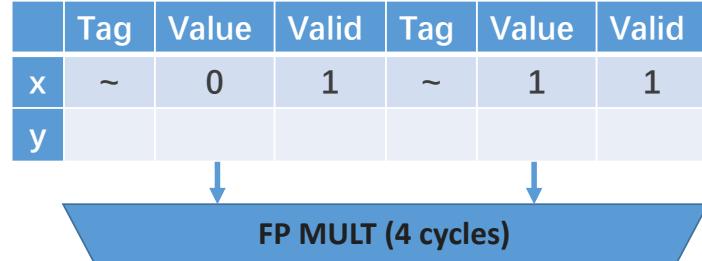


Instruction	Stage
muld f0, f1, f2	E2
adddd f0, f1, f5	E1
adddd f2, f3, f3	D
adddd f2, f4, f4	F
adddd f4, f5, f5	

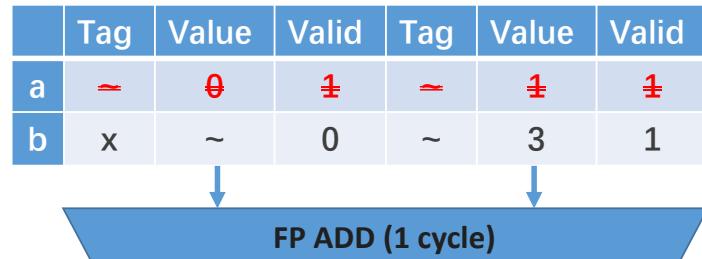


	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4		4	1
f5		1	1

Cycle 5

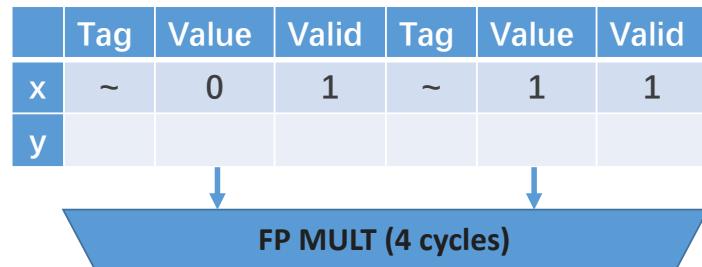


Instruction	Stage
muld f0, f1, f2	E3
adddd f0, f1, f5	WB
adddd f2, f3, f3	wE
adddd f2, f4, f4	wD
adddd f4, f5, f5	

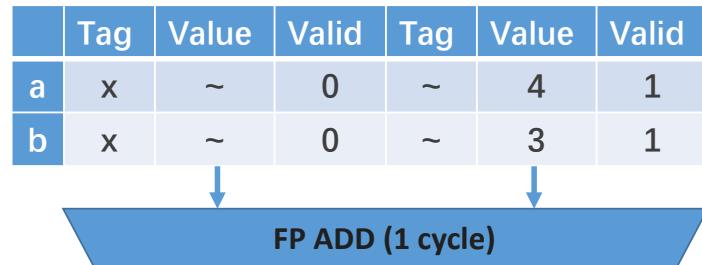


	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4	a	4	0
f5		1	1

Cycle 6

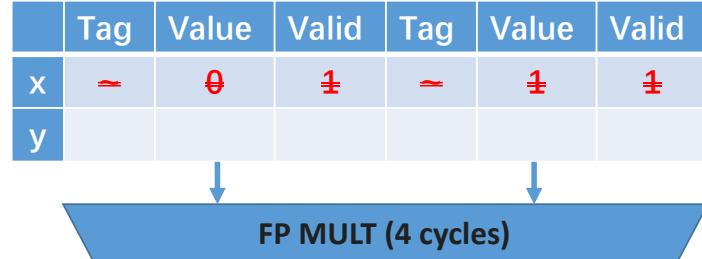


Instruction	Stage
muld f0, f1, f2	E4
addd f0, f1, f5	~
addd f2, f3, f3	wE
addd f2, f4, f4	D
addd f4, f5, f5	F

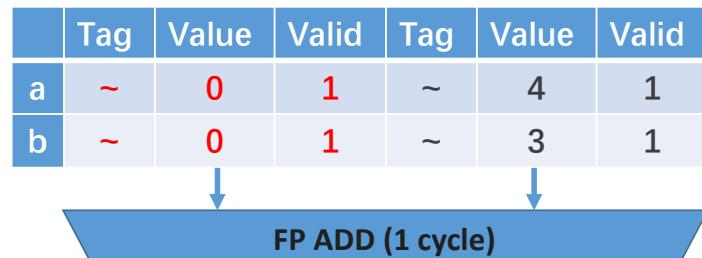


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3	b	3	0
f4	a	4	0
f5		1	1

Cycle 7

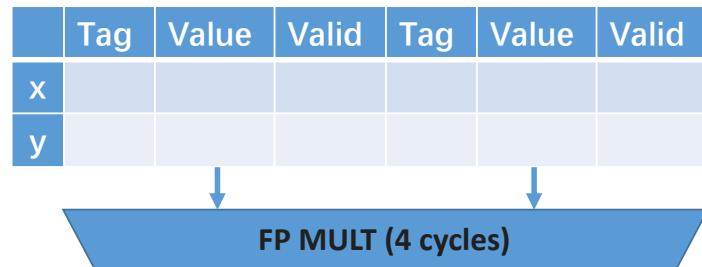


Instruction	Stage
muld f0, f1, f2	WB
addd f0, f1, f5	~
addd f2, f3, f3	wE
addd f2, f4, f4	wE
addd f4, f5, f5	wD

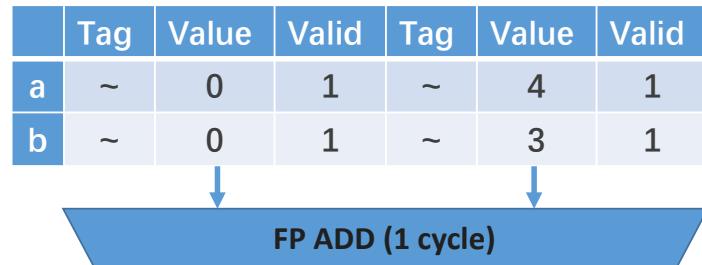


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3	b	3	0
f4	a	4	0
f5		1	1

Cycle 8

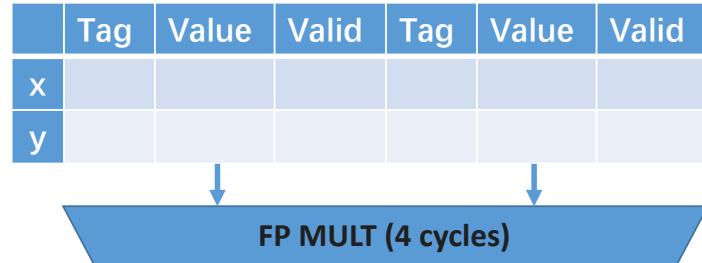


Instruction	Stage
muld f0, f1, f2	~
addd f0, f1, f5	~
addd f2, f3, f3	E1
addd f2, f4, f4	wE
addd f4, f5, f5	wD

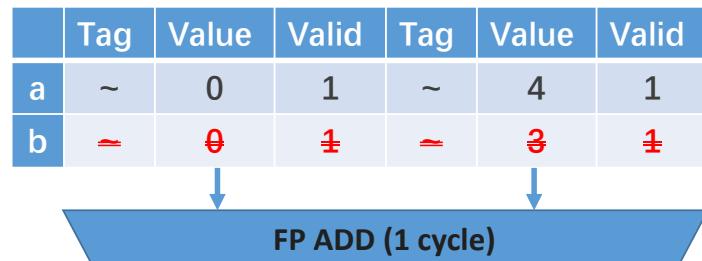


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4	a	4	0
f5		1	1

Cycle 9

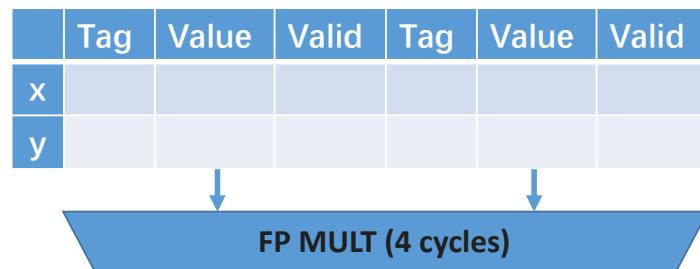


Instruction	Stage
muld f0, f1, f2	~
addd f0, f1, f5	~
addd f2, f3, f3	WB
addd f2, f4, f4	E1
addd f4, f5, f5	wD

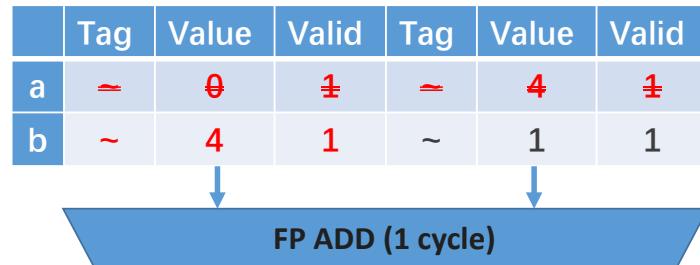


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5	b	1	0

Cycle 10

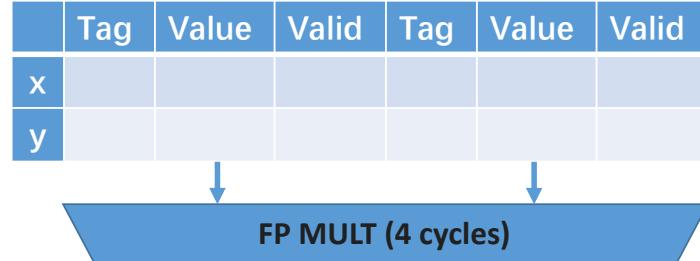


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	~
adddd f2, f4, f4	WB
adddd f4, f5, f5	D

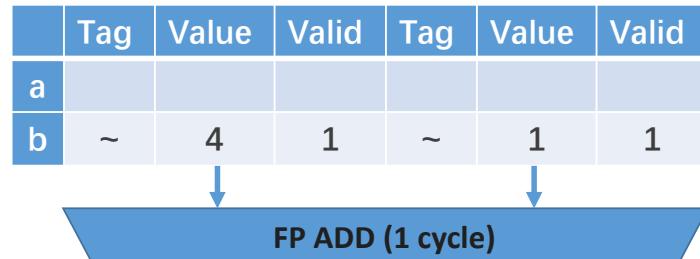


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5	b	1	0

Cycle 11

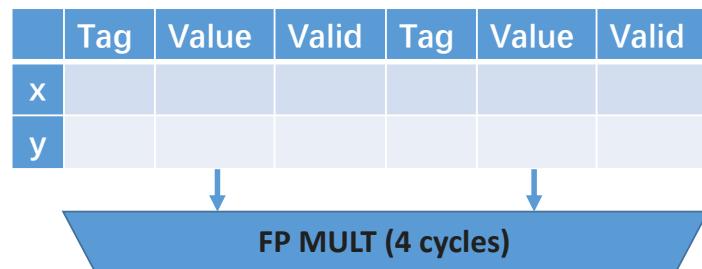


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	~
adddd f2, f4, f4	~
adddd f4, f5, f5	E1

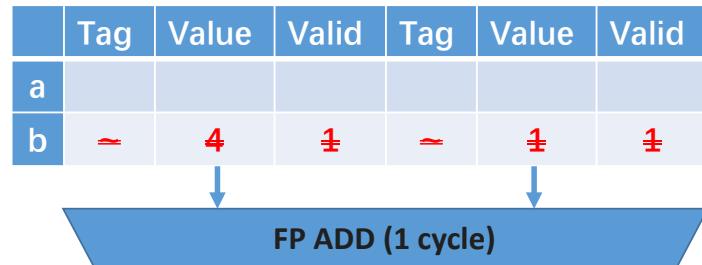


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5		5	1

Cycle 12

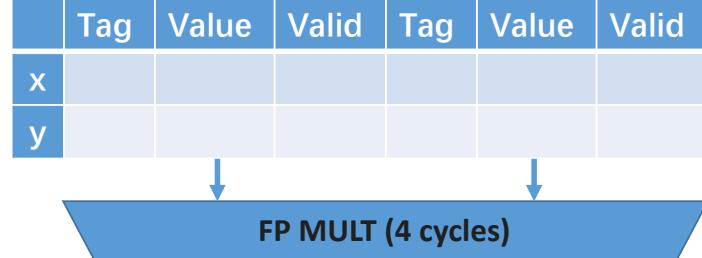


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	~
adddd f2, f4, f4	~
adddd f4, f5, f5	WB

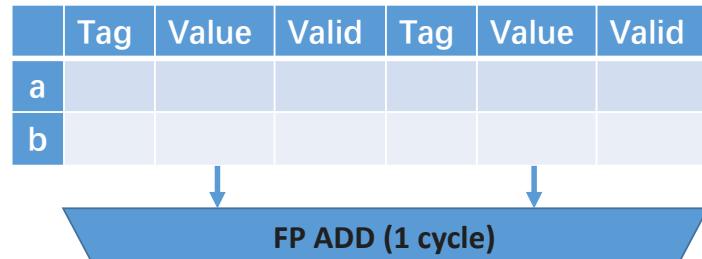


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5		5	1

Cycle 13



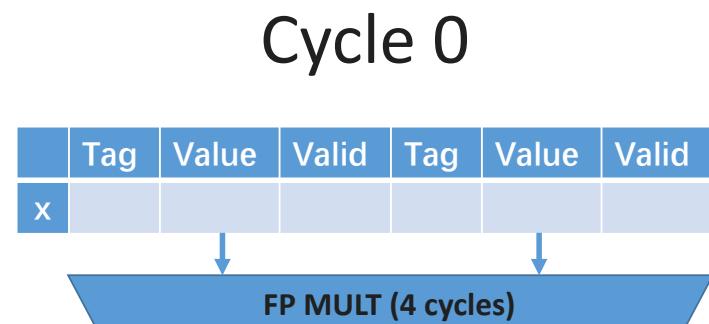
Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	~
adddd f2, f4, f4	~
adddd f4, f5, f5	~



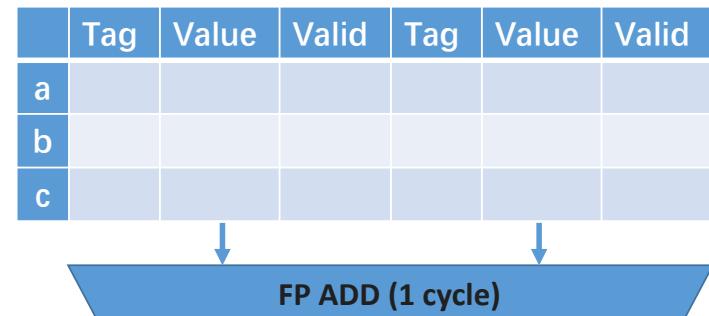
(c) Simulate cycle-by-cycle without stalling

At (b) - cycle 7 we found that FP ADD reservation station was full. The instruction had to wait until a free station was released. So we have to add one more station to FP ADD. We can also observe that FP MULT only need one reservation station at least.

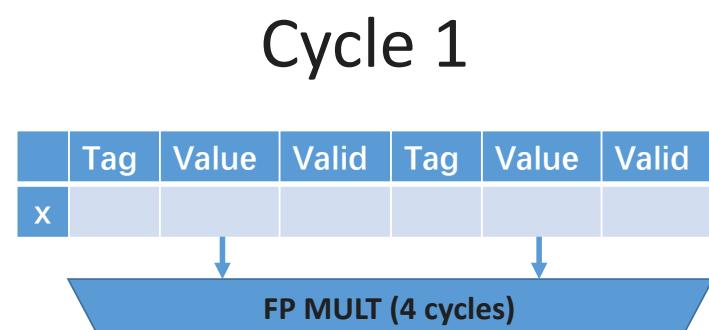
	Tag	Value	Valid
f0		0	1
f1		1	1
f2		2	1
f3		3	1
f4		4	1
f5		5	1



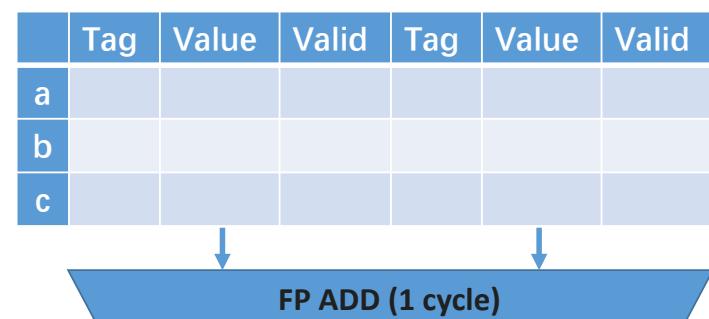
Instruction	Stage
muld f0, f1, f2	
addd f0, f1, f5	
addd f2, f3, f3	
addd f2, f4, f4	
addd f4, f5, f5	



	Tag	Value	Valid
f0		0	1
f1		1	1
f2		2	1
f3		3	1
f4		4	1
f5		5	1



Instruction	Stage
muld f0, f1, f2	F
addd f0, f1, f5	
addd f2, f3, f3	
addd f2, f4, f4	
addd f4, f5, f5	



	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3		3	1
f4		4	1
f5		5	1

Cycle 2

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	D
addd f0, f1, f5	F
addd f2, f3, f3	
addd f2, f4, f4	
addd f4, f5, f5	

	Tag	Value	Valid	Tag	Value	Valid
a						
b						
c						

FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3		3	1
f4		4	1
f5	a	5	0

Cycle 3

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	E1
addd f0, f1, f5	D
addd f2, f3, f3	F
addd f2, f4, f4	
addd f4, f5, f5	

	Tag	Value	Valid	Tag	Value	Valid
a	~	0	1	~	1	1
b						
c						

FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4		4	1
f5	a	5	0

Cycle 4

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	E2
adddd f0, f1, f5	E1
adddd f2, f3, f3	D
adddd f2, f4, f4	F
adddd f4, f5, f5	

	Tag	Value	Valid	Tag	Value	Valid
a	~	0	1	~	1	1
b	x	~	0	~	3	1
c						

FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4	c	4	0
f5		1	1

Cycle 5

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	E3
adddd f0, f1, f5	WB
adddd f2, f3, f3	wE
adddd f2, f4, f4	D
adddd f4, f5, f5	F

	Tag	Value	Valid	Tag	Value	Valid
a	~	0	1	~	1	1
b	x	~	0	~	3	1
c	x	~	0	~	4	1

FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4	c	4	0
f5	a	1	0

Cycle 6

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	E4
addd f0, f1, f5	~
addd f2, f3, f3	wE
addd f2, f4, f4	wE
addd f4, f5, f5	D

	Tag	Value	Valid	Tag	Value	Valid
a	c	~	0	~	1	1
b	x	~	0	~	3	1
c	x	~	0	~	4	1

FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3	b	3	0
f4	c	4	0
f5	a	1	0

Cycle 7

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1

FP MULT (4 cycles)

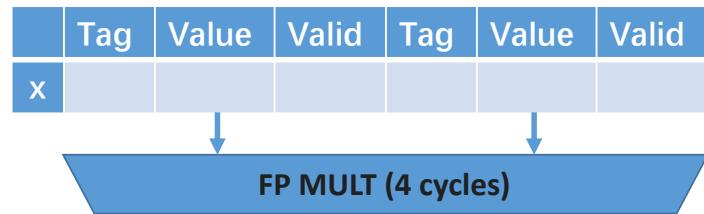
Instruction	Stage
muld f0, f1, f2	WB
addd f0, f1, f5	~
addd f2, f3, f3	wE
addd f2, f4, f4	wE
addd f4, f5, f5	wE

	Tag	Value	Valid	Tag	Value	Valid
a	c	~	0	~	1	1
b	~	0	1	~	3	1
c	~	0	1	~	4	1

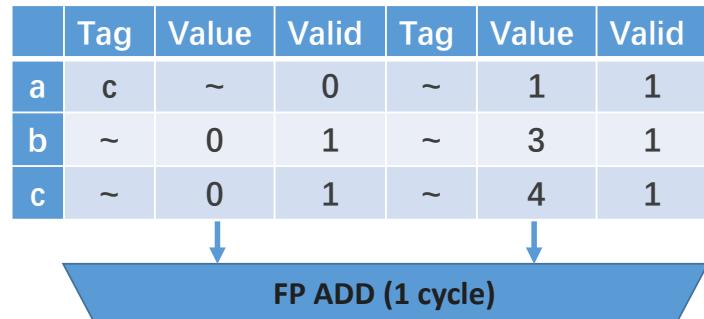
FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3	b	3	0
f4	c	4	0
f5	a	1	0

Cycle 8

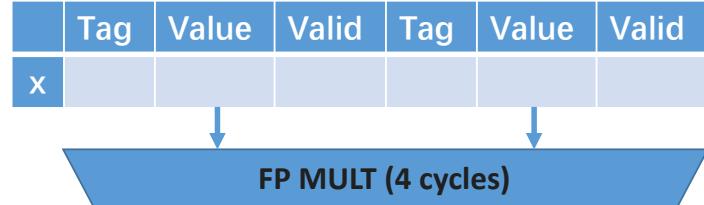


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	E1
adddd f2, f4, f4	wE
adddd f4, f5, f5	wE

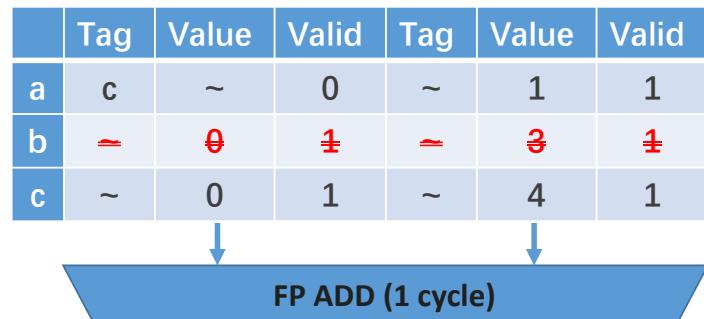


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3	3	1	1
f4	c	4	0
f5	a	1	0

Cycle 9

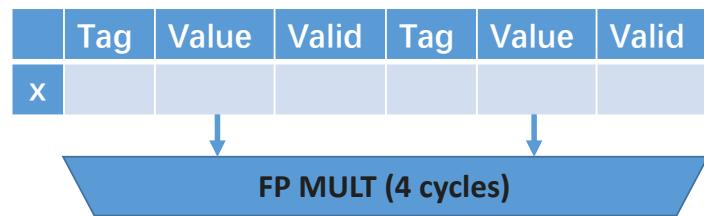


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	WB
adddd f2, f4, f4	E1
adddd f4, f5, f5	wE

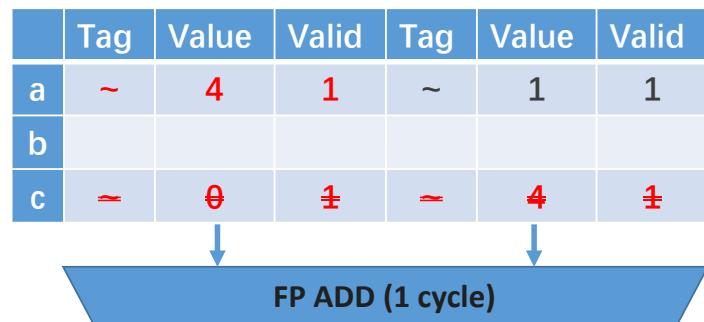


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5	a	1	0

Cycle 10

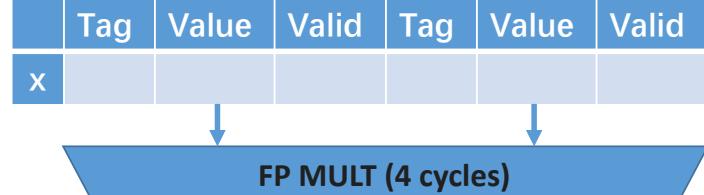


Instruction	Stage
muld f0, f1, f2	~
addd f0, f1, f5	~
addd f2, f3, f3	~
addd f2, f4, f4	WB
addd f4, f5, f5	wE

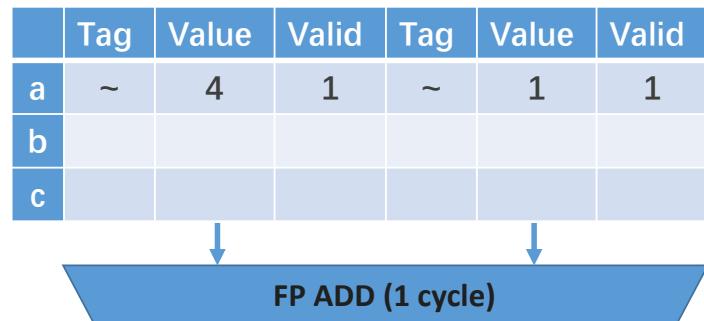


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5	a	1	0

Cycle 11

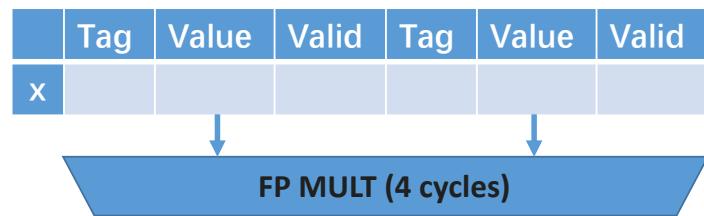


Instruction	Stage
muld f0, f1, f2	~
addd f0, f1, f5	~
addd f2, f3, f3	~
addd f2, f4, f4	~
addd f4, f5, f5	E1

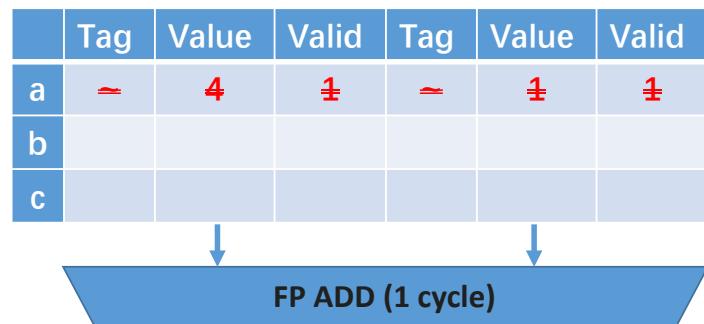


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5		5	1

Cycle 12

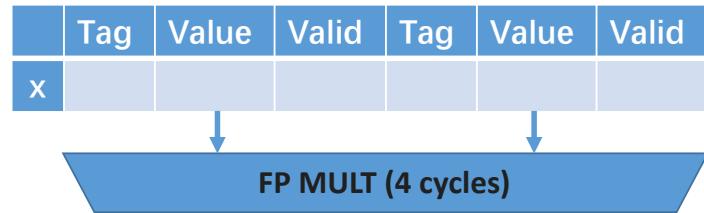


Instruction	Stage
muld f0, f1, f2	~
addd f0, f1, f5	~
addd f2, f3, f3	~
addd f2, f4, f4	~
addd f4, f5, f5	WB

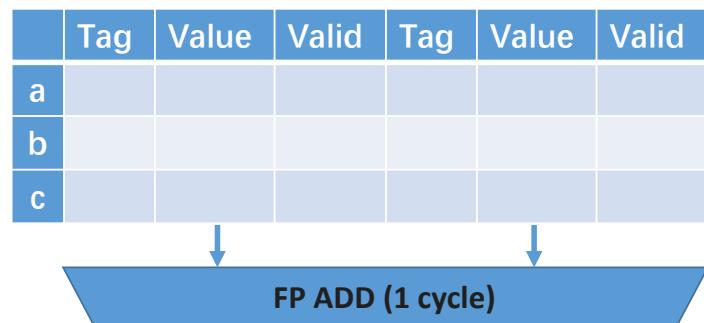


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5		5	1

Cycle 13



Instruction	Stage
muld f0, f1, f2	~
addd f0, f1, f5	~
addd f2, f3, f3	~
addd f2, f4, f4	~
addd f4, f5, f5	~

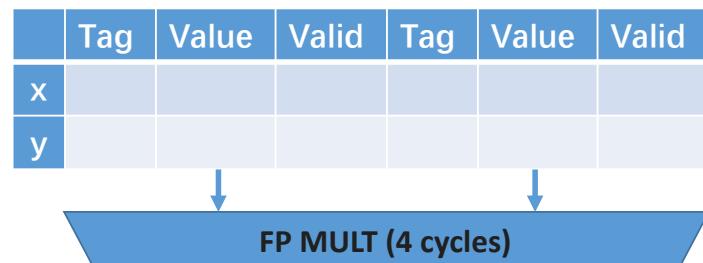


(d) Simulate cycle-by-cycle with parallel FP adders

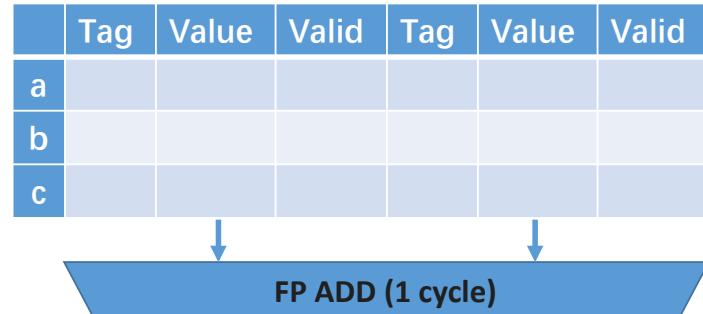
After simulation, we found that parallel process was needed at cycle 8. Two instructions could be dispatched at the same time. Thus, M = 2.

	Tag	Value	Valid
f0		0	1
f1		1	1
f2		2	1
f3		3	1
f4		4	1
f5		5	1

Cycle 0

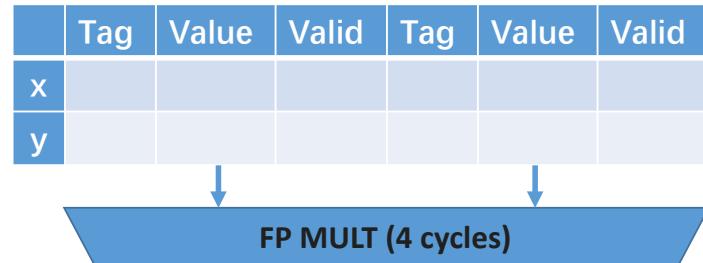


Instruction	Stage
muld f0, f1, f2	
adddd f0, f1, f5	
adddd f2, f3, f3	
adddd f2, f4, f4	
adddd f4, f5, f5	

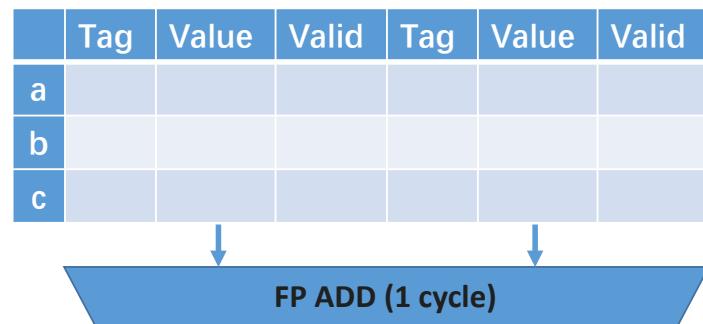


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		2	1
f3		3	1
f4		4	1
f5		5	1

Cycle 1

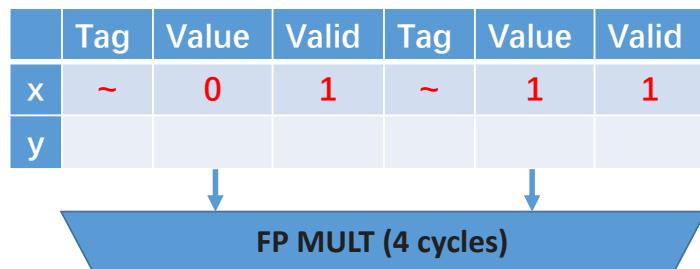


Instruction	Stage
muld f0, f1, f2	F
adddd f0, f1, f5	
adddd f2, f3, f3	
adddd f2, f4, f4	
adddd f4, f5, f5	

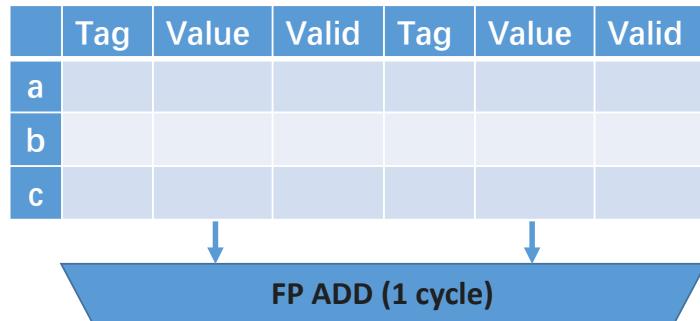


	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3		3	1
f4		4	1
f5		5	1

Cycle 2

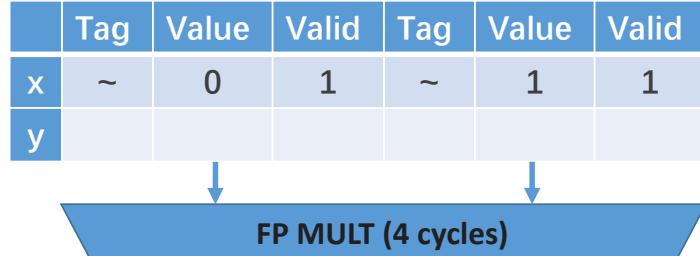


Instruction	Stage
muld f0, f1, f2	D
adddd f0, f1, f5	F
adddd f2, f3, f3	
adddd f2, f4, f4	
adddd f4, f5, f5	

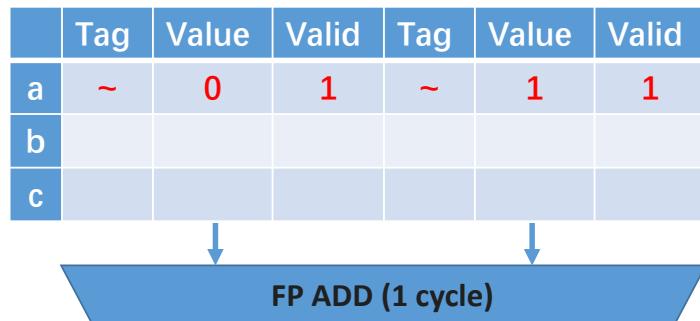


	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3		3	1
f4		4	1
f5	a	5	0

Cycle 3



Instruction	Stage
muld f0, f1, f2	E1
adddd f0, f1, f5	D
adddd f2, f3, f3	F
adddd f2, f4, f4	
adddd f4, f5, f5	



	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4		4	1
f5	a	5	0

Cycle 4

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1
y						

↓ ↓

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	E2
adddd f0, f1, f5	E1
adddd f2, f3, f3	D
adddd f2, f4, f4	F
adddd f4, f5, f5	

	Tag	Value	Valid	Tag	Value	Valid
a	~	0	1	~	1	1
b	x	~	0	~	3	1
c						

↓ ↓

FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4	c	4	0
f5		1	1

Cycle 5

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1
y						

↓ ↓

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	E3
adddd f0, f1, f5	WB
adddd f2, f3, f3	wE
adddd f2, f4, f4	D
adddd f4, f5, f5	F

	Tag	Value	Valid	Tag	Value	Valid
a	~	0	1	~	1	1
b	x	~	0	~	3	1
c	x	~	0	~	4	1

↓ ↓

FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2	x	2	0
f3	b	3	0
f4	c	4	0
f5	a	1	0

Cycle 6

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1
y						

↓ ↓

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	E4
adddd f0, f1, f5	~
adddd f2, f3, f3	wE
adddd f2, f4, f4	wE
adddd f4, f5, f5	D

	Tag	Value	Valid	Tag	Value	Valid
a	c	~	0	~	1	1
b	x	~	0	~	3	1
c	x	~	0	~	4	1

↓ ↓

FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3	b	3	0
f4	c	4	0
f5	a	1	0

Cycle 7

	Tag	Value	Valid	Tag	Value	Valid
x	~	0	1	~	1	1
y						

↓ ↓

FP MULT (4 cycles)

Instruction	Stage
muld f0, f1, f2	WB
adddd f0, f1, f5	~
adddd f2, f3, f3	wE
adddd f2, f4, f4	wE
adddd f4, f5, f5	wE

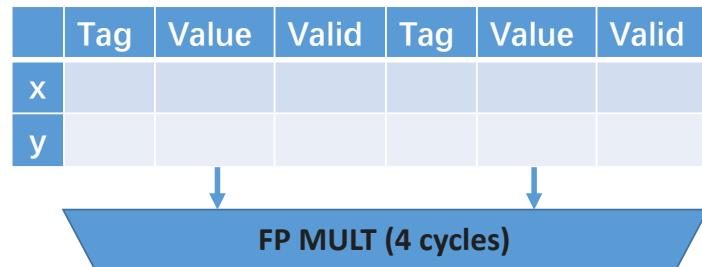
	Tag	Value	Valid	Tag	Value	Valid
a	c	~	0	~	1	1
b	~	0	1	~	3	1
c	~	0	1	~	4	1

↓ ↓

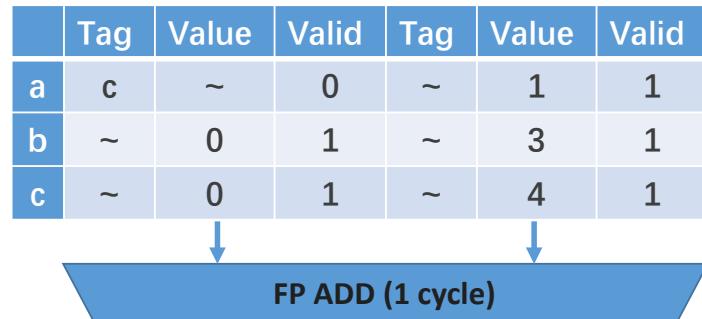
FP ADD (1 cycle)

	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3	b	3	0
f4	c	4	0
f5	a	1	0

Cycle 8

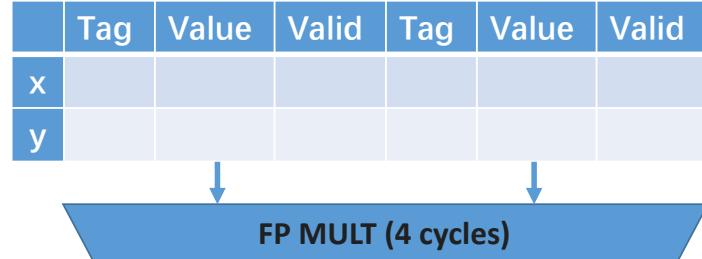


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	E1
adddd f2, f4, f4	E1
adddd f4, f5, f5	wE

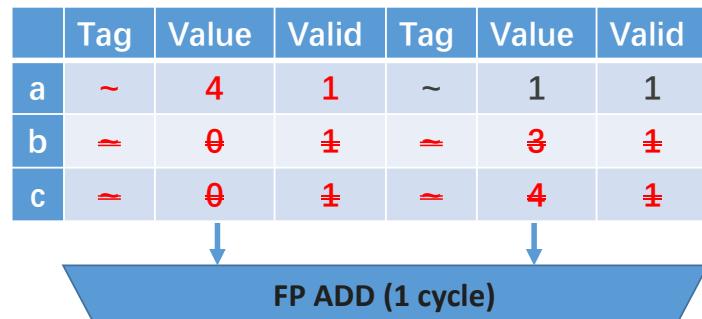


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3	3	1	1
f4	4	1	1
f5	a	1	0

Cycle 9

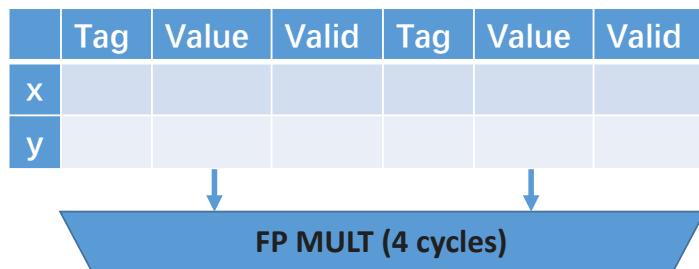


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	WB
adddd f2, f4, f4	WB
adddd f4, f5, f5	wE

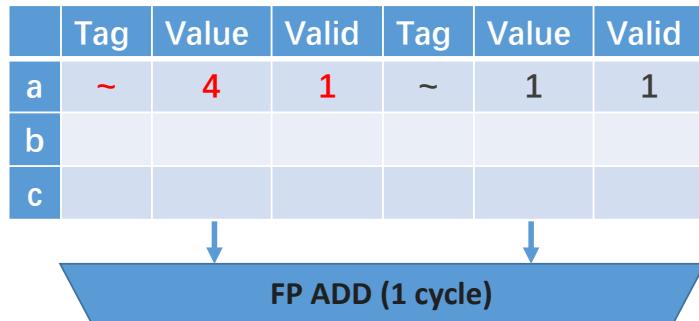


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5	a	1	0

Cycle 10

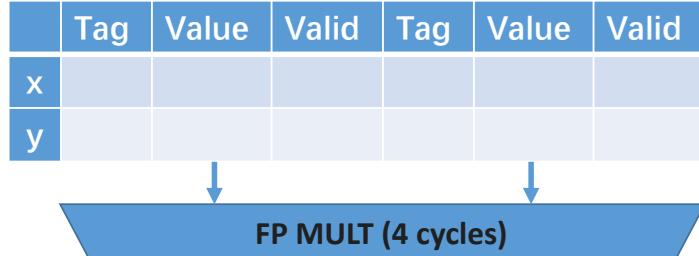


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	~
adddd f2, f4, f4	~
adddd f4, f5, f5	E1

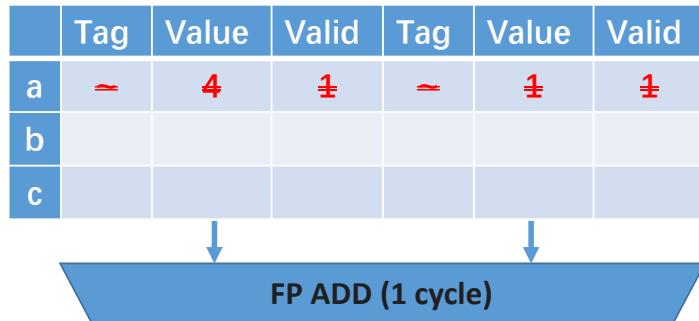


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5		5	1

Cycle 11

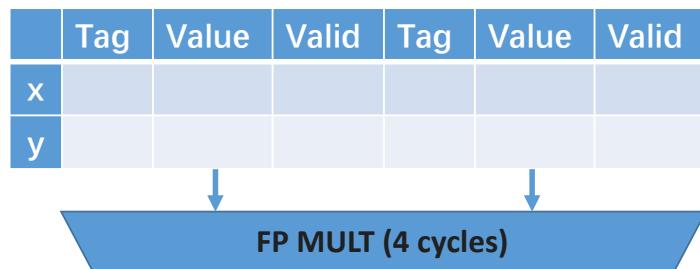


Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	~
adddd f2, f4, f4	~
adddd f4, f5, f5	WB

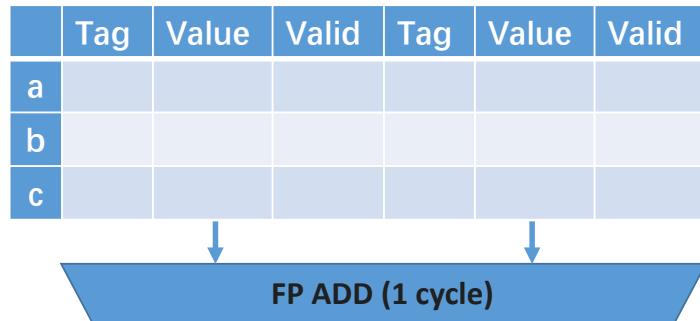


	Tag	Value	Valid
f0		0	1
f1		1	1
f2		0	1
f3		3	1
f4		4	1
f5		5	1

Cycle 12



Instruction	Stage
muld f0, f1, f2	~
adddd f0, f1, f5	~
adddd f2, f3, f3	~
adddd f2, f4, f4	~
adddd f4, f5, f5	~



Q2. Out-of-Order Execution Using Tomasulo's Algorithm + Re-order Buffer

(a) Simulate the execution

Cycle 0

LOOP: subi r1, r1, 1 Fetch
 muld f0, f1, f1
 addd f0, f2, f2
 bne r1, r0, LOOP
 addd f1, f2, f3

	Tag	Value	Valid
f0	0	1	
f1	1	1	
f2	2	1	
f3	3	1	

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	-	0	-	-	0	-
-	-	-	0	-	-	0	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FP MULT (4 cycles)

	Tag	Value	Valid
r0	0	1	
r1	2	1	

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	-	0	-	-	0	-
-	-	-	0	-	-	0	-

	Inst	Reg	Value	Valid
A	-	-	-	0
B	-	-	-	0
C	-	-	-	0
D	-	-	-	0
E	-	-	-	0
...				

ROB

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	-	0	-	-	0	-
-	-	-	0	-	-	0	-

INT ALU (1 cycle)



INT ALU (1 cycle)

Cycle 1

LOOP: subi r1, r1, 1 **Dispatch**
 muld f0, f1, f1 **Fetch**
 addd f0, f2, f2
 bne r1, r0, LOOP
 addd f1, f2, f3

	Tag	Value	Valid
f0		0	1
f1		1	1
f2		2	1
f3		3	1

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	-	0	-	-	0	-
-	-	-	0	-	-	0	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FP MULT (4 cycles)

	Tag	Value	Valid
r0		0	1
r1	A	2	0

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	-	0	-	-	0	-
-	-	-	0	-	-	0	-

	Inst	Reg	Value	Valid
A	subi	r1	-	0
B	-	-	-	0
C	-	-	-	0
D	-	-	-	0
E	-	-	-	0

...

ROB

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	2	1	-	-	0	A
-	-	-	0	-	-	0	-



INT ALU (1 cycle)

Cycle 2

LOOP: subi r1, r1, 1 Issue (E1)
 muld f0, f1, f1 Dispatch
 addd f0, f2, f2 Fetch
 bne r1, r0, LOOP
 addd f1, f2, f3

	Tag	Value	Valid
f0		0	1
f1	B	1	0
f2		2	1
f3		3	1

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	0	1	-	1	1	B
	-	-	0	-	-	0	-

	Tag	Value	Valid
r0		0	1
r1	A	2	0

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	-	0	-	-	0	-
	-	-	0	-	-	0	-

	Inst	Reg	Value	Valid
A	subi	r1	-	0
B	muld	f1	-	0
C	-	-	-	0
D	-	-	-	0
E	-	-	-	0
	...			

ROB

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	2	1	-	-	0	A
	-	-	0	-	-	0	-

INT ALU (1 cycle)



FP MULT (4 cycles)

FP ADD (1 cycle)



INT ALU (1 cycle)



FP MULT (4 cycles)



FP ADD (1 cycle)



INT ALU (1 cycle)



FP MULT (4 cycles)



FP ADD (1 cycle)



INT ALU (1 cycle)



FP MULT (4 cycles)



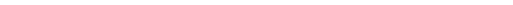
FP ADD (1 cycle)



INT ALU (1 cycle)



FP MULT (4 cycles)



FP ADD (1 cycle)

INT ALU (1 cycle)

FP MULT (4 cycles)

FP ADD (1 cycle)

INT ALU (1 cycle)

FP MULT (4 cycles)

FP ADD (1 cycle)

INT ALU (1 cycle)

FP MULT (4 cycles)

FP ADD (1 cycle)

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FP MULT (4 cycles)

FP ADD (1 cycle)

INT ALU (1 cycle)

FP MULT (4 cycles)

FP ADD (1 cycle)

INT ALU (1 cycle)

FP MULT (4 cycles)

FP ADD (1 cycle)

INT ALU (1 cycle)

Cycle 3

LOOP: subi r1, r1, 1 WB
 muld f0, f1, f1 Issue (E1)
 addd f0, f2, f2 Dispatch
 bne r1, r0, LOOP Fetch (and predict as Taken)
 addd f1, f2, f3

	Tag	Value	Valid
f0		0	1
f1	B	1	0
f2	C	2	0
f3		3	1

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	0	1	-	1	1	B
	-	-	0	-	-	0	-

⋮

FP MULT (4 cycles)

	Tag	Value	Valid
r0		0	1
r1	A	2	0

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	0	1	-	2	1	C
	-	-	0	-	-	0	-

	Inst	Reg	Value	Valid
A	subi	r1	1	1
B	muld	f1	-	0
C	addd	f2	-	0
D	-	-	-	0
E	-	-	-	0
	...			

ROB

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	-	0	-	-	0	-
	-	-	0	-	-	0	-



	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	-	0	-	-	0	-
	-	-	0	-	-	0	-



Cycle 4

LOOP: subi r1, r1, 1 Commit
 muld f0, f1, f1 Issue (E2)
 addd f0, f2, f2 Issue (E1)
 bne r1, r0, LOOP Dispatch
 LOOP: subi r1, r1, 1 Fetch

	Tag	Value	Valid
f0		0	1
f1	B	1	0
f2	C	2	0
f3		3	1

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	1	-	1	1	B
-	-	-	0	-	-	0	-
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮

FP MULT (4 cycles)

	Tag	Value	Valid
r0		0	1
r1	-	1	1

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	1	-	2	1	C
-	-	-	0	-	-	0	-

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	muld	f1	-	0	0
C	addd	f2	-	0	0
D	bne	-	-	0	T
E	-	-	-	0	
...					

ROB

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	1	1	-	0	1	D
-	-	-	0	-	-	0	-



Cycle 5

LOOP: subi r1, r1, 1
 muld f0, f1, f1 Issue (E3)
 addd f0, f2, f2 WB
 bne r1, r0, LOOP Issue (E1)
LOOP: subi r1, r1, 1 Dispatch
 muld f0, f1, f1 Fetch

	Tag	Value	Valid
f0		0	1
f1	B	1	0
f2	C	2	0
f3		3	1

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	0	1	-	1	1	B
	-	-	0	-	-	0	-



	Tag	Value	Valid
r0		0	1
r1	E	1	0

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	-	0	-	-	0	-
	-	-	0	-	-	0	-



	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	muld	f1	-	0	0
C	addir	f2	2	1	0
D	bne	-	-	0	T
E	subi	r1	-	0	0

...

ROB

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	1	1	-	0	1	D
	-	1	1	-	-	0	E



Cycle 6

LOOP: subi r1, r1, 1
 muld f0, f1, f1 Issue (E4)
 addd f0, f2, f2 Waiting
 bne r1, r0, LOOP WB(Taken)
 LOOP: subi r1, r1, 1 Issue (E1)
 muld f0, f1, f1 Dispatch
 addd f0, f2, f2 Fetch

	Tag	Value	Valid
f0		0	1
f1	F	1	0
f2	C	2	0
f3		3	1

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	0	1	-	1	1	B
	-	0	1	B	-	0	F

⋮

FP MULT (4 cycles)

	Tag	Value	Valid
r0		0	1
r1	E	1	0

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	-	0	-	-	0	-
	-	-	0	-	-	0	-

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	muld	f1	-	0	0
C	addd	f2	2	1	0
D	bne	-	-	1	T
E	subi	r1	-	0	0
F	muld	f1	-	0	0

...

ROB

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	-	0	-	-	0	-
	-	1	1	-	-	0	E

...

INT ALU (1 cycle)

Cycle 7

LOOP: subi r1, r1, 1
 muld f0, f1, f1 WB
 addd f0, f2, f2 Waiting
 bne r1, r0, LOOP Waiting
 LOOP: subi r1, r1, 1 WB
 muld f0, f1, f1 Waiting
 addd f0, f2, f2 Dispatch
 bne r1, r0, LOOP Fetch (and predict as taken)

	Tag	Value	Valid
f0		0	1
f1	F	1	0
f2	G	2	0
f3		3	1

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	0	1	-	0	1	F
⋮						
FP MULT (4 cycles)						

	Tag	Value	Valid
r0		0	1
r1	E	1	0

Tag	Value	Valid	Tag	Value	Valid	ROB
-	0	1	-	2	1	G
-	-	0	-	-	0	-
⋮						
FP ADD (1 cycle)						

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	muld	f1	0	1	0
C	addd	f2	2	1	0
D	bne	-	-	1	T
E	subi	r1	0	1	0
F	muld	f1	-	0	0
G	addd	f2	-	0	0
...					
ROB					

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-
⋮						
INT ALU (1 cycle)						



Cycle 8

```

LOOP: subi r1, r1, 1
muld f0, f1, f1      Commit
addd f0, f2, f2      Waiting
bne r1, r0, LOOP    Waiting
LOOP: subi r1, r1, 1  Waiting
muld f0, f1, f1      Issue(E1)
addd f0, f2, f2      Issue(E1)
bne r1, r0, LOOP    Dispatch
LOOP: subi r1, r1, 1  Fetch

```

	Tag	Value	Valid
f0	0	1	
f1	F	0	0
f2	G	2	0
f3		3	1

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	0	1	-	0	1	F
•			•			

FP MULT (4 cycles)

	Tag	Value	Valid
r0	0	1	
r1	E	1	0

Tag	Value	Valid	Tag	Value	Valid	ROB
-	0	1	-	2	1	G
-	-	0	-	-	0	-
•			•			

FP ADD (1 cycle)

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	-	-	-	0	0
C	addd	f2	2	1	0
D	bne	-	-	1	T
E	subi	r1	0	1	0
F	muld	f1	-	0	0
G	addd	f2	-	0	0
H	bne	-	-	0	T
...					

ROB

Tag	Value	Valid	Tag	Value	Valid	ROB
-	0	1	-	0	1	H
-	-	0	-	-	0	-
•			•			

INT ALU (1 cycle)

Cycle 9

```

LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2      Commit
bne r1, r0, LOOP    Waiting
LOOP: subi r1, r1, 1    Waiting
muld f0, f1, f1      Issue(E2)
addd f0, f2, f2      WB
bne r1, r0, LOOP    Issue(E1)
LOOP: subi r1, r1, 1    Dispatch
muld f0, f1, f1      Fetch
  
```

	Tag	Value	Valid
f0		0	1
f1	F	0	0
f2	G	2	0
f3		3	1

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	-	0	-	-	0	-
	-	0	1	-	0	1	F



	Tag	Value	Valid
r0		0	1
r1	I	1	0

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	-	0	-	-	0	-
	-	-	0	-	-	0	-



	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	-	-	-	0	0
C	-	-	-	0	0
D	bne	-	-	1	T
E	subi	r1	0	1	0
F	muld	f1	-	0	0
G	addd	f2	2	1	0
H	bne	-	-	0	T
I	subi	r1	-	0	0

	Tag	Value	Valid	Tag	Value	Valid	ROB
	-	0	1	-	0	1	H
	-	0	1	-	-	0	I



...

ROB

Cycle 10

```

LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP      Commit
LOOP: subi r1, r1, 1  Waiting
muld f0, f1, f1      Issue(E3)
addd f0, f2, f2      Waiting
bne r1, r0, LOOP      WB (not taken!)
LOOP: subi r1, r1, 1  Issue(E1)
muld f0, f1, f1      Dispatch
addd f0, f2, f2      Fetch

```

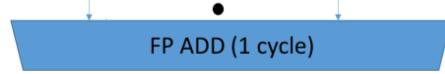
	Tag	Value	Valid
f0		0	1
f1	J	0	0
f2	G	2	0
f3		3	1

Tag	Value	Valid	Tag	Value	Valid	ROB
-	0	1	F	-	0	J
-	0	1	-	0	1	F



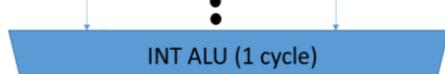
	Tag	Value	Valid
r0		0	1
r1	I	1	0

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-



Inst	Reg	Value	Valid	T/NT
A	-	-	0	0
B	-	-	0	0
C	-	-	0	0
D	-	-	0	0
E	subi	r1	0	1
F	muld	f1	-	0
G	addd	f2	2	1
H	bne	-	1	NT
I	subi	r1	-	0
J	muld	f1	-	0

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	0	1	-	-	0	I



...

ROB

Cycle 11 (Frozen for recovery)

```

LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP

LOOP: subi r1, r1, 1    Waiting
muld f0, f1, f1        Issue(E3)
addd f0, f2, f2        Waiting
bne r1, r0, LOOP      WB (not taken!)

LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2

```

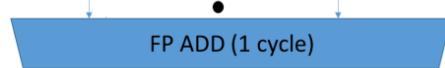
	Tag	Value	Valid
f0		0	1
f1	F	0	0
f2	G	2	0
f3		3	1

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	0	1	-	0	1	F



	Tag	Value	Valid
r0		0	1
r1	E	1	0

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-



Inst	Reg	Value	Valid	T/NT
A	-	-	0	0
B	-	-	0	0
C	-	-	0	0
D	-	-	0	0
E	subi	r1	0	1
F	muld	f1	-	0
G	addd	f2	2	1
H	bne	-	-	1
I	-	-	0	0
J	-	-	0	0

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-



...

ROB

Cycle 12

```

LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP
LOOP: subi r1, r1, 1 Commit
muld f0, f1, f1 Issue(E4)
addd f0, f2, f2 Waiting
bne r1, r0, LOOP Waiting
addd f1, f2, f3 Fetch

```

	Tag	Value	Valid
f0	0	1	
f1	F	0	0
f2	G	2	0
f3		3	1

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	0	1	-	0	1	F
•			•			

FP MULT (4 cycles)

	Tag	Value	Valid
r0	0	1	
r1	0	1	

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-



Inst	Reg	Value	Valid	T/NT
A	-	-	0	0
B	-	-	0	0
C	-	-	0	0
D	-	-	0	0
E	-	-	0	0
F	muld	f1	0	0
G	addd	f2	2	1
H	bne	-	1	NT
I	-	-	0	0
J	-	-	0	0

...

ROB

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-



Cycle 13

```

LOOP: sub r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP
LOOP: sub r1, r1, 1
muld f0, f1, f1      WB
addd f0, f2, f2      Waiting
bne r1, r0, LOOP    Waiting
addd f1, f2, f3      Dispatch

```

	Tag	Value	Valid
f0	0	1	
f1	F	0	0
f2	G	2	0
f3	I	3	0

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-

•

FP MULT (4 cycles)

	Tag	Value	Valid
r0	0	1	
r1	0	1	

Tag	Value	Valid	Tag	Value	Valid	ROB
-	0	1	-	2	1	I
-	-	0	-	-	0	-

•

FP ADD (1 cycle)

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	-	-	-	0	0
C	-	-	-	0	0
D	-	-	-	0	0
E	-	-	-	0	0
F	muld	f1	0	1	0
G	addd	f2	2	1	0
H	bne	-	-	1	NT
I	addd	f3	-	0	0
J	-	-	-	0	0

...

ROB

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-

•

INT ALU (1 cycle)

Cycle 14

```

LOOP: sub r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP
LOOP: sub r1, r1, 1
muld f0, f1, f1      Commit
addd f0, f2, f2      Waiting
bne r1, r0, LOOP    Waiting
addd f1, f2, f3      Issue(E1)

```

	Tag	Value	Valid
f0	0	1	
f1	0	1	
f2	G	2	0
f3	I	3	0

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-
•	•	•	•	•	•	•

FP MULT (4 cycles)

	Tag	Value	Valid
r0	0	1	
r1	0	1	

Tag	Value	Valid	Tag	Value	Valid	ROB
-	0	1	-	2	1	I
-	-	0	-	-	0	-
•	•	•	•	•	•	•

FP ADD (1 cycle)

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	-	-	-	0	0
C	-	-	-	0	0
D	-	-	-	0	0
E	-	-	-	0	0
F	-	-	-	0	0
G	addd	f2	2	1	0
H	bne	-	-	1	NT
I	addd	f3	-	0	0
J	-	-	-	0	0

...

ROB

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-
•	•	•	•	•	•	•

INT ALU (1 cycle)

Cycle 15

```

LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP
LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2      Commit
bne r1, r0, LOOP    Waiting
addd f1, f2, f3      WB

```

	Tag	Value	Valid
f0	0	1	
f1	0	1	
f2	2	1	
f3	1	3	0

	Tag	Value	Valid
r0	0	1	
r1	0	1	

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	-	-	-	0	0
C	-	-	-	0	0
D	-	-	-	0	0
E	-	-	-	0	0
F	-	-	-	0	0
G	-	-	-	0	0
H	bne	-	-	1	NT
I	addd	f3	2	1	0
J	-	-	-	0	0

...

ROB

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	-	0	-	-	0	-
-	-	-	0	-	-	0	-

FP MULT (4 cycles)

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	-	0	-	-	0	-
-	-	-	0	-	-	0	-

FP ADD (1 cycle)

	Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	-	0	-	-	0	-
-	-	-	0	-	-	0	-

INT ALU (1 cycle)

Cycle 16

```

LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP
LOOP: subi r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP      Commit
addd f1, f2, f3      Waiting

```

	Tag	Value	Valid
f0	0	1	
f1	0	1	
f2	2	1	
f3	1	3	0

	Tag	Value	Valid
r0	0	1	
r1	0	1	

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	-	-	-	0	0
C	-	-	-	0	0
D	-	-	-	0	0
E	-	-	-	0	0
F	-	-	-	0	0
G	-	-	-	0	0
H	-	-	-	0	0
I	addd	f3	2	1	0
J	-	-	-	0	0

...

ROB

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-

FP MULT (4 cycles)

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-

FP ADD (1 cycle)

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-

INT ALU (1 cycle)

Cycle 17

```

LOOP: sub r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP
LOOP: sub r1, r1, 1
muld f0, f1, f1
addd f0, f2, f2
bne r1, r0, LOOP
addd f1, f2, f3      Commit

```

	Tag	Value	Valid
f0	0	1	
f1	0	1	
f2	2	1	
f3	2	0	

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-
•						

FP MULT (4 cycles)

	Tag	Value	Valid
r0	0	1	
r1	0	1	

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-
•						

FP ADD (1 cycle)

	Inst	Reg	Value	Valid	T/NT
A	-	-	-	0	0
B	-	-	-	0	0
C	-	-	-	0	0
D	-	-	-	0	0
E	-	-	-	0	0
F	-	-	-	0	0
G	-	-	-	0	0
H	-	-	-	0	0
I	-	-	-	0	0
J	-	-	-	0	0

...

ROB

Tag	Value	Valid	Tag	Value	Valid	ROB
-	-	0	-	-	0	-
-	-	0	-	-	0	-
•						

INT ALU (1 cycle)

(b) minimum size of the ROB

As we see in Q2.1, there are at most 6 instructions in ROB when executing this code, but when there are 6 instructions in Cycle 9, the C item in ROB is in the process of committing. If ROB size is 6, the new dispatch can't take place in the C item in ROB (which is in committing) at the same clock cycle, so **the minimum ROB size is 7**.

Q3. Branch Prediction

(a) last-value prediction

The first 16 loops is shown below. We wrote a simple program to generate this table and calculate the mis-prediction rate. **The mis-prediction rate for branch B1 is always 0%. B2 converges to 50%. B3 converges to 100%.**

What's more from the table we could also observe that after $i=3$, the prediction and the actual behavior became periodic with period of 4. So we could easily get that mis-prediction rate $B1 = 50\%$, $B2 = 100\%$.

i	B1	B2	B3	Pre	N/T	Mis Rate
0	N			N	T	100.00%
0		N		N	T	100.00%
0			N	N	T	100.00%
1	T			T	T	50.00%
1		T		T	N	100.00%
1			T	T	N	100.00%
2	T			T	T	33.33%
2		N		N	N	66.67%
2			N	N	T	100.00%
3	T			T	T	25.00%
3		N		N	N	50.00%
3			T	T	N	100.00%
4	T			T	T	20.00%
4		N		N	T	60.00%
4			N	N	T	100.00%
5	T			T	T	16.67%
5		T		T	N	66.67%
5			T	T	N	100.00%
6	T			T	T	14.29%
6		N		N	N	57.14%
6			N	N	T	100.00%
7	T			T	T	12.50%
7		N		N	N	50.00%
7			T	T	N	100.00%
8	T			T	T	11.11%
8		N		N	T	55.56%
8			N	N	T	100.00%
9	T			T	T	10.00%
9		T		T	N	60.00%
9			T	T	N	100.00%
10	T			T	T	9.09%
10		N		N	N	54.55%
10			N	N	T	100.00%
11	T			T	T	8.33%
11		N		N	N	50.00%
11			T	T	N	100.00%
12	T			T	T	7.69%
12		N		N	T	53.85%
12			N	N	T	100.00%
13	T			T	T	7.14%
13		T		T	N	57.14%
13			T	T	N	100.00%
14	T			T	T	6.67%
14		N		N	N	53.33%
14			N	N	T	100.00%
15	T			T	T	6.25%
15		N		N	N	50.00%
15			T	T	N	100.00%

i	B1	B2	B3	Pre	N/T	Mis Rate
0	N			N	T	100.00%
1	T			T	T	50.00%
2	T			T	T	33.33%
3	T			T	T	25.00%
4	T			T	T	20.00%
5	T			T	T	16.67%
6	T			T	T	14.29%
7	T			T	T	12.50%
8	T			T	T	11.11%
9	T			T	T	10.00%
10	T			T	T	9.09%
11	T			T	T	8.33%
12	T			T	T	7.69%
13	T			T	T	7.14%
14	T			T	T	6.67%
15	T			T	T	6.25%

i	B1	B2	B3	Pre	N/T	Mis Rate
0		N		N	T	100.00%
1		T		T	N	100.00%
2		N		N	N	66.67%
3		N		N	N	50.00%
4		N		N	T	60.00%
5		T		T	N	66.67%
6		N		N	N	57.14%
7		N		N	N	50.00%
8		N		N	T	55.56%
9		T		T	N	60.00%
10		N		N	N	54.55%
11		N		N	N	50.00%
12		N		N	T	53.85%
13		T		T	N	57.14%
14		N		N	N	53.33%
15		N		N	N	50.00%

i	B1	B2	B3	Pre	N/T	Mis Rate
0			N	N	T	100.00%
1			T	T	N	100.00%
2			N	N	T	100.00%
3			T	T	N	100.00%
4			N	N	T	100.00%
5			T	T	N	100.00%
6			N	N	T	100.00%
7			T	T	N	100.00%
8			N	N	T	100.00%
9			T	T	N	100.00%
10			N	N	T	100.00%
11			T	T	N	100.00%
12			N	N	T	100.00%
13			T	T	N	100.00%
14			N	N	T	100.00%
15			T	T	N	100.00%

(b) separate 2-bit saturating counter prediction

The first 16 loops is shown below. We wrote a simple program to generate this table and calculate the mis-prediction rate. **The mis-prediction rate for branch B1 is always 0%.**

B2 converges to 25%. B3 converges to 50%.

What's more from the table we could also observe that after $i=3$, the prediction and the actual behavior became periodic with period of 4. So we could easy get that mis-prediction rate $B1 = 25\%$, $B2 = 50\%$.

i	B1	B2	B3	Pre	N/T	Mis Rate
0	SN			N	T	100.00%
0		SN		N	T	100.00%
0			SN	N	T	100.00%
1	WN			N	T	100.00%
1		WN		N	N	50.00%
1			WN	N	N	50.00%
2	ST			T	T	66.67%
2		SN		N	N	33.33%
2			SN	N	T	66.67%
3	ST			T	T	50.00%
3		SN		N	N	25.00%
3			WN	N	N	50.00%
4	ST			T	T	40.00%
4		SN		N	T	40.00%
4			SN	N	T	60.00%
5	ST			T	T	33.33%
5		WN		N	N	33.33%
5			WN	N	N	50.00%
6	ST			T	T	28.57%
6		SN		N	N	28.57%
6			SN	N	T	57.14%
7	ST			T	T	25.00%
7		SN		N	N	25.00%
7			WN	N	N	50.00%
8	ST			T	T	22.22%
8		SN		N	T	33.33%
8			SN	N	T	55.56%
9	ST			T	T	20.00%
9		WN		N	N	30.00%
9			WN	N	N	50.00%
10	ST			T	T	18.18%
10		SN		N	N	27.27%
10			SN	N	T	54.55%
11	ST			T	T	16.67%
11		SN		N	N	25.00%
11			WN	N	N	50.00%
12	ST			T	T	15.38%
12		SN		N	T	30.77%
12			SN	N	T	53.85%
13	ST			T	T	14.29%
13		WN		N	N	28.57%
13			WN	N	N	50.00%
14	ST			T	T	13.33%
14		SN		N	N	26.67%
14			SN	N	T	53.33%
15	ST			T	T	12.50%
15		SN		N	N	25.00%
15			WN	N	N	50.00%

i	B1	B2	B3	Pre	N/T	Mis Rate
0	SN			N	T	100.00%
1	WN			N	T	100.00%
2	ST			T	T	66.67%
3	ST			T	T	50.00%
4	ST			T	T	40.00%
5	ST			T	T	33.33%
6	ST			T	T	28.57%
7	ST			T	T	25.00%
8	ST			T	T	22.22%
9	ST			T	T	20.00%
10	ST			T	T	18.18%
11	ST			T	T	16.67%
12	ST			T	T	15.38%
13	ST			T	T	14.29%
14	ST			T	T	13.33%
15	ST			T	T	12.50%

i	B1	B2	B3	Pre	N/T	Mis Rate
0		SN		N	T	100.00%
1		WN		N	N	50.00%
2		SN		N	N	33.33%
3		SN		N	N	25.00%
4		SN		N	T	40.00%
5		WN		N	N	33.33%
6		SN		N	N	28.57%
7		SN		N	N	25.00%
8		SN		N	T	33.33%
9		WN		N	N	30.00%
10		SN		N	N	27.27%
11		SN		N	N	25.00%
12		SN		N	T	30.77%
13		WN		N	N	28.57%
14		SN		N	N	26.67%
15		SN		N	N	25.00%

i	B1	B2	B3	Pre	N/T	Mis Rate
0			SN	N	T	100.00%
1			WN	N	N	50.00%
2			SN	N	T	66.67%
3			WN	N	N	50.00%
4			SN	N	T	60.00%
5			WN	N	N	50.00%
6			SN	N	T	57.14%
7			WN	N	N	50.00%
8			SN	N	T	55.56%
9			WN	N	N	50.00%
10			SN	N	T	54.55%
11			WN	N	N	50.00%
12			SN	N	T	53.85%
13			WN	N	N	50.00%
14			SN	N	T	53.33%
15			WN	N	N	50.00%

(c) 2-level correlating prediction

The first 16 loops is shown below. We wrote a simple program to generate this table and calculate the mis-prediction rate. **The mis-prediction rate for branch B1 is always 0%.**

B2 converges to 25%. B3 converges to 25%.

What's more from the table we could also observe that after $i=7$, the prediction and the actual behavior became periodic with period of 4. So we could easy get that mis-prediction rate $B1 = B2 = 25\%$.

i	History	B1				B2				B3				Pre	N/T	Miss Rate
		N,N	N,T	T,N	T,T	N,N	N,T	T,N	T,T	N,N	N,T	T,N	T,T			
0	N,N	SN	SN	SN	SN									N	T	100.00%
0	N,T					SN	SN	SN	SN					N	T	100.00%
0	T,T									SN	SN	SN	SN	N	T	100.00%
1	T,T	WN	SN	SN	SN									N	T	100.00%
1	T,T					SN	WN	SN	SN					N	N	50.00%
1	T,N									SN	SN	SN	WN	N	N	50.00%
2	N,N	WN	SN	SN	WN									N	T	100.00%
2	N,T					SN	WN	SN	SN					N	N	33.33%
2	T,N									SN	SN	SN	WN	N	T	66.67%
3	N,T	ST	SN	SN	WN									N	T	100.00%
3	T,T					SN	SN	SN	SN					N	N	25.00%
3	T,N									SN	SN	WN	WN	N	N	50.00%
4	N,N	ST	WN	SN	WN									T	T	80.00%
4	N,T					SN	SN	SN	SN					N	T	40.00%
4	T,T									SN	SN	SN	WN	N	T	60.00%
5	T,T	ST	WN	SN	WN									N	T	83.33%
5	T,T					SN	WN	SN	SN					N	N	33.33%
5	T,N									SN	SN	SN	ST	N	N	50.00%
6	N,N	ST	WN	SN	ST									T	T	71.43%
6	N,T					SN	WN	SN	SN					N	N	28.57%
6	T,N									SN	SN	SN	ST	N	T	57.14%
7	N,T	ST	WN	SN	ST									N	T	75.00%
7	T,T					SN	SN	SN	SN					N	N	25.00%
7	T,N									SN	SN	WN	ST	N	N	50.00%
8	N,N	ST	ST	SN	ST									T	T	66.67%
8	N,T					SN	SN	SN	SN					N	T	33.33%
8	T,T									SN	SN	SN	ST	T	T	44.44%
9	T,T	ST	ST	SN	ST									T	T	60.00%
9	T,T					SN	WN	SN	SN					N	N	30.00%
9	T,N									SN	SN	SN	ST	N	N	40.00%
10	N,N	ST	ST	SN	ST									T	T	54.55%
10	N,T					SN	WN	SN	SN					N	N	27.27%
10	T,N									SN	SN	SN	ST	N	T	45.45%
11	N,T	ST	ST	SN	ST									T	T	50.00%
11	T,T					SN	SN	SN	SN					N	N	25.00%
11	T,N									SN	SN	WN	ST	N	N	41.67%
12	N,N	ST	ST	SN	ST									T	T	46.15%
12	N,T					SN	SN	SN	SN					N	T	30.77%
12	T,T									SN	SN	SN	ST	T	T	38.46%
13	T,T	ST	ST	SN	ST									T	T	42.86%
13	T,T					SN	WN	SN	SN					N	N	28.57%
13	T,N									SN	SN	SN	ST	N	N	35.71%
14	N,N	ST	ST	SN	ST									T	T	40.00%
14	N,T					SN	WN	SN	SN					N	N	26.67%
14	T,N									SN	SN	SN	ST	N	T	40.00%
15	N,T	ST	ST	SN	ST									T	T	37.50%
15	T,T					SN	SN	SN	SN					N	N	25.00%
15	T,N									SN	SN	WN	ST	N	N	37.50%

i	History	B1				B2				B3				Pre	N/T	Miss Rate
		N,N	N,T	T,N	T,T	N,N	N,T	T,N	T,T	N,N	N,T	T,N	T,T	~	~	~
0	N,N	SN	SN	SN	SN					N	T			100.00%		
1	T,T	WN	SN	SN	SN					N	T			100.00%		
2	N,N	WN	SN	SN	WN					N	T			100.00%		
3	N,T	ST	SN	SN	WN					N	T			100.00%		
4	N,N	ST	WN	SN	WN					T	T			80.00%		
5	T,T	ST	WN	SN	WN					N	T			83.33%		
6	N,N	ST	WN	SN	ST					T	T			71.43%		
7	N,T	ST	WN	SN	ST					N	T			75.00%		
8	N,N	ST	ST	SN	ST					T	T			66.67%		
9	T,T	ST	ST	SN	ST					T	T			60.00%		
10	N,N	ST	ST	SN	ST					T	T			54.55%		
11	N,T	ST	ST	SN	ST					T	T			50.00%		
12	N,N	ST	ST	SN	ST					T	T			46.15%		
13	T,T	ST	ST	SN	ST					T	T			42.86%		
14	N,N	ST	ST	SN	ST					T	T			40.00%		
15	N,T	ST	ST	SN	ST					T	T			37.50%		

i	History	B1				B2				B3				Pre	N/T	Miss Rate
		N,N	N,T	T,N	T,T	N,N	N,T	T,N	T,T	N,N	N,T	T,N	T,T	~	~	~
0	N,T					SN	SN	SN	SN					N	T	100.00%
1	T,T					SN	WN	SN	SN					N	N	50.00%
2	N,T					SN	WN	SN	SN					N	N	33.33%
3	T,T					SN	SN	SN	SN					N	N	25.00%
4	N,T					SN	SN	SN	SN					N	T	40.00%
5	T,T					SN	WN	SN	SN					N	N	33.33%
6	N,T					SN	WN	SN	SN					N	N	28.57%
7	T,T					SN	SN	SN	SN					N	N	25.00%
8	N,T					SN	SN	SN	SN					N	T	33.33%
9	T,T					SN	WN	SN	SN					N	N	30.00%
10	N,T					SN	WN	SN	SN					N	N	27.27%
11	T,T					SN	SN	SN	SN					N	N	25.00%
12	N,T					SN	SN	SN	SN					N	T	30.77%
13	T,T					SN	WN	SN	SN					N	N	28.57%
14	N,T					SN	WN	SN	SN					N	N	26.67%
15	T,T					SN	SN	SN	SN					N	N	25.00%

i	History	B1				B2				B3				Pre	N/T	Miss Rate
		N,N	N,T	T,N	T,T	N,N	N,T	T,N	T,T	N,N	N,T	T,N	T,T	~	~	~
0	T,T									SN	SN	SN	SN	N	T	100.00%
1	T,N									SN	SN	SN	WN	N	N	50.00%
2	T,N									SN	SN	SN	WN	N	T	66.67%
3	T,N									SN	SN	WN	WN	N	N	50.00%
4	T,T									SN	SN	SN	WN	N	T	60.00%
5	T,N									SN	SN	SN	ST	N	N	50.00%
6	T,N									SN	SN	SN	ST	N	T	57.14%
7	T,N									SN	SN	WN	ST	N	N	50.00%
8	T,T									SN	SN	SN	ST	T	T	44.44%
9	T,N									SN	SN	SN	ST	N	N	40.00%
10	T,N									SN	SN	SN	ST	N	T	45.45%
11	T,N									SN	SN	WN	ST	N	N	41.67%
12	T,T									SN	SN	SN	ST	T	T	38.46%
13	T,N									SN	SN	SN	ST	N	N	35.71%
14	T,N									SN	SN	SN	ST	N	T	40.00%
15	T,N									SN	SN	WN	ST	N	N	37.50%