Homework 3

CS-GY 6133

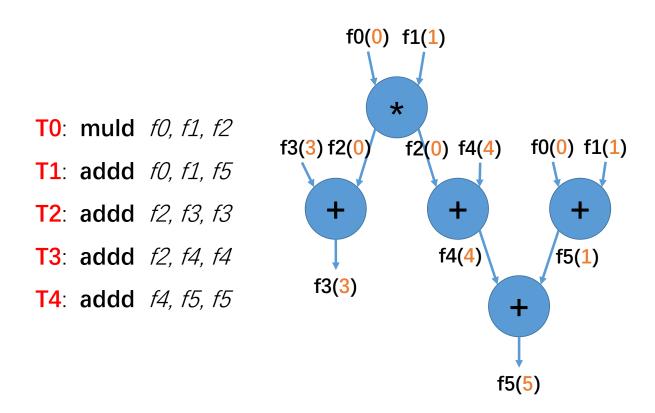
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Q1. Out-of-Order Execution Using Tomasulo's Algorithm

(a) Data-flow graph

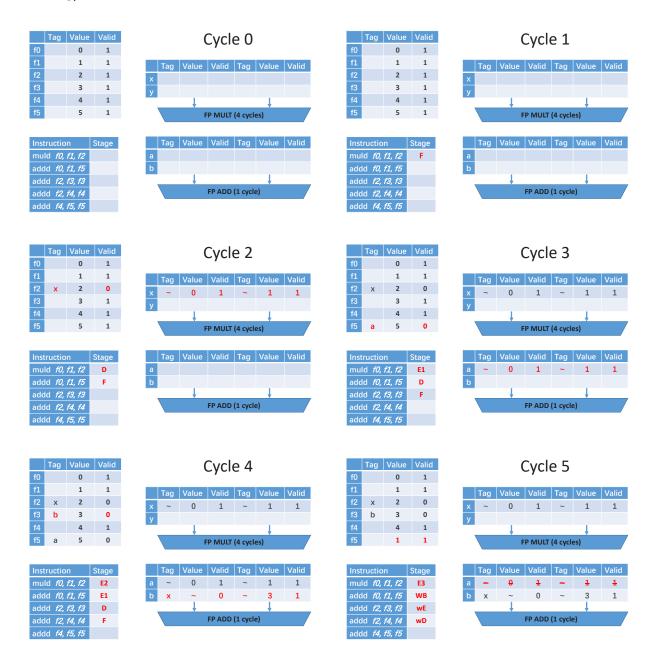
In our graph, fa(n) means that register a contains value n. After the code executes, the result should be:

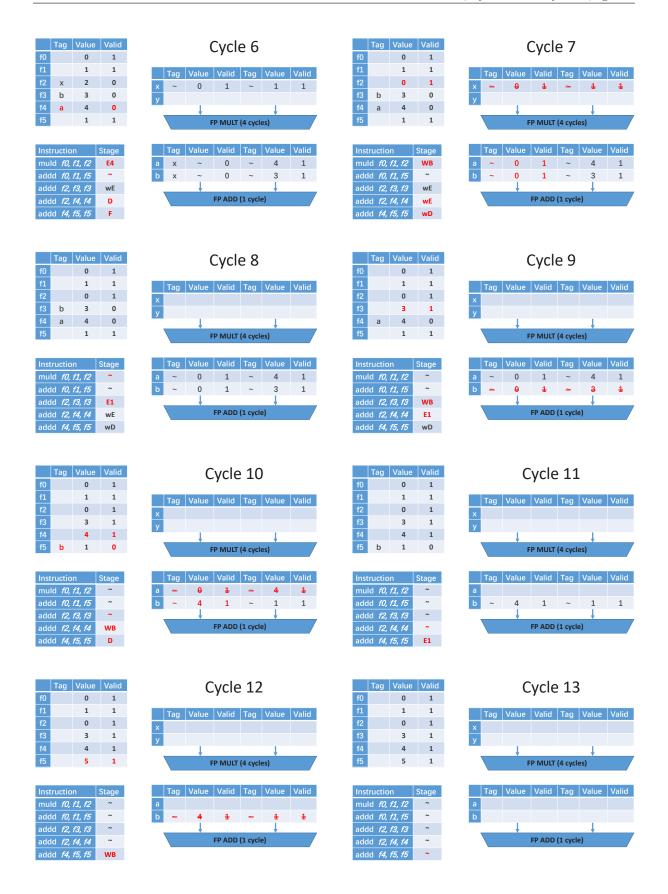
R[f0]=0, R[f1]=1, R[f2]=0, R[f3]=3, R[f4]=4, R[f5]=5.



(b) Simulate cycle-by-cycle

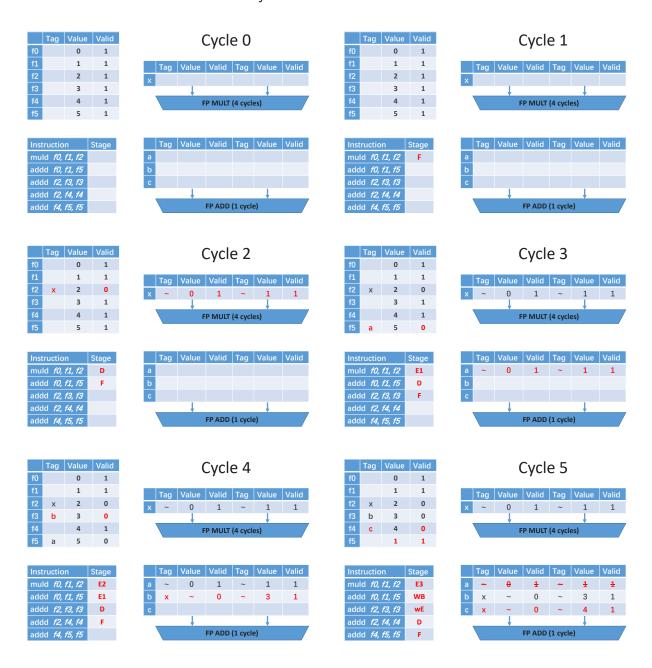
In the table below, 'wE' means waiting to execute (RAW dependency, waiting in reservation stations); 'wD' means waiting to decode/dispatch (reservation stations is full, instruction stalling).

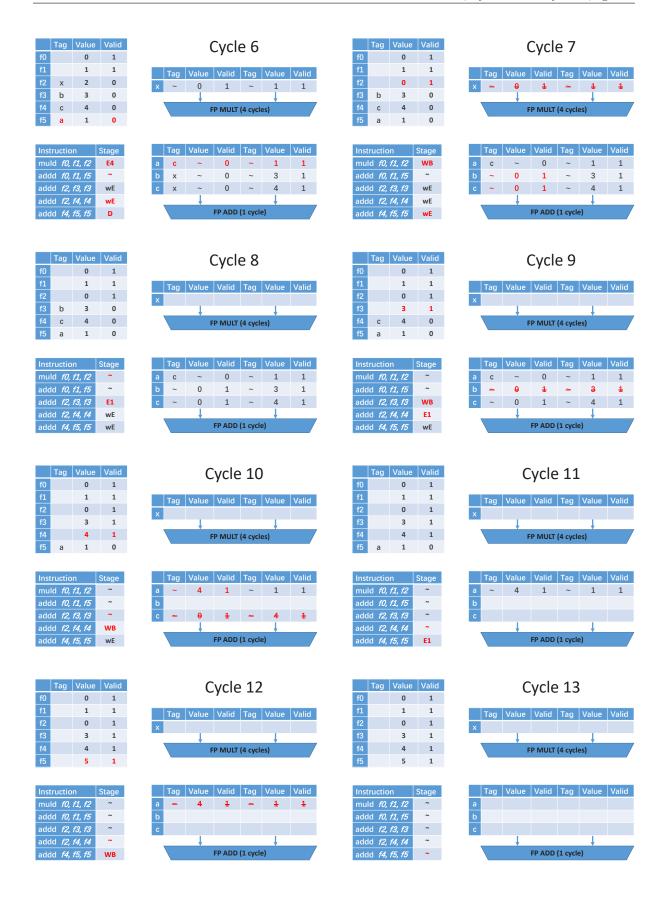




(c) Simulate cycle-by-cycle without stalling

At (b) - cycle 7 we found that FP ADD reservation station was full. The instruction had to wait until a free station was released. So we have to add one more station to FP ADD. We can also observe that FP MULT only need one reservation station at least.





(d) Simulate cycle-by-cycle with parallel FP adders

After simulation, we found that parallel process was needed at cycle 8. Two instructions could be dispatched at the same time. Thus, M=2.

