#### Control Unit

jx755

#### 1.1 inplementation

#### ctrl_unit.png

The control unit of the block diagram examines the instruction opcode bits [31 – 26] and decodes the instruction to generate control signals to be used in the additional modules.

in inst: 32-bit instruction

out lw: write back source selector signal for reg\_file

out sw: write-enable signal for data memory

out branch: branch indicator

out bnc\_type: branch type indicator

out jump: jump indicator

out funct: operation selector signal for ALU

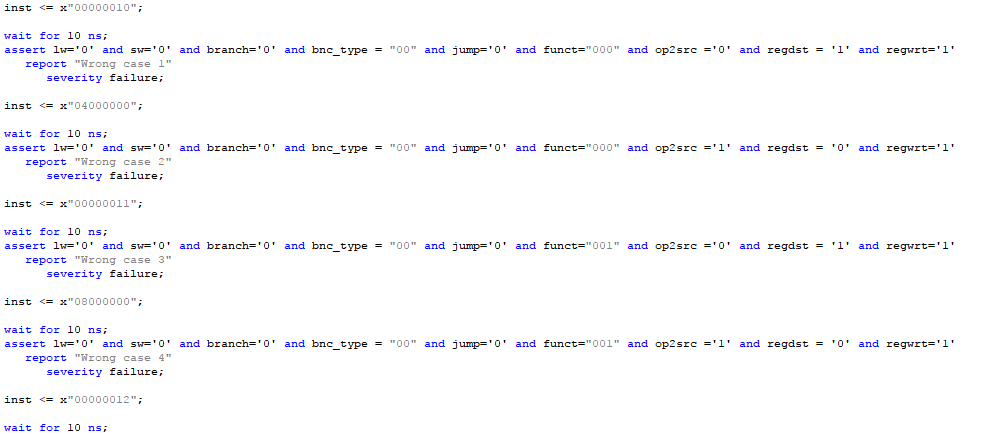
out op2src: op2 source selector signal for ALU

out regdst: register destination selector signal for reg\_file

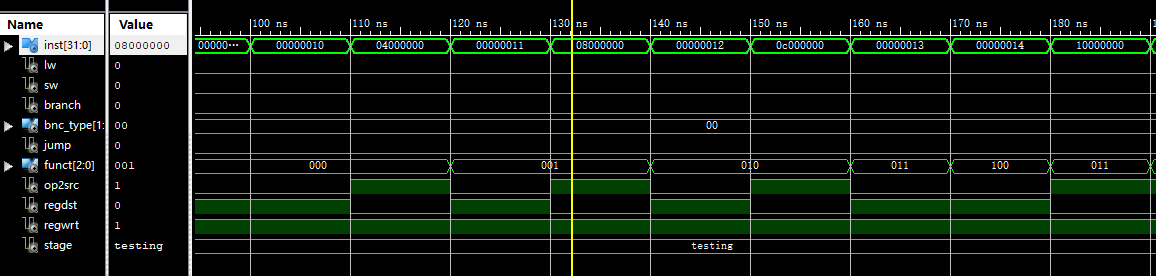
out regwrt: write-enable signal for file

##### 1.2 testbench

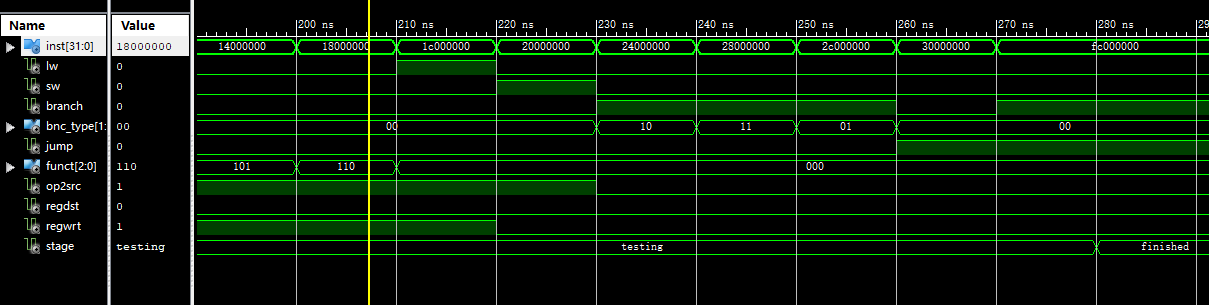
For each condition, I created one instruction to test correctness(bits unused is set to be zero) and used ‘assert’ statement to check the output automatically (see tb\_ctrl\_unit.vhd for details). The stage signal would change to FINISH only when all test cases passed, otherwise, the simulation would stop with severity level ‘failure’.



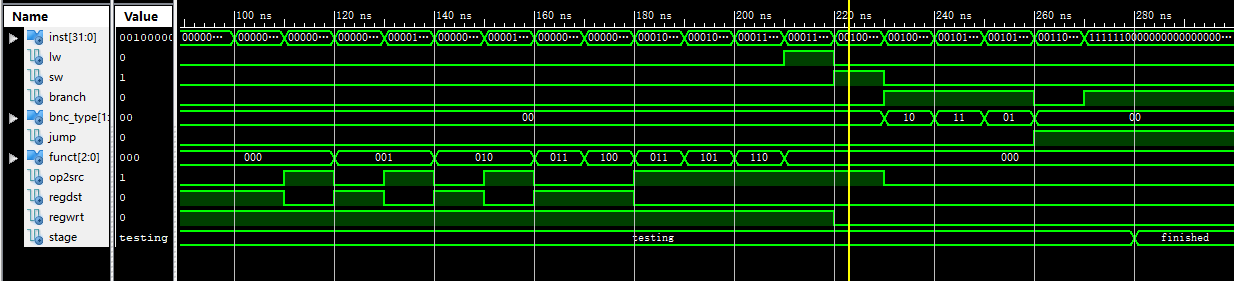
##### 1.3 Functional Simulation



1.3.1 Testing first 9 conditions

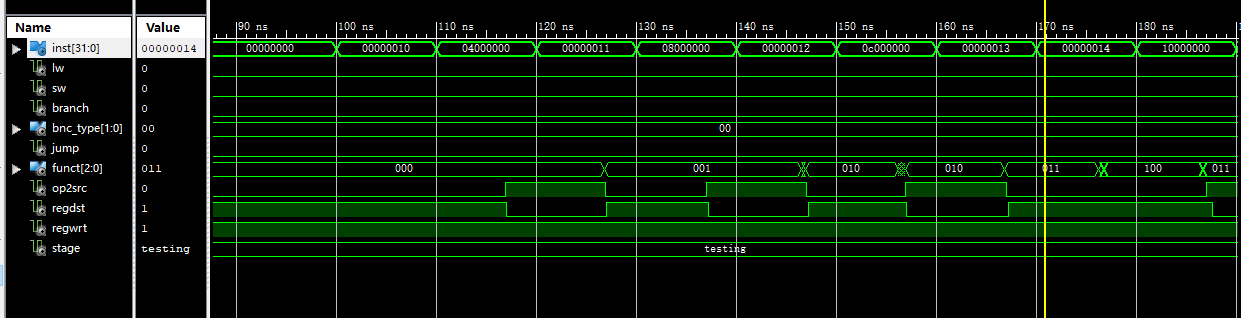


1.3.2 Testing latter 9 conditions

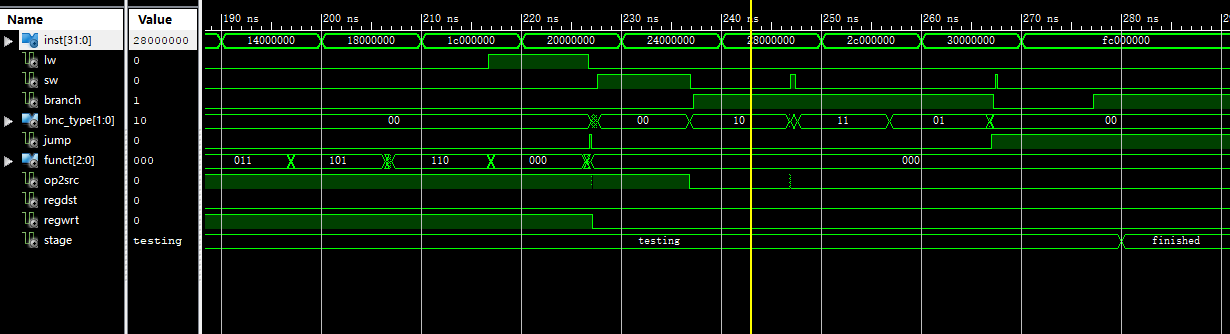


1.3.3 An overview with all cases passed.

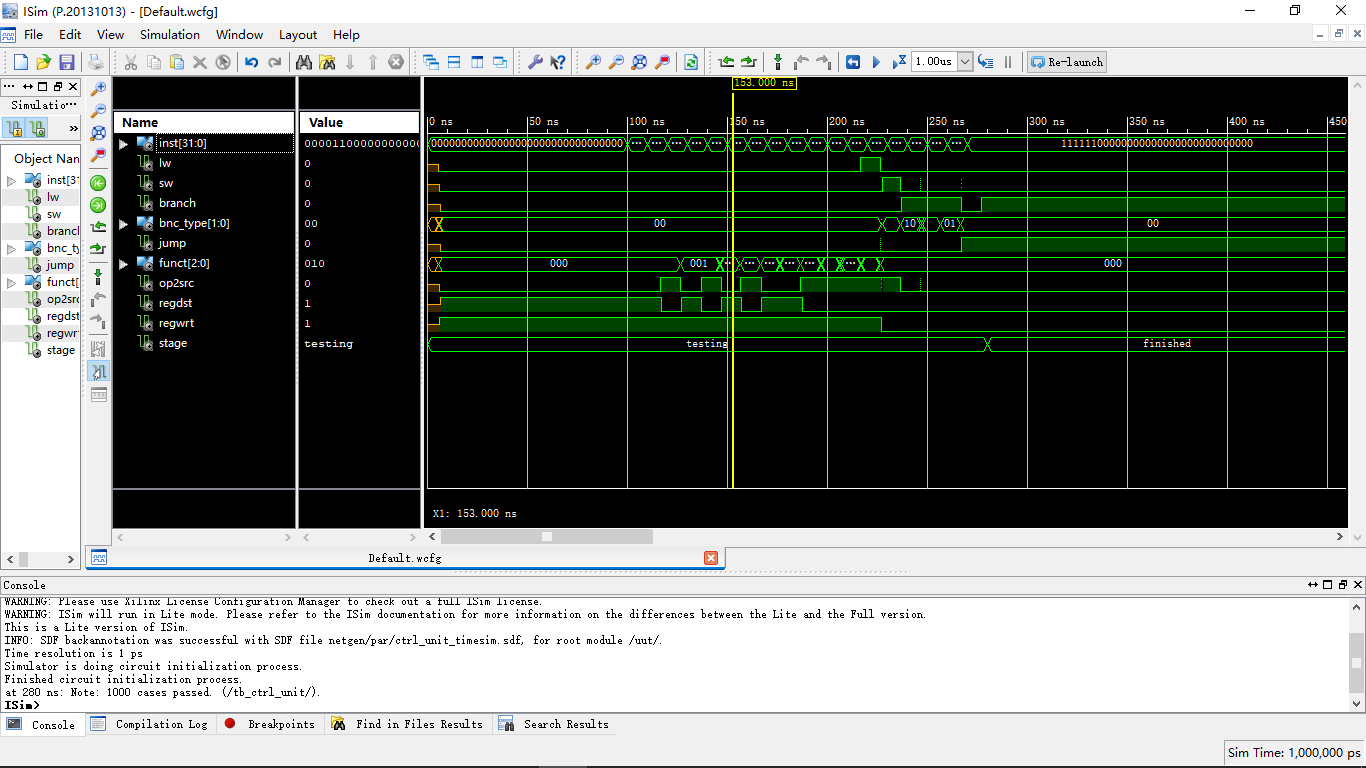
##### 1.4 Timing Simulation



1.4.1 Testing first 9 conditions



1.4.2 Testing latter 9 conditions



1.4.3 An overview with all cases passed.