Example 9.4 shows the whole description; the printout obtained from simulation is shown in Example 9.5. Figure 9.3 shows the timing diagram of the variables q, r, s as generated from Example 9.4. The point of showing all of this detail is to provide the reader with a complete example with detailed timing.

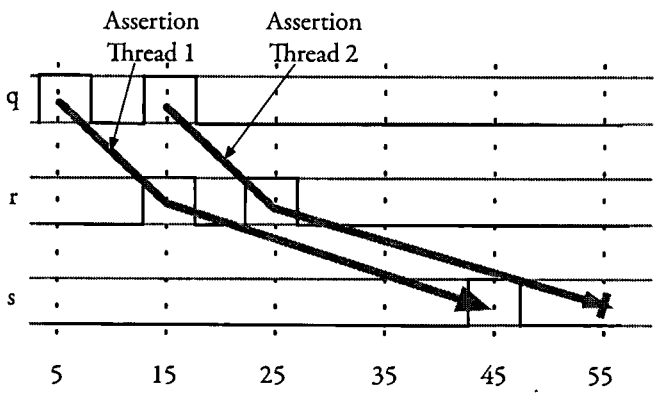

Figure 9.3 — Timing Diagram for Example 9.4

Note in the printout portion of the example that at time 45 "Yes!" is printed. This is assertion thread 1 succeeding at time 45 and printing its pass_ Statement. Assertion thread 2 starts at time 15 fails and prints "oops" at time 55 because it expects s to be TRUE.

A fine detail should not be overlooked at this point. Notice how the timing waveforms for q, r, and s were generated on lines 11-20 in Example 9.4. Specifically, q is set to 1 at time 4 and set back to 0 at time 6; this creates the first pulse on q that is recognized at time 5 by an assertion. One might ask if q could be set to 1 at time 5, when the clock edge occurs, and whether the assertion would still see it. These two situations are shown in Figure 9.4. The answer is *no* because the values used in assertions are the values sampled in the preponed part of the simulation kernel. As shown in the figure, if q changes at time 4, then the preponed value at time 5 of q is 1. However, if q changes at time 5, the preponed value of q is 0. That is, q has to be 1 *before* time 5 for it to be seen as 1 by an assertion at time 5.

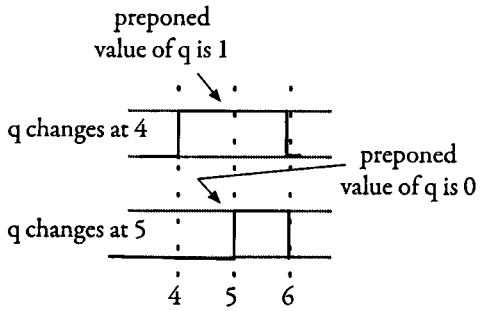

Figure 9.4 — Sampling Values in the Preponed Region

```
1          0 ck=0, q=0, r=0, s=0
2          4 ck=0, q=1, r=0, s=0
3          5 ck=1, q=1, r=0, s=0
4          6 ck=1, q=0, r=0, s=0
5         10 ck=0, q=0, r=0, s=0
6         14 ck=0, q=1, r=1, s=0
7         15 ck=1, q=1, r=1, s=0
8         16 ck=1, q=0, r=0, s=0
9         20 ck=0, q=0, r=0, s=0
10        24 ck=0, q=0, r=1, s=0
11        25 ck=1, q=0, r=1, s=0
12        26 ck=1, q=0, r=0, s=0
13        30 ck=0, q=0, r=0, s=0
14        35 ck=1, q=0, r=0, s=0
15        40 ck=0, q=0, r=0, s=0
16        44 ck=0, q=0, r=0, s=1
17        45 Yes!
18        45 ck=1, q=0, r=0, s=1
19        46 ck=1, q=0, r=0, s=0
20        50 ck=0, q=0, r=0, s=0
21 "ConcurrentAssertBasicBook.sv", 32:
22 assertQRS.P1a: started at 15s failed at 55s
23   Offending 's'
24 Error: "ConcurrentAssertBasicBook.sv", 32:
25 assertQRS.P1a: at time 55
26        55 oops
27        55 ck=1, q=0, r=0, s=0
28 $finish called from file
29 "ConcurrentAssertBasicBook.sv", line 20.
30 $finish at simulation time                56
```

Example 9.5 — Simulation Results of assertQRS

9.3 Sequences With Ranges and Repetitions

Sequence are widely use in specifying detailed protocols in digital systems and there is an extensive set of operators that can be used to specify the details of these. This section de-