**Tutorial 4  
LNGANG002 & BTJMAL001**

1.1.3

1. FPGAs are a collection of logic gates which can be rewired to perform different tasks as where microcontrollers are essentially miniature computers which can perform a variety of tasks specified by code.

Advantages:

* FPGAs offer better performance because of they can perform processing and calculations at a faster rate, compared to CPUs
* They are adaptable. Because they are so easily reprogrammable, you can adjust them to satisfy new requirements whenever you need.

Disadvantages:

* FPGAs have a higher power consumption and programmers do not have the ability to implement any power optimizations.
* The cost of production increases massively when higher quantities are   
  required.

1. Blocking assignments are evaluated and updated without any delay, as where non-blocking assignments will be evaluated immediately, however, they will only be updated at the end of the time step/after a delay.   
     
   In the snippets provided, the output for the blocking assignment will be the value of the input as the assignments for q1, q2 and out are evaluated and updated immediately.   
     
   For the non-blocking assignment, however, the output will be the initial value of q2. This is because q1 will only be set to the input at the end of the time step, thus q2 will be set to the initial value of q1, which will also only be updated at the end of the timestep. out will therefore be set to the initial value of q2 at the end of the timestep. q1 will however have the value of in at the end of the timestep.
2. Left:

* The output would be:  
  A B Out  
  0 1 x
* The reason the output is empty is because the module was instantiated with the variables in the incorrect order and because port mapping by order was used the value of the clk in the module is actually related to the value of A in the test bench, which never goes high thus the statement is not executed.

Right:

* The output would be:  
  A B Out  
  0 1 1
* This is the expected output and even though the arguments to the instantiation are in the incorrect order, port mapping my name was used to ensure that the correct values are used.

Port mapping by name is better to use when instantiating a module with many ports because although setting up the test bench might take slightly longer, there is a much smaller margin for error with regards to linking the incorrect variables when port mapping by name is used. Port mapping my order is useful when fewer ports are used.