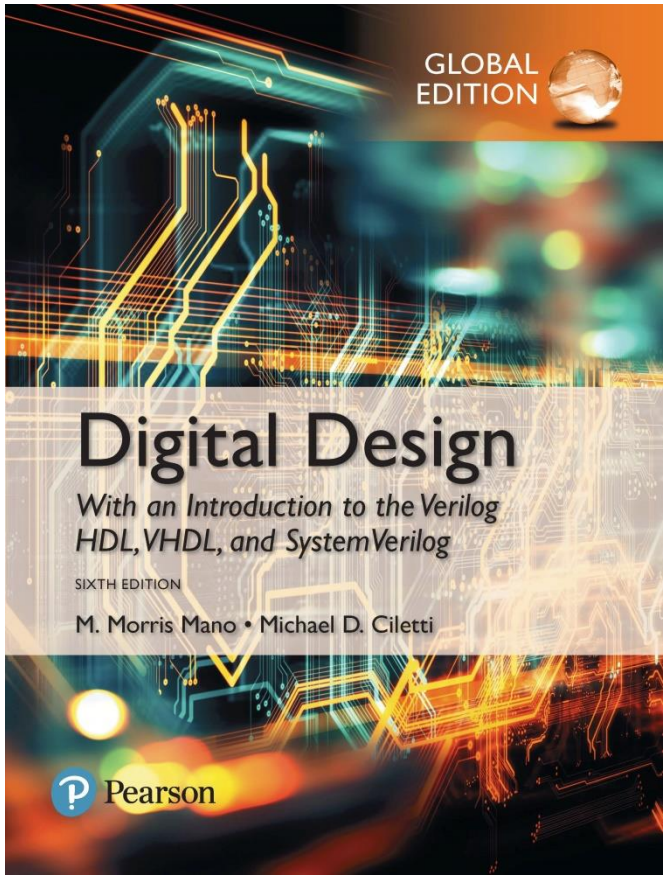
Digital Design

With an Introduction to the Verilog HDL, VHDL, and SystemVerilog

6th Edition, Global Edition

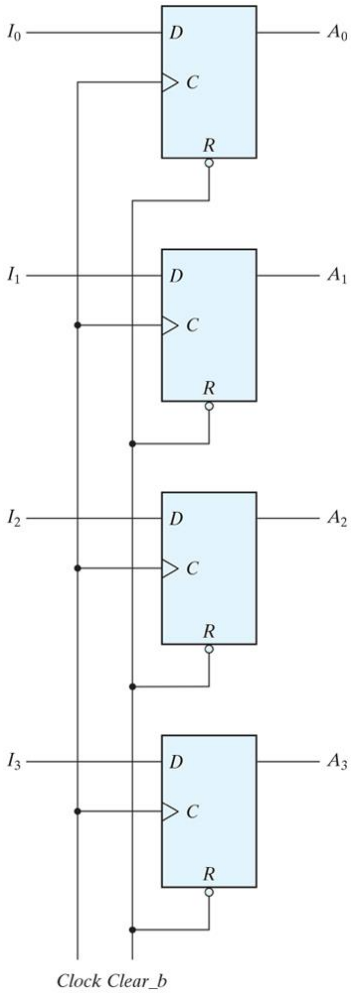


Chapter 06

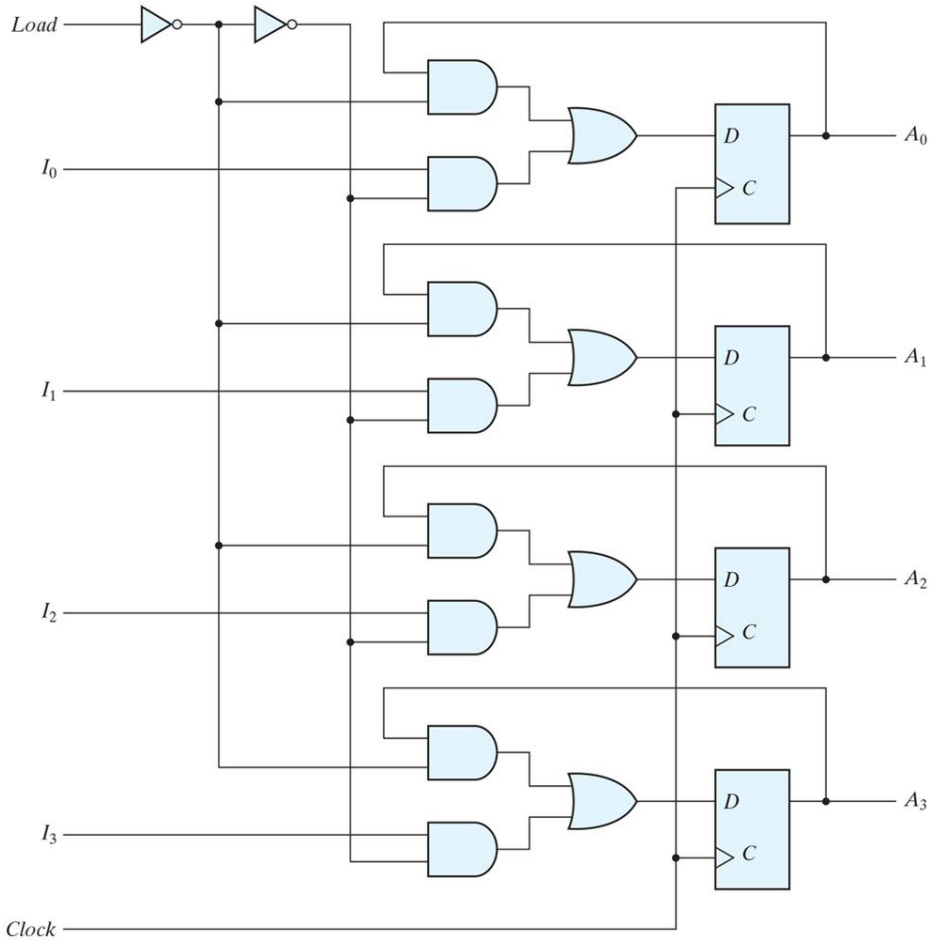
Registers and Counters

Pearson

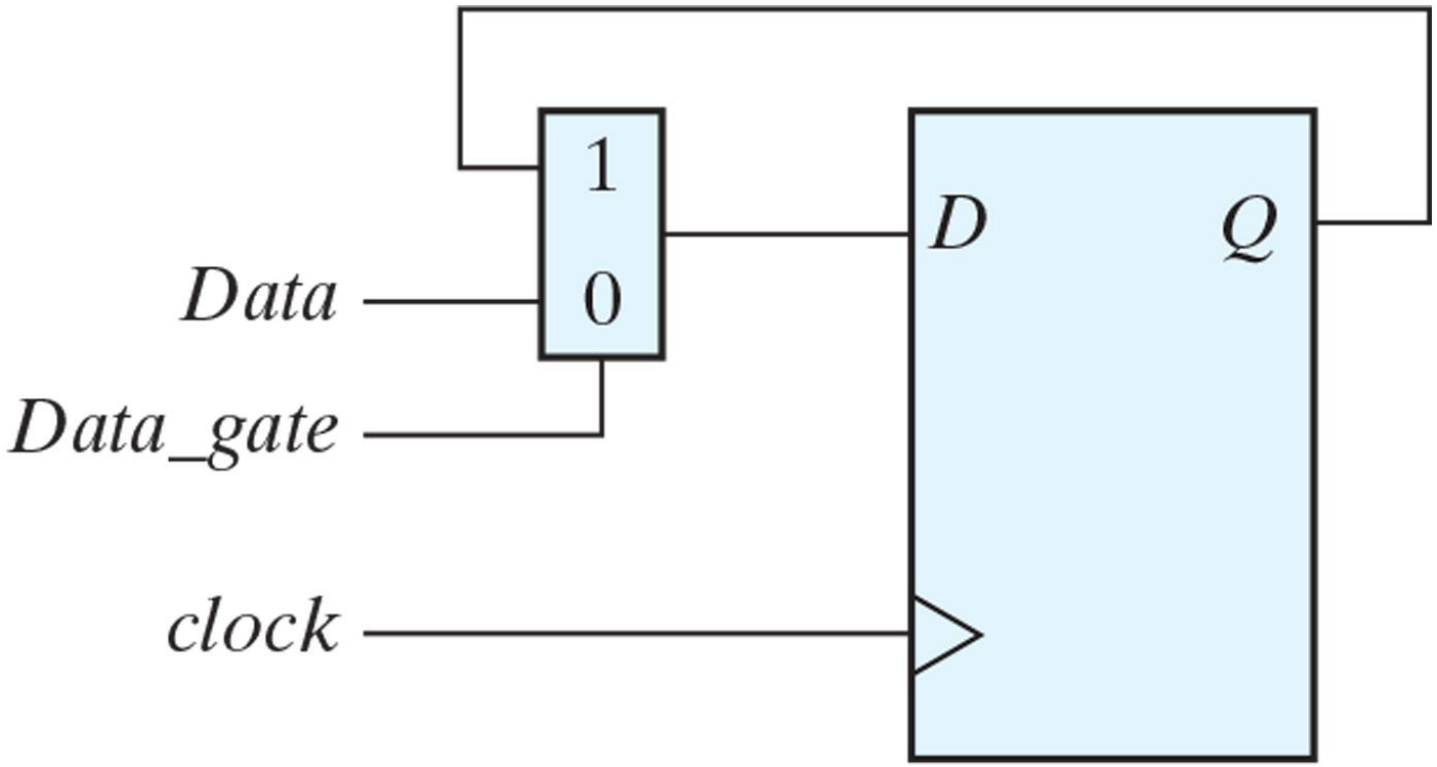
Four-bit register



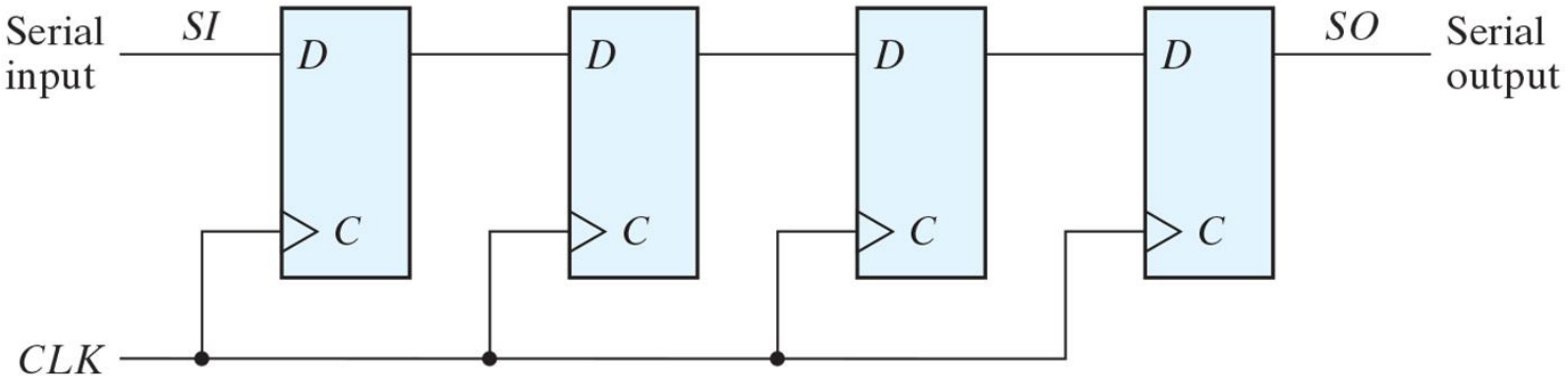
Four-bit register with parallel load



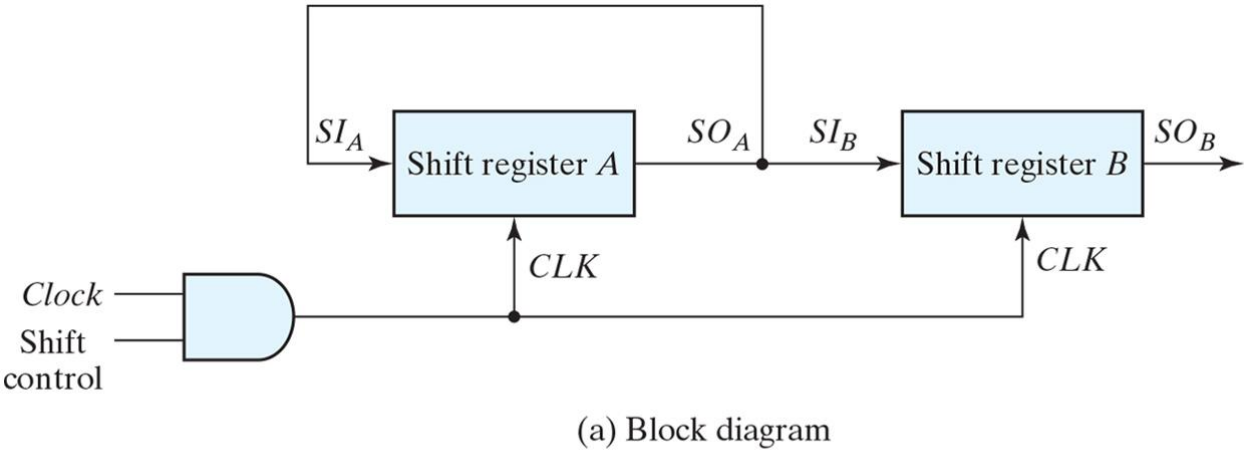
Exploiting MUX for Load



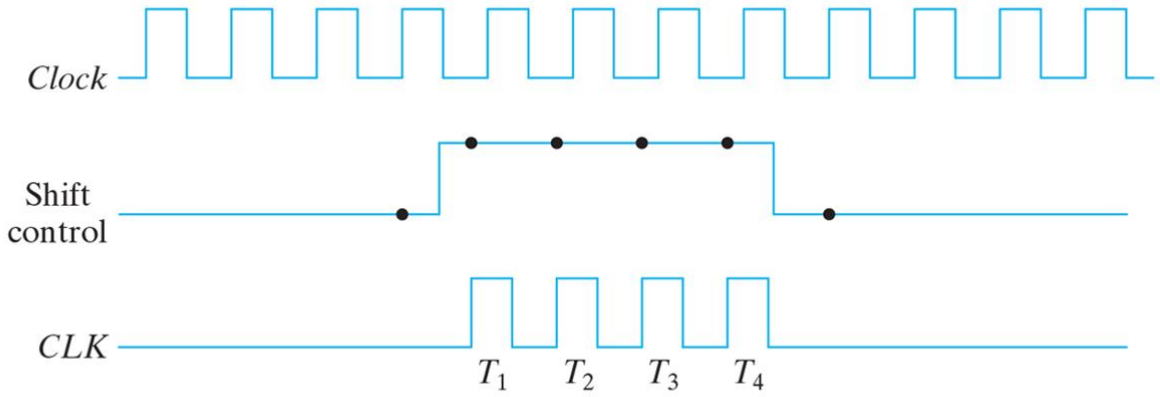
Four-bit shift register



Serial transfer from register *A* to register *B*.



(a) Block diagram

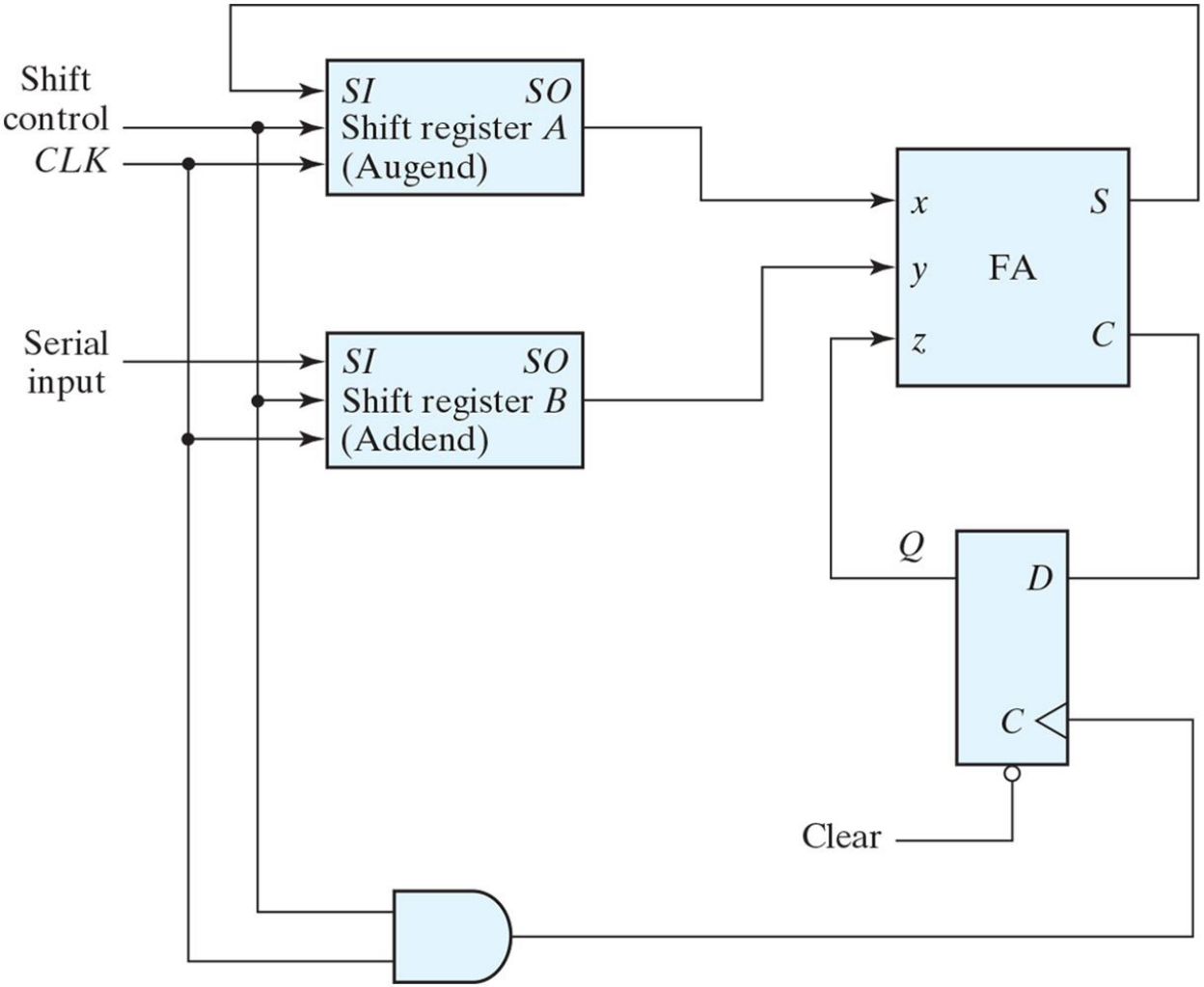


(b) Timing diagram

Serial-Transfer Example.

Timing Pulse	Shift Register *A*				Shift Register *B*			
Initial value	1	0	1	1	0	0	1	0
After T_1	1	1	0	1	1	0	0	1
After T_2	1	1	1	0	1	1	0	0
After T_3	0	1	1	1	0	1	1	0
After T_4	1	0	1	1	1	0	1	1

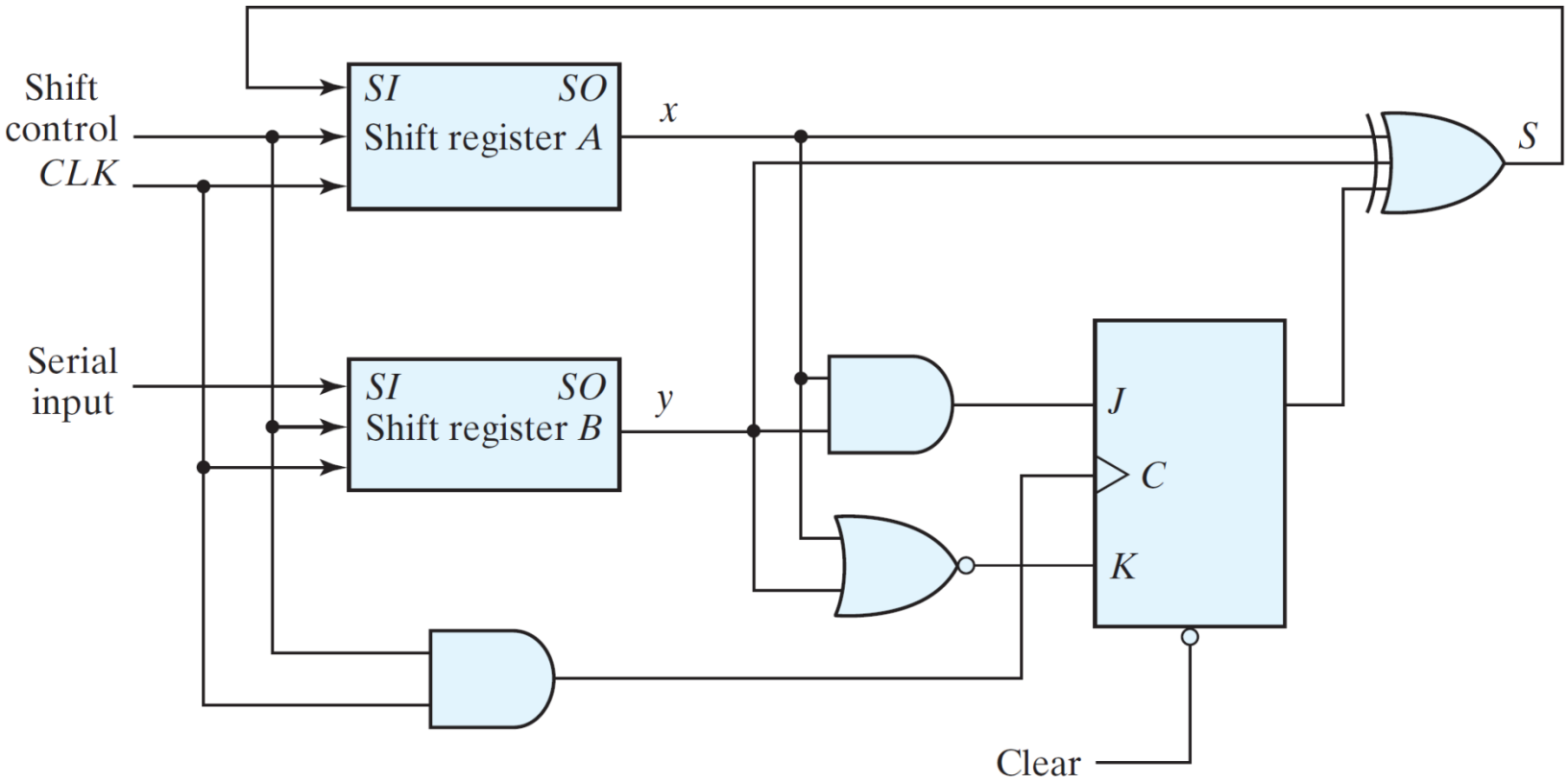
Serial adder.



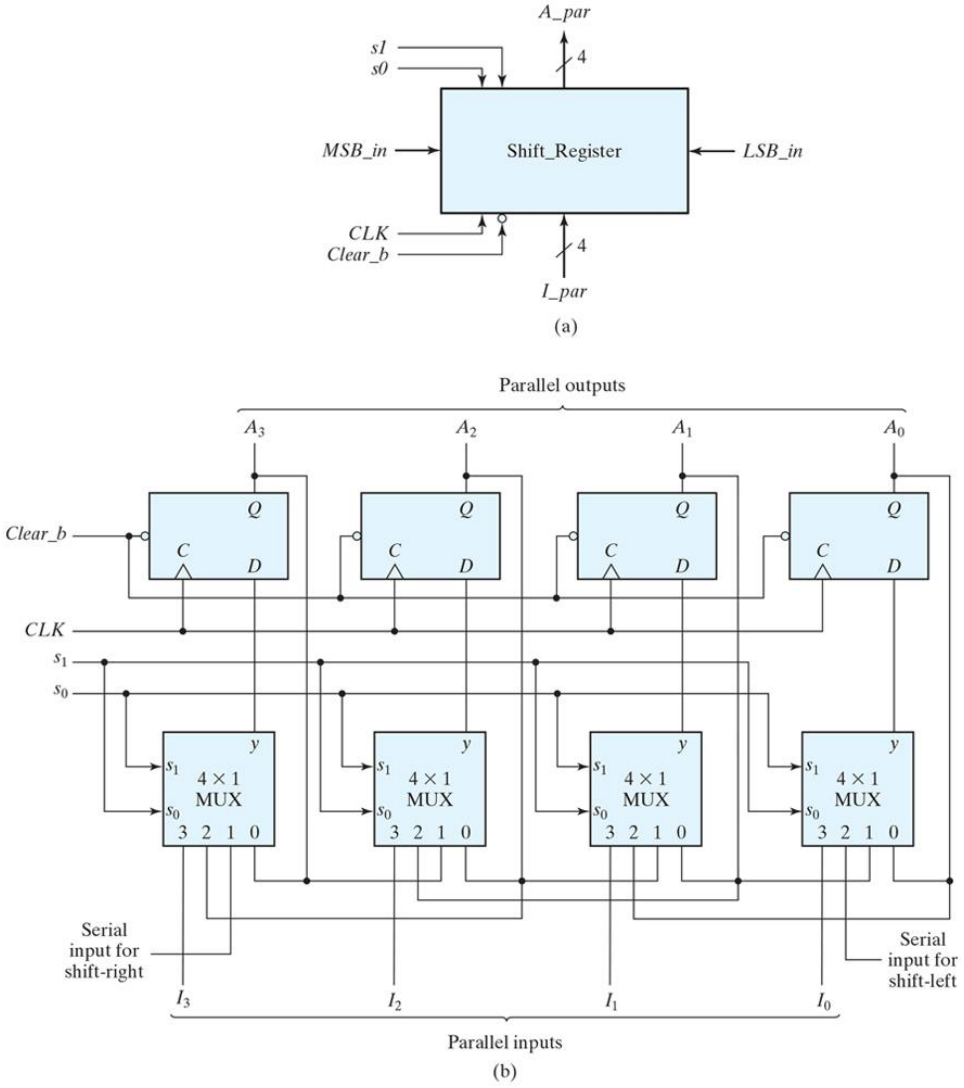
State Table for Serial Adder w/ JK FF

Present State	Inputs		Next State	Output	Flip-Flop Inputs	
Q	x	y	Q	S	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	0	1	0	X
0	1	0	0	1	0	X
0	1	1	1	0	1	X
1	0	0	0	1	X	1
1	0	1	1	0	X	0
1	1	0	1	0	X	0
1	1	1	1	1	X	0

Second form of serial adder.



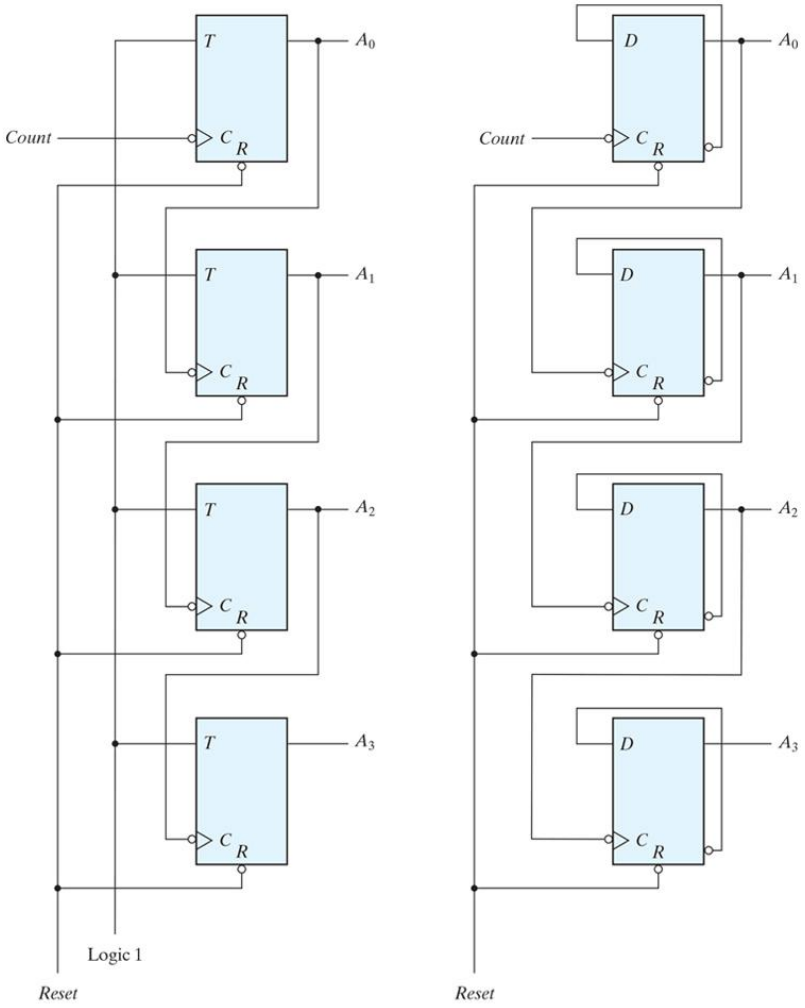
Four-bit universal shift register.



Function Table for the Register of Fig. 6.7.

Mode Control		
s_1	s_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

Four-bit binary ripple counter.



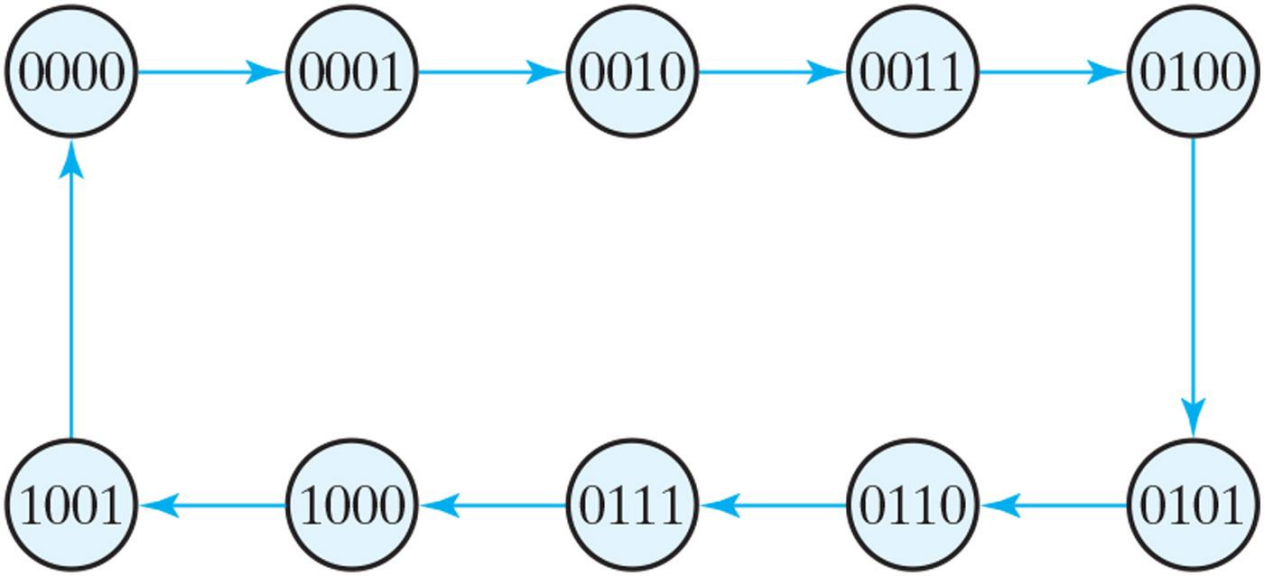
(a) With *T* flip-flops

(b) With *D* flip-flops

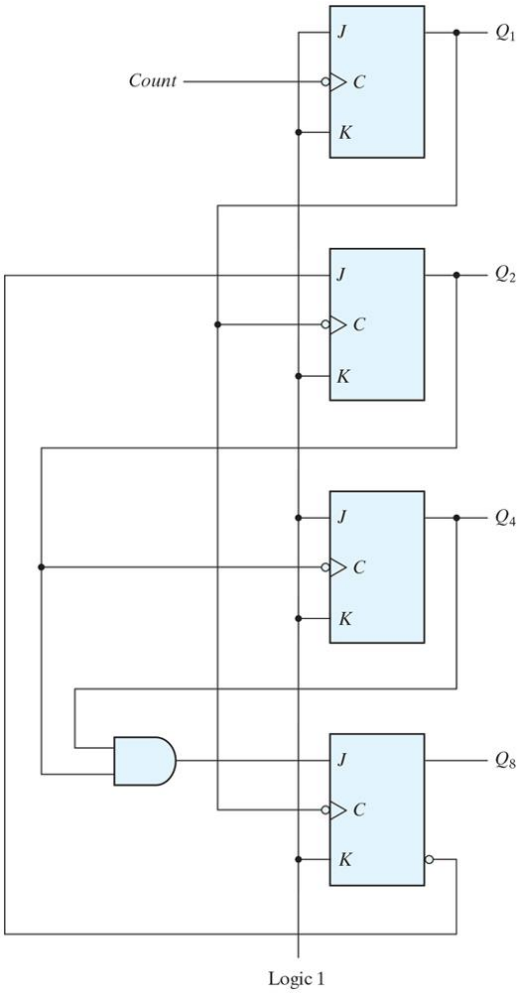
Binary Count Sequence.

A_3	A_2	A_1	A_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0

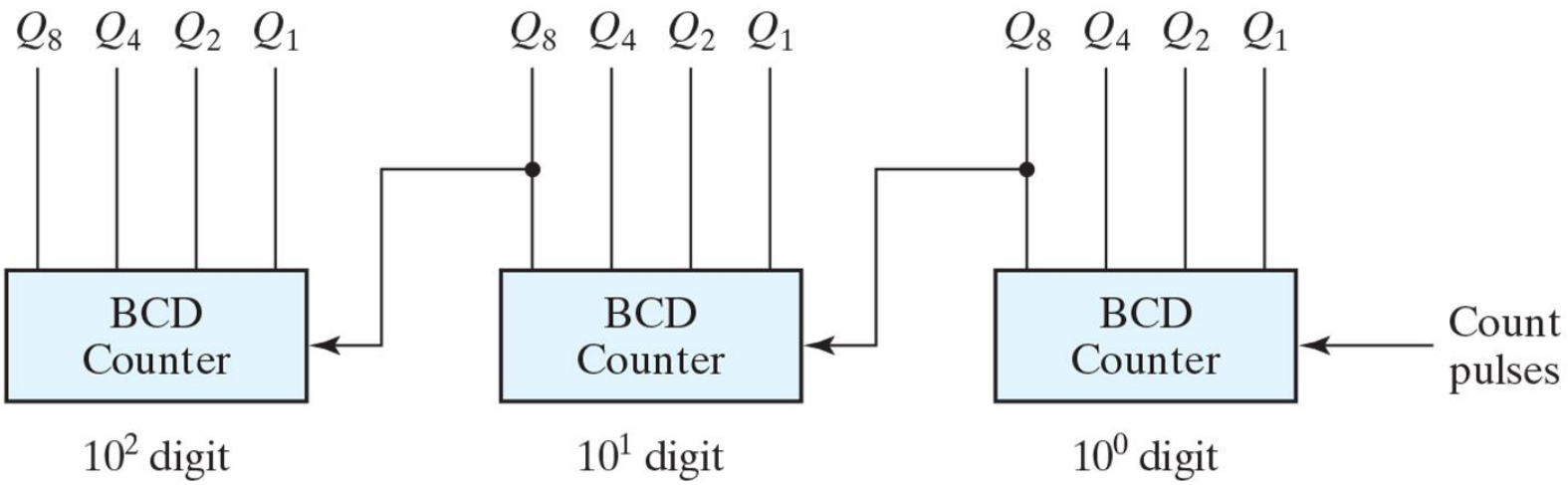
State diagram of a decimal BCD counter.



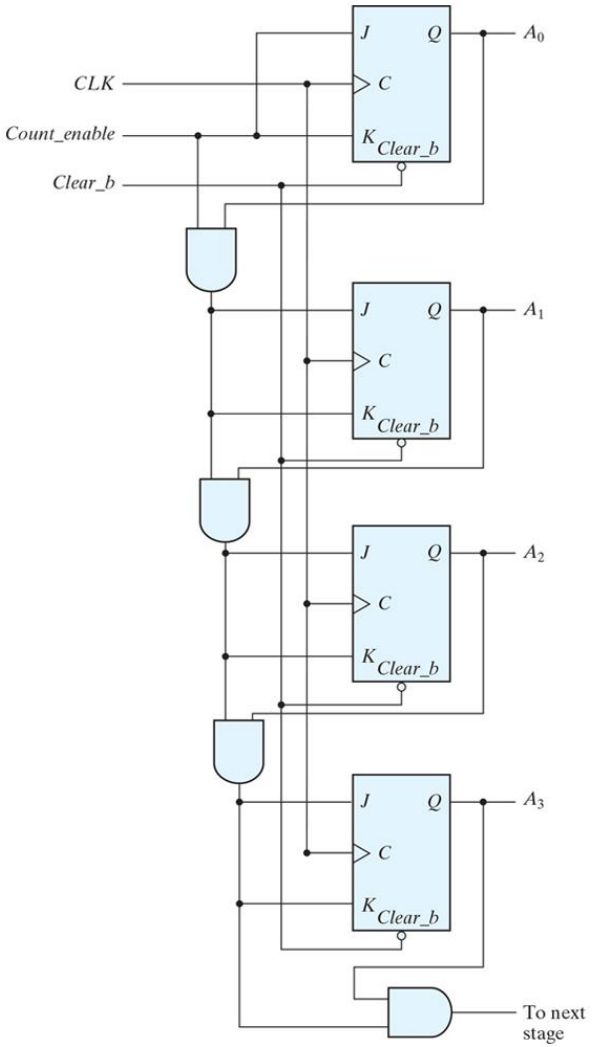
BCD ripple counter.



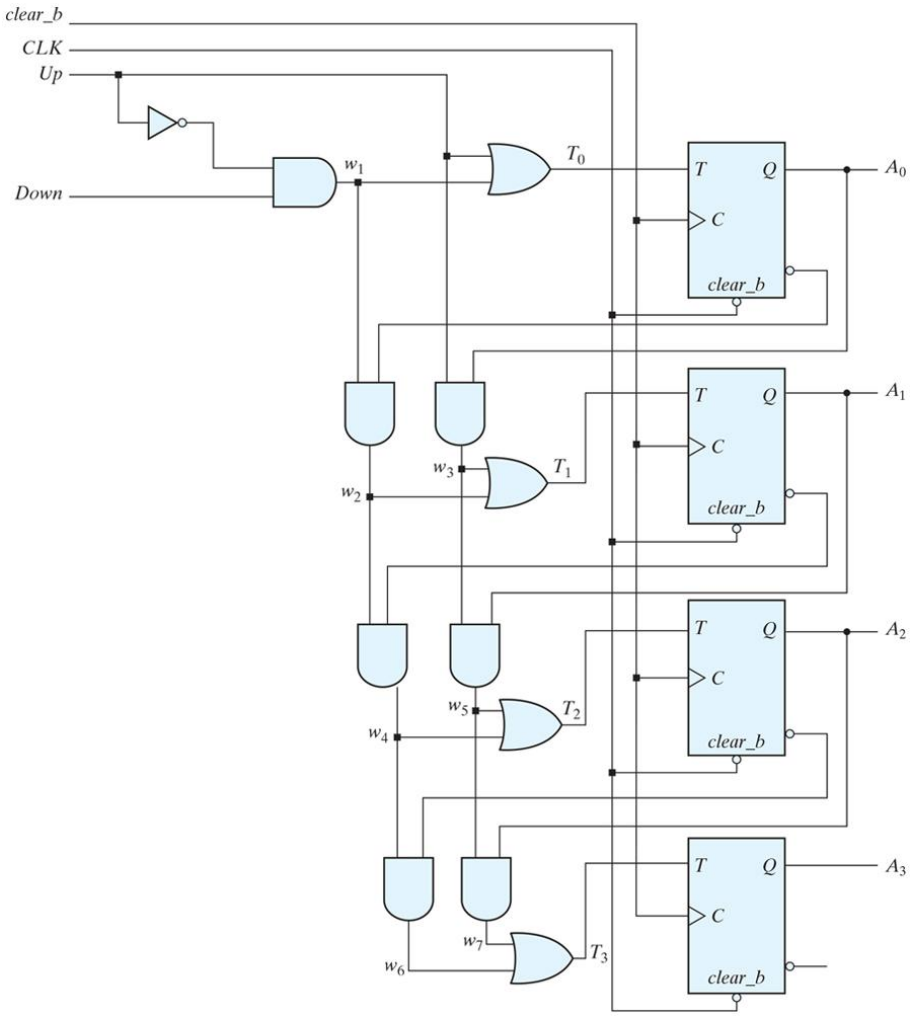
Block diagram of a three-decade decimal BCD counter.



Four-bit synchronous binary counter.



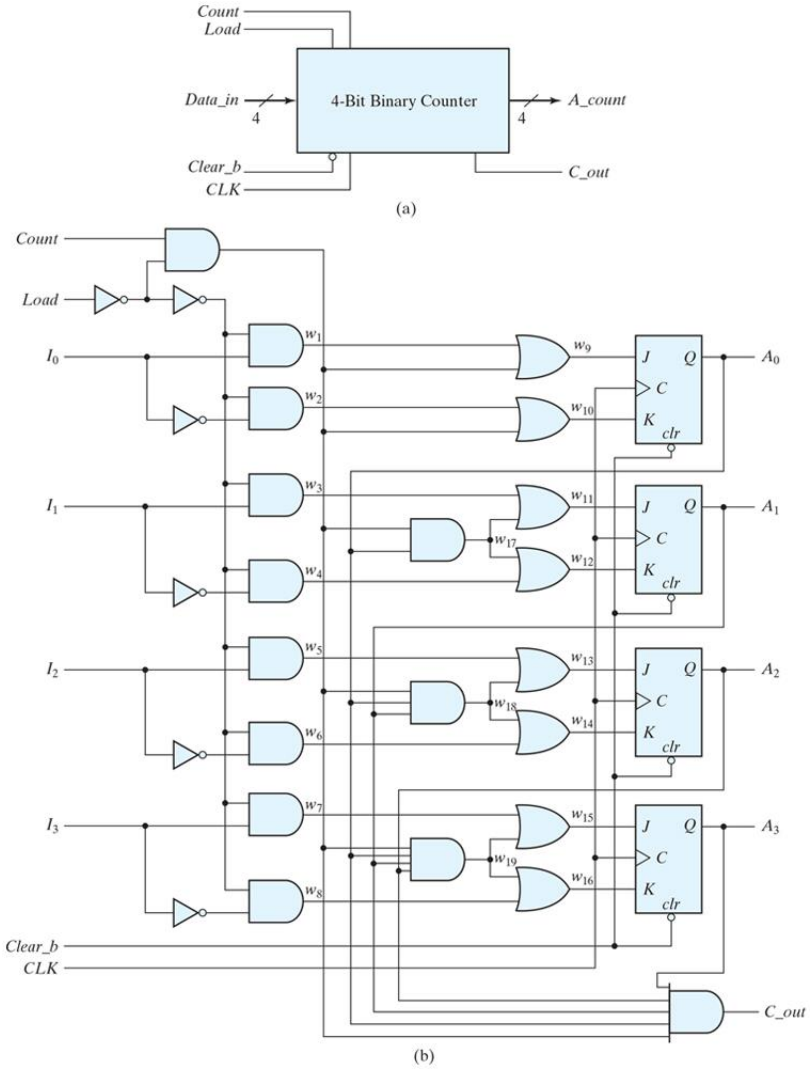
Four-bit up–down binary counter.



State Table for BCD Counter.

Present State				Next State				Output	Flip-Flop Inputs			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	y	T_{Q8}	T_Q4	T_{Q2}	T_{Q1}
0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	0	1
0	0	1	1	0	1	0	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	0	1
0	1	0	1	0	1	1	0	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	0	1
0	1	1	1	1	0	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	0	1
1	0	0	1	0	0	0	0	1	1	0	0	1

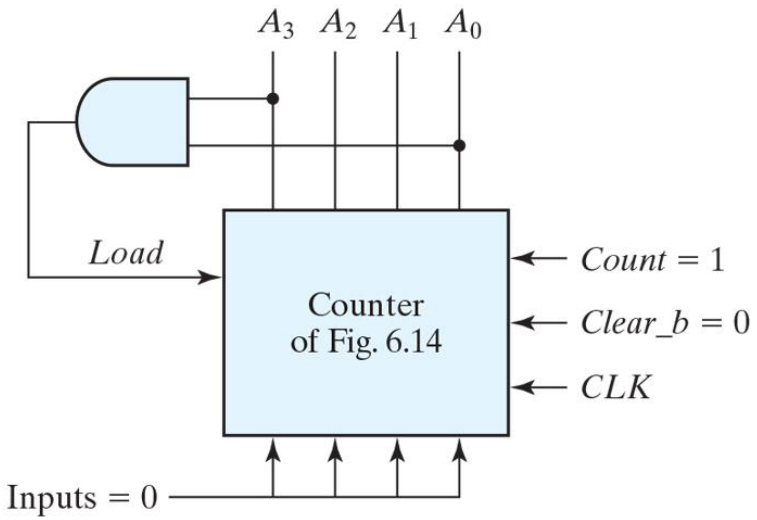
Figure 6.14
Four-bit binary counter with parallel load.



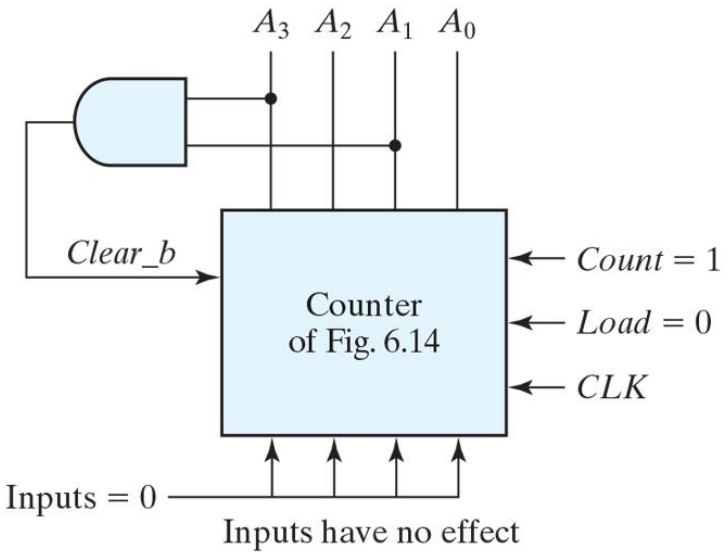
Function Table for the Counter of Fig. 6.14.

Clear_b	CLK	Load	Count	Function
0	X	X	X	Clear to 0
1	↑	1	X	Load inputs
1	↑	0	1	Count next binary state
1	↑	0	0	No change

Two ways to achieve a BCD counter using a counter with parallel load.



(a) Using the load input



(b) Using the clear input