

# ASSIGNMENT

Q1.

- (a) Differentiate between “hit” and “miss” with respect to cache memory.
- (b) How interrupts are handled? Explain.
- (c) Explain little endian and big endian data storage mechanisms.
- (d) Express  $A*B+(B*D+C*E)$  into reverse polish notation.
- (e) Differentiate between direct and indirect instruction.
- (f) Briefly list the types of interrupts with the help of suitable examples.”
- (g) Differentiate between RISC and CISC.
- (h) Explain updating techniques used in cache design.
- (i) Explain Virtual memory. Also state “Locality of Reference” principle.
- (j) What are different kinds of operation used in CPU design?

Q2.

- (a) Starting from initial value  $R=11011101$ , determine the sequence of binary values in R after a logical shift left, followed by a circular shift right, followed by a logical shift right and a circular shift.
- (b) Draw and explain the common bus system for the simple computer. Also, draw the various registers, types of bus (eg. Data bus, control bus, address bus and where they are being used). Also, explain LOAD, Selection and Fetch of data in those registers using appropriate diagram.

Q3 .

- (a) Convert the decimal 6 1.5867 into its binary equivalent.
- (b) Convert -6,75 (written in decimal) to floating point representation (single precision).
- {c) What do you mean by bus arbitration? Explain serial and parallel bus arbitration in

detail.

Q4.

- (a) Explain instruction cycle(fetch) and (decode) in detail. Also explain the working of computer registers used in it.
- (b) Draw an array multiplier circuit that multiplies a binary number of 4 bits with a number of 3 bits.
- (c) For the expression  $X=(A+B)*(C+D)$  when evaluated on stack machine how many number of machine instructions are required?

Q5.

- (a) Consider the following program segment used to execute on a hypothetical machine  
instructors are: Inst 1, Inst2, Inst3, Inst3, Inst5, Inst6, Inst7

Size(in words): 2,1,1,2,1,2,1 respectively.

Assume the word size of the instruction is 32 bit and the program has been loaded into the memory with starting address of 1000(decimal onwards). What could be the value present in PC during the execution of Inst6. (Memory byte addressable).

Q6.

- (a) Explain instruction formats with examples.
- (b) Consider a hypothetical processor which supports expand opcode technique. A 32 bit instruction is place in 256MW memory. If there exist 10, one address instruction then how many zero-address instruction are possible.

Q7.

- (a) Differentiate between hardwired control and micro programmed control. Is it Possible to have a hardwired control associated with a control memory?

(b) Explain various memory based addressing modes in detail with the help of suitable diagram.

Q8.

- (a) Discuss booth algorithm and perform  $-5 \times 2$  using this.
- (b) Discuss division algorithm (restoration method) and solve  $10/3$  using this.

Q9.

- (a) What do you mean by Memory Hierarchy and Cache Organization ? Also explain different mapping in cache (memory interfacing).
- (b) Explain pipelining in detail i.e. performance, advantages, implementation in Control Unit etc.  
Also explain pipeline Hazard and ways to overcome them.