2022 Digital IC Design

Homework 2: Traffic Light System

1. Introduction:

In this homework, you are requested to design a Traffic Light System (TLS). The TLS circuit will receive *Gin*, *Yin*, *Rin* signals representing the duration time of green light, yellow light and red light respectively, and output traffic light signal by *Gout*, *Yout*, and *Rout* according to the state of the system. The specification and the main functions of TLS circuit will be described in detail in the following section.

2. Design Specifications:

2.1 Block Overview

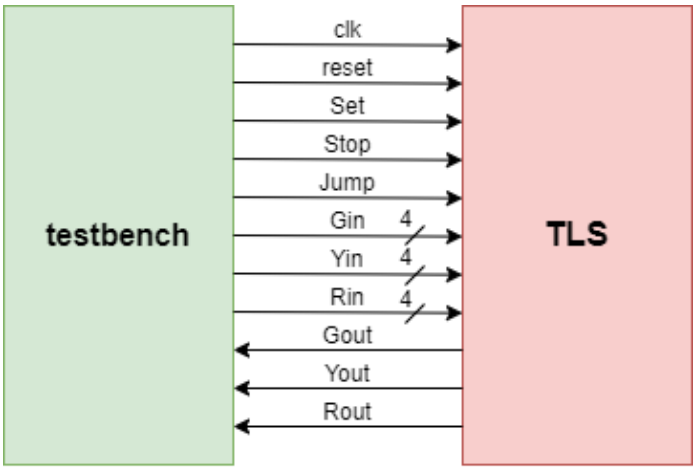

Fig. 1. The block overview.

2.2 I/O Interface

Signal Name	I/O	width	Description
clk	I	1	This circuit is a synchronous design triggered at the positive edge of clk.
reset	I	1	Active-high asynchronous reset signal.
Set	I	1	New setting value indication signal. When this signal is high, *Gin*, *Yin*, and *Rin* are the new duration time of green, yellow and red light respectively.
Stop	I	1	System stop indication signal. When this signal is high, TLS must maintain its current output and state until the stop signal goes low.
Jump	I	1	State jumping indication signal. TLS must transition to the red light immediately.
Gin	I	4	Setting value of green light duration time. The range

			of *Gin* is from 1 to 15. This signal is only valid when *Set* signal is high.
Yin	I	4	Setting value of yellow light duration time. The range of *Yin* is from 1 to 15. This signal is only valid when *Set* signal is high.
Rin	I	4	Setting value of red light duration time. The range of *Rin* is from 1 to 15. This signal is only valid when *Set* signal is high.
Gout	O	1	Green indicator of TLS output.
Yout	O	1	Yellow indicator of TLS output.
Rout	O	1	Red indicator of TLS output.

2.3 File Description

File Name	Description
TLS.v	The module of traffic light system, which is the top module in this design.
TLS_tb.v	The testbench file. The content in this file is **not allowed** to be modified.

2.4 System Description

2.4.1 Main functions of TLS

There are three control signals in TLS circuit, which are *Set*, *Stop*, and *Jump*. These signals will not be high at the same time. When *Set* signal is high, *Gin*, *Yin*, and *Rin* signals are valid. TLS has to set the duration time of the green, yellow and red light according to *Gin*, *Yin*, and *Rin*, respectively. When the time setting of the TLS is completed, TLS will output the corresponding signals in the order of green, yellow and red. The unit of the duration time is the clock cycle. For example, assume that the duration time of green light, yellow light, and red light are 4, 2 and 3, respectively. TLS must output *Gout* = 1, *Yout* = 0, *Rout* = 0 for 4 consecutive cycles, and then output *Gout* = 0, *Yout* = 1, *Rout* = 0 for 2 consecutive cycles. Finally, *Gout* = 0, *Yout* = 0, *Rout* = 1 is output for 3 consecutive cycles, and the state of TLS will transition to the green light again. Notably, the duration time of each light signal keeps unchanged until the *Set* signal is high.

When the *Stop* signal is high, TLS will remain in its current state until the *Stop* signal is pulled down. Meanwhile, the output light signal should be not changed, and the counting of the system should also stop. For example, assume the duration time of green light is 4, and the *Stop* signal becomes high at the second cycle of green light. The TLS will remain in the green state and output *Gout* = 1, *Yout* = 0, *Rout* = 0, and the counting will also remain. After the *Stop*

signal is pulled down, the green light state has to keep for another two cycles.

When the *Jump* signal is high, TLS must transition to the red light immediately. The count of the system will be reset at the same time. For example, assume the duration time of green light and red light are 4 and 2, respectively, and the *Jump* signal becomes high at the third cycle of green light. TLS will go to red light immediately and output *Gout* = 0, *Yout* = 0, *Rout* = 1 for 2 cycles. The *Jump* signal will only appear on green or yellow lights.

2.4.2 Timing diagram of *Set* signal

After the system reset, TLS will set the duration time of each light when *Set* signal is high. And the state of TLS will become green light at the same time. Be careful that the time duration of each light only changes when *Set* signal is pulled up. Otherwise, *Gin*, *Yin*, and *Rin* signals are invalid.

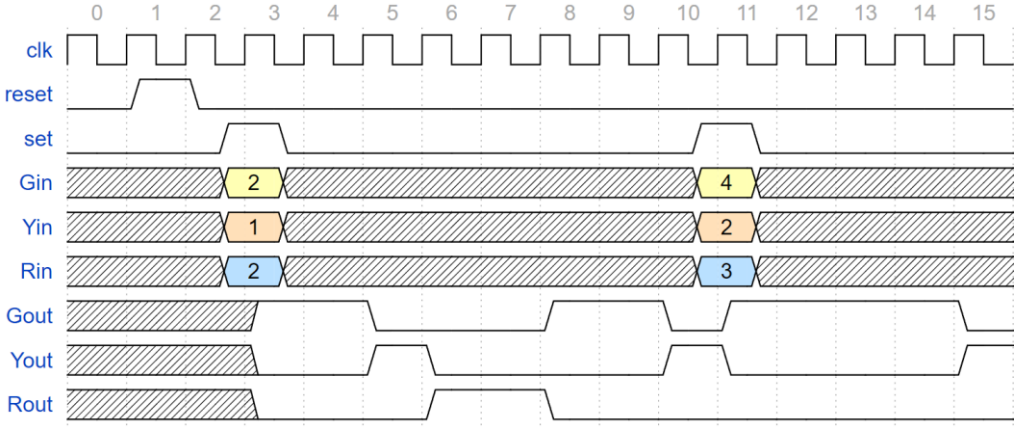

Fig. 2. Timing diagram of *Set* signal.

2.4.3 Timing diagram of *Stop* signal

When the *Stop* signal is high, TLS will remain in its current state until the *Stop* signal is pulled down. Meanwhile, the output light signal should be not changed, and the counting of the system should also stop.

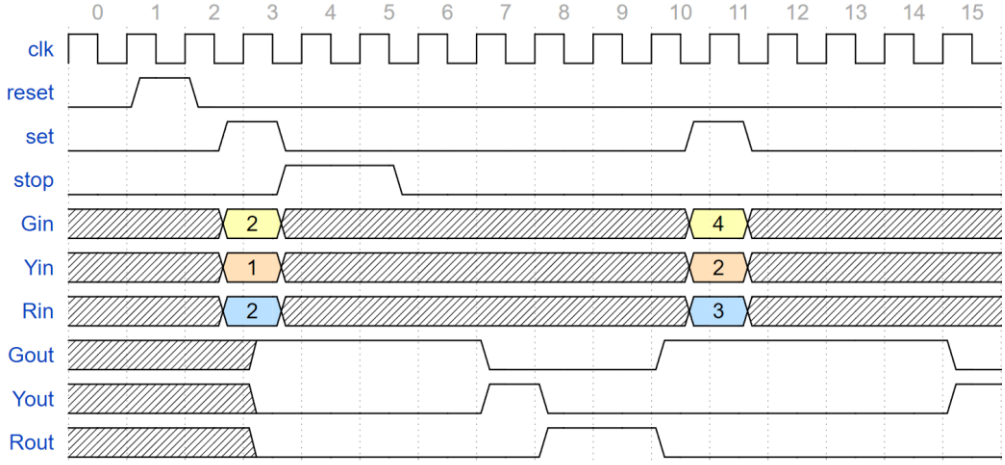

Fig. 3. Timing diagram of *Stop* signal.

2.4.4 Timing diagram of *Jump* signal

When the *Jump* signal is high, TLS must transition to the red light immediately. The count of the system will be reset at the same time. The *Jump* signal may be pulled up when the state is about to transition (Ex. at 8-th cycle). In this situation, the *Jump* signal has higher priority, so TLS will become red light and (*Gout*, *Yout*, *Rout*) should be (0, 0, 1).

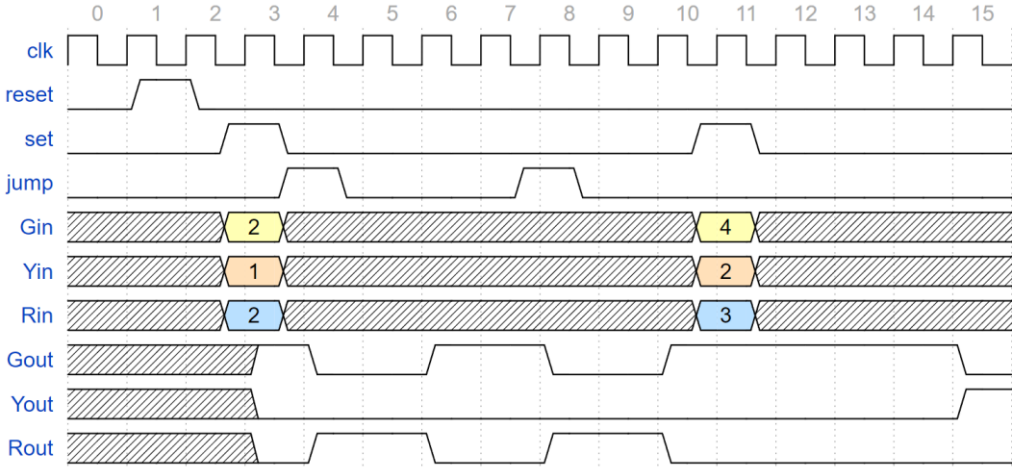

Fig. 4. Timing diagram of *Jump* signal.

3. Scoring:

3.1 Basic function testing **[60%]**

In stage 1, testbench will verify the basic function of your design. The TLS should be able to set duration time according to *Set*, *Gin*, *Yin*, and *Rin*, and change its state correctly. *Stop* and *Jump* signals will remain low in this stage. All of the results should be generated correctly, and you will get the following message in ModelSim simulation.

```
# --stage1 simulation--
#
# Setting1: PASS
#
# Setting2: PASS
#
# Setting3: PASS
#
# Setting4: PASS
#
# Setting5: PASS
#
# Setting6: PASS
#
# Setting7: PASS
#
# Setting8: PASS
#
# Setting9: PASS
#
# Setting10: PASS
#
```

Fig. 5. Simulation result of stage 1.

3.2 *Stop* situation testing **[20%]**

In stage 2, the TLS should be able to set duration time according to *Set*, *Gin*, *Yin*, and *Rin*, and change its state correctly. When *Stop* signal is high, TLS should process it properly to pass the simulation. All of the results should be generated correctly, and you will get the following message in ModelSim simulation.

```
# --stage2 simulation--
#
# Setting11: PASS
#
# Setting12: PASS
#
# Setting13: PASS
#
# Setting14: PASS
#
# Setting15: PASS
#
# Setting16: PASS
#
# Setting17: PASS
#
# Setting18: PASS
#
# Setting19: PASS
#
# Setting20: PASS
```

Fig. 6. Simulation result of stage 2.

3.3 *Jump* situation testing **[20%]**

In stage 3, the TLS should be able to set duration time according to *Set*, *Gin*, *Yin*, and *Rin*, and change its state correctly. When *Jump* signal is high, TLS should process it properly to pass the simulation. All of the results should be generated correctly, and you will get the following message in ModelSim simulation.

```
# --stage3 simulation--
#
# Setting21: PASS
#
# Setting22: PASS
#
# Setting23: PASS
#
# Setting24: PASS
#
# Setting25: PASS
#
# Setting26: PASS
#
# Setting27: PASS
#
# Setting28: PASS
#
# Setting29: PASS
#
# Setting30: PASS
```

Fig. 7. Simulation result of stage 3.

4. Submission:

4.1 Submitted files

You should classify your files into two directories and compress them to .zip format. The naming rule is HW2_studentID_name.zip. If your file is not named according to the naming rule, you will lose five points.

	RTL category
*.v	All of your Verilog RTL code
	Documentary category
*.pdf	The report file of your design (in pdf).

4.2 Report file

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible. If your report is incomplete, you may lose up to ten points.

4.3 Note

Please submit your .zip file to folder HW2 in moodle.

Deadline: 2022/4/8 16:55

If you have any problem, please contact TA by email

slnv126@gmail.com