# 2022 Digital IC Design Homework 3

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|---|---|
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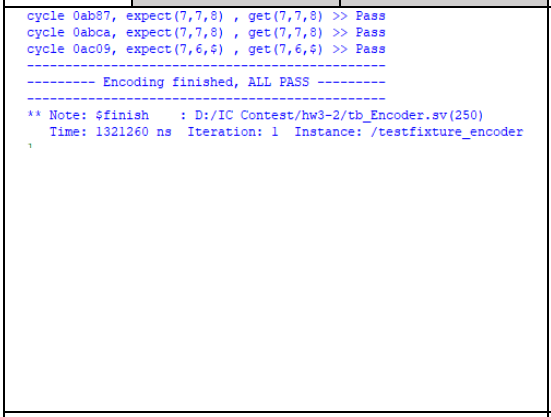
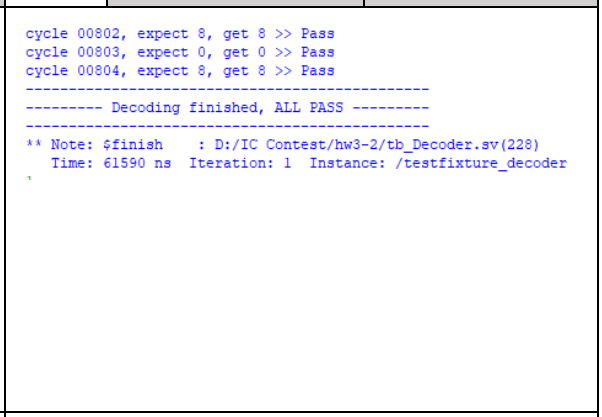
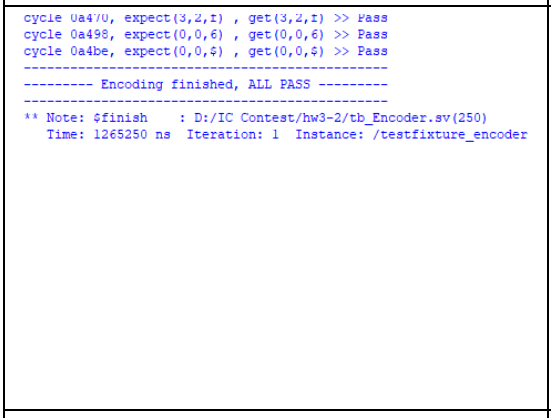
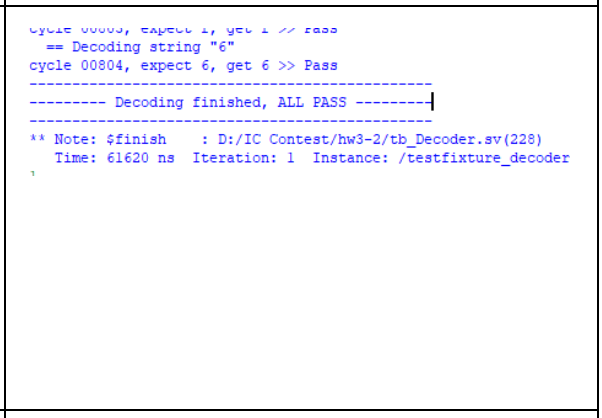
**Simulation Result**

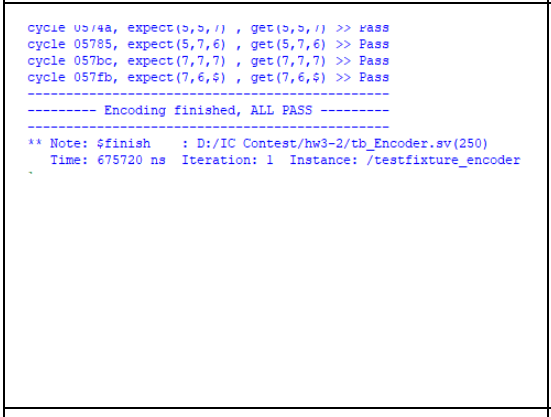
| Functional simulation | Pass (encoder) | Pass (decoder) | Gate-level simulation | Pass (encoder) | Pass (decoder) |
|---|---|---|---|---|---|

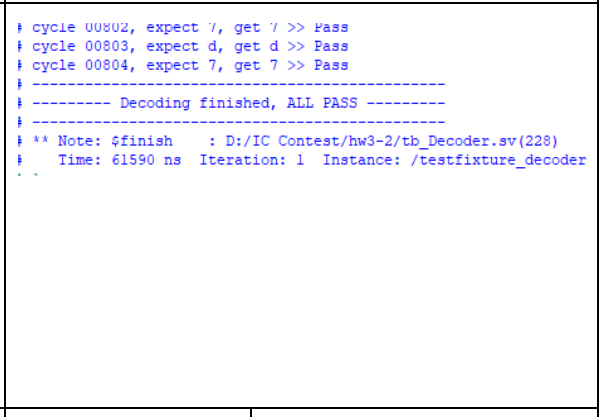


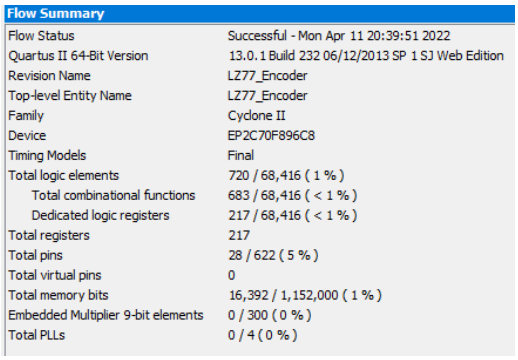



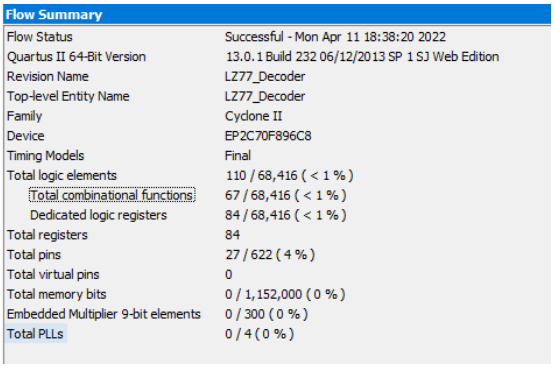




| Synthesis Result | encoder | decoder |
|---|---|---|
| Total logic elements | 720 | 110 |
| Total memory bit | 16392 | 0 |
| Embedded multiplier 9-bit element | 0 | 0 |

| | | |
|---|---|---|
| Simulation time img0 | 1321260 | 61590 |
| Simulation time img1 | 1265250 | 61620 |
| Simulation time img2 | 675720 | 61590 |



| Flow Summary | |
|---|---|
| Flow Status | Successful - Mon Apr 11 20:39:51 2022 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition |
| Revision Name | LZ77_Encoder |
| Top-level Entity Name | LZ77_Encoder |
| Family | Cyclone II |
| Device | EP2C70F896C8 |
| Timing Models | Final |
| Total logic elements | 720 / 68,416 ( 1 % ) |
| Total combinational functions | 683 / 68,416 ( < 1 % ) |
| Dedicated logic registers | 217 / 68,416 ( < 1 % ) |
| Total registers | 217 |
| Total pins | 28 / 622 ( 5 % ) |
| Total virtual pins | 0 |
| Total memory bits | 16,392 / 1,152,000 ( 1 % ) |
| Embedded Multiplier 9-bit elements | 0 / 300 ( 0 % ) |
| Total PLLs | 0 / 4 ( 0 % ) |



| Flow Summary | |
|---|---|
| Flow Status | Successful - Mon Apr 11 18:38:20 2022 |
| Quartus II 64-Bit Version | 13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition |
| Revision Name | LZ77_Decoder |
| Top-level Entity Name | LZ77_Decoder |
| Family | Cyclone II |
| Device | EP2C70F896C8 |
| Timing Models | Final |
| Total logic elements | 110 / 68,416 ( < 1 % ) |
| Total combinational functions | 67 / 68,416 ( < 1 % ) |
| Dedicated logic registers | 84 / 68,416 ( < 1 % ) |
| Total registers | 84 |
| Total pins | 27 / 622 ( 4 % ) |
| Total virtual pins | 0 |
| Total memory bits | 0 / 1,152,000 ( 0 % ) |
| Embedded Multiplier 9-bit elements | 0 / 300 ( 0 % ) |
| Total PLLs | 0 / 4 ( 0 % ) |

**Description of your design**

Encoder 設計分為 5 步驟 ， 第 1 步讀取 image，第 2 步填滿 lookahead_buffer，第三步找出最長的 match_len、offset 及 char_nxt，第 4 步左移 search_buffer 並將 look_ahead 中對應的字串移到 search_buffe，第 5 步看是否遇到$，有就結束沒有則重新回到第 2 步。

Decoder 每次將 search_buffer 左移一位及 code_len 減 1，並將 search_buffer 填入新的值，若 code_len 不為 0 就填入 search_buffer[code_pos]，若為 0 就填入 char_nxt 同時若 char_data 為$代表結束。

*Scoring = (Total logic elements + total memory bit + 9*embedded multiplier 9-bit element)*