2022 Digital IC Design Homework 2

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Functional Simulation Result

Stage 1	Pass	Stage 2	Pass	Stage 3	Pass

Stage 1

```
# ----------------------
# -- Simulation Start --
# ----------------------
# --stage1 simulation--
#
# Setting1: PASS
#
# Setting2: PASS
#
# Setting3: PASS
#
# Setting4: PASS
#
# Setting5: PASS
#
# Setting6: PASS
#
# Setting7: PASS
#
# Setting8: PASS
#
# Setting9: PASS
#
# Setting10: PASS
#
```

Stage 2

```
# --stage2 simulation--
#
# Setting11: PASS
#
# Setting12: PASS
#
# Setting13: PASS
#
# Setting14: PASS
#
# Setting15: PASS
#
# Setting16: PASS
#
# Setting17: PASS
#
# Setting18: PASS
#
# Setting19: PASS
#
# Setting20: PASS
#
```

Stage 3

```
# --stage3 simulation--
#
# Setting21: PASS
#
# Setting22: PASS
#
# Setting23: PASS
#
# Setting24: PASS
#
# Setting25: PASS
#
# Setting26: PASS
#
# Setting27: PASS
#
# Setting28: PASS
#
# Setting29: PASS
#
# Setting30: PASS
#
# ------------------------------------------------
# --    Simulation finish,  ALL PASS             --
# ------------------------------------------------
# ** Note: $finish    : D:/IC Contest/HW2/file/TLS_tb.sv(205)
#    Time: 97650 ns  Iteration: 1  Instance: /testfixture
```

Description of your design

count 為某燈號經過時間 ， Gtime,Ytime,Rtime 為各燈號持續時間

採用 2C1S 的設計模式 ， State Register 根據 clk 正源來改變 State,count,Gtime,Ytime,Rtime 這些需要記憶功能的 reg ， Next State Logic 根據 State 及 count 改變 NextState ， Output Logic 根據 State 改變 Gout,Yout,Rout 作為輸出。