

## 2022 Digital IC Design Homework 3

NAME	歐禮寬				
Student ID	F74074122				
Simulation Result					
Functional simulation	Pass (encoder)	Pass (decoder)	Gate-level simulation	Pass (encoder)	Pass (decoder)
<pre>cycle 0ab87, expect(7,7,8) , get(7,7,8) &gt;&gt; Pass cycle 0abca, expect(7,7,8) , get(7,7,8) &gt;&gt; Pass cycle 0ac09, expect(7,6,6) , get(7,6,6) &gt;&gt; Pass ----- Encoding finished, ALL PASS ----- ** Note: \$finish      : D:/IC Contest/hw3-2/tb_Encoder.sv(250)    Time: 1321260 ns  Iteration: 1  Instance: /testfixture_encoder </pre>			<pre>cycle 00802, expect 8, get 8 &gt;&gt; Pass cycle 00803, expect 0, get 0 &gt;&gt; Pass cycle 00804, expect 8, get 8 &gt;&gt; Pass ----- Decoding finished, ALL PASS ----- ** Note: \$finish      : D:/IC Contest/hw3-2/tb_Decoder.sv(228)    Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder </pre>		
<pre>cycle 0a470, expect(3,2,1) , get(3,2,1) &gt;&gt; Pass cycle 0a498, expect(0,0,6) , get(0,0,6) &gt;&gt; Pass cycle 0a4be, expect(0,0,6) , get(0,0,6) &gt;&gt; Pass ----- Encoding finished, ALL PASS ----- ** Note: \$finish      : D:/IC Contest/hw3-2/tb_Encoder.sv(250)    Time: 1265250 ns  Iteration: 1  Instance: /testfixture_encoder </pre>			<pre>cycle 00803, expect 1, get 1 // Pass == Decoding string "6" cycle 00804, expect 6, get 6 &gt;&gt; Pass ----- Decoding finished, ALL PASS ----- ** Note: \$finish      : D:/IC Contest/hw3-2/tb_Decoder.sv(228)    Time: 61620 ns  Iteration: 1  Instance: /testfixture_decoder </pre>		
<pre>cycle 0b7ea, expect(5,5,1) , get(5,5,1) &gt;&gt; Pass cycle 05785, expect(5,7,6) , get(5,7,6) &gt;&gt; Pass cycle 057bc, expect(7,7,7) , get(7,7,7) &gt;&gt; Pass cycle 057fb, expect(7,6,6) , get(7,6,6) &gt;&gt; Pass ----- Encoding finished, ALL PASS ----- ** Note: \$finish      : D:/IC Contest/hw3-2/tb_Encoder.sv(250)    Time: 675720 ns  Iteration: 1  Instance: /testfixture_encoder </pre>			<pre># cycle 00802, expect 7, get 7 &gt;&gt; Pass # cycle 00803, expect d, get d &gt;&gt; Pass # cycle 00804, expect 7, get 7 &gt;&gt; Pass # ----- Decoding finished, ALL PASS ----- # ** Note: \$finish      : D:/IC Contest/hw3-2/tb_Decoder.sv(228) #   Time: 61590 ns  Iteration: 1  Instance: /testfixture_decoder </pre>		
Synthesis Result			encoder	decoder	
Total logic elements			720	110	
Total memory bit			16392	0	
Embedded multiplier 9-bit element			0	0	

Simulation time img0	1321260	61590
Simulation time img1	1265250	61620
Simulation time img2	675720	61590
<div><div>Flow Summary</div><div><div>Flow Status</div><div>Successful - Mon Apr 11 20:39:51 2022</div><div>Quartus II 64-Bit Version</div><div>13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition</div><div>Revision Name</div><div>LZ77_Encoder</div><div>Top-level Entity Name</div><div>LZ77_Encoder</div><div>Family</div><div>Cyclone II</div><div>Device</div><div>EP2C70F896C8</div><div>Timing Models</div><div>Final</div><div>Total logic elements</div><div>720 / 68,416 ( 1 % )</div><div><div>Total combinational functions</div><div>683 / 68,416 ( &lt; 1 % )</div></div><div><div>Dedicated logic registers</div><div>217 / 68,416 ( &lt; 1 % )</div></div><div>Total registers</div><div>217</div><div>Total pins</div><div>28 / 622 ( 5 % )</div><div>Total virtual pins</div><div>0</div><div>Total memory bits</div><div>16,392 / 1,152,000 ( 1 % )</div><div>Embedded Multiplier 9-bit elements</div><div>0 / 300 ( 0 % )</div><div>Total PLLs</div><div>0 / 4 ( 0 % )</div></div></div>	<div><div>Flow Summary</div><div><div>Flow Status</div><div>Successful - Mon Apr 11 18:38:20 2022</div><div>Quartus II 64-Bit Version</div><div>13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition</div><div>Revision Name</div><div>LZ77_Decoder</div><div>Top-level Entity Name</div><div>LZ77_Decoder</div><div>Family</div><div>Cyclone II</div><div>Device</div><div>EP2C70F896C8</div><div>Timing Models</div><div>Final</div><div>Total logic elements</div><div>110 / 68,416 ( &lt; 1 % )</div><div><div>Total combinational functions</div><div>67 / 68,416 ( &lt; 1 % )</div></div><div><div>Dedicated logic registers</div><div>84 / 68,416 ( &lt; 1 % )</div></div><div>Total registers</div><div>84</div><div>Total pins</div><div>27 / 622 ( 4 % )</div><div>Total virtual pins</div><div>0</div><div>Total memory bits</div><div>0 / 1,152,000 ( 0 % )</div><div>Embedded Multiplier 9-bit elements</div><div>0 / 300 ( 0 % )</div><div>Total PLLs</div><div>0 / 4 ( 0 % )</div></div></div>	
<div>Description of your design</div> <div><div>Encoder 設計分為 5 步驟 ， 第 1 步讀取 image，第 2 步填滿 lookahead_buffer，第三步找出最長的 match_len、offset 及 char_nxt，第 4 步左移 search_buffer 並將 look_ahead 中對應的字串移到 search_buffe，第 5 步看是否遇到\$，有就結束沒有則重新回到第 2 步。</div><div>Decoder 每次將 search_buffer 左移一位及 code_len 減 1，並將 search_buffer 填入新的值，若 code_len 不為 0 就填入 search_buffer[code_pos]，若為 0 就填入 char_nxt 同時若 char_data 為\$代表結束。</div></div>		

*Scoring = (Total logic elements + total memory bit + 9\*embedded multiplier 9-bit element)*