UNIVERSITY OF INFORMATION TECHNOLOGY

COMPUTER ENGINEERING DEPARTMENT

FINAL EXAMINATION II (2019-2020)

COURSE: DEGITAL LOGIC DESIGN

Time duration: 70 minutes
(Paper materials are not allowed)
(OEP Students do the test by English, Regular Students do the test by Vietnamese)

1. Question 1: (5 points)

a. What is combinational circuit? Describe 5 combinational circuits

b. What is sequential circuit? Describe 5 sequential circuits

c. Describe 5 memory components

d. What is Register Transfer Logic (RTL) design?

Mục đích chính của thiết kế chức năng theo mô hình pipelined (pipelined functional unit design) là tăng cường hiệu suất bằng cách chia các pha thực hiện của một hoạt động thành các giai đoạn liên tiếp, cho phép xử lý đa nhiệm và chạy các lệnh song song.

e. How can we determine the operation frequency of a design circuit?

f. Compare the disadvantages and advantages between the single cycle design and the multiple cycle design?

g. What is the main purpose of a pipelined functional unit design?

h. What is the main purpose of a pipelined datapath design?

i. What is difference between register sharing technique and register merging technique?

j. What is difference between resource-constraint scheduling and time-constraint scheduling?

2. Question 2: (2 points)

a. Show a Moore-based Finite-state machine (4 states) with datapath (FSDM) architecture of a system design.

b. Show a Mealy-based Finite-state machine (7 states) with datapath (FSDM) architecture of a system design.

3. Question 3 (3 points)

Given: $\text{Sum} = \sum_{i=1}^{200} x_i$

a. Build the datapath to calculate the value of Sum.

b. Show the FSM graph to control the datapath built in (a).

This examination's learning outcomes (LO) (matching to subject syllabus's LO)

Question	LO	Description
1	G4	Ability to comprehend professional materials
2	G1	Ability to analyze finite state machine circuits, data paths, and control units.
3	G2	Ability to design and optimize the circuits use ASM and FSMD models in the design process

---

Approved by Head of Subject **Designed by**