UNIVERSITY OF INFORMATION TECHNOLOGY

COMPUTER ENGINEERING DEPARTMENT

FINAL EXAMINATION II (2021-2022)

COURSE: DEGITAL LOGIC DESIGN

Time duration: 90 minutes
(Paper materials are not allowed)
(OEP Students do the test by English, Regular Students do the test by Vietnamese)

Student only do TEST 1 or TEST2.

TEST 1: Students need only do Question 1. Question 2 is done and reported on class.

1. **Question 1: (4 points)**
    a. Describe 5 memory components
    b. How can we determine the operation frequency of a design circuit?
    c. What is combinational circuit? Describe 5 combinational circuits
    d. What is sequential circuit? Describe 5 sequential circuits
    e. What is Register Transfer Logic (RTL) design? What are the advantages of the RTL design?
    f. What is difference between register sharing technique and register merging technique?
    g. Draw the FSM architecture of Moore model.
    h. Draw the FSM architecture of Mealy model.
    i. What are functions of the datapath?
    j. What are functions of the controller?

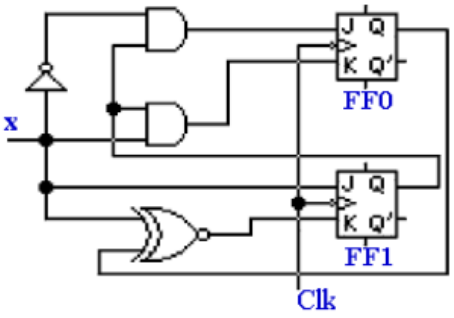
2. **Question 2 (6 points)**

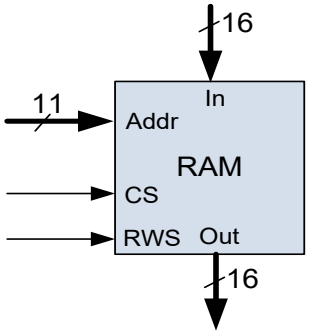
Design RTL circuits and do simulation on the Quartus for Square Root Approximation (SRA) using:

a. Register sharing technique
b. Functional-unit sharing technique. Two shared functional-unit groups, which are (abs/max) and (abs/min/+/-) are used to design.
c. Bus sharing technique.

TEST 2: Students need do all questions of the test

1. **Question 1: (1 point)**
   Analyze the circuit below based on Finite State Machine.





2. **Question 2: (1 point)**
   Design chip RAM 4Kx32 using chip RAM 11x16 as in the image above.

3. **Question 3: (2 points)**
   Design a 4-bit counter that count the following sequence 2, 4, 6, 8, 12, 14. The counter has the Reset function to reset the counter back to 2. Design the Reset function in two cases: a) Synchornous Reset; b) Asynchronous Reset

4. **Question 4: (2 points)**

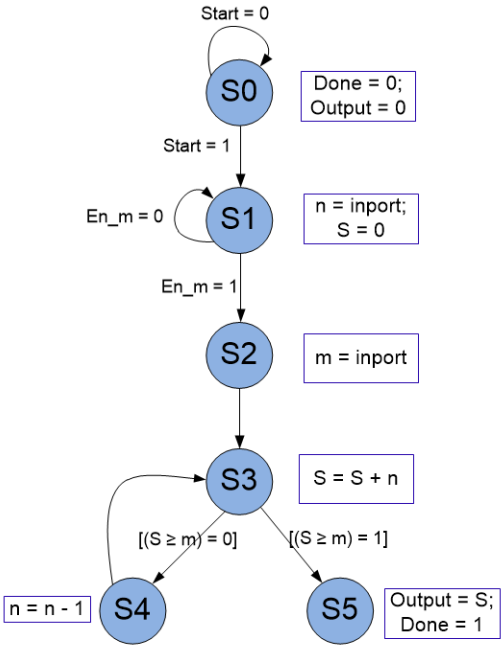
   Let's design below arithmetic operation circuits:

   a. Design a circuit to perform the Absolute operation
   b. Design a circuit to perform the Min/Max operation
   c. Design a shared circuit to perform the Absolute/Subtraction/Max/Min

5. **Question 5: (1.5 points)**
   Instruction set. Let's start the first step to design a simple processor (two-address instructions and an register file) to execute the equation: $z = (y^3 + 3x + 1)(x - 1)^2$, where, x, y are stored in data memory, z is also stored back the data memory after execution:
   a. Describe instructions we need in the instruction set to calculate above equation
   b. Write the sequence of instructions to compute the equation

6. **Question 6: (2.5 points)**
   Given the state transition diagram of a circuit design as in the image.
   a. Derive ASM chart. What is the type of your ASM? (Moore or Mealy)

b. Derive the state-action table.
c. Derive necessary equations to draw the circuit. Assume that states are encoded as natural binary, and D flipflops are used.



This examination's learning outcomes (LO) (matching to subject syllabus's LO)

Question	LO	Description
1	G4	Ability to comprehend professional materials
2	G2	Ability to know analyze the cost and latency of the circuits, use ASM and FSMD models in the design process
3	G1	Ability to analyze finite state machine circuits, data paths, and control units.
4	G2	Ability to to optimize the circuits use ASM and FSMD models in the design process
5	G1	
6	G2	

Approved by Head of Subject **Designed by**