Ho Chi Minh City National University
University of Information Technology
Computer Engineering

Report

Digital Logic Design

Subject: LIFO (Stack)

Class: CE118.P11.2

Instructor: Ta Tri Duc

Performed by students: Truong Thien Quy - 23521321

Ho Chi Minh City, 04/2023

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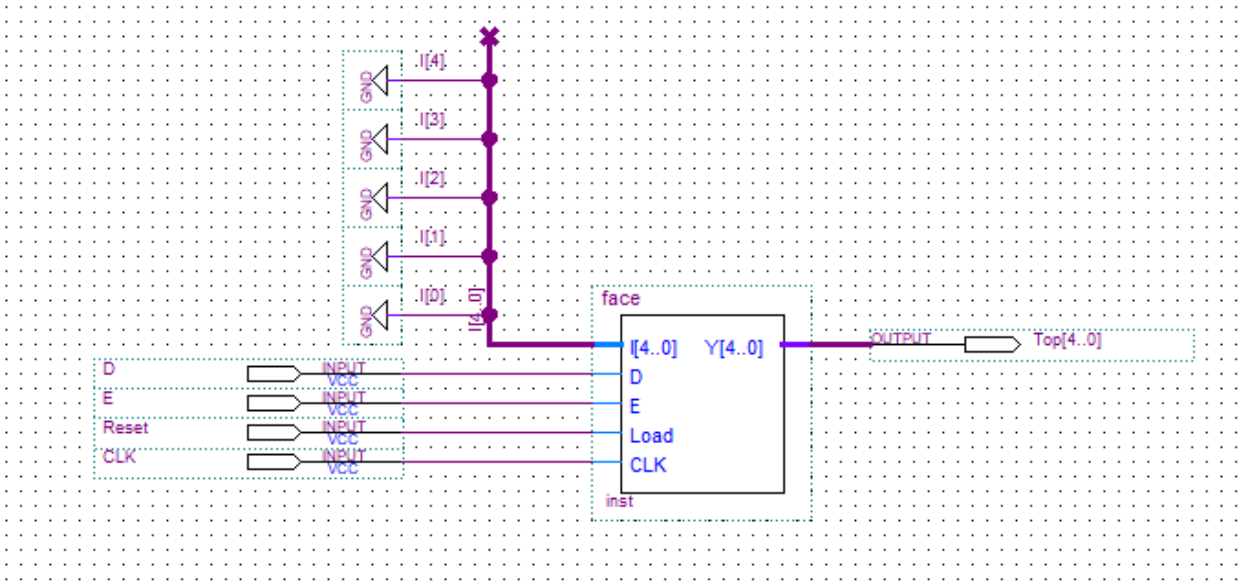
Top: The smallest empty address.



Use Up/down_counter to design the TOP block.

When E=0 it doesn't work

When E = 1:

D = 0: count up (push)

D = 1: count down (pop)

When Reset = 1: Ouput = 00000b

Top-1: The biggest address has data:

Use an Up/down_counter and Sub_00001 block to design the TOP-1 block.

Sub_00001 block is desined by 4 Sub_0 block and 1 Sub_1 block

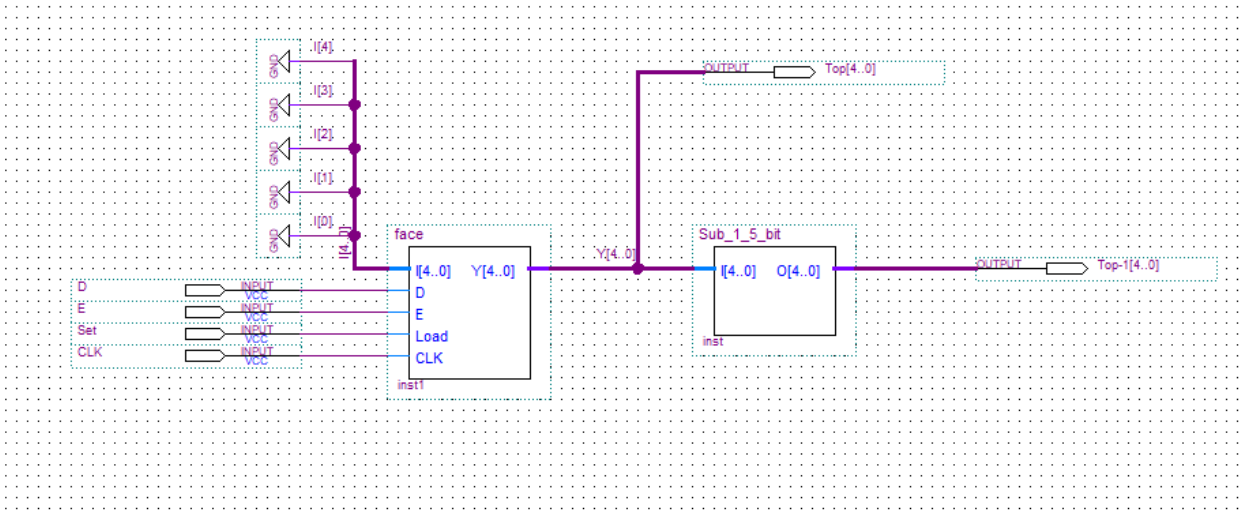
When E=0 it doesn't work

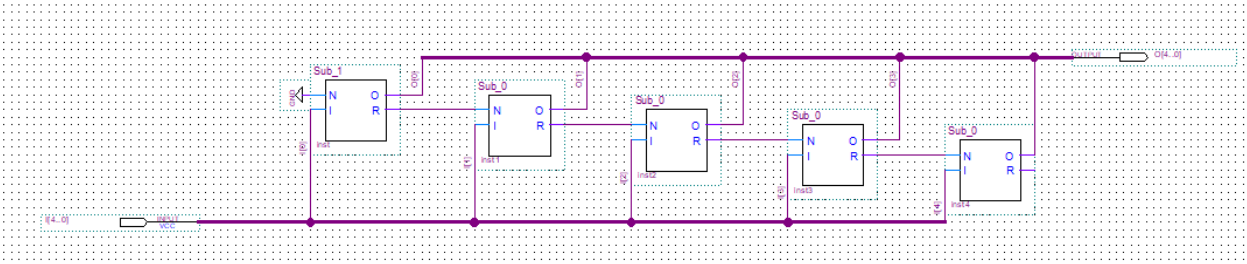
When E = 1:

D = 0: count up (push)

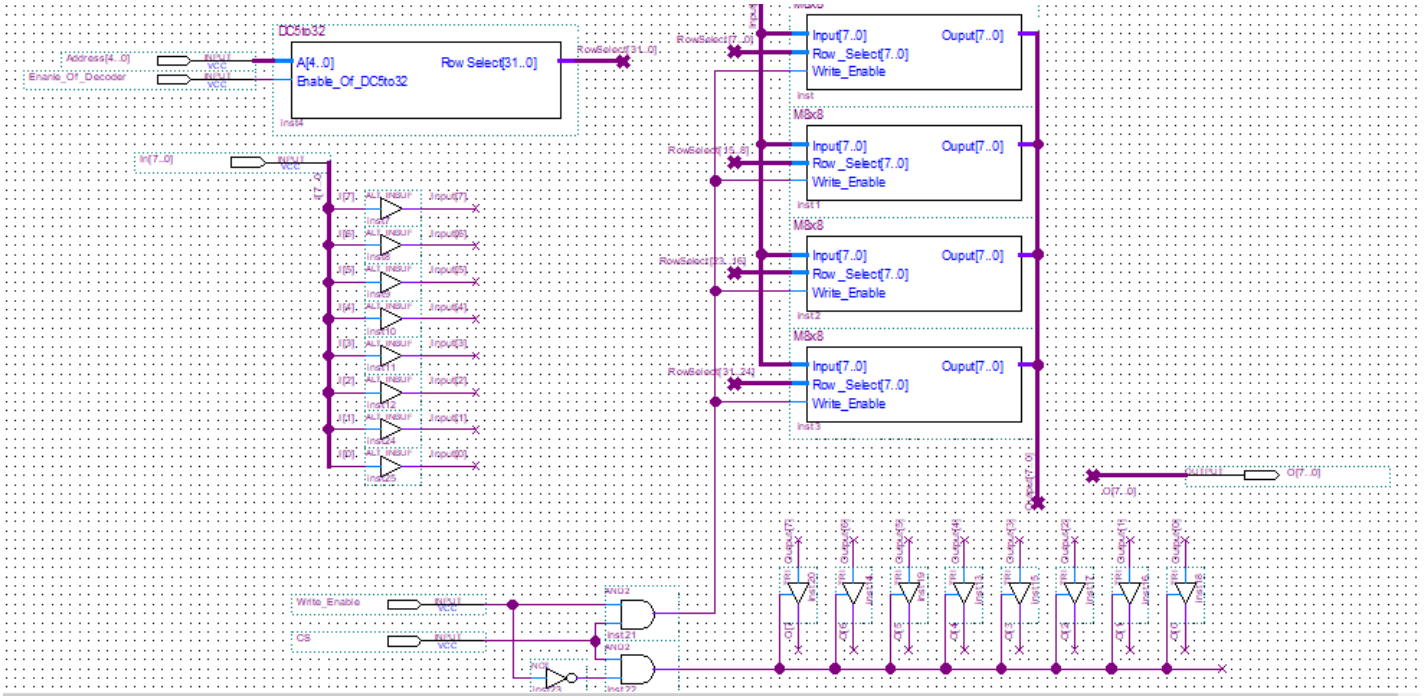
D = 1: count down (pop)

When Reset = 1: Ouput = 11111b





Ram 32x8:



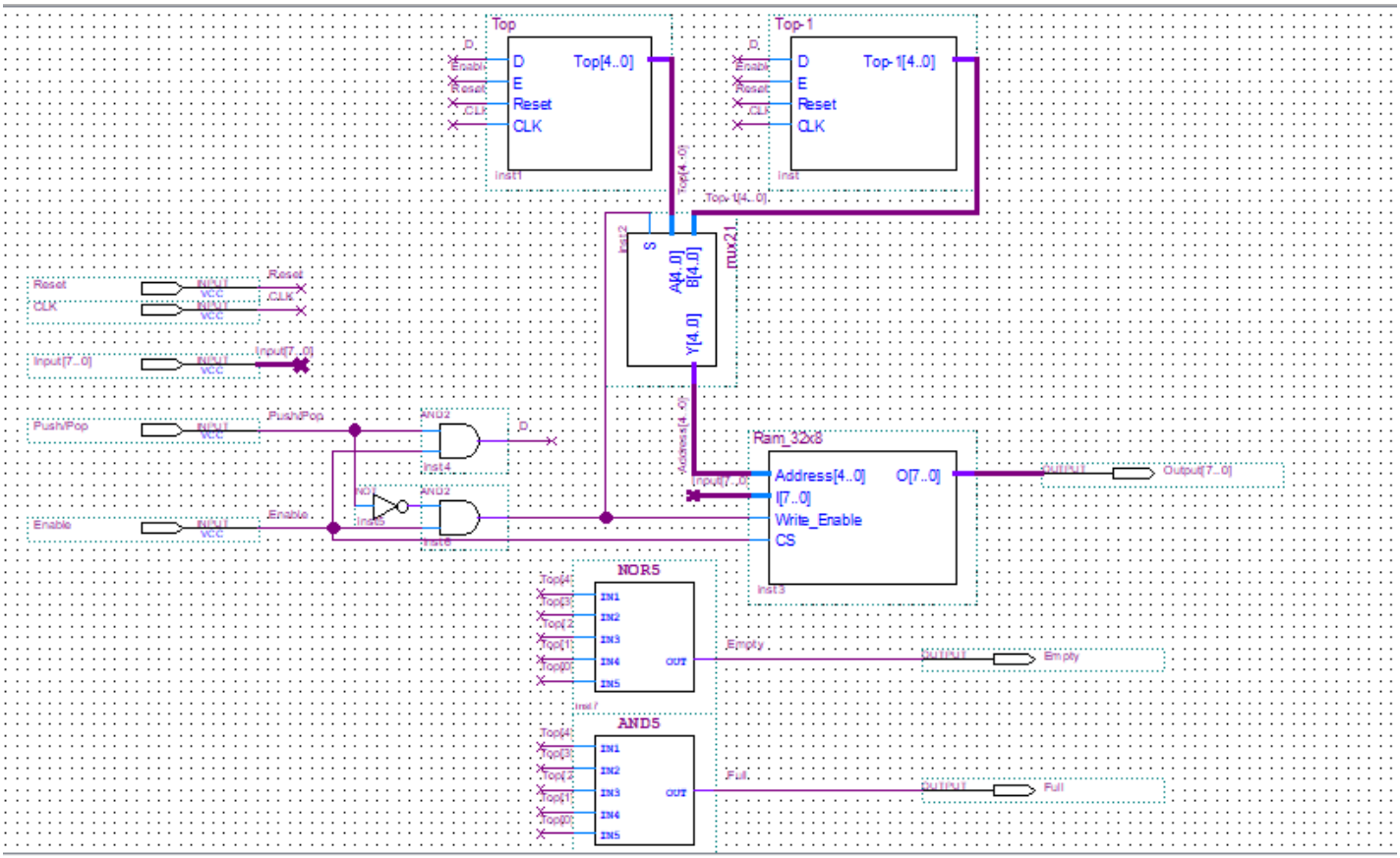
Connecting the 4 blocks of 8x8 designed above, we get a 32x8 block of memory cells.

The I/O signals are in turn connected to the IO buffers due to the CS x (RWS)' signal to control the signals in the read and write states.

The Row_Select pins connect to the 5 to 32 decoder to access the address of each row (register).

RWS x CS input to generate the Write_Enable signal.

Stack:



Push: Data → RAM (*TOP*); Increment Top, Top-1

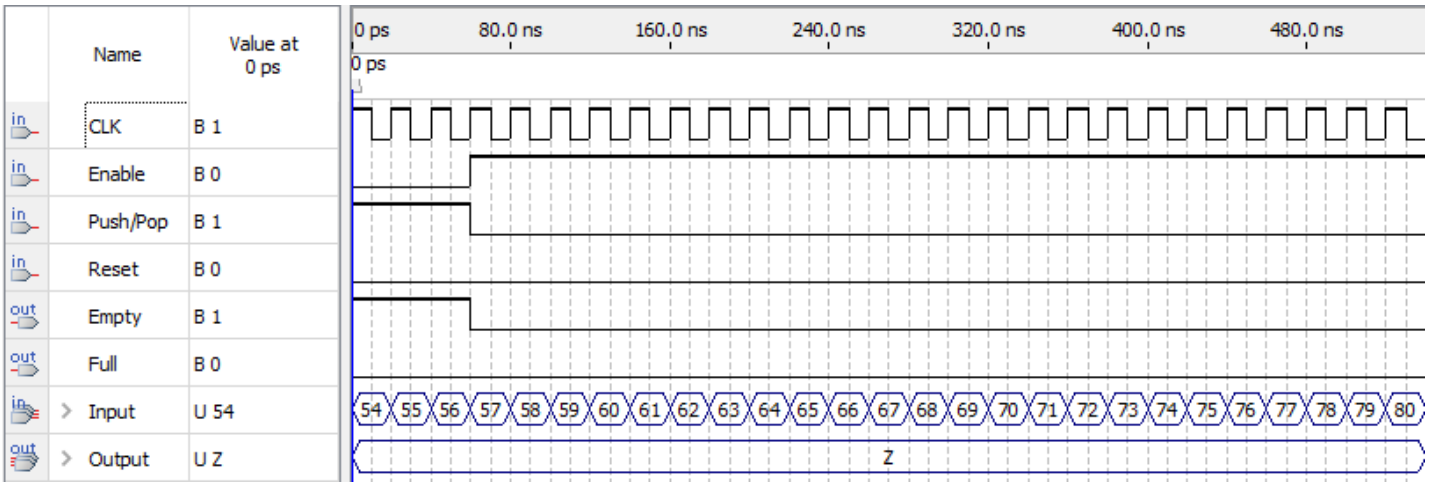
Pop: RAM (*Top-1*) → Data; Decrement Top, Top-1

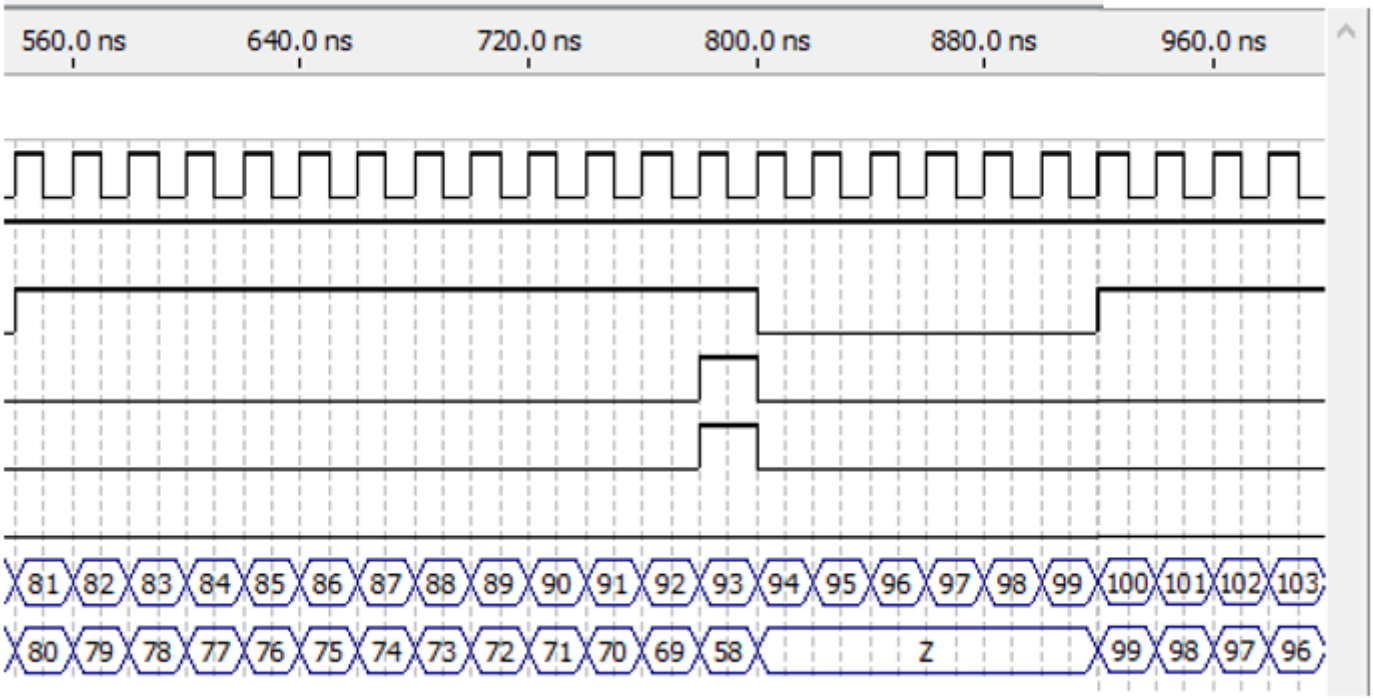
Stack is full when Top=1023

Stack is empty when Top=0

Location with address 1023 is never loaded

Waveform:


Name
Value at 0 ps
CLK
B 1
Enable
B 0
Push/Pop
B 1
Reset
B 0
Empty
B 1
Full
B 0
Input
U 54
Output
U Z
0 ps
80.0 ns
160.0 ns
240.0 ns
320.0 ns
400.0 ns
480.0 ns
0 ps
54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80
Z


560.0 ns
640.0 ns
720.0 ns
800.0 ns
880.0 ns
960.0 ns
81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100 101 102 103
80 79 78 77 76 75 74 73 72 71 70 69 58
Z
99 98 97 96