Ho Chi Minh City National University
University of Information Technology
Computer Engineering

Report

Digital Logic Design

Subject: Encoding B (Prioritized adjacency)

Class: CE118.P11.2

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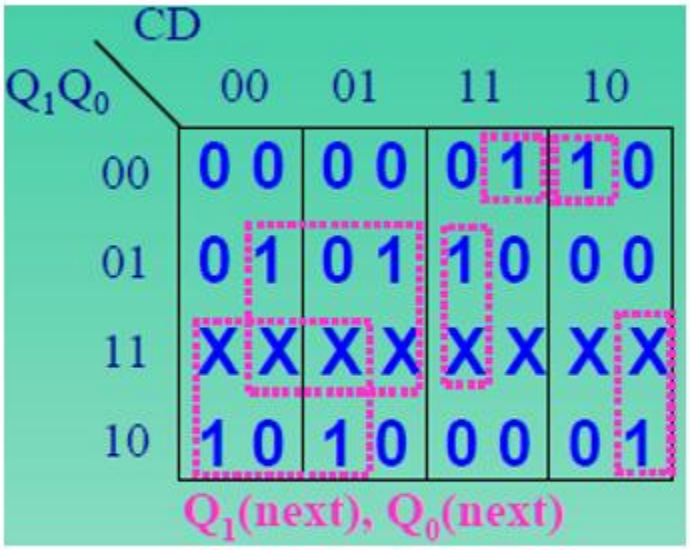
Truth table:

- Next state:

Present State	NEXT STATE		
	CD = 0X	CD = 10	CD = 11
S_0	$S_0/0$	$S_1/0$	$S_2/1$
S_1	$S_1/0$	$S_2/0$	$S_0/0$
S_2	$S_2/0$	$S_0/1$	$S_1/0$

STATE	ENCODING B Q_1Q_0
S_0	0 1
S_1	0 0
S_2	1 0

Next-state map



$$Q_0(next) = Q_0C' + Q_1CD' + Q_1'Q_0'CD$$
$$Q_1(next) = Q_1C' + Q_0CD + Q_1'Q_0'C'D'$$

- JK flipflop: Based on the nextstate-map and truth table of JK flip flop, we draw the truth table of J_0, K_0, J_1, K_1. From there form the expression to draw the circuit.

Q	Q(next)	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

J_0

Q_1 Q_0 \ CD	00	01	11	10
00	0	0	1	0
01	x	x	x	x
11	x	x	x	x
10	0	0	0	1

K_0

Q_1 Q_0 \ CD	00	01	11	10
00	x	x	x	x
01	0	0	1	1
11	x	x	x	x
10	x	x	x	x

$J_0 = Q_1'CD + Q_1CD'$ **$K_0 = C$**

J_1

Q_1 Q_0 \ CD	00	01	11	10
00	0	0	0	1
01	0	0	1	0
11	x	x	x	x
10	x	x	x	x

K_1

Q_1 Q_0 \ CD	00	01	11	10
00	x	x	x	x
01	x	x	x	x
11	x	x	x	x
10	0	0	1	1

$J_1 = Q_0CD + Q_0'CD'$ **$K_1 = C$**

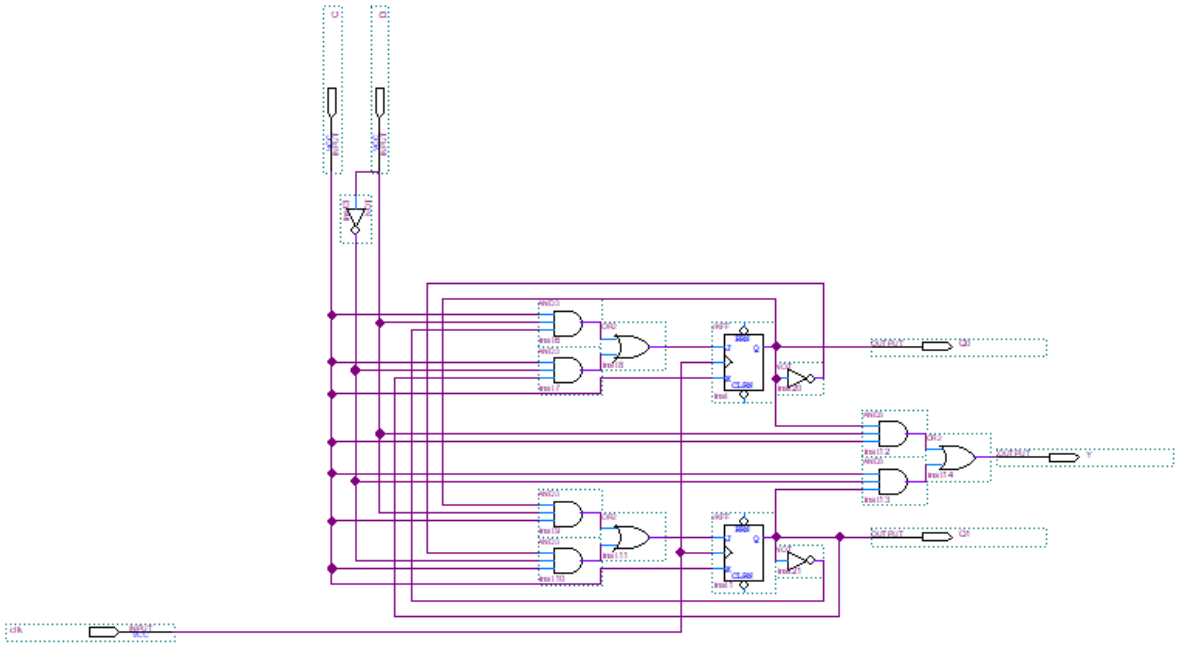
- Output:

Q_1Q_0 \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	0	0	0	1

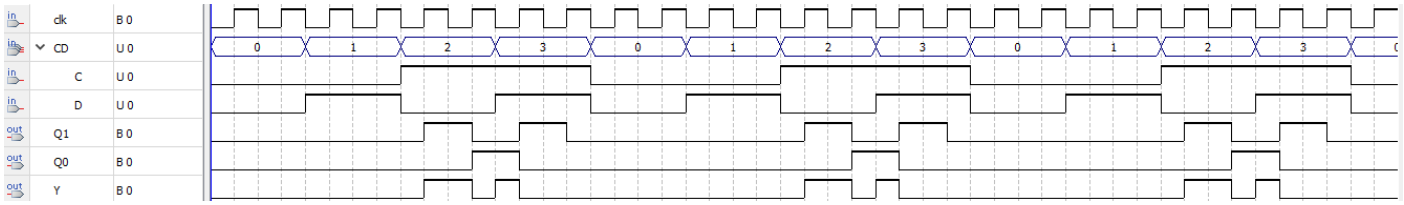
Y

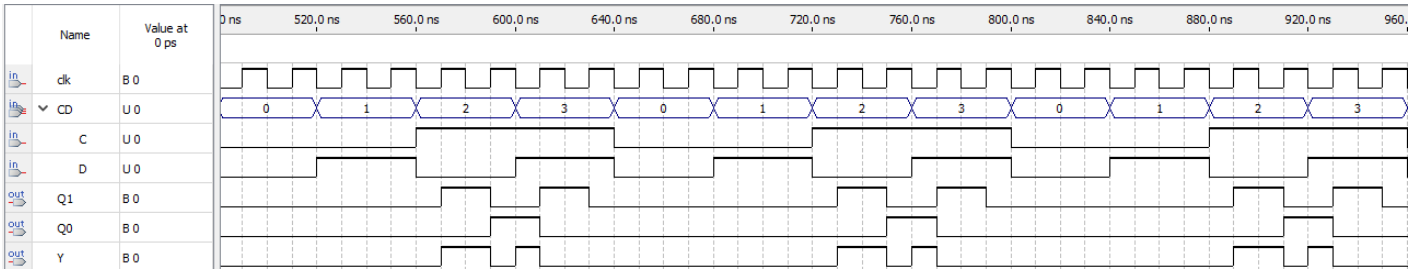
$Y = Q_0CD + Q_1CD'$

Schematic:



Waveform:





Next-state map

Q_1Q_0 \ CD	00	01	11	10
00	0 0	0 0	0 1	1 0
01	0 1	0 1	1 0	0 0
11	X X	X X	X X	X X
10	1 0	1 0	0 0	0 1

Q_1(next), Q_0(next)

$Q_0(next) = Q_0C' + Q_1CD' + Q_1'Q_0'CD$

$Q_1(next) = Q_1C' + Q_0CD + Q_1'Q_0'C'D'$

Based on these 2 tables to check the result of waveform

Q_1Q_0 \ CD	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	X	X	X	X
10	0	0	0	1

Y

$Y = Q_0CD + Q_1CD'$