UNIVERSITY OF INFORMATION TECHNOLOGY

COMPUTER ENGINEERING DEPARTMENT

FINAL EXAMINATION I (2020-2021)

COURSE: DEGITAL LOGIC DESIGN

Time duration: 65 minutes
(Paper materials are not allowed)
(OEP Students do the test by English, Regular Students do the test by Vietnamese)
(Students need only do PART I, PART II has been done on class)

PART I: PAPER TEST

1. Question 1: (2 points)

a. What is Register Transfer Logic (RTL) design?

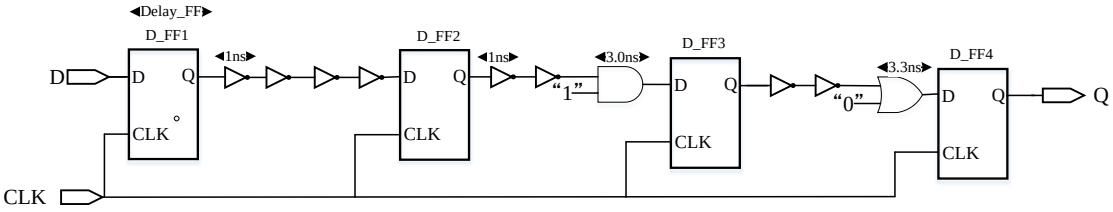
b. Compare the disadvantages and advantages between the single cycle design and the multiple cycle design?

c. What is the main purpose of a pipelined datapath design?

d. What is difference between register sharing technique and register merging technique?

e. What is difference between resource-constraint scheduling and time-constraint scheduling?

2. Question 2: (2 points)



a. Find the clock cycle if the delay of each flipflop (Delay_FF) is 0 ns.

b. Find the clock cycle if the delay of each flipflop (Delay_FF) is 10 ns.

PART II: COMPUTER TEST (DONE)

3. Question 3: (6 points)

Design the arithmetic unit for the square root approximation using both functional unit pipeline and datapath pipeline techniques.

This examination's learning outcomes (LO) (matching to subject syllabus's LO)

Question	LO	Description
1	G4	Ability to comprehend professional materials
2	G1	Ability to analyze finite state machine circuits, data paths, and control units.
3	G2	Ability to design and optimize the circuits use ASM and FSMD models in the design process

Approved by Head of Subject **Designed by**