Ho Chi Minh City National University
University of Information Technology
Computer Engineering

Report

Digital Logic Design

Subject: FIFO (Queue)

Class: CE118.P11.2

Instructor: Ta Tri Duc

Performed by students: Truong Thien Quy - 23521321

Ho Chi Minh City, 04/2023

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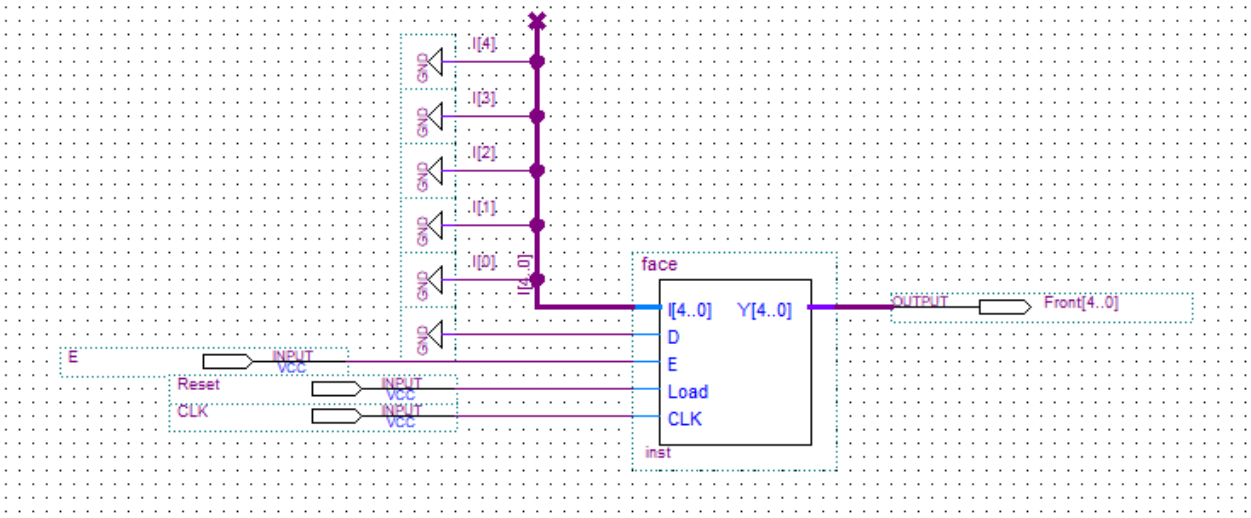
Front:

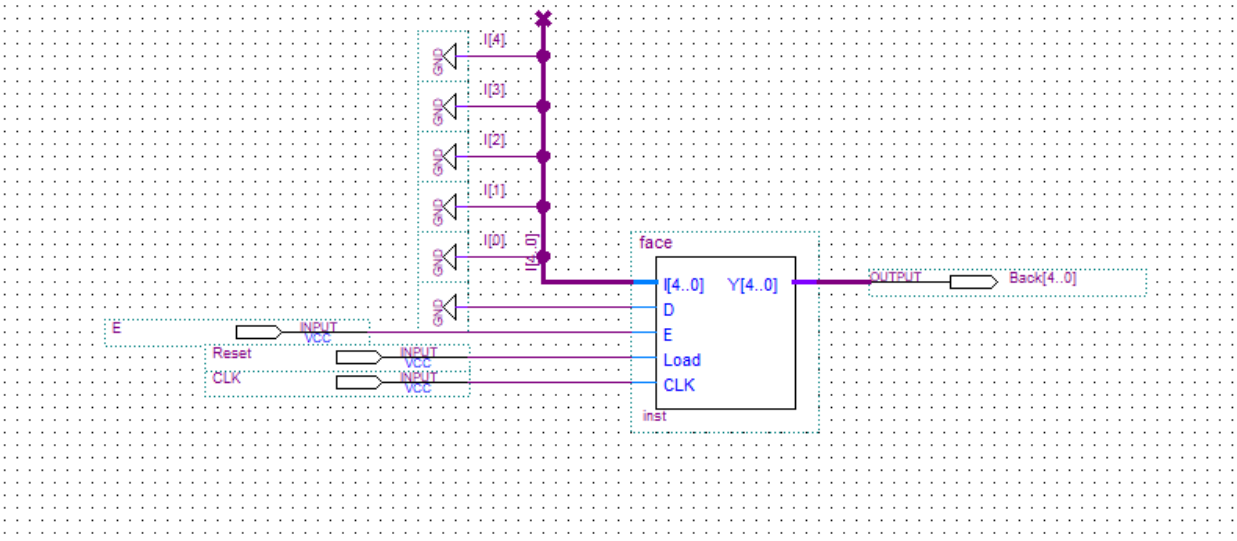


Use Up/down_counter to design the Front block.

Connect D with gnd to allway count up

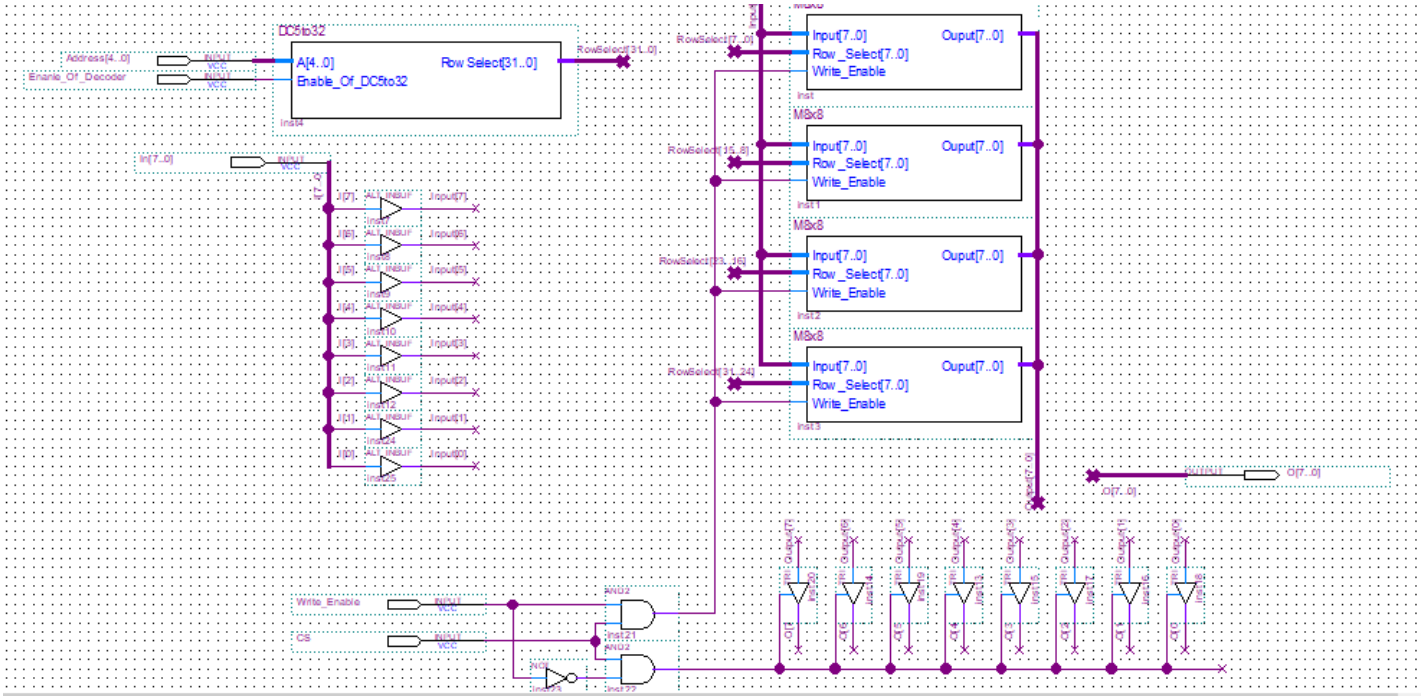
When Reset = 1, Output = 0

Back:



The same with Front

RAM



Connecting the 4 blocks of 8x8 designed above, we get a 32x8 block of memory cells.

The I/O signals are in turn connected to the IO buffers due to the CS x (RWS)' signal to control the signals in the read and write states.

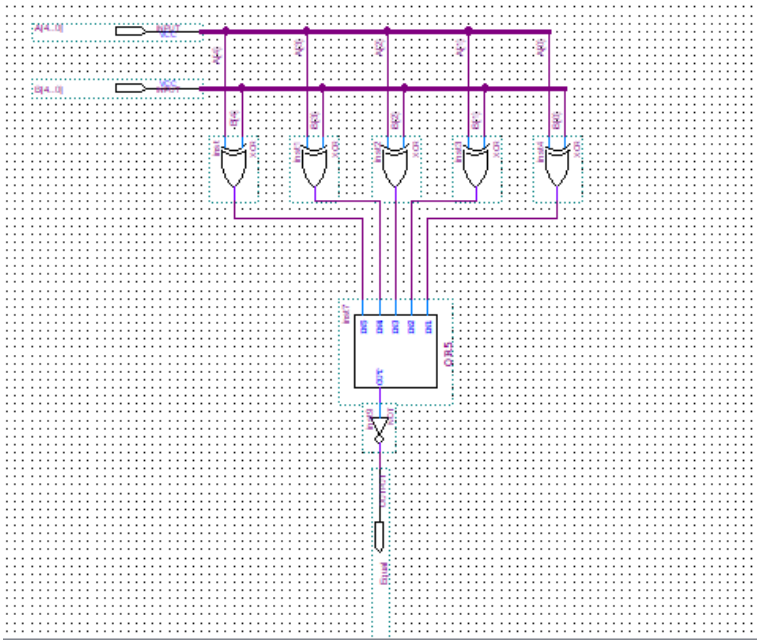
The Row_Select pins connect to the 5 to 32 decoder to access the address of each row (register).

RWS x CS input to generate the Write_Enable signal.

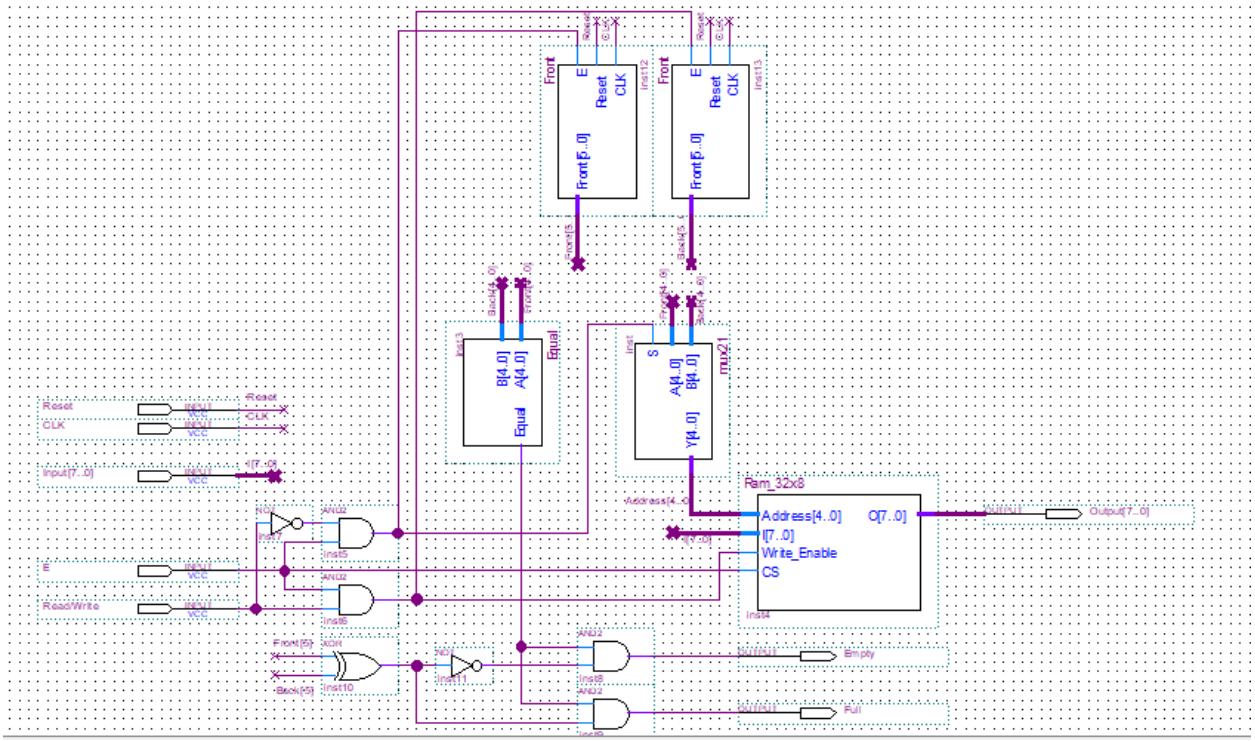
Equal:

Use 5 xor gate and 1 or5 to design Equal block

If A = B, output = 1. Else output = 0



Queue:



Push: Increment Back

Pop: Decrement Front

Using 5 bits, if it contains the same address, it is empty, but the highest bit weight is different, it is full

Waveform: