Ho Chi Minh City National University
University of Information Technology
Computer Engineering

Report

Digital Logic Design

Subject: Random Access Memory (RAM)

Class: CE118.P11.2

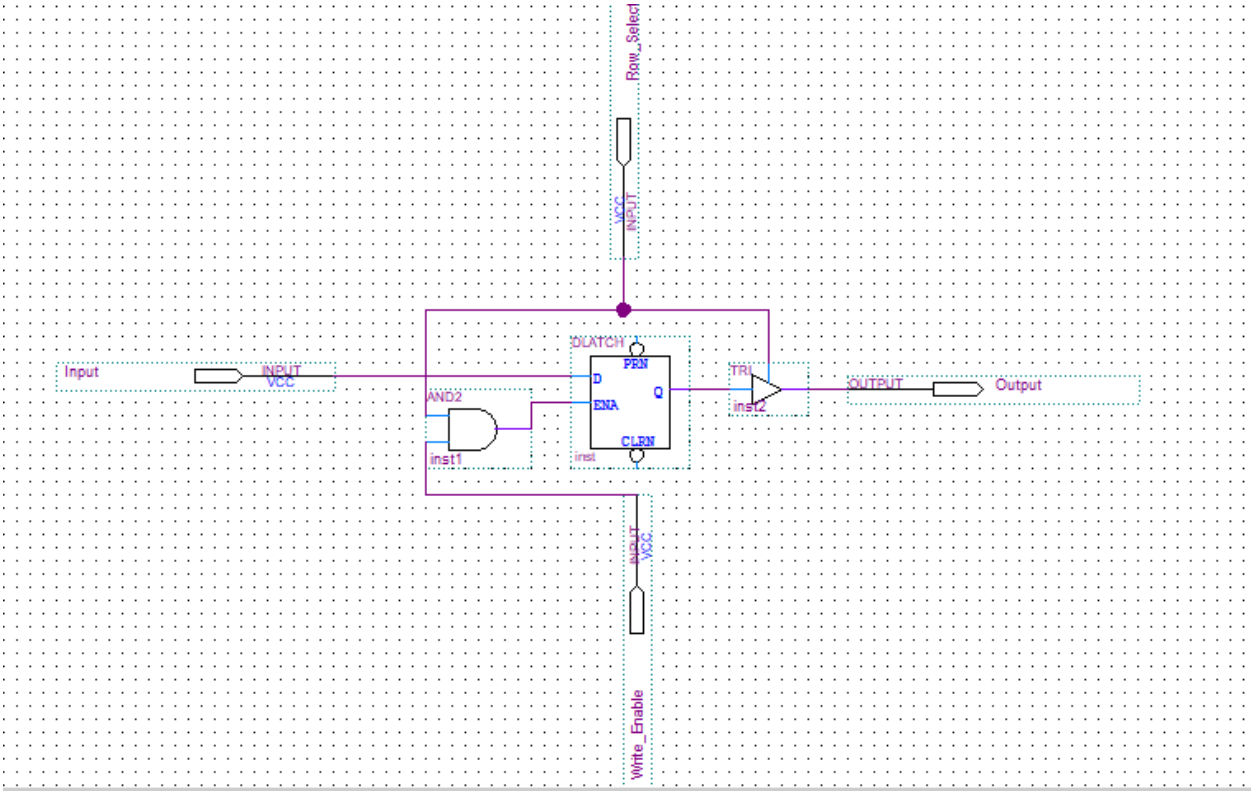
Instructor: Ta Tri Duc

Performed by students: Trương Thiên Quý

Ho Chi Minh City, 03/2024

Table of contents: Page

Memory cell:



Memory cell (MC) is the smallest unit used to store data in RAM.

In this design use D-latch. Buffer tri is used to control the output of MC.

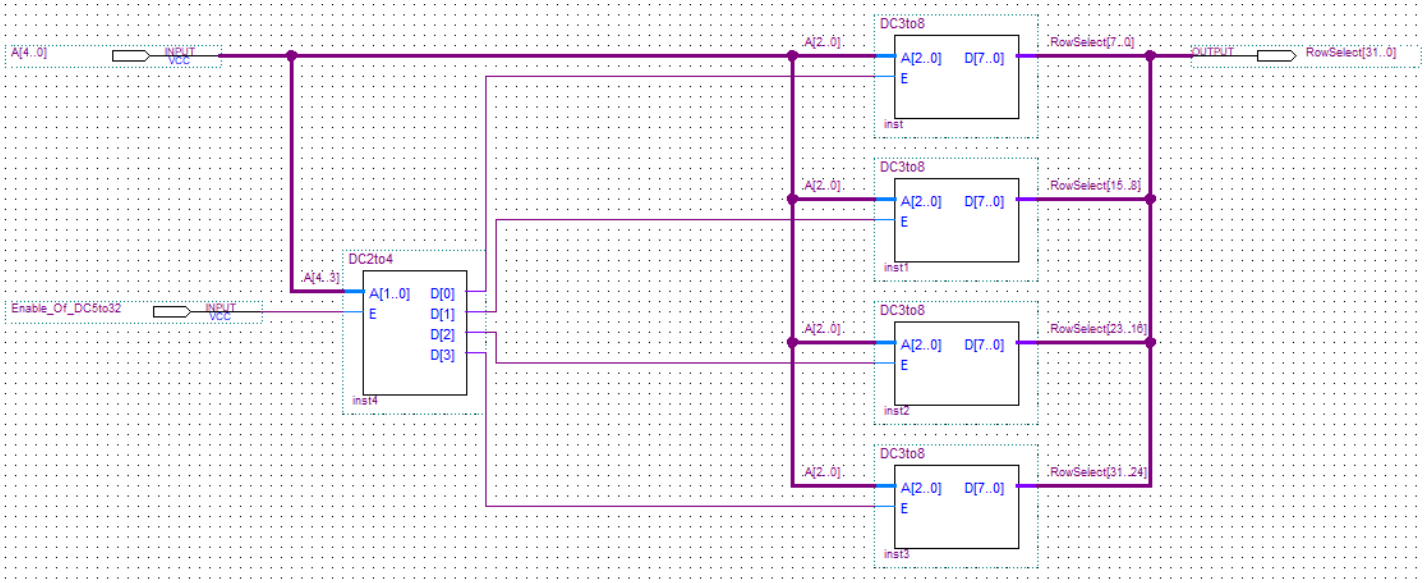
The input Row_Select connected to the buffer controls the output of the MC. Combined with Write_Enable to control read and write state.

8x8 Memory cell:

For convenient to design, we create a block of 8x8 memory cells with 64 MC.

The input and output signals still remain.

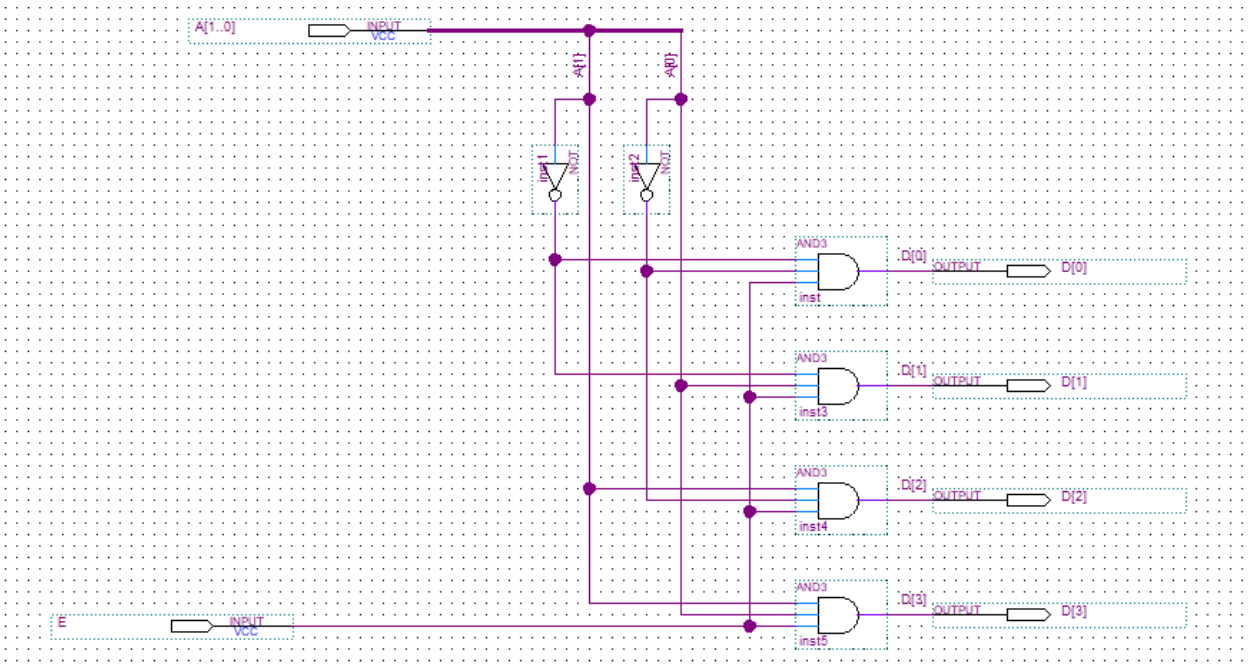
Decoder 5 to 32:



To control the registers through the Row_select signal, we use the decoder 5 to 32. Thus, the Ram bar will now have 32 addresses represented by 5 bits.

Components of decoder 5 to 32: We design decoder 5 to 32 with 4 decoders 3 to 8 and will control them with 1 decoder 2 to 4 as shown above:

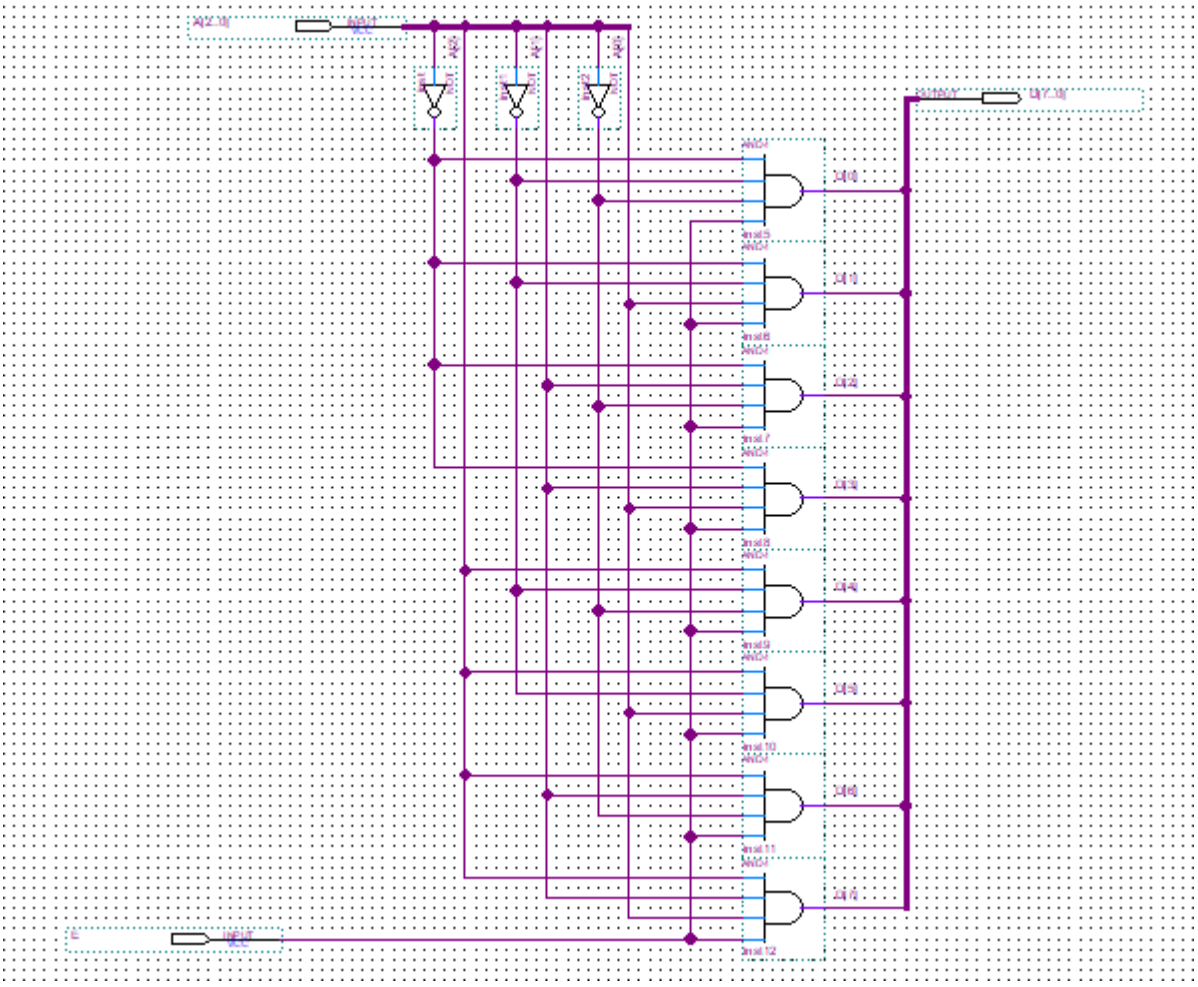
Decoder 2 to 4:



Truth table:

Input				Output			
E	A1	A0		D3	D2	D1	D0
0	x	x		0	0	0	0
1	0	0		0	0	0	1
1	0	1		0	0	1	0
1	1	1		0	1	0	0
1	1	0		1	0	0	0

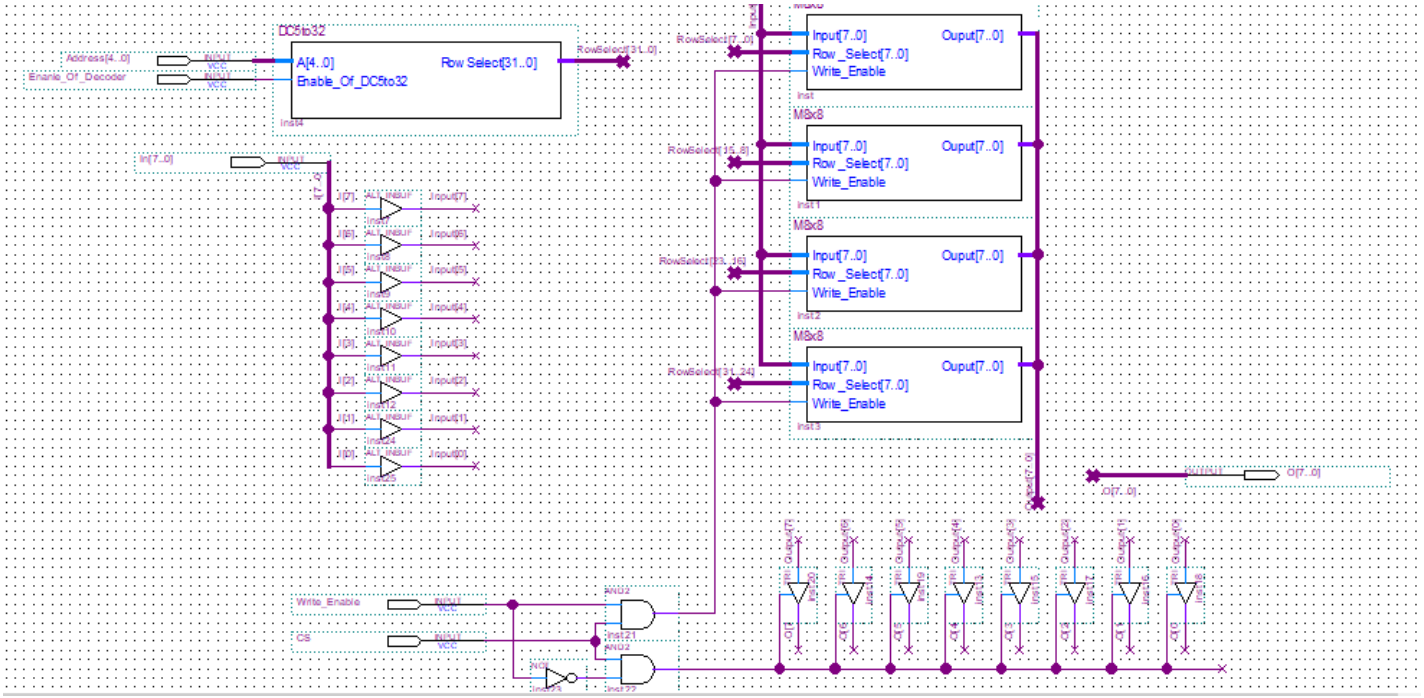
Decoder 3 to 8:



Truth table:

Input					Output							
E	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
0	x	x	x		0	0	0	0	0	0	0	0
1	0	0	0		0	0	0	0	0	0	0	1
1	0	0	1		0	0	0	0	0	0	1	0
1	0	1	1		0	0	0	0	0	1	0	0
1	0	1	0		0	0	0	0	1	0	0	0
1	1	0	0		0	0	0	1	0	0	0	0
1	1	0	1		0	0	1	0	0	0	0	0
1	1	1	1		0	1	0	0	0	0	0	0
1	1	1	0		1	0	0	0	0	0	0	0

Ram 32x8:



Connecting the 4 blocks of 8x8 designed above, we get a 32x8 block of memory cells.

The I/O signals are in turn connected to the IO buffers due to the CS x (RWS)' signal to control the signals in the read and write states.

The Row_Select pins connect to the 5 to 32 decoder to access the address of each row (register).

RWS x CS input to generate the Write_Enable signal.

Waveform: