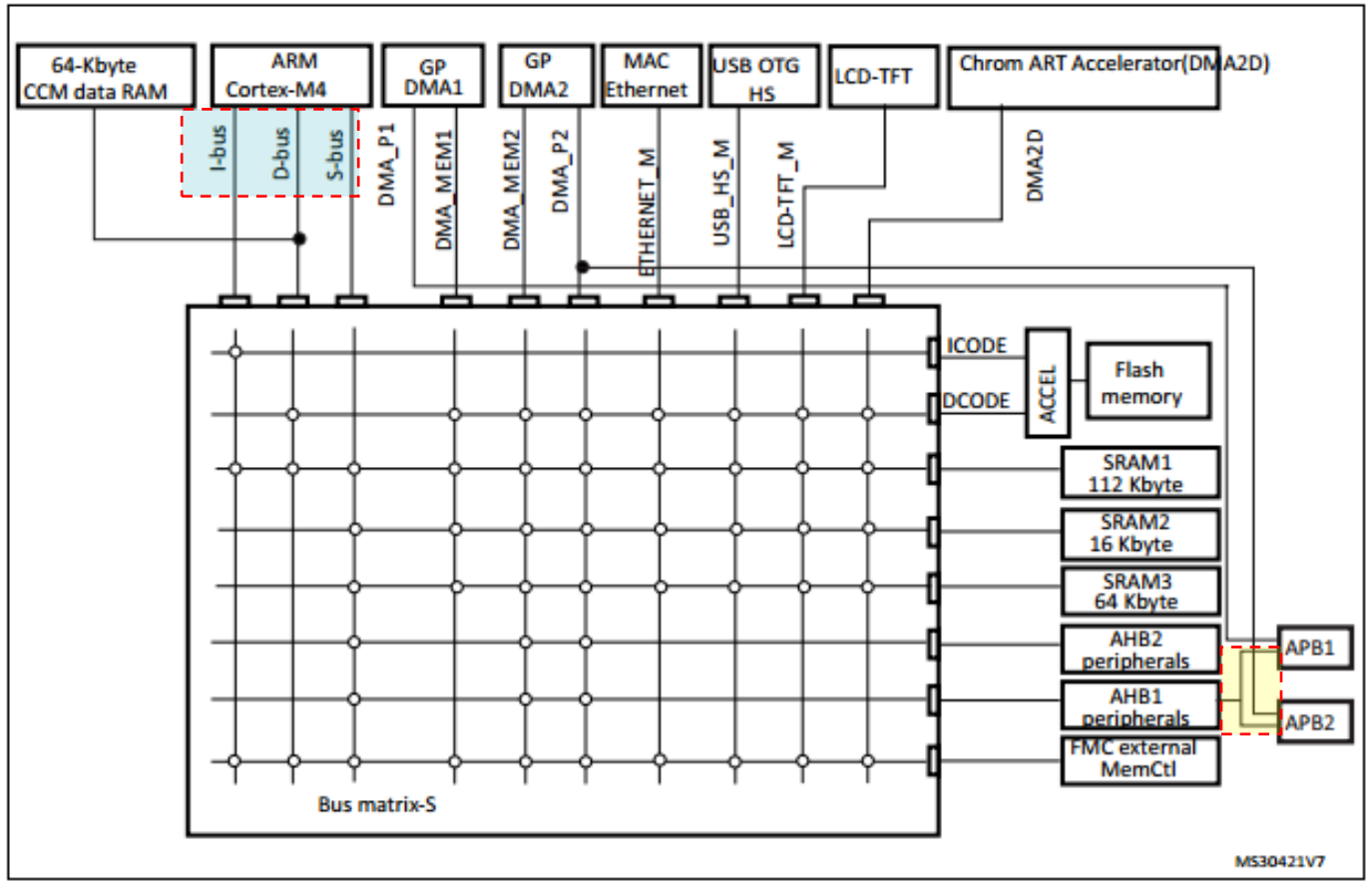
Clocking

05 Oct 2024

OUTLINE

1. Bus architecture
2. Clock Distribution
    - 2.1. HSE - High Speed External
    - 2.2. PLL - Phase Locked Loop
    - 2.3. System Clock
    - 2.4. MCO – uC Clock Output
3. Assignments

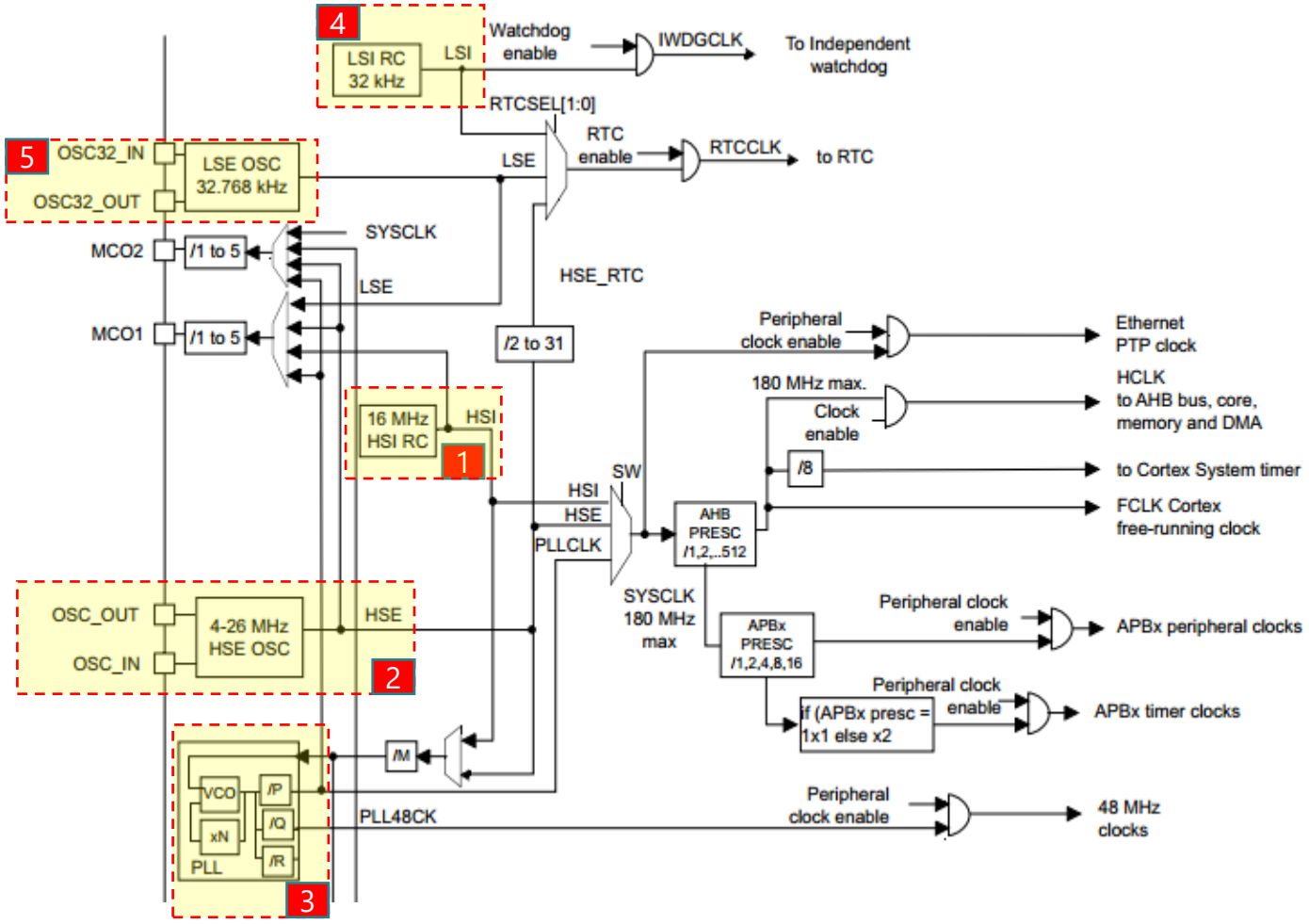
1. Bus architecture



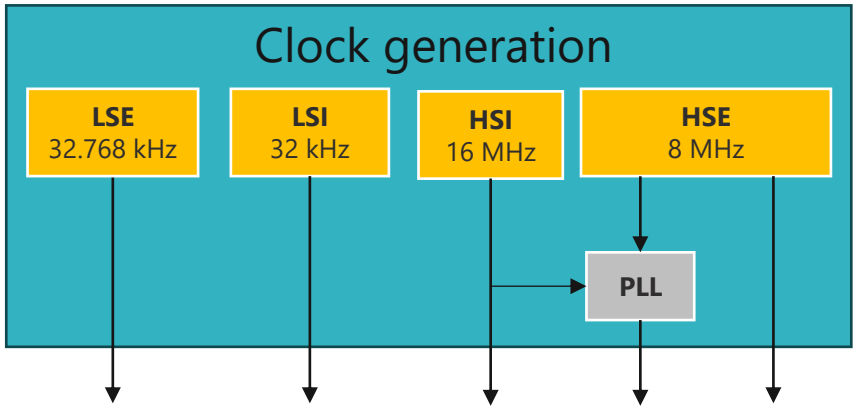
No.	Bus	Description
1	I-bus	Instruction bus - Fetch instructions
2	D-bus	Data bus - Literal load and debug access
3	S-bus	System bus - Access data located in a peripheral or in SRAM. - Instructions may also be fetched on this bus.

No.	Comp.	Description
1	BusMatrix	Manages the access arbitration between masters
2	AHB/APB bridges *Advanced High-performance Bus* *Advanced Peripheral Bus*	Provide full synchronous connections between the AHB and the two APB buses, allowing flexible selection of the peripheral frequency. After each device reset, all peripheral clocks are disabled

2. Clock Distribution



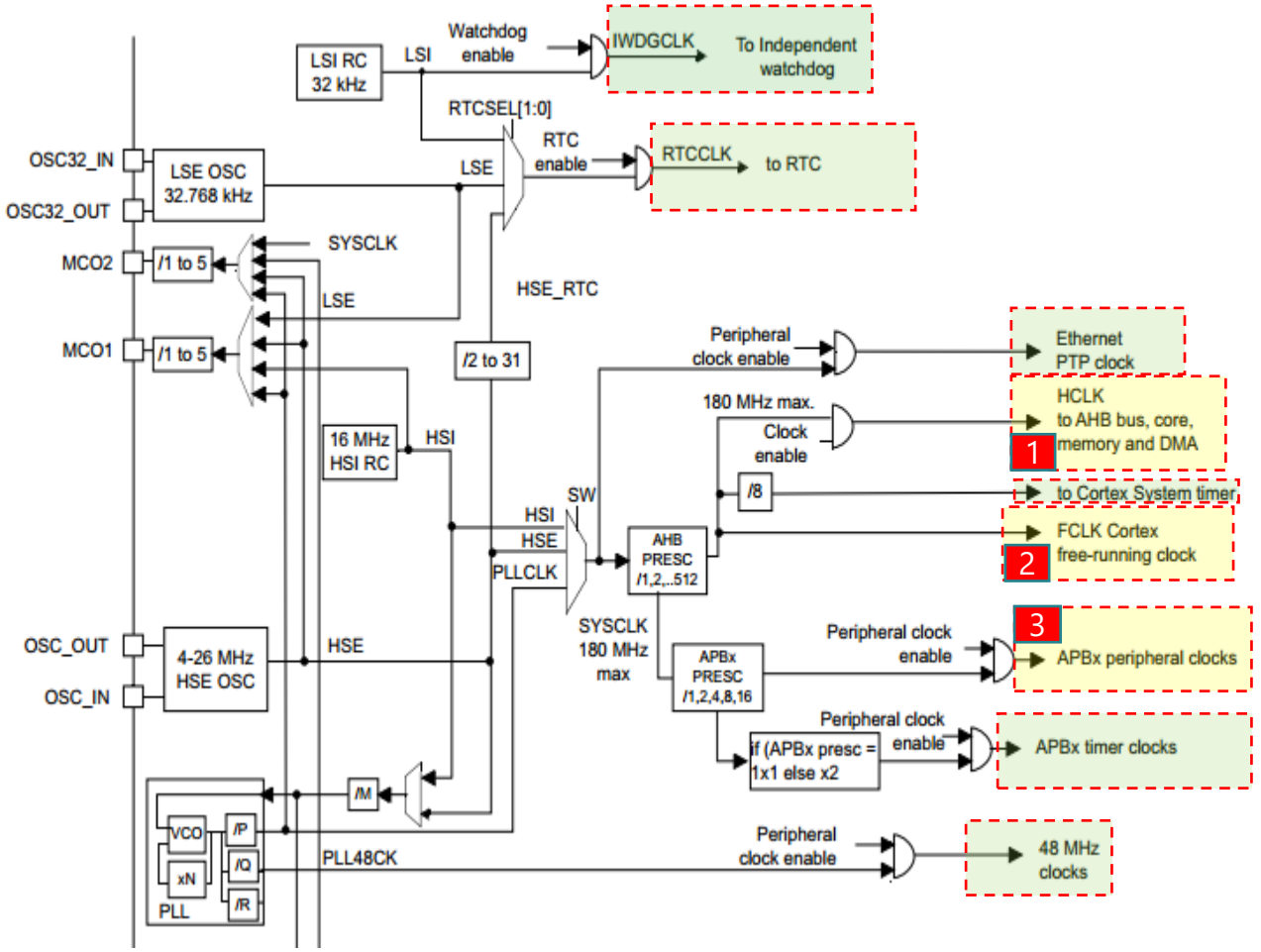
Clocking diagram



Input Clock Source :

No	Clock
1	HSI – High Speed Internal
2	HSE – High Speed External
3	PLL – Phase Locked Loop
4	LSI RC - Low Speed Internal
5	LSE – Low Speed External crysta

2. Clock Distribution



Clocking diagram

Output Clock Sources :

No.	Clock	Description
1	HCLK	Clock to AHB, core, memory
2	FCLK	Clock the Cortex
3	APBx_CLK	Clocks the chip peripherals

2.1. HSE - High Speed External

Initialize HSE – High Speed External:

RCC clock control register (RCC_CR)

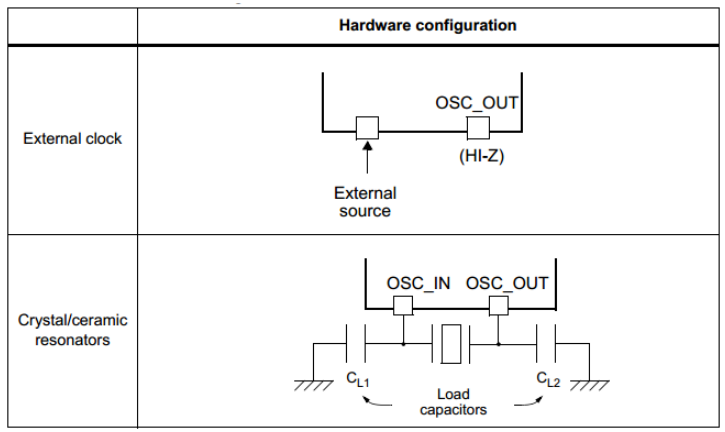
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Reserved		PLLSAIRDY	PLLSAION	PLLI2SRDY	PLLI2SON	PLLRDY	PLLON	Reserved				CSSON	HSEBYP	HSERDY	HSEON
		r	rw	r	rw	r	rw					rw	rw	r	rw

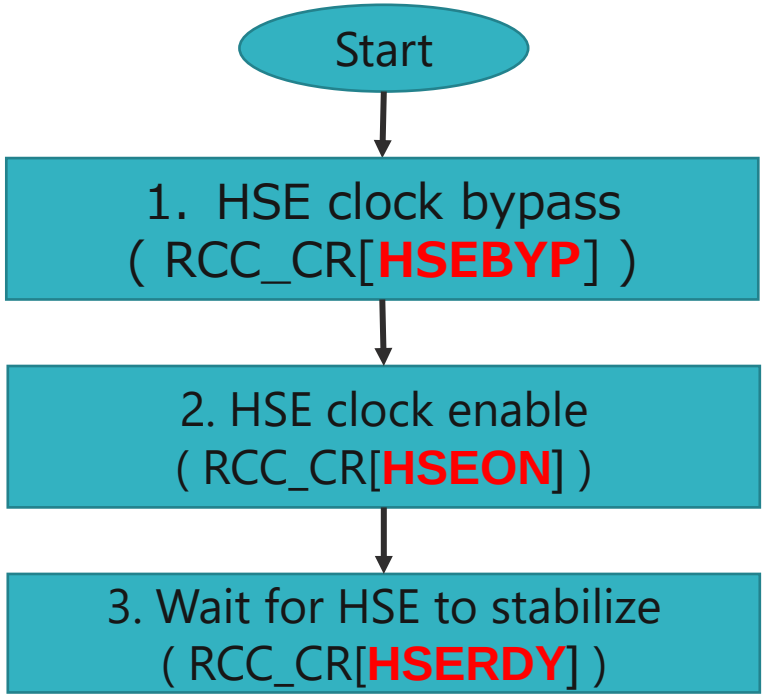
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HSICAL[7:0]								HSITRIM[4:0]					Res.	HSIRDY	HSION
r	r	r	r	r	r	r	r	rw	rw	rw	rw	rw		r	rw

Bit 18 **HSEBYP**: HSE clock bypass
Set and cleared by software to bypass the oscillator with an external clock. The external clock must be enabled with the HSEON bit, to be used by the device.
The HSEBYP bit can be written only if the HSE oscillator is disabled.
0: HSE oscillator not bypassed
1: HSE oscillator bypassed with an external clock

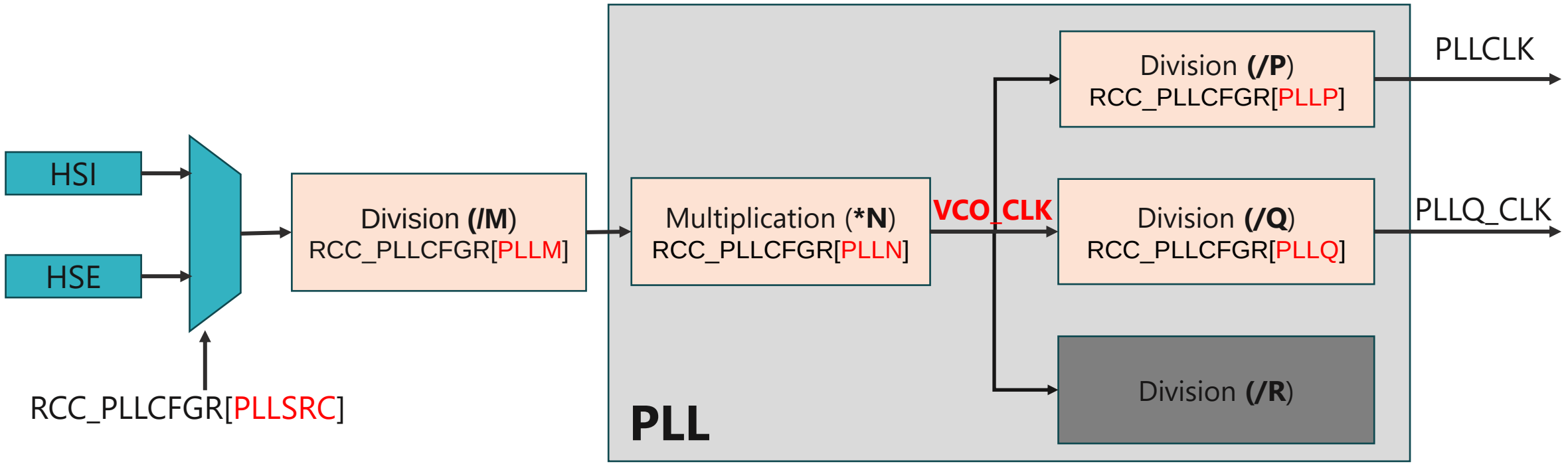
Bit 16 **HSEON**: HSE clock enable
Set and cleared by software.
Cleared by hardware to stop the HSE oscillator when entering Stop or Standby mode. This bit cannot be reset if the HSE oscillator is used directly or indirectly as the system clock.
0: HSE oscillator OFF
1: HSE oscillator ON

Bit 17 **HSERDY**: HSE clock ready flag
Set by hardware to indicate that the HSE oscillator is stable. After the HSEON bit is cleared, HSERDY goes low after 6 HSE oscillator clock cycles.
0: HSE oscillator not ready
1: HSE oscillator ready





2.2. PLL - Phase Locked Loop



$f_{(VCO\ clock)} = f_{(PLL\ clock\ input)} \times (PLLN / PLLM)$

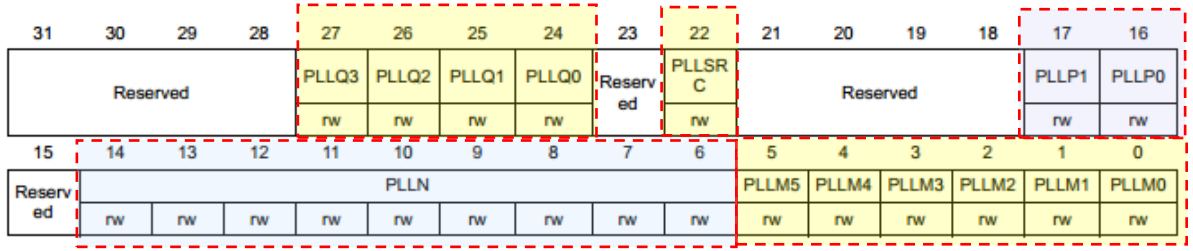
$f_{(PLL\ general\ clock\ output)} = f_{(VCO\ clock)} / PLLP$

$f_{(USB\ OTG\ FS,\ SDIO,\ RNG\ clock\ output)} = f_{(VCO\ clock)} / PLLQ$

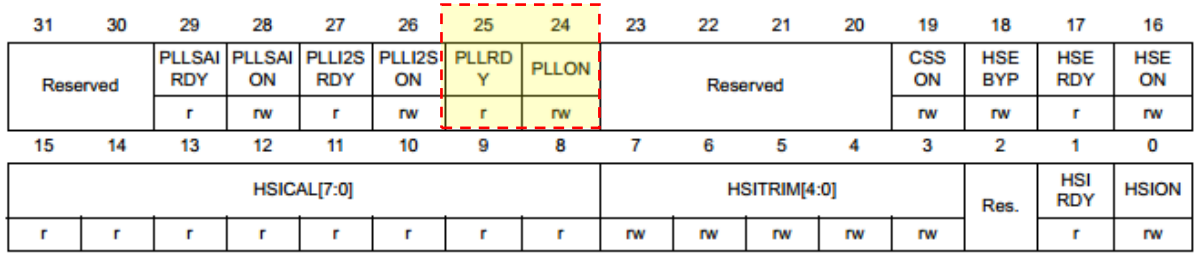
2.2. PLL - Phase Locked Loop

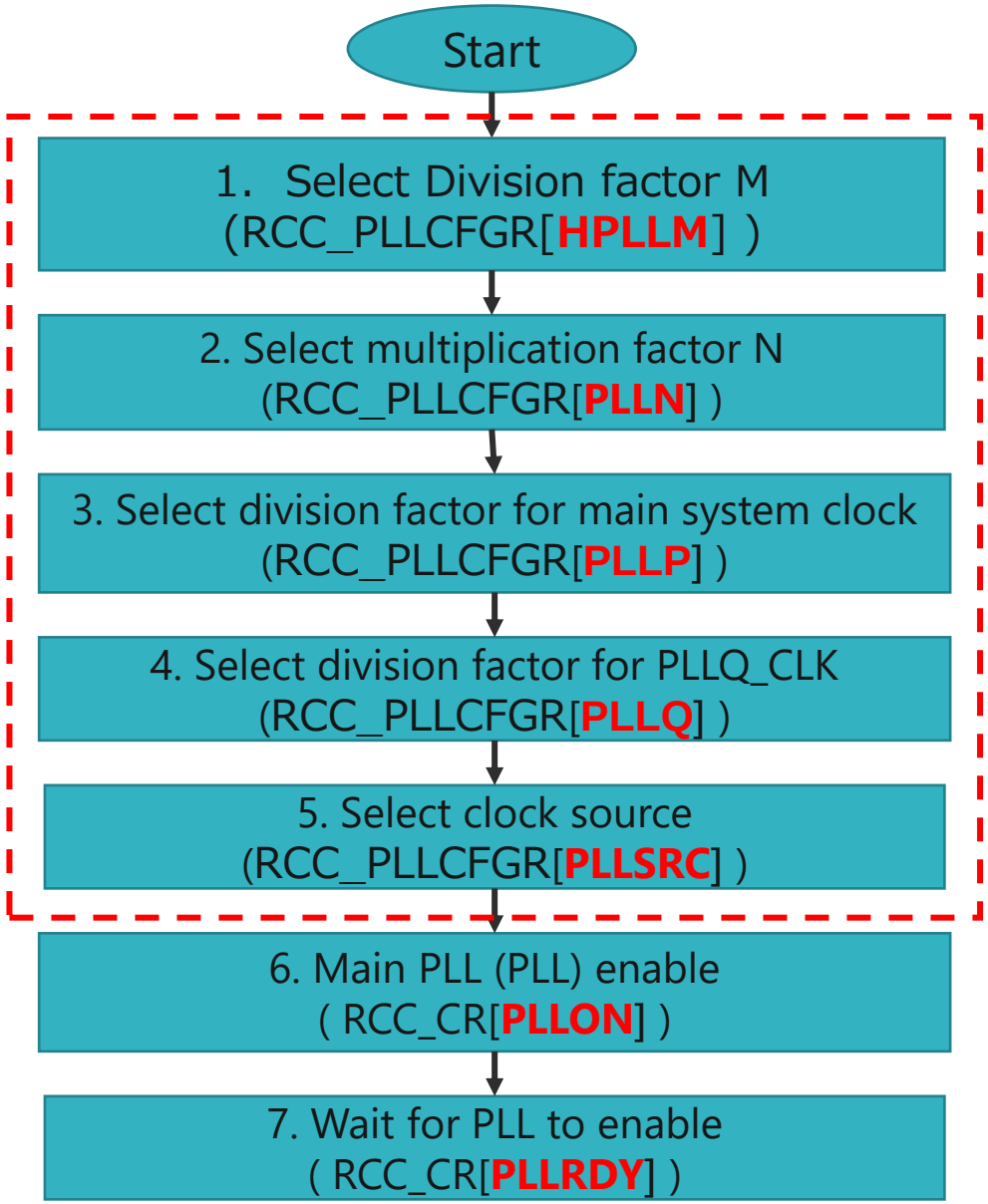
Setting PLL – Phase Locked Loop:

RCC PLL configuration register (RCC_PLLCFGR)

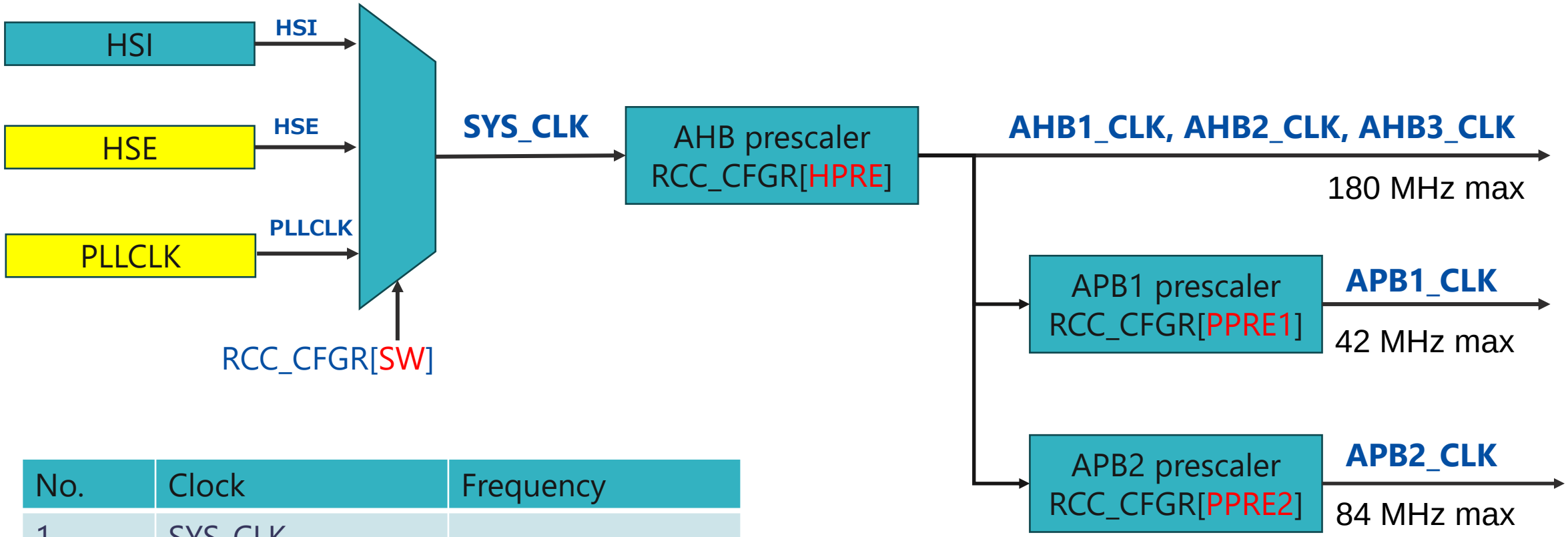


RCC clock control register (RCC_CR)





2.3. System Clock

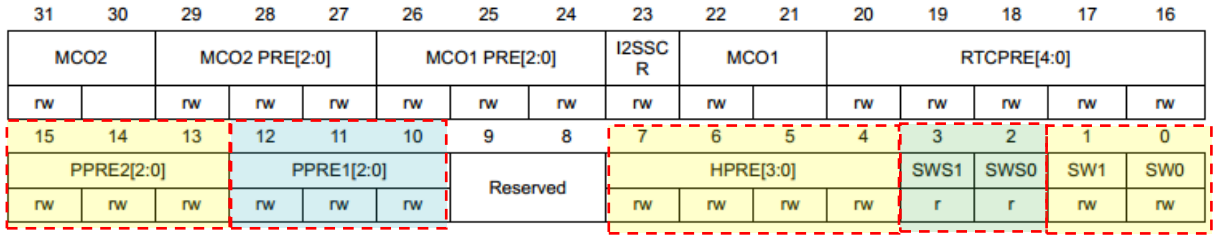


No.	Clock	Frequency
1	SYS_CLK	
2	AHBx_CLK	
3	APB1_CLK	
4	APB2_CLK	

2.3. System Clock

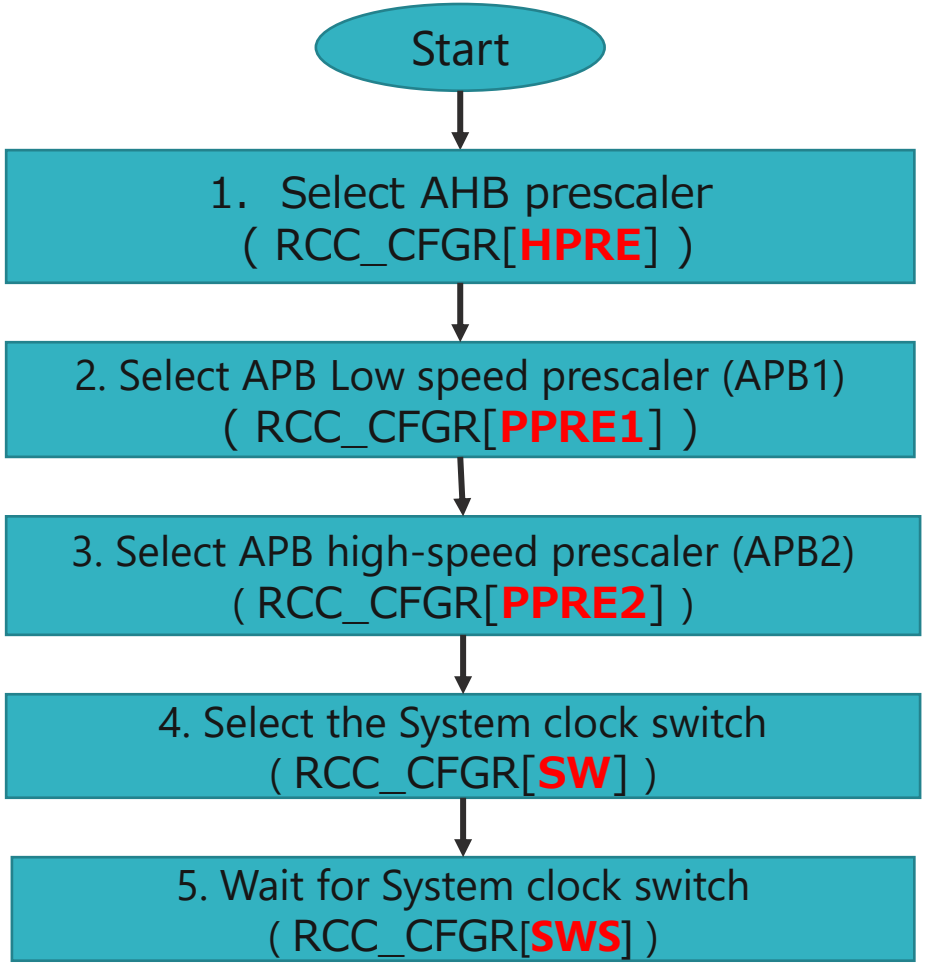
Setting System Clock:

RCC clock configuration register (RCC_CFGR)



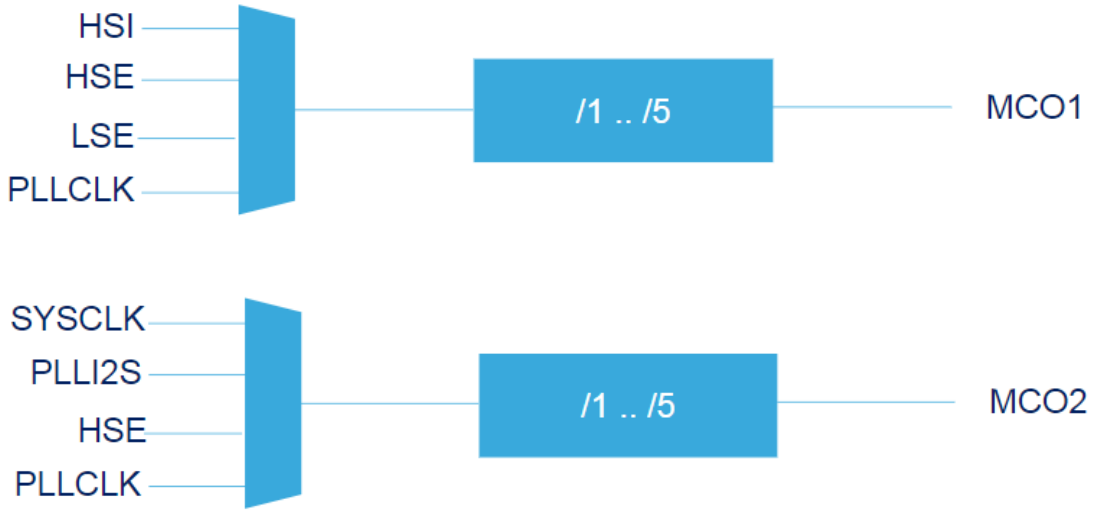
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCO2		MCO2 PRE[2:0]			MCO1 PRE[2:0]			I2SSCR	MCO1		RTCPRE[4:0]				
rw		rw	rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPRE2[2:0]			PPRE1[2:0]			Reserved		HPRE[3:0]				SWS1	SWS0	SW1	SW0
rw	rw	rw	rw	rw	rw			rw	rw	rw	rw	r	r	rw	rw



2.4. MCO – uC Clock Output

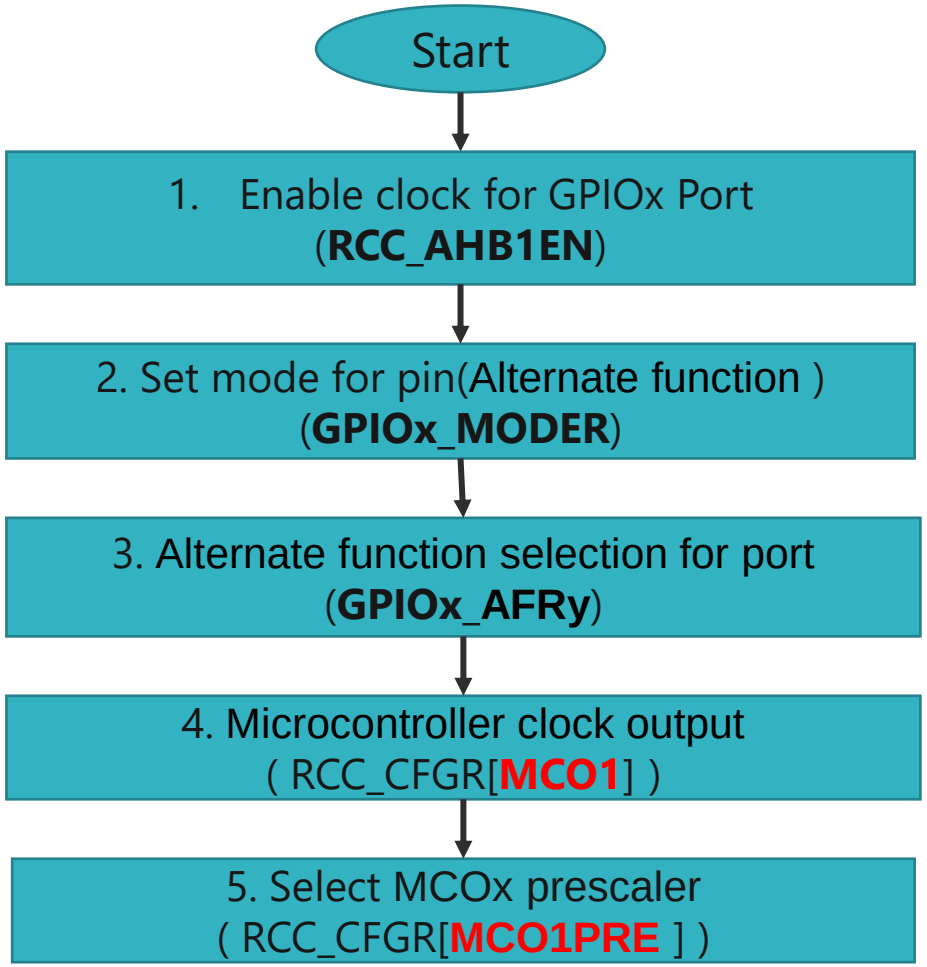
Setting MCOx:



RCC clock configuration register (RCC_CFGR)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MCO2		MCO2 PRE[2:0]			MCO1 PRE[2:0]			I2SSCR	MCO1		RTCPRE[4:0]				
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPRE2[2:0]			PPRE1[2:0]			Reserved		HPRE[3:0]				SWS1	SWS0	SW1	SW0
rw	rw	rw	rw	rw	rw			rw	rw	rw	rw	r	r	rw	rw



3.1. Assignment 1

Setting clocks:

- Initialize HSE – High Speed External
- Setting PLL:
    + PLLCLK = 180MHz
    + HSE oscillator clock selected as PLL
- Select PLLCLK as System clock source
- AHBx_CLK = 180Mhz
- APB1_CLK = 22.5MHz
- APB2_CLK = 45MHz

3.2. Assignment 2

Setting clocks:

- Initialize HSE – High Speed External
- Select HSE as System clock source
- AHBx_CLK = 8Mhz
- APB1_CLK = 2MHz
- APB2_CLK = 4MHz

3.3. Assignment 3

Initialize MCO1 pin:

- MCO1 pin = 2MHz

3.4. Assignment 4

Initialize MCO1 pin:

- MCO1 pin = 1MHz


Thank you