# SH20 QA

→ MIPS Processor for add, and sw

* complete FDE cycle, with dataflow

Remark:

1011

3 1011 <<2 = 5 1011.00

signed: -5 → -20

unsigned: 11 → 44

(*4)

$2^2$

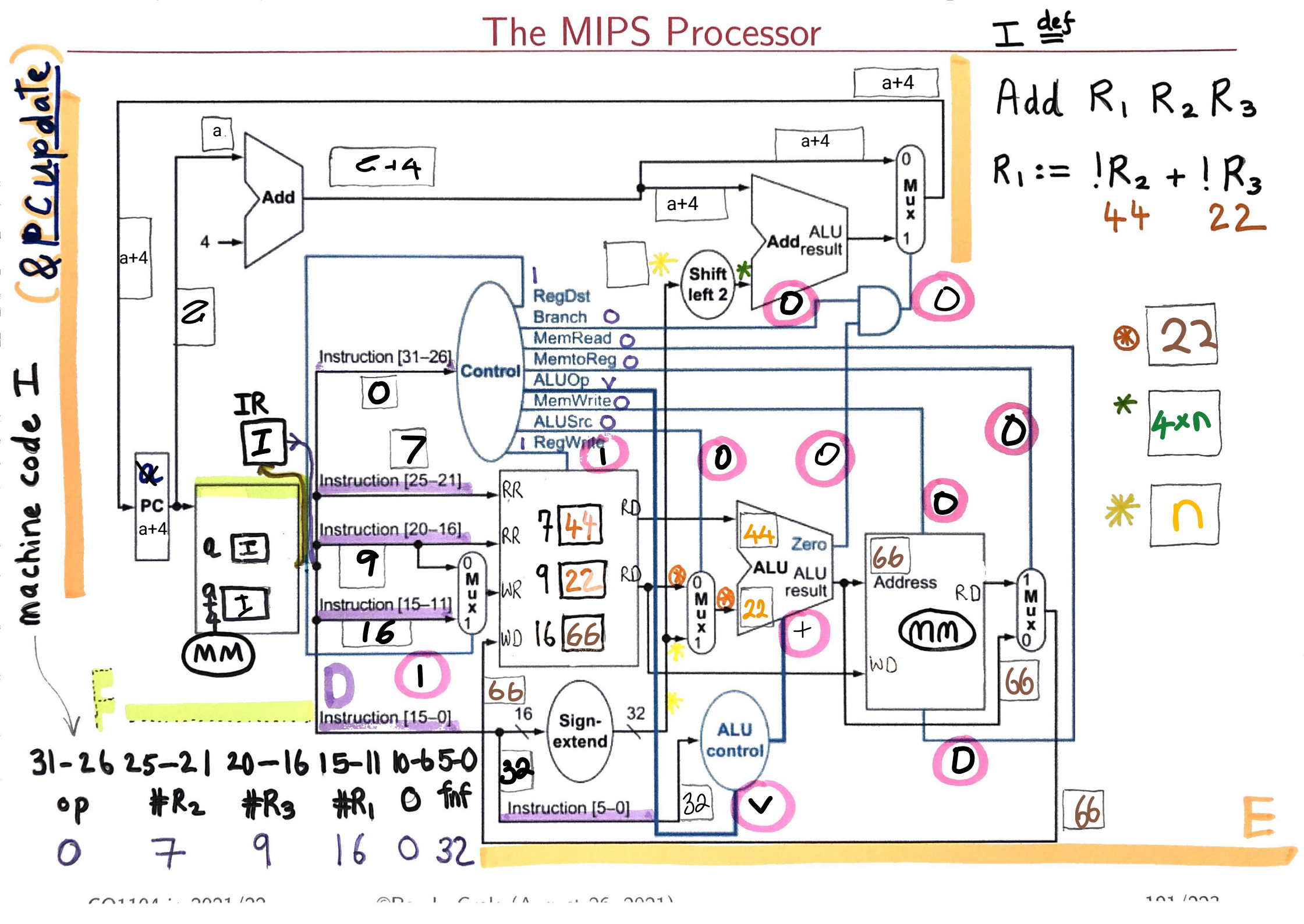
$10^2$

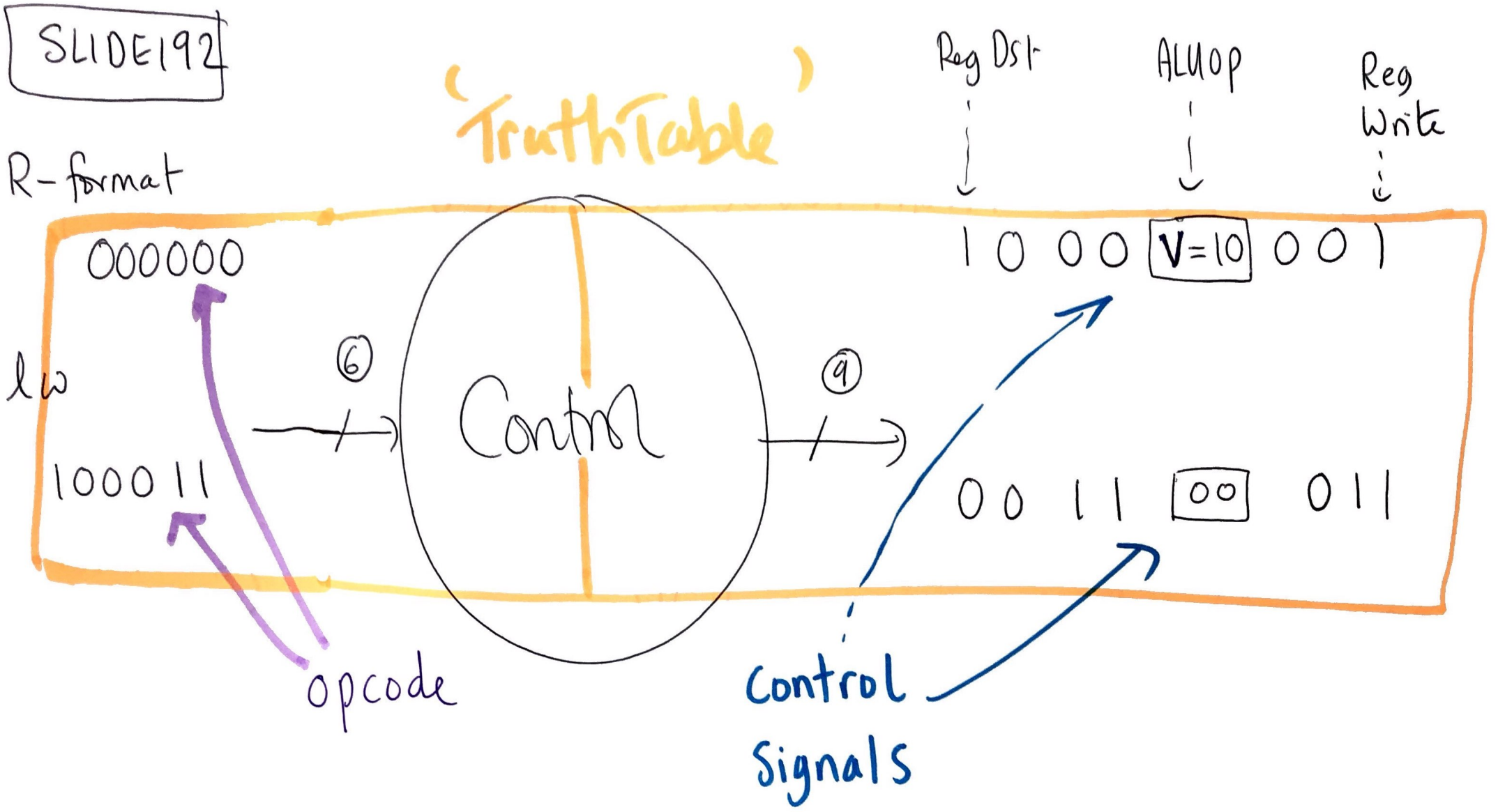
(* 100)

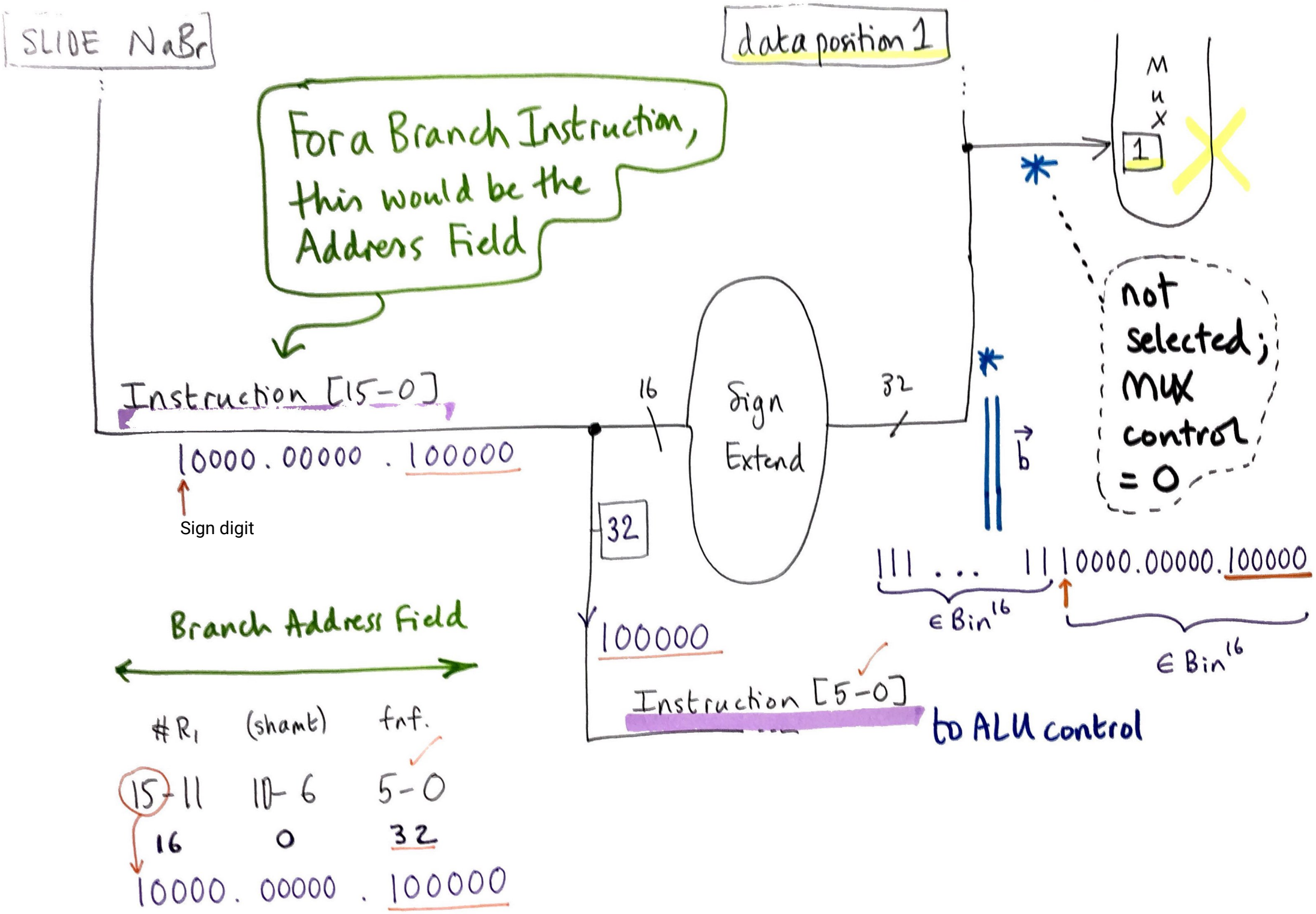
shift left 2

positions

# The MIPS Processor




SLIDE192
'TruthTable'
Reg Dst
ALUOp
Reg Write
R-format
000000
lw
100011
6
Control
9
1 0 0 0 V=10 0 0
0 0 1 1 00 0 1 1
opcode
Control Signals


SLIDE NaBr
data position 1
For a Branch Instruction, this would be the Address Field
Mux
1
not selected; MUX control = 0
Instruction [15-0]
16
Sign Extend
32
b
10000.00000.100000
Sign digit
32
111 ... 111 10000.00000.100000
∈ Bin16
∈ Bin16
100000
Instruction [5-0]
to ALU control
Branch Address Field
#R1 (shamt) fnf.
15-11 10-6 5-0
16 0 32
10000. 00000 . 100000