RISC-V SoC Project Phases

**Document Control**

Document Information

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**Project phases**

**Phase 1: Preparation Phase**  
**Objectives**

* Deliver multi-core RISC-V Based SoC with basic peripherals (GPIO, UART, I2C)
* Finish the learning plan which is parallel to the project

**Scope**

The project will be a complete HDL code for multi-core RISC-V SoC with only GPIO, UART and I2C peripherals (these peripherals could be third part or outsourced). With UVM testbench and any required tests related to such processor. No ASIC or FPGA implementations will be done in this project; yet, it will be included in next versions of the project.

**Timeframe**

The project will start in 11/8/2024 with a maximum total duration of 2 months

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| **Project Phases** | | |
| **Title** | **Description** | **Duration** |
| Preparation Phase | This phase includes all the learning required for the project | 11/8/2024 – 17/8/2024 (1 week) |
| Basic RISC-V Phase | This phase includes designing the basic RISC-V with multi-cycle | Estimated (3 days) |
| Pipelined RISC-V Phase | This phase includes adding pipelining to the processor and other features related to exceptions | Estimated (1 week) |
| Multi-core RISC-V Phase | This phase includes adding all required hardware to enable muti-core processing | Estimated (1 week) |
| SoC Phase | This Phase includes adding all the required hardware for SoC | Estimated (2 weeks) |

**Deliverables**

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| **Project Deliverables** | | |
| **Title** | **Description** | **Notes** |
| HDL Source code | All files that include the HDL code of the project | - |
| UVM Testbench | UVM testbench for the design in each stage | This may include any tests other that UVM |
| Documentation | Detailed documentation for the architecture | It is required for further development |

**Project Budget**

No budget for the project.