تمرین سری دوم طراحی سیستم های دیجیتال

کوثر دست باز ۹۸۲۴۳۰۲۳

امیرحسین ثابتی ۹۸۲۴۳۰۱۵

سوال ۱-
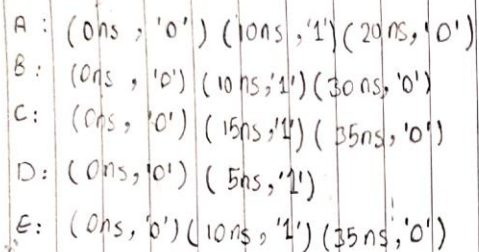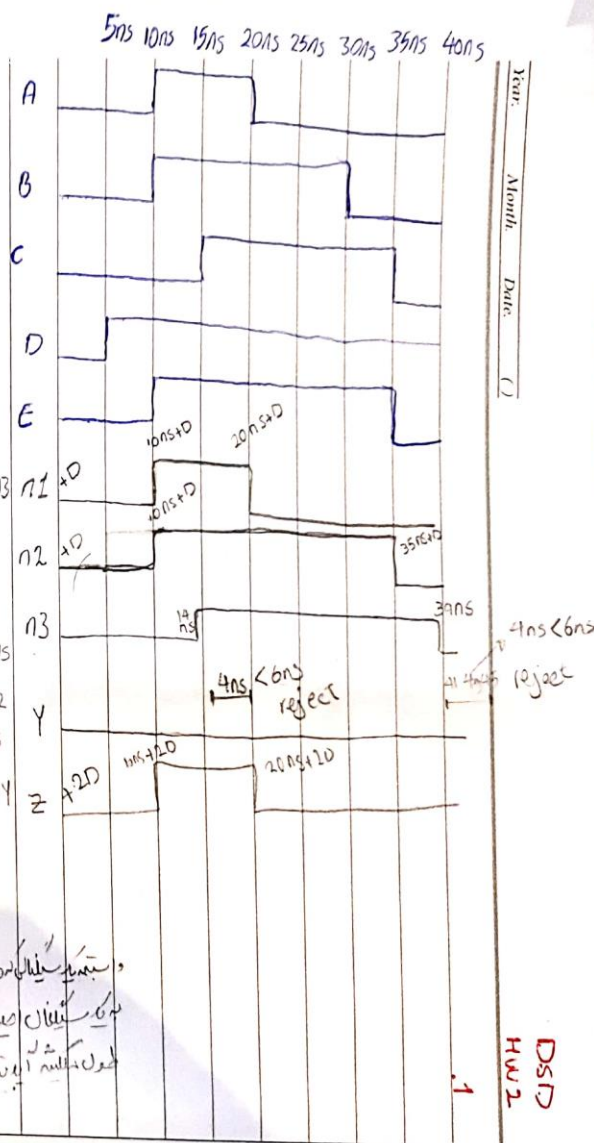
سوال۲-

-a

Std_logic را میتوان multiple drive کرد ولی std_ulogic را نمیتوان multiple drive کرد.

این را از آنجا متوجه شده ایم که فایل stdlogic.vhd را باز کردیم و در قطعه کد ها دیدیدم.

بین این دو یک رابطه subtype داریم که std_logic یک subtype برای std_ulogic است.

```
74  ----------------------------------------------------------------
75  -- resolution function
76  ----------------------------------------------------------------
77  function resolved (s : STD_ULOGIC_VECTOR) return STD_ULOGIC;
78
79
```

```
156    ------------------------------------------------------------------
157    -- conversion functions
158    ------------------------------------------------------------------
159    function To_bit          (s : STD_ULOGIC; xmap : BIT        := '0') return BIT;
160    function To_bitvector (s : STD_ULOGIC_VECTOR; xmap : BIT := '0') return BIT_VECTOR;
161
162    function To_StdULogic        (b : BIT) return STD_ULOGIC;
163    function To_StdLogicVector   (b : BIT_VECTOR) return STD_LOGIC_VECTOR;
164    function To_StdLogicVector   (s : STD_ULOGIC_VECTOR) return STD_LOGIC_VECTOR;
165    function To_StdULogicVector (b : BIT_VECTOR) return STD_ULOGIC_VECTOR;
166    function To_StdULogicVector (s : STD_LOGIC_VECTOR) return STD_ULOGIC_VECTOR;
167
168    alias To_Bit_Vector is
169       To_bitvector[STD_ULOGIC_VECTOR, BIT return BIT_VECTOR];
170    alias To_BV is
171       To_bitvector[STD_ULOGIC_VECTOR, BIT return BIT_VECTOR];
172
173    alias To_Std_Logic_Vector is
174       To_StdLogicVector[BIT_VECTOR return STD_LOGIC_VECTOR];
175    alias To_SLV is
176       To_StdLogicVector[BIT_VECTOR return STD_LOGIC_VECTOR];
177
178    alias To_Std_Logic_Vector is
179       To_StdLogicVector[STD_ULOGIC_VECTOR return STD_LOGIC_VECTOR];
180    alias To_SLV is
181       To_StdLogicVector[STD_ULOGIC_VECTOR return STD_LOGIC_VECTOR];
182
183    alias To_Std_ULogic_Vector is
184       To_StdULogicVector[BIT_VECTOR return STD_ULOGIC_VECTOR];
185    alias To_SULV is
186       To_StdULogicVector[BIT_VECTOR return STD_ULOGIC_VECTOR];
187
188    alias To_Std_ULogic_Vector is
189       To_StdULogicVector[STD_LOGIC_VECTOR return STD_ULOGIC_VECTOR];
190    alias To_SULV is
191       To_StdULogicVector[STD_LOGIC_VECTOR return STD_ULOGIC_VECTOR];
192
```

function To_bitvector (s : std_logic_vector ; xmap : bit := '0') **return** bit_vector;

function To_StdLogicVector (b : bit_vector) **return** std_logic_vector;

function TO_01 (s : BIT_VECTOR; xmap : STD_ULOGIC := '0')

Converts ' L' to . e' and ' H' to '1'. If there is any element different from these four, the entire vector is converted to the value defined by xmap, so the presence of metalogical values can be easily detected. The default value of xmap is '0'.

To_X01 (b : BIT_VECTOR)

Converts 'L' to '13' and 'H' to '1'. Any value besides these four is converted to 'X'.

To_X01Z (b : BIT_VECTOR)

Converts ' L ' to ' 13 ' and ' H' to ' 1 ' . Any value besides these four plus ' z' is converted to 'X'.

To_UX01 (b : BIT_VECTOR)

Converts ' L ' to '13' and ' H' to ' 1 ' . Any value besides these four plus ' U' is converted to 'X'.

-c

	U	X	0	1	Z	W	H	L	-
U	U	U	U	U	U	U	U	U	U
X	U	X	X	X	X	X	X	X	X
0	U	X	0	X	0	0	0	0	X
1	U	X	X	1	1	1	1	1	X
Z	U	X	0	1	Z	W	L	H	X
W	U	X	0	1	W	W	W	W	X
H	U	X	0	1	L	W	L	W	X
L	U	X	0	1	H	W	W	H	X
-	U	X	X	X	X	X	X	X	X

-d

subtype X01 is RESOLVED std_ulogic range 'x' to '1'

subtype X01Z is RESOLVED stdulogic range 'x' to 'z'

subtype UX01 is RESOLVED std_ulogic range 'U' to '1'

subtype UX01Z is RESOLVED std_ulogic range 'U' to 'Z';

۱)

TYPE mem-row is ARRAY(0 TO 31) of STD_LOGIC;

TYPE MEMORY is ARRAY(0 TO 1023)of mem-row;

۲)

TYPE memory IS ARRAY (0 TO 1023, 0 TO 31) OF STD_LOGIC;

۳)

TYPE student IS RECORD

  FirstName:string;

  LastName:string;

  StudentID:INTEGER;

 END RECORD;

۴)

TYPE elevator_floor IS(firstFloor,secendFloor,thirdFloor)