Shahid Beheshti University
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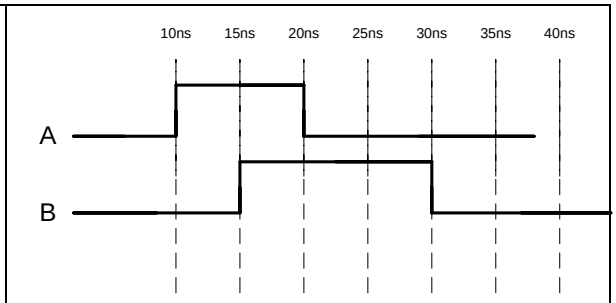
Computer Aided Digital System Design
Homework No.1

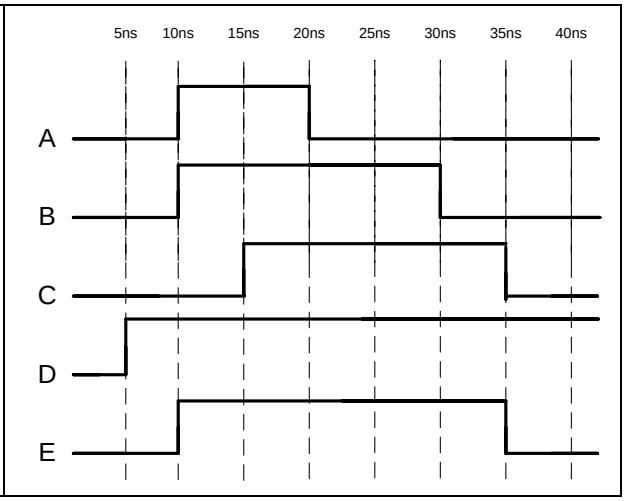
1. Design a FullAdder with Two 8-to-1 multiplexer.
2. What is clock gating?
3. Compare fuse-based and SRAM-based FPGAs.
4. Sketch the waveform of the output and internal signals.

```
ENTITY excercise1 IS
    PORT ( a, b : IN  bit;
           y    : OUT bit);
END test;
ARCHITECTURE test OF excercise1 IS
    SIGNAL n1 : bit;
BEGIN
    n1 <= NOT b AFTER 2 ns;
    y <= a AND n1 AFTER 3 ns;
END test;
```



5. Sketch the waveform of the output and internal signals.

```
ENTITY excercise1 IS
    PORT ( a, b, c, d, e : IN  bit;
           y             : OUT bit);
END test;
ARCHITECTURE test OF excercise1 IS
    SIGNAL n1, n2, n3 : bit;
BEGIN
    n1 <= a AND b;
    n2 <= d AND e;
    n3 <= n1 OR c AFTER 4 ns;
    y <= n3 XOR n2 AFTER 6 ns;
```



6.