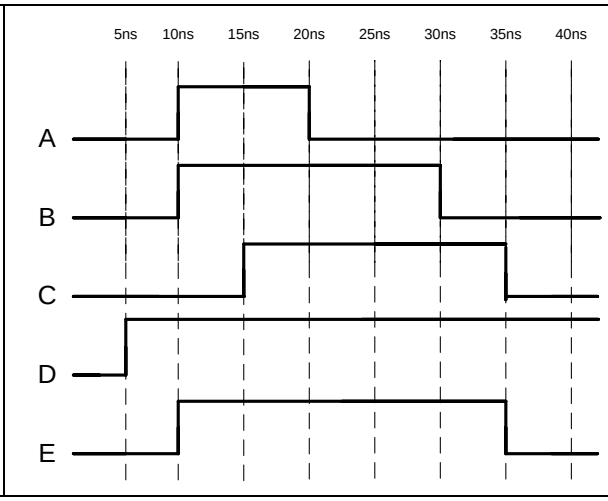
Shahid Beheshti University
Faculty of Computer Science and Engineering

Computer Aided Digital System Design
Homework No.2

1. Sketch the waveform of the output and internal signals using delay and Delta-delay

```
ENTITY excercise1 IS
    PORT ( a, b, c, d, e : IN  bit;
           y             : OUT bit);
END test;
ARCHITECTURE test OF excercise1 IS
    SIGNAL n1, n2, n3 : bit;
BEGIN
    n1 <= a AND b;
    n2 <= d AND e;
    n3 <= n1 OR c AFTER 4 ns;
    y <= n3 XOR n2 AFTER 6 ns;
    z <= n1 OR y;
```



2. Reply the following questions by viewing the files in MODELSIM/vhdlsrc/std , MODELSIM/vhdlsrc/ieee and MODELSIM/vhdlsrc/synopsys folders.
    a. Write the relation of type std_logic and std_ulogic.
    b. List the conversion function from std_logic and bit_vector.
    c. Write the resolution table of std_logic.
    d. Write the resolved subtypes of std_ulogic.

3. Define the following types
    a. A memory with 1024 rows such that each row is a big-endian 32 bit (array of array)
    b. A memory with 1024 rows such that each row is a big-endian 32 bit (matrix)
    c. A record type that defines a student.
    d. A state types describes the states of an 3-floor elevator.