

## Εργαστήριο 9<sup>ο</sup>:

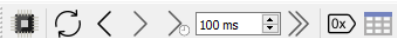
### 9.9 (1):

1. IF (fetch) προσοψίση της εντολής από την μνήμη.
2. ID (instruction decode/register file read) γίνεται αναγνώση των καταχωρητών κατά την αποκωδικοποίηση της εντολής, καθώς η μορφή που έχουν οι εντολές στον MIPS γίνεται ταυτόχρονα αναγνώση και αποκωδικοποίηση.
3. EX (execute/address calculation) εκτέλεση της λειτουργίας ή γίνεται υπολογισμός μιας διεύθυνσης.
4. MEM (memory access) γίνεται μείβαση και προσπερνάει ένας τιτέσττος στη μνήμη δεδομένων.
5. WB (write back) γίνεται εγγραφή αποτελεσμάτων σε ένα καταχωρητή.

(2) Οι βαθμίδες 1, 2 και 3 είναι χρήσιμες για όλες τις εντολές.

(3) α) Μόνο η 4<sup>η</sup> βαθμίδα δεν κάνει τίποτα από εντολές αρ. πράξεων

β) Η βαθμίδα WB δεν κάνει κάτι χρήσιμο για τις εντολές store



9.9 (4)

100  
1010  
01  
Editor

Processor



Memory

Source code

```
1 addi x5, x0, 1
2 addi x6, x0, 2
3
4 add x7, x6, x5
5 add x8, x7, x7
6
7 sw x8, 100(x0)
8 lw x9, 100(x0)
```



Executable code

0:	00100293	addi x5 x0 1
4:	00200313	addi x6 x0 2
8:	005303b3	add x7 x6 x5
c:	00738433	add x8 x7 x7
10:	06802223	sw x8 100(x0)
14:	06402483	lw x9 100(x0)

View mode: ☐ Binary ☒ Disassembled

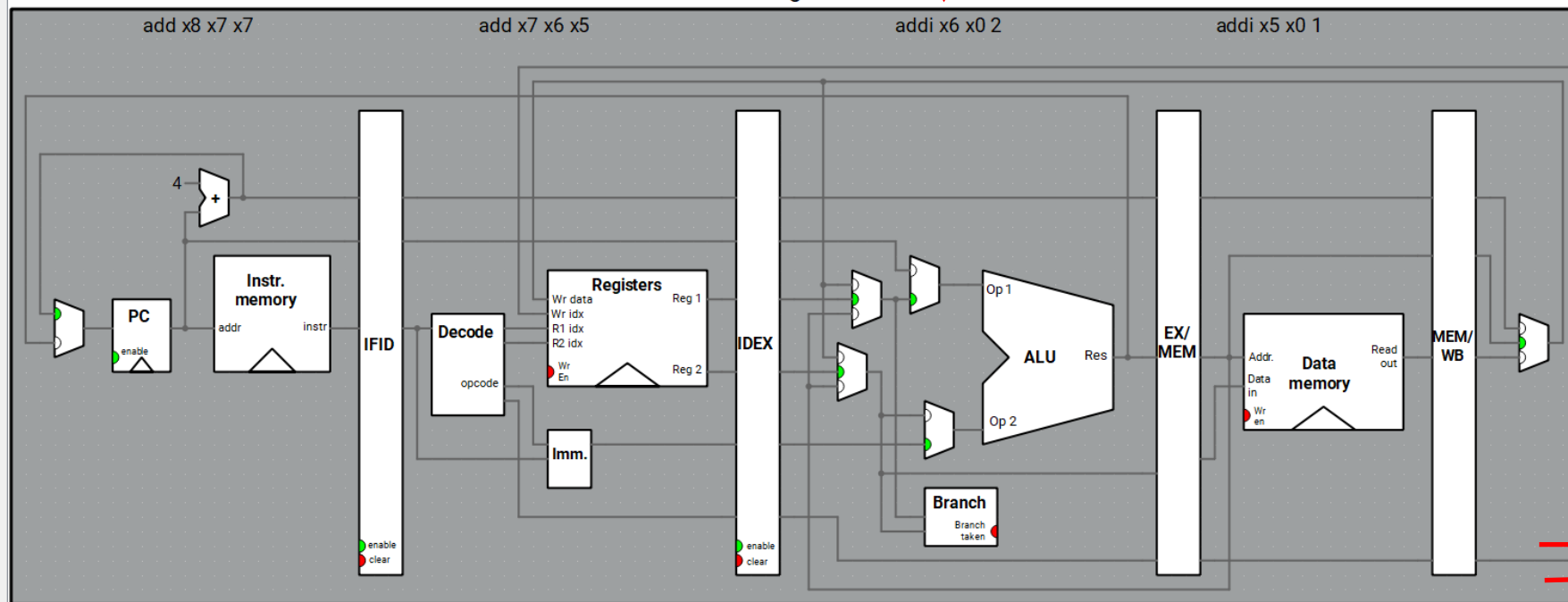
9.9 (4α)

1C0  
1010  
01  
Editor

Processor

Memory

## 5-Stage RISC-V Processor



## Registers

Name	Alias	Value
x0	zero	0x00000000
x1	ra	0x00000000
x2	sp	0x7fffffff0
x3	gp	0x10000000
x4	tp	0x00000000
x5	t0	0x00000000
x6	t1	0x00000000
x7	t2	0x00000000
x8	s0	0x00000000
x9	s1	0x00000000
x10	a0	0x00000000
x11	a1	0x00000000
x12	a2	0x00000000
x13	a3	0x00000000

Display type: Hex

## Instruction memory

BP	Addr	Stage	Instruction
<input type="checkbox"/>	0x0	MEM	addi x5 x0 1
<input type="checkbox"/>	0x4	EX	addi x6 x0 2
<input type="checkbox"/>	0x8	ID	add x7 x6 x5
<input type="checkbox"/>	0xc	IF	add x8 x7 x7
<input type="checkbox"/>	0x10		sw x8 100(x0)
<input type="checkbox"/>	0x14		lw x9 100(x0)

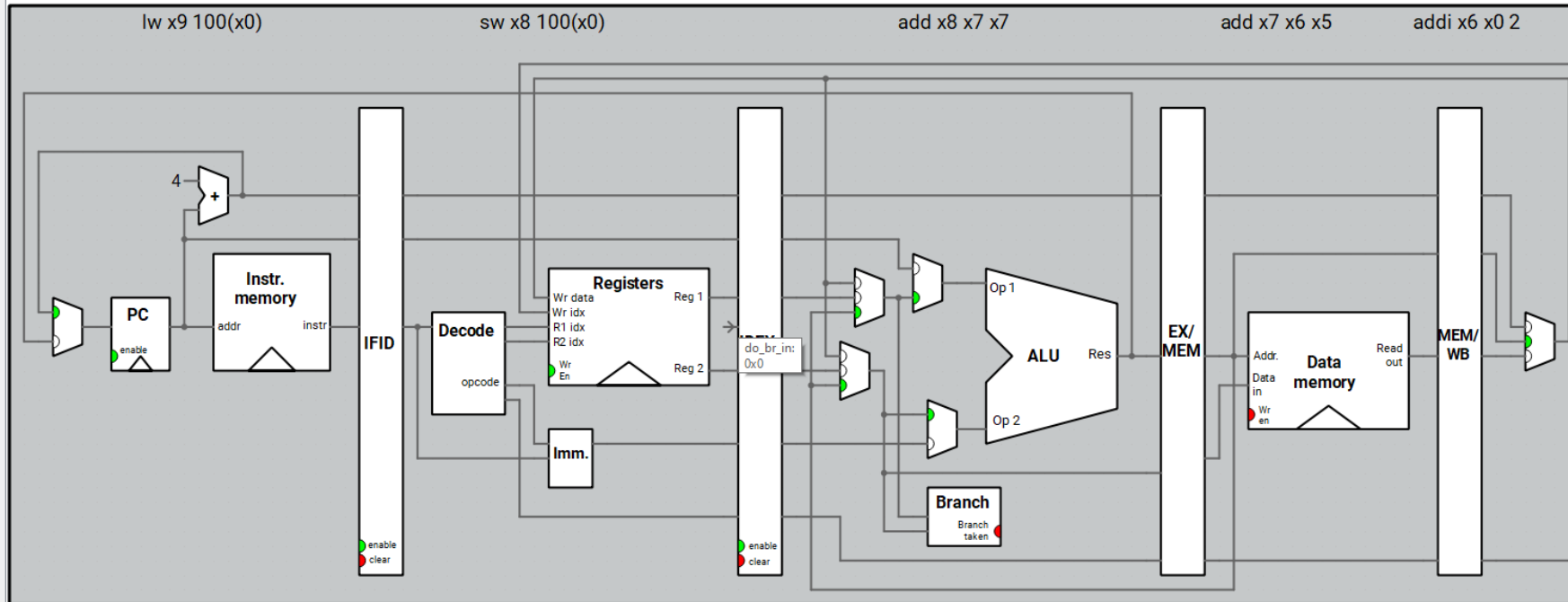
## Output

Εντολές μεταξύ καταχωρητών και σταθερών.

## Statistics

Cycles: 3  
Instrs. retired: 0  
CPI:   
IPC:

## 5-Stage RISC-V Processor



## Registers

Name	Alias	Value
x0	zero	0x00000000
x1	ra	0x00000000
x2	sp	0x7fffffff0
x3	gp	0x10000000
x4	tp	0x00000000
x5	t0	0x00000001
x6	t1	0x00000000
x7	t2	0x00000000
x8	s0	0x00000000
x9	s1	0x00000000
x10	a0	0x00000000
x11	a1	0x00000000
x12	a2	0x00000000
x13	a3	0x00000000

Display type: Hex

## Instruction memory

BP	Addr	Stage	Instruction
<input type="checkbox"/>	0x0		addi x5 x0 1
<input type="checkbox"/>	0x4	WB	addi x6 x0 2
<input type="checkbox"/>	0x8	MEM	add x7 x6 x5
<input type="checkbox"/>	0xc	EX	add x8 x7 x7
<input type="checkbox"/>	0x10	ID	sw x8 100(x0)
<input type="checkbox"/>	0x14	IF	lw x9 100(x0)

## Output

Εντολές αριθμητικών πράξεων.

## Statistics

Cycles: 5  
Instrs. retired: 1  
CPI: 5  
IPC: 0.2

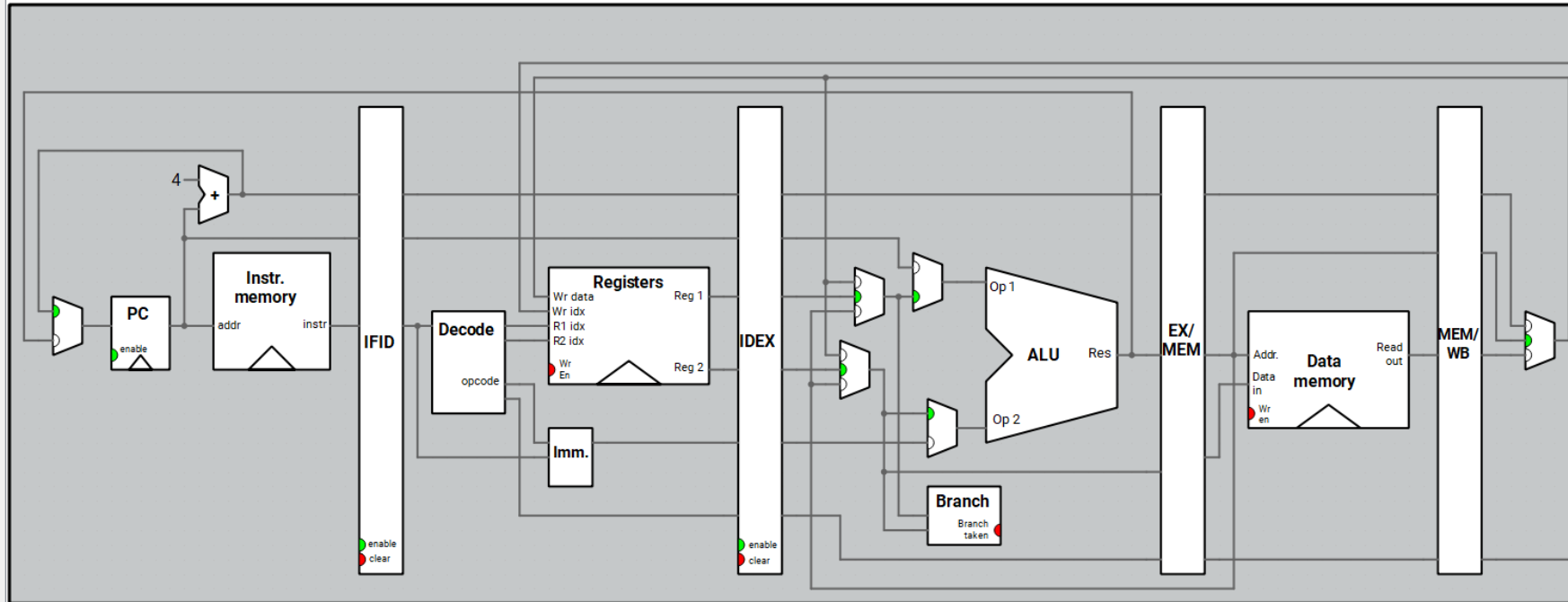
9.9 (4γ)

100  
1010  
01  
Editor

Processor

Memory

## 5-Stage RISC-V Processor



## Registers

Name	Alias	Value
x0	zero	0x00000000
x1	ra	0x00000000
x2	sp	0x7fffffff0
x3	gp	0x10000000
x4	tp	0x00000000
x5	t0	0x00000001
x6	t1	0x00000002
x7	t2	0x00000003
x8	s0	0x00000006
x9	s1	0x00000006
x10	a0	0x00000000
x11	a1	0x00000000
x12	a2	0x00000000
x13	a3	0x00000000

Display type: Hex

## Instruction memory

BP	Addr	Stage	Instruction
<input type="checkbox"/>	0x0		addi x5 x0 1
<input type="checkbox"/>	0x4		addi x6 x0 2
<input type="checkbox"/>	0x8		add x7 x6 x5
<input type="checkbox"/>	0xc		add x8 x7 x7
<input type="checkbox"/>	0x10		sw x8 100(x0)
<input type="checkbox"/>	0x14		lw x9 100(x0)

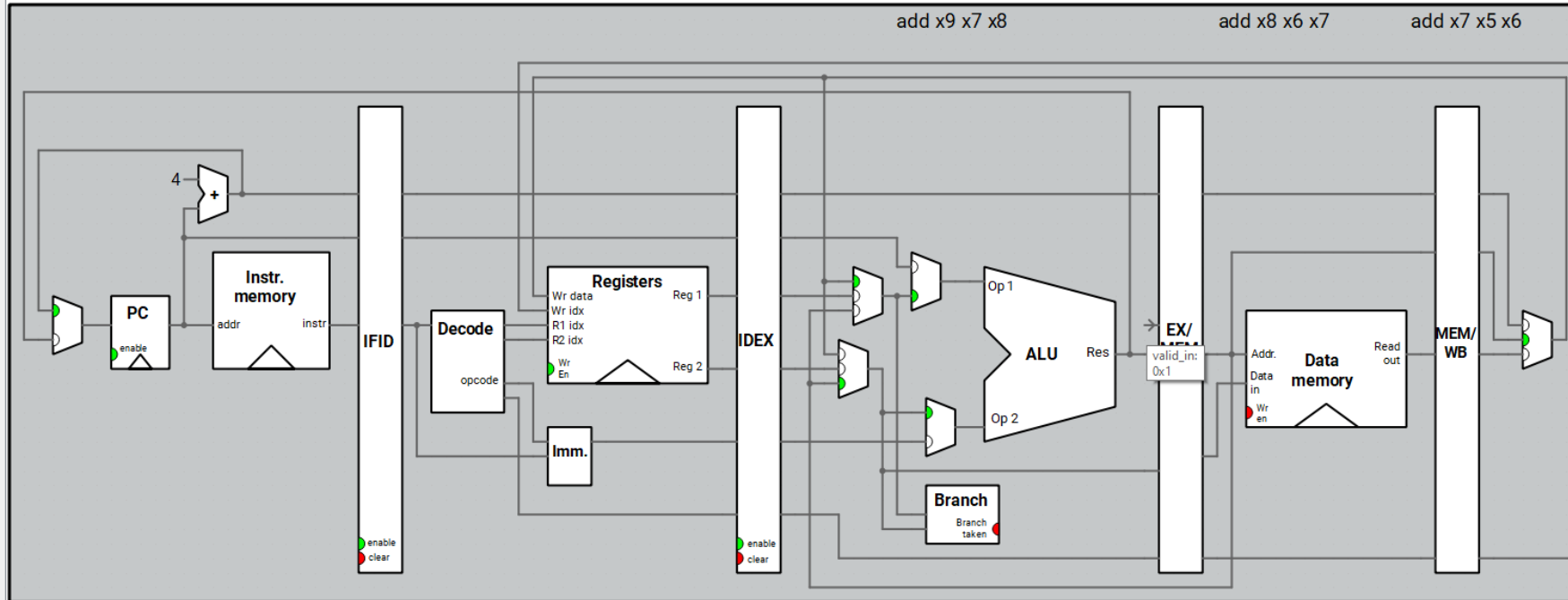
## Output

Εντολές load και store.

## Statistics

Cycles: 10  
Instrs. retired: 6  
CPI: 1.67  
IPC: 0.6

## 5-Stage RISC-V Processor



## Registers

Name	Alias	Value
x0	zero	0x00000000
x1	ra	0x00000000
x2	sp	0x7fffffff
x3	gp	0x10000000
x4	tp	0x00000000
x5	t0	0x00000000
x6	t1	0x00000000
x7	t2	0x00000000
x8	s0	0x00000000
x9	s1	0x00000000
x10	a0	0x00000000
x11	a1	0x00000000
x12	a2	0x00000000
x13	a3	0x00000000

Display type: Hex

## Instruction memory

BP	Addr	Stage	Instruction
<input type="checkbox"/>	0x0	WB	add x7 x5 x6
<input type="checkbox"/>	0x4	MEM	add x8 x6 x7
<input type="checkbox"/>	0x8	EX	add x9 x7 x8

## Output

## Statistics

Cycles:

Instrs. retired:

CPI:

IPC:



100 ms



9.9 (6)

100  
1010  
01  
Editor

Processor



Memory

Source code

```
1 .data
2 argument1: .word 1
3 argument2: .word 2
4 argument3: .word 3
5 argument4: .word 4
6 argument5: .word 5
7
8 .text
9 main:
10
11     la s0, argument1
12
13     lw s1, 0(s0)
14     lw s2, 4(s0)
15
16     add s7, s1, s2
17     sw s7, 16(s0)
18
19     lw s3, 8(s0)
20     sub, s10, s1, s3
21
22     sw s10, 12(s0)
```

Executable code

View mode: ☐ Binary ☒ Disassembled

```
00000000 <main>:
0:    10000417    auipc x8, 0x65536
4:    00040413    addi x8, x8, 0
8:    00042483    lw x9, 0(x8)
c:    00442903    lw x18, 4(x8)
10:   01248bb3    add x23, x9, x18
14:   01742823    sw x23, 16(x8)
18:   00842983    lw x19, 8(x8)
1c:   41348d33    sub x26, x9, x19
20:   01a42623    sw x26, 12(x8)
```

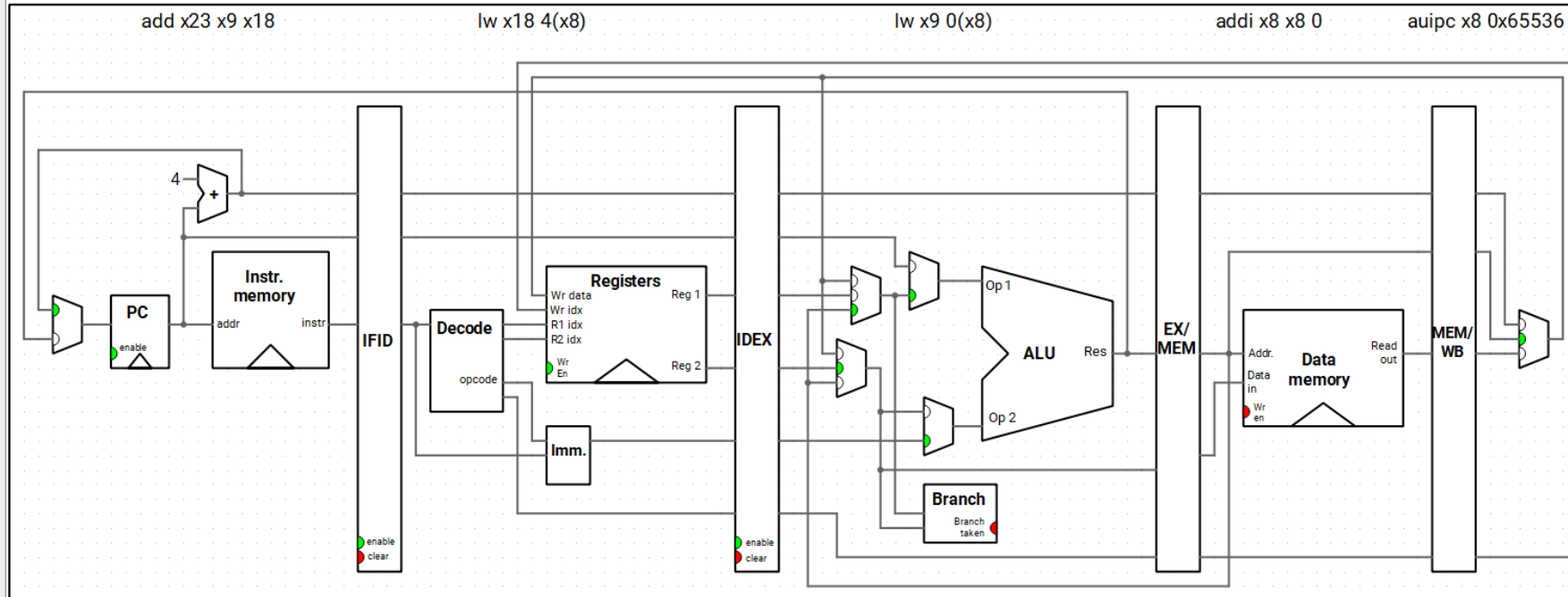
WB

100  
1010  
01  
Editor

Processor

Memory

## 5-Stage RISC-V Processor



## Registers

Name	Alias	Value
x2	sp	0x7fffffff0
x3	gp	0x10000000
x4	tp	0x00000000
x5	t0	0x00000000
x6	t1	0x00000000
x7	t2	0x00000000
x8	s0	0x00000000
x9	s1	0x00000000
x10	a0	0x00000000
x11	a1	0x00000000
x12	a2	0x00000000
x13	a3	0x00000000
x14	a4	0x00000000
x15	a5	0x00000000

Display type: Hex

## Instruction memory

BP	Addr	Stage	Instruction
<input type="checkbox"/>	0x0	WB	auipc x8 0x65536
<input type="checkbox"/>	0x4	MEM	addi x8 x8 0
<input type="checkbox"/>	0x8	EX	lw x9 0(x8)
<input type="checkbox"/>	0xc	ID	lw x18 4(x8)
<input type="checkbox"/>	0x10	IF	add x23 x9 x18
<input type="checkbox"/>	0x14		sw x23 16(x8)
<input type="checkbox"/>	0x18		lw x19 8(x8)
<input type="checkbox"/>	0x1c		sub x26 x9 x19
<input type="checkbox"/>	0x20		sw x26 12(x8)

## Statistics

Cycles: 4  
Instrs. retired: 0  
CPI:   
IPC:

## Output

1η Ακολουθία εντολών



Ripes

File Help

100 ms

0x

100

1010

01

Editor

Processor

Memory

5-Stage RISC-V Processor

sw x26 12(x8)

sub x26 x9 x19

lw x19 8(x8)

sw x23 16(x8)

add x23 x9 x18

PC

enable

Instr. memory

addr

instr

IFID

Decode

opcode

Registers

Wr data

Wr idx

R1 idx

R2 idx

Wr

En

Imm.

IDEX

Op 1

Op 2

Res

ALU

EX/MEM

Data memory

Addr.

Data in

Read out

Wr

en

MEM/WB

Branch

Branch taken

enable

clear

enable

clear

Output

2η Ακολουθία εντολών με lw

Statistics

Cycles: 9

Instrs. retired: 4

CPI: 2.25

IPC: 0.444

Registers

Name	Alias	Value
x11	a1	0x00000000
x12	a2	0x00000000
x13	a3	0x00000000
x14	a4	0x00000000
x15	a5	0x00000000
x16	a6	0x00000000
x17	a7	0x00000000
x18	s2	0x00000002
x19	s3	0x00000000
x20	s4	0x00000000
x21	s5	0x00000000
x22	s6	0x00000000
x23	s7	0x00000000
x24	s8	0x00000000

Display type: Hex

Instruction memory

BP	Addr	Stage	Instruction
<input type="checkbox"/>	0x0		auipc x8 0x65536
<input type="checkbox"/>	0x4		addi x8 x8 0
<input type="checkbox"/>	0x8		lw x9 0(x8)
<input type="checkbox"/>	0xc		lw x18 4(x8)
<input type="checkbox"/>	0x10	WB	add x23 x9 x18
<input type="checkbox"/>	0x14	MEM	sw x23 16(x8)
<input type="checkbox"/>	0x18	EX	lw x19 8(x8)
<input type="checkbox"/>	0x1c	ID	sub x26 x9 x19
<input type="checkbox"/>	0x20	IF	sw x26 12(x8)