ANALOG PROJECT

EE301

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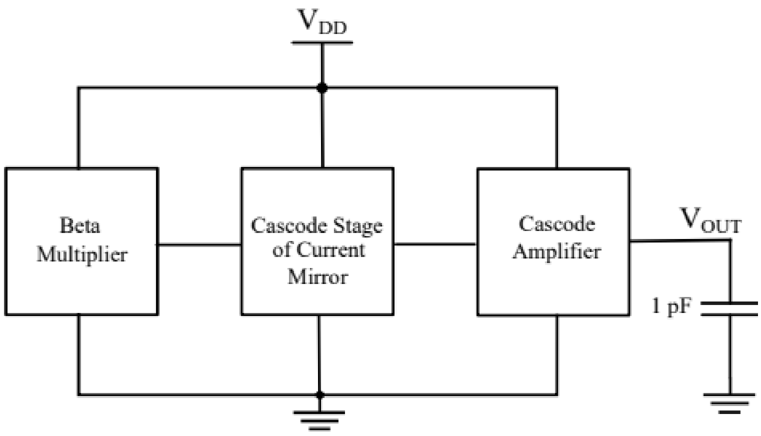
Aim:

To design and implement a Beta Multiplier, Cascode Current Mirror and Cascode Amplifier in 180nm and 22 nm technology nodes using in LtSpice for circuit simulation and Magic for layout desgin.

LtSpice Simulation:

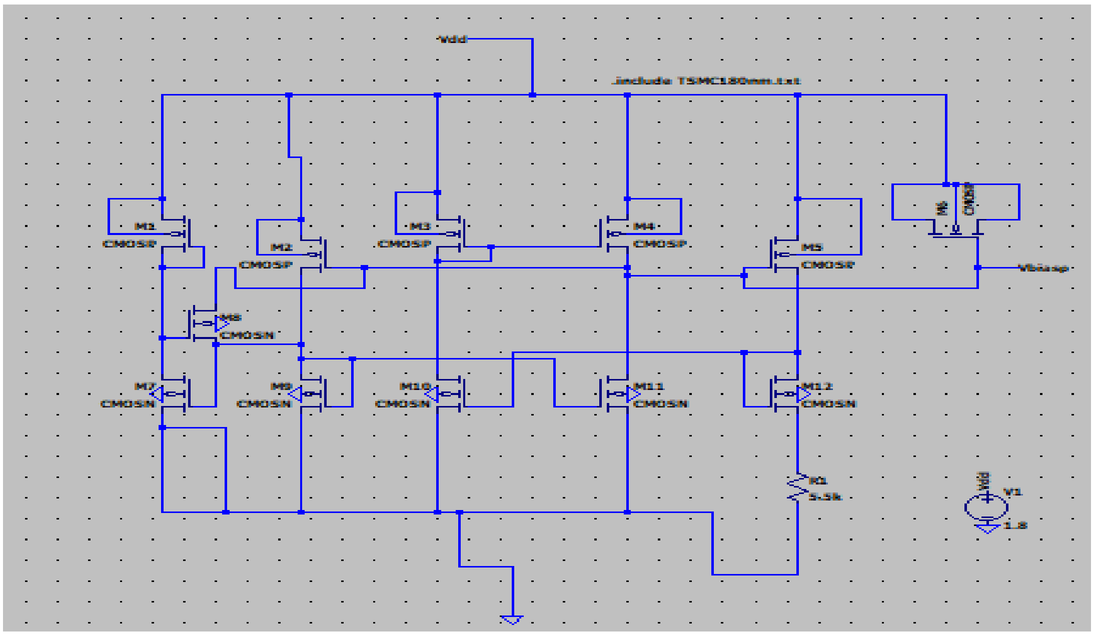
The overall block diagram of cascode amplifier with other blocks:



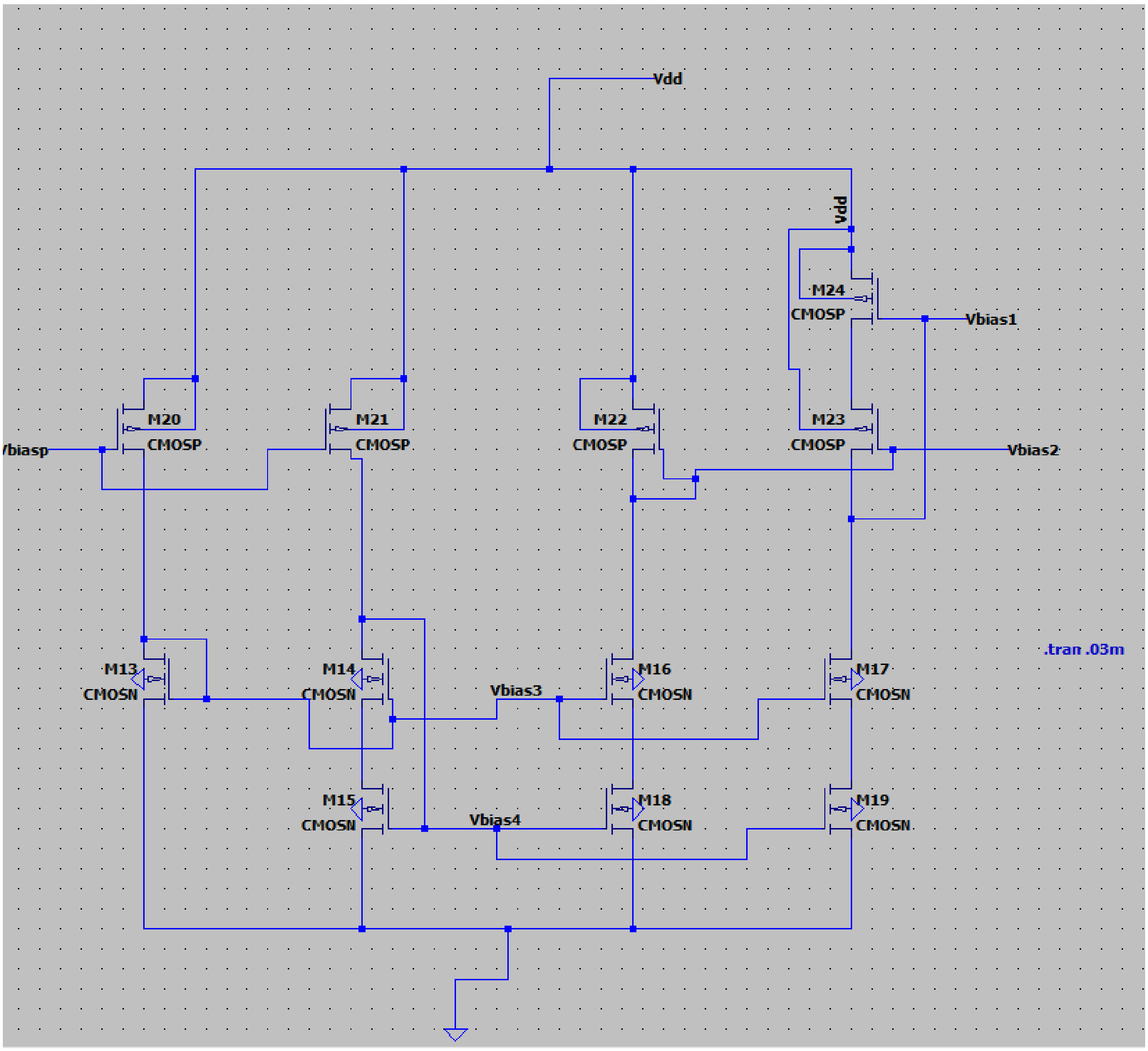
A) 180 nm Technology:

<u>Simulation</u>

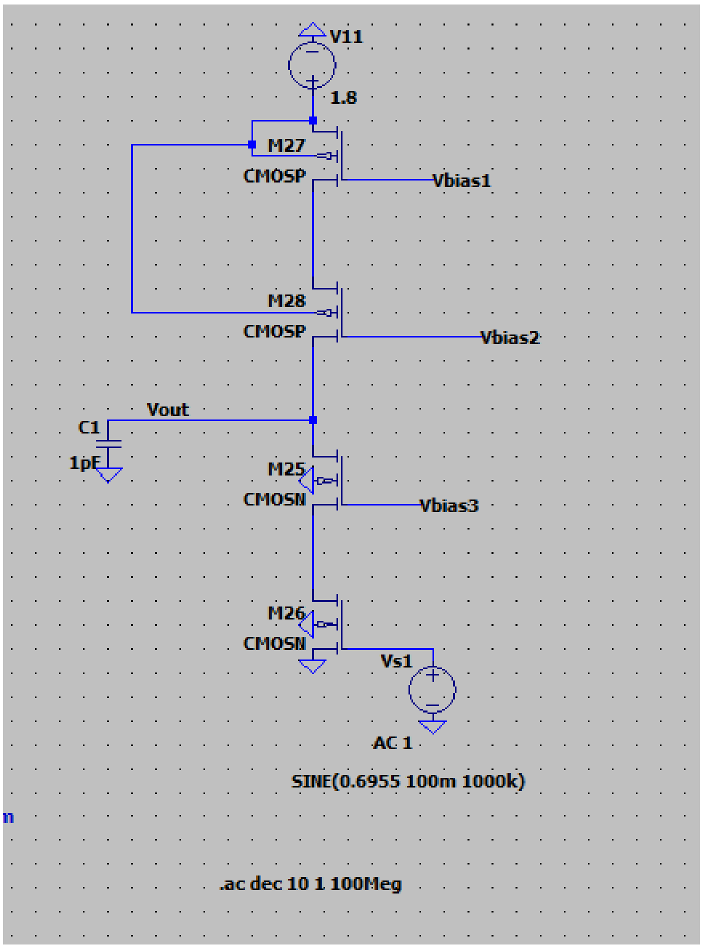
The following images display the LtSpice schematics for the Beta Multiplier, Cascode Current Mirror and Cascode Amplifier circuits designed in 180nm technolagy.In the Beta Multiplier and Cascode Current Mirror circuits, the W/L ratios were configured according to the specified values provided. For the Cascode Amplifer, the W/L ratio was determined through calculations, which are detailed in the following section.



Beta Multiplier

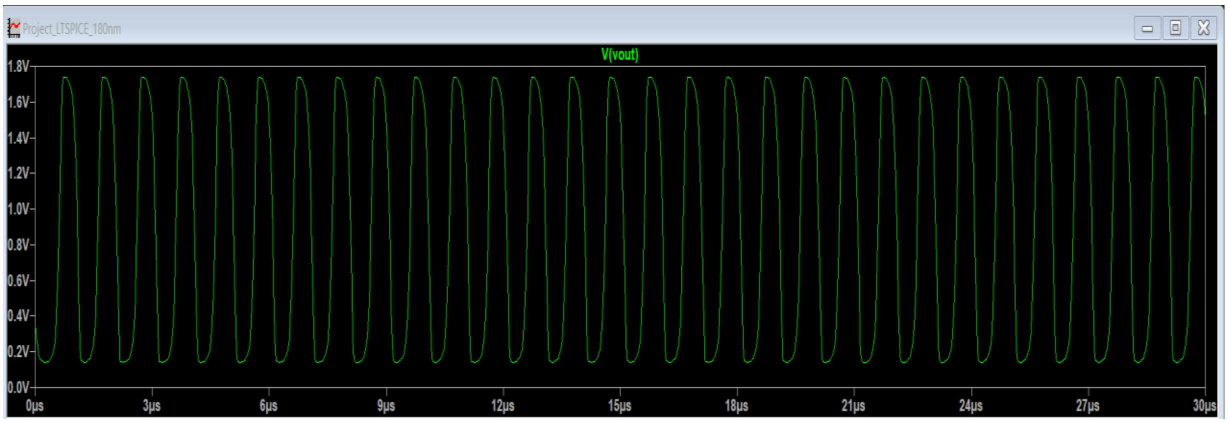


Cascode Current Mirror

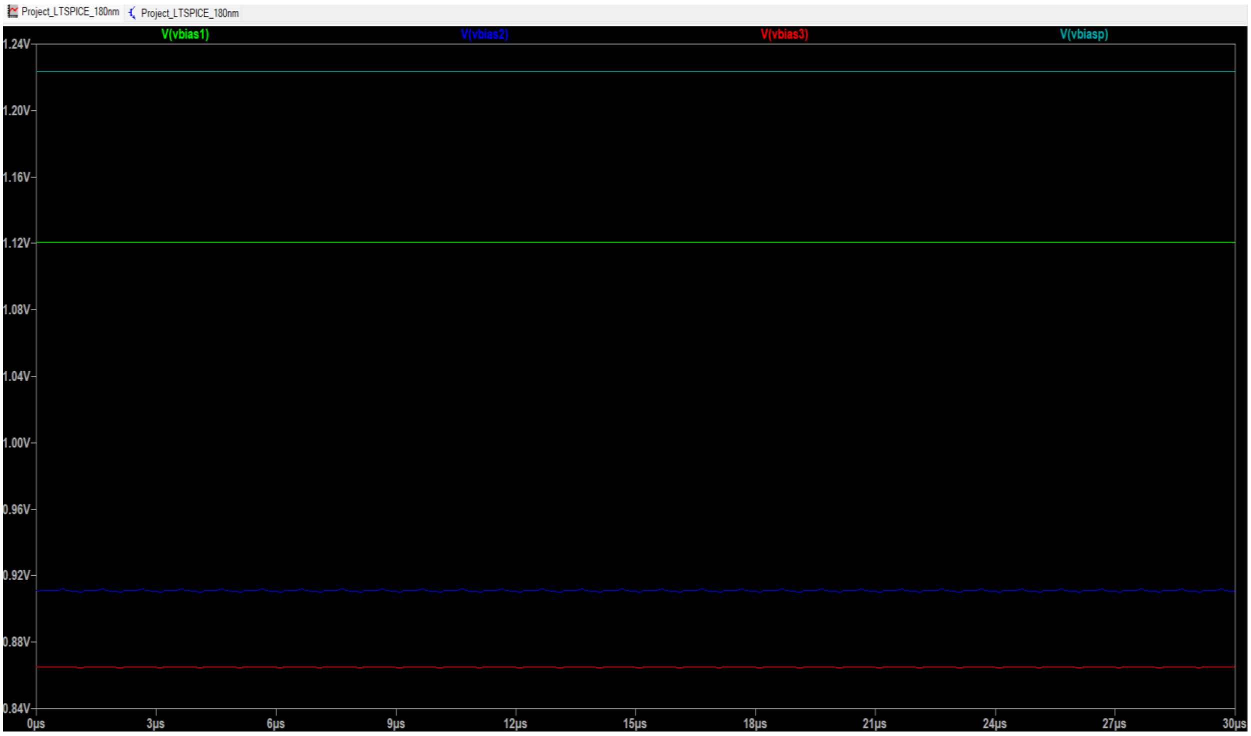


Cascode Amplifier

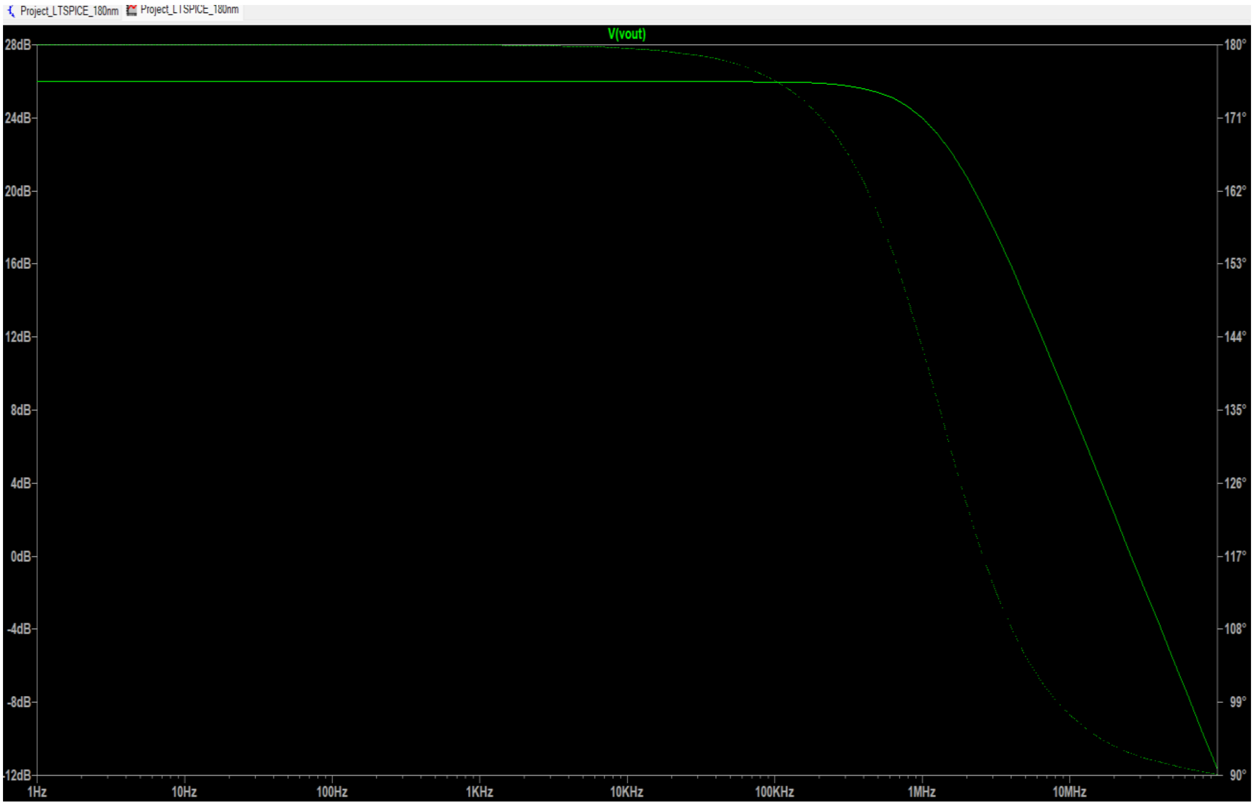
OUTPUT:



OUTPUT WAVEFORM



Vbias Values



Frequency Response

CALCULATION:

Given

$A_v = 20\ V/V$

$C_L = 1pF$

$V_{DD} = 1.8V$

$\mu_n C_{ox} = 350.8\ \mu A/V^2$

$\mu_p C_{ox} = 71.2\ \mu A/V^2$

unity Gain Band width (UGB) > 500 KHz

power Dissipation $(P_D) < 5mW$, $\lambda = 0.09$, $V_{th} = 0.5V$

calculation:

* Assumed Frequency location of pole

$$f_p = \frac{1}{2\pi R_{out} C}$$

* All Frequencies less than this should provide suitable gain

$= 20\log 20 = 26.02\ dB$

Let this f_p be 2.5MHz

$$\therefore 2.5 \times 10^6 = \frac{1}{2\pi \times R_{out} \times 10^{-12}}$$

$\therefore R_{out} = 63661.98\Omega$

* $g_m = \frac{A_v}{R_{out}} = \frac{20}{63661.98} = 0.0003145$

* $g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$

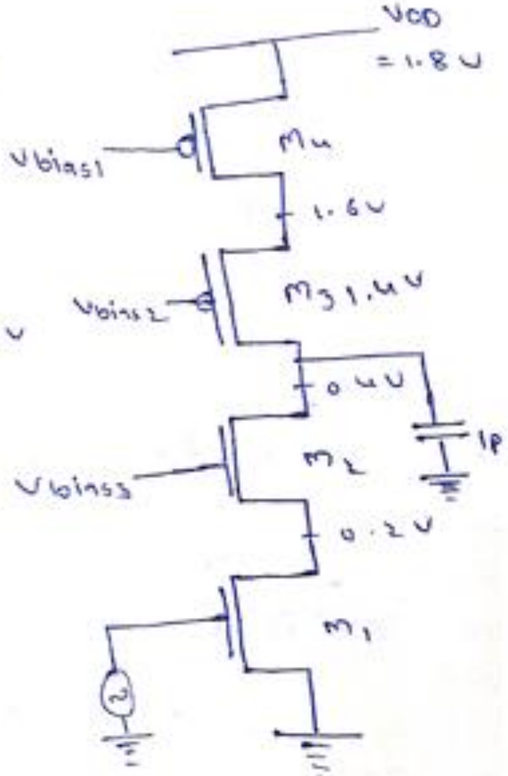
* $g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$

To find V_{ov}

we'll consider all mosfets to be at the edge of saturation.

$$\therefore V_{ov} = V_{DS}$$

also, we are taking drop across each mosfet $= 0.2V$ (by industrial standards).



1) M_1:

$V_D = 0.2V$, $V_S = 0$, $V_{ov} = 0.2V$

$\therefore V_G = 0.2 + V_{th} = 0.7V$

dc value $= V_G = 0.7V$

2) M_2

$V_D = 0.4V$, $V_S = 0.2V$, $V_{ov} = 0.2V$

$V_{ov} = V_{bias3} - V_S - V_{th}$

$\therefore V_{bias3} = 0.2 + 0.2 + 0.5$

$= 0.9V$

$V_{bias2} \le 0.9V$

$\therefore g_m = \mu_n C_{ox} \frac{W}{L} V_{ov}$

$0.000314 = 350.8 \times 10^{-6} \times \frac{W}{L} \times 0.2$

$$\boxed{\frac{W}{L}_{nmos} = 4.480}$$

→ Now, some I_D will flow through all the mosfets.

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V_{ov}^2 (1 + \lambda V_{DS})$$

(assuming the mosfets at edge of saturation)

$$I_D = \frac{1}{2} \times 350.8 \times 10^{-6} \times 0.04 \,(1+0.018)$$

$$= 33.146\,\mu A$$

* since same current flows through m_3 & m_4,

$$I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)' V_{ov}^2\,(1+\lambda V_{DS})$$

$$\left(\frac{W}{L}\right)'_{pmos} = \frac{33.146 \times 2}{71.2 \times 0.04 \times 0.018}$$

$$\left(\frac{W}{L}\right)'_{pmos} = 22.175$$

* power dissipation (P.D) = $V_{DD} \times I_D$

$$= 1.8 \times 32.146\,\mu$$
$$= 0.058 \;(< 5\,mW)$$

* Finding range of V_{bias2} & V_{bias1}:

$V_{ov} = 0.2V$

③ For m_3, $V_D = 1.4V$, $V_S = 1.6V$

For saturation

$$|V_{GS}| - |V_{th}| \leq V_{DS}$$

$$|V_{bias2} - V_S| - |-0.5| \leq |1.4 - 1.6|$$

$$\therefore V_{bias2} \geq 0.9V$$

④ For m_4, $V_D = 1.6V$, $V_S = 1.8V$

$$\therefore V_{bias1} \geq 1.1V$$

$\therefore$ It is 180nm Technology. $L = 180nm$

$\therefore$ W & L for NMOS & PMOS [in cascode amplifier]:

For NMOS

$L = 180nm$, $W = 180 \times 4.488 = 807.84\ nm$

$\frac{W}{L} = 4.488$

For pmos

$L = 180nm$, $W = 180 \times 22.175nm = 3991.5$

$\frac{W'}{L} = 22.175$

⇒ comparing simulation Results and theorectical values.

* v_s is taken to be 100mv [ac value]

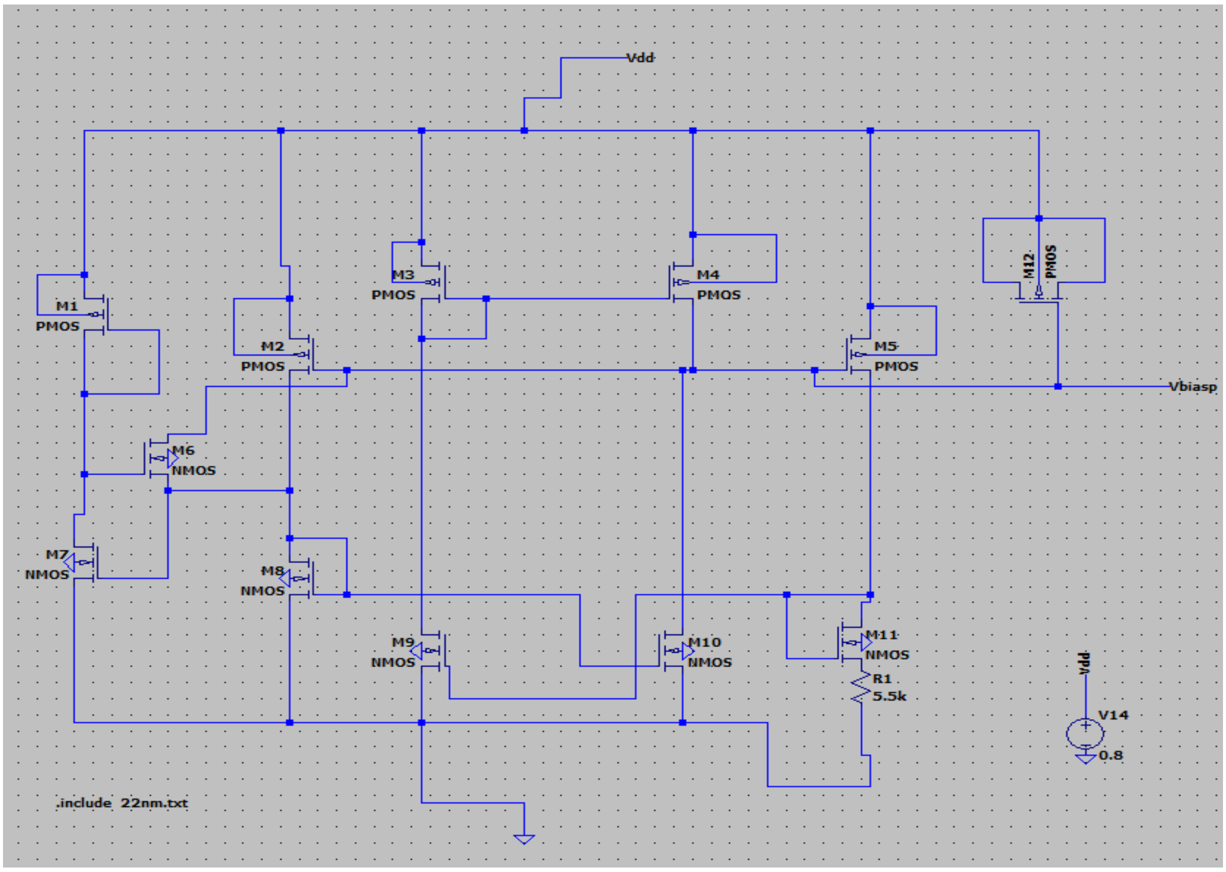
		Theoretical values	simulation values.
1.	Vbiasp	-	1.22 V
2.	Vbias 1	$\geq$ 1.1V	1.12 V
3.	Vbias 2	$\geq$ 0.9V	0.91V
4.	Vbias 3	$\leq$ 0.9V	0.867V
5.	v_s (dc)	0.7V	0.6955V
6.	UGB	> 500 kHz	30.23 MHz
7.	I_D	22.146 μA	22 μA
8.	A_v	26.02 dB	26.01 dB
9.	PD	< 5mW	0.058 mW

* Thus the given simulation satisfies all the requirements.

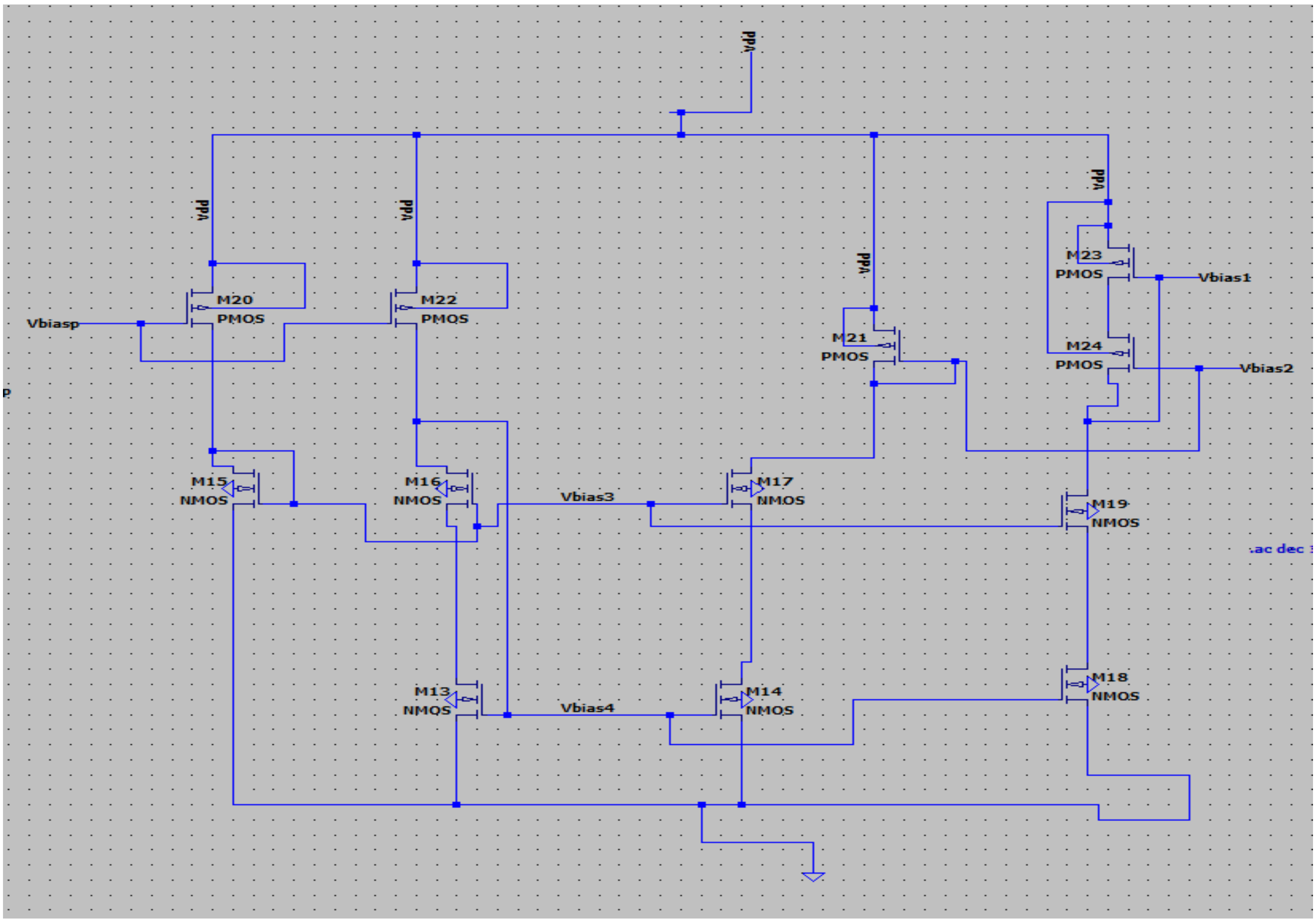
B) 22 nm Technology:

Simulation

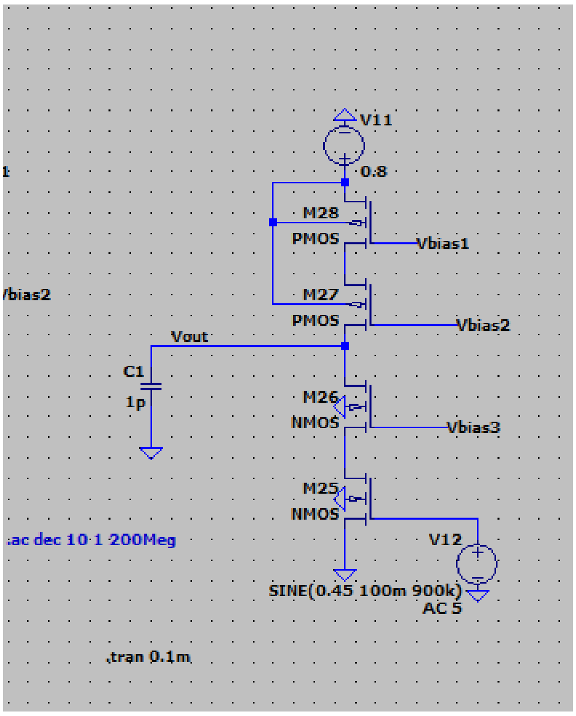
The following images display the LtSpice schematics for the Beta Multiplier, Cascode Current Mirror and Cascode Amplifier circuits designed in 22nm technolagy.In the Beta Multiplier and Cascode Current Mirror circuits, the W/L ratios were configured according to the specified values provided. For the Cascode Amplifer, the W/L ratio was determined through calculations, which are detailed in the following section.



Beta Multiplier



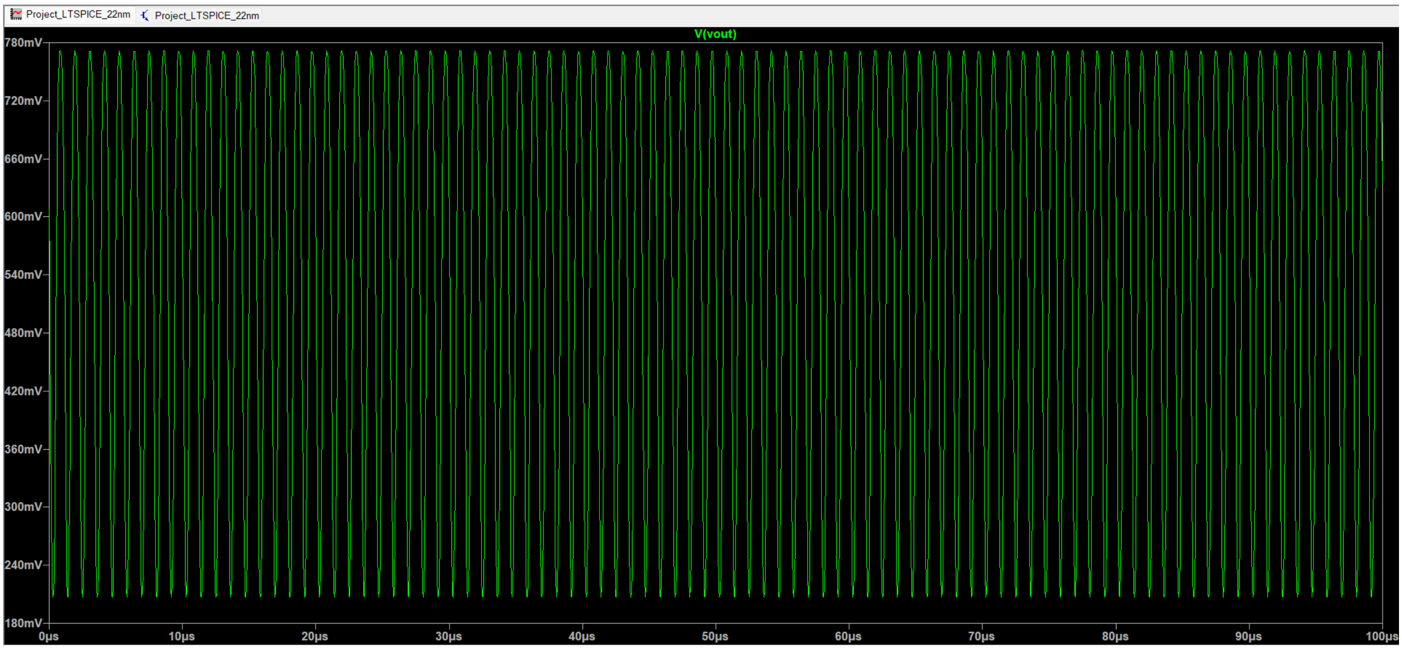
Cascode Current Mirror



Cascode Amplifier

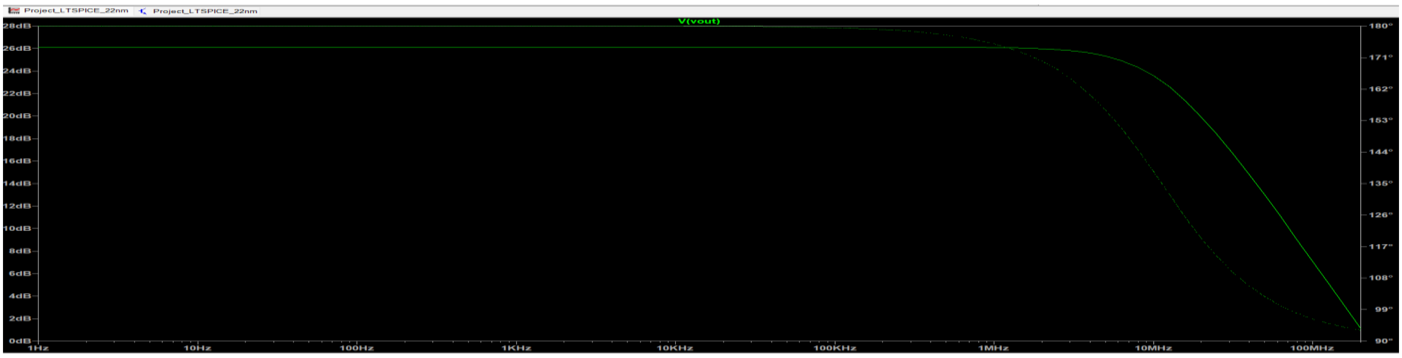
OUTPUT:

The Simulation outputs obtained were:



Output Waveform

Vbias Values



Frequency Response

CALCULATION:

The calculations are similar to 180nm Technology.

Given $A_v = 20\,V/V$

$V_{DD} = 0.8V$

$C_L = 1pF$

Assumed : (For 22nm)

$|V_{th}| = 0.3V$, $\mu_n C_{ox} = 100\,\mu A/V^2$, $\mu_p C_{ox} = 50\,\mu A/V^2$

$V_{ov} = 0.2V$

Frequency Location of pole $f_p = 2.5MHz$

$\rightarrow R_{out} = \frac{1}{2\pi f_p C_L} = 63661.98\Omega$

* $g_m = \frac{A_v}{R_{out}} = 0.000314S$

* $I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{ov}^2$

we knows, $g_m = \mu_n C_{ox}\frac{W}{L}V_{ov}$

$\therefore 0.000314 = 100\times10^{-6}\times\left(\frac{W}{L}\right)\times0.2$

$\left(\frac{W}{L}\right)_{nmos} = 15.7$

* $I_D = \frac{1}{2}\times100\times10^{-6}\times15.7\times0.04$ (Neglecting λ)

$= 31.4\,\mu A$

* since same current flows through m_3 & m_4

$I_D = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)' V_{ov}^2$

$$31.4\times10^{-6} = \frac{1}{2}\times 50\times10^{-6}\left(\frac{W}{L}\right)\times(0.04)$$

$$\boxed{\left(\frac{W}{L}\right)_{pmos} = 31.4}$$

* power dissipation (P.D.)

$= V_{DD}\times I_D$

$= 0.8\times 31.4\,\mu A$

$= 0.025\,mW\ (< 5\,mW)$

⟹ Finding range of V_{bias1}, V_{bias2}, V_{bias3} & V_s:

Assuming the mosfet to be at the edge of saturation.

1) M_1 : $V_D = 0.2V$, $V_S = 0V$, $V_{th} = 0.3V$

$V_G - V_S - V_{th} = V_D - V_S$

$\therefore V_G = 0.2 + 0.3 = 0.5V$

$\boxed{V_G = 0.5V}$

2) M_2 : $V_D = 0.4V$, $V_S = 0.2V$

$\therefore V_{bias3} = 0.2 + 0.3 + 0.2$

$\boxed{V_{bias3} = 0.7V}$

3) M_3 : $V_{GS} - V_{th} \geq -0.2$

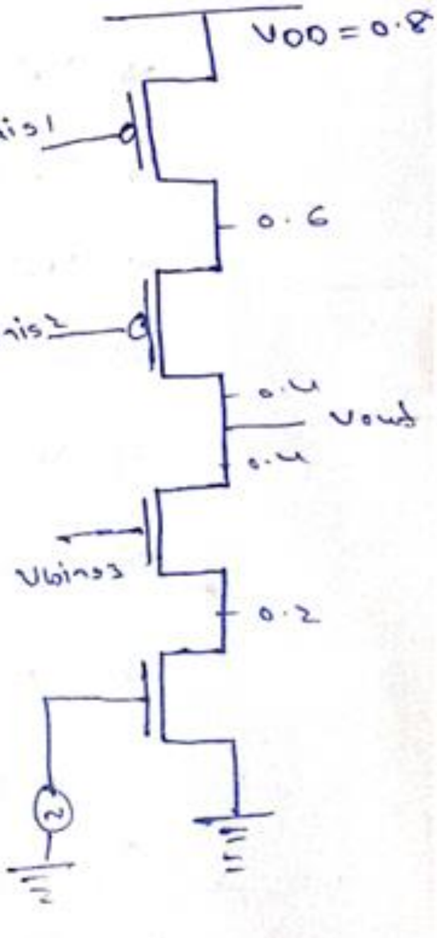
$V_{bias2} + 0.3 \geq -0.2$

$\boxed{\therefore V_{bias2} \geq 0.1V}$

4) M_4 : $V_{GS} - V_{th} \geq -0.2V$

$V_{bias1} - 0.8 + 0.3 \geq -0.2$

$\boxed{\therefore V_{bias1} \geq 0.2V}$



→ W & L calculated

* for NMOS

$L = 22nm, \quad W = 22 \times 15.7 = 345.4nm$

$\frac{W}{L} = 15.7$

* for PMOS

$L = 22nm, \quad W = 22 \times 31.4 = 690nm$

$\frac{W}{L} = 31.4$

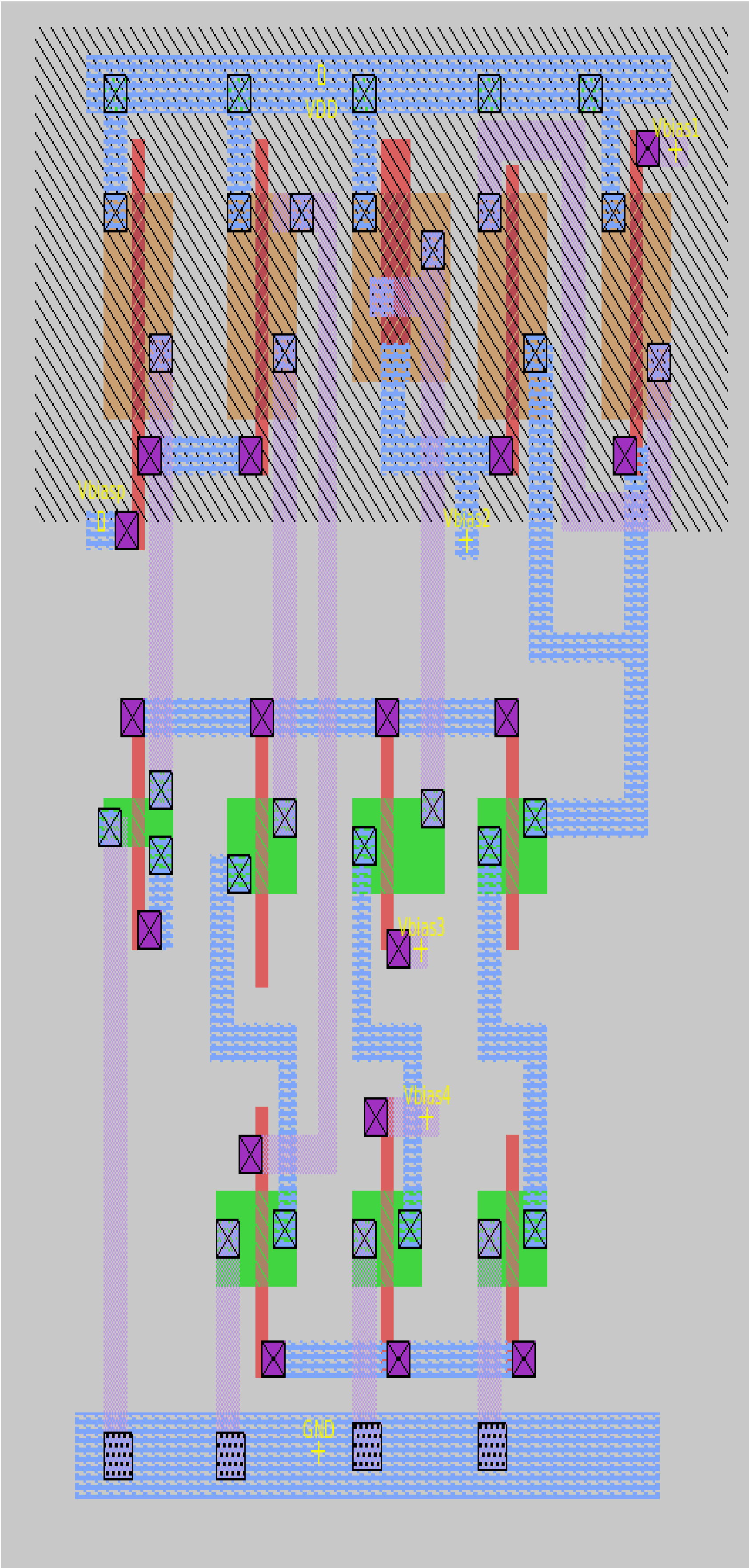
* comparing simulation Results and theoretical values:

		Theoretical values	simulation Results
1)	V_{biasp}	-	248.05mV
2)	V_{bias1}	$\geq 0.2V$	0.24 V
3)	V_{bias2}	$\geq 0.1V$	0.275 V
4)	V_{bias3}	$\leq 0.7V$	0.603 V
5)	$V_S(dc)$	0.5V	0.45 V
6)	V_{GB}	> 500KHz	210 MHz
7)	I_0	31.44 μA	20 μA
8)	A_v	26.02 dB	26.02 dB
9)	P.D	< 5mW	0.025mW

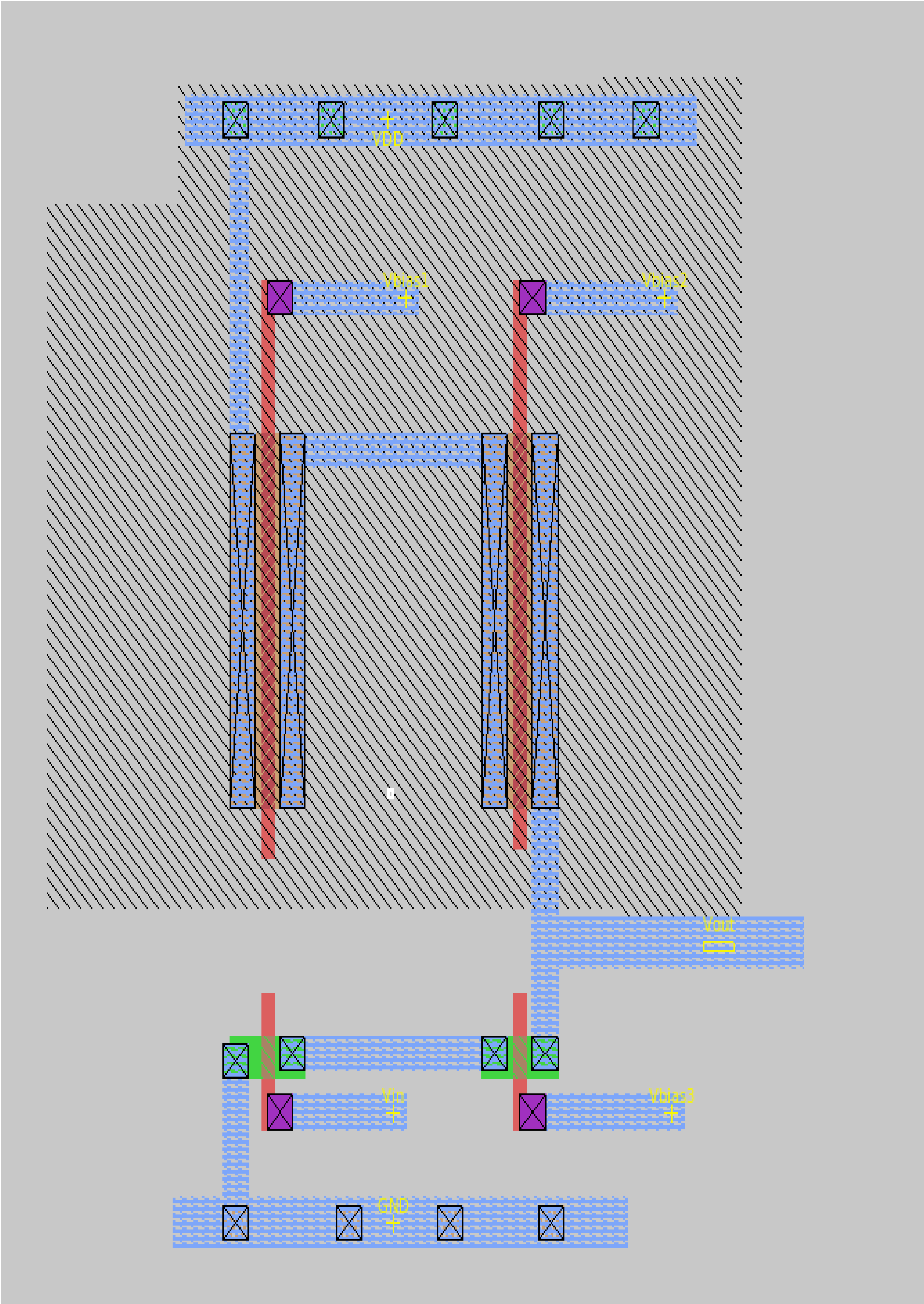
* Thus the given simulation satisfies all the requriments.

Magic Layout (for 180nm Technology):

The Layout is made using the W/L values calculated earlier.



Cascode Current Mirror



Cascode Amplifier

Required Specifications:

- **Gain**: The target gain is 20log(20)dB =26.02dB. The simulations achieved gains of 26 .01 dB for the 180nm technology and 26.02 dB for the22nm technology, meeting the required specification.
- **Power Dissipation**: The power dissipation should be below 5mW . Simulations resulted in power dissipation values of 0.058 mW for 180nm and 0.025 mW for 22nm, both well within the acceptable range.
- **Unity Gain Bandwidth (UGB)**: The UGB must exceed 500kHz . Simulations showed UGB values of 30.22 MHz for 180nm and 210MHz for 22nm, both surpassing the minimum requirement.
- **Frequency Response**: The frequency response for both technologies demonstrates characteristics of a low -pass filter .

All required specifications are successfully met in both the 180nm and 22nm technology simulations.

Difference between 180nm and 22nm Technology:

The 22nm technology has several advantages over the older 180nm technology. In 22nm, both the bias voltages (Vbias) and current levels are generally lower, resulting in reduced power consumption compared to 180nm technology. Additionally, 22nm technology offers a higher unity gain bandwidth and a higher cut-off frequency, meaning it can handle faster signal processing. Because 22nm transistors are much smaller—about eight times smaller than those in 180nm technology—more transistors can be packed onto a single chip, enhancing performance. However, the smaller size of 22nm transistors makes their layouts more complex to design, which can lead to higher design costs.

Conclusion:

we simulated the Beta Multiplier, Cascode Current Mirror, and Cascode Amplifier circuits for both 180nm and 22nm technologies using LTSpice. The simulation results closely matched the theoretical expectations and met all the required performance specifications. We also designed the layouts for the Cascode Current Mirror and Cascode Amplifier in 180nm technology using Magic. Finally, we compared the 180nm and 22nm technologies based on the LTSpice simulations and the Magic layouts.