KLEF
KONERU LAKSHMAIAH EDUCATION FOUNDATION
(Deemed to be university estd, u/s, 3 of the UGC Act, 1956)
(NAAC Accredited "A" Grade University)

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

20IE3150 – MIDGRADE CAPSTONE PROJECT-1 REPORT

ACADEMIC YEAR :2022-2023

III YEAR/V SEMESTER

I2C AND SPI PROTOCOLS DESIGN USING VERILOG

Submitted By

Student Name	Reg Number	Section
K.CHENNA KESHAVA REDDY	2000040320	03
CH. CHARAN TEJA	2000040317	03

BONAFIDE CERTIFICATE

This is to certify that this Project report of Designing a solar power system for home. This bonafide is work of KOTLA CHENNA KESHAV REDDY With Register No. 2000040320 and CHEVURI CHARAN TEJA with Register No. 2000040317 , III Year / V Semester, under the guidance of Dr. NGANGBAM PHALGUNI SINGH Sir, Department of Electronics and Communication Engineering, from **20IE3150 MIDGRADE CAPSTONE PROJECT -1** at Koneru Lakshmaiah Education Foundation in the year 2022-2023.

Signature of the Faculty in charge

Signature of the HOD/ECE

Submitted for the University Practical Examination held on……

INTERNAL EXAMINER

EXTERNAL EXAMINER

ABSTRACT

Currently, the most used serial communication protocols to exchange information between different electronic embedded devices are the SPI and I2C. For the implementation of each protocol, it was considered different modes of operation, such as master/slave mode sending or pending data mode. For the implementation of the I2C protocol was necessary to perform a tri-state buffer, which makes a bidirectional data line for a successful communication between devices, allowing to take advantage of these sources provided by the FPGA. Verilog is a hardware description language better known as HDL and it was used in the work to implement and simulate these communication protocols with the software version 14.7 of Xilinx ISE Design Suite. There are many communication protocols for both short and long-distance communication purpose such as ETHERNET, USB, SATA, PCI-EXPRESS are used for long distance and I2C and SPI are used for short distance communications. SPI is a serial interface protocol, compared to other protocols, it has high transmission speed, simple to use and little pins advantages. The four interfaces are required by standard SPI protocol at least. Usually, the devices which based on SPI protocol are divided into master device and slave-device for transmitting the data. The chip selects signal, and clock signal have been generated by the master-device when the data exchange has been processes is often considered as the “little” communication protocol which is used for On-Board communication

Required Software:

1. Xilinx Vivado

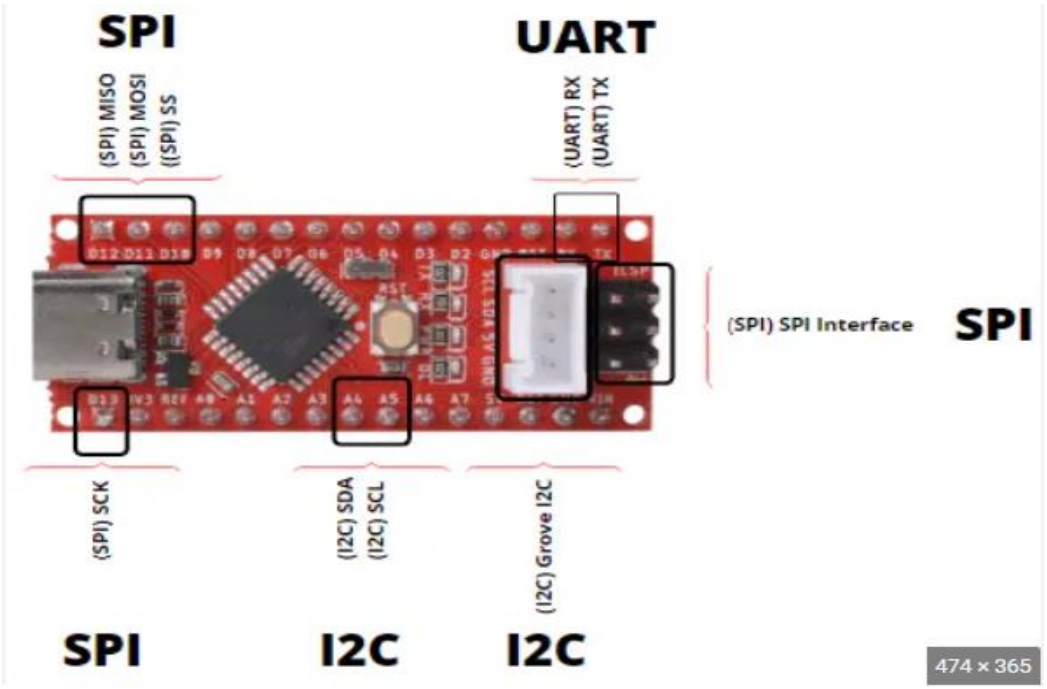
Introduction:

Nowadays, the integration of different embedded electronic modules include at least some of these functions: intelligent control, general purpose circuits, analog and digital I/O data ports, volatile memories (RAM), non-volatile memories (EEPROM, FLASH), real time clocks, ADC, among others. The integration is possible because of the development of different kind of wired and wireless communications. The integrated circuit peripherals allow for the interaction among electronic devices for exchanging data, either the integrated circuit performs the default connection tasks or must be implemented by software. The wired communication protocols SPI e I2C are important for this work, so this paper summarizes their main features. I2C (Inter-Interface Circuit). The I2C bus uses a bit in the device address to indicate read or write operations. The Master transmits the Slave's Address and a Read or Write bit to indicate the direction of the transfer. The I2C bus can be either a single master or multi-master. Each electronic embedded device has a unique 7-bit or 10-bit address and it is limited to 8 bit's transfers. The I2C supports three basic modes of operation providing different levels of performance and device's address mapping: standard mode (up to 100 Kbits/sec, 7 bit addressing); fast mode (up to 400 Kbits/sec, addressing between 7 to 10 bits); high-speed mode (up to 3.4 Mbits/sec, addressing between 7 to 10 bits)

SPI (Serial Protocol Interface). The SPI bus is a 4-wire full-duplex interface synchronous serial data link [3]. Indeed, it is a (3+N)-wire interface where N is the number of devices connected to a single master device on the bus. Only one master can be active on the bus. Unlike I2C, SPI supports a transfer size of integer multiples of 8 bits. Technically the SPI bus shift register's length limits the size of the data transfers. The SPI bus can support a variety of transfer speeds, but the bus is limited by the system´s clock. The SPI interface is generally able data rates of several Mbits/sec. This paper describes the procedure used to implement the synchronous serial communication protocols SPI and I2C by means of the hardware programming language Verilog HDL (Hardware Description Language). The outline of this paper is divided in four sections. Section 2 discusses the research course; section 3 illustrates the methods used in the development of this work. Section 4 reports the obtained results and conclusions.

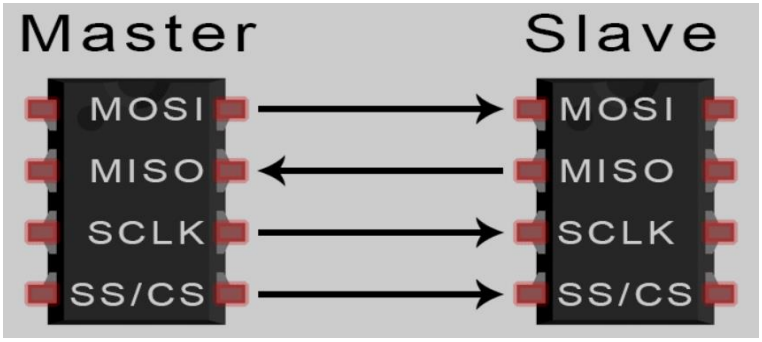
Keywords - Serial Peripheral Interface (SPI), System Verilog, System- on-Chip (SoC), Intellectual Property (IP).

Peripheral Devices:



SPI-PROTOCOL:

Standard SPI is a high-speed, full-duplex, synchronous communication bus [4]. For saving the chip ports and space on PCB layout, the ports of the SPI only take four lines. It is working in the Master-Slave full duplex mode which has one master device and one slave device and requires four lines whose components are SDI (data in), SDO (data out), SCK (clock), SS (Slave select) .When the SPI master wants to send data to a slave, it will pull the SS line low for selecting slave, and activates the clock signal which usable between the master and the slave at same time. The master transmits the data to the MOSI (master's SDO and slave's SDI) line and receives the data from the MISO (master's SDI and slave's SDO) line at the time. SPI is a serial communication protocol, that data is transmitted bit by bit. The clock pulse is provided by SCK and SDI, SDO is based on this pulse to making the data transmission. Data output through the master's SDO line at the rising or falling edge of the clock and be read by slave in the falling or rising edge followed. So 8-bit data transfer need at least 8 times the clock signal changes



SPI Signal Descriptions:

Master In Slave Out (MISO)

The MISO line is configured as an input in a master device and as an output in a slave device. It is one of the two lines that transfer serial data in one direction, along with the most significant bit sent first. The MISO line of a slave device is placed in the high-impedance state if the slave is not selected.

SPI Interface Signals		
PICname	**Master**	**Slave**
SCK	Serial clock output from master [SCK]	Input to Slave[SCK]
SDO	Serial data output from master[MOSI]	Input to slave[MOSI]
SDI	Serial data input from slave [MISO]	Output from slave[MISO]
SS	Optional slave (chip) select [SS]	Slave select [SS]

Master Out Slave In (MOSI) The MOSI line is configured as output in a master device and as an input in a slave device. It is one of the two lines that transfer serial data in one direction, with the most significant bit sent first

Serial Clock (SCK) The serial clock is used to synchronize data movement both in and out of the device through its MOSI and MISO lines. The Master and Slave devices are capable of exchanging a byte of information during a sequence of eight clock cycles. Since SCK is generated by the master device, this line becomes an input on a slave device.

Slave Select (SS bar) The slave select input line is used to select a slave device. It has to be low prior to data transactions and must stay low for the duration of the transaction.

SPI DATA TRANSMISSION:

The SPI has four modes of operation, 0 through 3. These modes essentially control the way data is clocked in or out of an SPI device. The configuration is done by two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock. The clock phase (CPHA) control bit selects one of the two fundamentally different transfer formats. To ensure a proper communication between master and slave both devices have to run in the same mode. This can require a reconfiguration of the

SPI MODE	CPOL	CPHA	SHIFT SCK EDGE	CAPTURE SCK EDGE
0	0	0	Falling	Raising
1	0	1	Raising	Falling
2	1	0	Raising	Falling
3	1	1	Falling	Raising

master to match the requirements of different peripheral slaves. SPI is a Synchronous data transmission; Clock plays important role in this Communication. For describing the clock information, we have two flags called CPOL and CPHA in SPI Control Register. The CPOL clock polarity control bit specifies an active high or low clock. The CPHA clock phase control bit selects one of two different transmission formats. The communication is initiated by the master all the time. The master first configures the clock, using a frequency, which is than or equal to the maximum frequency that the slave device supports. The master then selects the desired slave for communication by pulling the chip select (SS) line of that slave-peripheral to low state. Data transfer is organized by using Shift register with some given word size such as 8- bits in both master and slave. They are connected in a ring. While master shifts register value out through MOSI line, the slave shifts data in to its shift register and sends data to master from slave by MISO line

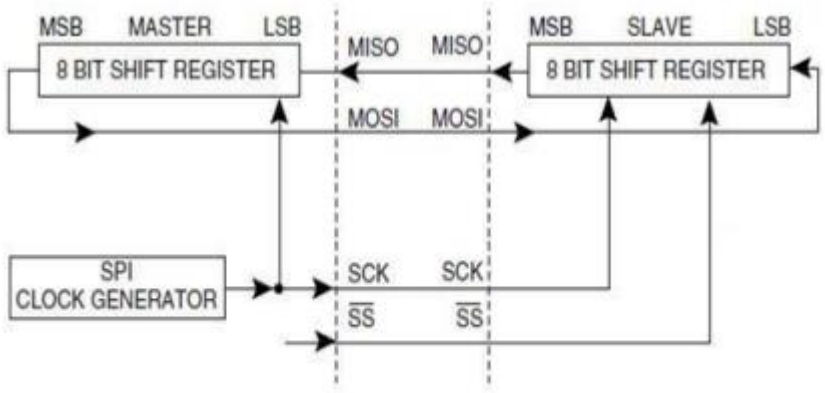
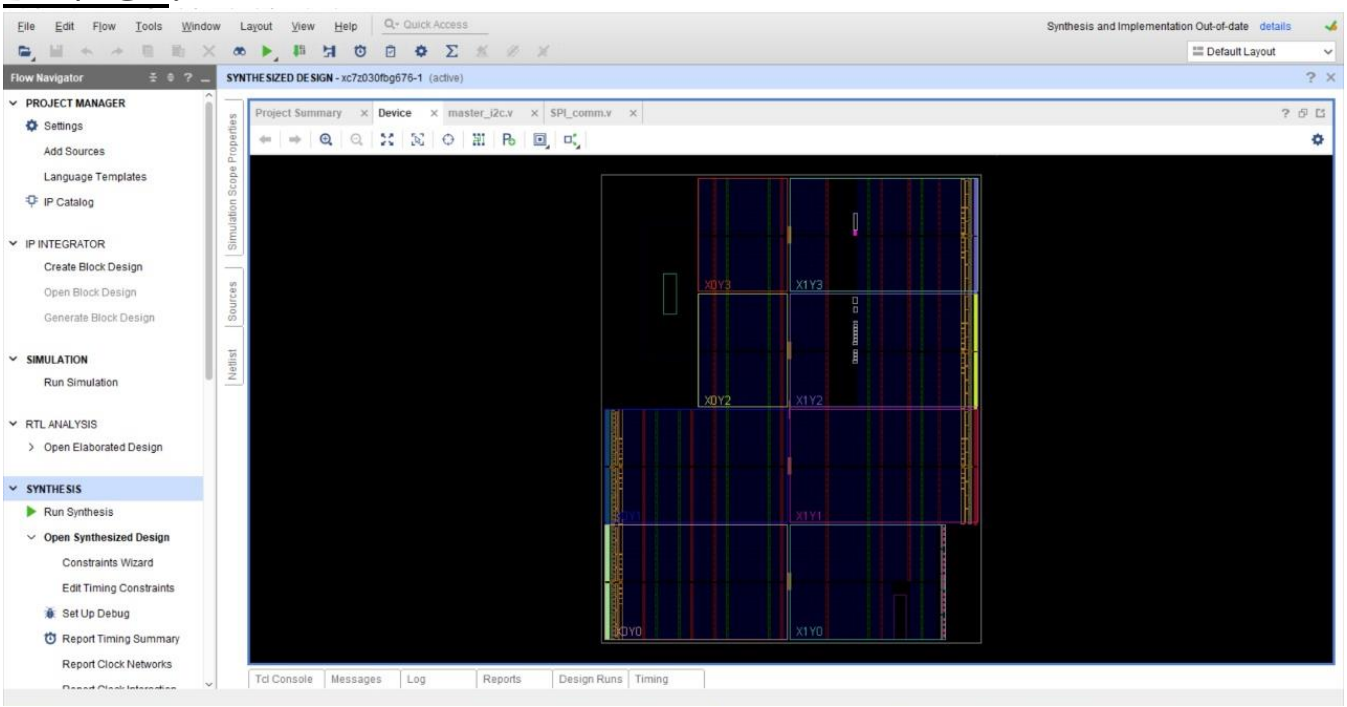
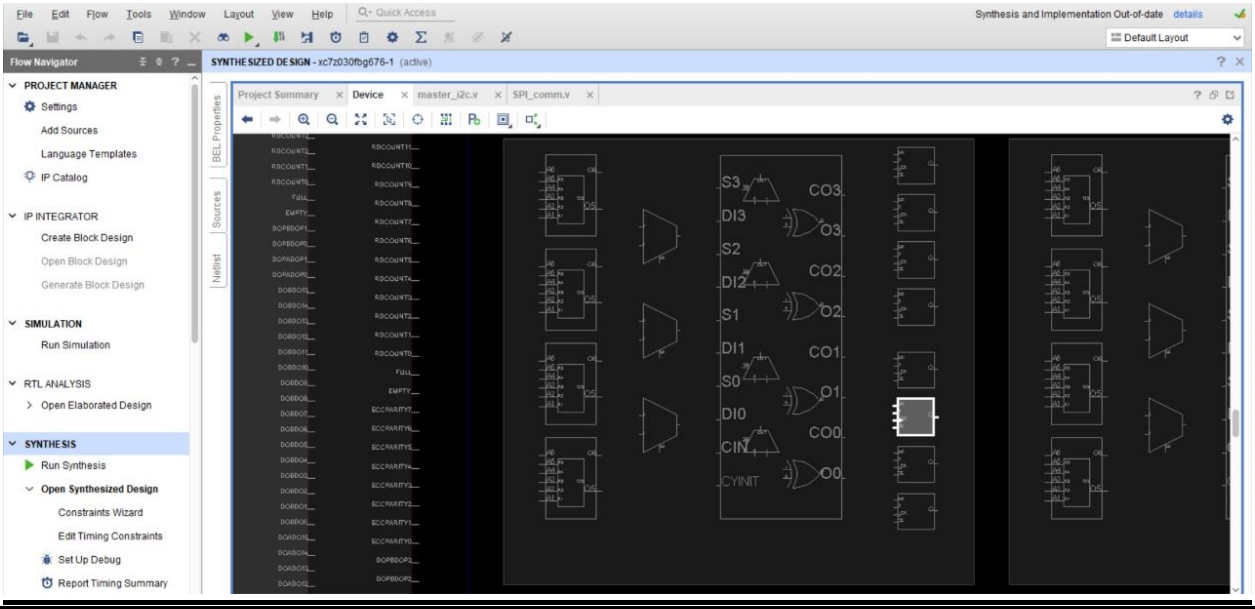


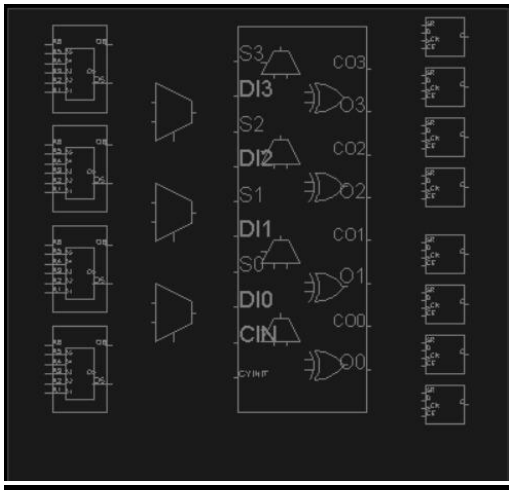
Figure2: SPI Data Transmission of 8-bit from Master to slave

DEVICE:



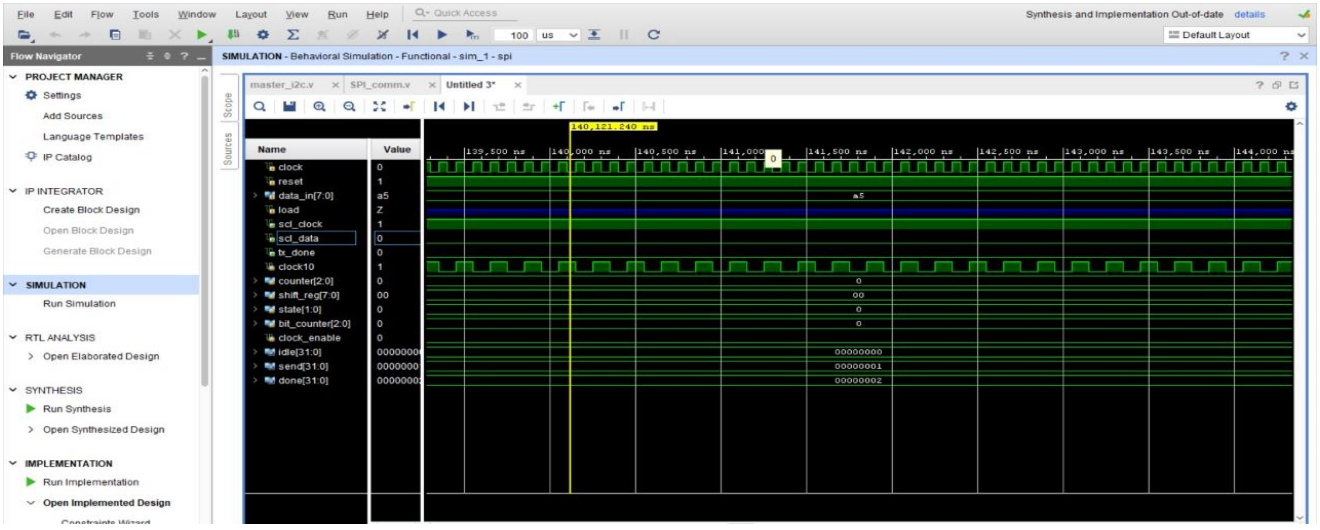


The individual LOOKUP T :



OUTPUT GRAPHS :

The output graphs of SPI protocol in Xilinx vivado software :



I2C(Inter-Integrated Circuit) :

In serial communication protocol, RS232, Rs485 and SPI(Serial Peripheral Interface) require more pins and pins are costly resources in VLSI. Inter-Integrated Circuit (I2C) is a bidirectional, half duplex, 2-wire serial communication protocol developed by Philips. I2C is a multi-master , multi-slave and single ended communication protocol, where each of that device can be addressed by its unique address with just a two general purpose I/O pins SDA (serial data line) and SCL (serial clock line).

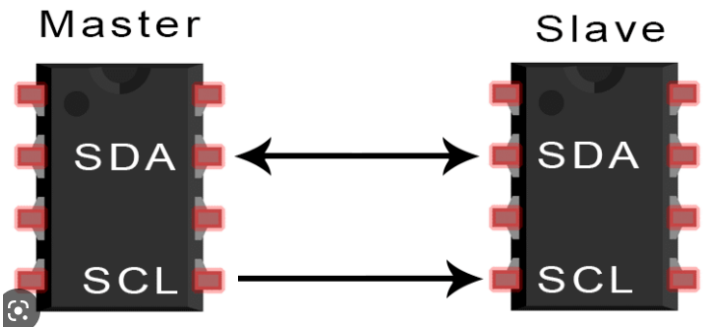
SCL acts as a clock line for I2C bus where SDA acts as a data line. It is typically used for attaching lower-speed peripheral Integrated circuit to microprocessors and microcontroller in short-distance, intra-board communication. There are many versions of I2C according to communication speed.

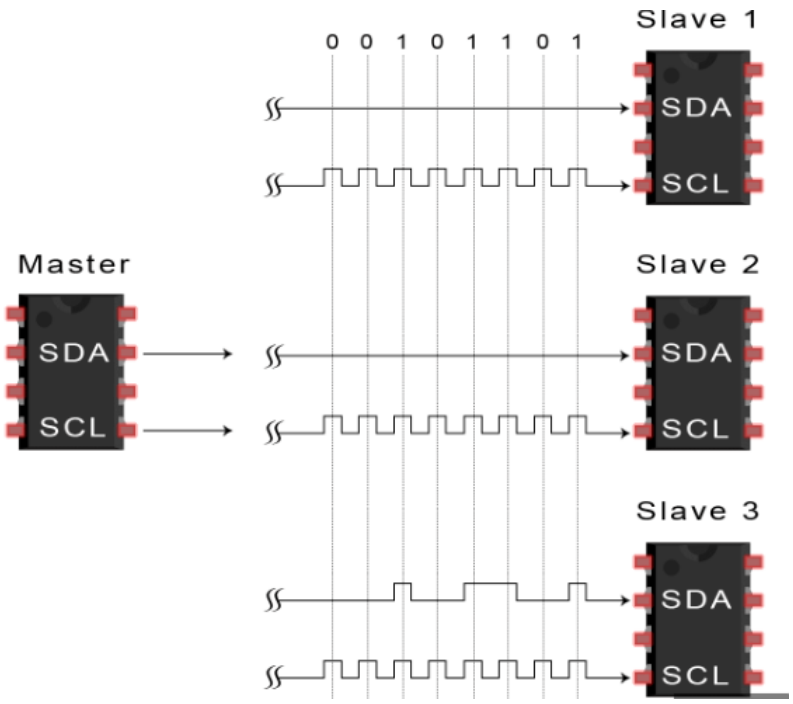
So implementation of master slave I2C in Hardware Description Language (HDL) like Verilog helps to understand how two devices communicate using master and slave technology. Verilog coding help to verify all possible options to test master and slave module. The I 2C bus is a standard bidirectional interface that uses a controller, known as the master, to communicate with slave devices.

A slave may not transmit data unless it has been addressed by the master. Each device on the I 2C bus has a specific device address to differentiate between other devices that are on the same I 2Cbus. The physical I 2C interface consists of the serial clock (SCL) and serial data (SDA) lines.

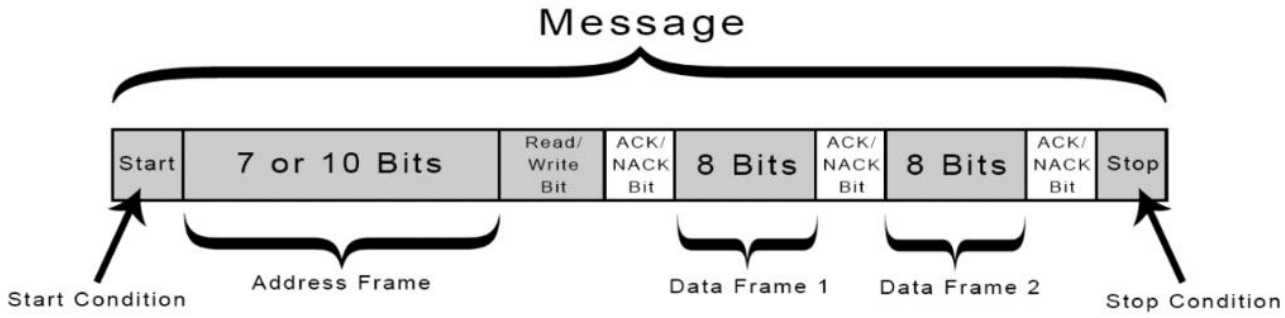
Specification :

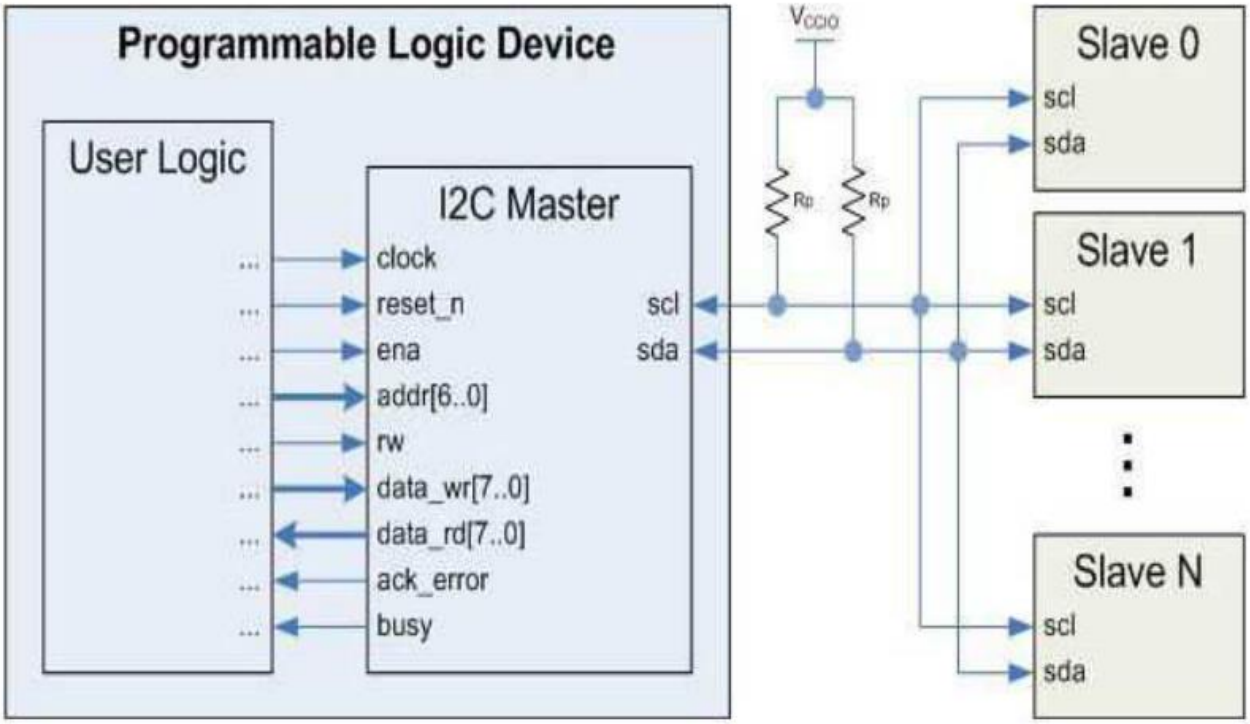
♣ **Serial clock(SCL)**: Master sends serial clock signal to control data transfer process between slave and master.
♣ **Serial Data(SDL):** The data transfer between master and slave, vice versa takes place using SDL signal.



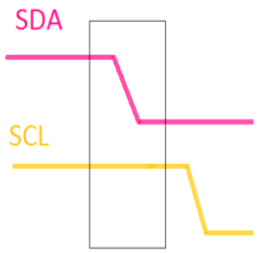


FRAME FORMAT:

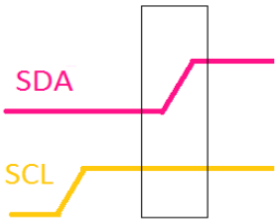




- **Start** – high-to-low transition of the SDA line while SCL line is high



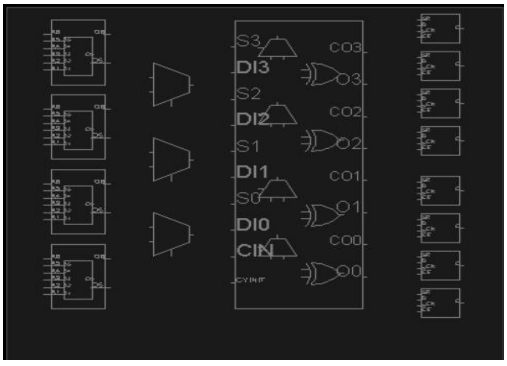
- **Stop** – low-to-high transition of the SDA line while SCL line is high.



DEVICE:

The layouts of lookup tables in the device：

Individual Lookup table：



Output Graphs：