Αρχιτεκτονική Προηγμένων Υπολογιστών και Επιταχυντών Lab 2 Report

Δάιος Γρηγόριος - **ΑΕΜ** 10334
Παπαδάκης Κωνσταντίνος Φώτιος - **ΑΕΜ** 10371

December 23, 2025

Contents

Chapter 1

Console Output

When running the software and hardware emulation we note significantly larger “Load Binary File to Alveo U200” times. This increase can be attributed to the need to run an internal HDL simulator capable of accurately showcasing the kernel’s behavior.

1.1 Software

```
<terminated> (exit value: 0) SystemDebugger_lab2_system_lab2 [OpenCL] /mnt/data2/lab_fpga/student8/lab2/Emulation-SW/lab2 (12/19/25, 12:47 PM)
[Console output redirected to file:/mnt/data2/lab_fpga/student8/lab2/Emulation-SW/SystemDebugger_lab2_system_lab2.launch.log
Found Platform
Platform Name: Xilinx
INFO: Reading /mnt/data2/lab_fpga/student8/lab2_system/Emulation-SW/binary_container_1.xclbin
Loading: '/mnt/data2/lab_fpga/student8/lab2_system/Emulation-SW/binary_container_1.xclbin'
Trying to program device[0]: xilinx_u200_gen3x16_xdma_2_202110_1
Kernel Name: imageDiffPosterize_1, CU Number: 0, Thread creation status: success
Device[0]: program successful!
Kernel Name: imageDiffPosterize_1, CU Number: 0, State: Start
Kernel Name: imageDiffPosterize_1, CU Number: 0, State: Running
Kernel Name: imageDiffPosterize_1, CU Number: 0, State: Idle
----------------- Key execution times -----------------
Allocate Memory in Host Memory                          :    0.410 ms
Fill the buffers                                        :    0.168 ms
Run Software Reference                                  :    0.334 ms
Load Binary File to Alveo U200                          :   29.061 ms
Allocate Buffer in Global Memory                        :    0.219 ms
Set the Kernel Arguments                                :    0.040 ms
Copy input data to device global memory                 :    0.321 ms
Launch the Kernel                                       :    0.423 ms
Copy Result from Device Global Memory to Host Local Memory :    2.255 ms
Compare the results of the Device to the simulation     :    0.055 ms
TEST PASSED
device process sw_emu_device done
Kernel Name: imageDiffPosterize_1, CU Number: 0, Status: Shutdown
```

Figure 1.1: sw_emu

1.2 Hardware

```
<terminated> (exit value: 0) SystemDebugger_lab2_system_1_lab2 [OpenCL] /mnt/data2/lab_fpga/student8/lab2/Emulation-HW/lab2 (12/19/25, 2:19 PM)
[Console output redirected to file:/mnt/data2/lab_fpga/student8/lab2/Emulation-HW/SystemDebugger_lab2_system_1_lab2.launch.log]
Found Platform
Platform Name: Xilinx
INFO: Reading /mnt/data2/lab_fpga/student8/lab2_system/Emulation-HW/binary_container_1.xclbin
Loading: '/mnt/data2/lab_fpga/student8/lab2_system/Emulation-HW/binary_container_1.xclbin'
Trying to program device[0]: xilinx_u200_gen3x16_xdma_2_202110_1
INFO: [HW-EMU 05] Path of the simulation directory : /mnt/data2/lab_fpga/student8/lab2/Emulation-HW/.run/15940/hw_em/device0/binary_0/be
INFO: [HW-EMU 01] Hardware emulation runs simulation underneath. Using a large data set will result in long simulation times. It is reco
configuring dataflow mode with ert polling
scheduler config ert(1), dataflow(1), slots(16), cudma(0), cuisr(0), cdma(0), cus(1)
Device[0]: program successful!
----------------- Key execution times -----------------
Allocate Memory in Host Memory                           :    0.528 ms
Fill the buffers                                         :    0.268 ms
Run Software Reference                                   :   17.265 ms
Load Binary File to Alveo U200                           : 43448.398 ms
Allocate Buffer in Global Memory                         :  141.558 ms
Set the Kernel Arguments                                 :    0.043 ms
Copy input data to device global memory                  :    0.305 ms
Launch the Kernel                                        :    0.060 ms
Copy Result from Device Global Memory to Host Local Memory : 171210.906 ms
Compare the results of the Device to the simulation      :    0.052 ms
TEST PASSED

 socket connect is not established/broken
INFO: [HW-EMU 06-0] Waiting for the simulator process to exit
INFO: [HW-EMU 06-1] All the simulator processes exited successfully
INFO: [HW-EMU 07-0] Please refer the path "/mnt/data2/lab_fpga/student8/lab2/Emulation-HW/.run/15940/hw_em/device0/binary_0/behav_wavefo
```

Figure 1.2: hw_emu

Chapter 2

Kernels and Compute Units

The compute unit which the kernel instantiates runs around 2 times faster on the hardware emulation when compared to the software emulation. This means that the hardware-wise optimizations were able to achieve better performance even though it wasn't that impressive.

2.1 Software

Kernels & Compute Units

Kernel Execution

Kernel	Enqueues	Total Time (ms)	Min Time (ms)	Avg Time (ms)	Max Time (ms)
imageDiffPosterize	1	0.959	0.959	0.959	0.959

Top Kernel Execution

Kernel	Kernel Instance Address	Context ID	Command Queue ID	Device	Start Time (ms)	Duration (ms)
imageDiffPosterize	0x5575039e3120	0	0	xilinx_u200_gen3x16_xdma_2_202110_1-0	30.706	0.959

Compute Unit Utilization

Compute Unit	Kernel	Device	Calls	Dataflow Execution	Max Parallel Executions	Dataflow Acceleration	CU Device Utilization (%)	CU Kernel Utilization (%)	Total Time (ms)	Min Time (ms)	Avg Time (ms)	Max Time (ms)	Clock Freq (MHz)
imageDiffPosterize_1	imageDiffPosterize	xilinx_u200_gen3x16_xdma_2_202110_1-0	1	No	0	1.000000x	92.894	92.894	0.891	0.891	0.891	0.891	300.000

Figure 2.1: sw_kernels

2.2 Hardware

Kernels & Compute Units

Kernel Execution (includes estimated device times)

Kernel	Enqueues	Total Time (ms)	Min Time (ms)	Avg Time (ms)	Max Time (ms)
Name of kernel	1	0.513	0.513	0.513	0.513

Top Kernel Execution

Kernel	Kernel Instance Address	Context ID	Command Queue ID	Device	Start Time (ms)	Duration (ms)
imageDiffPosterize	0x559d10396e30	0	0	xilinx_u200_gen3x16_xdma_2_202110_1-0	0.039	0.513

Compute Unit Utilization (includes estimated device times)

Compute Unit	Kernel	Device	Calls	Dataflow Execution	Max Parallel Executions	Dataflow Acceleration	CU Device Utilization (%)	CU Kernel Utilization (%)	Total Time (ms)	Min Time (ms)	Avg Time (ms)	Max Time (ms)	Clock Freq (MHz)
imageDiffPosterize_1	imageDiffPosterize	xilinx_u200_gen3x16_xdma_2_202110_1-0	1	Yes	1	1.000000x	98.061	98.061	0.503	0.503	0.503	0.503	300.000

Figure 2.2: hw_kernels

Chapter 3

Kernel Data Transfers

On the hardware emulation implementation we can see that the kernel transfers are comprised of 14487 reads and 592 writes. Bandwidth utilization is 78% on the writes and 70% on the reads. There is space for improvement.

3.1 Hardware

Kernel Data Transfers

Kernel Transfer

Compute Unit Port	Kernel Arguments	Device	Memory Resources	Transfer Type	Number of Transfers	Transfer Rate (MB/s)	BW Util wrt Current Port Config (%)	BW Util wrt Ideal Port Config (%)	Max BW on Current Port Config (MB/s)	Max BW on Ideal Port Config (MB/s)	Avg Size (KB)	Avg Latency (ns)
imageDiffPosterize_1/m_axi_gmem	A|B|C|C_filt	xilinx_u200_gen3x16_xdma_2_202110_1-0	DDR[1]	WRITE	592	945.413	78.784	4.924	1200.000	19200.000	0.055	17.568
imageDiffPosterize_1/m_axi_gmem	A|B|C|C_filt	xilinx_u200_gen3x16_xdma_2_202110_1-0	DDR[1]	READ	14487	848.548	70.712	4.420	1200.000	19200.000	0.006	3.987

Top Kernel Transfer

Compute Unit	Device	Number of Transfers	Avg Bytes per Transfer	Transfer Efficiency (%)	Total Data Transfer (MB)	Total Write (MB)	Total Read (MB)	Total Transfer Rate (MB/s)
imageDiffPosterize_1	xilinx_u200_gen3x16_xdma_2_202110_1-0	15079	8.000	0.196	0.121	0.033	0.088	872.740

Figure 3.1: hw_kernel_data_trans

Chapter 4

Host Data Transfers

Here we see clearly what we implemented in our code. The host writes from CPU RAM (DRAM) to the FPGA's global memory the 2 matrices **A** and **B** and when the kernel concludes its execution the host can read the **C_filt** matrix to compare with the software reference in the host/testbench code.

4.1 Software

Host Data Transfers

Host Transfer

No data. To generate data run Hardware Emulation or on Hardware Platform. See Profiling the Application

Top Memory Writes

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Writing Rate (MB/s)
0x2000	0	0	30.144	N/A	32.768	N/A
0xa000	0	0	30.575	N/A	49.152	N/A

Top Memory Reads

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Reading Rate (MB/s)
0xa000	0	0	31.738	N/A	32.768	N/A

Figure 4.1: sw_data_trans

4.2 Hardware

Host Data Transfers

Host Transfer

Context:Number of Devices	Transfer Type	Number of Buffer Transfers	Transfer Rate (MB/s)	Avg Bandwidth Utilization (%)	Avg Size (KB)	Total Time (ms)	Avg Time (ms)
context0:1	READ	1	0.761	N/A	32.768	N/A	N/A
context0:1	WRITE	2	1.185	N/A	40.960	N/A	N/A

Top Memory Writes

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Writing Rate (MB/s)
0x800000000	0	0	43602.600	N/A	32.768	N/A
0x800008000	0	0	43647.300	N/A	49.152	N/A

Top Memory Reads

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Reading Rate (MB/s)
0x800008000	0	0	214759.000	N/A	32.768	N/A

Figure 4.2: hw_host_data_trans

Chapter 5

Timeline

5.1 Software

Entire timeline:

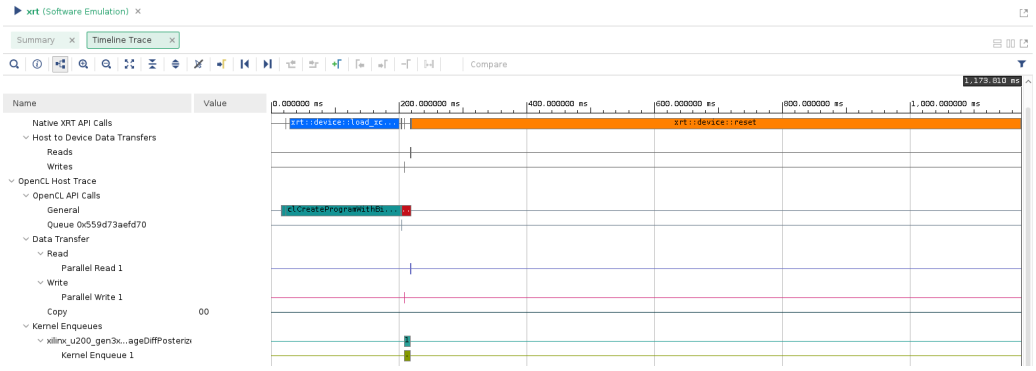


Figure 5.1: sw_timeline

Zoomed in:

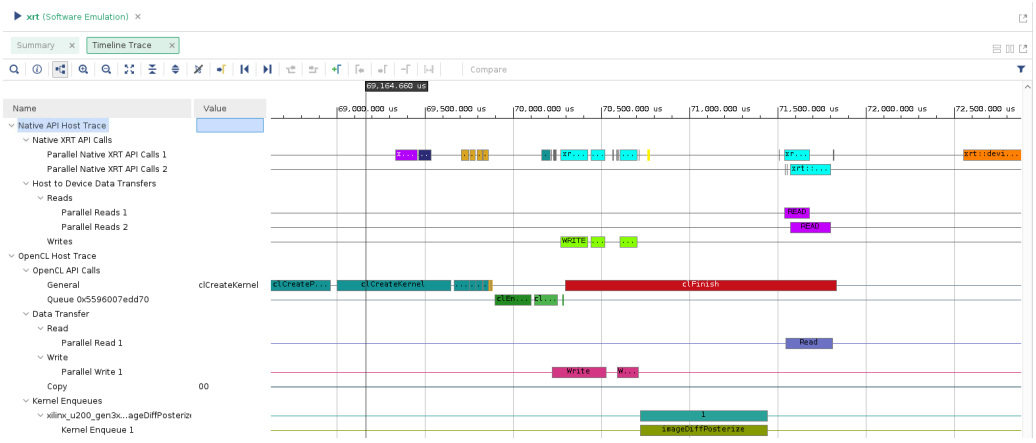


Figure 5.2: sw_timeline_zoom

5.2 Hardware

Entire timeline:

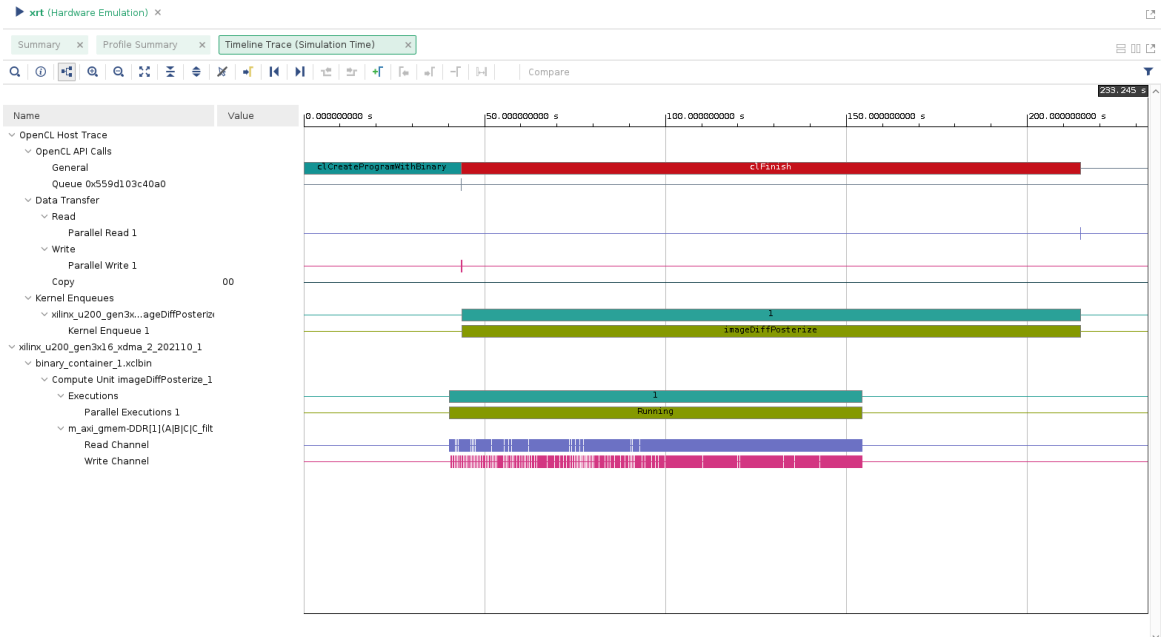


Figure 5.3: hw_timeline

Zoomed in at around 42 - 45 seconds:

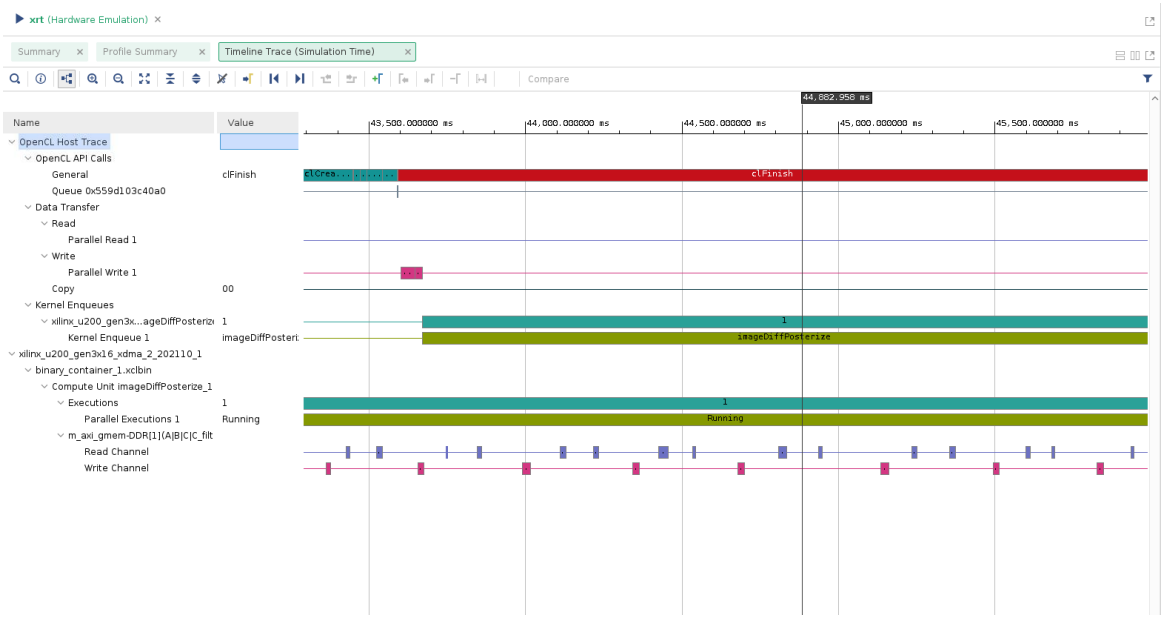


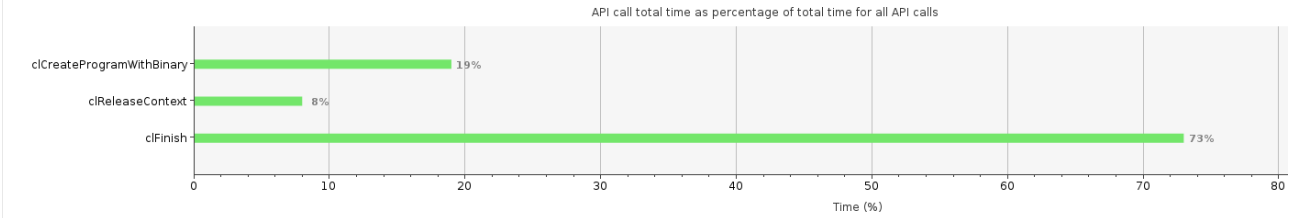
Figure 5.4: hw_timeline_zoom

Chapter 6

API Calls

6.1 Hardware

API Calls: OpenCL API Calls



API Name	Calls	Total Time (ms)	Min Time (ms)	Avg Time (ms)	Max Time (ms)
clCreateBuffer	4	141.521	20.878	35.380	49.547
clCreateCommandQueue	1	0.017	0.017	0.017	0.017
clCreateContext	1	13.486	13.486	13.486	13.486
clCreateKernel	1	1.116	1.116	1.116	1.116
clCreateProgramWithBinary	1	43364.200	43364.200	43364.200	43364.200
clEnqueueMigrateMemObjects	2	0.269	0.006	0.135	0.263
clEnqueueTask	1	0.056	0.056	0.056	0.056
clFinish	1	171211.000	171211.000	171211.000	171211.000
clGetDeviceIDs	2	0.006	0.002	0.003	0.004
clGetDeviceInfo	2	0.025	0.004	0.013	0.021
clGetPlatformIDs	2	0.023	0.002	0.012	0.021
clGetPlatformInfo	2	0.003	0.001	0.002	0.002
clReleaseCommandQueue	1	0.010	0.010	0.010	0.010
clReleaseContext	1	18355.000	18355.000	18355.000	18355.000
clReleaseDevice	4	0.018	0.002	0.005	0.008
clReleaseKernel	1	84.538	84.538	84.538	84.538
clReleaseMemObject	12	0.027	0.001	0.002	0.006
clReleaseProgram	1	0.005	0.005	0.005	0.005
clRetainDevice	4	0.014	0.001	0.004	0.010
clRetainMemObject	8	0.014	0.001	0.002	0.003
clSetKernelArg	5	0.033	0.002	0.007	0.017

Figure 6.1: hw_api_calls

Chapter 7

Zip Contents

- lab2.cpp
  - Final form of lab2's kernel. Run on Vitis.
- tb_lab2.cpp
  - The host which manages the lab2's kernel. Run on Vitis.
- lab2.pdf
  - This report