2022

Low-Level HW Digital Systems I

LAB MANUAL

Contents

1 Introduction

This document describes briefly the prerequisites required to set up the tools for compiling, simulating, and verifying the circuits you will design as part of the coursework for this course. The document is divided into two sections. The following section includes some guidelines regarding the simulators you can use and some concise instructions on how to install and use a simulator offered for free for Intel's FPGAs. Section **Error! Reference source not found.** describes the simulator set up, the coursework you need to complete and the deliverables.

2 Simulation Tools

A well-established tool for RTL simulation has been the Modelsim simulator [1] of Mentor-Graphics (now part of Siemens). Unfortunately, the student edition of this great tool is not available any longer. Thus, you need to seek another simulator that effectively have integrated Modelsim in their environment. There are few available options, which you can use for free for student projects. These options include, for example, the Quartus tool from Intel [2] and Libero® SoC Design Suite from Microchip [3].

We recommend the use of Quartus provided on [2], which supports both a Windows and a Linux version. Unfortunately, there are no simulation tools that we know of and presently support Mac OS. Thus, Mac users need to find a work around. In the following, we succinctly describe how to install and use the Intel simulator. Note that we cannot offer you any technical support on this topic (I managed to get the tool up and running, hence, I am confident you will have no problems either).

2.1 Questa – Intel FPGA Edition

Follow the steps below to install the Quartus simulator for RTL simulation. Alternatively, you can use any other tools you like.

- Go to [2], click on Individual files in the Download Section and select to download the Questa*-Intel® FPGA Edition. Please check you have sufficient disk space to proceed with the installation. Although the tool requires about 1 GB during the installation process you may need much more (possibly up to 30 GB [4]). Also, check the memory requirements of the simulator (as with any other tool).
- During the installation process, you SHOULD select Intel FPGA **Starter** Edition as only this edition offers a free license for 1 year.
- Once the tool installation is complete, a process that takes quite long (tens of minutes depending on your computer), you need to acquire a license file. Please visit the Intel® FPGA Self Service Licensing Center (SSLC) and sing up using your **institutional email** (please do not use your personal email, e.g., gmail).
- After registration, you will receive a confirmation email from Intel. Using this email, log on SSLC and click on the "Sign up for Evaluation or Free Licences" tab and select Questa*-Intel® FPGA Starter Edition, as depicted in Fig. 1, where you edit the number of seats to one. Click on "Get license".

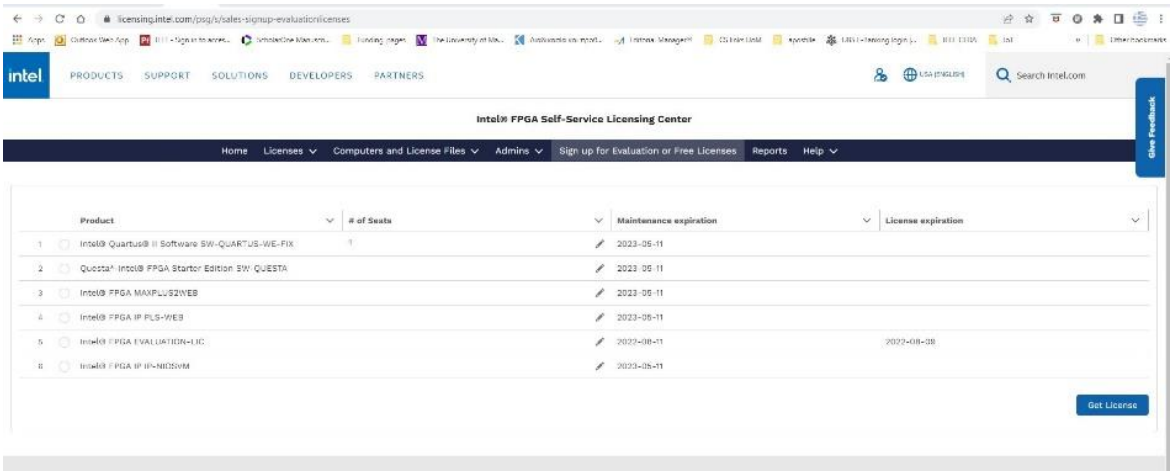

Fig. 1. SSCL Screen

- You will need to provide the NIC of your computer (physical or MAC address of your Ethernet or wireless card, which consists of 12 hex digits) that is used identify your computer (execute `ipconfig -all` on the Windows command prompt to obtain this hex number). Please note that you can support up to 3 devices with the same license file. In this case, you need to install the software on all three machines. In addition, note that you cannot run the software remotely but only locally with this type of free license.
- Typically, it takes some time (nominally up to 12 hrs) to register your account on SSCL, although you have received the activation email. So, allow some time for this to happen before you attempt to check out a license.
- By selecting the proper type of license, you will receive an email where the license file with the extension .dat will be attached. Save this file to a desired location, typically, some folder within the top level directory `intelFPGA`. This file is used by the license daemon of the tools, located in the path C:\intelFPGA\21.1\questa_fse\win64.
- An environment variable should also be added to the system. For Windows, right click on Start, select System, Advanced System Settings, Environment Variables, and create a New variable called MGLS_LM_LICENSE_FILE and provide the path where you stored the license file you received from Intel (*.dat). Click OK. An example of this setup is shown in
- You can now start using the software. Also use the Intel® FPGA Software Installation and Licensing manual available on the elearning course webpage. Note that you are interested in the Intel FPGA **Starter** Edition.

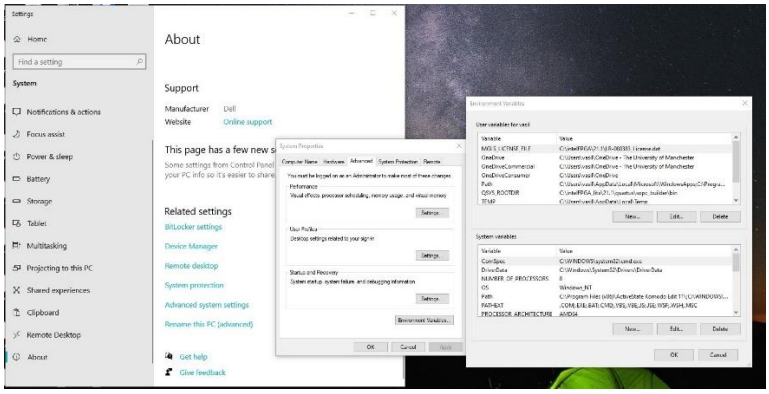

Fig. 2. Setting up the environment library for Questa – Intel FPGA simulator.

3 References

[1]. ModelSim [Online]. Available: https://eda.sw.siemens.com/en-US/ic/modelsim/ (accessed on 12/5/22).

[2]. Questa*-Intel® FPGA Edition [Online]. Available: https://www.intel.com/content/www/us/en/software-kit/684216/intel-quartus-prime-lite-edition-design-software-version-21-1-for-windows.html (accessed on 12/5/2022).

[3]. Libero [Online]. Available: https://www.microchip.com/en-us/products/fpgas-and-plds/fpga-and-soc-design-tools/fpga/libero-software-later-versions (accessed on 12/5/2022).

[4]. https://www.intel.com/content/www/us/en/docs/programmable/683472/22-1/minimum-hardware-requirements.html (accessed on 13/5/2022).

[5]. Intel® FPGA Self Service Licensing Center (SSLC) [Online]. Available: https://tinyurl.com/yc8f8es4 (accessed 13/5/2022).

4 Appendix

The following figures help you understand the simulation tool and should be read with subsection **Error! Reference source not found.**.

Fig. 3. Started a new project and ready to add files (right click in the project area for these menus to appear).

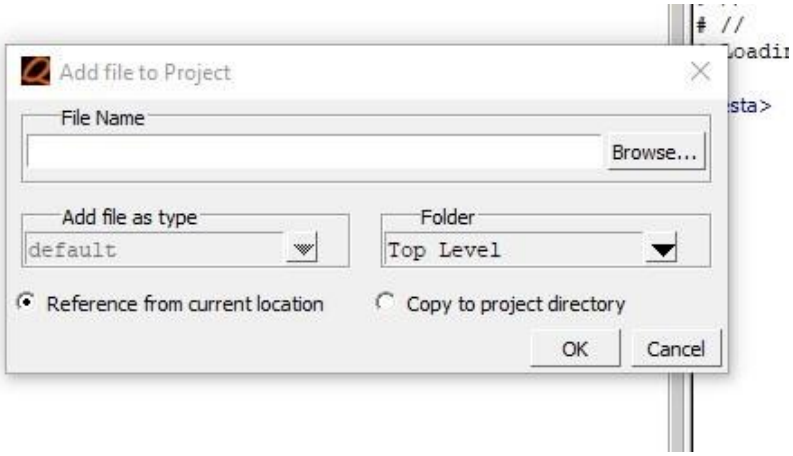

Fig. 4. Browse and pick the files you need (copy or not the files to the project directory).

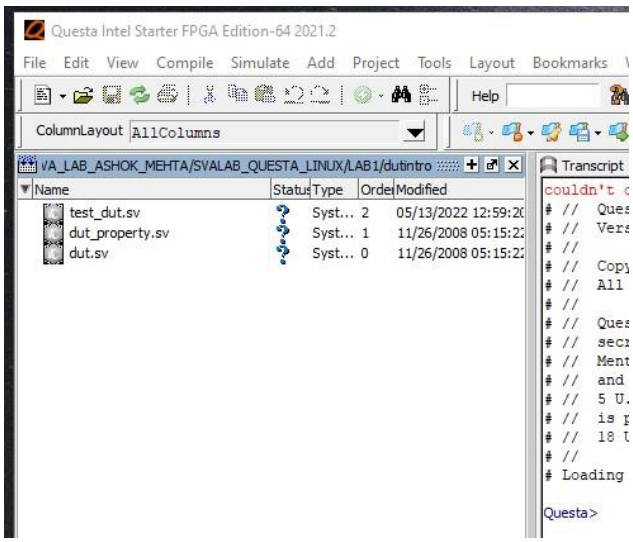

Fig. 5. Files were added to the project and are now ready to be compiled.

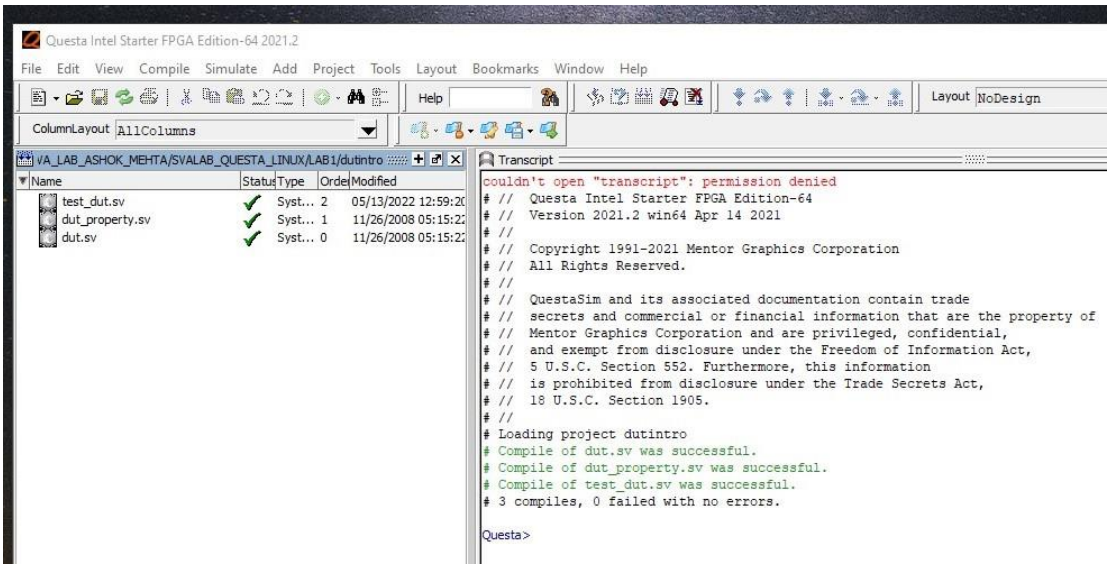

Fig. 6. All files have now been complied (question marks turns to ticks).

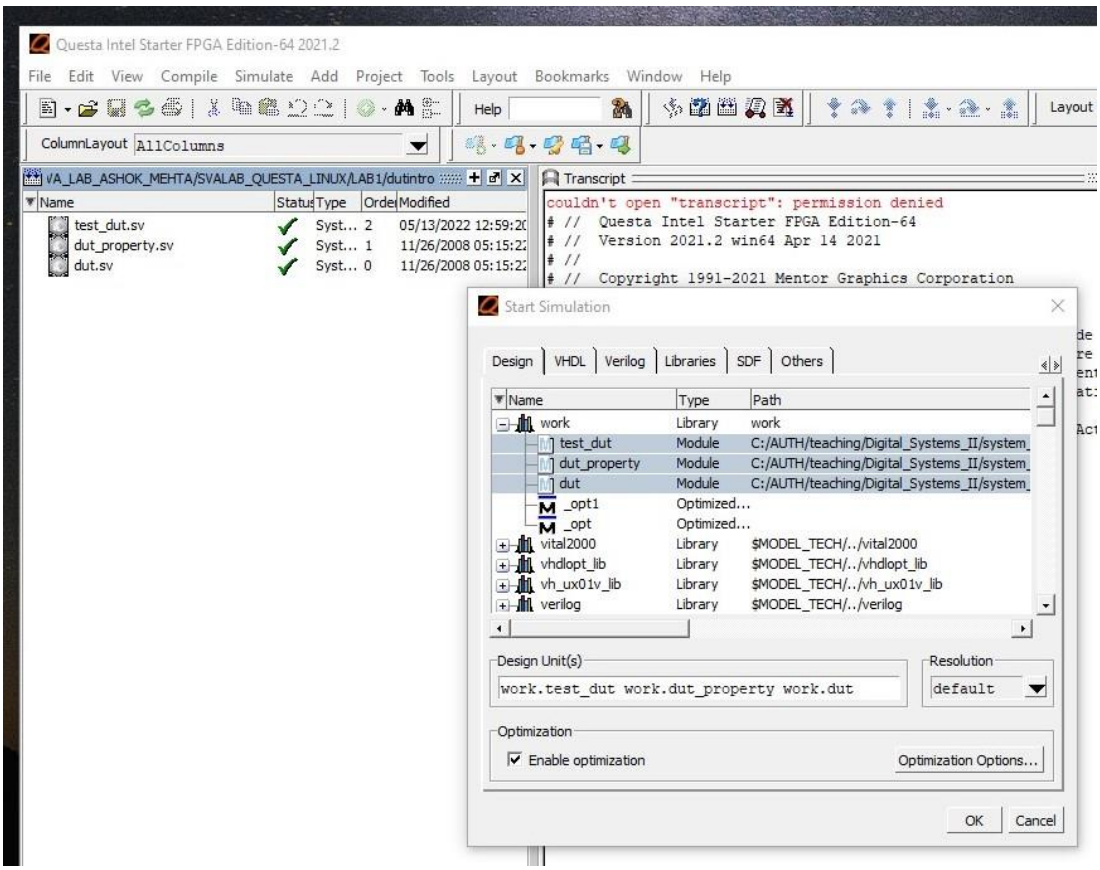

Fig. 7. Click on Simulate -> Start Simulation and select the compiled files to be simulated. Click on optimization options (see next Figure).

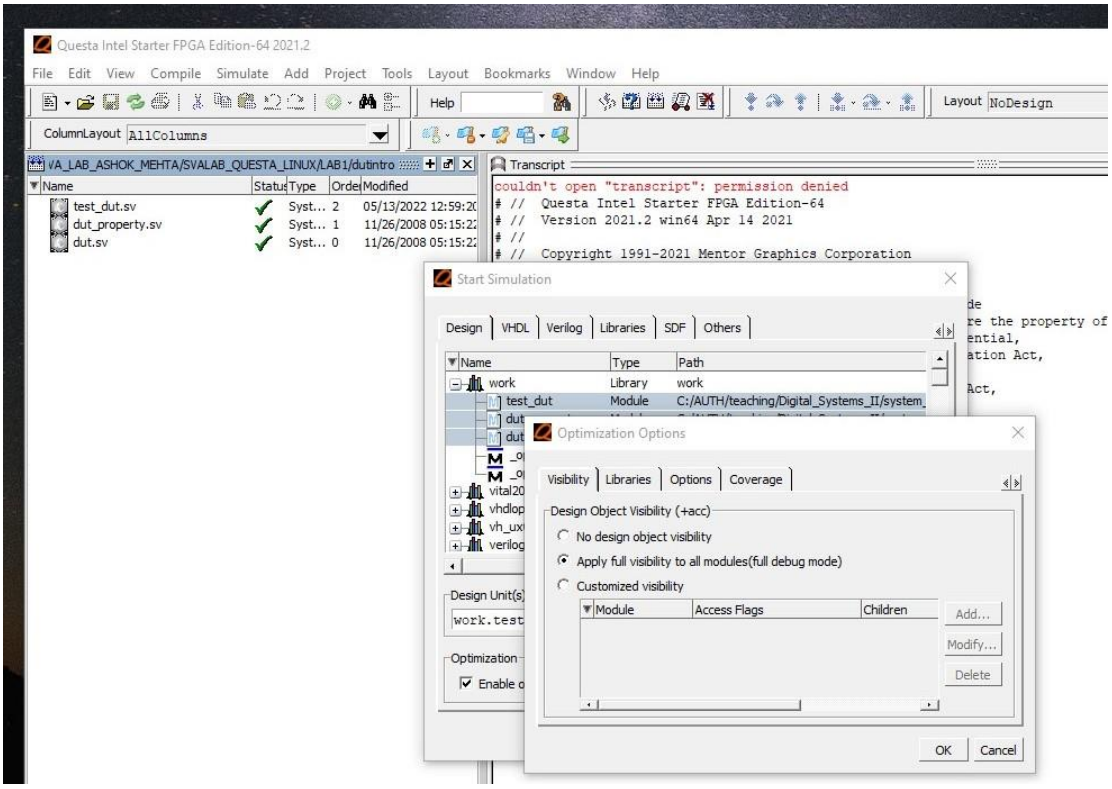

Fig. 8. Full visibility allows you to display all internals signals in the waveform window.

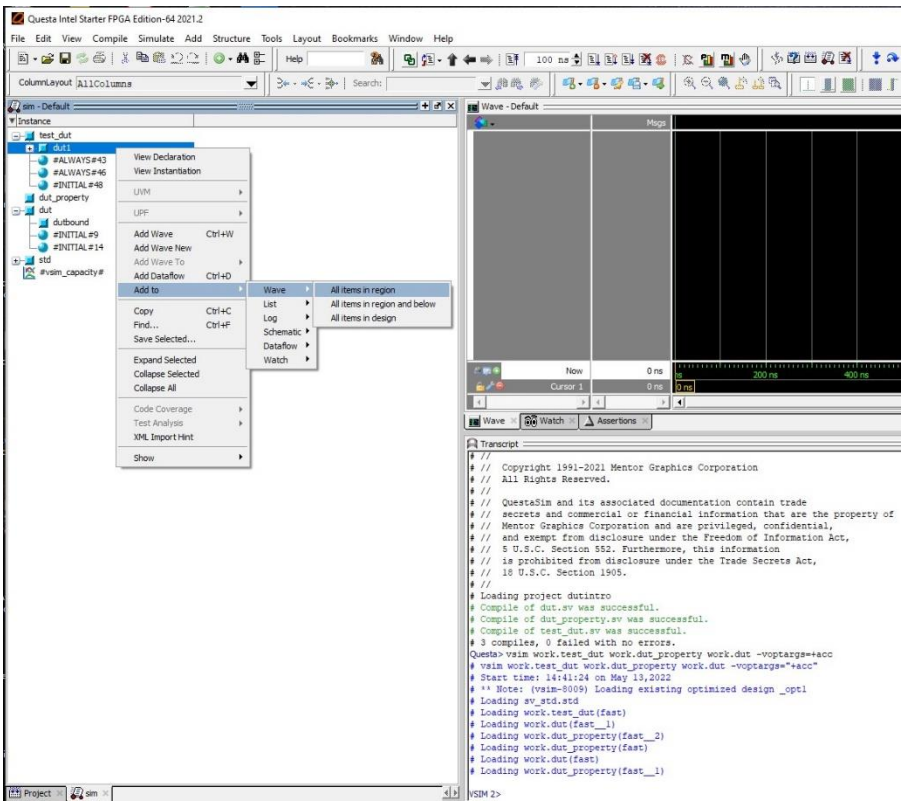

Fig. 9. Once the files are loaded for simulation, you can select which signals to be displayed (right click).

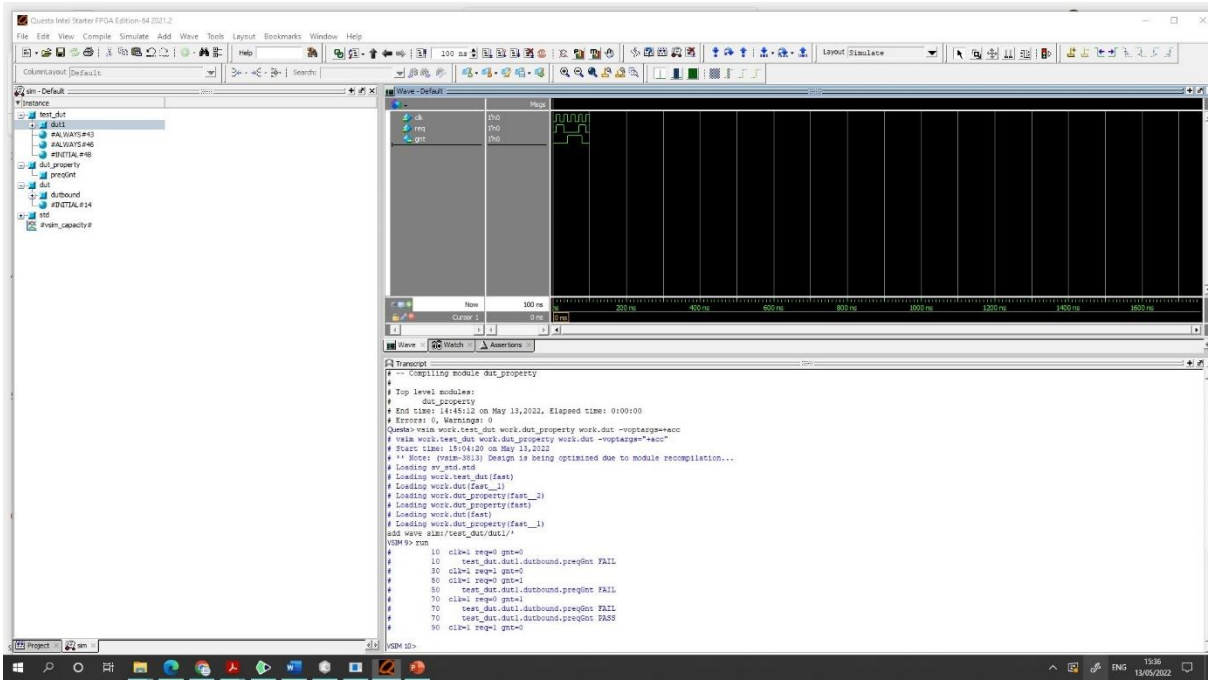

Fig. 10. Simulated DUT. See also the simulator transcript window at the bottom and the related reports.

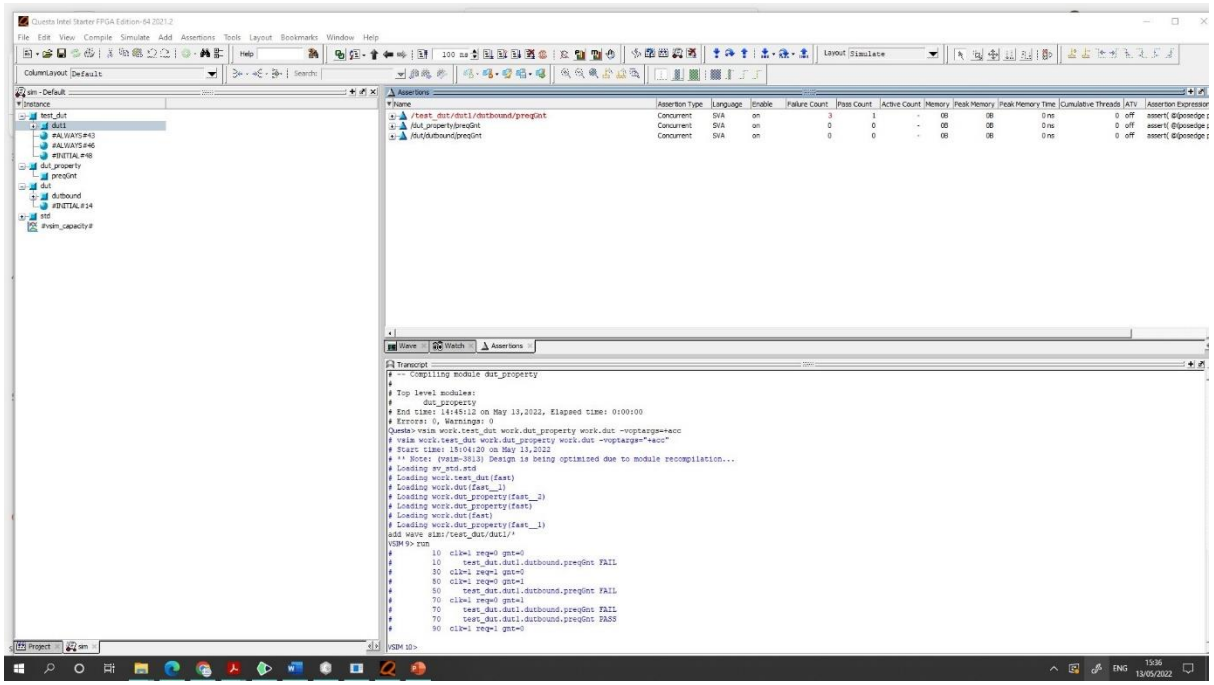

Fig. 11. Simulated DUT. The Assertions tab displays all related info about the properties checked in file dut_property.sv