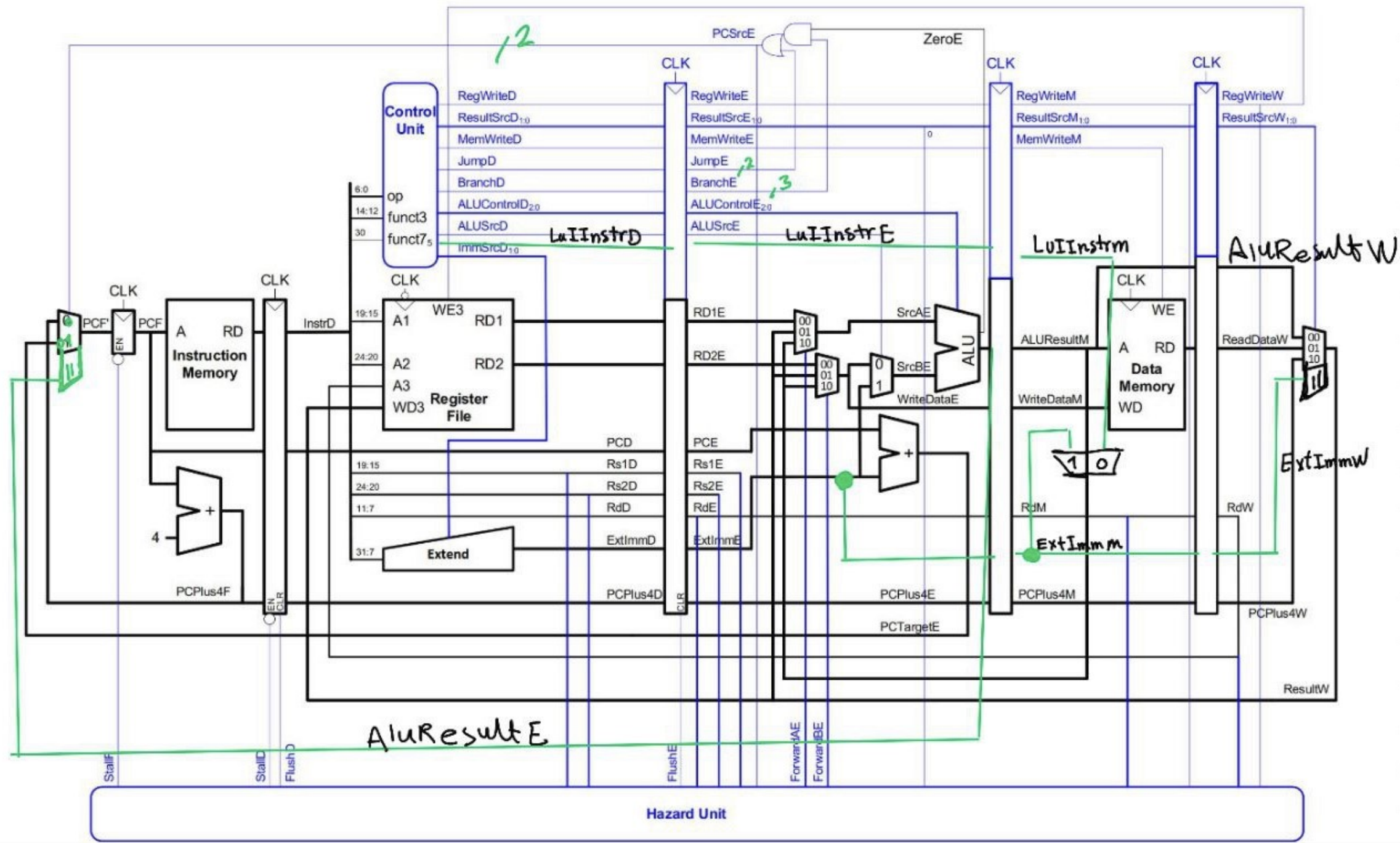


# Computer Architecture - Computer Assignment 4

## RISC-V Pipeline Implementation

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### Datapath Design



Controller Design (Combinational)

op	f3	f7	ResultSrcD	MemWriteD	ALUSrcD	ImmSrcD	RegWriteD	ALUOp	LUIInstr	JumpD	BranchD
Load Word	–	–	2'b01	1'b0	1'b0	I_TYPE_ImmSrc	1'b1	2'b00	1'b1	2'b00	3'b000
I-Type	–	–	2'b00	1'b0	1'b1	I_TYPE_ImmSrc	1'b1	2'b10	1'b0	2'b00	3'b000
S-Type	–	–	2'b00	1'b1	1'b1	S_TYPE_ImmSrc	1'b0	2'b00	1'b0	2'b00	3'b000
B-Type	BEQ	–	2'b00	1'b1	1'b0	B_TYPE_ImmSrc	1'b0	2'b01	1'b0	2'b00	branchEq
B-Type	BNE	–	2'b00	1'b1	1'b0	B_TYPE_ImmSrc	1'b0	2'b01	1'b0	2'b00	branchNEq
B-Type	BLT	–	2'b00	1'b1	1'b0	B_TYPE_ImmSrc	1'b0	2'b01	1'b0	2'b00	branchLEq
B-Type	BGE	–	2'b00	1'b1	1'b0	B_TYPE_ImmSrc	1'b0	2'b01	1'b0	2'b00	branchGEq
R-Type	–	–	2'b00	1'b0	1'b0	–	1'b1	2'b10	1'b0	2'b00	3'b000
U-Type	–	–	2'b11	1'b0	1'b0	U_TYPE_ImmSrc	1'b1	2'b00	1'b1	2'b00	3'b000
JALR	–	–	2'b10	1'b0	1'b1	I_TYPE_ImmSrc	1'b1	2'b00	1'b0	jumpRegister	notBranch
JAL	–	–	2'b10	1'b0	1'b1	J_TYPE_ImmSrc	1'b1	2'b00	1'b0	jump	notBranch

ALUControl

ALUOp	op	f3	f7	ALUControl
2'b00	–	–	–	ALU_ADD
2'b01	–	–	–	ALU_SUB
2'b10	I-Type	ADDI_F3	–	ALU_ADD
2'b10	–	ADD_F3	ADD_F7	ALU_ADD
2'b10	–	SUB_F3	SUB_F7	ALU_SUB
2'b10	–	XOR_F3	–	ALU_XOR
2'b10	–	AND_F3	–	ALU_AND
2'b10	–	OR_F3	–	ALU_OR
2'b10	–	SLT_F3	–	ALU_SLT
2'b10	–	SLTU_F3	–	ALU_SLTU

PCSrcE

BranchE	ZeroE	ResSignE	jumpE	PCSrcE
branchEq	1'b1	–	–	2'b01
branchNEq	1'b0	–	–	2'b01

BranchE	ZeroE	ResSignE	jumpE	PCSrcE
branchLEq	–	1'b1	–	2'b01
branchGEq	–	1'b0	–	2'b01
notBranch	–	–	jump	2'b01
notBranch	–	–	jumpRegister	2'b10
–	–	–	–	2'b00