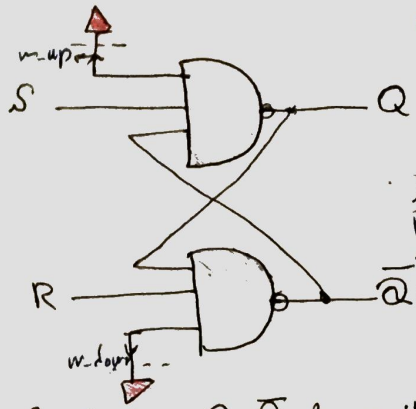
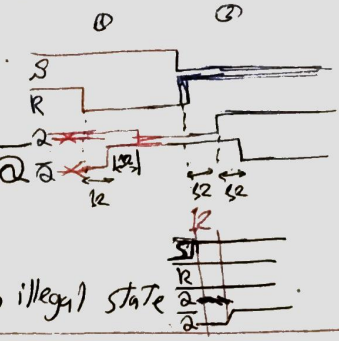
Kourosh Alinaghi

810101476

1)

a)

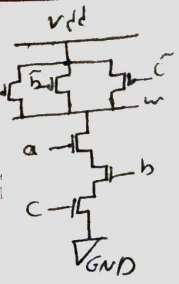




⇒ Worst case delay of the circuit = 24ns

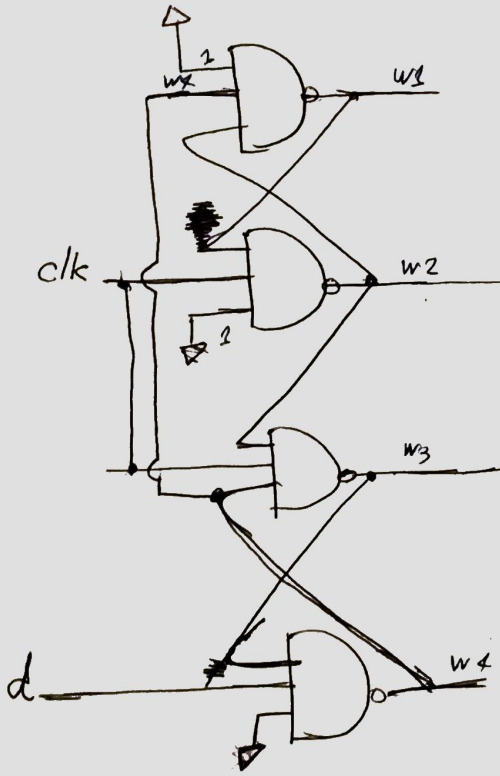
b)

worst case NAND delay = 3×4 = 22ns



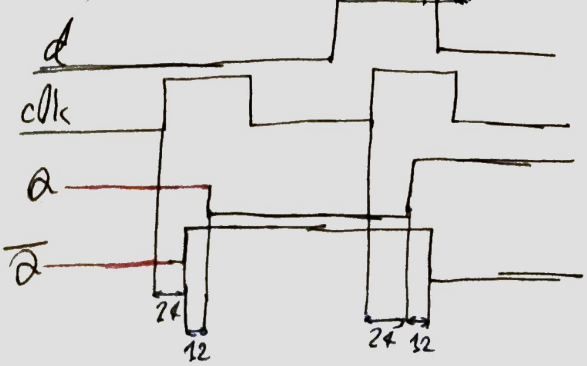
c) when $\{S, R\} = \{0, 0\} \Rightarrow Q = \bar{Q} = 1 \Rightarrow$ illegal state

2)



d & c) when we violate the Tsetup (like changing clk and d at the same time) our circuit becomes unstable and our outputs change forever. but if we put a little bit of Q delay in here (dt) the circuit would work just fine as expected. $\bar{Q}$ because our clk is positive edge.

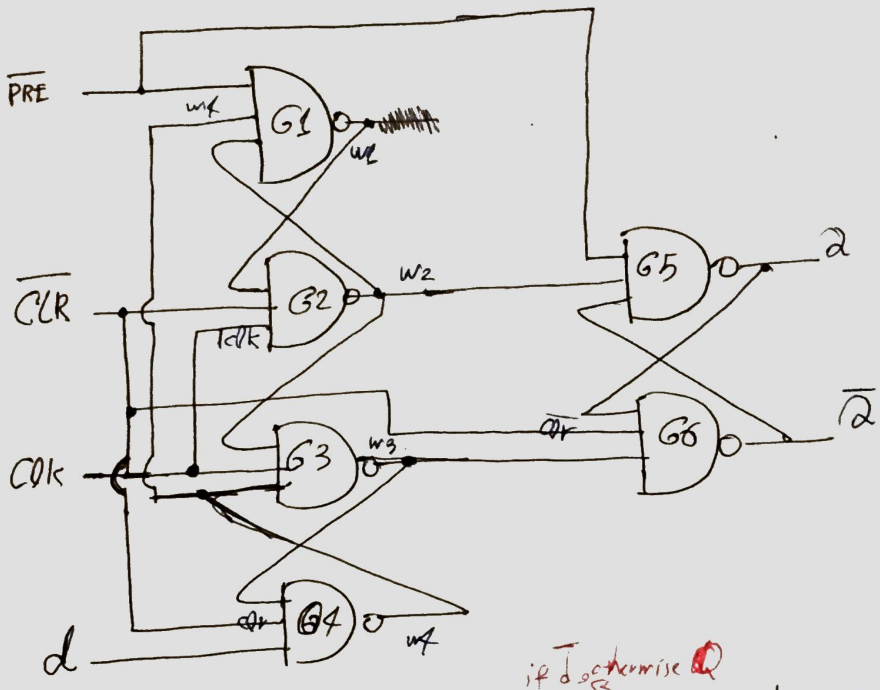
b)



changing d while clk is active wont effect the output

when d is 0/1, when clk becomes 1, $\bar{Q}/Q$ after 24 ns becomes 1/0 and 12ns after that, (12, 24, 36ns) $Q/\bar{Q}$ becomes 0/1.

3)



f) when clk is set to 1, after 24ns the $\overline{Q}$ output changes and 12ns after that the Q input is changed. but when pre or clr inputs change, only 12ns after that Q/$\overline{Q}$ output is changed (through G5 NAND) an 12ns after that, $\overline{Q}$/Q output changes.

g) when pre or clr are active, our G5/G6 conduct 0 to the Q/$\overline{Q}$ outputs, no matter what our clock&d values are.

h) when both pre and clr are active, Q and $\overline{Q}$ become 1 after 12ns (through G5 and G6)