



North-South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Name: CSE332L- Computer Organization and Architecture Lab

Experiment Number: 05

Experiment Name: Design of a Register File

Experiment Date: 21-04-2021

Report Submission Date: 28-03-2021

Section: 6

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Score

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Remarks:

Exp: Lab 05– Design of a Register File.

Objectives:

- Design a register file that is 16 bits wide. Label properly the inputs/outputs/selections
- Design the interfacing for reading data from any of those registers.
- Design the interfacing for writing data to any of those registers.

Logic Circuit Diagram:

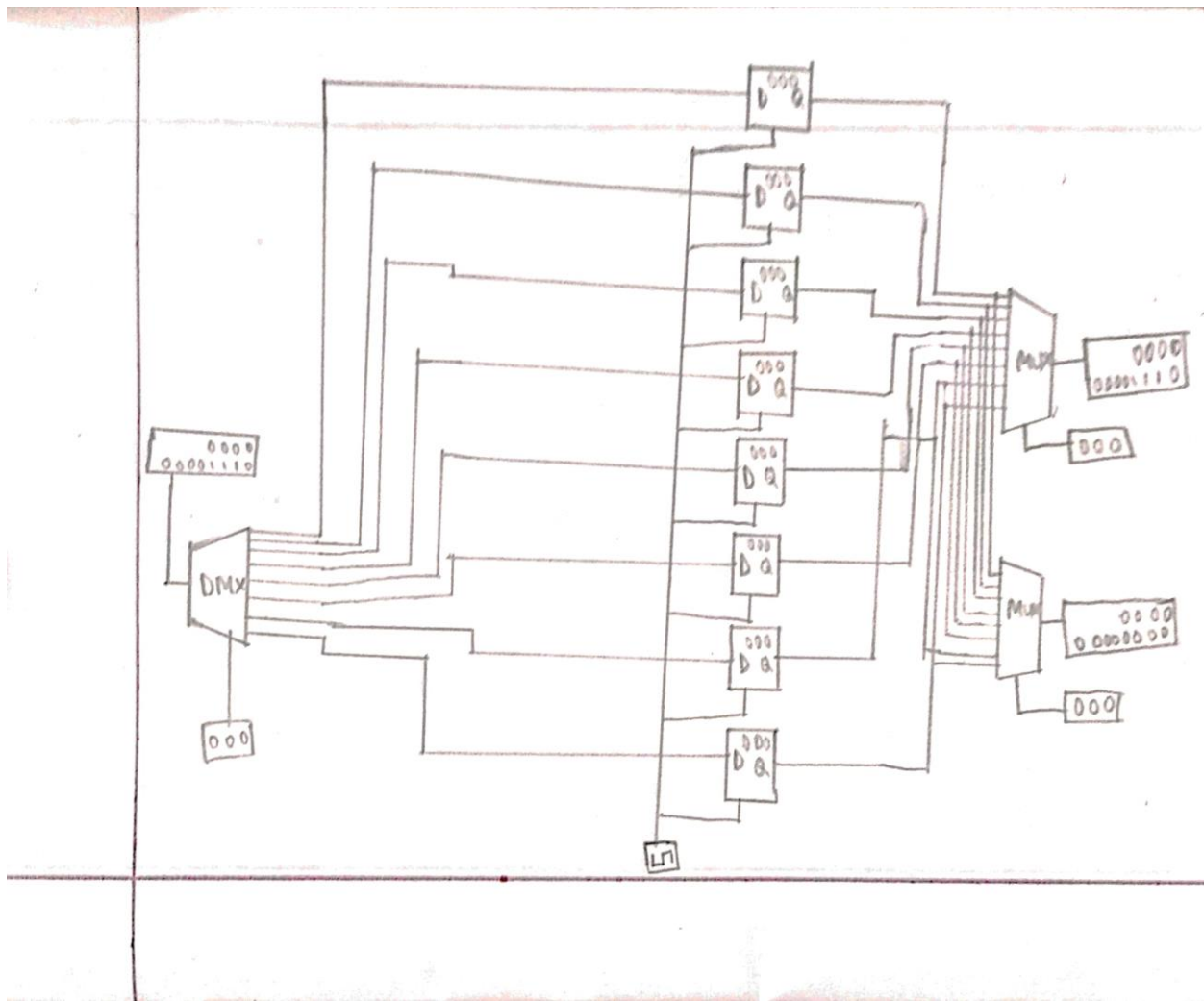
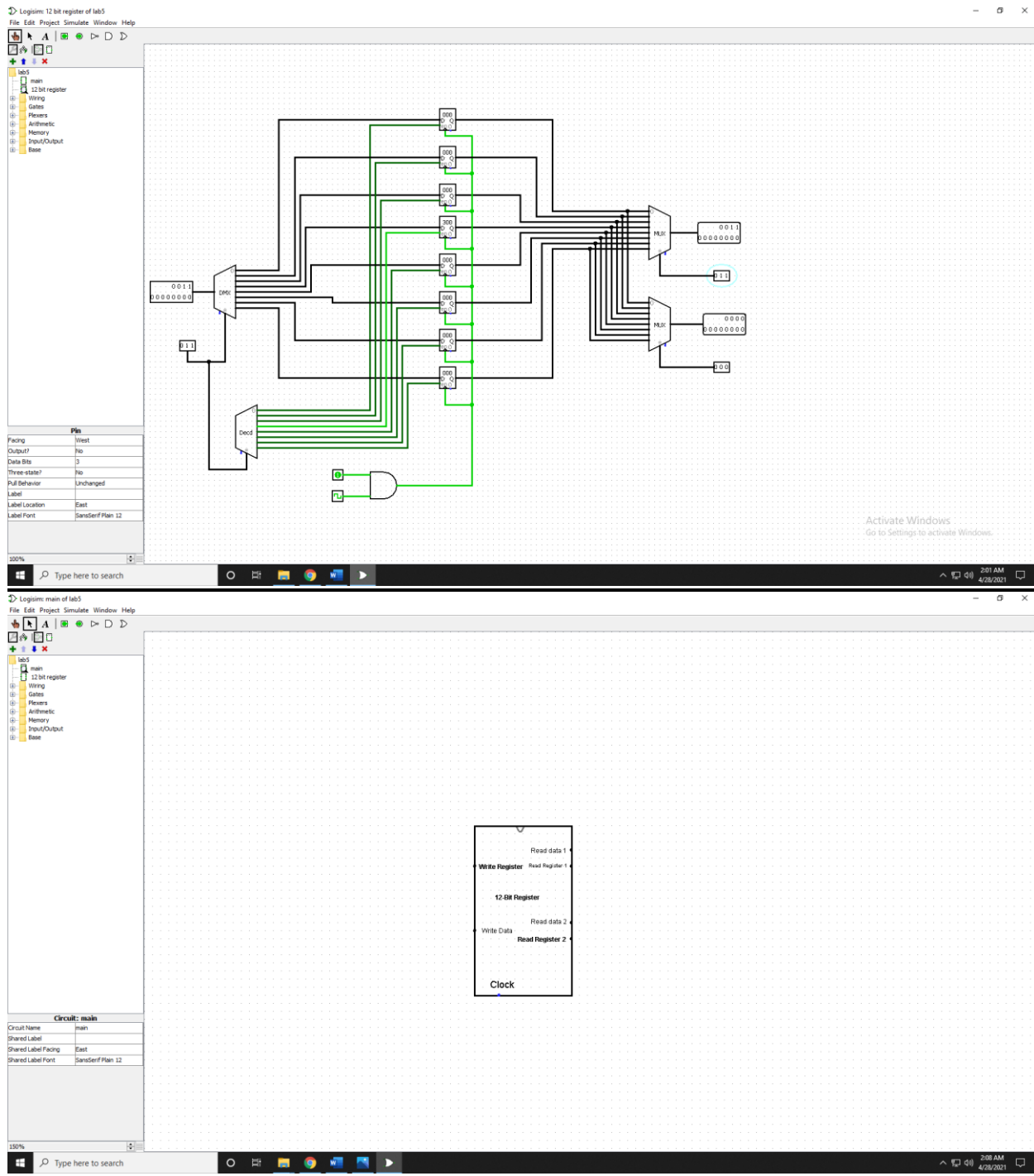


Fig-Circuit Diagram

Logic Circuit Diagram (Screenshot):



Discussion:

The essential is objective of this test to plan an 8-bit enroll record. In this exploration, I've developed an 8-bit enroll record on Logisim. The enroll is made of 8 Enroll, 1 Decoder, 2 Mux. All of these components are of 8 data bits.

Firstly, I need to compose a few respect on the enroll. For this case, I have chosen a 12-bit input which is actually "write information in," in this segment, I got to put parallel values for the comparing decimal value. Then, I have associated these 12-bit values with each of the registers. At that point, I have selected the enrollment by using "Compose address," which sets the enrollment in which the register will store the input respect. Usually a write operation. At that point, we can store up to 12 values within the 8 bits enroll at a time. The 3 bits compose address instructions are passed through the decoder at that point and after that, each of the signals is passed through each of the AND doors. Firstly, I have to type in a few respect on the enrollment. For this case, I have chosen a 12-bit input which is actually "write information in," in this segment, I got to put twofold values for the comparing decimal value. Then, I have associated these 12-bit values with each of the registers.

There's a common "Write enable" for each of the and doors as input. The yield of the AND doors is passed through each of the registers. There's a common connection for giving a clock within the enroll. By following this, able to store values within the register. In the moment portion, we'll perform the perused operation. We need to peruse the values from the enrollment, so for this case, we need to interface the yields of the enrollment with the MUX. We utilized two mux so that ready to appear two distinctive yields put away within the diverse enroll at a time. The output of the Mux will appear us the respect that we have put away within the register. So, we got to select the enroll by utilizing RS and RT to studied the as of now put away values within the enroll. Here, we got to put the register's comparing twofold respect to peruse the information from that enroll. Typically how we can examine put away information from each of the registers.