

North South University
Department of Electrical & Computer Engineering

LAB REPORT

Course Name: CSE332L

Experiment Number: **04**

Experiment Name: **Design of a 4-bit Binary Up-Down counter**

Experiment Date: 31/03/2021

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Faculty: SFM

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Section: 06

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Score

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Remarks:

Title: Design of a 4-bit Binary Up-Down counter

Objectives:

A register that goes through a predetermined sequence of states upon the application of input pulses, is called a counter. The input pulses may be clock pulses or may originate from an external source. They may occur at uniform intervals of time or at random. They are used for generating time signals to control the sequence of operations in digital computers.

A counter that follows the binary number sequence is called a binary counter. A 4-bit binary counter is a register of 4 flip-flops and associated gates that follows a sequence of states according to the binary count of 4 bits, from 0 to 15. We assume that the LSB is always complemented on every state. The sequence works on the fact that the next significant bit will be complemented only when a previous bit makes a transition from 1 to 0. For example, in case of transition from binary 0011 to 0100(4 to 5), 3rd bit does transition from 0 to 1. So, the 4th bit isn't complemented.

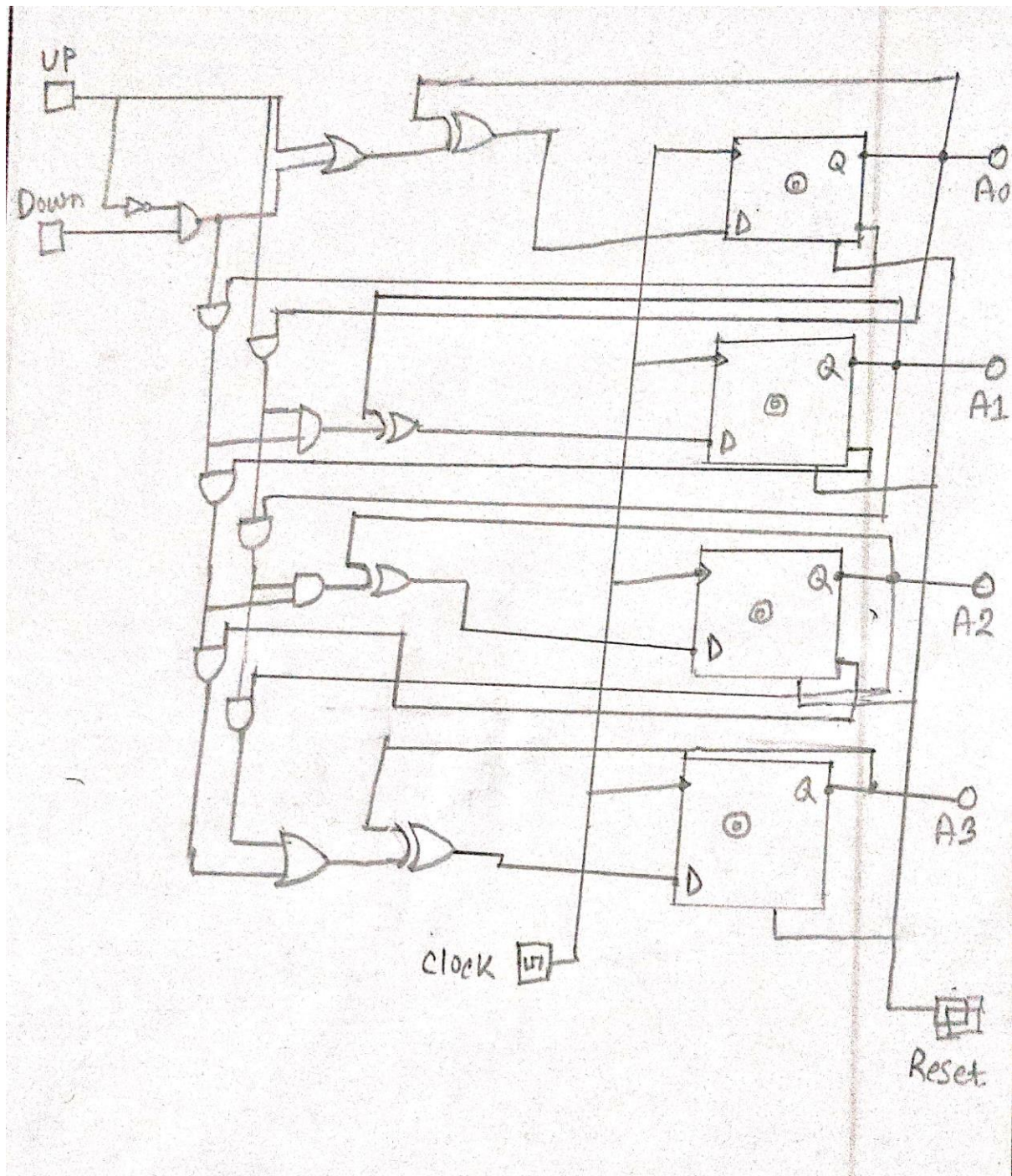
Apparatus:

1. 4 D-Flip Flop, 4 X-OR gates, 4 OR gate and 7 AND gate.
2. Wires for connection.
3. Clock Logic Diagram

Function Table:

Clock pulse	A	B	C	D
P0	0	0	0	0
P1	0	0	0	1
P2	0	0	1	
P3	0	0	1	1
P4	0	1	0	0
P5	0	1	0	1
P6	0	1	1	0
P7	0	1	1	1
P8	1	0	0	0
P9	1	0	0	1
P10	1	0	1	0
P11	1	0	1	1
P12	1	1	0	0
P13	1	1	0	1
P14	1	1	1	0
P15	1	1	1	1

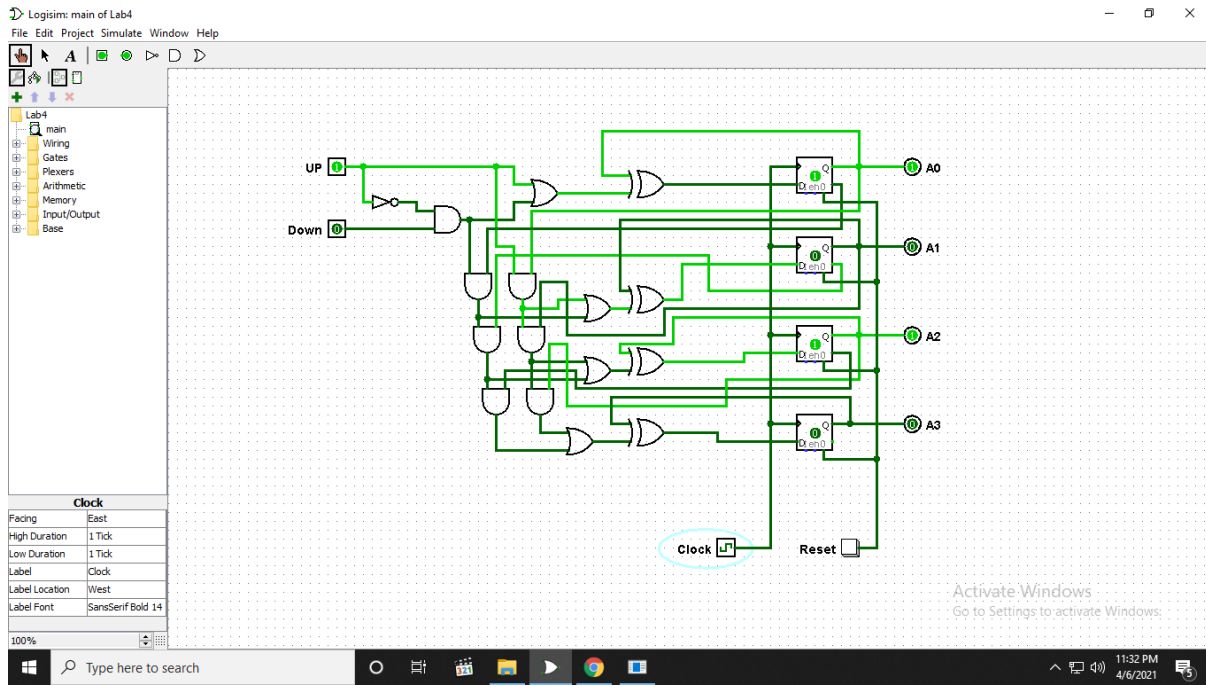
Logic Diagram:



Procedure:

1. There are 4 D-Flip Flop, 4 X-OR gates, 4 OR gates, 7 AND gates, 2 input and 4 outputs.
2. At first, the up-counter input and the down-counter input with a (NOT) gate and (AND) are connected with a OR gate.
3. The output of the OR gate is connected to the input of the X-OR gate and the output is connected with the D-Flip Flop.
4. Then the two AND gates are connected with the up and down counter and the one port the first AND gate is connected with D-Flip Flop and the other one with the X-OR gate.
5. And the input of the X-OR gate is connected with the output of D-Flip Flop will also give the Output A0.
6. There are clock and reset button with the 4 D-Flip Flops.
7. So, the other 3 D-Flop Flops are connected with the remaining gates by the same procedure will give us the outputs A1, A2 and A3.

Logisim works screenshot(s):



Discussion:

In lab 4, I construct a Design of a 4-bit Binary Up-Down counter. A 4-bit down counter is a digital counter circuit, which provides a binary countdown from binary 1111 to 0000. I increasing 4 I got wrong output because of wrong calculation. It took some time but finally I found out where the problem was fix the circuit and then solved it properly. By the help of our class lab instructor I fix that problem also.

