



**North South University**  
Department of Electrical & Computer Engineering

**LAB REPORT**

Course Name: CSE332L

Experiment Number: **06**

Experiment Name: **Design of an ALU.**

Experiment Date: 28/04/2021

Report Submission Date: 05/05/2021

Faculty: SFM

Submitted to: Md Saidur Rahman

Section: 06

Student Name: **Koushik Banerjee**

Score

Student ID: **1812171642**

Remarks:

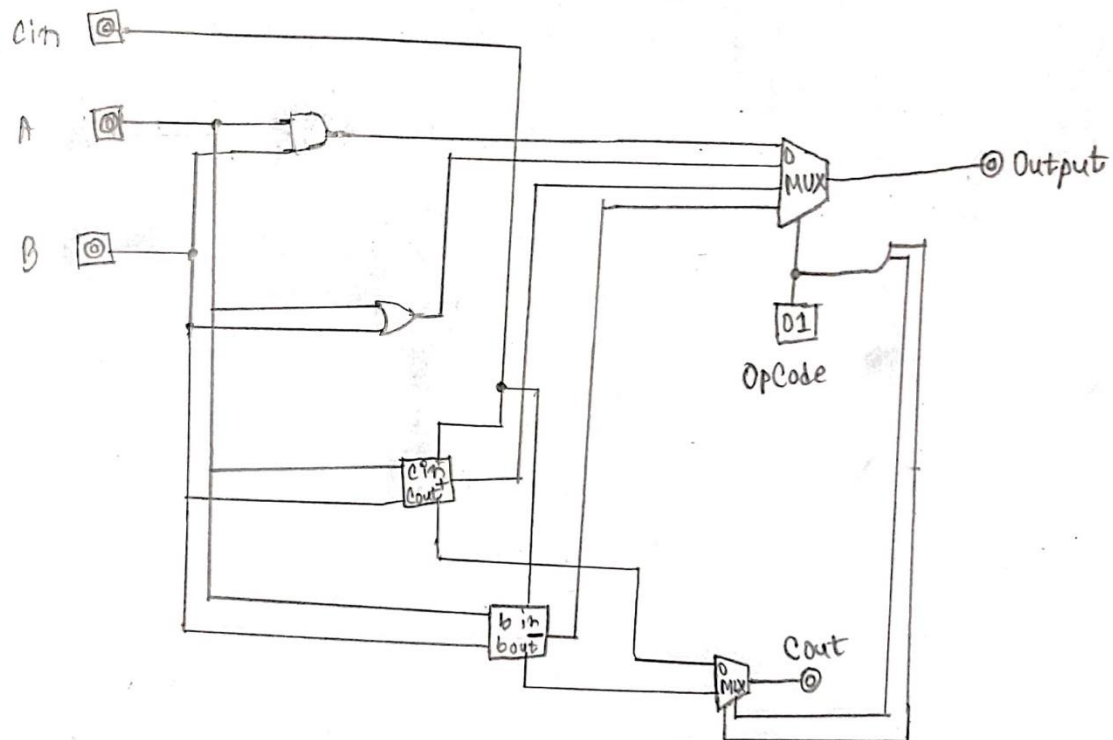
**Title:** Lab 06– Design of an ALU.

**Objective:**

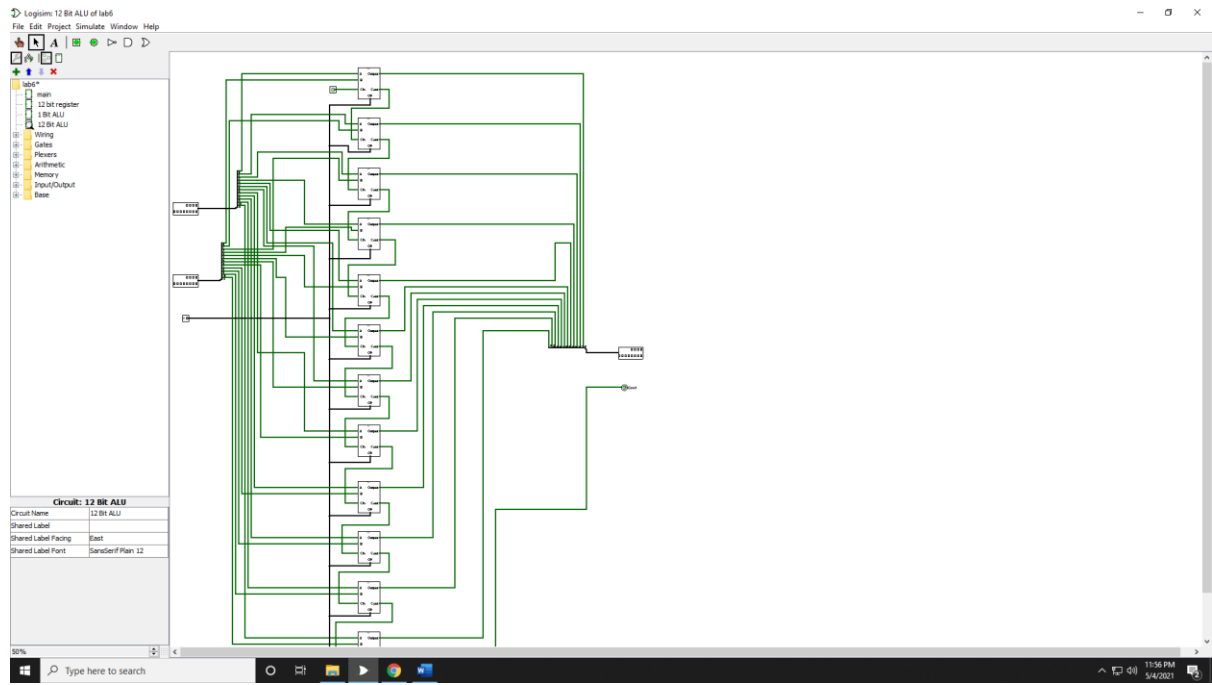
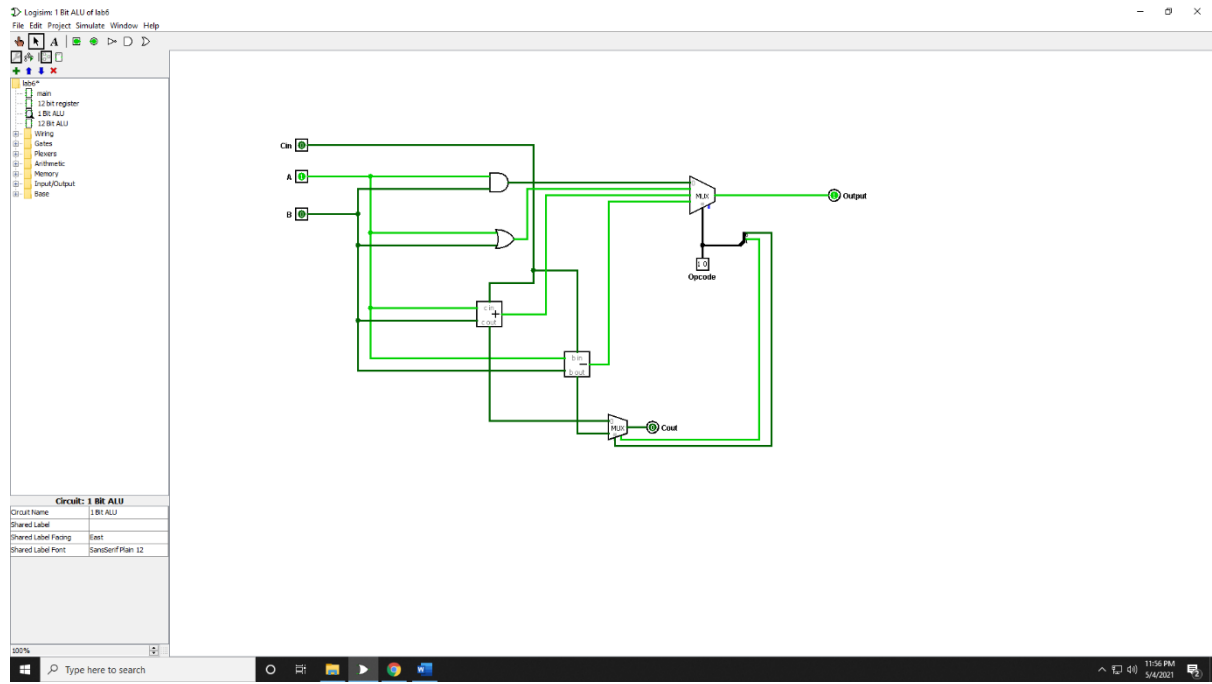
We will have the following objectives to fulfill:

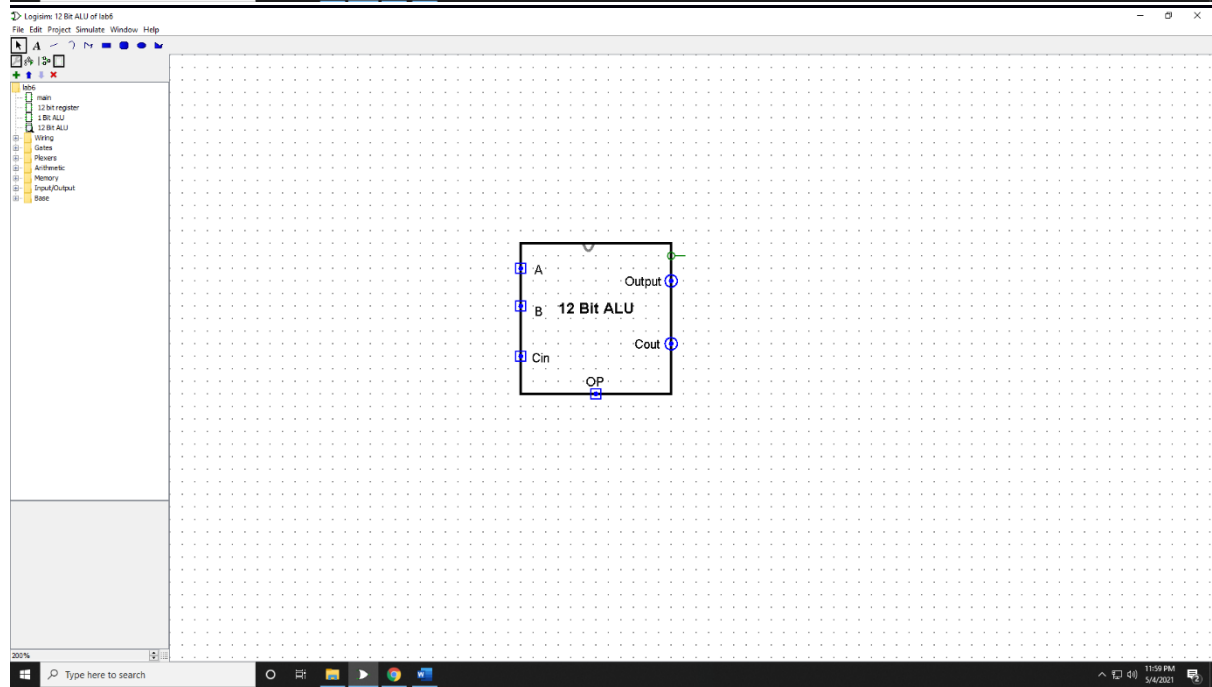
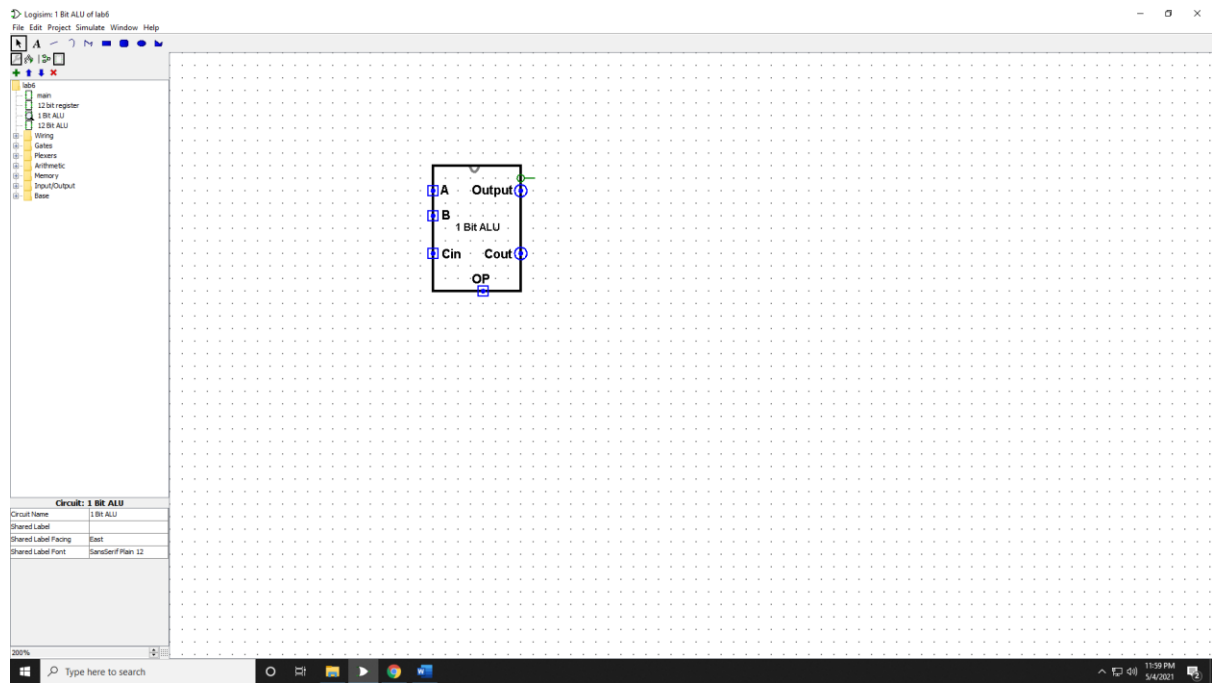
- 1) Build 1-bit ALU with a specific set of instructions
- 2) Incorporate equality check (zero signal), overflow detection, and other necessary flags
- 3) Build 12-bit ALU by connecting 12 one-bit ALU.

**Logic Circuit Diagram:**



**Logisim works screenshot(s):**





**Discussion:**

In lab 6, I learn how to design an ALU. The essential objective of this exploration is to plan a 1-bit ALU with particular information and plan a 12-bit ALU by interfacing 12 one-bit ALU. In this test, I've created a 12-bit ALU by utilizing the Logisim device. Firstly, I have planned a 1bit ALU utilizing 1 AND gate, 1 OR door, 1x1 bit adder, 1x1 bit subtractor. The yield of these four has passed through a 4x1 bit Mux. The yield of the MUX specifically goes to the result segment. Within the Mux, there's a 2-bit choice for ALU opcode that must be changed whereas performing the rationale operation. For Controlling that portion, we utilized one more mux 2x1. A and B are the two inputs that are given by the client. There's C-in that has to be associated with adder's and sub tractor's C-in. Within the moment portion, I have created a 12-bit ALU by utilizing 12 one-bit ALU. In this area, the inputs are A and B. Both of them comprise 12 bits. So also, each bit ALU takes inputs from A and B. the yield is associated with the result.