

# North South University Department of Electrical & Computer Engineering

# **LAB REPORT**

Course Name: **CSE231L** Experiment Number: 08

**Experiment Name: Synchronous Sequential Circuits** 

Experiment Date: 03/01/2021

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Section:

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Remarks:	

## **LAB-08: Synchronous Sequential Circuits**

#### **Objectives:**

- 1. Gain a practical understanding of State Diagrams and State Tables.
- 2. Understand the concept of designing Sequential Circuits using Flip-Flops.
- 3. Design and implement a Synchronous Sequential Circuit given a State Diagram.

#### **Apparatus:**

- 1.IC 7474 (Dual D Flip-Flops)
- 2.IC 74107 (Dual JK Flip-Flops)
- 3.Trainer board
- 4.1 x IC 74107 JK Flip-Flop
- 5. 1 x IC 7408 2-input AND gates
- 6. 1 x IC 7404 Hex inverters (NOT gates)

#### Theory:

**Synchronous Sequential Circuits:** Digital sequential logic circuits are divided into synchronous and asynchronous types. In synchronous sequential circuits, the state of the device changes only at discrete times in response to a clock signal. In asynchronous circuits the state of the device can change at any time in response to changing inputs. In automata theory and digital electronics, synchronous circuit is a digital circuit in which the changes in the state of memory elements are synchronized by a clock signal. In a sequential digital logic circuit, data is stored in memory devices called flip-flops or latches.

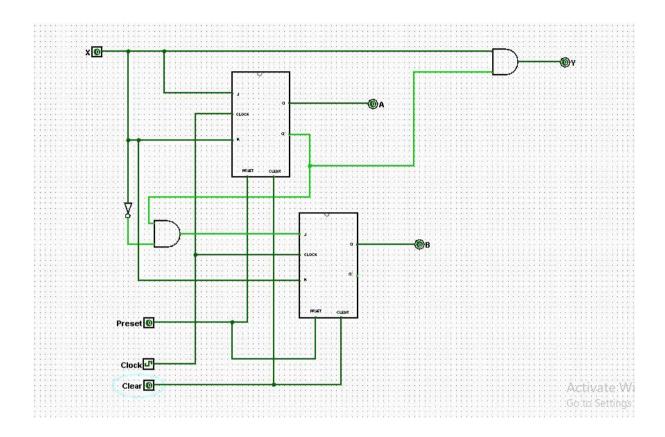
**State Table:** The relationship that exists among the inputs, outputs, present states and next states can be specified by either the state table or the state diagram. State Table. The state table representation of a sequential circuit consists of three sections labeled present state, next state and output. The present state designates the state of flip-flops before the occurrence of a clock pulse. The next state shows the states of flip-flops after the clock pulse, and the output section lists the value of the output variables during the present state. It is essentially a truth table in which the inputs include the current state along with other inputs, and the outputs include the next state along with other outputs. ... A state-transition table is one of many ways to specify a finite-state machine. Other ways include a state diagram.

#### **State Diagram:**

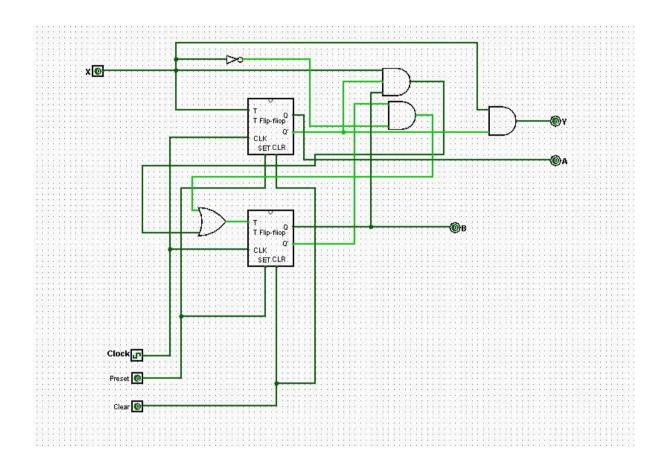
A state diagram shows the behavior of classes in response to external stimuli. Specifically, a state diagram describes the behavior of a single object in response to a series of events in a system. Sometimes it's also known as a Harel state chart or a state machine diagram. In addition to graphical symbols, tables or equations, flip-flops can also be represented graphically by a state diagram. In this diagram, a state is represented by a circle, and the transition between states is indicated by directed lines (or arcs) connecting the circles. A state diagram consists of states, transitions, events, and activities.

## **Circuit Diagram:**

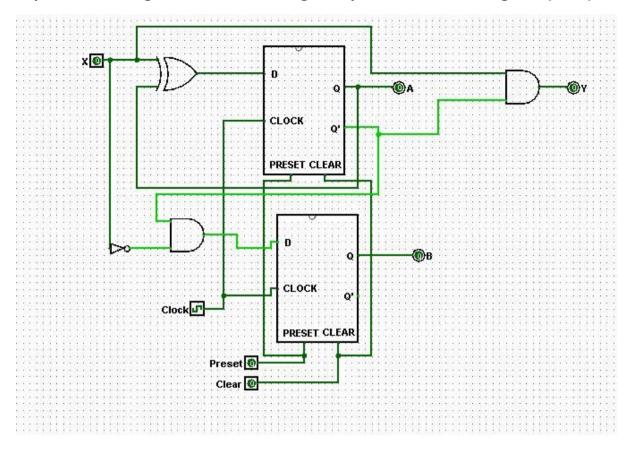
## Experiment-1: Figure F1: Constructing a Sequential Circuit using JK Flip-Flop.



## **Experiment-2: Figure F2: Constructing a Sequential Circuit using T Flip-Flop.**



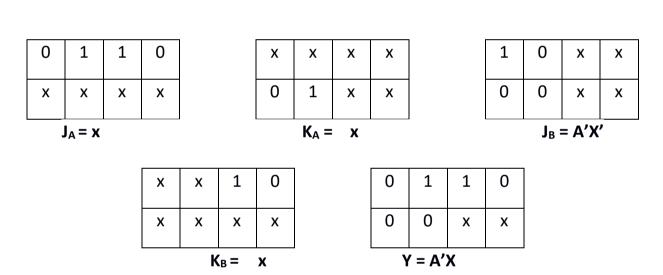
Experiment-3: Figure F3: Constructing a Sequential Circuit using D Flip-Flop.



## **Data Table:**

Experiment-1: Table 01: State table for circuit using JK Flip-Flop.

Presen	t state	Input	Nex	t state	Output	Fli	p-flop inp	ut functio	ns
A	В	X	A	В	Y	$J_A$	K <sub>A</sub>	$J_{B}$	K <sub>B</sub>
0	0	0	0	1	0	0	X	1	X
0	0	1	1	0	1	1	X	0	X
0	1	0	0	1	0	0	X	X	0
0	1	1	1	0	1	1	X	X	1
1	0	0	1	0	0	X	0	0	X
1	0	1	0	0	0	X	1	0	X
1	1	0	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X



Experiment-2: Table 02: State table for circuit using T Flip-Flop.

Preser	nt state	Input	Nex	t state	Output	Flip-flop in	put functions
Α	В	Х	Α	В	Υ	T <sub>A</sub>	Тв
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	0
0	1	1	1	0	1	1	1
1	0	0	1	0	0	0	0
1	0	1	0	0	0	1	0
1	1	0	Х	х	Х	х	Х
1	1	1	Х	х	Х	Х	х

0	1	1	0
0	1	Х	Х

 $T_A = x$ 

1	0	1	0
0	0	Х	Х

 $T_B = A'B'X' + BX$ 

0	1	1	0		
0	0	Х	Х		
\/					

Y = A'X

# Experiment-3: Table 03: State table for circuit using D Flip-Flop.

Presen	t state	Input	Nex	t state	Output	Flip-flop in	put functions
Α	В	Х	Α	В	Y	D <sub>A</sub>	$D_B$
0	0	0	0	1	0	0	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	1
0	1	1	1	0	1	1	0
1	0	0	1	0	0	1	0
1	0	1	0	0	0	0	0
1	1	0	Х	Х	х	Х	Х
1	1	1	Х	Х	х	Х	Х

0	1	1	0
1	0	Х	Х

 $D_A = A'X + AX'$ 

1	0	0	1
0	0	Х	Х

 $D_B = A'X'$ 

0	1	1	0
0	0	Х	Х

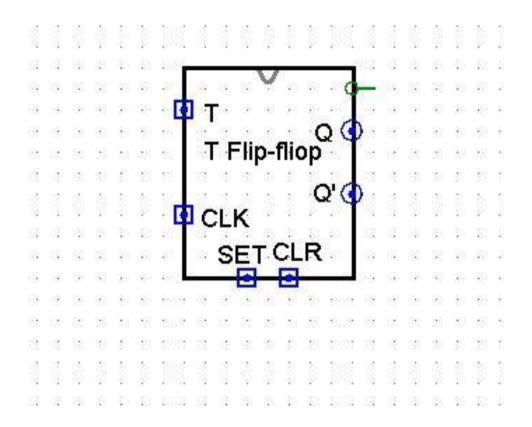
Y = A'X'

### **Experiment-2:**

Ques-01: Reason behind the output y equation of JK and T be the same

**ANS**: The T is the advanced form of JK flip flop. The K input of the JK flip flop is assigned to negation of J input in T flip flop. The T flip flop is made to remove the Race condition of the JK flip flop. In JK flip flop, when both JK input is 00 or 11 the race condition occurs. But in T flip flop as K is the inverse of J, the race condition never occurs.

Experiment-3: IC Diagram for the logic circuit in T Flip-Flop



#### **Discussion:**

In lab 8 and in the lab class I face couple of problem doing the IC circuit, I had done mistake on JK Flip-Flop. There were 1 extra input. I got confused to find out where the problem was. It took some time but finally I found out where the problem was and fix IC circuit and then solved it properly. During the implementation of D Flip-Flop, I also faced some problem there. By the help of our class lab instructor I fix that problem also. That was all human e error problem. After understanding all the problem and practicing that problem, I answered all the questions.