
# North South University

Department of Electrical & Computer Engineering

## LAB REPORT

Course Name: **CSE231L**

Experiment No: 03

Experiment Name: **Combinational Logic Design**

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Section: 03

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| Remarks: | |
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# LAB-03: Combinational Logic Design

## Objectives:

1. Become familiarized with the analysis of combinational logic networks.
2. To learn the implementation of networks using the two canonical forms.

## Apparatus:

1. Trainer Board
2. 1 x IC 4073 Triple 3-input AND gates
3. 2 x IC 4075 Triple 3-input OR gates 4. 1 x IC 7404 Hex Inverters (NOT gates)

## Theory:

**Combinational logic design:** Combinational Logic Circuits are only determined by the logical function of their current input state, logic "0" or logic "1", at any given instant in time.

The result is that combinational logic circuits have no feedback, and any changes to the signals being applied to their inputs will immediately have an effect at the output. In other words, in a Combinational Logic Circuit, the output is dependents at all times on the combination of its inputs. Thus a combinational circuit is memoryless.

So if one of its inputs condition changes state, from 0-1 or 1-0, so too will the resulting output as by default combinational logic circuits have "no memory", "timing" or "feedback loops" within their design.

**Canonical forms:**

In Boolean algebra, Boolean function can be expressed as Canonical Disjunctive Normal Form known as minterm and some are expressed as Canonical Conjunctive Normal Form known as maxterm.

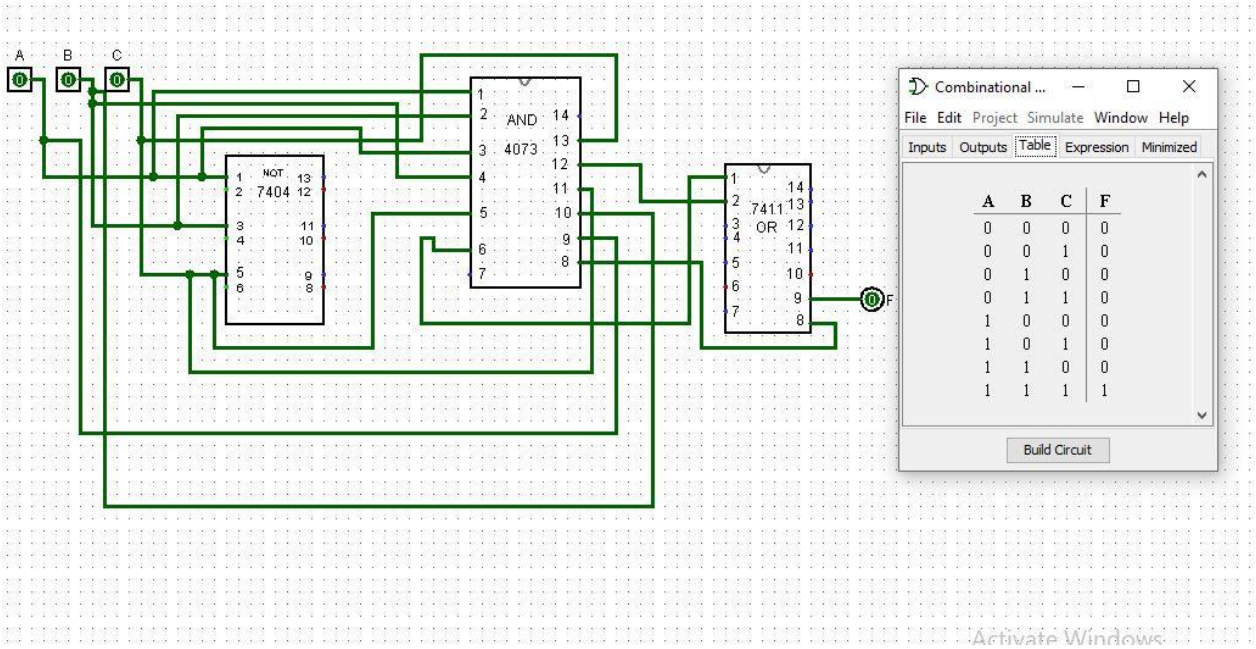
In Minterm, we look for the functions where the output results in "1" while in Maxterm we look for function where the output results in "0".

**Min terms and Max terms:**

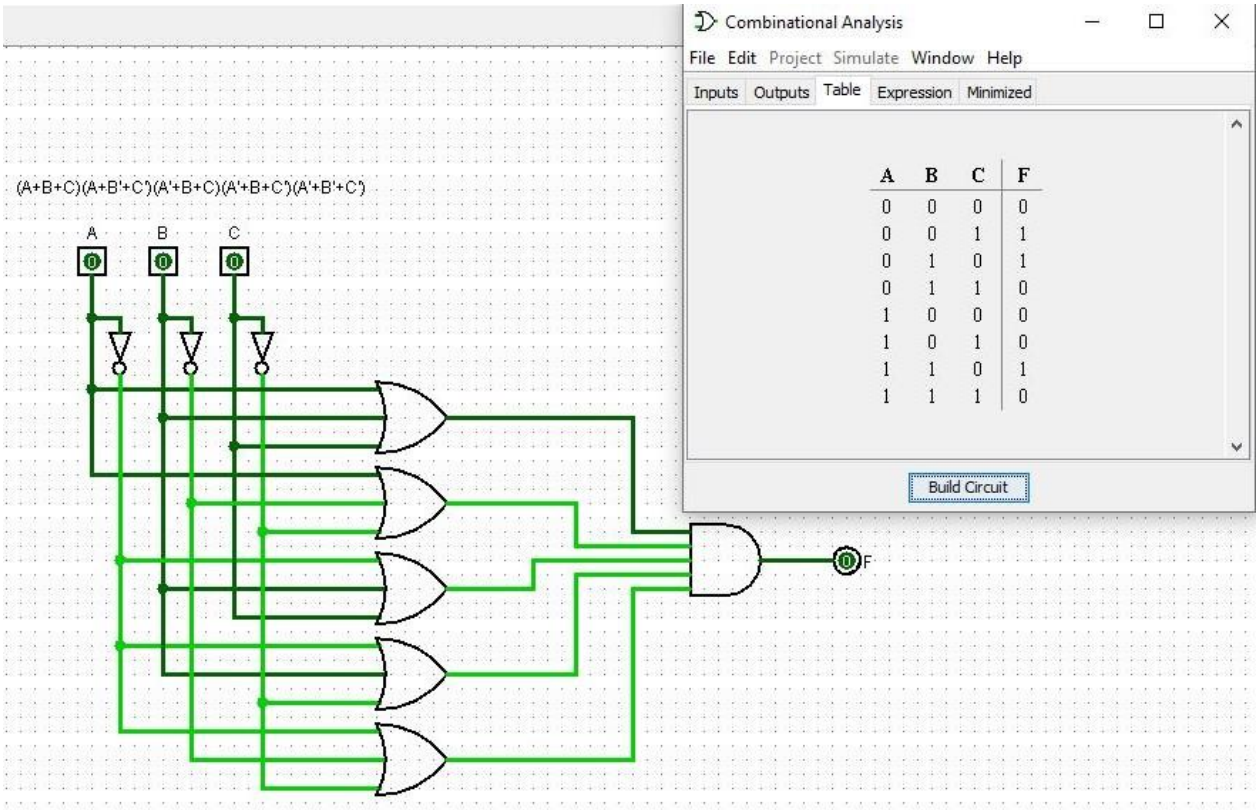
A minterm is a Boolean AND function containing exactly one instance of each input variable or its inverse. A maxterm is a Boolean OR function with exactly one instance of each variable or its inverse. For a combinational logic circuit with n input variables, there are
$2^n$ possible minterms and $2^n$ possible maxterms.

## Circuit Diagram:

**IC diagram for the 1st canonical form of the circuit:**



**Simulation of the circuit for the 2nd canonical form:**




| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

## Data Table:

**Table 1: Truth table to a combinational circuit**

| Input Reference | A B C | F | Min term | Max term |
|---|---|---|---|---|
| 0 | 0 0 0 | 0 | | A+B+C |
| 1 | 0 0 1 | 1 | A'B'C | |
| 2 | 0 1 0 | 1 | A'BC | |
| 3 | 0 1 1 | 0 | | A+B'+C' |
| 4 | 1 0 0 | 0 | | A'+B+C |
| 5 | 1 0 1 | 0 | | A'+B+C' |
| 6 | 1 1 0 | 1 | ABC' | |
| 7 | 1 1 1 | 0 | | A'+B'+C' |

**Table 2: 1st and 2nd canonical forms of the combinational circuit of table 1.**

| | Shorthand Notation | Function |
|---|---|---|
| 1st Canonical form | $F=\sum(1, 2, 6)$ | A'B'C+A'BC+ABC' |
| 2nd Canonical form | $F=\prod( 0, 3, 4, 5, 7)$ | (A+B+C)(A+B'+C')(A'+B+C)(A'+B+C')(A'+B'+C') |

**Discussion:**

In lab 3 and in the lab class I face couple of problem doing the IC circuit , I had done mistake in min terms but I solve that out by following the equation. But in max terms I face problem to solve in that equation I got confused to find out where the problem was. It took some time but finally I found out where the problem was and fix IC circuit and then solved it properly. By the help of our class lab instructor I fix that problem also. That was all human e error problem. After understanding all the problem and practicing that problem, I answered all the questions.