LAB-03: Combinational Logic Design

Objectives:

Apparatus:

Theory:

Combinational logic design:

Canonical forms:

Min terms and Max terms:

Circuit Diagram:

IC diagram for the 1st canonical form of the circuit.

Simulation of the circuit for the 2nd canonical form.

Data Table:

Table 1: Truth table to a combinational circuit

Input Reference	A B C	F	Min term	Max term
0	0 0 0			
1	0 0 1			
2	0 1 0			
3	0 1 1			
4	1 0 0			
5	1 0 1			
6	1 1 0			
7	1 1 1			

Table 2: 1st and 2nd canonical forms of the combinational circuit of table 1.

	Shorthand Notation	Function
1st Canonical form	F=∑(1, 2, 6)	
2nd Canonical form	F=∏(0, 3, 4, 5, 7)	

Discussion: