North South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Name: CSE231

Experiment Number: Introduction to Flip-Flops and Shift Registers

Experiment Name: **LAB-07-A: Introduction to Flip-Flops and Shift Registers**

LAB-7B: BCD to Seven Segment Decoder

Experiment Date: 27/12/20

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Section: 03L

Group Number: 01

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Remarks:	

LAB-07-A: Introduction to Flip-Flops and Shift Registers

Objectives:

Learn about the concept of states in digital logic and how Flip-Flop circuits can be used to store state
information.
Understand the internal logic of J-K Flip-Flops and implement one using basic logic gates.
Understand the relationship between J-K, T and D Flip-Flops and observe the characteristics of all three.
Implement a shift register using D Flip-Flops and analyze its operation.

Apparatus:

The 7474 is a 14 pin IC which requires a Ground connection at pin 7 and VCC at pin 14. Pins 2 and 12 serve as
the inputs for the two Flip-Flops and pins 5 and 9 act as the corresponding outputs. Pins 6 and 8 provide the
inverse of the outputs. Pin 3 is the clock input for the first Flip-Flop and pin 11 is the clock input for the second
Flip-Flop.

Theory:

Flip-Flop: In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information – a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.
A flip-flop is a device which stores a single bit (binary digit) of data; one of its two states represents a "one" and the other represents a "zero". Such data storage can be used for storage of state, and such a circuit is described as sequential logic in electronics.

D Flip-Flop: The D flip-flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. A D flip-flop can be made from a set/reset flip-flop by tying the set to the reset through an inverter.

T Flip-Flop: T flip – flop is an edge triggered device i.e. the low to high or high to low transitions on a clock signal of narrow triggers that is provided as input will cause the change in output state of flip – flop.

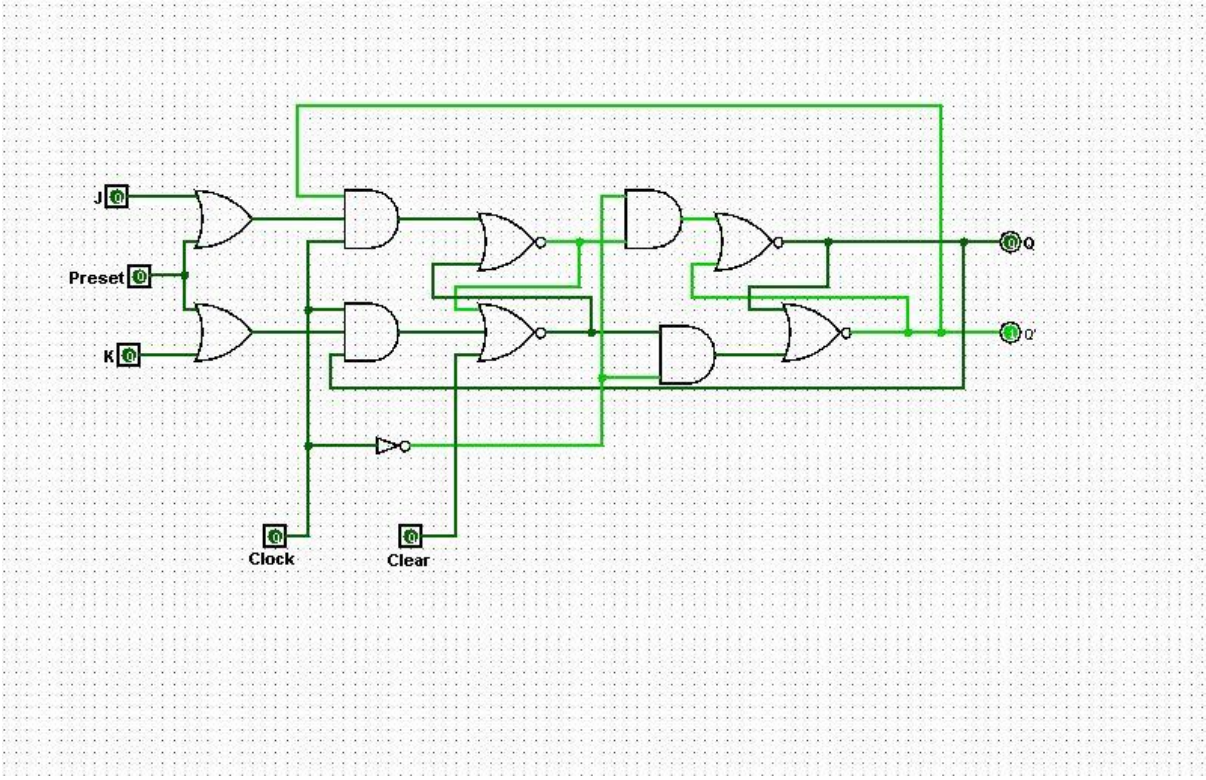
JK Flip-Flop: The JK flip flop is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”.

Registers:

Registers are a type of computer memory used to quickly accept, store, and transfer data and instructions that are being used immediately by the CPU. The registers used by the CPU are often termed as Processor registers.

Circuit Diagram:

Figure F1: Constructing a Master slave JK Flip-Flop using AND and NOR gates.



Data Table:

Experiment-1:

Table 01: J-K Flip-Flop using AND and NOR gates.

J	K	Q	Q'
1	0	1	0
0	0	0	1
0	1	0	1
0	0	0	1
1	1	1	0
1	0	1	0
1	0	1	0
1	1	0	1

Experiment-2:

Table 02: T and D Flip-Flops using J-K Flip-Flops.

T	Q
0	0
1	1

D	Q
0	0
1	1

Table F.2.1 **Table F.2.2**

Table 03: Right shift register using D Flip-Flops .

States	Input	Output
Initial State	X	XXXX
T1	1	1XXX
T2	0	01XX
T3	1	101X
T4	0	0101

Question and Answer:

Experiment-2:

Difference between T and D Flip-Flops.

ANS: The T-Flip flop will change its output from on to off, or vice versa, each time it receives an input. The D-Flip flop will change its output to whatever the signal at the other input is, each time it recieves an input.

Experiment-3:

Q-01: Why we need shift registers

ANS:

Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format.

Q-02: If the output of last D Flip-Flop is connected to the input of first one.

ANS:

The major drawback of the SR flip-flop (i.e. its indeterminate output and ... 5.3.1 is called a level triggered D Type flip-flop because whether the D input is active or ... the last input state that occurred during the clock pulse, (period RT in Fig. ... flip-flops may be connected in cascade, with the Q output of the first flip-flop in the.

Discussion:

In lab 7 and in the lab class I face couple of problem doing the IC circuit, I had done mistake on JK Flip-Flop. There were 1 extra input. I got confused to find out where the problem was. It took some time but finally I found out where the problem was and fix IC circuit and then solved it properly. During the implementation of D Flip-Flop, I also faced some problem there. By the help of our class lab instructor I fix that problem also. That was all human e error problem . After understanding all the problem and practicing that problem, I answered all the questions.

LAB-7B: BCD to Seven Segment Decoder (0-15)

Objectives:

Learn about the concept of states in digital logic and how Flip-Flop circuits can be used to store state
information.
Understand the internal logic of J-K Flip-Flops and implement one using basic logic gates.
Understand the relationship between J-K, T and D Flip-Flops and observe the characteristics of all three.
Implement a shift register using D Flip-Flops and analyze its operation.

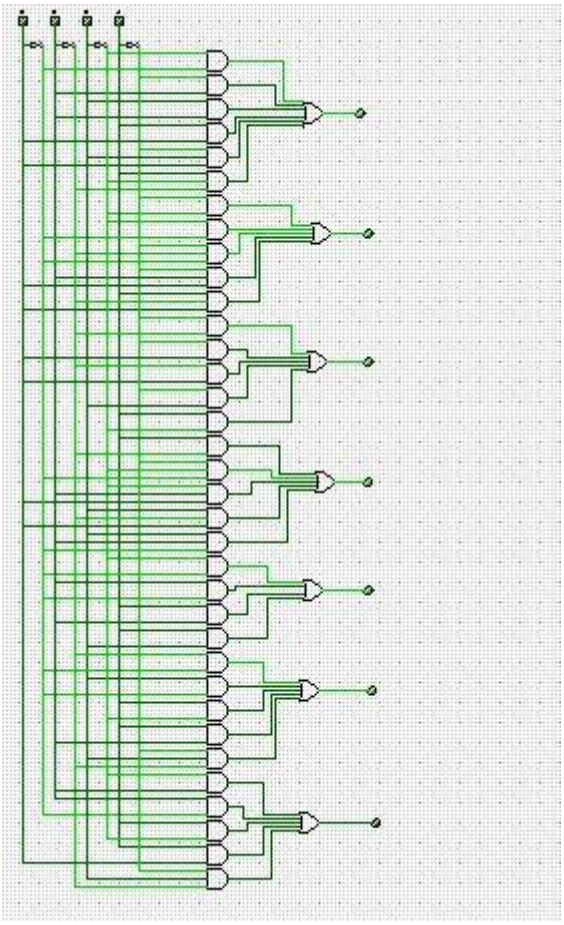
Equipments:

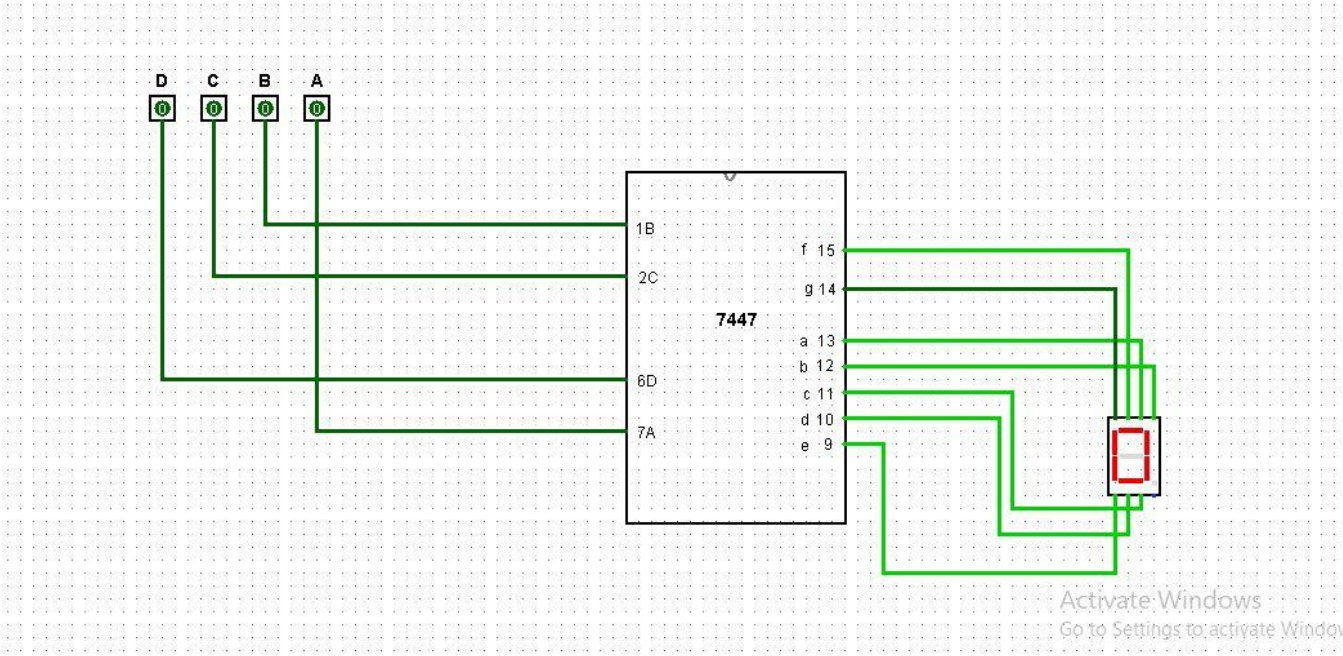
- Trainer board
- IC 7447, resistors, seven segment display
- Wires for connection

Theory:

A BCD to Seven Segment decoder is a combinational logic circuit that accepts a decimal digit in BCD (input) and generates appropriate outputs for the segments to display the input decimal digit. The truth table is extracted from the CD4511 IC datasheet. This truth table is interactive. For combination where all the inputs (A, B, C and D) are zero (see **Truth Table**), our output lines are a = 1, b = 1, c = 1, d = 1, e = 1, f = 1 and g = 0. So 7 segment display shows 'zero' as output.

Circuit Diagram:





Data Table:

Decimal	Inputs				output						
	D	C	B	A	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	1	1	1	0	1	1	1
11	1	0	1	1	0	0	1	1	1	1	1
12	1	1	0	0	1	0	0	1	1	1	0
13	1	1	0	1	0	1	1	1	1	0	1
14	1	1	1	0	1	0	0	1	1	1	1
15	1	1	1	1	1	0	0	0	1	1	1

Task: Draw logic circuit diagram for the above truth table using 4 variable K-map Result will show as Decimal numbers 0-9 and then A-F for (10-15) total 16 digits in 0-F serial order.

Show your work on the K-Map and Functions Here Below.

1	0	1	1
0	1	1	1
1	0	1	1
1	1	0	1

1	1	1	1
1	0	1	0
0	1	0	0
1	1	0	1

1	1	1	0
1	1	1	1
0	1	0	0
1	1	1	1

1	0	1	1
0	1	0	1
1	1	0	1
1	1	1	0

1	0	0	1
0	0	0	1
1	1	1	1
1	1	1	1

0	0	1	1
1	1	0	1
1	0	1	1
1	1	1	1

0	0	1	1
1	1	0	1
0	1	1	1
1	1	1	1

Write down the Boolean Functions for each K map

A = AB'C'+A'BD+B'D'+A'C+A'D'+BC

B=A'C'D'+A'CD+AC'D+A'B'+B'D'

C=A'C+A'D+C'D+A'B+AB'

D=A'B'D'+BC'D+BCD'+AC

E=B’D’+CD’+A

F=A’BC’+B’C+BD’+AB’+AC

G=A’BC’+B’C+CD’+AB’+AD

Discussion:

In BCD to Seven Segment Decoder I face couple of problem doing the IC circuit, I had done mistake on logic diagram. Then I figure out how to build logic diagram. After understanding all the problem and practicing that problem, by following equation I solve the logic diagram. Then build Seven Segment Decoder ic. In the end I answered all the questions.