

Electronics Workshop Project Report

Course Code: EC2.202

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1 Overview

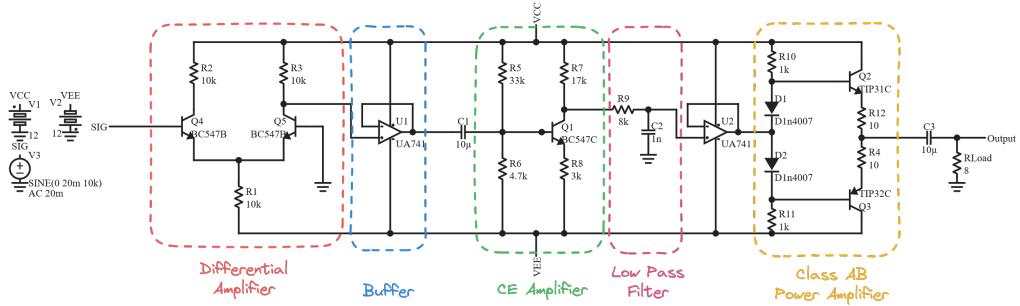


Figure 1: Amplifier Schematic

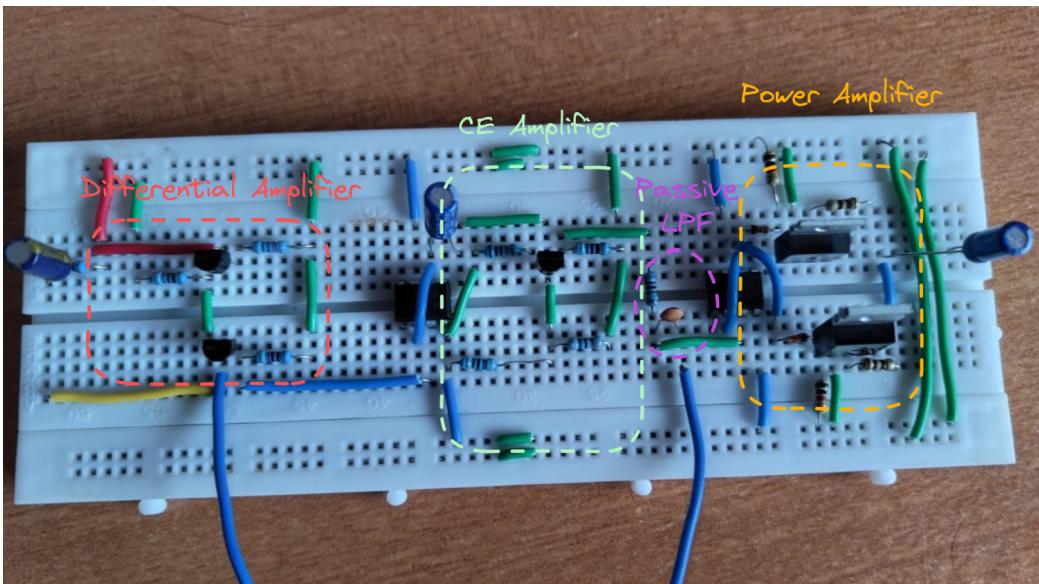


Figure 2: Hardware Implementation of the entire circuit

The objective of this project was to design an audio amplifier which takes in a sound input via a mic and amplifies it to a suitable level to drive an 8Ω speaker, within a power budget of 0.5 W

The performance of an audio amplifier is based upon 4 major parameters:

- Frequency response
- Noise

- Gain
- Distortion

The **first stage** is a pre-amplifier, the **second stage** is a common emitter amplifier to achieve the necessary voltage gain, the **third stage** is a passive low pass filter with a cutoff frequency of 20 kHz and the **last stage** is a class-AB power amplifier to achieve the necessary power levels. We also have intermediate buffers in between stages to prevent loading and to prevent the bias points from getting perturbed for each stage.

Our design utilises this 4-stage architecture to reach suitable current and voltage levels to drive the speaker, while consuming about 500 mW and an overall voltage gain of 113 times.

2 Pre-Amplifier

It is not possible to send an input signal straight to the common emitter amplifier or the power amplifier because this would produce a signal that is too noisy to drive the load (speaker). Thus, a weak electrical signal is transformed into a strong enough output signal to withstand noise and be brought to line level in this stage. A pre-amplifier should have high input impedance i.e., a minimal amount of current is required to sense the input signal and low output impedance to ensure no voltage is dropped at the output.

This stage is also called a pre-amplifier stage which has been implemented using a differential amplifier in the single-ended unbalanced output configuration i.e., one end of the input is connected to the microphone and the other end is grounded.

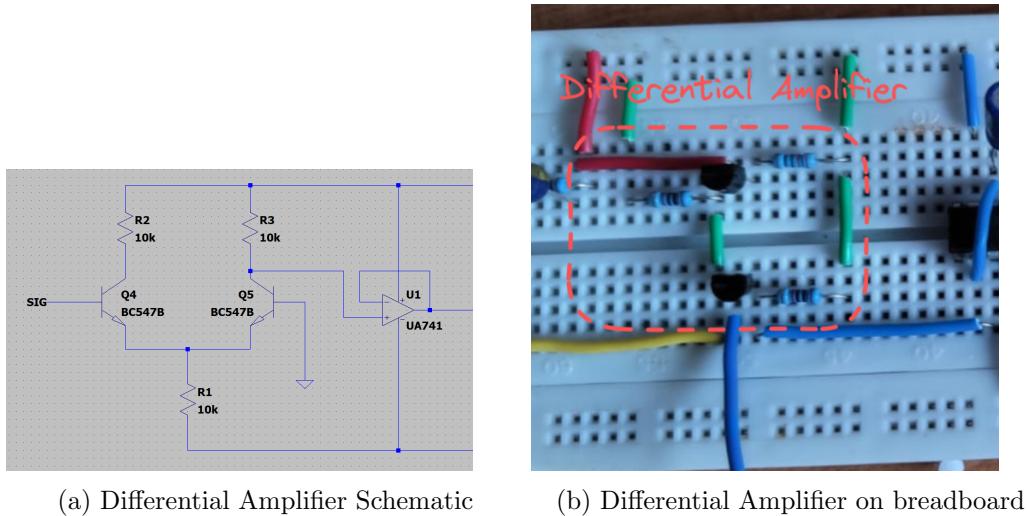


Figure 3: Pre-Amplifier Stage

The differential amplifier de-noises and amplifies an input signal of amplitude 20 mV to an output signal of amplitude 2 V, which is a gain of 100, close to the simulation gain of ≈ 93 .

The gain of a differential-amplifier can be calculated as $A_v = -g_m \cdot R_C$. As $g_m = 0.01$ and $R_C = 10 \text{ k}\Omega$, hence $A_v = 100$.

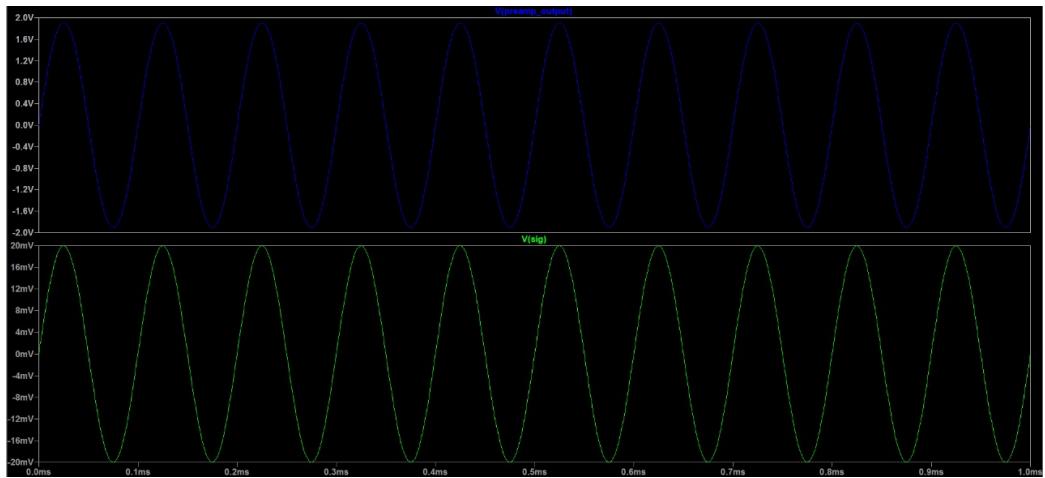


Figure 4: Simulation results for the pre-amplifier design

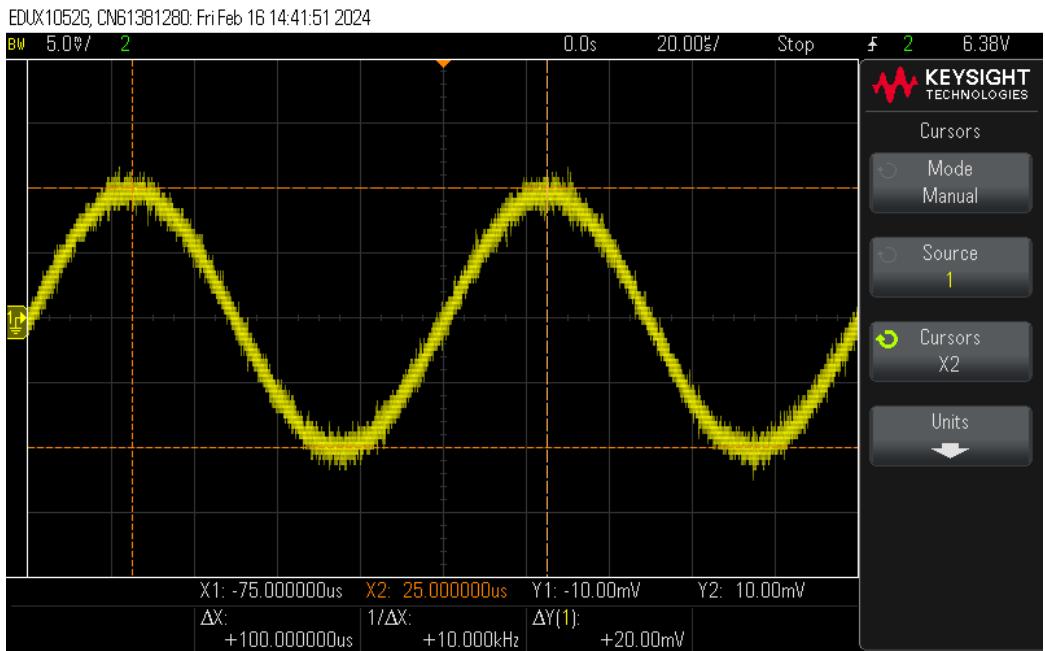


Figure 5: From the actual circuit: Input to the pre-amplifier

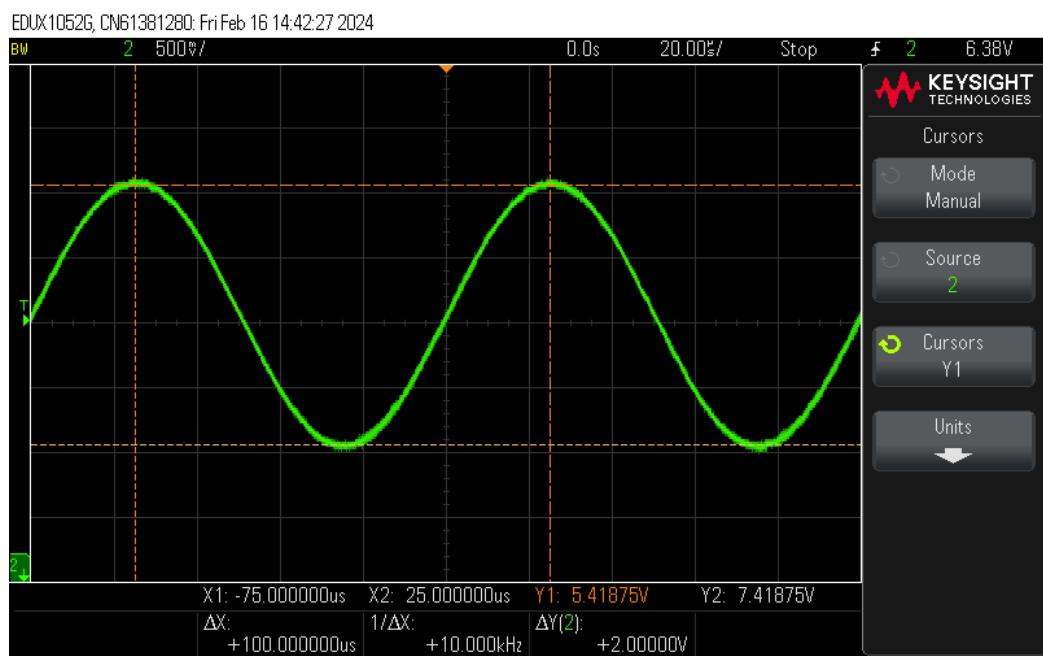
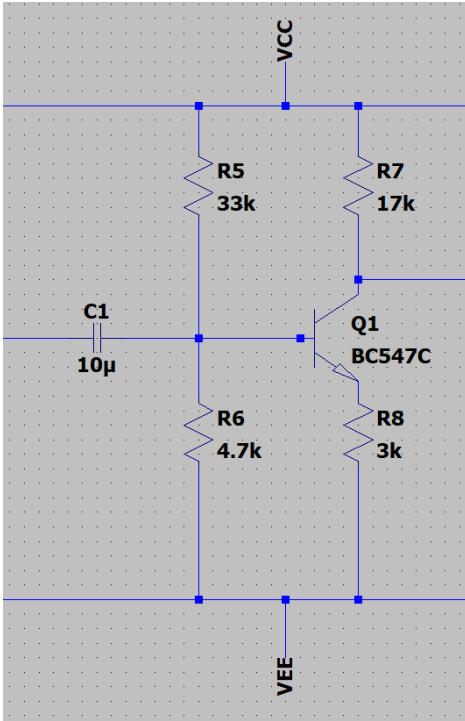
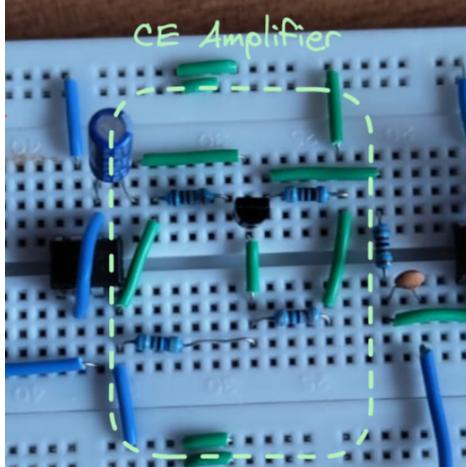


Figure 6: From the actual circuit: Output from the pre-amplifier

3 Common Emitter Amplifier



(a) CE Amplifier Schematic



(b) CE Amplifier on breadboard

Figure 7: CE Amplifier Stage

This stage takes in the output of the differential amplifier ($V_{pp} \approx 3.8 \text{ V}$), and amplifies it further to $V_{pp} \approx 12.8 \text{ V}$, providing a voltage gain of 3.37 times.

Since, we have used a single common emitter amplifier stage, it introduces a phase shift. From the small signal model of a common emitter stage we know that its voltage gain is given by the following equation:

$$\text{Gain} = -\frac{R_C}{\frac{1}{g_m} + R_E}$$

which can be approximated as $-\frac{R_C}{R_E}$ for $R_E \gg \frac{1}{g_m}$

The common emitter stage introduces a 180° phase shift because as the input increases i.e. the voltage at the base of the transistor increases, the current flowing through the base increases.

Since, $I_C = \beta \times I_B$, the collector current also increases which leads to more

voltage being dropped across the collector resistor and hence less voltage at the output terminal; since $V_{out} = V_{CC} - I_C R_C$. This leads to an inverted output from the common emitter stage.

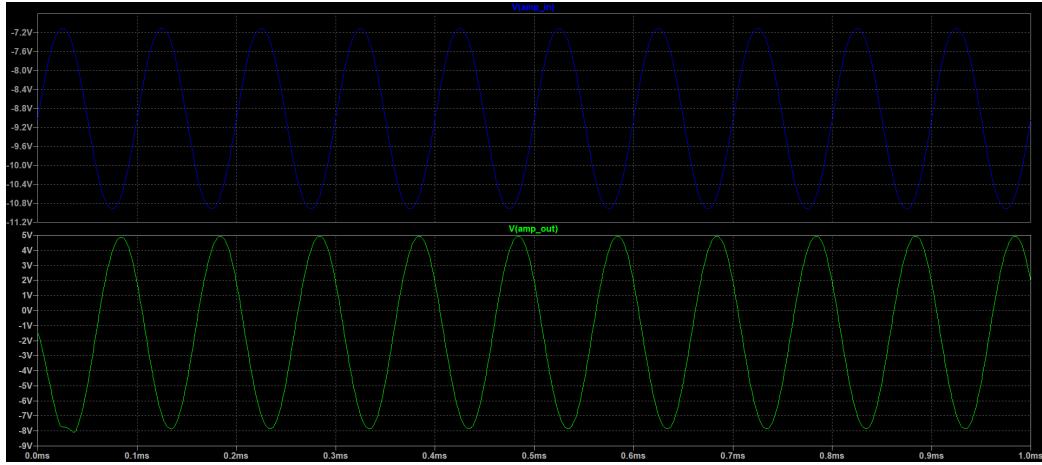


Figure 8: Simulation results for the CE amplifier design

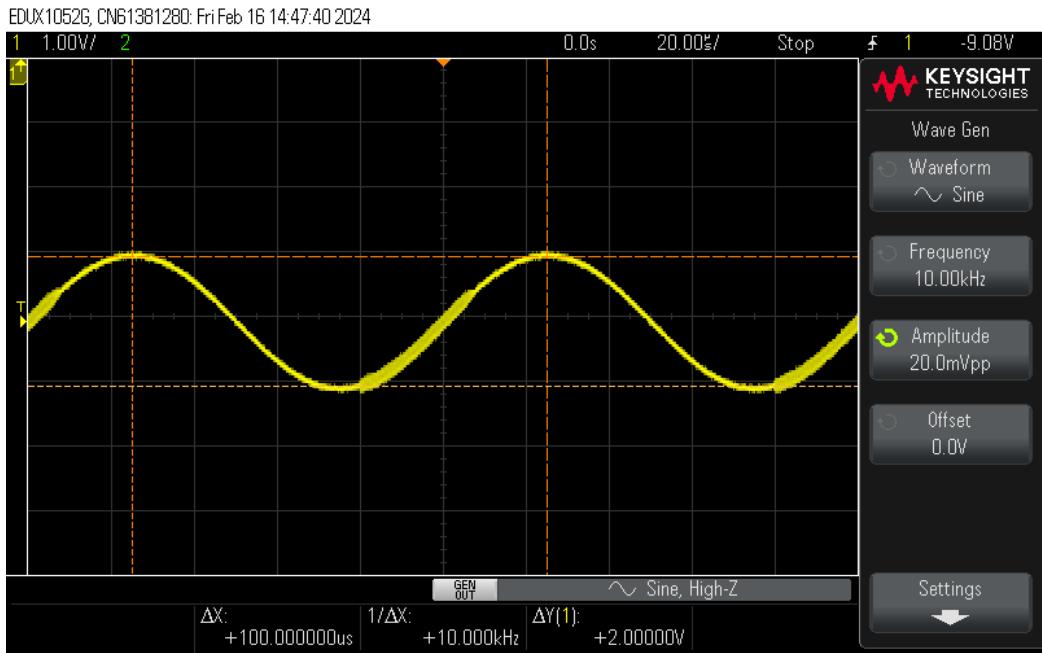


Figure 9: From the actual circuit: Input to the CE amplifier

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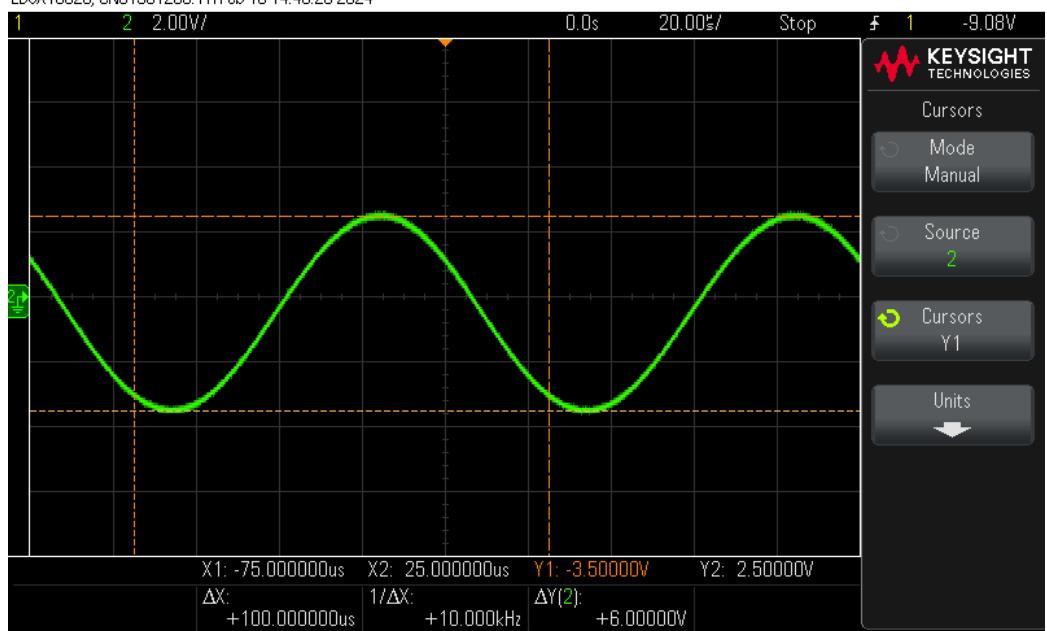


Figure 10: From the actual circuit: Output from the CE amplifier

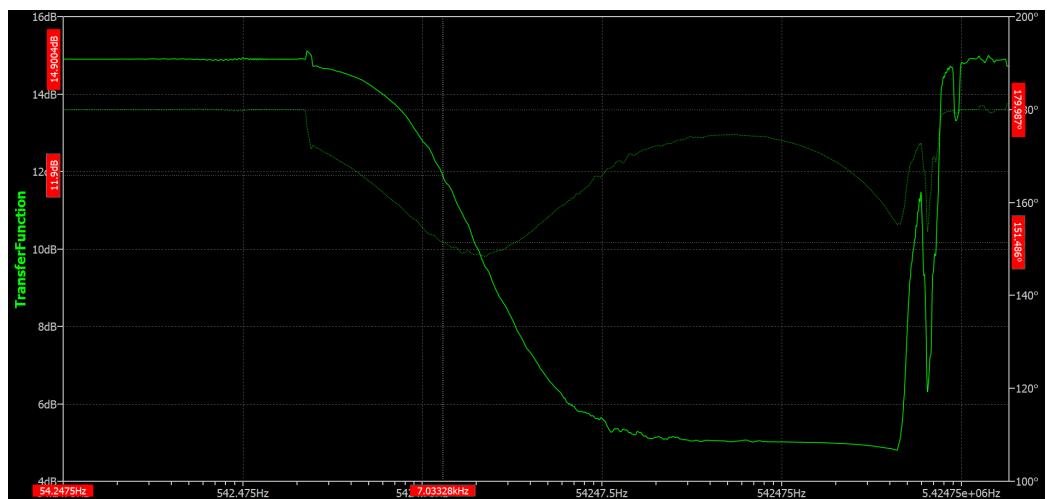


Figure 11: Bode plot of the stage from simulation

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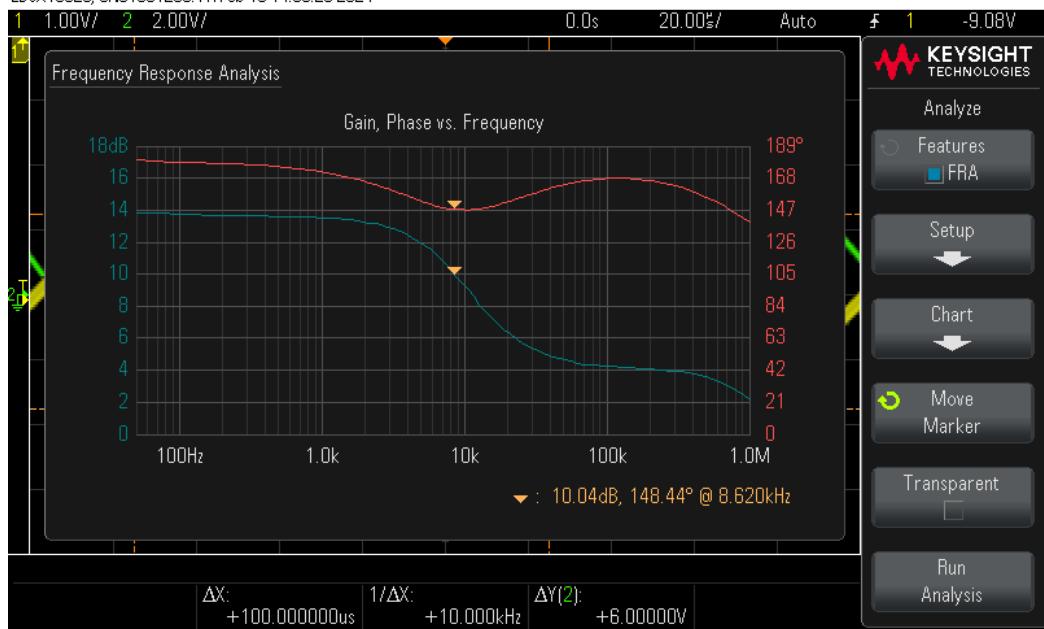
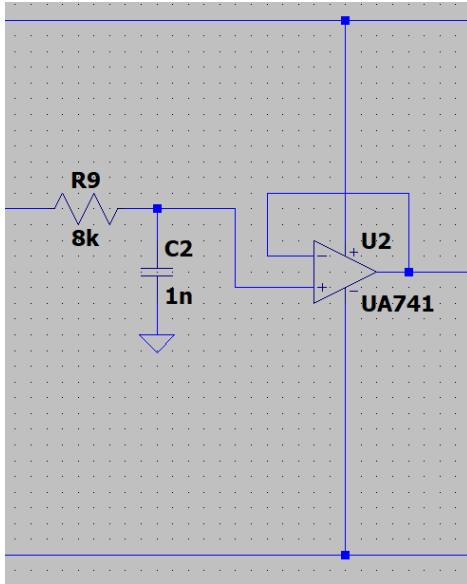
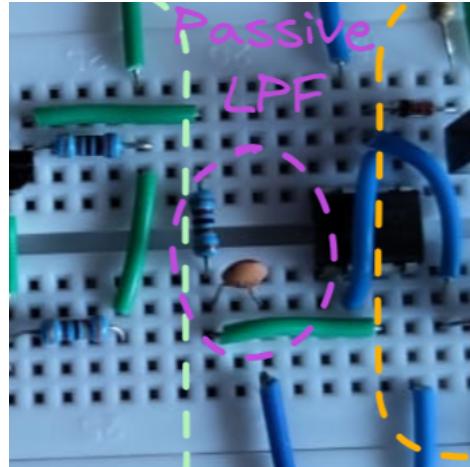


Figure 12: Bode plot of the stage from the actual circuit

4 Low-Pass Filter



(a) Low Pass Filter Schematic



(b) Low Pass Filter on Breadboard

Figure 13: Filter Stage

The filter stage is typically used to adjust the balance of high and low frequencies, permitting the manual adjustment of the frequency response so that we can get frequency selective amplification. This stage helps us eliminate the unwanted noise added in the previous stage of the system and improves the overall tone.

In our implementation, we wish to keep 20 Hz to 20 kHz (which is the ideal hearing range of a human) prominent and attenuate the other frequencies. Here we have implemented a passive low pass filter with a cutoff frequency of 20 kHz. A high-pass filter to attenuate frequencies below 20 Hz has not been implemented since there is negligible presence of frequencies in the range of 0 Hz to 20 Hz.

Calculation for the cutoff frequency:

$$f_c = \frac{1}{2 \cdot \pi \cdot R \cdot C} = \frac{1}{2 \cdot \pi \cdot 8 \cdot 10^3 \cdot 1 \cdot 10^{-9}} = 19.89 \text{ kHz} \approx 20 \text{ kHz}$$

The various plots for this circuit are given below:

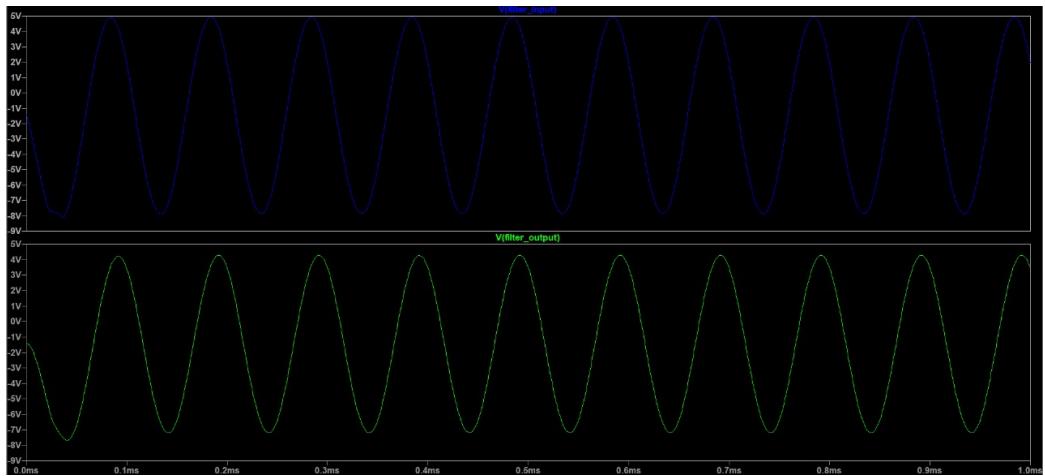


Figure 14: Simulation results for the filter stage

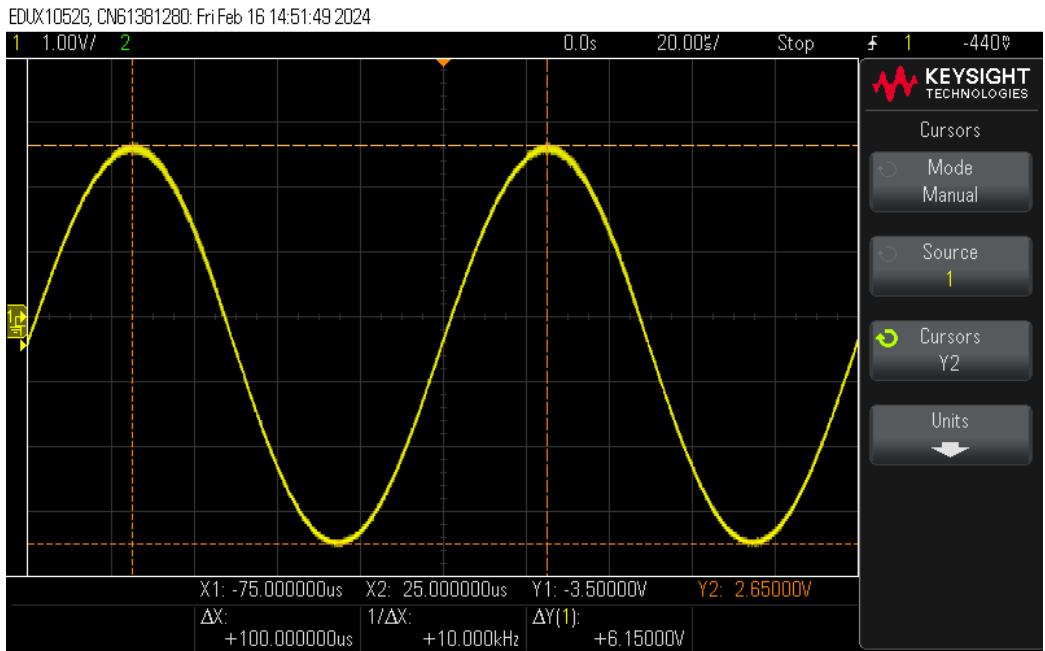


Figure 15: From the actual circuit: Input to the filter stage

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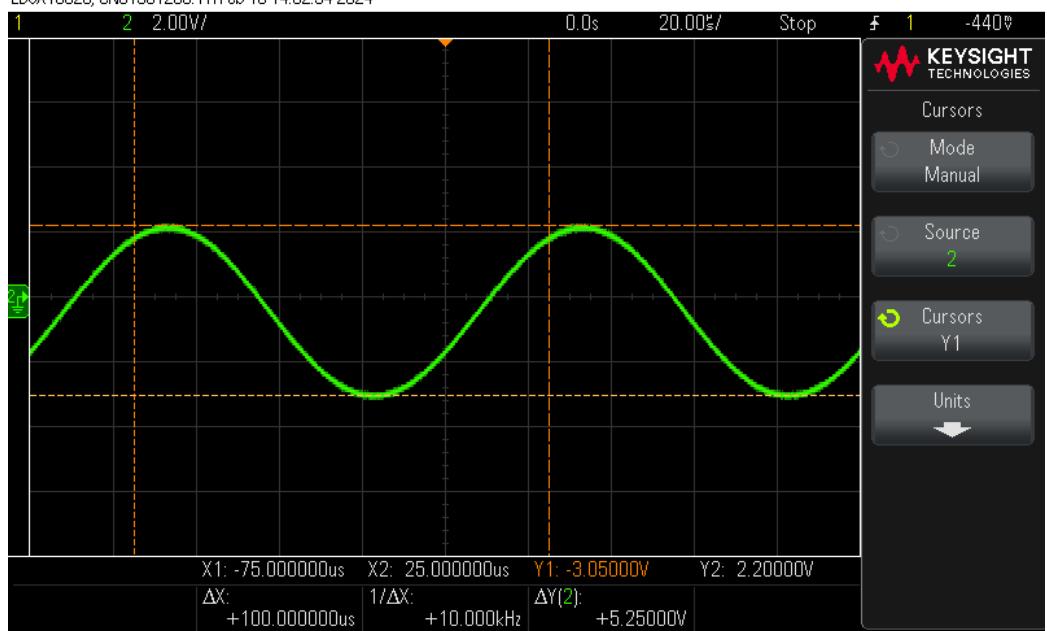


Figure 16: From the actual circuit: Output from the filter stage

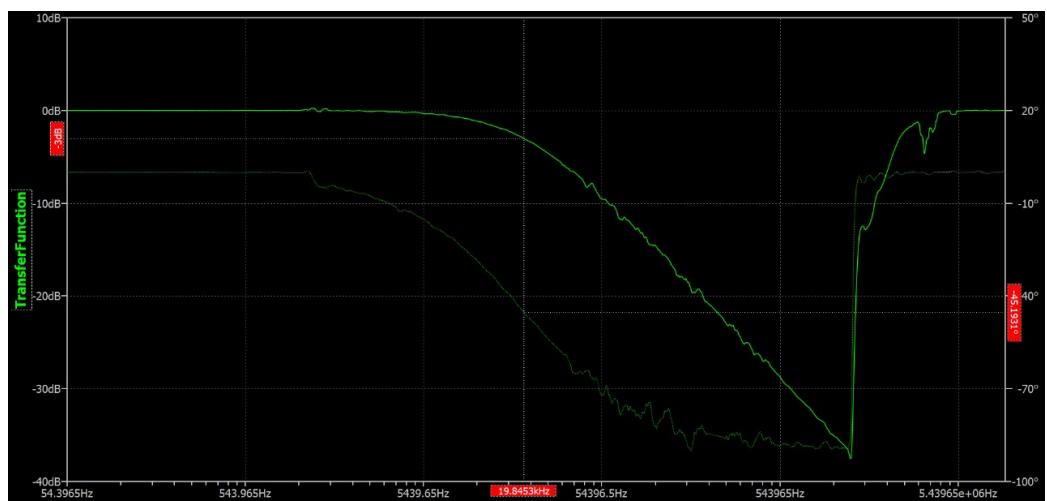


Figure 17: Bode plot of the filter stage from simulation

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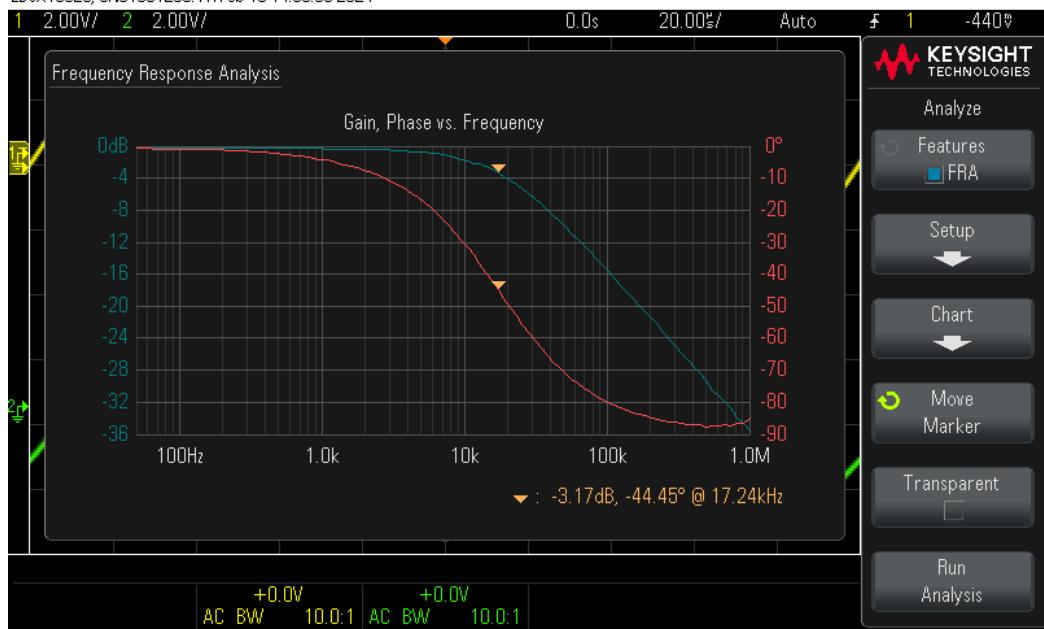
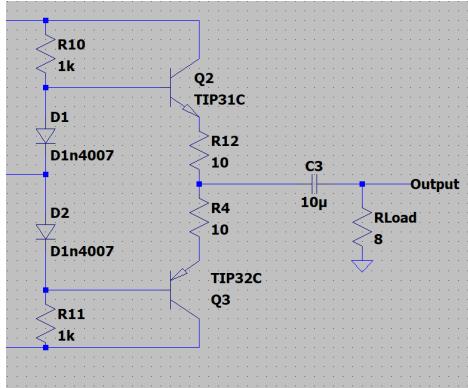
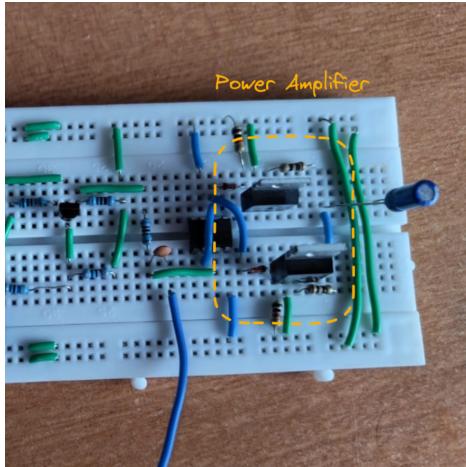


Figure 18: Bode plot of the filter stage from the actual circuit

5 Power Amplifier



(a) Power Amplifier Schematic



(b) Power Amplifier on Breadboard

Figure 19: Class AB power amplifier Stage

The class AB power amplifier receives the amplified and filtered output from the preceding stages, and amplifies the current thus amplifying the overall power being supplied to the 8Ω speaker at the output.

The average power being supplied before the output stage (class AB power amplifier) to the buffer was $\approx 13.58\text{ mW}$ and the average power being supplied after the output stage to the speaker (labelled load in the schematic) was $\approx 393\text{ mW}$ i.e. 29 times the input power.

The Class AB power amplifier has been designed using TIP-31 (NPN) and TIP-32 (PNP) power transistors, since they can handle large amounts of current flowing through them and they have faster switching speeds unlike normal transistors.

Our design utilises two 10Ω resistances as heat sinks to deal with the thermal runaway, which might occur when conducting such high current.

We chose to implement a class-AB power amplifier instead of a class-A or class-B configuration as it gets rid of the cross over distortion seen in class-B setups and it also provides us with higher efficiency than class-A designs.

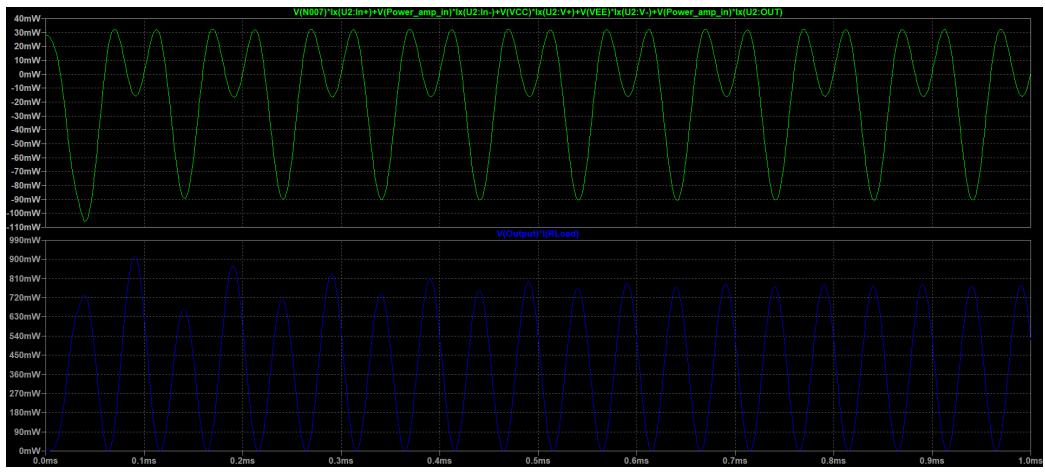


Figure 20: Simulation Results: Power being supplied to the buffer (before power amplifier) vs Power being supplied to the load (after power amplifier)

6 Complete Circuit Plots

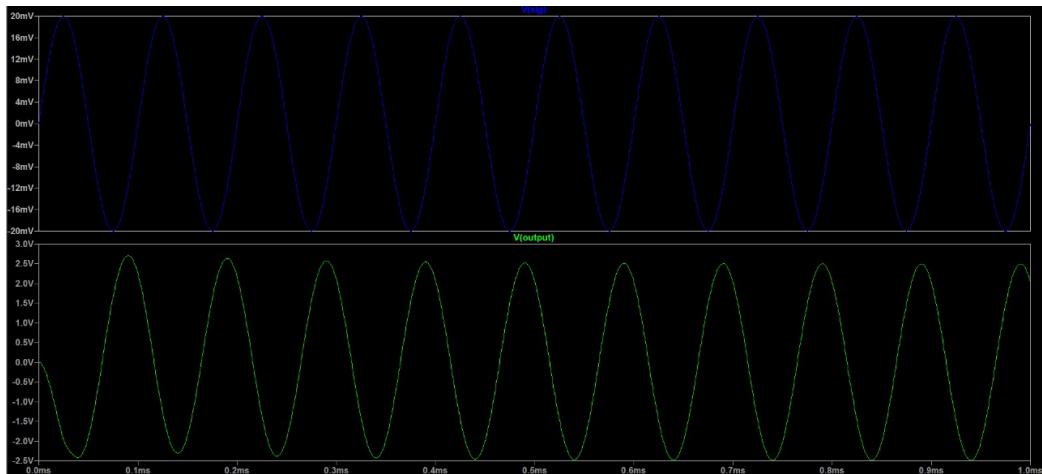


Figure 21: Simulation Results for the entire circuit

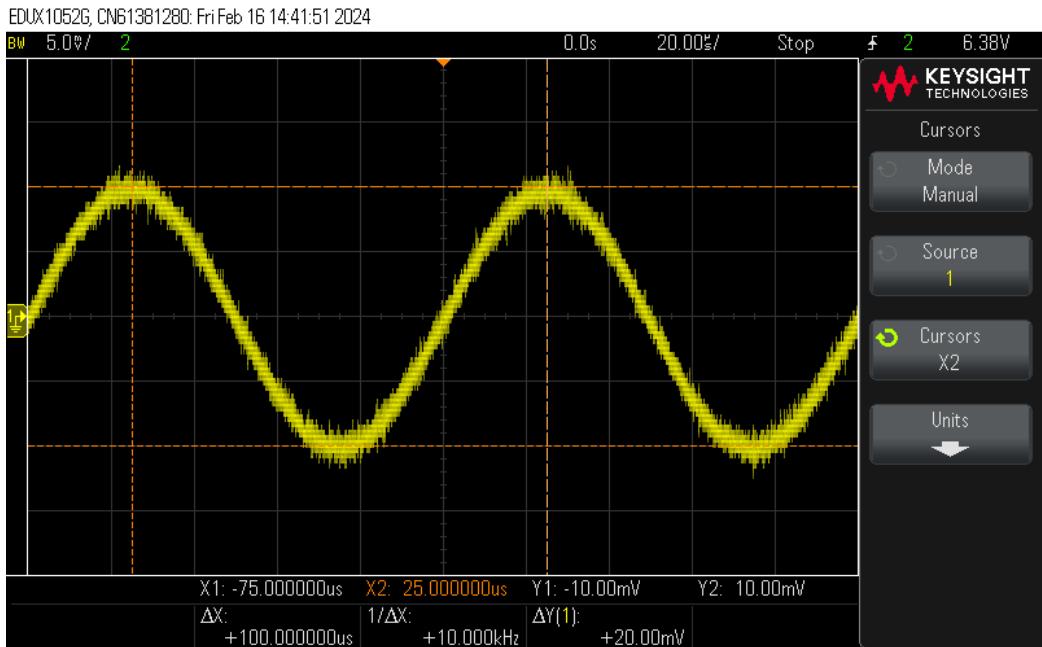


Figure 22: From the actual circuit: Input to the circuit

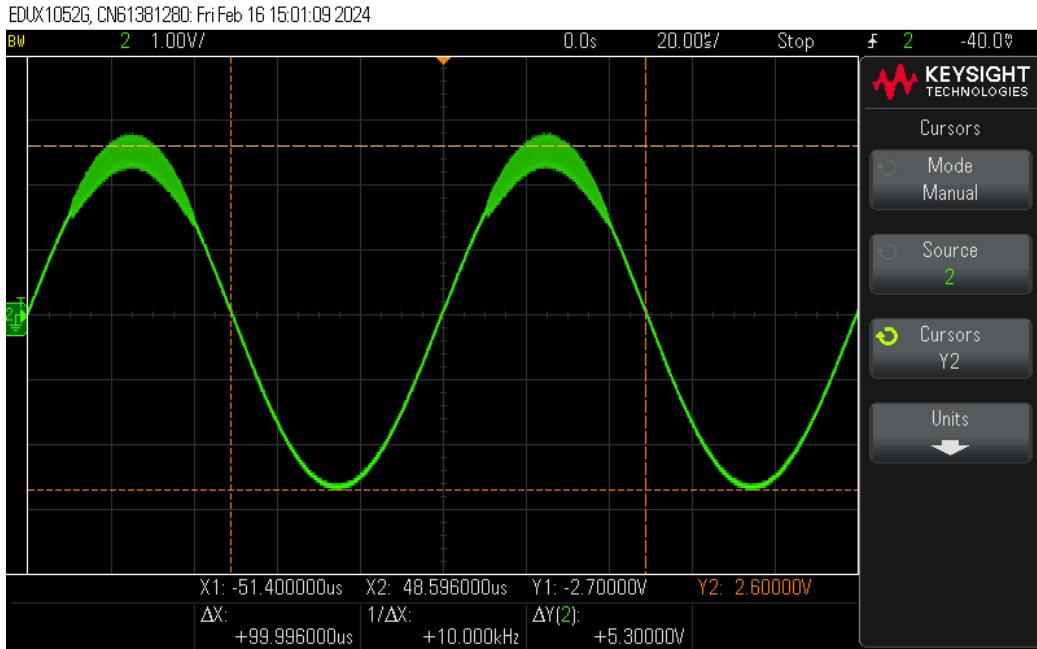


Figure 23: From the actual circuit: Output of the complete circuit

7 Observations and Conclusion

While designing and implementing our audio amplifier we made the following observations:

- 1. Mismatched transistors do not perform well.** We need well-matched transistors for a differential amplifier as one of the key assumptions often made while analysing them is that both the transistors in the differential pair draw equal current. This is not true if the devices aren't well matched. We were not able to find a pair of well matched MOSFETs within the lab inventory and were forced to resort to BJTs. This mismatch is exaggerated in discrete components, compared to ICs.
- 2. Need of proper coupling and biasing between stages.** We need to either use buffers along with coupling capacitors since we are doing discrete biasing, to ensure that the output of one stage doesn't perturb the operating point of another stage and all stages remain properly biased. An alternative solution would be to design a DC-coupled amplifier which doesn't use coupling capacitors. But that could not be used for high frequency applications.

3. **Need to deal with thermal runaway.** If the power amplifier is left unchecked without any sinks, it will lead to thermal runaway which can cause destruction of the transistors or capacitors and other components connected to it in the subsequent stages. As such to deal with it, we have utilised two 10Ω resistors as heat sinks, connected to output of the power transistors.
4. **Contribution of all the stages to the overall frequency response.** All the stages in the circuit have their individual frequency response characteristics and since they are cascaded in our design, the overall frequency response of the system shall be the product of their individual responses. It may lead to unwanted frequency response of the overall system. While designing the audio amplifier we need to take account of the high frequency behavior of all the components not just the filters.

Even though our design succeeds by providing us a good gain value (113 times), staying within the power budget ($P_{avg} \approx 393\text{ mW}$), it is by no means a high fidelity audio amplifier. As such there still exists further scope for improvement. Some of the ways in which it can be improved are as follows:

1. **Use of better matched transistors.** Instead of using multiple discrete transistors which not only are poorly matched (relatively) but also introduce a lot of noise of their own accord, a better approach would be to use transistors that come in IC like packages i.e. multiple transistors on the same IC i.e. use of **transistor arrays**. Besides all of the previously mentioned merits, they also save up on PCB/bread-board area.
2. **Use of a class D amplifier.** Instead of using a class AB power amplifier as the output stage, we could use a class-D amplifier for better power efficiency. But it will be a trade-off between fidelity and power efficiency as it is not easy to design a high fidelity class-D power amplifier.
3. **Use of a higher order active filter.** Instead of using a first order passive low pass filter, if we were to use a higher order active filter, we would get a much better frequency response and cutoff frequencies. We could even implement tone control by using an active filter with adjustable cutoff frequency. At the same time, we would need to carefully balance the trade-off between improved magnitude response and a degraded phase response with the higher order filters.

4. **Use of multiple intermediate gain stages to achieve higher overall gain.** In the above presented configuration our design achieves ≈ 41 dB, if we were to use multiple stages for gain we would achieve an even higher overall gain and if we were to use an even number of gain stages, it would get rid of any inversion introduced by those stages.
5. **Use of amplifiers with positive feedback loop** An alternative approach to increasing the overall gain of the system, it would not only need to higher gain but can also be used for noise suppression.