Vivado Project Options:
  Target Device : xc7a200t–fbg676
  Speed Grade : –2
  HDL : verilog
  Synthesis Tool : VIVADO

If any of the above options are incorrect, please click on "Cancel", cha

MIG Output Options:
  Module Name : mig_7series_0
  No of Controllers : 1
  Selected Compatible Device(s) : ––

FPGA Options:
  System Clock Type : Differential
  Reference Clock Type : Differential
  Debug Port : OFF
  Internal Vref : enabled
  IO Power Reduction : ON
  XADC instantiation in MIG : Enabled

Extended FPGA Options:
  DCI for DQ,DQS/DQS#,DM : enabled
  Internal Termination (HR Banks) : 40 Ohms

/***/
/*   Controller 0   */

```
/*****************************************************************/
Controller Options :
   Memory                   : DDR3_SDRAM
   Interface                : NATIVE
   Design Clock Frequency       : 3000 ps (333.33 MHz)
   Phy to Controller Clock Ratio : 2:1
   Input Clock Period           : 2999 ps
   CLKFBOUT_MULT (PLL)          : 4
   DIVCLK_DIVIDE (PLL)          : 1
   VCC_AUX IO                   : 1.8V
   Memory Type                  : Components
   Memory Part                  : MT41J128M8XX-125
   Equivalent Part(s)           : --
   Data Width                   : 64
   ECC                      : Disabled
   Data Mask                    : enabled
   ORDERING                     : Strict

AXI Parameters :
   Data Width                   : 256
   Arbitration Scheme           : RD_PRI_REG
   Narrow Burst Support         : 0
   ID Width                 : 4

Memory Options:
   Burst Length (MR0[1:0])          : 8 - Fixed
   Read Burst Type (MR0[3])         : Sequential
   CAS Latency (MR0[6:4])           : 5
   Output Drive Strength (MR1[5,1]) : RZQ/7
   Controller CS option             : Enable
   Rtt_NOM - ODT (MR1[9,6,2])       : RZQ/4
   Rtt_WR - Dynamic ODT (MR2[10:9]) : Dynamic ODT off
```

Memory Address Mapping : BANK_ROW_COLUMN

Bank Selections:

Bank: 33

Byte Group T0: DQ[32–39]
Byte Group T1: DQ[40–47]
Byte Group T2: DQ[48–55]
Byte Group T3: DQ[56–63]

Bank: 34

Byte Group T1: Address/Ctrl–0
Byte Group T2: Address/Ctrl–2
Byte Group T3: Address/Ctrl–1

Bank: 35

Byte Group T0: DQ[0–7]
Byte Group T1: DQ[8–15]
Byte Group T2: DQ[16–23]
Byte Group T3: DQ[24–31]

Reference_Clock:

SignalName: clk_ref_p/n

PadLocation: M21/M22(CC_P/N) Bank:

System_Clock:

SignalName: sys_clk_p/n

PadLocation: P4/N4(CC_P/N) Bank: 34

System_Control:

SignalName: sys_rst

PadLocation: No connect Bank: Select

SignalName: init_calib_complete

PadLocation: No connect Bank: Select

SignalName: tg_compare_error

PadLocation: No connect Bank: Select