Tsubasa Koyama

Curriculum Vitae

Software Engineer II, Pegasus Verification System
Cadence Design Systems, Inc., Taiwan
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Homepage *GitHub* *LinkedIn*

Employment History

Sep. 2023 – present **Software Engineer II, Pegasus Verification System**, *Cadence Design Systems, Inc.*, Taiwan

- Layout Versus Schematic (LVS) RC-mode
  - Implemented a new netlist comparison algorithm for internal testing, achieving ∼6× speedup and ∼80% memory reduction, enhancing overall in-house testing turnaround time.
  - Contributed to LVS RC extraction development for evolving advanced-node requirements across multiple leading foundries, improving engine performance and reducing gaps between new and legacy engines.

Education

Sep. 2021 – Aug. 2023 **MSc, Computer Science**, *National Tsing Hua University*, Taiwan

- Tsing Hua Emerging Technology Automation (THETA) Lab
  - Advisor: **Prof. Tsung-Yi Ho**
  - Research Focus: Electronic Design Automation (EDA), Artificial Intelligence (AI)
- Master Thesis: *Hybrid Refinement Strategy for Package Substrate Routing*
- Overall GPA: *3.86/4.30*

Sep. 2017 – Jun. 2021 **BSc, Computer Science and Information Engineering**, *Tamkang University*, Taiwan

- Independent Study: *TRIP-2-GO ∼ A Convenient Platform for Traveler ∼*
- Overall GPA: *3.96/4.00*

Selected Publications

2025 Ding-Hsun Lin, **Tsubasa Koyama**, Yu-Jen Chen, Keng-Tuan Chang, Chih-Yi Huang, Chen-Chao Wang, and Tsung-Yi Ho. "Hybrid Detour Refinement Strategy for Package Substrate Routing," *30th Asia and South Pacific Design Automation Conference (**ASP-DAC**)*, 2025

2024 **Tsubasa Koyama**, Ding-Hsun Lin, Yu-Jen Chen, Keng-Tuan Chang, Chih-Yi Huang, Chen-Chao Wang, and Tsung-Yi Ho. "Hybrid Refinement Strategy for Package Substrate Routing," *The 25th Workshop on Synthesis And System Integration of Mixed Information technologies (**SASIMI**)*, 2024

2023 Peng-Tai Huang, **Tsubasa Koyama**, Keng-Tuan Chang, Chih-Yi Huang, Chen-Chao Wang, and Tsung-Yi Ho. "Deep Learning based Refinement for Package Substrate Routing," *73rd IEEE Electronic Components and Technology Conference (**ECTC**)*, 2023

Selected Coursework

2023 **VLSI Design for Manufacturability**, *Algorithm Implementation*, GitHub repo.

- The manufacturing-aware physical design are introduced in this course. Some representative research works in this area are studied and a variety of algorithmic techniques for solving these challenging problems efficiently are learnt.
- Implemented Algorithm: Timing-Aware Fill Insertion (Modified ICCAD'18 CAD Contest Problem C)

2022 **FPGA Architecture and CAD**, *Algorithm Implementation*, GitHub repo.

- This course introduces the characteristics, evolution and usage of field-programmable technologies, and also look into some advanced researches related to FPGA architecture and CAD.
- Implemented Algorithm: Topology-Driven Partitioning for Multi-FPGA Systems

2022 **VLSI System Design**, *SW & HW Design Implementation*, GitHub repo.

- This course covers modern preespectives on the digital VLSI system designs including the concepts of system with hardware and software components, and their integration, efficient hardware design and its methodology, and synthesis-based (cell-based) design flow.
- Implemented Design: Convolutional Neural Network Accelerator for Image Denoising

2021 **Advanced Logic Synthesis**, *Algorithm Implementation*, GitHub repo.
- This course covers various aspects of logic optimization including logic minimization, timing optimization, technology mapping, low power design, synthesis for finite state machines, hardware security.
- Implemented Algorithm: Two-stage Algorithm for Technology Mapping

2021 **VLSI Physical Design Automation**, *Algorithm Implementation*, GitHub repo.
- This is a course on algorithms for VLSI physical design automation. Topics include partitioning, floorplanning, placement, routing, and other related issues.
- Implemented Algorithms: Two-way Min-cut Partitioning, Fixed-outline Floorplan Design, Routing with Cell Movement Advanced (ICCAD'21 CAD Contest Problem B)

Areas, Services, and Skills

EDA Areas	Physical Design Automation, Package Substrate Routing Algorithms
AI Areas	Classification, Object Detection, Reinforcement Learning
Other Areas	RTL Design, Synthesis, Automatic Placement & Routing
Tools	Innovus, Allegro, Virtuoso, IC Compiler, Design Compiler, VCS, Formality, PrimeTime, etc.
Programming	C, C++, Python, Verilog, TCL, Shell Script
TA	Introduction of Integrated Circuit Design (CS, 2022)
Languages	Japanese (native; JLPT N1: full score), Mandarin (native), English (vantage; TOEIC: 855)

Extracurricular Activities

2022 **Synopsys Purple 100 Program - Fastrack to SoC Design Career** -
Module A: SoC Frontend Design, Module B: Physical Design

2017 – 2021 **Teaching Assistant** at Sunny English, Taipei

2019 **Web Development Summer Camp** hosted by GSS Corporation & TKU

2018 **Vice Captain** of TKU Department Volleyball Team

Hobbies Playing Sports (Volleyball, Badminton, etc.), Playing Board Games, Going to Karaoke, Listening to Music, Watching Anime, Reading Light Novels