

Автоматизоване проектування комп'ютерних та систем

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Частина 1. Тема №2. Основи систем автоматизованого проектування. (2 години)

Частина 1. Тема №3. Високорівневе проектування комп'ютерних систем і автоматичний синтез до нижчих рівнів. (8 годин)

Частина 1. Тема №4. Проектування комп'ютерних систем на рівні топології кристалу. (10 годин)

Частина 1. Тема №5. Проектування комп'ютерних систем на рівні топології друкованої плати. (2 години)

Частина 2. Тема №6. Прикладне програмування комп'ютерних систем за допомогою високорівневих фреймворків. (6 годин)

SW: Application
SW: C++ Boost
SW: C++ STL
SW: C++11
SW: C++
SW: C
SW: Assembler

SW

(TLM)HW: SystemC/SystemVerilog

(Architecture, CE)

HW

(RTL)HW: VHDL/Verilog

(Logic Circuit, CE)(1)

HW: VHDL/Verilog

(Logic Circuit, CE)(2)

HW: SPICE/Verilog

(Physical Design, EE)(1)

HW: SPICE

(Physical Design, EE)(2)

HW: SPICE/GDSII

(Physical Design, EE-PD)

tape-in

(DFM)HW: GDSII

(Physical Design, EE-PD)

tape-out

Високорівневе проектування комп'ютерних систем і автоматичний синтез до низьких рівнів.



The screenshot shows the Open SystemC Initiative website. At the top left is the SystemC logo, and at the top right is the text "OPEN SYSTEMC INITIATIVE" with the tagline "Defining & Advancing SystemC Standards". Below this is a navigation bar with links: ABOUT OSCI, LOGIN, DOWNLOADS, WORKING GROUPS, SYSTEMC COMMUNITY, NEWS & EVENTS, and DISCUSSION FORUMS. A search bar is located on the right side of the navigation bar. On the left side of the page, there is a sidebar with links: Overview, About SystemC, Regional User Groups, and Resources. The main content area is titled "About SystemC" and includes a sub-header "The Language for System-Level Modeling, Design and Verification". The text below describes SystemC as a language built in standard C++ by extending the language with the use of class libraries, addressing the need for a system design and verification language that spans hardware and software.

SYSTEMC™

OPEN SYSTEMC INITIATIVE
Defining & Advancing SystemC Standards

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Overview
About SystemC
Regional User Groups
Resources

Home » [SystemC Community](#) » **About SystemC**

About SystemC

The Language for System-Level Modeling, Design and Verification

Ratified as IEEE Std. 1666™-2005, SystemC™ is a language built in standard C++ by extending the language with the use of class libraries. SystemC addresses the need for a system design and verification language that spans hardware and software. The language is particularly suited to model system's partitioning, to evaluate and verify the assignment of blocks to either hardware or software implementations, and to architect and measure the interactions between and among functional blocks. Leading companies in the intellectual property (IP), electronic design automation (EDA), semiconductor, electronic systems, and embedded software industries currently use SystemC for architectural exploration, to deliver high-performance hardware blocks at various levels of abstraction and to develop virtual platforms for hardware/software co-design.

Високорівневе проектування комп'ютерних систем і автоматичний синтез до нищих рівнів.

Standard **Active**

IEEE 1800-2017 - IEEE Standard for SystemVerilog--Unified Hardware Design, Specification, and Verification Language

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ACCESS VIA SUBSCRIPTION

Explore This Standard

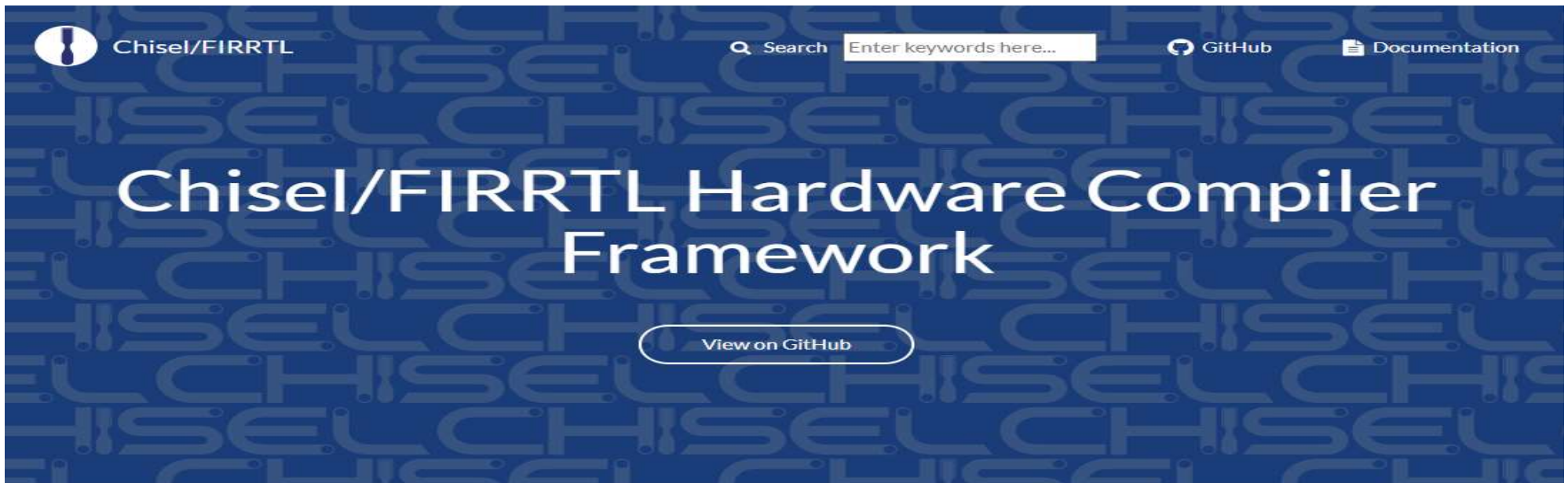
- Standard Details
- Additional Resources
- Working Group

Standard Details

The definition of the language syntax and semantics for SystemVerilog, which is a unified hardware design, specification, and verification language, is provided. This standard includes support for modeling hardware at the behavioral, register transfer level (RTL), and gate-level abstraction levels, and for writing testbenches using coverage, assertions, object-oriented programming, and constrained random verification. The standard also provides application programming interfaces (APIs) to foreign programming languages. (The PDF of this standard is available at no cost at <https://ieeexplore.ieee.org/browse/standards/get-program/page> compliments of Accellera Systems Initiative)

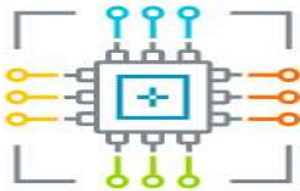
Sponsor Committee **C/DA - Design Automation**

**Високорівневе проектування комп'ютерних систем і
автоматичний синтез до нижчих рівнів.**



CHISEL

ARM



Processor IP >

Arm is the leading technology provider of processor IP, offering the widest range of processors to address the performance, power, and cost requirements of every device. Arm CPUs and NPUs include Cortex-A, Cortex-M, Cortex-R, Neoverse, Ethos and SecurCore.



Security IP >

CryptoCell, TrustZone, SecurCore, Cortex-M35P



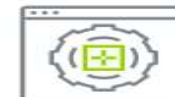
System IP >

CoreLink, CoreSight, Coherent Mesh Network, AMBA and more



Graphics and Multimedia >

Arm Mali GPUs and Mali Camera series of ISPs



Software and Development Tools >

Keil RTX5, Allinea Studio, Compilers, Debuggers and more

ARM

arm Developer

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All IP Products

Processors

Graphics and multimedia processors

System IP

Physical IP

Security IP

Subsystem

All IP Products

Arm DevSummit

Join our global community of hardware designers and software developers for an online event that puts cutting-edge technology right at your fingertips.

Processors

Design, verify and program Arm processors.

Graphics and Multimedia Processors

Arm Mali multimedia IP includes Mali graphics processors and Mali camera image signal processors.

System IP

Configure and build performant, power efficient SoCs, which you can differentiate by combining Arm processors with your own IP elements using AMBA interfaces.

Physical IP

Artisan Physical IP delivers the most comprehensive and advanced physical IP solution in the industry. Available for free through the DesignStart Tier of Arm Flexible Access, Artisan Physical IP is the fastest, simplest route to a custom System on Chip.

Security IP

Explore subsystems that provide platform level security, acceleration and offloading.

Subsystem

Learn more about Corstone, and directly integrate solutions into your design.

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arm Developer

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IP configuration tools

Open Source Software

Embedded

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Graphics and gaming

Development boards

Simulation models

Licensing

Simulation models

Arm Flexible Access Models

The Arm Flexible Access Model package allows SoC architects to make a well-informed decision on what Arm IP and IP configuration to choose for their next project.

DesignStart simulation models

DesignStart simulation models allow developers to evaluate the performance of Arm technology, and enable software teams to begin sooner.

Fast Models

Fast Models are accurate, flexible programmer's view models of Arm IP, allowing you to develop software like drivers, firmware, OS, and applications before silicon availability.

Cycle Models

Cycle Models are compiled directly from Arm RTL and retain complete functional and cycle accuracy. This enables you to confidently make architectural decisions, optimize performance, or develop bare-metal software.

Fixed Virtual Platforms

Running at speeds comparable to the real hardware, Fixed Virtual Platforms are complete simulations of an Arm system, including processor, memory, and peripherals.

AMBA TLM library

The Arm AMBA Transaction-Level Modeling (TLM) library allows you to model and simulate approximately-timed and cycle-accurate AXI4 and ACE ports.

ARM

arm IP Exchange

Cycle Models

Home Models Platforms Support

Cortex A-Series

- Cortex-A32
- Cortex-A35
- Cortex-A53
- Cortex-A55

Cortex R-Series

- Cortex-R5
- Cortex-R52
- Cortex-R8
- Cortex-R82
- Cortex-R52+

Cortex M-Series

- Cortex-M0+
- Cortex-M23
- Cortex-M33
- Cortex-M7
- Cortex-M55

Cortex-A55 Cycle Model

The Arm® Cortex-A55 core delivers the best combination of power efficiency and performance in its class. It is part of the first generation of application CPUs based on DynamIQ technology and features the latest Armv8-A architecture extensions, with dedicated machine learning instructions. The Cortex-A55 Cycle Model includes the DynamIQ Shared Unit (DSU).

DSU r4p1 supports Cortex-A55 r2p0.

Supported Rxy Rev: r4p1

Supported Platforms: SystemC, PlatformArchitect, RSM

AMBA TLM Library

Overview

Arm Flexible Access Models

DesignStart Simulation Models ▾

Fast Models ▾

Cycle Models ▾

Fixed Virtual Platforms ▾

AMBA TLM ▾

Overview

The Arm AMBA Transaction-Level Modeling (TLM) library allows you to model and simulate approximately-timed (AT) and cycle-accurate (CA) AXI4 and ACE ports. This C++ library is provided as a pre-compiled binary library.

This library is intended for use with:

- Arm Cycle Models
- Custom AT and CA models used for virtual prototype development
- Third-party models that use supported AMBA interfaces

RISC-V



RISC-V Exchange: Cores & SoCs

This page is a collection of available intellectual property (IP) cores and SoCs in the RISC-V ecosystem. This list is curated by the community – which includes you! Add cores, SoC platforms, and SoCs to the list by filing a pull request on the [GitHub repository](#). If you have any questions about this process, [contact us](#) for help.

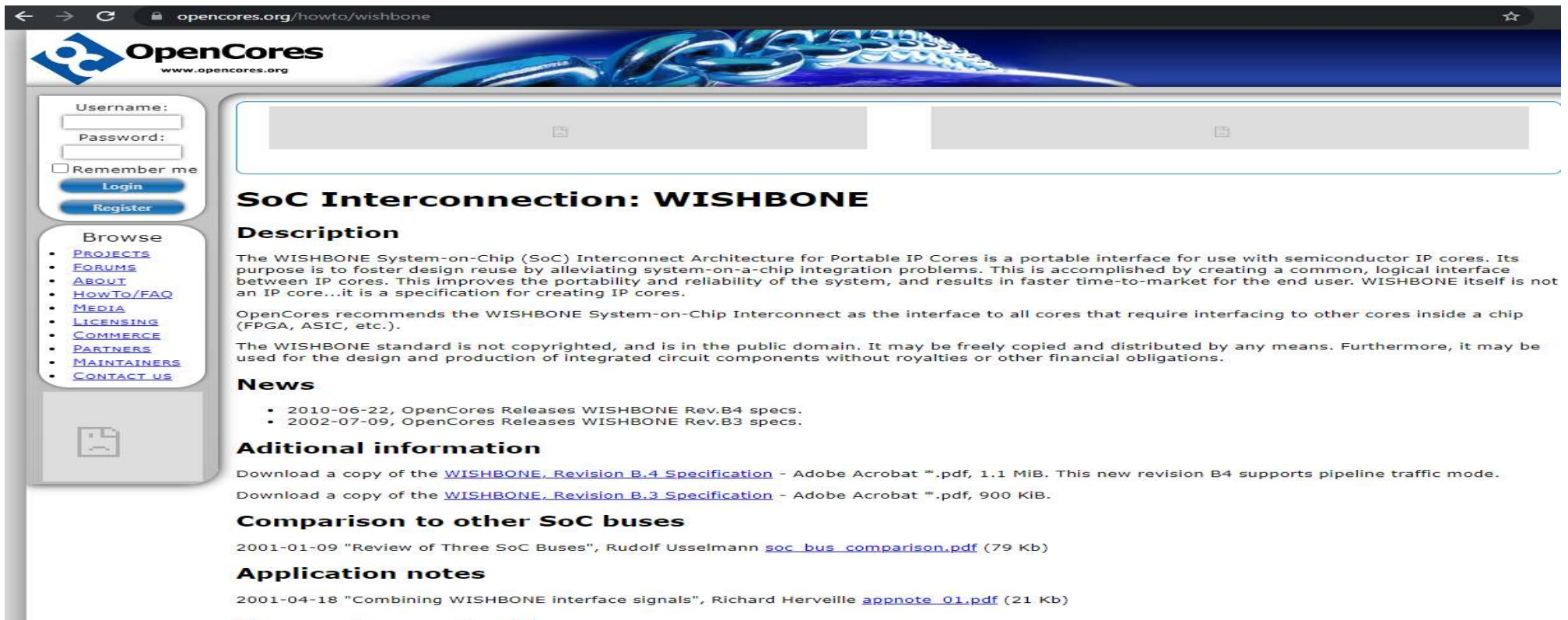
Please note that the Exchange can showcase available physical hardware on the [Available Boards](#) page.

- Cores
- SoC Platforms
- SoCs

Search:

Name	Supplier	Links	Capability	Priv. spec	User spec	Primary Language	License
RV32EC_P2	IQonIC Works	Website	RV32	1.11	RV32E[M]C/RV32I[M]C	SystemVerilog	IQonIC Works Commercial License
RV32IC_P5	IQonIC Works	Website	RV32	1.11	RV32I[M][N][A]C	SystemVerilog	IQonIC Works Commercial License

Wishbone



The screenshot shows the OpenCores.org website with the URL `opencores.org/howto/wishbone` in the browser address bar. The page features a blue header with the OpenCores logo and a decorative image of a chip. On the left, there is a sidebar with a login/register section and a 'Browse' menu. The main content area is titled 'SoC Interconnection: WISHBONE' and includes a 'Description' section, a 'News' section with two bullet points, an 'Additional information' section with two download links, a 'Comparison to other SoC buses' section with a link, and an 'Application notes' section with a link.

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SoC Interconnection: WISHBONE

Description

The WISHBONE System-on-Chip (SoC) Interconnect Architecture for Portable IP Cores is a portable interface for use with semiconductor IP cores. Its purpose is to foster design reuse by alleviating system-on-a-chip integration problems. This is accomplished by creating a common, logical interface between IP cores. This improves the portability and reliability of the system, and results in faster time-to-market for the end user. WISHBONE itself is not an IP core...it is a specification for creating IP cores.


OpenCores recommends the WISHBONE System-on-Chip Interconnect as the interface to all cores that require interfacing to other cores inside a chip (FPGA, ASIC, etc.).


The WISHBONE standard is not copyrighted, and is in the public domain. It may be freely copied and distributed by any means. Furthermore, it may be used for the design and production of integrated circuit components without royalties or other financial obligations.

News

- 2010-06-22, OpenCores Releases WISHBONE Rev.B4 specs.
- 2002-07-09, OpenCores Releases WISHBONE Rev.B3 specs.

Additional information

Download a copy of the [WISHBONE, Revision B.4 Specification](#) - Adobe Acrobat , 1.1 MiB. This new revision B4 supports pipeline traffic mode.

Download a copy of the [WISHBONE, Revision B.3 Specification](#) - Adobe Acrobat , 900 KIB.

Comparison to other SoC buses

2001-01-09 "Review of Three SoC Buses", Rudolf Usselmann [soc_bus_comparison.pdf](#) (79 Kb)

Application notes

2001-04-18 "Combining WISHBONE interface signals", Richard Herveille [appnote_01.pdf](#) (21 Kb)

Wishbone

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WISHBONE


Wishbone is an open source standard bus that connects slave peripherals to a master CPU. Instant SoC V1.2 supports Wishbone and you can easily add your own VHDL or Verilog peripherals to the Instant SoC RISC-V system. Instant SoC supports the B4 version of Wishbone.

The diagram illustrates the Wishbone Bus architecture. On the left is the 'Instant SoC Wishbone Master' and on the right is the 'Wishbone Slave'. They are connected via a central bus. The master's output signals (RST_O, ADI_O, DAT_O, WE_O, STB_O, ACK_I, CYC_O) are connected to the slave's input signals (RST_I, CLK_I, ADI_I, DAT_I, WE_I, STB_I, ACK_O, CYC_I). A 'SysCik' signal is shown at the top, connected to the master's RST_O and the slave's RST_I.

Wishbone Bus

To add a Wishbone component you simply creates a [FC_Wishbone](#) object in C++ with a file path to the component and Instant SoC adds the component and maps all Wishbone bus signals to the system. The file could be a Verilog (*.v) or VHDL (*.vhd) source file. You can add any number of the component to the system.

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CoreConnect Bus Architecture

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(Click on column header to sort)

Documents	Type	Date (mm/dd/yy)
Processor Local Bus (128-bit)	Specifications	05/02/07
IBM CoreConnect and CPU support cores	Product Brief	07/24/06
IBM CoreConnect Bus Cores	Product Brief	07/24/06
Device Control Register Bus 3.5 Architecture Specifications	Specifications	01/27/06
CoreConnect FAQ	FAQ	09/06/02
DCR Addressing with the CoreConnect DCR Master	Application Note	05/08/02
On-Chip Peripheral Bus	Specifications	04/01/01
CoreConnect Bus Architecture	Product Brief	09/01/99
CoreConnect Bus Architecture	White Paper	09/01/99
IBM On-Chip Bus Model Toolkits	Product Brief	06/01/98

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AMBA



arm
SYSTEM IP
AMBA

AMBA: The Standard for On-Chip Communication

AMBA is a freely available open standard for the connection and management of functional blocks in a system-on-chip. AMBA specifications are widely adopted as the standard for on-chip communication and provide a standard interface for IP re-use. This helps reduce the risks and costs of developing multi-processor designs with many controllers and peripherals. Different AMBA specifications outline the interfaces and protocols for use in applications across multiple market areas. Two key specifications include CHI and AXI. CHI defines the architecture for fully coherent, high-performance multi-core systems; AXI is used for a wide range of high-performance applications, including mobile computing, networking, automotive, and high-performance IoT.

Проектування комп'ютерних систем на рівні топології кристалу



The banner features a dark background with a glowing blue circuit board pattern. In the center, a black rectangular chip is highlighted with a white border. The text 'Electronic Design Automation' is prominently displayed in white, with the tagline 'Siemens EDA: Where electronic innovation meets tomorrow.' below it. A blue button with white text 'Read Our Latest Blogs' is positioned on the left side of the banner.

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Проектування комп'ютерних систем на рівні топології кристалу

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☐ Analog Design Environment:

- Cadence Spectre
- ADE L/XL/GXL

☐ Layout Design

- Virtuoso Layout Suite L/XL/GXL

☐ DFT

- TetraMax for ATPG

☐ Synthesis & Lint

- Spyglass

☐ STA

- Primetime-SI

☐ Formal Verification

- Conformal

☐ Place & Route

- Innovus

☐ Extraction

- Quantus

☐ Physical Verification

- Calibre LVS/DRC

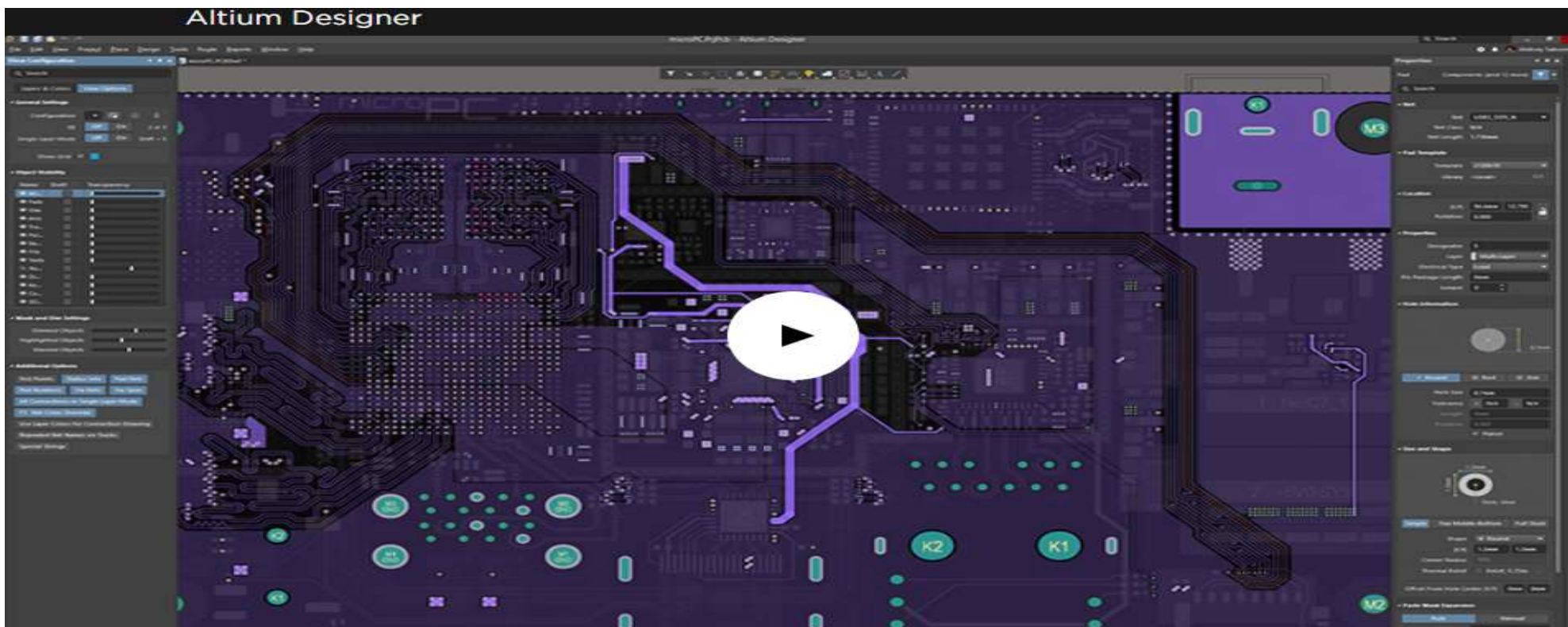
☐ Power & IR Drop Analysis

- Voltus

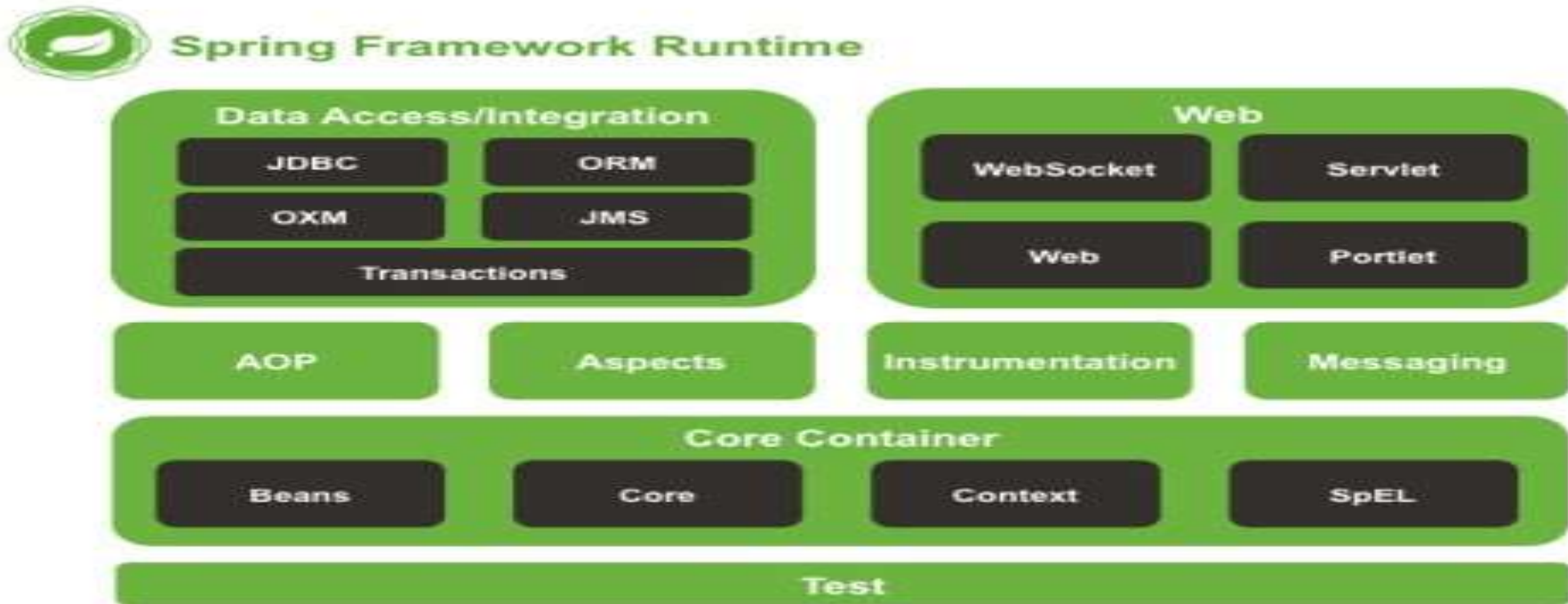
☐ Design Verification

- Incisive

Проектування комп'ютерних систем на рівні топології друкованої плати



Прикладне програмування комп'ютерних систем за допомогою високорівневих фреймворків



Прикладне програмування комп'ютерних систем за допомогою високорівневих фреймворків

