Автоматизоване проектування комп`ютерних та систем

Автоматизоване проектування комп`ютерних та систем

Частина 1. Тема №2. Основи систем автоматизованого проектування. (2 години)

Частина 1. Тема №3. Високорівневе проектування комп`ютерних систем і автоматичний синтез до нищих рівнів. (8 годин)

Частина 1. Тема №4. Проектування комп`ютерних систем на рівні топології кристалу. (10 годин)

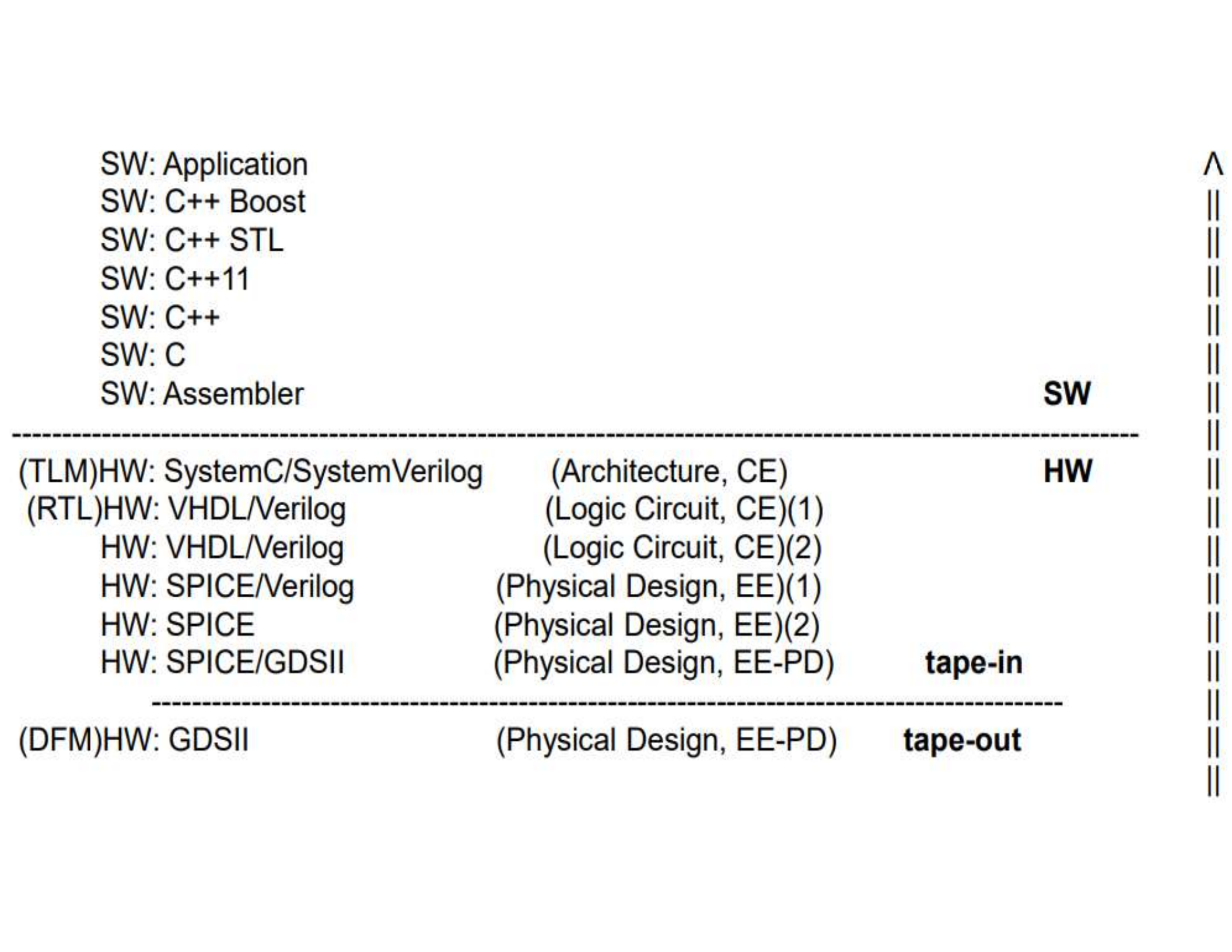
Частина 1. Тема №5. Проектування комп`ютерних систем на рівні топології друкованої плати. (2 години)

Частина 2. Тема №6. Прикладне програмування комп`ютерних систем за допомогою високорівневих фреймворків. (6 годин)

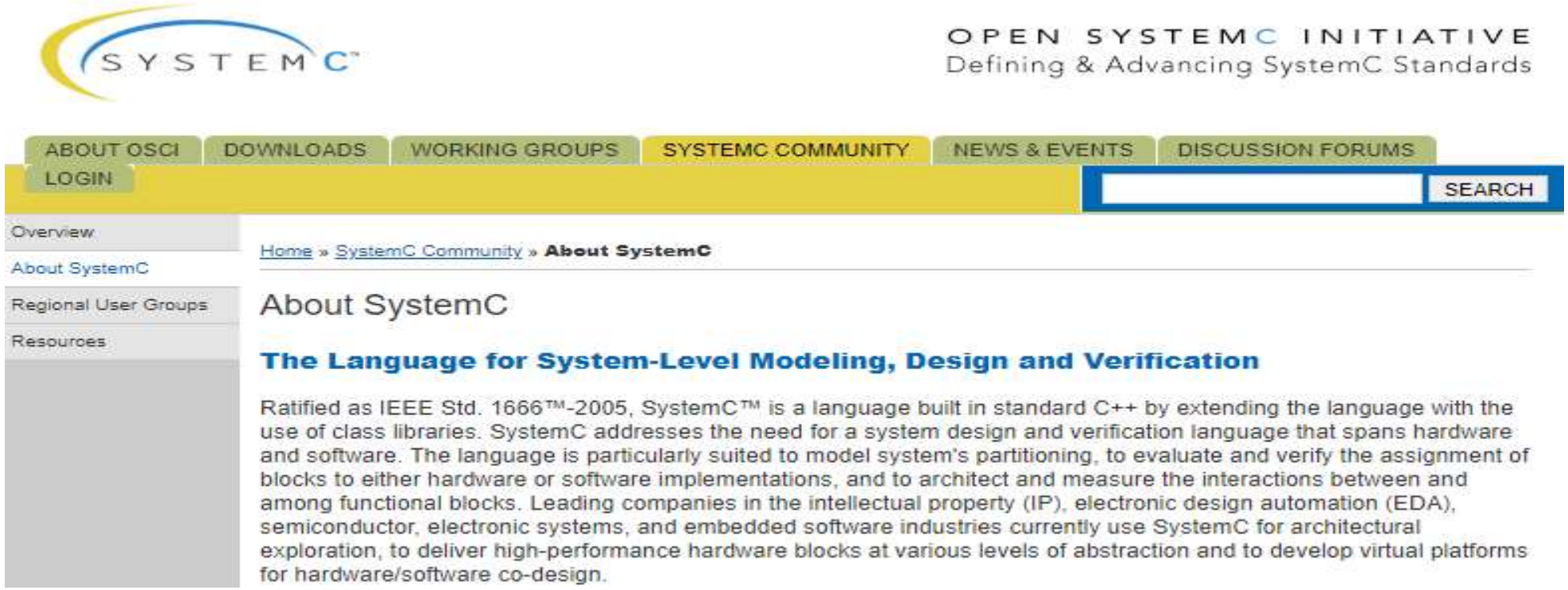
SW: Application
SW: C++ Boost
SW: C++ STL
SW: C++11
SW: C++
SW: C
SW: Assembler **SW**

(TLM)HW: SystemC/SystemVerilog (Architecture, CE) **HW**
(RTL)HW: VHDL/Verilog (Logic Circuit, CE)(1)
HW: VHDL/Verilog (Logic Circuit, CE)(2)
HW: SPICE/Verilog (Physical Design, EE)(1)
HW: SPICE (Physical Design, EE)(2)
HW: SPICE/GDSII (Physical Design, EE-PD) **tape-in**

(DFM)HW: GDSII (Physical Design, EE-PD) **tape-out**

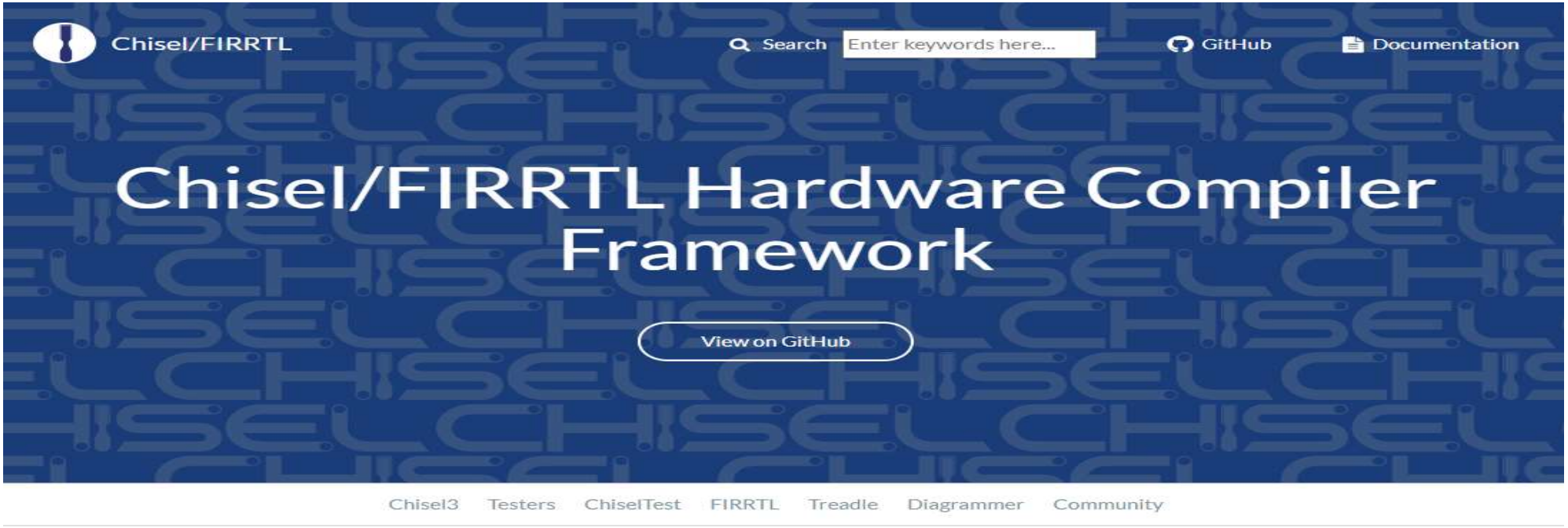


Високорівневе проектування комп`ютерних систем і автоматичний синтез до нищих рівнів.



Високорівневе проектування комп`ютерних систем і автоматичний синтез до нищих рівнів.

Високорівневе проектування комп`ютерних систем і автоматичний синтез до нищих рівнів.



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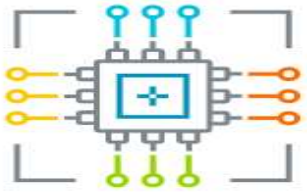
ARM



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System IP >

CoreLink, CoreSight, Coherent Mesh Network, AMBA and more

Graphics and Multimedia >

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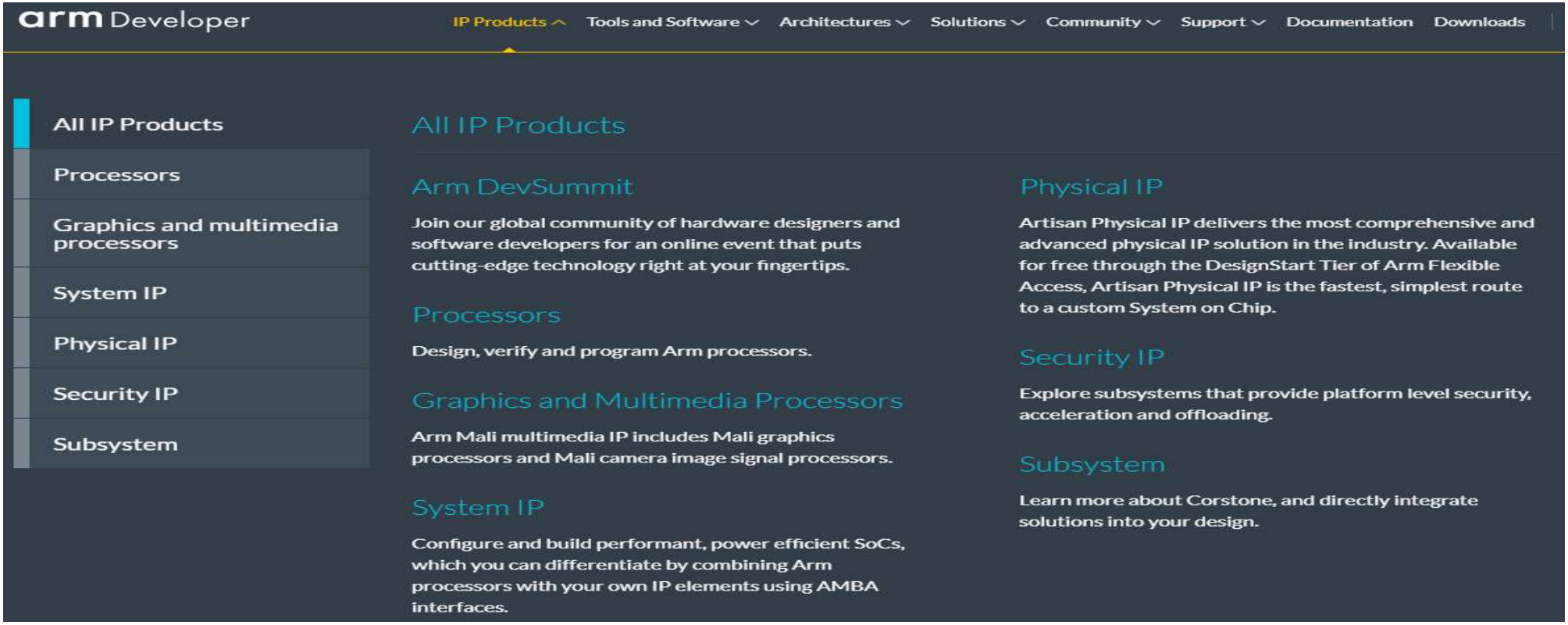
Keil RTX5, Allinea Studio, Compilers, Debuggers and more

ARM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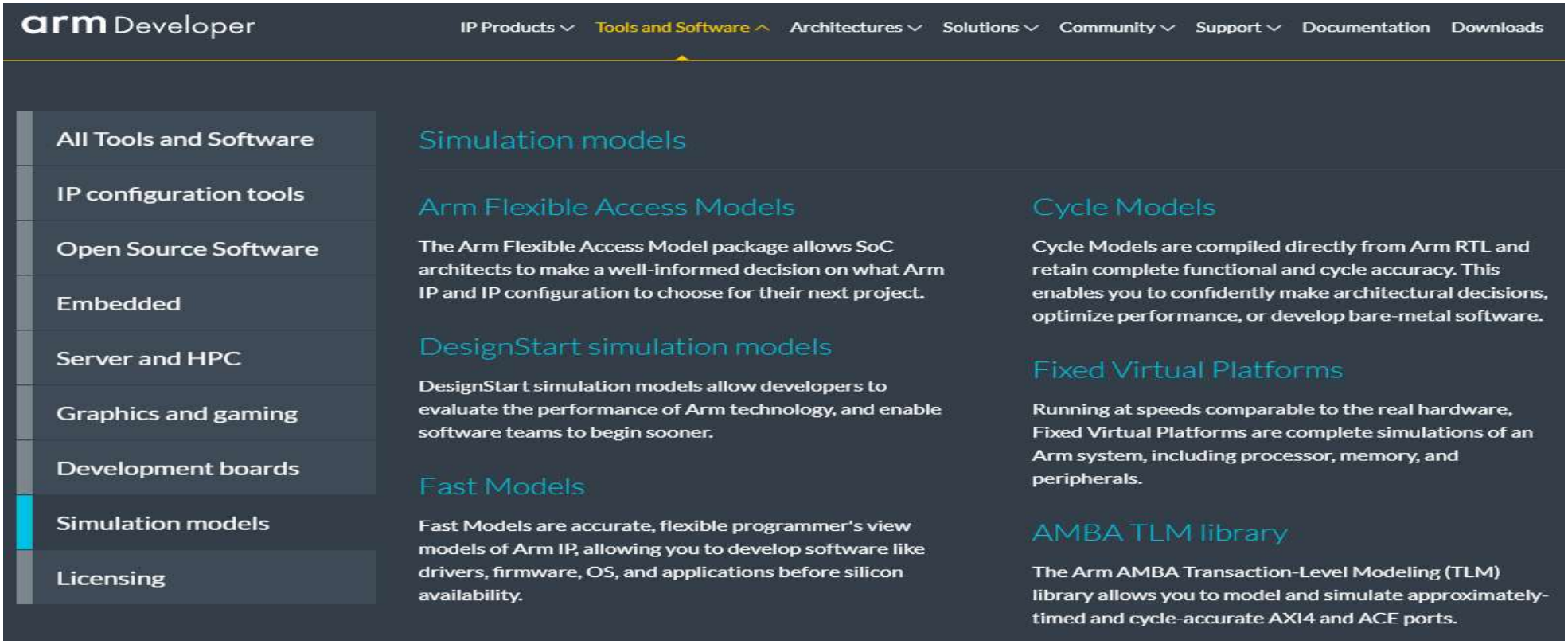
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The Arm Flexible Access Model package allows SoC architects to make a well-informed decision on what Arm IP and IP configuration to choose for their next project.
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DesignStart simulation models allow developers to evaluate the performance of Arm technology, and enable software teams to begin sooner.
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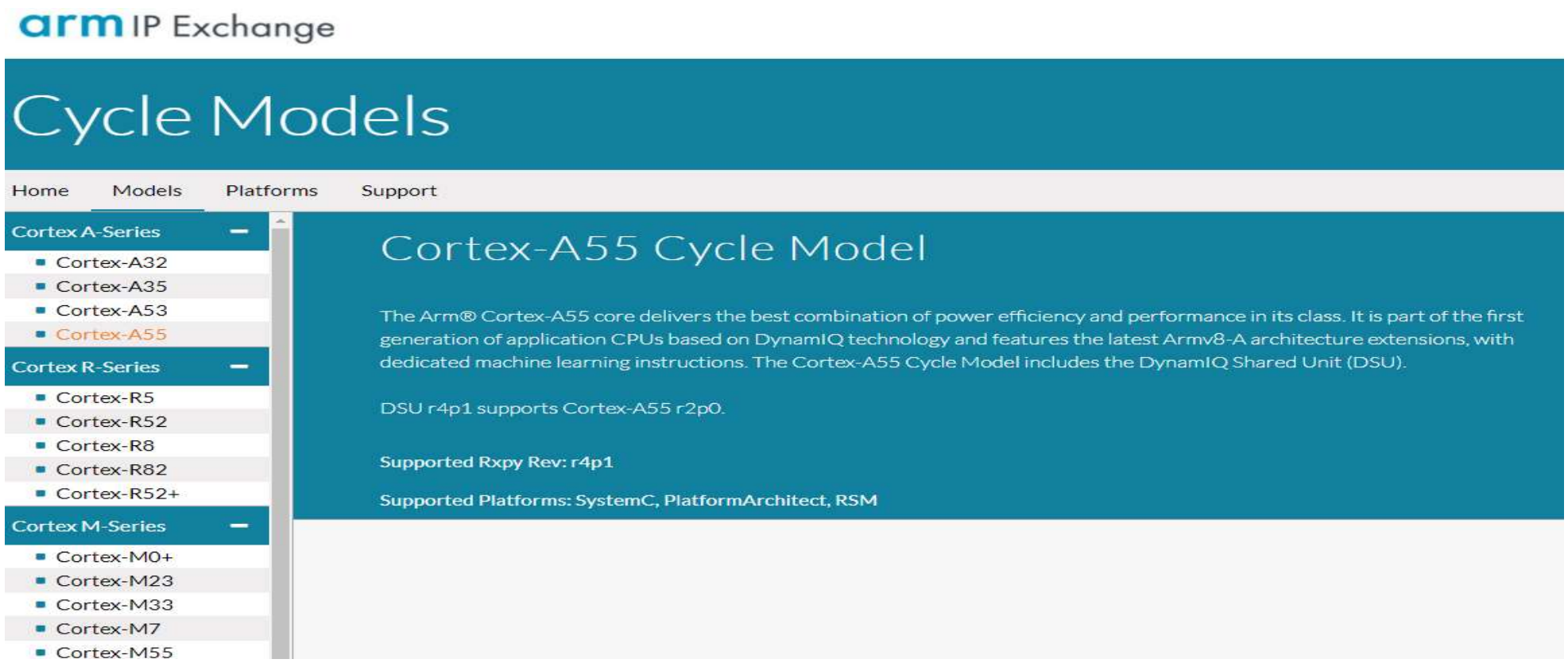
Running at speeds comparable to the real hardware, Fixed Virtual Platforms are complete simulations of an Arm system, including processor, memory, and peripherals.
AMBA TLM library
The Arm AMBA Transaction-Level Modeling (TLM) library allows you to model and simulate approximately-timed and cycle-accurate AXI4 and ACE ports.

ARM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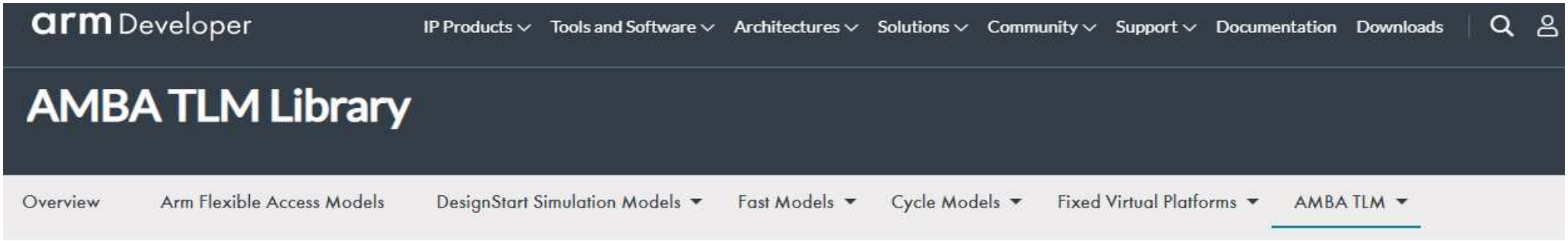
Cortex-A55 Cycle Model
The Arm® Cortex-A55 core delivers the best combination of power efficiency and performance in its class. It is part of the first generation of application CPUs based on DynamIQ technology and features the latest Armv8-A architecture extensions, with dedicated machine learning instructions. The Cortex-A55 Cycle Model includes the DynamIQ Shared Unit (DSU).
DSU r4p1 supports Cortex-A55 r2p0.
Supported Rxpy Rev: r4p1
Supported Platforms: SystemC, PlatformArchitect, RSM

ARM



Overview

The Arm AMBA Transaction-Level Modeling (TLM) library allows you to model and simulate approximately-timed (AT) and cycle-accurate (CA) AXI4 and ACE ports. This C++ library is provided as a pre-compiled binary library.

This library is intended for use with:

- Arm Cycle Models

- Custom AT and CA models used for virtual prototype development

- Third-party models that use supported AMBA interfaces

RISC-V

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RISC-V Exchange: Cores & SoCs

This page is a collection of available intellectual property (IP) cores and SoCs in the RISC-V ecosystem. This list is curated by the community – which includes you! Add cores, SoC platforms, and SoCs to the list by filing a pull request on the GitHub repository. If you have any questions about this process, contact us for help.

Please note that the Exchange can showcase available physical hardware on the Available Boards page.

Cores | SoC Platforms | SoCs

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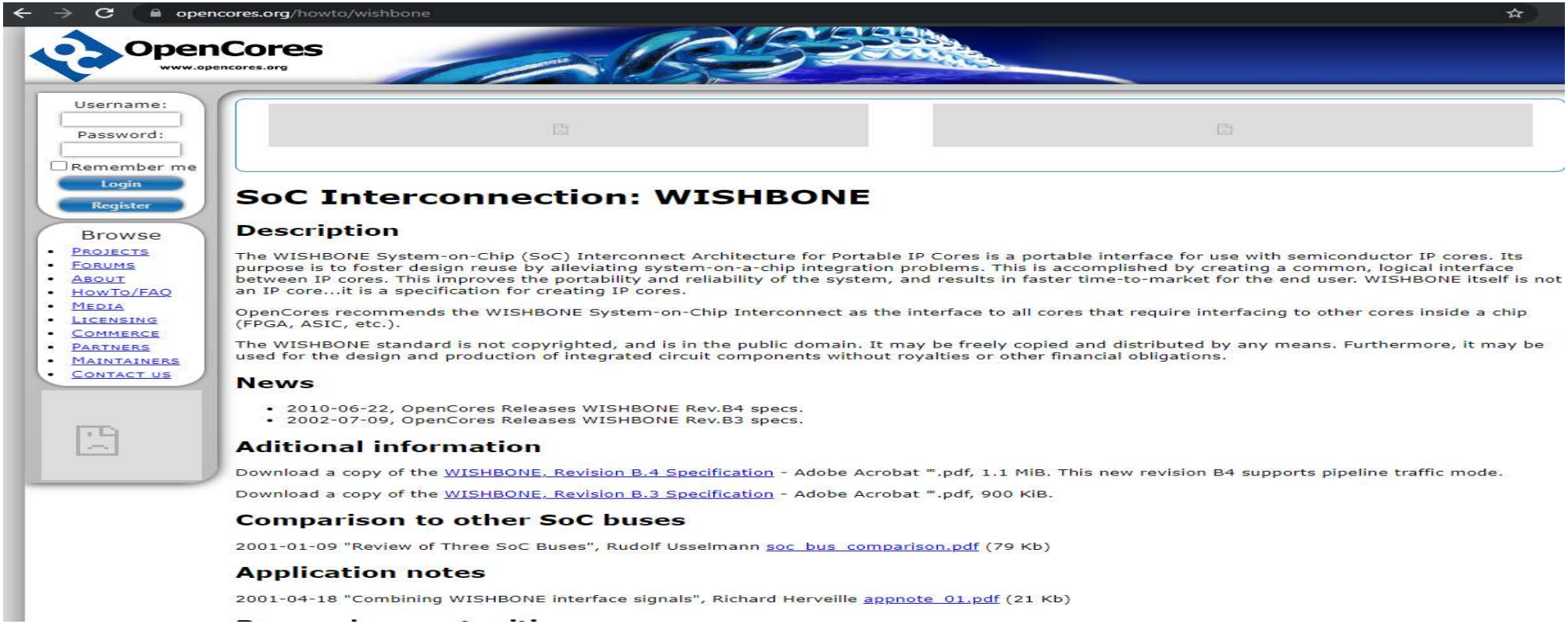
RV32IC_P5	IQonIC Works	Website	RV32	1.11	RV32I[M][N][A]C	SystemVerilog	IQonIC Works Commercial License

Wishbone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SoC Interconnection: WISHBONE
Description
The WISHBONE System-on-Chip (SoC) Interconnect Architecture for Portable IP Cores is a portable interface for use with semiconductor IP cores. Its purpose is to foster design reuse by alleviating system-on-a-chip integration problems. This is accomplished by creating a common, logical interface between IP cores. This improves the portability and reliability of the system, and results in faster time-to-market for the end user. WISHBONE itself is not an IP core...it is a specification for creating IP cores.
OpenCores recommends the WISHBONE System-on-Chip Interconnect as the interface to all cores that require interfacing to other cores inside a chip (FPGA, ASIC, etc.).
The WISHBONE standard is not copyrighted, and is in the public domain. It may be freely copied and distributed by any means. Furthermore, it may be used for the design and production of integrated circuit components without royalties or other financial obligations.
News
2010-06-22, OpenCores Releases WISHBONE Rev.B4 specs.
2002-07-09, OpenCores Releases WISHBONE Rev.B3 specs.
Aditional information
Download a copy of the WISHBONE, Revision B.4 Specification - Adobe Acrobat *.pdf, 1.1 MiB. This new revision B4 supports pipeline traffic mode.
Download a copy of the WISHBONE, Revision B.3 Specification - Adobe Acrobat *.pdf, 900 KiB.
Comparison to other SoC buses
2001-01-09 "Review of Three SoC Buses", Rudolf Usselmann soc_bus_comparison.pdf (79 Kb)
Application notes
2001-04-18 "Combining WISHBONE interface signals", Richard Herveille appnote_01.pdf (21 Kb)

Wishbone

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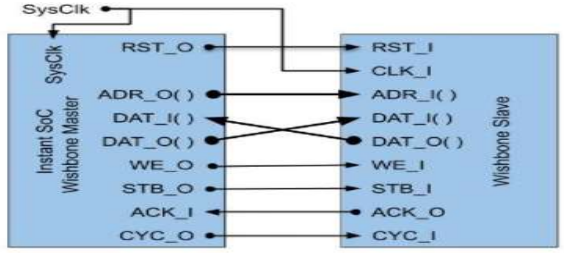
WISHBONE

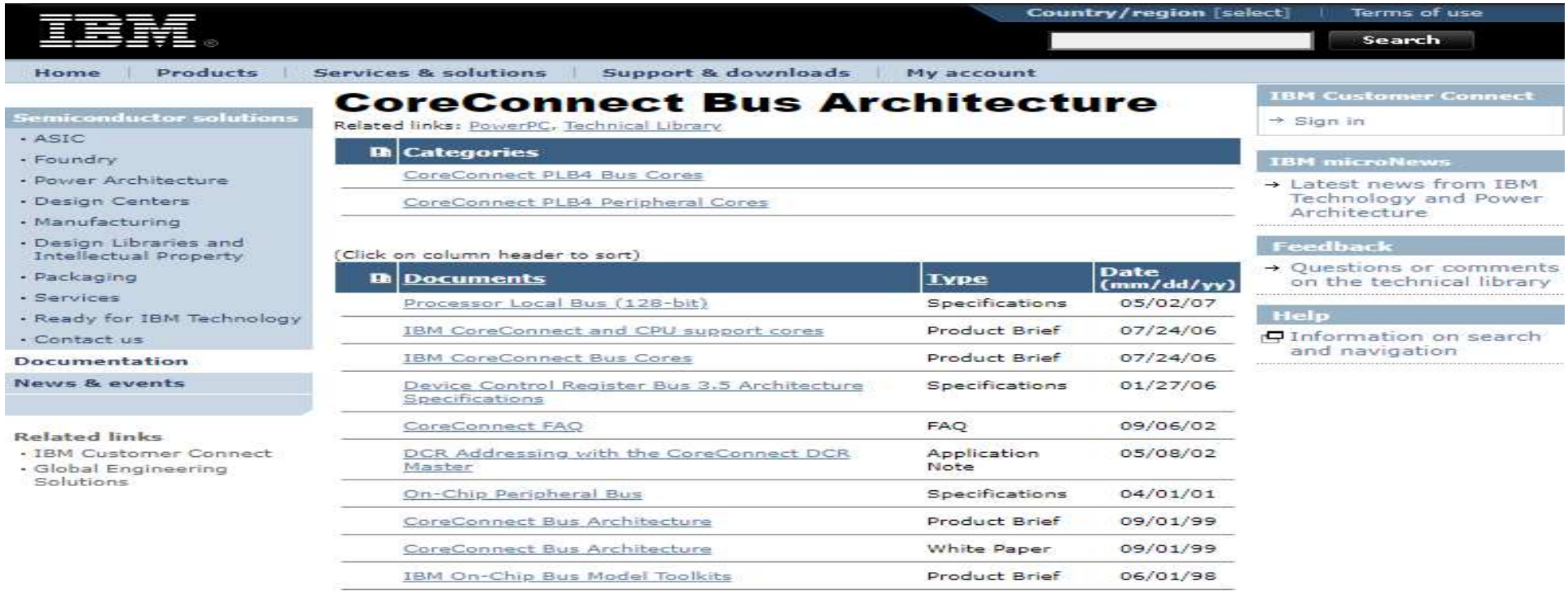
Wishbone is an open source standard bus that connects slave peripherals to a master CPU. Instant SoC V1.2 supports Wishbone and you can easily add your own VHDL or Verilog peripherals to the Instant SoC RISC-V system. Instant SoC supports the B4 version of Wishbone.



Wishbone Bus

To add a Wishbone component you simply creates a FC_Wishbone object in C++ with a file path to the component and Instant SoC adds the component and maps all Wishbone bus signals to the system. The file could be a Verilog (*.v) or VHDL (*.vhd) source file. You can add any number of the component to the system

CoreConnect



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IBM CoreConnect Bus Cores	Product Brief	07/24/06
Device Control Register Bus 3.5 Architecture Specifications	Specifications	01/27/06
CoreConnect FAQ	FAQ	09/06/02
DCR Addressing with the CoreConnect DCR Master	Application Note	05/08/02
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AMBA: The Standard for On-Chip Communication
AMBA is a freely available open standard for the connection and management of functional blocks in a system-on-chip. AMBA specifications are widely adopted as the standard for on-chip communication and provide a standard interface for IP re-use. This helps reduce the risks and costs of developing multi-processor designs with many controllers and peripherals. Different AMBA specifications outline the interfaces and protocols for use in applications across multiple market areas. Two key specifications include CHI and AXI. CHI defines the architecture for fully coherent, high-performance multi-core systems; AXI is used for a wide range of high-performance applications, including mobile computing, networking, automotive, and high-performance IoT.

Проектування комп`ютерних систем на рівні топології кристалу

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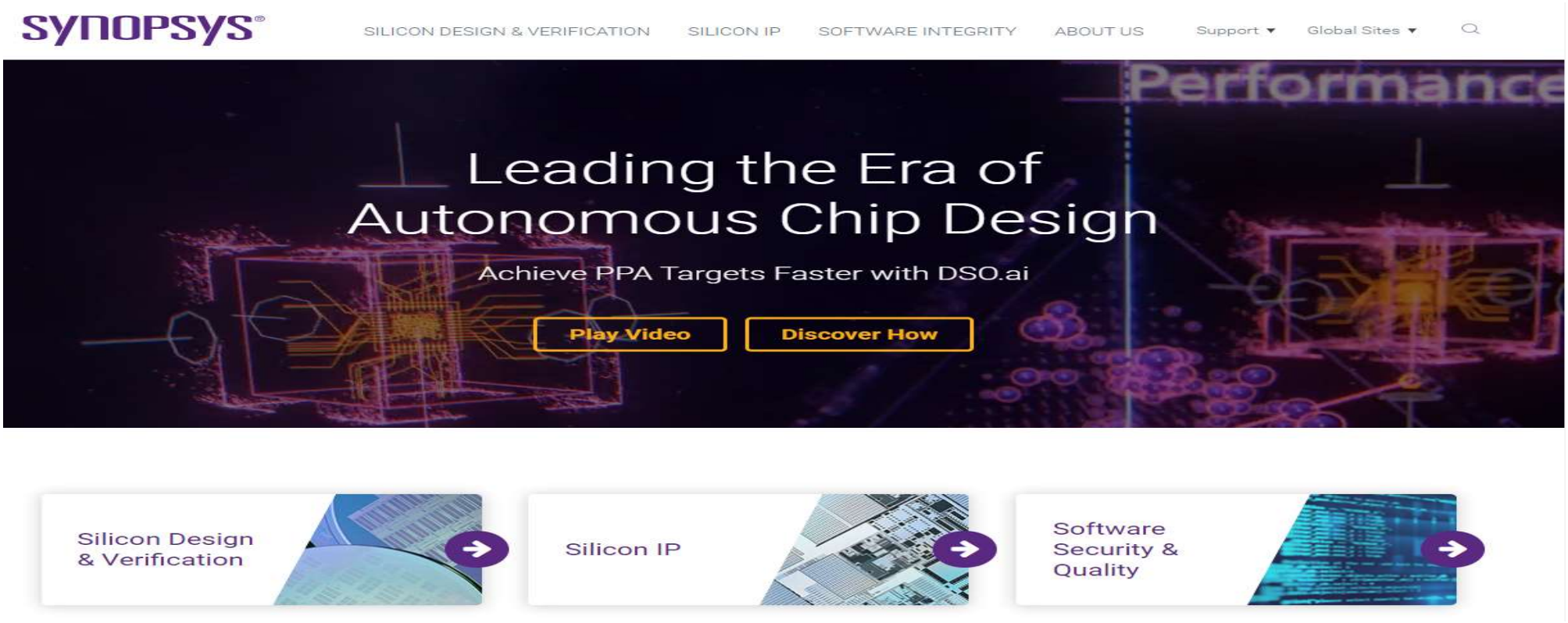
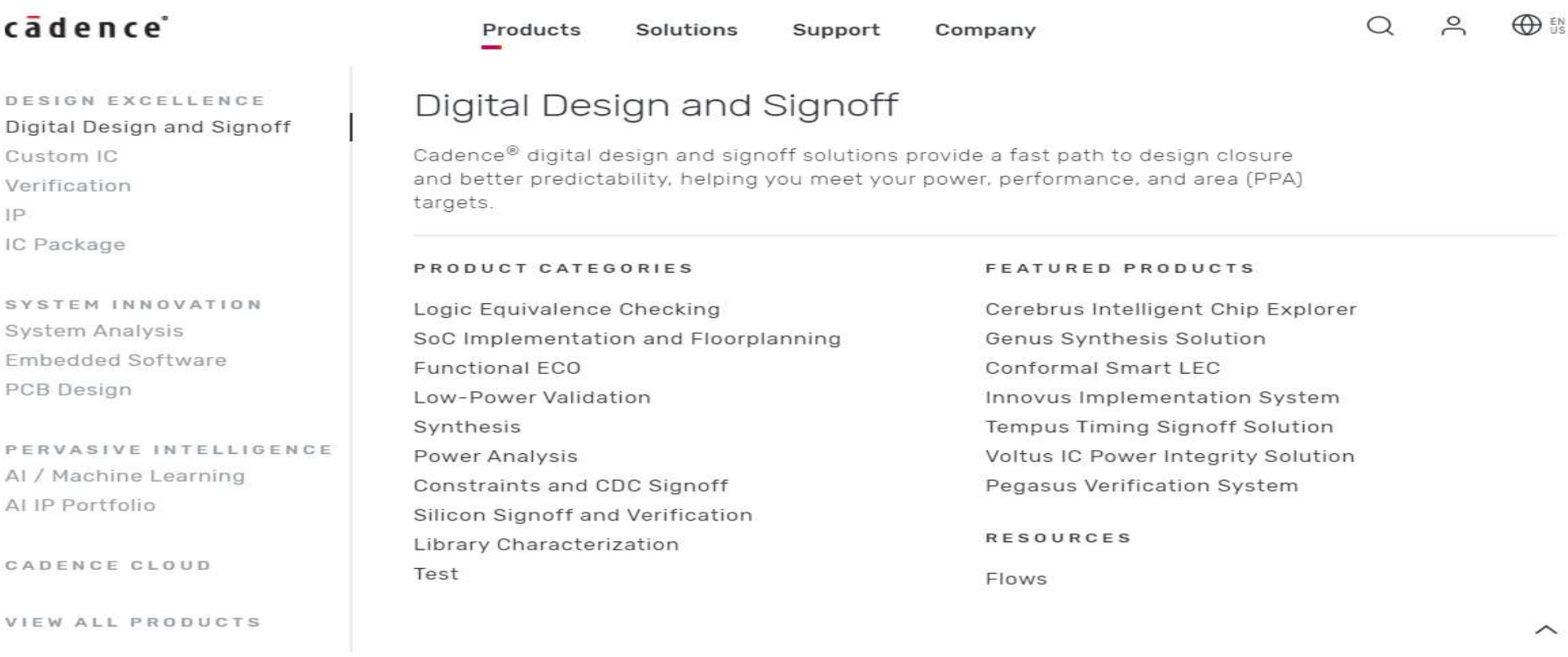
Проектування комп`ютерних систем на рівні топології кристалу



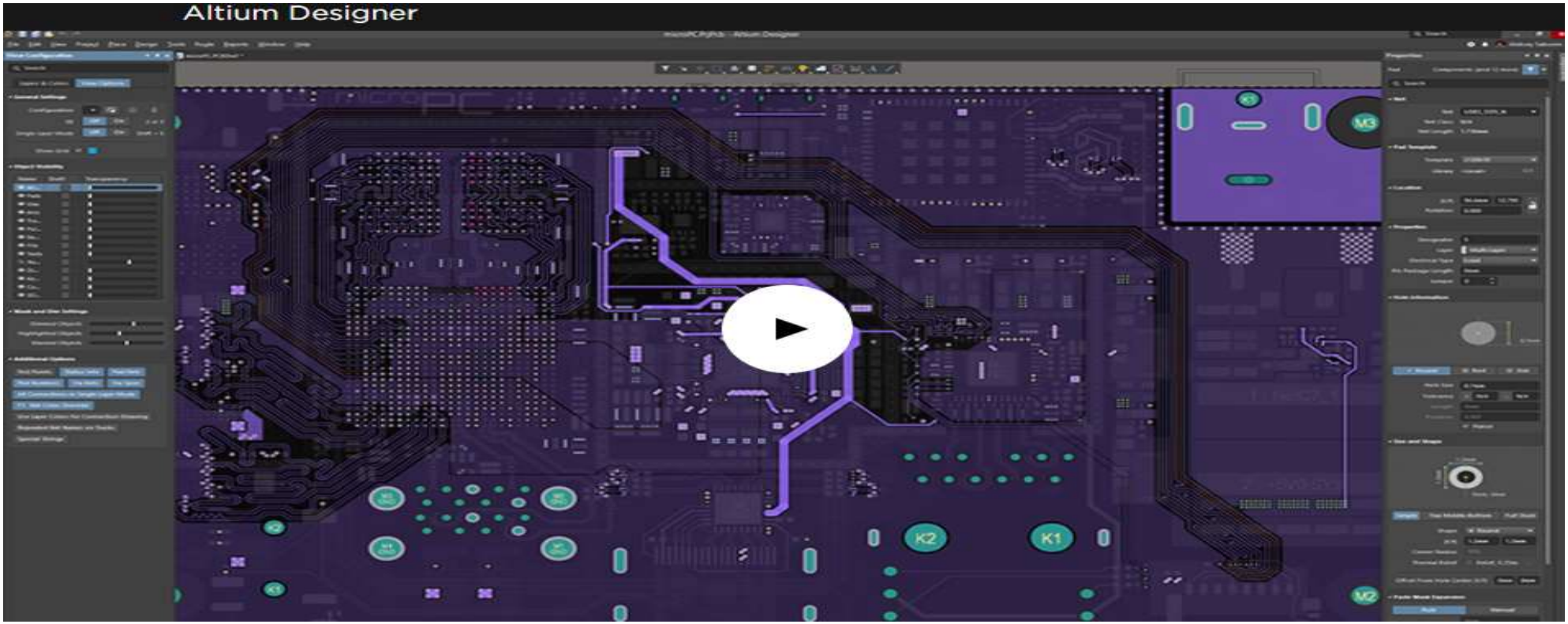
Проектування комп`ютерних систем на рівні топології кристалу



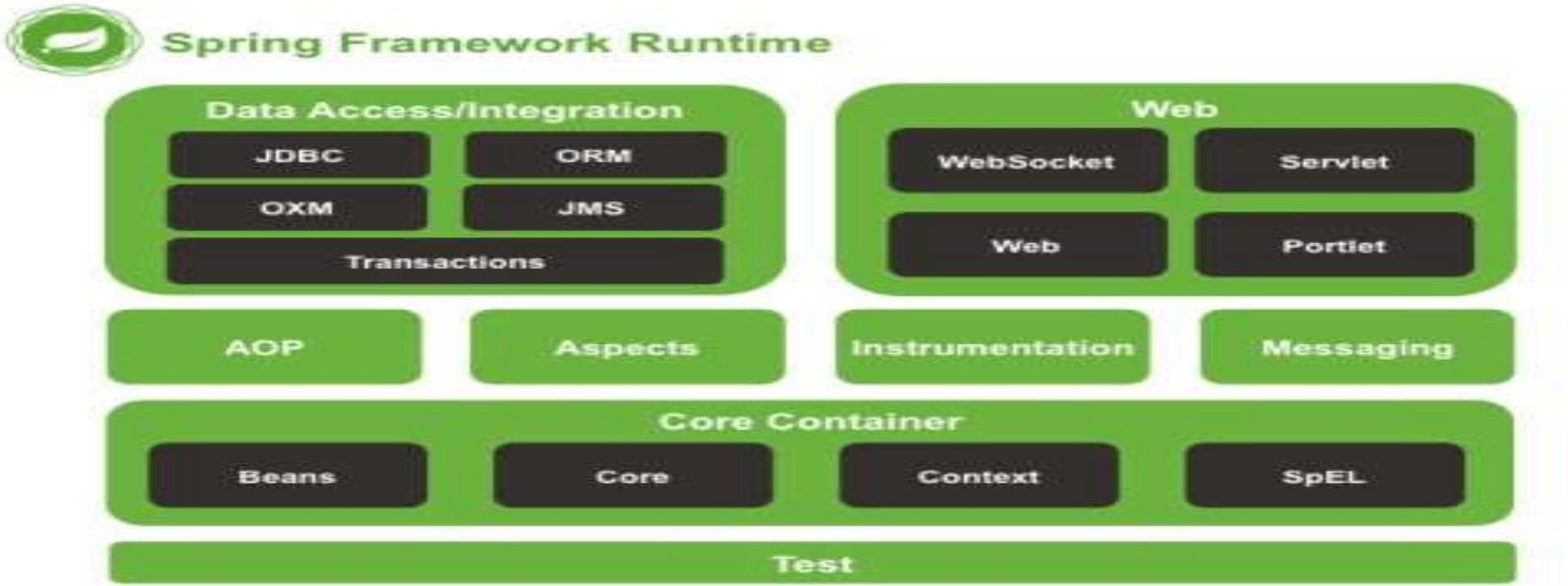
Проектування комп`ютерних систем на рівні топології кристалу

- Analog Design Environment:
  - Cadence Spectre
  - ADE L/XL/GXL
- Layout Design
  - Virtuoso Layout Suite L/XL/GXL
- DFT
  - TetraMax for ATPG
- Synthesis & Lint
  - Spyglass
- STA
  - Primetime-SI
- Formal Verification
  - Conformal
- Place & Route
  - Innovus
- Extraction
  - Quantus
- Physical Verification
  - Calibre LVS/DRC
- Power & IR Drop Analysis
  - Voltus
- Design Verification
  - Incisive

Проектування комп`ютерних систем на рівні топології друкованої плати



Прикладне програмування комп`ютерних систем за допомогою високорівневих фреймворків



Прикладне програмування комп`ютерних систем за допомогою високорівневих фреймворків