

Bachelor Thesis

Benchmark of RISC-V in BTOR2

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Declaration

I hereby declare that I am the sole author and composer of my thesis and that no other sources or learning aids, other than those listed, have been used. Furthermore, I declare that I have acknowledged the work of others by providing detailed references of said work.

I hereby also declare that my Thesis has not been prepared for another examination or assignment, either wholly or excerpts thereof.

Place, Date

Signature

Abstract

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1 Motivation

This is a template for an undergraduate or master's thesis. The first sections are concerned with the template itself. If this is your first thesis, consider reading.

2 RISC-V

2.1 Overview

2.2 The RISC-V ISA

2.3 Simulation of RISC-V

2.3.1 Saving the State of a RISC-V Processor

3 BTOR2

3.1 Model Checking

3.2 The BTOR2 Language

3.3 The BTOR2 Witness

4 Transforming RISC-V to BTOR2

4.1 The Concept

4.2 Encoding

4.2.1 Constants

4.2.2 State Representation

4.2.3 Initialization

4.2.4 Computing values

Opcode

funct3 & funct7

Registers

Immediate

4.2.5 Command Detection

4.2.6 Next-State-Logic

4.2.7 Constraints

4.3 Testing for Correctness

4.3.1 State Fuzzer

4.3.2 Automated Logging

4.4 Functional vs Relational Next-State-Logic

5 Benchmarks

5.1 MultiAdd in Functional and Relational Next-State-Logic

5.2 Memory Operations

5.3 Results

Bibliography

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