CHAPTERS	REV	REV	REV	ST NT	DPP	WT	PYQ	PYQ	TWT	SWT
COMPUTER NETWORKS										
IPV4 Addressing										
Error Control										
Flow Control										
IPV4 Header & Fragmentation										
TCP & UDP										
Medium Access Control										
Routing Protocols										
Switching										
Application Layer Protocols										
IP Support protocol										
OSI & TCP/Stack Protocol										
		OPE	RATIN	G SYS	TEMS		<u> </u>			
Introduction & Background										
Process Management										
CPU Scheduling										
Process Synchronization										
DeadLock										
Memory Management										
File System & Device										
Management System Calls & Threads										
System cans & Timeaus				RAMN	AING					
Data Turana ( Organistana	l	C - I	אטטו	KAIVIIV	IIING		l	l		
Data Types & Operators Control Flow Statements										
Functions & Storage Classes										
Arrays & Pointers										
Strings										
Structures & Union										
Miscellaneous Topics										
DATA STRUCTURES										
Introduction										
Arrays										
Linked List										
Stack & Queues										
Trees										
Graphs										
Hashing										
DIGITAL LOGIC										
Logic Gates										
Minimization										
Combinational Circuit										
Sequential Circuit										
Number System										

CHAPTERS	REV	REV	REV	ST NT	DPP	WT	PYQ	PYQ	TWT	SWT
THEORY OF COMPUTATION										
Finite Automata										
Push Down Automata										
Turning Machine Recursively										
Enumerable										
Decidability										
Decidability		CO	MDII F	R DES	SIGN					
Lexical & Syntax Analysis				IN DES	NON					
Syntax Directed Translation										
Intermediate Code & Code										
Optimization										
Optimization			AI GOI	RITHN	15					
Analysis Of Algorithms		<i>F</i>	TEGOI	TITIIV	13					
Design Strategies										
Greedy Method										
Dynamic Programming										
Graph Algorithms										
Heap Algorithms										
Backtracking & Branch -										
Bound										
	DATA	BASE	MANA	AGEM	ENT S	YSTEN	1			
FD's and Normalisation										
Transaction and Concurrency										
Control										
ER Model										
Query Language										
File Organisation & Indexing										
COMF	PUTER	ORG	ANISA	TION	& AR	CHITE	CTURE			
Introduction Of COA										
Machine Instruction and										
Addressing Modes										
Floating Point Representation										
ALU and Control Unit										
Instruction And Pipelining										
Cache Memory										
Secondary Memory & IO										
Interface										
DISCRETE MATHEMATICS										
Graph Theory										
Mathematical Logic										
Set Theory										
Combinatorics										
ENGINEERING MATHEMATICS										
Linear Algebra										
Calculus										
Probability & Statistics			I							

## General Aptitude Section

CHAPTERS	CLASS PROBLEMS	DPPS	WEEKLY TEST	CAT LV 1	CAT LV 2	MOCK TEST
Averages						
Percentages						
Simple & Compound Intrest						
Profit and Loss						
Mixtures & Alligations						
Ratio and Propotion						
Counting Theory						
Time and Work						
Pipes and Cisterns						
Speed, Distance and Time						
Boats, Trains, Races						
Mensuration 2D, 3D						
Geometry						
Data Interpretation						
Probability						
Set Theory						
Permutation & Combinations						
Calandana						
Calenders Clocks						
Number System						
Number System						
Blood Relations						
Coding & Decoding						
Directions						
Arrangements and Rankings						
Cubes & Dices						
Venn Digrams						
Paper Folding						
Image Formations						