Q.1) Max Marks: 1

Assuming a page size of 1 KB and that each page table entry (PTE) takes 4 bytes, how many levels of page tables would be required to map a 34-bit address if every page table fits into a single page_____________

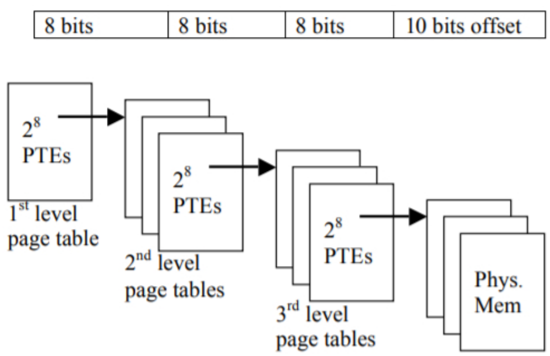
Correct Answer

Solution: (3)

Answer: 3

Solution:

Since a page is 210 bytes (1 KB) and each PTE is 22 bytes (4 bytes), a 1-page page table contains 256 or 28 PTEs (210 /22 =28). Each entry points to a page that is 210 bytes (1 KB). With one level of page tables we can address a total of 28 x 210 = 218 bytes). Adding another level yields another 28 pages of page tables, addressing a total of 28 x 28 x 210 = 226 bytes. Finally, adding a third level 28 pages of page tables, addressing a total of 28 x 28 x 28 x 210 = 234 bytes. So, we need 3 levels.



Q.2) Max Marks: 1

A computer has 4 page frames. The time of loading, time of last access and the R and M bits for each page are as shown below (the times are in clock ticks):

page	loaded	Last ref	R	M
0	130	280	0	0
1	235	270	1	0
2	140	282	1	1
3	170	281	1	1

Which page will LRU replace if it wants to load page5 in to the memory?

A 0

B 1 Correct Option

Solution: (B)

Solution:

Page	Loaded	Last ref	R	M
0	130	280	0	0
1	235	270	1	0
2	140	282	1	1
3	170	281	1	1

In LRU replacement algorithm we replace the page which is not referred from long back. From the given information above

Page 0 → Last Ref (280)

Page 1 → Last Ref (270)

Page 2 → Last Ref (282)

Page 3 → Last Ref (281)

→ Page 1 is not referred from long back.

C 2

D 3

Q.3)

Max Marks: 1

Assume that you have a page-reference string for a process with m frames (initially all empty). The page-reference string has length p; n distinct page numbers occur in it. Then the lower bound and upper bound on the number of page faults for any page replacement algorithms respectively.

A m,p

B n,p

Correct Option

Solution: (B)

Answer: B

Explanation:

lower bound on the number of page faults: n when all pages in reference string must page in (given distinct page numbers)

upper bound on the number of page faults: p when every page in ref string causes a fault

C m,n

D None of these

Q.4)

Max Marks: 1

Consider the following statements

a. FIFO with N+1 pages of memory always performs better than FIFO with N pages of memory.

b. Paging approaches suffer from internal fragmentation, which decreases as the size of a page decreases

c. TLBs are more beneficial with multi-level page tables than with linear (single-level) page tables.

Which of the following are not TRUE?

A **Only a**

Correct Option

Solution: (A)

Answer: I

Solution:

a. False; FIFO with N+1 pages can even perform worse(belady's anomaly).

b. True, because the cost of walking a multi-level page table is higher than walking a single level (i.e., more memory accesses are needed)

c. True; internal fragmentation (the amount of wasted space) decreases if smaller units of allocation are used.

B **Only b & c**

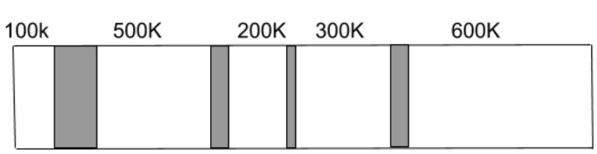
C **a, b & c**

D **Only b**

Q.5)

Max Marks: 1

Given memory holes (i.e., unused memory blocks) of 100K, 500K, 200K, 300K and 600K (in address order) as shown below, If each of the first-fit, next-fit, best-fit and worst-fit algorithms allocate memory requests for 290K, 420K, 110K and 350K (in this order) what is the ascending order of the remaining space left in 600K block(algorithm wise) if implemented. The shaded areas are used/allocated regions and are not available.



Note: Assume variable partitioning.

A **First fit < Next fit < Best fit < Worst fit**

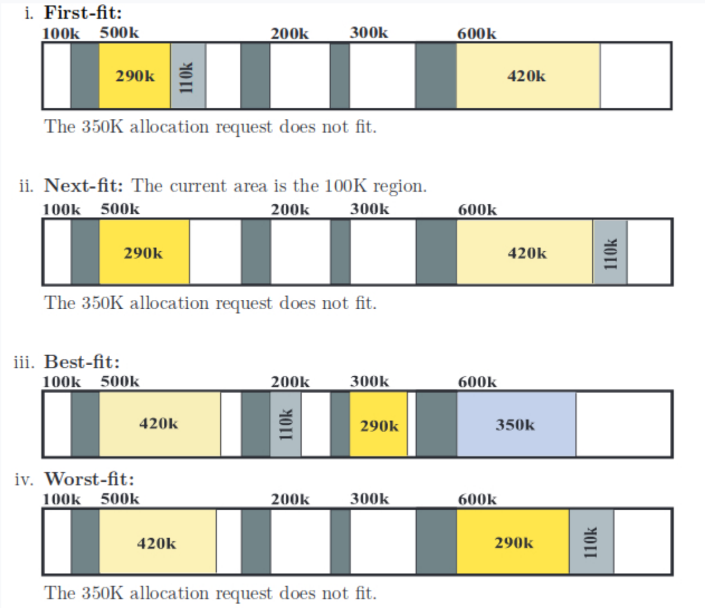
B Next fit < Worst fit < First fit < Best fit

C Best fit < First fit < Worst fit < Next fit

D Next fit < First fit < Worst fit < Best Fit **Correct Option**

Solution: (D)
Answer : D

Explanation:
NF < FF < WF < BF
As, 70K < 180K < 200K < 250K



Q.6) **Max Marks: 1**

A paging system uses 16-bit address and each page can hold 4K addresses. The following shows the pagetables of two running processes,Process 1 and Process 2. Translate the logical addresses in thetable below to their corresponding physical addresses, and fill the table entries with your answers.

Process 1

0	3
1	7
2	1
3	5

Process 2

0	2
1	0
2	6
3	4

Process	Address	Page	Physical Address
process1	11,034	a1	b1
process2	12,345	a2	b2

A a1 = 7, b1 = 16,441 & a2 = 4, b2 = 6931

B a1 = 3, b1 = 6938 & a2 = 2, b2 = 16,441

C a1 = 2, b1 = 16442 & a2 = 3, b2 = 6931

D None of these **Correct Option**

Solution: (D)

Answer: IV
Solution:
Consider the logical address 11034 generated by process 1. Since page size is 4K = 4096, logical address 11034 is in page 2 = 11034/4096, and the offset is 11034 - 2× 4096 = 2842. From process 1's page table, page 2 is in page frame 1, and, hence, the corresponding physical address is 1× 4096 + 2842 = 6938. The second logical address 12345 is translated the same way with process 2's page table.

Process	*Address*	*Page #*	*Offset*	*Physical Address*
Process 1	11,034	2	2842	6,938

Process 2	12,345	3	57	16,441

Q.7)

Max Marks: 1

Consider a machine with a physical memory of 8 GB, a page size of 8 KB, and a page table entry size of 4 bytes. Without a cache or TLB, how many memory operations are required to read or write a single 32-bit word would be required for 46-bit virtual address space if every page table fits into a single page___________

Correct Answer

Solution: (4)

Answer: 4

Solution:

Since each PTE is 4 bytes and each page contains 8KB, then a one-page page table would point to 2048 or 211 pages, addressing a total of 211 * 213 = 224 bytes. Continuing this process:

Depth	*Address Space*
1	2^{24} *bytes*
2	2^{35}*bytes*
3	2^{46}*bytes*

Without extra hardware, performing a memory operation takes 4 actual memory operations: 3 page table lookups in addition to the actual memory operation.

Q.8)

Max Marks: 1

Consider the segment table: Find the physical address for the following logical address <1,219>

Segment	base	length
0	1000	110
1	1800	90
2	2000	900
3	3200	68
4	4300	980

A 2019

B 319

C 1119

D None of these — Correct Option

Solution: (D)

Answer: IV

Solution:

It's an Illegal address since the size of the segment1 is 90 and its logical address is referring 219.

Q.9)

Max Marks: 1

If page fault service time is 50ms and memory access time is 100ns, then what will be EMAT, if the probability of page fault is p ?

A 500000+100p ns

B 100+500000p ns

C 10^−7 + 5p×10^−2 seconds

D 10^−7 + 49.9p×10^−3 seconds — Correct Option

Solution: (D)

Answer : 10^−7 + 5p×10^−2 seconds

Explanation:

EMAT = P(Page Fault Service Time) + (1-p)(100)ns

= p(50 * 10^-3) ns + (1 - p) 100 ns

= p(50 * 10^-3 * 10^-4 * 10^4) + 10^-7 - 10^-7 p

= p(500000 * 10^-7 - 10^-7) + 10^-7

= 10^-7 * p (500000 - 1) + 10^-7

= 10^−7 + 49.9p * 10^−3 seconds.

Q.10)

Max Marks: 1

In a 32-bit machine we subdivide the virtual address into 4 segments as follows:

8-bit	8-bit	6-bit	10-bit

We use a 3-level page table, such that the first 8 bits are for the first level and so on.

What is the size of the page tables for a process that has 256KB of memory starting at address 0? Assume each page-table entry is 4 bytes.__________(in bytes)

Correct Answer

Solution: (3072)

Answer: 3072

Solution:

Actual page table size: (256 + 256 + 4 * 64) * 4Bytes = 3072 Bytes

Q.11)

Max Marks: 2

Given the following stream of page references by an application, calculate the number of page faults the application would incur with the following page replacement algorithms such as FIFO, LRU and OPT. Assume that all pages are initially free and has 3 physical pages.
Reference Stream: A B C D A B E A B C D E B A B
Which of the following holds TRUE?

A **LRU > FIFO > OPT** — Correct Option

Solution: (A)

Solution:

FIFO: 11

11 page faults

Refrence stream:	A	B	C	D	A	B	E	A	B	C	D	E	B	A	B
oldest page	A	A	A	B	C	D	A	A	A	B	E	E	C	D	D
		B	B	C	D	A	B	B	B	E	C	C	D	B	B
Newest page			C	D	A	B	E	E	E	C	D	D	B	A	A
page fault	√	√	√	√	√	√	√			√	√		√	√	

LRU:12

12 page faults

Refrence stream:	A	B	C	D	A	B	E	A	B	C	D	E	B	A	B
least recently used	A	A	A	B	C	D	A	B	E	A	B	C	D	E	E
		B	B	C	D	A	B	E	A	B	C	D	E	B	A
most recently page			C	D	A	B	E	A	B	C	D	E	B	A	B
page fault	√	√	√	√	√	√	√			√	√	√	√	√	

OPT: 8

8 page faults

On a page fault, replace the page used furthest in the future.

Refrence stream:	A	B	C	D	A	B	E	A	B	C	D	E	B	A	B
	A	B	C	D	D	D	E	E	E	E	E	E	E	E	E
		A	B	B	B	B	B	B	B	B	B	B	B	B	B
			A	A	A	A	A	A	A	C	D	D	D	A	A
page fault	√	√	√	√			√			√	√			√	

B **OPT < LRU < FIFO**

C **FIFO > LRU > OPT**

D **LRU > OPT > FIFO**

Q.12)

Max Marks: 2

A certain computer system has the physical address space as 2^{16} bytes . And consists of 2byte page table entries . Assume that each page table entry contains (beside other information) 1 bit for valid , 3 bit for protection and 1 bit for dirty . How many bits are available in page table entry for storing the aging information for the page ?

Assume that the page size is 512 bytes ?

A 3

B 4 Correct Option

Solution: (B)
Answer: II
Solution:

Since physical address space = 2^16

page size = frame size = 512 bytes

So number of frames = 2^16/2^9= 2^7

Number of bits used to address frame = $\log_2(2^7)$= 7 bits

since page table entry is 2 bytes = 16 bits

so now page table entry bit = no of bit used for farme number + 1 valid + 3 bit for protection + 1 dirty bit + Required Aging information

so 16 = 7+1+3+1+x

x=4

C 5

D 6

Q.13) Max Marks: 2

Assume that amount of memory on a system is inversely proportional to the page fault rate. Each time page fault rate doubles, when memory is reduced by half. Currently the system has 128 MB of memory. The main memory access time is 1 μsec and page fault service time is 1 msec. The overall effective access time is 112 μsec. If the memory is decreased to 32 MB then the overall effective access time is ________(μsec) (Round of upto two decimal places)

Correct Answer

Solution: (440.56)
Answer:440.56
Explanation:
Calculated page fault rate from data,
112= p(1 ms)+ (1-p)(1microsecond)

P=0.111. Now memory is divided by 4 and page fault rate is inversely proportional so page fault rate multiplied by 4 gives 0.44

Now effective time is
0.444(1000)+ 0.56(1)= 440.56 microsecond

Q.14) Max Marks: 2

Consider a system using 2 level paging applicable page table is divided into 2k pages each size 4kB. If PAS is 64 MB which is divided into 16K frames . PTE size is 2B in both the levels calculate the length of PA, LA and number of entry at second level?

A 26, 34,2^{12}

B 29, 34, 2^{12}

C 26, 32, 2^{11}

D 26, 34, 2^{11} Correct Option

Solution: (D)
Answer:D
Explanation:
PA = bits to address 64 MB = 26 bits
LA = bits to index into outer table + bits to index into 1 inner page table + bits to index page size
= bits to select one of 2^{11} entries + bits to select one of 2^{11} entries + bits to index 4 KB
= 11 + 11 + 12 = 34 bits

# of entries in 1 page table at second level = pagesize÷entrysize
= 4KB ÷ 2B = 2^{11} entries

Q.15)

Max Marks: 2

Consider a processor has virtual address 52 bits, the physical address is 32 bits and the page size is 16KB. Each individual table at any level of the page table occupies a single page of physical memory. Using multi level paging, how many entries are there in each individual page table page. Consider page table entry requires additional 14 bits for the special purpose?

A <2, 12, 12, 12> — Correct Option

Solution: (A)

Answer: I

Solution:

virtual address = 52 bits

page size = 16kB = 14 bits

No. of pages = 2^{38}

hence sum of all bits (in ans) = 38

also for frames ,

No. of frames = 32-14=2^{18}

page table entry = 18+ (additional) 14 bits = 32 bits = 2^{2}B

in each page = $2^{14}/2^{2}=2^{12}$

i.e. at max there can be 2^{12} pages in any page table .

hence, ans is option I

< 2, 12, 12, 12 >

B <10,14,14,14>

C <4,14,14,14>

D <10,12,14,14>

close