

All    Correct Answers    Wrong Answers    Not Attempted Questions

Q.1)

The minimum size of the memory required to implement 2-bit multiplier is \_\_\_\_\_

Max Marks: 1



Correct Answer

Solution: (64)

Solution: 64 bits

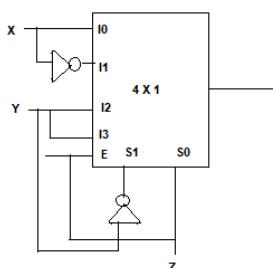
The result of multiplication of two 2-bit number will be of  $2 * 2 = 4$  bits  
 Total number of multiplication possible are:  $2^2 * 2^2 = 2^4$

Therefore, the size of the memory will be:  $2^4 * 2^2 = 2^6 = 64$  bits

Q.2)

Consider the below give circuit.

Max Marks: 1



Which of the following is the correct expression representing F?



X'YZ

Correct Option

Solution: (A)

Solution: (i)

According to the given circuit:

I0 = X

I1 = X'

I2 = Y = I3

E = Z

S1 = Y'

S2 = Z

Since  $F = E(S1'S0' \cdot I0 + S1'S0 \cdot I1 + S1S0' \cdot I2 + S1S0 \cdot I3)$ 

Therefore, the expression will be:

$$\Rightarrow Z(YZ'X + YZX' + Y'Z'Y + Y'ZY)$$

$$\Rightarrow Z(XYZ' + X'YZ)$$

$$\Rightarrow X'YZ$$

Hence, the correct option is (i)



X'Y



XYZ'



X'YZ'

Q.3)

Total number of 2 X 1 multiplexer required in order to implement 16 X 1 multiplexer are \_\_\_\_\_

Max Marks: 1



Correct Answer

Solution: (15)

Solution: 15

Number of Mux required to construct M X 1 Mux using N X 1 Mux is calculated as follows:

Here, M = 16 and N = 2

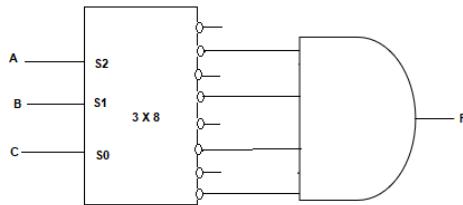
$$\# \text{ levels} = \log_2 M = \log_2 16 = 4$$

$$\text{Total number of devices} = \sum_{i=1}^{16/4} (M/N^i) = 16/2^1 + 16/2^2 + 16/2^3 + 16/2^4 = 8 + 4 + 2 + 1 = 15$$

Hence, the total number of multiplexers required are 15

Q.4)

Consider the below given combinational circuit:



The total number of free variables in function  $F(A, B, C)$  are \_\_\_\_\_

Max Marks: 1

Correct Answer

Solution: (2)

Solution: 2

Here the function  $F$  is given in the form of the maxterms i.e  $F(A, B, C) = \pi(1, 3, 5, 7)$   
Hence, the k-map will be:

A\BC	00	01	11	10
0		0	0	
1		0	0	

Since, only a quad is required to cover all maxterms, hence, the minimal expression will be:  $C'$

Thus, the total number of free variables are 2.

Q.5)

Given a XY-FF whose function table is:

Max Marks: 1

X	Y	$Q_n$
0	0	0
0	1	$Q^*$
1	0	$Q$
1	1	1

Which of the following is correct about the expression of J and K if XY-FF is realised using JK-FF?

A

 $J = X, K = Y$ 

B

 $J = Y, K = X$ 

C

 $J = X'Q, K = Y$ 

D

 $J = Y, K = X'$ 

Correct Option

Solution: (D)

Solution: (iv)

Since, XY-FF is realised using JK-FF, therefore we will be in need to build the excitation table of JK-FF

The excitation table of JK-FF is:

Q	$Q_n$	J	K
0	0	0	$\Phi$
0	1	1	$\Phi$
1	0	$\Phi$	1
1	1	$\Phi$	0

Based on the excitation table of JK-FF and function table of XY-FF we can build the characteristic table of them

A	B	Q	$Q_n$	J	K
0	0	0	0	0	$\Phi$
0	0	1	0	$\Phi$	1
0	1	0	1	1	$\Phi$
0	1	1	0	$\Phi$	1
1	0	0	0	0	$\Phi$
1	0	1	1	$\Phi$	0
1	1	$\Phi$	$\Phi$	$\Phi$	$\Phi$

1	1	1	1	$\Phi$	0
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The k-map for J will be:

X\YQ	00	01	11	10
0	0	$\Phi$	$\Phi$	1
1	0	$\Phi$	$\Phi$	1

Since only 1 quad is required, therefore,  $J = Y$

The k-map for K will be:

X\YQ	00	01	11	10
0	$\Phi$	1	1	$\Phi$
1	$\Phi$	0	0	$\Phi$

Since only 1 pair is possible, therefore,  $K = X'$

Hence, the correct option is (iv)

Q.6)

The minimum number of D-FF required to design a mod-130 counter are \_\_\_\_\_

Max Marks: 1

Correct Answer

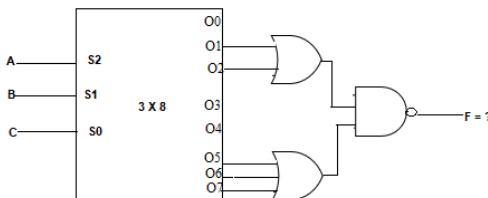
Solution: (8)

For a mod-130 counted we need 130 FF. Therefore,  
 $2^n \geq 130 \Rightarrow n \geq 8$

Q.7)

What is the minimal expression for function  $F(A, B, C)$  for the given combinational circuit?

Max Marks: 1



A  $AC + BC + A'B + B'C + C'$

B  $AC + BC + A'B + B'C'$

C  $AC + A'B + B' + C'$

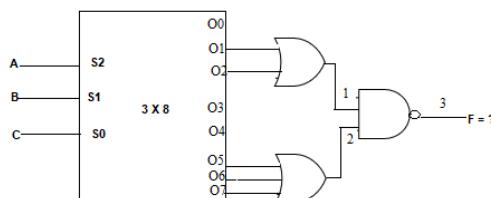
D None of the above

Correct Option

Solution: (D)

Solution: (iv)

For the given circuit:



Expression at 1 will be:  $ABC' + AB'C$

Expression at 2 will be:  $A'BC' + A'B'C + A'B'C' = A'BC' + A'B'$

Expression at 3 will be:

$\Rightarrow ((ABC' + AB'C) \cdot (A'BC' + A'B'))'$

$\Rightarrow (ABC' + AB'C)' + (A'BC' + A'B')'$

$\Rightarrow (A' + B' + C)(A' + B + C') + (A + B' + C)(A + B)$

$\Rightarrow A' + A'B + A'C' + A'B' + B'C' + A'C + BC + A + AB + AC + BC$

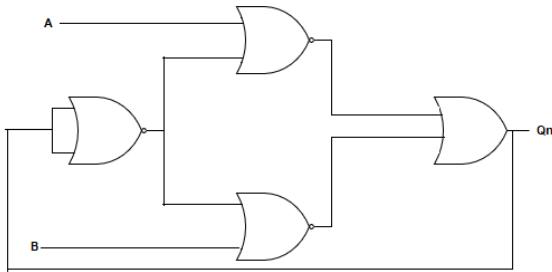
Since  $A + A' = 1$  and 1 and any term = 1. Hence, the whole expression will be 1

Thus, none of the above options are correct about the minimal expression of function F.

Q.8)

Consider the below given sequential circuit of AB-FlipFlop:

Max Marks: 1



What will be the value of  $Q_n$  if A and B are 0, 1 respectively?

A  $Q = Q_n = 1$

B  $Q_n = Q'$

C  $Q_n = Q$

Correct Option

Solution: (c)

The expression of the AB-FF is:  $(A + Q')^* + (B + Q')^* = A'Q + B'Q$

The function table will be:

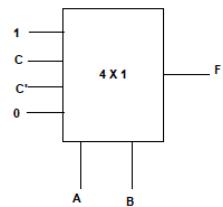
A	B	$Q_n$
0	0	Q
0	1	Q
1	0	Q
1	1	0

D  $Q_n = Q = 0$

Q.9)

Which of the following is the correct canonical sum of product for the function F shown in the below given circuit?

Max Marks: 1



A  $F(A, B, C) = \Sigma(2, 5, 6, 7)$

B  $F(A, B, C) = \Sigma(0, 1, 2, 3)$

C  $F(A, B, C) = \Sigma(0, 1, 3, 4)$

Correct Option

Solution: (c)

Solution: (iii)

Based on the given MUX circuit along with the inputs, the expression for F will be given as:

$$\Rightarrow F = S1'S0' \cdot I0 + S1'S0 \cdot I1 + S1S0' \cdot I2 + S1S0 \cdot I3$$

$$\Rightarrow A'B' \cdot 1 + A'B \cdot C + AB' \cdot C' + AB \cdot 0$$

$$\Rightarrow A'B' + A'BC + AB'C'$$

On expanding the first term we will get:

$$\Rightarrow A'B'C (M_1) + A'B'C' (M_0) + A'BC (M_3) + AB'C' (M_4)$$

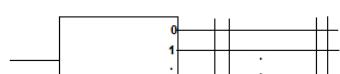
Hence  $F(A, B, C) = \Sigma(0, 1, 3, 4)$

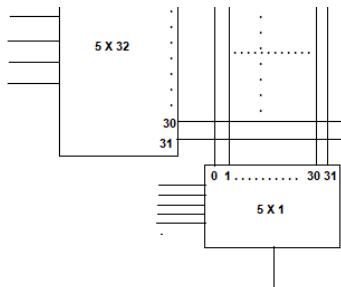
D None of the above

Q.10)

Which of the following is true about the number of links and connections for the given memory circuit?

Max Marks: 1





A 1024 connections and 64 links

B 1025 connections and 1024 links

C 64 connections and 1024 links

Correct Option

**Solution:** (c)

**Solution:** (iii)

As we know vertical lines represents the number of functions implemented and each horizontal line represents the minterms. When we buy a ROM, there are connections between every link. A user burns/removes the connections as per the requirement. Every ROM is expressed in terms of ROM matrix and Decoder. ROM matrix consists of links and connections. The lines entering the matrix and leaving it are called connections while the intersection of rows and columns are called links.

Therefore, the number of connections in memory circuit is given as # of vertical lines + number of horizontal lines (# of output lines of decoder + # of functions implemented by MUX) = 32 + 32 = 64

While the number of links in memory circuit is given as # of vertical lines \* # of horizontal lines (intersection of output lines of decoder and all function lines of mux) = 32 \* 32 = 1024.

Hence, the correct option is (iii).

D 80 connections and 1024 links

**Q.11)**

Max Marks: 2

Consider a JK'- FF (a JK-FF with an inverter at input K). Which of the following options are correct about the JK'-FF?

A It is equivalent to D-FF for J=0 and K=1 and vice-versa.

B At J = 0, K = 0, The JK'-FF will set the value of Q<sub>n</sub>.

C Both (i) and (ii)

D Neither (i) nor (ii)

Correct Option

**Solution:** (D)

**Solution:** (iv)

The expression of JK'-FF will be:  $JQ' + KQ$ . Based on this, the function table of this FF will be:

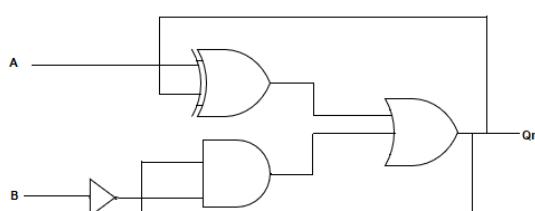
J	K	Q <sub>n</sub>
0	0	0
0	1	Q
1	0	Q'
1	1	1

At J=0, K = 1 and vice-versa, the FF will behave as T-FF and not as D-FF. Therefore (i) is incorrect.

At J = 0 and K = 0, the value of Q<sub>n</sub> will be reset and note set. Hence, the correct option is (iv).

**Q.12)**

Max Marks: 2



Which of the following is correct about the minterms for the above given sequential circuit?

A  $F(A, B, Q) = \Sigma(1, 2, 3, 4, 5, 6)$

B  $F(A, B, Q) = \Sigma(1, 3, 4, 5, 6)$

Correct Option

**Solution:** (B)

**Solution:** (ii)

For the given sequential circuit the equation for  $Q_n$  will be:

$$Q_n = A \oplus Q + B'Q = A'Q + AQ' + B'Q$$

The function table will be:

A	B	$Q_n$
0	0	Q
0	1	Q
1	0	1
1	1	$Q'$

Based on this, we can make the characteristic table:

A	B	Q	$Q_n$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Thus, the minterms for the function  $Q_n$  will be: 1, 3, 4, 5, 6

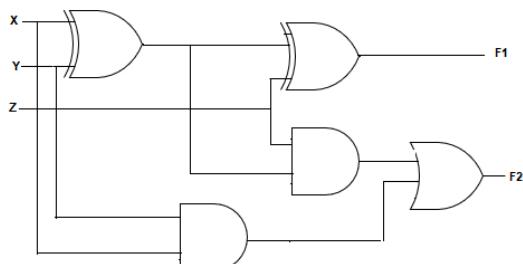
C  $F(A, B, Q) = \Sigma(1, 2, 3, 4, 5)$

D None of the above

Max Marks: 2

Q.13)

Consider the below given circuit:



The propagation delay for  $F_1$  and  $F_2$  if the delay for AND and OR gate is 1.2ms. The EX-OR gate is implemented using the AND, OR gate with the assumption that inputs are available in both complemented and uncomplemented form.

A  $P_{F_1} = 4.8\text{ms}, P_{F_2} = 3.6\text{ms}$

B  $P_{F_1} = 3.6\text{ms}, P_{F_2} = 4.8 \text{ ms}$

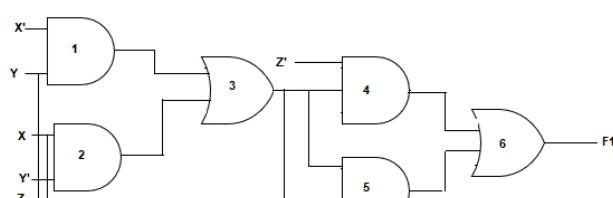
C  $P_{F_1} = 4.8\text{ms}, P_{F_2} = 4.8\text{ms}$

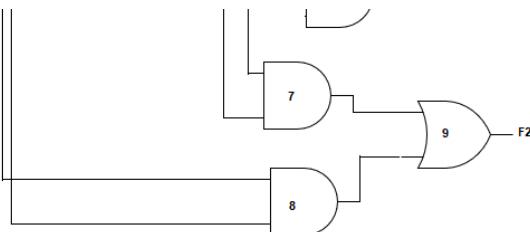
Correct Option

**Solution:** (C)

**Solution:** (iii)

On implementing the EX-OR using AND, OR gates, the circuit will be:





For F1:

The delay after crossing gate 1 and 2 will be 1.2 ms and after crossing gate 3, the delay will be  $1.2 + 1.2 = 2.4$ ms.

The output of gate 4 will be available after  $2.4 + 1.2 = 3.6$ ms (same for gate 5), thus the output of gate 6 will be available at  $3.6 + 1.2 = 4.8$ ms. Hence, the propagation delay for F1 will be 4.8 ms.

For F2:

Gate 7 input is available after the execution of gate 3. Thus, the output of gate 7 will be delayed by  $2.4 + 1.2 = 3.6$ ms while output of gate 8 was available after 1.2ms only, but it can't proceed further as gate 7 output was delayed. Hence, the output of gate 9 is delayed by  $1.2 + 3.6 = 4.8$ ms.

Hence, the correct option is (iii)

D None of the above

Q.14)

Max Marks: 2

A 4-bit carry lookahead adder adds two 4-bit numbers. The adder is designed without making use of the EX-OR gates. The propagation delay for all gates is given as 2.4 time units. What will be the overall delay of adder if we assume that inputs are made available in both complemented and uncomplemented form and carry network has been implemented using AND, Or gates.

A 7.2 time units

B 10.8 time units

C 12.0 time units

D 14.4 time units

Correct Option

Solution: (D)

Solution: (iv)

For carry lookahead adder we know that:

$$G_i = X_i Y_i$$

$$P_i = X_i \oplus Y_i$$

$$\text{Sum (S)} = P_i \oplus \text{Carry (C}_i\text{)}$$

Where,  $C_i$  for 4-bit is given as (in terms of G and P):

$$C_0 = G_0 + P_0 C_0$$

$$C_1 = G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$C_2 = G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_0$$

$$C_3 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 C_0$$

$G_i$  and  $P_i$  could be calculated in  $2.4 + 2.4 = 4.8$  time units in parallel. ( $P_i$  will take more time as XOR gate is implemented using 2 level AND, OR gates)

Sum could be calculated in  $2.4 + 2.4 = 4.8$  time units. (XOR is implemented using 2 level AND, OR gates)

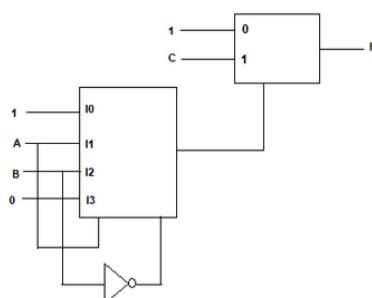
Once,  $G_i$  and  $P_i$  are available, the carry calculation will take  $2.4 + 2.4 = 4.8$  time units. (first level for all AND gates and second for all OR gates)

Thus the total time taken will be = sum of all the 3 step procedure =  $4.8 + 4.8 + 4.8 = 14.4$  time units.

Q.15)

Max Marks: 2

Which of the following is correct about the minterms presents in the canonical sum of product form of function F shown in the combinational circuit given below?



A  $F(A, B, C) = \Sigma(0, 1, 2, 3, 4, 7)$

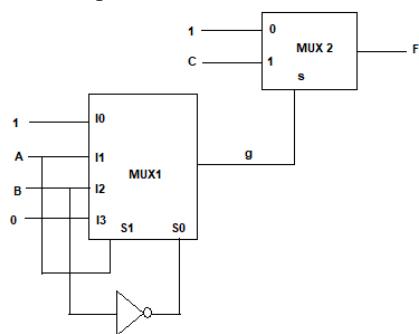
B  $F(A, B, C) = \Sigma(0, 1, 2, 5, 6, 7)$

C  $F(A, B, C) = \Sigma(0, 1, 3, 4, 7)$

**Solution:** (D)

Solution: (iv)

Here, For the given combinational circuit



$$S_1 = A, S_0 = B'$$

The function  $g$  will be given as:

$$\Rightarrow S_1' S_0' \cdot I_0 + S_1' S_0 \cdot I_1 + S_1 S_0' \cdot I_2 + S_1 S_0 \cdot I_3$$

$$\Rightarrow A'B'C + A'B'C' + AB'C' + AB'C$$

$$\Rightarrow A'B + AB$$

The function  $g$  is given as a select line in MUX 2. Hence the expression for  $F$  will be given as:

$$\Rightarrow S' \cdot I_0 + S \cdot I_1$$

Here,  $S$  is nothing but  $g$  i.e  $A'B + AB$ 

Therefore,

$$\Rightarrow (A'B + AB)' \cdot 1 + (A'B + AB) \cdot C$$

$$\Rightarrow (A + B')(A' + B') + A'BC (M_2) + ABC (M_7)$$

$$\Rightarrow AB' + A'B' + A'BC (M_2) + ABC (M_7)$$

$$\Rightarrow AB'C (M_4) + AB'C' (M_6) + A'B'C (M_1) + A'B'C' (M_0) + A'BC (M_5) + ABC (M_3)$$

Hence, the correct option is (iv)

close