1. The most appropriate matching for the following pairs is:-

   X: Indirect addressing 1: Loops
   Y: Immediate addressing 2: Pointers
   Z: Auto decrement addressing 3: Constants

   a)X−3,Y−2,Z−1
   b)X−1,Y−3,Z−2
   c)X−2,Y−3,Z−1
   d)X−3,Y−1,Z−2

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE 2000

2. Which is the most appropriate match for the items in the first column with the items in the second column:

   X.Indirect Addressing
   Y.Indexed Addressing
   Z.Base Register Addressing

   I.Array implementation
   II.Writing relocatable code
   III.Passing array as parameter

   a) (X, III), (Y, I), (Z, II)
   b) (X, II), (Y, III), (Z, I)
   c) (X, III), (Y, II), (Z, I)
   d) (X, I), (Y, III), (Z, II)

   Hindi [CLICK HERE]

English [CLICK HERE]

GATE 2001

3. Consider the following assembly language program for a hypothetical processor. A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments.

   If the initial value of register A is A0 the value of register B after the program execution will be

   (A) the number of 0 bits in A0
   (B) the number of 1 bits in A0
   (C) A0
   (D) 8

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE 2003

4. [continuation of last question]
   Which of the following instructions when inserted at location X will ensure that the value of register A after program execution is the same as its initial value ?
   (A) RRC A, #
   (B) NOP ; no operation
   (C) LRC A, # 1 ; left rotate A through carry flag by one bit
   (D) ADD A, # 1

   ANSWER - reffer the video solution of previous question i have covered both parts in that video

   GATE 2003

5. Q) Which of the following addressing modes are suitable for program relocation at run time?

   I. Absolute addressing

II. Based addressing
III. Relative addressing
IV.Indirect addressing

(a)I and IV
(b)I and II
(c)II and III
(d)I, II and IV

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2004

6. Using a 4–bit 2's complement arithmetic, which of the following additions will result in an overflow?

(i) 1100+1100
(ii) 0011+0111
(iii) 1111+0111

a. i only
b. ii only
c. iii only
d. i and iii only

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2004

7. Vid missing / lost

8. Consider the following program segment for a hypothetical CPU having three user registers R1, R2 and R3.

Instruction	Operation	Instruction Size(in words)
MOV R1,5000;	R1 ← Memory[5000]	2
MOV R2, (R1);	R2 ← Memory[(R1)]	1
ADD R2, R3;	R2 ← R2 + R3	1
MOV 6000, R2;	Memory [6000] ← R2	2
HALT	Machine halts	1

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

(A) 1007
(B) 1020
(C) 1024
(D) 1028

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2004

9. [continuation of last question]

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs during the executing the ADD instruction, the return address (in decimal) saved in the stack will be
(A) 1007
(B) 1004
(C) 1005
(D) 1016

ANSWER - reffer the video solution of previous question(1.8) i have covered all three parts in that video

GATE 2004

10. [continuation of last question]

Let the clock cycles required for various operations be as follows: Register to/ from memory transfer: 3 clock cycles ADD with both operands in register : 1 clock cycle Instruction fetch and decode : 2 clock cycles per word The total number of clock cycles required to execute the program is

(A) 29
(B) 24
(C) 23
(D) 20

ANSWER - reffer the video solution of previous question(1.8) I have covered all three parts in that video

GATE 2004

11. Consider a three word machine instruction

    ADD A[R0], @ B

    The first operand (destination) “A [R0]” uses indexed addressing mode with R0 as the index register. The second operand (source) “@ B” uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).The number of memory cycles needed during the execution cycle of the instruction is

    (A) 3
    (B) 4
    (C) 5
    (D) 6

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2005

12. Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

1) A[1] = B[J];	a) Indirect addressing
2) while [*A++];	b) Indexed, addressing
3) int temp = *x;	c) Autoincrement

(A) (1, c), (2, b), (3, a)
(B) (1, a), (2, c), (3, b)
(C) (1, b), (2, c), (3, a)
(D) (1, a), (2, b), (3, c)

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2005

13. A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

(A) 400
(B) 500
(C) 600
(D) 700

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2006

14. Which of the following statements about relative addressing mode is FALSE?

(A) It enables reduced instruction size
(B) It allows indexing of array elements with same instruction
(C) It enables easy relocation of data
(D) It enables faster address calculations than absolute addressing

Hindi [CLICK HERE]

English [CLICK HERE]

GATE 2006

15. The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

```
MOVI    Rs, 1           ; Move immediate
LOAD    Rd, 1000(Rs)    ; Load from memory
ADDI    Rd, 1000        ; Add immediate
STOREI  0(Rd), 20       ; Store immediate
```

Which of the statements below is TRUE after the program is executed ?
(A) Memory location 1000 has value 20
(B) Memory location 1020 has value 20
(C) Memory location 1021 has value 20
(D) Memory location 1001 has value 20

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2006

16. Consider a new instruction named branch-on-bit-set (mnemonic bbs). The instruction “bbs reg, pos, label” jumps to label if bit in position pos of register operand reg is one. A register is 32 bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.

temp←reg & mask

Branch to label if temp is non-zero. The variable temp is a temporary register. For correct emulation, the variable mask must be generated by:

(A) mask ← 0 x 1 o pos
(B) mask ← 0 x ffffffff o pos
(C) mask ← pos
(D) mask ← 0 × f

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2006

17. Data forwarding techniques can be used to speed up the operation in presence of data dependencies. Consider the following replacements of LHS with RHS.

R1→Loc,Loc→R2 ≡ R1→R2,R1→Loc
R1→Loc,Loc→R2 ≡ R1→R2
R1→Loc,R2→Loc ≡ R1→Loc
R1→Loc,R2→Loc ≡ R2→Loc

In which of the following options, will the result of executing the RHS be the same as executing the LHS irrespective of the instructions that follow ?
(A) (i) and (iii)
(B) (i) and (iv)
(C) (ii) and (iii)
(D) (ii) and (iv)

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2007

18. Following table indicates the latencies of operations between the instruction producing the result and instruction using the result.

Instruction producing the result	**Instruction using the result**	**Latency**
ALU Operation	ALU Operation	2
ALU Operation	Store	2
Load	ALU Operation	1
Load	Store	0

Consider the following code segment:

Load R1, Loc 1;	Load R1 from memory location Loc1
Load R2, Loc 2;	Load R2 from memory location Loc 2
Add R1, R2, R1;	Add R1 and R2 and save result in R1
Dec R2;	Decrement R2
Dec R1;	Decrement R1
Mpy R1, R2, R3;	Multiply R1 and R2 and save result in R3
Store R3, Loc 3;	Store R3 in memory location Loc 3

What is the number of cycles needed to execute the above code segment assuming each instruction takes one cycle to execute?

A)7
B)10
C)13
D)14

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2007

19. Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	R1←M[3000]	2
LOOP:	MOV R2,(R3)	R2←M[R3]	1
	ADD R2,R1	R2←R1 + R2	1
	MOV (R3),R2	M[R3]←R2	1
	INC R3	R3←R3 + 1	1
	DEC R1	R1←R1 − 1	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal. Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is:

(A) 10
(B) 11
(C) 20
(D) 21

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2007

20. [continuation of last question]
Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:
(A) 100
(B) 101
(C) 102
(D) 110

ANSWER - reffer the video solution of previous question(1.19) I have covered all three parts in that video

GATE 2007

21. [continuation of last question]
Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction “INC R3”, what return address will be pushed on to the stack?

(A) 1005
(B) 1020
(C) 1024
(D) 1040

ANSWER - reffer the video solution of previous question(1.19) I have covered all three parts in that video

GATE 2007

22. A processor that has carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two 2’s complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be:

(A) 1, 1, 0
(B) 1, 0, 0

(C) 0, 1, 0
(D) 1, 0, 1

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2008

23. Assume that EA = (X)+ is the effective address equal to the contents of location X, with X incremented by one word length after the effective address is calculated; EA = −(X) is the effective address equal to the contents of location X, with X decremented by one word length before the effective address is calculated; EA = (X)− is the effective address equal to the contents of location X, with X decremented by one word length after the effective address is calculated. The format of the instruction is (opcode, source, destination), which means (destination ← source op destination). Using X as a stack pointer, which of the following instructions can pop the top two elements from the stack, perform the addition operation and push the result back to the stack.

    (A) ADD (X)−, (X)
    (B) ADD (X), (X)−
    (C) ADD −(X), (X)+
    (D) ADD −(X), (X)+

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2008

24. pending

25. pending

26. Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the

addressing mode implemented by this instruction for operand in memory?

(A) Immediate Addressing
(B) Register Addressing
(C) Register Indirect Scaled Addressing
(D) Base Indexed Addressing

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2011

27. pending

28. A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____.

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2014

29. For computers based on three-address instruction formats, each address field can be used to specify which of the following:

    S1: A memory operand
    S2: A processor register
    S3: An implied accumulator register

    (A) Either S1 or S2
    (B) Either S2 or S3
    (C) Only S2 and S3
    (D) All of S1, S2 and S3

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2015

30. Consider a processor with byte-addressable memory. Assume that all registers, including Program Counter (PC) and Program Status Word (PSW), are of size 2 bytes. A stack in the main memory is implemented from memory location (0100)16 and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is (016E)16. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

    • Store the current value of PC in the stack.
    • Store the value of PSW register in the stack.
    • Load the starting address of the subroutine in PC.

    The content of PC just before the fetch of a CALL instruction is (5FA0)16. After execution of the CALL instruction, the value of the stack pointer is

    A.$(016A)_{16}$
    B.$(016C)_{16}$
    C.$(0170)_{16}$
    D.$(0172)_{16}$

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2015

31. A processor has 40 distinct instructions and 24 general purpose registers. A 32-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is _____

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2016

32. Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____

    Hindi [CLICK HERE]

English [CLICK HERE]

GATE 2016

33. Consider the C struct defines below:

```
struct data {
   int marks [100] ;
   char grade;
   int cnumber;
};
struct data student;
```

The base address of student is available in register R1. The field student.grade can be accessed efficiently using

(A) Post-increment addressing mode. (R1)+
(B) Pre-decrement addressing mode, -(R1)
(C) Register direct addressing mode, R1
(D) Index addressing mode, X(R1), where X is an offset represented in 2's complement 16-bit representation.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2017

34. Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC- relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

Instr. No.	Instruction
i:	add R2, R3, R4
i+1:	sub R5, R6, R7
i+2:	cmp R1, R9, R10
i+3:	beq R1, Offset

If the target of the branch instruction is i, then the decimal value of the Offest is _____.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2017

35. The following are some events that occur after a device controller issues an interrupt while process L is under execution.

(P) The processor pushes the process status of L onto the control stack.
(Q) The processor finishes the execution of the current instruction.
(R) The processor executes the interrupt service routine.
(S) The processor pops the process status of L from the control stack.
(T) The processor loads the new PC value based on the interrupt.

Which of the following is the correct order in the which the events above occur?

(A) QPTRS
(B) PTRSQ
(C) TRPQS
(D) QTPRS

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2018

36. pending

37. A processor has 16 integer registers (R0, R1, … , R15) and 64 floating point registers (F0, F1, … , F63). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type 4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F).

The maximum value of N is _____ .

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2018

38. The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A15 to A0. What is the range of address (in hexadecimal) of the memory system that can get enabled by the chip select (CS) signal?

(A) C800 to CFFF
(B) CA00 to CAFF
(C) C800 to C8FF
(D) DA00 to DFFF

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2019

39. If there are m input lines and n output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of m+n is _____ .

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2020

40. A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is _____ .

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2020

1. pending

2. Arrange the following configurations for CPU in decreasing order of operating speeds;

   Hardwired Control, vertical microprogramming, horizontal microprogramming

   (A) Hardwired control, Vertical microprogramming, Horizontal microprogramming.
   (B) Hardwired control, Horizontal microprogramming, Vertical microprogramming.
   (C) Horizontal microprogramming, Vertical microprogramming, Hardwired control.
   (D) Vertical microprogramming, Horizontal microprogramming, Hardwired control.

   Note-i have covered 2 questions in this video
   Hindi [CLICK HERE]
   English [CLICK HERE]

GATE 1999

3. pending

4. Consider the following data path of a simple non-pilelined CPU. The registers A, B, A1, A2, MDR, the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size 8 × (2:1) and the DEMUX is of size 8 × (1:2). Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and

MDR (Memory Date Register). SP can be decremented locally.

The CPU instruction “push r”, where = A or B, has the specification

M[SP]←r
SP←SP−1

How many CPU clock cycles are needed to execute the “push r” instruction?
(A) 1
(B) 3
(C) 4
(D) 5

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2001

5. Not in syllabus

6. pending

7. Horizontal microprogramming :

   (A) does not require use of signal decoders
   (B) results in larger sized microinstructions than vertical microprogramming
   (C) uses one bit for each control signal
   (D) all of the above.

   Note-i have covered 2 questions in this video
   Hindi [CLICK HERE]
   English [CLICK HERE]

GATE 2002

8. pending

9. The amount of ROM needed to implement a 4 bit multiplier is

   (A) 64 bits
   (B) 128 bits
   (C) 1 Kbits
   (D) 2 Kbits

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2004

10. A CPU has only three instructions I1, I2 and I3, which use the following signals in time steps T1-T5:

    I1 : T1 : Ain, Bout, Cin
    T2 : PCout, Bin
    T3 : Zout, Ain
    T4 : Bin, Cout
    T5 : End

    I2 : T1 : Cin, Bout, Din
    T2 : Aout, Bin
    T3 : Zout, Ain
    T4 : Bin, Cout
    T5 : End

    I3 : T1 : Din, Aout
    T2 : Ain, Bout
    T3 : Zout, Ain
    T4 : Dout, Ain
    T5 : End
    Which of the following logic functions will generate the hardwired control for the signal Ain ?

    (A) T1.I1 + T2.I3 + T4.I3 + T3
    (B) (T1 + T2 + T3).I3 + T1.I1
    (C) (T1 + T2).I1 + (T2 + T4).I3 + T3
    (D) (T1 + T2).I2 + (T1 + T3).I1 + T3

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2004

11. pending

12. pending

13. A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions I1 to I4 as shown below:

    Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively?

    ((Ij+Ik)Tn indicates that the control signal should be generated in time step Tn if the instruction being executed is Ij or Ik)

    (A) S5=T1+I2·T3 and S10=(I1+I3)·T4+(I2+I4)·T5
    (B) S5=T1+(I2+I4)·T3 and S10=(I1+I3)·T4+(I2+I4)·T5
    (C) S5=T1+(I2+I4)·T3 and S10=(I2+I3+I4)·T2+(I1+I3)·T4+(I2+I4)·T5
    (D) S5=T1+(I2+I4)·T3 and S10=(I2+I3)·T2+I4·T3+(I1+I3)·T4+(I2+I4)·T5

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2005

14. A line L in a circuit is said to have a stuck-at-0 fault if the line permanently has a logic value 0. Similarly a line L in a circuit is said to have a stuck-at-1 fault if the line permanently has a logic value 1. A circuit is said to have a multiple stuck-at fault if one or more lines have stuck at faults. The total number of distinct multiple stuck-at faults possible in a circuit with N lines is

    (A) 3^N
    (B) 3^N – 1
    (C) 2^N – 1
    (D) 2

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2005

15. An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

    Group 1 : 20 signals, Group 2 : 70 signals, Group 3 : 2 signals, Group 4 : 10 signals, Group 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

(A) 0
(B) 103
(C) 22
(D) 55

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2005

16. Consider the following data path of a CPU.

The, ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR

The instruction “add R0, R1” has the register transfer interpretation R0 ←R0 + R1. The minimum number of clock cycles needed for execution cycle of this instruction is:
(A) 2
(B) 3
(C) 4
(D) 5

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2005

17. [continuation of last question]

The instruction “call Rn, sub” is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

Rn ← PC + 1;
PC ← [PC];

The minimum number of CPU clock cycles needed during the execution cycle of this instruction is:

(A) 2
(B) 3
(C) 4
(D) 5

ANSWER - reffer the video solution of previous question i have covered both parts in that video

GATE 2005

18. The floating point unit of a processor using a design D takes 2t cycles compared to t cycles taken by the fixed point unit. There are two more design suggestions D1 and D2. D1 uses 30% more cycles for fixed point unit but 30% less cycles for floating point unit as compared to design D. D2 uses 40% less cycles for fixed point unit but 10% more cycles for floating point unit as compared to design D. For a given program which has 80% fixed point operations and 20% floating point operations, which of the following ordering reflects the relative performances of three designs?(Di > Dj denotes that Di is faster than Dj)

    (A) D1 > D > D2
    (B) D2 > D > D1
    (C) D > D2 > D1
    (D) D > D1 > D2

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2007

19. Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125

control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

(A) 125, 7
(B) 125, 10
(C) 135, 7
(D) 135, 10

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2008

20. Which of the following is/are true of the auto-increment addressing mode?

I. It is useful in creating self-relocating code.
II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation.
III. The amount of increment depends on the size of the data item accessed.

(A) I only
(B) II only
(C) III Only
(D) II and III only

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2008

21. Pending

22. A CPU generally handles an interrupt by executing an interrupt service routine:-

(A) As soon as an interrupt is raised
(B) By checking the interrupt register at the end of fetch cycle.
(C) By checking the interrupt register after finishing the execution of the current instruction.

(D) By checking the interrupt register at fixed time intervals.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2009

23. The amount of ROM needed to implement a 4 bit multiplier is

(A) 64 bits
(B) 128 bits
(C) 1 Kbits
(D) 2 Kbits

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2012

24. Consider the following sequence of micro-operations.

MBR ← PC
MAR ← X
PC ← Y
Memory ← MBR

Which one of the following is a possible operation performed by this sequence?

(A) Instruction fetch
(B) Operand fetch
(C) Conditional branch
(D) Initiation of interrupt service

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2013

25. A multiplexer is placed between a group of 32 registers and an accumulator to regulate data movement such that at any given point in time the content of only one register will move to the accumulator. The number of select lines needed for the multiplexer is _____ .

Hindi [CLICK HERE]
English [CLICK HERE]

26. Consider the following data path diagram.

R0 ← R1 + R2
The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and w indicate read and write operations, respectively.

Which one of the following is the correct order of execution of the above steps ?
(A) 2, 1, 4, 5, 3
(B) 1, 2, 4, 3, 5
(C) 3, 5, 2, 1, 4
(D) 3, 5, 1, 2, 4

Hindi [CLICK HERE]
English [CLICK HERE]

1. Comparing the time T1 taken for a single instruction on a pipelined CPU with time T2 taken on a non pipelined but identical CPU, we can say that

   (A) T1 <= T2
   (B) T1 >= T2
   (C) T1 < T2
   (D) T1 is T2 plus the time taken for one instruction fetch cycle

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE 2000

2. Pending

3. Pending

4. Pending

5. Pending

6. Video lost

7. In an enhancement of a design of a CPU, the speed of a floating point unit has been increased by 20% and the speed of a fixed point unit has been increased by 10%. What is the overall speedup achieved if the ratio of the number of floating point operations to the number of fixed point operations is 2:3 and the floating point operation used to take twice the time taken by the fixed point operation in the original design?

   (A) 1.155
   (B) 1.185
   (C) 1.255
   (D) 1.285

   Hindi [CLICK HERE]

English [CLICK HERE]

GATE 2004

8. A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 nanoseconds respectively. Registers that are used between the stages have a delay of 5 nanoseconds each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be

   (A) 120.4 microseconds
   (B) 160.5 microseconds
   (C) 165.5 microseconds
   (D) 590.0 microseconds

   Hindi [CLICK HERE]
   English [CLICK HERE]

GATE 2004

9. A 5 stage pipelined CPU has the following sequence of stages:

   IF — Instruction fetch from instruction memory,
   RD — Instruction decode and register read,
   EX — Execute: ALU operation for data and address computation,
   MA — Data memory access - for write access, the register read at RD stage is used,
   WB — Register write back.

   Consider the following sequence of instructions:

   I1 : L R0, 1oc1; R0 ← M[1oc1]
   I2 : A R0, R0; R0 ← R0 + R0
   I3 : S R2, R0; R2 ← R2 - R0

   Let each stage take one clock cycle.

   What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I1 ?
   (A) 8
   (B) 10
   (C) 12
   (D) 15

   Hindi [CLICK HERE]
   English [CLICK HERE]

GATE 2005

10. We have two designs D1 and D2 for a synchronous pipeline processor. D1 has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design D2 has 8 pipeline stages each with 2 nsec execution time How much time can be saved using design D2 over design D1 for executing 100 instructions?

    (A) 214 nsec
    (B) 202 nsec
    (C) 86 nsec
    (D) – 200 nsec

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2005

11. A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 109 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:

    (A) 1.0 second
    (B) 1.2 seconds
    (C) 1.4 seconds
    (D) 1.6 seconds

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2006

12. The data path shown in the figure computes the number of 1s in the 32-bit input word corresponding to an unsigned even integer stored in the shift register.The unsigned counter, initially zero, is incremented if the most significant bit of the shift register is incremented if the most significant bit of the shift register is 1.

    The micro-program for the control is shown in the table below with missing control words for micro-instructions I_1, I_2, ….. I_n.

The counter width (k), the number of missing micro-instructions (n), and the control word for microinstructions I_1, I_2, ….. I_n are, respectively,

(A) 32, 5, 010
(B) 5, 32, 010
(C) 5, 31, 011
(D) 5, 31, 010

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2006

13. A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement $X=(S-R*(P+Q))/T$ is given below. The values of variables P,Q,R,S and T are available in the registers $R0,R1,R2,R3$ and $R4$ respectively, before the execution of the instruction sequence.

The number of Read-After-Write (RAW) dependencies, Write-After-Read(WAR) dependencies, and Write-After-Write (WAW) dependencies in the sequence of instructions are, respectively,

(A) 2, 2, 4
(B) 3, 2, 3
(C) 4 ,2, 2
(D) 3 ,3, 2

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2006

14. [continuation of last question]

The IF, ID and WB stages take 1 clock cycle each. The EX stage takes 1 clock cycle each for the ADD, SUB and STORE operations, and 3 clock cycles each for MUL and

DIV operations. Operand forwarding from the EX stage to the ID stage is used. The number of clock cycles required to complete the sequence of instructions is

(A) 10
(B) 12
(C) 14
(D) 16

ANSWER - reffer the video solution of previous question(3.13) i have covered all three parts in that video

GATE 2006

15. A processor takes 12 cycles to complete an instruction I. The corresponding pipelined processor uses 6 stages with the execution times of 3, 2, 5, 4, 6 and 2 cycles respectively. What is the asymptotic speedup assuming that a very large number of instructions are to be executed?

(A) 1.83
(B) 2
(C) 3
(D) 6

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2007

16. Consider a pipelined processor with the following four stages:

IF: Instruction Fetch
ID: Instruction Decode and Operand Fetch
EX: Execute
WB: Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD	R2, R1, R0	R2 ← R0 + R1
MUL	R4, R3, R2	R4 ← R3 * R2
SUB	R6, R5, R4	R6 ← R5 - R4

(A) 7
(B) 8
(C) 10
(D) 14

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2007

17. A non pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the latches is 0.5 nsec. The speedup of the pipeline processor for a large number of instructions is

    (A) 4.5
    (B) 4.0
    (C) 3.33
    (D) 3.0

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2008

18. Pending

19. Pending (2 part question—--> lost part 1)

20. Delayed branching can help in the handling of control hazards
    The following code is to run on a pipelined
    processor with one branch delay slot:

    I1: ADD R2←R7+R8
    I2 : SUB R4← R5-R6
    I3 : ADD R1← R2+R3
    I4 : STORE Memory [R4]←[R1]
    BRANCH to Label if R1== 0
    Which of the instructions I1, I2, I3 or I4 can legitimately occupy the delay slot without any other program modification?

    (A) I1
    (B) I2

(C) I3
(D) I4

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2008

21. Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below:

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?
For (i=1 to 2) {I1; I2; I3; I4;}

(A) 16
(B) 23
(C) 28
(D) 30

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2009

22. A 5-stage pipelined processor has Instruction Fetch(IF),Instruction Decode(ID),Operand Fetch(OF),Perform Operation(PO)and Write Operand(WO)stages.The IF,ID,OF and WO stages take 1 clock cycle each for any instruction.The PO stage takes 1 clock cycle for ADD and SUB instructions,3 clock cycles for MUL instruction,and 6 clock cycles for DIV instruction respectively.Operand forwarding is used in the pipeline.What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
I0 :MUL R2 ,R0 ,R1	R2 ← R0 *R1
I1 :DIV R5 ,R3 ,R4	R5 ← R3/R4
I2 :ADD R2 ,R5 ,R2	R2 ← R5+R2

```
I3 :SUB R5 ,R2 ,R6          R5 ← R2-R6
```

(A) 13
(B) 15
(C) 17
(D) 19

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2010

23. Consider an instruction pipeline with four stages (S1, S2, S3 and S4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are as given in the figure:

    What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?
    (A) 4.0
    (B) 2.5
    (C) 1.1
    (D) 3.0

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2011

24. Pending

25. Consider an instruction pipeline with five stages without any branch prediction: Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions I1, I2, I3, ..., I12 is executed in this pipelined processor. Instruction I4 is the only branch

instruction and its branch target is I9. If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

(A) 132
(B) 165
(C) 176
(D) 328

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2013

26. Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is_____.

(A) 4
(B) 8
(C) 6
(D) 7

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2014

27. Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is _____.

(A) 1.6
(B) 3.2
(C) 1.2
(D) 0.8

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2014

28. Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

    P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.

    P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.

    P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.

    P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

    Which processor has the highest peak clock frequency?

    (A) P1
    (B) P2
    (C) P3
    (D) P4

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2014

29. An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency 2.2/3 ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is _____.

    Hindi [CLICK HERE]

English [CLICK HERE]

GATE 2014

30. Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speed up achieved in this pipelined processor is ____32____.

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2015

31. Consider the sequence of machine instructions given below:

    MUL R5, R0, R1
    DIV R6, R2, R3
    ADD R7, R5, R6
    SUB R8, R7, R4

    In the above sequence, R0 to R8 are general purpose registers. In the instructions shown, the first register stores the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the Result (WB). The IF, OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD or SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instructions is ____13 cycle____

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2015

32. Consider the following code sequence having five instructions I1 to I5. Each of these instructions has the following format.

    OP Ri, Rj, Rk

    where operation OP is performed on contents of registers Rj and Rk and the result is stored in register Ri.

I1 : ADD R1, R2, R3
I2 : MUL R7, R1, R3
I3 : SUB R4, R1, R5
I4 : ADD R3, R2, R4
I5 : MUL R7, R8, R9

Consider the following three statements:

S1: There is an anti-dependence between instructions I2 and I5.
S2: There is an anti-dependence between instructions I2 and I4.
S3: Within an instruction pipeline an anti-dependence always creates one or more stalls.

Which one of above statements is/are correct?

(A) Only S1 is true
(B) Only S2 is true
(C) Only S1 and S2 are true
(D) Only S2 and S3 are true

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2015

33. Pending

34. The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is _____ percent.

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2016

35. Consider a 3 GHz (gigahertz) processor with a three-stage pipeline and stage latencies v1, v2, and v3 such that ($\tau 1$) = 3($\tau 2$)/4 = 2($\tau 3$). If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is _____ GHz, ignoring delays in the pipeline registers

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2016

36. Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units UF and UG, respectively. Given two instances of UF and two instances of UG, it is required to implement the computation F(G(Xi)) for i goes from 1 to 10. ignoring all other delays, the minimum time required to complete this computation is _____ nanoseconds
Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2016

37. Instruction execution in a processor is divided into 5 stages. Instruction Fetch(IF), Instruction Decode (ID), Operand Fetch(OF), Execute(EX), and Write Back(WB), These stages take 5,4,20, 10 and 3 nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. Two pipelined implementations of the processor are contemplated:

    (i) a naive pipeline implementation (NP) with 5 stages and
    (ii) an efficient pipeline (EP) where the OF stage id divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively.

    The speedup (correct to two decimals places) achieved by EP over NP in executing 20 independent instructions with no hazards is _____.

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2017

38. The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Writeback (WB), The IF, ID, OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

The number of clock cycles required for completion of execution of the sequence of instruction is _____ .

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2018

39. Consider a non-pipelined processor operating at 2.5 GHz. It takes 5 clock cycles to complete an instruction. You are going to make a 5- stage pipeline out of this processor. Overheads associated with pipelining force you to operate the pipelined processor at 2 GHz. In a given program, assume that 30% are memory instructions, 60% are ALU instructions and the rest are branch instructions. 5% of the memory instructions cause stalls of 50 clock cycles each due to cache misses and 50% of the branch instructions cause stalls of 2 cycles each. Assume that there are no stalls associated with the execution of ALU instructions. For this program, the speedup achieved by the pipelined processor over the non-pipelined processor (round off to 2 decimal places) is _____ .

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2020

1. pending
2. pending

3. pending

4. pending
5. pending
6. pending
7. pending
8. pending
9. pending
10. pending
11. pending
12. pending
13. Consider a system with 2 level caches. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns, 10ns, and 500 ns, respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

    (A) 13.0 ns
    (B) 12.8 ns
    (C) 12.6 ns
    (D) 12.4 ns

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2004

14. Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is 8, 12, 0, 12, 8

    (A) 2

(B) 3
(C) 4
(D) 5

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2004

15. A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec. What percentage of the memory cycle time is used for refreshing?

(A) 10
(B) 6.4
(C) 1
(D) 0.64

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2005

16.

pending

17. Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. The number of bits needed for cache indexing and the number of tag bits are respectively

(A) 10, 17
(B) 10, 22
(C) 15, 17
(D) 5, 17

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2005

18. Consider a 2-way set associative cache memory with 4 sets and total 8 cache blocks (0-7) and a main memory with 128 blocks (0-127). What memory blocks will be

present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement. Assuming that initially the cache did not have any memory block from the current job?

0 5 3 9 7 0 16 55

(A) 0 3 5 7 16 55
(B) 0 3 5 7 9 16 55
(C) 0 5 7 9 16 55
(D) 3 5 7 9 16 55

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2005

19. A cache line is 64 bytes. The main memory has latency 32ns and bandwidth 1G.Bytes/s. The time required to fetch the entire cache line from the main memory is

(A) 32 ns
(B) 64 ns
(C) 96 ns
(D) 128 ns

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2006

20. A computer system has a level-1 instruction cache (1-cache), a level-1 data cache (D-cache) and a level-2 cache (L2-cache) with the following specifications:

The length of the physical address of a word in the main memory is 30 bits. The capacity of the tag memory in the I-cache, D-cache and L2-cache is, respectively,

(A) 1 K x 18-bit, 1 K x 19-bit, 4 K x 16-bit
(B) 1 K x 16-bit, 1 K x 19-bit, 4 K x 18-bit
(C) 1 K x 16-bit, 512 x 18-bit, 1 K x 16-bit
(D) 1 K x 18-bit, 512 x 18-bit, 1 K x 18-bit

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2006

21. A CPU has a cache with block size 64 bytes. The main memory has k banks, each bank being c bytes wide. Consecutive c − byte chunks are mapped on consecutive banks with wrap-around. All the k banks can be accessed in parallel, but two accesses to the same bank must be serialized. A cache block access may involve multiple iterations of parallel bank accesses depending on the amount of data obtained by accessing all the k banks in parallel. Each iteration requires decoding the bank numbers to be accessed in parallel and this takes k2ns.The latency of one bank access is 80 ns. If c=2 and k=24, the latency of retrieving a cache block starting at address zero from main memory is:

    (A) 92 ns
    (B) 104 ns
    (C) 172 ns
    (D) 184 ns

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2006

22. Consider two cache organizations: The first one is 32 KB 2-way set associative with 32-byte block size. The second one is of the same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has a latency of 0.6 ns while a kbit comparator has a latency of k/10 ns. The hit latency of the set associative
    organization is h1 while that of the direct mapped one is h2.

    The value of h1 is:
    (A) 2.4 ns
    (B) 2.3 ns
    (C) 1.8 ns
    (D) 1.7 ns

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2006

23. [continuation of last question]

The value of h2 is:
(A) 2.4 ns
(B) 2.3 ns
(C) 1.8 ns
(D) 1.7 ns

ANSWER - reffer the video solution of previous question i have covered both parts in that video

GATE 2006

24. A CPU has a 32 KB direct mapped cache with 128-byte block size. Suppose A is a two dimensional array of size 512×512 with elements that occupy 8-bytes each. Consider the following two C code segments, P1 and P2.

P1:

```
for (i=0; i{512; i++)
 {
   for (j=0; j{512; j++)
          {
                 x += A[i][j];
        }
}
```

P2:

```
for (i=0; i{512; i++)
{
   for (j=0; j{512; j++)
          {
                 x += A[j][i];
        }
}
```

P1 and P2 are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses

experienced by P1 be M1 and that for P2 be M2 .

The value of M1 is:
(A) 0
(B) 2048
(C) 16384
(D) 262144

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2006

25. [continuation of last question]

    The value of the ratio M1/M2 is:

    (A) 0
    (B) 1/16
    (C) 1/8
    (D) 16

    ANSWER - reffer the video solution of previous question i have covered both parts in that video

    GATE 2006

26. Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20-bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

    (A) 9,6,5
    (B) 7, 7, 6
    (C) 7, 5, 8
    (D) 9, 5, 6

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2007

27. Consider a machine with a byte addressable main memory of 2^16 bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in

the system. A 50 × 50 two-dimensional array of bytes is stored in the main memory starting from memory location 1100H. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data cache misses will occur in total?

(A) 40
(B) 50
(C) 56
(D) 59

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2007

28. [continuation of last question]

Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

(A)line 4 to line 11
(B)line 4 to line 12
(C)line 0 to line 7
(D)line 0 to line 8

ANSWER - reffer the video solution of previous question i have covered both parts in that video

GATE 2007

29. Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

The number of bits in the TAG, SET and WORD fields, respectively are:
(A) 7, 6, 7
(B) 8, 5, 7
(C) 8, 6, 6
(D) 9, 4, 7

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2008

30. [continuation of last question]

While accessing the memory location 0C795H by the CPU, the contents of the TAG field of the corresponding cache line is
(A) 000011000
(B) 110001111
(C) 00011000
(D) 110010101

ANSWER - reffer the video solution of previous question i have covered both parts in that video

GATE 2008

31.
pending

32.
pending

33. Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i { 1024; i++)
   for(j = 0; j { 1024; j++)
      ARR[i][j] = 0.0;
```

The size of double is 8Bytes. Array ARR is located in memory starting at the beginning of virtual page 0xFF000 and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR.

The total size of the tags in the cache directory is:

(A)32Kbits
(B)34Kbits
(C)64Kbits
(D)68Kbits

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2008

34. [continuation of last question]

Which of the following array elements have the same cache index as ARR[0][0]?

(A)ARR[0][4]
(B)ARR[4][0]
(C)ARR[0][5]
(D)ARR[5][0]

ANSWER - reffer the video solution of previous question i have covered all three parts in that video

GATE 2008

35. [continuation of last question]

The cache hit ratio for this initialization loop is:

(A)0%
(B)25%
(C)50%
(D)75%

ANSWER - reffer the video solution of previous question i have covered all three parts in that video

GATE 2008

36. How many 32K x 1 RAM chips are needed to provide a memory capacity of 256K-bytes?

(A) 8
(B) 32
(C) 64
(D) 128

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2009

37. Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order:

    0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155.

    Which one of the following memory block will NOT be in cache if LRU replacement policy is used?
    (A) 3
    (B) 8
    (C) 129
    (D) 216

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2009

38. A main memory unit with a capacity of 4 megabytes is built using 1M × 1-bit DRAM chips. Each DRAM chip has 1K rows of cells with 1K cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is:-

    A.100 nanoseconds
    B.100×2^10 nanoseconds
    C.100×2^20 nanoseconds
    D.3200×2^20 nanoseconds

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2010

39. A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds. 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively.

    When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken for this transfer?
    (A) 2 nanoseconds
    (B) 20 nanoseconds
    (C) 22 nanoseconds
    (D) 88 nanoseconds

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2010

40. [continuation of last question]

    When there is a miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken for these transfers?

    (A) 222 nanoseconds
    (B) 888 nanoseconds
    (C) 902 nanoseconds
    (D) 968 nanoseconds

    ANSWER - reffer the video solution of previous question i have covered both the parts in that video

    GATE 2010

41. An 8KB direct-mapped write-back cache is organized as multiple blocks, each size of 32-bytes. The processor generates 32-bit addresses. The cache controller contains

the tag information for each cache block comprising of the following.

◎ 1 valid bit
◎ 1 modified bit
◎ As many bits as the minimum needed to identify the memory block mapped in the cache.

What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

(A) 4864 bits
(B) 6144 bits
(C) 6656 bits
(D) 5376 bits

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2011

42. A computer has a 256 KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.
The number of bits in the tag field of an address is

(A) 11
(B) 14
(C) 16
(D) 27

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2012

43. [continuation of last question]

The size of the cache tag directory is
(A) 160 Kbits
(B) 136 bits

(C) 40 Kbits
(D) 32 bits

ANSWER - reffer the video solution of previous question i have covered both the parts in that video

GATE 2012

44. In a k-way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set (s+1). The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from.

    (A) (j mod v) * k to (j mod v) * k + (k-1)
    (B) (j mod v) to (j mod v) + (k-1)
    (C) (j mod k) to (j mod k) + (v-1)
    (D) (j mod k) * v to (j mod k) * v + (v-1)

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2013

45. A RAM chip has a capacity of 1024 words of 8 bits each (1K × 8). The number of 2 × 4 decoders with enable line needed to construct a 16K × 16 RAM from 1K × 8 RAM is

    (A) 4
    (B) 5
    (C) 6
    (D) 7

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2013

46. An access sequence of cache block address is of length N and contains n unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by k. What is the miss ration is the access sequence is passed through a cache of associativity A }= k exercising

least-recently used replacement policy.

(A) n/N
(B) 1/N
(C) 1/A
(D) k/n

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2014

47. A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is _____

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2014

48. pending

49. pending

50. pending

51. The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is _____.

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2014

52. Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The

average read access time in nanoseconds is_____.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2015

53. Consider a machine with a byte addressable main memory of 2^20 bytes, block size of 16 bytes and a direct mapped cache having 212 cache lines. Let the addresses of two consecutive bytes in main memory be (E201F)16 and (E2020)16. What are the tag and cache line address (in hex) for main memory address (E201F)16?

    (A) E, 201
    (B) F, 201
    (C) E, E20
    (D) 2, 01F

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2015

54. A processor can support a maximum memory of 4GB, where the memory is word-addressable (a word consists of two bytes). The size of address bus of the processor is at least _____bits.

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2016

55. The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is _____ bits

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2016

56. A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.

The smallest cache size required to ensure an average read latency of less than 6 ms is _____ MB.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2016

57. Consider a 2-way set associative cache with 256 blocks and uses LRU replacement. Initially the cache is empty. Conflict misses are those misses which occur due to the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of access to memory blocks :

    0, 128, 256, 128, 0, 128, 256, 128, 1, 129, 257, 129, 1, 129, 257, 129

    is repeated 10 times. The number of conflict misses experienced by the cache is _____ .

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2017

58. A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is _____ bits.

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2017

59. Consider a two-level cache hierarchy L1 and L2 caches. An application incurs 1.4 memory accesses per instruction on average. For this application, the miss rate of L1 cache 0.1, the L2 cache experience on average. 7 misses per 1000 instructions. The miss rate of L2 expressed correct to two decimal places is _____.

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2017

60. Consider a machine with byte addressable memory of 232 bytes divided into blocks of size 32 bytes. Assume a direct mapped cache having 512 cache lines is used with this machine. The size of tag field in bits is _____

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2017

61. The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

Cache	**Read access time (in nanoseconds)**	**Hit ratio**
I-cache	2	0.8
D-cache	2	0.9
L2-cache	8	0.9

The read access time of main memory in 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the write-back policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is _____

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2017

62. In a two-level cache system, the access times of L1 and L2 1 and 8 clock cycles, respectively. The miss penalty from the L2 cache to main memory is 18 clock cycles. The miss rate of L1 cache is twice that of L2. The average memory access time(AMAT) of this cache system is 2 cycles. The miss rates of L1 and L2 respectively are:

(A) 0.111 and 0.056
(B) 0.056 and 0.111
(C) 0.0892 and 0.1784

(D) 0.1784 and 0.0892

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2017

63. A 32 – bit wide main memory unit with a capacity of 1 GB is built using 256M X 4-bit DRAM chips. The number of rows of memory cells in the DRAM chip is 214. The time taken to perform one refresh operation is 50 nanoseconds. The refresh period is 2 milliseconds. The percentage (rounded to the closest integer) of the time available for performing the memory read/write operations in the main memory unit is _____

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2018

64. The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, the length (in number of bits) of the tag field is
(A) $P - N - \log_2 K$
(B) $P - N + \log_2 K$
(C) $P - N - M - W - \log_2 K$
(D) $P - N - M - W + \log_2 K$

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2018

65. A certain processor uses a fully associative cache of size 16 kB, The cache block size is 16 bytes. Assume that the main memory is byte addressable and uses a 32-bit address. How many bits are required for the Tag and the Index fields respectively in the addresses generated by the processor?

(A) 24 bits and 0 bits
(B) 28 bits and 4 bits

(C) 24 bits and 4 bits
(D) 28 bits and 0 bits

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2019

66. A certain processor deploys a single-level cache. The cache block size is 8 words and the word size is 4 bytes. The memory system uses a 60 MHz clock. To service a cache-miss, the memory controller first takes 1 cycle to accept the starting address of the block, it then takes 3 cycles to fetch all the eight words of the block, and finally transmits the words of the requested block at the rate of 1 word per cycle.

    The maximum bandwidth for the memory system when the program running on the processor issues a series of read operations is _____ × 10^6 bytes/sec.

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2019

67. A direct mapped cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is _____ .

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2020

68. A computer system with a word length of 32 bits has a 16 MB byte- addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.

    A1 = 0x42C8A4,
    A2 = 0x546888,
    A3 = 0x6A289C,
    A4 = 0x5E4880

    Which one of the following is TRUE ?

    (A) A1 and A4 are mapped to different cache sets.

(B) A2 and A3 are mapped to the same cache set.
(C) A3 and A4 are mapped to the same cache set.
(D) A1 and A3 are mapped to the same cache set.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2020

1. pending
2. pending
3. pending
4. pending
5. pending
6. pending
7. pending
8. pending
9. pending

10. pending

11. pending

12. pending

13. pending

14. A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

    (A)5.0%
    (B)1.0%
    (C)0.5%
    (D)0.1%

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2004

15. pending

16. pending

17. pending

18. pending

19. A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be 4 microsec. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode?

    (A) 15
    (B) 25
    (C) 35

(D) 45

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2005

20. Consider a disk drive with the following specifications: 16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one 4 byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

    (A)10
    (B)25
    (C)40
    (D)50

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2005

21. pending

22. pending

23. Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively:

    (A) 256 Mbyte, 19 bits
    (B) 256 Mbyte, 28 bits
    (C) 512 Mbyte, 20 bits
    (D) 64 Gbyte, 28 bit

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE 2007

24. Consider a Direct Mapped Cache with 8 cache blocks (numbered 0-7). If the memory block requests are in the following order

3, 5, 2, 8, 0, 63, 9,16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82,17, 24.

Which of the following memory blocks will not be in the cache at the end of the sequence ?
(A) 3
(B) 18
(C) 20
(D) 30

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2007

25. A hard disk system has the following parameters :

◎ Number of tracks = 500
◎ Number of sectors/track = 100
◎ Number of bytes /sector = 500
◎ Time taken by the head to move from one track to adjacent track = 1 ms
◎ Rotation speed = 600 rpm.

What is the average time taken for transferring 250 bytes from the disk ?

(A) 300.5 ms
(B) 255.5 ms
(C) 255.0 ms
(D) 300.0 ms

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2007

26. pending

27. A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple (c, h, s), where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0th sector is addressed as (0, 0, 0), the 1st sector as (0, 0, 1), and so on

The address {400,16,29} corresponds to sector number:
(A) 505035
(B) 505036

(C) 505037
(D) 505038

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2009

28. [continuation of last question]

The address of the 1039th sector is
(A) (0, 15, 31)
(B) (0, 16, 30)
(C) (0, 16, 31)
(D) (0, 17, 31)
ANSWER - reffer the video solution of previous question i have covered both parts in that video

GATE 2009

29. An application loads 100 libraries at start-up. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10 ms. Rotational speed of disk is 6000 rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected)

(A) 0.50 s
(B) 1.50 s
(C) 1.25 s
(D) 1.00 s

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2011

30. On a non-pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

Initialize the address register
Initialize the count to 500
LOOP: Load a byte from device

Store in memory at address given by address register
Increment the address register
Decrement the count
If count != 0 go to LOOP

Assume that each statement in this program is equivalent to machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speedup when the DMA controller based design is used in place of the interrupt driven program based input-output?
(A) 3.4
(B) 4.4
(C) 5.1
(D) 6.7

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2011

31. Consider a hard disk with 16 recording surfaces (0–15) having 16384 cylinders (0–16383) and each cylinder contains 64 sectors (0–63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is ⟨cylinder no.,surface no.,sector no.⟩ . A file of size 42797 KB is stored in the disk and the starting disk location of the file is ⟨1200,9,40⟩. What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?

(A)1281
(B)1282
(C)1283
(D)1284

Hindi [CLICK HERE]
English [CLICK HERE]

GATE 2013

32. Consider a disk pack with a seek time of 4 milliseconds and rotational speed of 10000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors. Assume that every sector access necessitates a seek, and the average rotational latency for accessing each sector is half of the time for one complete rotation. The total time (in milliseconds) needed to read the entire file is _____.

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2015

33. Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of 50 × 106 bytes/sec. If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512 byte sector of the disk is _____

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2015

34. The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29,154 kilobytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____

    Hindi [CLICK HERE]
    English [CLICK HERE]

GATE 2016

35. pending

of