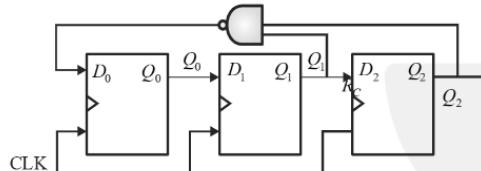


Q.62 A is a 9 bit signed integer the 2's complement representation of A is $(765)_8$ the 2's complement representation of $6 \times A$ is?

- (A) $(202)_8$ (B) $(676)_8$
 (C) $(457)_8$ (D) $(675)_8$

Q.63 Consider the equation $(57)x = (Y7)_{10}$ where X & Y are unknown then find the number of possible solution.

Q.64 For the circuit shown in figure below what is the output $Q_2 Q_1 Q_0$ as per four clock pulse. Initially all flip flop are reset.



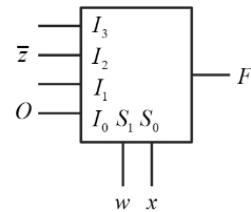
Answers

Digital Logic

1.	D	2.	B	3.	C	4.	B	5.	B
6.	3	7.	D	8.	C	9.	A	10.	D
11.	A	12.	D	13.	D	14.	2	15.	A
16.	D	17.	B	18.	B	19.	B	20.	C
21.	1	22.	B	23.	B, C	24.	B	25.	A
26.	C	27.	C	28.	C	29.	B	30.	B
31.	D	32.	219	33.	B	34.	B	35.	B
36.	C	37.	A	38.	A	39.	D	40.	B
41.	D	42.	C	43.	A	44.	A	45.	A
46.	B	47.	C	48.	D	49.	C	50.	B
51.	C	52.	100	53.	D	54.	D	55.	B
56.	A	57.	A	58.	D	59.	A	60.	C
61.	C,D	62.	B	63.	6	64.	B	65.	C

- (A) 100 (B) 110
 (C) 101 (D) 010

Q.65 The 4 to 1 multiplexer shown below implements the Boolean expression



If $F(w, x, y, z) = \Sigma m(4, 5, 7, 8, 10, 12, 15)$

The input to I_1 & I_3 will be

- (A) $yz, y'z'$ (B) $y+z', y \oplus z$
 (C) $y'+z, y \odot z$ (D) $y'+z, y \oplus z$

Explanations**Digital Logic****1. (D)**

The given number 1000 comes under special case of 2's complement which has single '1' followed by zeros.

Decimal equivalent number of 2's complement representation with single '1' followed by 'n' number of zeros = $-(2^n)$.

Given 2's complement number contain 3 zeros after '1', so the decimal number is $-(2^3) = -8$. Hence, the correct option is (D).

2. (B)**(i) Decimal to Hexadecimal :**

$$\begin{array}{r} 16 \mid 43 \\ \hline 2 \quad 11 \text{ (B)} \end{array}$$

Hence, $(43)_{10} \rightarrow (2B)_{16}$

(ii) Decimal to BCD :

$$(43)_{10} = (01000011)_{BCD}$$

Hence, the correct option is (B).

3. (C)

Given : $X = 01110$ and $Y = 11001$

MSB of both numbers represent sign bit. Since MSB of X is 0, hence it is positive number and since MSB of Y is 1, hence it is negative number.

$$\begin{array}{r} X = 01110 \\ + Y = +11001 \\ \hline Z = ①00111 \end{array}$$

↓
Discard carry

Since carry is discarded in the addition of two number represented in 2's complement, hence

$$X + Y = 00111$$

$X + Y$, in 6 - bit representation = 000111

Hence, the correct option is (C).

4. (B)

Given : $P = 11101101, Q = 11100110$

Both P and Q are in signed 2's complement form.

The MSB denotes sign of given number i.e. if MSB is 0 then given number is positive and if MSB is 1 then given number is negative.

$$P = 11101101$$

Since MSB of P is 1, hence it is a negative number.

Original number $P = 2$'s complement of P

Thus, the 2's complement of P will be

$$= 10010011$$

$$= -19$$

Similarly, the 2's complement of Q will be

$$= 10011001$$

$$\begin{array}{r} + 1 \\ \hline 10011010 \end{array}$$

$$= -26$$

$$\text{Thus, } P - Q = -19 - (-26) = +7$$

$$\text{Now, } +7 = 00000111$$

The signed 2's complement of a positive number is identical to the sign magnitude form of the positive number.

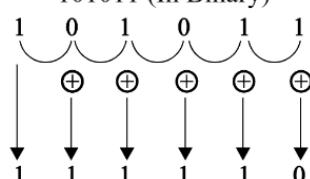
$$+7 = 00000111$$

Hence, the correct option is (B).

5. (B)

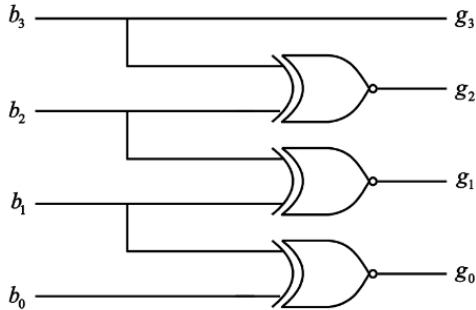
Given number

101011 (In Binary)



Gray code

For four bit binary $(b_3 b_2 b_1 b_0)$ to four bit gray code $(g_3 g_2 g_1 g_0)$



Circuit for Binary to Gray

Hence, answer is option (B).

6. 3

$$\begin{aligned}(x8)_y &= (123)_5 \\ y > x, y &> 8 \\ xy + 8 &= 1 \times 5^2 + 2 \times 5 + 3 \\ xy + 8 &= 25 + 10 + 3 \\ xy &= 30\end{aligned}$$

As we have,

$$\begin{aligned}y &> x \text{ and } y > 8 \\ xy + 8 &= 38 \\ xy &= 30 \\ x = 1, y &= 30 \text{ valid} \\ x = 2, y &= 15 \text{ valid} \\ x = 3, y &= 10 \text{ valid}\end{aligned}$$

Hence, 3 possible values exists.

7. (D)

$$(101)_b = (467)_{10} - (D2)_{16} \quad \dots(i)$$

Converting into equivalent decimal numbers,

$$\begin{aligned}(D2)_{16} &= (2 \times 16^0) + (13 \times 16^1) = 210 \\ (101)_b &= (1 \times b^0) + (0 \times b^1) + (1 \times b^2) = b^2 + 1\end{aligned}$$

From equation (i),

$$\begin{aligned}b^2 + 1 &= 467 - 210 \\ b^2 + 1 &= 257 \\ b^2 &= 256 \\ b &= 16\end{aligned}$$

Hence, the correct option is (D).

8. (C)

Given : $(A72E)_{16}$

Each hexadecimal bit is represented by 4 bit.

$$(101001100101110)_2$$

For octal representation grouping of 3 bit is done.

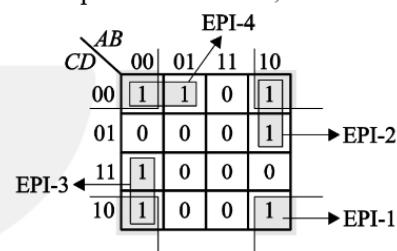
$$\begin{array}{ccccccc}0 & 0 & 1 & 0 & 0 & 1 & 1 \\ 5 & 4 & 3 & 2 & 1 & 0\end{array}$$

$$(123456)_8$$

Hence, the correct option is (C).

9. (A)

Given K-map is shown below,



To find the number of essential prime implicants, follow the procedures listed below :

- (i) Make all possible pairs in decreasing order i.e. from Oct → Quad → Pair → Single.
- (ii) For every group, find the number of 1's that are only one time circled i.e. the number of Essential Prime Implicants (EPI). Hence, the number of Essential Prime Implicants (EPI) = 4.

Hence, the correct option is (A).

10. (D)

Given y in SOP form as,

$$y = A + \bar{A}B$$

Converted above equation into standard canonical SOP form as,

$$y = A(B + \bar{B}) + \bar{A}B$$



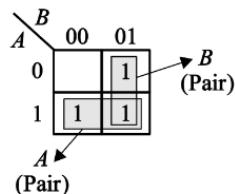
$$y = A\bar{B} + \underset{(10)}{AB} + \underset{(01)}{\bar{A}B}$$

So, y can be written in the form of minterms as,

$$y = \Sigma m(01, 10, 11)$$

$$y = \Sigma m(1, 2, 3)$$

Apply K-map for minimization of y ,



So, minimized form of y from K-map is,

$$y = A + B$$

Hence, the correct option is (D).

11. (A)

Minimization using K-map,

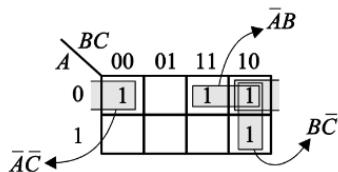
$$y = \underset{(000)}{\bar{A}\bar{B}\bar{C}} + \underset{(010)}{\bar{A}B\bar{C}} + \underset{(011)}{\bar{A}BC} + \underset{(110)}{AB\bar{C}}$$

So, y can be written in minterm form as,

$$y = \Sigma m(000, 010, 011, 110)$$

$$y = \Sigma m(0, 2, 3, 6)$$

y can be minimized using K-map in SOP form as, shown below,



Minimized expression of y is given below,

$$y = \bar{A}\bar{C} + \bar{A}B + B\bar{C}$$

Hence, the correct option is (A).

12. (D)

The number of distinct Boolean expression for n variables (N) = 2^{2^n}

Here, $n = 4$

$$\text{Hence, } N = 2^{2^4} = 2^{16} = 65536$$

Hence, the correct option is (D).

13. (D)

Given Y in SOP form as,

$$Y = \bar{A}\bar{B}\bar{C}D + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D}$$

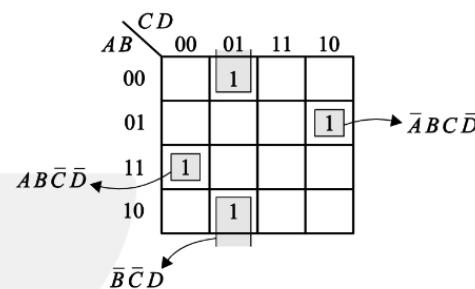
Minimization using K-map :

$$Y = \underbrace{\bar{A}\bar{B}\bar{C}D}_{(0001)} + \underbrace{\bar{A}BC\bar{D}}_{(0110)} + \underbrace{A\bar{B}\bar{C}D}_{(1001)} + \underbrace{AB\bar{C}\bar{D}}_{(1100)}$$

Y can be written in minterms as,

$$Y = \sum m(1, 6, 9, 12)$$

K-map for Y in SOP form as,



Therefore, minimized Y from above K-map,

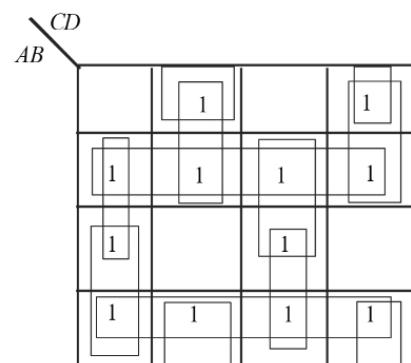
$$Y = \bar{A}BC\bar{D} + \bar{B}\bar{C}D + AB\bar{C}\bar{D}$$

Hence, the correct option is (D).

14. 2

Given :

$$f(A, B, C, D) = \Sigma(1, 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, 15)$$



There is only 2 essential prime implicants.

Hence, the correct answer is 2.



15. (A)

Given :

$$F = (X + Y)(X + \bar{Y}) + \overline{(X\bar{Y}) + \bar{X}}$$

$$F = (X + Y\bar{Y}) + \overline{(X\bar{Y}) + \bar{X}} \quad [\because Y\bar{Y} = 0]$$

$$F = X + \overline{(X\bar{Y}) + \bar{X}}$$

Applying De-Morgan's Rule

$$F = X + \overline{X\bar{Y}}\bar{X}$$

Again, apply De-Morgan rule,

$$F = X + (\bar{X} + Y)X$$

$$F = X + \bar{X}X + YX \quad [\because \bar{X}X = 0]$$

$$F = X + YX$$

$$F = X(1 + Y) \quad [\because 1 + Y = 1]$$

$$F = X(1) = X$$

Hence, the correct option is (A).

16. (D)

Given 4-variable function (F) in SOP form is,

$$\begin{aligned} F(w, x, y, z) &= wy + xy + \bar{w}x\bar{y}z \\ &\quad + \bar{w}\bar{x}y + xz + \bar{x}\bar{y}\bar{z} \end{aligned}$$

Converting each product term of (F) into standard canonic minterms as,

$$wy \rightarrow \begin{cases} w\bar{x}\bar{y}\bar{z} = 10 = m_{10} \\ w\bar{x}yz = 11 = m_{11} \\ wx\bar{y}\bar{z} = 14 = m_{14} \\ wxyz = 15 = m_{15} \end{cases}$$

$$xy \rightarrow \begin{cases} \bar{w}xy\bar{z} = 6 = m_6 \\ \bar{w}xyz = 7 = m_7 \\ wxy\bar{z} = 14 = m_{14} \\ wxyz = 15 = m_{15} \end{cases}$$

$$\bar{w}xyz \rightarrow 7 = m_7$$

$$\bar{w}\bar{x}y \rightarrow \begin{cases} \bar{w}\bar{x}\bar{y}\bar{z} = 2 = m_2 \\ \bar{w}\bar{x}yz = 3 = m_3 \end{cases}$$

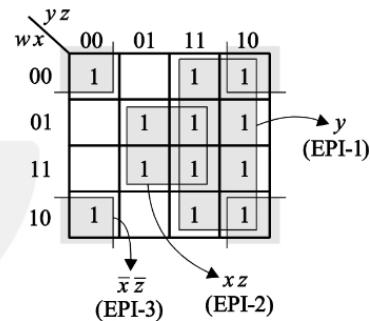
$$xz \rightarrow \begin{cases} \bar{w}x\bar{y}z = 5 = m_5 \\ \bar{w}xyz = 7 = m_7 \\ wx\bar{y}z = 13 = m_{13} \\ wxyz = 15 = m_{15} \end{cases}$$

$$\bar{x}\bar{y}\bar{z} \rightarrow \begin{cases} w\bar{x}\bar{y}\bar{z} = 8 = m_8 \\ \bar{w}\bar{x}\bar{y}\bar{z} = 0 = m_0 \end{cases}$$

So, function $F(w, x, y, z)$ is in SOP form,

$$\begin{aligned} F(w, x, y, z) &= \Sigma m(0, 2, 3, 5, 6, 7, \\ &\quad 8, 10, 11, 13, 14, 15) \end{aligned}$$

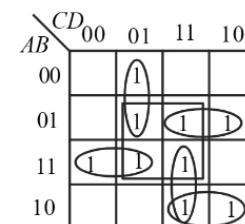
K-map for F is shown below,



Essential prime implicants : Number of prime implicants in which any of "1" is one time grouped is called Essential Prime implicant. Hence, essential prime implicants are $y, xz, \bar{x}\bar{z}$.

Hence, the correct option is (D).

17. (B)



$$SOP = \underbrace{\bar{A}\bar{C}D + AB\bar{C} + \bar{A}BC + A\bar{B}C + BD}_{ePI}$$

Total literals = 14.

Hence, the correct option is (B).



18. (B)

Given :

$$F(X, Y, Z) = \Sigma m(1, 2, 5, 6, 7) \rightarrow \text{SOP form}$$

Expression is given in SOP form but options are given in POS form. Hence, convert it into POS form.

Maxterm of given function is shown below,

$$F(X, Y, Z) = \Pi M(0, 3, 4) \rightarrow \text{POS form}$$

$$F(X, Y, Z) = \Pi M(000, 011, 100)$$

$$F(X, Y, Z) = (X + Y + Z)(X + \bar{Y} + \bar{Z}) \\ (\bar{X} + Y + Z)$$

Hence, the correct option is (B).

19. (B)

The given expression is,

$$f(A, B, C, D) = AD + ABCD + ACD \\ + \bar{A}B + A\bar{C}D + \bar{A}\bar{B} + \bar{A}\bar{B} + A\bar{A}$$

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$		1	1	1	1
$\bar{A}B$		1	1	1	1
$A\bar{B}$			1		
AB					
$A\bar{B}$			1	1	

Minimized expression of $f(A, B, C, D)$ is

$\bar{A} + D$.

Hence, the correct option is (B).

20. (C)

Given :

$$f(A, B, C, D) = \Sigma m(1, 5, 7, 12, 13, 14) \\ + d(0, 3, 11, 15)$$

AB	CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	x	1	x		
$\bar{A}B$		1	1		
$A\bar{B}$		1	1	x	1
AB					
$A\bar{B}$			x		

$$f(A, B, C, D) = \bar{A}D + AB$$

Output for $A, B, C, D = 0011, 1011$ and 1111

is,

$$f(0, 0, 1, 1) = 1 + 0 = 1$$

$$f(1, 0, 1, 1) = 0 + 0 = 0$$

$$f(1, 1, 1, 1) = 0 + 1 = 1$$

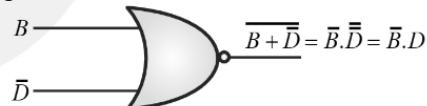
Hence, the correct option is (C).

21. 1

AB	00	01	11	10
CD				
00		d	d	
01	1			d
11	1			1
10		d	d	

$\bar{B}.D$

Here clearly says that complement of input is also present.



Only 1 NOR gate is required.

22. (B)

Given 4-variable function (F) is,

$$F = (\bar{X} + \bar{Y})(Z + W)$$

Apply De-Morgan law,

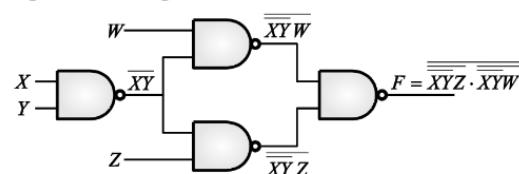
$$F = (\bar{X}\bar{Y})(Z + W)$$

$$F = (\bar{X}\bar{Y})Z + (\bar{X}\bar{Y})W$$

Again, apply De-Morgan law,

$$F = \overline{\overline{XYZ} \cdot \overline{XYW}}$$

This function can be implemented using only 2-input NAND gates:

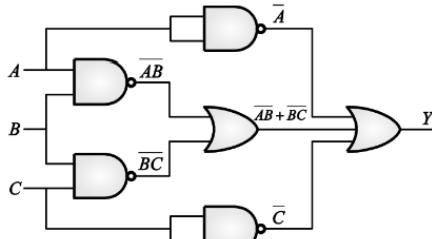




Thus, minimum number of 2-input NAND gate required to realize the given function are 4.
Hence, the correct option is (B).

23. B,C

Given logic circuit is shown below,



Output Y can be written as given below,

$$Y = \bar{A} + \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C} \rightarrow \text{Option (C)}$$

Apply De-Morgan rule,

$$\begin{aligned} Y &= \bar{A} + (\bar{A} + \bar{B}) + (\bar{B} + \bar{C}) + \bar{C} \\ &\quad (\because \bar{A} + \bar{A} = \bar{A}, \bar{B} + \bar{B} = \bar{B}, \bar{C} + \bar{C} = \bar{C}) \end{aligned}$$

$$Y = \bar{A} + \bar{B} + \bar{C} \rightarrow \text{Option (B)}$$

Hence, the correct options are (B) and (C).

24. (B)

Given : Output of a logic gate is “1”, when all its inputs are at logic “0”.

There are only three gates i.e., NOR, NAND and EX-NOR which will produce logic 1 at its output, when all of its input is at logic 0.

NOR gate :



$$Y_0 = 1 \text{ when } X = Y = 0$$

NAND gate :



$$Y_0 = 1 \text{ when } X = Y = 0$$

EX-NOR gate :



$$Y_0 = 1 \text{ when } X = Y = 0$$

Hence, the correct option is (B).

25. (A)

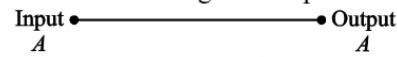
$$\text{Given : } F = A + A\bar{B} + A\bar{B}C$$

$$F = A(1 + \bar{B} + \bar{B}C)$$

$$(\because 1 + \text{Any literal} = 1)$$

$$F = A$$

To implement A , zero NAND gates are required, we can use a connecting wire to produce A .



Hence, the correct option is (A).

26. (C)

Given logic gate is shown below,



This is an EX-NOR gate, output of an EX-NOR gate is given by,

$$F = A \odot B$$

$$F = AB + \bar{A}\bar{B}$$

Here, $A = A$ and $B = 0$

$$\text{Hence, } F = A0 + \bar{A}\bar{0}$$

$$F = 0 + \bar{A}$$

$$F = \bar{A}$$

Hence, the correct option is (C).

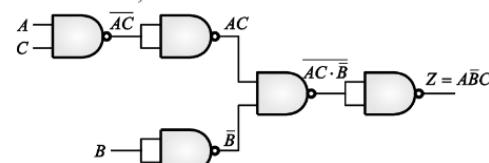
27. (C)

$$\text{Given : } Z = A\bar{B}C$$

Z can also be written as,

$$Z = \overline{A\bar{B}C} = \overline{\overline{AC}}\bar{B}$$

Realization of Z using two input NAND gate is shown below,



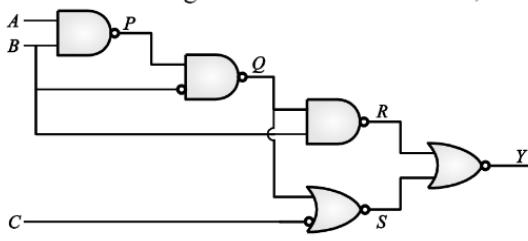
Thus, minimum number of 2-input NAND gates required to realize the given function are 5.

Hence, the correct option is (C).

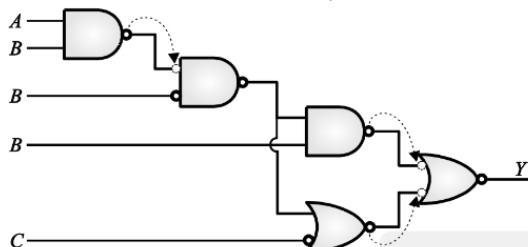


28. (C)

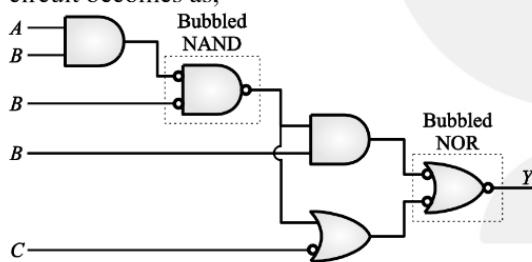
Given logic circuit is shown below,



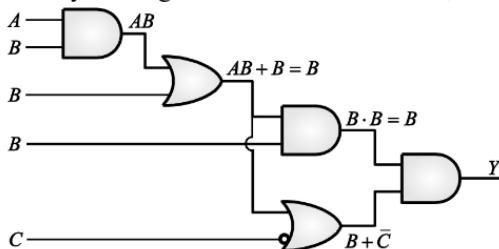
Given circuit is shown below,



Shifting bubbles as shown by dotted lines then circuit becomes as,



Replace bubble AND by OR gate and bubbled NOR by AND gate so circuit becomes as,



$$\text{So, } Y = \bar{B} \cdot (B + \bar{C})$$

$$Y = B \cdot B + B\bar{C} \quad (\because BB = B)$$

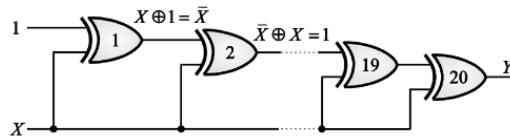
$$Y = B(1 + \bar{C}) \quad (\because 1 + \bar{C} = 1)$$

$$Y = B$$

Hence, the correct option is (C).

29. (B)

Digital circuit is shown below,



From above circuit,

$$\text{Output of 1st EX-OR gate } X \oplus 1 = \bar{X}$$

$$\text{Output of 2nd EX-OR gate } = \bar{X} \oplus X = 1$$

Hence, it can be concluded that output will be '1' for even numbers of EX-OR gates and output will be \bar{X} for odd number of EX-OR gates.

$$\text{i.e. output after 20th EX-OR gate} = 1.$$

Hence, the correct option is (B)

30. (B)

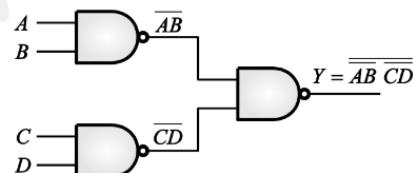
$$\text{Given : } Y = AB + CD$$

Y can also be written as,

$$Y = \overline{\overline{AB} + \overline{CD}}$$

$$Y = \overline{\overline{AB}} \overline{\overline{CD}}$$

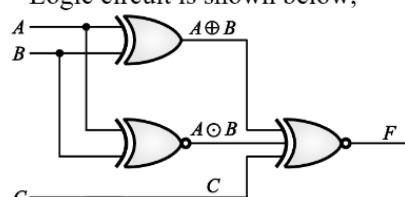
Now realize the function Y , using 2-input NAND gate.



Hence, the correct option is (B).

31. (D)

Logic circuit is shown below,



Output F can be written as

$$F = (A \oplus B) \odot (A \odot B) \odot C$$

complement of XNOR

$$\text{i.e. } A \oplus B = \overline{A \odot B}$$

and XNOR is equality detector

$$\text{So, } (A \oplus B) \odot (A \odot B) \odot C = 1$$

$$\text{Now, } F = (A \oplus B) \odot (A \odot B) \odot C$$

We Know that XNOR hate output are high when number of one's are appeared even time. If we perform XOR and XNOR for two variables only one output are high.

Because they both are complement of each other, and if we want $F = 1$ then C must be 1.

$$\Rightarrow C = 1 \text{ is the required input condition}$$

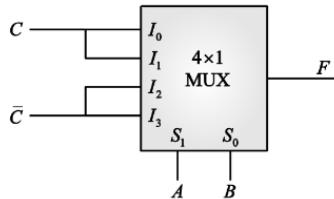
Hence, the correct options are (D).

32. 219

1. Convert 92 to bcd = 10010010
2. Convert to grey cod = 11011011
3. Values of select lines set are 11011011, where leftmost digit is MSB. So decimal equivalent of 11011011 will be the selected input line $\Rightarrow m = 219$

33. (B)

Given : A 4×1 MUX as shown below,



Output F can be written as,

$$F = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

Here, selection lines : $S_1 = A, S_0 = B$

Inputs : $I_0 = I_1 = C$ and $I_2 = I_3 = \bar{C}$

$$\text{Thus, } F = \bar{A} \bar{B} C + \bar{A} B \bar{C} + A \bar{B} \bar{C} + A B C$$

$$F = \bar{A} C (\bar{B} + B) + A \bar{C} (\bar{B} + B)$$

$$(\because B + \bar{B} = 1)$$

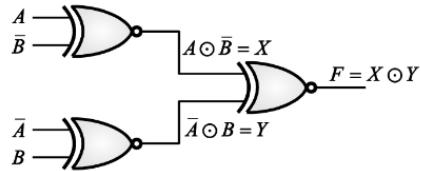
$$F = \bar{A} C + A \bar{C}$$

$$F = A \oplus C$$

Hence, the correct option is (B).

34. (B)

Given : Logic circuit as shown below,



From above logic circuit,

$$X = A \odot \bar{B} \text{ and } Y = \bar{A} \odot B$$

Output F is given by,

$$F = X \odot Y$$

$$F = (A \odot \bar{B}) \odot (\bar{A} \odot B)$$

$$F = (A \odot \bar{A}) \odot (B \odot \bar{B})$$

$$F = 0 \odot 0 \quad [\because X \odot \bar{X} = 0]$$

$$F = 1$$

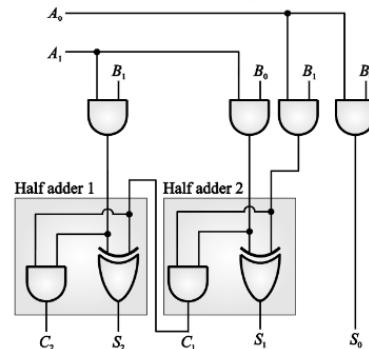
Hence, the correct option is (B).

35. (B)

2-bit multiplication can be represented as given below,

$$\begin{array}{r} & B_1 & B_0 \\ \times & A_1 & A_0 \\ \hline + & A_0 B_1 & A_0 B_0 \\ A_1 B_1 & A_1 B_0 & \vdots \\ \hline S_2 & S_1 & S_0 \end{array}$$

The above expression can be represented by logic circuit as shown below,



Thus, 2 EX-OR and 6 AND gates are used.

Hence, the correct option is (B).

36. (C)

Output Z can be written as,

$$Z = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3$$

The number of multiplexer required to implement $n \times 1$ MUX using $m \times 1$ MUX is given below,

$$\frac{n}{m} + \frac{n}{m^2} + \frac{n}{m^3} + \dots \text{ so on until ratio } \leq 1$$

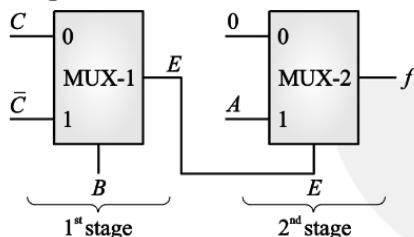
Since, $n = 4$ and $m = 2$

Hence, number of 2×1 MUX required to realize

$$4 \times 1 \text{ MUX} = \frac{4}{2} + \frac{4}{2^2} = 2 + 1 = 3$$

37. (A)

Given logic circuit is shown below,



Output of the 1st stage E is given by,

$$E = \bar{B}C + B\bar{C}$$

Output of the 2nd stage f is given by,

$$f = \bar{E} \cdot 0 + E \cdot A$$

Hence, $f = EA$

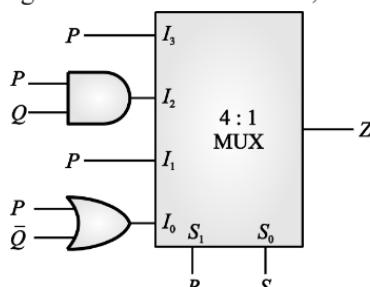
$$f = (\bar{B}C + B\bar{C})A$$

$$f = A\bar{B}C + AB\bar{C}$$

Hence, the correct option is (A).

38. (A)

Given logic circuit is shown below,



Inputs : $I_0 = P + \bar{Q}$, $I_1 = P$, $I_2 = PQ$, $I_3 = P$

Selection lines : $S_1 = R$, $S_0 = S$

Thus Z becomes as,

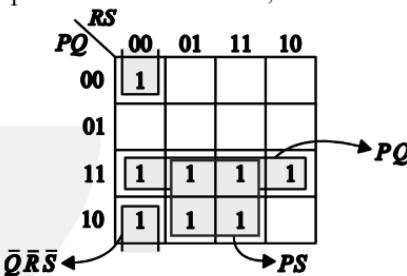
$$Z = \bar{R}\bar{S}I_0 + \bar{R}SI_1 + R\bar{S}I_2 + RSI_3$$

$$Z = \bar{R}\bar{S}(P + \bar{Q}) + \bar{R}SP + R\bar{S}PQ + RSP$$

$$Z = P\bar{R}\bar{S} + \bar{Q}\bar{R}\bar{S} + P\bar{R}S + \underbrace{PQR\bar{S}}_{(14)} + PRS$$

$$Z = \sum m(0, 8, 9, 11, 12, 13, 14, 15)$$

K-map for Z is shown below,

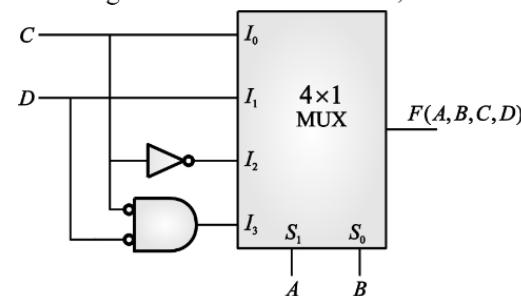


$$Z = PQ + PS + \bar{Q}\bar{R}\bar{S}$$

Hence, the correct option is (A).

39. (D)

Given logic circuit is shown below,



Output F , of the above circuit is given by,

$$F = \bar{S}_1\bar{S}_0I_0 + \bar{S}_1S_0I_1 + S_1\bar{S}_0I_2 + S_1S_0I_3 \quad \dots(i)$$

Selection line : $S_1 = A$, $S_0 = B$

Inputs : $I_0 = C$, $I_1 = D$, $I_2 = \bar{C}$, $I_3 = \bar{C}\bar{D}$

Put all the above values in equation (i),

$$F = \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}\bar{C} + AB\bar{C}\bar{D}$$

Converting above equation standard canonical SOP form,

1	0	1	1	0	m_{11}
1	1	0	0	1	m_{12}

$$\begin{aligned}
F &= \bar{A}\bar{B}C(D+\bar{D}) + \bar{A}BD(C+\bar{C}) \\
&\quad + A\bar{B}\bar{C}(D+\bar{D}) + AB\bar{C}\bar{D} \\
F &= \underbrace{\bar{A}\bar{B}CD}_{(3)} + \underbrace{\bar{A}\bar{B}C\bar{D}}_{(2)} + \underbrace{\bar{A}BCD}_{(7)} + \underbrace{\bar{A}B\bar{C}D}_{(5)} \\
&\quad + \underbrace{A\bar{B}\bar{C}D}_{(9)} + \underbrace{A\bar{B}\bar{C}\bar{D}}_{(8)} + \underbrace{AB\bar{C}\bar{D}}_{(12)}
\end{aligned}$$

Thus, $F = \Sigma m(2, 3, 5, 7, 8, 9, 12)$

Hence, the correct option is (D).

40. (B)

Let, 2-bit input binary number A and B as,

$$\begin{aligned}
A &= A_1 A_0 \\
B &= B_1 B_0
\end{aligned}
\right\} \text{2-bit input binary number}$$

According to question,

$$Y = 1, \text{ if } A > B$$

$$Y = 0 \text{ otherwise}$$

Based on above condition we can form truth table is shown below,

A_1	A_0	B_1	B_0	Y	Min-term
				$A > B$	
0	0	0	0	0	m_0
0	0	0	1	0	m_1
0	0	1	0	0	m_2
0	0	1	1	0	m_3
0	1	0	0	1	m_4
0	1	0	1	0	m_5
0	1	1	0	0	m_6
0	1	1	1	0	m_7
1	0	0	0	1	m_8
1	0	0	1	1	m_9
1	0	1	0	0	m_{10}

1	1	0	1	1	m_{13}
1	1	1	0	1	m_{14}
1	1	1	1	0	m_{15}

Now, the truth table for $(A > B)$ is shown below,

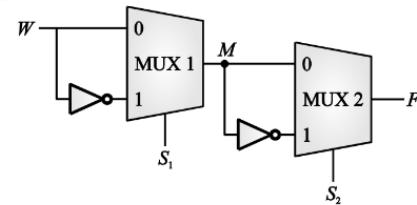
A_1	A_0	B_1	B_0	Y	Min-term
0	1	0	0	1	m_4
1	0	0	0	1	m_8
1	0	0	1	1	m_9
1	1	0	0	1	m_{12}
1	1	0	1	1	m_{13}
1	1	1	0	1	m_{14}

Thus, the number of combinations for which the output is logic “1” = 6.

Hence, the correct option is (B).

41. (D)

Given multiplexer circuit is shown below,



Output of MUX 1 is given by,

$$M = \bar{S}_1 W + S_1 \bar{W}$$

$$M = S_1 \oplus W$$

Output of MUX 2 is given by,

$$F = \bar{S}_2 M + S_2 \bar{M}$$

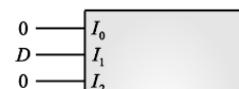
$$F = \bar{S}_2 (S_1 \oplus W) + S_2 (\bar{S}_1 \oplus \bar{W})$$

$$F = S_2 \oplus S_1 \oplus W$$

Hence, the correct option is (D).

42. (C)

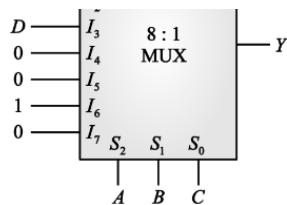
Given 8x1 MUX shown below,



$B \rightarrow$ Borrow

Thus, circuit diagram and expression of difference (D) and borrow (B) of half subtractor is shown below,





Here, A, B, C are the selection lines.

Output Y for 8×1 MUX is given by,

$$\begin{aligned} Y = & \bar{A}\bar{B}\bar{C}I_0 + \bar{A}\bar{B}CI_1 + \bar{A}B\bar{C}I_2 \\ & + \bar{A}BCI_3 + A\bar{B}\bar{C}I_4 + A\bar{B}CI_5 \\ & + AB\bar{C}I_6 + ABCI_7 \end{aligned} \quad \dots(i)$$

From figure,

$$I_0 = I_2 = I_4 = I_5 = I_7 = 0$$

$$I_1 = I_3 = D$$

$$I_6 = 1$$

Put the above values in equation (i),

$$Y = \bar{A}\bar{B}CD + \bar{A}BCD + AB\bar{C}$$

$$Y = \bar{A}CD(\bar{B} + B) + AB\bar{C}$$

$$Y = \bar{A}CD + AB\bar{C}$$

Hence, the correct option is (C).

43. (A)

$$X = A_1\bar{B}_1 + (A_1 \odot B_1)(A_0\bar{B}_0) \text{ (output)}$$

$$A_1 = 1, B_1 = 0 \text{ then } X = 1$$

If $A_1 = B_1$ (when MSB are equal)

$$A_0 = 1, B_0 = 0 \text{ then } X = 1$$

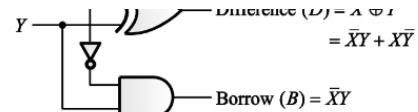
It is equal to 1 when $A > B$.

Hence, (A) is correct.

44. (A)

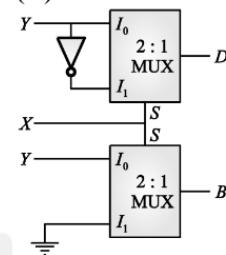
Given : X and $Y \rightarrow$ Input

$$D = X - Y \rightarrow \text{Difference}$$



Choosing from options,

From option (A) :



For upper MUX,

$$D = \bar{S}I_0 + SI_1$$

$$\text{Here, } S = X, I_0 = Y, I_1 = \bar{Y}$$

$$D = \bar{X}Y + X\bar{Y}$$

$$D = X \oplus Y$$

For lower MUX,

$$B = \bar{S}I_0 + SI_1$$

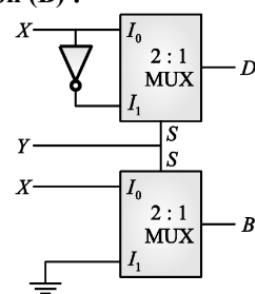
$$\text{Here, } S = X, I_0 = Y, I_1 = 0$$

$$B = \bar{X}Y + X0$$

$$B = \bar{X}Y$$

So, D shows expression of difference and B shows expression of borrow of half-subtractor. Thus, option (A) is correct.

From option (B) :



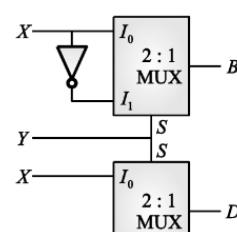
For upper MUX,

$$D = \bar{S}I_0 + SI_1$$

$$\text{Here, } S = Y, I_0 = X, I_1 = \bar{X}$$

$$D = \bar{Y}X + Y\bar{X}$$

$$D = X \oplus Y$$



for lower MUX,

$$B = \bar{S}I_0 + SI_1$$

Here, $S = Y, I_0 = X, I_1 = 0$

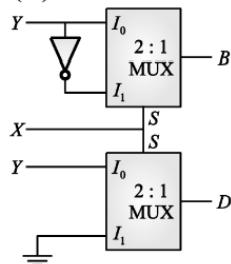
$$B = \bar{Y}X + Y(0)$$

$$B = \bar{Y}X$$

So, D shows expression of difference of half subtractor but B does not shows expression of borrow of half-subtractor.

Thus, option (B) is incorrect.

From option (C) :



For upper MUX,

$$B = \bar{S}I_0 + SI_1$$

Here, $S = X, I_0 = Y, I_1 = \bar{Y}$

$$B = \bar{X}Y + X\bar{Y}$$

$$B = X \oplus Y$$

For lower MUX,

$$D = \bar{S}I_0 + SI_1$$

Here, $S = X, I_0 = Y, I_1 = 0$

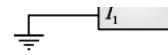
$$D = \bar{X}Y + X(0)$$

$$D = \bar{X}Y$$

So, D does not shows expression of difference of half subtractor and B does not shows expression of borrow of half-subtractor.

Thus, option (C) is incorrect.

From option (D) :



For upper MUX,

$$B = \bar{S}I_0 + SI_1$$

Here, $S = Y, I_0 = X, I_1 = \bar{X}$

$$B = \bar{Y}X + Y\bar{X} = (X \oplus Y)$$

For lower MUX,

$$D = \bar{S}I_0 + SI_1$$

Here, $S = Y, I_0 = X, I_1 = 0$

$$D = \bar{Y}X + Y(0)$$

$$D = \bar{Y}X$$

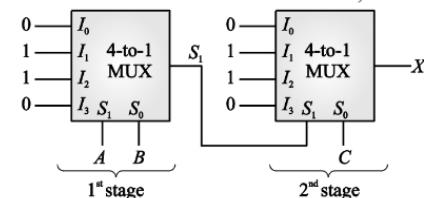
So, D does not shows expression of difference of half subtractor and B does not shows expression of borrow of half-subtractor.

Thus, option (D) is incorrect.

Hence, the correct option is (A).

45. (A)

Given MUX circuit is shown below,



Output S_1 of the 1st stage is given by,

$$S_1 = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + ABI_3$$

Here, $I_0 = I_3 = 0$

and $I_1 = I_2 = 1$

Hence, $S_1 = \bar{A}\bar{B} \cdot 0 + \bar{A}B \cdot 1 + A\bar{B} \cdot 1 + AB \cdot 0$

$$S_1 = \bar{A}B + A\bar{B}$$

$$S_1 = A \oplus B$$

Output X of the 2nd stage is given by

$$X = \bar{S}_1\bar{S}_0I_0 + \bar{S}_1S_0I_1 + S_1\bar{S}_0I_2 + S_1S_0I_3$$

Here, $I_0 = I_3 = 0$

$$I_1 = I_2 = 1 \text{ and } S_1 = A \oplus B, S_0 = C$$

$$\begin{aligned} \text{Hence, } X &= (\overline{A \oplus B})\bar{C} \cdot 0 + (\overline{A \oplus B}) \cdot C \cdot 1 \\ &\quad + (A \oplus B)\bar{C} \cdot 1 + (A \oplus B)C \cdot 0 \end{aligned}$$

III. I/P of Binary to seven segment display

$$= 10$$

Which display '2'

Hence, the correct option is (B).

47. (C)

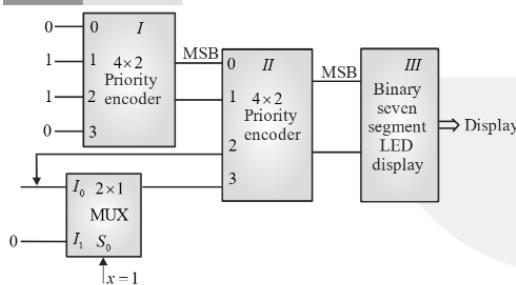
One inverter

SR flip flop

$$\begin{aligned}
 X &= (\overline{A \oplus B})C + (A \oplus B)\bar{C} \\
 X &= A \oplus B \oplus C = \Sigma m(1, 2, 4, 7) \\
 X &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC
 \end{aligned}$$

Hence, the correct option is (A).

46. (B)



I. Priority Encoder

$$B_1 B_0 \rightarrow O/Ps \text{ having } B_1 \text{ as MSB.}$$

$$\begin{aligned}
 B_1 &= I_1 I_0 (I_2 \oplus I_3) \\
 &= 0.1 (I \oplus 0) = 0
 \end{aligned}$$

$$\begin{aligned}
 B_0 &= I_0' I_2' (I_1 \oplus I_3) \\
 &= 1.0 (1 \oplus 0)
 \end{aligned}$$

MSB(B_1) = 0 $\rightarrow I_0$ of IInd P. Encode

$B_0 = 0 \rightarrow I_1$ of II P. Encode

MUX

$$\begin{aligned}
 y &= \bar{S}_0 I_0 + S_1 I_1 \\
 &= 0.1 + 1.0 = 0 \\
 &= y = 0 \rightarrow I_3 \text{ of II}^{\text{nd}} \text{ P. Encode}
 \end{aligned}$$

$I_0 = 1.7$ MUX $\rightarrow I_2$ of IInd P. Encode

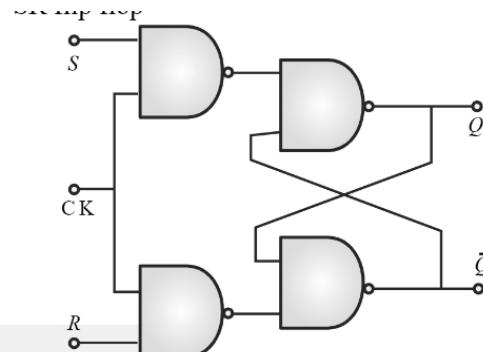
II. P. Encoder

$$P_1 = I_1' I_0' (I_2 \oplus I_3) = 1.1 (1 \oplus 0) = 1$$

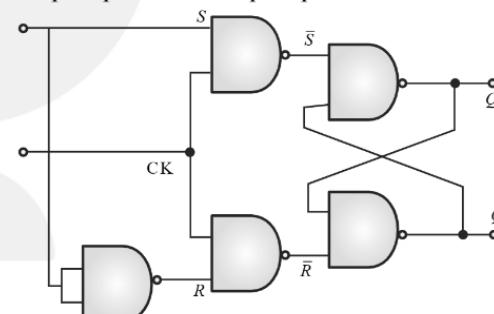
$$P_0 = I_1' I_2' (I_1 \oplus I_3) = 0$$

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Digital Logic



D flip flop from SR flip flop



48. (D)

Dividing pulse train by 2 means making period of pulse double or making frequency as half. This can be done if JK flip flop works in toggle mode ($J = 1$ and $K = 1$) and flip flop should be negative edge triggered so output changes only on negative transition of pulse.

So, option (D) is answer.

49. (C)

In Johnson counter if you have n number of flip flop then we have $2N$ state. So it is also known as mod $2N$ counter.

Q_A	Q_B	Q_C	Q_D
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1

$$= A_3 A_2 A_1 A_0 = 1010.$$

Hence, the correct option is (C).

52. 100

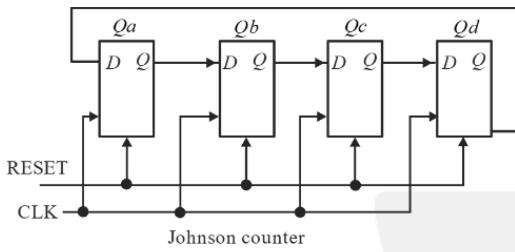
Given : Modulo, $M = 1024$

$$f_{clock} = 1 \text{ MHz}$$

For Ripple counter, $M = 2^n$

where, $M = \text{Modulo of counter}$

0	0	0	1
Repeat			

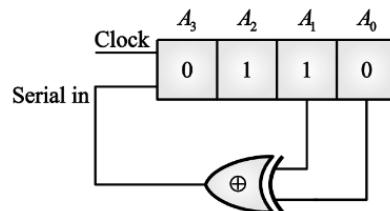


50. (B)

The count goes from 5 to 14 and then as soon as we get 15 preset occurs so 15 will not be considered as output as preset occurs and output becomes 5 and then again it goes from 5 to 14. So, it is mod 10 counter (option B).

51. (C)

Given : 4 bit serial in parallel out right shift, shift register is shown below,



Clock	$A_3 = A_1 \oplus B_0$	A_3	A_2	A_1	A_0
0 (initial)	1	0	1	1	1
1	0	1	0	1	1
2	1	0	1	0	1
3	1	1	0	1	0

Content of shift register after 3-clock pulse

n = Number of flip flops

Hence, $n = \log_2 M$

$$n = \log_2(1024)$$

$$n = \log_2 2^{10}$$

$$n = 10$$

Propagation delay of a ripple counter is given by,

$$t_{pd} = \frac{1}{n f_{clock}}$$

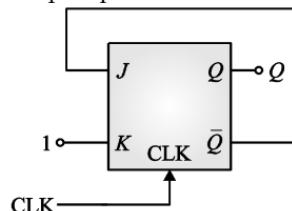
$$t_{pd} = \frac{1}{10 \times 10^6} = 10^{-7} \text{ sec}$$

$$t_{pd} = 100 \text{ ns}$$

Hence, the maximum permissible propagation delay per flip flop stage is **100 nsec**.

53. (D)

J-K flip flop is shown below,



State table for input and output of above J-K flip-flop are shown below,

CLK	Input		Output Q
	$J = \bar{Q}$	$K = 1$	
0	-	-	0 [initially]
1	1	1	1
2	0	1	0



3	1	1	1
4	0	1	0
5	1	1	1
6	0	1	0
7	1	1	1

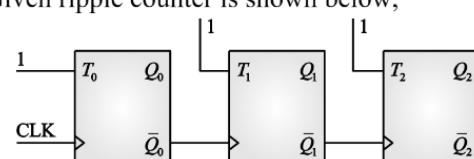
Thus, the sequence is 010101 and output waveform is shown below,



Hence, the correct option is (D).

55. (B)

Given ripple counter is shown below,



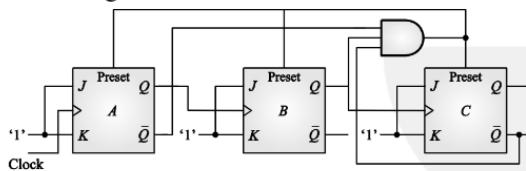
Given : $Q_2 Q_1 Q_0 = 011 \rightarrow$ Initial state

It is a ripple counter with positive edge triggered and output of \bar{Q} is connected to clock of next

(The arrangement of JK-flip-flop given in question work as alternate 1 and 0 generator.)

54. (D)

Given logic circuit is shown below,



From the above circuit we can observe :

- (1) The flip flops are positive edge triggered, and the output Q of one flip flop acts as clock input for next flip flop hence, it is a down counter.
- (2) The output of the AND gate is connected to preset input,

Preset is 1 only when $\bar{C}B\bar{A}=1$ (i.e. $C=0, B=1, A=0$)

C B A CLK

C	B	A	CLK	State
1	1	1	1	1
1	1	0	2	1
1	0	1	3	0
1	0	0	4	0
0	1	1	5	0
0	1	0	6	1
1	1	1		1

(At this point preset = 1 and counter preset to 111)

Hence, the given circuit is a MOD-5 down counter.

Hence, the correct option is (D).

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Digital Logic

Q flip-flop. Hence, it is an up-counter.

$$\begin{array}{ccccccc} Q_2 & Q_1 & Q_0 & \xrightarrow{\text{Nextstate}} & Q_2 & Q_1 & Q_0 \\ 0 & 1 & 1 & & 1 & 0 & 0 \end{array}$$

(3) (4)

Hence, the correct option is (B).

56. (A)

Count sequence for synchronous counter is given by,

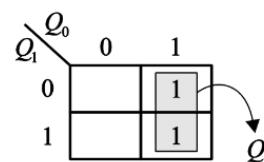


State table for above sequence is shown below,

Present state		Next state		Inputs	
Q_1	Q_0	Q'_1	Q'_0	D_1	D_0
0	0	0	1	0	1
0	1	1	1	1	1
1	1	1	0	1	0
1	0	0	0	0	0

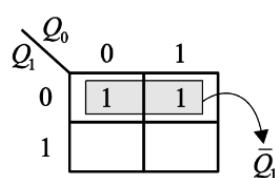
(Inputs D_1 and D_0 are sets according to the excitation table of D-flip-flop).

K-map for D_1 is shown below,



Hence, $D_1 = Q_0$

K-map for D_0 is shown below,



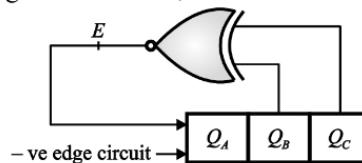
Thus, $D_0 = \bar{Q}_1$

Hence, the correct option is (A).

57. (A)

Given circuit is 2-bit synchronous sequential circuit as shown below,

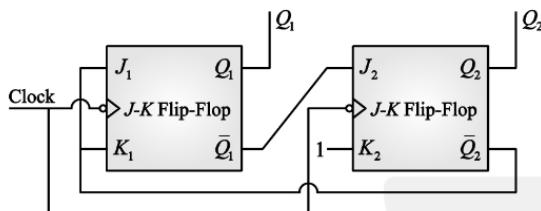
Given circuit is a 3-bit synchronous sequential circuit, with D-flip-flop are connected in cascaded manner so circuit can be reduced into shift register format as,



(Initially $Q_A Q_B Q_C = 000$)

So, state table formed as,

CLK	E = 0	Q ⁻	Q ⁺	Q ⁻	Q ⁺
0	0	000	000	000	000
1	0	000	000	000	000
0	1	000	000	000	000



State table for the given counter is shown below,

Present state		Inputs				CP	Next states	
Q_1	Q_2	$J_1 = \bar{Q}_2$	$K_1 = \bar{Q}_2$	$J_2 = \bar{Q}_1$	$K_2 = 1$		Q_1^+	Q_2^+
0	0	1	1	1	1	↑	1	1
1	1	0	0	0	1	↑	1	0
1	0	1	1	0	1	↑	0	0
0	0	1	1	1	1	↑	1	1

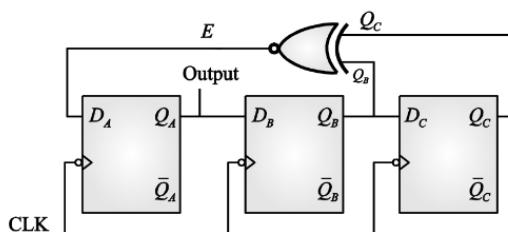
Thus, the count sequence ($Q_1 Q_2$) is

11, 10, 00, 11, 10...

Hence, the correct option is (A).

58. (D)

Given logic circuit is shown below,



CLR	$\Sigma = \Sigma_B \cup \Sigma_C$	Σ_A	Σ_B	Σ_C
0	-	0	0	0
1	1 → 1	0	0	0
2	1 → 1	1	0	0
3	0 → 0	1	1	1
4	1 → 1	0	1	1
5	0 → 0	1	1	0
6	0 → 0	0	0	1
7	0 → 0	0	0	0

So, count of (Q_A^+) → 01101000.....

Hence, the correct option is (D).

59. (A)

Given counter is asynchronous counter with negative edge triggering.

Q is applied as negative edge triggering clock.

Hence it is an up counter.

Reset signal = $\overline{Q_2 Q_0}$

Q_2	Q_1	Q_0	Reset = $\overline{Q_2 Q_0}$
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
0	0	0	0

Counter resets at 101 hence, it is a MOD-5 counter.

Hence, the correct option is (A).

60. (C)

61. (C,D)

Any function is self dual function if its complement is always self dual.

(0.7)(1,6)(2,5)(3,4) are the pairs for self dual

Option (A) is false because here no element for pair (1, 6)

Option (B) (0,7) and (1,6) are both appeared

$$X \geq 8 \& Y \leq 9$$

Because if number is 7 then minimum possible base is 8

Similarly if base is 10 then maximum possible number is 9

So we solve these two equations.

$$(57)x = (Y7)_{10}$$

$$5 \times X^1 + 7 \times X^0 = Y \times 10^1 + 7 \times 10^0$$

$$5X + 7 = 10Y + 7$$

$$5X = 10Y$$

$$X = 2Y \quad \dots(i)$$

is $Y = 1 \ X = 2$ - False because $(X > 8)$

in a single pair so it is also false

Option (C) True :- Because $\{0, 1, 2, 4\}$ all are appeared in a different pair

Option (D) True: Because $\{3, 5, 6, 7\}$ all are appeared in different pair

62. (B)

$A = (765)_8$ is 111110101 in binary note that most significant bit in the binary representation is 1, which implies that the number is negative. To get the actual value of the number perform the 2's complement of the number we get A as -11

$$(765)_8 = 111110101$$

↓

2's complement 000001011 = -11

And $6 \times A$ is $= -11 \times 6 = -66$

Since 6 A is also negative we need to find 2's compliment of it (-66) binary representation of $66 = 001000010$ 2's compliment of $66 = -66 = 110111110 = (676)_8$

So the correct option is B

63. 6

$$(57)_X = (Y7)_{10}$$

According to the number system concept

26

Digital Logic

Clock status	Output states			Inputs		
	Q_2	Q_1	Q_0	D_2	D_1	D_0
	0	0	0			
After 1 st clock pulse	0	0	1	0	0	1
After 2 nd clock pulse	0	1	1	0	1	1
After 3 rd	1	1	1	1	1	1

is $Y = 2, X = 4$ - False because ($X \geq 8$)

is $Y = 3, X = 6$ - False because ($X \geq 8$)

is $Y = 4, X = 8$ - True

is $Y = 5, X = 10$ - True

is $Y = 6, X = 12$ - True

is $Y = 7, X = 14$ - True

is $Y = 8, X = 16$ - True

is $Y = 9, X = 18$ - True

is $Y = 10, X = 20$ -

False because ($Y \leq 9$)

So total 6 cases are possible

64. (B)

In the above diagram,

We know that initially all flip flop are reset and $Q_{n+1} = D$ that means if D is one than Q is also 1 in below table.

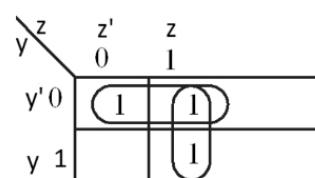
Q_2 is MSB & Q_0 is LSB

$$D_2 = Q_1$$

$$D_1 = Q_0$$

& $D_0 = \overline{Q_1 Q_2}$ or Q_1 NAND Q_2 we know that

$Q_{n+1} = D$ that means is D is one then Q_1 is initially all flip flop are reset



$$I_1 = y' + z$$

$$I_2 = z' \text{ (Given in question)}$$

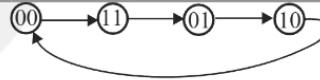
$$I_3 = y'z' + yz = y \oplus z$$

Present state	Flip flop Inputs		Next states			
	Q_0	Q_1	$D_0 = \bar{Q}_0$	$D_1 = Q_0 \oplus \bar{Q}_1$ $= Q_0 \odot Q_1$	Q_0^+	Q_1^+
Q_0						

clock pulse						
After 4 th clock pulse	1	1	0	1	1	0

Correct option is B

0	0	1	1	1	1
1	1	0	1	0	1
0	1	1	0	1	0
1	0	0	0	0	0



Hence, the correct option is (C).



65. (C)

We have 4 variables (w, x, y, z) here $w \& x$ are selection line so $y \& z$ are inputs and the function is $=\sum m(4, 5, 7, 8, 10, 12, 15)$

So 4:1 mux table are

	$W'X'$	$W'X$	WX'	WX
	00	01	10	11
	I_0	I_1	I_2	I_3
$y'z' 00$	0	(4)	(8)	(12)
$y'z 01$	1	(5)	9	13
$yz' 10$	2	6	(10)	14
$yz 11$	3	(7)	11	(15)

Lecture 02 (Combinational Logic Circuits)

