Branch : CSE & IT **Batch : Hinglish**

Computer Organization and Architecture

Introduction to COA

DPP

1. [MCQ]

Consider 64 bit hypothetical CPU which support 256 KB memory space processer is enhanced with word addressable memory. How many address pins are saved in enhanced CPU to refer the memory?

(a) 1 (b) 2

(c) 3 (d) 4

2. [MCQ]

How many 128×8 bit RAMs are required to design 32K × 32 bit RAM ?

(a) 512 (b) 1024

(c) 128 (d) 32

3. [MCQ]

Consider 32 bits hypothetical CPU which supports word addressable memory used to execute the following code. The code starting address is 2000.

Instruction	**Size in bytes**
I_1	16
I_2	12
I_3	16
I_4	12
I_5	8
I_6	8

During the execution of I_4 Instruction what would be the value present in the program counter (PC).

(a) 2011 (b) 2013

(c) 2014 (d) 2018

4. [MCQ]

Match the column I with column II and select the correct answer.

	Column -I		Column -II
A.	Program counter (PC)	(i)	Contain the instruction currently being executed by CPU
B.	Memory Address Register (MAR)	(ii)	That contain temporary result or first operand of ALU operation
C.	Instruction Register (IR)	(iii)	Contain the starting address of the next instruction to be fetch.
D.	Accumulator (AC)	(iv)	Contain the address of memory location used for either read or write operation.

(a) A- (iii) B-(i) C – (iv) D-(ii)

(b) A- (iii) B-(iv) C – (ii) D-(i)

(c) A- (ii) B-(iv) C – (i) D-(iii)

(d) A- (iii) B-(iv) C – (i) D-(ii)

5. [MCQ]

What does the following program produce when run on an 8085 microprocessor ?

```
LDA   8000 H (Load)
MVI   B, 30 H
ADD   B
STA   8001 H (Store)
```

(a) Read a number from input port and store it in memory.

(b) Read a number from input device with address 8000H and store it in memory at location.

(c) Read a number from memory at location 8000H and store it in memory location 8001H.

(d) None of these

6. [MCQ]

Consider 64 bits hypothetical CPU which supports byte addressable memory used to execute the following code. The code starting address is 1000.

Instruction	Size of bytes
I_1	2
I_2	4
I_3	4
I_4	4
I_5	2
I_6	6

During the execution of I_5 Instruction. What would be the value present is the program counter (PC).

(a) 1014 (b) 1015

(c) 1016 (d) 1021

7. [NAT]

To execute a program, instructions has to be brought from memory using bus to CPU. If the bus has 8 lines then almost one 8-bit (1byte) can be transferred at a time.

The how many memory access are required in this cases to transfer a 32 bit instruction from memory to the CPU?

8. [MCQ]

Consider the statements

S_1: In little endian, lower address contain lower byte and higher address contain higher byte.

S_2: In big Endian, lower address contain higher byte and higher address contain lower byte.

(a) Only S_1 is true

(b) Only S_2 is true

(c) Both S_1 & S_2 are true

(d) Neither S_1 nor S_2 is true.

9. [MCQ]

Consider the statements

S_1: Accumulator Stores the results of calculations made by ALU.

S_2: Program counter keeps track of the memory location of the current instruction by which process is currently dealing with.

(a) Only S_1 is true

(b) Only S_2 is true

(c) Both S_1 & S_2 are true

(d) Neither S_1 nor S_2 is true.

10. [MSQ]

Which of the statements is/are true?

(a) Memory address register stores the memory locations in instruction that needed to be fetched from memory.

(b) Memory data register stores the instruction fetched from memory or any data that is to be transferred to and stored in memory.

(c) Instruction register stores the most recently fetched instruction.

(d) Instructions buffer register contains the instruction which are not to be executed immediately.

Answer Key

1. **(c)**
2. **(b)**
3. **(c)**
4. **(d)**
5. **(c)**
6. **(c)**
7. **(4 to 4)**
8. **(c)**
9. **(a)**
10. **(a,b,c,d)**

Hints & Solutions

1. (c)

By default memory is byte addressable

Memory space = 256 KB

$= 2^{18}$ Bytes

$\boxed{\text{Address pins} = 18}$

In enhanced processor

Word size = 64 bit

Memory space = 256 × k × 8 bits

$= 2^{15} \times 64$ bits

$\boxed{\text{Address pins} = 15}$

Saved address pins = 18 – 15

= 3

2. (b)

$$\text{Number of RAMS required} = \frac{32k \times 32 \text{bits}}{128 \times 8 \text{ bits}}$$

$$= \frac{2^{15} \times 2^5}{2^7 \times 2^3} = 2^{10} = 1024$$

3. (c)

Word size = 32 bits

= 4 bytes

= 1 w

Instruction	Size in bytes
I_1	16 (4w) 2000 – 2003
I_2	12 (3w) 2004 – 2006
I_3	16 (4w) 2007 – 2010
I_4	12 (3w) 2011 – 2013
I_5	8 (2w) $\boxed{2014}$ – 2015
I_6	8 (2w) 2016 – 2017
	2018

During the execution of I_4 instruction program counter will hold the address I_5 Instruction.

Ans = 2014

4. (d)

A → (iii) B → (iv)

C → (i) D → (ii)

5. (c)

The given program will read a number from memory at location 8000H and store it in memory location 8001 H.

6. (c)

Memory is byte addressable!

Instruction	Size in bytes
I_1	2 1000 – 1001
I_2	4 1002 – 1005
I_3	4 1006 – 1009
I_4	4 1010 – 1013
I_5	2 1014 – 1015
I_6	6 $\boxed{1016}$ – 1021

During the execution of I_5 instruction the program counter will hold the start address of I_6 instruction.

$\boxed{\text{Ans.} = 1016}$

7. (4)

As me have 8 data lines in dataline, at a point of time or in a cycle, 8 bits data can be transferred, So if we want to access 32 bits then $\frac{32}{8} = 4$ cycles are required so 4 memory access.

8. (c)

Both the given statement are true about memory address interpretation.

9. (a)

S_1 (True): Accumulators stores the results of calculations made by ALU.

S_2(False): Program counter keeps track of the memory location of the next instruction to be deals with but not the current instruction.

10. (a, b, c, d)

(a) **True:** Memory address stores the memory location of instruction that are needed to be fetched from memory.

(b) **True:** Memory data register stores the instruction fetched from memory or any data that is to be transferred to and stored in memory.

(c) **True:** Current instruction register stores the most recently fetched instructions.

(d) **True:** Instruction buffer register contains the instructions which are not to executed immediately.

❐❐❐

Branch : CSE & IT Batch : Hinglish

Computer Organization and Architecture

ALU and Control Unit

DPP

1. [MCQ]

The sequence of events that happiness during typical fetch operation is-

(a) PC → MAR → Memory →MDR → IR

(b) PC → Memory →MDR → IR

(c) PC → Memory → IR

(d) PC → MAR → Memory → IR

2. [MCQ]

Which set of instruction transfer the memory word specified by the effective address to AC or Load to AC?

(a) DR ←[MAR]
AC ←AC + DR , E← Cout, SC ← O

(b) DR ← [MAR]
AC ← DR, SC ← O

(c) [MAR] ← AC, SC ← O

(d) DR ← [MAR]
AC ← AC^ DR, SC ←O

3. [MCQ]

Consider a CPU with 128 instructions in the instruction set, where each operation needs 8 cycles. If 60 control signals needed to be generated by the control unit. If signal address field format is used then what is the minimum size of the control word, if horizontal micro programming is used for control unit?

(a) 128 (b) 67

(c) 17 (d) 70

4. [NAT]

Consider a single address field format is used for branch control logic. Assume that the control word is 64 bits wide. The control portion of the micro instruction format is divided in two field.

A micro-operation field of 24 bits specified the micro-operations to be performed. An address selection field specifies a condition, based on the flags, that will cause a micro-instruction branch. There are 16 flags. How many bits are there in address bits?

5. [MCQ]

Which of the following statement is false about CISC architecture?

(a) CISC machine instructions may include complex addressing modes, which requires many clock cycles to carry out.

(b) CISC control unit are typically micro programmed allowing the instruction set to be more flexible.

(c) In the CISC instruction set, all arithmetic/logic instruction must be register based.

(d) None of the above.

[MCQ]

6. Which of the following is the micro program of indirect operand fetch cycle?

(a) t_1 : MAR ← IR [Address]
t_2 : MBR ← M [MAR]
t_3 : AC ← MBR

(b) t_1 : MAR ← (PC)
t_2 : MBR ← Memory
PC ← (PC) + 1
t_3 : IR ← MBR

(c) t_1 : MAR ← (IR (Address)
t_2 : MBR ← Memory
t_3 : MAR ← MBR
t_4 : MBR ← Memory
t_5 : Accumulator ← MBR

(d) None of the above

7. [NAT]

For the operand fetch using indirect addressing mode, how many number of cycles are required to bring the operand in the CPU?

8. [NAT]

Consider a micro-programmed control unit design which supports 7 groups of mutually exclusive control signals.

Groups	Gr1	Gr2	Gr3	Gr4	Gr5	Gr6	Gr7
Control Signals	2	10	4	1	18	23	6

How many more control bits are required using horizontal micro-programming over vertical micro-programming?

9. [MCQ]

Consider a hypothetical control unit, which supports 512 bytes of control word memory. If the control word is 20 bits long and hardware contains 4 flags and supports 16 branch conditions, what is the maximum number of control signals that can be generated at a time using horizontal micro-programming and vertical micro-programming respectively?

(a) 1,1 (b) 32,32

(c) 32, 1 (d) 1, 32

10. [MCQ]

Vertical micro-programming, horizontal micro-programming and hardwired control are used for control unit design. Which among them has highest and lowest operational speed respectively?

(a) Highest: Hardwired control

(b) Highest: Vertical micro-programming

(c) Lowest: Vertical micro-programming

(d) Lowest: Horizontal micro-programming

Answer Key

1. **(a)**
2. **(b)**
3. **(d)**
4. **(36 to 36)**
5. **(c)**
6. **(c)**
7. **(4)**
8. **(43)**
9. **(c)**
10. **(**a, c**)**

Hints & Solutions

1. (a)

Mirco – operation of fetch instruction:

1. PC→ MAR
2. [MAR]→ MBR
   PC + 1 → PC
3. [MBR] → IR

2. (b)

LDA AC load to AC instruction transfer the memory word specified by the effective address to AC

T_1: MDR ← [MAR]

T_2: AC ← MDR, SC ← O

3. (d)

Total number of cycles = 128 inst. × 8 cycles
= 2^{10} cycles.

Or we can say

Total number of micro-operations = 2^{10}

Bits needed for addressing control memory = $\log 2^{10}$ = 10

Minimum size of control word = 60 + 10 = 70

4. (36 to 36)

In a single address field, the option for next address are as follows:

1. Address field.
2. Instruction register code.
3. Next sequential address.

The address-selection signals determine which option is selected. The approach reduces the number of address field to one.

There are total 16 flags. Hence 4 bits are needed in the address selection bit.

64 – (24 + 4) = 36 bits are needed in the address field.

5. (c)

In RISC instruction set all arithmetic/logic must be register based but not in CISC.

6. (c)

Mirco program of indirect operand fetch cycle:

t_1 : MAR ← (IR Address)

t_2 : MBR ← Memory

t_3 : MAR ← MBR

t_4 : MBR ← Memory

t_5 : Accumulator ← MBR

7. (4)

The microprogram for operand fetch using indirect addressing mode is as follows:

t_1 : MAR ← IR [Address]

t_2: MBR ← Memory

Thus, in these two cycles effective address i.e., the address of the operand is brought to the CPU.

t_3 : MAR ← MBR

t_4: MBR ← Memory

These, two cycles are required to bring operand from memory to the CPU.

So, total 4 cycles are required.

8. (43)

For vertical Micro programming:

Micro-Instruction format:

Gr1	Gr2	Gr3	Gr4	Gr5	Gr6	Gr7
$\log_2 2$	$\log_2 10$	$\log_2 4$	$\log_2 1$	$\log_2 18$	$\log_2 23$	$\log_2 6$

Total control bits required = 1 + 4 + 2 + 1 + 5 + 5 + 3.
= 21 bits

[For horizontal micro-programming]

Micro instruction format:

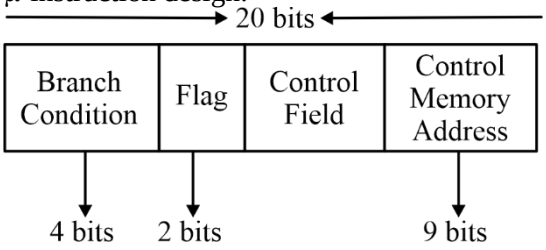
Gr1	Gr2	Gr3	Gr4	Gr5	Gr6	Gr7
2	10	4	1	18	23	6

Total bits required = 2 + 10 + 4+1+18 + 23 + 6
= 64 bits

So, horizontal micro programming requires, 64-21 = 43, more bits.

9. (c)

μ-instruction design:



Control word memory = 512 bytes

So, control memory address field require = 9 bits

Number of flags = 4

So, number of flag bits required = 2

Number of branch conditions = 16

So, number of branch condition bits required = 4

Number of bits required for control field = 20 - (4 + 2 + 9) = 5

Therefore, number of control signals that can be generated = 25 = 32 In Horizontal micro-programming for each control signal 1 bit is there, So, all control signals can be activated at a time.

∴ Maximum degree of parallelism for horizontal microprogramming = 32

∴ In vertical microprogramming only 1 control signal can be activated at a time.

∴ Maximum degree of parallelism for vertical micro-programming = 1

∴ Option (c) is correct.

10. (a, c**)**

Highest: hardwired control

Lowest: vertical micro-programming.

- In hardwired, control logic is implemented using gates and flipflops. So, it is fastest.
- In horizontal microprogramming for each control signal a separate bit is used.
- In vertical microprogramming, control signals are expressed in form of encoded binary format.

Thus, a decoder is used.

So, for 'n' control signals log bits are used so it has slowest operational speed.

Branch : CSE & IT Batch - (Hinglish)

Computer Organisation and Architecture

Cache Memory

DPP

[MCQ]

1. Consider a processor that can support a maximum memory of 8GB, where the memory is word-addressable (a word consists of 2 bytes). Then the size of the address bus of the processor is at least _____bits.

(a) 31 (b) 32
(c) 33 (d) 34

[NAT]

2. Assume a direct mapped cache having 8 cache lines, each cache line consists of 2 words and each word is of one byte. The address bus consists of 7 bits, then the tag field of the cache consists of _____ bits.

[NAT]

3. Assume a 32-bit addressable physical memory and 2 MB cache block of size 8 kB each, then how many bits are required in the tag field of the cache address if the cache is 4-way set associative _____

[MCQ]

4. Consider a 16-Kbyte cache with the following features, each block will hold 32 bytes of data (not including tag, valid, etc …), The cache would be 2-way set associative, physical addresses are 32 bits and data is addressed to the word and words are of 32 bits long. Then how many blocks would be in this cache and how many bits of tag are stored with each block entry?

(a) 512, 19 (b) 512,22
(c) 256, 20 (d) 512, 21

[MCQ]

5. Consider a 16 KB, two-way associative cache with 32-Byte cache line and a 64 bits address space, there will be p bits used for index. Let suppose if that same cache were fully associative, you need q bits to be used for the index then the value for p + q = _____.

(a) 6 (b) 7
(c) 8 (d) 9

[NAT]

6. Consider a system having 512KB, 16-way set associative L_2 cache with a 128 byte cache line size, Then how many cache lines are present? ____

[NAT]

7. Assume a cache with 32-bit address, 768 blocks and a block size of 128 bytes, tags are 17 bits then what is the associativity of the cache_____?

[MCQ]

8. Assume a direct mapped cache memory with 16 cache block (0 – 15) and a main memory having 256 blocks (0 to 255). Assume that, initially the cache did not have any memory block, Consider the following sequence of memory block references:
3, 180, 43, 2, 191, 881, 190, 14, 181, 44, 186 and 253, Then which memory blocks will be present in the cache after the above sequence of memory block reference?

(a) 2,3, 180, 43, 2, 191, 190, 88, 14, 181, 44, 186
(b) 2,3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 181, 44, 186, 253
(c) 2, 3, 180, 181, 881, 186, 43, 44, 253, 14, 191
(d) None of the above

[MCQ]

9. Assume the access patterns x, y, z, y, x where each letter corresponds to a unique cache block and also assume that there was no access to any block before this and all conflicts are random. Then what is the probability of the second access to x being a hit on a direct mapped cache with 4 line (closet to)?

(a) 40% (b) 50%
(c) 80% (d) 100%

[MCQ]

10. Which one is the fastest cache mapping function among the following?

(a) Fully associative mapping
(b) Set associative mapping
(c) Direct mapping
(d) None of these

[MCQ]

11. Suppose a cache has 70% hit ratio, an access time of 50 ns on a cache hit and an access time of 120 ns on a cache miss then what is the effective access time_____(using hierarchical memory)

(a) 90 ns (b) 92ns
(c) 86 ns (d) 96ns

[MCQ]

12. Suppose local hit rate for L_1 cache is 20% and the local hit rate for L_2 cache is also 30%. The hit time for the L_1 cache is 8 cycle, the hit time for L_2 cache is 20 cycles and access time for main memory is 30 cycles then what is average memory access time in cycle? (approximately)

(a) 41 (b) 45
(c) 46 (d) 44

[MSQ]

13. Choose the correct statements from the following.

(a) Instruction, and data stored in cache are regularly used by the CPU, if data not present in cache then it always transfers from main memory.
(b) Data is stored on temporary basis in cache memory.
(c) Programs stored in cache takes more time to execute.
(d) Cache memory has limited capacity.

[MCQ]

14. Consider the following statements.

S_1: If size of the block is increased then compulsory misses can be reduced.

S_2 : If associativity of cache is increased then that can lead to increasing conflict misses.

(a) only S_1 is true
(b) only S_2 is true
(c) both S_1 and S_2 are true
(d) neither S_1 nor S_2 is true

[NAT]

15. Consider a 128 word cache and the main memory is divided into 32 word blocks. The main memory access time is 50 μs / word and the cache access time is 20 μs/word. The hit ratio for read operation is 80% and for the write operation is 90%. Whenever a cache miss happens, associated block must be the brought from main memory to cache for both read and write operation. Let there be 40% references for write operations. If the write back updation policy is used and at any point of time 80% cache blocks are modified, then what is the T_{avg}? (upto 1 decimal in μ sec)

[NAT]

16. A 16-way set associative cache of size 128KB is used in a system with 32-bit address. For such cache memory, the memory size is ___. (in Kbytes) Provided block size is 4 bytes.

Answer Key

1. **(b)**
2. **(3)**
3. **(13)**
4. **(a)**
5. **(c)**
6. **(4096)**
7. **(3)**
8. **(c)**
9. **(d)**
10. **(a)**
11. **(c)**
12. **(a)**
13. **(b, d)**
14. **(a)**
15. **(481)**
16. **(76)**

Hints & Solutions

1. (b)

8GB

$2^3 \times$ GB

$2^3 \times 2^{30} / 2^1$

↓

32 address lines

2. (3)

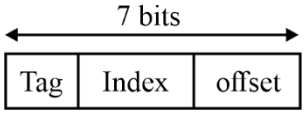
8 cache lines = 2^3 cache lines

$\therefore$ 3 bits for index

As given 1 line = 2 words = 2 bytes

$\therefore$ 1 bit for offset

Address size = 7 bits



Tag bits = 7 – 3 – 1 = 3 bits

3. (13)

$$\text{Number of lines in cache} = \frac{\text{cache size}}{\text{block size}}$$

$$= \frac{2 \times 2^{20}}{8 \times 2^{10}} = 2^8$$

$$\text{Number of sets in cache} = \frac{2^8}{4 - \text{way of associativity}}$$

$$= \frac{2^8}{2^2} = 2^6$$

$\therefore$ 6 bits for index

Block size = 2^{13}, means 13 bits are required for offset.

Tag bits = 32 – 6 – 13 = 13 bits.

4. (a)

Cache size = 2^{14} bytes

Block size = 2^5 bytes

$$\text{Word size} = \frac{32}{8}\text{ bytes} = 4 \text{ bytes} = 2^2 \text{ bytes}$$

$$\text{Number of lines} = \frac{\text{cache size}}{\text{block size}} \quad \frac{2^{14}}{2^5} = 2^9 = 512 \text{ blocks}$$

Now, Tag bits

As 2^9 lines are in cache and cache is 2-way set associative.

$2^8 = 8$ bits for a set.

Tag bits = PA – (index + offset)

= 32 – (8 + 5)

= 19 bits.

5. (c)

Cache size = 2^{14} bytes

Line size = 2^5 bytes

$$\text{Lines} = \frac{2^{14}}{2^5} = 2^9 \text{ lines}$$

2-way set associative cache = 2^8 sets.

8 bits for index = p

As index bits in fully associative = 0 = q

$\therefore$ p + q = 8 + 0 $\Rightarrow$ 8 which is option (c).

6. (4096)

Cache size = 512×2^{10} bytes = 2^{19} bytes

Cache line size = 2^7 bytes

$$\text{Number of lines} = \frac{512 \times 2^{10}}{2^7} = 2^9 \times 2^3$$

$= 2^9 \times 2^3$

$= 2^{12}$

= 4096.

7. (3)

Tag= 17 bits.

Block size = 2^7 bytes

7 bits for offset field.

Index bits = 32- (17 + 7) = 8

2^8 sets = 256 blocks

Total 768 block, therefore $\Rightarrow \frac{768}{256}$ = 3 way set associative.

8. (c)

Number of blocks = Memory address block mod number of blocks

	0
881	1
2	2
3	3
180	4
181	5
	6
	7
	8
	9
186	10
43	11
44	12
253	13
~~190~~ 14	14
191	15

8 mod 16 = 8
180 mod 16 = 4
43 mod 16 = 11
4 mod 16 = 4
191 mod 16 = 15
881 mod 16 = 1
190 mod 16 = 14
14 mod 16 = 14
181 mod 16 = 5
44 mod 16 = 12
186 mod 16 = 10
253 mod 16 = 13
Blocks present in cache after execution of sequence of jobs are:
2, 3, 180, 181, 881, 186, 43, 44, 253, 14, 191
$\therefore$ option (c) is correct.

9. (d)

x, y, z all of the of them corresponds to unique cache block, if they come in different block and we have 4 cache blocks in the cache.

x
y
z

The probability of hit on second accesses is 1 which is 100%.

10. (a)

In associative mapping both the address and data of the memory word are stored. The associative mapping method used by cache memory is very fast as well as flexible.

11. (c)

Effective access time = cache hit × cache access time + cache miss (cache access + mm access)
= 0.70(50) + 0.30(50 + 120)
= 35 + 51 = 86ns.

12. (a)

$AMAT = (L_{1H}T + (L_{1M}R \times (L_{2H}T + (L_{2M}R \times MEM))))$
$= 8 + (0.8 \times (20 + (0.7 \times 30))$
$= 8 + 0.8\ (20 + 21)$
$= \lceil 40.8 \rceil = 41$

13. (b, d)

(a): Instruction, and data stored in cache are regularly used by the CPU, if data not present in cache then it always transfers from main memory. **False**

b: Data is stored on temporary basis in cache memory. **True**

c: Programs stored in cache takes less time to execute. **False**

d: Cache memory has limited capacity. **True**

14. (a)

S_1 (True): Compulsory misses can be reduced by increasing the line size.

S_2 (False): Increasing the associativity decreases conflict misses.

15. (481)

Here dirty bit signifies the modified bit.

$T_{avgR} = h_r \times t_c + (1 - h_r)$ [% dirty bit $(t_m + t_c + t_m)$ + % clean bit $(t_m + t_c)$]

$\Rightarrow 0.8 \times 20 + 0.2\ (0.8\ (1600 + 20 + 1600) + .02\ (1600 + 20))$

$\Rightarrow 16 + 0.2 \times 2900$

$16 + 580$

$\Rightarrow 596$

$T_{avgW} = h_w \times t_c + (1 - h_w)$ [% dirty bit $(t_m + t_c + t_m)$ + % clean bit $(t_m + t_c)$]

$\Rightarrow 0.9 \times 20 + (0.1)\ (0.8\ (1600 + 20 + 1600) + 0.2\ (1600 + 20))$

$\Rightarrow 18 + 0.1 \times 2900$

$\Rightarrow 308$

$T_{avg} \Rightarrow 0.6(596) + 0.4(308)$

$\Rightarrow 357.6 + 123.2$

$\Rightarrow 480.8 \cong 481$ µsec.

Note: main memory access time $\Rightarrow$ 32 words* 50µsec

$\Rightarrow 1600$ µsec.

16. (76)

Cache memory size = 128KB = 2^{17}B

Main memory size = 32 bits

P = 16-way set associative

The block size = 2^2 Bytes

Number of cache block = $\frac{2^{17}}{2^2} = 2^{15}$

Number of sets $\Rightarrow \frac{2^{15}}{2^4} = 2^{11}$

For set associative mapping technique:

Tag bits + set bits + block offset bits = main memory

$\Rightarrow$ Tag bits + 11 + 2 = 32 bits

Tag bits = 19 bits

Tag memory size = S*P* tag space line

$\Rightarrow 2^{11} * 2^4 * 19$ bits

$\Rightarrow 2^{15} * 19$ bits

$\Rightarrow$ 32K * 19 bits

$\Rightarrow$ 608 K bits

$\Rightarrow$ 76 KB.

Branch : CSE & IT **Batch : Hinglish**

Computer Organization and Architecture

Floating Point Representation

DPP

1. [NAT]

Consider the following 1EEE single precision floating point number shown below.

010000111101 0000 0000 0000 0000 0000

The decimal equivalued of above number is_____.

2. [MCQ]

Consider the hexadecimal representation in IEEE754 signal precision floating number system: 0X43758000. What is the decimal value represented by it?

(a) 245.5 (b) 244.5

(c) 240.5 (d) None of the above

3. [MCQ]

In IEEE 754 single precision floating point standard the number

1111 11111 0000 0000 0000 0000 0000 000 represents.

(a) NAN

(b) $-\infty$

(c) A negative normalized number

(d) None of the above

4. [MCQ]

Consider the following hexadecimal value in the IEEE 754 signal precision floating point number: 0XC4127000, then what is the value represented by it in decimal?

(a) (-585.75) (b) (-586.75)

(c) (–580.75) (d) None of these

5. [MCQ]

What is IEEE 754 32 bits floating point format representation of 16?

(a) 010 00011 0000 0000 0000 0000 0000 0000

(b) 011 000011 0000 0000 0000 0000 0000 000

(c) 0100000111 0000 0000 0000 0000 0000 000

(d) None of the above

6. [MCQ]

Consider the following binary value in 1EEE 754 signal precision floating point number representation.

0 10000111 1111010 0000 0000 0000 0000 what decimal value is it representing?

(a) 300 (b) 400

(c) 500 (d) None of these

Answer Key

1. **(416)**
2. **(a)**
3. **(b)**
4. **(a)**
5. **(a)**
6. **(c)**

Hints & Solutions

1. (416)

S	E	M
1 bit	8 bits	23 bits

0	10000111	101 0000 0000 0000 0000 0000

Value $= 1.M \times 2^{E-127}$
$= 1.1010 \times 2^{135-127}$
$= (1.1010)_2 \times 2^8$
$= (1.625 \times 2^8)$
$= (416)_{10}$

2. (a)

010000 110111 01011 00000 00000 00000
Actual exponent = stored – binary
= 134 – 127
= 7
$= 1.11\ 101011 \times 2^7$
$= 1.111\ 01\ 011 \times 2^7 \times 2^{-8}$
$= 1111\ 010111 \times 2^{-1}$
$= \frac{491}{2} = 245.5$

3. (b)

1	11111111	0000 0000……0
1bit	8bits	23bits
S	E	M

The value + ∞ and – ∞ are represented with an exponent of all ones and a mantissa of all zeros. The sign bit distinguishes between – ∞ and + ∞.

4. (a)

C4127000

1	10001000	00100100111 0000 0000 0000

Exponent = 136 – 127
Actual exponent = 9
So, the number will be $= -1.\ 00100100111 \times 2^9$
$= 100\ 1001\ 00111 \times 2^9 \times 2^{-11}$
$= -2343 \times 2^{-2}$
$= -585.75$
∴ (a) is correct option.

5. (a)

$(16)_{10} = (10000)_2$
$10000 = 1.0000 \times 2^4$
Exponent = 4
Mantissa = all zeros
Exponent stored = 4 + 127 (bias)
= 131

0 10000011 0000 0000 0000 0000 0000 000
Sign bit exponent mantissa

6. (c)

S	E	M
0	10000111	111101 0000 0000 0000 00000

Sign bit is + so it is 0
Exponent = 135 – 127
= 8
Mantissa = 1111101
$= 1.111101 \times 2^8$
$= (1.953125) \times 256$
$= 500$

❐❐❐

Branch : CSE & IT **Batch : Hinglish**

Computer Organization & Architecture
Instructions Pipelining

DPP

[NAT]

1. Consider a non-pipelined processor with 25 ns cycle time is divided into 5 stages with latencies of 5ns, 7ns, 3ns, 6ns and 4ns. If the pipeline latch latency is 1 ns then the maximum clock frequency to be applied is _____ MHz

[MCQ]

2. Consider a 4-stage pipeline with delays of 320 ns, 260 ns, 340 ns and 300 ns respectively. Inter stage buffer delay is 10 ns, register uses constant clock rate, then what is the total time taken to process 2000 data items on this pipelined system _____ (in micro seconds)

(a) 700.05 (b) 701.05
(c) 142.05 (d) None of these

[MCQ]

3. Assume a 5-segment single cycle processor (non-pipelined) and a 5-segment pipelined processor. Cycle time of non-pipelined processor is 10 times that of pipelined processor. Assume also that there are no stalls in the pipelined processor then what is the speed up achieved over non-pipelined processor if pipelined processor phase time is 2ns?

(a) 5 (b) 10
(c) 15 (d) 20

[MCQ]

4. Consider a pipelined machine X operating at 1 GHz that has speed up factor of 5 and operating upto 60% efficiency, then how many segments are present in the machine X? _____

(a) 5 (b) 6
(c) 7 (d) 9

[MCQ]

5. Consider a machine with frequencies of instruction, type of instructions, and cycles. Given below.

Instruction type	Frequency	Cycles
Load	40%	1
Store	15%	2
Branch	20%	2
ALU	25%	2

What is the average CPI?

(a) 2.0 (b) 1.5
(c) 1.6 (d) 3.0

[MCQ]

6. Consider 5 stage of two processors x and y have the following latencies:

Type	IF	ID	EX	MA	WB
x	400	500	450	650	200
y	300	250	200	290	240

Also consider that each pipeline costs 20ps extra for the register between pipeline stages. Which of the following pairs of tuples represent the cycle time, latency of one instruction and the throughput for a pipelined processor for both types x and y?

(a) $\left(670, 3350, \frac{1}{670}\right)\left(320, 1600, \frac{1}{320}\right)$

(b) $\left(670, 3350, \frac{1}{3350}\right)\left(320, 1600, \frac{1}{1600}\right)$

(c) $\left(3350, 670, \frac{1}{3350}\right)\left(1600, 320, \frac{1}{1600}\right)$

(d) None of the above

[MCQ]

7. Consider the sequence of instruction and a 5-stage pipeline (IF, ID, EX, MEM, and WB).

	Opcode	Destination	Source1	Source 2
I_1:	ADD	R_2	R_3	R_4 (1^{st} instruction to enter the pipeline)
I_2:	SUB	R_3	R_4	R_2
I_3:	MUL	R_2	R_3	R_4(last instruction to enter the pipeline)

How many RAW data hazards does the ID stage need to detect for this instruction sequence?

(a) 1 (b) 2

(c) 3 (d) 4

[NAT]

8. Consider a 5-stage pipelined processor having instruction fetch (IF), operand fetch (ID), instruction execution (IE), memory access (MA) and write back (WB) segments. The segments mentioned takes 1 clock cycle each for any instructions. Consider the given code fragment below.

Instruction	**Meaning of instruction**
I_0: load R_2, [100]	//R_2 = MEM [100]
I_1: load R_4, 5[R_3]	//R_4 = MEM [R_3 + 5]
I_2: MUL R_5, R_2, R_4	//R_5 = R_2 × R_4
I_3: DIV R_6, R_2, R_5	//R_6 = R_2 / R_5
I_4: SUB R_7, R_5, R_6	//R_7 = R_5 -R_6

What is the number of clock cycle needed to execute the above sequence of instruction?

Answer Key

1. **(125)**
2. **(b)**
3. **(b)**
4. **(d)**
5. **(c)**
6. **(a)**
7. **(b)**
8. **(18)**

Hints & Solutions

1. (125)

Sol. Largest delay = 7 + 1 = 8 ns

$f_{max} = \frac{1}{8}$ ns = 125 MHz

2. (b)

Sol. pipeline time (t_p) = (n + k – 1) × T_{seg}

Where n is the number of instruction, k is the number of segment/stages and T_{seg} is maximum delay in segment.

= (2000 + 4 – 1) × (340 + 10) ns

= (2003) × (350) ns

= 701.05 μs

3. (b)

Sol. Given,

For non-pipelined processor, cycle time is 10 times more than that of pipelined machine's cycle time.

Cycle time for pipelined machine is 2 ns.

∴ Cycle time for non-pipelined machine is 20 ns

$$\text{Speed up} = \frac{t_n}{t_p} \Rightarrow \frac{\cancel{20}^{10}}{\cancel{2}} = 10 \text{ ns}$$

∴ option (b) is correct.

4. (d)

Sol. $$\eta = \frac{\text{speed up}}{\text{number of stages}}$$

$$\frac{60}{100} = \frac{5}{k}$$

$$k = \frac{5}{0.6} \Rightarrow 8.33$$

= 9 stages

Therefore, if we take 9 stages then the efficiency would be 0.6.

5. (c)

Sol. $$\text{Average CPI} = \frac{\sum_{i=1}^{n} \text{instruction frequency}_i \times \text{CPI}_i}{\sum_{i=1}^{n} \text{instruction frequency}_i}$$

$$= \frac{0.4\times1 + 0.15\times2 + 0.2\times2 + 0.25\times2}{1} = 1.6$$

6. (a)

Sol. **For non-pipelined processor**

Cycle time: There is no pipelining, so the cycle time instructions will be going through all the stages each cycle.

So, x : Cycle time = 2200 ps

y : Cycle time : 1280 ps

The latency for an instruction is also the same. Since each instruction takes 1 cycle to go from beginning fetch to end of write back/Throughput is also $\frac{1}{\text{Cycle}}$ instruction per second.

For pipelined processor of

Cycle time: in this we take time of longest stage.

Type x: In this MM takes 650ps and there is 20ps overhead so in total 670 is cycle time.

Type y: In this IF takes 300 ps and there is overhead of 20 ps so in total 320 is the cycle time.

Latency: It is total time taken to execute an instruction.

Type x : 670 × 5 = 3350 ps

Type y : 320 × 5 = 1600 ps

Throughput: it is the number of instructions executed per unit time and also throughput calculated considering large number of instructions.

Type x : 1 instruction per 670 ps = $\frac{1}{670}$

Type y : 1 instruction per 320 : $\frac{1}{320}$.

7. (b)

Sol. $I_1 \rightarrow I_2$ on R_2

$I_2 \rightarrow I_3$ on R_3

∴ for a given program and pipeline, there are 2 hazards.

8. (18)

Sol. RAW dependency between

$I_0 - I_2$, $I_1 - I_2$, $I_2 - I_3$, $I_3 - I_4$

Cycles	IF	ID	EX	MA	WB
C_1	I_0				
C_2	I_1	I_0			
C_3	I_2	I_1	I_0		
C_4		I_2	I_1	I_0	
C_5	I_3	I_2	-	I_1	I_0
C_6	-	I_2			I_1
C_7	-	I_2			
C_8	I_4	I_3	I_2		
C_9	-	I_3		I_2	
C_{10}	-	I_3			I_2
C_{11}	-	I_3			
C_{12}		I_4	I_3		
C_{13}		I_4		I_3	
C_{14}		I_4			I_3
C_{15}		I_4			
C_{16}			I_4		
C_{17}				I_4	
C_{18}					I_4

Branch : CSE & IT

Batch : Hinglish

Computer Organization and Architecture

Machine Instructions and Addressing Mode

DPP

[MCQ]

1. Which of the following is primitive instruction in the CPU?

(a)

opcode	Address
4 bits	6 bits

(b)

opcode	Address-1	Address-2
4 bits	4 bits	4 bits

(c)

opcode	Address
4 bits	2 bits

(d)

opcode	Address-1	Address-2
2 bits	12 bits	8 bits

[NAT]

2. Consider a hypothetical system which support only-2 address instructions. If size of the instruction is 28 bit and size of each address is 10 bits then, the maximum number of instructions the system can support_____.

[NAT]

3. Consider a digital computer which support 64 3-address instruction. If the size of each address is 14 bits, then the instruction is of _____ bytes.

[MCQ]

4. The correct sequence in Fetch-Execute cycle is:

(a) Decode, Fetch, Execute

(b) Fetch, Execute, Decode

(c) Fetch, Decode, Execute

(d) None of the above

[MCQ]

5. Consider a system which supports 2 - address instructions only. The system has 2^P K bytes of memory. If there are 'q' distinct instructions supported by system then, what is the size of instruction?

(a) (q + p) bits

(b) [logq + 2 (P + 10)] bits

(c) (logq + 2P) bits

(d) log (p + q) bits

[MCQ]

6. Consider a system which support 2 - address instructions add 1-address instruction both. Suppose, the system has 6 bits instruction and 2 - bits addresses. If there are three 2 - address in the system then, maximum and minimum how many 1 - address instruction the system can support?

(a) 15, 1 (b) 4, 1

(c) 16, 0 (d) None

[MCQ]

7. Consider a PC - relative mode type branch instruction, which takes branch on addresses 680 in memory. The instruction has offset value 420. What is the address of this instruction in memory. If each instruction is stored in memory on 2 - locations?

(a) 258 (b) 280

(c) 282 (d) 260

[MCQ]

8. Consider a 6 - word instruction which is of the following type:

opcode	Mode-1	Mode-2	Address-1	Address-2

The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand of size 2 - words, each address is of 2 word and main memory takes 20 ns for each word access. What is the different between fetch cycle of instruction time and execution cycle of instruction time?

[Note : Register access time is negligible.]

(a) 260 ns (b) 20 ns

(c) 40 ns (d) 120 ns

[MCQ]

9. Consider a computer with 34 bits instruction and 14 bits addresses. If there are 60 2 - address instruction and 65000 1 - address instruction then, how many maximum 0 - address instruction can be formulated?

(a) 65536 K (b) 8576 K

(c) 16384 K (d) None

[MCQ]

10. If an opcode is of 4 bit then, how many maximum minimum type of instruction supported by CPU?

(a) 15, 1 (b) 15, 0

(c) 16, 1 (d) 16, 0

Answer Key

1. **(d)**
2. **(256)**
3. **(6)**
4. **(c)**
5. **(b)**
6. **(b)**
7. **(a)**
8. **(c)**
9. **(b)**
10. **(c)**

Hints & Solutions

1. (d)

Sol. Instruction with small opcode is known as primitive instruction in the CPU.

Therefore, Option (d) is right.

2. (256)

Sol. Instruction size = 28 bits

2-address format:

opcode	Address-1	Address-2
8 bits	10 bits	10 bits

Maximum opcode = 2^8

Maximum number of instructions = 256

3. (6)

Sol. Opcode = log64

= 6 bits

3-address format:

opcode	Address-1	Address-2	Address-3
8 bits	14 bits	14 bits	4 bits

Instruction size = 6 + 3 × 14

= 48 bits

= 6 bytes.

4. (c)

Sol. The correct sequence is

Instruction fetch

Instruction decode

Execution

Therefore, Option (c) is right.

5. (b)

Sol. Memory size = 2^P k bytes

= 2^P × 210 bytes

= 2^{p+10} bytes

Address size = P + 10 bits (each)

Number of instructions = q distinct

Opcode = $\log_2 q$

2-address format:

opcode	Address-1	Address-2
log q	P + 10	P + 10

Instruction size = log q + 2 (p + 10)

logq + 2 (P + 10) bits

Therefore, option (b) is right.

6. (b)

Sol. 2-address format:

opcode	Address-1	Address-2
2 bits	2 bits	2 bits

Number of opcodes = 4

Unused opcode = 4 – 3 = 1

1 -address format:

opcode	Address-1
4 bits	2 bits

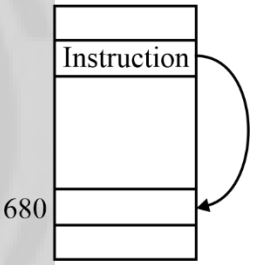
Maximum 1-address = 1 × 2^2 = 4

Minimum 1-address = 1

7. (a)

Sol. Target address = 680

Offset (relative location) = 420



Target address = PC value + offset

680 = PC + 420

PC = 680 – 420

PC = 260

PC hold next instruction address

Instruction address = 260 – 2 (2-location)

= 258

8. (c)

Sol. Fetch cycle:

Operand = 2-word

Address = 2-word

1 word fetch time = 20 ns

6 words fetch time = 6 × 20 = 120 ns

Execution cycle:

In register indirect mode first operand will take = 1 memory access

= 2 word = 2 × 20 = 40 ns

Second operand = 2 memory

$= 2 \times 2 \times 20 = 80$ ns

For write back 1 memory access

$= 1 \times 2 \times 20 = 40$ ns

Total execution time = 40 + 80 + 40 = 160 ns

Difference = 160 – 120 = 40 ns

Hence, option (c) is correct.

9. (b)

Sol. 2 - Address Format:

opcode	Address-1	Address-2
6 bits	14 bits	14 bits

Number of opcodes = $2^6 = 64$

Unused opcode = 64 – 60 = 4

1 - Address Format:

opcode	Address-1
20 bits	14 bits

Maximum opcode = $4 \times 2^{14} = 65536$

Unused opcode – 65536 – 65000 = 536

0 - Address Format:

opcode
34 bits

0 - address opcode = $2^{14} \times 536 = 8576$ k

10. (c)

Sol. Opcode = 4bits

Maximum operation = $2^4 = 16 = 16$ (16 instruction)

Minimum = 1 (Always)

Therefore, option (c) is right.

Branch : CSE & IT Batch : Hinglish

Computer Organization and Architecture
Secondary memory & I/O interface

DPP

[MCQ]

1. Which of the following is/are not the major functions for an IO module?

(a) Control and timing

(b) Error detection

(c) Processor communication

(d) Single instruction multiple data stream (SIMD)

[NAT]

2. Consider a system with data transfer rate is 10 KBPS. Data are exchanged between the processor and I/O interface. The performance gain when IO device is operating under interrupt mode over programmed IO mode)__.

Note (Interrupt interface over head is 15 μsec)

(round off 1 decimal places)

[MSQ]

3. In programmed I/O execution, the transfer time depends on _____.

(a) I/O speed

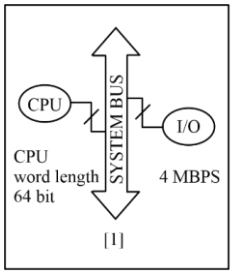
(b) Data size

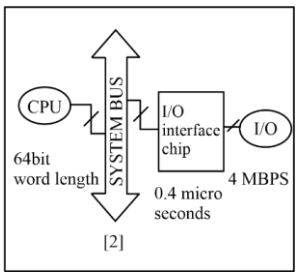
(c) Latency of I/O interface chip

(d) None of these

[NAT]

4. Consider the following scenario





Calculate the speedup when I/O device is operating under programmed I/O over interrupt mode ____.

[MCQ]

5. Which of the following interrupts are caused by software instructions are known as ?

(a) Hardware interrupt

(b) Exception interrupt

(c) Maskable interrupt

(d) Normal interrupt

6. [NAT]

Consider 16 MBPS I/O device interfaced to 32-bit CPU using DMA interface. DMA contain 16-bit count register, 32 bit data register and five, 8 bit address register. Data file size is 512 kB. How many DMA cycles are required to transfer the file?

7. [NAT]

A processor can support a maximum memory of 32 GB, where the memory is word addressable (a word consist of 2 bytes). The size of the address bus of the processor is at least _____bits.

8. [MCQ]

A hard disk has 32 sectors per track, 10 platters each with 2 recording surface and 500 cylinders.

The address of a sector is given as a triple <c, h, s>, where c is cylinder number, h is surface number and s is the sector number. Thus the 0^{th} sector is addressed as <0, 0, 0>, the 1^{st} sector as <0, 0, 1> and so on. The address of the <20, 10, 3> corresponds to sector number?

Answer Key

1. **(d)**
2. **(6.66 to 6.66)**
3. **(a, b)**
4. **(0.2 to 0.2)**
5. **(d)**
6. **(2)**
7. **(34)**
8 **(13123)**

Hints & Solutions

1. (d)

- The major functions for an IO module are
- Control and timing
- Error detection
- Device communication
- Data buffering
- Processor communication
- SIMD is one of the types of parallel processor system.

2. (6.66 to 6.66)

Data are exchanged between processor and I/O (programmed I/O)

- Word length not given, assume byte addressable.
- **Programmed IO**

10 KB _____1 sec

1B _____?

$= \frac{1}{10}$

$= 100\ \mu$ sec

$ET_{\text{programmed I/O}} = 100\mu$ sec

$$S \text{ (performance gain)} = \frac{ET_{\text{programmed I/O}}}{ET_{\text{interface I/O}}}$$

$$= \frac{100}{15} = 6.66$$

3. (a, b)

In interrupt driven I/O mode CPU time (execution per transfer) depends on latency of an I/O interface chip. Where as in programmed I/O CPU time depends on data size and I/O speed.

4. (0.2 to 0.2)

Programmed I/O mode:

CPU time = depends on I/O speed and data size

Word length = 64 bits (8 bytes)

$ET_{\text{programmed I/O}}$ = 4 MB _____1 sec

8 B _____?

$$ET_{\text{programmed I/O}} = \frac{8B}{4MB}$$

= 2 microseconds

Interrupt I/O:

CPU time = latency of an I/O interface chip

$ET_{\text{interface I/O}} = 0.4\mu$ sec

$$\text{Speedup(s)} = \frac{ET_{\text{interfaceI/O}}}{ET_{\text{programmed I/O}}} = \frac{0.4}{2}$$

= 0.2.

5. (d)

The definition of normal interrupts is interrupts which are caused by the software instructions are called software interrupt.

Hence, option (d) is correct.

6. (2)

DMA operation cycle is controlled by the count register.

Count register = 16 bit, so it maintains 65536 counts.

In every count one word data will be transferred.

Therefore, data transmission/DMA cycle = 65536 W

65536 × 32 bit

65536 × 4-byte

$2^{16} \times 2^2 = 2^{18}$ B = 256 kB

1 DMA cycle → 256 kB

Number of DMA cycle – 1 file (512 kB)

$$\Rightarrow \frac{512\ \cancel{kB}}{256\ \cancel{kB}} = 2 \text{ cycles}$$

7. (34)

Given 1word = 2 Byte, 1 byte = $\frac{1}{2}$ word

Memory = 32 GB $\Rightarrow 32G \times \frac{1}{2}$ word

$\Rightarrow$ 16 G words = 2^{34}

The size of the address bus of the processor = $\lceil \log_2 2^{34} \rceil$

$\Rightarrow$ 34 bits

8. (13123)

$20 \times 32 \times 2 \times 10 + 10 \times 32 + 3 \Rightarrow 12800 + 320 + 3$

$\Rightarrow 13123$