



Kunal Jha

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BOOKMARKS

MY PROFILE

REPORTS

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NEWS

TEST SCHEDULE

TOPICWISE : DIGITAL LOGIC-1 (GATE - 2020) - REPORTS

OVERALL ANALYSIS

COMPARISON REPORT

SOLUTION REPORT

ALL(17)

CORRECT(2)

INCORRECT(5)

SKIPPED(10)

Q. 1

Solution Video

Have any Doubt ?

Given $(6y3)_x + (54)_x = 487$, what can be the possible value of base x and y respectively A 10, 2 B 8, 7

Your answer is Correct

Solution :

- (b)
- (i) $x > y$
- (ii) $x > 6$

$$\begin{aligned}x &= 8, y = 7 \\(673)_8 + (54)_8 &= (487)_{10} \\(443)_{10} + (44)_{10} &= (487)_{10}\end{aligned}$$

 C 11, 3 D None of these

QUESTION ANALYTICS



Q. 2

Solution Video

Have any Doubt ?



Which of the following is incorrect?

 A A decoder with an enable input can function as a demultiplexer. B A full adder can be implemented using single 3×8 decoder.

Correct Option

Solution :

- (d)
- All statements are correct.

 C A encoder will output 101 if priority is given to an input with higher subscript number and input D_2, D_4, D_5 and logic 1. D None of the above

QUESTION ANALYTICS



Q. 3

Solution Video

Have any Doubt ?

The boolean function $Y(A, B, C) = A\bar{B} + A \oplus C$. The SOP and POS from will be A $Y = \Sigma(1, 2, 3, 6, 7)$ and $Y = \Pi(0, 4, 5)$ B $Y = \Sigma(1, 3, 4, 5, 6)$ and $Y = \Pi(0, 2, 7)$

Correct Option

Solution :

(b)

$$Y = A\bar{B} + A \oplus C$$

$$= A\bar{B} + A\bar{C} + \bar{A}C$$

So,

$$SOP = \Sigma(1, 3, 4, 5, 6)$$

$$POS = \Pi_M(0, 2, 7)$$

 C $Y = \Sigma(0, 2, 5, 6)$ and $Y = \Pi(1, 3, 4, 7)$ D None of the above

Your answer is Wrong

QUESTION ANALYTICS



Q. 4

Solution Video

Have any Doubt ?



In the circuit shown below as an example the propagation delay of NAND : NOR :: 1 : 2. What is the number of NAND and NOR gates required to get the time period T of 30 nsec respectively?

(Assume propagation delay of NAND gates is $\frac{3}{2}$ nsec).



A 1,7

B 2,4

Correct Option

Solution :

(b)

$$T = 2 \times t_{pd}$$

T = Time period

t_{pd} = Sum of propagation delay of all the gates

$$30 \text{ nsec} = 2 \times t_{pd}$$

$$t_{pd} = 15 \text{ nsec}$$

i.e. total delay of the logic gates must be 15 nsec.

(Number of NAND gates (x) \times NAND gates propagation delay + Number of NOR gates (y) \times NOR gates propagation delay) = 15 nsec

$$= x \times \frac{3}{2} \text{ nsec} + y \times \frac{3}{2} \times 2 \text{ nsec}$$

Using option (b)

$$= 2 \times \frac{3}{2} \text{ nsec} + 4 \times \frac{3}{2} \times 2 \text{ nsec}$$

$$\Rightarrow 3 \text{ nsec} + 12 \text{ nsec} = 15 \text{ nsec}$$

Hence option (b) is correct.

C 3,5

D 3,3

QUESTION ANALYTICS

+

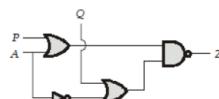
Q. 5

Solution Video

Have any Doubt ?

Q

The circuit shown below is used to implement the function $Z = f(A, B) = \bar{A} + B$. The values of P and Q are



A $P = A, Q = B$

Your answer is Wrong

B $P = B, Q = \bar{A}$

C $P = \bar{B}, Q = O$

D $P = O, Q = \bar{B}$

Correct Option

Solution :

(d)

$$\bar{Z} = (P + A)(Q + \bar{A})$$

$$\bar{Z} = PQ + AQ + \bar{A}P$$

If

$$Z = \bar{A} + B$$

$$\bar{Z} = \bar{A} + B = A\bar{B}$$

$$Q = \bar{B}, P = O$$

QUESTION ANALYTICS

+

Q. 6

Solution Video

Have any Doubt ?

Q

Consider the function $F(x, y, z) = xy + x'z + yz$. All the variables are available in complemented and non-complemented form. The minimum number of gates required to implement the above function is _____. (All gates are available only with 2-inputs)

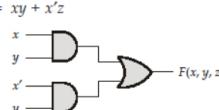
3

Correct Option

Solution :

3

$$\begin{aligned} F(x, y, z) &= xy + x'z + yz \\ &= xy + x'z + x'y'z + xyz \\ &= xy + x'z \end{aligned}$$



Total 3 gates are required.

Your Answer is 4

QUESTION ANALYTICS

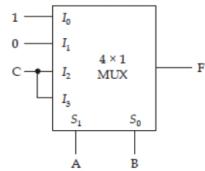
Q. 7

Solution Video

Have any Doubt?



The number of minterms of the following function F is _____.

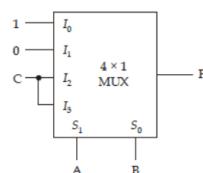


4

Correct Option

Solution :

4



$$\begin{aligned} F &= \bar{A}\bar{B} \cdot 1 + \bar{A}B \cdot 0 + A\bar{B}C + ABC \\ &= \bar{A}\bar{B} + A\bar{B}C + ABC \\ &= \sum m(0, 1, 5, 7) \end{aligned}$$

4

Your Answer is 3

QUESTION ANALYTICS

Q. 8

Solution Video

Have any Doubt?



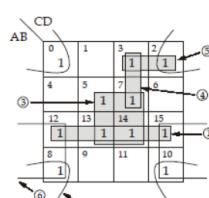
Given $F(A, B, C, D) = \sum m(0, 2, 3, 5, 7, 8, 10, 12, 13, 14, 15)$.
The number of prime implicants is _____.

6

Correct Option

Solution :

6



Number of prime implicants = 6.

6

Your Answer is 4

QUESTION ANALYTICS

Q. 9

Solution Video

Have any Doubt?



When $(-89)_{10}$ is represented in sign 2's complement form, the sum of bits will be _____.

5

Your answer is Correct

Solution :

5

Binary representation of $(89)_{10} = (01011001)$
 $(-89)_{10} = 2's \text{ complement of } (01011001)$
So, 2's complement of $(01011001) = (10100110) + (1) = 10100111$
Sum of bits = 5

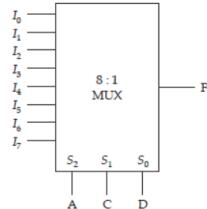
QUESTION ANALYTICS



Q. 10

[▶ Solution Video](#)[☞ Have any Doubt ?](#)

The logic function $F(A, B, C, D) = AD + ABD + ABC + ACD$ is to be realized using an 8 to 1 multiplexer shown in the figure.



The input I_6 to the multiplexer will be

A 0

B 1

C \bar{B}

D B

Correct Option

Solution :

(d)

To select I_6 , (A, C, D) should be $(1, 1, 0)$.

Now, $F = AD + ABD + ABC + ACD$

Put, $A = 1, C = 1, D = 0$

$$= 1.0 + 1.1.0 + 1.1.1 + 1.1.0$$

$$F = B$$

Thus input I_6 must be equal to B.

QUESTION ANALYTICS





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[OVERALL ANALYSIS](#)
[COMPARISON REPORT](#)
[SOLUTION REPORT](#)
[ALL\(17\)](#)
[CORRECT\(2\)](#)
[INCORRECT\(5\)](#)
[SKIPPED\(10\)](#)
Q. 11
[▶ Solution Video](#)
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Match List-I with List-II and select the correct answer using the codes given below the lists:

List-I
List-II

- | | |
|---------------------------------------|----------------------------|
| A. $(A \oplus B) \oplus (B \oplus C)$ | 1. $(A \odot C)$ |
| B. $AB + \bar{A}C + BC$ | 2. $(A + B) \odot (A + C)$ |
| C. $(A \odot B) \odot (B \odot C)$ | 3. $AB + \bar{A}C$ |
| D. $A + (B \odot C)$ | 4. $(A \oplus C)$ |
| | 5. $\bar{A}B \oplus AC$ |

Codes

	A	B	C	D
(a)	4	3	1	2
(b)	3	4	1	2
(c)	2	3	1	2
(d)	4	3	5	2

A. a

Correct Option

Solution :

$$\begin{aligned}
 (a) \quad & (A \oplus B) \oplus (B \oplus C) \\
 \Rightarrow & (\overline{A \oplus B})(B \oplus C) + (A \oplus B)(\overline{B \oplus C}) \\
 \Rightarrow & (AB + \bar{A}\bar{B})(\bar{A}\bar{C} + \bar{B}\bar{C}) + (\bar{A}\bar{B} + A\bar{B})(BC + \bar{B}\bar{C}) \\
 \Rightarrow & AB\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C} \\
 \Rightarrow & \bar{A}\bar{C}(B + \bar{B}) + A\bar{C}(B + \bar{B}) \\
 (\bar{A}\bar{C} + A\bar{C}) & = A \oplus C \\
 (A) \text{ matches with (4)} \\
 AB + \bar{A}\bar{C} + BC & = AB + \bar{A}C \\
 \text{This is consensus law in XOR algebra.} \\
 (C) \text{ matches with (1)} \\
 (B) \text{ matches with (3)} \\
 A + (B \odot C) & = (A + B) \odot (A + C) \\
 & \text{Follows distributive law} \\
 (D) \text{ matches with (2)}
 \end{aligned}$$

B. b
C. c
D. d
QUESTION ANALYTICS

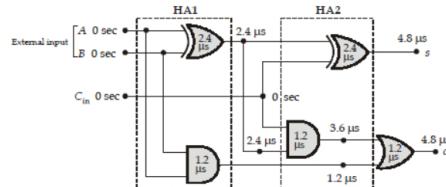
Q. 12
[▶ Solution Video](#)
[Have any Doubt ?](#)


A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 μ sec. A 4-bit ripple carry binary adder is implemented by using full adders. The total propagation delay of this 4-bit binary adder is

A. 19 μ sec
B. 19.2 μ sec
C. 12 μ sec

Correct Option

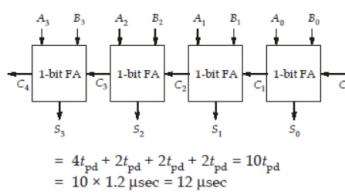
Solution :

 (c)
 For one full Adder:

 The propagation delay of AND / OR gate t_{pd} = 1.2 μ sec.

 The propagation delay of EX-OR gate $2t_{pd}$ = 2.4 μ sec.

- Binary Adder external inputs are available to all HA1's simultaneously.
- First HA1 output of all full adders are available simultaneously with delay of 2.4 μ sec (i.e., $2t_{pd}$).

- Carry generate from previous full adder is passing only through HAZ of next full adder.
- The delay of LSB full adder = t_{pd}
- The 4 bit ripple carry binary delay:



D 38.4 μsec

QUESTION ANALYTICS

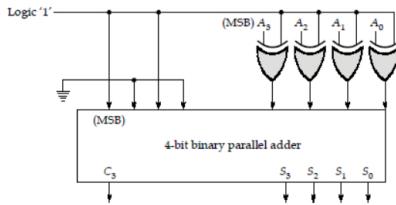
Q. 13

Solution Video

Have any Doubt ?



Consider the digital circuit shown below:



The digital circuit acts as

A 9's complement circuit

Correct Option

Solution :

(a)

$$\begin{aligned}
 \text{Let addend } &= A_3 A_2 A_1 A_0 = A \text{ (Say)} \\
 &= 1010
 \end{aligned}$$

4-bit binary parallel adder output

$$\begin{aligned}
 &= (1010)_2 + \bar{A} \\
 &= (1001)_2 + \bar{A} + 1 = (1001)_2 - (A)_2 \quad [2's \text{ complement subtraction}] \\
 &= (9)_{10} - (A)_{10} \\
 &= 9's \text{ complement of } A
 \end{aligned}$$

B 0's complement circuit

C 5's complement circuit

D 9's complement circuit if $C_3 = 0$ and 10's complement circuit if $C_3 = 1$.

QUESTION ANALYTICS

Q. 14

Solution Video

Have any Doubt ?



The minimal function that can detect a 'divisible' by 3' 8421 BCD code digit (representation is $D_8 D_4 D_2 D_1$) is given by

A $D_8 D_1 + D_4 D_2 + D_8 D_2 D_1$

B $D_4 D_1 + D_4 D_2 + D_8 \bar{D}_4 \bar{D}_2 D_1$

C $D_8 D_1 + D_4 D_2 \bar{D}_1 + \bar{D}_4 D_2 D_1 + \bar{D}_8 \bar{D}_4 \bar{D}_2 \bar{D}_1$

Correct Option

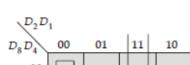
Solution :

(c)

Numbers divisible by 3 in 8421 BCD system is = 0, 3, 6, 9.

Decimal No.	BCD No. 8421	F(Output)
0	0 0 0 0	1
1	0 0 0 1	0
2	0 0 1 0	0
3	0 0 1 1	1
4	0 1 0 0	0
5	0 1 0 1	0
6	0 1 1 0	1
7	0 1 1 1	0
8	1 0 0 0	0
9	1 0 0 1	1

$$F = \Sigma m (0, 3, 6, 9) + d (10, 11, 12, 13, 14, 15)$$



	v	v	v	v
01	0	0	0	1
11	x	x	x	x
10	0	1	x	x

$$\bar{D}_8 \bar{D}_4 \bar{D}_2 \bar{D}_1 + D_8 D_1 + D_4 D_2 \bar{D}_1 + \bar{D}_4 D_2 D_1$$

D $D_4 D_2 \bar{D}_1 + \bar{D}_4 D_2 D_1 + D_8 D_4 D_2 D_1$

QUESTION ANALYTICS



Q. 15

Solution Video

Have any Doubt?



The maximum number of Boolean expressions that can be formed for the function $f(x, y, z)$ satisfying the relation $f(\bar{x}, \bar{y}, \bar{z}) = f(x, y, z)$ is _____.

16

Correct Option

Solution :

16

For every combination of x, y, z the function value remains same for input $\bar{x}, \bar{y}, \bar{z}$.

x	y	z	$f(x, y, z) = f(\bar{x}, \bar{y}, \bar{z})$
0	0	0	either 0 or 1
1	0	1	
0	0	1	either 0 or 1
1	0	0	
0	1	0	either 0 or 1
1	1	1	
0	1	1	either 0 or 1
1	1	0	either 0 or 1

Effectively there are only four rows for the truth table of the function $f(x, y, z)$.

∴ Total Boolean expressions possible is $2^4 = 16$.

QUESTION ANALYTICS



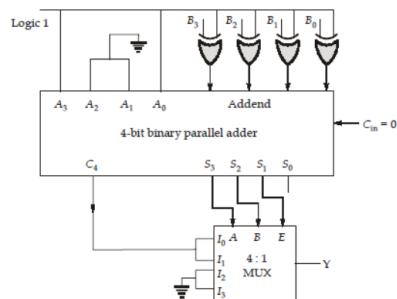
Q. 16

Solution Video

Have any Doubt?



Consider the digital circuit shown below:



What will be the output Y , if the number $B_3 B_2 B_1 B_0 = 0101$ _____.

1

Correct Option

Solution :

1

Addend will be = 1010

$$\begin{aligned} S_3 S_2 S_1 S_0 &= 1010 + A_3 A_2 A_1 A_0 + C_{in} \\ &= 1010 + 1001 \\ &= 0011 \quad (C_4 = 1) \end{aligned}$$

$$AB = 00$$

and

$$E = C_4 = 1$$

So,

$$Y = 1$$

QUESTION ANALYTICS



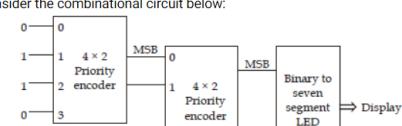
Q. 17

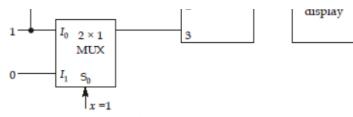
Solution Video

Have any Doubt?



Consider the combinational circuit below:



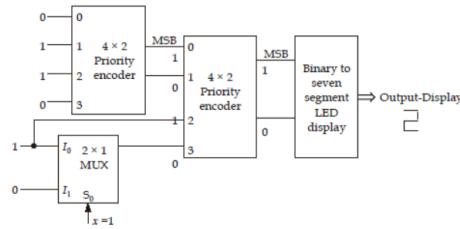


The output of the combinational circuit is _____.

Correct Option

Solution :

2



QUESTION ANALYTICS

+

Item 11-17 of 17 « previous 1 2 next »



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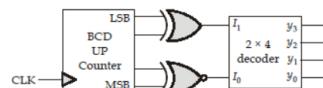
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[OVERALL ANALYSIS](#)
[COMPARISON REPORT](#)
[SOLUTION REPORT](#)
[ALL\(17\)](#)
[CORRECT\(3\)](#)
[INCORRECT\(4\)](#)
[SKIPPED\(10\)](#)
Q. 1
[Solution Video](#)
[Have any Doubt ?](#)


For the circuit shown below:


 For how many number of clock pulses for which y_2 is '1'?

A 2 clock pulses

B 3 clock pulses

Correct Option

Solution :

(b)

$$I_1 = Q_1 \oplus Q_0$$

$$I_0 = Q_3 \odot Q_2$$

Clock	Q_3	Q_2	Q_1	Q_0	I_1	I_0	y_2
0	0	0	0	0	0	1	0
1	0	0	0	1	1	1	0
2	0	0	1	0	1	1	0
3	0	0	1	1	0	1	0
4	0	1	0	0	0	0	0
5	0	1	0	1	1	0	1
6	0	1	1	0	1	0	1
7	0	1	1	1	0	0	0
8	1	0	0	0	0	0	0
9	1	0	0	1	1	0	1
10	0	0	0	0	0	1	0

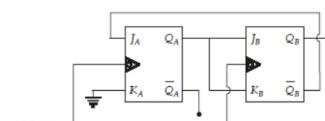
 Since, in 10 clock cycle y_2 is 1 for 3 clock cycles.

C 10 clock pulses

D 6 clock pulses

[QUESTION ANALYTICS](#)

Q. 2
[Solution Video](#)
[Have any Doubt ?](#)

 A circuit is designed with 2 – J-K FF's. If the output ($\theta_A \theta_B$) = 10 at starting, what will be the output ($\theta_A \theta_B$) after 13th clock pulse.

A 00

B 10

C 11

 Your answer is **Correct**
Solution :
 (c)

$$N = 2, K = 13$$

$$K \% 2 = 1$$

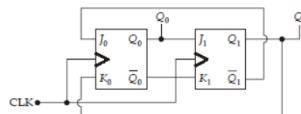
Clock	Q_A	Q_B	FFA		FFB	
			$J_A = \bar{Q}_B$	$K_A = 0$	$J_B = Q_A$	$K_B = Q_A$
1	1	0	0	0	1	1
2	1	1	0	0	1	1

D 01

[QUESTION ANALYTICS](#)

Q. 3
[Solution Video](#)
[Have any Doubt ?](#)


In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1 Q_0 = 00$. The state ($Q_1 Q_0$), immediately after the 334th clock pulse is



A 00

Your answer is Wrong

B 01

C 10

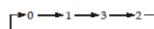
D 11

Correct Option

Solution :

(d)

Clk	Q_1	Q_0	FF1		FF0	
			$J_1 = Q_0$	$K_1 = \bar{Q}_0$	$J_0 = \bar{Q}_1$	$K_0 = Q_1$
0	0	0	0	1	1	0
1	0	1	1	0	1	0
2	1	1	1	0	0	1
3	1	0	0	1	0	1
4	0	0				



$$N = 4$$

$$K = 334$$

$$K \% N = 2 = (11)_2$$

QUESTION ANALYTICS

Q. 4

Solution Video

Have any Doubt ?



Consider the following IEEE single precision floating point number shown below:

0 1000011110100000000000000000000

What is the octal equivalent of above number?

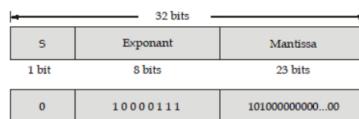
A 640

Your answer is Correct

Solution :

(a)

Format of single precision floating point is



$$\begin{aligned} \text{Value} &= 1.M \times 2^{-127} \\ &= 1.1010 \times 2^{135-127} \\ &= (1.1010)_2 \times 2^8 \\ &= 1.625 \times 2^8 \\ &= (416)_{10} \end{aligned}$$

Octal representation

$$\begin{array}{r} 8 | 416 \\ 8 | 52 \\ \hline 6 \quad 4 \end{array}$$

Octal representation is (640).

B 520

C 770

D 235

QUESTION ANALYTICS

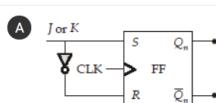
Q. 5

Solution Video

Have any Doubt ?

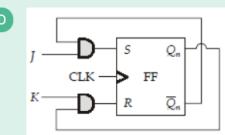
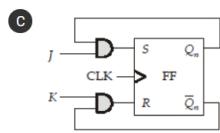
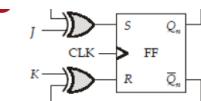


Which of the following represents J-K flip-flop?



B

Your answer is Wrong



Correct Option

Solution :
(d)

$$S(J, K, Q_n) = J\bar{Q}_n$$

$$R(J, K, Q_n) = KQ_n$$

So, option (d) matches correct as per equation.

QUESTION ANALYTICS



Q. 6

[▶ Solution Video](#)

[Have any Doubt ?](#)



The lowest frequency in kHz, if a 6 MHz clock frequency is applied to a cascaded counter of modulus-2 counter and modulus-3 counter are _____.

1000

Correct Option

Solution :
1000

Resulting mode in cascade counter

$$= M \times N = 2 \times 3 = 6$$

$$\text{Lowest output frequency} = \frac{6 \times 10^6}{6} = 1000 \text{ kHz}$$

QUESTION ANALYTICS



Q. 7

[▶ Solution Video](#)

[Have any Doubt ?](#)



For a Mod-10 counter, Johnson counter uses X FF's, ring counter uses Y FF's and ripple counter uses Z FF's. Then X + Y + Z will be _____.

19

Correct Option

Solution :
19

For MOD - 10 counter

X = Johnson counter required = 5 FF's

Y = ring counter required = 10 FF's

Z = ripple counter required = 4 FF's

$$X + Y + Z = 5 + 10 + 4 = 19 \text{ FF's}$$



Your Answer is 25

QUESTION ANALYTICS



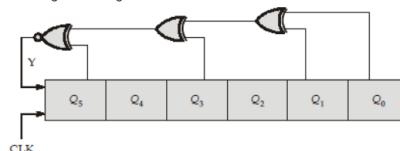
Q. 8

[▶ Solution Video](#)

[Have any Doubt ?](#)



A six bit right shift register is initialized to a value of 100000. Minimum number of clock pulses needed to produce 101101 from the given initial value is _____.



5

Your answer is Correct

Solution :
5

Let the output of XNOR gate is Y

$$Y = (Q_3 \oplus Q_1 \oplus Q_0) \odot Q_5$$

CLK	Y	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
-		1	0	0	0	0	0
1	0	0	1	0	0	0	0
2	1	1	0	1	0	0	0
3	1	1	1	0	1	0	0
4	0	0	1	1	0	1	0
5	1	1	0	1	1	0	1

Minimum five clock pulses are required to get the sequence 101101

QUESTION ANALYTICS



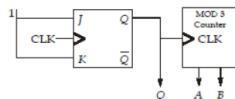
Q. 9

Solution Video

Have any Doubt ?



In figure, initially $Q = A = B = 0$. After five clock triggers, the states of Q , A and B will be respectively is _____.



110

Correct Option

Solution :

110

J-K flip-flop will change for every clock pulse. Mod-3 counter will change whenever Q is changing from 0 to 1 because it is ripple counter.

CLK	Q	A	B
1	0	0	0
2	1	1	1
3	0	1	1
4	1	0	1
5	0	0	1
	1	1	0

QUESTION ANALYTICS



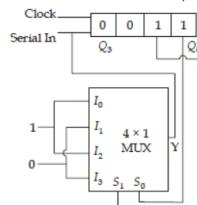
Q. 10

Solution Video

Have any Doubt ?



The initial content of serial IN parallel OUT, right shift, shift register shown below is 0011. After how many clock pulses, the content of register will return to its initial value.



A 7

B 8

Correct Option

Solution :

(b)

Clock	$S.I = Y$	$Q_3 \ Q_2 \ Q_1 \ Q_0$				Initial state
		S_1	S_0	MUX inputs		
1	0	0	0	1	1	1
2	0	0	0	0	1	0
3	1	0	0	0	0	0
4	1	1	0	0	0	0
5	1	1	1	1	0	0
6	1	1	1	1	1	0
7	0	0	1	1	1	0
8	0	0	1	1	1	0

After 8 clock pulse.

C 11

D 13

QUESTION ANALYTICS





Kunal Jha

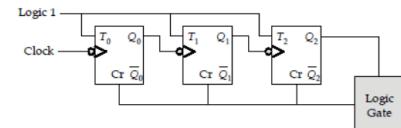
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[SOLUTION REPORT](#)
[ALL\(17\)](#)
[CORRECT\(3\)](#)
[INCORRECT\(4\)](#)
[SKIPPED\(10\)](#)
Q. 11
[▶ Solution Video](#)
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The 3-bit ripple counter (shown below) is to be designed as a MOD 4 counter



What is the best architecture of the 'Logic gate'?

- A a 3-bit input AND gate
- B a 2-input AND gate
- C a NOT gate
- D a wire connection (no logic gate needed)

Correct Option

Solution :
 (d)

	Q ₂	Q ₁	Q ₀	Cr
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
1	0	0	0	1

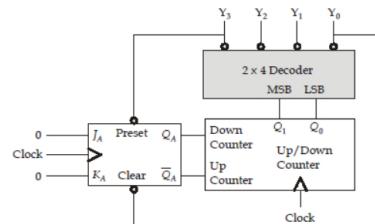
So the output Q₂ can be directly connected to clear.

∴ Best architecture is a wire connection.

[QUESTION ANALYTICS](#)

Q. 12
[▶ Solution Video](#)
[Have any Doubt ?](#)


Consider the circuit given below:



Assuming the initial value of counter output (Q₁, Q₀) as zero, the counter output for 8 clock pulses in decimal form is

- A 0, 3, 2, 1, 0, 1, 2, 3

- B 0, 1, 2, 3, 2, 1, 0, 1

Correct Option

Solution :

(b)

$$\text{Initially } Q_0 = Q_1 = 0$$

$$\Rightarrow Y_0 = 0$$

⇒ J-K flip-flop is cleared

$$Q_A = 0 \quad \bar{Q}_A = 1$$

As clock pulse is applied counter starts up counting

As counter reaches Q₁ = 1, Q₀ = 1 after 3 clock pulses J-K flip flop is preset.

$$\Rightarrow Q_A = 1 \quad \bar{Q}_A = 0$$

⇒ Counter starts down counting until Y₀ is low and this repeats.

So, Output Q₁ Q₀ in decimal form is

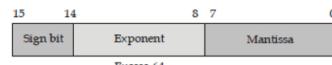
0, 1, 2, 3, 2, 1, 0, 1....

- C 0, 1, 2, 3, 3, 2, 1, 0

- D 0, 3, 2, 1, 0, 0, 1, 2

[QUESTION ANALYTICS](#)


Consider the following floating point format:



Mantissa is a pure fraction in sign-magnitude form. What is the representation of decimal number 0.625×2^{18} in hexadecimal without normalization and rounding off?

A 52B0

B 52A0

Correct Option

Solution :

(b)

$$\text{Biased exponent} = 18 + 64 = 82$$

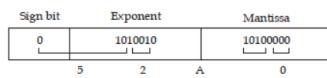
Representing 82 in binary

$$(82)_2 = (1010010)_2$$

Representing mantissa in binary

$$(0.625)_{10} = (0.10100000)_2$$

Floating point representation is as follows:



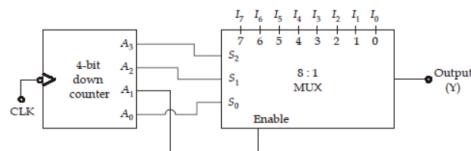
C 52A1

D None of these

QUESTION ANALYTICS

+

A 4-bit Down counter is used to control the output of the multiplexer as shown in figure. The counter is initially at $(1111)_2$, then the output of the multiplexer will follow the sequence



A $I_7, 0, I_6, 0, I_5, 0 \dots$

B $I_7, 0, 0, I_6, 0, I_5 \dots$

C $I_7, I_6, I_5, I_4, I_3 \dots$

D $I_7, I_6, 0, 0, I_5, I_4, 0, 0 \dots$

Correct Option

Solution :

(d)

	S_2	S_1	E	S_0	
	A_3	A_2	A_1	A_0	
1 st clock	1	1	1	1	-15 I_7
2 nd	1	1	0	0	-14 I_6
3 rd	1	1	0	1	-13 0
4 th	1	1	0	0	-12 0
5 th	1	0	1	1	-11 I_5
6 th	1	0	1	0	-10 I_4

For 1st and 2nd clock pulses, enable is 1

$$S_2 \quad S_1 \quad S_0 \\ 1^{\text{st}} \text{ clock pulse} - \quad 1 \quad 1 \quad 1 \rightarrow 1_7$$

$$2^{\text{nd}} \text{ clock pulse} - \quad 1 \quad 1 \quad 0 \rightarrow 1_6$$

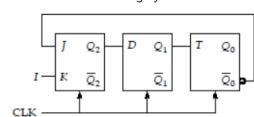
For 3rd and 4th clock pulse, enable is 0,

So, Y is 0

QUESTION ANALYTICS

+

Consider the following synchronous counter made up of JK, D, T flip-flops.



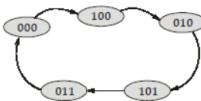
The modulus value of the counter is _____.

5

Correct Option

Solution :
5

Clock	Present state			$J_2 = \bar{Q}_0, K_2 = 1$	$D_1 = Q_2$	$T_0 = Q_1$
	Q_2	Q_1	Q_0			
0	0	0	0	1	1	0
1	1	0	0	1	1	0
2	0	1	0	1	0	1
3	1	0	1	0	1	0
4	0	1	1	0	1	1
5	0	0	0			



The number of used states = 5
 \therefore Modulus value = 5

QUESTION ANALYTICS

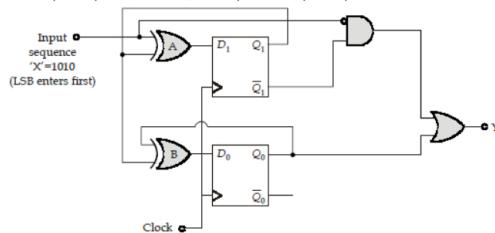
Q. 16

Solution Video

Have any Doubt ?

Consider a clocked sequential circuit as shown in the figure below. Assuming initial state to be $Q_1 Q_0 = 00$

For an input sequence $X = 1010$, the respective output sequence will be _____.



1001

Correct Option

Solution :
1001

Clock	X	$Q_1 Q_0$	FF1		$Y = \bar{X} \bar{Q}_1 + Q_0$
			$D_1 = Q_1 \oplus X$	$D_0 = Q_1 \oplus Q_0$	
0	0	0 0	0	0	1
1	1	0 0	1	0	0
2	0	1 0	1	1	0
3	1	1 1	0	0	1
4	0	0 0			

Answer is 1001.

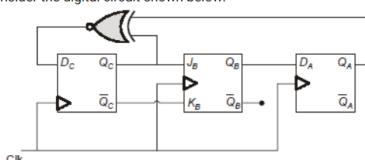
QUESTION ANALYTICS

Q. 17

Solution Video

Have any Doubt ?

Consider the digital circuit shown below:



If initially $Q_A Q_B Q_C$ is at 110 then minimum number of clock required to get $Q_A Q_B Q_C$ equal to 011 is _____.

6

Correct Option

Solution :
6

Given that,

$$D_A = Q_B$$

$$J_B = Q_C$$

$$K_B = \bar{Q}_C$$

$$D_C = Q_C \odot Q_A$$

So, the state table is

Clock	Present state			Next state			D_A	J_B	K_B	D_C
	Q_A	Q_B	Q_C	Q_A	Q_B	Q_C				
1	1	1	0	1	0	0	1	0	1	0
2	1	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	1	0	0	1	1
4	0	0	1	0	1	0	0	1	0	0
5	0	1	0	1	0	1	1	0	1	1
6	1	0	1	0	1	1	0	1	0	1

Hence 6 clock pulses are required.

Your Answer is 6

 QUESTION ANALYTICS

+

Item 11-17 of 17 | « previous | 1 | 2 | next »



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[SOLUTION REPORT](#)
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Q. 1
[▶ Solution Video](#)
[Have any Doubt ?](#)


Let $f(A, B) = A' + B$, then which of the given options is the simplified form of the function $f(f(x + y, y), z)$?

A $xy' + z$

Correct Option

Solution :

$$\begin{aligned}
 \text{(a)} \quad \text{Given,} \quad f(A, B) &= A' + B \\
 f(f(x + y, y), z) &= f((x + y)' + y, z) \\
 &= ((x + y)' + y)' + z \\
 &= (x + y) \cdot y' + z \\
 &= xy' + z
 \end{aligned}$$

Hence option (a) is correct.

B $x' + z$

C $x + z$

D $x + z'$

QUESTION ANALYTICS


Q. 2
[▶ Solution Video](#)
[Have any Doubt ?](#)


Consider the following statements:

- I. An RS Latch is a type of flip-flop with a 1-bit memory.
 - II. An encoder has n input lines and $2n$ output lines.
 - III. Left shift register can be termed for either division or multiplication.
- Which of the above is correct statements?

A I only

Correct Option

Solution :

- (a)
- Statement I is correct.
- Encoder has 2^n input and n -output lines.
- Left shift register is termed as multiplication by 2.

B II only

C II and III only

D I and III only

QUESTION ANALYTICS


Q. 3
[▶ Solution Video](#)
[Have any Doubt ?](#)


Consider the below digital circuit. The output f of both the circuit is same.

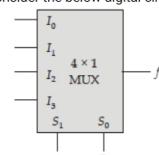


Figure (a)

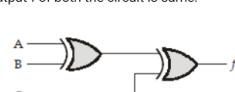


Figure (b)

What is the correct combinations of inputs of multiplexer using the codes given below?

- | | | | |
|-------|-------|-------|-------|
| I_0 | I_1 | I_2 | I_3 |
|-------|-------|-------|-------|
- (a) C \bar{C} C C
 - (b) 0 1 C \bar{C}
 - (c) 1 \bar{C} \bar{C} C
 - (d) C 0 1 C

A a

Correct Option

Solution :

- (a) Output of figure (b) is

$$\begin{aligned} f &= A \oplus B \oplus C \\ &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \end{aligned}$$

Output of figure (a) is

$$f = \bar{A}\bar{B}I_0 + \bar{A}BI_1 + A\bar{B}I_2 + AB\bar{I}_3$$

On comparison

$$I_0 = C, I_1 = \bar{C}, I_2 = \bar{C}, I_3 = C$$

So option (a) is correct.

B b

C c

D d

QUESTION ANALYTICS



Q. 4

Solution Video

Have any Doubt ?



The expression $f = \overline{\overline{AB} + DC + AB + A}$ when reduces, gives

A 0

Correct Option

Solution :
(a)

$$\begin{aligned} f &= \overline{\overline{AB} + DC + AB + A} \\ &= \overline{\overline{A} + \overline{B} + DC + A + A} \\ &= \overline{1 + \overline{B} + DC} \quad (A + \overline{A} = 1) \\ &= 0 \end{aligned}$$

B 1

C $\overline{A + DC}$

D $A + DC$

QUESTION ANALYTICS



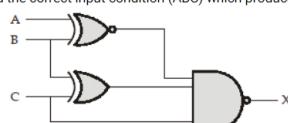
Q. 5

Solution Video

Have any Doubt ?



Find the correct input condition (ABC) which produces X = 0 in the logic circuit shown below:



A 111

B 101

C 100

D 001

Correct Option

Solution :
(d)

To make output at X = 0, all the input to the NAND gate should be 1.

$$X = \overline{(A \oplus B)(B \oplus C)C}$$

- So C must be 1 and B must be 0 to make $(B \oplus C)$ output 1.
- Now B is 0 then A must be 0 to make $(A \oplus B)$ output 1.
- Hence (ABC) must be (001) to get X = 0.

QUESTION ANALYTICS



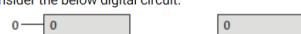
Q. 6

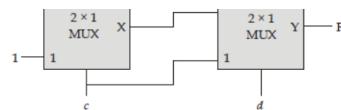
Solution Video

Have any Doubt ?



Consider the below digital circuit.





A $c \oplus d$

B $c \odot d$

C cd

D c

Correct Option

Solution :

(d)

$$\begin{aligned} X &= \bar{c} \cdot 0 + c \cdot 1 = c \\ F &= \bar{d}x + dc \\ &= \bar{d}c + dc \\ &= (\bar{d} + d)c = c \end{aligned}$$

QUESTION ANALYTICS

+

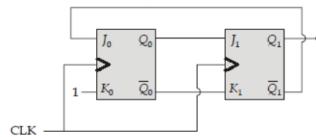
Q. 7

Solution Video

Have any Doubt ?

Q

If the initial state of the counter $Q_1 Q_0$ shown below is 01, then what is the modulus of the counter?



A 1

B 2

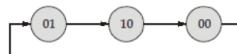
C 3

Correct Option

Solution :

(c)

CLK	Q_1	Q_0	$J_0 = \bar{Q}_1$	$K_0 = 1$	$J_1 = Q_0$	$J_2 = \bar{Q}_0$
0	0	1	1	1	1	0
1	1	0	0	1	0	1
2	0	0	1	1	0	1
3	0	1				



The number of state $N = 3$

D 4

QUESTION ANALYTICS

+

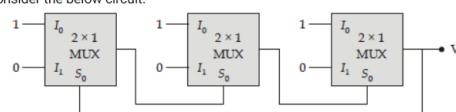
Q. 8

Solution Video

Have any Doubt ?

Q

Consider the below circuit:



The propagation delay of each multiplexer is 50 ns. The frequency of the output signal V is

A 4 MHz

B 3.33 MHz

Correct Option

Solution :

(b)

Each MUX is acting as a NOT gate thus it is ring oscillator with 3 NOT gates.

$$\text{Hence, } f = \frac{1}{2Nt_{pd}}$$

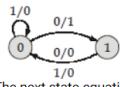
$$f = \frac{1}{2 \times 3 \times 50 \text{ ns}} = \frac{10^3 \times 10^6 \text{ Hz}}{300} = 3.33 \text{ MHz}$$

C 5 MHz

Q. 9

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider the below state diagram:



The next state equation of the above flip-flop will be when Y represents input is

A $\overline{Y - Q_n}$

B $Y \oplus Q_n$

C YQ_n

D $\overline{Y + Q_n}$

Correct Option

Solution :
(d)

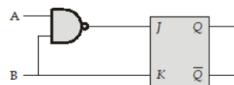
Present state (Q_n)	Input (Y)	Next state (Q_{n+1})
0	1	0
0	0	1
1	1	0
1	0	0

$$Q_{n+1} = \overline{Q_n + Y}$$

Q. 10

[▶ Solution Video](#)[Have any Doubt ?](#)

An AB flip-flop is constructed from a JK flip-flop as shown in the below figure. The expression for the next state Q_{n+1} is



A $\overline{B} + \overline{A}\bar{Q}_n$

Correct Option

Solution :
(a)

A	B	J	K	Q_{n+1}
0	0	1	0	1
0	1	1	1	\bar{Q}_n
1	0	1	0	1
1	1	0	1	0

$$\begin{aligned} Q_{n+1} &= \overline{AB} + \overline{A}\bar{B}\bar{Q}_n + A\bar{B} \\ &= \overline{B} + \overline{A}\bar{B}\bar{Q}_n \\ &= \overline{B} + \overline{A}\bar{Q}_n \end{aligned}$$

B $AB + A\bar{B} + \bar{A}\bar{B}\bar{Q}_n$

C $\overline{AB} + Q_n$

D $\overline{AB} + \overline{A}\bar{B} + \bar{A}\bar{B}\bar{Q}_n$



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ALL(33) CORRECT(0) INCORRECT(0) SKIPPED(33)

Q. 11

Solution Video

Have any Doubt ?



Given that $306_{10} = 615$ in some number system. The base of such system will be _____.

7

Correct Option

Solution :

7

$$(306)_{10} = (615)_x$$

$$306 = 6x^2 + x + 5$$

By substitution, $x = 7$ equate the equation
 So the base will be 7.

QUESTION ANALYTICS



Q. 12

Solution Video

Have any Doubt ?



If the number of unused states in K-bit Johnson counter is 52, then the number of unused states when ring counter is implemented using same K-bit flip-flop is _____.

58

Correct Option

Solution :

58

$$\text{Number of unused state in Johnson counter} = 2^K - 2K$$

$$= 2^K - 2K = 52$$

By substitution $K = 6$

$$\text{Now, number of unused state in ring counter} = 2^K - K$$

$$= 2^6 - 6 = 58$$

QUESTION ANALYTICS



Q. 13

Solution Video

Have any Doubt ?



A modulo-8 ripple counter uses J-K flip-flops. If the propagation delay of each flip-flop is x ns and the maximum clock frequency that can be used is 4 MHz, then the value of x is _____ (Upto 2 decimal places)

83.33 [83.30 - 83.40]

Correct Option

Solution :

83.33 [83.30 - 83.40]

Number of flip-flops for mod-8 ripple counter = 3

$$\text{Maximum clock frequency} = f = \frac{1}{T}$$

$$\Rightarrow 4 \text{ MHz} = \frac{1}{3 \times x \text{ ns}} \text{ Hz}$$

$$\Rightarrow 4 \times 10^6 \text{ Hz} = \frac{10^9}{3 \times x} \text{ Hz}$$

$$\Rightarrow x = \frac{10^9}{4 \times 10^6 \times 3} = \frac{10^3}{12} = 83.33$$

QUESTION ANALYTICS



Q. 14

Solution Video

Have any Doubt ?



The value denoted by 110000100111100000 ... 0 in IEEE 754. Signal precision standard in decimal is _____.

-62

Correct Option

Solution :

-62

Format	1 bit	8 bit	23 bit
	Sign	Exponent	Mantissa
			32
	1	1000100	11110000...0

$$= (-1)^s (1.E) \times 2^{E-127}$$

$$= (-1)^1 (1.1111) \times 2^{132-127}$$

$$= -(1.111) \times 2^5$$

$$= -(62)_{10}$$

QUESTION ANALYTICS

+

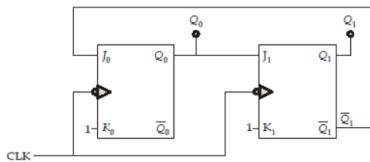
Q. 15

Solution Video

Have any Doubt ?

?

Consider the following counter:



The number of states present in above counter is _____.

3

Correct Option

Solution :

3

Initial state	FF1		FF0				
	CLK	Q ₁	Q ₀	J ₁ = Q ₀	K ₁ = 1	J ₀ = Q̄ ₁	K ₀ = 1
1	0	0	1	1	1	1	1
2	1	0	1	1	1	1	1
3	0	0	0	0	1	0	1

Counter is switching in the sequence 0 → 1 → 2 → 0 → 1 → 2

∴ Number of states present in the counter are 3.

QUESTION ANALYTICS

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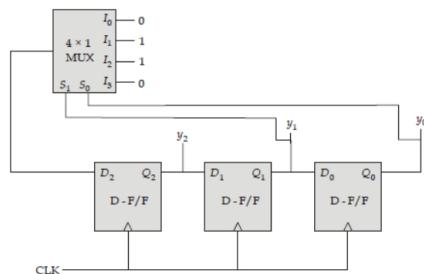
Q. 16

Solution Video

Have any Doubt ?

?

A three bit pseudo random number generator is shown in the figure. Initially the value of output $y = y_2y_1y_0$ is set to 111.



The value of output y after three clock cycles is _____.

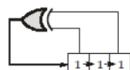
100

Correct Option

Solution :

100

The 4 : 1 MUX acts as an XOR gate and the figure/circuit can be simplified as



CLK cycle	y ₂	y ₁	y ₀
0 th	1	1	1
1 st	0	1	1
2 nd	0	0	1
3 rd	1	0	0

After 3rd clock cycles, y is 100.

QUESTION ANALYTICS

+

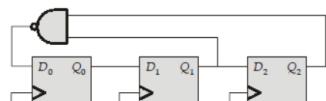
Q. 17

Solution Video

Have any Doubt ?

?

In the circuit shown below, initially all flip-flops are reset. The output $Q_2Q_1Q_0$ after three clock pulses is





A 011

B 111

Correct Option

Solution :
(b)
In the circuit we have

$$D_0 = \overline{Q_1 Q_2} = \bar{Q}_1 + \bar{Q}_2$$

$$D_1 = Q_0$$

$$D_2 = Q_1$$

	Present input			Input			Next state		
CLK	Q_2	Q_1	Q_0	D_2	D_1	D_0	Q_2^*	Q_1^*	Q_0^*
0	0	0	0	-	-	-	-	-	-
1	0	0	0	0	0	1	0	0	1
2	0	0	1	0	1	1	0	1	1
3	0	1	1	1	1	1	1	1	1

After 3 clock pulses output $Q_2 Q_1 Q_0 = 111$

C 011

D 110

QUESTION ANALYTICS



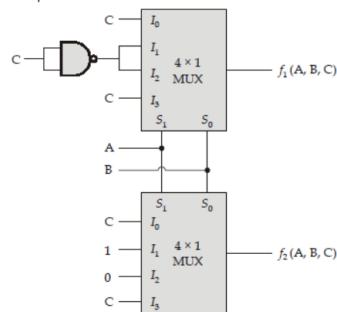
Q. 18

Solution Video

Have any Doubt ?



The multiplexer circuit shown below will function as a



A Full adder

B Full subtractor

Correct Option

Solution :
(b)
For 1st 4 × 1 MUX

$$\begin{aligned} f_1(A, B, C) &= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC \\ &= \Sigma m(1, 2, 4, 7) \end{aligned}$$

For 2nd 4 × 1 MUX

$$\begin{aligned} f_2(A, B, C) &= \bar{A}\bar{B}C + \bar{A}B \cdot 1 + A\bar{B} \cdot 0 + ABC \\ &= \Sigma m(1, 2, 3, 7) \end{aligned}$$

- $f_1(A, B, C)$ represents difference of full subtractor.
- $f_2(A, B, C)$ represents borrow of full subtractor.

C Half adder

D Half subtractor

QUESTION ANALYTICS



Q. 19

Solution Video

Have any Doubt ?



For the map shown below, the minimized logical expression in sum of product (SOP) form is

	CD	00	01	10	11
AB	00	1		1	1
	01				
	10		1	1	
	11	1	1	1	1

A $\bar{B}\bar{D} + AD + AC$

B $AB + AD + \bar{B}\bar{D}$

C $AB + A\bar{C}D + AC\bar{D} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{D}$

Correct Option

Solution :
(c)

		CD	00	01	10	11
		AB	00	1	1	1
			01			
			10		1	1
			11	1	1	1

$$F(A, B, C, D) = AB + A\bar{C}D + AC\bar{D} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{D}$$

D $\bar{A}\bar{B}\bar{C} + AC + \bar{A}\bar{B}\bar{D}$

 QUESTION ANALYTICS

+

Q. 20

 Solution Video

 Have any Doubt ?

Bookmark

Consider the following boolean function:

$$Y = (B + C)(\bar{A} + \bar{D})$$

The minimum number of 2 input NAND gates required to implement the above function is

A 3

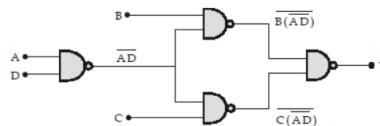
B 4

Correct Option

Solution :
(b)

$$\begin{aligned} Y &= (B + C)(\bar{A} + \bar{D}) = (B + C)(\bar{A}\bar{D}) \\ &= B(\bar{A}\bar{D}) + C(\bar{A}\bar{D}) \end{aligned}$$

Implementation is as follows:



$$\begin{aligned} Y &= \overline{\overline{B}(\overline{A}\overline{D})} \times \overline{\overline{C}(\overline{A}\overline{D})} \\ &= B(\overline{A}\overline{D}) + C(\overline{A}\overline{D}) \\ &= (B + C)(\overline{A}\overline{D}) \\ &= (B + C)(\bar{A} + \bar{D}) \end{aligned}$$

C 5

D 6

 QUESTION ANALYTICS

+

Item 11-20 of 33

« previous

1

2

3

4

next »



Kunal Jha

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[SOLUTION REPORT](#)
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Q. 21
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Consider a J/K flip-flop with $J = Q'$ and $K = 1$. Assuming that the flip-flop was initially cleared and then clocked for 6 pulses. What will be the sequence of bits at the output Q ?

A 011001

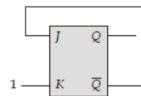
B 100100

C 101010

Correct Option

Solution :

(c)



	J	K	Q	\bar{Q}
1	1	1	1	0
2	0	1	0	1
3	1	1	1	0
4	0	1	0	1
5	1	1	1	0
6	0	1	0	1

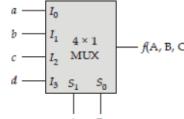
The output Q will be 101010.

D 010010

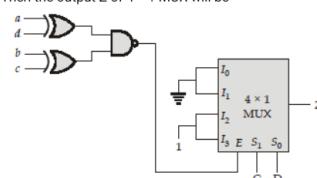
[QUESTION ANALYTICS](#)

Q. 22
[▶ Solution Video](#)
[Have any Doubt ?](#)


Given $f(A, B, C) = \sum m(0, 1, 4, 5)$ for the given 4×1 MUX



Then the output Z of 4×1 MUX will be


A 0

Correct Option

Solution :

(a)

For the given 4×1 MUX, 'A' and 'B' are select lines and 'C' be the input

I_0	I_1	I_2	I_3
0	2	4	6
1	3	5	7

So,

$$I_0 = 1 = a$$

$$I_1 = 0 = b$$

$$I_2 = 1 = c$$

$$I_3 = 0 = d$$

So,

$$a \oplus d = b \oplus c = 1$$

So, output of NAND gate is 0 i.e. MUX 'E' connected to '0'.

The MUX is in disable state. MUX is having active high enable, but E = 0, so that MUX is in disable state.

Hence MUX output Z is equal to '0'.

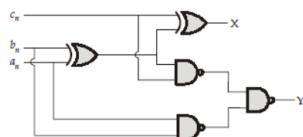
B $C\bar{D}$
C CD

D 1

Q. 23

[▶ Solution Video](#)[Have any Doubt ?](#)

A circuit is shown below:



The propagation time for each NAND gate is 10 nsec. What is the time required to get the output Y (in nsec). (Assume that all other gates are implemented using minimum number of NAND gates)

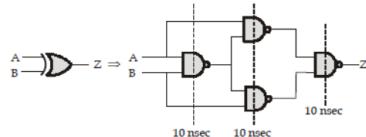
 A 20 B 40 C 50

Correct Option

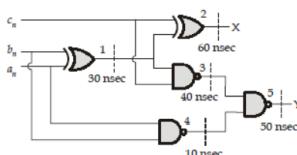
Solution :

(c)

An Ex-OR gate can be represented as



So, for EX-OR gate, it will take 30 nsec to get the output.



So, to get the output Y, it will take 50 nsec.

 D 60

Q. 24

[▶ Solution Video](#)[Have any Doubt ?](#)

For synchronous series counter of modulus 256, the propagation delay for each flip flop is 25 nsec and propagation delay of each two input AND gate is 5 nsec. What is the maximum frequency of the MOD-256 counter? (in MHz)

 A 18.18

Correct Option

Solution :

(a)

The total delay for synchronous series counter

$$= t_{pd} \text{ (of FF)} + (n - 2) t_{pd} \text{ (of AND gate)}$$

where

n = Number of flip-flops

As

M $\leq 2^n$ (Where M = modulus)

So,

256 $\leq 2^n$

n = 8

Total delay = 25 + (8 - 2) 5

$$= 25 + 30 = 55 \text{ nsec}$$

So, the maximum frequency of MOD-256 counter will be

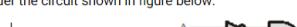
$$= \frac{1}{55 \text{ nsec}} = 18.18 \text{ MHz}$$

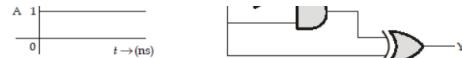
 B 19.18 C 20.19 D 17.18

Q. 25

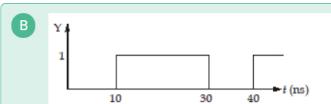
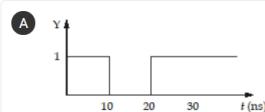
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Consider the circuit shown in figure below:



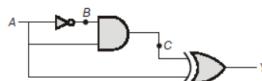


If propagation delay of NOT gate is 10 nsec, AND gate is 20 nsec and X-OR gate is 10 nsec. If A is connected to V_{CC} at $t = 0$, then waveform for output Y is

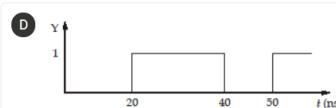
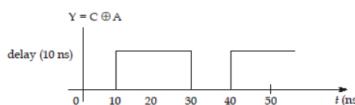
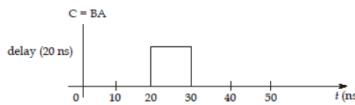
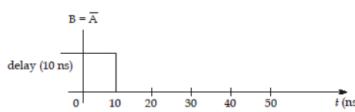
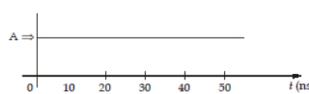


Correct Option

Solution :
(b)



	A	B	C	Y
0 < t < 10 ns	1	1	0	0
10 ns < t < 20 ns	1	0	0	1
20 ns < t < 30 ns	1	0	1	1
30 ns < t < 40 ns	1	0	0	0
40 ns < t	1	0	0	1



QUESTION ANALYTICS



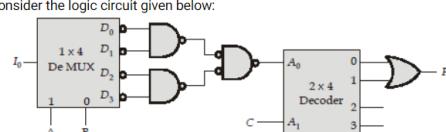
Q. 26

Solution Video

Have any Doubt ?



Consider the logic circuit given below:



The minimized expression for F is

A \bar{C}

Correct Option

Solution :
(a)

$$\begin{aligned} F &= \bar{A}_1 \bar{A}_0 + \bar{A}_1 A_0 \\ &= \bar{A}_1 \\ \text{where, } A_1 &= C \\ \therefore F &= \bar{C} \end{aligned}$$

B I_0

C C

D \bar{I}_0

QUESTION ANALYTICS



Q. 27

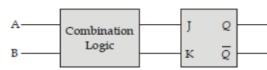
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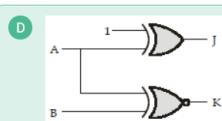
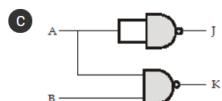
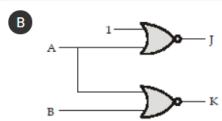
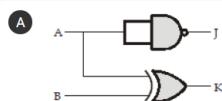


A new two input flip flop is designed as shown in figure. The table shows the characteristic table of the A-B flip-flop.

A	B	Q_{n+1}
0	0	\bar{Q}_n
0	1	1
1	0	Q_n
1	1	0



The combination logic is



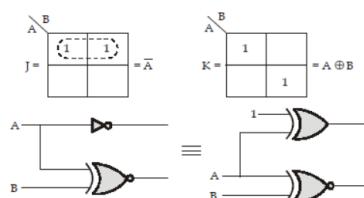
Correct Option

Solution :

(d)

State Table

A	B	Q_{n+1}	J	K
0	0	\bar{Q}_n	1	1
0	1	1	1	0
1	0	Q_n	0	0
1	1	0	0	1



QUESTION ANALYTICS



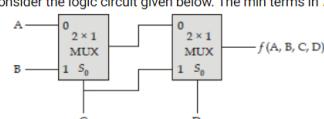
Q. 28

Solution Video

Have any Doubt ?



Consider the logic circuit given below. The min terms in $f(A, B, C, D)$ are



A $\Sigma m(1, 3, 5, 6, 7, 11, 14)$

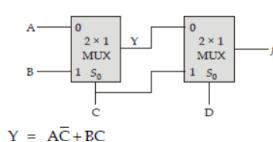
B $\Sigma m(3, 6, 7, 8, 10, 12, 14, 15)$

C $\Sigma m(3, 6, 7, 8, 11, 12, 14, 15)$

Correct Option

Solution :

(c)



$$Y = A'C + BC$$

$$f = Y\bar{D} + CD$$

$$f = (A\bar{C} + BC)\bar{D} + CD = A\bar{C}\bar{D} + BCD + CD$$

			CD
		1	
		1	1
1		1	1
1		1	

$$f(A, B, C, D) = \Sigma m(3, 6, 7, 8, 11, 12, 14, 15)$$

D $\Sigma m(3, 6, 7, 9, 11, 12, 14, 15)$

QUESTION ANALYTICS



Q. 29

Solution Video

Have any Doubt ?



Two 4-bit shift register are cascaded as shown in below figure.



A 4-bit input 1001 is applied, then after how many clock pulses the same 4-bit data will appear at the output _____.

8

Correct Option

Solution :

	SIPO	PISO
Initially	0 0 0 0	0 0 0 0
CLK		
1	1 0 0 0	0 0 0 0
2	0 1 0 0	1 0 0 0
3	0 0 1 0	0 1 0 0
4	1 0 0 1	0 0 1 0
5		1 0 0 1
6		x 1 0 0
7		x x 1 0
8		x x x 1

So, after 8 pulses the output from PISO will be same as input in SIPO.

QUESTION ANALYTICS



Q. 30

Solution Video

Have any Doubt ?



The minimum number of 2-input NOR gates required to implement the boolean function $F = \bar{X}Z + \bar{X}W + \bar{Y}Z + \bar{Y}W$ is _____.

5

Correct Option

Solution :

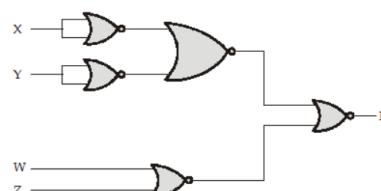
5

$$F = \bar{X}Z + \bar{X}W + \bar{Y}Z + \bar{Y}W$$

K-map

	WZ	00	01	11	10
XY		0	1	1	1
00		0	1	1	1
01		0	1	1	1
11		0	0	0	0
10		0	1	1	1

$$F = (\bar{X} + \bar{Y})(W + Z)$$



Total 5 NOR gates are required.

QUESTION ANALYTICS





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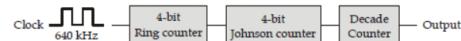
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Q. 31
[Solution Video](#)
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If the input frequency applied to given system is 640 kHz then the output frequency will be _____ kHz.


2
[Correct Option](#)
Solution :
2

Given, Input frequency = 640 kHz

$$\text{Output frequency after 4-bit ring counter} = \frac{640}{4} = 160 \text{ kHz}$$

$$\text{Output frequency after 4-bit Johnson counter} = \frac{160}{8} = 20 \text{ kHz}$$

$$\text{Output frequency after decade counter} = \frac{20}{10} = 2 \text{ kHz}$$

[QUESTION ANALYTICS](#)

Q. 32
[Solution Video](#)
[Have any Doubt ?](#)


Consider the logical functions given below:

$$f_1(A, B, C) = \Sigma(2, 3, 4)$$

$$f_2(A, B, C) = \Pi M(0, 1, 3, 6, 7)$$



If f is logic zero, then maximum number of possible minterms in function f_3 are _____.

6
[Correct Option](#)
Solution :
6

$$f_1(A, B, C) = \Sigma(2, 3, 4)$$

$$f_2(A, B, C) = \Pi M(0, 1, 3, 6, 7) = \Sigma(2, 4, 5)$$

$$f_1 \cdot f_2 = \Sigma m(2, 4)$$

For function f to be zero

$$f_3 = \Pi M(2, 4)$$

$$f_3(A, B, C) = \overline{[f_1(A, B, C) \cap f_2(A, B, C)]}$$

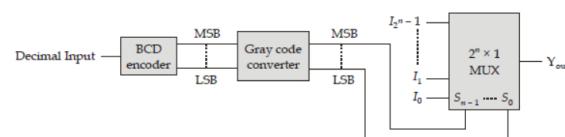
$$= \Sigma(0, 1, 3, 5, 6, 7)$$

Maximum minterms possible are 6.

[QUESTION ANALYTICS](#)

Q. 33
[Solution Video](#)
[Have any Doubt ?](#)


Consider the circuit given below:



If the decimal input is 89 then Y_{out} corresponds to I_m , then the value of m is _____.

205
[Correct Option](#)
Solution :
205

$$\text{Decimal input} = 89$$

$$\text{BCD} = 1000\ 1001$$

$$\text{Gray code output} = 11001101$$

$$\text{Select lines } (S_{n-1} \dots S_1 S_0) = (11001101)_2 = 205$$

Y_{out} corresponds to I_m so the m is 205.

[QUESTION ANALYTICS](#)