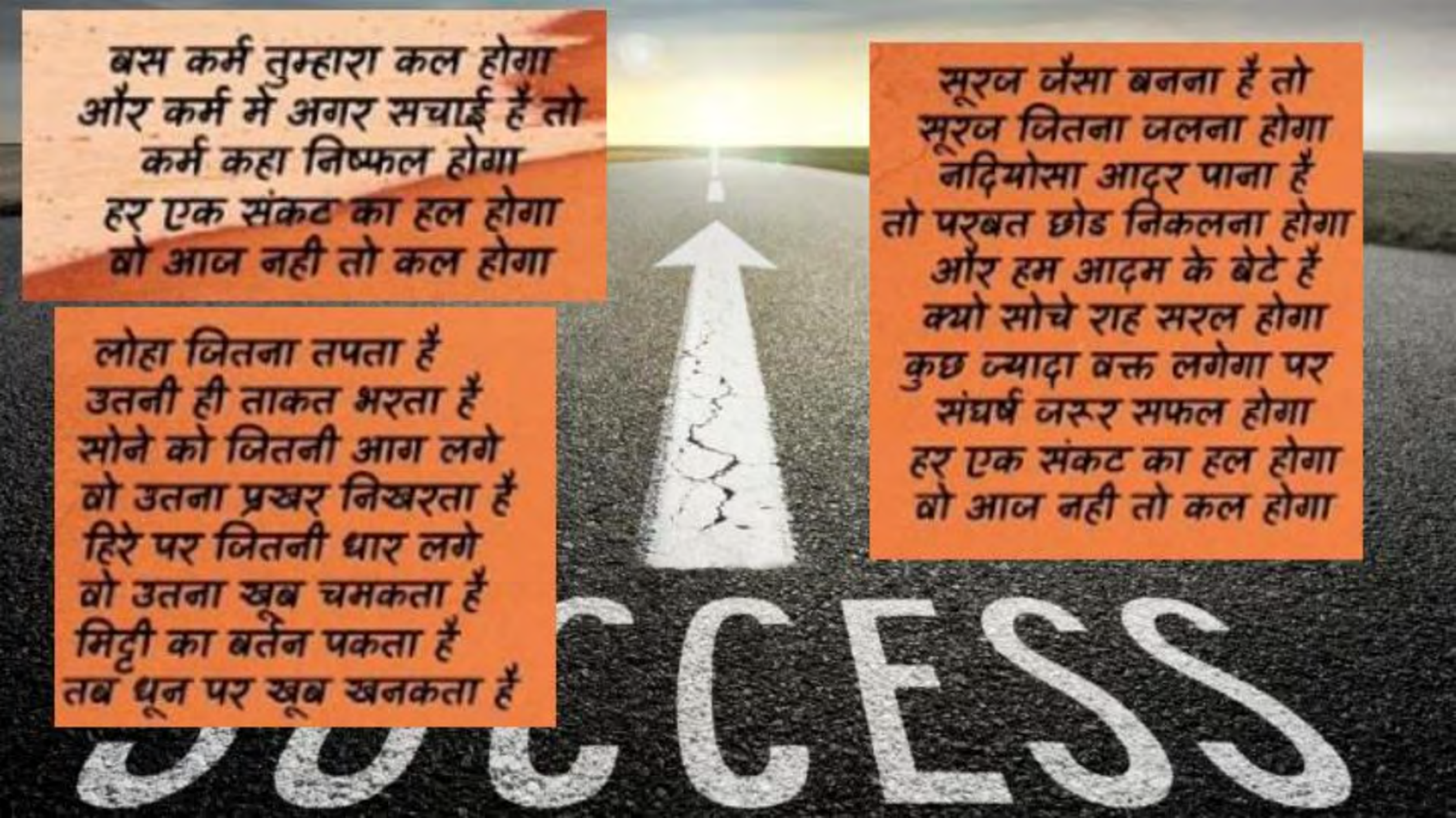
EC/EE/CS & IT/IN

Digital Electronics

Combinational circuit - Parallel Adder

LECTURE NO. 6

Chandan Jha Sir (CJ Sir)


बस कर्म तुम्हारा कल होगा
और कर्म मे अगर सचाई है तो
कर्म कहा निष्फल होगा
हर एक संकट का हल होगा
वो आज नही तो कल होगा
लोहा जितना तपता है
उतनी ही ताकत भरता है
सोने को जितनी आग लगे
वो उतना प्रखर निखरता है
हिरे पर जितनी धार लगे
वो उतना खूब चमकता है
मिट्टी का बर्तन पकता है
तब धून पर खूब खनकता है
सूरज जैसा बनना है तो
सूरज जितना जलना होगा
नदियोसा आदर पाना है
तो परबत छोड निकलना होगा
और हम आदम के बेटे है
क्यो सोचे राह सरल होगा
कुछ ज्यादा वक्त लगेगा पर
संघर्ष जरूर सफल होगा
हर एक संकट का हल होगा
वो आज नही तो कल होगा
CCESS

QUESTION

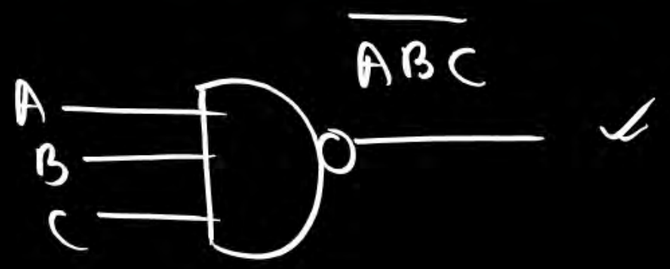
The combinational circuit given below implements which of the following

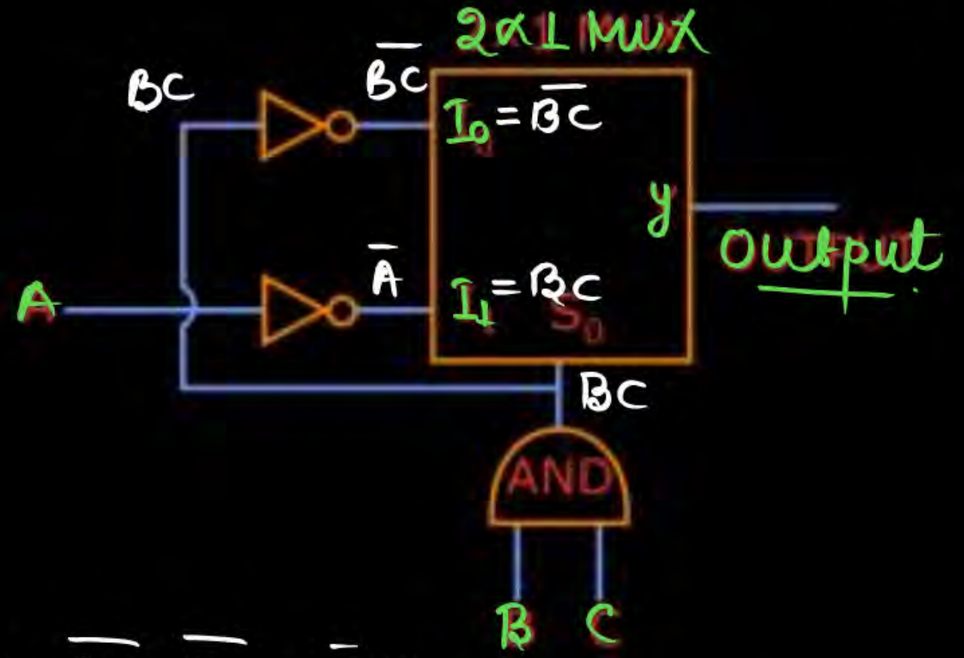
A. NAND

B. NOR

C. X OR

D. NONE





$$y = \overline{BC}\cdot\overline{BC} + \overline{A}BC$$

$$= \overline{BC} + \overline{A}BC \qquad (BC = X)$$

$$= \overline{X} + \overline{A}X = (\overline{A}+\overline{X})(\overline{X}+X)$$

$$= \overline{A} + \overline{X}$$

$$= \overline{A\cdot X} = \overline{A\cdot BC}$$

QUESTION

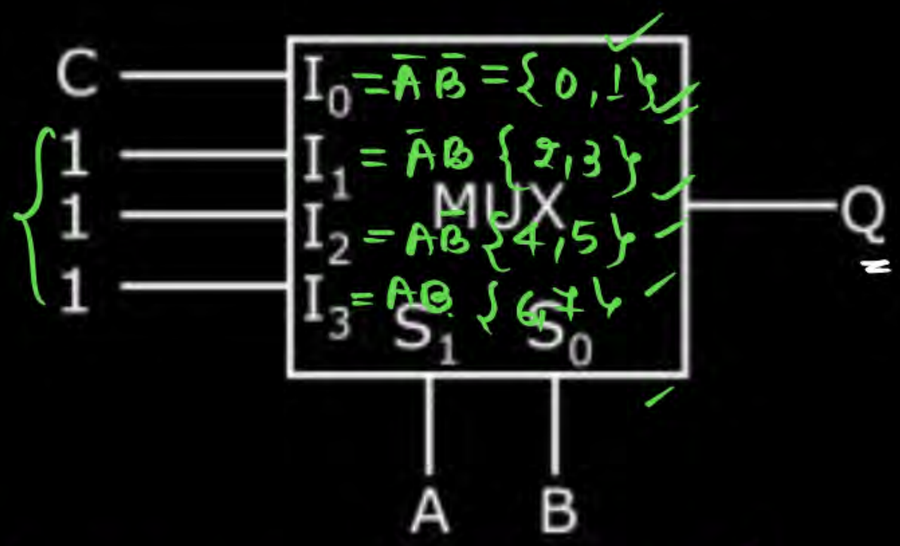
The combinational circuit given below, output Q will be

A. $A \oplus B \oplus C$

B. ABC

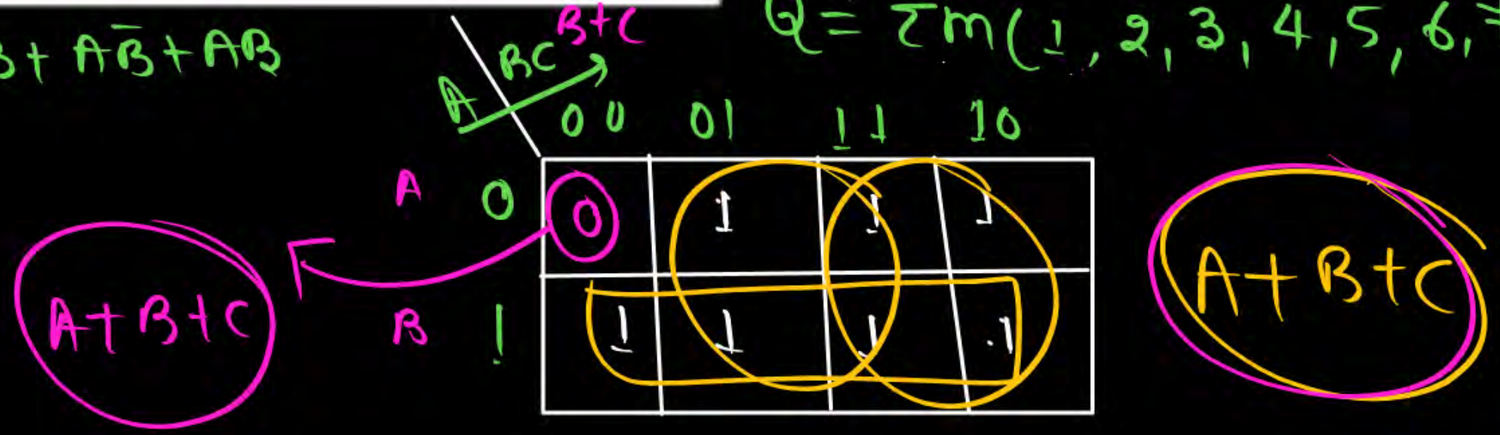
C. AB+C

D. A+B+C



$Q = \bar{A}\bar{B}C + \bar{A}B + A\bar{B} + AB$

$Q = \Sigma m(1,2,3,4,5,6,7)$



QUESTION

In 8 bit comparator total number of combination will be

- A. 128K
- B. 64K
- C. 32K
- D. none

'n' bit comparator

2^{2n}

$2^{2\times 8} = 2^{16} \Rightarrow 2^6 \cdot 2^{10}$

$\Rightarrow$ 64 K

$2^{10} = K$

$2^{20} = M$

$2^{30} = G$

ABOUT ME

- Cleared Gate Multiple times with double Digit Rank (AIR 23, AIR 26)
- Qualified ISRO Exam
- Mentored More then 1 Lakhs+ Students (Offline & Online)
- More then 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs

Chandan Jha

RECAPE

Comparator

n bit comparator

T.C = 2^{2n}

Equal ⇒ 2^n

Unequal com ⇒ $2^{2n} - 2^n$

Greater = Less = $\frac{2^{2n} - 2^n}{2}$

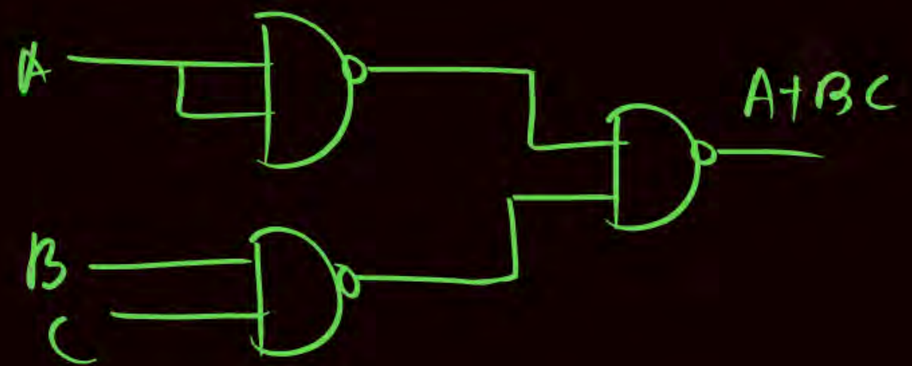
Semiminimized Expression

A > B : $A_1\bar{B}_1 + (A_1 \odot B_1)A_0\bar{B}_0$

A < B : $\bar{A}_1B_1 + (A_1 \odot B_1)\bar{A}_0B_0$

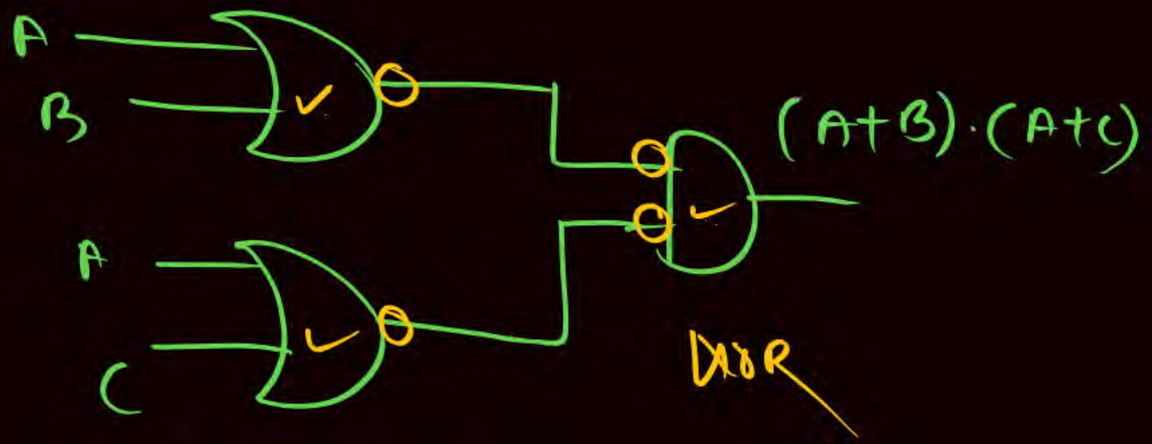
A = B : $(A_1 \odot B_1)(A_0 \odot B_0)$

$A+BC$



(3)

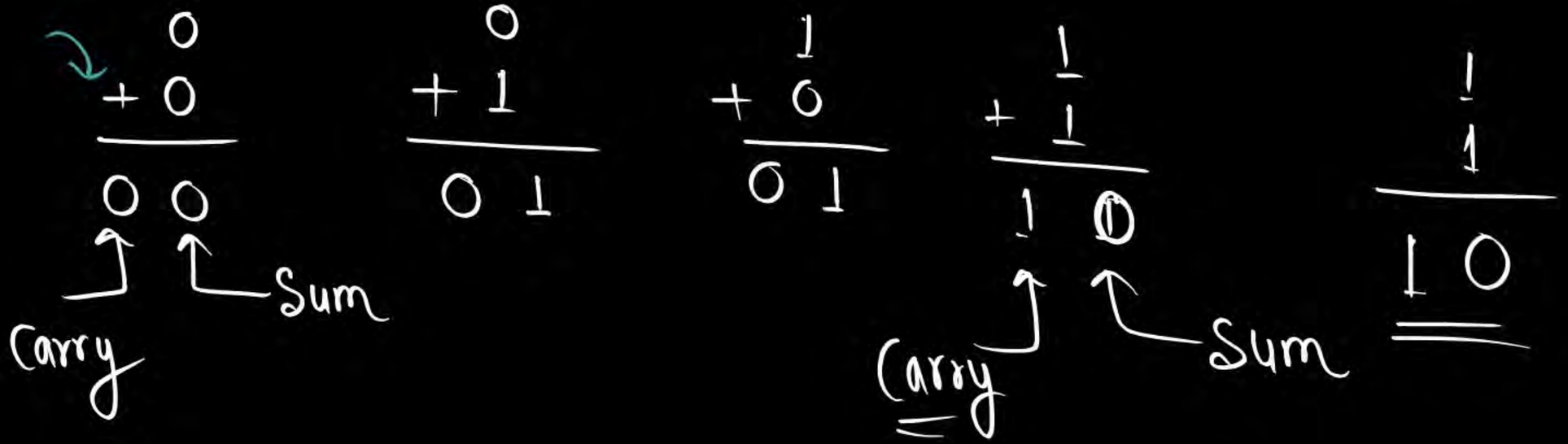
$A+BC = (A+B)(A+C)$



(3)

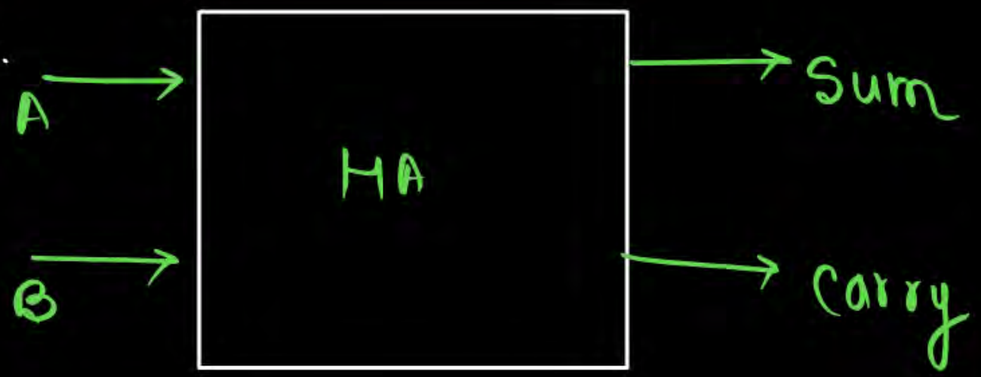
HALF ADDER

→ 2 bit adder



HALF ADDER

Step-1.



Step-2.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

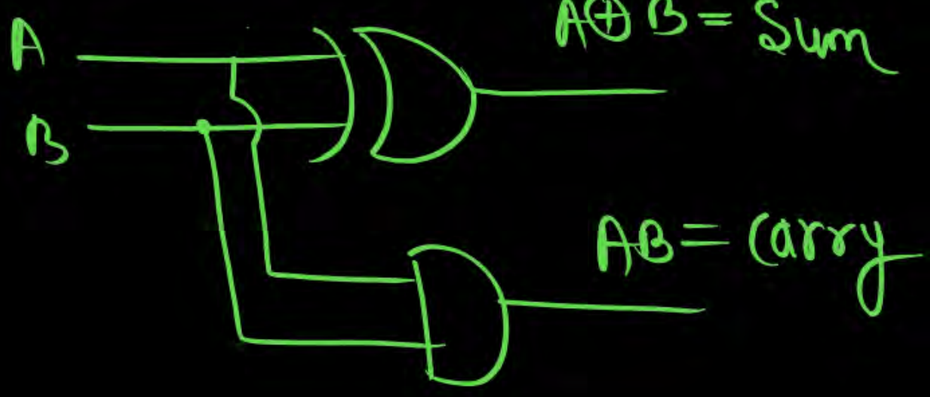
Step 3. $Sum = \bar{A}B + A\bar{B} = A \oplus B$

$Carry = AB$

Step 4.

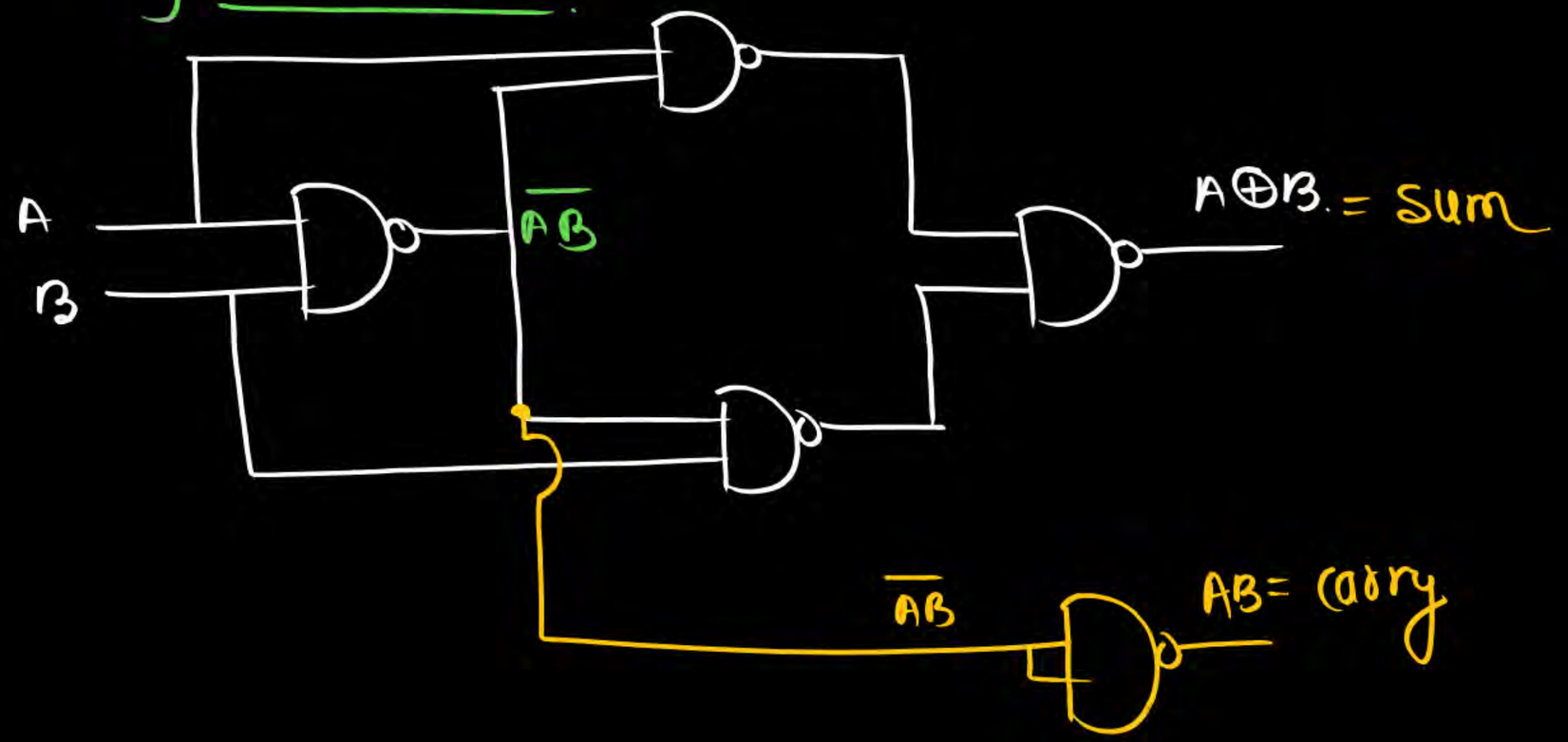
~~6~~ 5

Step 5.



HALF ADDER

By NAND GATE



5

NOR

5

FULL ADDER

Step 2:

	A	B	C	Sum	Carry
0	0	0	0	0	0
1	0	0	1	1	0
2	0	1	0	1	0
3	0	1	1	0	1
4	1	0	0	1	0
5	1	0	1	0	1
6	1	1	0	0	1
7	1	1	1	1	1

Step3 & Step4

$$Sum = \Sigma m(1,2,4,7) = A \oplus B \oplus C$$

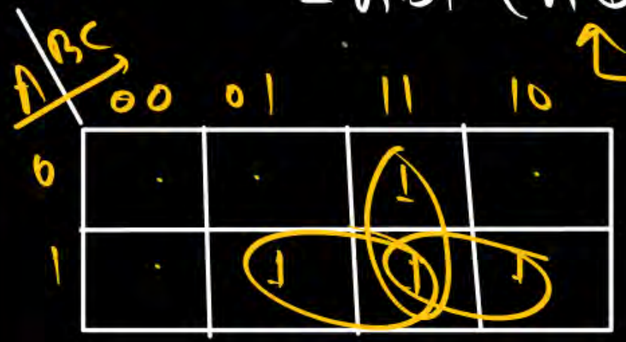
$$Carry = \Sigma m(3,5,6,7)$$

$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= (\bar{A}B + A\bar{B})C + AB(\bar{C} + C)$$

$$= AB + (A \oplus B) \cdot C$$

Semiminimized



$$= AB + BC + AC$$

HALF ADDER/SUBTRACTOR

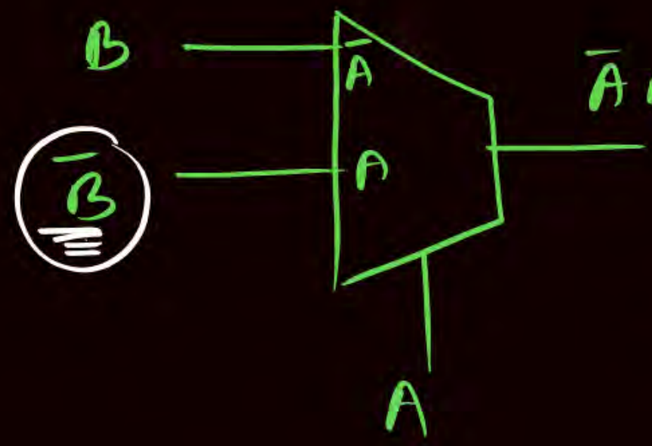
Sum = A ⊕ B

Carry = AB

NAND/NOR

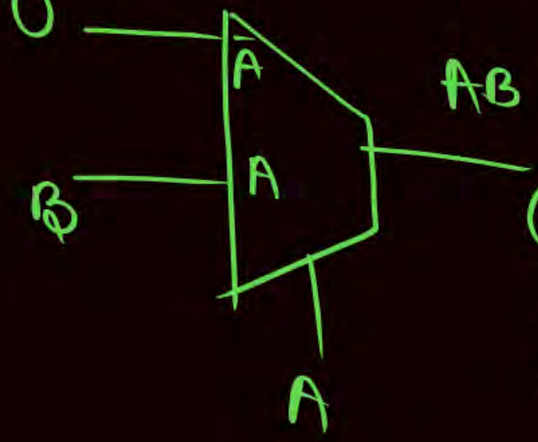
Q+

2X1 MUX → ? → HALF ADDER



$\bar{A}B + A\bar{B} = A \oplus B$

Sum



AB

Carry

1

FULL ADDER

→ 3 bit adder

$$\begin{array}{r} 0\,0 \\ 0\,0 \\ +\;\;0 \\ \hline 0\,0 \end{array}$$

carry ← 0 0 → sum

$$\begin{array}{r} 0\,0 \\ 0\,0 \\ +\;\;1 \\ \hline 0\,1 \end{array}$$

$$\begin{array}{r} 0\,0 \\ 0\,1 \\ +\;\;1 \\ \hline 1\,0 \end{array}$$

$$\begin{array}{r} 1\,1 \\ 1\,1 \\ +\;\;1 \\ \hline 1\,1 \end{array}$$

Step 1

Full adder

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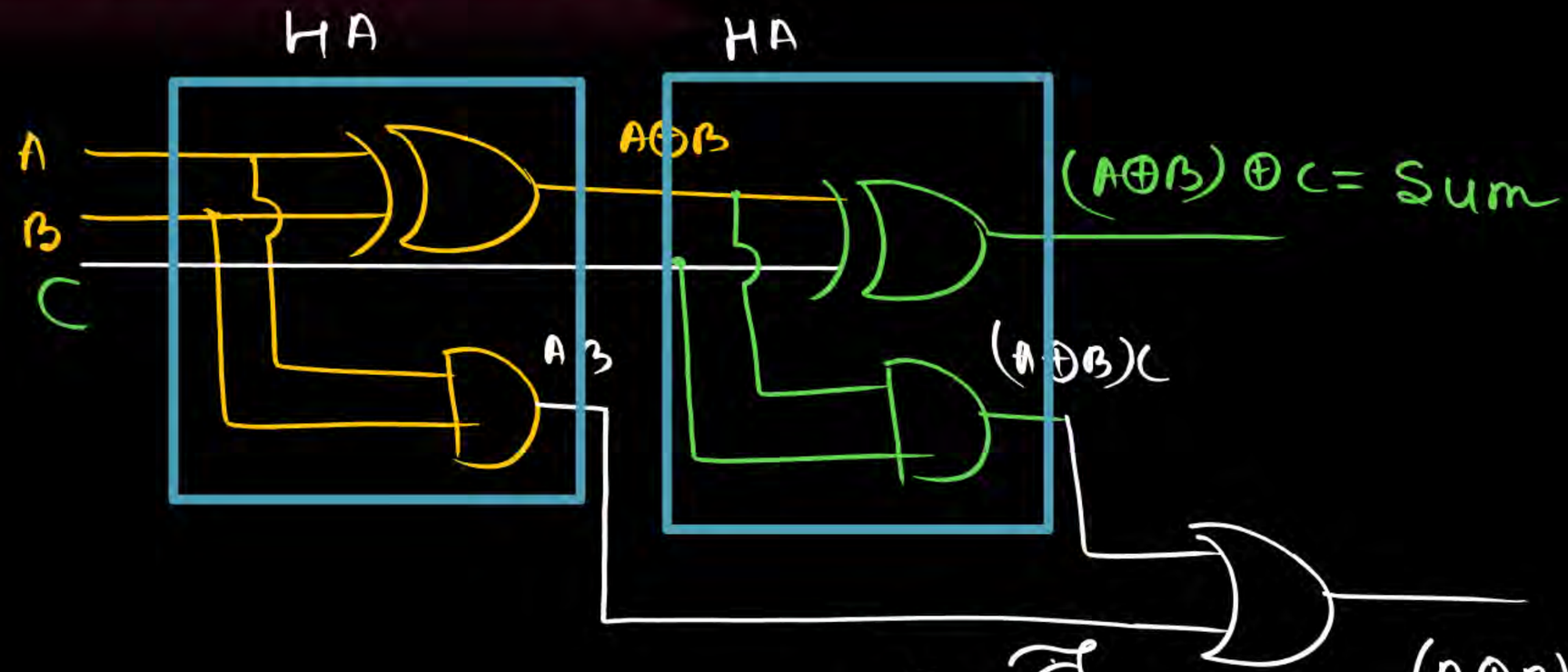
Sum $= A \oplus B \oplus C$

$$\text{Carry} = AB + BC + AC$$
$$= (A \oplus B)C + AB$$
$$= \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

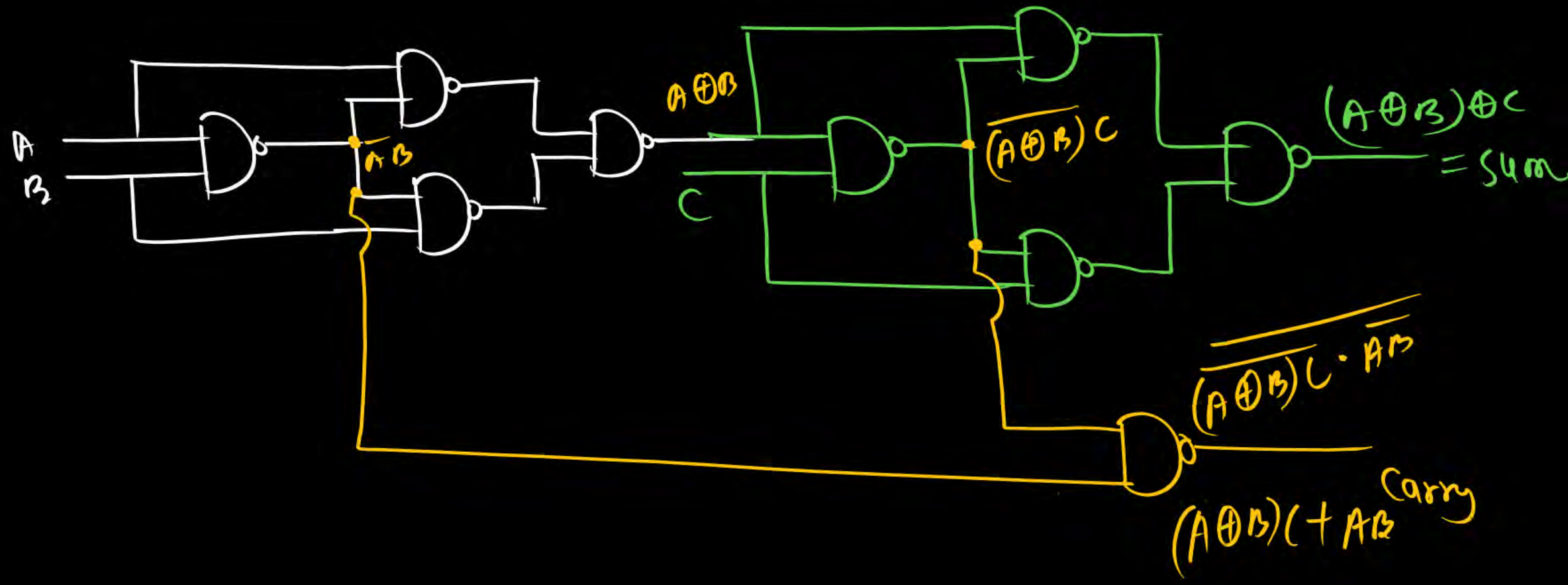
FULL ADDER



1 Full adder = 2 HA + 1 OR

FULL ADDER

→ Number of NAND = 9



QUESTION

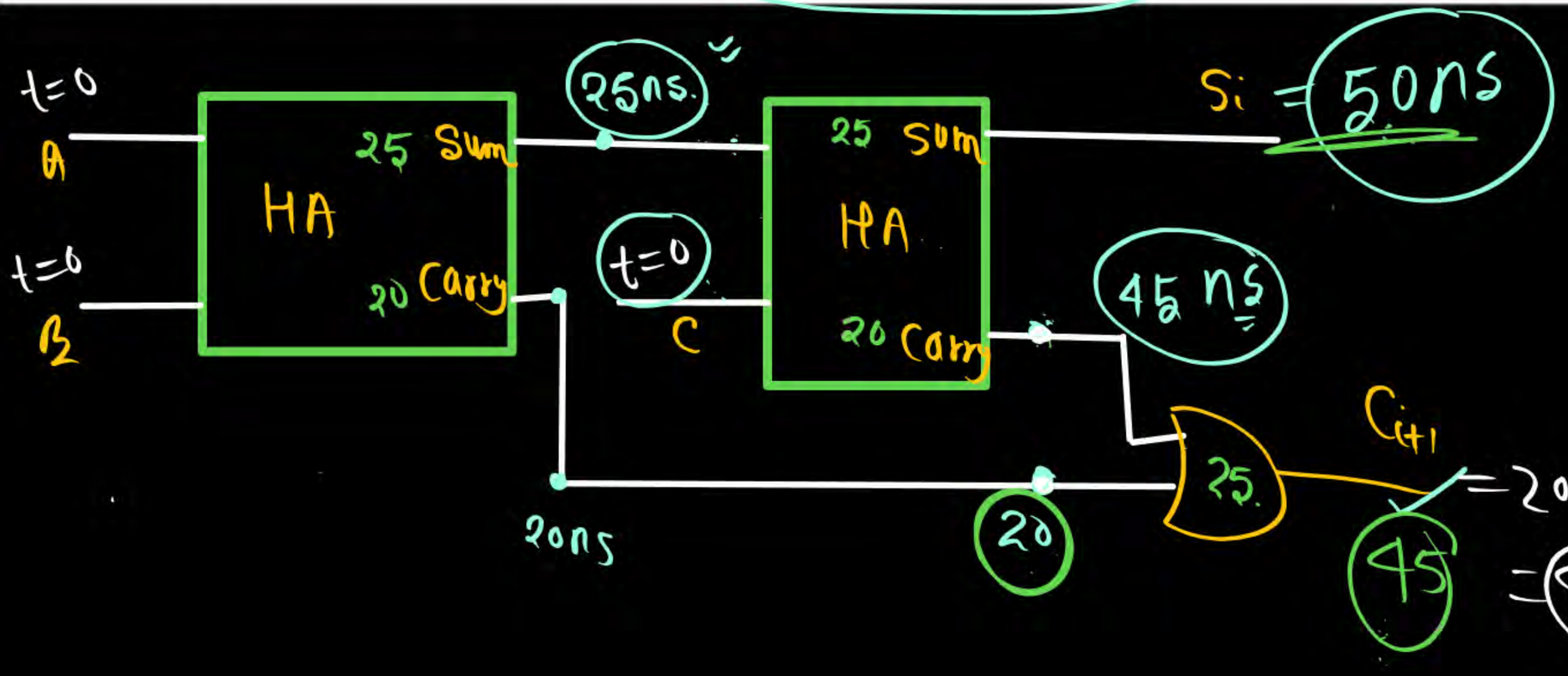
$T_{sum} = 50ns$ $T_{carry} = 45\ ns$

A full adder is implemented with two half adders and one OR gate. OR gate is used to derive the final carry function of full adder. In each half adder, T_{sum} = 25ns and T_{carry} = 20ns and T_{OR} = 25ns.

The minimum time required to derive both the sum and carry function of a full adder after applying the inputs is _____ ns

Maximum Time

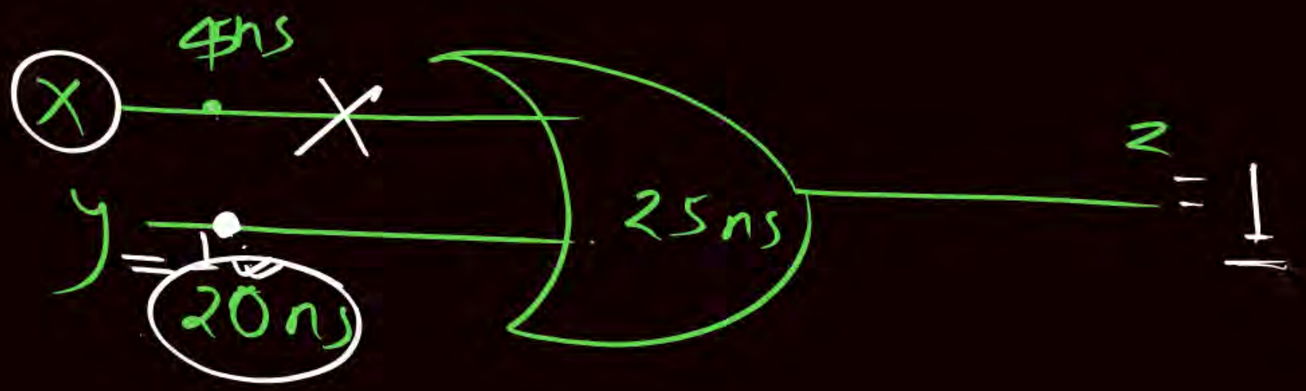
70ns



Minimum Time

20+25=45ns

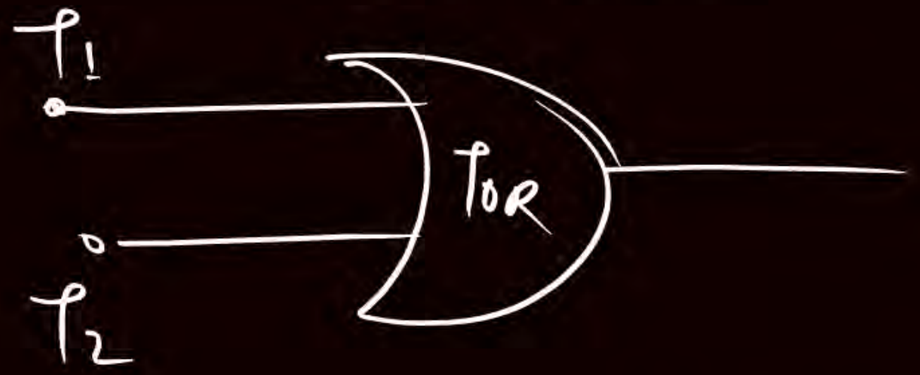
50ns



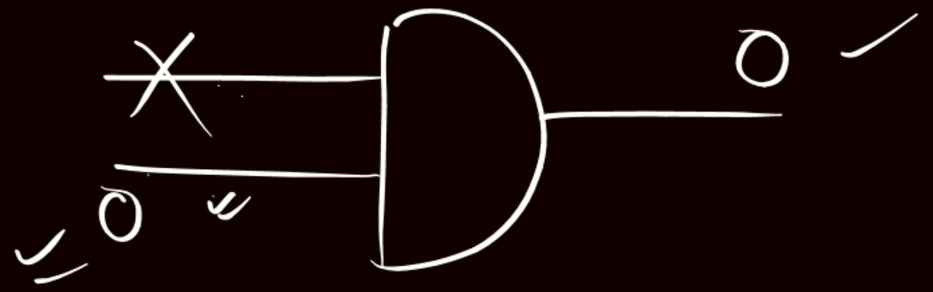
minimum Delay

#DEC

min delay



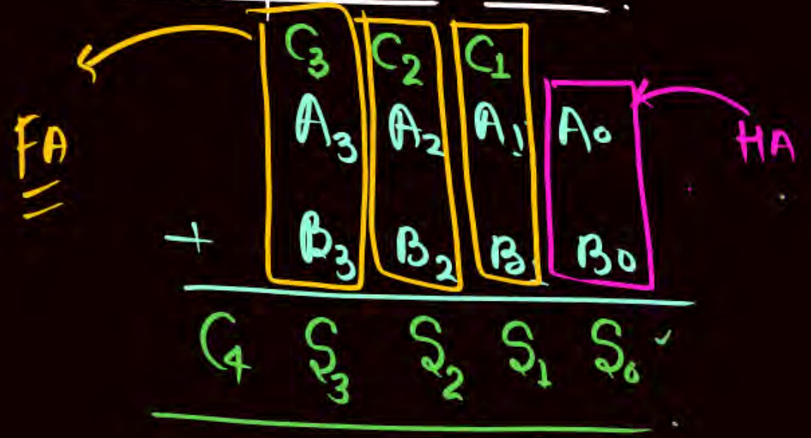
Minimum Delay = $Min(T_1, T_2) + T_{OR}$




Jorden

"PARALLEL ADDER"

4 bit parallel adder



4 bit parallel adder

→ 3 FA + 1 HA

→ 7 HA + 3 OR GATE

→ 4 FA

n bit parallel adder

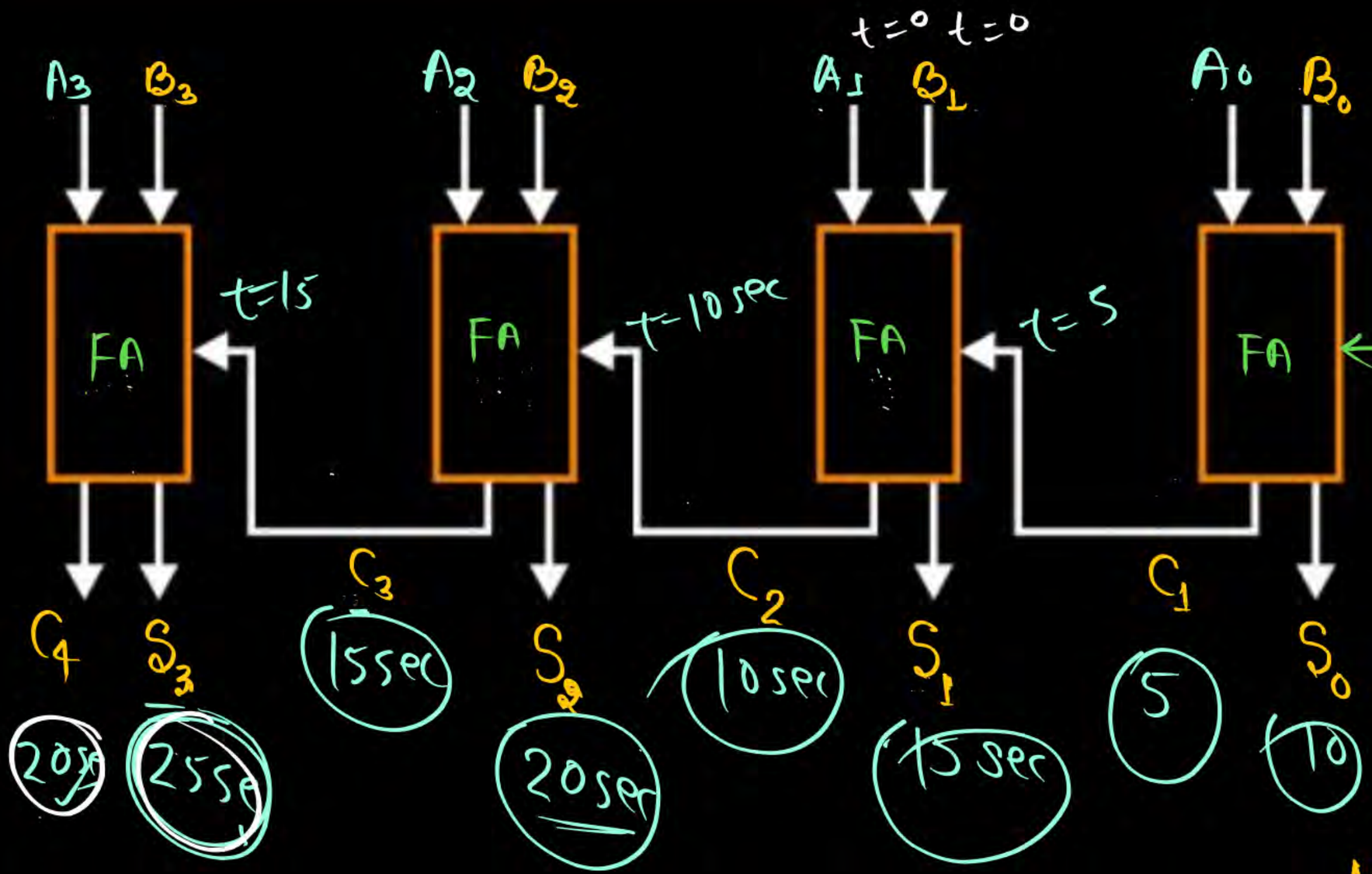
→ (n-1) FA + 1 HA

→ (2n-1) HA + (n-1) OR

→ n FA

PARALLEL ADDER

RIPPLE CARRY ADDER



$T_{sum} = 10$ sec

$T_{carry} = 5$ sec

(A) 20
(B) 25
(C) 35
(D) 90
(E) Sir, Mujhe nahi aata. Mai Tare jameen par hu.

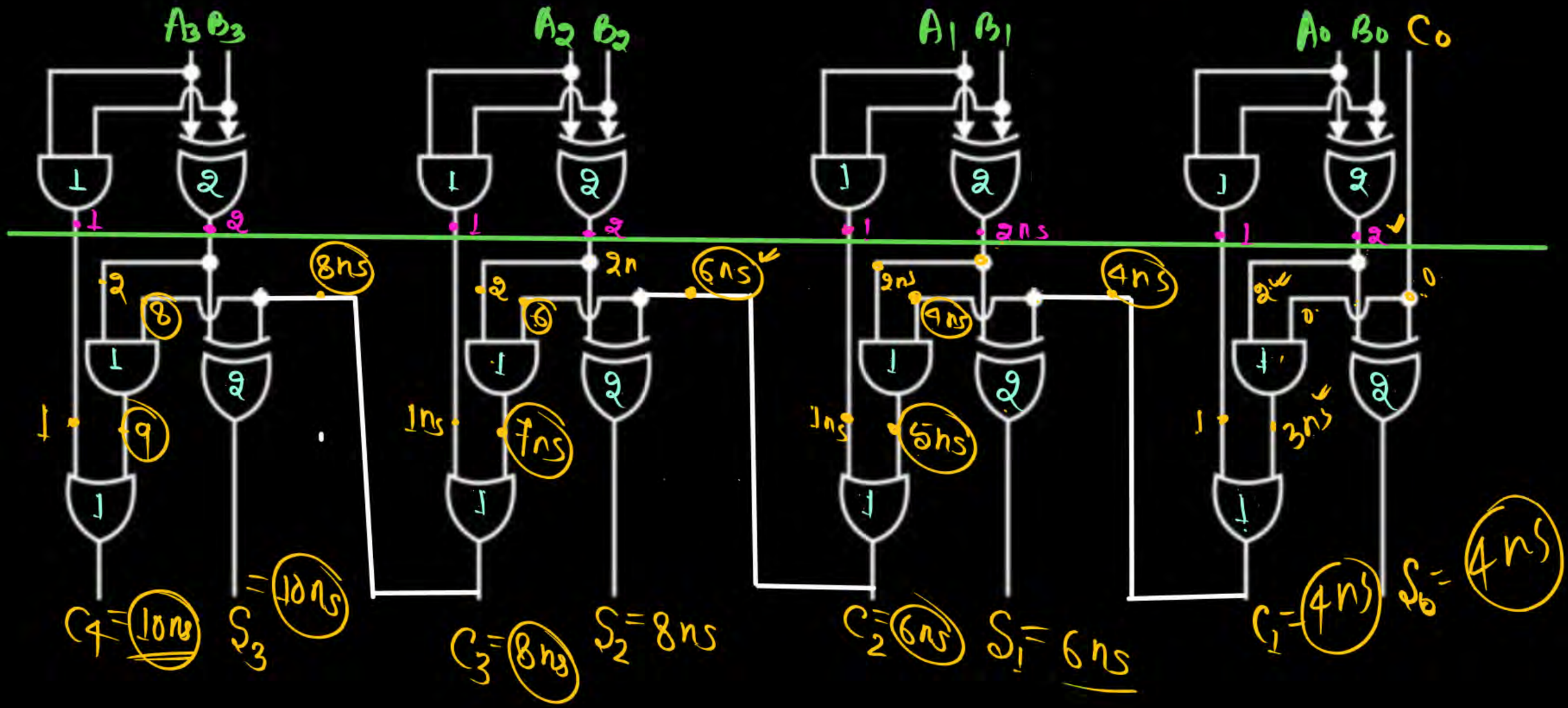
n bit Ripple carry adder

Maximum Delay

$$T = (n-1)T_{carry} + Max\{T_{sum}, T_{carry}\}$$

PARALLEL ADDER

X-OR → 2ns.
AND/OR → 1ns



Maximum Delay

$T_{AND} / T_{OR} = 1\,ns$

$T_{X\text{-}OR} = 2\,ns$

$T_{sum} = 4\,ns$

$T_{carry} = 4\,ns$

$$T = (n-1)\{T_{AND} + T_{OR}\} + Max\{T_{sum}, T_{carry}\}$$

$n \rightarrow$ no. of bits.

$T = (4-1)\{1+1\} + Max\{4, 4\}$

$= 3 \times 2 + 4$ ns

$= 10$ ns

QUESTION

A 16-bit ripple carry adder is realized using 16 identical full adders. The carry propagation delay of each full adder is 12 ns and the sum propagation delay of each full adder is 15 ns. The worst case delay of this 16 bit adder will be _____ ?

A. 195

B. 220

C. 250

D. NONE

carry

sum

$T = (n-1)T_{carry} + \max\{T_{sum}, T_{carry}\}$

$= (16-1)\,12ns + \max\{15ns, 12ns\}$

$= 15 \times 12 + 15$

$= 195\,ns$

QUESTION

4-bit parallel binary adder is built using four full adders. If each full adder takes 44ns to produce the sum bit and 14ns to produce carry bit, then the time required for addition of two 4-bit numbers is.

A. 100

B. 86

C. 126

D. NONE

$T_{sum} = 44ns$

$T_{carry} = 14ns$

$n = 4$

$T = (n-1)T_{carry} + T_{sum}$

$= 3 \times 14 + 44$

$= 86ns$

QUESTION

PYQ

$T_{AND}/T_{OR} = 1.2\ \mu s$

$T_{XOR} = 2.4\ \mu s$

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is,

A. 19.2

B. 12

C. 25

D. NONE

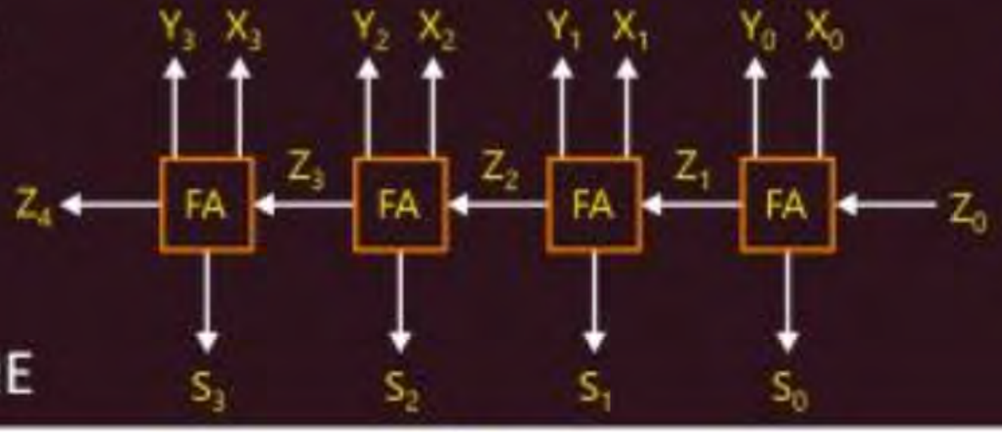


Figure-I

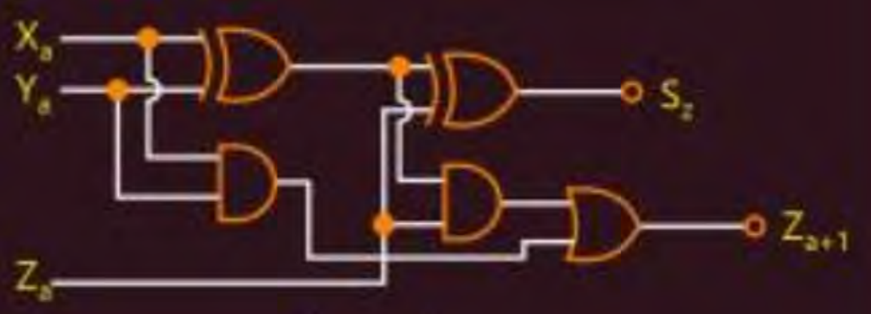
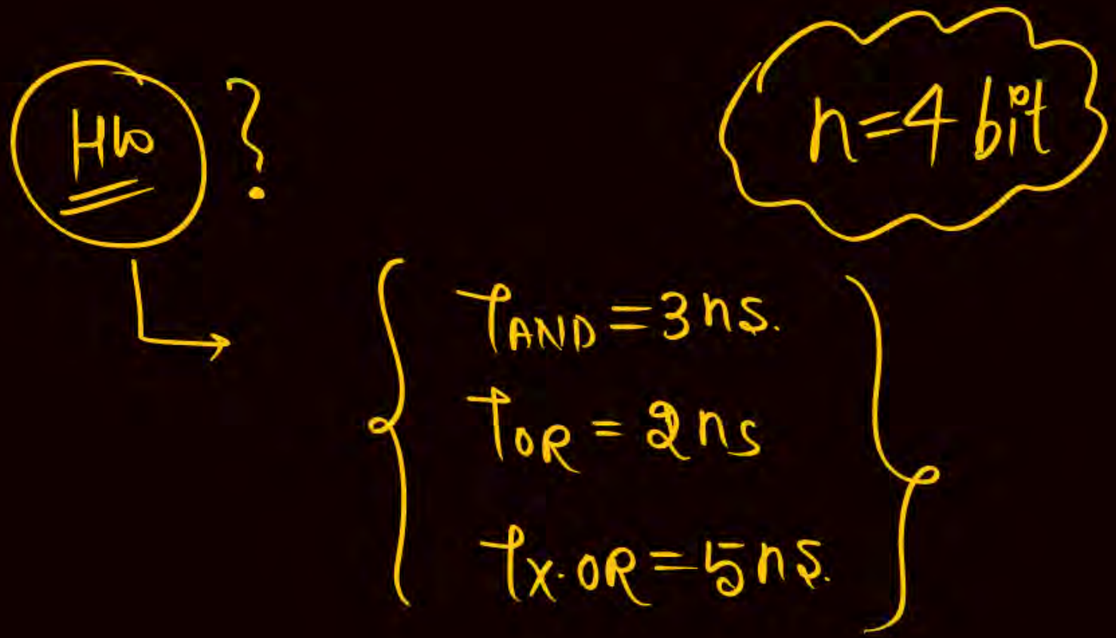


Figure-II


Hw ?
n=4 bit
$t_{AND} = 3\,ns.$
$t_{OR} = 2\,ns$
$t_{X\text{-}OR} = 5\,ns.$

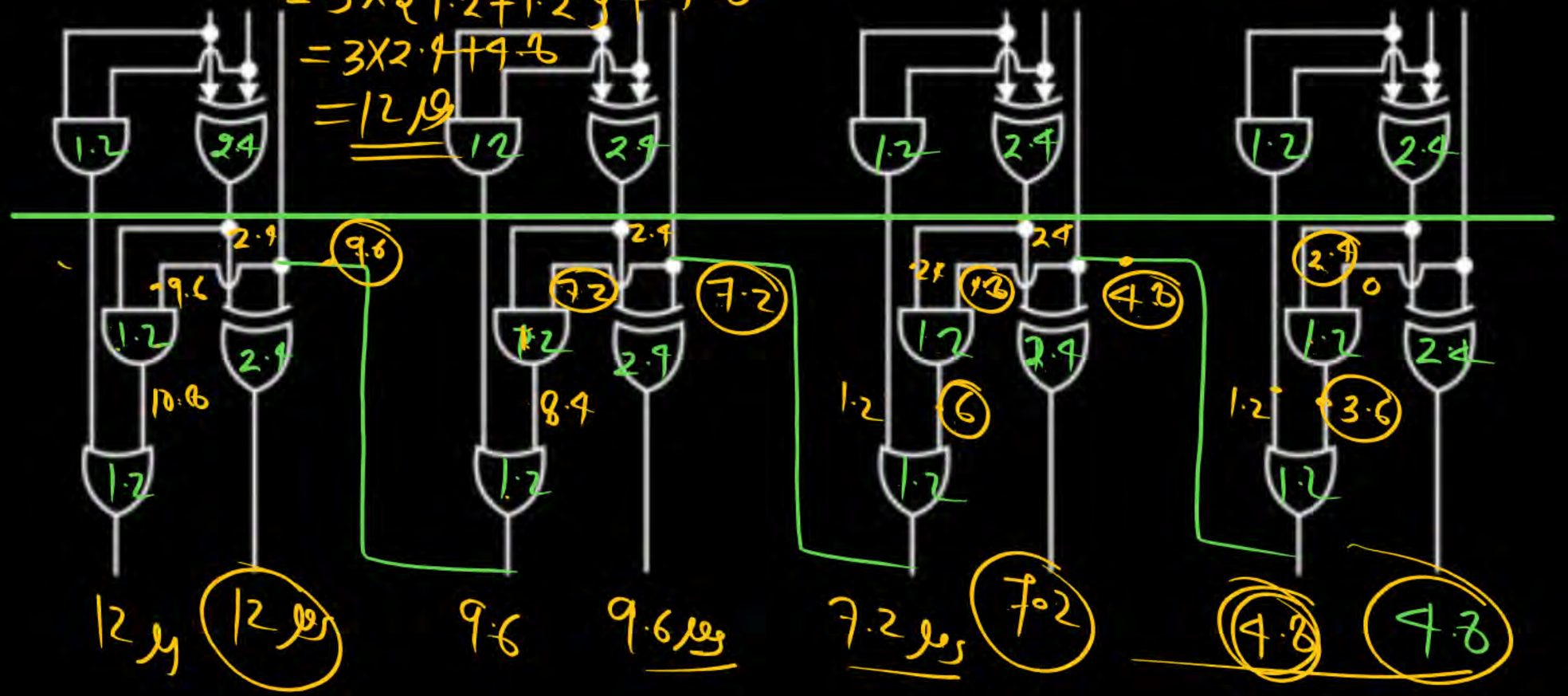
$$T = (n-1)\{T_{AND} + T_{OR}\} + Mux\{T_{sum}, T_{carry}\}$$

4.8

$= 3 \times \{1.2 + 1.2\} + 4.8$

$= 3 \times 2.4 + 4.8$

$= 12.0$



QUESTION

HW.

Figure I show a 4-bits ripple carry adder realized using full adders and Figure II shows the circuit of a full-adder (FA). The propagation delay of the XOR, AND and OR gates in Figure II are 20 ns, 15 ns and 10 ns respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

At t=0, the inputs to the 4-bit adder are changed to

$X_3X_2X_1X_0 = 1100$, $Y_3Y_2Y_1Y_0 = 0100$,

And $Z_0 = 1$

The output of the ripple carry adder will be stable at t (in ns) = _____

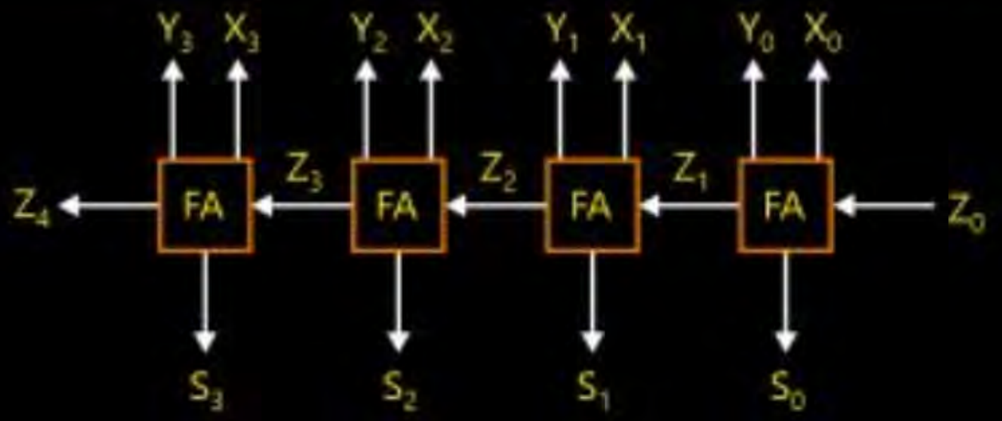


Figure-I

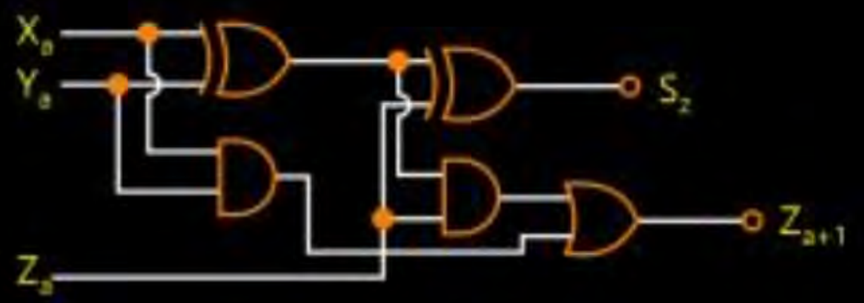
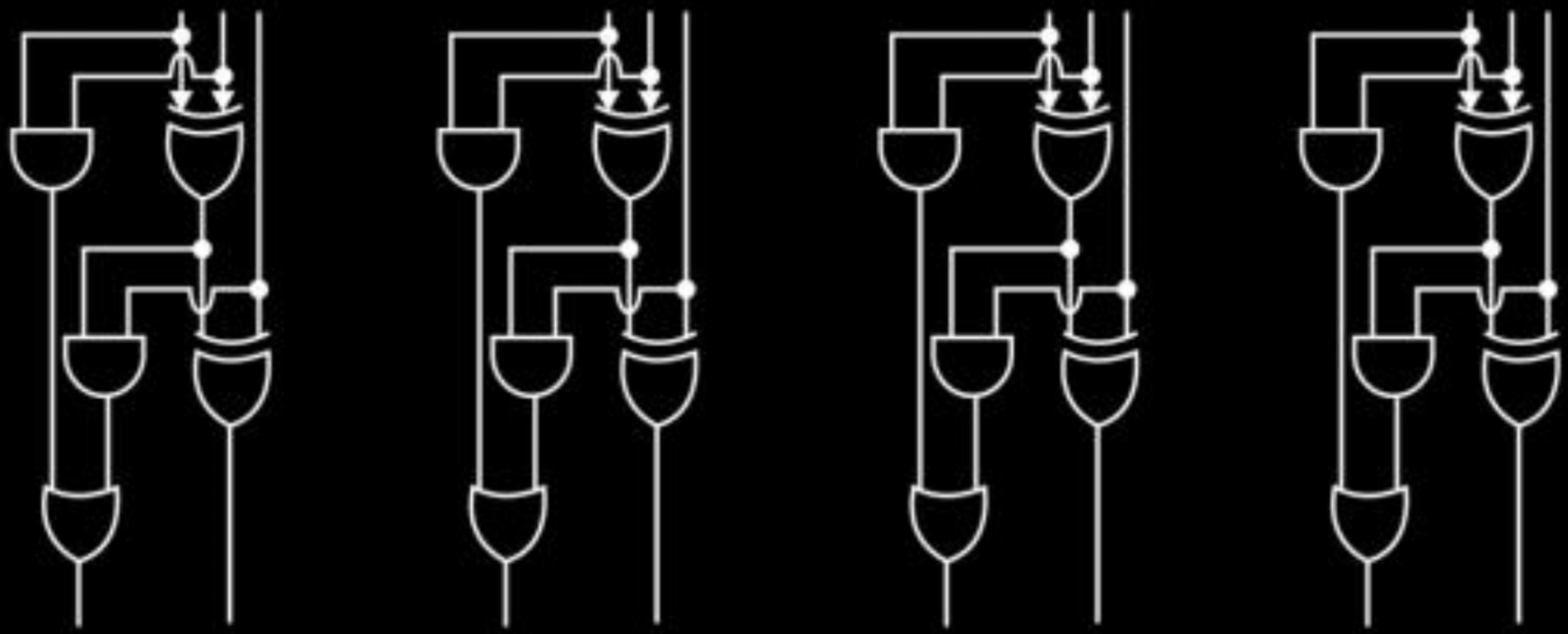


Figure-II




10 AM

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Digital Electronics

L-1 Line

8:00 AM