



**EC/EE/CS/IN**

# Digital Electronics

Logic Gate  
NOT, AND, OR,  
NAND GATE

LECTURE NO. 1



**Chandan Jha Sir (CJ Sir)**

## DIGITAL ELECTRONICS (EE)

No. of Questions

1 to 3 ~ 4

Marks

✓ 2 to 5 ✓

Frequently Asked Topics

k-MAP

✓ Combinational Circuits  
(Multiplexers, Adders), Sequential  
Circuits (Flip Flops and Counters),  
Minimization, Logic Gates,  
Number System, DAC

# Last 5 Year's Trend (2018-2022) for GATE

## DIGITAL CIRCUITS (EC)

No. of Questions

Marks

6 to 7

8 to 11

Frequently Asked Topics

Combinational Circuits (Multiplexers,  
Adders), Sequential Circuits (Flip  
Flops and Latches), Finite State  
Machine, State Transition Diagram,  
Memory, Digital Circuit Design(Using  
MOSFET and CMOS), Minimization,  
Logic Gates, Number System,  
DAC/ADC,

# Last 5 Year's Trend (2018-2022) for GATE

## DIGITAL ELECTRONICS (CS & IT)

No. of Questions

3 to 5 ✓

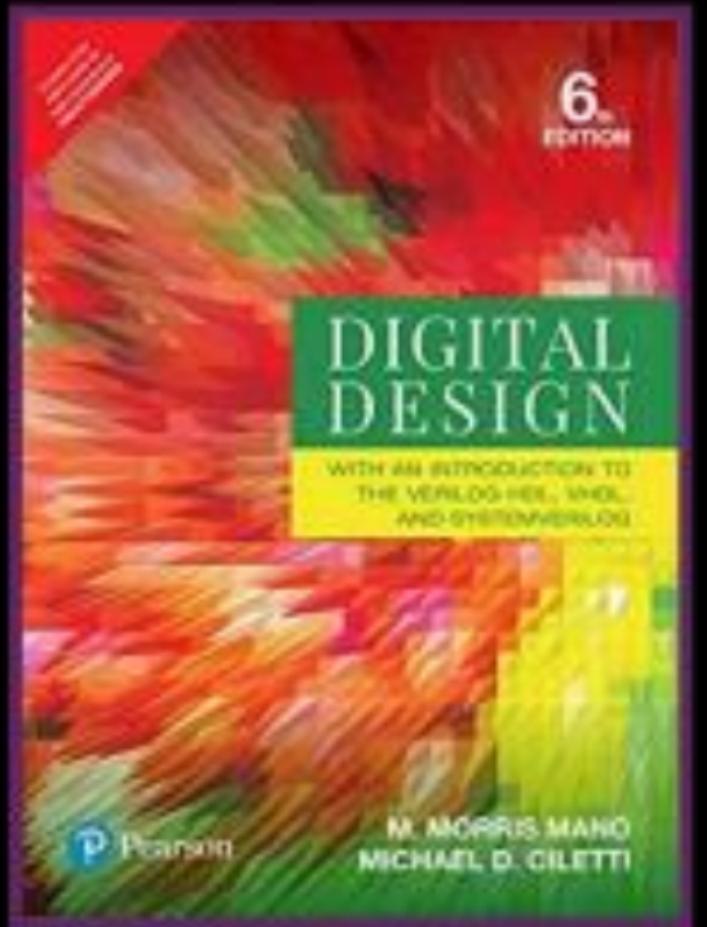
Marks

5 to 8

Frequently Asked Topics

Combinational Circuits (Multiplexers, Adders), Sequential Circuits (Flip Flops and Counters), Boolean Algebra, Minimization, Logic Gates, Number System,

# Reference Books



NOTES  
↓  
Topic



**Book Name:** Digital Design

**Author:** M. Morris Mano & Michael D. Ciletti

**Publisher:** Pearson Publishers

**Book Name:** Modern Digital Electronics

**Author:** R.P. Jain

**Publisher:** Mc GrawHill Education

## ABOUT ME

- Cleared Gate Multiple times with double Digit Rank  
**(AIR 23, AIR 26)**
- Qualified ISRO Exam
- Mentored More than 1 Lakh+ Students (Offline & Online)
- More than 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs



✓ Chandan Jha

# Syllabus

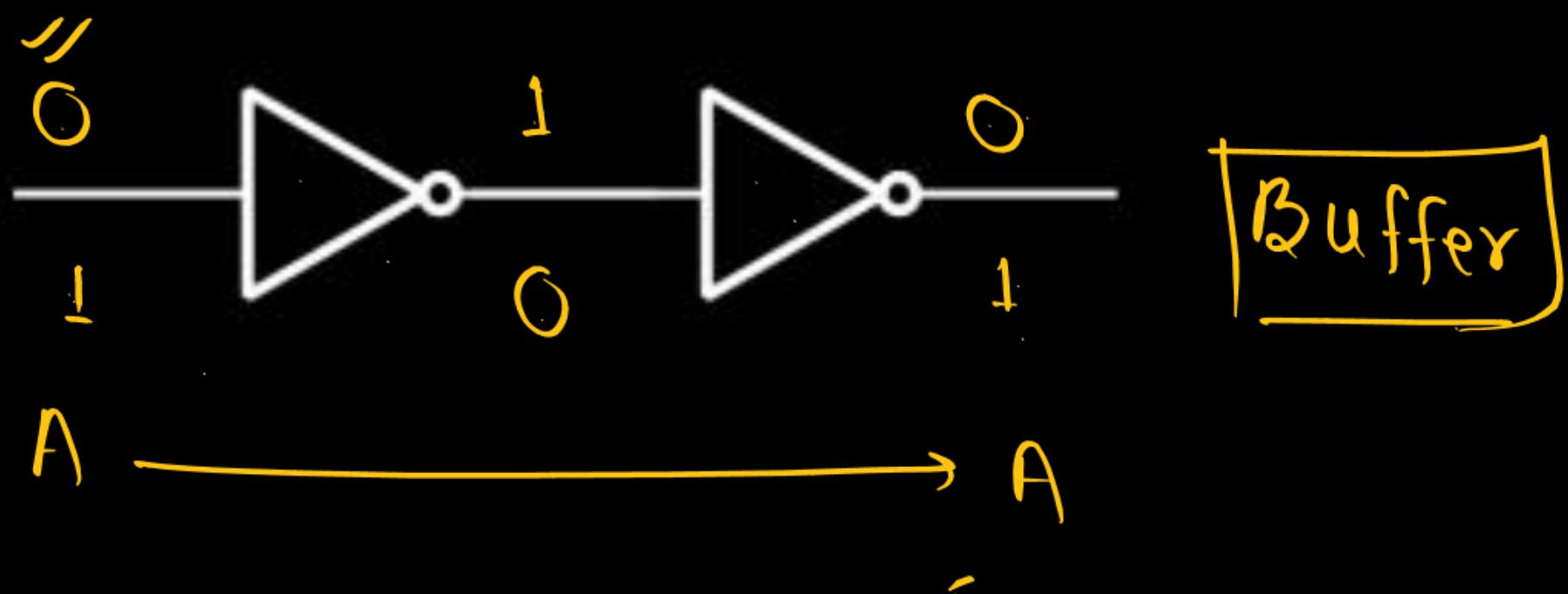
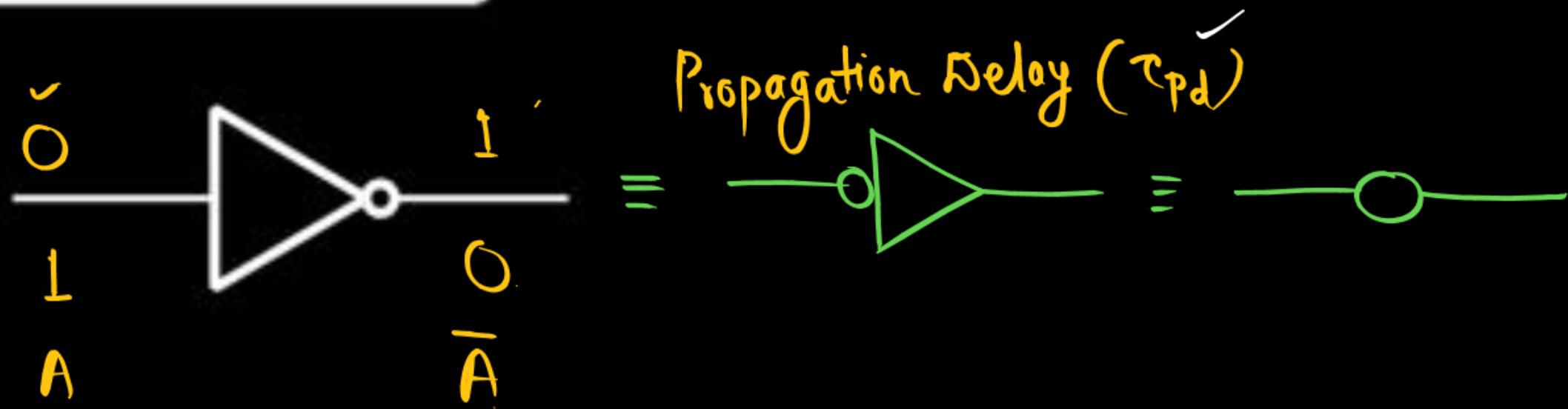
EC/EE/IN/CS.

Chapter	Topic
Logic GATE	NOT, AND, OR, NAND, NOR, X-OR, X-NOR.
Minimization	Boolean algebra, K-MAP
Combinational Circuit	Comparator, MUX, <u>D</u> <u>A</u> <u>D</u>
EC/EE/IN/CS.	parallel adder, Multiplier, Decoder.
Sequential Circuit	Latches, Flip-Flops, Registers, Counters
Number System	Base conversion, Magnitude Rep.
Memory	RAM, ROM
FSM	State Reduction, Sequence Detector
ADC/DAC	EC/EE/IN

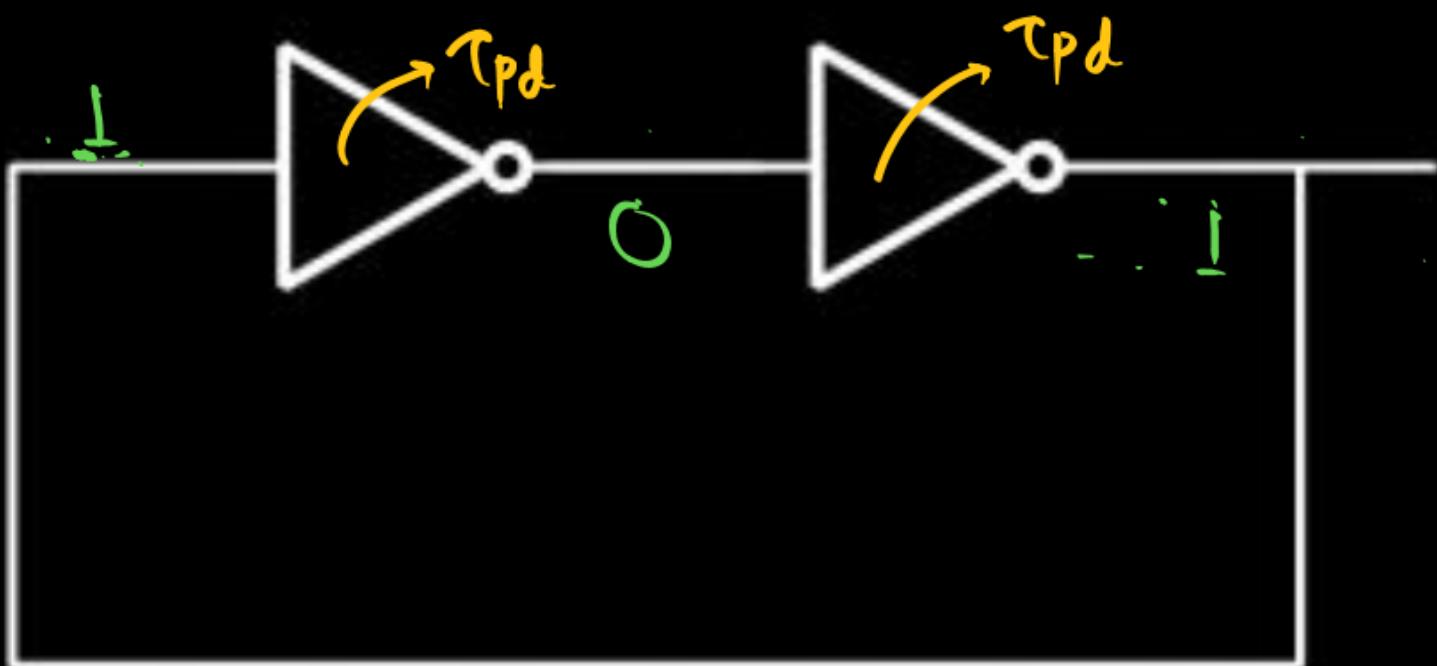
# INVERTER

(NOT GATE/ NEGATION)

P  
W



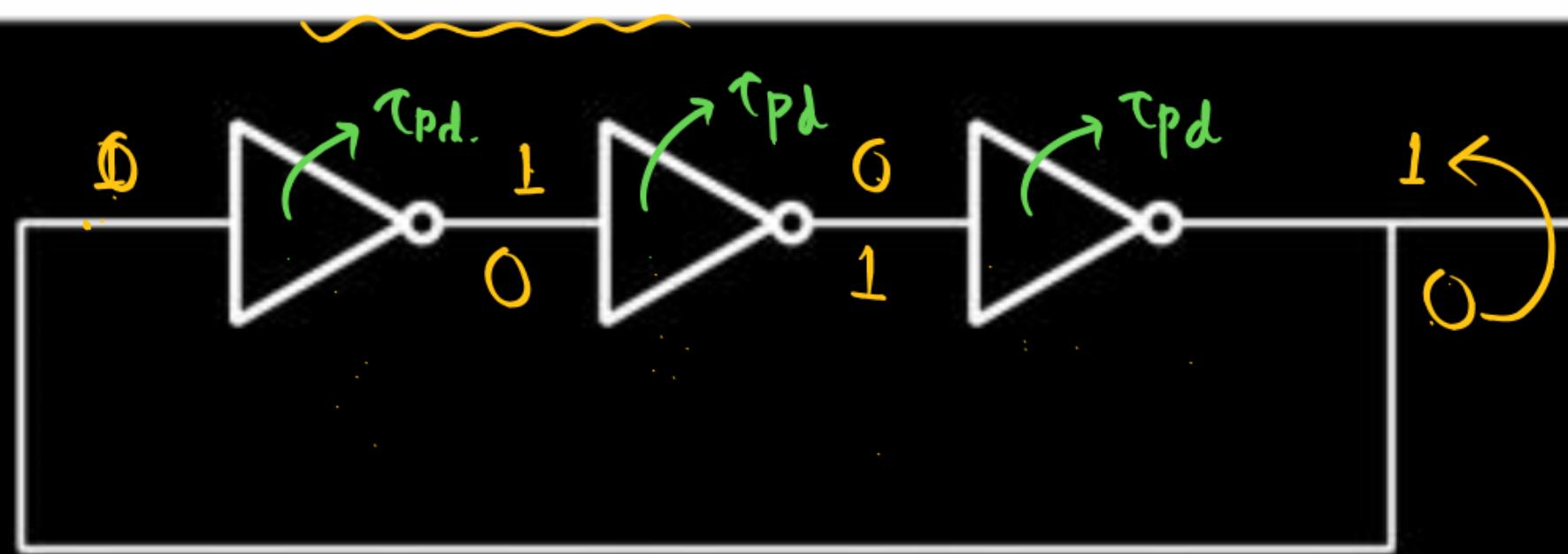
# When Even Number Of NOT GATE in LOOP



$0 \rightarrow 0 \rightarrow 0 \rightarrow 0 \rightarrow 0 \rightarrow \dots$   
 $1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow 1 \rightarrow \dots$

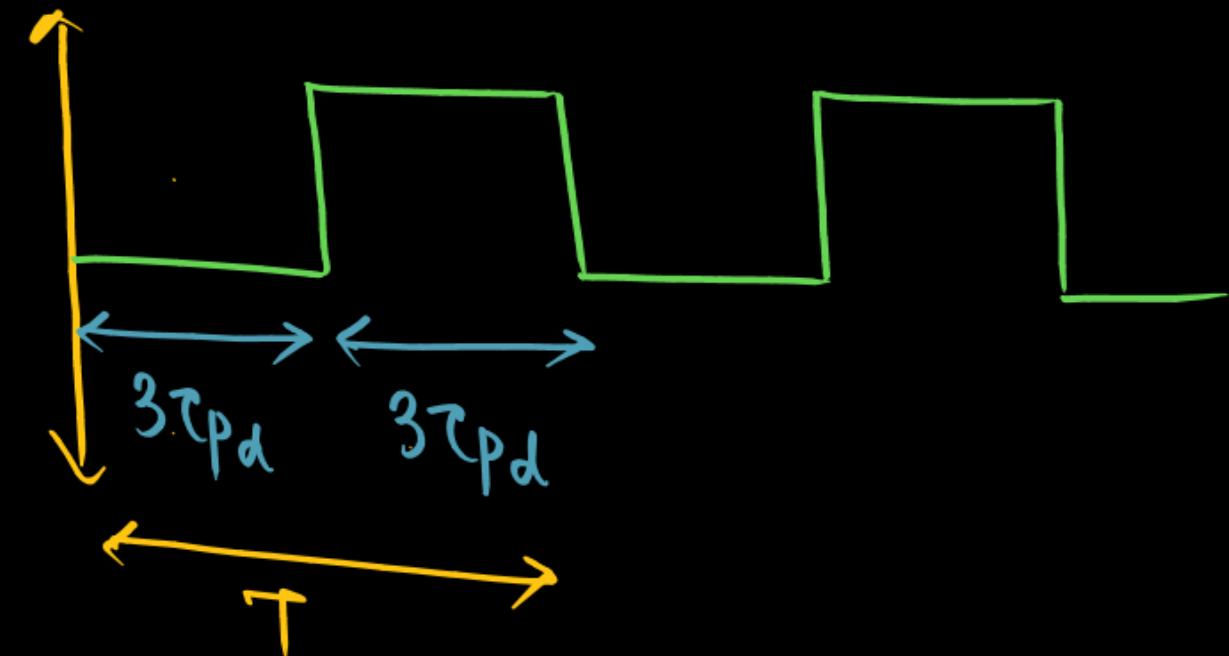
→ Basic memory element  
→ Bistable Multivibrator

# When ODD Number Of NOT GATE in LOOP



$3\tau_{pd}$     $3\tau_{pd}$     $3\tau_{pd}$     $3\tau_{pd}$

$0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow \dots$



- 1> Asstable Multivibrator ✓
- 2> Square wave generator ✓
- 3> Clock generator ✓
- 4> Free Running circuit ✓
- 5> Ring oscillator ✓

$$T = 6\tau_{pd}$$

$$T = 2 \times 3 \times \tau_{pd}$$

$$T = 2N \times \tau_{pd}$$

$$T = 2N \times \tau_{pd}$$

$N \rightarrow$  No. of NOT GATE in loop

(Odd)

$$f = \frac{1}{T}$$

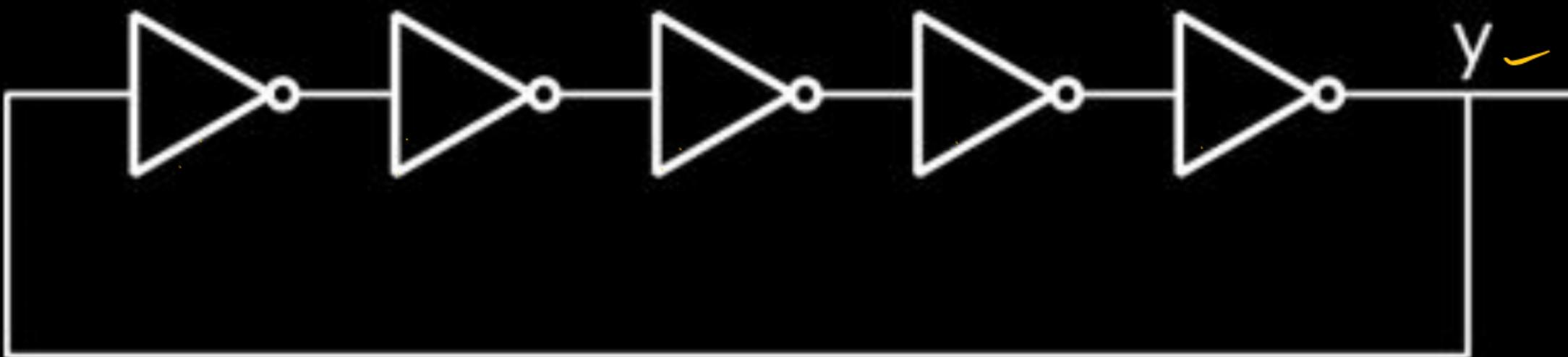
$$f = \frac{1}{2N \times \tau_{pd}}$$



$$f = \frac{1}{2 \times 5 \times \tau_{pd}}$$

Q.

For the circuit given below, all NOT Gates are identical to each other and having propagation delay 10 ps. Find the frequency of generated wave form?

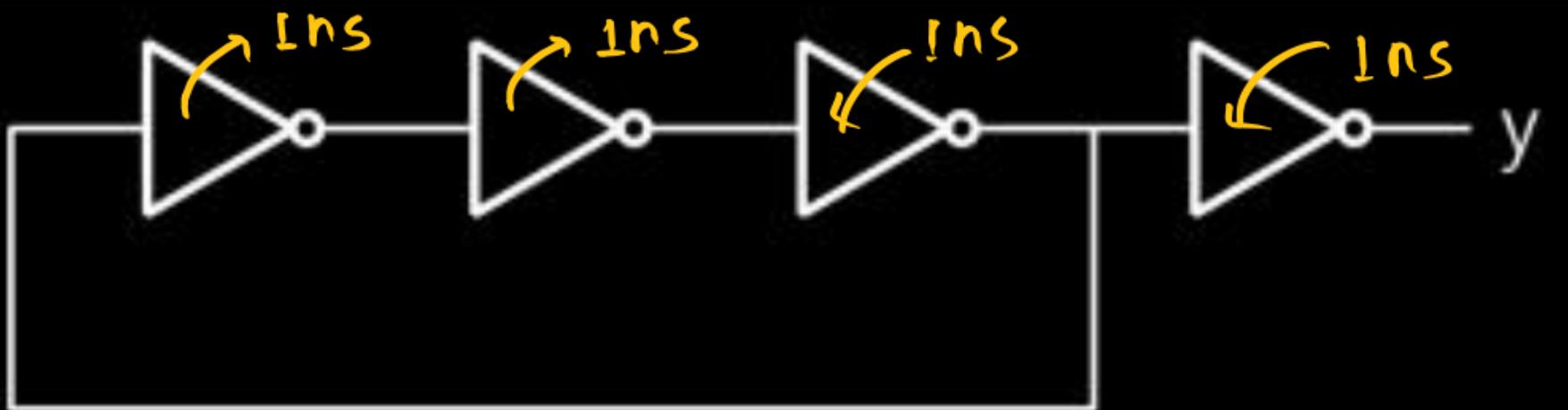
P  
W

$$\begin{aligned}
 f &= \frac{1}{2N \times T_{pd}} \Rightarrow f = \frac{1}{2 \times 5 \times 10 \times 10^{-12}} \text{ Hz} \\
 f &= \frac{10^{12}}{10 \times 10} \text{ Hz} = \frac{10^{10} \times 10^9}{10 \times 10} \text{ Hz} = 10 \times 10^9 \text{ Hz} \\
 &= \underline{\underline{10 \text{ GHz}}}
 \end{aligned}$$

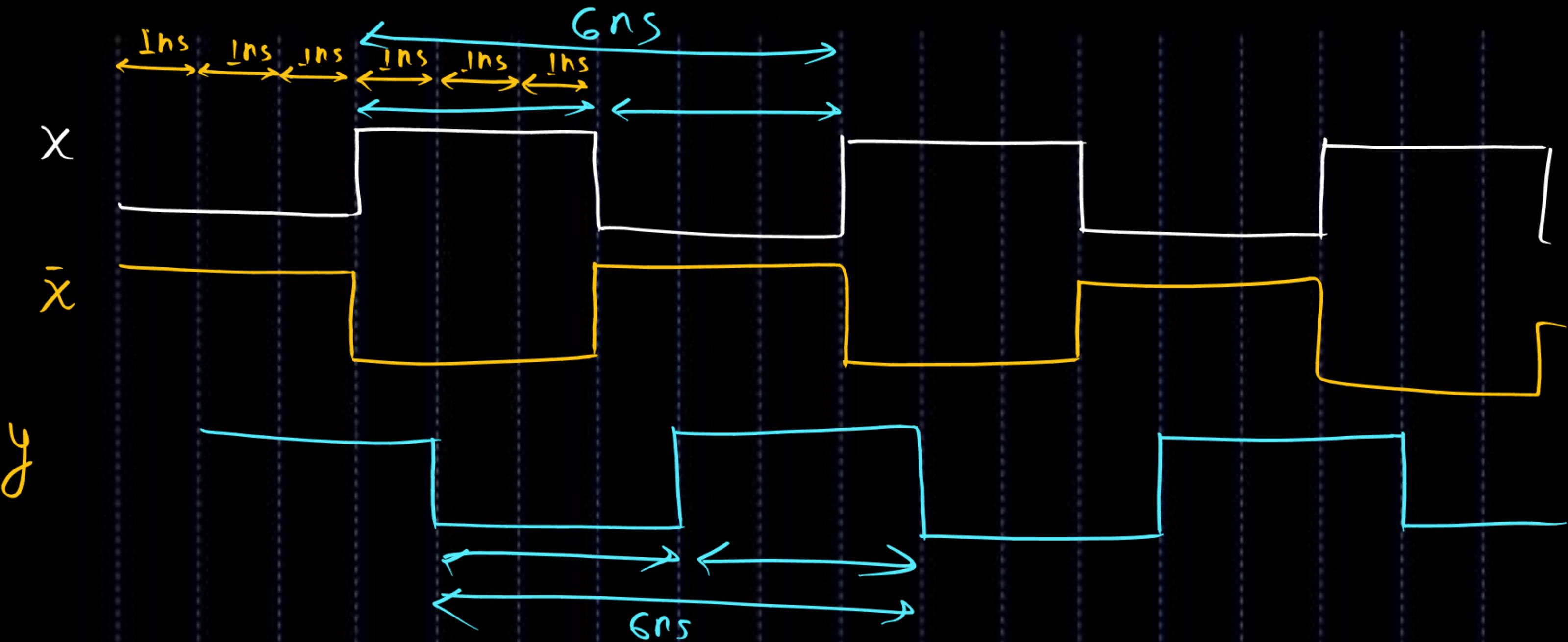
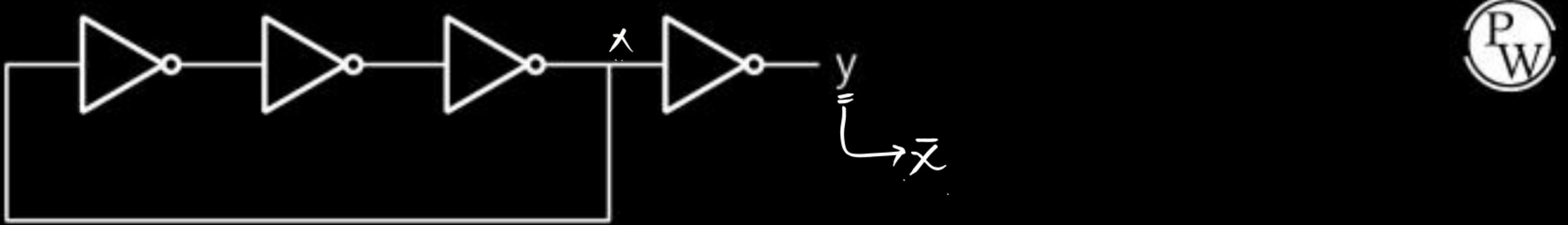
Q.

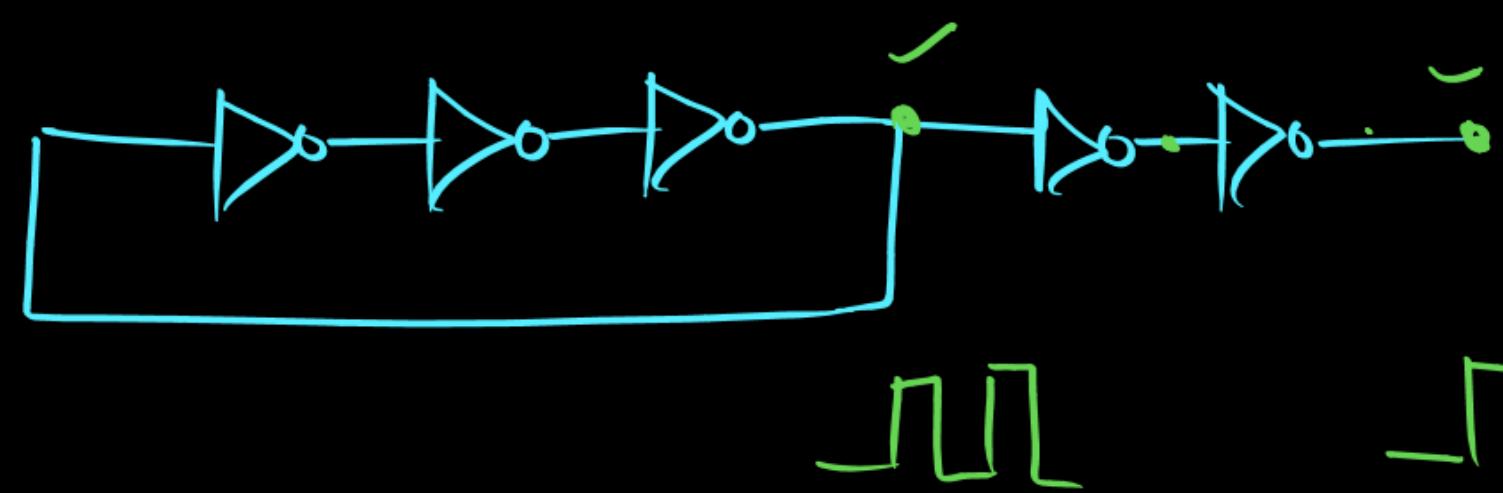
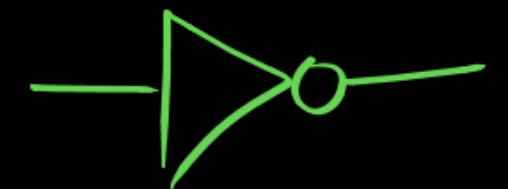
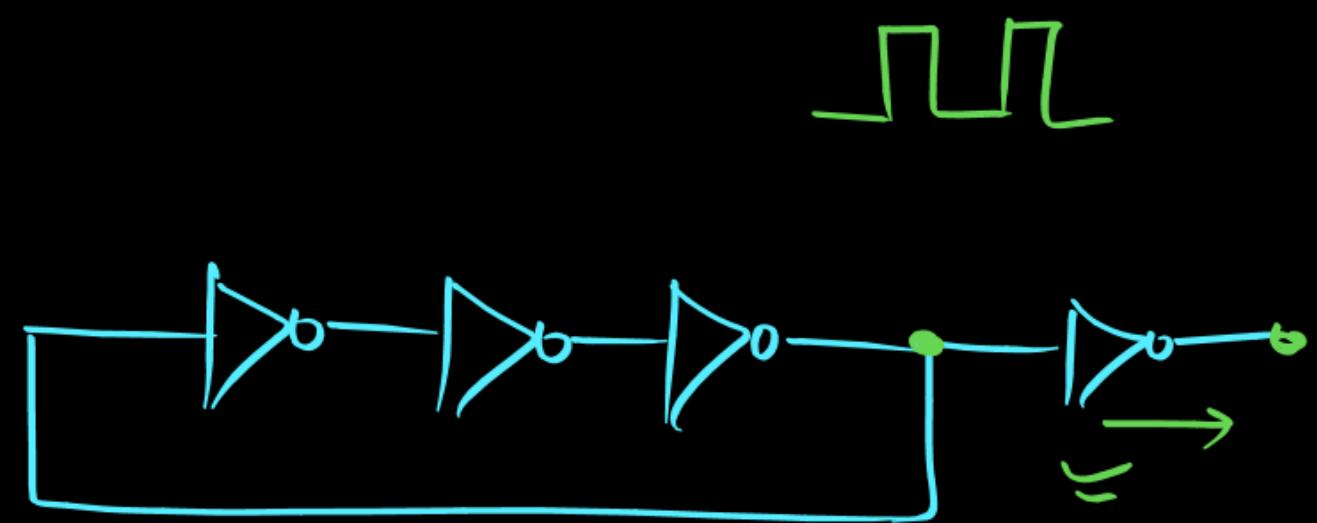
Sketch the waveform of y?

P  
W



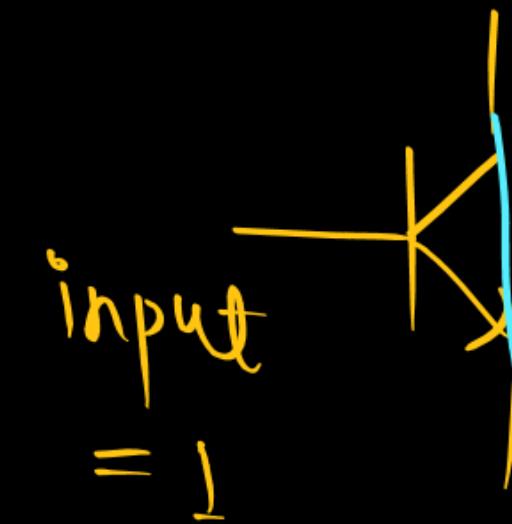
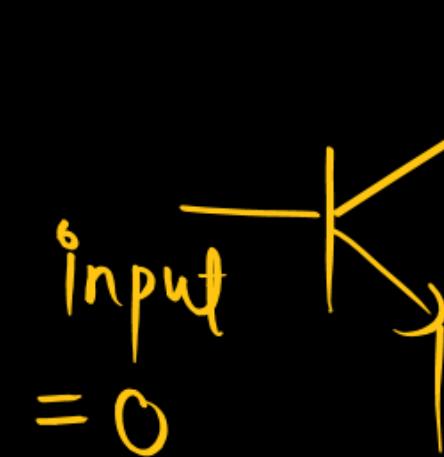
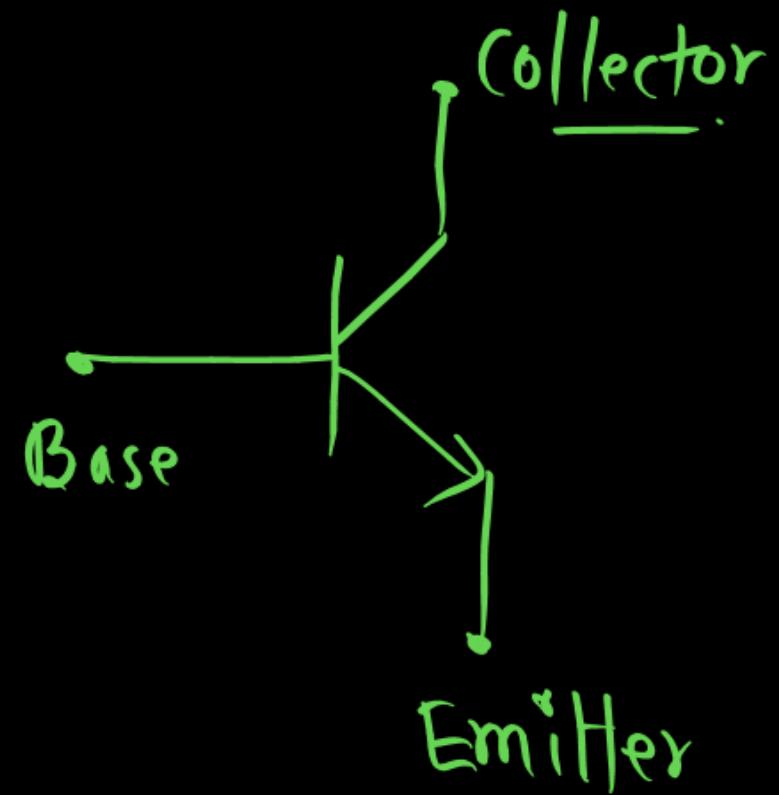
Astable





$f = \frac{1}{6Cpd}$

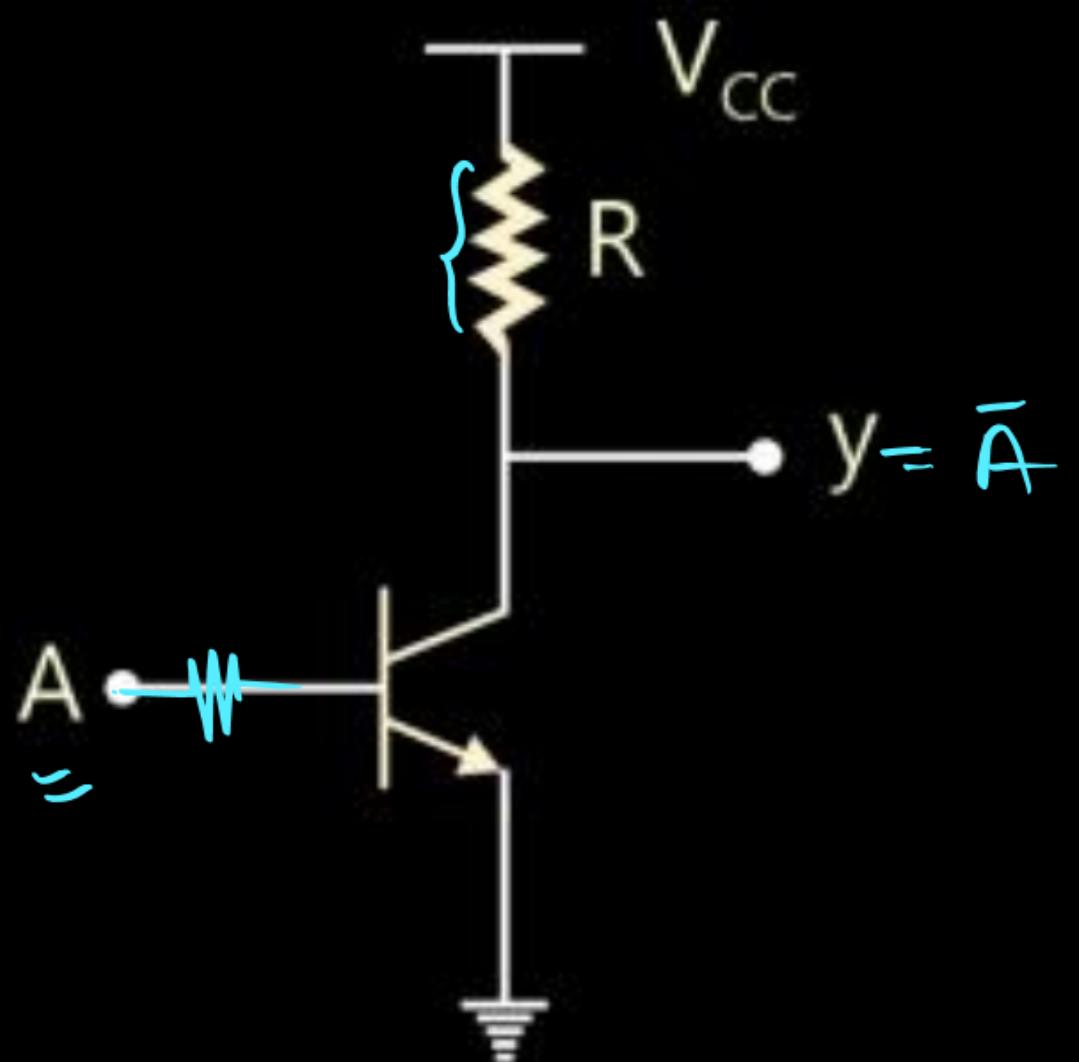
## NPN → Transistor



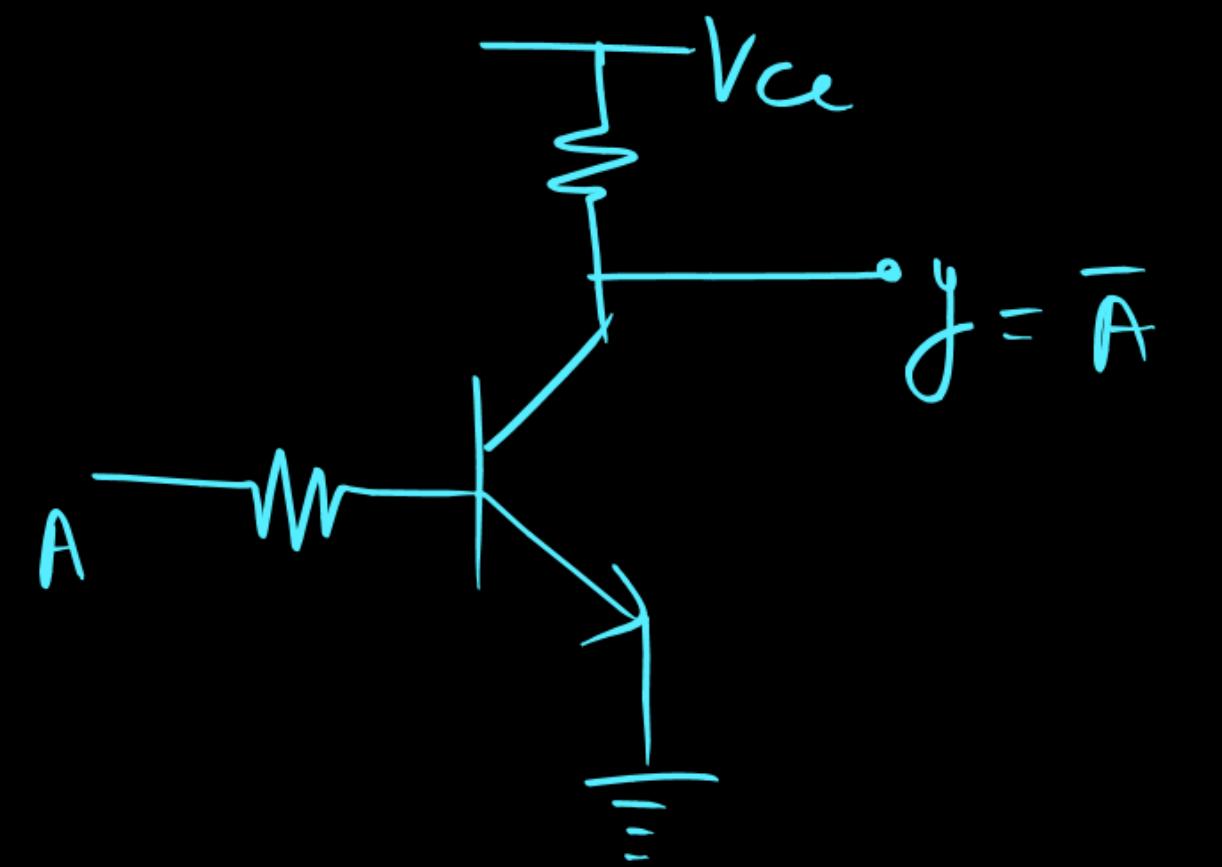
Cutoff → OFF  
↓  
open circuit

Saturation → ON  
↓  
Short circuit

# Circuit Diagram



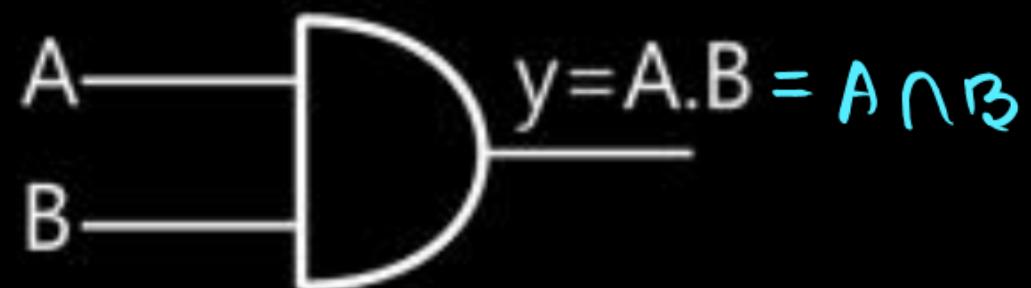
A(Input)	Transistor	y(Output)
0	Cutoff	1
1	Saturation	0



## (2) AND GATE

P  
W

(a) Symbol



(b) Truth Table

Truth Table		
A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

$$A \cdot \bar{A} = 0$$

$$\begin{matrix} \bar{A} \\ A \end{matrix} \quad \{1, 2, 3\}$$

72 ok 45k

$$1 \cdot A = A$$

$$\begin{matrix} B \\ \{2, 3, 9\} \end{matrix} \quad Y = \{2, 3\}$$

ANDing

$$0 \cdot 0 = 0$$

$$0 \cdot 1 = 0$$

$$1 \cdot 0 = 0$$

$$1 \cdot 1 = 1$$

$$1 \cdot A = A$$

$$A \cdot A = A$$

$$A \cdot 0 = 0$$

$$A \cdot \bar{A} = 0$$



$$0 + 0 = 0$$

$$0 + 1 = 1$$

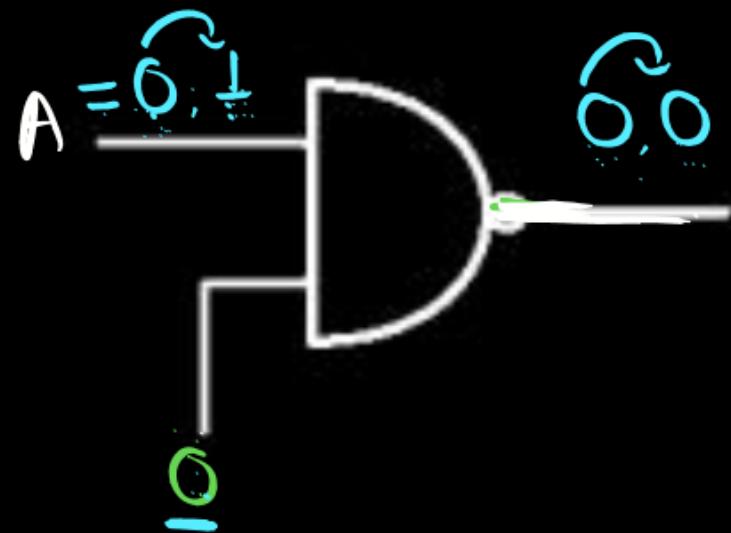
$$1 + 0 = 1$$

$$1 + 1 = 1$$

$$1 + A = 1$$

$$A + \bar{A} = 1$$

$$1 + AB = 1$$

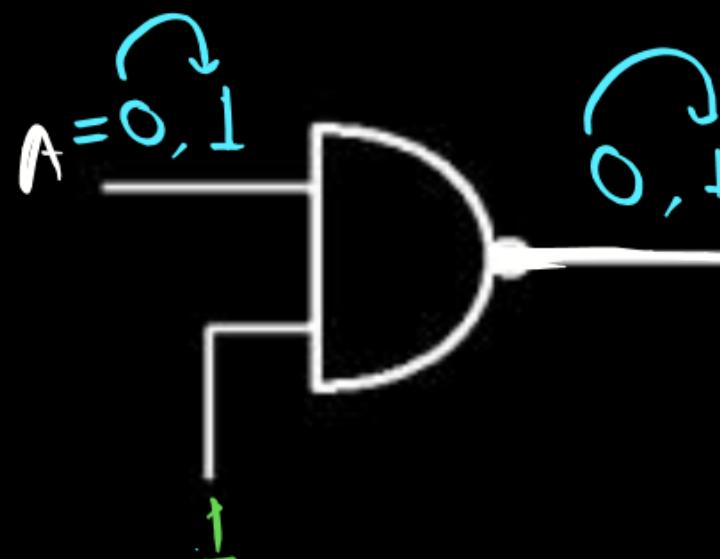
**(2) AND GATE****(c) Enable/Disable**

Control '0' Disabled

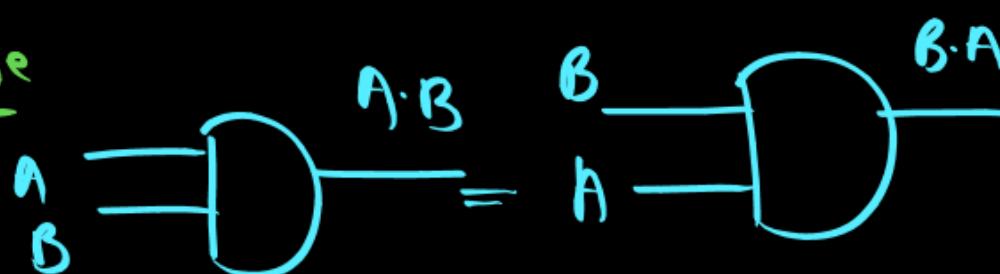
Floating terminal, Control input, Strobe

**(d) Commutative law**

$$A \cdot B = B \cdot A$$



Control '1' Enabled ✓



**Associative law**

$$A \cdot B \cdot C = (A \cdot B) \cdot C$$

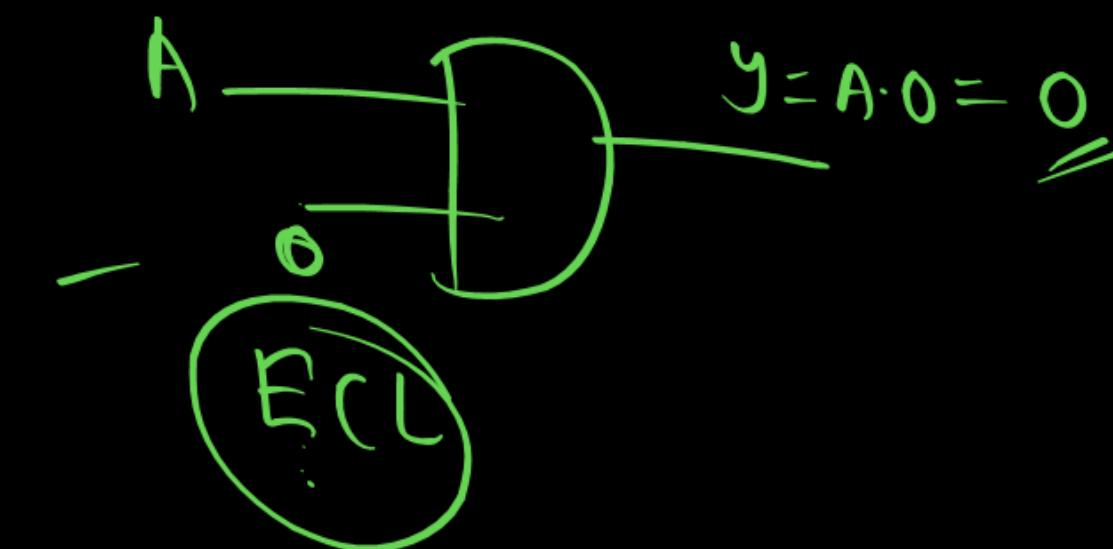
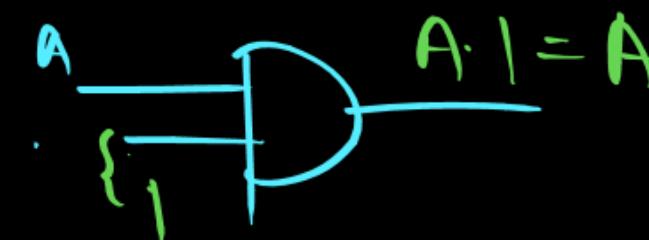
$\Rightarrow$  Associative Law: ✓

$$(A \cdot B) \cdot C = A \cdot (B \cdot C)$$

**Key Points:**

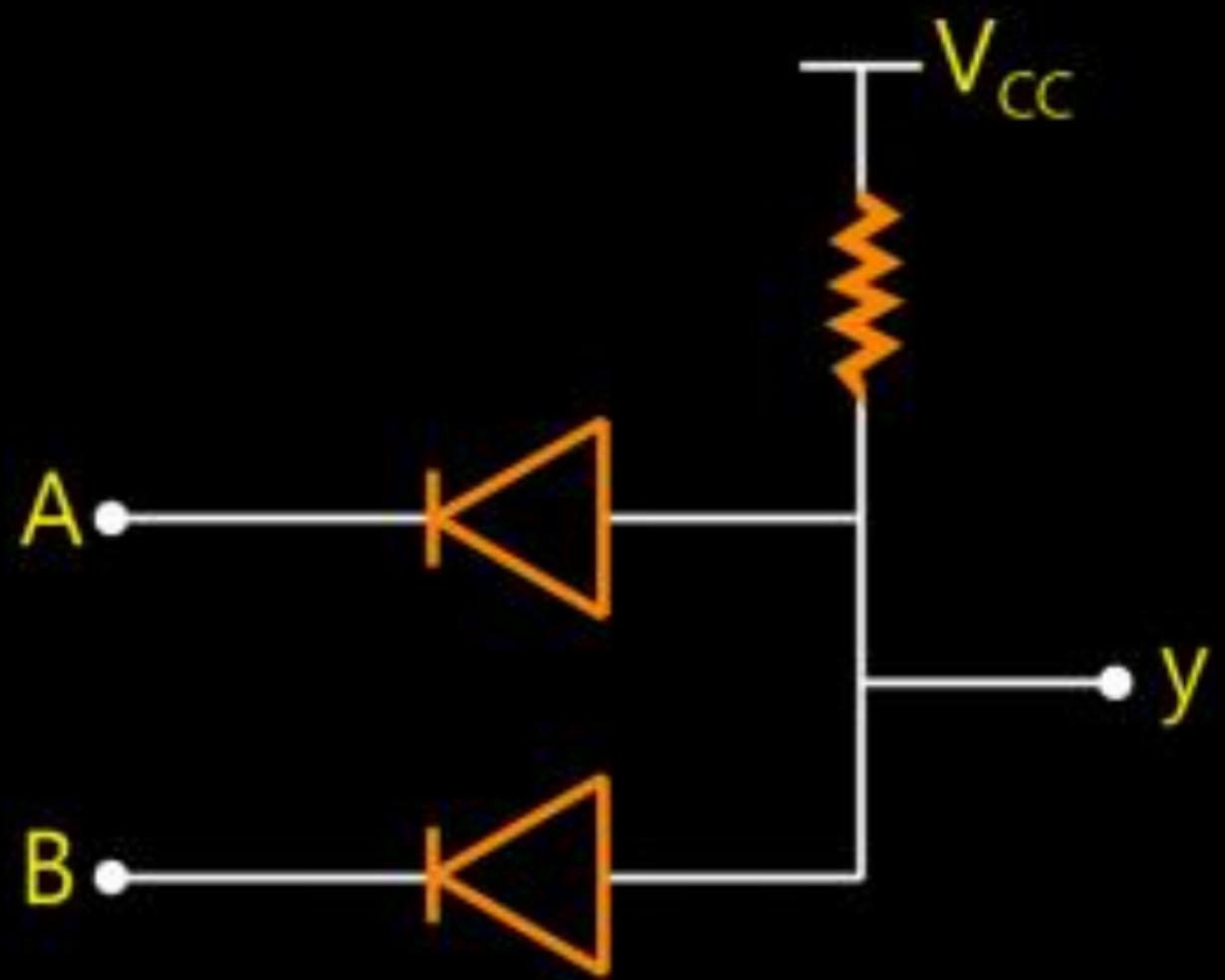
1. Whenever logic are designed by TTL (Transistor transistor logic) then floating terminal always works as a high. ✓
2. Whenever logic are designed by ECL (Emitter coupled logic) then floating terminal always works as a low.

TTL



# Circuit Diagram

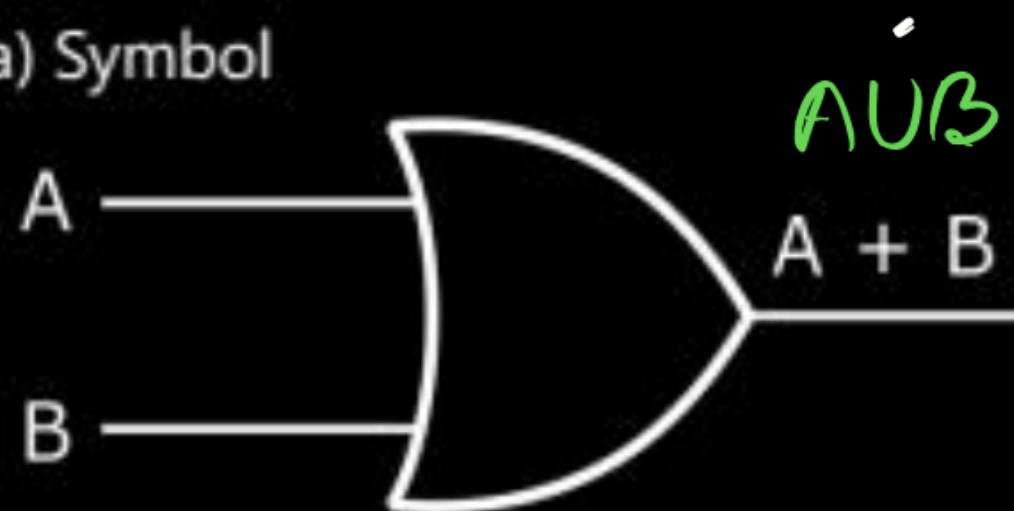
P  
W



A	B	$D_A$	$D_B$	y
0	0			
0	1			
1	0			
1	1			

# OR GATE

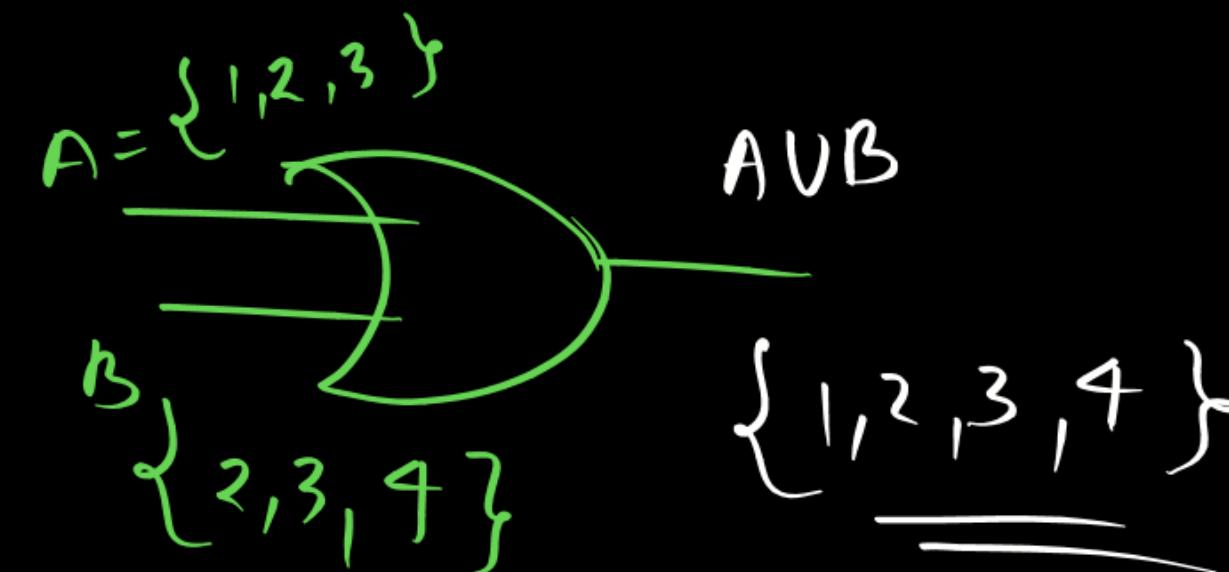
(a) Symbol



(b) Truth Table

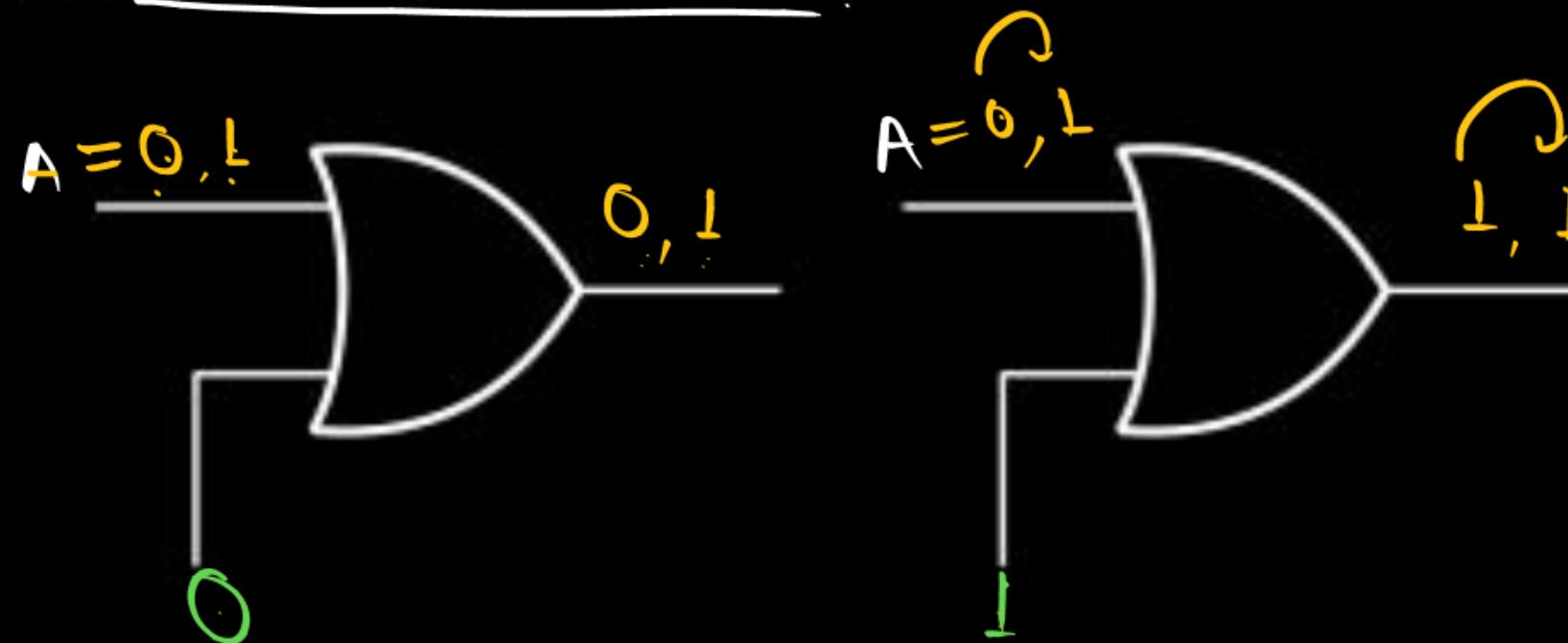
**Truth Table**

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



# OR GATE

(c) Enable/disable



Control '0' Enabled

(d) Commutative Law

$$A + B = B + A$$

Associative Law

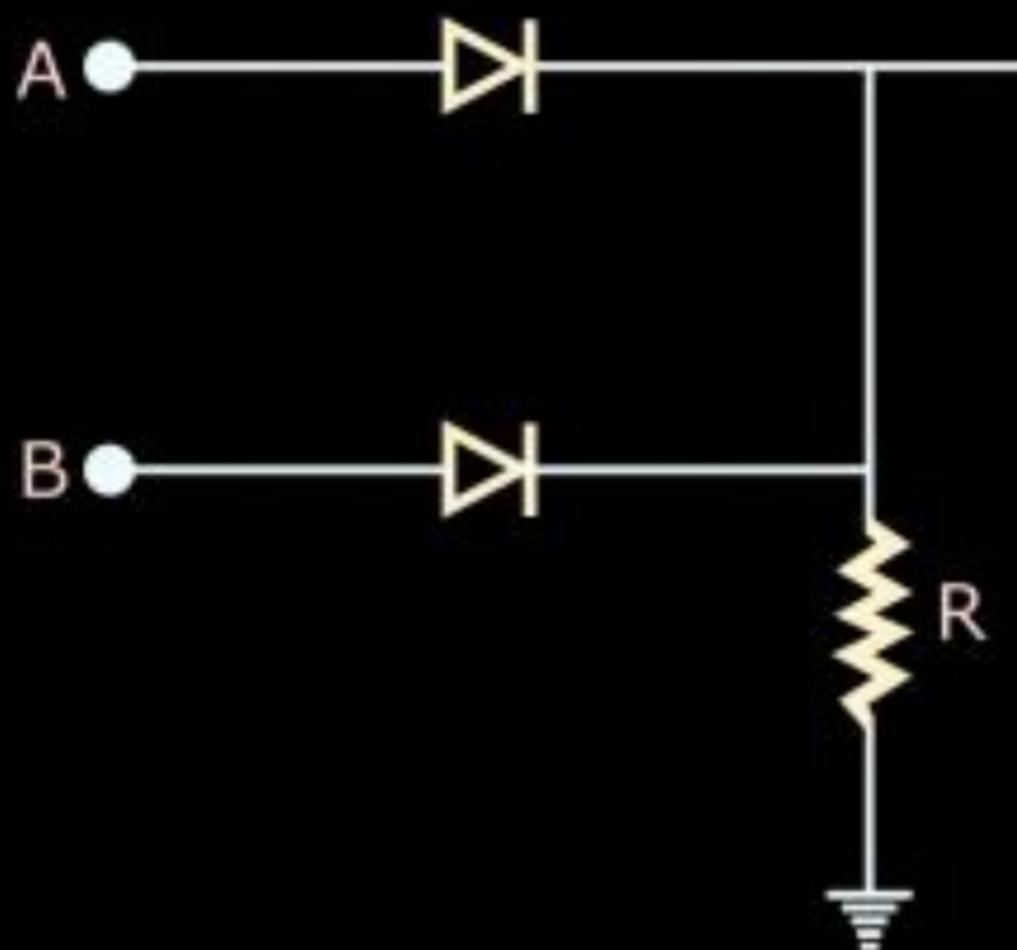
$$(A+B)+C = A+(B+C)$$

$$A + B + C = (A + B) + C$$



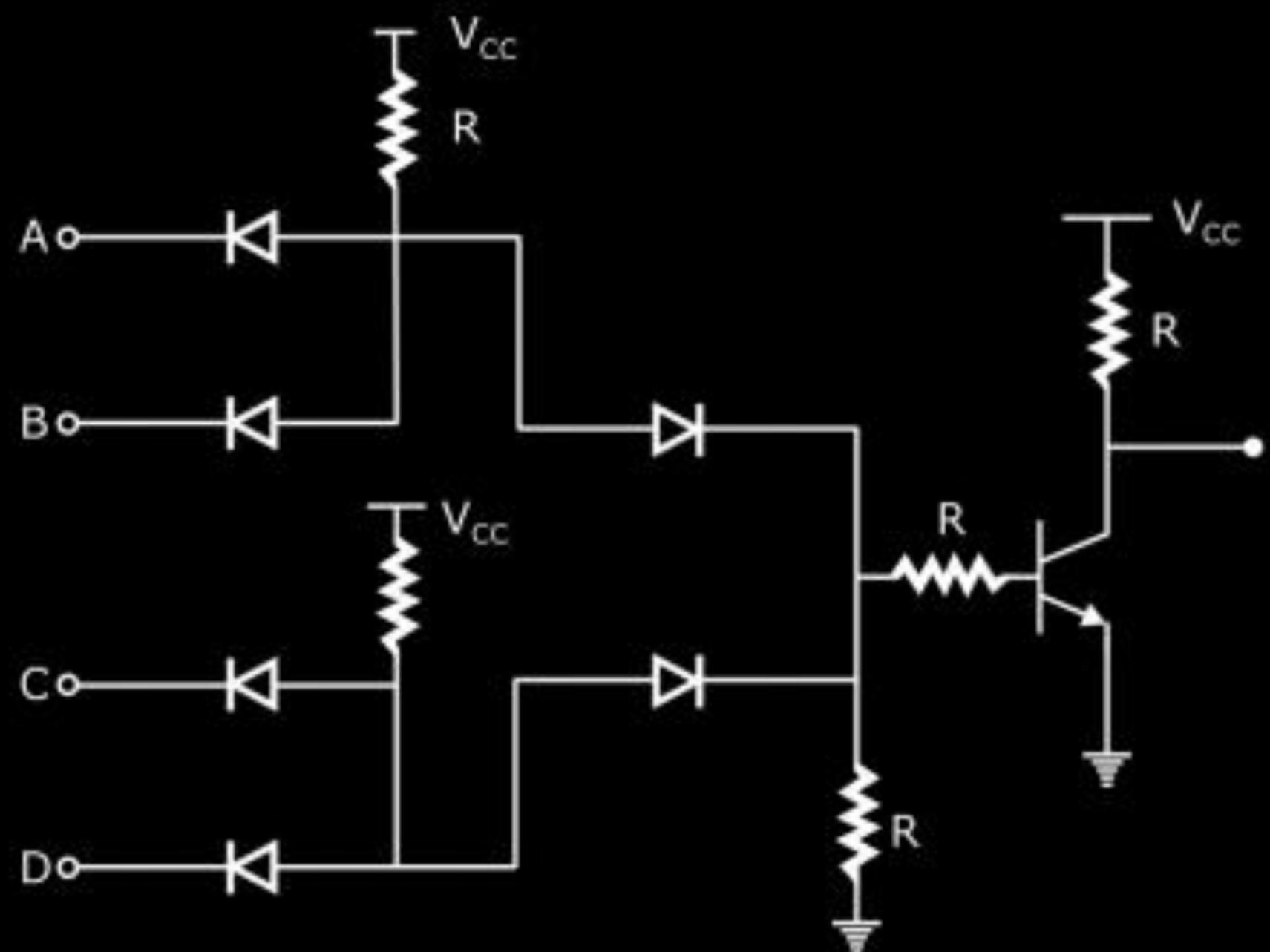
# OR GATE

(e) Circuit diagram



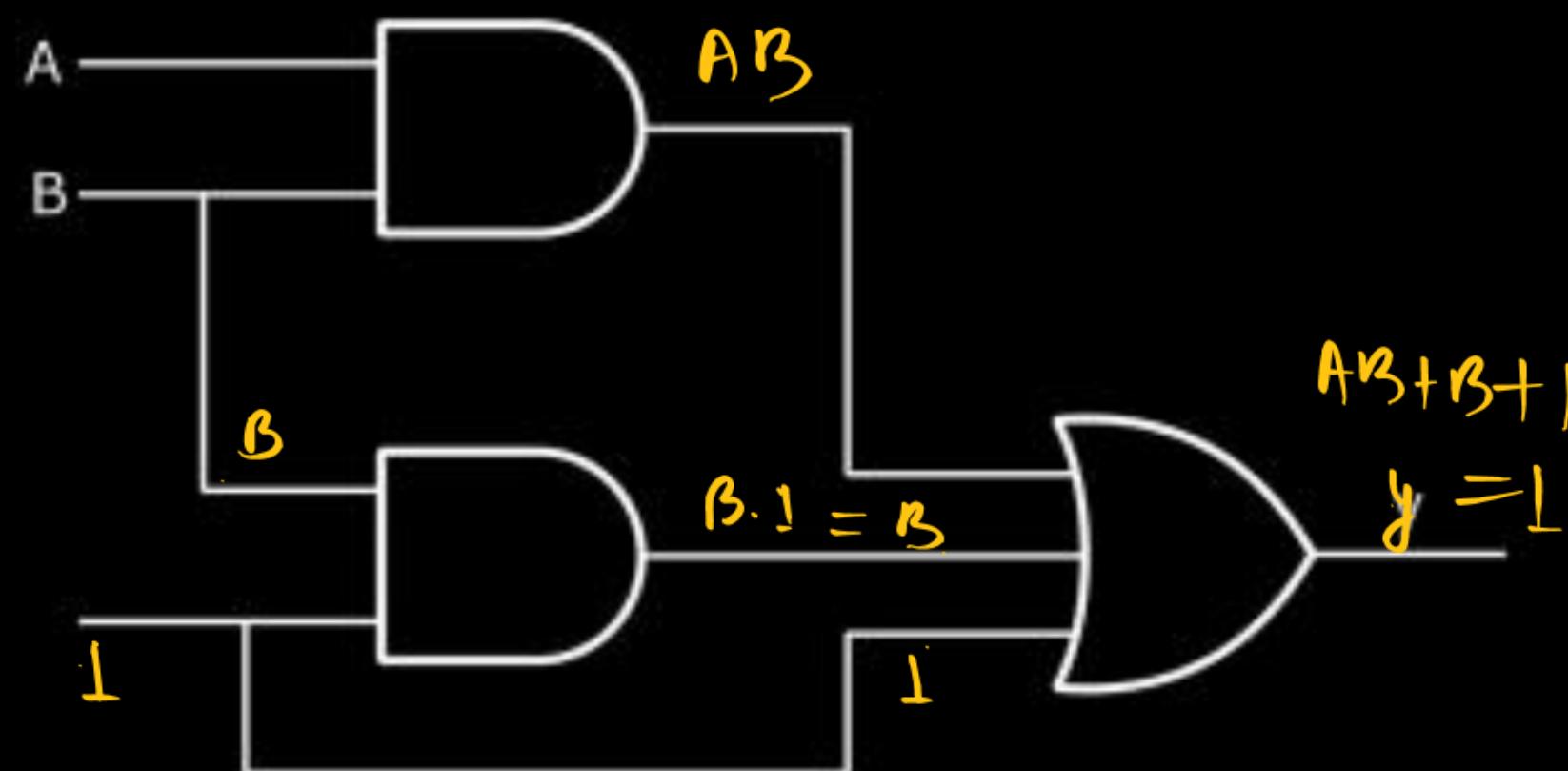
A	B	$D_A$	$D_B$	y
0	0			
0	1			
1	0			
1	1			

Q.1 The output  $y$  will be —



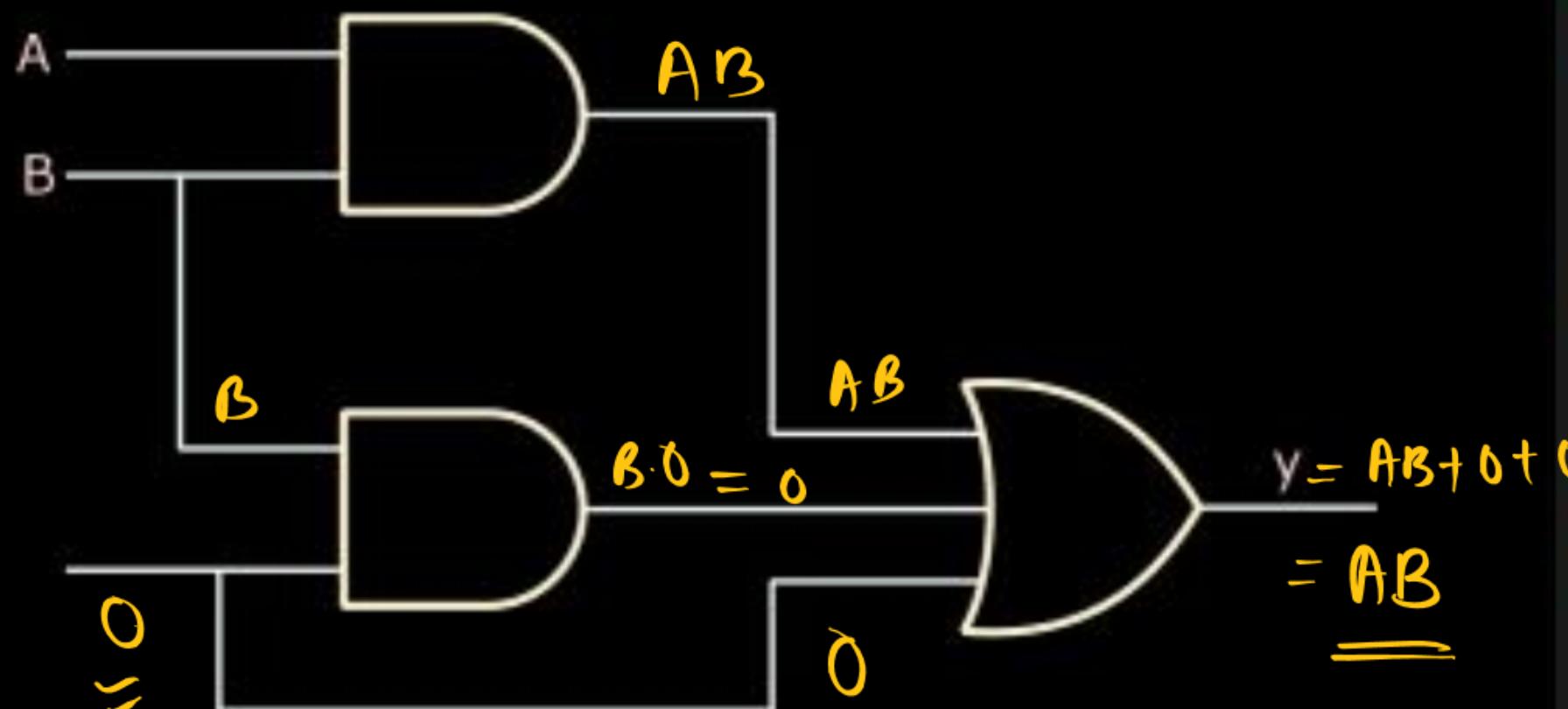
- A 0
- B 1
- C  $(AB + CD)$
- D  $AB + CD$

Q.2 If the logic given below are design with TTL then the output Y will be-



- A 0
- B A
- C 1
- D None of the above

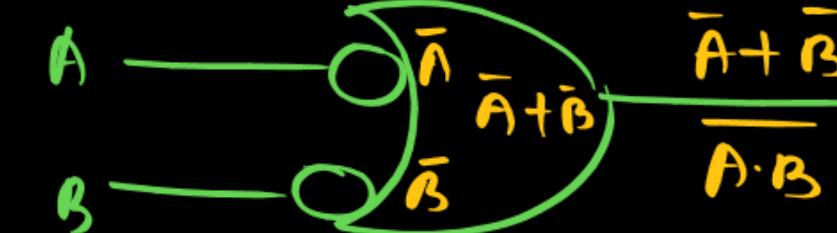
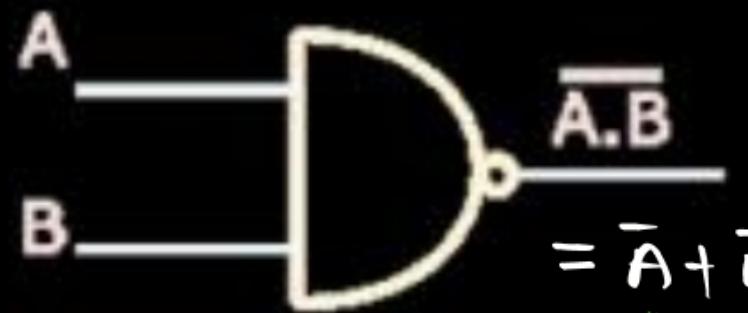
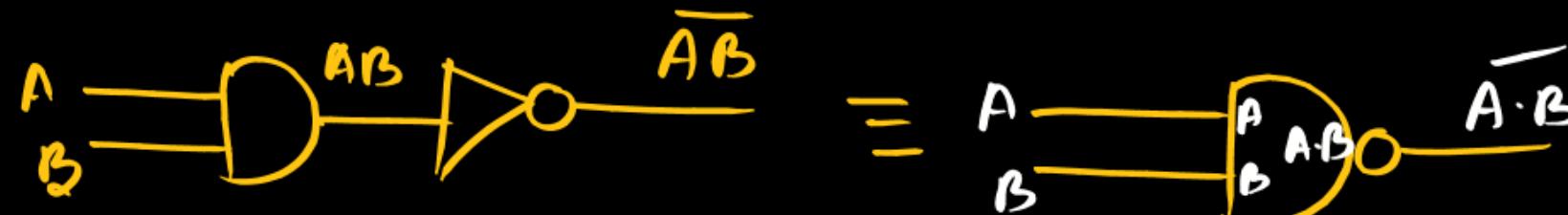
Q.3 If the logic given below are design with ECL then the output Y will be-



- fastest Logic
- A 0
  - B A
  - C 1
  - D None of the above

# NAND GATE

P  
W



De Morgan's Law

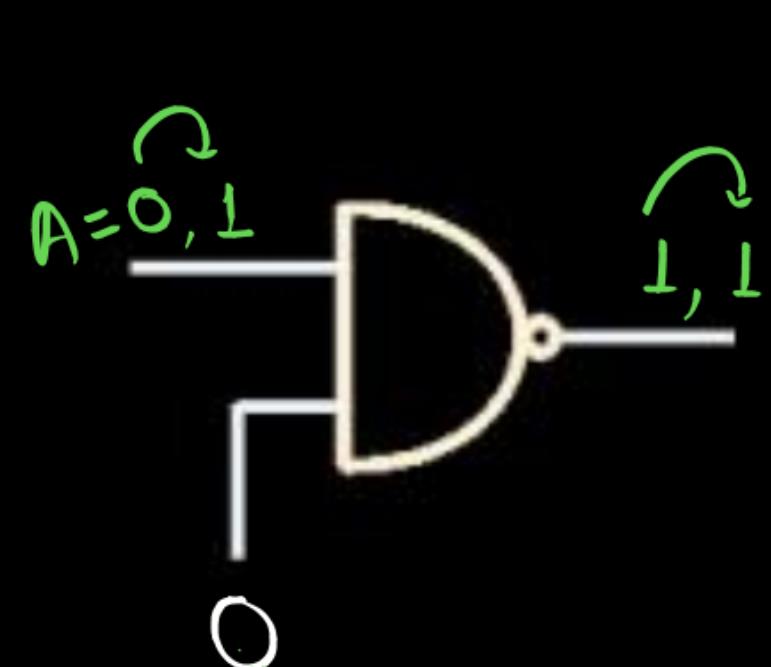
$$\overline{AB} = \overline{A} + \overline{B}$$

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

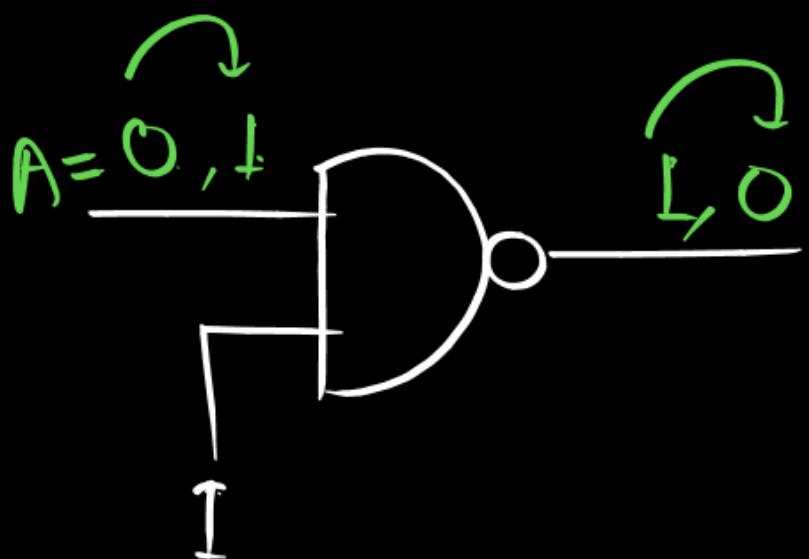
Bubbled OR = NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

## Enable/Disable



Control '0' Disable.



Control '1' Enabled.

Commutative Law ✓

$$\overline{A \cdot B} = \overline{B \cdot A}$$

Associative Law ✗

$$\overline{\overline{(A \cdot B)} \cdot C} \neq \overline{A \cdot (\overline{B \cdot C})}$$

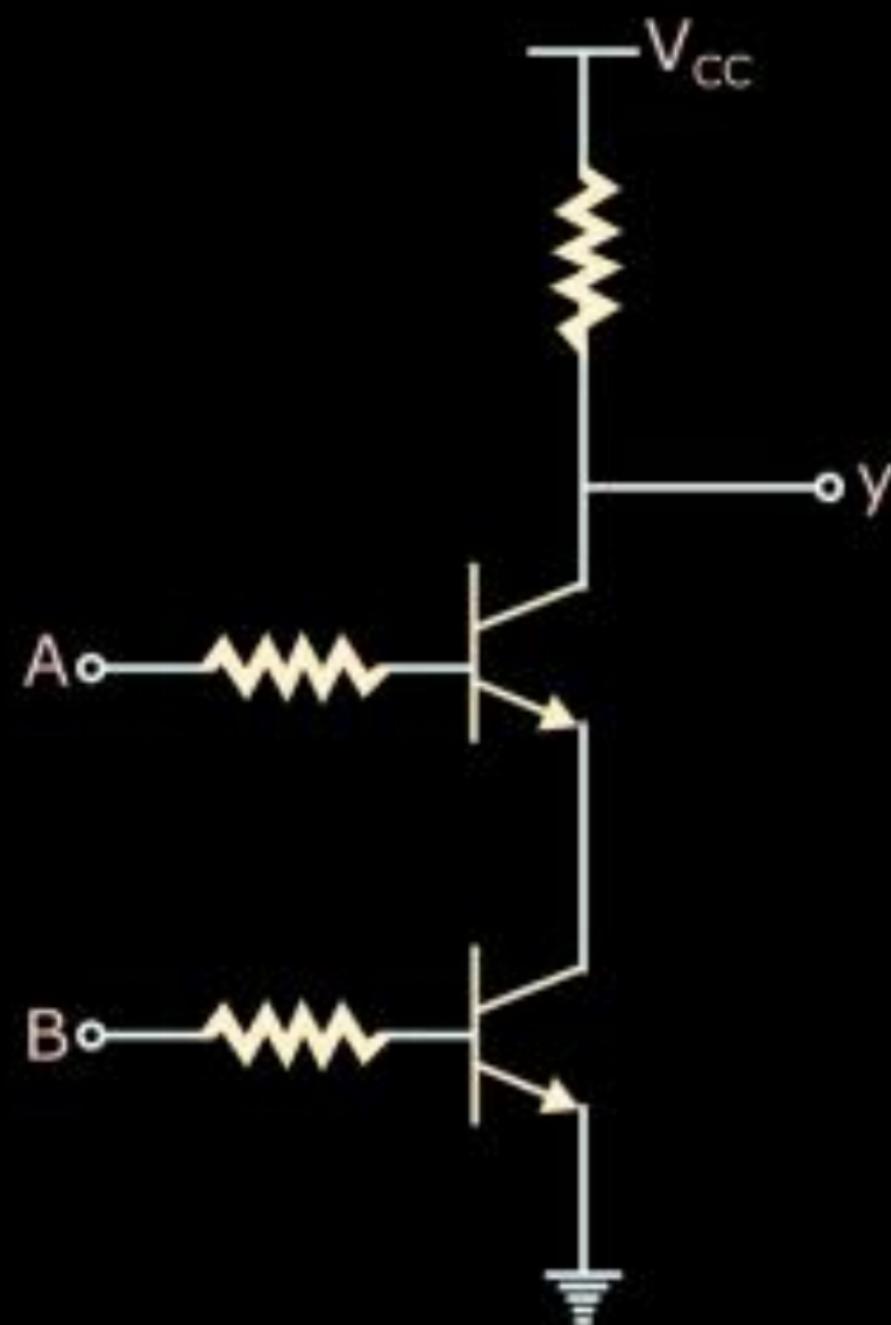


commutatiu  
✓

Associatiue Law

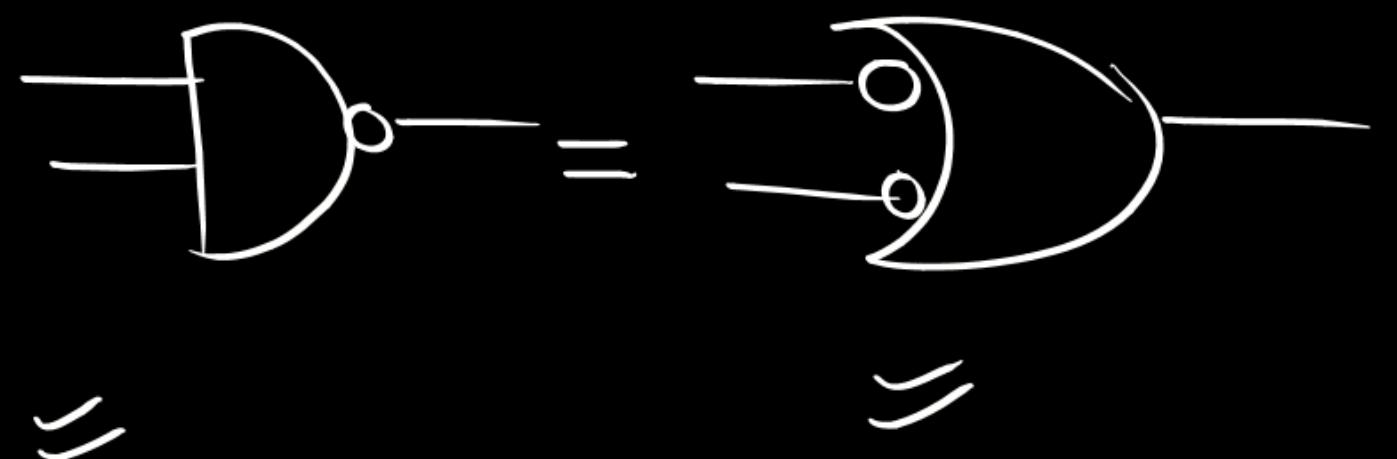
✗

# Circuit Diagram



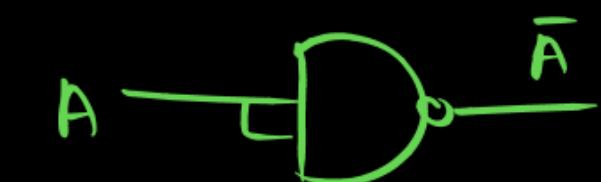
A	B	$T_A$	$T_B$	y
0	0			
0	1			
1	0			
1	1			

## Alternate Symbol

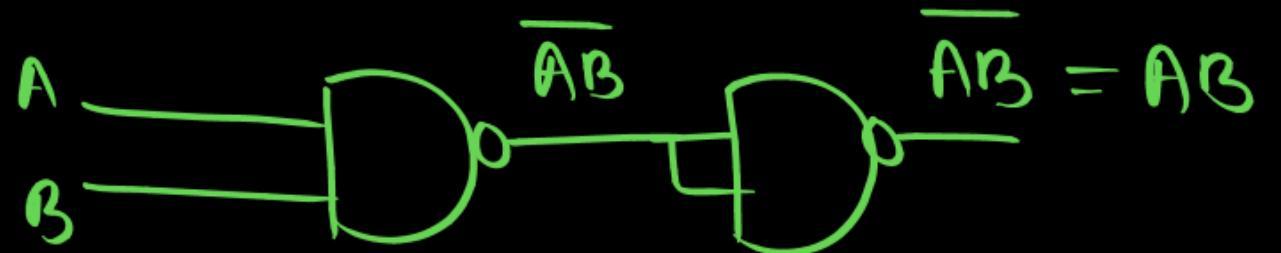


# NAND as Universal LOGIC

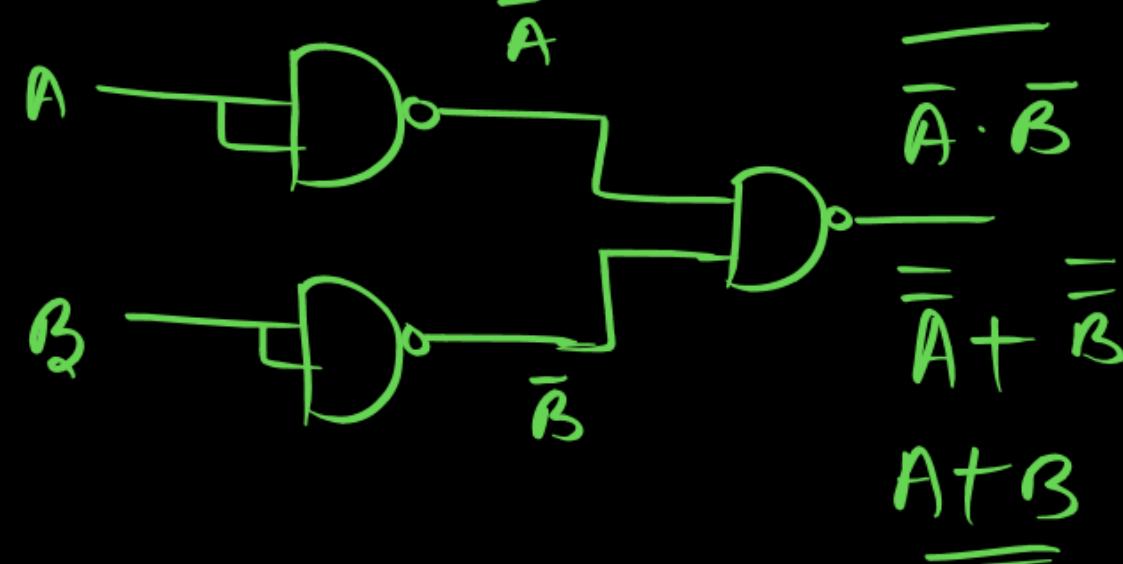
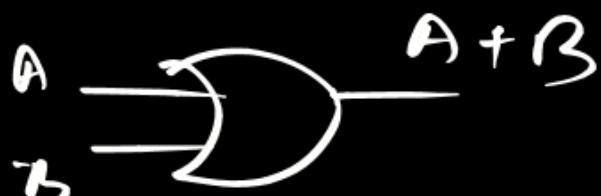
① NOT GATE:



② AND GATE

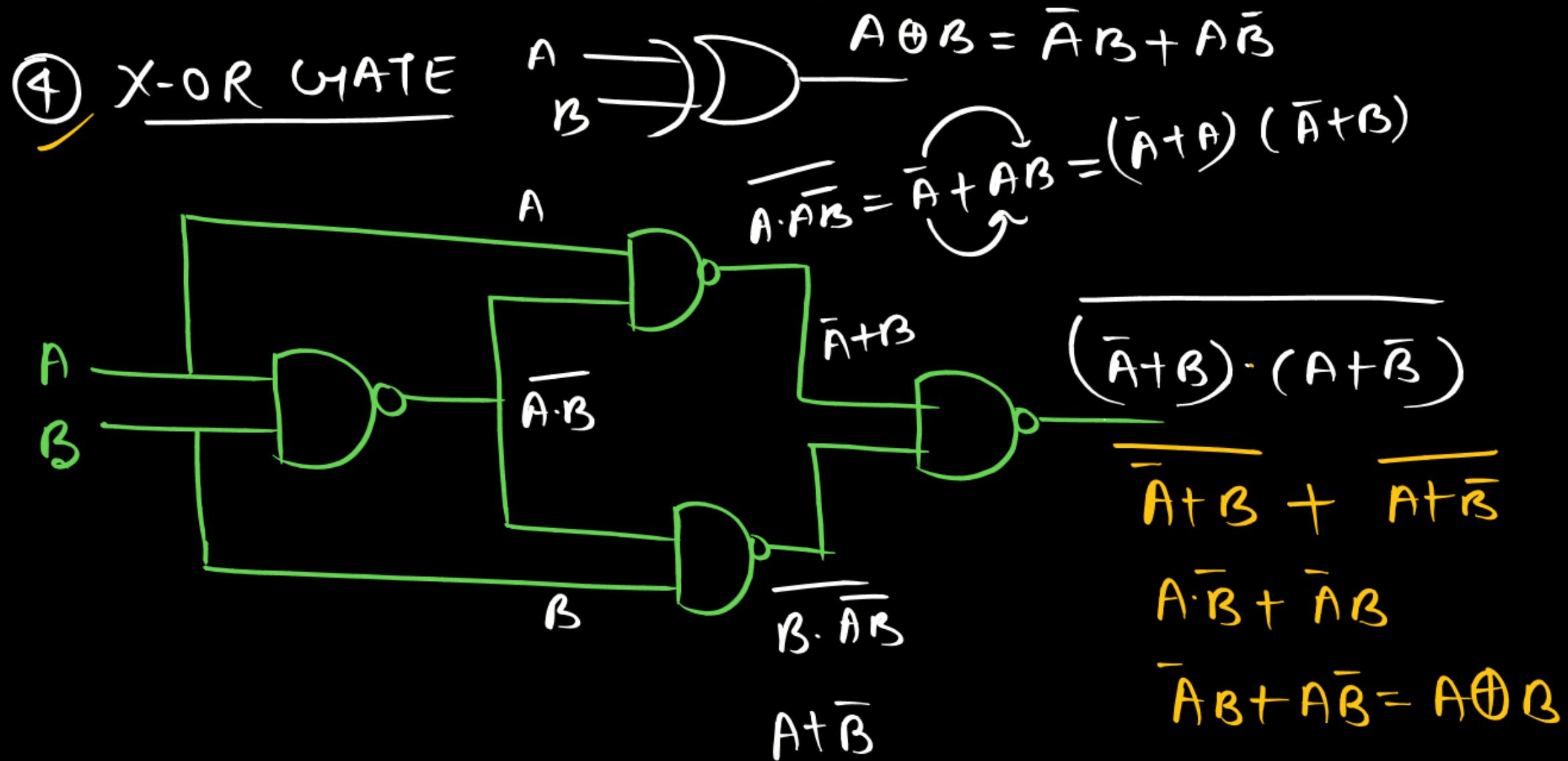


③ OR GATE:



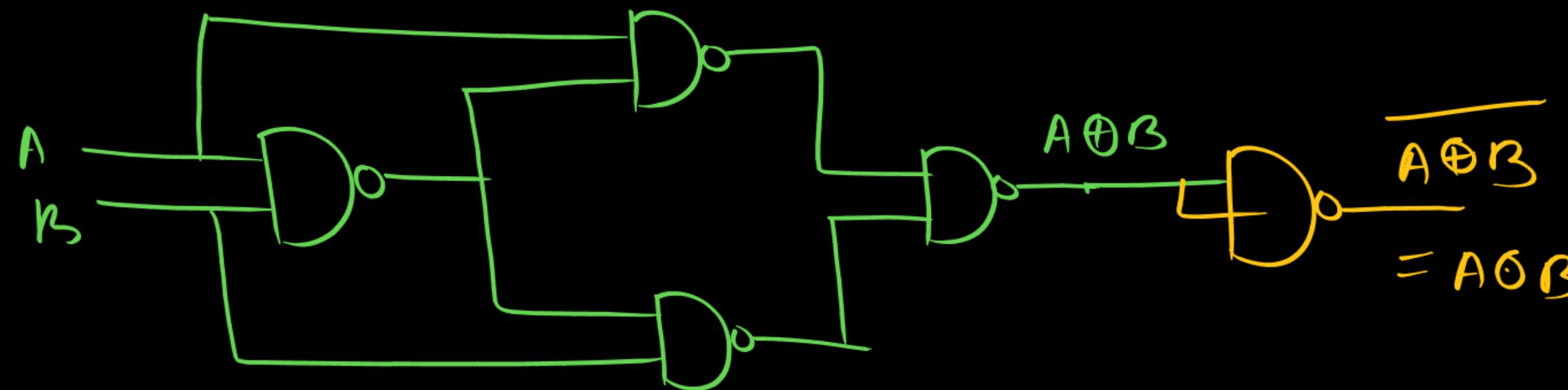
NOR

# NAND as Universal LOGIC



⑤ X-NOR GATE


$$A \oplus B = \overline{A \oplus B}$$
$$= \overline{AB} + A\overline{B}$$

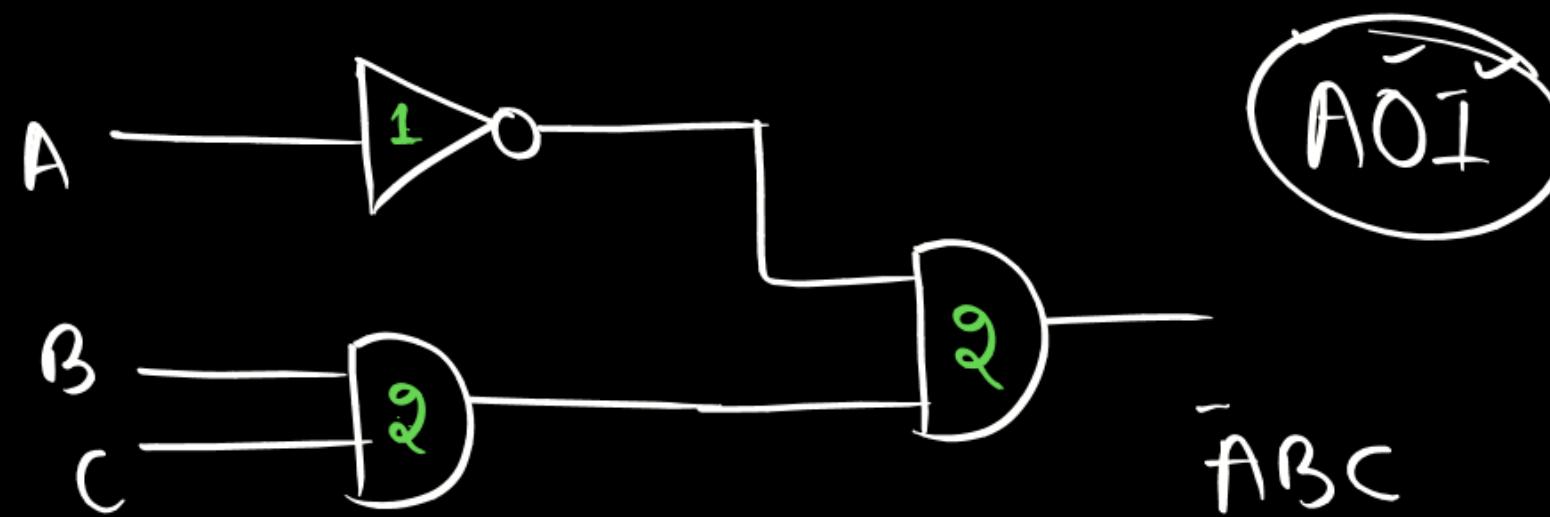


	NAND	NOR
NOT	1.	1
AND	2}	3
OR	3}	2
X-OR	4}	5
X-NOR	5}	4
NAND	1}	4
NOR	4}	1

# How To Find Minimum Number Of NAND GATE

$$Q = f = \bar{A}BC$$

Minimum no. of NAND GATE = ?



$$1 + 2 + 2 + \cancel{5} = 5$$

Ans

case(1)

Ex.

$$f = A \cdot \bar{B} \cdot C \cdot \bar{D} \cdot \bar{E} \cdots$$

$n \rightarrow$  no. of Variables.

$k \rightarrow$  no. of complement Variables.

NAND

$$(2n-2)+k$$

$$\textcircled{1} f = \bar{A} \cdot B \cdot C$$

$$h=3 \\ k=1$$

$$(2n-2)+k$$

$$(2 \times 3 - 2) + 1$$

$$(6 - 2) + 1$$

$$= \textcircled{5}$$

NOR

$$(3n-3)+k$$

$$(3 \times 3 - 3) + 1$$

$$6 + 1$$

$$= \textcircled{7}$$

NOR  $\textcircled{2} f = \bar{A} \cdot B \cdot \bar{C} \cdot D \cdot E \cdot F$   $h=6 \\ k=2$

$$(3n-3)+k$$

$$(2 \times 6 - 2) + 2$$

$$12$$

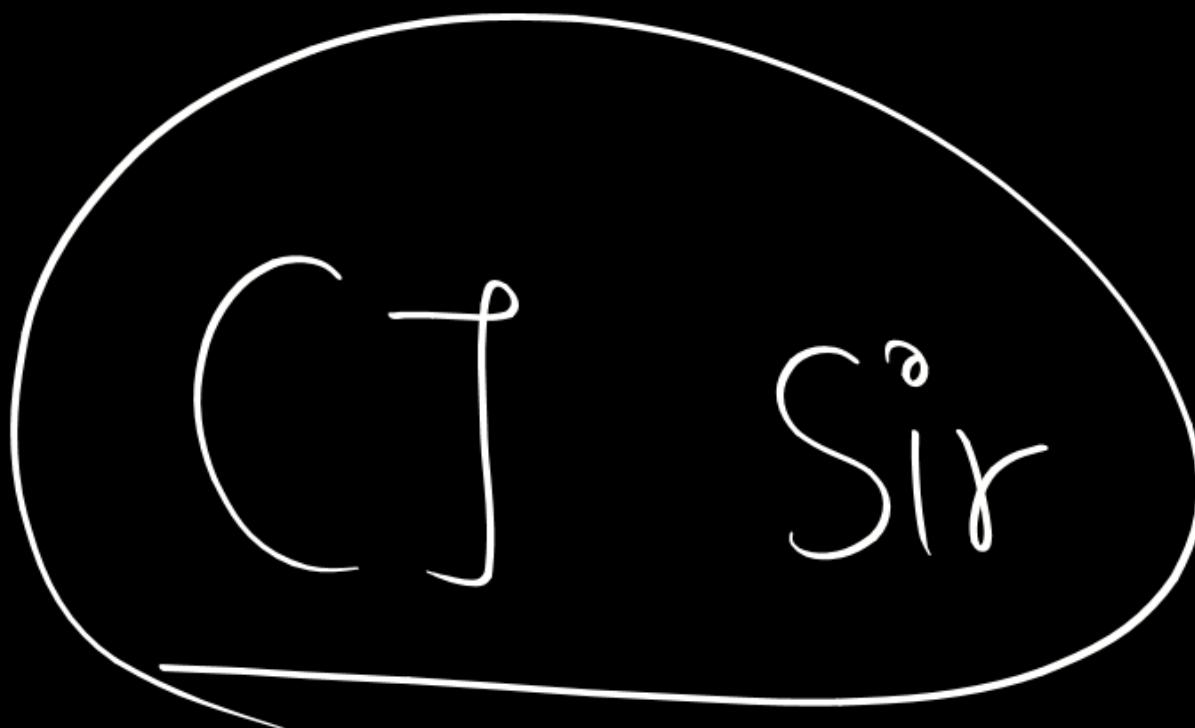
$$(3 \times 6 - 3) + 2$$

$$17$$

# How To Find Minimum Number Of NAND GATE

	case(3)	NAND	NOR
Ex. $f = \bar{A} + B + C$	$n=3$ $k=1$	$(3n-3) + k$ $(3 \times 3 - 3) + 1$ 7	$(2n-2) + k$ $(2 \times 3 - 2) + 1$ 5
Ex. $f = \bar{A} + B + \bar{C} + D + E + \bar{F}$	$n=6$ $k=3$	$(3n-3) + 3$ 18	$(2n-2) + 3$ 13

# How To Find Minimum Number Of NAND GATE



Joshua Bell

1 hours

NP

8.06 AM

\$18 

THANK  
You! ☺

