EC/EE/CS/IN

DIGITAL ELECTRONICS

51 Questions of Digital Electronics part 1

LECTURE NO. 15

CHANDAN JHA SIR (CJ SIR)

बेहतर से बेहतर की तलाश करो,

मिल जाए नदी तो समंदर की तलाश करो।

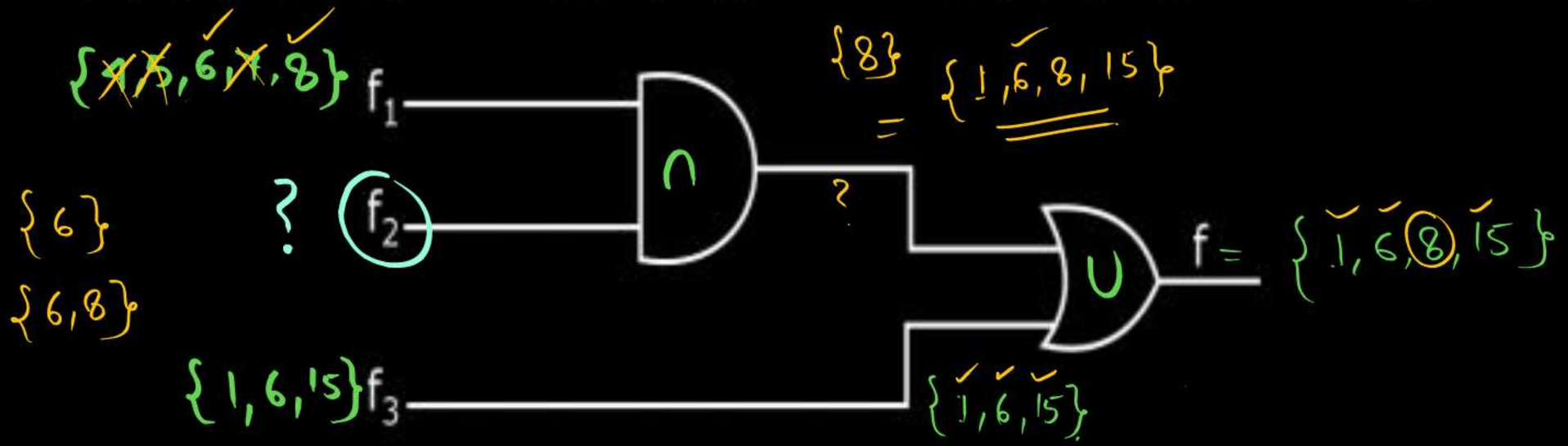
टूट जाते हैं शीशे पत्थरों की चोट से,

तोड़ से पत्थर ऐसे शीशे की तलाश करो।


जीवन में इतना तो संघर्ष कर
लेना चाहिए की अपने बच्चे का
आत्मविश्वास बढ़ाने के लिए
दूसरों का उदाहरण न देना पड़े।

51 Questions of Digital Electronics part 1

Ex. 1. $f_1 = \Sigma m(4,5,6,7,8)$ $f_3 = \Sigma m(1,6,15)$ $f = \Sigma m(1,6,8,15)$. Then f_2 will be-



(A) Σm (4, 6)

(B) Σm (4, 8)

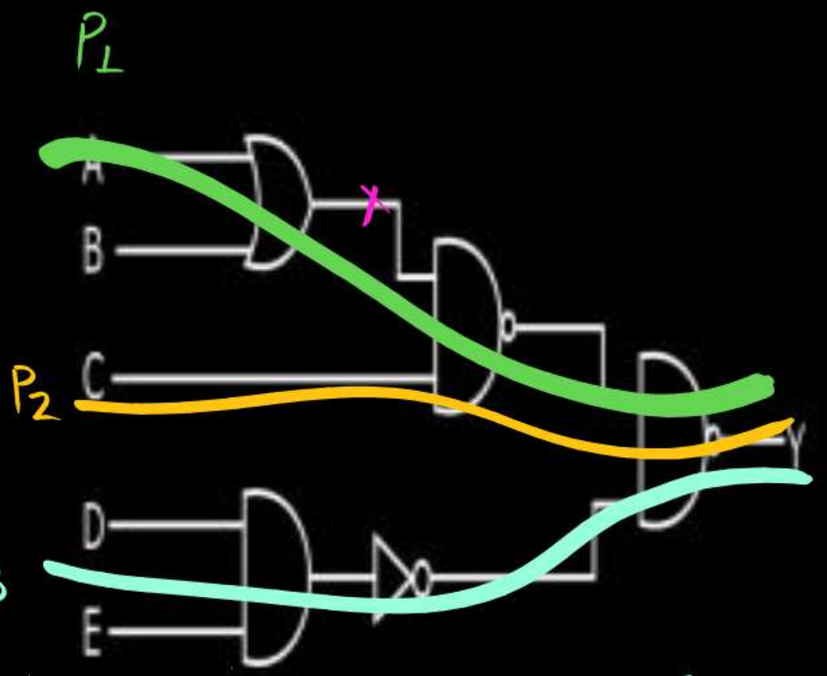
(C) Σm (6, 8)

(D) Σm (4, 6, 8)

51 Questions of Digital Electronics part 1

Ex. 2. If delays through, the gate are given as
OR gate = 5 sec
NAND gate = 4 sec
AND gate = 2 sec
Inverter gate = 1 sec
The worst case propagation delay is

[Maximum delay]



P1
5+4+9 = 13ns

P2
4+4 = 8ns

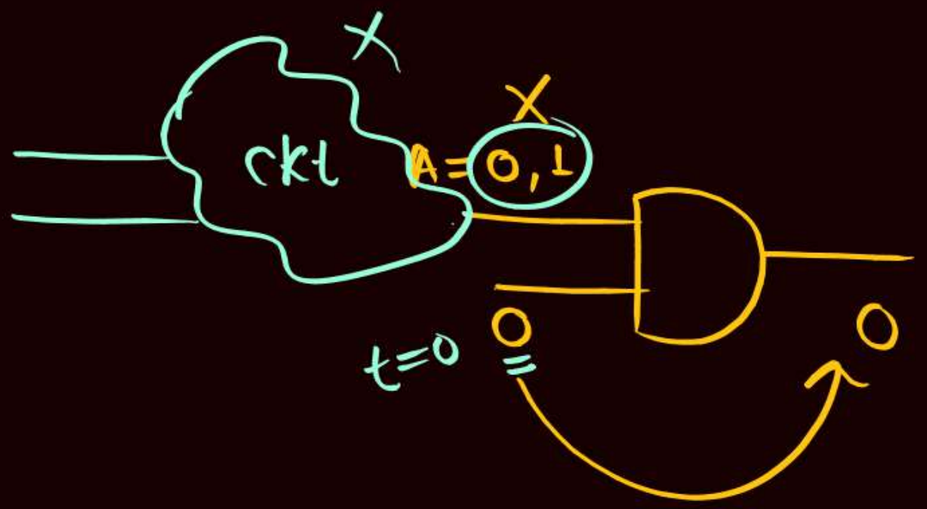
P3
2+1+4
7ns

A 12

B 16

C 13

D 5

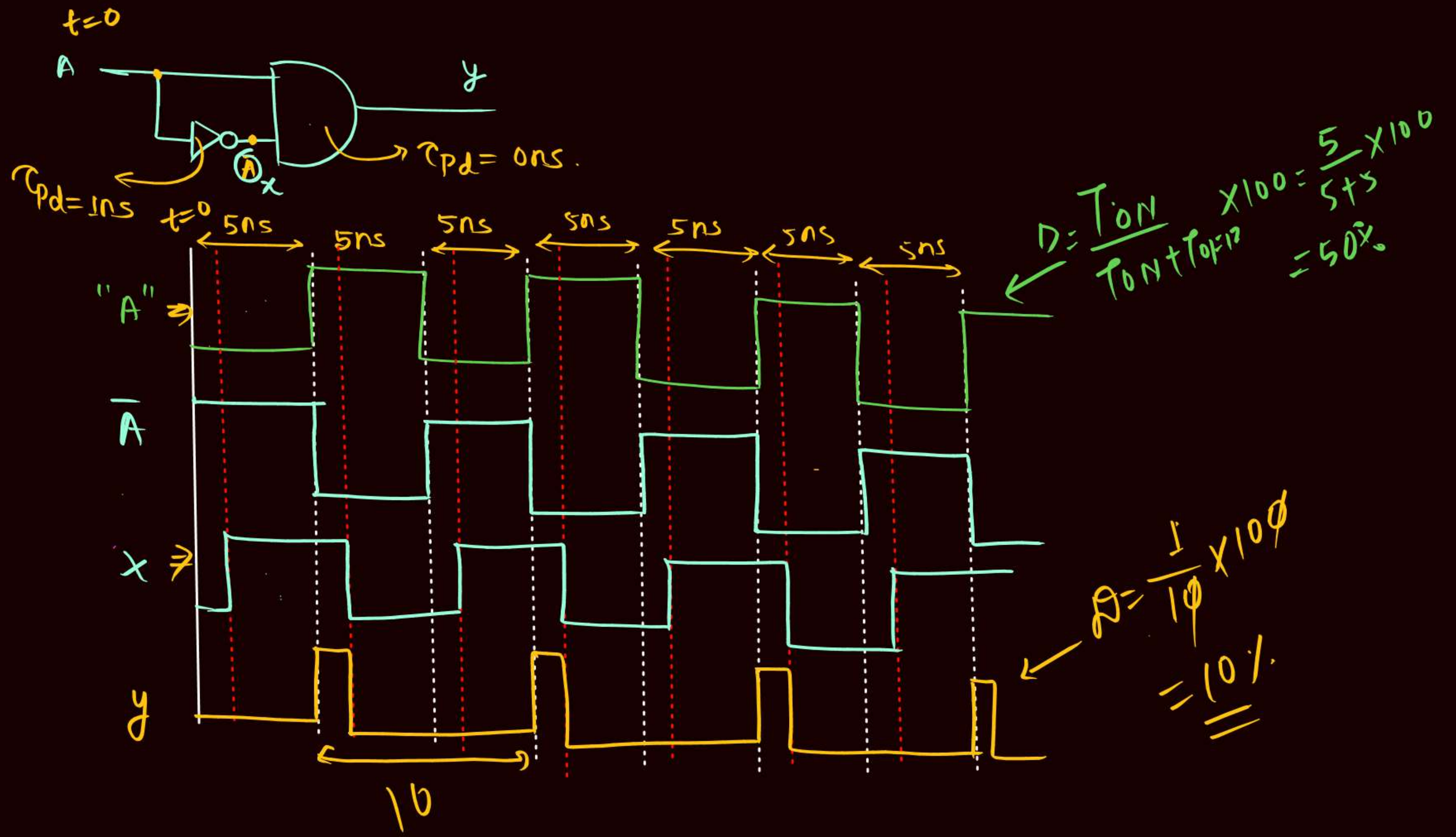


Maximum delay

$\tau_{ckt} + \tau_{AND}$

Minimum delay

$\Rightarrow \tau_{AND}$

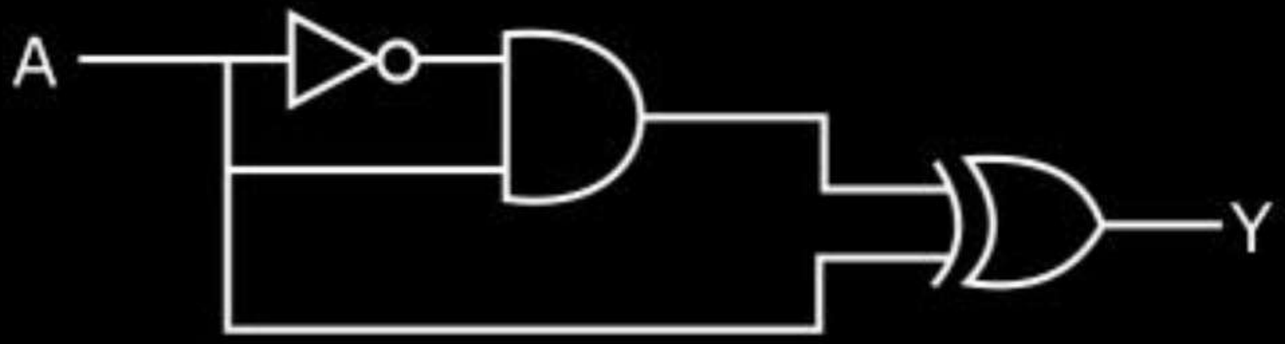

t=0
A
y
τ_{pd}= 0ns.
τ_{pd}=1ns
t=0
5ns
5ns
5ns
5ns
5ns
5ns
5ns
"A"
$\bar{A}$
x
y
10
D= $\frac{T_{ON}}{T_{ON}+T_{OFF}}$ x100 = $\frac{5}{5+5}$ x100 = 50%.
D= $\frac{1}{10}$ x100 = 10%

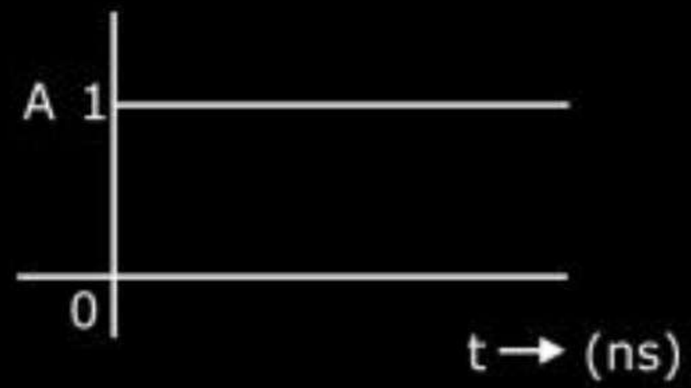
51 Questions of Digital Electronics part 1

Ex. 3. Consider the circuit shown in figure below

If propagation delay of NOT gate is 10 nsec, AND gate is 20 nsec and *X-OR* gate is 10 nsec.

If A is connected to V_{CC} at t = 0, then waveform for output Y is



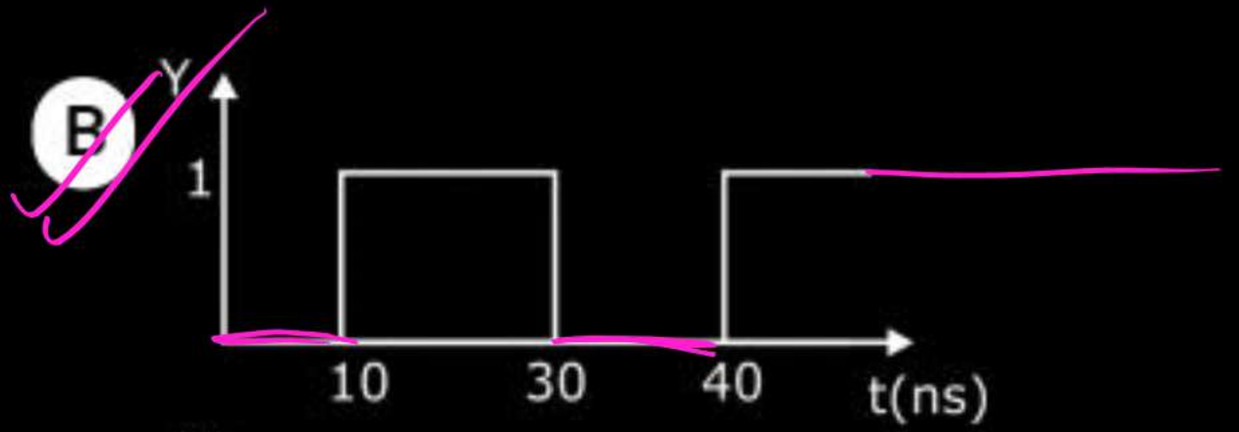


51 Questions of Digital Electronics part 1

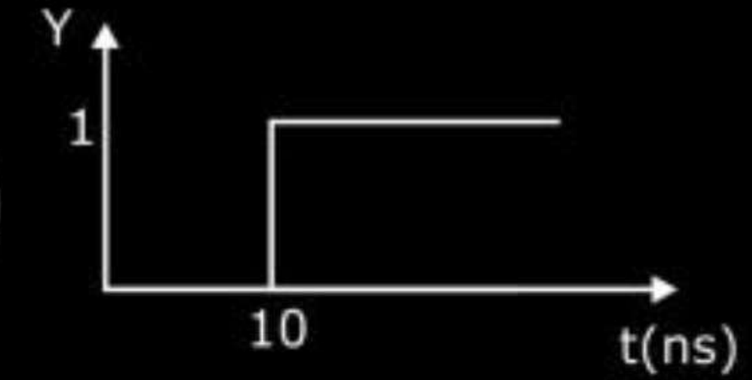
Ex. 3.

A

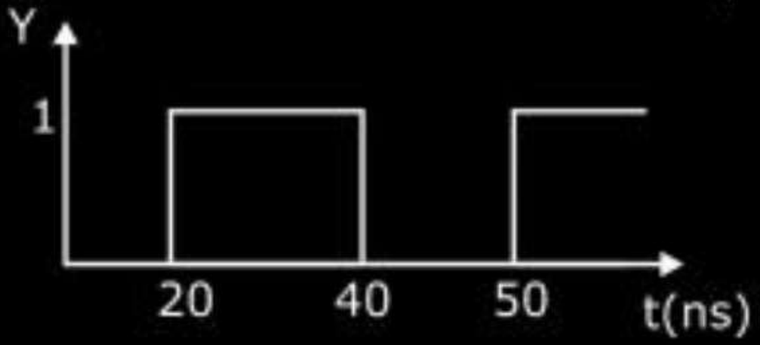
B



C



D



51 Questions of Digital Electronics part 1

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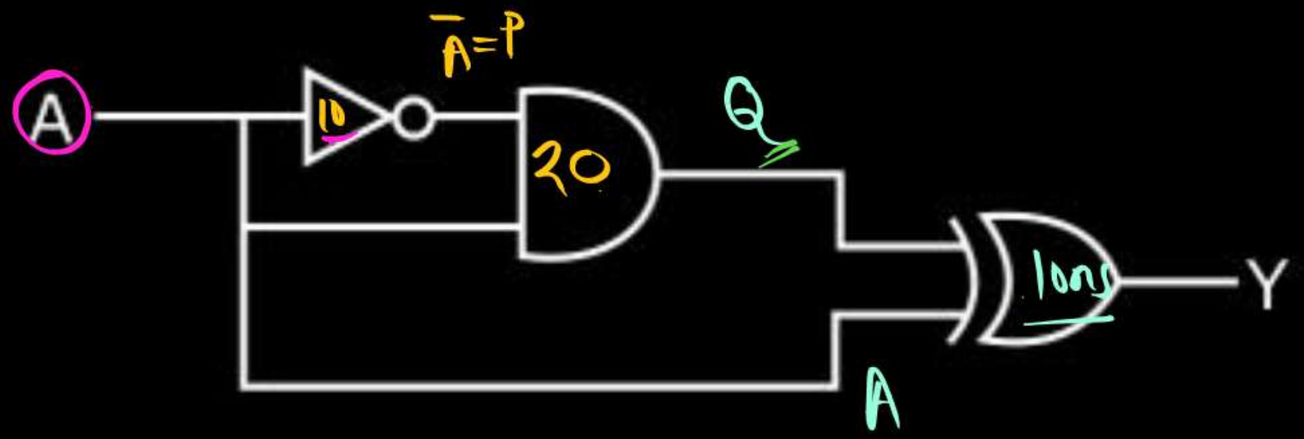
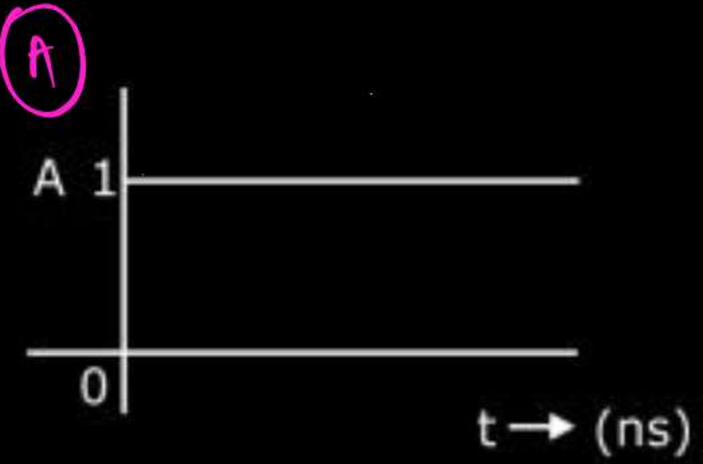
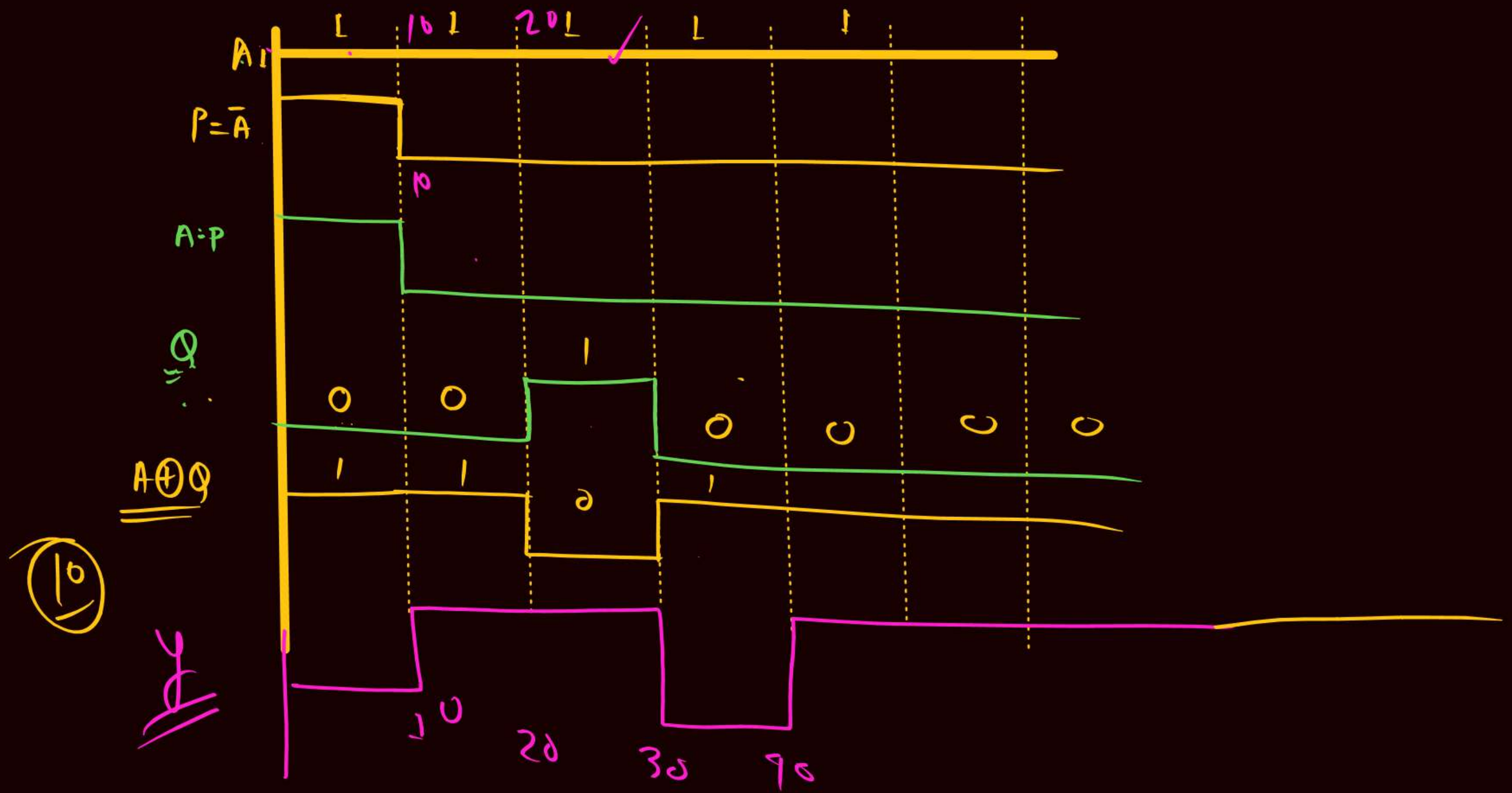





A
P=Ā
A:P
Q
A⊕Q
Y
10
20
30
40

NOTE

$f = \bar{A} \cdot B \cdot \bar{C} \cdot D \cdot \bar{E} \cdot F \ldots\ldots$

$n \rightarrow$ no. of Variables.

$k \rightarrow$ no. of Variables with complements.

NAND

$(2n-2)+k$

Ex. $f = \bar{A} \cdot \bar{B} \cdot C$

$n=3 \quad k=2$

$(2\times3-2)+2$

6

NOR

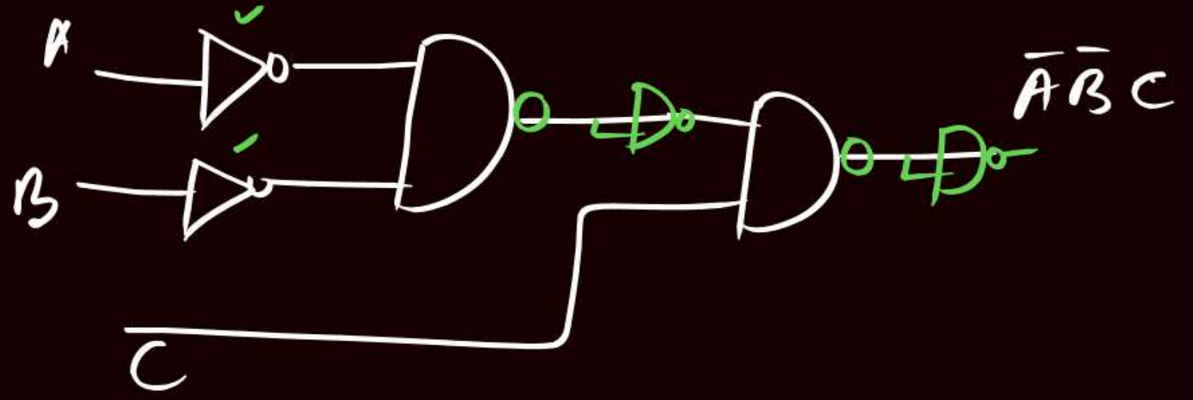
$(3n-3)-k$

Ex. $(3\times3-3)-2$

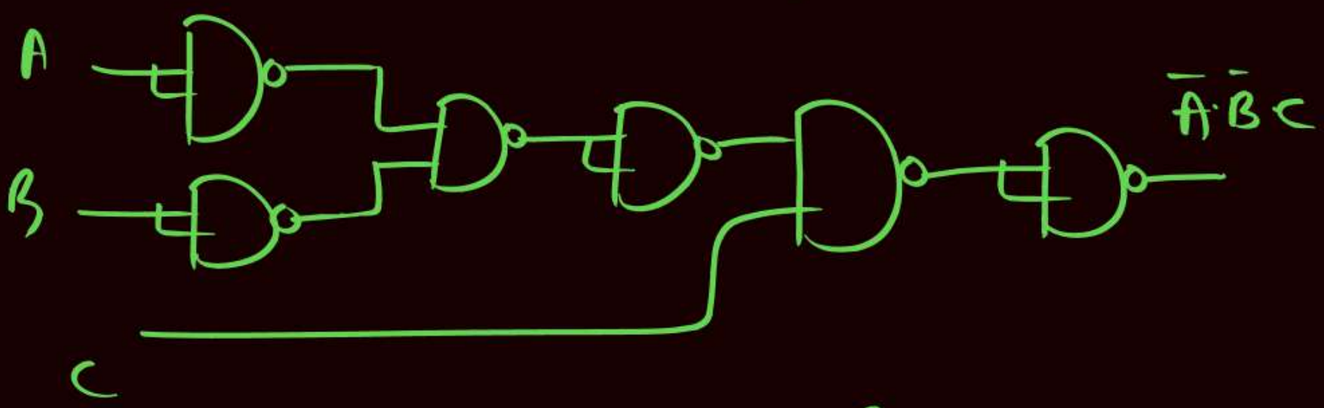
$(9-3)-2$

4

NAND



6



6

NOTE

$f = \bar{A} \cdot B \cdot \bar{C} \cdot D \cdot \bar{E} \cdot F \ldots\ldots$

$n \rightarrow$ no. of Variables.

$K \rightarrow$ no. of Variables with complements.

NAND

$(2n-2)+K$

Ex. $f = \bar{A} \cdot \bar{B} \cdot C$

$n=3 \quad K=2$

$(2\times3-2)+2$

6

NOR

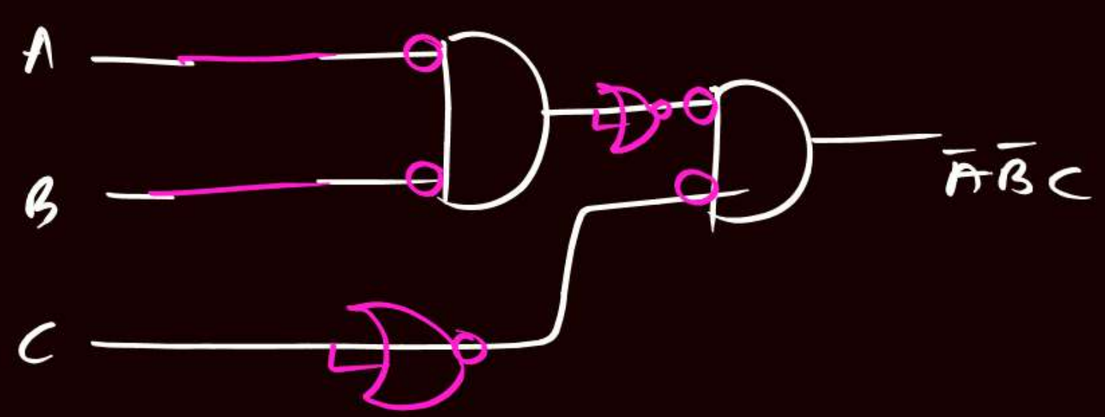
$(3n-3)-k$

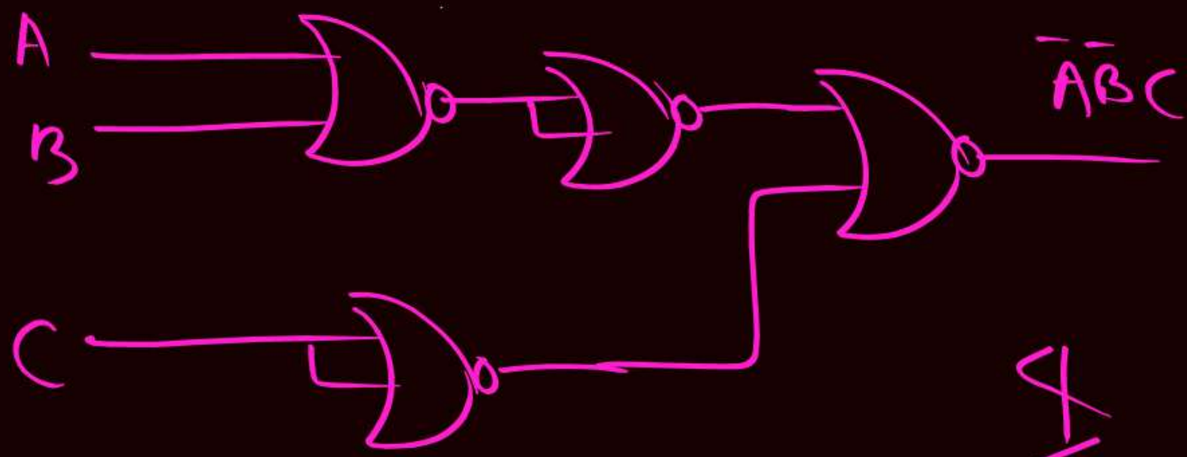
Ex. $(3\times3-3)-2$

$(9-3)-2$

4

NOR





4

51 Questions of Digital Electronics part 1

Ex. 4. Find the minimum number of two input NAND GATE required to implement the Boolean function-

$f = AB + CD + F$

3.

$AB + CD = X$ → (3)

$f = X + F$ → (3)

(3 + 3)

A 9

B 8

C 6

D 12

51 Questions of Digital Electronics part 1

HW.

Ex. 5. Find the minimum number of two input NAND GATE required to implement the function-

$f(A, B, C, D) = AB + BC + CD + DA$

(A) 9

(B) 8

(C) 6

(D) 12

51 Questions of Digital Electronics part 1

Ex. 6. Find the minimum number of two input NAND GATE required to implement the Boolean function-

$f = A\overline{B} + C$

(A) 3
(B) 4
(C) 5
(D) 6

51 Questions of Digital Electronics part 1

Ex. 7. For a Mod-10 counter, Johnson counter uses X FF's, ring counter uses Y FF's and ripple counter uses Z FF's. Then X + Y + Z will be

FF

$M \leq 2^n$

$n \geq \log_2 M$

$n \geq \log_2 10$

$n \geq 3.\text{something}$

$n = 4$

Johnson counter → MOD 2N

$= 10$

Ring counter → MOD → 10

M

Ripple counter ⇒ MOD = 10

N → FF

X = 5

N-FF

Y = 10

Z = 4

$\leq 2^n$

X + Y + Z

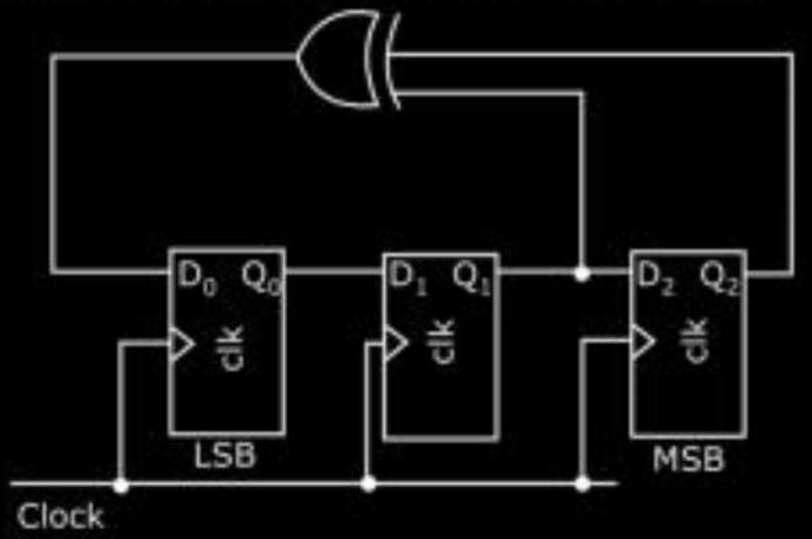
5 + 10 + 4 = 19

51 Questions of Digital Electronics part 1

HW.

Ex. 8. Consider the circuit below with initial state $Q_0 = 1$, $Q_1 = Q_2 = 0$. The state of the circuit is given by the value of $4Q_2 + 2Q_1 + Q_0$

which one of the following is the correct state sequence of the circuit?



A 1,3,4,6,7,5,2

B 1,2,5,3,7,6,4

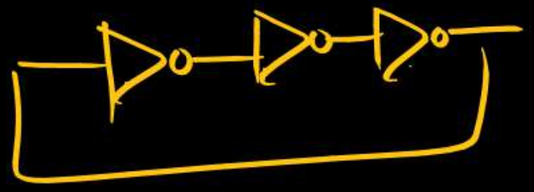
C 1,2,7,3,5,6,4

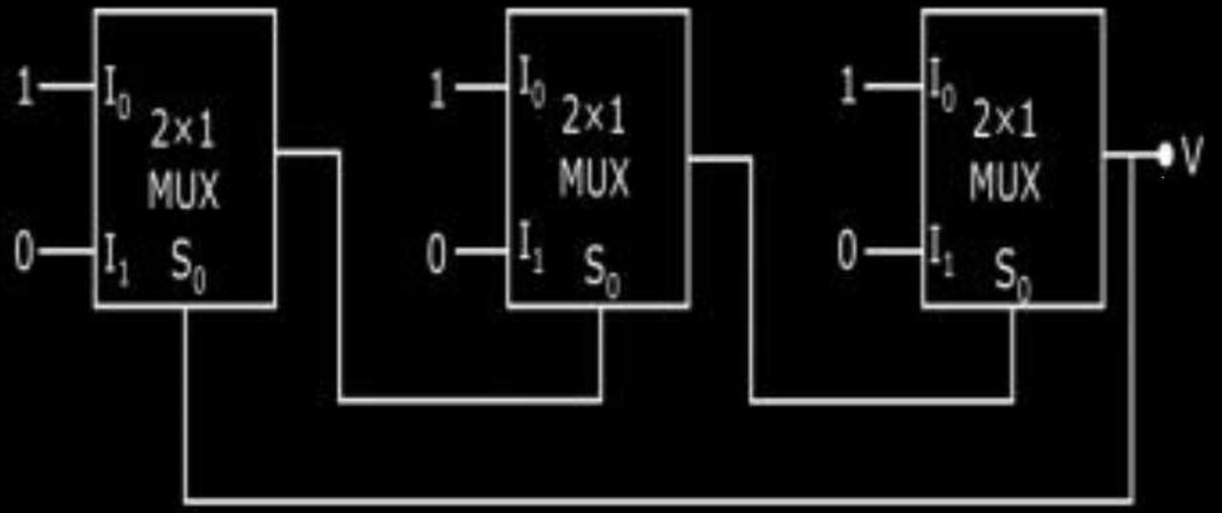
D 1,6,5,7,2,3,4

51 Questions of Digital Electronics part 1

HW

Ex. 9. Consider the below circuit: The propagation delay of each multiplexer is 50 ns. The frequency of the output signal V is





(A) 4 MHz

(B) 4.33 MHz

(C) 5 MHz

(D) 5.33 MHz

51 Questions of Digital Electronics part 1

Ex. 10. The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0,0,1,1,2,2,3,3,0,0,...) is_____.

A 0

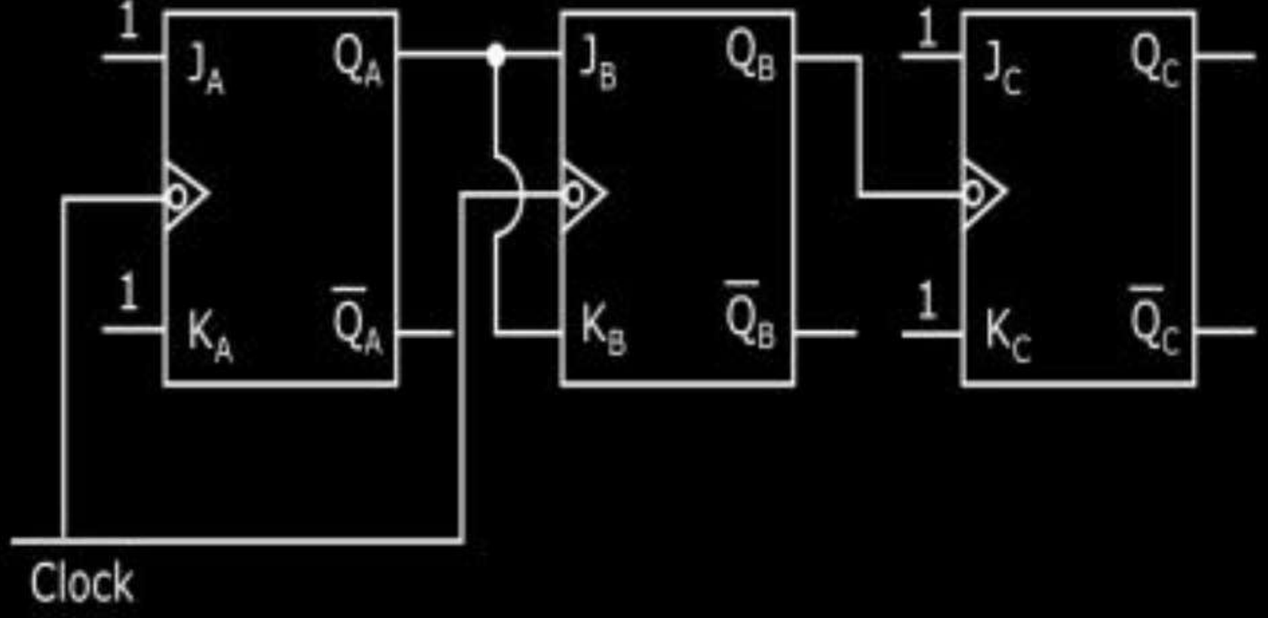
B 1

C 2

D 3

51 Questions of Digital Electronics part 1

Ex. 11. For the circuit shown in the figure, if the present state is 011 (Q_C Q_B Q_A) Then after 3 clock cycles state is

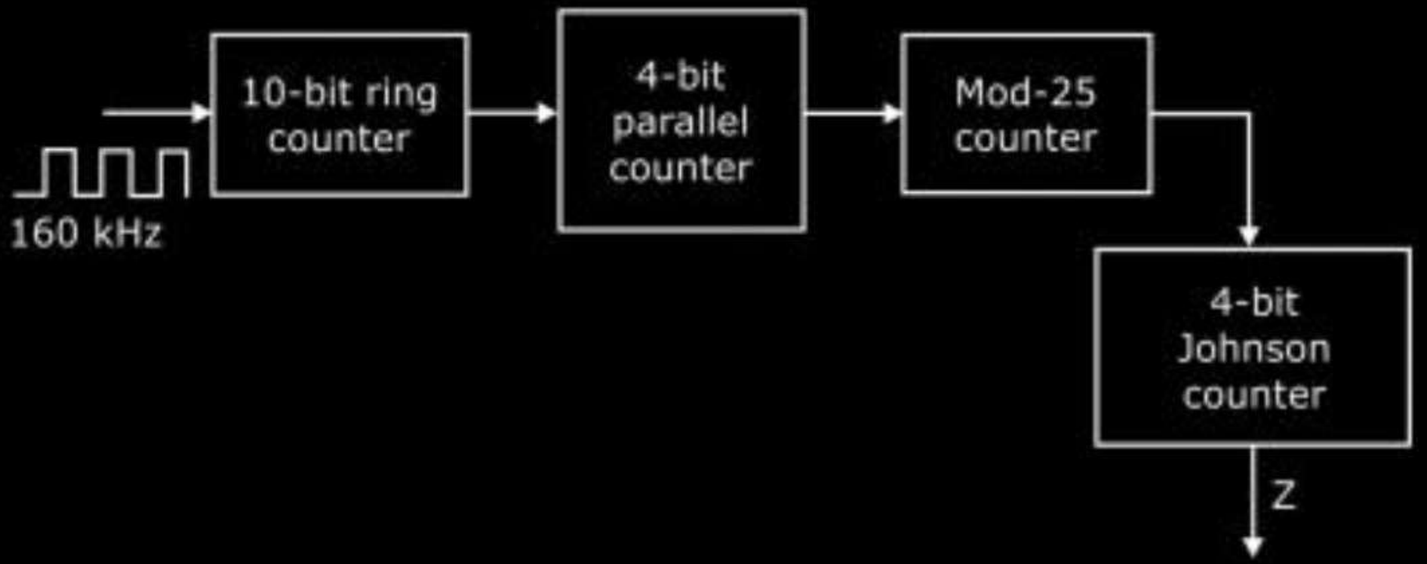


(A) 110 (B) 000

(C) 111 (D) 001

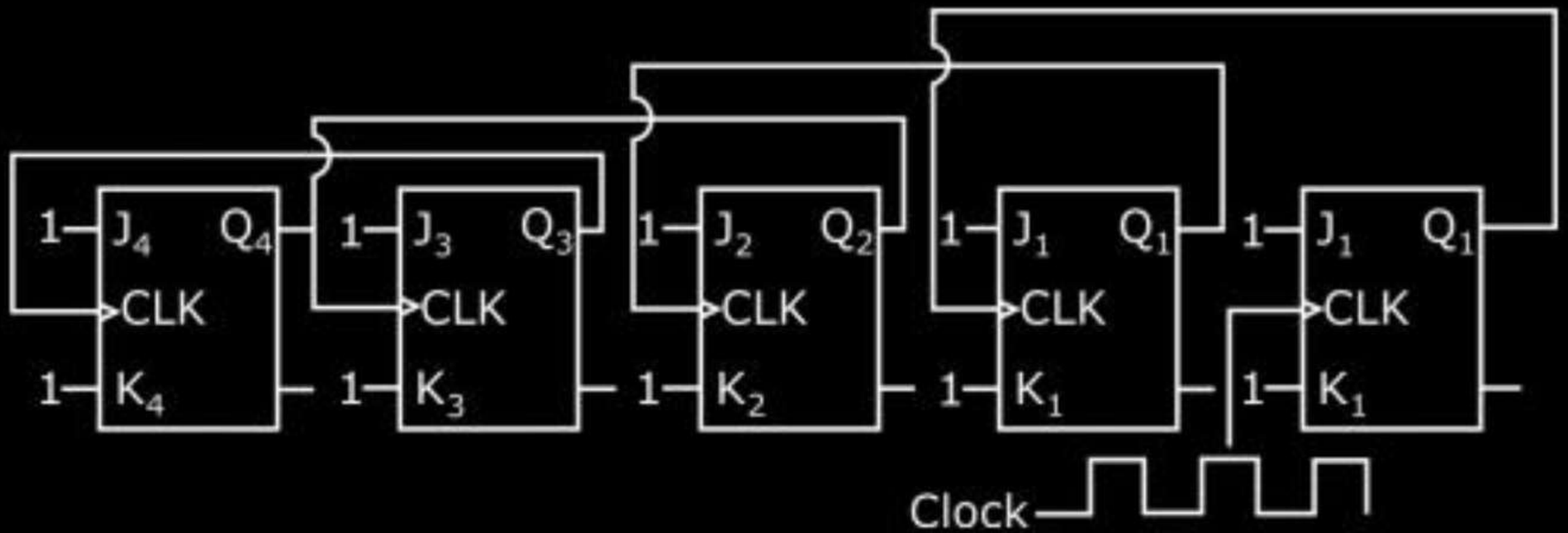
51 Questions of Digital Electronics part 1

Ex. 12. Frequency of output (z) is _____ Hz.



51 Questions of Digital Electronics part 1

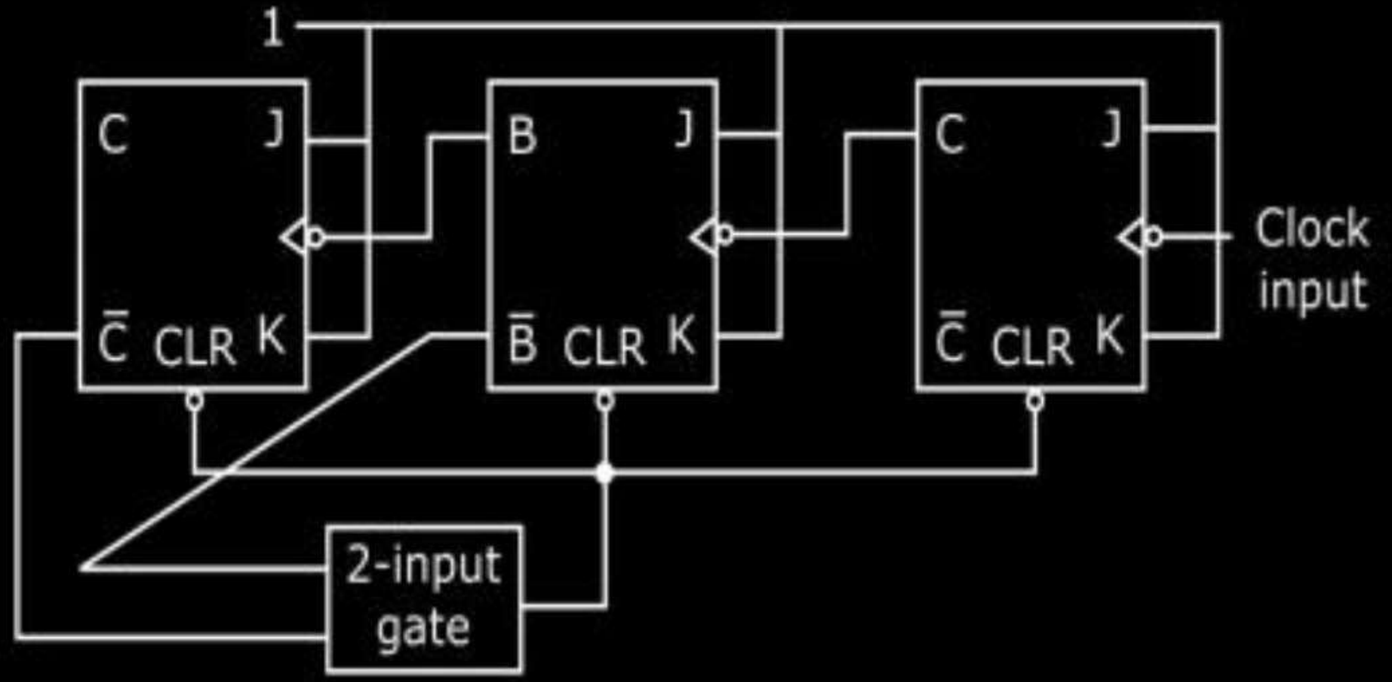
Ex. 13. Five J-K flip-flops are cascaded to form the circuit shown in figure. Clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in KHz) of the waveform at Q_3 is _____ .



51 Questions of Digital Electronics part 1

Ex. 14. In the modulo-6 ripple counter shown in below, figure the output of the 2-input gate is used to clear the J-K flip-flops.

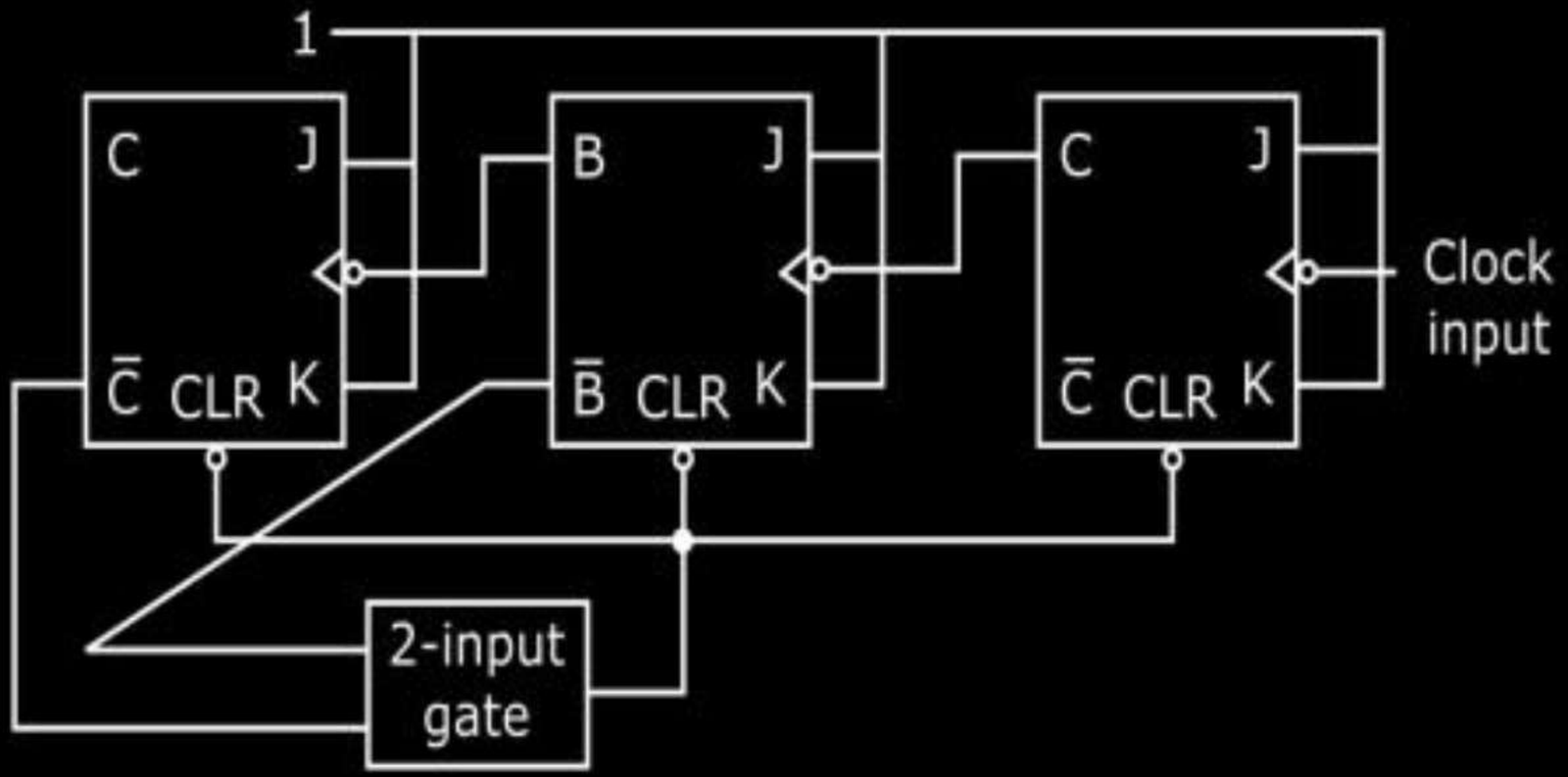
The 2-input gate is



(A) a NOR gate (B) an EX-OR gate

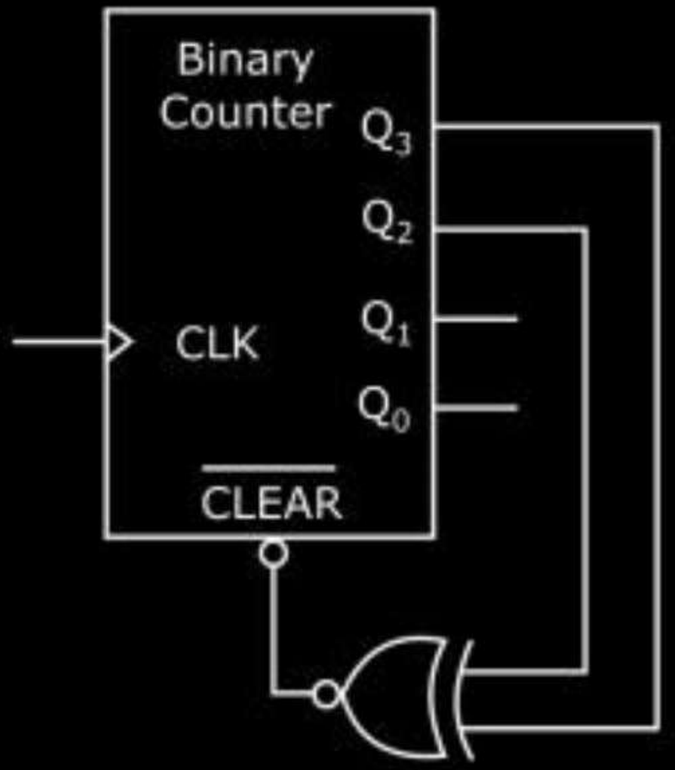
(C) an OR gate (D) an AND gate

51 Questions of Digital Electronics part 1



51 Questions of Digital Electronics part 1

Ex. 15. The figure shows a binary counter with synchronous clear input. With the decoding log shown, the counter works as a



A mod-2 counter

B mod-4 counter

C mod-5 counter

D mod-6 counter


THANK
YOU!