EC/EE/CS/IN

DIGITAL ELECTRONICS

51 Questions of Digital Electronics part-II

LECTURE NO. 16

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शौक को कभी पाला नहीं जाता,
काँच के खिलौनों को कभी उछाला नहीं जाता
मिल जाती हैं मंजिल कोशिश करने पर
हर बात को किस्मत पर टाला नहीं जाता!!

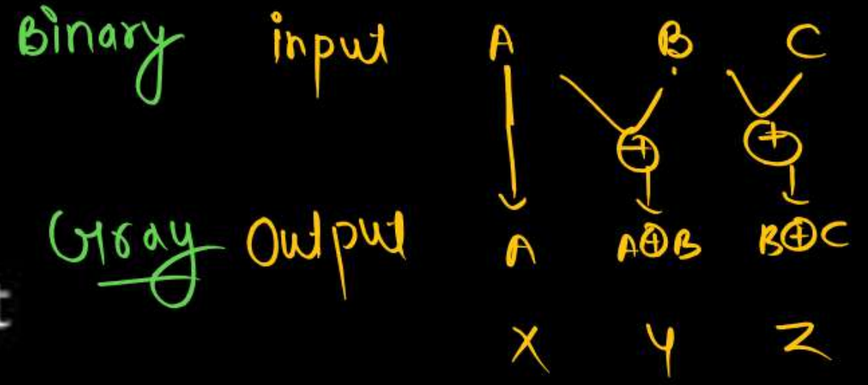
Q.1 The combination circuit shown in the figure below represents

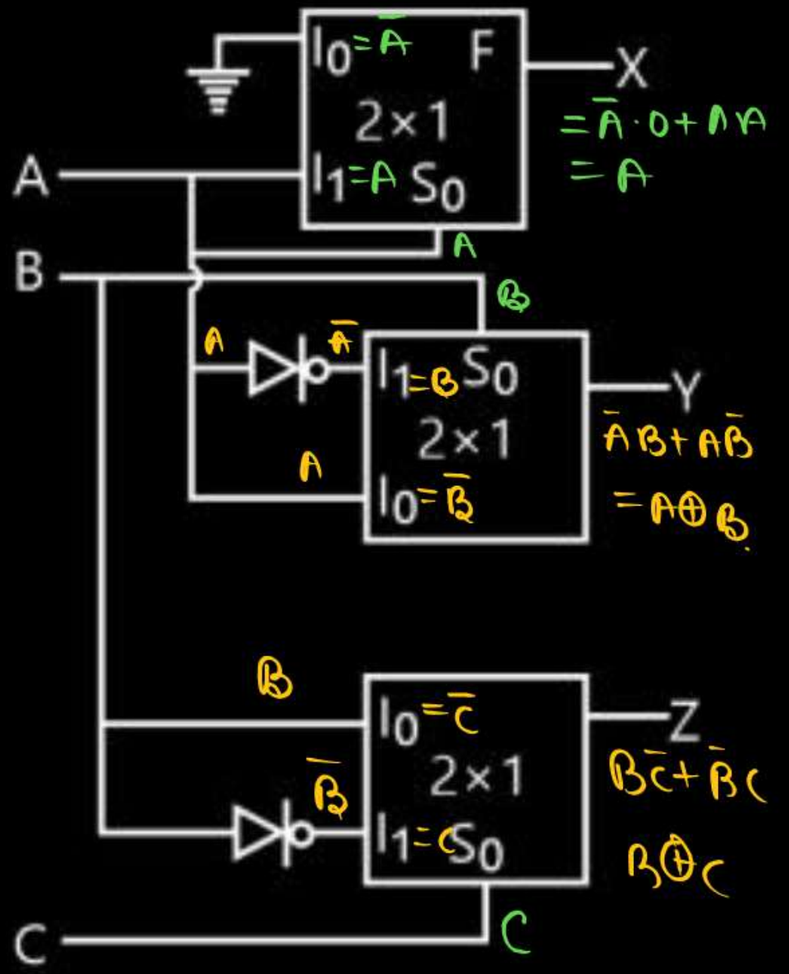
A Priority Encoder

B Comparator Circuit

C Binary to Grey code converter

D Odd sequence circuit





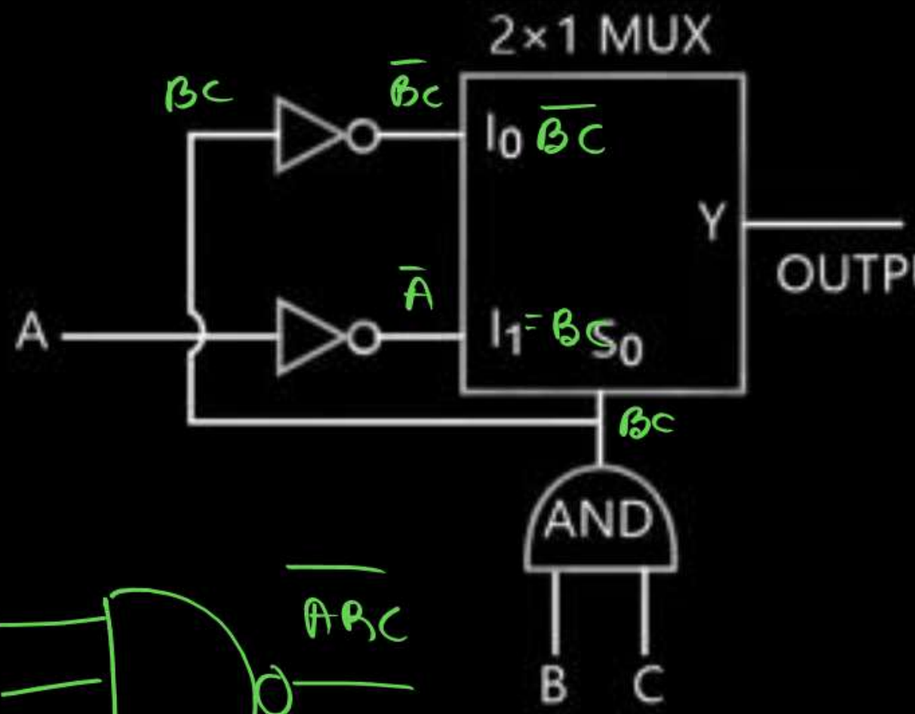
Q.2 The combinational circuit given below implements which of the following

(A) NOR gate

(B) XOR gate

(C) NAND gate

(D) None of these



$= \overline{BC} \cdot \overline{BC} + \bar{A}BC$

$= \overline{BC} + \bar{A}BC \quad BC = X$

$= \bar{X} + \bar{A}X$

$= (\bar{A} + \bar{X})(\bar{X} + X)$

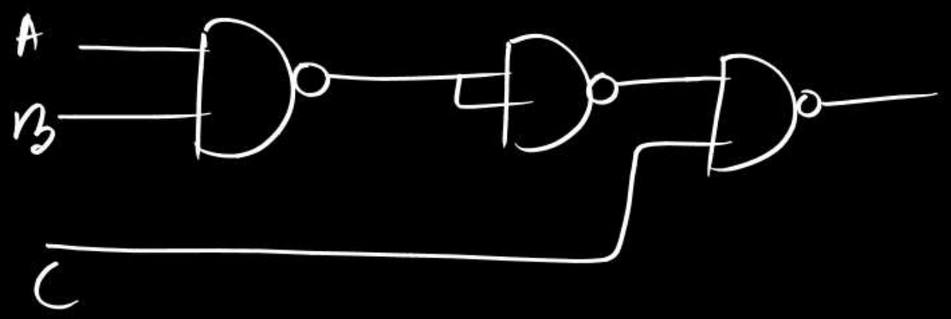
$= \bar{A} + \bar{X}$

$= \overline{A \cdot X}$

$= \overline{ABC}$

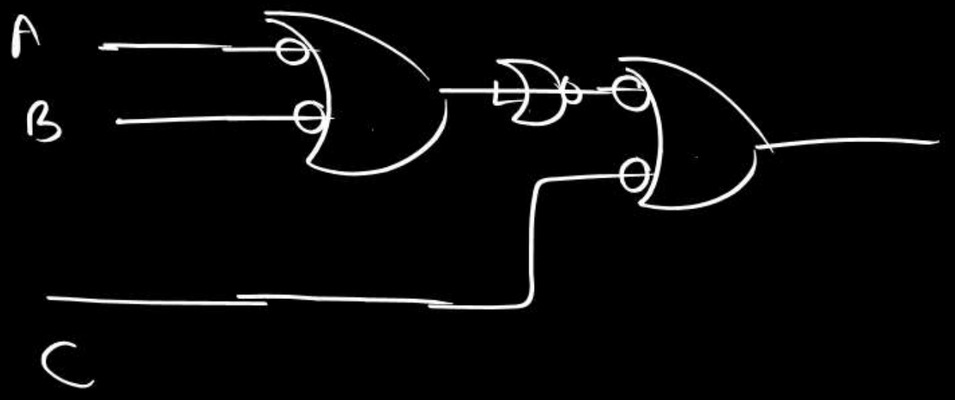
$f = \overline{A \cdot B \cdot C}$

↳ Two input NAND GATE ?



$f = \bar{A} + \bar{B} + \bar{C}$

(n=3) (k=3)



$\Rightarrow (3n-3)-k$

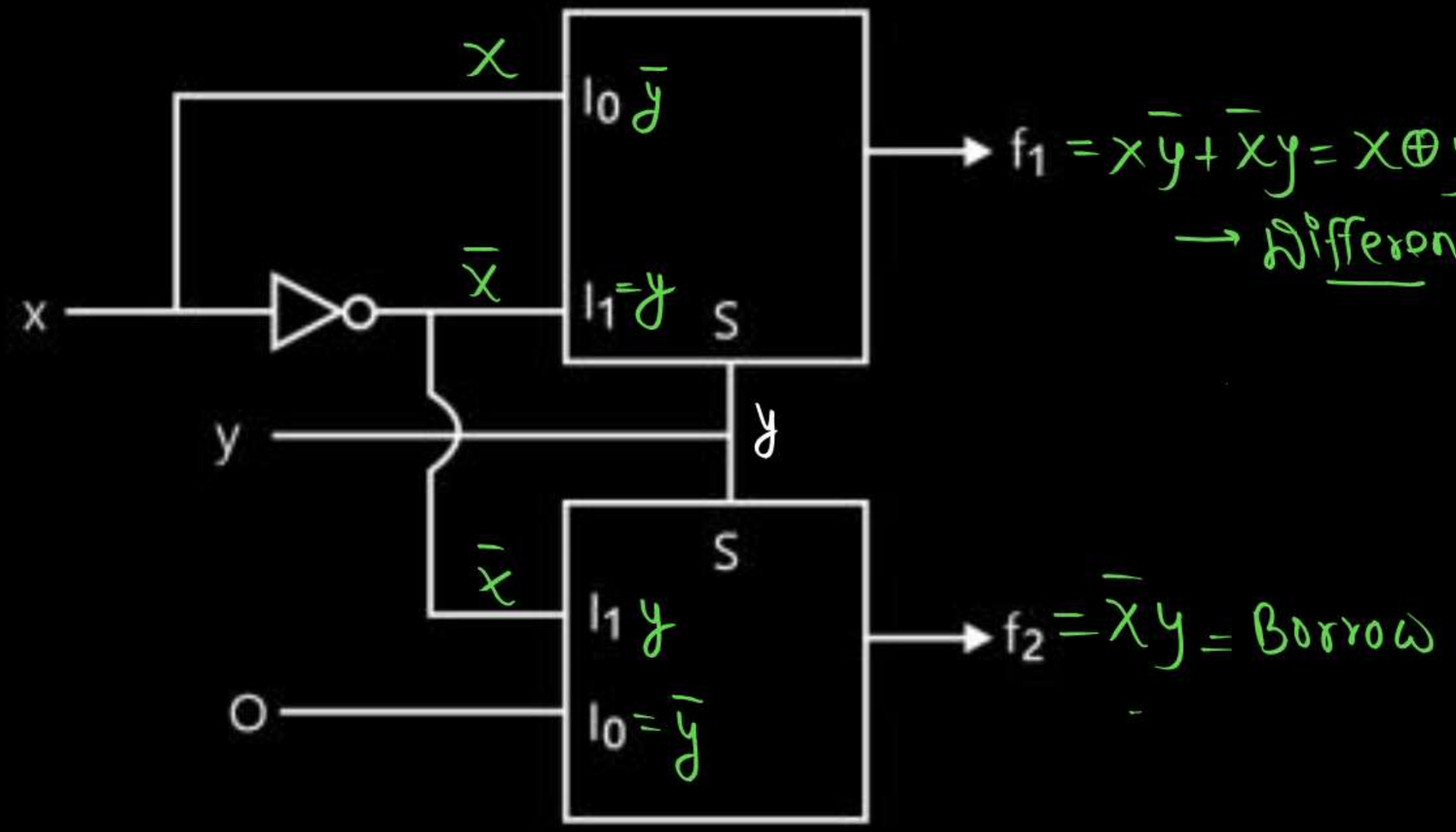
$\Rightarrow (3\times3-3)-3$

$9-3-3$

(3) Ans

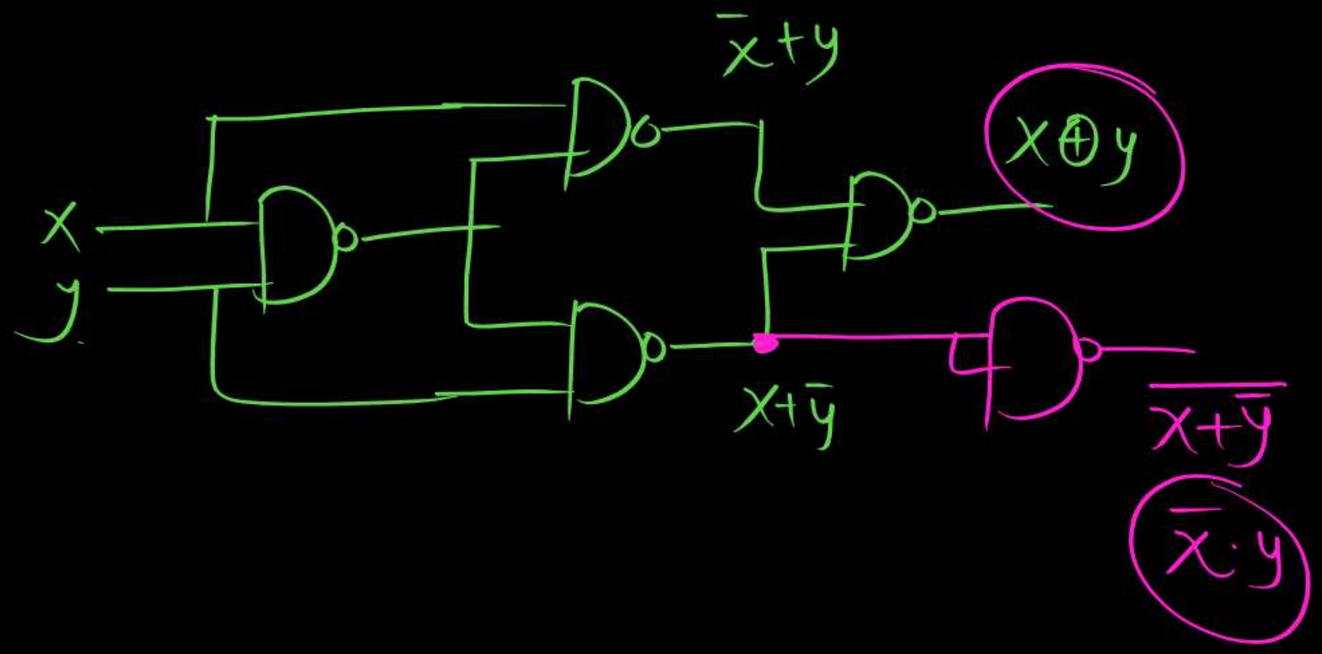
(3)

Q.3 Minimum number of NAND gates required to implement following combinational circuit are_____.



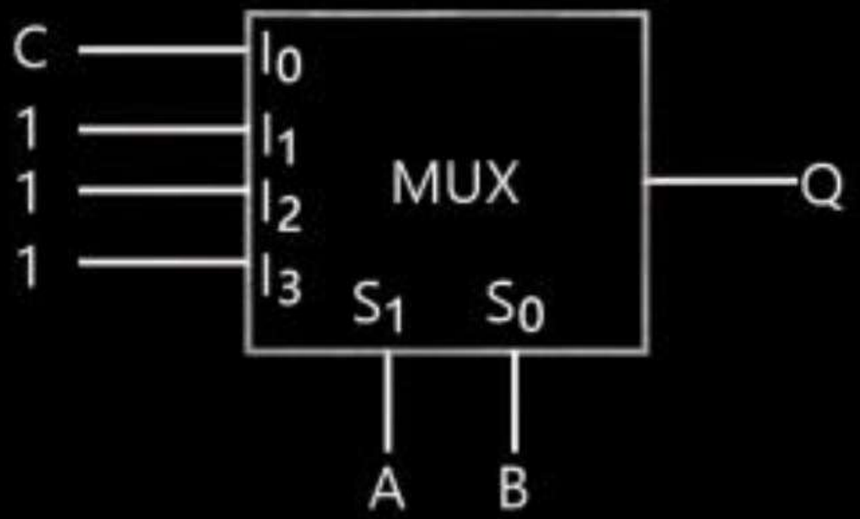
Half subtractor

5


x
y
$\bar{x}+y$
$x \oplus y$
$x+\bar{y}$
$\overline{x+\bar{y}}$
$\bar{x} \cdot y$

Q.4 The combinational logic circuit shown in the given figure has an output Q which is

HW

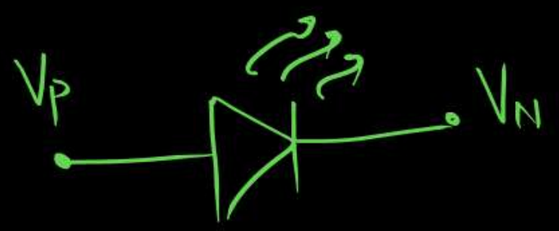


(A) ABC

(B) A + B + C

(C) $A \oplus B \oplus C$

(D) A.B + C

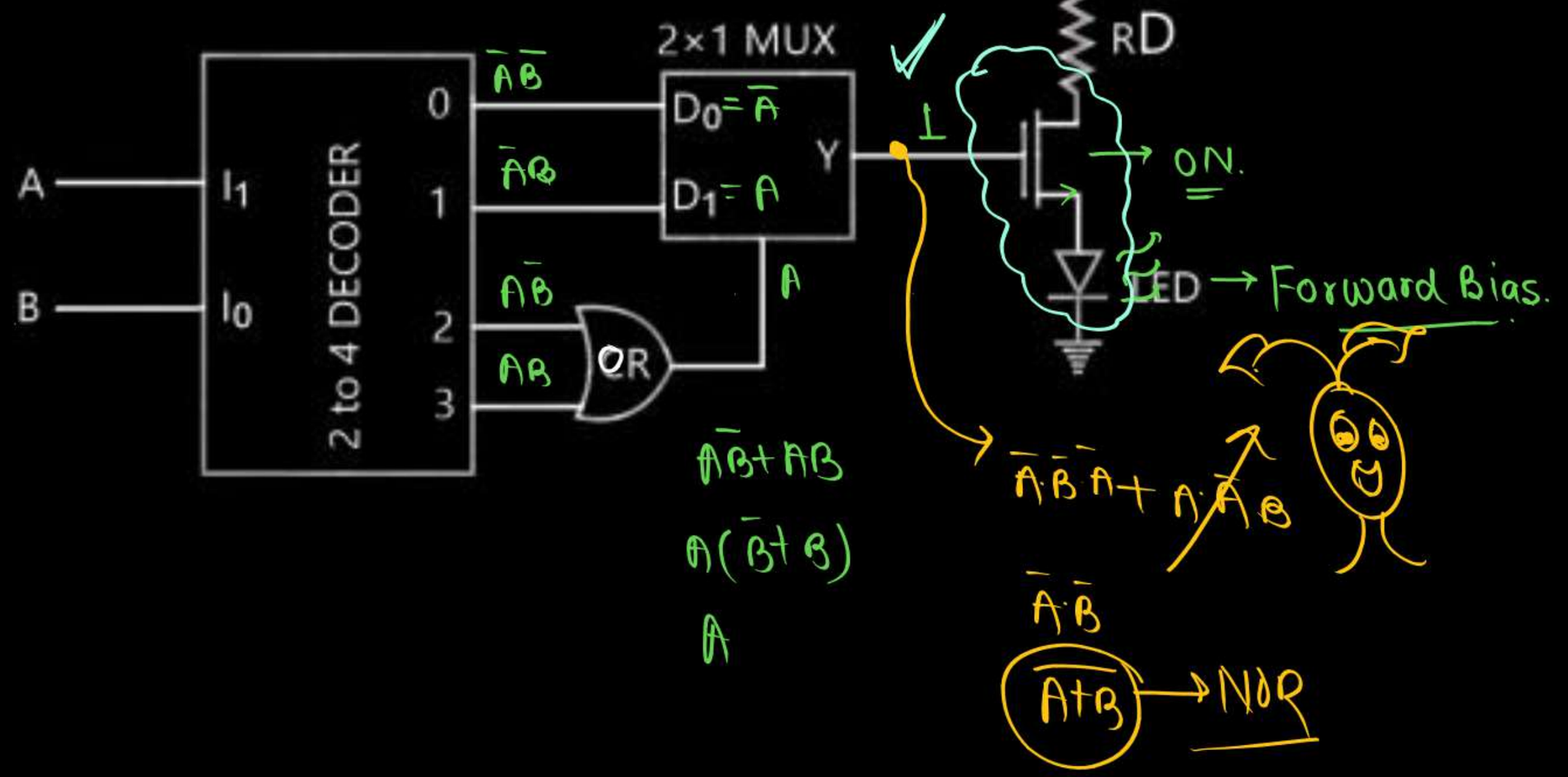


$V_P > V_N \rightarrow FB$

$V_P \leq V_N \rightarrow RB$

Q.5 Consider the combinational circuit given below. For how many combinations of A & B does the LED glow?

A	B	$y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



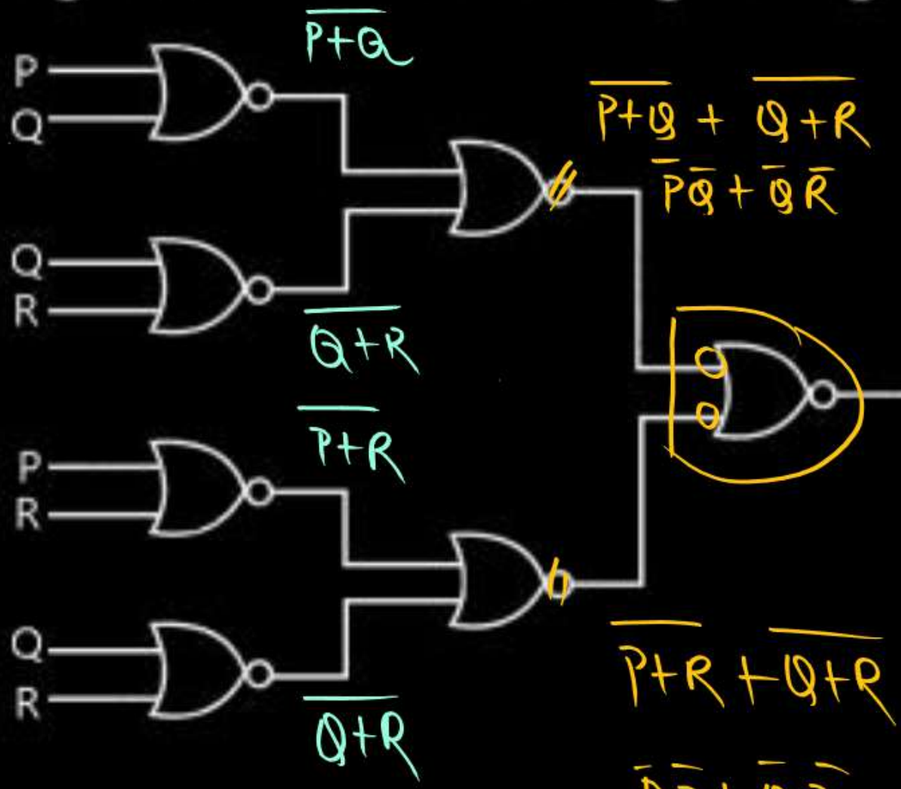
Q.6 What is the Boolean expression for the output f of the combinational logic circuit of NOR gates given below?

(A) $\overline{Q+R}$

(B) $\overline{P+Q}$

(C) $\overline{P+R}$

(D) $\overline{P+Q+R}$



$f=(\bar{P}\bar{Q}+\bar{Q}\bar{R})(\bar{P}\bar{R}+\bar{Q}\bar{R})$

$=\bar{P}\bar{Q}\bar{R}+\bar{P}\bar{Q}\bar{R}+\bar{P}\bar{Q}\bar{R}+\bar{Q}\bar{R}$

$=\bar{Q}\bar{R}(\bar{P}+\bar{P}+\bar{P}+1)$

$=\bar{Q}\bar{R}$

$=\overline{Q+R}$

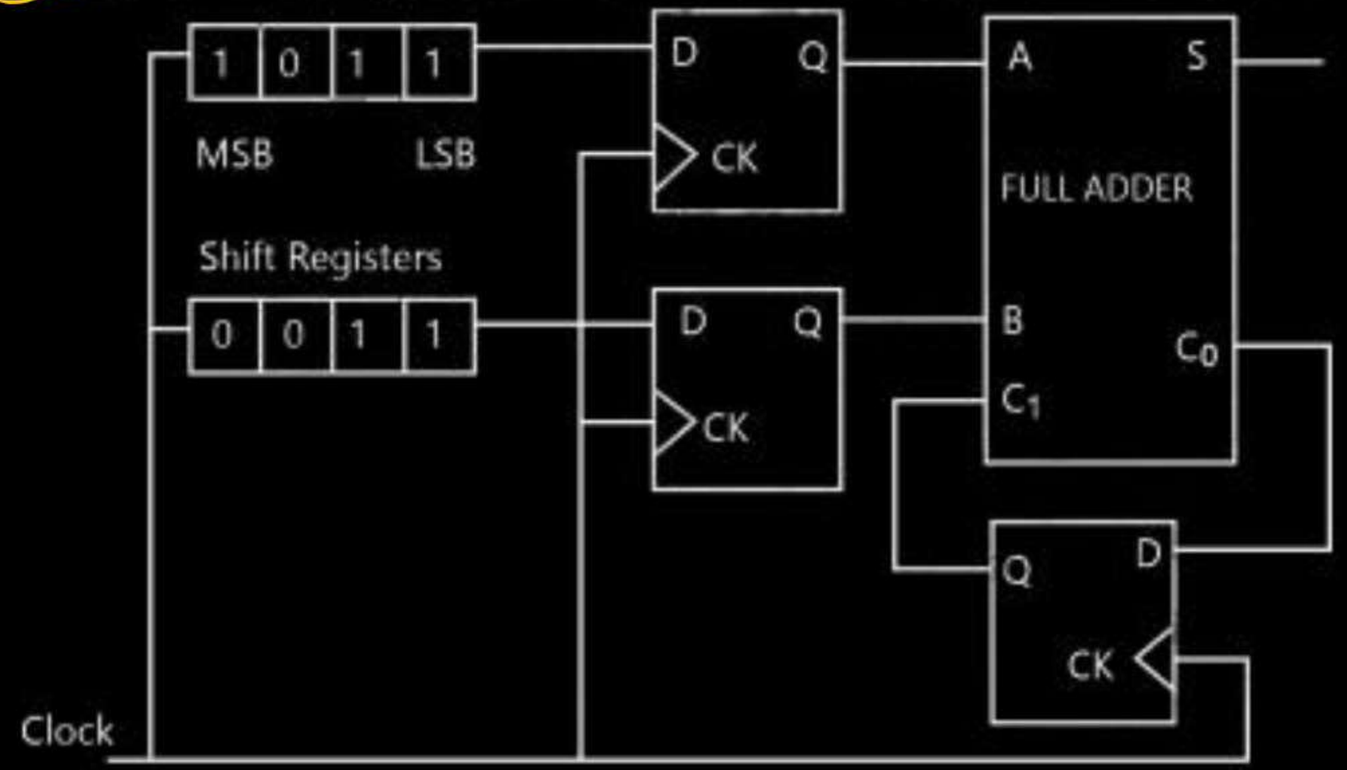
Q.7 For the circuit shown in figure below, two 4-bit parallel-in serial-out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip-flops are in clear state. After applying two clock pulses, the outputs of the full-adder should be

(A) $S = 0, C_0 = 0$

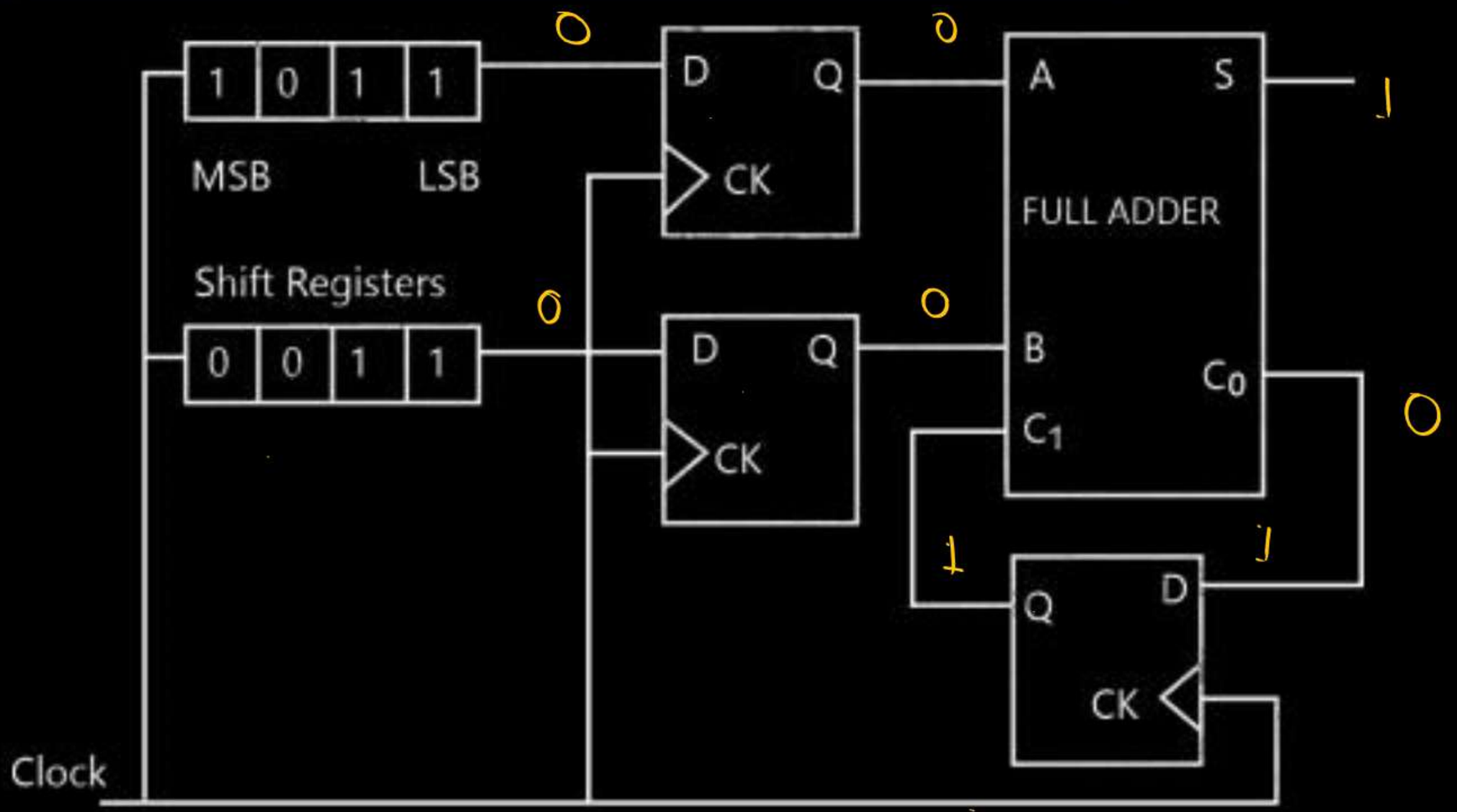
(B) $S = 0, C_0 = 1$

(C) $S = 1, C_0 = 0$

(D) $S = 1, C_0 = 1$



51 Questions of Digital Electronics part-II



CLOCK	S	C_0
1	0	1
2	1	1
3	1	0

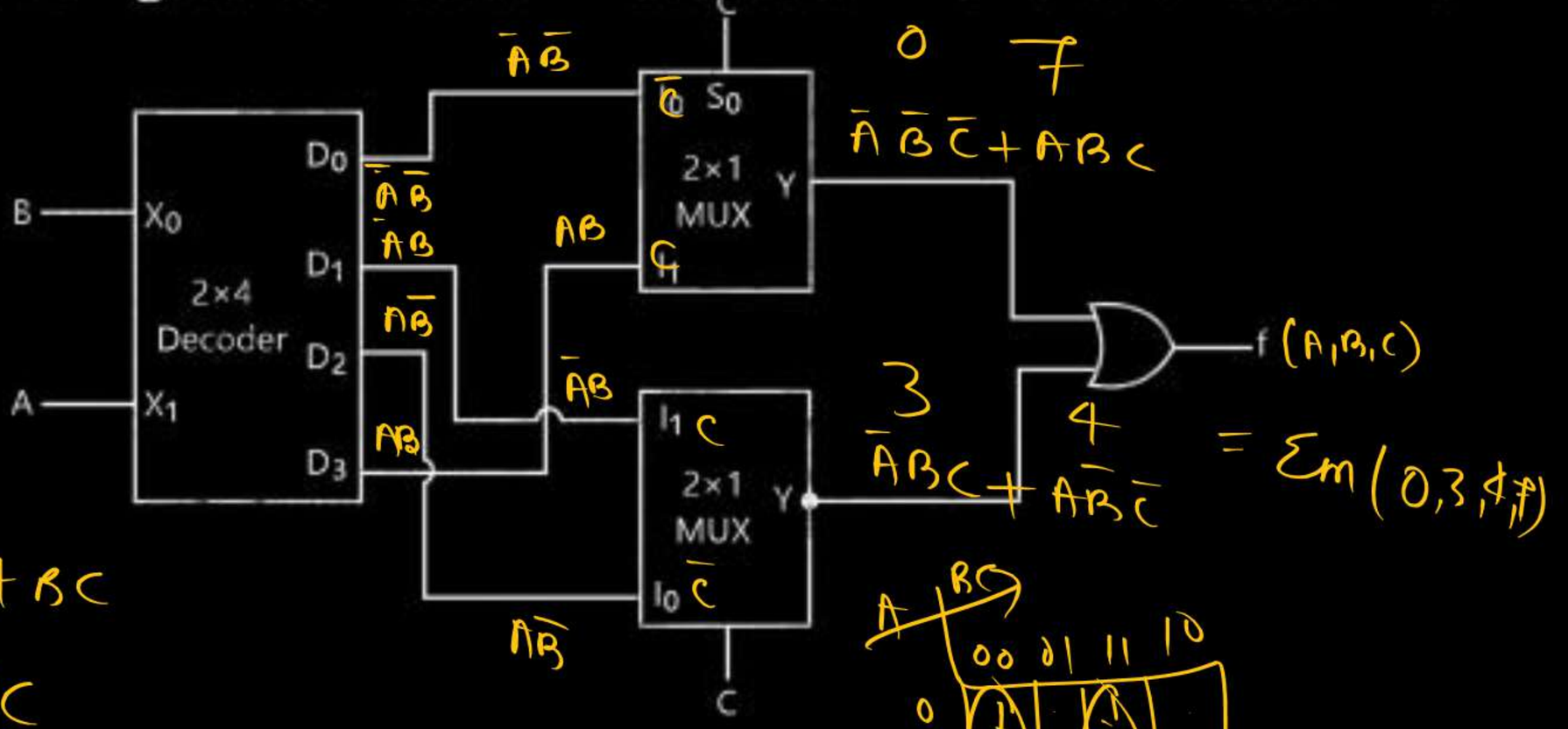
Q.8 A logic function 'f' is implemented by the circuit shown in the figure below. The circuit consists of one 2×4 decoder, two 2×1 multiplexers and a two input or gate connected in cascade. Then the function f is equal to.

(A) $A \oplus B$

(B) $A \oplus B \oplus C$

(C) $B \odot C$

(D) $A \odot B$



$\bar{A}\bar{B}$ $\bar{A}\bar{B}$ $\bar{A}B$ $A\bar{B}$ AB AB $A\bar{B}$

0 $\bar{A}\bar{B}\bar{C}+AB\bar{C}$

7 $\bar{A}\bar{B}C+AB\bar{C}$

3 $\bar{A}BC+A\bar{B}C$

4

$= \Sigma m(0,3,4,7)$

$\bar{B}\bar{C}+BC$

$B \odot C$

51 Questions of Digital Electronics part-II

Q.9 If a Full Adder is taking 20ns to produce carry and 40ns to produce sum. The maximum frequency of 4-bit parallel addition in MHz is 10.

→ addition/second.

$$T = (n-1)T_{carry} + Max\{T_{sum}, T_{carry}\}$$

$$= (4-1)\,20ns + 40ns$$

$$= 60ns + 40ns$$

$$= 100ns$$

$$f = \frac{1}{100 \times 10^{-9}}$$

$$f = \frac{100 \times 10^{6}}{100}$$

$$f = 10\ MHz$$

51 Questions of Digital Electronics part-II

Q.10

HW

A full adder is implemented with two half adders and one OR gate. OR gate is used to derive the final carry function of full adder. In each half adder, Tsum = 25ns and Tcarry = 20ns and TOR = 25ns.

The minimum time required to derive both the sum and carry function of a full adder after applying the inputs is _____ ns

51 Questions of Digital Electronics part-II

Q.11 Consider the following statements for 3 input variables a, b, c. The Boolean function y = ab + bc + ca represents

1. a 3-input majority gate.
2. a 3-input minority gate.
3. carry output of a full adder.
4. product circuit for a, b, and c.

Which of the above statements are correct?

(A) 1 and 3 only

(B) 2 and 3 only

(C) 1 and 3 only

(D) 3 and 4 only

Full adder

Sum = A⊕B⊕C

Carry = $\Sigma m(3,5,6,7)$

= AB+BC+AC

$y = \Sigma m(3,5,6,7)$

A	B	C	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

[illegible] = [illegible]

AB+BC+AC

Q.12 21DA having minimum base conversion to decimal is-

HW

comment

(A) 6079

(B) 10173

(C) 2073

(D) None of these

$(21DA)_{14} = (\quad)_{10}$

Q.13 Let us consider the following equation in a 6-bit binary number system X = A + BA is given A point as $(001010)_2$ in 1's complement binary number system, B is given as $(111010)_2$ in signed number system. What would be X in 2's complement number system?

HW

(A) $(110000)_2$

(B) $(010000)_2$

(C) $(101011)_2$

(D) $(110101)_2$

Q.14 In 2's complement number system, the range of values for 16-bit numbers is given as

(A) –32768 to +32768

(B) –32767 to +32767

(C) –32767 to +32768

(D) –32768 to +32767

51 Questions of Digital Electronics part-II

Q.15 –24 in 2's complement form is

A 11101000

B 01001000

C 01111111

D 00111111

51 Questions of Digital Electronics part-II

Q.16 $(1217)_8$ is equivalent to

A $(1217)_{16}$

B $(028F)_{16}$

C $(2297)_{10}$

D $(0B17)_{16}$

Q.17 73_x (in base – x number system) is equal to 54_y (in base – y number system), the possible values of x and y are

A. 8, 16

B. 10, 12

C. 9, 13

D. 8, 11

Q.18 The 2's complement representation of -17

A 01110

B 101111

C 11110

D 10001


THANK
YOU!