EC/EE/CS & IT/IN

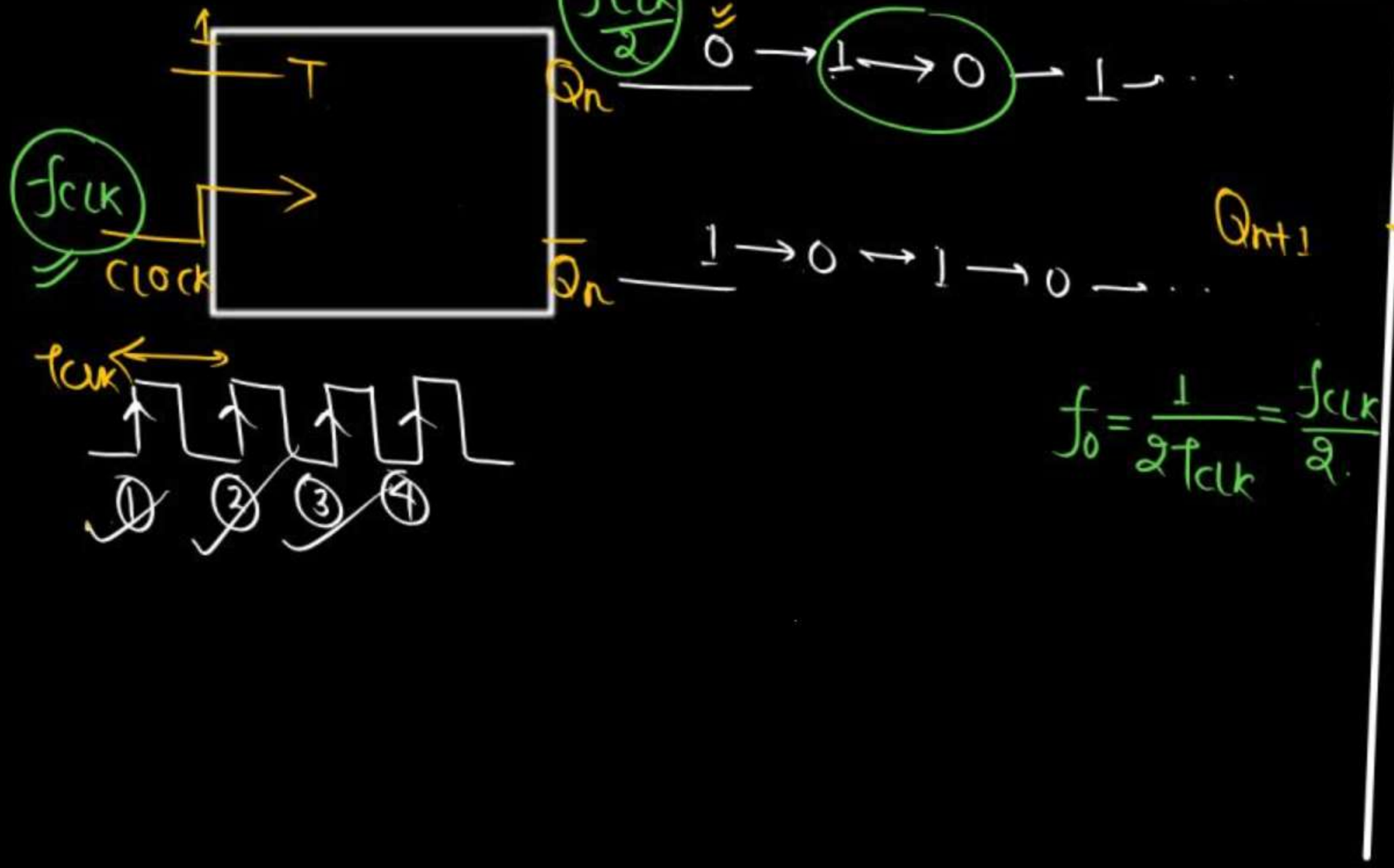
Digital Electronics

Asynchronous Counter

LECTURE NO. 10

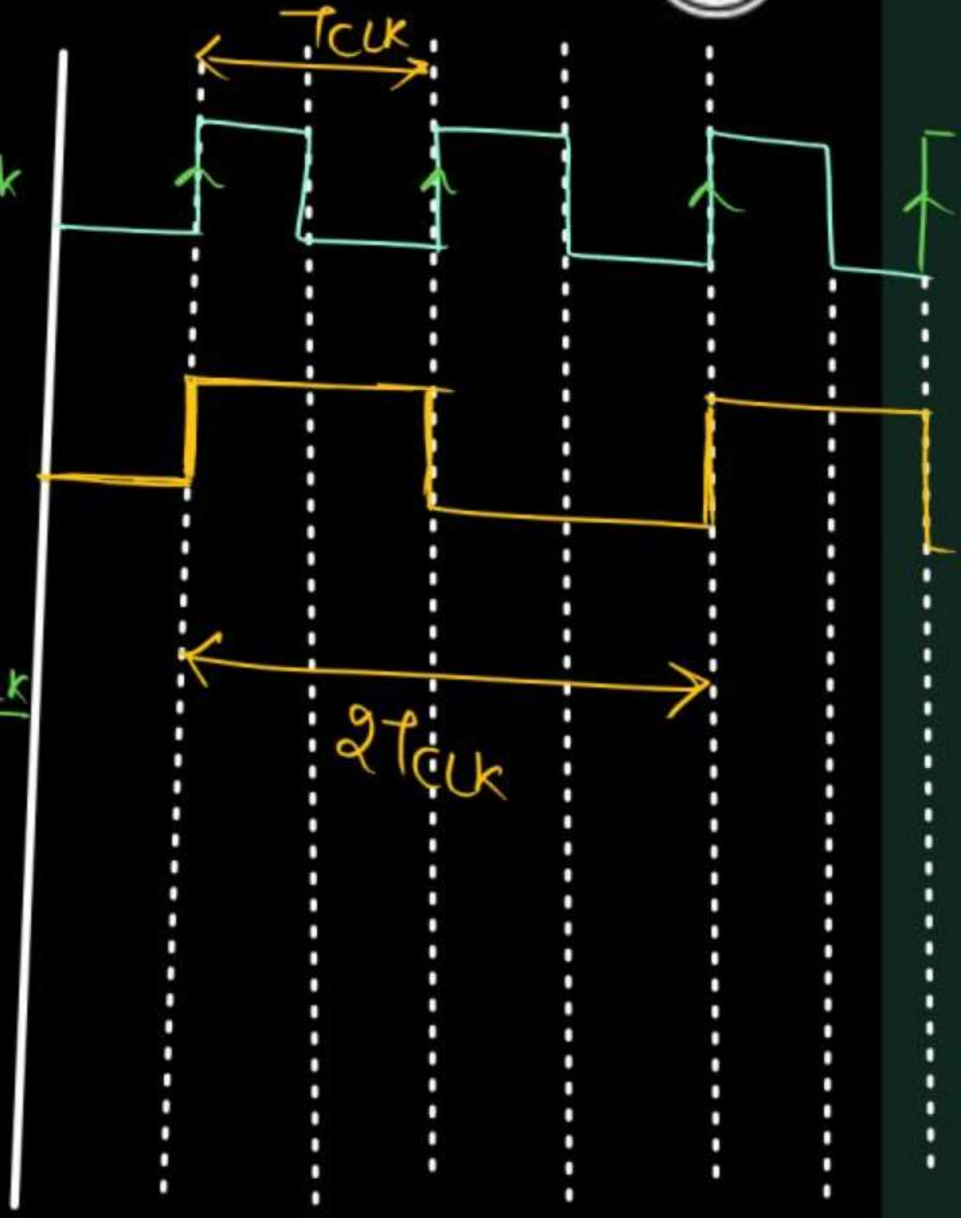
Chandan Jha Sir (CJ Sir)

TOGGLE MODE OF THE FLIP FLOP

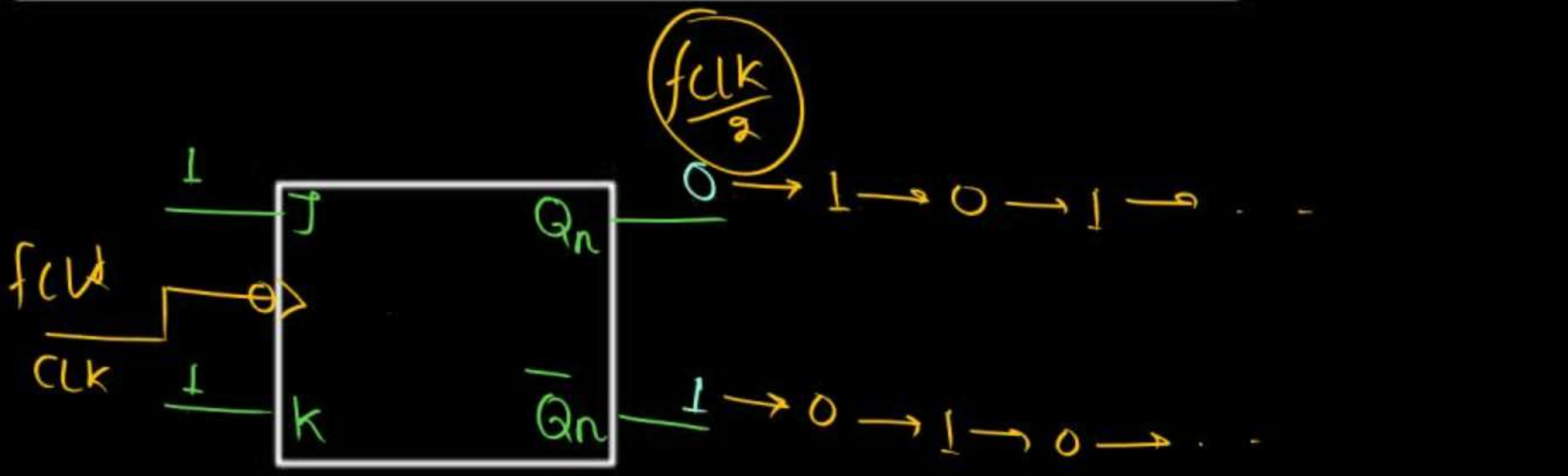


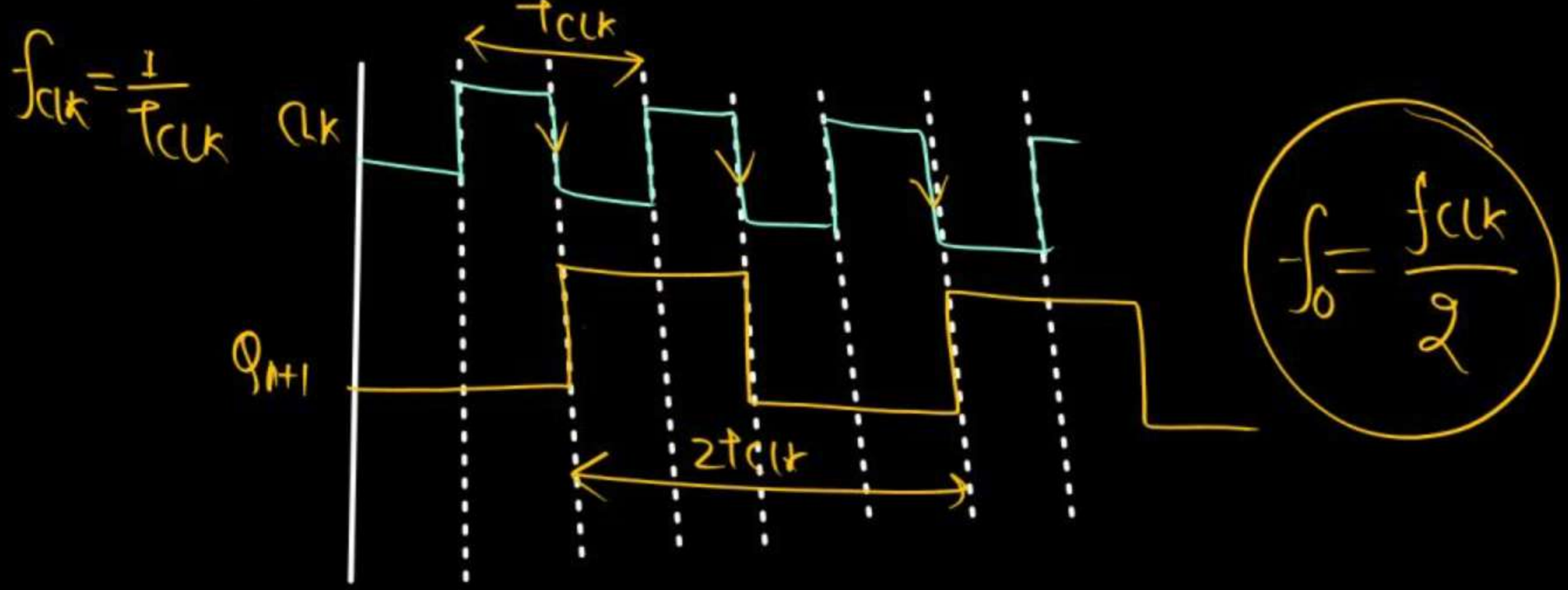
$$f_{clk} = \frac{1}{T_{clk}\,Clock}$$

$$f_0 = \frac{1}{2T_{clk}} = \frac{f_{clk}}{2}$$

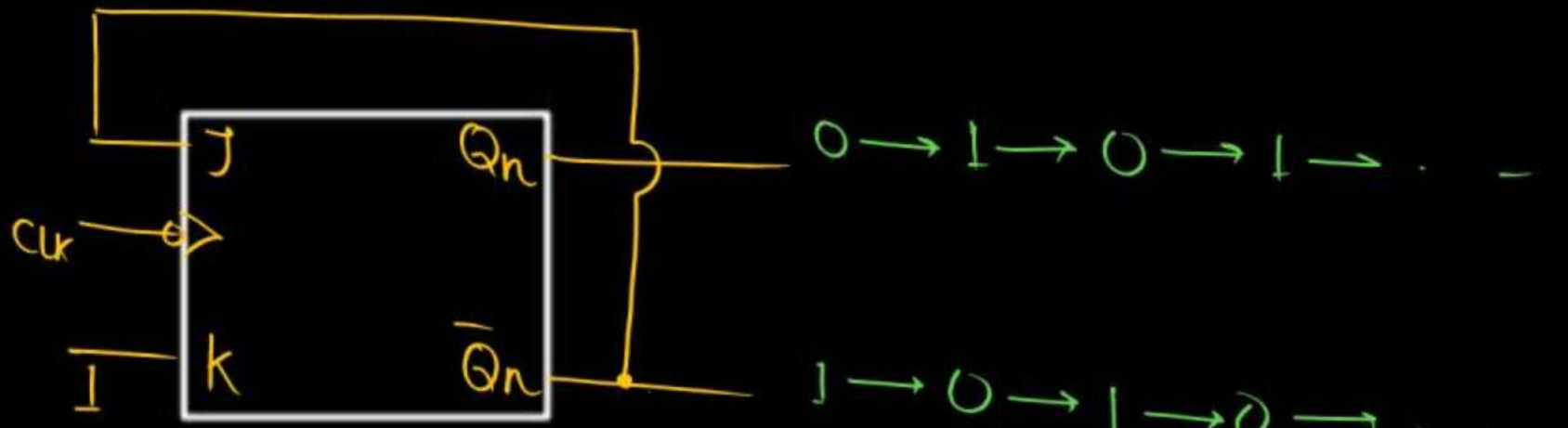


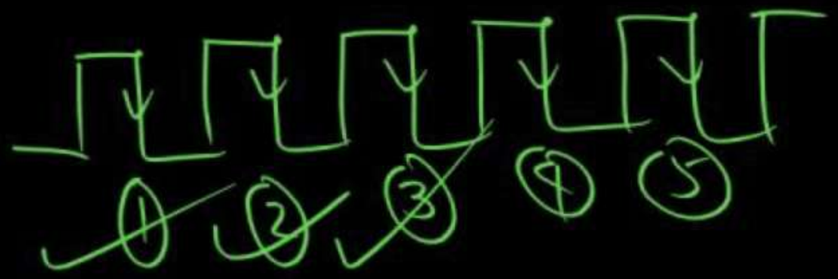
TOGGLE MODE OF THE FLIP FLOP



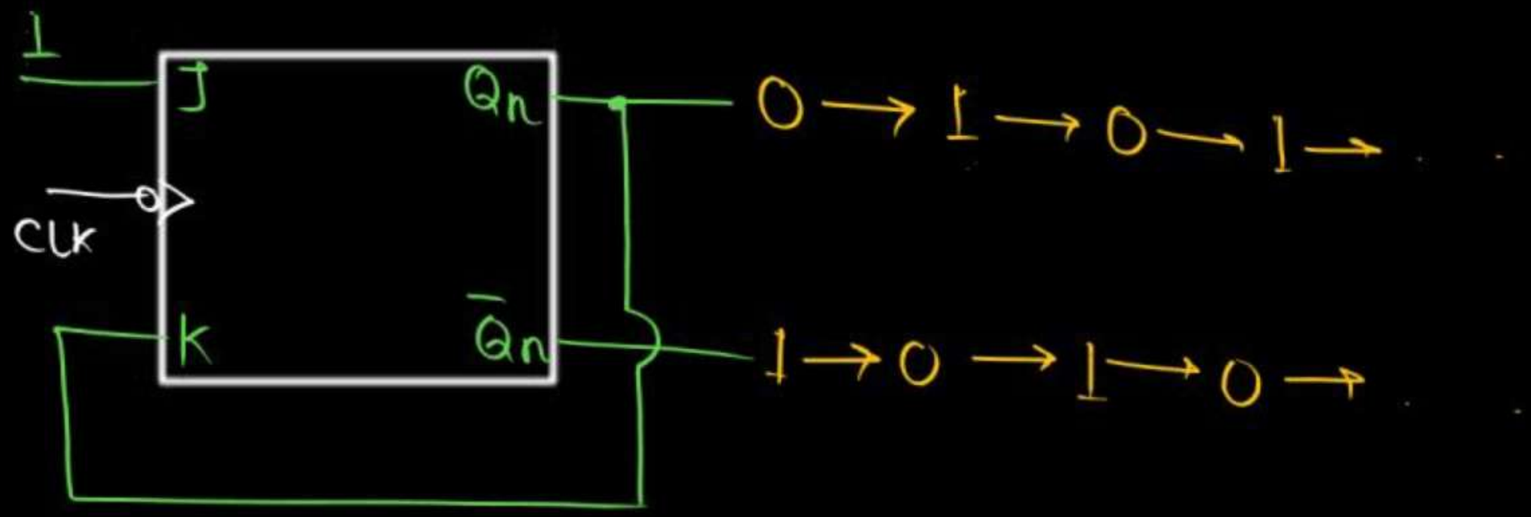


TOGGLE MODE OF THE FLIP FLOP

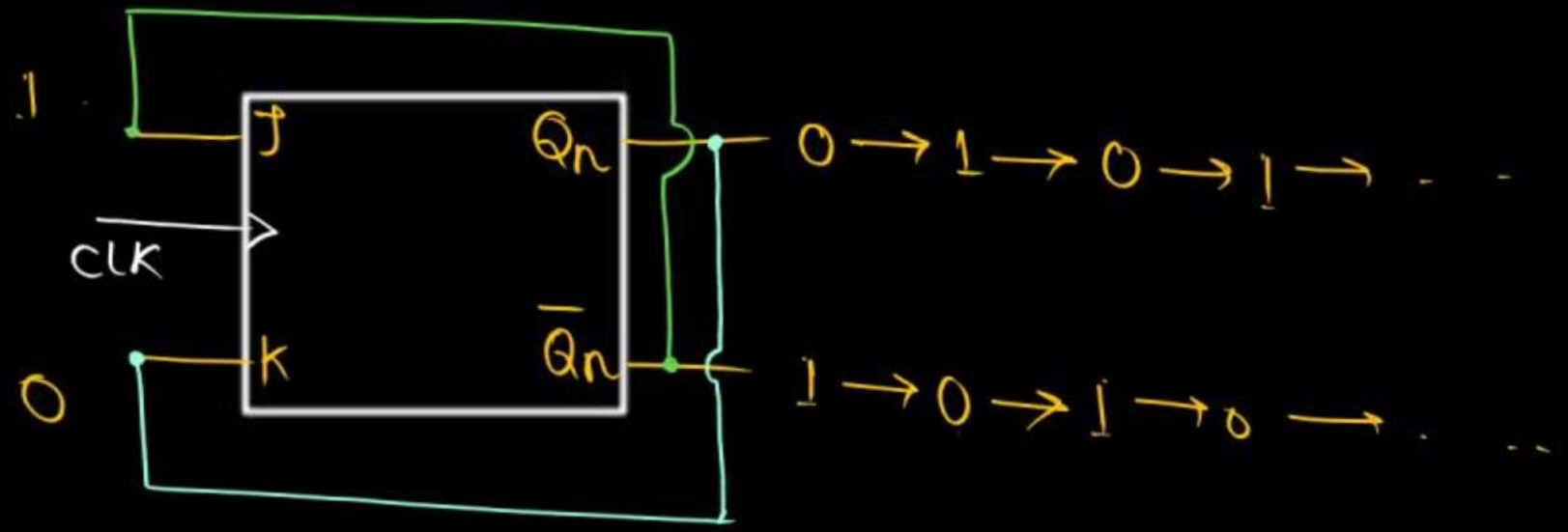




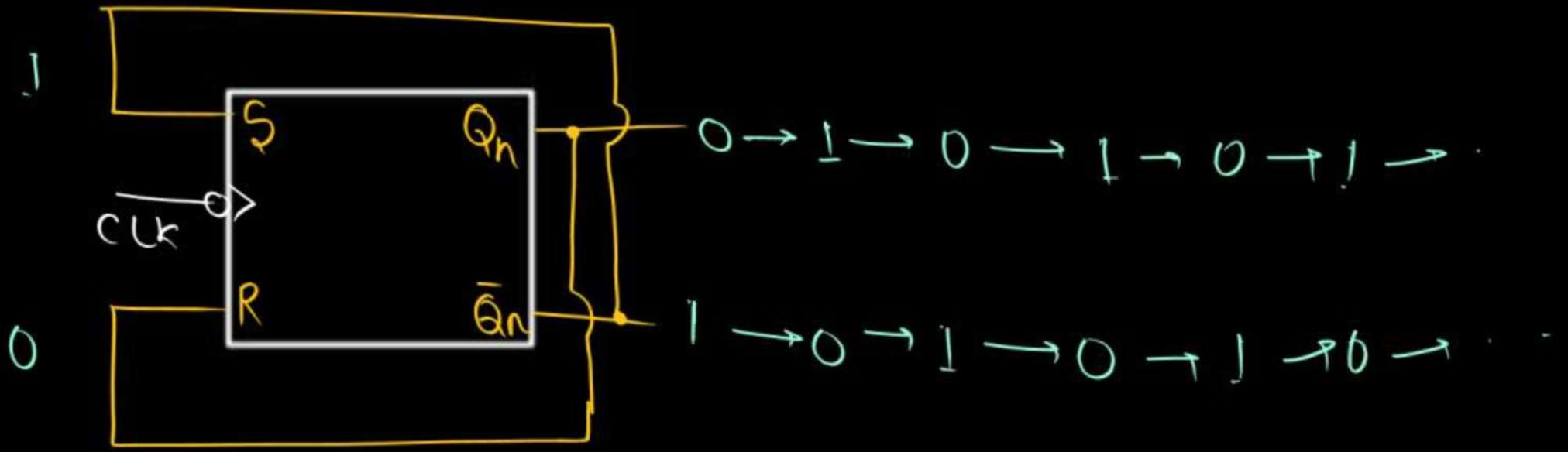
TOGGLE MODE OF THE FLIP FLOP



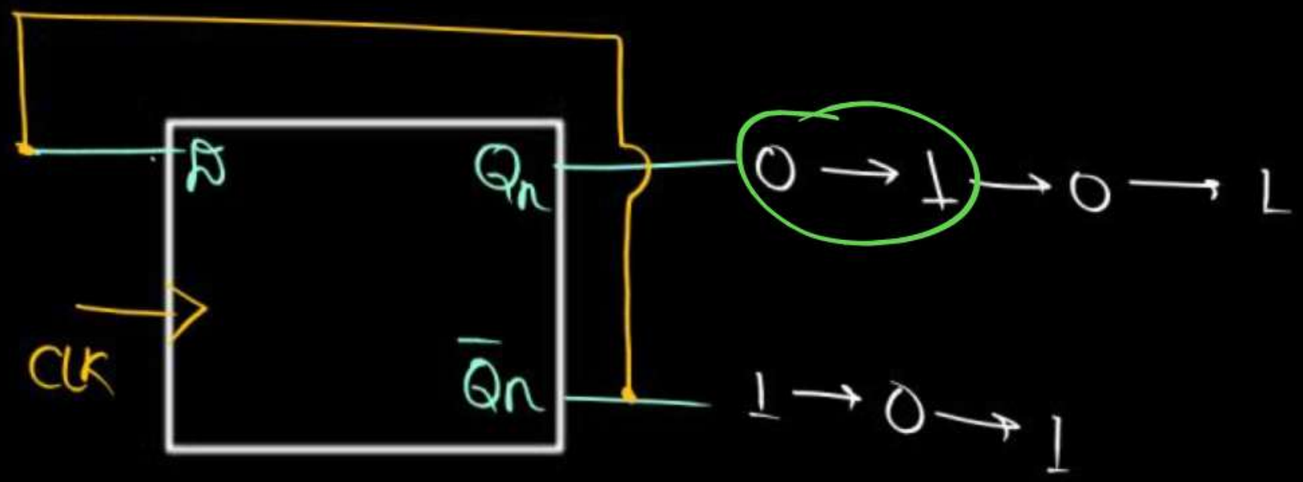
TOGGLE MODE OF THE FLIP FLOP



TOGGLE MODE OF THE FLIP FLOP



TOGGLE MODE OF THE FLIP FLOP



Counters

1. Counter are used to count number of clock.
2. Counters are also known as frequency divider circuit.

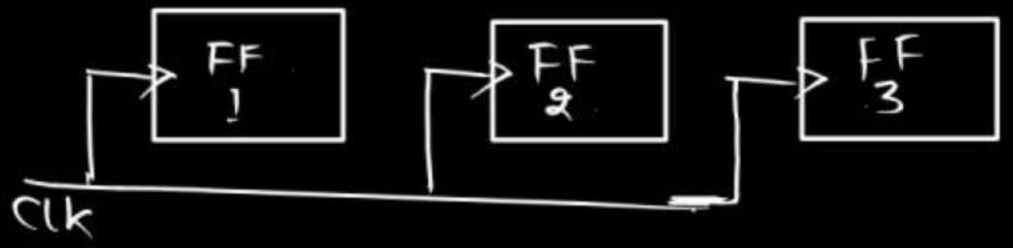
① Synchronous counter

② Asynchronous counter

UP	DOWN	RANDOM
1	5	1
2	4	3
3	3	2
4	2	5
5	1	4

Synchronous Counters

1. All the flip flops are connected with same clock.



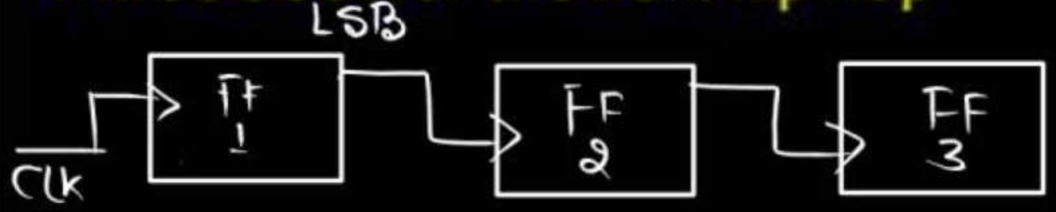
② fast

③ All type of counting are possibble.

④ Ex. Ring, Johnson counter

Asynchronous Counters

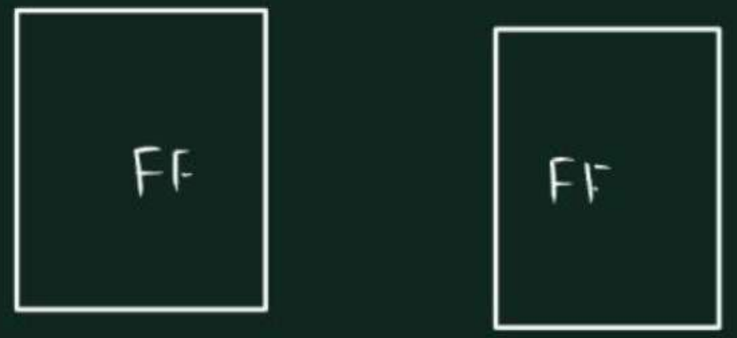
1. Only one Flip Flop having External clock and the outputs of that flip flop will be clock for the next flip flop



② Slow

③ Generally UP & DOWN counting are possible.

④ Ex. Ripple counter



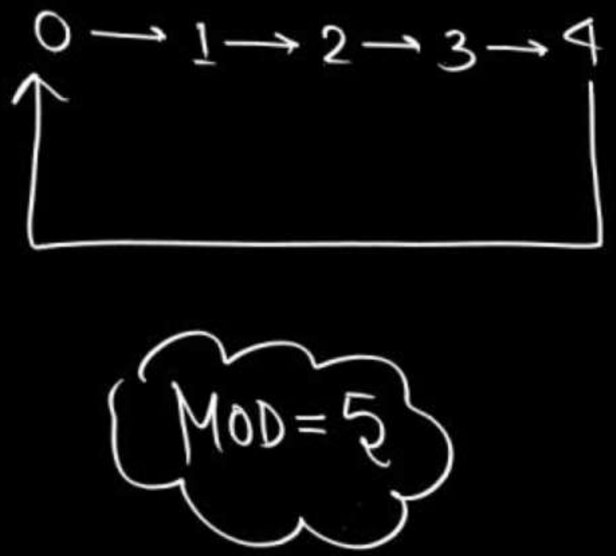
$$\left\{\begin{matrix} 0 & 0 \\ 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{matrix}\right\}$$

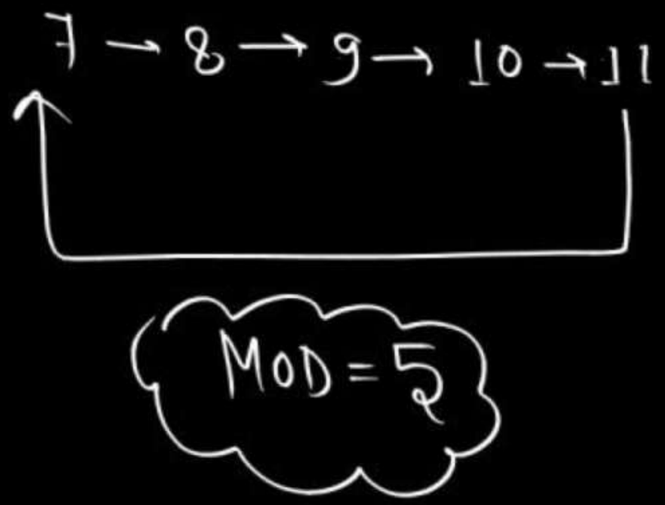
Maximum number of states $= 2^n$

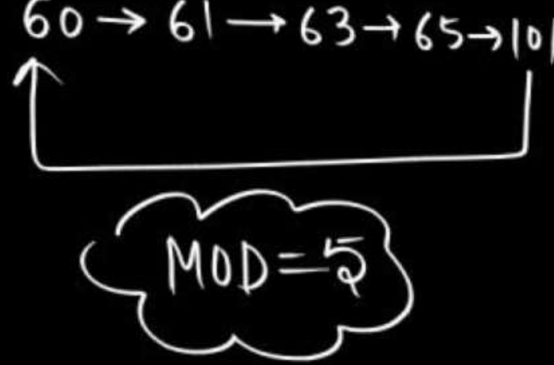
$n \rightarrow$ Number of FF

MOD

Number of states used by the counter.







$$\text{MOD}(M) \leq 2^n$$

$$M \leq 2^n$$

$$n \geq \log_2 M$$

J

Q MOD-10 counter.

no. of FF ?

$M \leq 2^n$

$n \geq \log_2 M$

$n \geq \log_2 10$

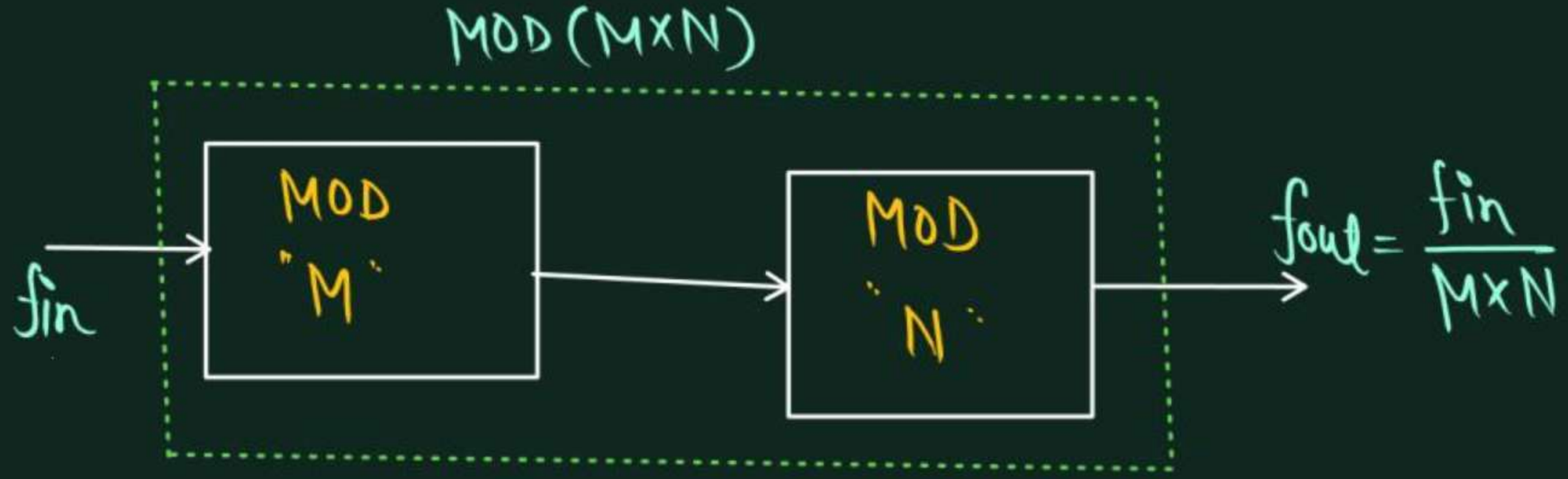
$n \geq 3.\text{something}$

$n \approx 4$

₹.10
NOTE

1.

2.



BCD

↳ Binary coded decimal

↳ Every decimal number are represented by 4 bit

BCD

100
101
102
103
104
105
106
107
108
109

XNOD-1D

0 → 0000
1 → 0001
2 → 0010
3 → 0011
4 → 0100
5 → 0101
6 → 0110
7 → 0111
8 → 1000
9 → 1001

BCD

Q When MOD '5' counter is cascaded by MOD '2' counter Then it will become.

(A) MOD-10 counter

(B) BCD counter

(C) Both (A) & B

(D) MOD '7' counter

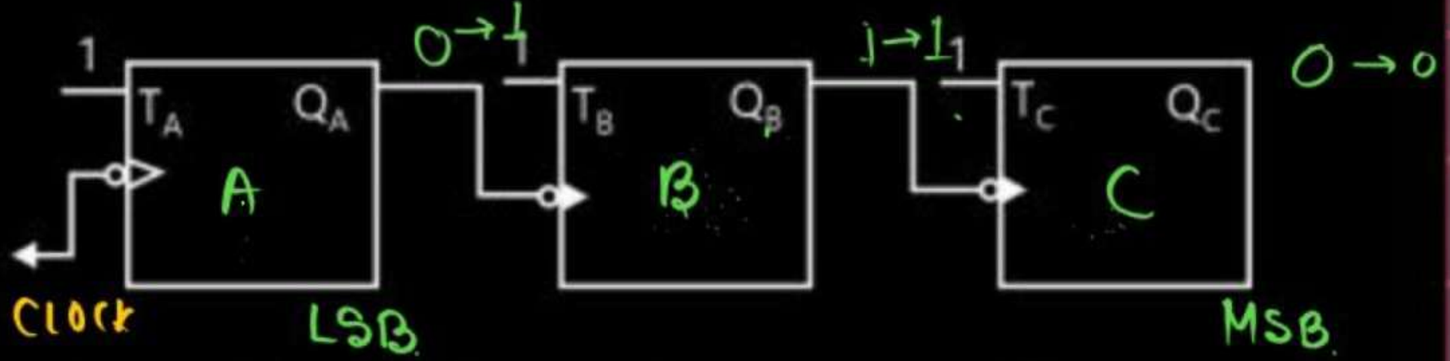
(E) Sir, Mujhe ata to hai par mai batunga nahi.

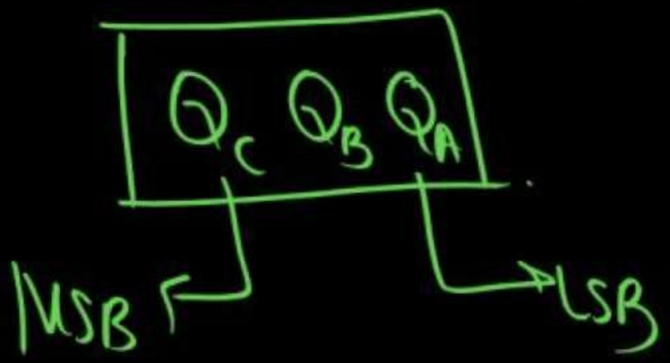
$5 \times 2 = 10$

MOD

Asynchronous Counter

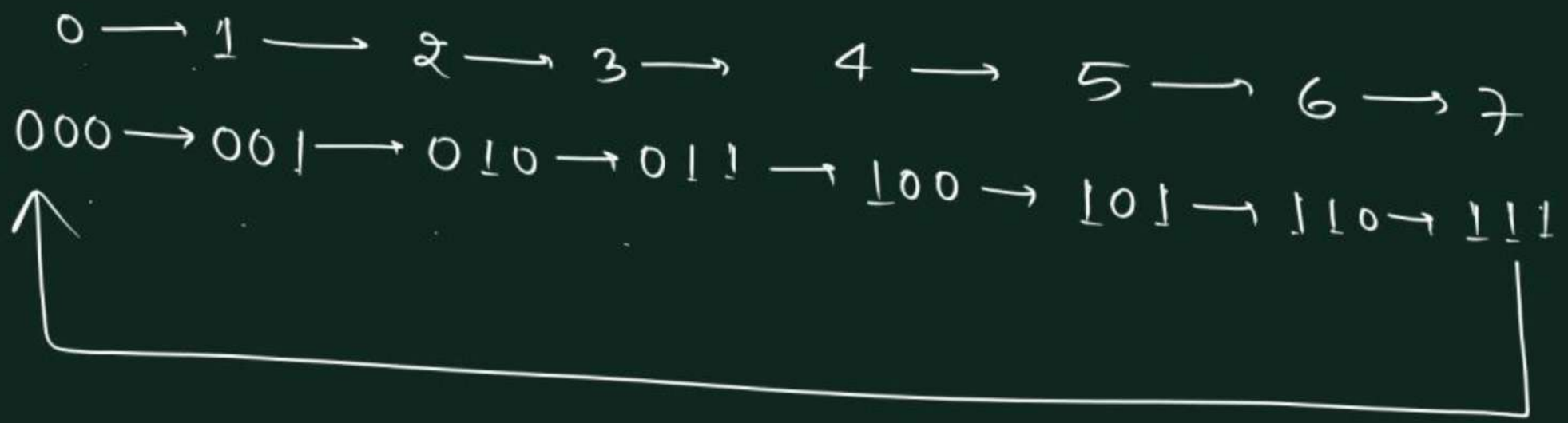
3 bit Ripple counter





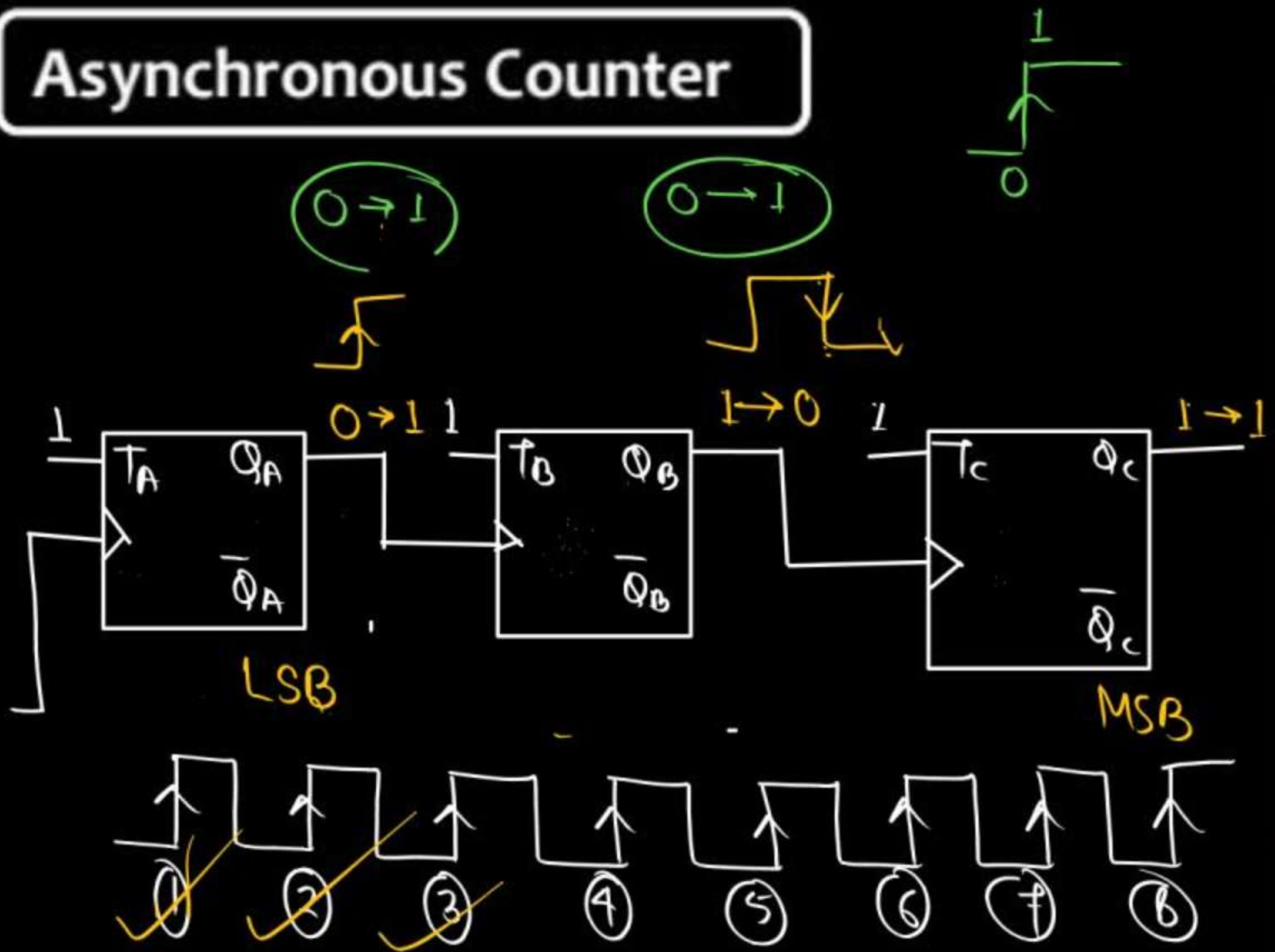
clock	Q_C	Q_B	Q_A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

Ext. clk



MOD "8" UP RIPPLE COUNTER

Asynchronous Counter



clock	Q_C	Q_B	Q_A
0	0	0	0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	1	0

000 → 111 → 110 → 101 → 100 → 011 → 010 → 001 → 00

MOD 8 DOWN RIPPLE COUNTER

Asynchronous Counter

Bubble

- 0 → −ve.
- $\overline{Q}$ → +ve

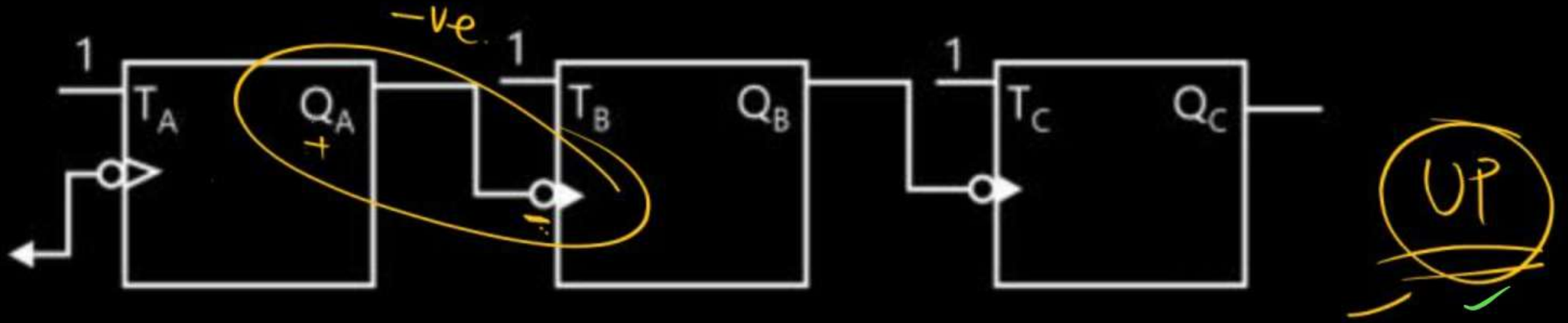
−ve → UP
+ve → DOWN

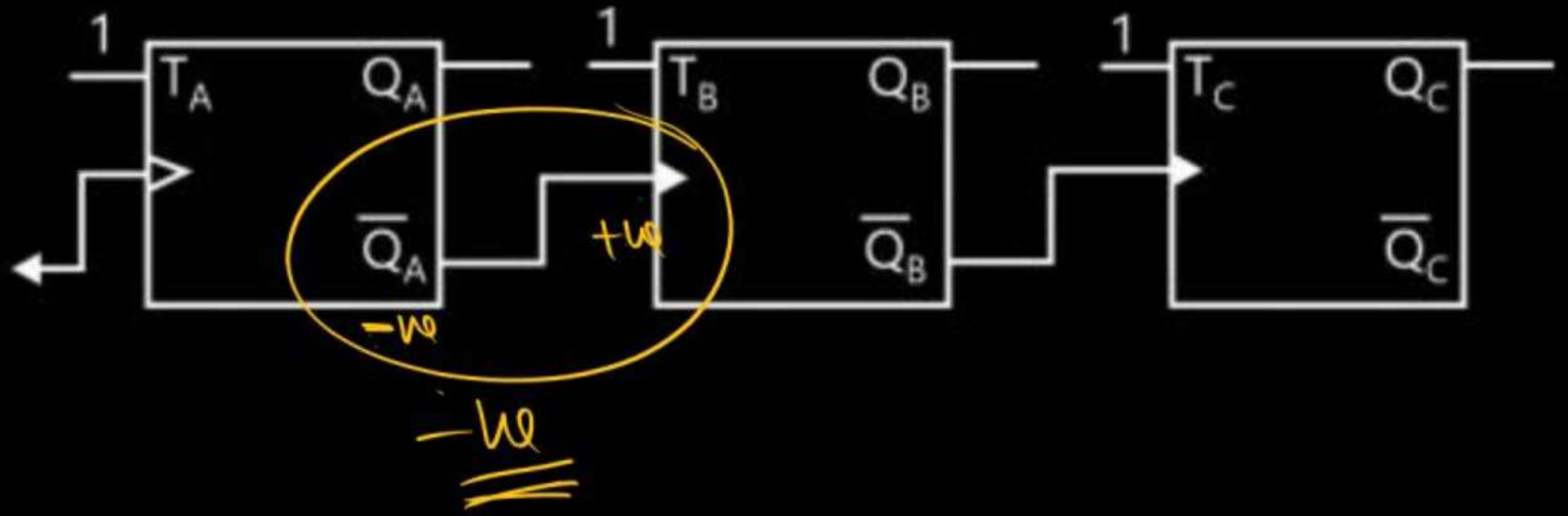
clock	Q_C	Q_B	Q_C
0			
1			
2			
3			
4			
5			
6			
7			
8			

Asynchronous Counter

-ve → UP

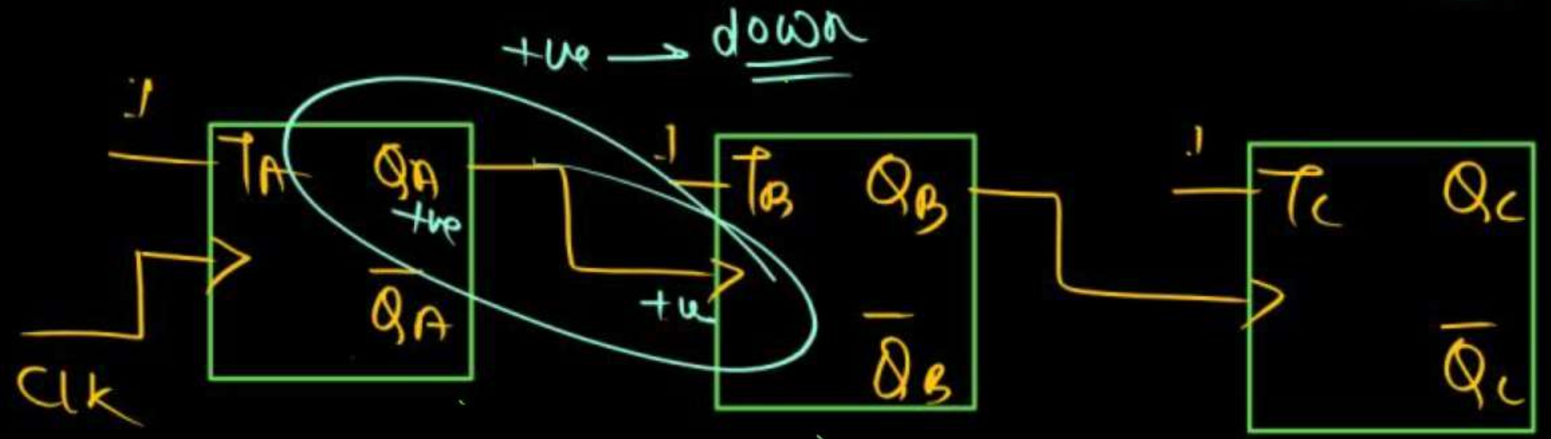
+ve → DOWN



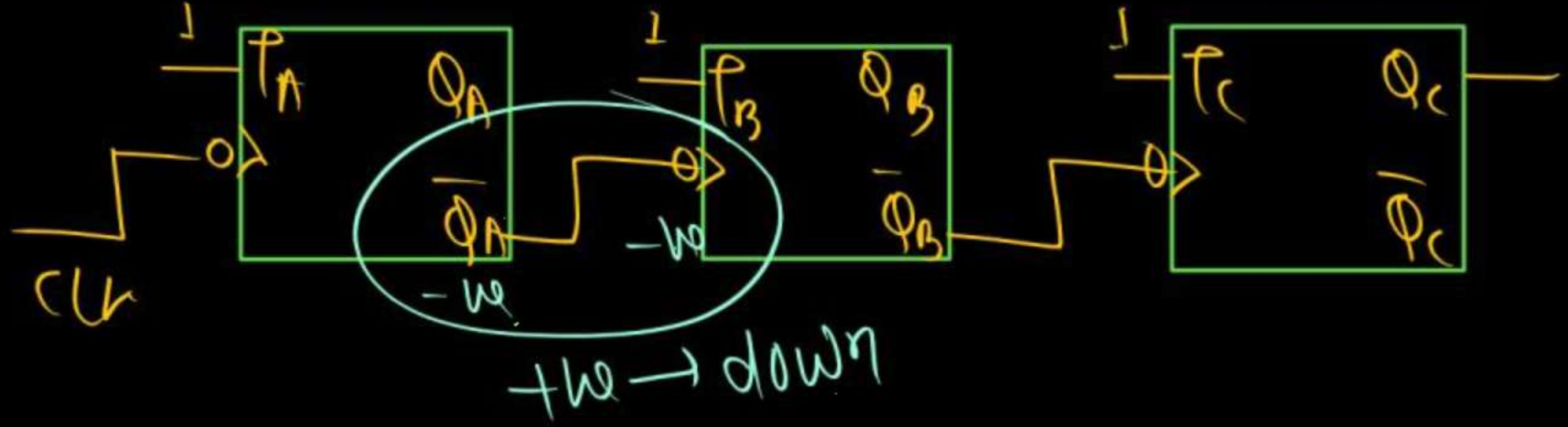


Asynchronous Counter

$n \rightarrow 2^n$



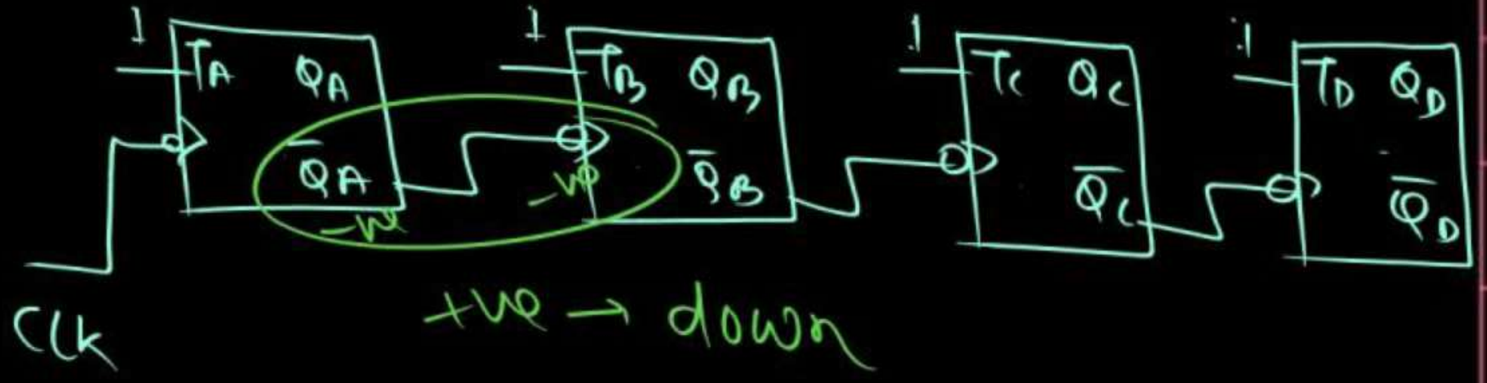
DOWN



Down counter

Asynchronous Counter

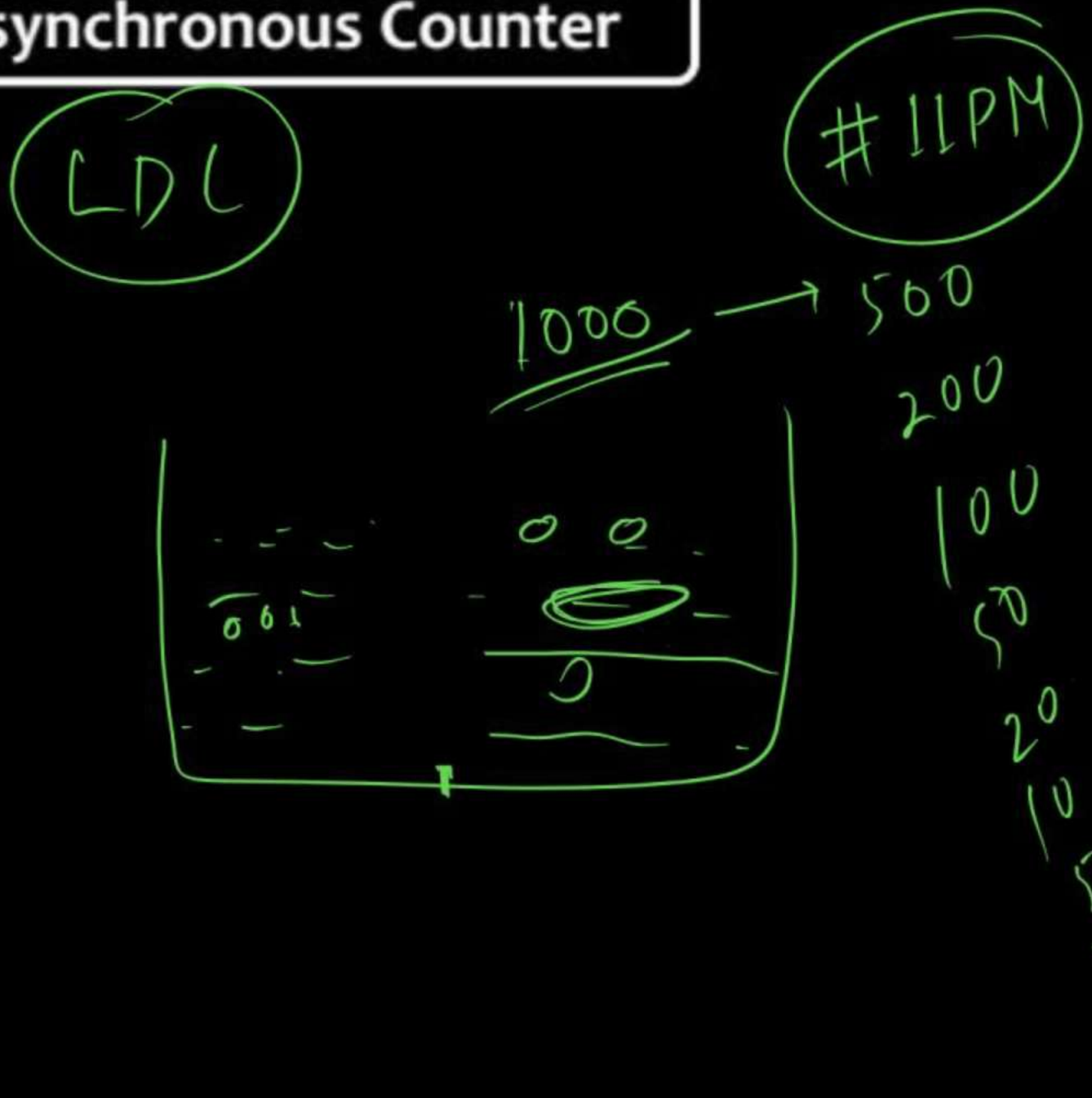
MOD = 2^4 = 16



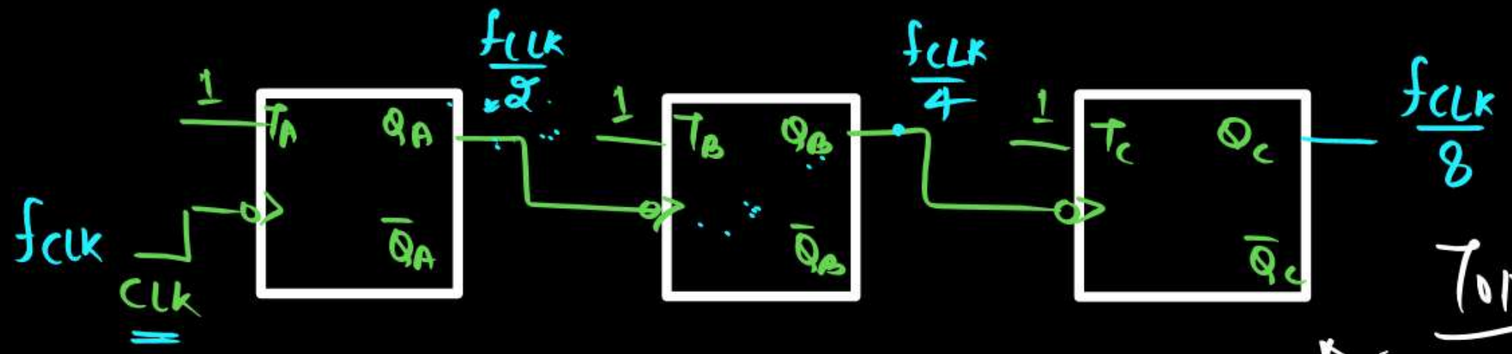
MOD 16 down Ripple counter

clock	Q_C	Q_B	Q_C	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				

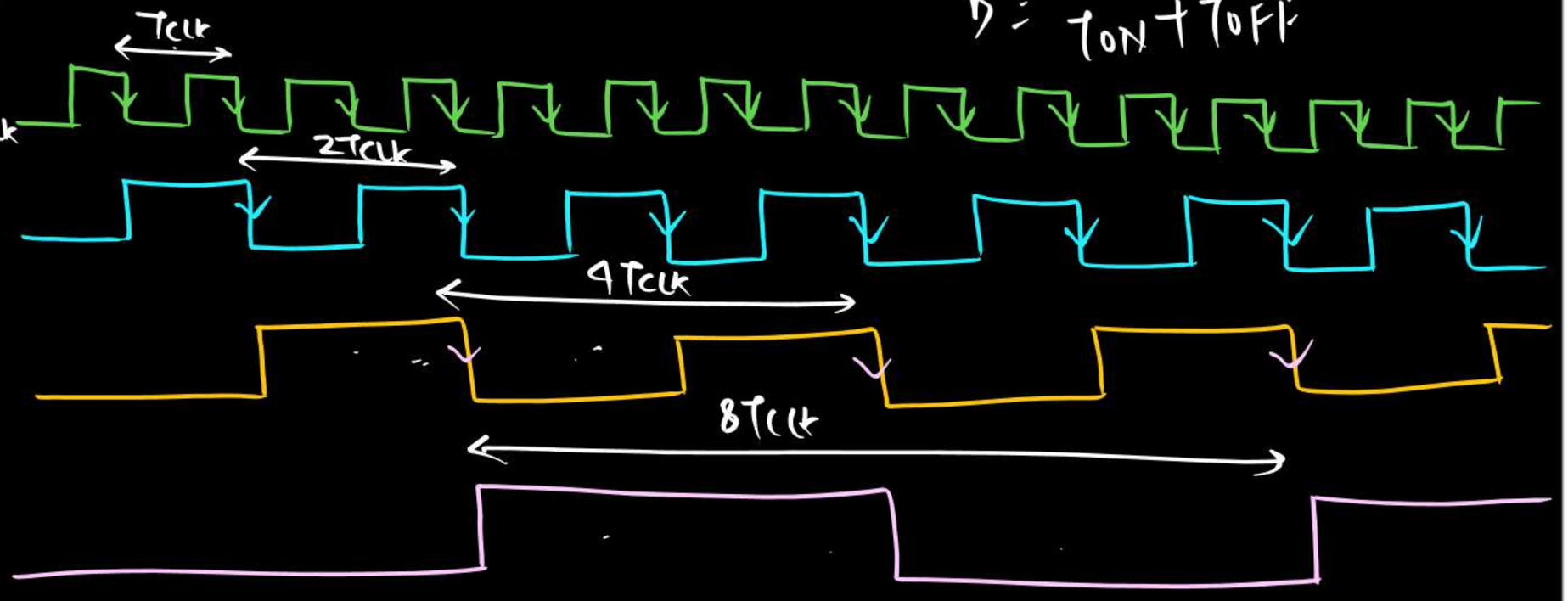
Asynchronous Counter



clock	Q_C	Q_B	Q_C	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				



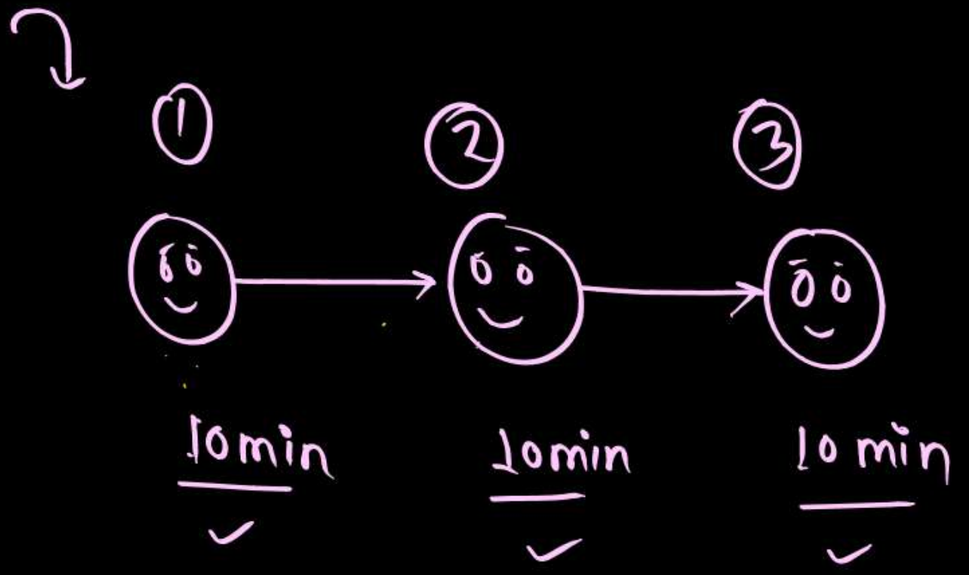
$$\eta = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

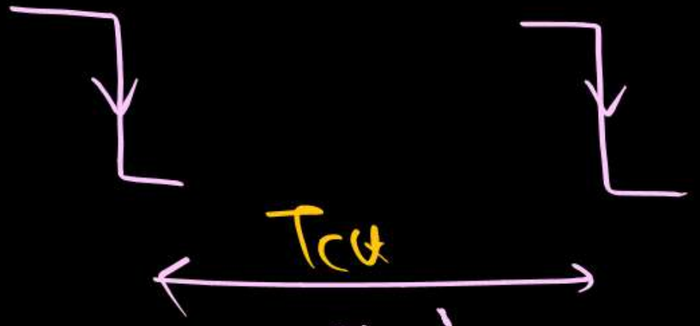


$$f_{Q_A} = \frac{1}{2T_{CLK}} = \frac{f_{CLK}}{2} \quad Q_A$$

$$f_{Q_B} = \frac{1}{4T_{CLK}} = \frac{f_{CLK}}{4} \quad Q_B$$

$$f_{Q_C} = \frac{1}{8T_{CLK}} = \frac{f_{CLK}}{8} \quad Q_C$$



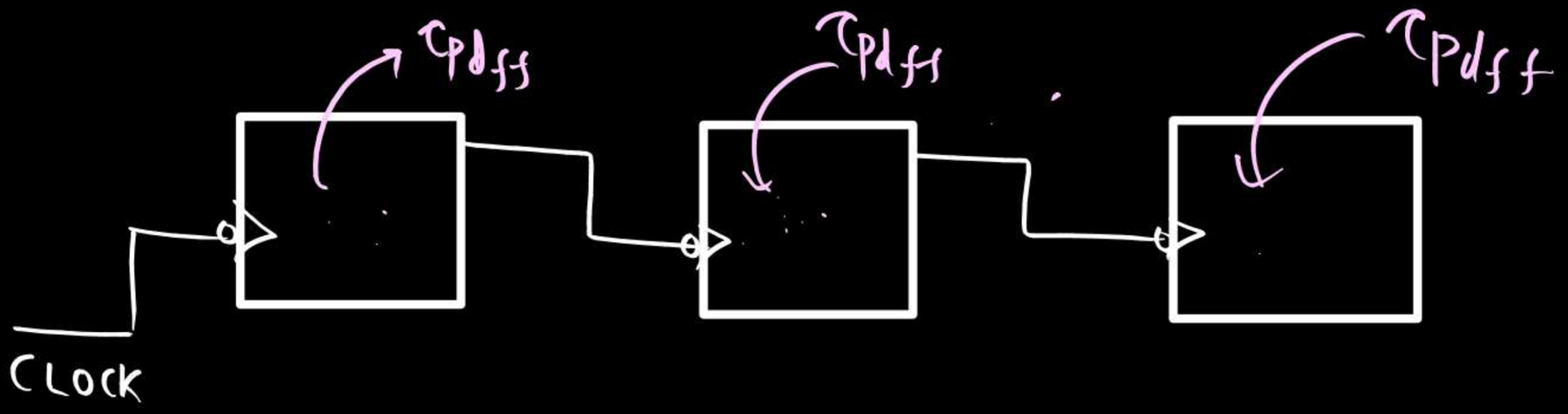


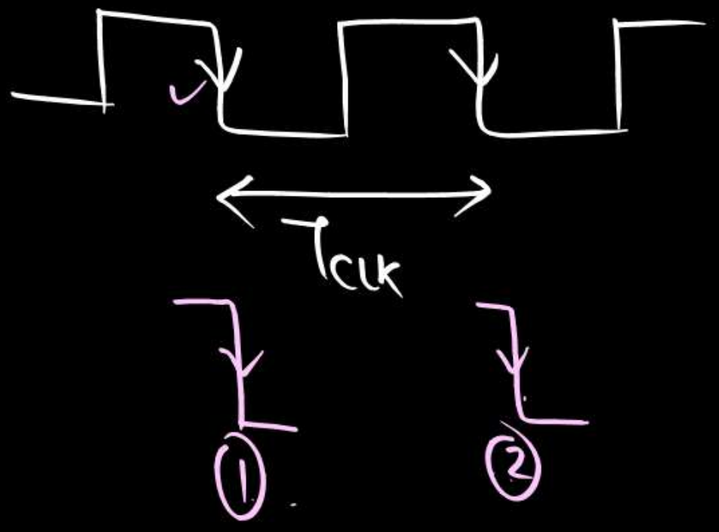
T_{cu}

30 min

3 × 10 min

$n \times T_{pd}$





$$T_{clk} \geq 3\tau_{pd_{ff}}$$

"n" FF

$$T_{clk} \geq n \cdot \tau_{pd_{ff}}$$

$$\frac{1}{T_{clk}} \leq \frac{1}{n \cdot \tau_{pd_{ff}}}$$

$$f_{clk} \leq \frac{1}{n \cdot \tau_{pd_{ff}}}$$

$$(f_{clk})_{max} = \frac{1}{n \cdot \tau_{pd_{ff}}}$$

$T_{clk} \geq$ Sum of Delay of all the FF

(Asynchronous)

Q In BCD counter. Delay of FF is 10ns.

all FF are identical.

Find the clock frequency for stable operation?

$$f_{CLK} \leq \frac{1}{n \cdot \tau_{pdff}}$$

$$\leq \frac{1}{4 \times 10 \times 10^{-9}} \text{ Hz}$$

$$\leq \frac{10^9}{4 \times 10} \text{ Hz}$$

$$\leq \frac{1000}{4} \times 10^6 \text{ Hz}$$

$$\leq 250 \text{ MHz}$$

$(f_{CLK})_{max} = 25 \text{ MHz}$

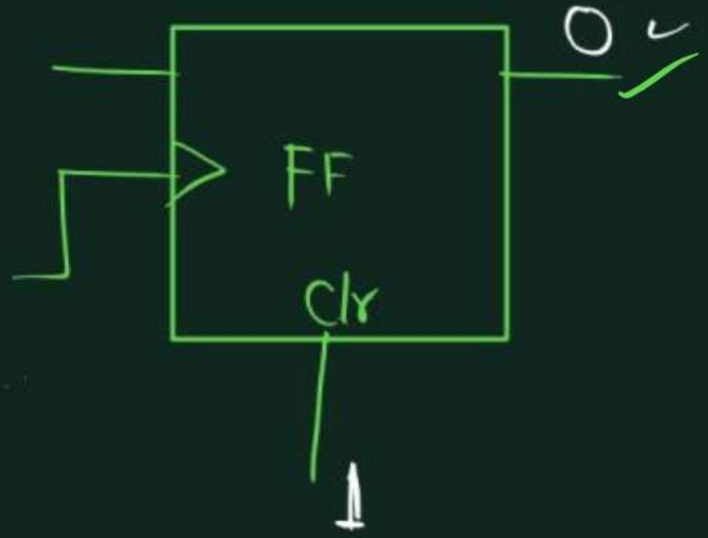
MOD = 10

$M \leq 2^n$

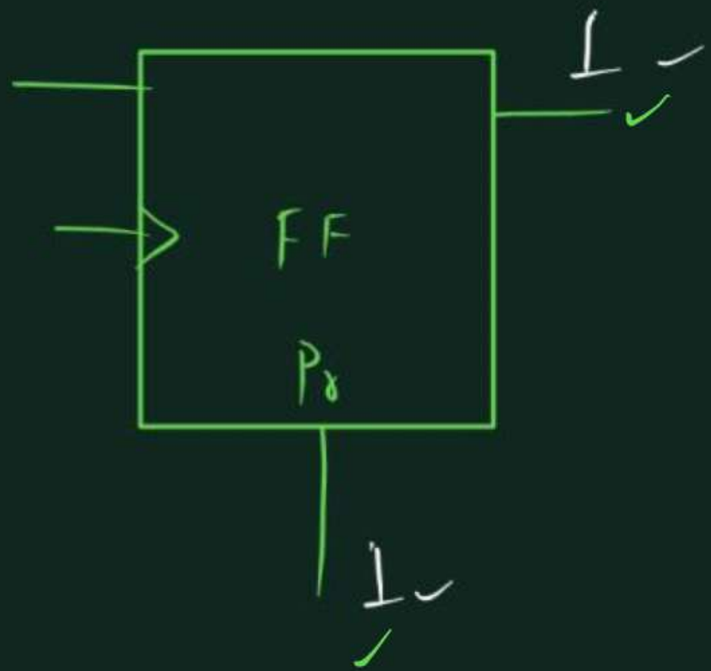
$n \geq \log_2 M$

$n \approx 4$

Reset (Clr)



Preset

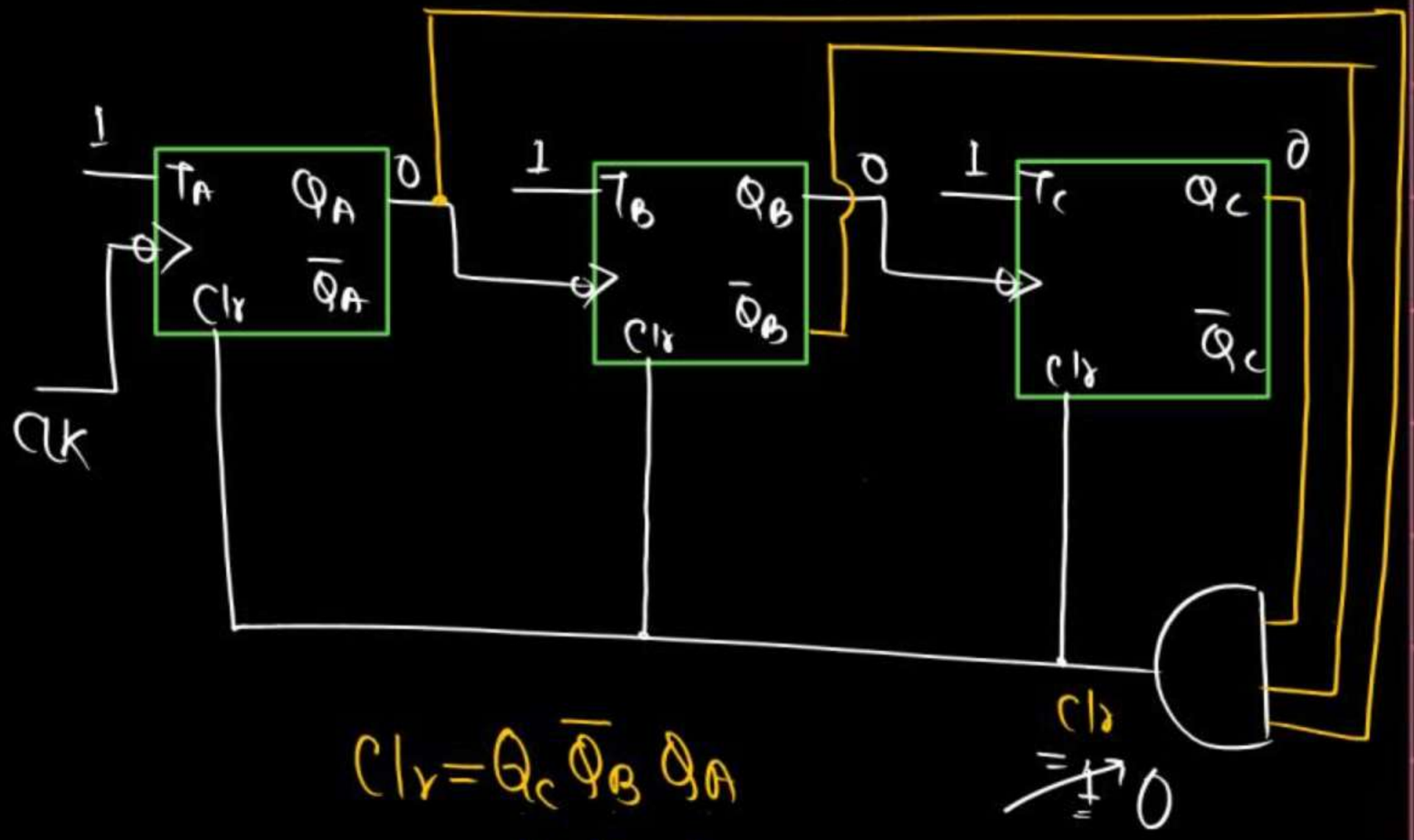


Asynchronous Counter

(UP) $Clr = Q_C \cdot \bar{Q}_B \cdot Q_A$ → (5) MOD

101

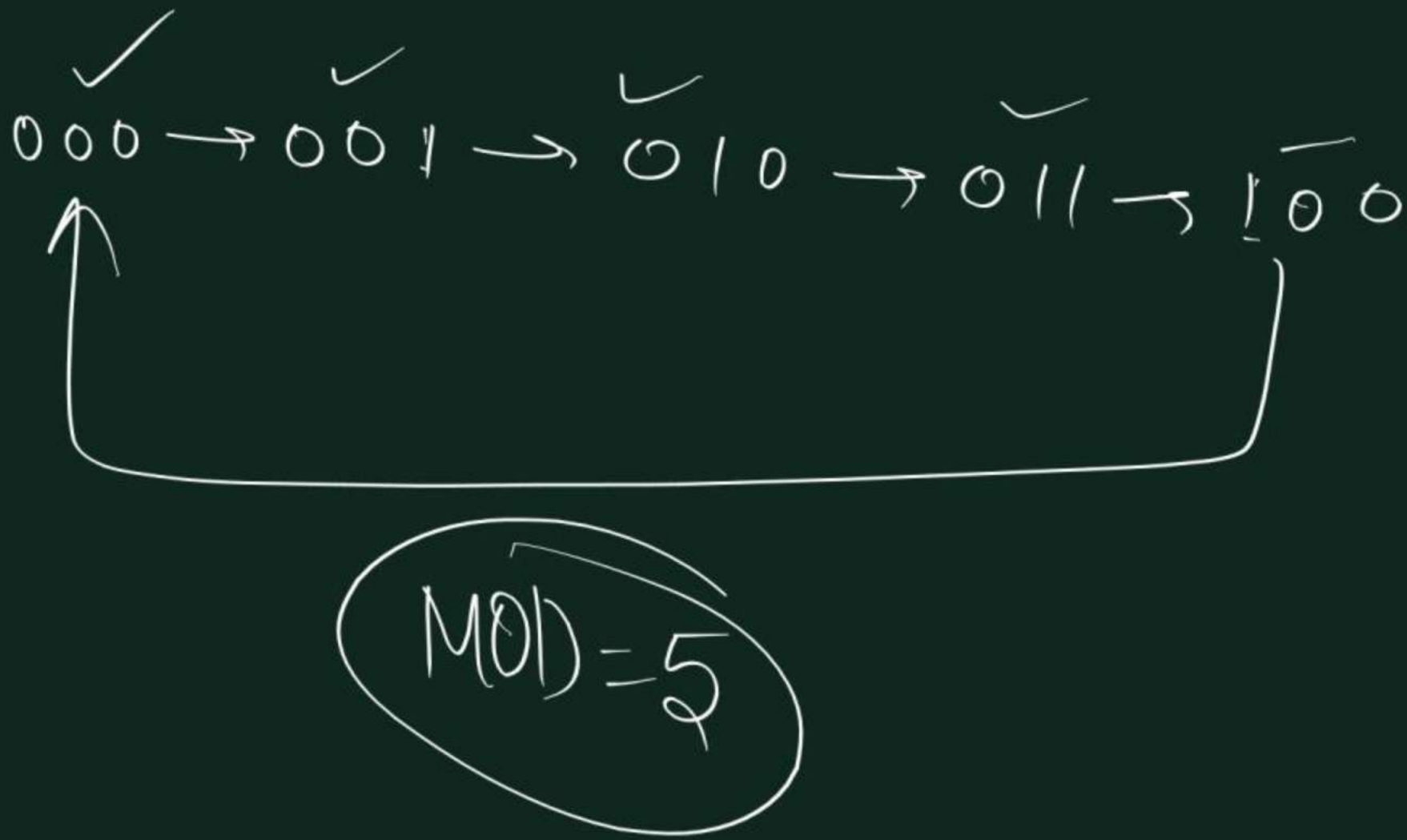
MOD-5 UP COUNTER



$Clr = Q_C \bar{Q}_B Q_A$

1 0 1

clock	Q_C	Q_B	Q_A	$Clr = Q_C \bar{Q}_B Q_A$
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1→0	0→0	1→0	1→0
6	0	0	1	0
7	0	1	0	0
8	0	1	1	0

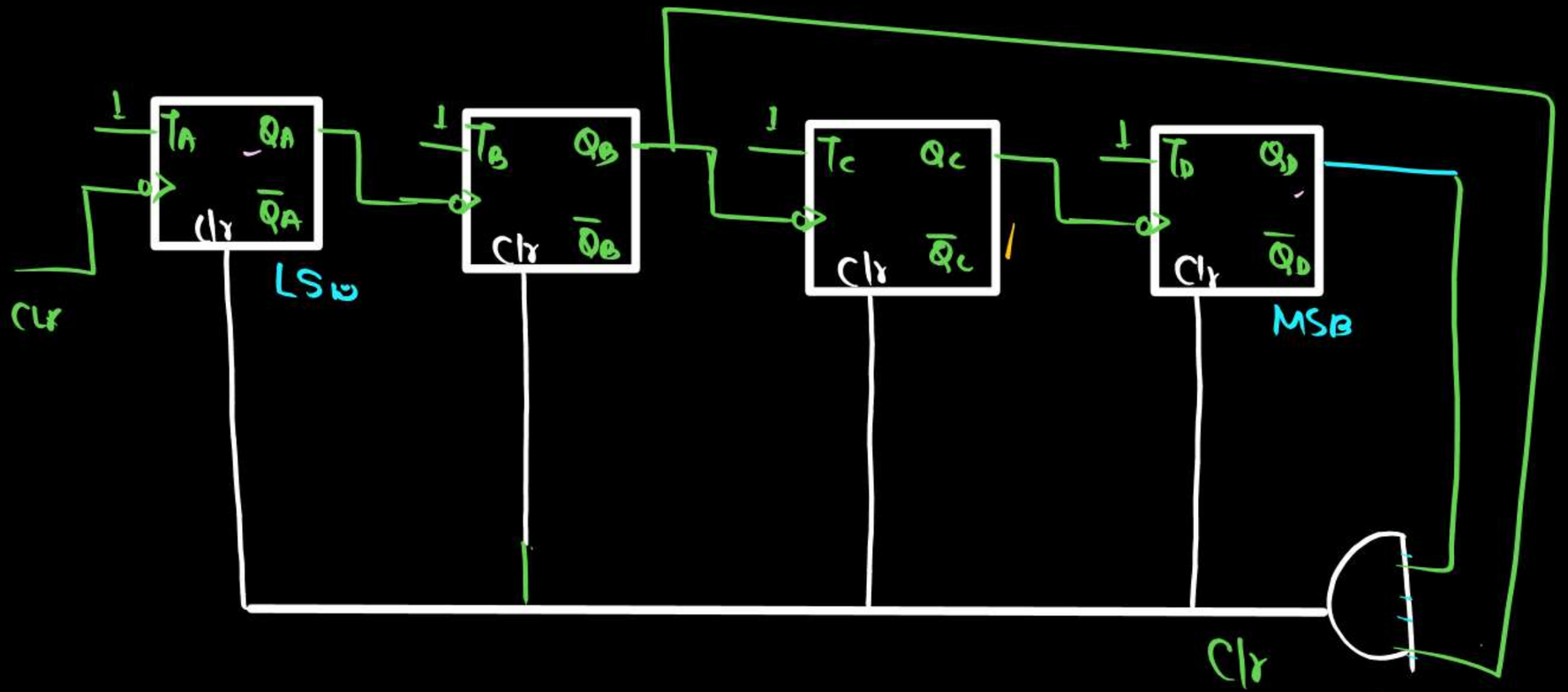

000 → 001 → 010 → 011 → 100
MOD = 5

जीत की ख़ातिर बस जूनून चाहिए,
जिसमें उबाल हो ऐसा खून चाहिए,
ये आसमान भी आ जाएगा ज़मीन पर,
बस इरादों में जीत की गूँज चाहिए।

Asynchronous Counter

clock	Q_C	Q_B	Q_C	Clr
0				
1				
2				
3				
4				
5				
6				
7				
8				

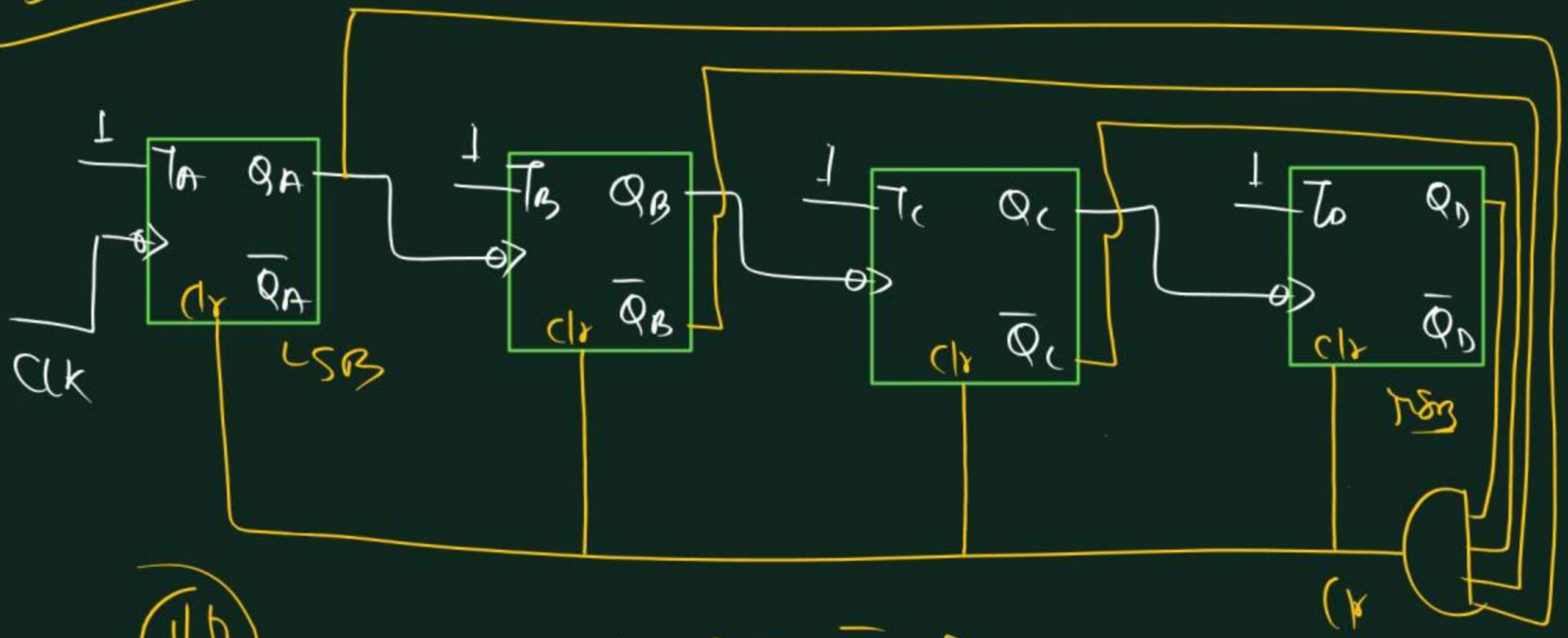
BCD Ripple counter:



$$Clr = Q_D \bar{Q}_C Q_B \bar{Q}_A$$

1 0 1 0 → (10) → MOD

#SHANDAR ♡



VP

$Clr = Q_D \bar{Q}_C \bar{Q}_B Q_A$

1 0 0 1 → 9

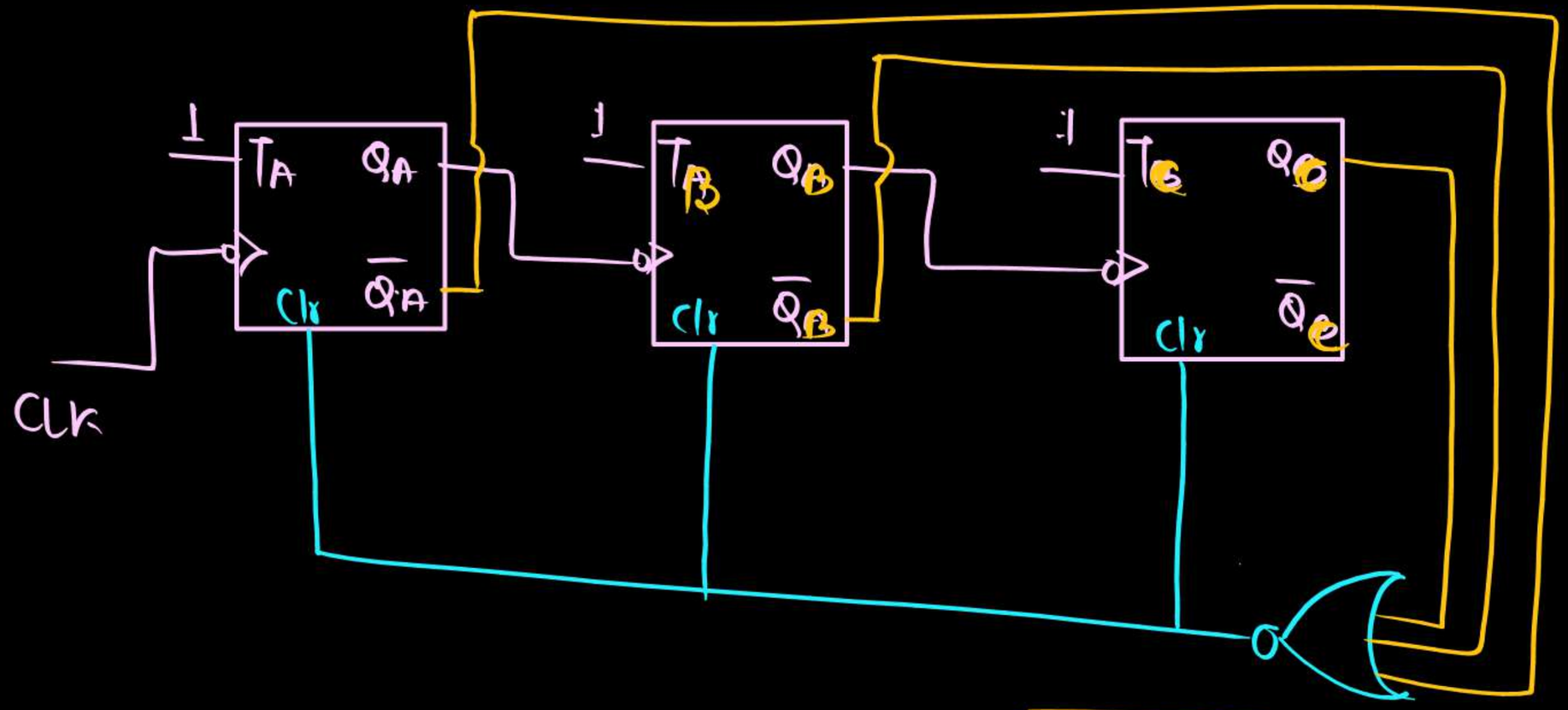
MOD-9 UP Ripple counter

Asynchronous Counter

$Q_D Q_C Q_B Q_A$

Q: Design a BCD counter

$Clr =$



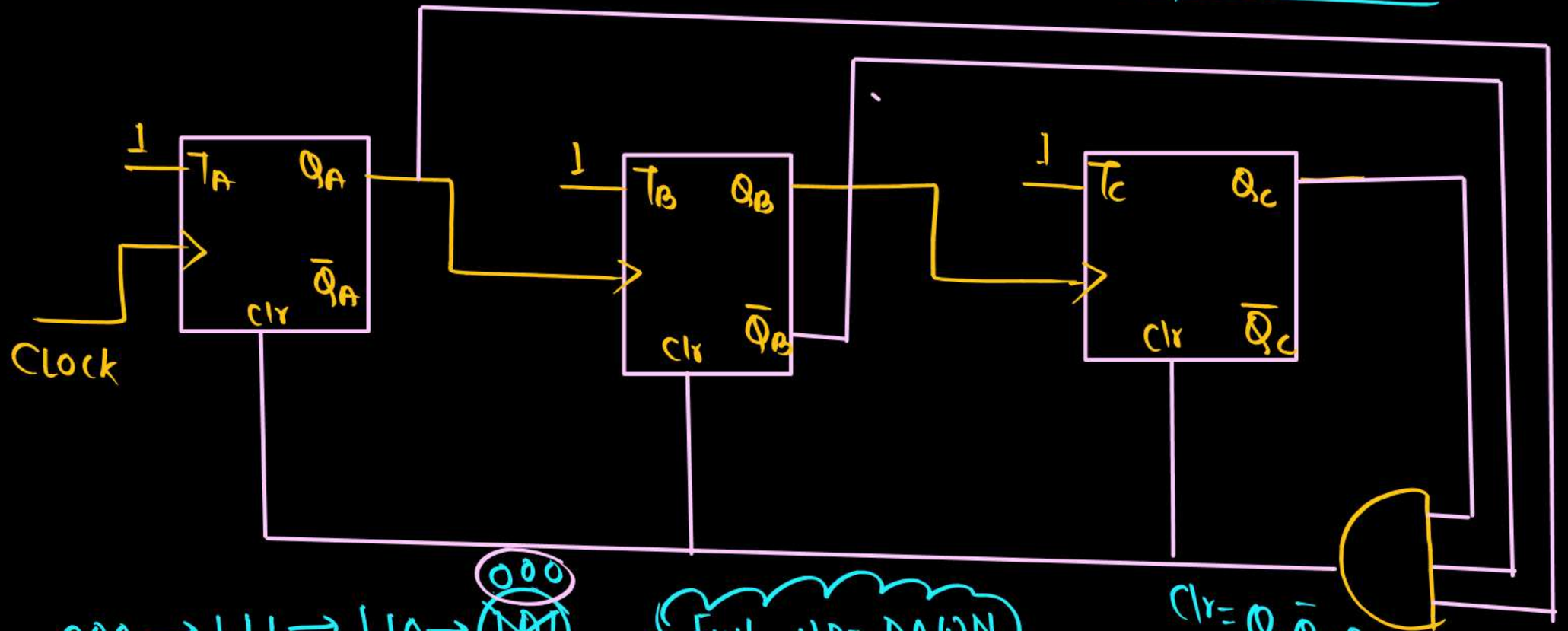
$$\overline{Clr} = Q_C + \overline{Q_B} + \overline{Q_A}$$

$$Clr = \overline{Q_C} \cdot Q_B \cdot Q_A$$

0 1 1 → MOD-3

Asynchronous Counter

Mod-3 Down Ripple counter :



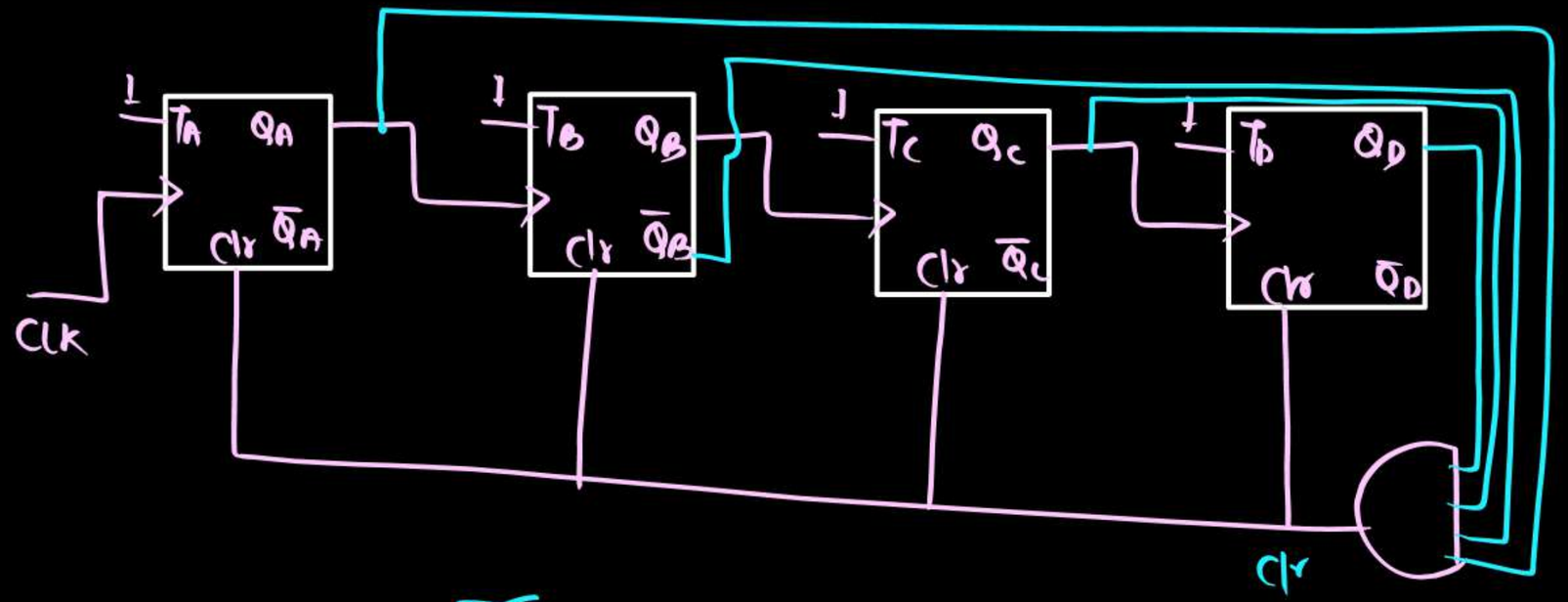
000 → 111 → 110 → ~~101~~ → 000

Full - UP = DOWN

8 - 5 = (3)

$Clr = Q_C \bar{Q}_B Q_A$

(1 0) →



$Clr = Q_D Q_C \bar{Q}_B Q_A$

1 1 0 1

= (13)

Full → 16

UP → 13

DOWN = FULL − UP

= 16 − 13

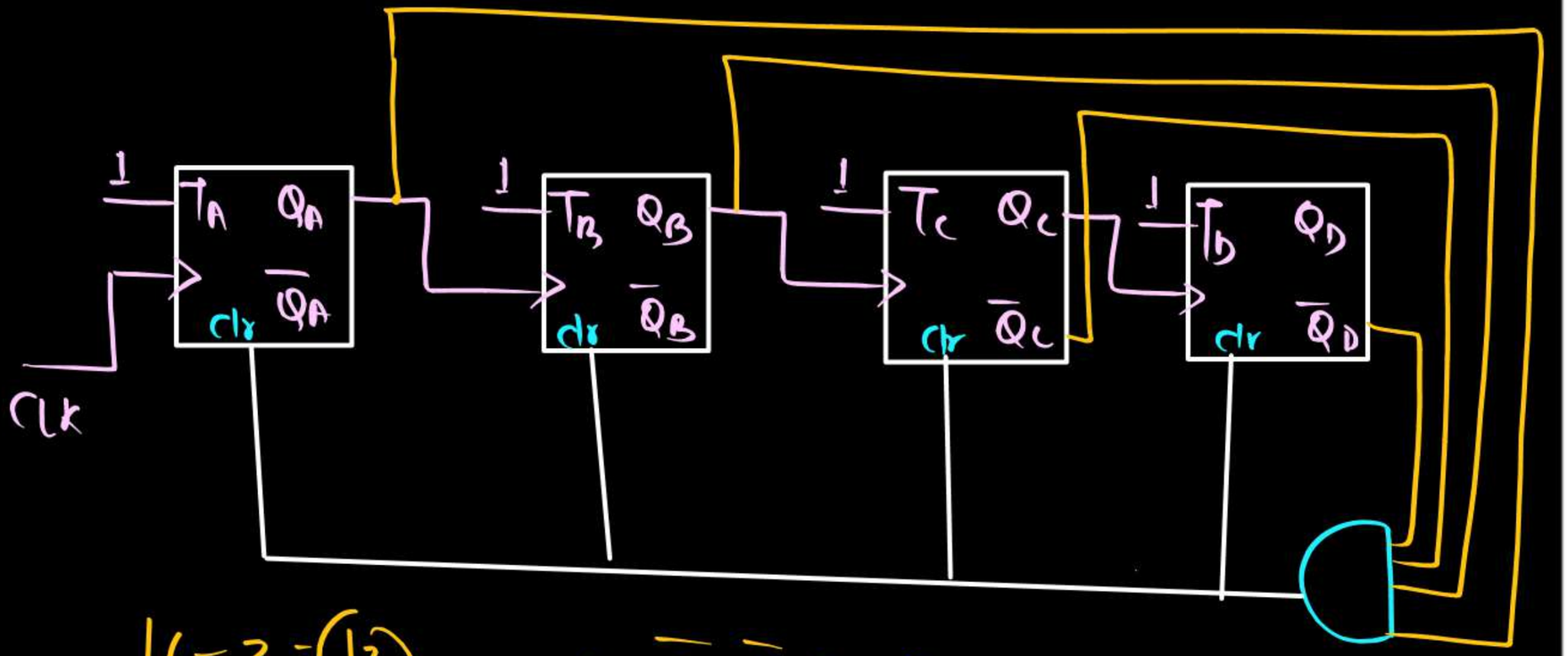
= (3)

Q Design (MOD-13) Down Ripple counter by using 4 FF ?

FULL - UP = DOWN

UP = FULL - DOWN

= 16 - 13 = (3)



3 = 0011

$Clr = \bar{Q}_D \bar{Q}_C Q_B Q_A$

16 - 3 = (13)

down

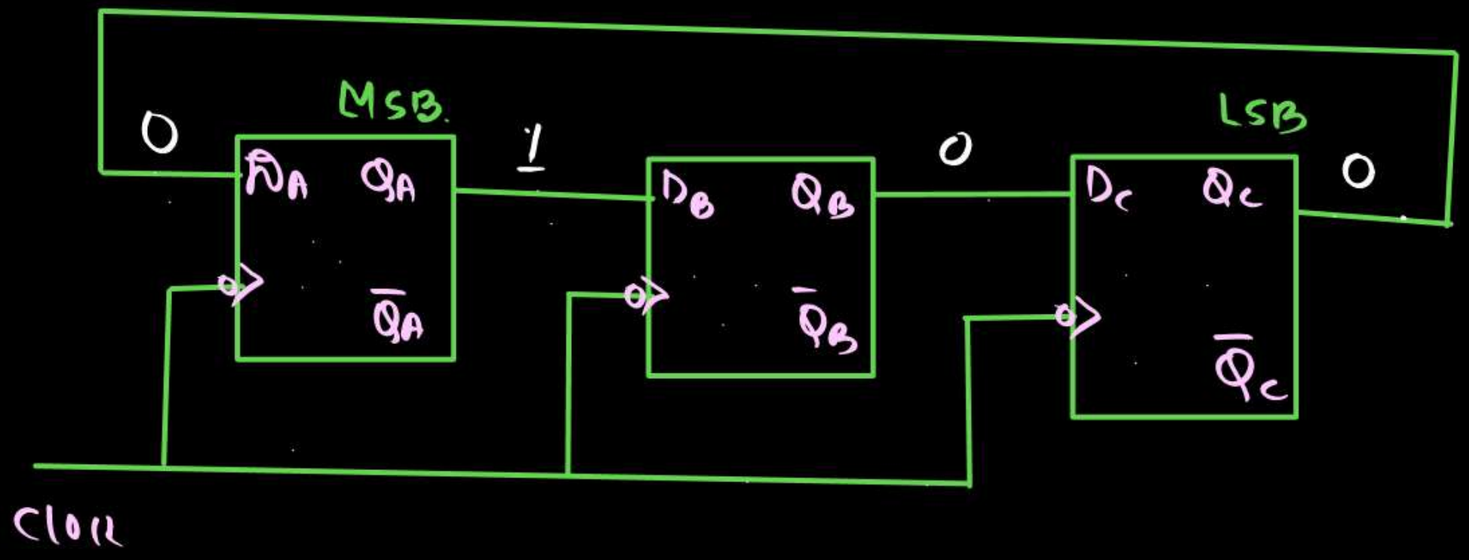
$Clr = \bar{Q}_D \bar{Q}_C Q_B Q_A$

0 0 1 1 → UP = 3

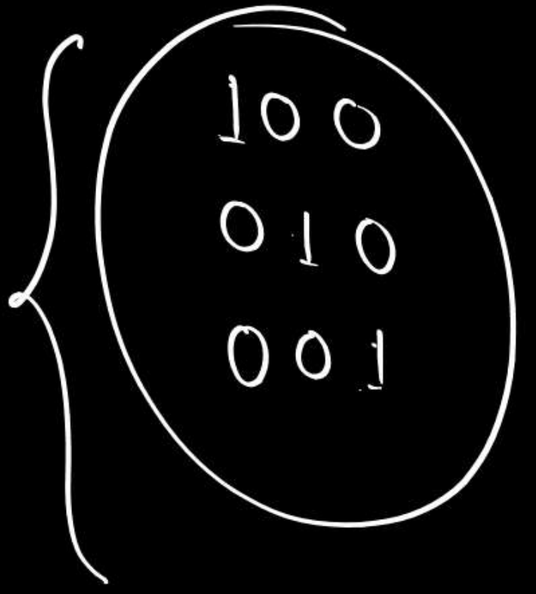
Synchronous counter

1. Ring counter
2. Johnson counter

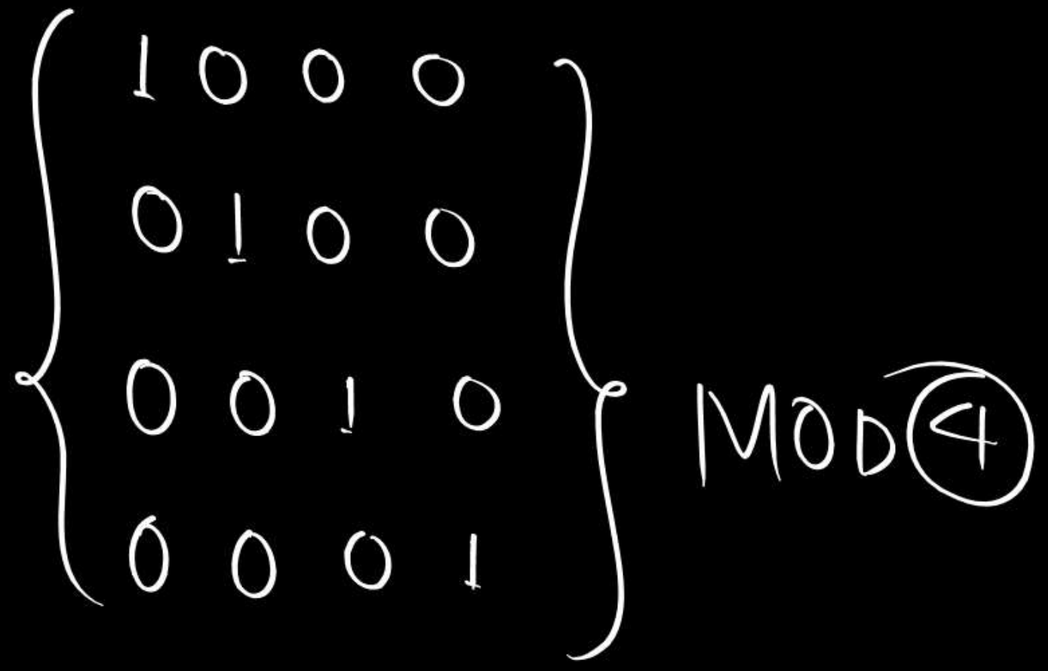
RING COUNTER :→



Clock	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	0	1	0
3	0	0	1
4	1	0	0



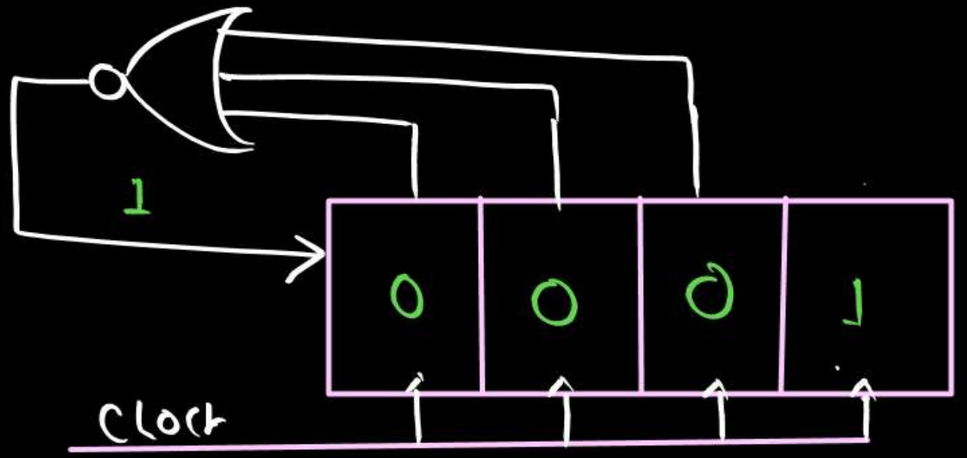
MOD = 3

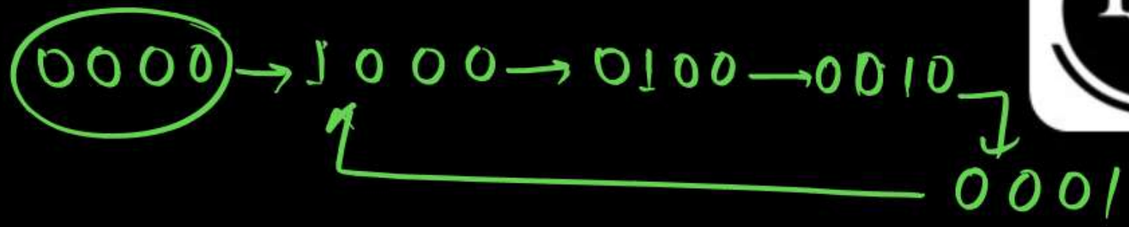

1 0 0 0
0 1 0 0
0 0 1 0
0 0 0 1
MOD 4

N bit Ring counter.

MOD = N.

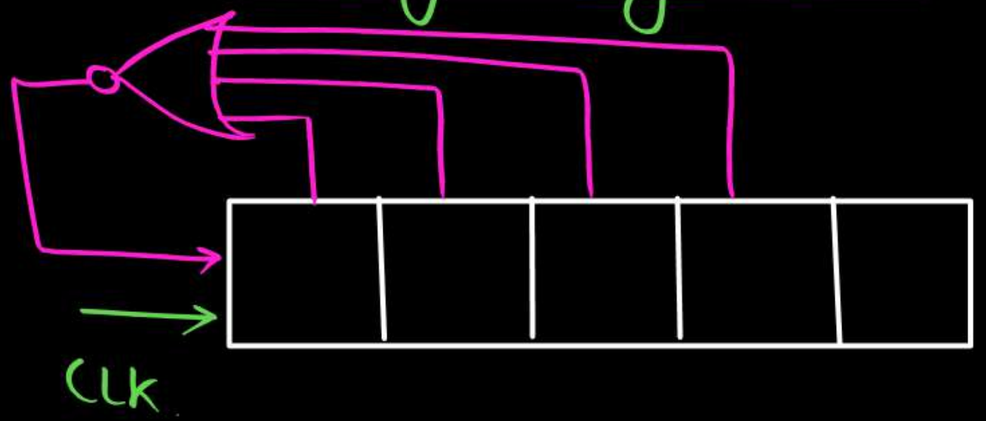
Symbolic Representation:





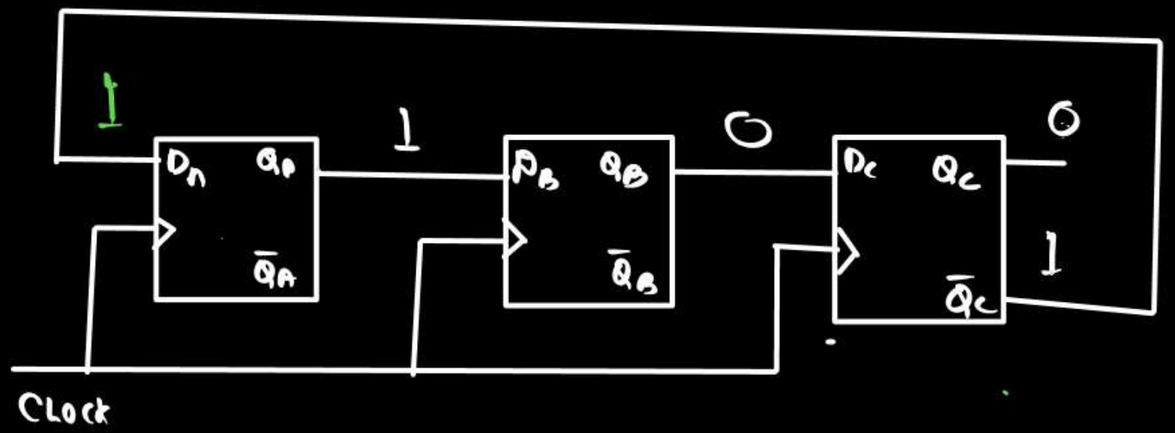
Clock	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	1	0	0	0

Self starting Ring counter



Johnson counter

- Twisted Ring counter
- Creeping counter
- Mobies counter
- Walking counter



CLock	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	0	0	0
7	1	0	0

$$\left\{\begin{matrix} 0\,0\,0 \\ 1\,0\,0 \\ 1\,1\,0 \\ 1\,1\,1 \\ 0\,1\,1 \\ 0\,0\,1 \end{matrix}\right\} \text{MOD 6}$$

4 bit Johnson counter

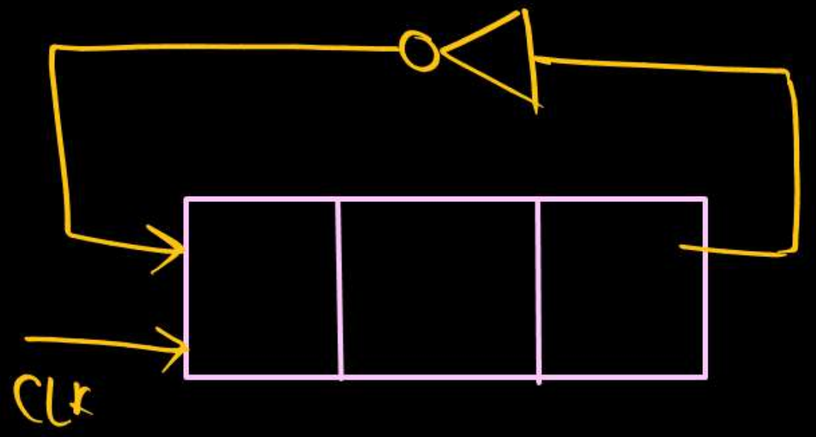
8 MOD

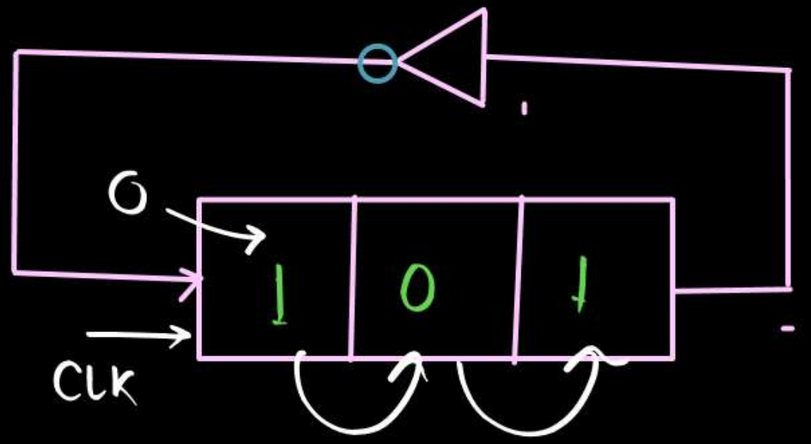
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1

'N' bit Johnson counter

Used state = MOD = 2N

Symbolic Representation



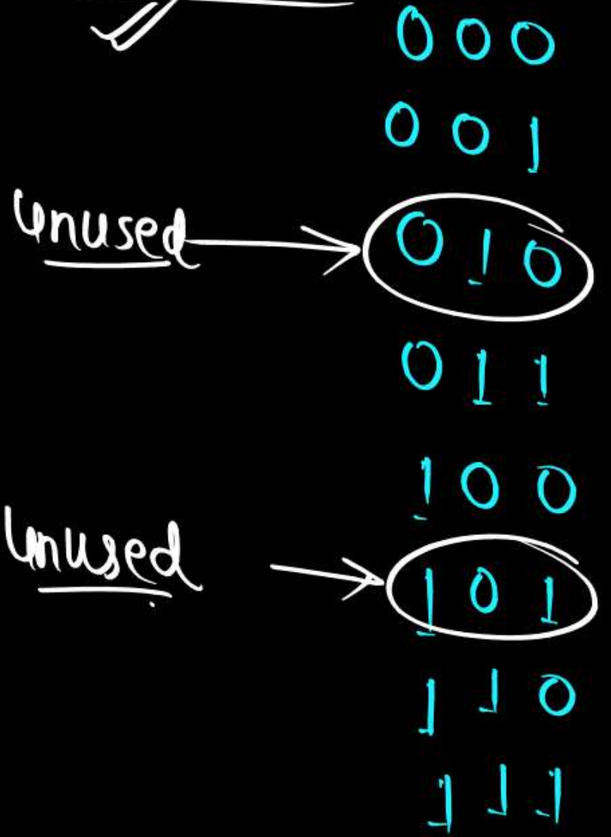


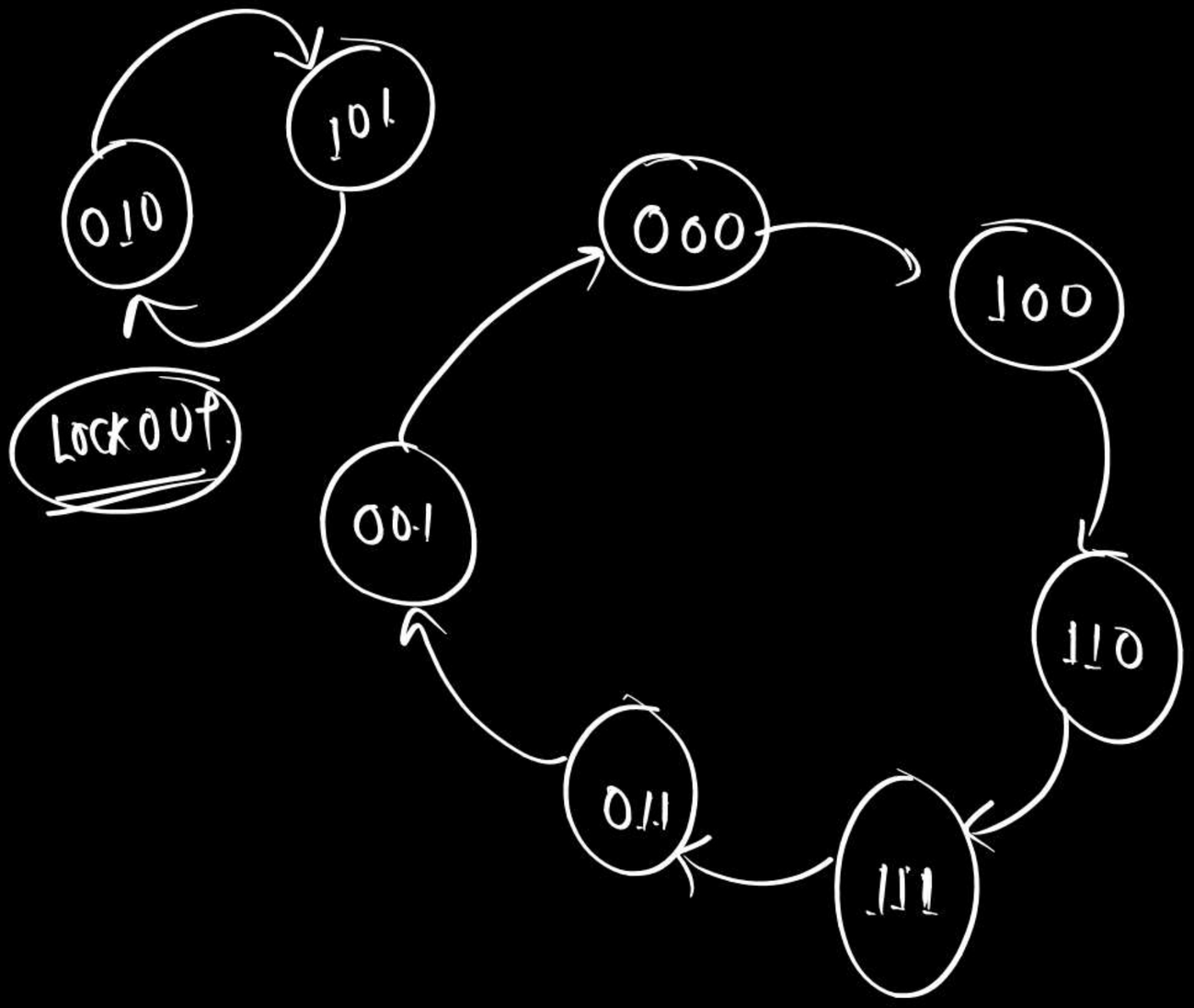
LOCKOUT PROBLEM

Clock	Q_1	Q_2	Q_3
0	0	1	0
1	1	0	1
2	0	1	0
3	1	0	1
4	0	1	0

LOCK

goto unused state




000
100
110
111
011
001
101
010
Lockout

Synchronous counter Design.

Step-1 : Write the present and Next state.

Step 2. Write the excitation table of Flip-Flop.

Step 3. Write the Logical expression

Step 4. Minimization

Step 5 → Hardware Implementation.

Q Design a synchronous counter by using (T-FF) which count

$Q_1 Q_0$

{ 00 → 01 → 10 → 11 }

Step 1.

Step 2.

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	0	0	1	1

Step 3.
Step 4

$T_1 = \bar{Q}_1 Q_0 + Q_1 Q_0$

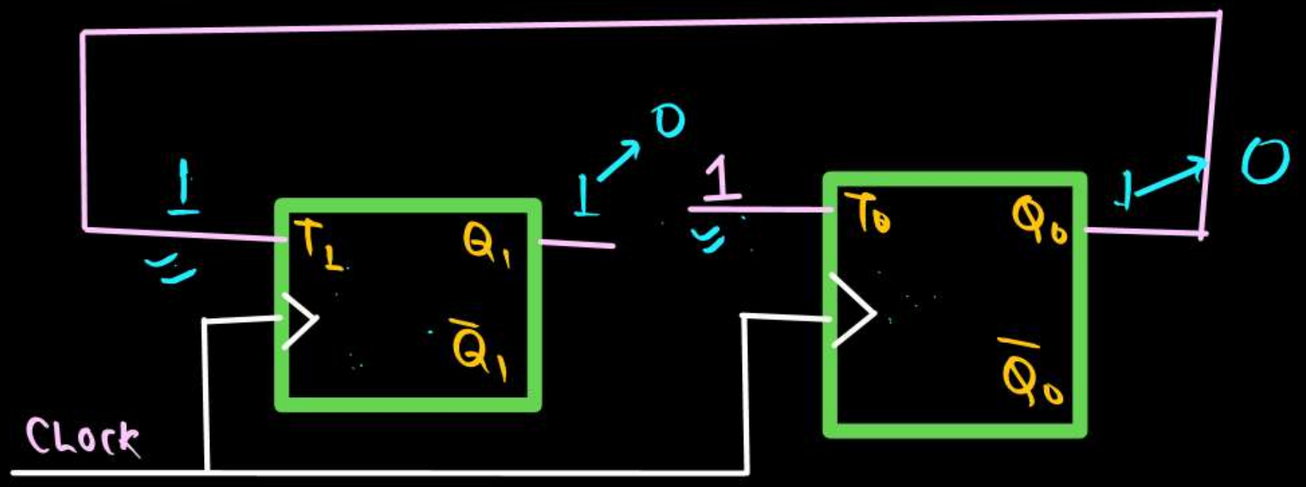
$T_1 = Q_0 (\bar{Q}_1 + Q_1)$

$\boxed{T_1 = Q_0}$

$\boxed{T_0 = 1}$

Step 5:

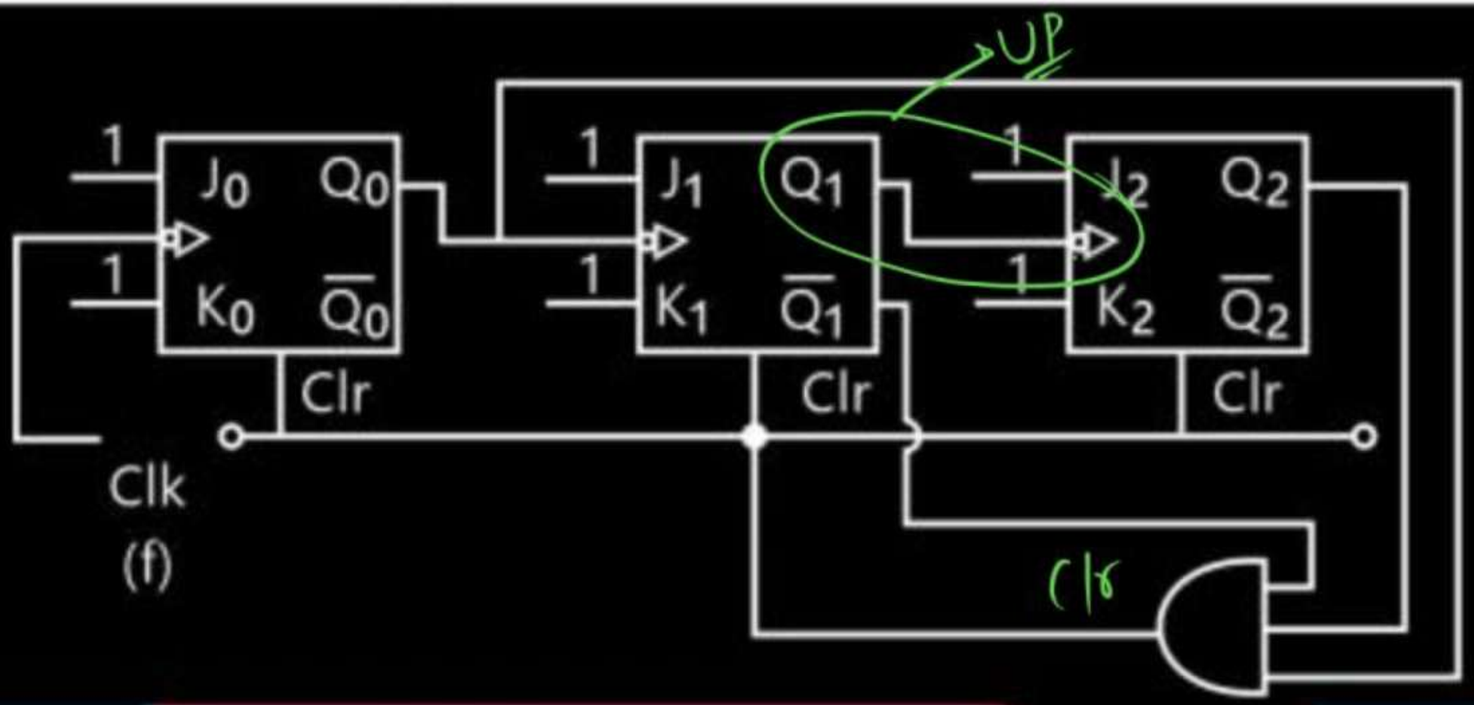
$T_1 = Q_0$ $T_0 = 1$



Clock	Q_1	Q_0
0	0	0
1	0	1
2	1	0
3	1	1
4	0	0

#CHAMKA

Q. Which type of counter is shown below?



Clr = $Q_2\bar{Q}_1Q_0$

1 0 1 = 5

A mod 5 down counter

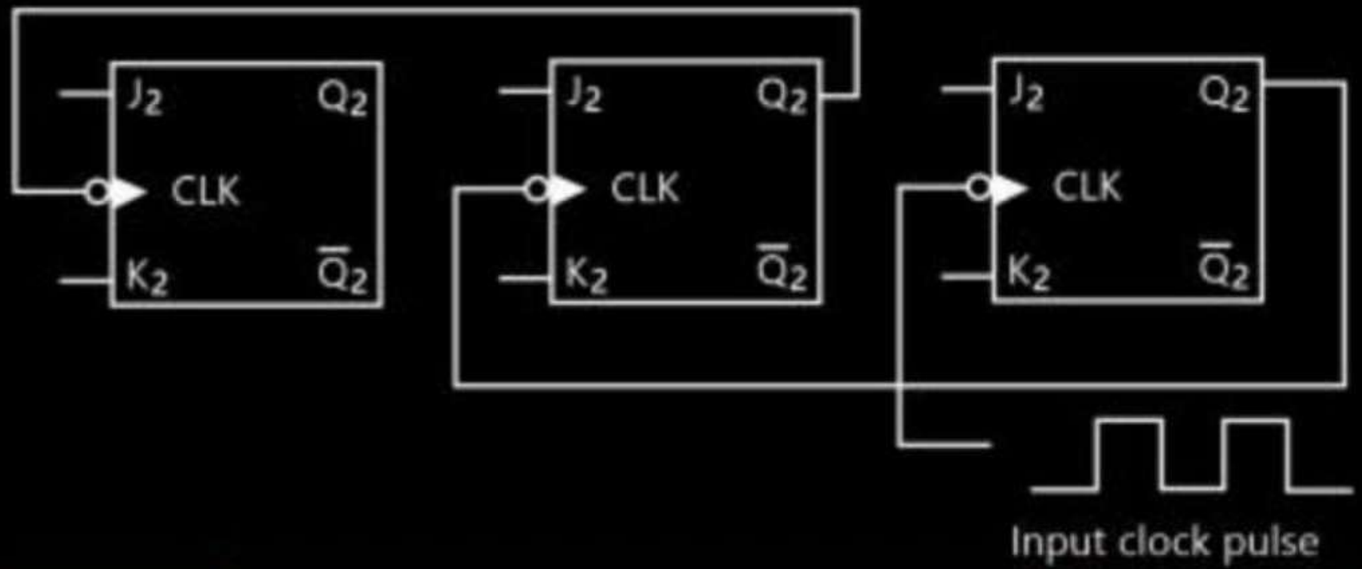
B mod 5 up counter

C mod 6 up counter

D mod 6 down counter

Q. Consider the following counter

If counter starts at 000, what will be the count after 13 clock pulses?



HW

Comment

A 100

B 101

C 110

D 111

BCD

$Cl_2 = ?$

सपने उनके सच होते हैं,
जिनके सपनों में जान होती है,
पँखो से कुछ नहीं होता,
हौंसलो से उड़ान होती है।


THANK
YOU!