



Kunal Jha
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 Computer Science Engineering(CS)

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TOPICWISE : COMPUTER ORGANIZATION AND ARCHITECTURE-1(GATE - 2020) - REPORTS

OVERALL ANALYSIS COMPARISON REPORT **SOLUTION REPORT**

ALL(17) CORRECT(4) INCORRECT(6) SKIPPED(7)

Q. 1

Solution Video Have any Doubt ?



Consider the following statements with respect to control unit.
 S_1 : Operating speed of vertical microprogramming is higher than that of horizontal microprogramming.
 S_2 : Horizontal microprogramming needs signal decoders as like vertical microprogramming.

Which of the following option is correct?

- A Both S_1 and S_2 are correct
- B Only S_1 is correct
- C Only S_2 is correct

- D None of S_1 or S_2 is correct

Correct Option

Solution :

- (d)
- Since, vertical microprogram encode the control signals hence a signal decoder is needed which decrease the operational speed of vertical micro-programming in comparison with horizontal micro-programming.
- Since, the control signal bits under horizontal microprogram control unit are not encoded. Hence no signal decoder is needed.

QUESTION ANALYTICS



Q. 2

Solution Video Have any Doubt ?



In a 16 bit computer instruction format, the size of address field is 5 bits. The computer uses expanding opcode technique. It has two 2-address instructions and 1024 one address instruction.
 How many zero-address instruction can be formulated?

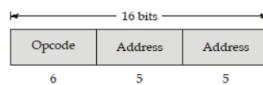
- A 28720
- B 30704

- C 30720

Correct Option

Solution :

- (c)
Address format



Number of operations = $2^6 = 64$

Number of free opcodes after 2-address = $64 - 2 = 62$

Number of 1 add instruction = $62 \times 2^5 = 1984$

Free opcodes after 1-address instructions = $1984 - 1024 = 960$

Number of 0 add instruction = $960 \times 2^5 = 30720$

- D 32704

QUESTION ANALYTICS



Q. 3

Solution Video Have any Doubt ?



The following assembly code is to be executed in a 3-stage pipelined processor with hazard detection and resolution in each stage. The stage are IF, OF (one or more as required) and execution (including write-back operation). What are the number of possible RAW, WAW and WAR hazards in the execution of the code.

Instruction

Meaning

I_1 : Inc R_0	$R_0 \leftarrow (R_0) + 1$
I_2 : Mul ACC, R_0	Acc $\leftarrow (ACC) \times (R_0)$
I_3 : Store R_1 , ACC	$R_1 \leftarrow (ACC)$
I_4 : Add ACC, R_0	Acc $\leftarrow (ACC) + (R_0)$
I_5 : Store M, ACC	M $\leftarrow (ACC)$

- A 6, 1, 2

- B 5, 3, 3

- C 5, 3, 2

Your answer is Wrong

Octal representation

$$\begin{array}{r} 8 \mid 416 \\ 8 \quad | 52 \quad 0 \\ \hline 6 \quad 4 \end{array}$$

Octal representation is (640).

QUESTION ANALYTICS**Q. 7****Solution Video****Have any Doubt ?**

A RISC processor has 208 registers. Each window has 4 input, 8 local and 4 output register. The total number of global registers are _____. The register windows are 16 in numbers.

16Your answer is **Correct** 16**Solution :****16**

Number of registers in RISC = G + W (L + C)
 $208 = G + 16(8 + 4)$
 $G = 16$

QUESTION ANALYTICS**Q. 8****Solution Video****Have any Doubt ?**

A PC relative mode branch instruction is 5 B long. The address of the instruction in decimal is 238715. The branch target address if the signed displacement is -32 is _____.

238688

Correct Option

Solution :**238688**

238715	I_1
238716	I_1
238717	I_1
238718	I_1
238719	I_1
238720	
238721	

Fetch I_1 IR:
PC = 238720

Effective address = PC + Relative value
= 238720 + (-32)
= 238688

Your Answer is **23688****QUESTION ANALYTICS****Q. 9****Solution Video****Have any Doubt ?**

Consider a hypothetical control unit that supports 5 groups of mutually exclusive control signals. Also assume that group-1 and group-2 are using horizontal micro-programming whereas group- 3, 4 and 5 are using vertical micro-programming. The total number of bits used for control words are _____.

Groups	G_1	G_2	G_3	G_4	G_5
Control signals	3	9	6	13	10

23

Correct Option

Solution :**23**

Group-1 and 2 are using horizontal micro-programming.
Hence, total bits are:

$$3 + 9 = 12$$

Group-3, 4 and 5 are using vertical micro-programming.
Hence, total bits are:

$$\lceil \log_2 6 \rceil + \lceil \log_2 13 \rceil + \lceil \log_2 10 \rceil = 3 + 4 + 4 = 11$$

$$\text{Total bits for control word} = 12 + 11 = 23 \text{ bits}$$

QUESTION ANALYTICS**Q. 10****Solution Video****Have any Doubt ?**

Consider a CPU, where all the instructions require 6 clock cycles to complete their execution. Under the instruction set there are 215 instructions and a total of 125 control signals are needed to be generated by the control unit. While designing the horizontal micro-programmed control unit, single address field format is used for branch control logic.

What is the minimum size of control word and control address register.

A 136, 11

Correct Option

Solution :

(a)
Since, it uses horizontal micro-programmed that requires 1 bit/control signal.
For 125 control signal, we need 125 bits.
Total number of micro-operation instruction = $215 \times 6 = 1290$
It requires 11 bit.

B 7, 12

C 7, 11

D 125, 12

 QUESTION ANALYTICS





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ALL(17)

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SKIPPED(7)

Q. 11

Solution Video

Have any Doubt ?



Consider the following statements:

 S_1 : Comparing the time T_1 taken for a single instruction on a pipelined CPU with time T_2 taken on a non-pipelined but identical CPU we can say that $T_1 \leq T_2$. S_2 : The performance of pipelined processor suffers if the pipeline stages have different delays.

Which of the following option is correct?

 A Both S_1 and S_2 are correct B Only S_1 is correct C Only S_2 is correct

Your answer is Correct

Solution :

(c)

- In pipelined CPU, there will be buffer delays. So, for single instruction non-pipelined CPU takes less time compared to pipelined CPU.
- Structural dependencies cause hazards during pipelining if stages having different delays.

 D None of S_1 or S_2 is correct

QUESTION ANALYTICS



Q. 12

Solution Video

Have any Doubt ?



An instruction pipeline consists of following 5 stages:

IF = Instruction Fetch, ID = Instruction Decode, EX = Execute,

MA = Memory Access and WB = Register Write Back.

Consider the following code:

- LOAD $R_1, [1000]$ $R_1 = \text{Memory} [1000]$
- LOAD $R_2, 4(R_2)$ $R_2 = \text{Memory} [R_2 + 4]$
- MUL R_4, R_1, R_3 $R_4 = R_1 \times R_3$
- DIV R_5, R_1, R_4 $R_5 = R_1 \div R_4$
- SUB R_6, R_4, R_5 $R_6 = R_4 - R_5$

Assume that each stage takes 1 clock cycle for all the instructions. The number of cycles saved to execute the code, by using operand forwarding over a without operand forwarding is

 A 7 B 8

Correct Option

Solution :

(b)

With operand forwarding

	1	2	3	4	5	6	7	8	9	10
I_1	IF	ID	EX	MA	WB					
I_2		IF	ID	EX	MA	WB				
I_3			IF	ID	X	EX	MA	WB		
I_4				IF	X	ID	EX	MA	WB	
I_5						IF	ID	EX	MA	WB

10 cycles are required

Without operand forwarding

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IF	ID	EX	MA	WB													
IF	ID	EX	MA	WB													
	IF	ID	X	X	X	EX	MA	WB									
		IF	X	X	X	ID	X	X	X	EX	MA	WB					
						IF	X	X	X	ID	X	X	EX	MA	WB		

S = Stall, 18 cycles are required.

The number of cycles saved using with operand forwarding = 18 - 10 = 8.

 C 9

Your answer is Wrong

 D 10

QUESTION ANALYTICS



Q. 13

Solution Video

Have any Doubt ?



Consider 1GHz clock frequency processor, uses different operand access modes shown below:

Operand Access Mode	Frequency (%)
---------------------	---------------

Register	20
Immediate	20
Memory Indirect	40
Auto Indexed	20

Assume that 8 cycle consumed for memory reference, 4 cycles consumed for arithmetic computation and 0 cycles consumed when the operand is in register instruction itself. What is the average operand fetch rate (in million words/sec) of the processor?

A 117.45 M words/sec

B 113.63 M words/sec

Correct Option

Solution :

(b)

$$\begin{aligned}\text{Average cycles/instruction} &= \{(0.2 \times 0) + (0.2 \times 0) + (0.4 \times 16) + (0.2 \times 12)\} \\ &= \{6.4 + 2.4\} = 8.8 \text{ cycles}\end{aligned}$$

So, average time = 8.8 nsec

1 operand requires 8.8 nsec

Number of operands fetched in 1 sec

$$\text{Number of operands} = \frac{1 \text{ sec}}{8.8 \text{ nsec}} = 0.113636 \times 10^9 \text{ operand/sec}$$

Operand fetch rate = 113.636 million words/sec

C 217.45 M words/sec

D 316.45 M words/sec

QUESTION ANALYTICS



Q. 14

Solution Video

Have any Doubt ?

Consider the cache memory which is 30 times faster than main memory and it can be used 90% of the total time. What is the speedup gain by cache memory?

A 7.33

B 7.46

C 7.69

Correct Option

Solution :

(c)

$$\begin{aligned}\text{Speedup (S)} &= \frac{1}{(1 - \text{Cache \% used}) + \left[\frac{\text{Cache \% used}}{\text{Speedup using cache}} \right]} \\ &= \frac{1}{(1 - F) + \left(\frac{F}{S} \right)} = \frac{1}{(1 - 0.9) + \left(\frac{0.9}{30} \right)} = \frac{1}{(0.1) + \left(\frac{0.9}{30} \right)} \\ &= \frac{30}{3.9} = 7.69\end{aligned}$$

D 7.52

QUESTION ANALYTICS



Q. 15

Solution Video

Have any Doubt ?

Consider the following program segment:

	Instruction	Meaning	Instruction size (in word)
I_1	Load $r_0, 300$	$r_0 \leftarrow [300]$	2
I_2	MOV $r_1, 5000$	$r_1 \leftarrow \text{Mem}[5000]$	2
I_3	MOV $r_2, (r_1)$	$r_2 \leftarrow \text{Mem}[r_1]$	1
I_4	Add r_0, r_2	$r_0 \leftarrow r_0 + r_2$	1
I_5	MOV, 6000, r_0	$\text{Mem}[6000] \leftarrow r_0$	2
I_6	HALT	Machine Halts	1

Consider that the memory is byte addressable with word size 16 bits and the program has been loaded starting from memory location $(2000)_{10}$. The return address will be saved in the stack, if an interrupt occurs while the CPU has been halted after executing the HALT instruction is _____.

2016

Correct Option

Solution :

2016

	Instruction	Instruction size	Location
I_1	Load $r_0, 300$	2 word	2000-2003
I_2	MOV $r_1, 5000$	2 word	2004-2007
I_3	MOV $r_2, (r_1)$	1 word	2008-2009
I_4	Add r_0, r_2	1 word	2010-2011
I_5	MOV, 6000, r_0	2 word	2012-2015
I_6	HALT	1 word	2016-2017

∴ Since 1 word is of 2 bytes.

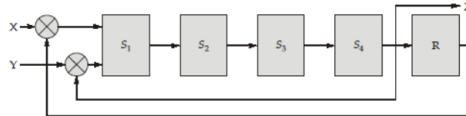
If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address 2016 is saved in the stack.

QUESTION ANALYTICS

Q. 16

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider a multiplier pipeline with 5 stages which consist of input lines X and Y and output line Z. The pipeline has a register R as its output, where the temporary result can be stored and feed back to S₁ at a later point in time. The inputs X and Y are multiplexed with the outputs R and Z.



Assume that elements of vector A are fed in to the pipeline through input X, one element per cycle. The minimum number of clock cycles required to compute the product of an element vector.

The following code is running on a above pipeline with operand forwarding.

Instruction	Meaning
I ₁ : Load ACC, R	ACC \leftarrow (R) [R = A _j]
I ₂ : Inc, R	R \leftarrow (R) + 1
I ₃ : Mul ACC, R	ACC \leftarrow (ACC) \times (R)
I ₄ : Store R, ACC	R \leftarrow (ACC)

How many cycles required to compute the program _____.

7

Correct Option

Solution :

7

The minimum number of clock cycles can be obtained by writing its assembly code. The process in obtaining the outputs Z and R from input line X or Y via the same manner, such that the codes are not much different except there is a line code to execute store command when using input line X. The code is as follows:

Instruction	Meaning
I ₁ : Load ACC, R	ACC \leftarrow (R) [R = A _j]
I ₂ : Inc, R	R \leftarrow (R) + 1
I ₃ : Mul ACC, R	ACC \leftarrow (ACC) \times (R)
I ₄ : Store R, ACC	R \leftarrow (ACC)

Constructing the table:

	1	2	3	4	5	6	7
I ₁	F	D	E	W			
I ₂		F	D	E	W		
I ₃			F	D	E	W	
I ₄				F	D	E	W

So, the minimum clock cycles required to complete one process is 7 clock cycles.

Your Answer is 8

QUESTION ANALYTICS

Q. 17

[▶ Solution Video](#)[Have any Doubt ?](#)

A 5-stage pipelined processor has IF, ID, EX, MA and WB. WB stage operation is divided into two parts. In the first part register write operation and in the second part register read operation is performed. The latency of all those stages are 300, 400, 500, 500 and 300 (in nano seconds) respectively. Consider, the following code is executed on this processor, operand forwarding is used in the pipeline

Instruction No.	Instruction	Meaning of Instruction
I ₁	ADD R ₀ , R ₀ , R ₄	R ₀ \leftarrow R ₀ + R ₄
I ₂	SUB R ₀ , R ₄ , R ₃	R ₀ \leftarrow R ₄ - R ₃
I ₃	ADD R ₀ , R ₂ , R ₃	R ₀ \leftarrow R ₂ + R ₃
I ₄	SUB R ₀ , R ₀ , R ₄	R ₀ \leftarrow R ₀ - R ₄

The program execution time _____ (ns).

4000

Your answer is Correct4000

Solution :

4000

Cycle	1	2	3	4	5	6	7	8
I ₁	IF	ID	EX	MA	WB			
I ₂	IF	ID	EX	MA	WB			
I ₃		IF	ID	EX	MA	WB		
I ₄			IF	ID	EX	MA	WB	

8 Cycles \times 500 ns = 4000 ns

QUESTION ANALYTICS





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OVERALL ANALYSIS COMPARISON REPORT **SOLUTION REPORT**

ALL(17) CORRECT(8) INCORRECT(6) SKIPPED(3)

Q. 1

Solution Video

Have any Doubt ?



Consider the following statements:

- S_1 : More than one word are put in one cache block to reduce the miss penalty.
 S_2 : Virtual memory increases the degree of multiprogramming.
 S_3 : Increasing the RAM of a computer typically improves performance because virtual memory increase.

How many of the above statements are correct?

A Only S_1 and S_2

B Only S_1 and S_2

Your answer is Correct

C Only S_2

D All S_1 , S_2 and S_3

QUESTION ANALYTICS



Q. 2

Solution Video

Have any Doubt ?



A computer has a 256 KB, K-way set associative write-back data cache with block size of 32 B. The address sent to the cache controller by the processor is of 32 bits. In addition to the address tag, each cache tag directory contains 2 valid bits and 1 modified bit. If 16 bits are used to address tag. What is the minimum value of K?

A 6

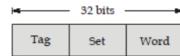
B 5

C 4

Your answer is Correct

Solution :

(c)
 Address format:



Block size = 32 B

\therefore Bits needed for word offset = 5

Number of tag bits = 16

Address bits = $32 - (16 + 5) = 32 - 21 = 11$

$$\text{Number of sets} = \frac{\text{Number of cache lines}}{\text{K-way}}$$

$$\text{Number of cache lines} = \frac{2^{18}}{2^5} = 2^{13} \quad \left[\begin{array}{l} \because 18 \text{ bits since Cache is of } 256 \text{ KB,} \\ 5 \text{ bits because block size is } 32 \text{ B} \end{array} \right]$$

$$\text{Number of sets} = \frac{2^{13}}{K} = 2^{11}$$

$$K = \frac{2^{13}}{2^{11}} = 4$$

Hence, the cache is 4-way set associative.

D None of these

QUESTION ANALYTICS



Q. 3

Solution Video

Have any Doubt ?



A computer system that used memory mapped IO configuration, has a 32-bit address space. Address with 1's in the two MSB refer to devices. What is the maximum amount of memory space and IO address space can be referenced in such a system respectively?

A 3×2^{30} and 1×2^{30}

Your answer is Correct

Solution :

(a)

The given address space is of 32 bits. Also, it is given that '11' as the MSB in those 32 bits, refer to

IO devices. That means out of 32 '2'-bits are fixed, so total IO address space can be 1×2^{30} . Similarly, since '11' are reserved hence, the total memory address space will be 3×2^{30} .

- B 1×2^{30} and 3×2^{30}
- C 2×2^{20} and 1×2^{20}
- D 3×2^{32} and 1×2^{32}

QUESTION ANALYTICS

Q. 4

Solution Video

Have any Doubt?



Which of the following is/are true?

S_1 : The main advantage of direct mapping is that the cache hit ratio increases drastically if two or more frequently used blocks map onto same region.
 S_2 : For two level memory hierarchy cache and main memory, WRITE THROUGH results in more write cycles to main memory than WRITE BACK.

- A Only S_1
- B Both S_1 and S_2
- C Only S_2
- D None of these

Correct Option

Solution :

(c) S_1 : Main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on to same region.

S_2 : Because each and every WRITE operation is done simultaneously on both cache and main memory. WRITE THROUGH results in more cache cycles than WRITE BACK.

QUESTION ANALYTICS

Q. 5

Solution Video

Have any Doubt?



Consider the following statements:

S_1 : 3 control signals are needed for memory data register.
 S_2 : The main advantage of direct mapping is that the cache hit ratio increases drastically if two or more frequently used blocks map onto same block.
 Which of the following option is correct ?

- A Only S_1 is true
- B Only S_2 is true
- C Both S_1 and S_2 are true
- D Neither of S_1 or S_2 is true

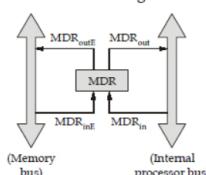
Correct Option

Solution :

(d)

Considering each statement:

S_1 : 4-control signals are needed for each data register.



MDR is directly connected to data lines of the processor. It has 2 input and 2 output. Data may be loaded into MDR either from memory or from internal bus. Data present in MDR may be placed on either bus are memory. It requires total 4 control signals.

S_2 : The main disadvantage of direct mapping is that cache hit ratio decreases sharply if two or more frequently used blocks map on the same region.

QUESTION ANALYTICS

Q. 6

Solution Video

Have any Doubt?



Consider a system which employs an interrupt driven I/O for a particular device that transfer data at an average of 10 KBps on a continuous basis. Assume that interrupt processing takes about 100 μ s (i.e. jump to the interrupt service routine (ISR), execute it and return to the main program). The fraction of processor time which is consumed by this I/O device when it is interrupted for every byte is _____ (Upto 2 decimal places)

(1.00) [1.00 - 1.10]

Your answer is Correct!

Solution :
 (1.00) [1.00 - 1.10]
 The device generates

LAW OF RAYLEIGH

$$10 \times 1000 = 10,000 \text{ Bps}$$

i.e. 10240 B are transmitted per second

$$1 \text{ Byte} = \frac{1}{10,000} \text{ sec} = 100 \mu\text{sec}$$

Given, that each interruption take 100 μsec

$$\therefore \text{Fraction of processor time consumed} = \frac{100 \mu\text{sec}}{100 \mu\text{sec}} = 1$$

QUESTION ANALYTICS

Q. 7

Solution Video

Have any Doubt?



Consider a small 2-way set associative cache memory, consisting of 4 blocks. For choosing the block to be replaced, use LRU scheme. Consider that block address 4 and 2 are already there in cache. The number of cache misses for the following sequence of block addresses 4, 6, 8, 16, 2, 4 are _____.

5

Your answer is Correct5

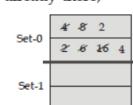
Solution :

5

Cache will be divided as,



Since block addresses 4 and 2 are already there,



Total number of misses = 5

QUESTION ANALYTICS

Q. 8

Solution Video

Have any Doubt?

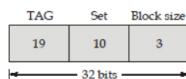


Consider a 32 bit microprocessor that has on chip 32 K byte 4 way set associative cache. Block size of cache is two 32 bit words. The set number (in decimal) to which the word from memory location FAFEEBE1 wrapped _____.

380

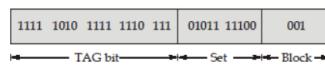
Correct Option

Solution :
380



$$\text{Number of lines} = \frac{32 \times 2^{10} \text{ B}}{2^3 \text{ B}} = 2^{12}$$

$$\text{Number of set} = \frac{2^{12}}{4 \text{ Way}} = 2^{10}$$



$$\text{Set} = 010111100 = 380$$

Your Answer is 1019

QUESTION ANALYTICS

Q. 9

Solution Video

Have any Doubt?



A cache block has 64 kbyte. The main memory has latency 64 μsec and bandwidth 1 GBps. The total time required to fetch the entire cache block from the main memory (in μsec , $1\text{G} = 10^9$) is _____.

128

Your answer is Correct128

Solution :

128

For 1 second it take 10^9 byte

$$\text{So for 64 kbyte it takes} = \frac{64k}{10^9} = 64 \mu\text{sec}$$

Main memory latency = 64 μsec

Total time required to fetch = $64 \mu\text{sec} + 64 \mu\text{sec} = 128 \mu\text{sec}$

Q. 10

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider the following statement. Out of the statements choose the one which best characterize computers that use memory mapped I/O.

A the computer provides special instruction for manipulating I/O port.

B I/O ports are placed at address on bus and as accessed just like other memory location.

Your answer is **Correct**

Solution :

(b)

Memory mapped I/O uses the same address bus to address both memory and I/O devices the memory and registers of the I/O devices are mapped to address values. So, when an address is accessed by the CPU, it may refer to a portion of physical RAM, but it can also refer to memory of I/O device.

C to perform an I/O operation, it is sufficient to place the data in an address and call the channel to perform the operation

D ports are referenced only by memory mapped instruction of the computer and are located at hardwired memory location.



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SKIPPED(3)

Q. 11

Solution Video

Have any Doubt ?



Match List-I with List-II and select the correct answer using the codes given below the lists:

List-I

- A. Programmed IO
- B. Interrupt driven IO
- C. Direct memory access

List-II

1. On I/O command issued by the processor, the processor busy-waits for the operation to be completed.
2. After issuing an I/O command, processor continues to execute subsequent instructions, and is interrupted by the concerned module, when latter has completed its work.
3. Processor send a request for the transfer of a block of data to the concerned module and is interrupted when the entire block has been transferred.

Which of the following code is correct?

Codes:

	A	B	C
(a)	1	3	2
(b)	1	2	3
(c)	2	1	3
(d)	1	3	2

 A a B b

Correct Option

Solution :

(b)

Programmed I/O: Processor issues an IO command, on behalf of a processor, to an IO module; that process then busy-waits for the operation to be completed before proceeding.

Interrupt driven I/O: The processor issues an IO command on behalf of a process, continues to execute subsequent instruction, and is interrupted by the IO module when the latter has completed its work.

Direct memory access: A DMA module controls the exchange of data between main memory and IO module.

 C c

Your answer is Wrong

 D d

QUESTION ANALYTICS



Q. 12

Solution Video

Have any Doubt ?



In a vectored interrupt:

 A The interrupting device supplies the branch information to the processor through an interrupt vector.

Correct Option

Solution :

(a)

A vectored interrupt is the one, where CPU actually knows the address of the ISR in advance, with the help of an interrupt vector, the interrupting device supplies the branch information to the processor.

 B The CPU does not know, which device cause the interrupt without polling each I/O interface. C The branch address is always assigned to a fixed location in memory.

Your answer is Wrong

 D None of the above

QUESTION ANALYTICS



Q. 13

Solution Video

Have any Doubt ?



The designers of a cache system need to reduce the number of cache misses that occur in a certain group of programs. Which of the following statements is/are true?

S₁ : If compulsory misses are most common, then the designers should consider increasing the cache line size to take better advantage of locality.S₂ : If capacity misses are most common, then the designers should consider increasing the total cache size so it can contain more lines.S₃ : If conflict misses are most common, then the designers should consider increasing the cache's associativity, in order to provide more flexibility when a collision occurs. A S₃ only

B S_1 and S_2 only

C S_2 and S_3 only

Your answer is Wrong

D All of these

Correct Option

Solution :

(d)

Increasing the cache line size brings in more from memory when a miss occurs. If accessing a certain byte suggests that nearby bytes are likely to be accessed soon (locality), then increasing the cache line essentially prefetches those other bytes. This, in turn, forestalls a later cache miss on those other bytes.

If misses occur because the cache is too small, then the designers should increase the size!

Conflict misses occur when multiple memory locations are repeatedly accessed but map to the same cache location. Consequently, when they are accessed, they keep kicking one another out of the cache. Increasing the associativity implies that each chunk of the cache is effectively doubled so that more than one memory item can rest in the same cache chunk.

QUESTION ANALYTICS

Q. 14

Solution Video

Have any Doubt?



A 4-way set associative cache memory consists of 128 blocks. The main memory consist of 32768 memory blocks and each block contain 512 eight bit words. Find how many bits are needed to represent TAG, SET and WORD field respectively?

A 5, 9, 10

B 10, 6, 8

C 10, 9, 5

D 10, 5, 9

Your answer is Correct

Solution :

(d)

$$\text{Main memory size} = 32768 \text{ blocks}$$

$$1 \text{ block} = 512 \text{ words}$$

$$= 32768 \times 512 \text{ words} = 2^{15} \times 2^9 = 2^{24} \text{ words}$$

Main memory takes 24 bits.

$$\text{Block size} = 512 \text{ words} = 2^9 \text{ words}$$

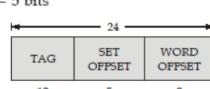
Number of bits for block size = 9 bits.

Number of blocks in set associative = 128

Number of blocks in one set = 4

$$\text{Number of sets in cache} = \frac{128}{4} = 32 = 2^5$$

Number of bits in set offset = 5 bits



$$\text{Number of TAG bits} = 24 - (9 + 5) = 10 \text{ bits}$$

QUESTION ANALYTICS

Q. 15

Solution Video

Have any Doubt?



Consider a system that uses interrupt-driven I/O for a particular device which has an average data transfer rate of 10 KBps. The processing of the interrupt which includes the time to jump to ISR, its execution and returning to the main program is 250 μ s. The fraction of processor time of consume by I/O device, if I/O device interrupts for every 2 byte (in %) is _____.

80

Correct Option

Solution :

80

Number of interrupts generated = 5000 interrupt/sec

Time by 1 interrupt = 200 μ sec

Time consumed by every interrupt = 250 μ s

$$\text{Fraction of processor time consumed} = \frac{200}{250} = 0.8$$

In % = $0.8 \times 100 = 80$

Your Answer is 1.25

QUESTION ANALYTICS

Q. 16

Solution Video

Have any Doubt?



Suppose that a processor has access to three levels of memory. Level 1 contain 2000 words and has an access time of 0.02 msec. Level 2 contain 10,000 words and has an access time of 0.2 msec. Level 3 contains 20,000 words and has an access time of 2 msec. Assume that if a word to be accessed is in level 1, then processor access it directly. If it is in level 2 the word is first transferred to L_1 and then accessed by the processor. Similarly for L_3 the word is transferred to L_2 then to L_1 and then accessed. The hit ratio for level 1 is 0.65 and for level 2 is 0.45. The average access time (in μ sec) is _____.

475

Correct Option

Solution :

$$\begin{aligned} T_{\text{avg}} &= h_1 t_1 + (1 - h_1) t_2 (t_2 + t_3) + (1 - h_1) (1 - h_2) (t_3 + t_2 + t_1) \\ &= 0.65 \times 0.02 + 0.35 \times 0.45 \times 0.22 + 0.35 \times 0.55 \times 2.22 \\ &= 0.013 + 0.03465 + 0.42735 \\ &= 0.475 = 475 \mu\text{sec} \end{aligned}$$

 QUESTION ANALYTICS



Q. 17

 Solution Video

 Have any Doubt ?



A DMA module is transferring characters to memory using cycle stealing mode, from a device which is transmitting at a rate of 19200 bps. The rate at which processor is fetching the instruction is 2 million instructions per second (2 MIPS). Due to DMA, CPU slowed down by _____ (in %, upto 2 decimal places).

0.11 [0.10 - 0.12]

Correct Option

Solution :

0.11 [0.10 - 0.12]

DMA transfer character at rate of 19200 bpsec

8 bit = 1 character

So, 192000 bit = 2400 character

So, 1 sec = 2400 character

$$\begin{aligned} 1 \text{ character (X)} &= \frac{1}{2400} = 416.7 \times 10^{-6} \text{ sec} \\ &= 416.6 \mu\text{sec} \end{aligned}$$

Processor fetch rate is 2 MIPS

1 MIPS = 1 sec

$$1 \text{ Instruction (Y)} = \frac{1}{2 \times 10^6} = 0.5 \mu\text{sec}$$

$$\% \text{ slow down using DMA} = \left(\frac{Y}{X+Y} \right) \times 100$$

$$= \left(\frac{0.5}{416.6 + 0.5} \right) \times 100 = 0.11\%$$

Your Answer is 55

 QUESTION ANALYTICS



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OVERALL ANALYSIS COMPARISON REPORT **SOLUTION REPORT**

ALL(33) CORRECT(17) INCORRECT(7) SKIPPED(9)

Q. 1

Solution Video

Have any Doubt ?



The concept of pipelining improves performance by

- A Eliminating data hazards
- B Decreasing instruction latency
- C Decreasing the cache miss rate
- D Instruction level parallelism

Your answer is Correct

Solution :

(d)
 Instruction pipelining is a technique that implements a form of parallelism called instruction level parallelism with a single processor.
 It therefore allows faster CPU throughput.

QUESTION ANALYTICS



Q. 2

Solution Video

Have any Doubt ?

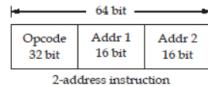


A hypothetical system which has 64 bit instructions and 16 bit address. If there are 102 and 256 1-address and 2-address instructions respectively, then how many 0-address (zero) instructions can be formulated?

- A $((2^{32} - 256 \times 2^{16}) - 102) \times 2^{16}$
- B $((2^{32} - 102) \times 2^{16} - 256) \times 2^{16}$
- C $((2^{32} - 256) \times 2^{16} - 102) \times 2^{16}$

Your answer is Correct

Solution :
 (c)



- $(2^{32} - 256)$ instruction left after 2-address instruction.
 - Number of 1-address instruction = $((2^{32} - 256) \times 2^{16})$.
 - Number of 0-address instruction = $((2^{32} - 256) \times 2^{16} - 102) \times 2^{16}$.
- So, option (c) is correct.

- D None of the above

QUESTION ANALYTICS



Q. 3

Solution Video

Have any Doubt ?



In the architecture of 8085 microprocessor match the following:

- | List-I | List-II |
|-------------------------------|-----------------------------|
| A. Processing unit | 1. Interrupt |
| B. Instruction unit | 2. General purpose register |
| C. Storage and Interface unit | 3. ALU |
| | 4. Timing and Control |

Codes:

- | A | B | C |
|-------|---|---|
| (a) 4 | 1 | 2 |
| (b) 3 | 4 | 2 |
| (c) 2 | 3 | 1 |
| (d) 1 | 2 | 4 |

- A a

- B b

Your answer is Correct

Solution :

(b)
 Processing unit → Arithmetic logical unit
 Instruction unit → Timing and signal
 Storage and interface unit → General purpose register.

C c

D d

QUESTION ANALYTICS +

Q. 4

Solution Video

Have any Doubt ?



Which of the following is correct statement?

- A** In memory - mapped I/O, the CPU can manipulate I/O data residing in interface registers that are used to manipulate memory words.

Your answer is Wrong

- B** The isolated I/O method isolates memory and I/O addresses so that memory address range is not affected by interface address assignment.

Correct Option

Solution :

(b)

- **Isolated Input/Output:** This configuration uses the common bus and common address space but different control signal for both memory and input/output, so that memory address range is not affected by interface address assignment.
- **MemoryMappedInput/Output:** This configuration uses common bus and common control signals but unique address space.

- C** In asynchronous serial transfer of data the two units share a common clock.

- D** In synchronous serial transmission of data the two units have different clocks.

QUESTION ANALYTICS +

Q. 5

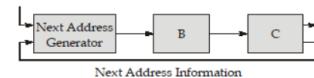
Solution Video

Have any Doubt ?



The general configuration of the microprogrammed control unit is given below:

External Conditions



What are blocks B and C in the diagram respectively?

- A** Block address register and cache memory

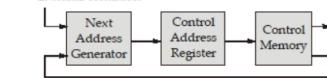
- B** Control address register and control memory

Correct Option

Solution :

(b)

External condition



- C** Branch register and cache memory

- D** Control address register and random access memory

QUESTION ANALYTICS +

Q. 6

Solution Video

Have any Doubt ?



Match List-I (Addressing Mode) with List-II (Location of operand) and select the correct answer:

List-I

- A. Implied
- B. Immediate
- C. Register
- D. Register Indirect

List-II

1. Registers which are in CPU
2. Register specifies the address of the operand.
3. Specified in the address field of an instruction
4. Specified implicitly in the definition of instruction

Codes:

A B C D

- | | | | | |
|-----|---|---|---|---|
| (a) | 4 | 3 | 1 | 2 |
| (b) | 4 | 1 | 3 | 2 |
| (c) | 4 | 2 | 1 | 3 |
| (d) | 4 | 3 | 2 | 1 |

a

Your answer is Correct

Solution :

- (a) Implied addressing mode: Specified implicitly in the definition of instruction.
- Immediate addressing mode: Specified in the address field of an instruction.
- Register addressing mode: Registers which are in CPU.
- Register indirect addressing mode: Register specifies the address of the operand.

b

c

d

QUESTION ANALYTICS



Q. 7

▶ Solution Video

Have any Doubt ?



Consider 16 way set associative cache of 64 KB with a block size 32 B. Cache memory is managed with a 32 bit address. In the cache controller each tag is comprising of 1 valid bit, 1 modified bit and 3 replacement bits. How much space is required in the cache controller to hold the tag information in bits

A 51200

Your answer is Correct

Solution :

(a)

$$\text{Number lines} = \frac{64\text{K}}{32} \Rightarrow 2^{11}$$

$$\text{Number sets} = \frac{2^{11}}{2^4} \Rightarrow 2^7$$



$$\begin{aligned}\text{Tag memory size} &= S \times P \times \# \text{ tag bits} \\ &= 128 \times 16 \times 25 = 51200 \text{ bits}\end{aligned}$$

B 46000

C 37600

D 45379

QUESTION ANALYTICS



Q. 8

▶ Solution Video

Have any Doubt ?



Match List-I with List-II and select the correct answer using the codes given below the lists:

List-I

- | | |
|-----------------------------|--------------------------------|
| A. To access constant value | List-II |
| B. Global variable | 1. Indirect addressing mode |
| C. Pointer | 2. Direct addressing mode |
| D. Array | 3. Based index addressing mode |
| Codes: | 4. Immediate addressing mode |

A B C D

- (a) 1 2 3 4
- (b) 2 3 4 1
- (c) 4 2 1 3
- (d) 2 3 1 4

a

b

c

Your answer is Correct

Solution :

(c)

- To access constant value Immediate addressing mode is used.
- Global variable are using Direct addressing mode.
- Pointer are implemented using Indirect addressing mode.
- Array are implemented using Based index addressing mode.

d

QUESTION ANALYTICS



Consider we have the following values in the given memory locations:

Location	Value
1000	1300
1100	1200
1200	800
1300	1200

Consider that the index register R1 store 200 and is always implicitly used for the indexed addressing mode. What datum is loaded into the accumulator if the instruction is "LOAD 1000" for direct addressing mode, indirect addressing mode and base (indexed) addressing modes respectively.

A 1200, 800, 1100

B 1200, 800, 1300

C 1100, 1200, 800

D 1300, 1200, 800

Your answer is **Correct**

Solution :

(d)

Instruction : "Load 1000"

Direct Addressing Mode: Since the content of location '1000' is '1300'. Hence, 1300 will be loaded.

Indirect Addressing Mode: The content of location '1000' is '1300'. The content of memory location '1300' is '1200'. Hence, 1200 will be loaded.

Base (Indexed) Addressing Mode: $[1000 + 200] \Rightarrow [1200]$. The content of memory location '1200' is 800.

 QUESTION ANALYTICS

+

Assume that ADD x, y, z ; denotes $x \leftarrow y + z$, SUB x, y, z ; $x \leftarrow y - z$ and MUL x, y, z ; Consider the following assembly code.

I_1 : SUB R_1, R_2, R_3 ;

I_2 : ADD R_2, R_1, R_3 ;

I_3 : ADD R_3, R_1, R_2 ;

I_4 : SUB R_1, R_2, R_3 ;

Find the number of RAW dependencies in the above assembly code.

A 2

Correct Option

Solution :

(a)

There are 2 True-data dependencies such as $I_1(R_1) \rightarrow I_2(R_1)$, and $I_2(R_2) \rightarrow I_3(R_2)$.

B 5

Your answer is **Wrong**

C 3

D 6

 QUESTION ANALYTICS

+



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Q. 11
[▶ Solution Video](#)
[Have any Doubt ?](#)


A program consists of mainly different types of instructions. The table for instruction type, Cycle Per Instruction (CPI) and frequency of such instructions in the program is given below:

Type	CPI	Frequency (%)
ALU	1	35
Branch	2	12
LOAD/STORE	3	28
MEMORY referring	4	25

The average CPI of the program is _____. (Upto 2 decimal places)

2.43 [2.40 - 2.45]

Your answer is **Correct** 2.43

Solution :

2.43 [2.40 - 2.45]

$$\text{Average CPI} = \sum \text{CPI}_i \times \text{Frequency}_i$$

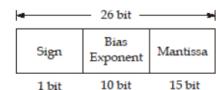
$$= 1 \times 0.35 + 2 \times 0.12 + 3 \times 0.28 + 4 \times 0.25$$

$$= 0.35 + 0.24 + 0.84 + 1.0 = 2.43$$

QUESTION ANALYTICS


Q. 12
[▶ Solution Video](#)
[Have any Doubt ?](#)


Consider the following hypothetical floating point format.



The bias value in the floating point format when the formt uses excess code form is _____.

512

Correct Option

Solution :

512

$$\text{Bias exponent in representation} = 10 \text{ bit}$$

$$= 2^{10} = 1024$$

So, excess code form uses the half of the range as a bias i.e. 512.

QUESTION ANALYTICS


Q. 13
[▶ Solution Video](#)
[Have any Doubt ?](#)


A process takes 20 ns on a cache hit and 400 μ s on a cache miss to read an instruction. Approximately 20% of the time read request is found in the cache. Then the average access time is ____ μ s.
 (Upto 3 decimal places)

320.004 [320.000 - 320.010]

Correct Option

Solution :

320.004 [320.000 - 320.010]

$$T_{\text{read miss}} (T_m) = 400 \mu\text{s}$$

$$T_{\text{read hit}} (T_h) = 20 \text{ ns}$$

$$\text{Hit ratio (h)} = 0.2$$

$$T_{\text{avg}} = 0.2 \times 0.02 \mu\text{s} + 0.8 \times 400 \mu\text{s}$$

$$= 0.004 \mu\text{s} + 320 \mu\text{s}$$

$$= 320.004 \mu\text{s}$$

Your Answer is 360

QUESTION ANALYTICS


Q. 14
[▶ Solution Video](#)
[Have any Doubt ?](#)


A device with data transfer rate of 20 KBps is connected to a CPU byte wise. Assume byte transfer time between the device and CPU is negligible and interrupt overhead is 20 μ sec. The performance gain under interrupt mode over program controlled mode is _____. (Upto 1 decimal place)

Solution :
2.5 [2.5 - 2.5]

$$\begin{aligned}20 \text{ KB} &= 1 \text{ sec} \\1 \text{ B} &=? \\ \text{Transfer time of 1 byte} &= \frac{1}{20 \text{ K}} = 0.05 \text{ ms} \\ET_{\text{Prog. I/O}} &= 0.05 \text{ ms} \\ET_{\text{INT - I/O}} &= 20 \mu\text{sec} \\ \text{Performance gain} &= \frac{ET_{\text{Prog. I/O}}}{ET - \text{I/O}} = \frac{0.05 \text{ ms}}{20 \mu\text{sec}} = 2.5\end{aligned}$$

QUESTION ANALYTICS

Q. 15

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider a non-pipelined processor with a clock rate of 5 GHz and an average CPI of 5. The processor is upgraded to 5 stage pipeline processor and clock rate reduced to 4 GHz. The speedup achieved in the pipelined processor is _____.

4

Your answer is **Correct4**

Solution :
4

- Non pipelined processor $= 5 \times \frac{1}{5 \text{ GHz}} = 1 \text{ ns}$
 - Pipelined processor $= 1 \times \frac{1}{4 \text{ GHz}} = 0.25 \text{ ns}$
- $$\text{Speedup} = \frac{1 \text{ ns}}{0.25 \text{ ns}} = \frac{1}{0.25} = 4$$

QUESTION ANALYTICS

Q. 16

[▶ Solution Video](#)[Have any Doubt ?](#)

A micro programmed control unit supporting 450 instructions. Each instruction takes 20 micro operations. If 18 flags and 85 control signal are supported then the size of control words of vertical micro programmed control unit is _____ bits.

26

Your answer is **Correct26**

Solution :
26
Control word:

Flags	Control signal	Control word offset
$\log_2 18$ = 5 bit	$\log_2 85$ = 7 bit	$\log_2 (450 \times 20)$ = 14 bit

$$\begin{aligned}\text{Length of control word} &= \text{Flag} + \text{Control signal} + \text{Address} \\&= 5 \text{ bit} + 7 \text{ bit} + 14 \text{ bit} = 26 \text{ bit}\end{aligned}$$

QUESTION ANALYTICS

Q. 17

[▶ Solution Video](#)[Have any Doubt ?](#)

A 4-way set associative cache has lines of 32-byte and a total cache size of 16 KB. Which of the 256 MB main memory block is mapped on to the set '50' of the cache memory?

A $(CFED09B)_{16}$

B $(FB3DC2C)_{16}$

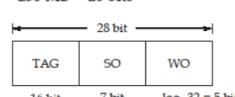
Correct Option

Solution :
(b)

$$\text{Number of lines} = \frac{16 \text{ KB}}{32 \text{ B}} = \frac{2^{14}}{2^5} = 2^9$$

$$\text{Number of sets} = \frac{2^9}{2^2} = 2^7$$

Physical address size = 256 MB = 28 bits



Total set will be from 0 to 127 (using 7 bits).

In option (b)

$$(FB3DC2C)_{16} = \underbrace{FB}_{16 \text{ bit}} \underbrace{3D}_{7 \text{ bit}} \underbrace{01100100}_{5 \text{ bit}} C$$

LA
set
WO
↓
It's decimal value is 50

Hence option (b) is correct.

C $(FDE1400B)_{16}$

D $(CFED109B)_{16}$

QUESTION ANALYTICS +

Q. 18

Solution Video

Have any Doubt?



A 1-address machine and 2-address machine executes the instructions to compute $X = (A + B \times C) / (D - E \times F)$. The instructions available for 1-address machine is LOAD, STORE, ADD, SUB, MUL, and DIV. The instructions available for 2-address machine is MOV, ADD, SUB, MUL and DIV. How many extra instructions required by 1-address machine compared to 2-address machine?

A 2

Your answer is Correct

Solution :

(a)

$$X = (A + B \times C) / (D - E \times F)$$

1-Address Machine:

1. LOAD E
2. MUL F
3. STORE T
4. LOAD D
5. SUB T
6. STORE F
7. LOAD B
8. MUL C
9. ADD A
10. DIV T
11. STORE X

So, total 11 instruction in 1-address machine.

2-Address Machine:

1. MOV R₀, E
2. MUL R₀, F
3. MOV R₁, D
4. SUB R₁, R₀
5. MOV R₀, B
6. MUL R₀, C
7. ADD R₀, A
8. DIV R₁, R₀
9. MOV X, R₀

Total 9 instructions in 1-address machine.

So, 2 extra instruction is required in 1-address machine.

B 5

C 8

D 11

QUESTION ANALYTICS +

Q. 19

Solution Video

Have any Doubt?



Suppose a system has 2-level cache design L_1 and L_2 . The miss penalty from L_2 cache to memory is 300 cycles and hit time of L_2 cache is 100 cycles. In total 900 memory reference only 200 miss in L_1 and 80 miss in L_2 cache. What is the average stall per instruction if there are 3 memory reference per instruction?

A 146.66 cycles

Correct Option

Solution :

(a)

3 memory reference \rightarrow 1 instruction
900 memory reference \rightarrow ? instruction

$$\text{Number of instruction} = \frac{900}{3} = 300$$

$$\begin{aligned} \text{Number of memory stalls/instruction} &= \left[\frac{\text{Number of miss } L_1}{\text{Number of instruction}} \times \text{Hit } L_2 \right] \\ &\quad + \left[\frac{\text{Number of miss } L_2}{\text{Number of instruction}} \times \text{Miss penalty } L_2 \right] \\ &= \left[\frac{200}{300} \times 100 \right] + \left[\frac{80}{300} \times 300 \right] \\ &= \left[\frac{200}{3} + 80 \right] \simeq 146.66 \text{ cycles} \end{aligned}$$

B 138.37 cycles

C 89.45 cycles

D 97.44 cycles

QUESTION ANALYTICS



Q. 20

Solution Video

Have any Doubt?



Consider a 5 GHz clock frequency processor used to execute the following program segment on a pipelined processor.

Instruction	Size (in words)	Meaning
$I_1 : \text{MOV } r_0, [300]$	3	$r_0 \leftarrow M[300]$
$I_2 : \text{MOV } r_1, @ 400$	4	$r_1 \leftarrow M[[400]]$
$I_3 : \text{MUL } r_0, r_1$	2	$r_0 \leftarrow r_0 * r_1$
$I_4 : \text{MOV } r_1, @ 500$	4	$r_2 \leftarrow M[[500]]$
$I_5 : \text{DIV } r_0, r_2$	1	$r_0 \leftarrow r_0 / r_2$

Each memory references and ALU operation consumes 3 cycles and 1 cycles respectively. The total time required to complete the program execution is

A 8.4 ns

B 7.33 ns

Your answer is Wrong

C 15.62 ns

D 11.8 ns

Correct Option

Solution:
(d)

IF	ID	OF	PD and WB
$I_1 : 1 \text{ memory reference}$	2 memory reference	1 memory reference	—
$I_2 : 1 \text{ memory reference}$	3 memory reference	2 memory reference	—
$I_3 : 1 \text{ memory reference}$	1 memory reference	—	1 ALU operation
$I_4 : 1 \text{ memory reference}$	3 memory reference	2 memory reference	—
$I_5 : 1 \text{ memory reference}$	—	—	1 ALU operation

$$\begin{aligned} \text{Total Execution Time} &= (\text{Number of memory reference} \times 3 \text{ cycles} + \text{Number of ALU} \\ &\quad \text{operation} \times 2 \text{ cycles}) \times \text{cycle time} \\ &= (19 \times 3 + 2 \times 1) \times \frac{1}{5 \text{ GHz}} \\ &= \frac{59}{5} \text{ ns} = 11.8 \text{ ns} \end{aligned}$$

QUESTION ANALYTICS



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Q. 21

Solution Video

Have any Doubt ?



Consider the following sequence of instructions executed on a 5 stage pipelined processor. Data dependency is resolved by operand forwarding techniques. MOV instruction output present in 4th stage and ALU operation output present in 3rd stage.

I_1 : MOV R_0 , M[300]
 I_2 : SUB R_0 , R_1
 I_3 : ADD R_2 , R_1
 I_4 : MOV R_3 , @ 200
 I_5 : MUL R_2 , R_3

What is the number of cycles required to complete the program? (Assume each stage takes 1 cycle time)

A 8

B 9

C 10

D 11

Your answer is Wrong

Correct Option

Solution :
 (d)

	1	2	3	4	5	6	7	8	9	10	11
I_1	IF	ID	EX	MM	WB						
I_2	IF	ID	ID	EX	MM	WB					
I_3		IF	IF	ID	EX	MM	WB				
I_4				IF	ID	EX	MM	WB			
I_5					IF	ID	ID	EX	MM	WB	

Total 11 cycles are required.

QUESTION ANALYTICS



Q. 22

Solution Video

Have any Doubt ?



Consider two different implementations of the same instruction set architecture, P_1 and P_2 . Processor P_1 runs on a clock rate of 1.5 GHz and P_2 runs on 2.5 GHz. There are four classes of instructions A, B, C and D. The CPI's of each implementation are given in the following table.

	Class A	Class B	Class C	Class D
CPIs of P_1	1	2	3	4
CPIs of P_2	2	2	2	2
Frequency	10%	10%	50%	30%

Given a program with 10^6 instructions divided into 4 classes according to the frequencies in the above table. Choose the correct statement from the following.

A P_1 is faster than P_2

B P_2 is faster than P_1

Your answer is Correct

Solution :
 (b)

$$\begin{aligned}
 P_1 \text{ CPU time} &= \frac{[1 \times 0.1 + 2 \times 0.1 + 3 \times 0.5 + 4 \times 0.3]}{1.5 \times 10^9} \\
 &= 2 \times 10^{-9} \text{ sec} = 2 \text{ nsec} \\
 P_2 \text{ CPU time} &= \frac{[2 \times 0.1 + 2 \times 0.1 + 2 \times 0.5 + 2 \times 0.3]}{2.5 \times 10^9} \\
 &= 0.8 \times 10^{-9} \text{ sec} = 0.8 \text{ nsec} \\
 \therefore P_2 &\text{ is faster than } P_1 \text{ processor.}
 \end{aligned}$$

C P_1 is same as P_2

D None of these

QUESTION ANALYTICS



Q. 23

Solution Video

Have any Doubt ?



Consider the following floating point format.

Sign(s)	Exponent (E)	Mantissa (M)
1 bit	8 bits	23 bits

The decimal number (- 48.625) has following hexadecimal representation with normalization and rounding off

A C4228000

B 42428000

C C2428000

Correct Option

Solution :

(c)

The decimal number is = (- 48.625)

Binary number representation of (- 48.625)

Normalization form = 1.10000101×2^5

Mantissa field is = 100001010000000000000000

Exponent field is = $5 + 127 = 132 = (1000100)_2$

Value in given format is

Sign(s)	Exponent (E)	Mantissa (M)
1	100 00100	100 00101000000000000000

So the hexadecimal representation is $(C2428000)_{16}$.

D None of these

QUESTION ANALYTICS



Q. 24

Solution Video

Have any Doubt ?



A set associative cache consists of 128 lines divided into 8 lines set. If main memory contains 4 K blocks of 1024 words each, then the size of set, tag and word bits are respectively.

A (5, 7, 10)

B (4, 8, 10)

Correct Option

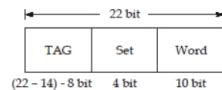
Solution :

(b)

$$\text{Number of sets} = \frac{128}{8} = 2^4 = 4 \text{ bits}$$

Number of blocks in MM = 4 K = 2^{12}

$$\begin{aligned}\text{Total MM size} &= 2^{12} \times 1024 \text{ words} \\ &= 2^{12} \times 2^{10} \text{ words} \\ &= 2^{22} \text{ words}\end{aligned}$$



$$\begin{aligned}\text{TAG bits} &= \text{Total} - (\text{Set} + \text{Word}) \text{ bit} \\ &= 22 - (10 + 4) = 8 \text{ bit}\end{aligned}$$

C (8, 4, 10)

Your answer is Wrong

D (4, 9, 10)

QUESTION ANALYTICS



Q. 25

Have any Doubt ?



A micro-instruction format has micro-ops field which is divided into three subfields F1, F2, F3 each having seven distinct micro-operations, condition field CD for four status bits, branch field BR having four options used in conjunction with address field ADF. The address space is of 128 memory locations. The size of micro-instruction is

A 17 bits

B 20 bits

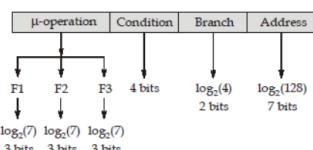
C 22 bits

Your answer is Correct

Solution :

(c)

μ -instruction format:



Size of one micro-instruction = $(3 + 3 + 3) + 4 + 2 + 7 = 22 \text{ bits}$

So, option (c) is correct answer.

32 bits

QUESTION ANALYTICS

Q. 26

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider the following statements:

- S_1 : Hardwired control unit design is not suitable in design and testing places.
- S_2 : Horizontal micro programmed control unit design is implemented using sum of product expression on a flip-flops.
- S_3 : Vertical micro programmed control unit allows high degree of the parallelism with respect to horizontal μ -program control unit.
- S_4 : In the control unit design control signals are represented in a encoding format/decoding format/SOP format.

Which of the following statements are true?

A S_1 only S_2 only**B** S_1 and S_4 , S_3 only**C** S_1 and S_4 only**D** S_1 , S_2 and S_4

Correct Option

Solution :

(d)

- Hardwired control unit design is not suitable in design and testing places because small modification change the working of whole system. So, we have to design again.
- Horizontal control unit design is implemented using sum of product expression on a flip-flops.
- Vertical micro programmed control unit allows low degree of the parallelism, whereas horizontal micro programmed control unit allows high degree of the parallelism.
- In the control unit design control signals are represented in a encoding format/decoding format/SOP format.

QUESTION ANALYTICS

Q. 27

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider the following statements:

- (i) To increment or decrement its value Program Counter (PC) does not require ALU operation.
- (ii) Memory conflict in structural dependency can be minimized using operand forwarding technique.
- (iii) Delayed branch technique is used to optimize the control dependency.

Which of the following is true?

A (i) - false, (ii) - true, (iii) - true**B** (i) - false, (ii) - false, (iii) - true

Your answer is Wrong

C (i) - true, (ii) - false, (iii) - false**D** (i) - true, (ii) - false, (iii) - true

Correct Option

Solution :

(d)

- (i) is true, it is logically done.
- (ii) is false, structural dependency resolved using re-naming.
- (iii) Delayed branch re-arranges code to reduce control dependency.

QUESTION ANALYTICS

Q. 28

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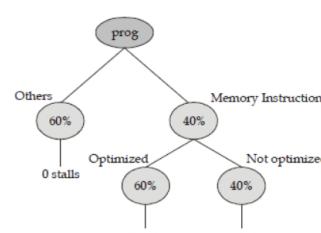
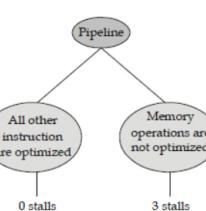
Consider 5 stage pipeline which allows overlapping of all the instructions except memory based instructions. Penalty of the memory based instruction is 3 cycles. In the program 40% memory instructions are present, among them 60% are optimized. What is the average instruction execution time?
(Assume the pipeline cycle time as 8 ns)

A 9.76 ns**B** 11.84 ns

Your answer is Correct

Solution :

(b)



Number of stalls/Instruction = $(0.4 \times 0.4 \times 3) = 0.48$
 Average instruction ET = $(1 + \# \text{ stalls} / \text{Instruction}) \times \text{Cycle time}$
 $= (1 + 0.48) \times 8 \text{ ns} = 11.84 \text{ ns}$

C 14.84 ns

D 13.76 ns

QUESTION ANALYTICS



Q. 29

Solution Video

Have any Doubt?



Consider a disk drive with the following specifications. 16 surfaces, 128 tracks/surfaces, 256 sectors/track, 512 B/sector, rotations speed 3600 rpm. The disk is operated in cycle stealing mode whereby whenever one byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 5 byte word from the memory in each DMA cycle. Memory cycle time is 50 μsec . The maximum percentage of time that the CPU gets blocked during DMA operation is _____. (Upto 2 decimal places)

28.40 [28.30 - 28.50]

Correct Option

Solution :

28.40 [28.30 - 28.50]

3600 revolution \rightarrow 1 min (60 sec)

$$1 \text{ revolution} \rightarrow \frac{60}{3600} = 16.6 \text{ msec}$$

1 revolution time \rightarrow 1 track data

? time \rightarrow 1 byte

$$\Rightarrow \frac{16.6 \text{ ms}}{256 \times 512} = 0.126 \text{ ms} = 126 \mu\text{sec}$$

$$\Rightarrow X = 126 \mu\text{sec}$$

1 byte word, so word size = 1 byte prepare for 1 word either for read/write.

$$Y = 50 \mu\text{sec}$$

$$\% \text{ time CPU blocked} = \left(\frac{Y}{X+Y} \right) \times 100 = 28.4$$

QUESTION ANALYTICS



Q. 30

Solution Video

Have any Doubt?



Consider the machine with a byte addressable main memory of 2^{16} byte, block size of 16 byte and a 2 way set associative mapped cache having 2^{10} lines. Suppose there are two bytes in main memory i.e. first byte address $[E\ 0\ F]_{16}$ and second byte address $[E\ 2\ 0\ 8]_{16}$ respectively then the difference of the set value (in decimal) between given two bytes i.e. (SET value of second byte – SET value of 1st byte) is _____.

31

Your answer is Correct31

Solution :

31

Block size = 16 byte = 2^4 byte = 4 bits

Blocks in main memory = 2^{10}

$$\text{So number of sets} = \frac{2^{10}}{2^4} = 2^9 \Rightarrow 512 \text{ sets}$$

Number of bits in physical address = 2^{16} byte \rightarrow 16 bits



SET value₁ = 00000001 = Decimal value = $(1)_{10}$

SET value₂ = 00010000 = Decimal value = $(32)_{10}$

$$\begin{aligned} \text{Difference} &= \text{SET}_2 - \text{SET}_1 \\ &= 32 - 1 = (31)_{10} \end{aligned}$$

QUESTION ANALYTICS



Item 21-30 of 33

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Kunal Jha

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Q. 31
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Consider the following program segment:

Instruction	Meaning	Size (words)
I_1 LOAD $r_0, 500$	$r_0 \leftarrow [500]$	2
I_2 MOV r_1, r_0	$r_1 \leftarrow [r_0]$	1
I_3 ADD r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_4 INC r_0	$r_0 \leftarrow r_0 + 1$	1
I_5 INC r_1	$r_1 \leftarrow r_1 + 1$	1
I_6 ADD r_0, r_1	$r_0 \leftarrow r_0 + r_1$	1
I_7 Store r_1, r_0	$M[r_1] \leftarrow r_0$	2
I_8 Halt	Stop	1

 Assume that memory is word addressable with word size 32 bits. Program is loaded into memory location $(3001)_{10}$ onwards. The value of PC at the end of execution of above program is _____.

3010

 Your answer is **Correct3010**
Solution :

3010

Word addressable storage

3001 – 3002

3003

3004

3005

3006

3007

3008 – 3009

3010

Valid program counter value after program is 3010.

QUESTION ANALYTICS

Q. 32
[▶ Solution Video](#)
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Assume that five instructions of the loop body starting memory locations are 1000, 1004, 1008, 1012 and 1016 respectively. Assume each instruction takes 4 bytes of memory. The offset needed to return to the loop are _____.

-20

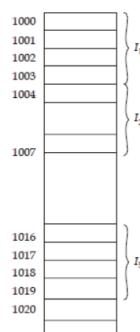
 Your answer is **Correct-20**
Solution :

-20

 Suppose 5 instructions are I_1, I_2, I_3, I_4 and I_5 .

PC value at the end of loop = 1020

Offset = -20


QUESTION ANALYTICS

Q. 33
[▶ Solution Video](#)
[Have any Doubt ?](#)


Consider a cache consisting of 128 blocks of 16 words each. Main memory has 64 K words and given main memory is 16 bit addressable. The difference between tag memory size of Associative Mapping and Direct Mapping is _____ (bits).

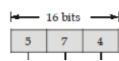
896

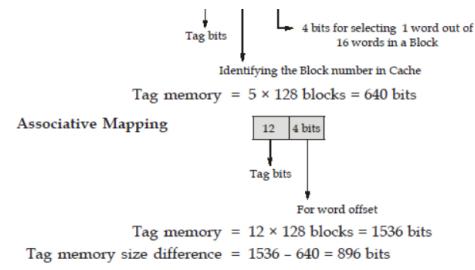
Correct Option

Solution :

896

Direct Mapping





QUESTION ANALYTICS

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