

Electronics and Communication Engineering And CSE



Digital Electronics
Digital Logic
Lecture 01



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Topics to be Covered

1. Logic Gates

2. Questions

NOT GATE

AND GATE

OR GATE

NAND GATE

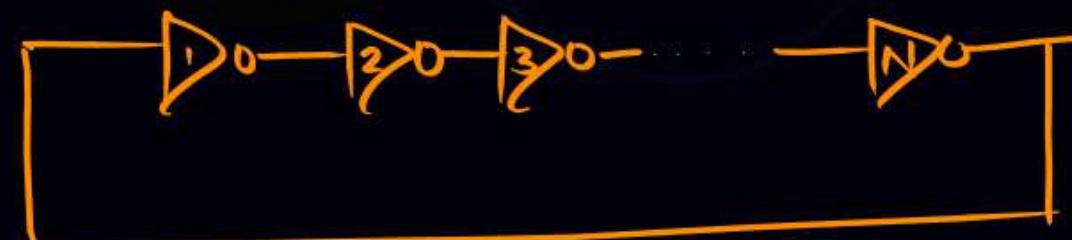
NOR GATE

X-OR GATE

X-NOR GATE

NOT GATE

When odd no. of NOT GATE in loop: \rightarrow



N \rightarrow odd

$$T = 2N \times \tau_{pd}$$

$\tau_{pd} \rightarrow$ propagation delay of NOT GATE

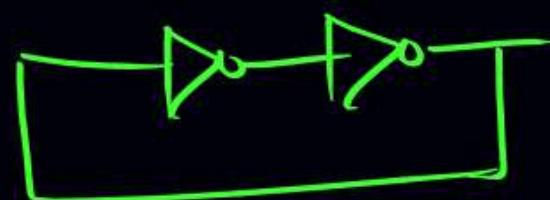
$$f = \frac{1}{T}$$

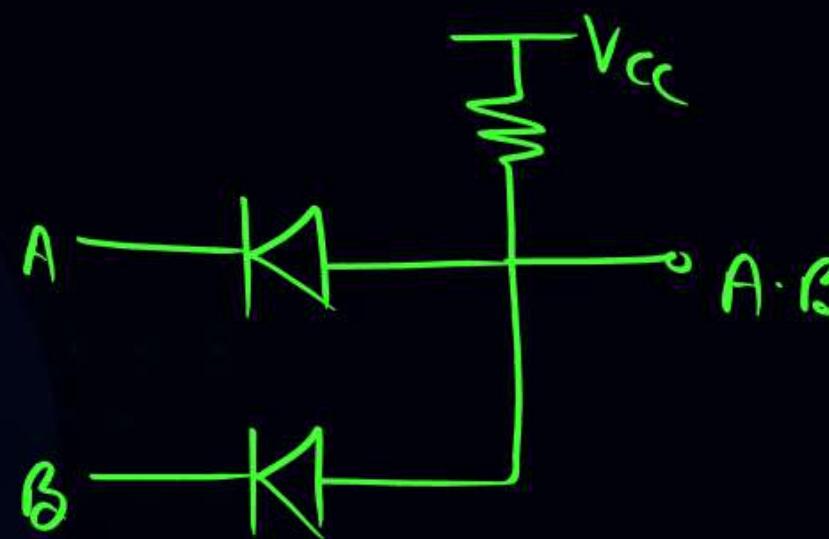
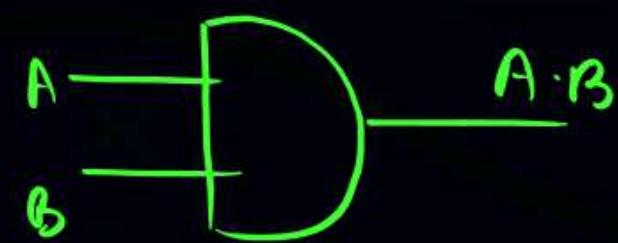
$f = \frac{1}{2N \times \tau_{pd}}$

$$f = \frac{1}{2[\text{sum of delay of all the NOT GATE}]}$$

When Even no. of NOT GATE in Loop:-

↳ Basic memory element

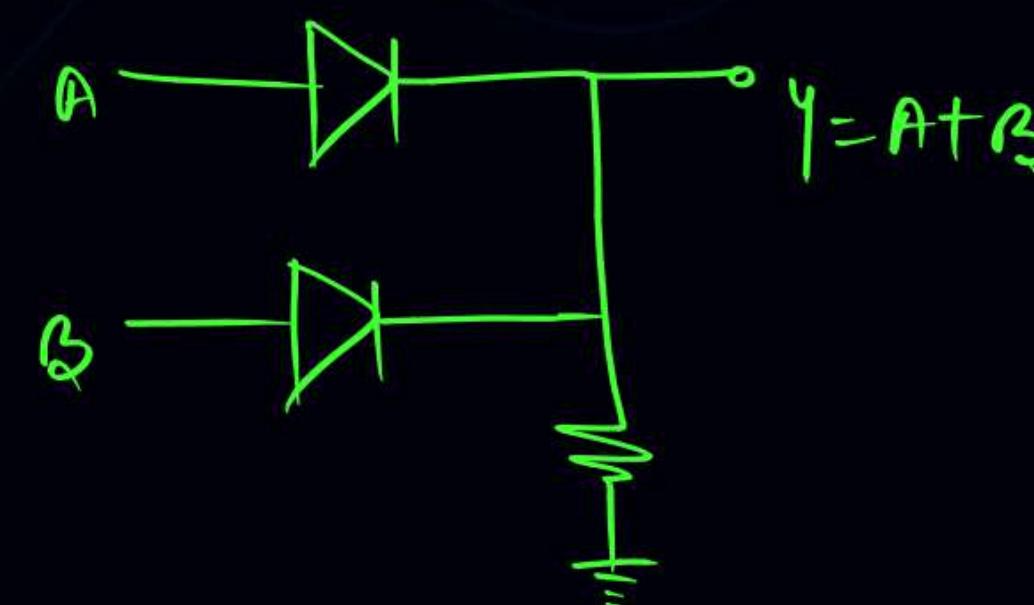


AND GATE.

A	B	$Y = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE

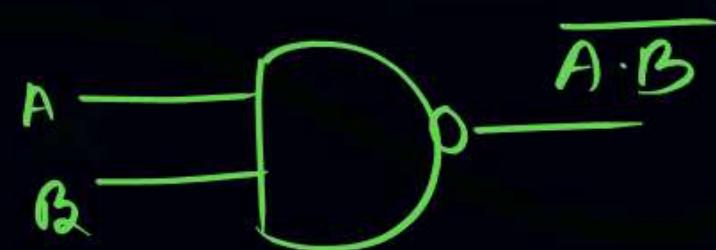
A	B	$y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1



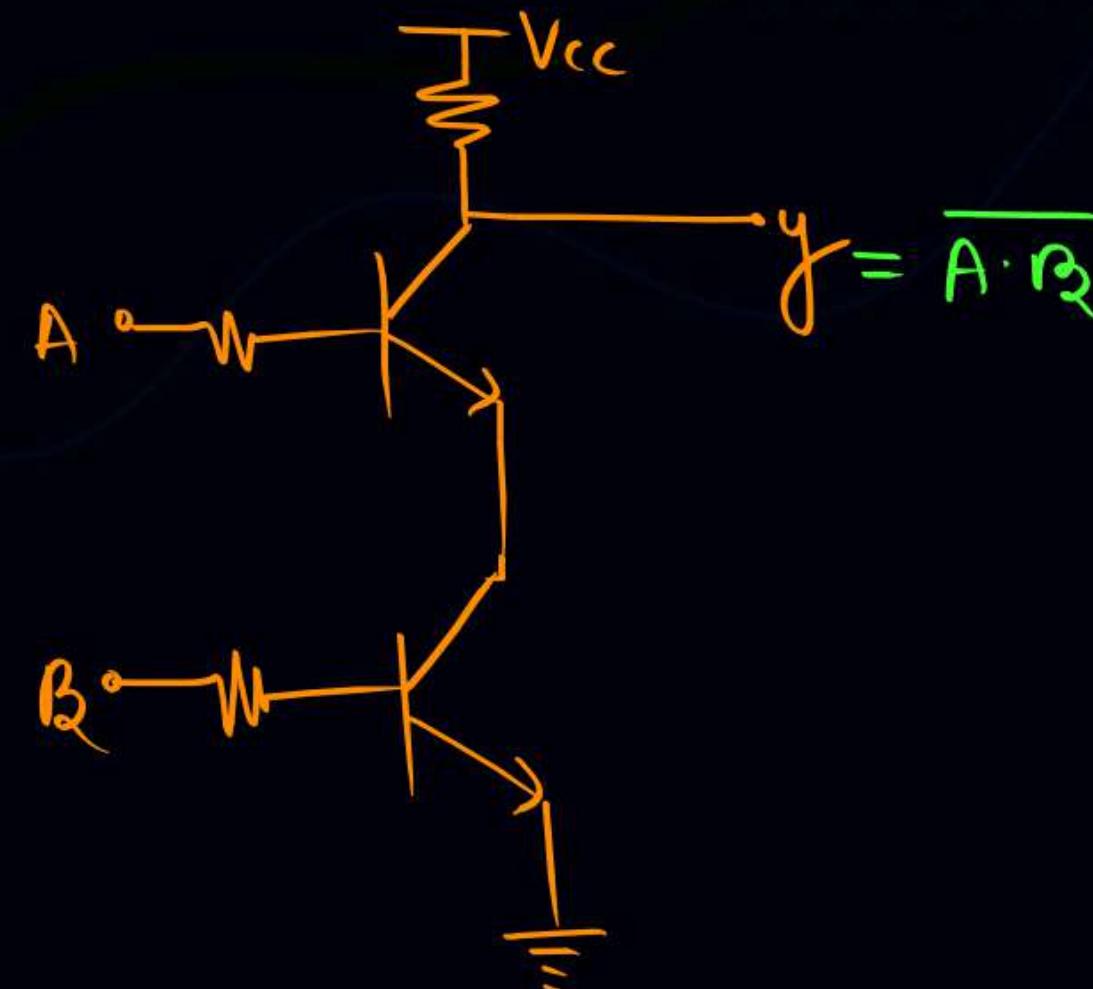
NOTE :-

- 1> When ever any Logic are designed by  Transistor-Transistor Logic Then floating terminal by default works as HIGH.
- 2> When ever any Logic are designed by  Emitter coupled Logic, then floating terminal works as LOW
- 3> ECL is the fastest among all the Logic family

④ NAND GATE :-



A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

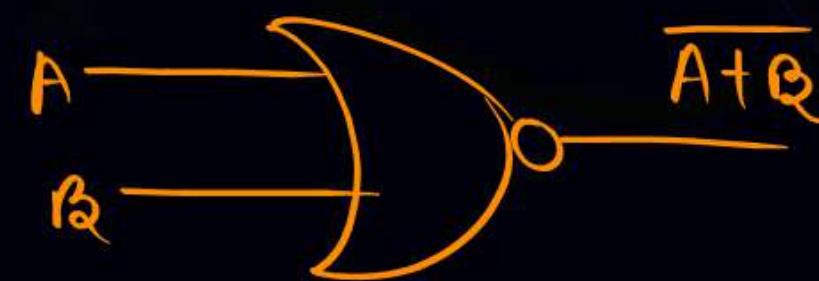


NAND }
NOR } → commutative law ✓

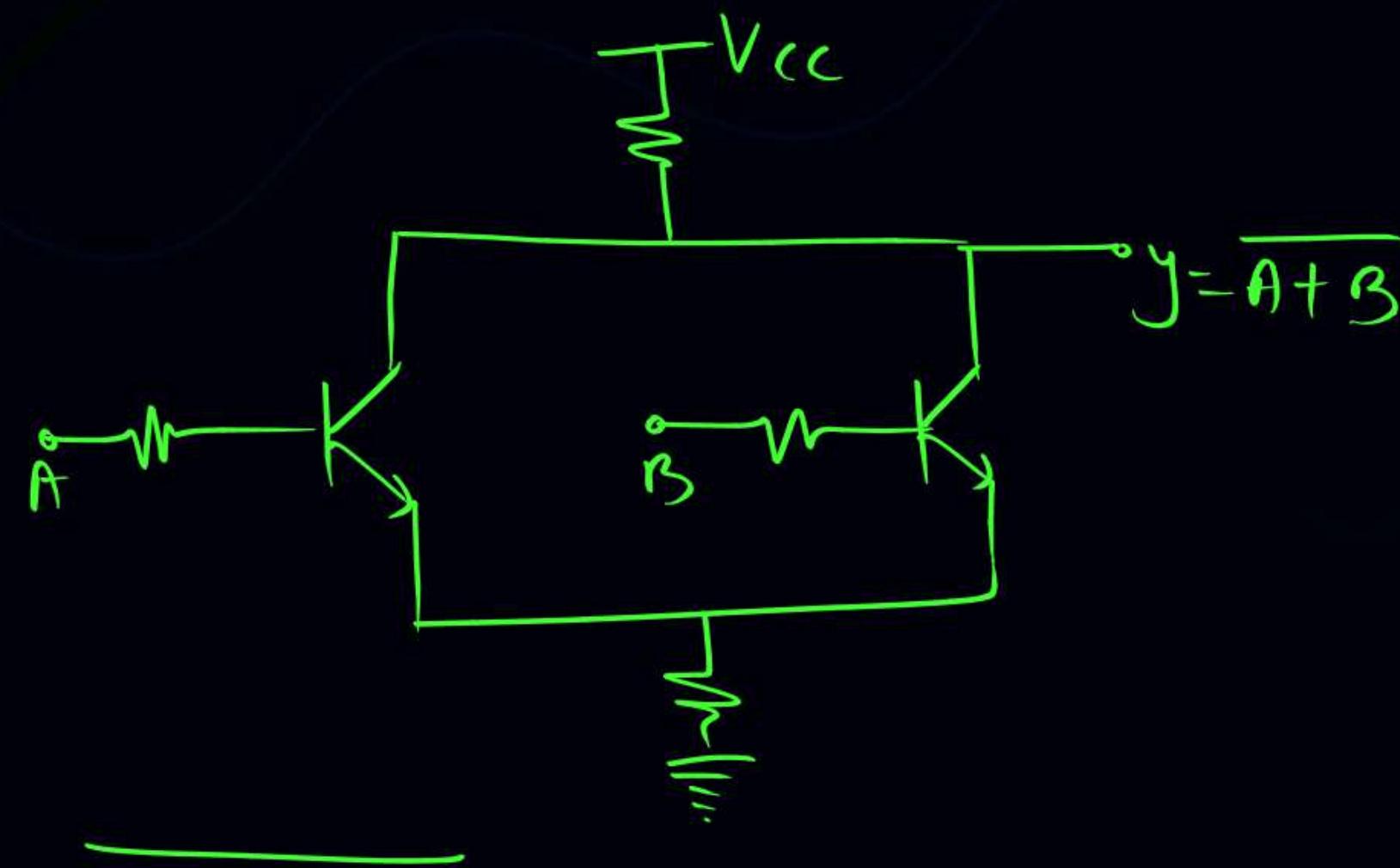
Associative Law ✗

$$\overline{(\overline{A}B)}C \neq \overline{A \cdot (\overline{B}C)}$$

⑤ NOR GATE :-



A	B	$y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



$$\overline{(A+B)} + C \neq A + (\overline{B+C})$$

Universal Logic

① $\overline{A \cdot B} = \overline{A} + \overline{B}$

② $\overline{A+B} = \overline{A} \cdot \overline{B}$

③ $\overline{\overline{A} \cdot B}$

④ $A \cdot \overline{B}$

⑤ $\overline{A} + B$

⑥ $A + \overline{B}$

⑦ MUX

⑧ Decoder + OR logic

⑥ X-OR GATE :



$$A \oplus B = \begin{cases} \bar{A}B + A\bar{B} \\ (A+B)(\bar{A}+\bar{B}) \end{cases}$$

$$A \oplus A = 0$$

$$A \oplus 0 = A$$

$$A \oplus \bar{A} = 1$$

$$A \oplus 1 = \bar{A}$$

A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

$$A \oplus A \oplus A \dots \oplus A = \begin{cases} 0 & \text{even no. of "A"} \\ A & \text{odd no. of "A"} \end{cases}$$

$$A \oplus B \oplus C = \sum m(1, 2, 4, 7)$$

X-OR expression will be always minimized expression.

X-NOR GATE :-



$$A \odot B = \begin{cases} \bar{A}\bar{B} + AB \\ (\bar{A}+B)(A+\bar{B}) \end{cases}$$

$$A \odot A = 1$$

$$A \odot 1 = A$$

$$A \odot \bar{A} = 0$$

$$A \odot 0 = \bar{A}$$

A	B	$A \odot B$
0	0	1
0	1	0
1	0	0
1	1	1

$$A \odot B = \overline{A \oplus B}$$

$$A \odot B \odot C \odot D = \overline{A \oplus B \oplus C \oplus D}$$

$$(A \odot B) \odot C = A \oplus B \oplus C$$

$$A \odot B = \bar{A} \odot \bar{B} = \overline{A \oplus B} = \bar{A} \oplus \bar{B} = A \oplus \bar{B}$$

$$A \oplus B = \bar{A} \oplus \bar{B} = \overline{A \odot B} = \bar{A} \odot \bar{B} = A \odot \bar{B}$$

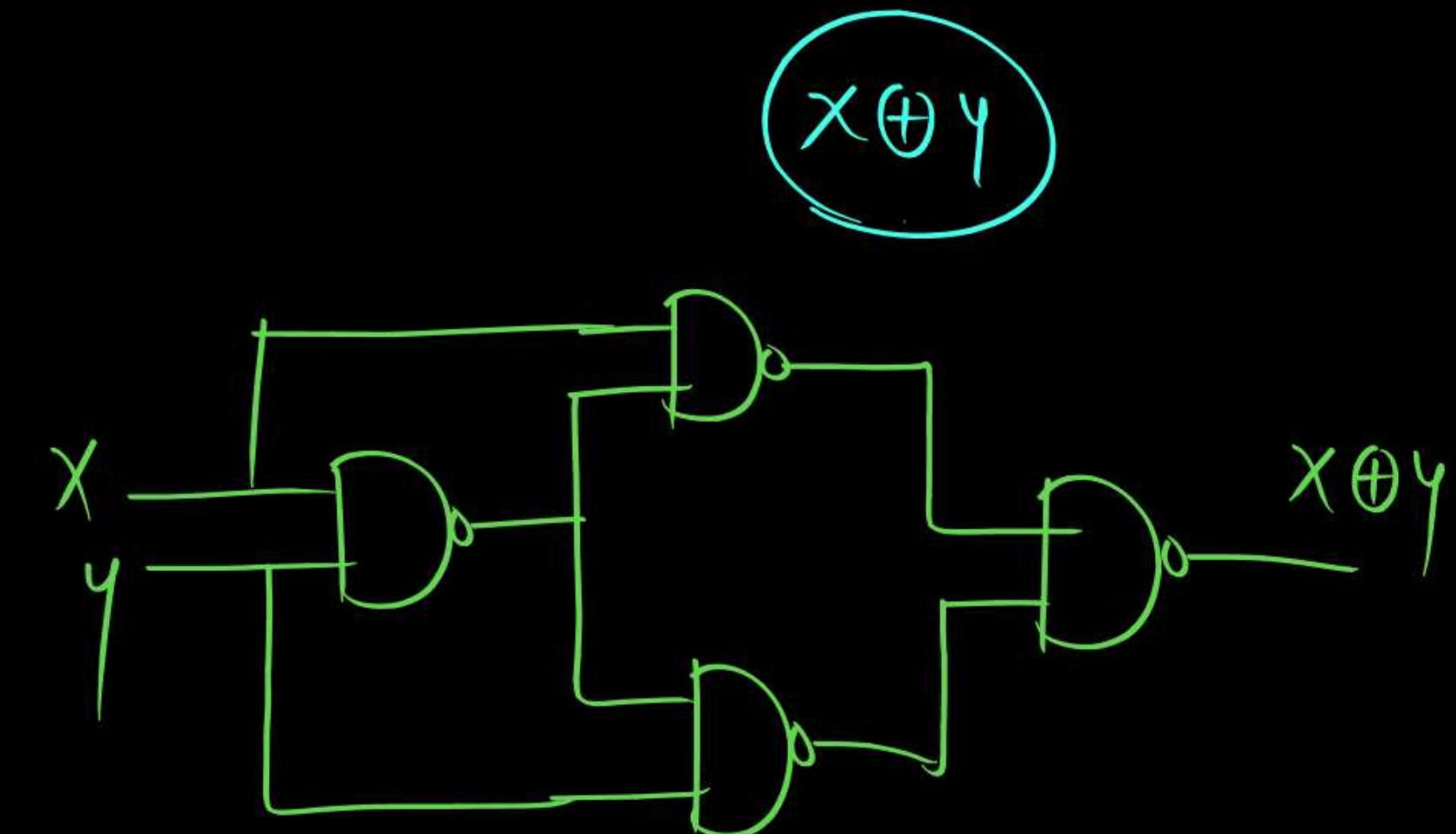
NOTE

* $AB \oplus A \oplus B = A + B$

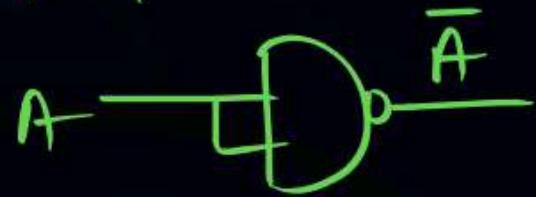
#Q.

Assuming that only the X and Y logic inputs are available and their complements \bar{X} and \bar{Y} are not available, what is the minimum number of two-input NAND gates required implementing $X \oplus Y$?

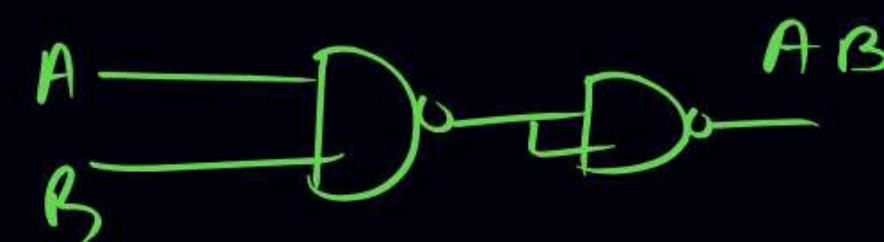
- (a) 2
- (b) 3
- (c) 4
- (d) 5



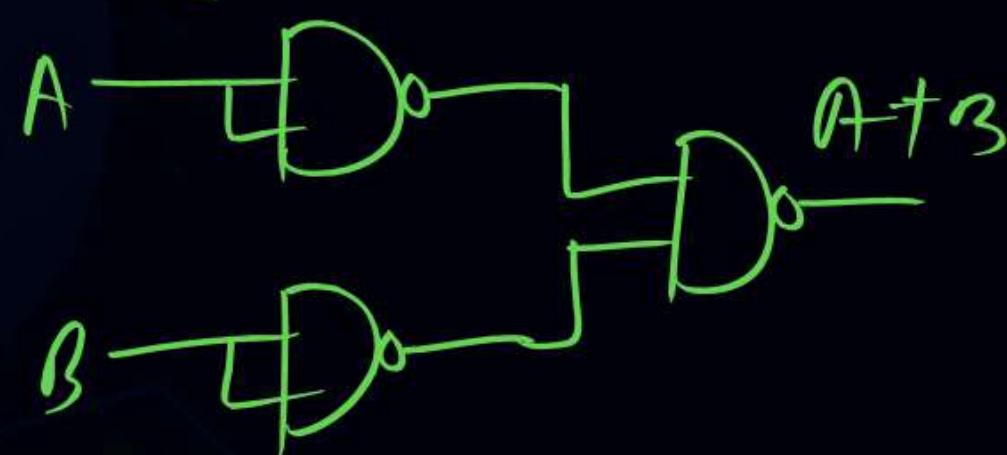
NOT



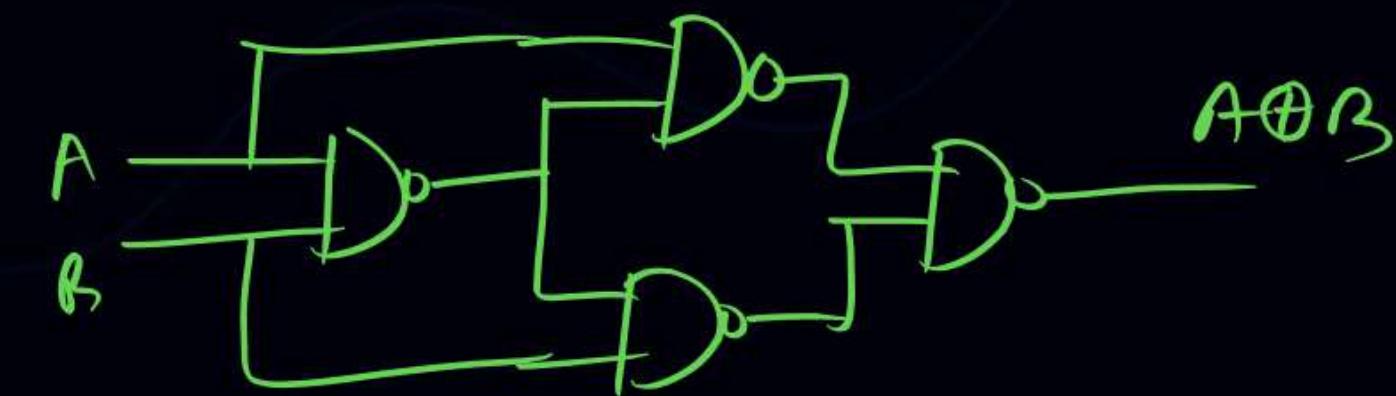
AND



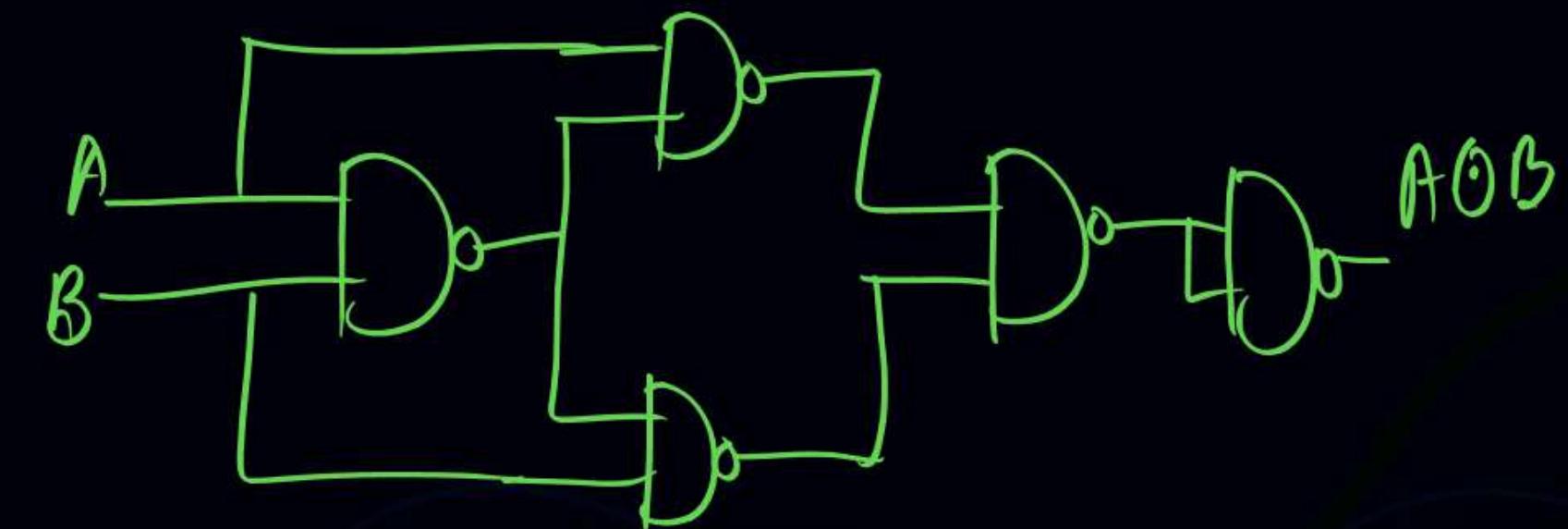
OR



X-OR

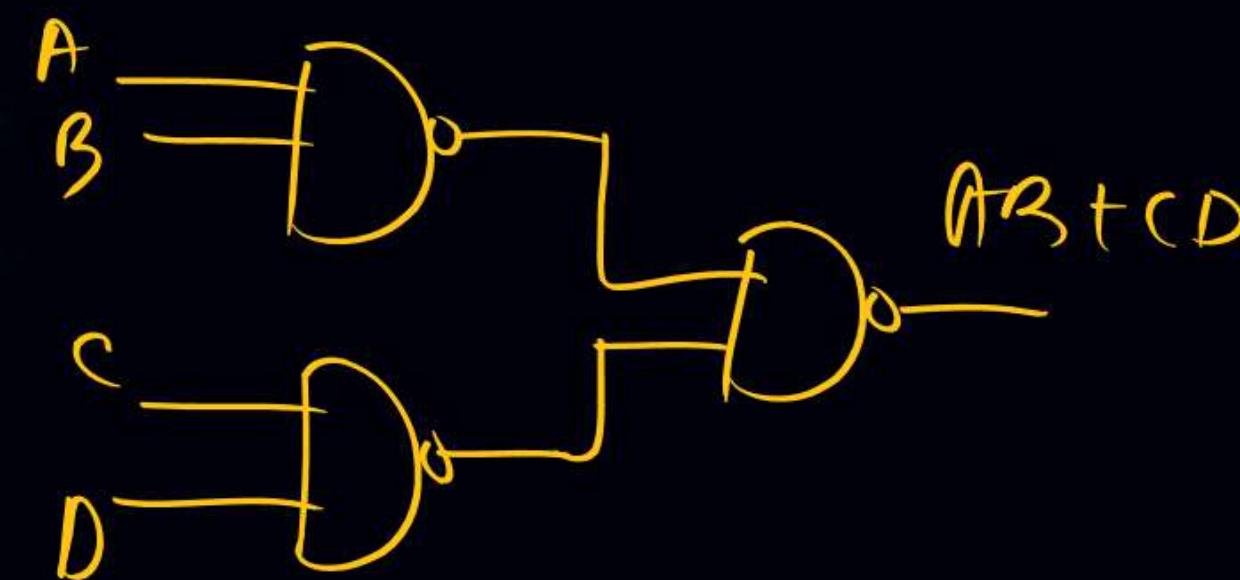


X-NOR

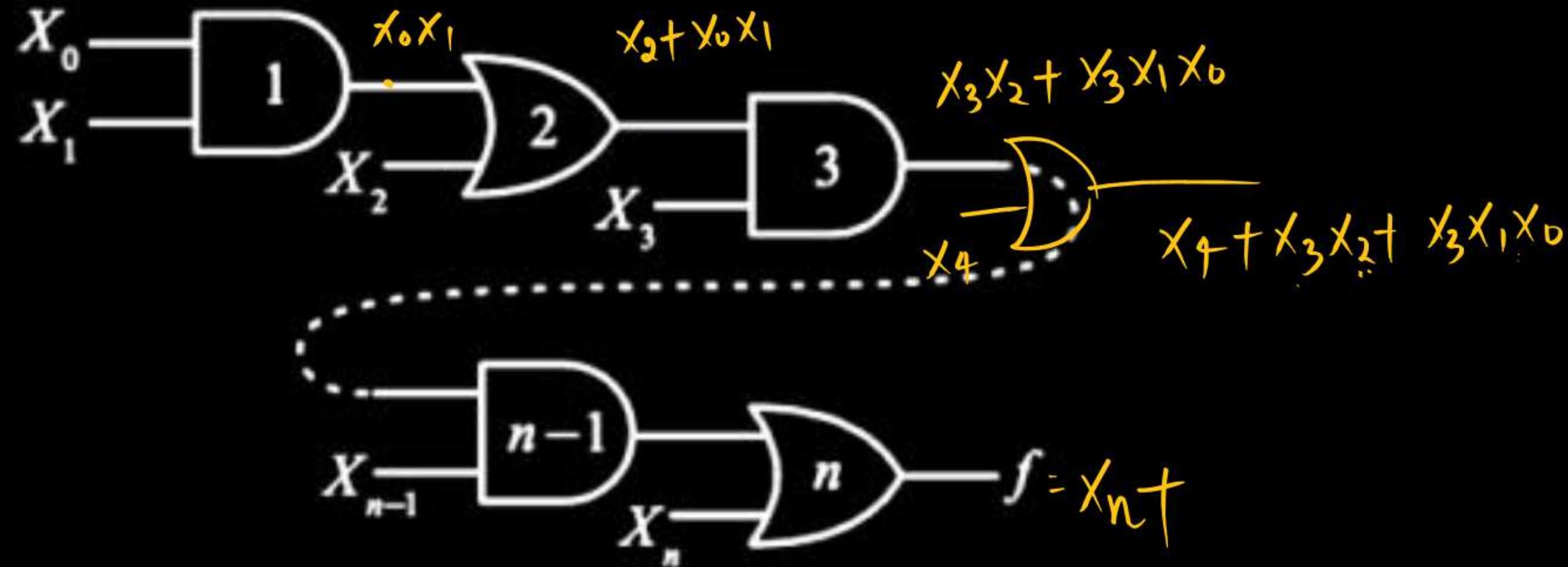


	NAND	NOR
NOT	1	1
AND	2 } 3	3
OR	3 }	2
XOR	4 }	5
XNOR	5 }	4
NAND	1 }	4
NOR	4 }	1

$$\begin{array}{c} AB + CD \\ \hline \end{array} \rightarrow \text{NAND}_3$$

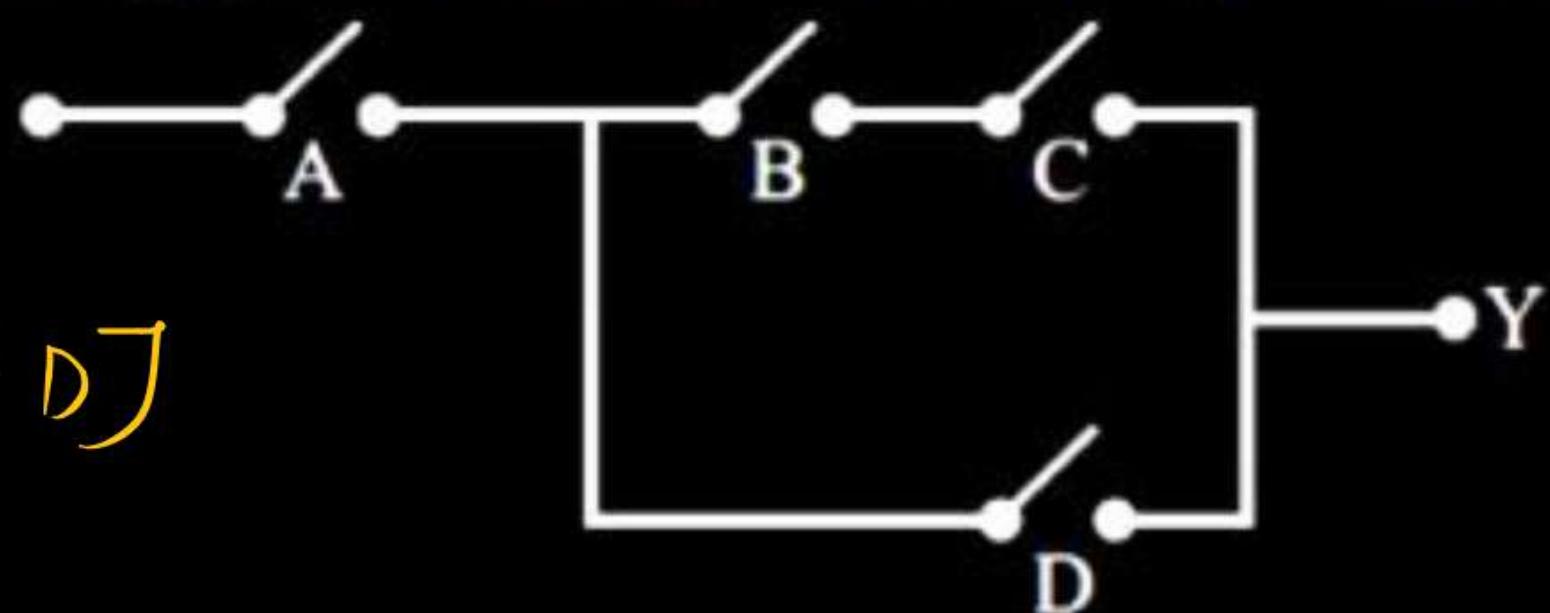


#Q. In the given network of AND and OR gates, f can be written as



- (a) $X_0X_1X_2\dots X_n + X_1X_2\dots X_n + X_2X_3\dots X_n\dots X_n$
- (b) $X_0X_1 + X_2 + X_3 + \dots + X_{n-1}\dots X_n$
- (c) $X_0 + X_1 + X_2 + \dots + X_n$
- ~~(d)~~ $X_0X_1X_3\dots X_{n-1} + X_2 + X_3 + X_5\dots X_{n-1} + \dots + X_{n-2} + X_{n-1} + X_n$

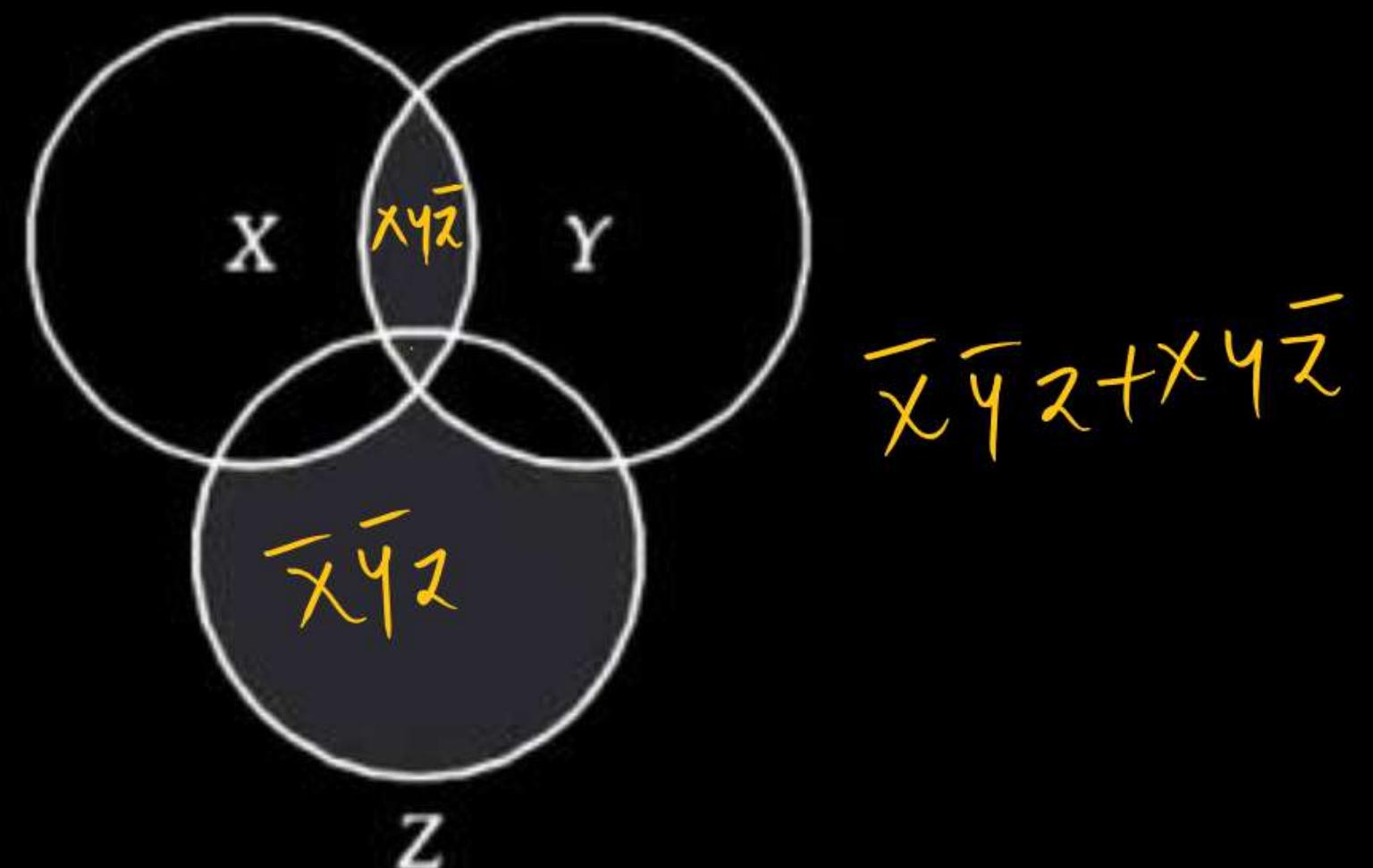
#Q. For the switch circuit, taking open as 0 and closed as 1, the expression for the circuit in Y



$$A \cdot [B \cdot C + D]$$

- (a) $A + (B + C) D$
- (b) $A + BC + D$
- ~~(c) $A(BC + D)$~~
- (d) None of these

#Q. The Boolean expression for the shaded area in the Venn diagram is



- (a) $\bar{X} + \bar{Y} + Z$
- (b) $XYZ + \bar{X}YZ$
- (c) $X + Y + Z$
- (d) $\bar{X}\bar{Y}Z + XY$

#Q. For the identity $AB + \bar{A}C + BC = AB + \bar{A}C$, the dual from is

- (a) ~~$(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$~~
- (b) $(\bar{A} + \bar{B})(\bar{A} + \bar{C})(\bar{B} + \bar{C}) = (\bar{A} + \bar{B})(A + \bar{C})$
- (c) $(A + B)(\bar{A} + C)(B + C) = (\bar{A} + \bar{B})(A + \bar{C})$
- (d) $\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C} = \bar{A}\bar{B} + A\bar{C}$

$$(A+\beta) \cdot (\bar{A}+\gamma) \cdot (\beta+\gamma) = (A+\beta) \cdot (\bar{A}+\gamma)$$

#Q.

Minimum number of 2-inputNAND gates that will be required to implement the function :

$$Y = \underbrace{AB + CD}_{X} + EF$$

(a) 4

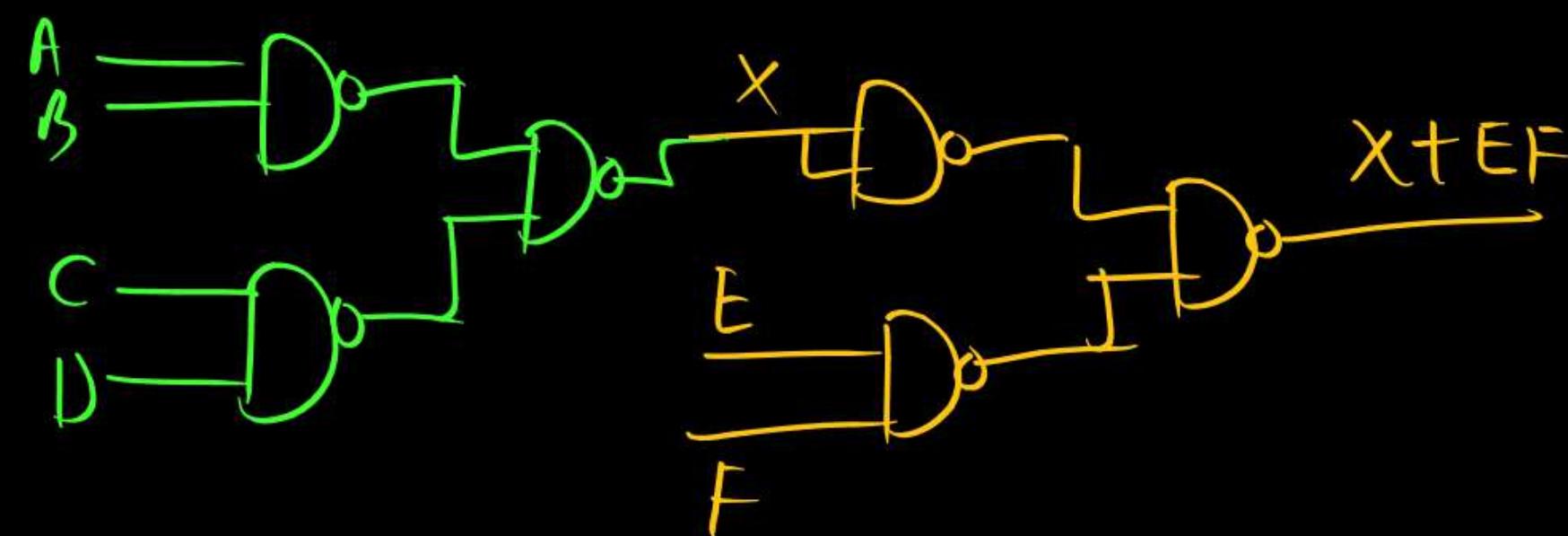
X

(b) 5

(c) 6

(d) 7

$$Y = X + EF = X \cdot X + EF$$



#Q. #

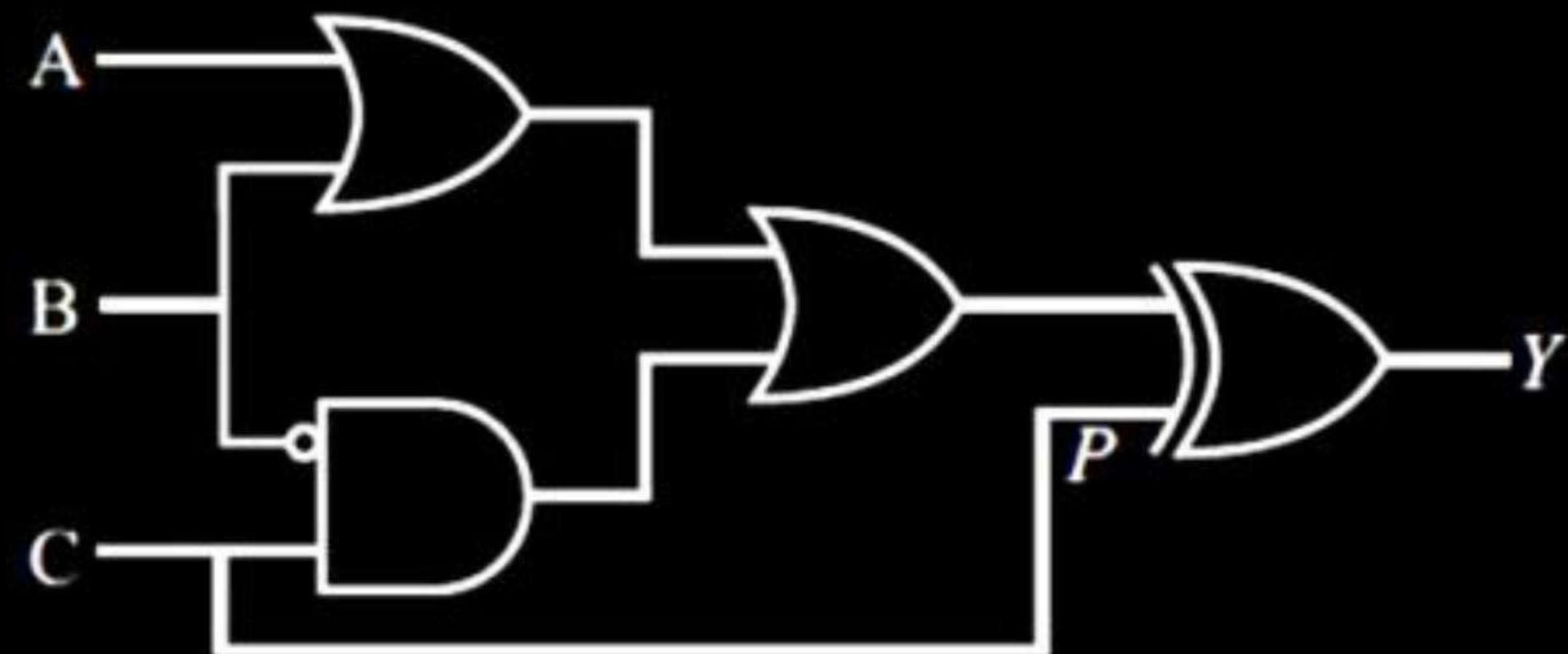
Which of the following is the Boolean function for Majority Voting, assuming A, B, C are inputs and Y is output?

- (a) $Y = AB + AC + CB$
- (b) $Y = A + B + C$
- (c) $Y = ABC$
- (d) $Y = AB + BC$

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$Y = \sum m(3, 5, 6, 7)$$

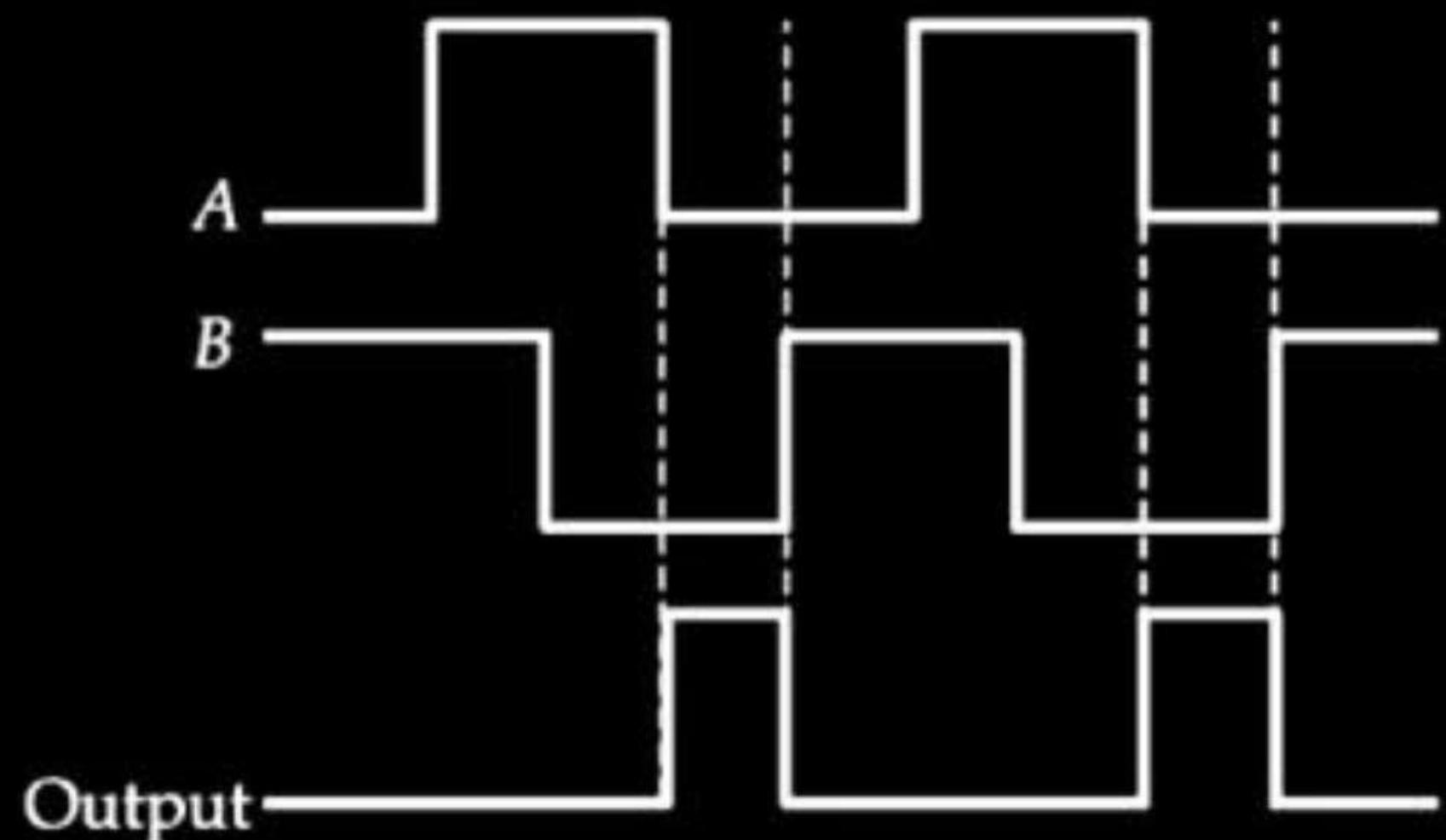
#Q. What will be the output of the following circuit, if point-P is stuck at 1 ?



- (a) $A + B + C$
- (b) $A' B' C'$
- (c) $(A B C)'$
- (d) 0

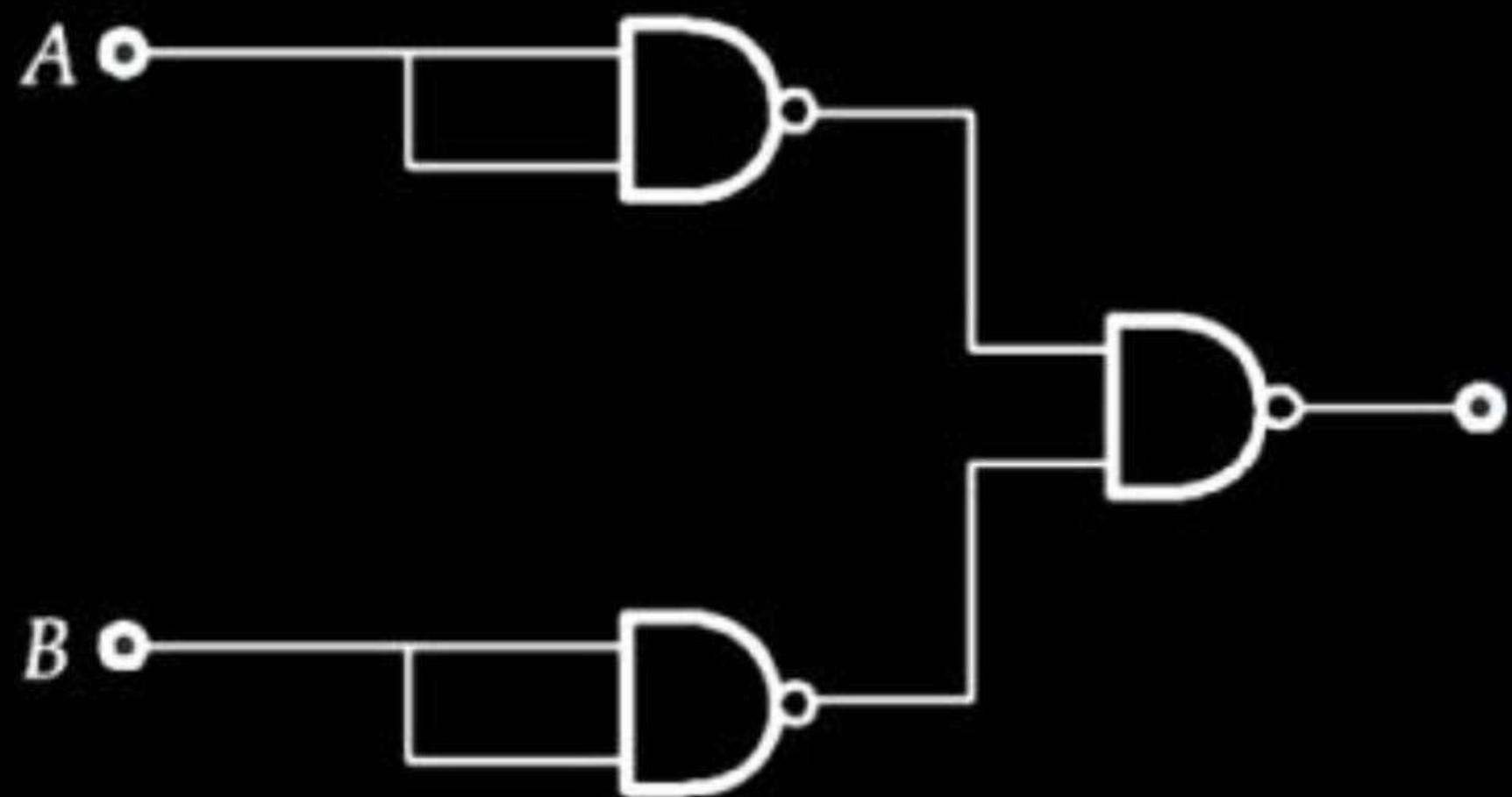
#Q

If the input signals (A and B) and output signal are as below then the circuit element is



- (a) AND Gate
- (b) OR Gate
- (c) NOR Gate
- (d) XOR Gate

#Q. The output equivalent circuit of following circuit is



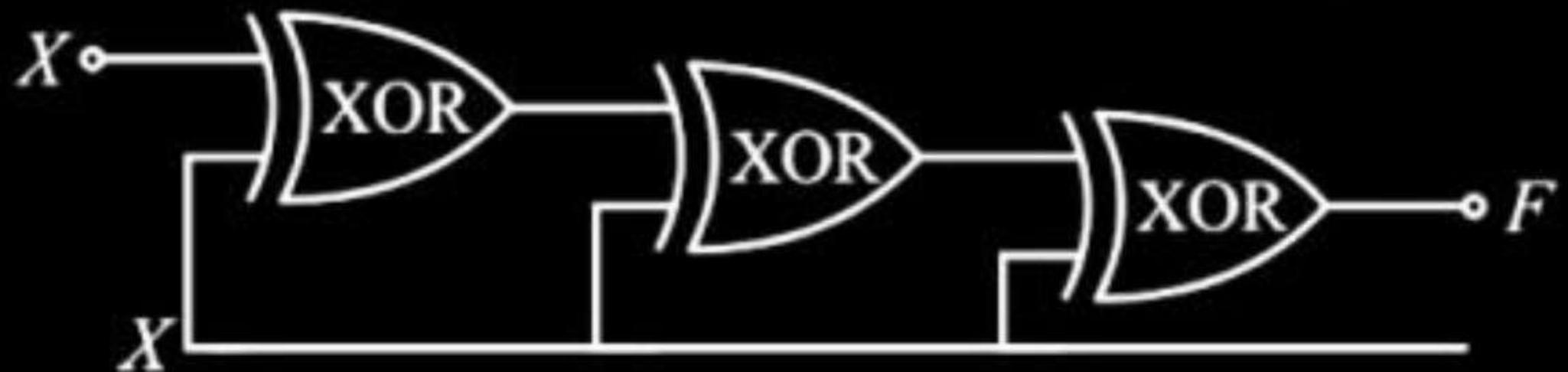
- (a) INVERTER
- (b) AND
- (c) OR
- (d) NOR

#Q.

Which of the following statement is correct?

- (a) NAND and NOR functions are Commutative and Associated.
- (b) Both NAND and NOR functions are neither Commutative nor Associative.
- (c) NAND and NOR functions are Associative but Commutative.
- (d) NAND and NOR functions are Cumulative but not Associative.

#Q. For the circuit shown in the below figure, the output F will be



- (a) 1
- (b) zero
- (c) X
- (d) \bar{X}

#Q.

Which logical operation is performed by ALU of 8085 to complement a number?

- (a) AND
- (b) NOT
- (c) OR
- (d) EXCLUSIVE OR

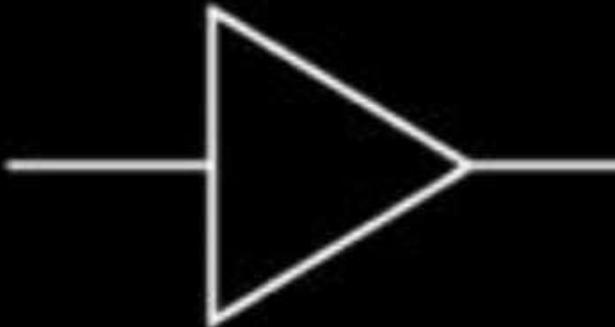
#Q.

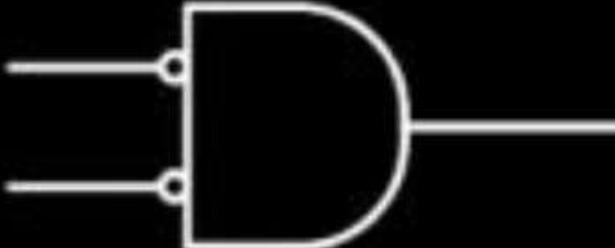
Match List-I (Circuit Symbols) with List-II (Nomenclature) and select the correct answer using the codes given below:

List-I

List-II

- A.  1. NAND

- B.  2. NOR

- C.  3. Buffer

- D.  4. Schmitt trigger

Codes:	A	B	C	D
(a)	4	3	1	2
(b)	3	4	2	1
(c)	4	3	2	1
(d)	3	4	1	2

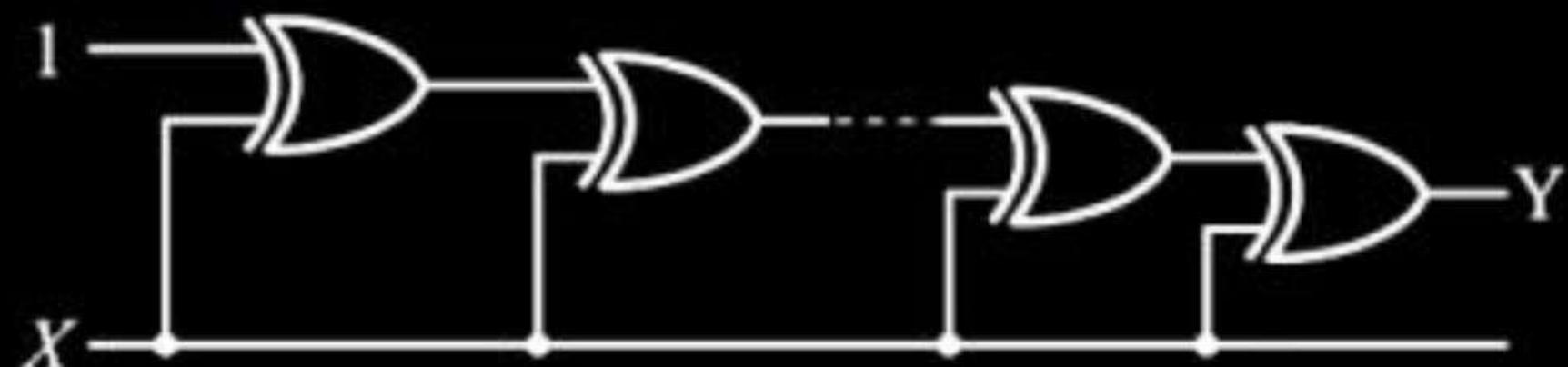
#Q.

Which one of the following statements is correct? For a 4-input NOR gate, when only two inputs are to be used, the best option for the unused inputs is to

- (a) connect them to the ground
- (b) connect them to V_{cc}
- (c) keep them open
- (d) connect them to the used inputs

#Q.

If the input to the digital circuit of the below figure consisting of a cascade of 20 XOR gates is X , then the output Y ?



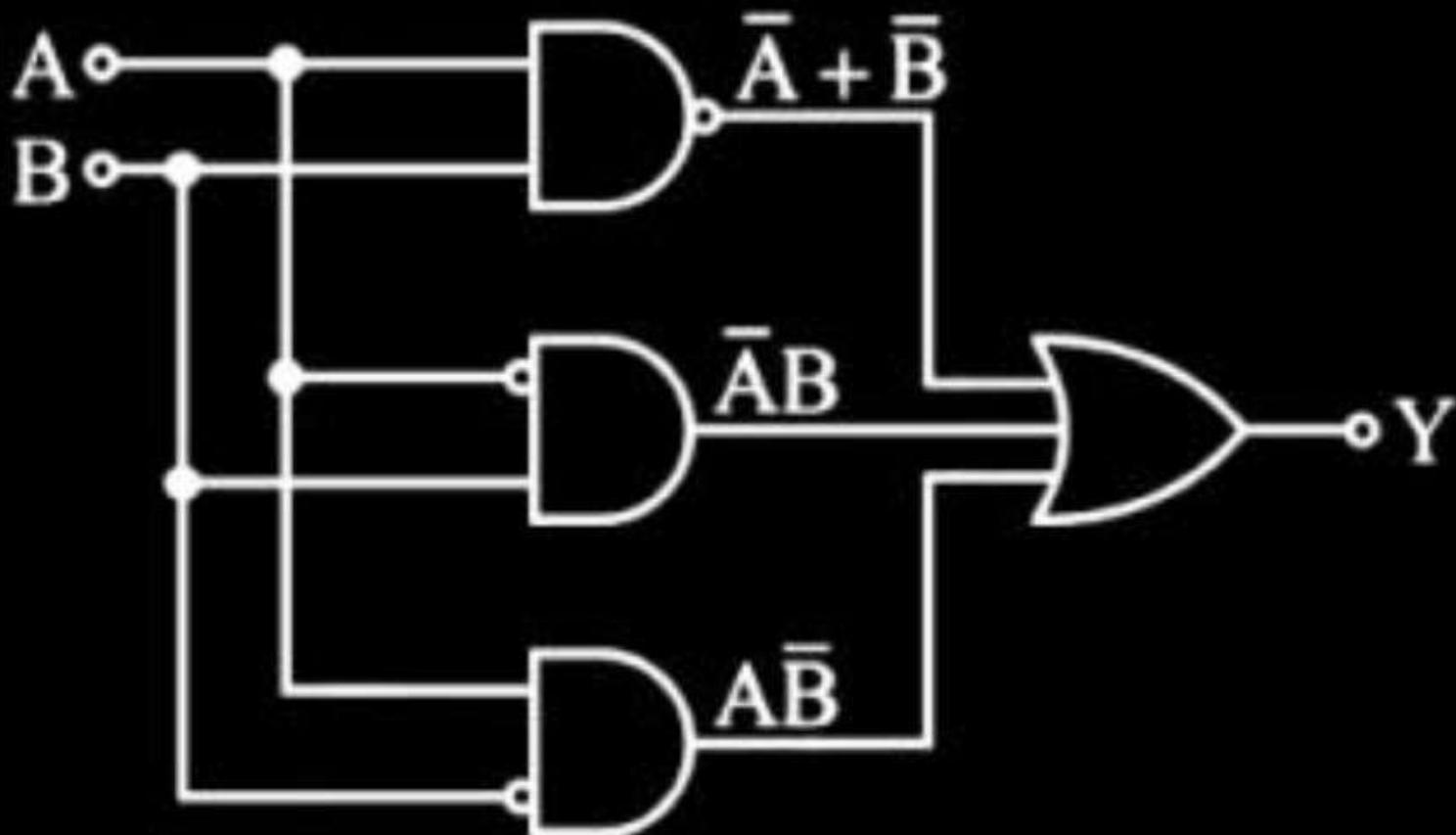
- (a) 0
- (b) 1
- (c) X
- (d) X^2

#Q.

The AND function can be realized by using only n number of NOR gates. What is n equal to?

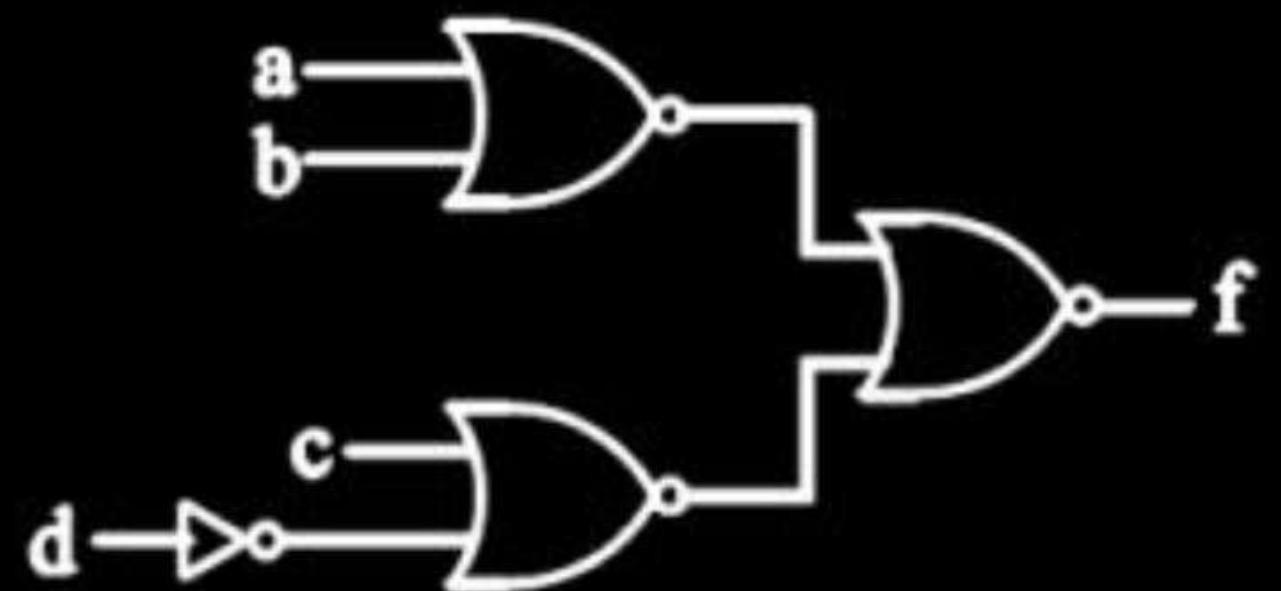
- (a) 2
- (b) 3
- (c) 4
- (d) 5

#Q. In the given circuit, the output Y equals which one of the following?



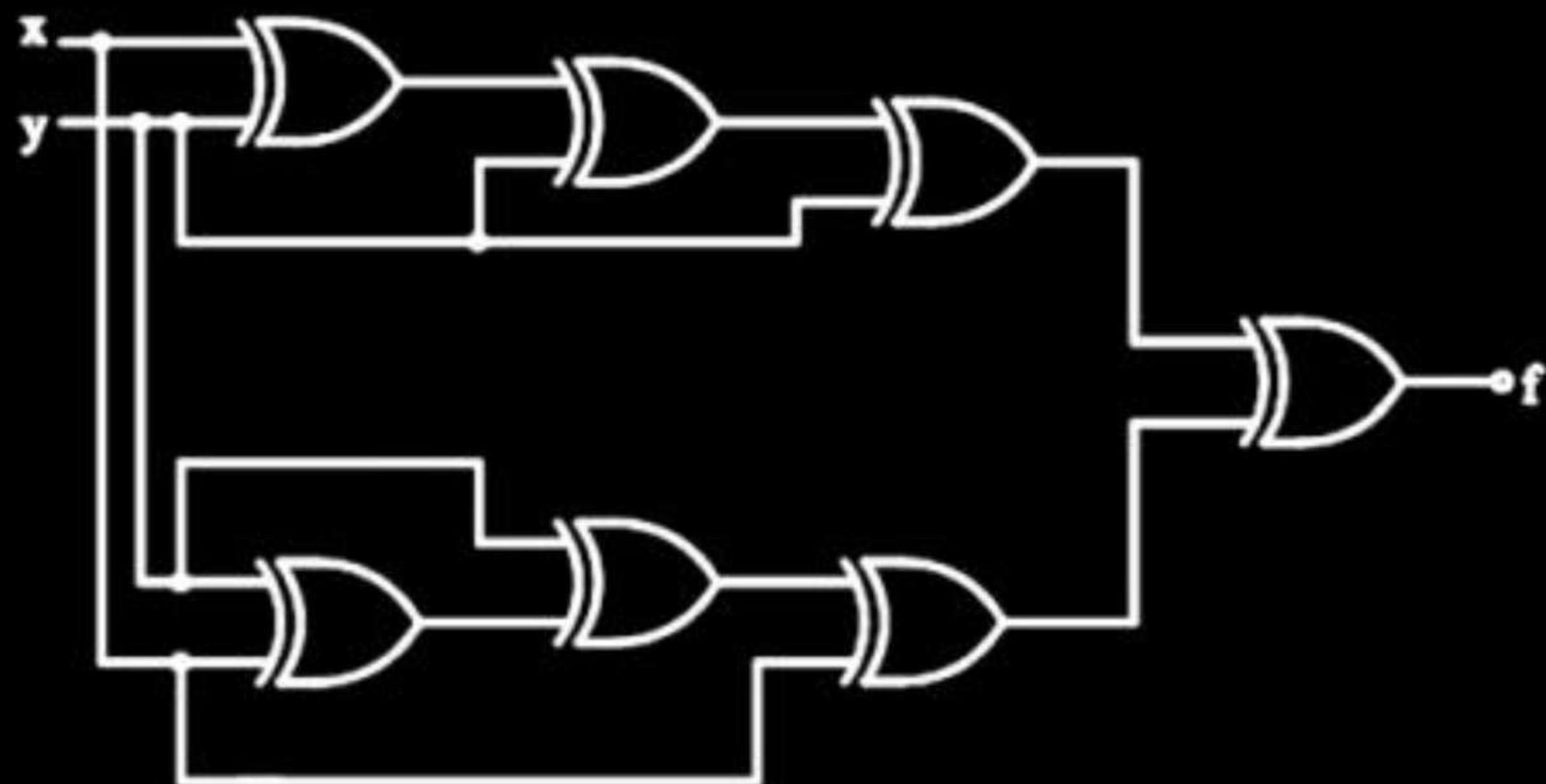
- (a) $A + B$
- (b) $\bar{A}\bar{B} + A\bar{B}$
- (c) AB
- (d) $\bar{A} + \bar{B}$

#Q. Which one of the following is the correct output (f) of the below circuit?



- (a) $(a + b)(c + \bar{d})$
- (b) $(\bar{a} + \bar{b})(c + \bar{d})$
- (c) $(a + \bar{b})(c + \bar{d})$
- (d) $(a + b)(\bar{c} + \bar{d})$

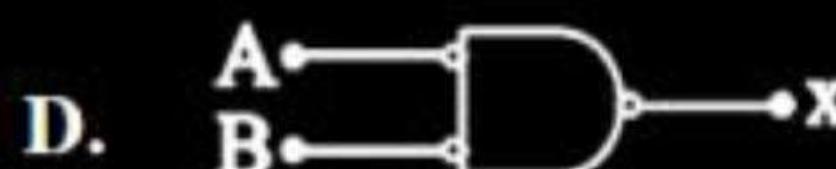
#Q. The circuit shown below generates the function of



- (a) $x \oplus y$
- (b) 0
- (c) $x\bar{y} + yx + \bar{y}x$
- (d) $x \cdot \bar{y}$

#Q.

Match List I with List II and select the correct answer using the code given below the lists :

List-I**List-II**

1. AB

2. \overline{AB}

3. $A + B$

4. $\overline{A + B}$

Codes : A B C D

(a) 3 1 4 2

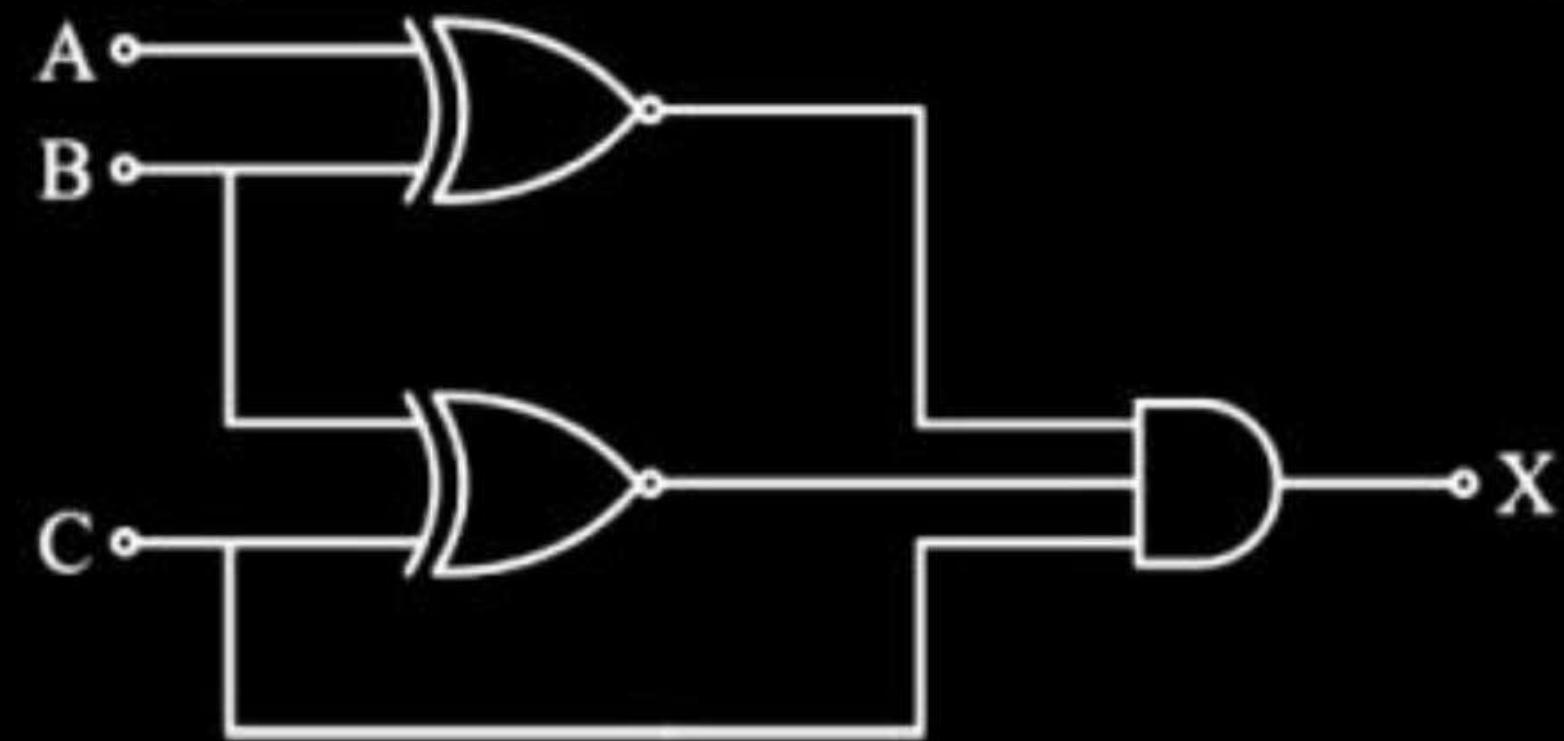
(b) 2 1 4 3

(c) 3 4 1 2

(d) 2 4 1 3

#Q.

For logic circuit shown, the required inputs A, B and C to make the output $X = 1$ are, respectively,



- (a) 1, 0 and 1
- (b) 0, 0 and 1
- (c) 1, 1 and 1
- (d) 0, 1 and 1

#Q.

Statement (I) : XOR gate is not a universal gate

Statement (II) : It is not possible to realize any Boolean function using XOR gates only

- (a) Both (I) and (II) is true and R is the correct explanation of A
- (b) Both (I) and (II) is true but R is NOT the correct explanation of A
- (c) (I) is true but (II) is false
- (d) (I) is false but (II) is true

#Q.

If the output of a logic gate is ‘1’ when all its inputs are at logic ‘0’, the gate is either

- (a) A NAND or A NOR
- (b) An AND or an EX-NOR
- (c) An OR or an NAND
- (d) An EX-OR or an EX-NOR

#Q. NAND and NOR gates are called ‘Universal’ gates primary because

- (a) they are available everywhere.
- (b) they are widely used in I.C. packages.
- (c) they can be combined to produce AND, OR and NOR gate.
- (d) they can be manufactured easily.

#Q.

Statement (I) : When all inputs of a NAND gate are shorted to get a single input, single output gate, it becomes an inverter.

Statement (II) : When all inputs of a NAND gate are at logic ‘0’ level the output is at logic ‘0’ level.

- (a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
- (b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).
- (c) Statement (I) is true but Statement (II) Is false.
- (d) Statement (I) is false but Statement (II) Is true.

#Q.

Statement (I) : XOR gate is not a universal gate.

Statement (II) : It is not possible to realize all Boolean function using XOR gates only.

- (a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
- (b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).
- (c) Statement (I) is true but Statement (II) Is false.
- (d) Statement (I) is false but Statement (II) Is true.

#Q. The logical expression, $ABC + A\bar{B}C + A\bar{B}\bar{C}$

- (a) $\bar{A}(B + C)$
- (b) $\bar{A} + \bar{B} + \bar{C}$
- (c) $\bar{A}\bar{B}\bar{C}$
- (d) $A(\bar{C} + \bar{B})$

#Q.

Which one of the following relations from the Boolean algebra pertaining to, 'AND' operation cannot be verified when A and B can take on only the value 0 or 1?

- (a) $AB = BA$
- (b) $AA = A$
- (c) $A1 = 1$
- (d) $A0 = 0$

#Q.

Consider the following regarding the drawbacks of BCD arithmetic over binary arithmetic :

1. Perform arithmetic operations indirectly on decimal data.
2. Take more time for execution.
3. Less efficient use of memory.
4. Small number of computations are required.

Which of the above drawbacks are correct?

- (a) 1 and 4 only
- (b) 2 and 3 only
- (c) 1, 2 and 3 only
- (d) 1, 2, 3 and 4

#Q.

The open collector output of two 2-input NAND gates are connected to a common pull-up resistor. If the inputs of the gates are A, B and C, D respectively, the output is equal to

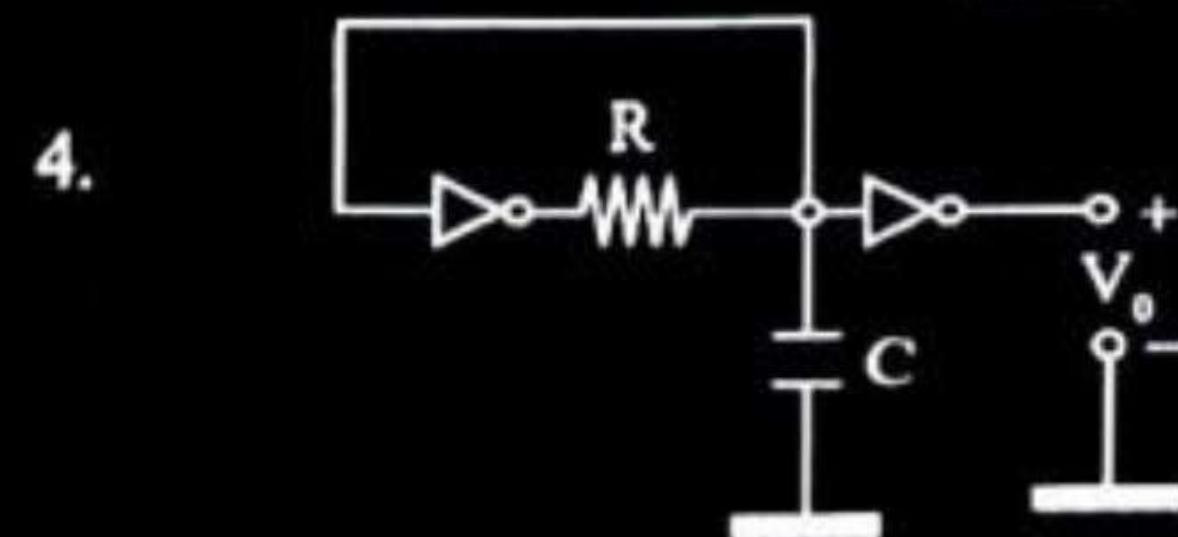
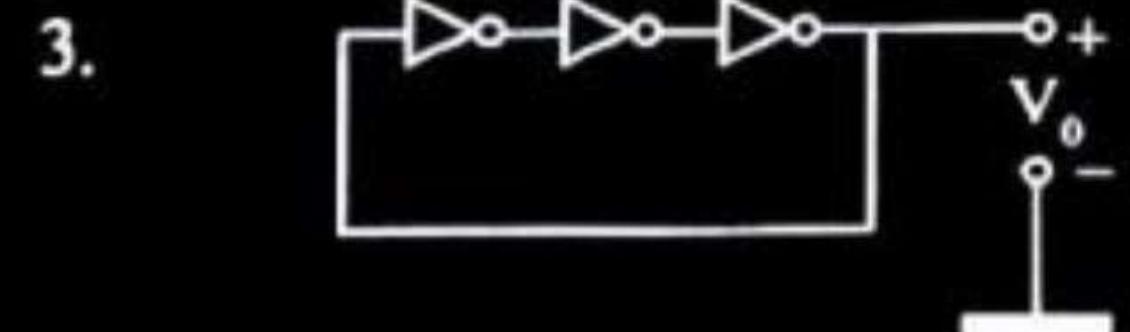
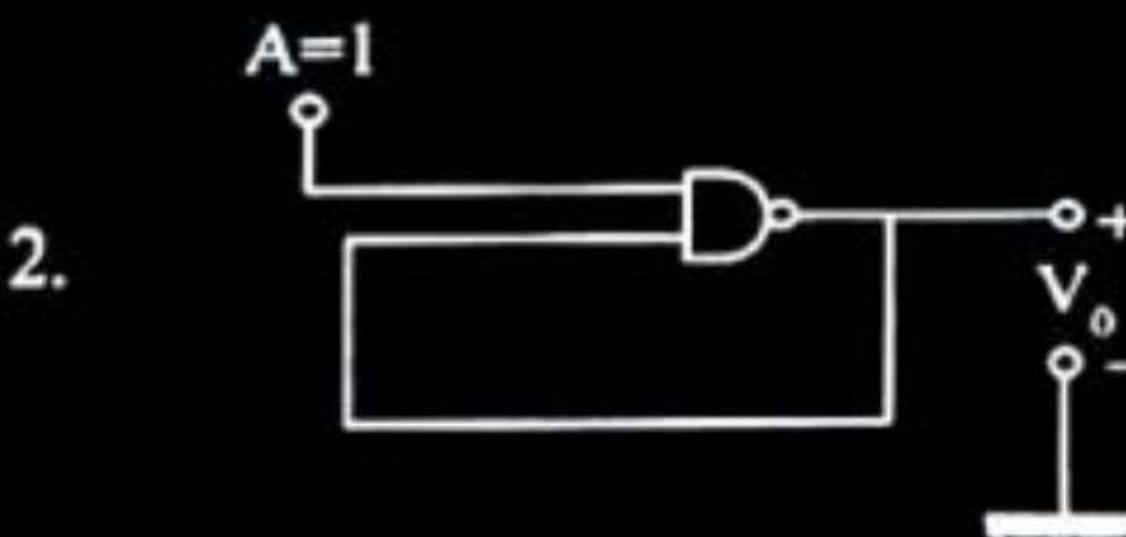
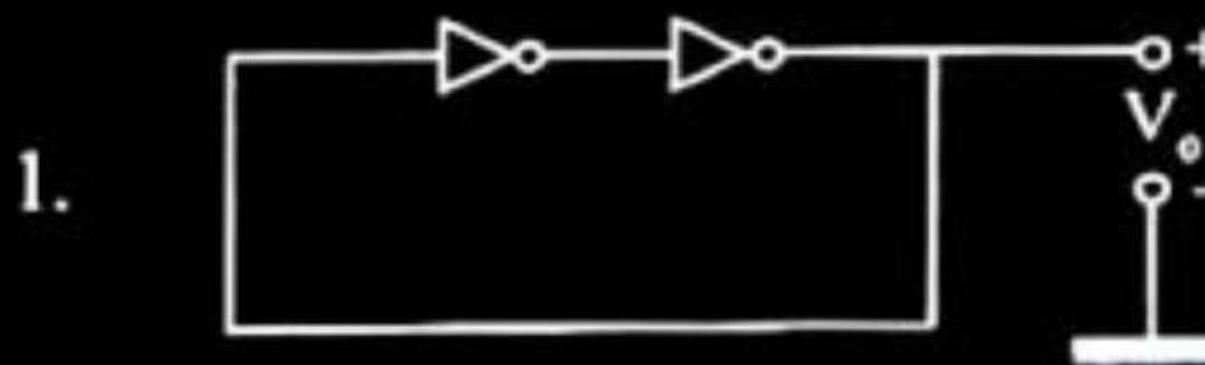
- (a) $\overline{AB} \cdot \overline{CD}$
- (b) $\overline{AB} + \overline{CD}$
- (c) $AB + CD$
- (d) $AB \cdot CD$

#Q. How is inversion achieved using EX - OR gate?

- (a) Giving input signal to the two input lines of the gate tied together.
- (b) Giving input to one input line and logic zero to the other line.
- (c) Giving input to one input line and logic one to the other line.
- (d) Inversion cannot be achieved using EX-OR gate.

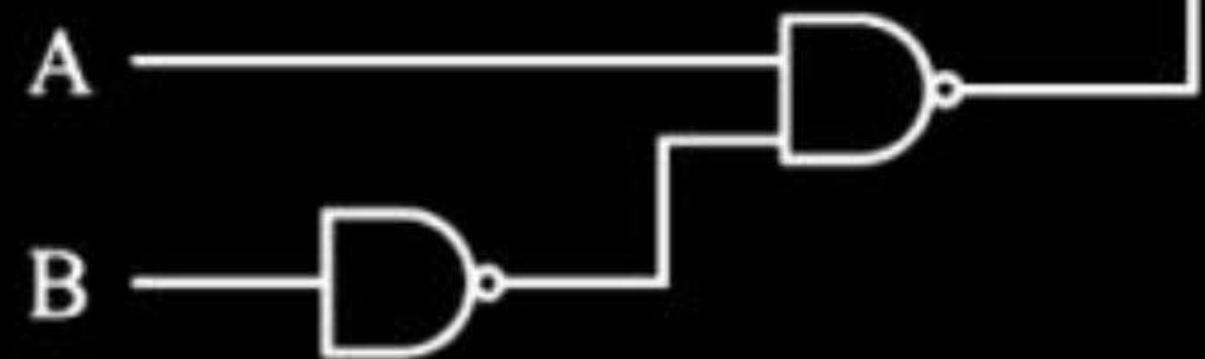
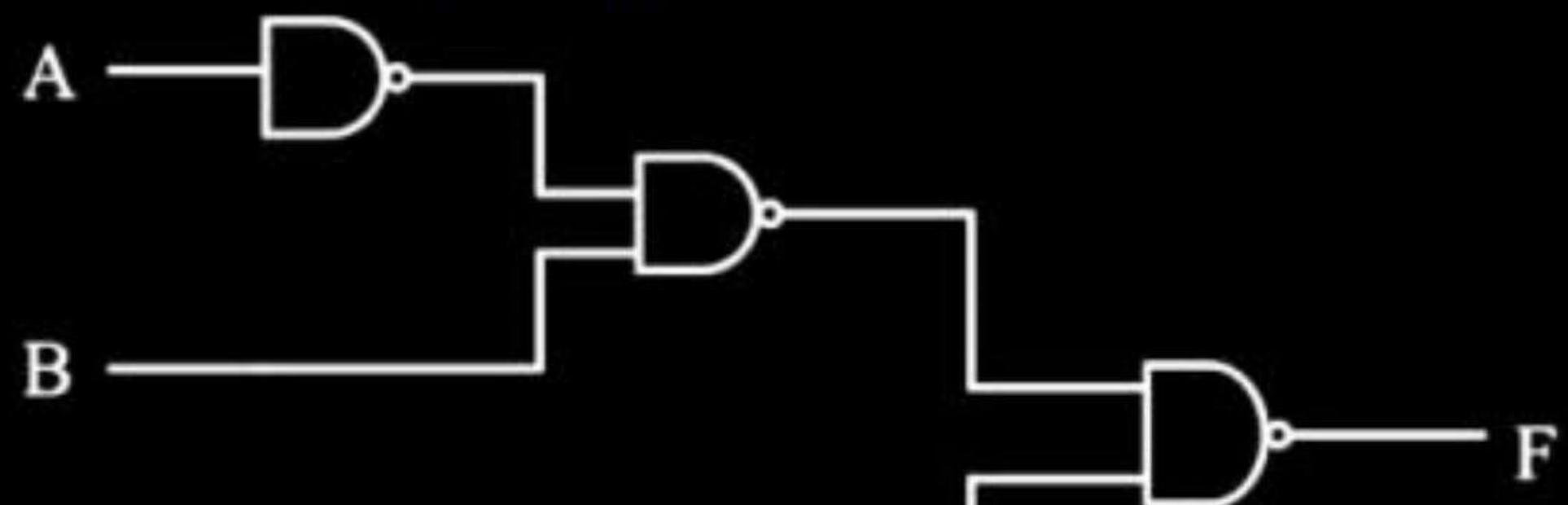
#Q.

Consider the following circuits (Assume all gates to have a finite propagation delay). Which of these circuits generate a periodic square wave output?



- (a) 1 and 2
- (b) 3 and 4
- (c) 2, 3 and 4
- (d) 1, 2, 3 and 4

#Q. The circuit shown below is functionally equivalent to



- (a) NOR gate
- (b) OR gate
- (c) EX-OR gate
- (d) NAND gate

#Q.

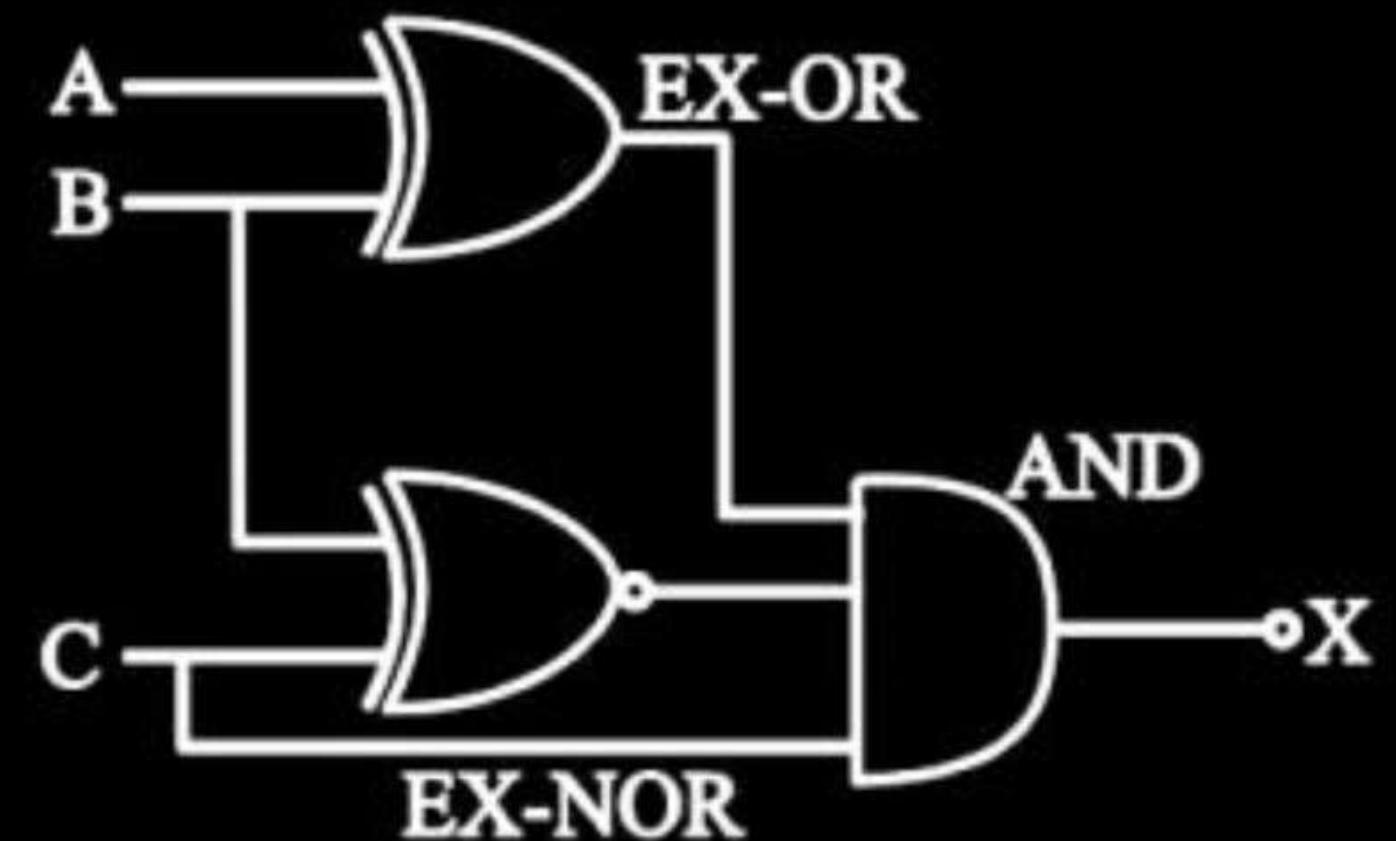
Assume that only x and y logic inputs are available, and their complements \bar{x} and \bar{y} are not available.
What is the minimum number of 2-input NAND gates required to implement $x \oplus y$?

- (a) 2
- (b) 3
- (c) 4
- (d) 5

#Q.

Consider the following logic circuit :

What is the required input condition (A, B, C) to make the output X = 1, for the below logic circuit?



- (a) (1, 0, 1)
- (b) (0, 0, 1)
- (c) (1, 1, 1)
- (d) (0, 1, 1)

#Q.

The output of a two level AND-OR gate network is F . What is the output when all the gates are replaced by NOR gates?

- (a) F
- (b) \overline{F}
- (c) F^D
- (d) \overline{F}^D

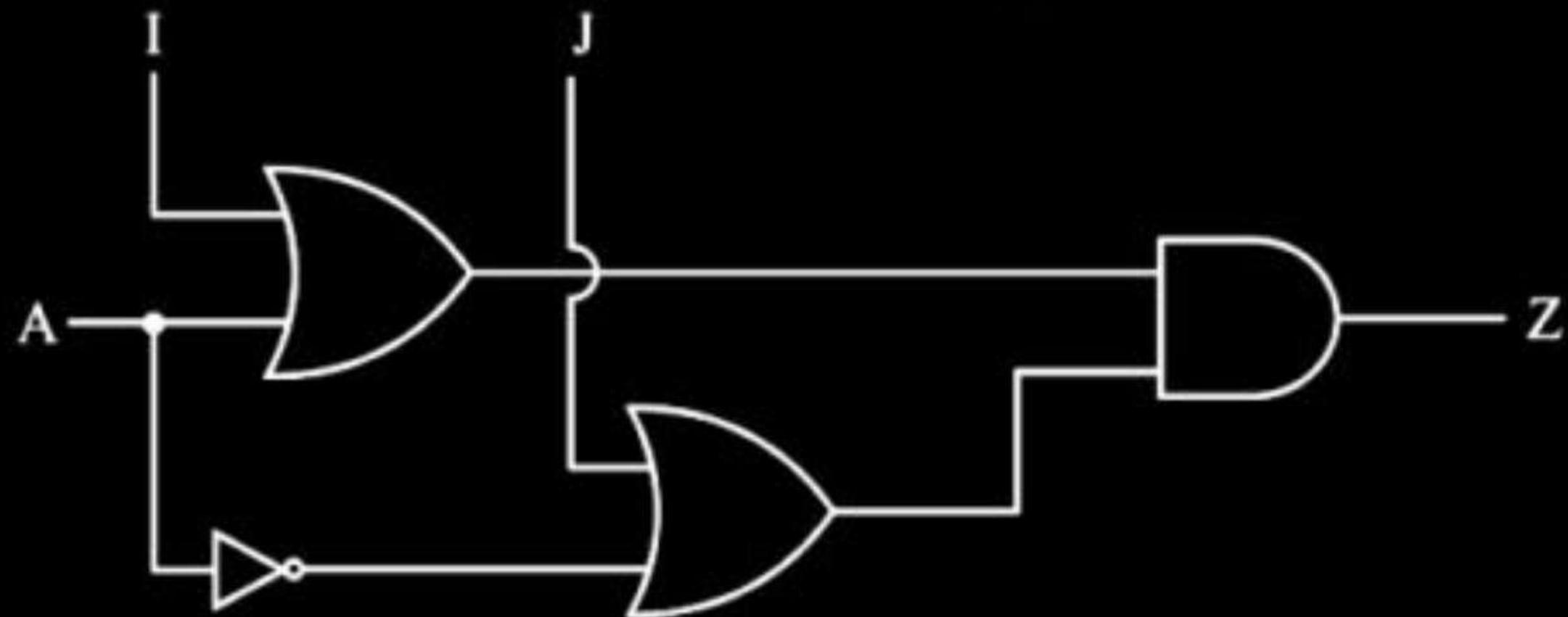
#Q.

The Boolean expression $Y(A, B, C) = A + BC$ is to be realize using 2-input gates of only one type.
What is the minimum number of gates required for the realization?

- (a) 1
- (b) 2
- (c) 3
- (d) 4 or more

#Q.

The circuit shown below is to be used to implement the function $Z = f(A, B) = \bar{A} + B$.

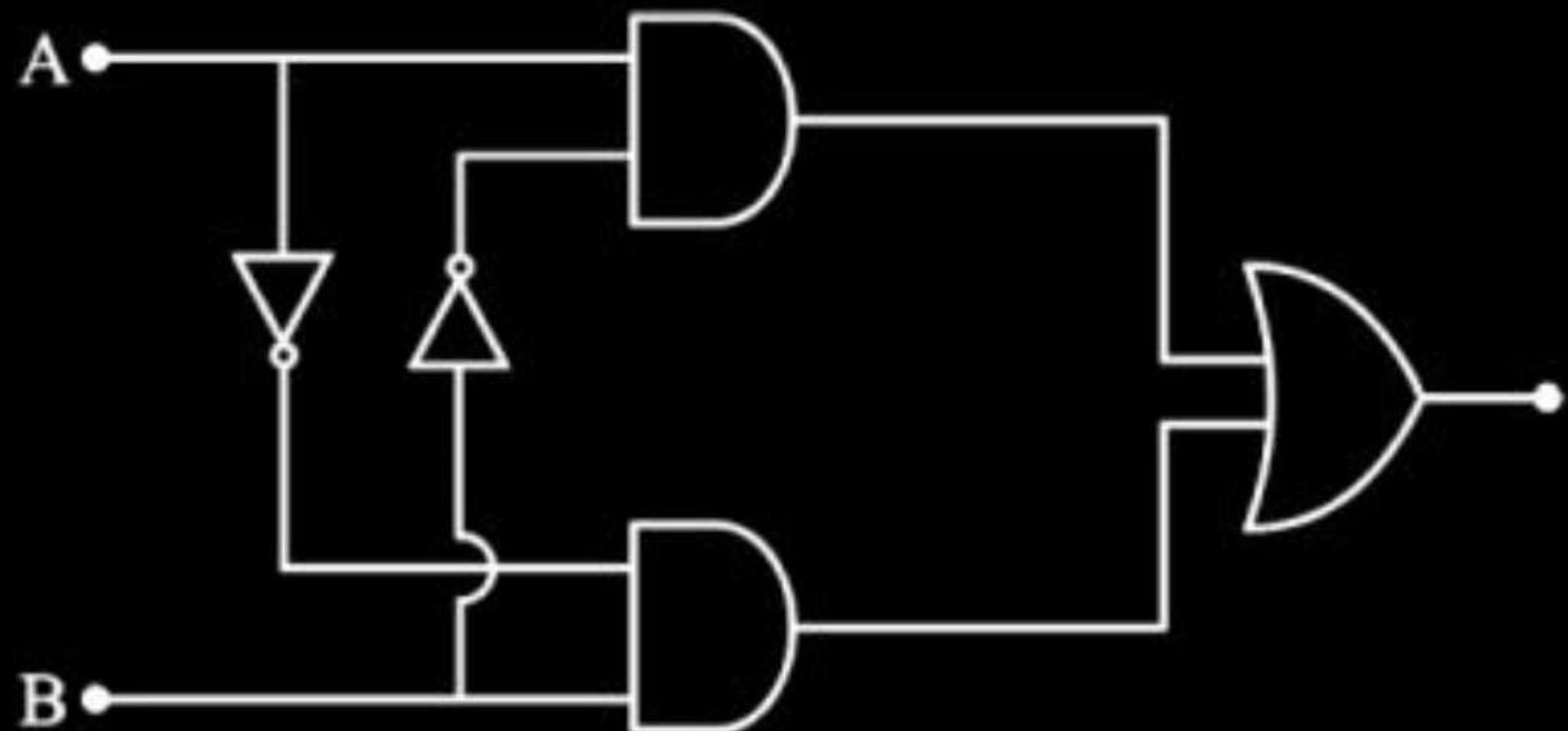


What values are to be selected for I and J ?

- (a) I = 0, J = B (b) I = 1, J = B
- (c) I = B, J = 1 (d) I = \bar{B} , J = 0

#Q.

Which one of the following logical operations is performed by the digital circuit shown below?

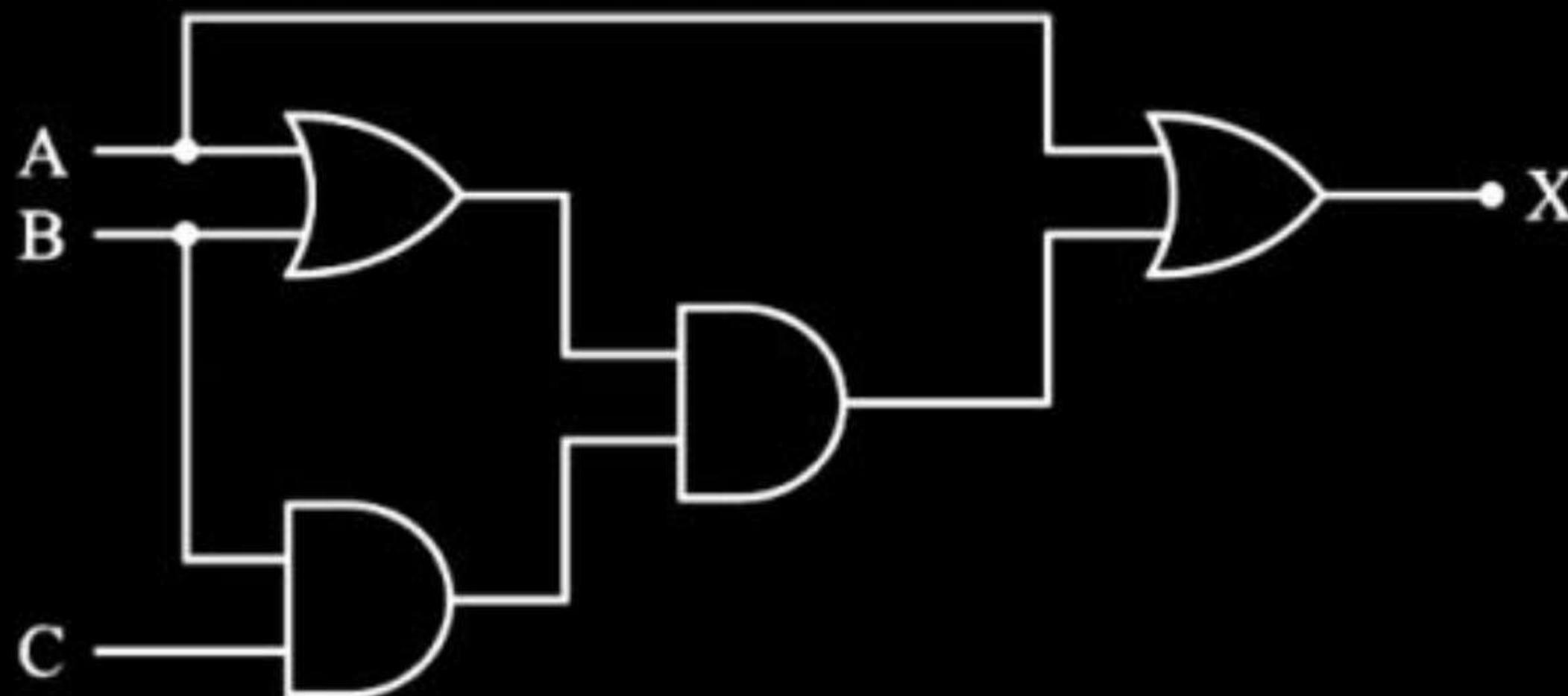


- (a) NOR
- (b) NAND
- (c) EX-OR
- (d) OR

#Q. What is the Boolean expression $A \oplus B$ equivalent to ?

- (a) $AB + \bar{A}\bar{B}$
- (b) $\bar{A}B + A\bar{B}$
- (c) B
- (d) \bar{A}

#Q. For the logic circuit given below, what is the simplified Boolean function?



- (a) $X = AB + C$
- (b) $X = BC + A$
- (c) $X = AB + AC$
- (d) $X = AC + B$

#Q.

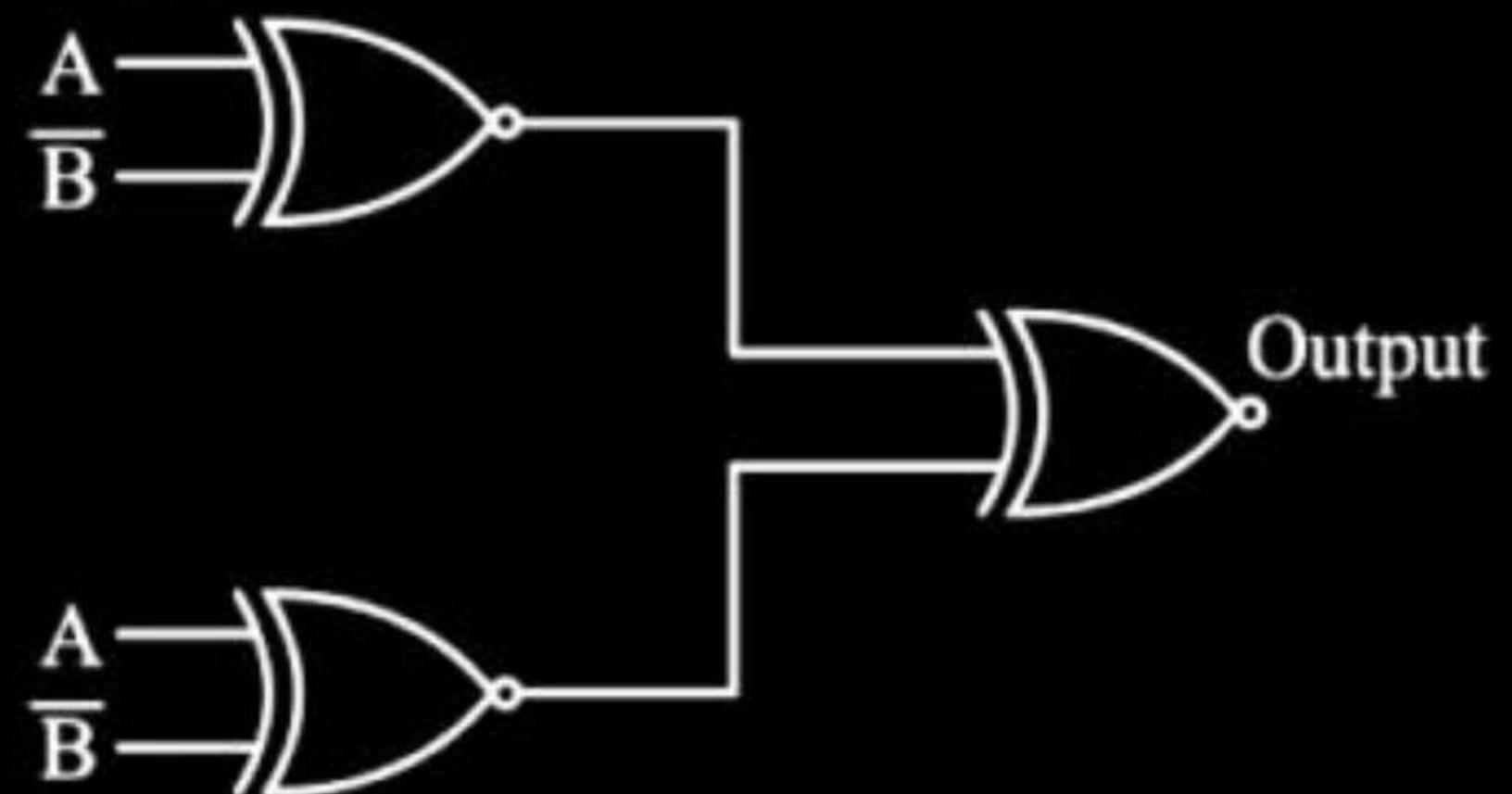
The black box in the below figure consists of a minimum complexity circuit that uses only AND, OR and NOT gates.

The function $f(X, Y, Z) = 1$ whenever X, Y are different and 0 otherwise. In addition the 3 inputs X, Y, Z are never all the same value. Which one of the following equations leads to the correct design for the minimum complexity circuit?



- (a) $X'Y + XY'$
- (b) $X + Y'Z$
- (c) $X'Y'Z' + XY'Z$
- (d) $XY + Y'Z + Z'$

#Q. The output of the circuit shown in the figure is equal to



- (a) 0
- (b) 1
- (c) $\bar{A}B + A\bar{B}$
- (d) $(\overline{A * B}) * (\overline{A * B})$

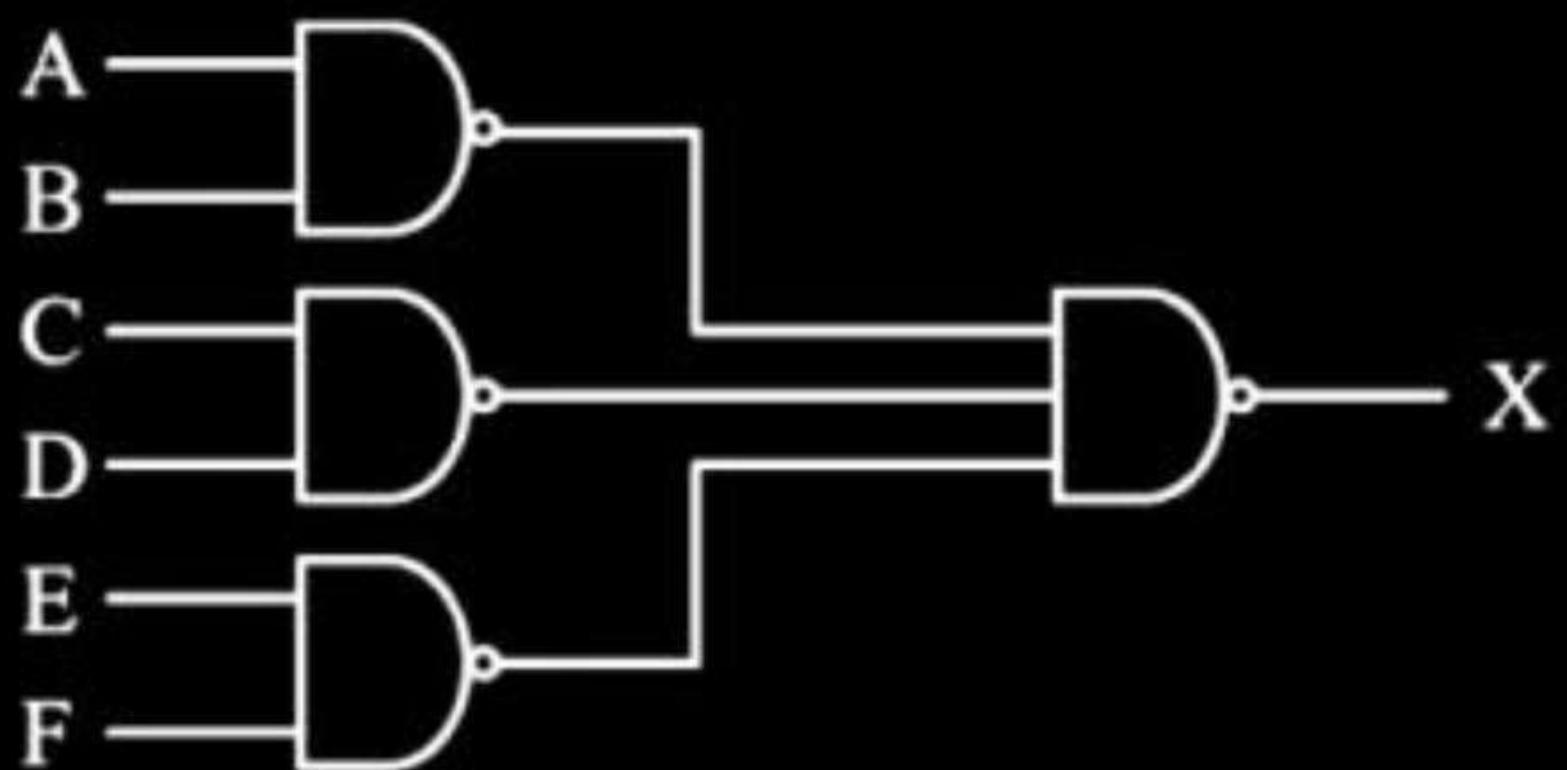
#Q. Which of the following are universal gates

1. NAND
2. NOR
3. XOR

Select the correct answer from the codes given below:

- (a) 1 and 2 only
- (b) 1 and 3 only
- (c) 2 and 3 only
- (d) 1, 2 and 3

#Q.



The output X of the above logic circuits is

- (a) $AB + CD + EF$
- (b) $\overline{AB} + \overline{CD} + \overline{EF}$
- (c) $(A + B)(C + D)(E + F)$
- (d) $\overline{(A + B)} + \overline{(C + D)} + \overline{(E + F)}$

#Q.

Assertion (A) : When all inputs of a NAND-gate are shorted to get a one input, one output gate, it becomes an inverter.

Reason (R) : When all inputs of a NAND - gate are at logic '0' level, the output is at logic ' 1 ' level

#Q.

In NOR - NOR configuration, the minimum number of NOR gates needed to implement the switching function $X + X\bar{Y} + X\bar{Y}Z$ is

- (a) 5
- (b) 3
- (c) 2
- (d) 0

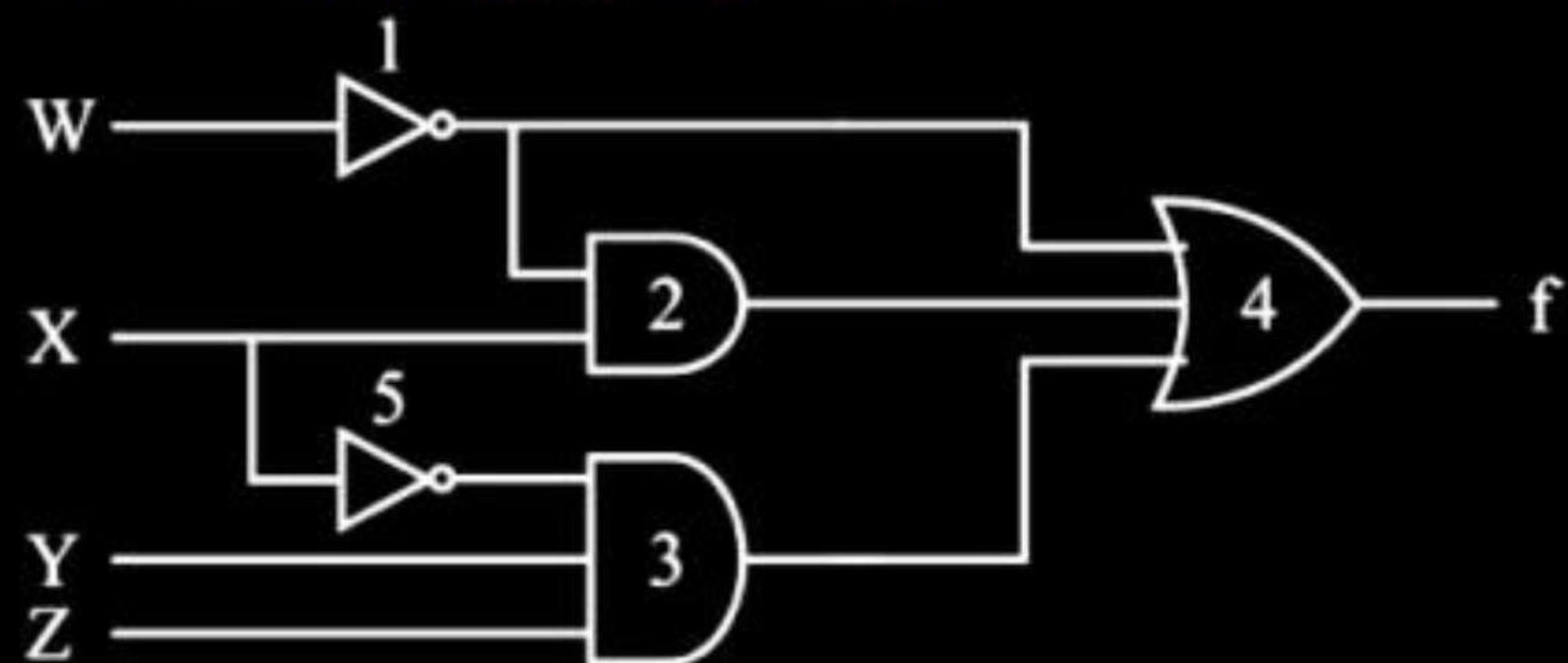
#Q. Which of the following are universal gate?

- 1. AND 2. NAND
 - 3. OR 4. NOR
 - 5. NOT
-
- (a) 1, 2, 3, 4 and 5
 - (b) 1, 3 and 4 only
 - (c) 2, 3 and 5 only
 - (d) 2 and 4 only

#Q. The logic function; $\text{Out} = ab + be + ca$ defines :

1. The output of a 3-input XOR gate
 2. The output of a 3-input majority gate
 3. The sum output of a full adder
 4. The carry output of a full adder
- | | |
|-------------|-------------|
| (a) 1 and 2 | (b) 2 and 3 |
| (c) 3 and 4 | (d) 2 and 4 |

#Q. Consider the following gate network:



Which one of the following gates is redundant?

- (a) Gate No. 1 (b) Gate No. 2
- (c) Gate No. 3 (d) Gate No. 4

#Q.

The minimum number of NAND gates required to implement $A + A\bar{B} + A\bar{B}C$ is equal to

- (a) Zero
- (b) 1
- (c) 4
- (d) 7

#Q.

Statement (I) : A NAND gate represents a universal logic family.

Statement (II) : Only two NAND gates are sufficient to accomplish any of the basic gates.

#Q.

The minimum number of gates required to realize the function $AB + \bar{C}$ (Using NAND gates only) is

- (a) 2
- (b) 3
- (c) 4
- (d) 6

#Q.

Which one of the following statements is correct?

- (a) TTL logic cannot be used in digital circuits
- (b) Digital circuits are linear circuits
- (c) AND gate is a logic circuit whose output is equal to its highest input.
- (d) In a four-input AND circuits, all inputs must be high for the output to be high.

#Q. The output of a NOR gate is

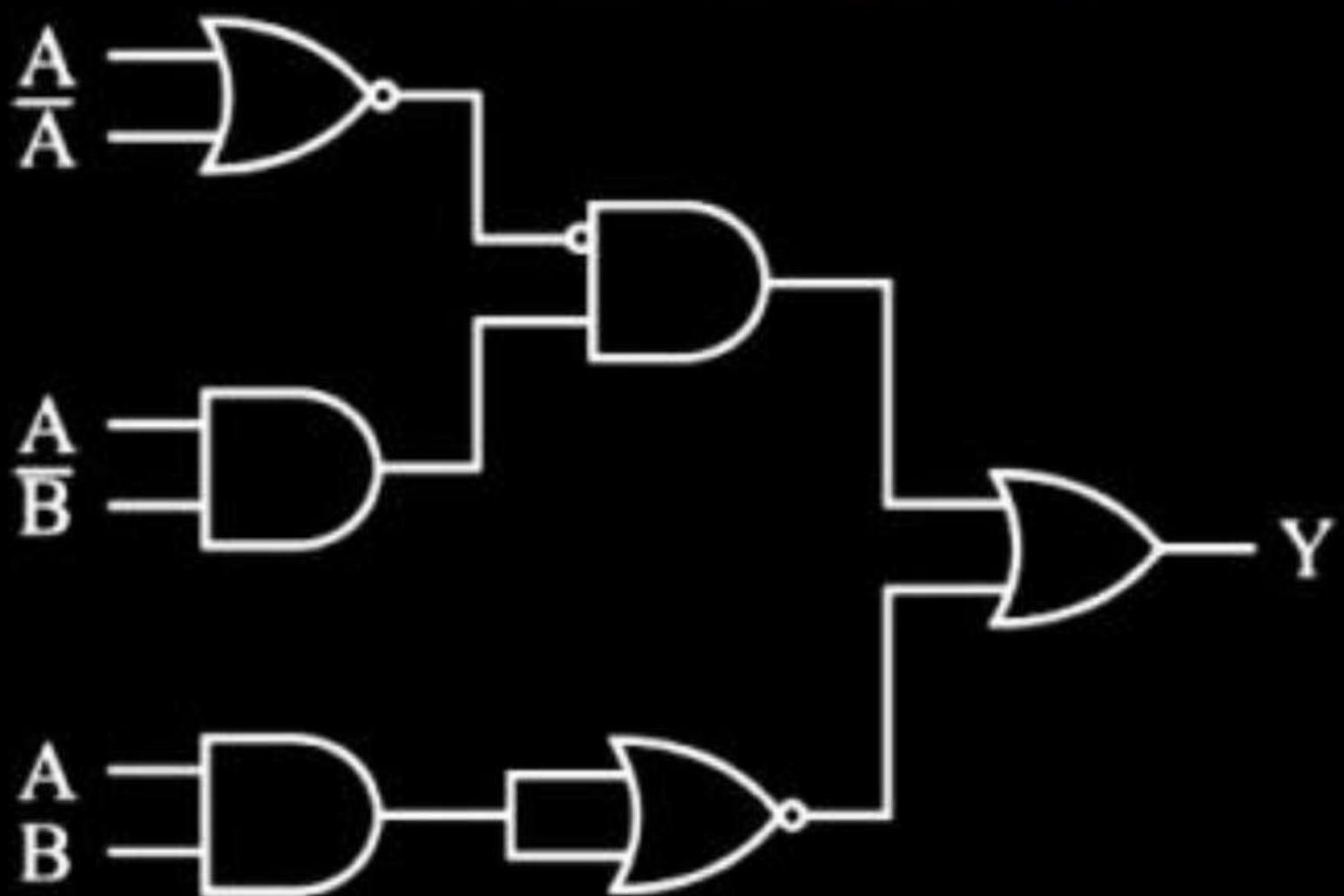
- (a) high if all of its inputs are high
- (b) low if all of its inputs are low
- (c) high if all of its inputs are low
- (d) high if only one of its inputs is low

#Q.

Statement (I) : The maximum number of logic gate inputs that can be driven from the output of a single logic gate is called ‘fan-out’ .

Statement (II) : ‘Fan-out’ is due to the current sourcing when the output is high, and is due to the current sinking when the output is low. Thus two different values for ‘fan-out’ may result.

#Q. What is the output Y for the logic circuit shown in the figure?



- (a) $A\bar{B} + \bar{A}B$
- (b) $A\bar{B} + \bar{A} + \bar{B}$
- (c) $\bar{A}\bar{B} + \overline{AB}$
- (d) $\bar{A} + \bar{B}$

Thank you
GW
Soldiers!



Electronics and Communication Engineering And CSE



Digital Electronics

Digital Logic

Lecture 02

By- CHANDAN JHA SIR





Topics to be Covered

- 1. Boolean Algebra
- 2. Karnaugh Map
-
-
-
-
-

$$\cancel{A+B}C = (A+B)(A+C)$$

$$\overline{ABC} = \bar{A} + \bar{B} + \bar{C}$$

$$\underline{AB} + \underline{\bar{A}}C + BC = AB + \bar{A}C$$

$$\overline{A+B+C} = \bar{A} \cdot \bar{B} \cdot \bar{C}$$

$$(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$$

$$(A+B)(\bar{A}+C) = \bar{A}B + AC$$

	$A \bar{B} C$	\bar{B}	B
	\bar{A}		
A	0	1	
	2	3	

	$A \bar{B} C$	$\bar{B} \bar{C}$	$\bar{B} C$	$B \bar{C}$	$B \bar{C}$
	\bar{A}	00	01	11	10
	0				
	1				
A	0	0	1	3	2
	4	5	7	6	

		$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	CD
		00	01	11	10
$\bar{A}\bar{B}$	00	0	1	3	2
$\bar{A}B$	01	4	5	7	6
$A\bar{B}$	11	12	13	15	14
$A\bar{B}$	10	8	9	11	10

Minimization Rule

Try to make Less number of groups and Bigger group.

$16 = 2^4 \rightarrow$ 4 Variable Reduce

$8 = 2^3 \rightarrow$ 3 Variable Reduce

$4 = 2^2 \rightarrow$ 2 Variable Reduce

$2 = 2^1 \rightarrow$ 1 Variable Reduce

$1 = 2^0 \rightarrow$ 0 Variable Reduce

#Q. The function shown in the figure when simplified will yield a result with

✓ SOP \rightarrow 7 terms

POS \rightarrow 8 terms

		AB	CD			
		00	01	11	10	
		00	1	0	1	0
		01	0	1	0	0
		11	1	0	1	0
		10	0	1	0	1

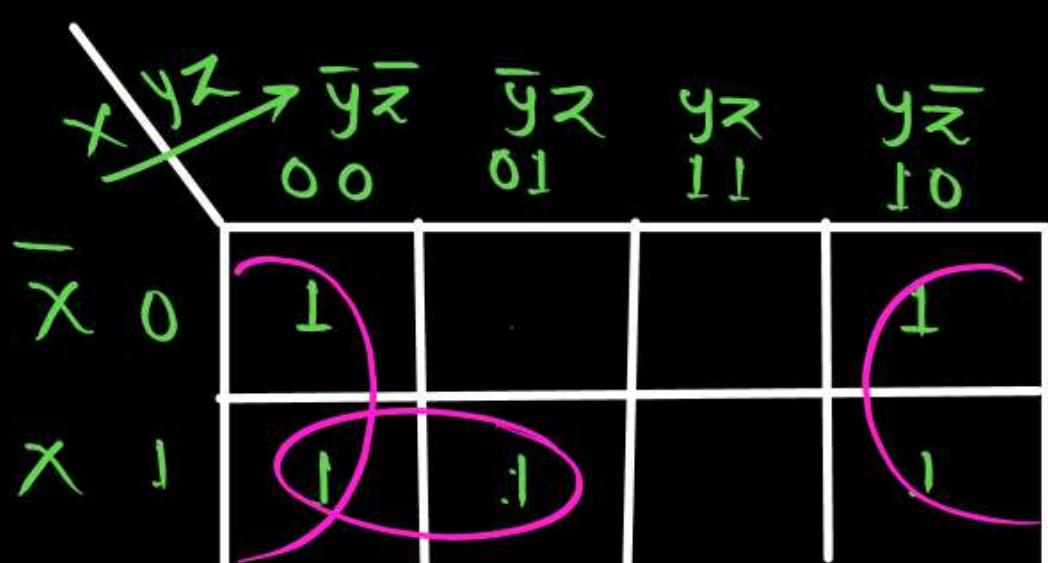
- (a) 2 terms
~~(c) 7 terms~~

- (b) 4 terms
(d) 16 terms

#Q. Simplify Boolean function represented in sum of product of min-terms,

$$F(x, y, z) = \Sigma(0, 2, 4, 5, 6)$$

- (a) ~~$z' + xy'$~~
- (b) $x'y'z' + xyz + xy'z'$
- (c) $xyz + x' + y' + z'$
- (d) $xy + yz + zx$



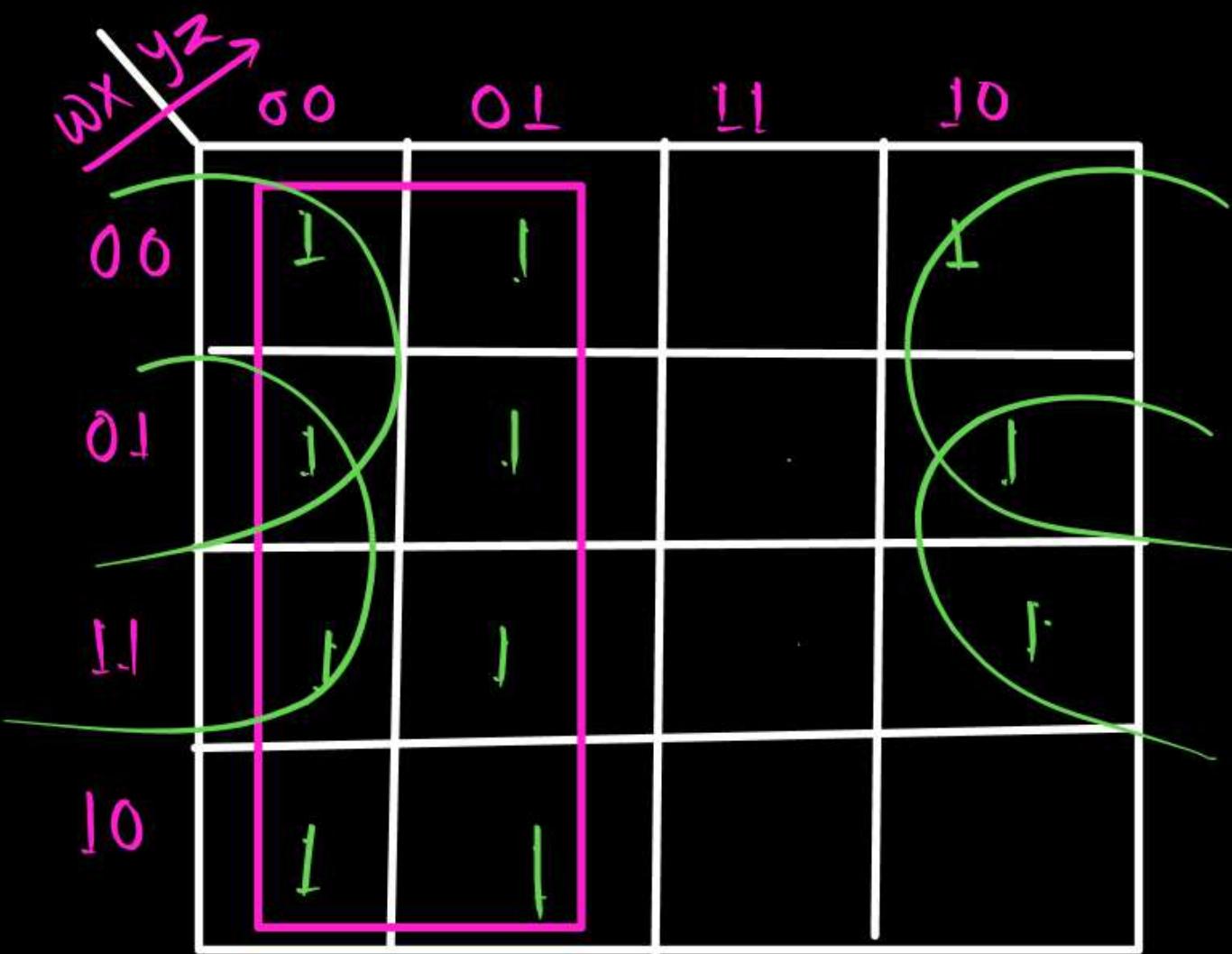
$$\bar{z} + x\bar{y}$$

#Q. Simplify the Boolean expression:

$$F(w, x, y, z) = \Sigma(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$$

- (a) $w + x + y + z$
- ~~(b) $y' + w'z' + xz'$~~
- (c) $y + w'z' + xz$
- (d) $x + z'w'y + x'$

$$\bar{y} + \bar{w}\bar{z} + x\bar{z}$$



#Q.

The Boolean function $\underbrace{(x+y)(\bar{x}+z)(y+z)}$ is equal to which one of the following expressions ?

- (a) $(x+y)(y+z)$
- (b) $(\bar{x}+z)(y+z)$
- (c) $(x+y)(\bar{x}+z)$
- (d) $(x+y)(y+\bar{z})$

→ Consensus Theorem

$$(x+y)(\bar{x}+z)$$

#Q.

$$AB + \bar{A}C = (A + C)(\bar{A} + B)$$

Which one of the following is the dual form of the Boolean identity given above?

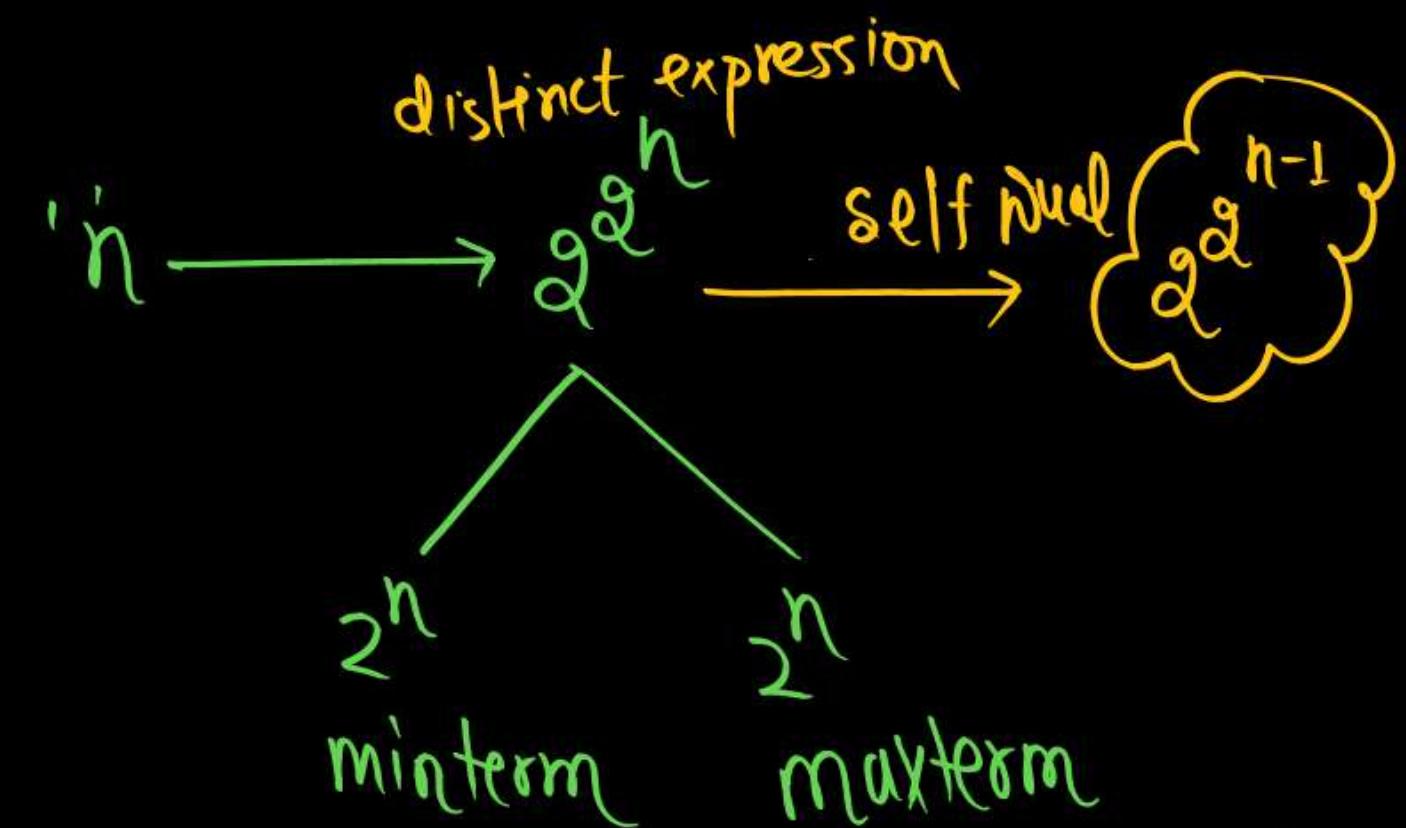
(a) $AB + \bar{A}C = AC + \bar{A}B$

(b) $(A + B)(\bar{A} + C) = (A + C)(\bar{A} + B)$

~~(c)~~ $(A + B)(\bar{A} + C) = AC + \bar{A}B$

(d) $AB + \bar{A}C = AB + \bar{A}C + BC$

$$(A+B)(\bar{A}+C) = AC + \bar{A}B$$



#Q. What does the Boolean expression

$$\underline{AD + ABCD + ACD} + \underline{\bar{A}B + \bar{A}\bar{B}}$$

on minimization result into?

- (a) $A + D$
- (b) $AD + \bar{A}$
- (c) AD
- (d) ~~$\bar{A} + D$~~

$$\begin{aligned} & AD[1 + BC + C] + \bar{A}[B + \bar{B}] \\ & AD + \bar{A} = (A + \bar{A})(\bar{A} + D) \\ & = \bar{A} + D \end{aligned}$$

#Q. If A and B are Boolean variables, then what is $(A + B) \cdot (A + \bar{B})$ equal to? 

- (a) B
- ~~(b) A~~
- (c) A + B
- (d) AB

$$A + BC = (A + B)(A + C)$$

$$A + B \cdot \bar{B} = (A + B)(A + \bar{B})$$

A

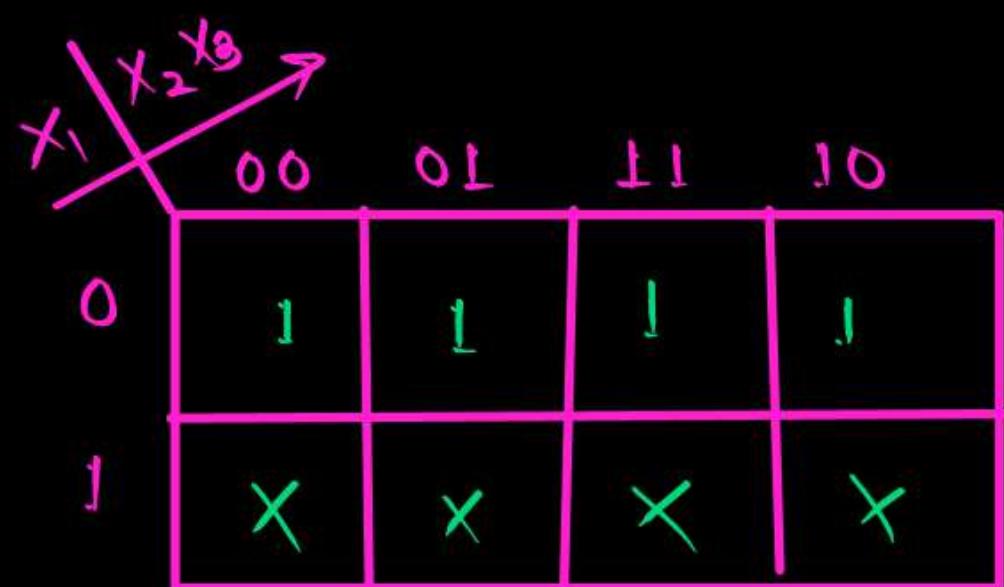
time/cj sir

#Q. When the Boolean function

$$F(X_1X_2X_3) = \sum(\underline{0, 1, 2, 3}) + \sum \phi (\underline{4, 5, 6, 7})$$

is minimized, what does one get?

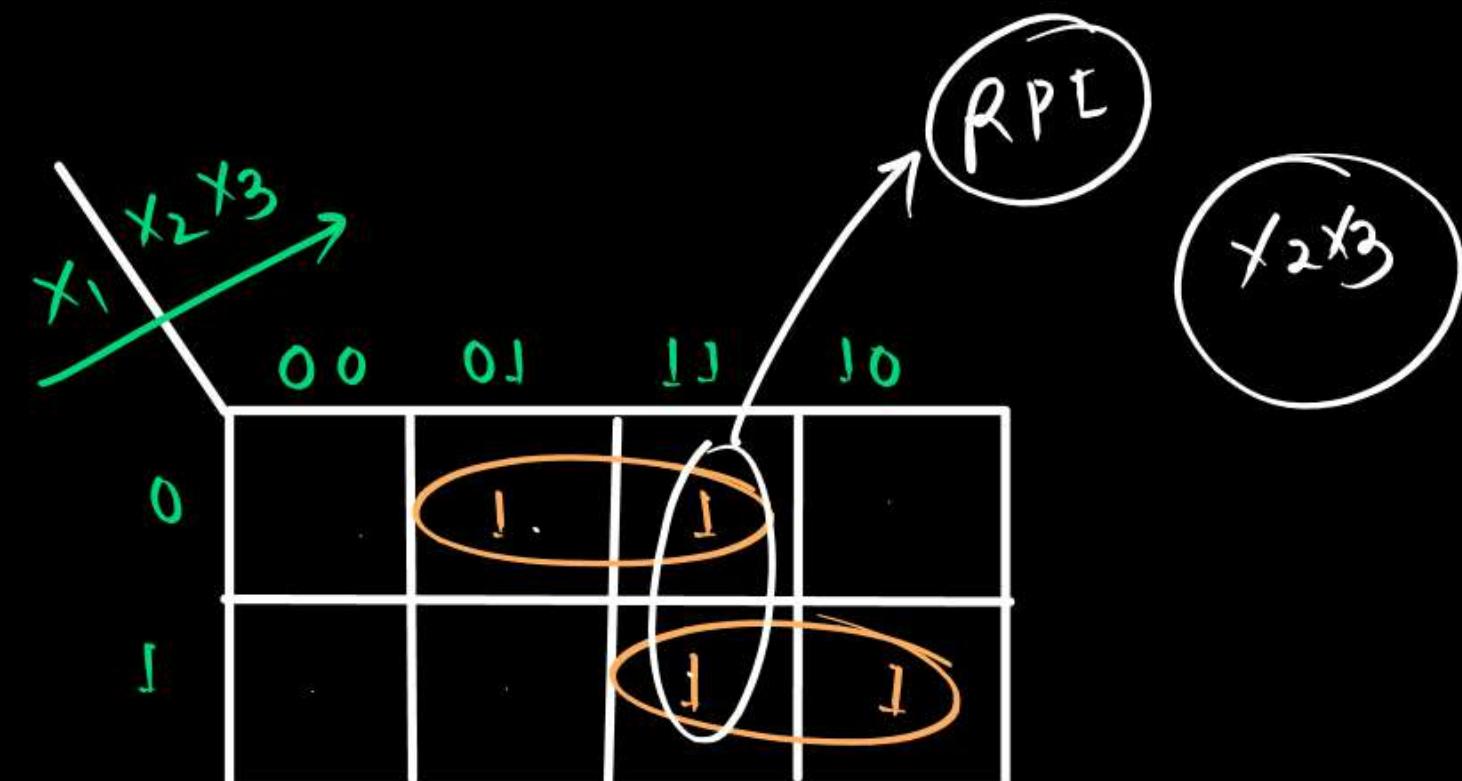
- (a) 1
(b) 0
(c) X_1
(d) X_3



#Q.

By inspecting the Karnaugh map plot of the switching function $F(X_1 X_2 X_3) = \Sigma (1, 3, 6, 7)$ can say that the redundant prime implicant is

- (a) $\bar{X}_1 X_3$
- (b) ~~$X_2 X_3$~~
- (c) $X_1 X_2$
- (d) X_3



#Q.

 f \bar{f}

Match List-I (Boolean Logic Function) with List-II (Inverse of Function) and select the correct answer using the code given below the lists:

List-I

$$ab[1+c] + bc + ca$$

A. $ab + bc + ca + abc$

B. $ab + \bar{a}\bar{b} + \bar{c}$ $f = ab + bc + ac$

C. $a + bc$

D. $(\bar{a} + \bar{b} + \bar{c})(a + \bar{b} + \bar{c})(\bar{a} + \bar{b} + c)$

List-II

1. $\bar{a}(\bar{b} + \bar{c})$

2. $\bar{a}\bar{b} + \bar{b}\bar{c} + \bar{c}\bar{a}$

3. $(a \oplus b)c$

4. $abc + \bar{a}bc + ab\bar{c}$

Codes:	A	B	C	D
(a)	3	2	1	4
(b)	2	3	1	4
(c)	3	2	4	1
• (d)	2	3	4	1

$$\bar{f} = \overline{a+b+c} = \bar{a} \cdot (\bar{b} + \bar{c})$$

$$\bar{f} = \overline{ab+bc+ac}$$

$$= (\bar{a}+\bar{b})(\bar{b}+\bar{c})(\bar{a}+\bar{c})$$

$$= (\bar{a}\bar{b} + \bar{a}\bar{c} + \bar{b}\bar{c} + \bar{b}\bar{c}) (\bar{a} + \bar{c})$$

$$= \bar{b} [\bar{a} + \bar{c}] + \bar{a}\bar{c}] \{ \bar{a} + \bar{c} \}$$

$$= \{ \bar{b} + \bar{a}\bar{c} \} \{ \bar{a} + \bar{c} \}$$

$$= \bar{a}\bar{b} + \bar{a}\bar{c} + \bar{b}\bar{c}$$

.....

#Q.

Consider the following statements:

1. Minimization using Karnaugh map may not provide unique solution.
2. Redundant grouping in Karnaugh map may result in non-minimized solution.
3. Don't care states if used in Karnaugh map for minimization, the minimal solution is not obtained.

Which of the statements given above are correct?

- (a) 1, 2 and 3 (b) 2 and 3 only
(c) 1 and 3 only ~~(d) 1 and 2 only~~

		1	1	
1	X	X		

#Q.

The Boolean functions can be expressed in canonical SOP (Sum Of Products) and POS (Product Of Sums) form. For the functions, $Y = A + \bar{B}C$

Which are such two forms

- (a) $Y = \Sigma(1, 2, 6, 7)$ and $Y = \Pi(0, 2, 4)$
- (b) ~~$Y = \Sigma(1, 4, 5, 6, 7)$ and $Y = \Pi(0, 2, 3)$~~
- (c) $Y = \Sigma(1, 2, 5, 6, 7)$ and $Y = \Pi(0, 1, 3)$
- (d) $Y = \Sigma(1, 2, 4, 5, 6, 7)$ and $Y = \Pi(0, 2, 3, 4)$

$$Y = \begin{matrix} 1 & 0 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{matrix} \quad \begin{matrix} 0 & 0 & 1 \\ 1 & 0 & 1 \end{matrix}$$

$$\begin{matrix} \Sigma m(1, 4, 5, 6, 7) \\ \Pi M(0, 2, 3) \end{matrix}$$

$$Y = A + \bar{B}C$$

$$Y = A(\bar{B} + B)(\bar{C} + C) + (\bar{A} + A)BC$$

$$= A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC + \bar{A}BC + ABC$$

100 101 110 111 011 111

#Q.

The Boolean function $A + BC$ is a reduced form of which one of the following

- (a) $AB + BC$
- (b) $\bar{A}B + A\bar{B}C$
- ~~(c) $(A + B) \cdot (A + C)$~~
- (d) None of the above

#Q. Which one of the following statements is not correct?

- (a) $X + \bar{X}Y = X$ ✗
- (b) $X(\bar{X} + Y) = XY$ ✓
- (c) $XY + X\bar{Y} = X$ ✓
- (d) $ZX + Z\bar{X}Y = ZX + ZY$ ✓

#Q. Which of the following Boolean algebra rules is correct?

- (a) $A \cdot \bar{A} = 1$ ✗
- (b) $A + AB = A + B$ ✗
- ~~(c) $A + \bar{A}B = A + B$~~ ✓
- (d) $A(A + B) = B$ ✗

#Q.

What are the ultimate purposes of minimizing logic expressions?

1. To get a small size expression
2. To reduce the number of variables in the given l expression
3. To implement the function of the logic expression with least hardware
4. To reduce the expression for making it feasible for hardware implementation.

Select the correct answer from the codes given below.

- | | |
|-----------------------|-------------|
| (a) 1 only | (b) 2 and 3 |
| (c) 3 only | (d) 3 and 4 |

#Q. The Boolean expression

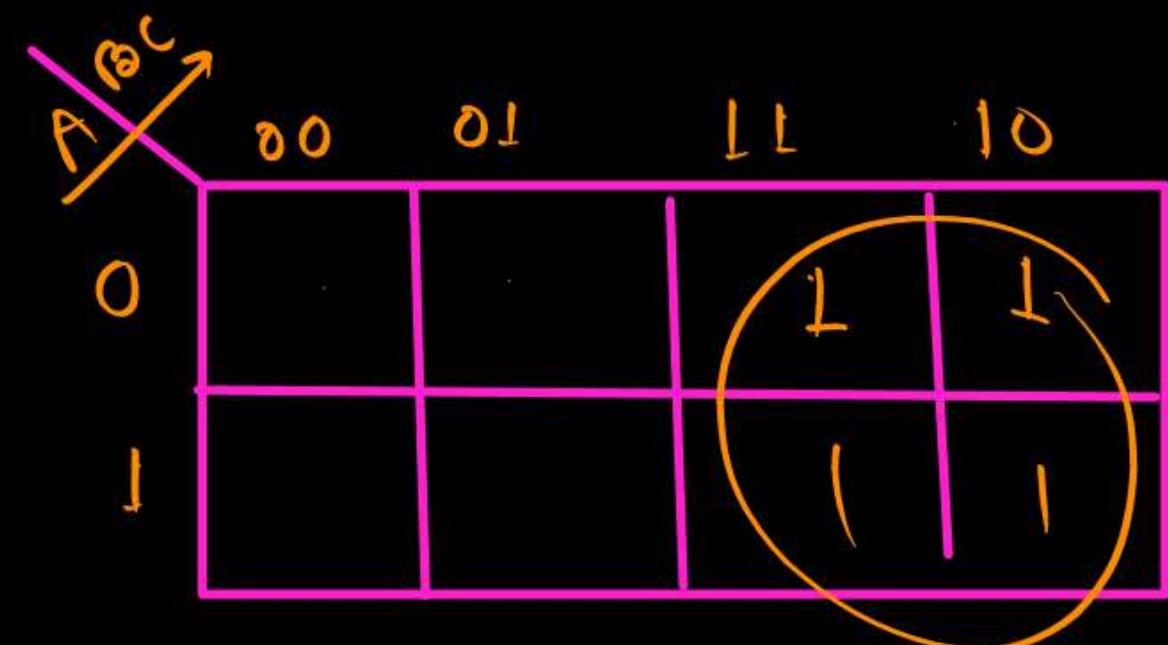
$$\overline{A + \bar{B} + C} + \overline{\bar{A} + \bar{B} + C} + \overline{A + \bar{B} + \bar{C}} + ABC$$

reduces to

- (a) A
- (b) B
- (c) C
- (d) $A + B + C$

$$\bar{A}B\bar{C} + AB\bar{C} + \bar{A}BC + ABC$$

$$\bar{A}B\bar{C} + AB\bar{C} + \bar{A}BC + ABC$$



$$B =$$

#Q. The standard SOP expression for Boolean expression $A\bar{B} + AC + \bar{B}C$ is :

(a) ~~$A\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + ABC$~~

(b) $AB\bar{C} + \bar{A}BC + ABC$

(c) $A\bar{B}C + AB\bar{C} + ABC$

(d) $\bar{A}\bar{B}C + AB\bar{C} + A\bar{B}\bar{C}$

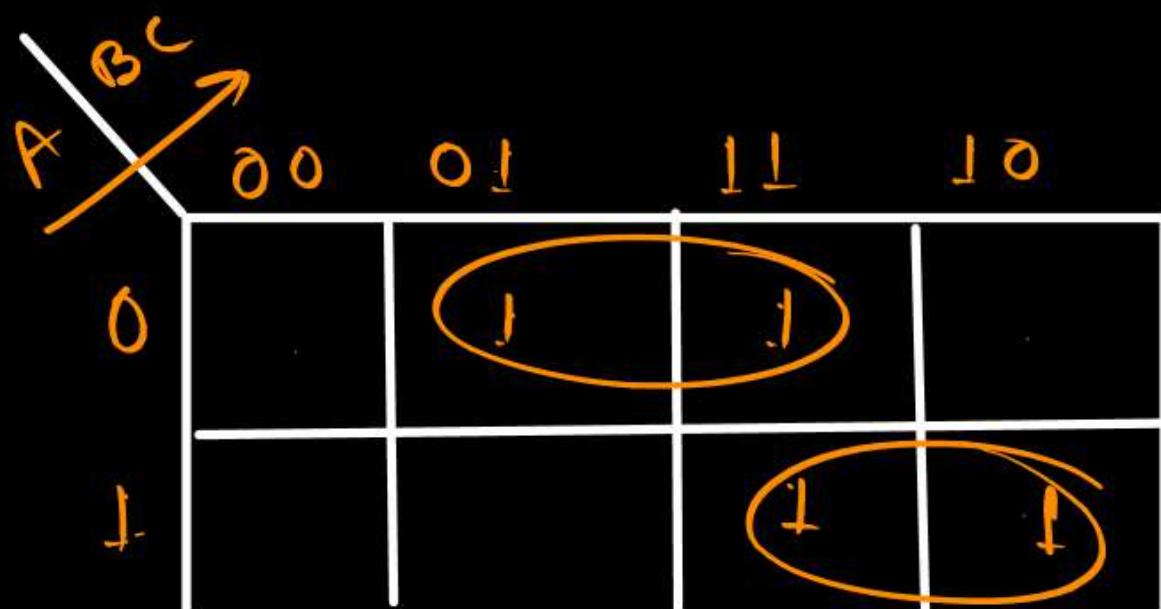
$$A\bar{B} + BC$$

$$A\bar{B}\bar{C} + A\bar{B}C + \bar{A}B\bar{C} + ABC$$

#Q. The complement of the expression $Y = ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}BC$

is :

- (a) $(A + \bar{B})(A + \bar{C})$
- (b) $(\bar{A} + B)(A + C)$
- (c) $(A + \bar{B})(\bar{A} + C)$
- ~~(d) $(\bar{A} + \bar{B})(A + \bar{C})$~~



$$f = \bar{A}C + AB$$

$$\bar{f} = (\bar{A} + \bar{C}) \cdot (\bar{A} + \bar{B})$$

#Q. The logic function $f = \overline{x \cdot \bar{y} + \bar{x} \cdot y}$ is the same as

(a) $f = (x+y)(\bar{x}+\bar{y}) = x \oplus y$

$$f = \overline{x \oplus y} = x \odot y = \bar{x}\bar{y} + x\bar{y}$$

~~(b)~~ $f = \overline{(\bar{x}+\bar{y})(x+y)} = \overline{x \oplus y} = x \odot y$

$$\left\{ \begin{array}{l} (\bar{x}+\bar{y})(\bar{x}+y) \\ (x+y)(\bar{x}+y) \end{array} \right.$$

(c) $f = \overline{(x \cdot y)}(\bar{x} \cdot \bar{y})$

(d) None of the above

$$x \oplus y = \left\{ \begin{array}{l} \bar{x}y + x\bar{y} \\ (\bar{x}+y) \cdot (x+y) \end{array} \right.$$

#Q.

If the Boolean expression $\bar{P}Q + QR + PR$ is minimized, the expression becomes

- (a) $\bar{P}Q + QR$
- ~~(b) $\bar{P}Q + PR$~~
- (c) $QR + PR$
- (d) $\bar{P}Q + QR + PR$

$$\bar{P}Q + PR$$

#Q.

Match List - I with List - II and select the correct answer using the code given below the lists :

List-I

- A. AND gate
- B. OR gate
- C. NOT gate

List-II

- 1. Boolean complementation
- 2. Boolean addition
- 3. Boolean multiplication

	Codes :	A	B	C
(a)	3	1	2	
(b)	1	2	3	
(c)	3	2	1	
(d)	1	3	2	

#Q. The Boolean equation $X = [(A + \bar{B})(B + C)]B$ can be simplified to

(a) $X = \bar{A}B$

$$X = (AB + AC + \bar{B}C)B$$

(b) $X = A\bar{B}$

$$X = AB + ABC$$

~~(c)~~ $X = AB$

$$X = AB(H)$$

(d) $X = \bar{A}\bar{B}$

$$X = AB$$

#Q. The correct expression is

- ✓ (a) $\bar{A}B + A\bar{B} = \overline{AB}(A + B)$
- ✗ (b) $\bar{A}B + \bar{A}\bar{B} = AB(\bar{A} + \bar{B})$
- ✗ (c) $\bar{A}B + A\bar{B} = AB(\bar{A} + \bar{B})$
- ✗ (d) $\bar{A}B + \bar{A}\bar{B} = \overline{AB}(A + B)$

$$(\bar{A} + \bar{B})(A + B) = A \oplus B = \bar{A}B + A\bar{B}$$

$$(A + \bar{B})(\bar{A} + B) = A \odot B = \bar{A}\bar{B} + AB$$

#Q. Simplified form of the logic expression $(A + \bar{B} + C)(A + \bar{B} + \bar{C})(A + B + C)$

is

- (a) $\bar{A}B + \bar{C}$
- ~~(b) $A + \bar{B}C$~~
- (c) A
- (d) $AB + \bar{C}$

	00	01	11	10
0	0	1	0	0
1	1	1	1	1

$$\underline{\underline{A + \bar{B}C}}$$

#Q. Logic function $(\bar{A} + B)(A + \bar{B})$ can be reduced to

- (a) B
- (b) \bar{B}
- (c) A
- (d) \bar{A}

$$\bar{A}B + A\bar{B} = B(\bar{A} + A)$$

$$= \textcircled{B}$$

#Q. Logic function $\underline{A}\bar{B}D + \underline{A}\bar{B}\bar{D}$ can be reduced to :

- (a) $\bar{A}\bar{B}$
- (b) $A\bar{B}$
- (c) $\bar{B}\bar{D}$
- (d) $A\bar{D}$

#Q. The logic function $f(A, B, C, D) = (\bar{A} + BC)(B + CD)$ can be expressed to:

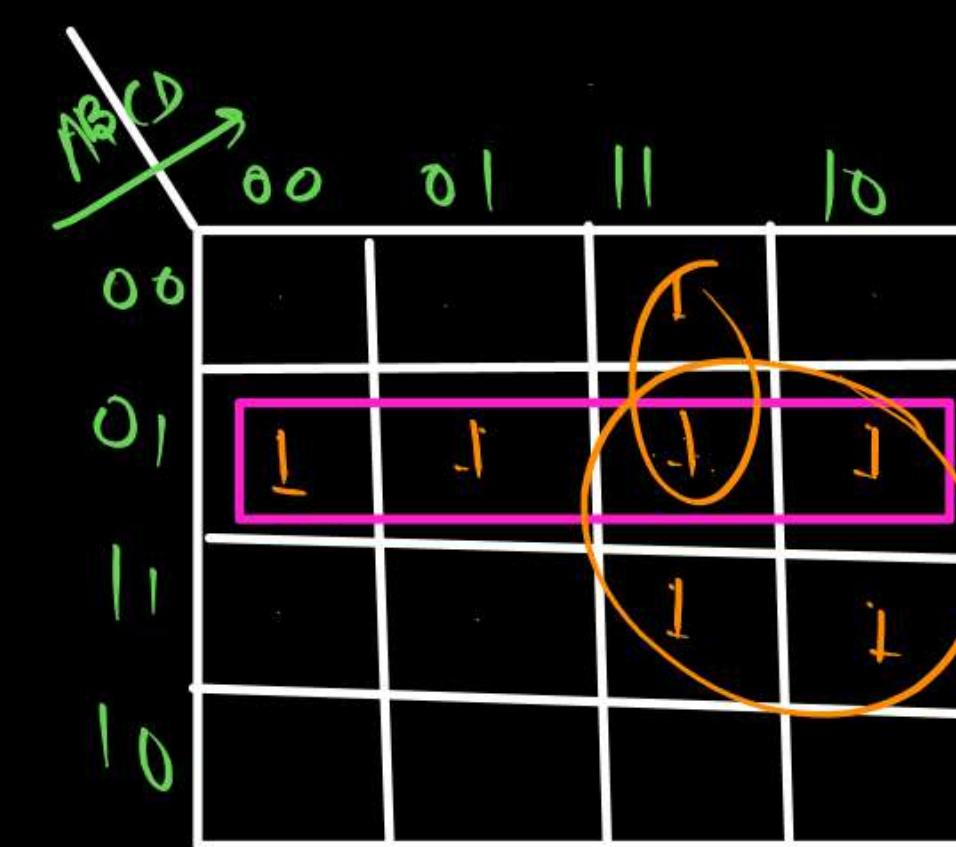
- (a) $\bar{A}B + BC + \bar{A}CD + BCD$
- (b) $AB + A\bar{B} + \bar{A}CD + BCD$
- (c) $AB + \bar{A}\bar{B} + \bar{A}CD + B\bar{C}D$
- (d) $A\bar{B} + \bar{A}B + \bar{A}CD + BCD$

$$\Rightarrow \bar{A}B + \bar{A}CD + BC + BCD$$

0100	0011	0110	0111
0101	0111	0111	1111
0110		1110	
0111		1111	

$\bar{A}B + BC + \bar{A}CD$

→ minimized



#Q. The logic function ($\bar{A} + \bar{B}$) can be expressed in terms of min terms as:

- (a) $A\bar{B} + B\bar{A}$ X
- (b) ~~$\bar{A}B + \bar{B}A + \bar{A}\bar{B}$~~
- (c) $\bar{A}\bar{B} + \bar{A}B$ X
- (d) $AB + \bar{B}A$ X

$$\bar{A}(B + \bar{B}) + \bar{B}A$$

$$\bar{A} + \bar{B}A = \bar{A} + \bar{B}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

$$\bar{A} + \bar{B}$$

#Q. The min terms for $AB + ACD$ are

- (a) $\bar{A}\bar{B}CD + AB\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D} + \bar{A}BCD$
- ~~(b) $AB\bar{C}\bar{D} + AB\bar{C}D + ABC\bar{D} + ABCD + A\bar{B}CD$~~
- (c) $A\bar{B}CD + AB\bar{C}D + ABC\bar{D} + \bar{A}BCD + A\bar{B}C\bar{D}$
- (d) $AB\bar{C}D + A\bar{B}CD + \bar{A}BCD + ABC\bar{D} + \bar{A}\bar{B}CD$

$$AB(C(\bar{C}+\bar{C})(\bar{D}+D)) + A(\bar{B}+\bar{B})(CD)$$

#Q. On simplification of expression

$$Y = \overline{(A \cdot B + \bar{C})(\bar{A} + B + C)}$$

Hb

using Boolean algebra, the solution is

- (a) $(A \cdot B + C)(A + B \cdot C)$
- (b) $(\bar{A} + \bar{B} + \bar{C})(A + B + C)$
- (c) $(A \cdot B + \bar{C})(A \cdot C + \bar{B})$
- (d) $(B \cdot C + \bar{A})(A \cdot B + \bar{C})$

#Q. K-map method of simplification can be applied when the given function is in

- (a) Product of sum form
- (b) Sum of product form
- (c) Canonical form → Each term
- (d) Any form

Should contain all the
Variable.

$$f(A, B, C) = A + \bar{B}C + B\bar{C}$$

#Q. The function $Y = A + \bar{B} \cdot C$ in canonical sum of product form is

- (a) $Y = \Sigma m(1, 3, 5, 6, 7)$
- ~~(b) $Y = \Sigma m(1, 4, 5, 6, 7)$~~
- (c) $Y = \Sigma m(2, 3, 5, 6)$
- (d) $Y = \Sigma m(2, 3, 5, 7)$

$A \ B \ C$	$A \ \bar{B} \ C$
$1 \ 0 \ 0 \rightarrow 4$	$0 \ 0 \ 1 \rightarrow 1$
$1 \ 0 \ 1 \rightarrow 5$	$0 \ 0 \ 0 \rightarrow 0$
$1 \ 1 \ 0 \rightarrow 6$	$1 \ 0 \ 1 \rightarrow 7$
$1 \ 1 \ 1 \rightarrow 7$	

$\{m(1, 4, 5, 6, 7)$

$$\begin{aligned}
 Y &= A(\bar{B}+B)(\bar{C}+C) + (\bar{A}+A)\bar{B}C \\
 &= A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC + \cancel{\bar{A}\bar{B}C} \\
 &= \underline{\Sigma m(1, 4, 5, 6, 7)}
 \end{aligned}$$

#Q.

The simplified form of the Boolean expression $AB + A(B + C) + B(B + C)$ is given by

- (a) $AB + AC$
- (b) $\cancel{B} + AC$
- (c) $BC + AC$
- (d) $AB + C$

$$\begin{aligned} & AB + AB + AC + B + BC \\ & B(A + 1 + C) + AC \\ & \textcircled{B + AC} \end{aligned}$$

#Q.

$$\hat{f}(A, B, C, D)$$

$$\overline{F(A, B, D)}$$

Product of Max terms representation for the Boolean function $\overline{F} = \overline{B}D + \overline{A}D + BD$ is

- (a) $\prod M(1, 3, 5, 7)$
- (b) ~~$\prod M(0, 2, 4, 6)$~~
- (c) $\prod M(0, 1, 2, 3)$
- (d) $\prod M(4, 5, 6, 7)$

A	B	C	D	$\overline{A} \otimes \overline{B} \otimes \overline{C} \otimes D$	$A \otimes B \otimes \overline{C} \otimes \overline{D}$	$A \otimes B \otimes C \otimes D$
0	1	0	1	1	0	001
0	1	1	1	3	0	011
1	1	0	1	9	1	001
1	1	1	1	11	1	101

$$\begin{aligned} F = & \overline{A} \overline{B} D + A \overline{B} D + \overline{A} \overline{B} D + \overline{A} B D \\ & + \overline{A} B D + A B D \end{aligned}$$

$$\sum m(1, 3, 5, 7, 9, 11, 13, 15)$$

$$\prod M(0, 2, 4, 6)$$

#Q. Simplified form of the Boolean expression

$$Y = \overline{(A \cdot B + \bar{C})(\bar{A} + \bar{B} + C)}$$

- (a) $\bar{A}\bar{C} + A\bar{C} + \bar{B}\bar{C} + \bar{B}C$
- (b) ~~$(\bar{A} + \bar{B} + \bar{C})(A + B + C)$~~
- (c) $(\bar{A} + \bar{B})(A + \bar{C})$
- (d) $A(B + C)$

$$Y = \overline{A \cdot B + \bar{C}} + \overline{(\bar{A} + B)} + C$$

$$Y = (\bar{A} + \bar{B}) \cdot C + (A + B) \cdot \bar{C}$$

$$Y = \bar{A}C + \bar{B}C + A\bar{C} + B\bar{C}$$

$$Y = \text{Sum}(1, 3, 5, 4, 6, 2)$$

$$(A + B + C)(\bar{A} + \bar{B} + \bar{C}) \quad \text{TIN}(0, \neq)$$

#Q. What is the function $Y = A + \bar{B}C$ in Product-of-Sums (POS) form?

- (a) $M_6 M_5 M_4 M_3$
- (b) $M_3 M_2 M_1 M_0$
- ~~(c) $M_0 M_2 M_3$~~
- (d) $M_4 M_3 M_2 M_1$

$$\begin{aligned}
 Y &= A + \bar{B}C \\
 &= \begin{array}{r}
 100 \\
 101 \\
 110 \\
 111
 \end{array} \quad \begin{array}{r}
 00 \\
 01 \\
 10 \\
 11
 \end{array} \\
 &= \sum m(1, 4, 5, 6, 7)
 \end{aligned}$$

#Q. The simplification in minimal sum of product (SOP) of

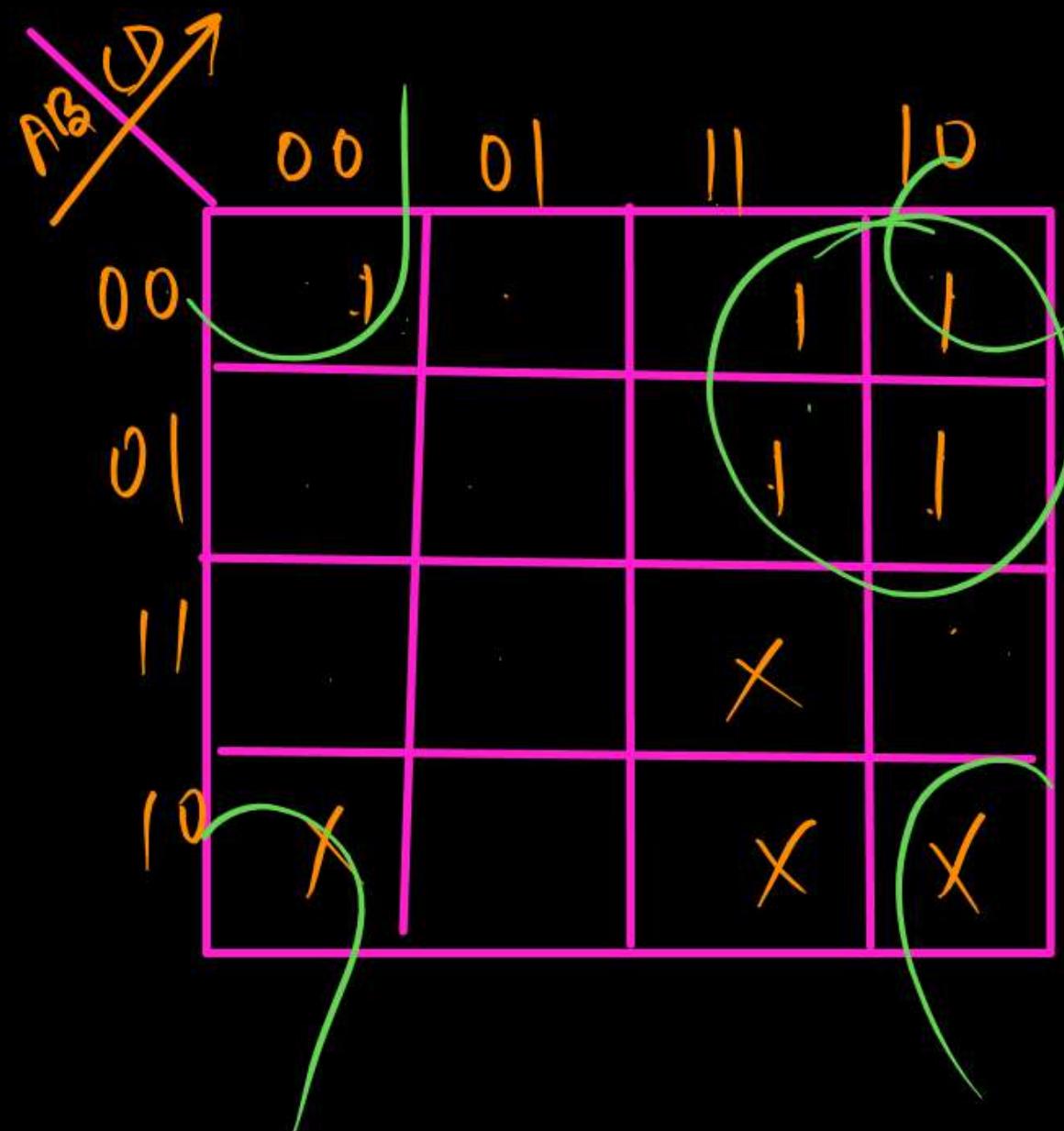
$$Y = F(A, B, C, D)$$

$$= \Sigma m(0, 2, 3, 6, 7) + \Sigma d(8, 10, 11, 15)$$

$$\bar{B}\bar{D} + \bar{A}C$$

using K-maps is

- (a) $Y = AC + B\bar{D}$
- (b) $Y = A\bar{C} + B\bar{D}$
- (c) $Y = \bar{A}\bar{C} + \bar{B}D$
- (d) ~~$Y = \bar{A}C + \bar{B}\bar{D}$~~



#Q. The min-term expansion of

Ans F(A, B, C) = AB + B \bar{C} + A \bar{C} is

- (a) m₂ + m₄ + m₆ + m₁
- (b) m₀ + m₁ + m₃ + m₅
- (c) m₇ + m₆ + m₂ + m₄
- (d) m₂ + m₃ + m₄ + m₅

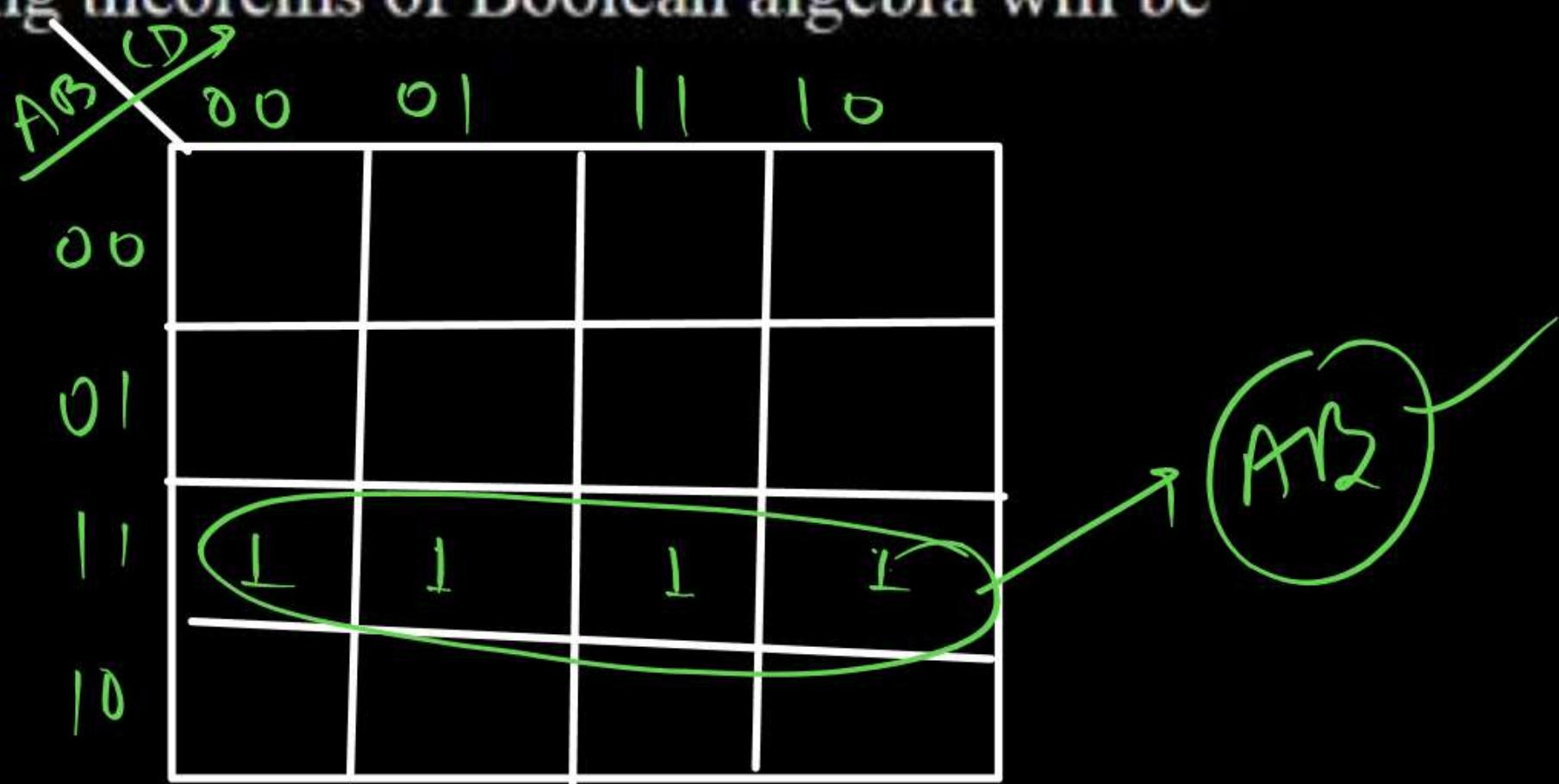
#Q.

Consider the following expression:

$$A \cdot B \cdot C \cdot D + A \cdot B \cdot \bar{C} \cdot \bar{D} + A \cdot B \cdot C \cdot \bar{D} + A \cdot B \cdot \bar{C} \cdot D + A \cdot B \cdot C \cdot D \cdot E + A \cdot B \cdot \bar{C} \cdot \bar{D} \cdot \bar{E} + A \cdot B \cdot \bar{C} \cdot D \cdot E$$

The simplification of this by using theorems of Boolean algebra will be

- (a) $A + B$
- (b) $A \oplus B$
- (c) $(A + B)(A \cdot B)$
- (d) $A \cdot B$



#Q.

An electric power generating station supplies power to three loads A, B and C. Only a single generator is required when any one load is switched on. When more than one load is on, an auxiliary generator must be started. The Boolean equation for the control of switching of the auxiliary generator will be

- (a) $AA + BB + CC$
- (b) $ABC + BCA + CAB$
- (c) $AB + AC$
- (d) $AB + AC + BC$

Hv
~~A~~

#Q. An expression $f = \overline{\overline{AB}} + \overline{A} + AB$ can be reduced to

- (a) A
- (b) B
- (c) 0
- (d) 1

Hw

#Q. K-map is used to minimize the number of

- (a) Flip-flops in digital circuits
- (b) Layout spaces in digital circuits for fabrication
- (c) Functions of 3,4, 5 or 6 variables
- (d) Registers in CPU

✓

#Q. Express the Boolean function $F = A + \bar{B}C$ as a sum of minterms?

- (a) $ABC + \bar{A}\bar{B}C$
- (b) $A\bar{B}C + \bar{A}\bar{B}C + A\bar{B}\bar{C}$
- (c) $ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$
- (d) $AB\bar{C} + A\bar{B}C + \bar{A}\bar{B}\bar{C}$

#Q. The simplified form of the function

$F(A, B, C, D) = \Sigma m(1, 5, 6, 7, 11, 12, 13, 15)$ is

- (a) $\bar{A}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + A\bar{C}D + BD$
- (b) $\bar{A}\bar{C}D + \bar{A}BC + AB\bar{C} + ACD + BD$
- (c) $\bar{A}\bar{C}D + \bar{A}BC + AB\bar{C} + ACD$
- (d) $\bar{A}\bar{C}D + \bar{A}BC + \bar{A}B\bar{C} + ACD$

time/CJSIR

Thank you
GW
Soldiers!



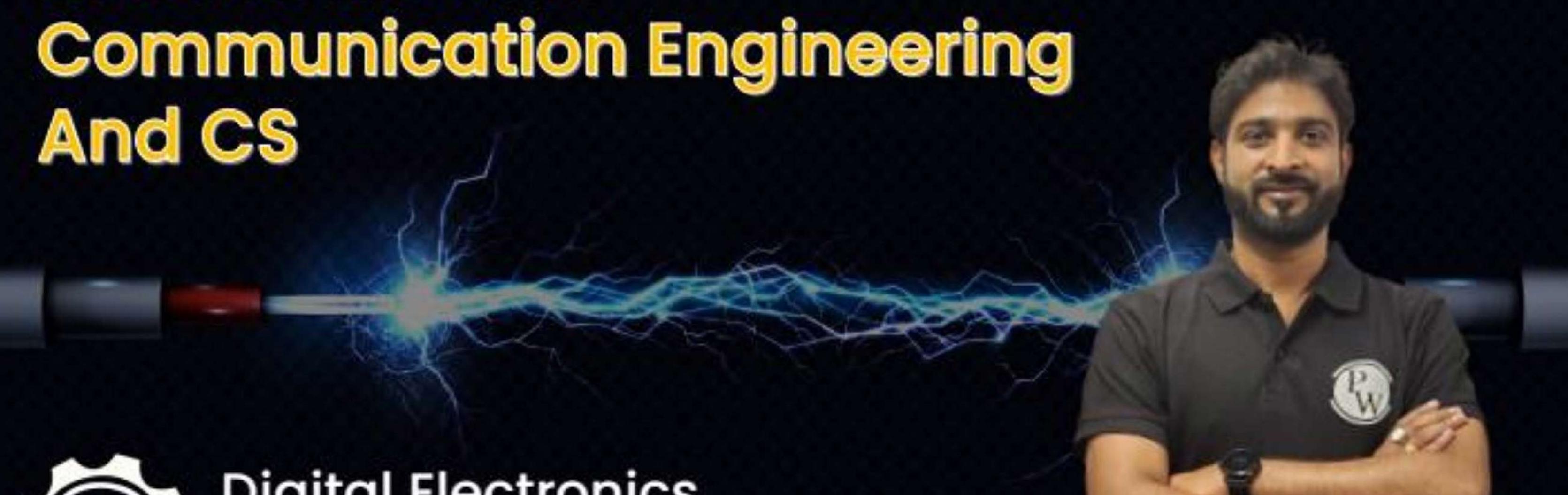
Electronics and Communication Engineering And CS



Digital Electronics

Lecture- 03

Digital Logic



By- CHANDAN JHA SIR



1. Combinational circuit

✓ comparator

MUX

DE-MUX

Encoder

Decoder

HA

FA

H.S.

F.S.

serial adder

parallel adder

LACA

Multiplier

complement Adder | sub.

Design process of combinational circuit

COMPARATOR

"n" bit

$$\text{Total combination} = 2^{2n}$$

$$\text{Equal combination} = 2^n$$

$$\text{Unequal combination} = 2^{2n} - 2^n$$

$$\text{Less} = \text{Greater} = \frac{2^{2n} - 2^n}{2}$$

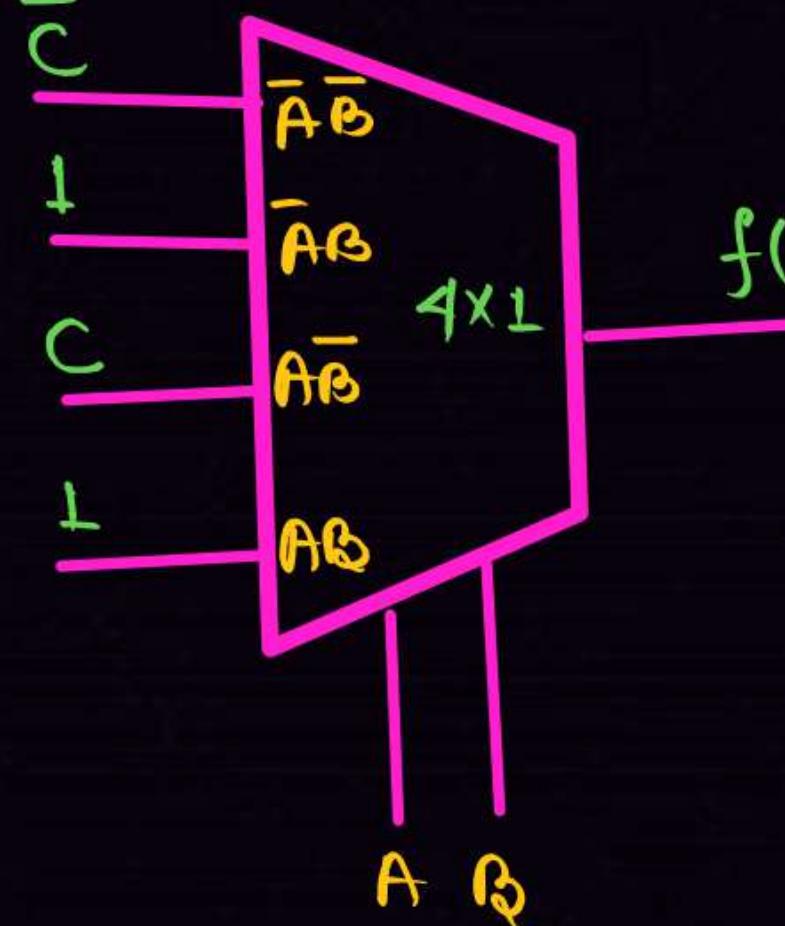
semiminimized expression



$$X(A > B) = A_1 \bar{B}_1 + (A_1 \odot B_1) A_0 \bar{B}_0$$

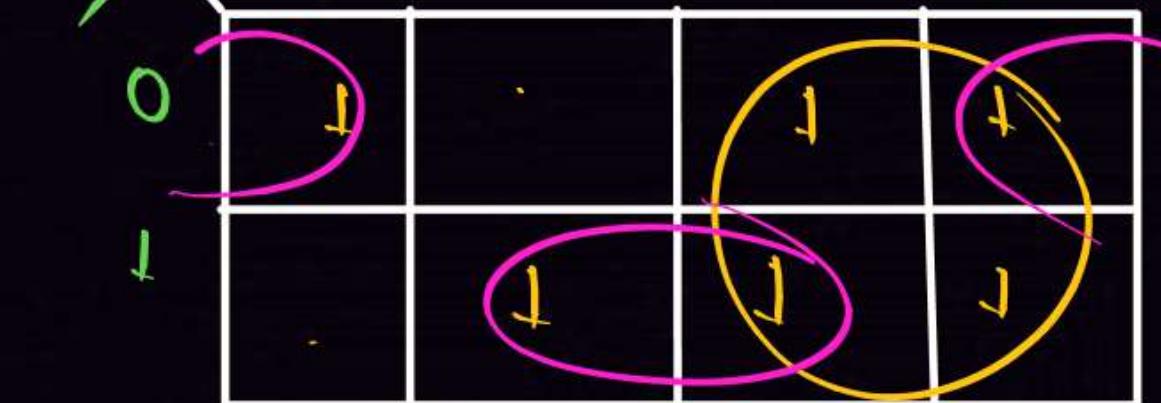
$$Y(A < B) = \bar{A}_1 B_1 + (A_1 \odot B_1) \bar{A}_0 B_0$$

$$Z(A = B) = (A_1 \odot B_1) \cdot (A_0 \odot B_0)$$

MUXEx

$$\begin{aligned}
 f(A, B, C) &= \bar{A}\bar{B}\bar{C} + \bar{A}B + A\bar{B}C + AB \\
 &= \bar{A}\bar{B}\bar{C} + \bar{A}B(\bar{C}+C) + A\bar{B}C + AB(\bar{C}+C) \\
 &= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + AB\bar{C}
 \end{aligned}$$

$$f = \sum m(0, 2, 3, 5, 6, 7)$$

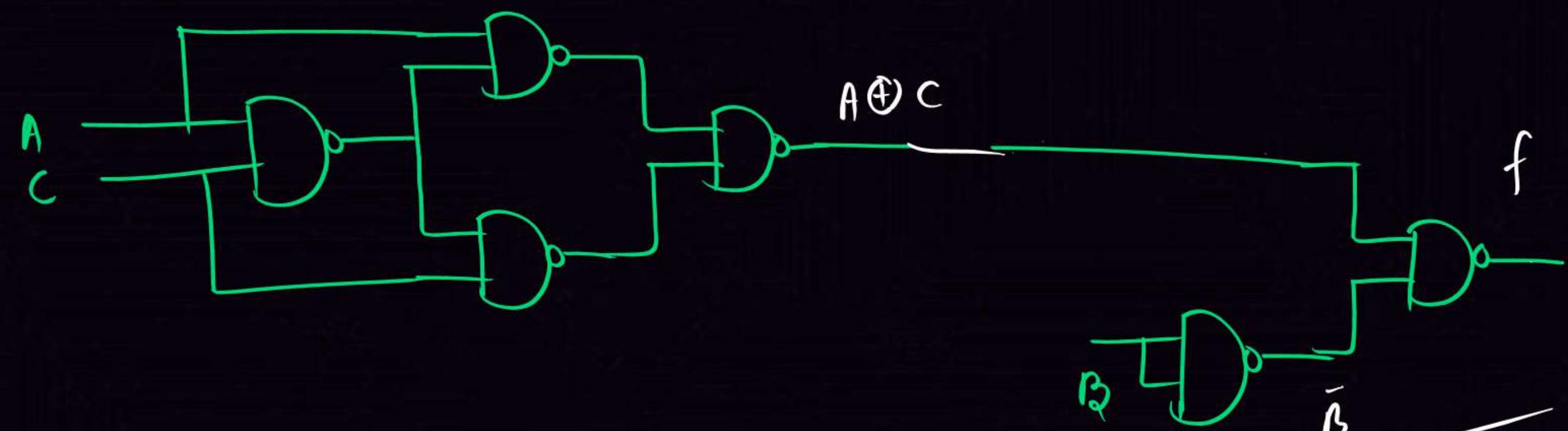


$$= B + \bar{A}\bar{C} + AC$$

$$B + \overline{A} \bar{C} + A C$$

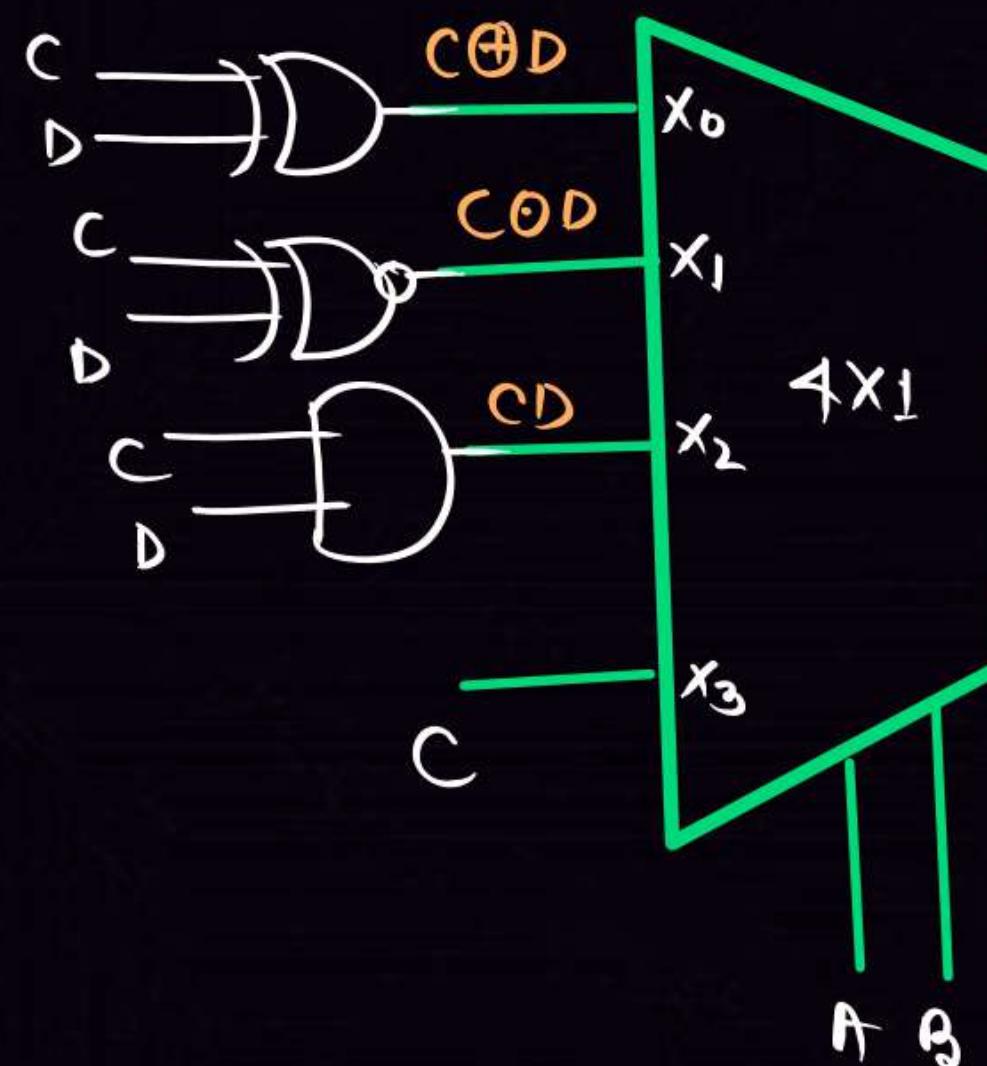
$$B + X$$

Design by NAND GATE
 $X = A \odot C$



$$\text{Ans} = 6_{10}$$

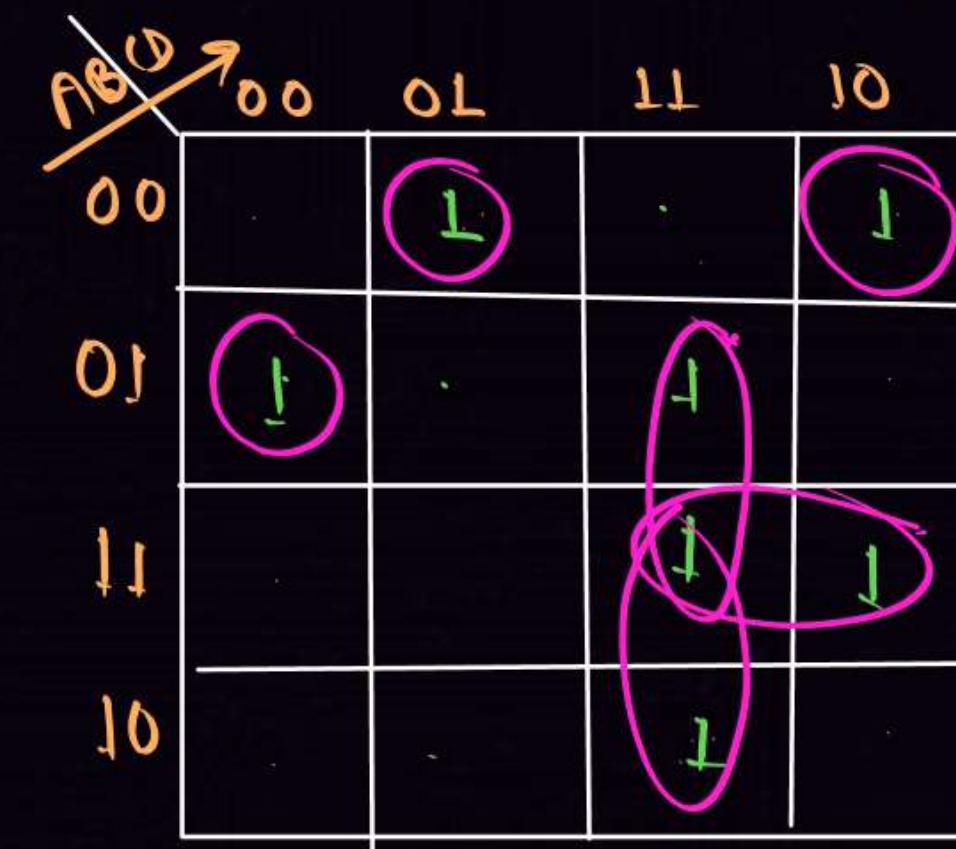
$$\begin{aligned}
 f &= (\overline{A} \oplus C) \cdot \overline{B} \\
 &= B + \overline{\overline{A} \oplus C} = B + A \odot C
 \end{aligned}$$



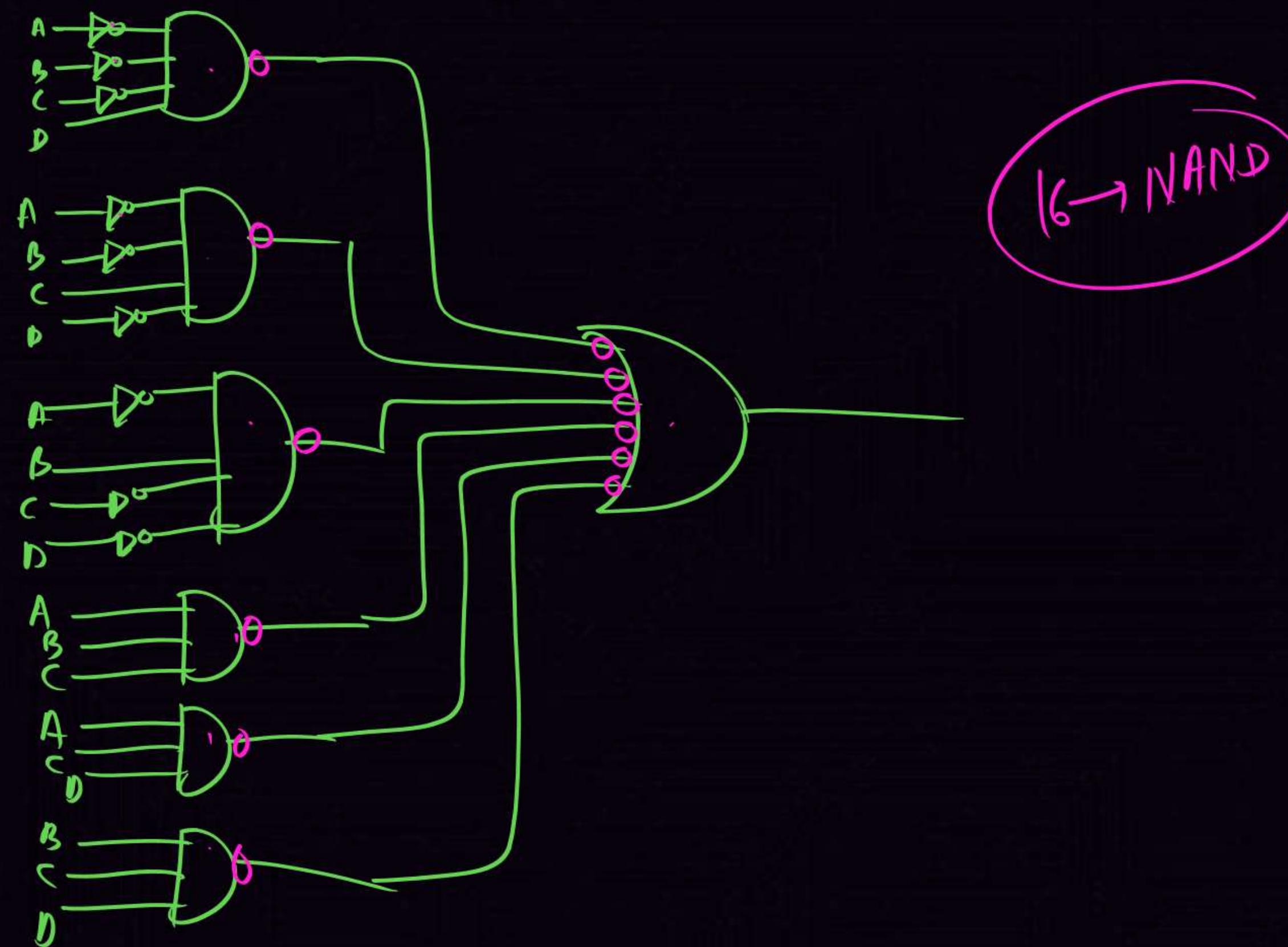
$$\begin{aligned} & \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}CD + \bar{A}B\bar{C}\bar{D} + BCD + ABC \\ & + ABC \end{aligned}$$

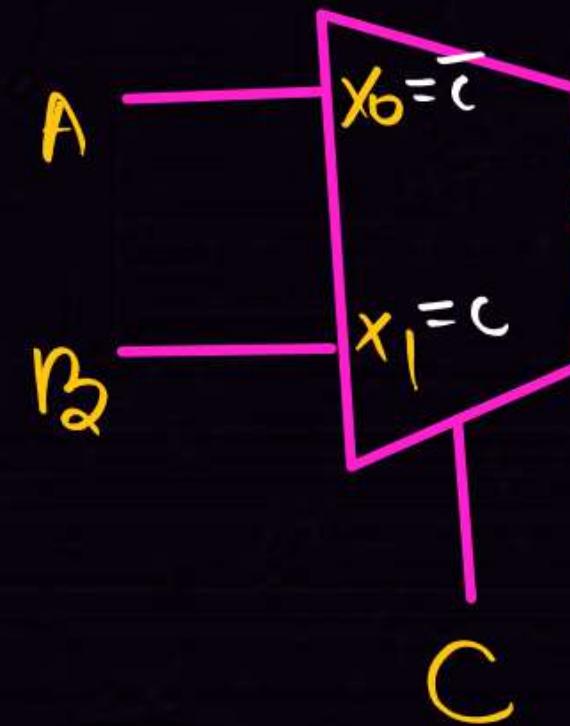
$$\begin{aligned} f(A, B, C, D) &= \bar{A}\bar{B}(\bar{C}D + \bar{C}\bar{D}) + \bar{A}B(\bar{C}\bar{D} + C\bar{D}) + A\bar{B}CD \\ & + ABC \end{aligned}$$

$$= \sum m(1, 2, 4, 7, 11, 14, 15)$$

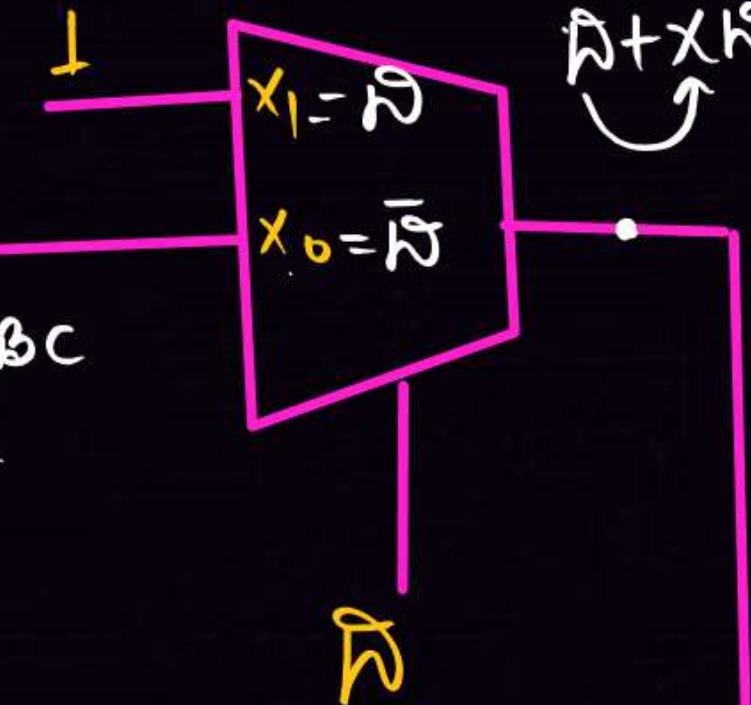


$$\bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}C + ACD + BC\bar{D}$$



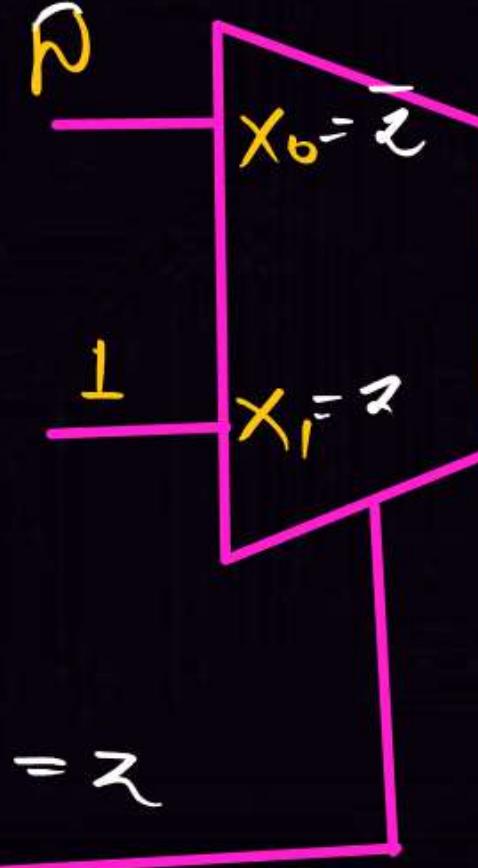
Q

$$A\bar{c} + Bc = x$$



$$\bar{r} + x\bar{r} = x + \bar{r}$$

$$A\bar{c} + Bc + \bar{r} = z$$



$$f(A, B, C, D)$$

$$= \bar{z} \cdot \bar{r} + z \cdot$$

$$= (\bar{z} + z) \cdot (z + \bar{r})$$

$$= z + \bar{r}$$

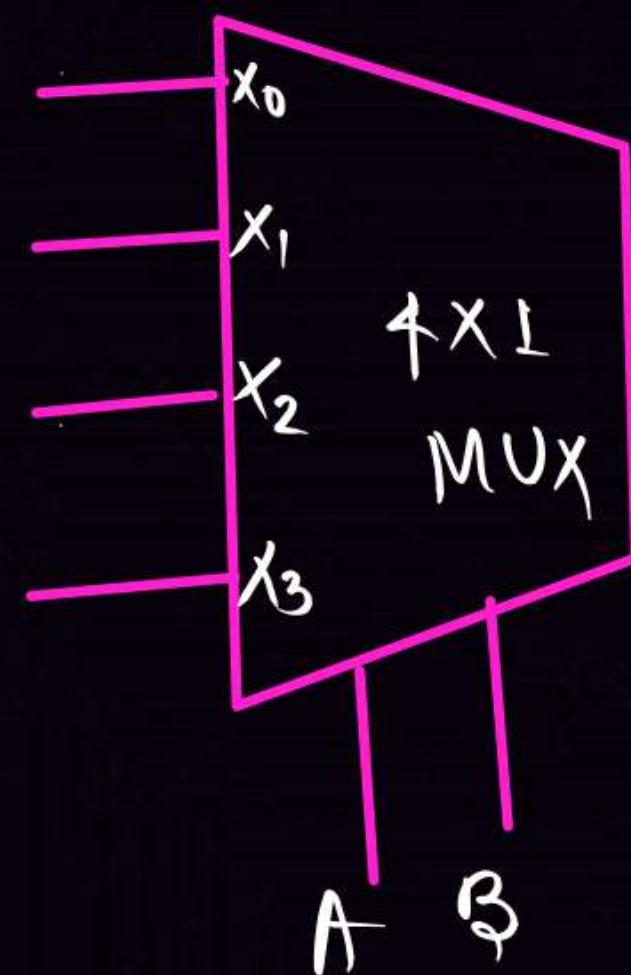
$$= A\bar{c} + Bc + \bar{r} + \bar{r}$$

$$= A\bar{c} + Bc + \bar{r}$$

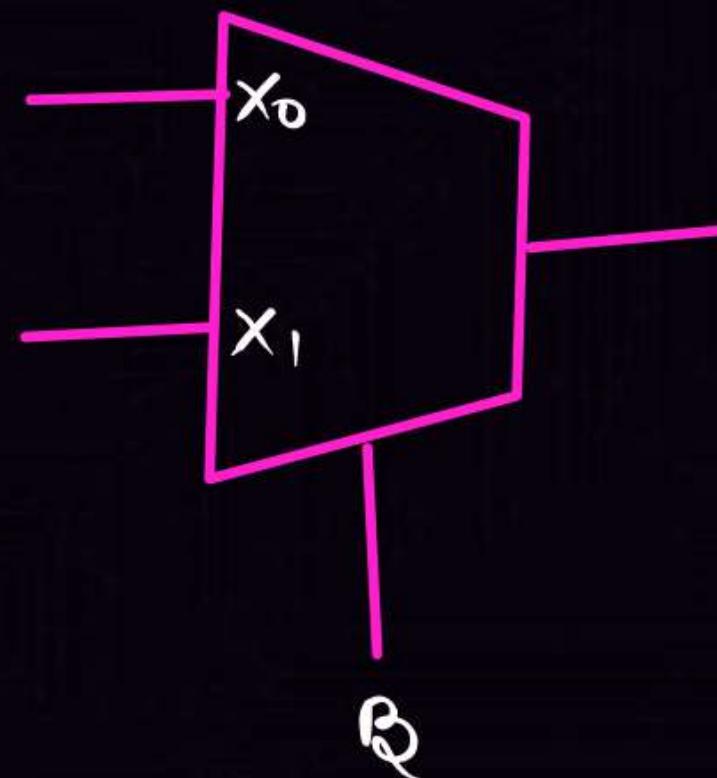
Q. $f(A, B, C) = \sum m(0, 1, 3, 6, 7)$ Implement by given MUX?

Input of the MUX are -

(i)



(ii)



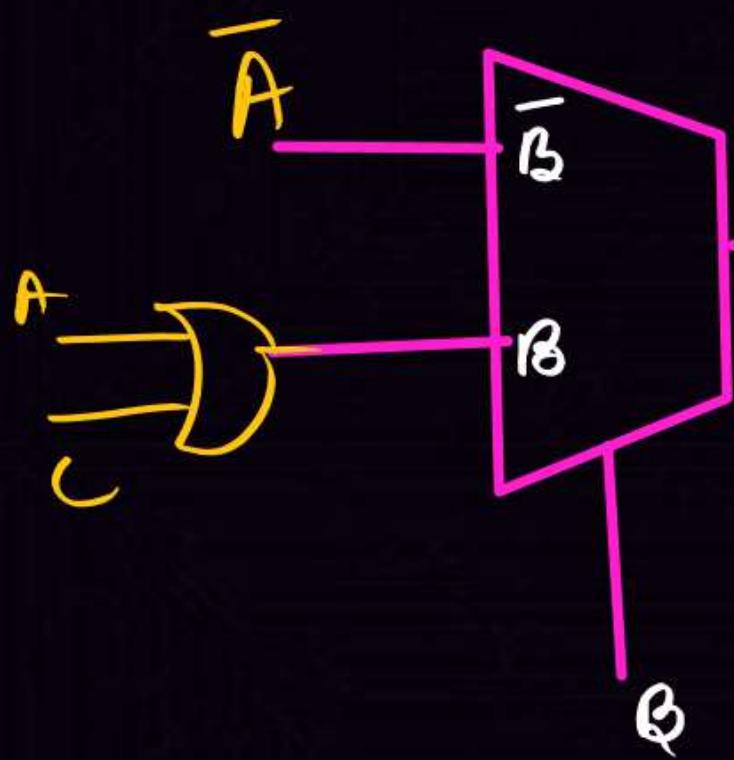
By 4x1 MUX

$f(A, B, C) = \bar{A}\bar{B} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}BC + ABC + ABC + ABC$

$$= \sum m(0, 1, 3, 6, 7)$$

	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	AB
\bar{C}	0	2	4	6
C	1	3	5	7
	1	C	0	1

By 2x1 MUX \Rightarrow



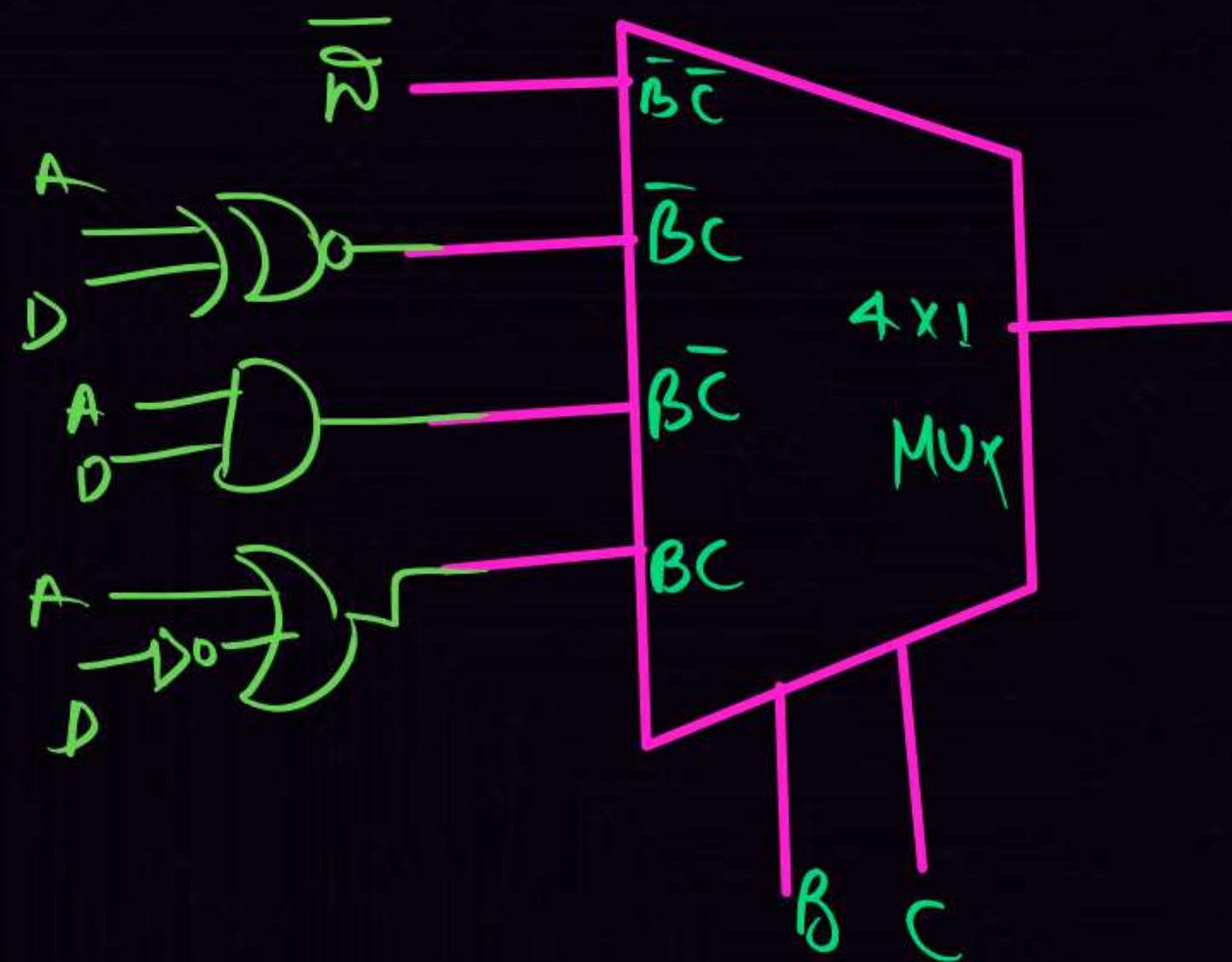
$$\begin{aligned}
 f(A, B, C) &= \bar{A}\bar{B} + (A+C)B \\
 &= \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C \\
 &\quad + AB\bar{C} + ABC + \bar{A}BC \\
 &= \sum m(0, 1, 3, 5, 7)
 \end{aligned}$$

	\bar{B}	B
$\bar{A}\bar{C}$	0	2
$\bar{A}C$	1	3
$A\bar{C}$	4	6
AC	5	7
	$\bar{A}\bar{C} + \bar{A}C$	$\bar{A}C + A\bar{C} + AC$
	$\bar{A}(C + \bar{C})$	$A + C$
	$= \bar{A}$	

$$f(A, B, C, D) = \sum m(0, 2, 6, 8, 11, 13, 14, 15)$$

4x1 MUX

BC as a select line

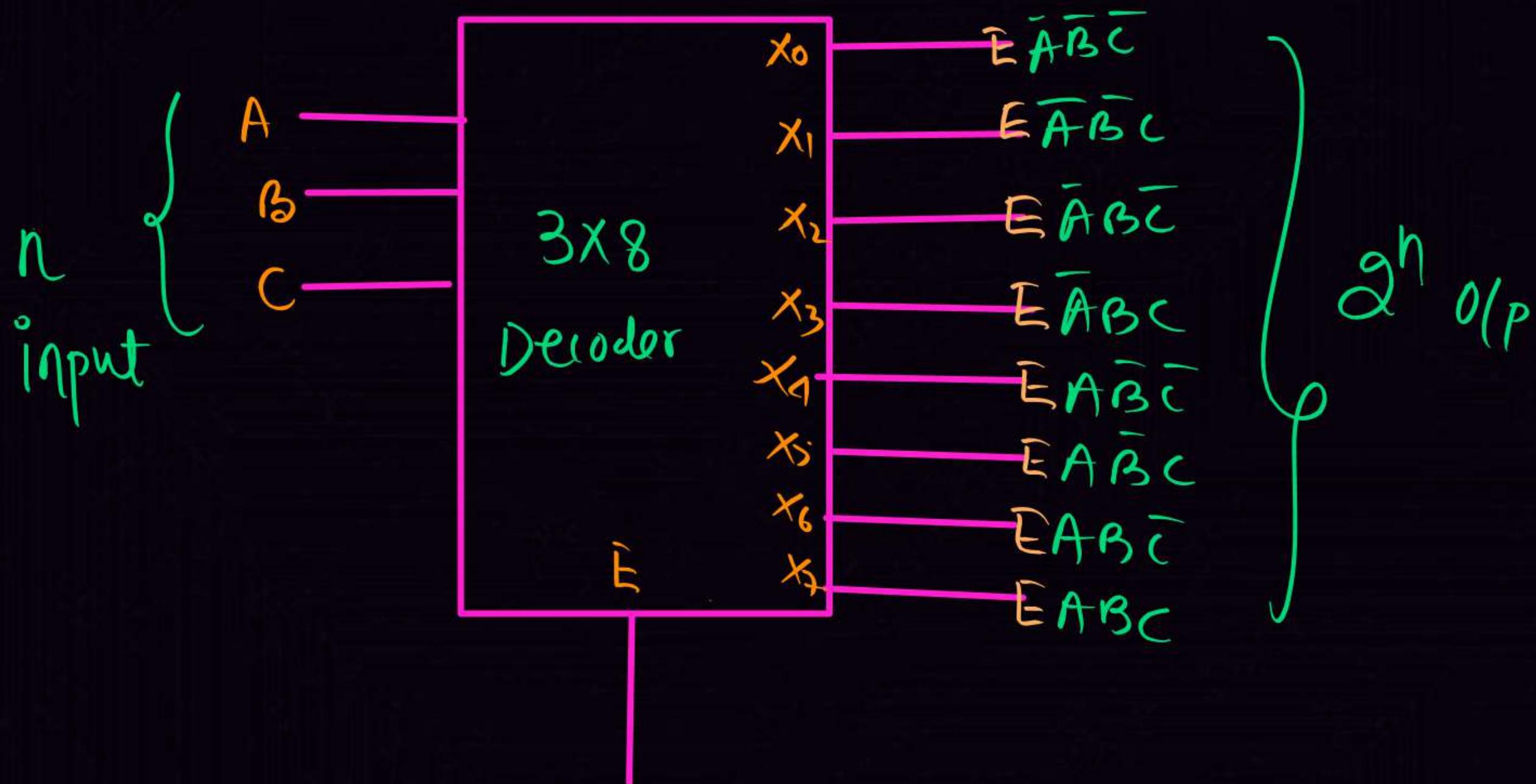


$\bar{B}\bar{C}$	$\bar{B}C$	$B\bar{C}$	BC	
$\bar{A}\bar{D}$	0	2	4	6
$\bar{A}D$	1	3	5	7
$A\bar{D}$	8	10	12	14
AD	9	11	13	15
	\bar{D}	$A\bar{D}D$	AD	$A+\bar{D}$

$$Q = \underbrace{4 \times 1 \text{ MUX}}_{\frac{64}{4} + \frac{16}{4} + \frac{4}{4}} \xrightarrow{16 + 4 + 1 = 21} \underbrace{64 \times 1 \text{ MUX}}$$

$$Q = \underbrace{8 \times 1 \text{ MUX}}_{\frac{64}{8} + \frac{8}{8}} \xrightarrow{8 + 1 = 9} \underbrace{64 \times 1 \text{ MUX}}$$

Alg

DECODER

Half Adder

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = AB$$

$$\text{NAND} | \text{NOR} = \textcircled{5}$$

Half subtractor

$$\text{Diff} = A \oplus B$$

$$\text{Borrow} = \bar{A}B$$

$$\text{NAND} | \text{NOR} = \textcircled{5}$$

Full adder

$$\text{Sum} = A \oplus B \oplus C$$

$$\text{Carry} = \sum m(3, 5, 6, 7)$$

$$= AB + AC + BC$$

$$= (A \oplus B)C + AB$$

$$\text{NAND/NOR} \rightarrow 9$$

1 FA = 2HAT + LOR

Full subtractor

$$\text{Diff} = A \oplus B \oplus C$$

$$\text{Borrow} = \sum m(1, 2, 3, 7)$$

$$= \bar{A}B + \bar{A}C + BC$$

$$= (\overline{A \oplus B})C + \bar{A}B$$

$$\text{NAND/NOR} = 9$$

1 Full subtractor = 2H.S + LOR

Q Design a Binary to BCD decoder :-

Decimal

Time / CJ SIR

Answer key

Thank you
GW
Soldiers!



Electronics and Communication Engineering

Computer Science



Digital Electronics

Lecture- 04

Digital Logic



By- CHANDAN JHA SIR



Topics to be Covered

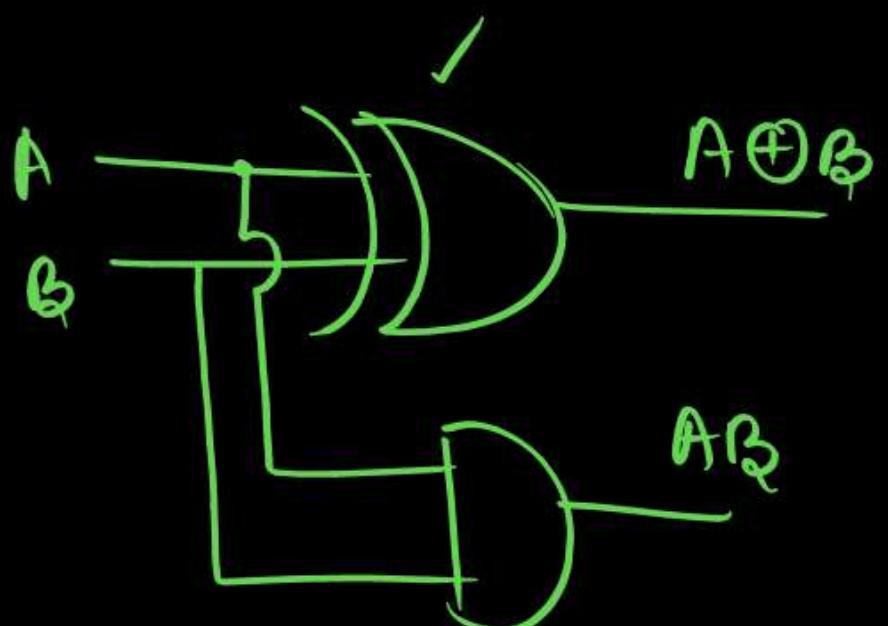
1. Combinational Circuit
2. Type here
3. Type here
4. Type here
5. Type here
6. Type here

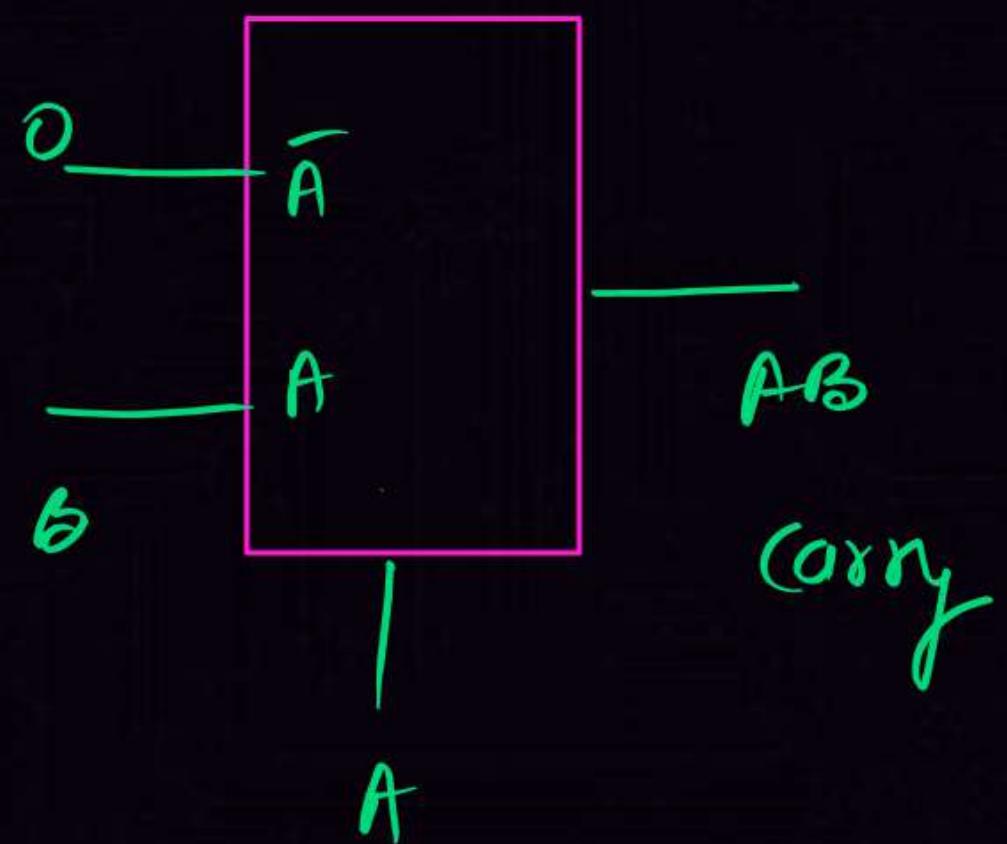
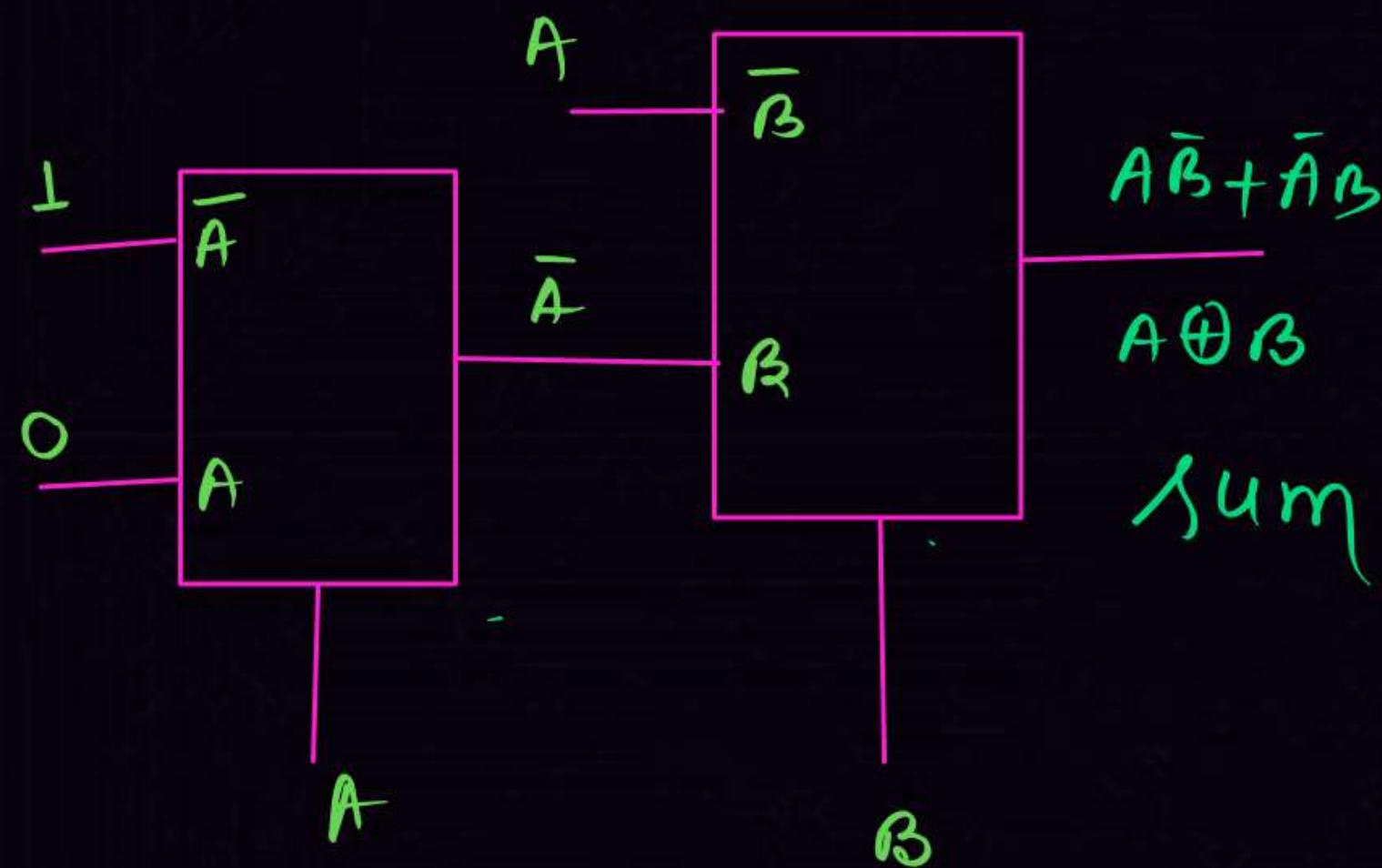
#Q. A half - adder can be constructed using two 2-input logic gates. One of them is an AND-gate, the other is

- (a) OR
- (b) NAND
- (c) NOR
- (d) EX-OR

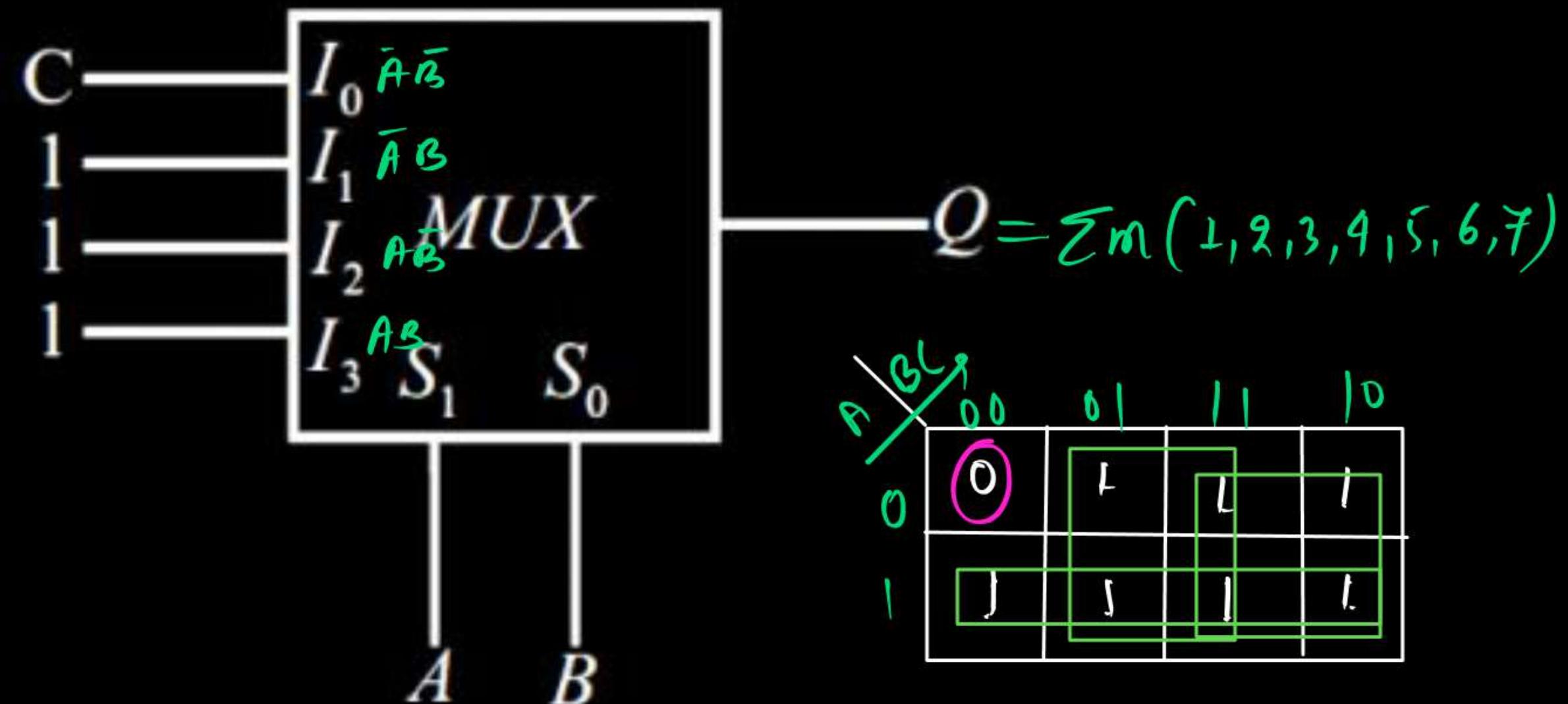
$$\text{Sum} = A \oplus B$$

$$\text{Carry} = AB$$





#Q. The combinational logic circuit shown in the given figure has an output Q which is

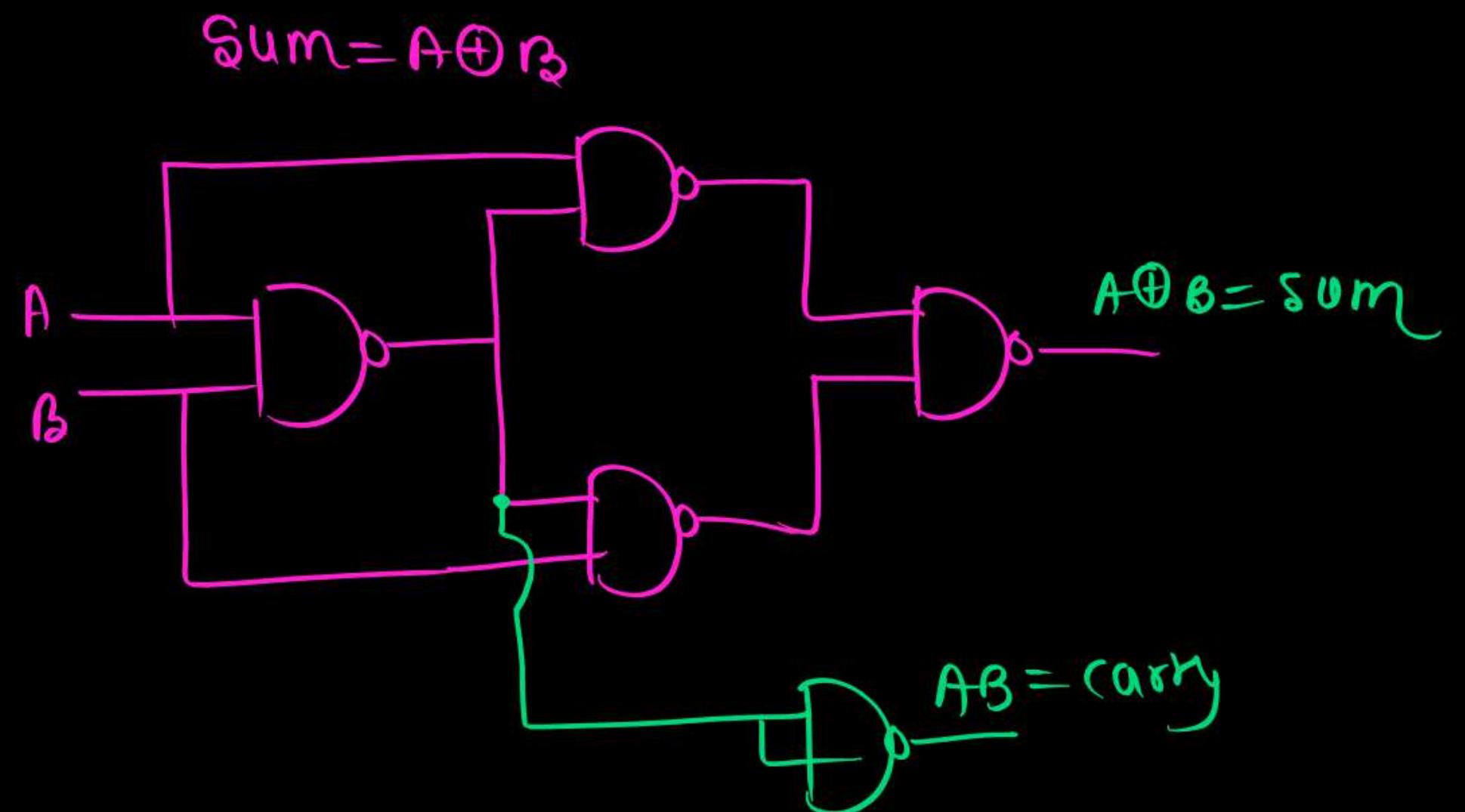


- (a) $A \cdot B \cdot C$
- (b) ~~$A + B + C$~~
- (c) $A \oplus B \oplus C$
- (d) $A \cdot B + C$

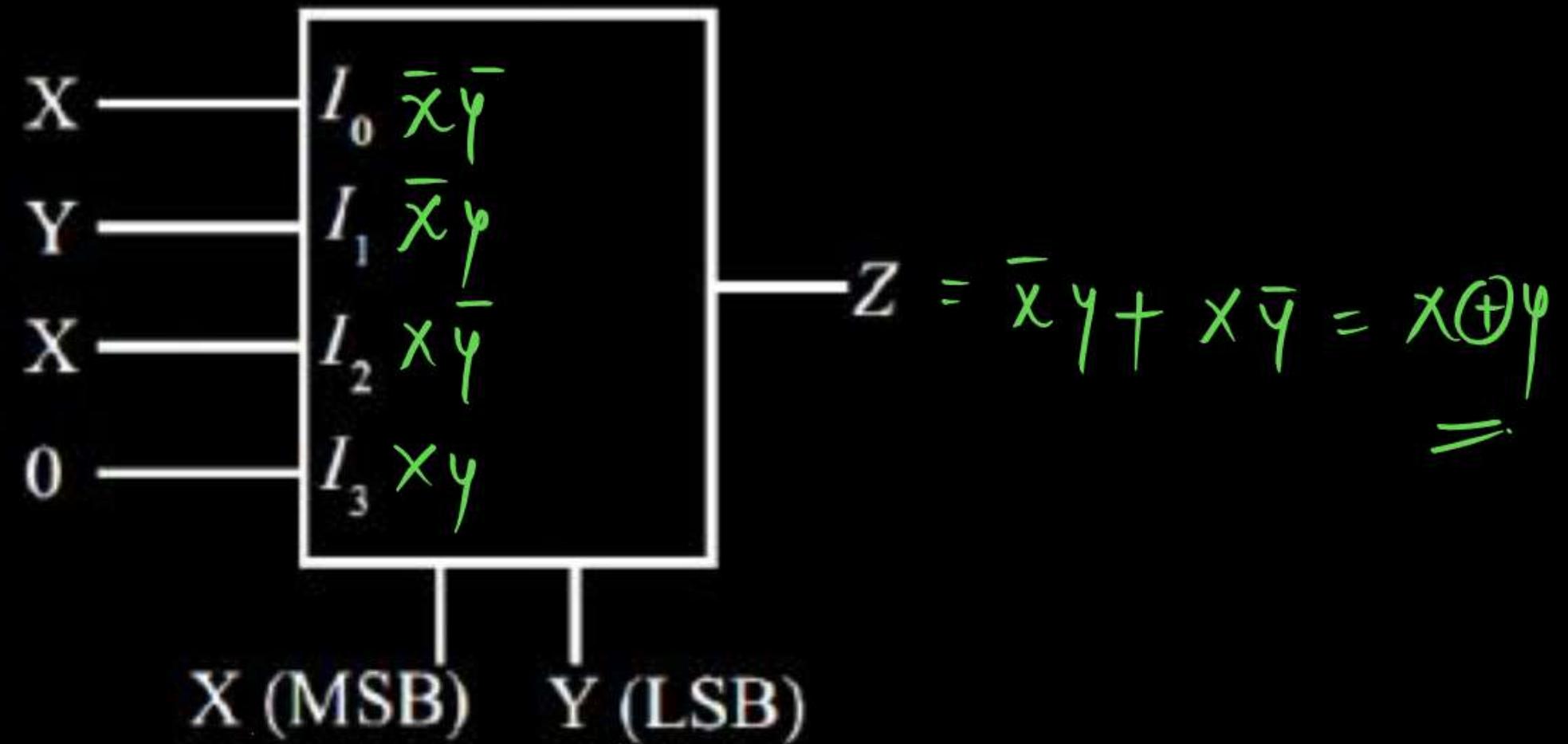
$A + B + C$

#Q. The sum S of A and B in a half adder can be implemented by using K NAND gates. The value of K is

- (a) 3
- (b) 4
- (c) 5
- (d) None of these

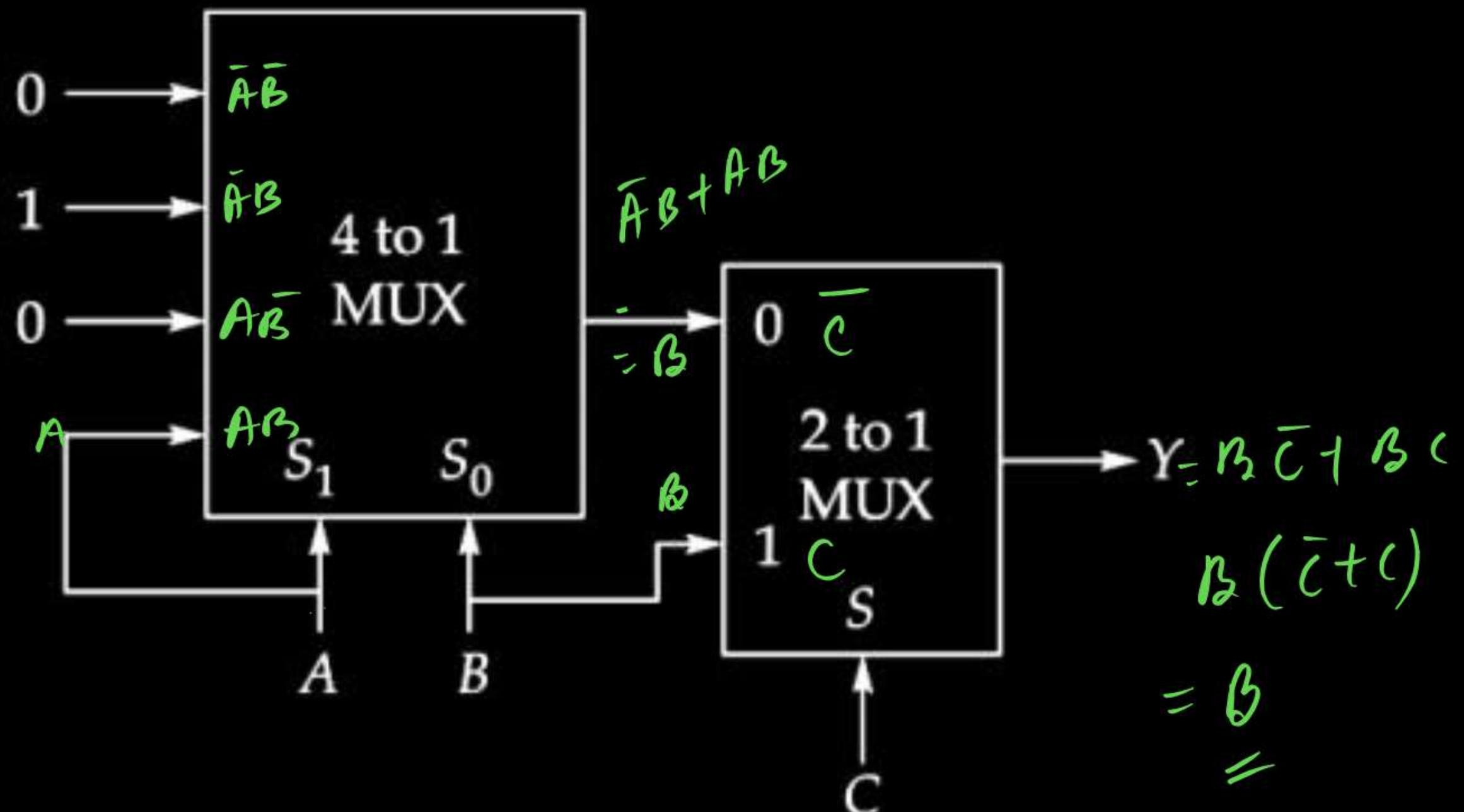


#Q. The logic function implemented by following 4 : 1 MUX is



- (a) $Z = X$ and Y (b) $Z = X$ or Y
~~(c)~~ $Z = X$ XOR Y (d) $Z = X$ XNOR Y

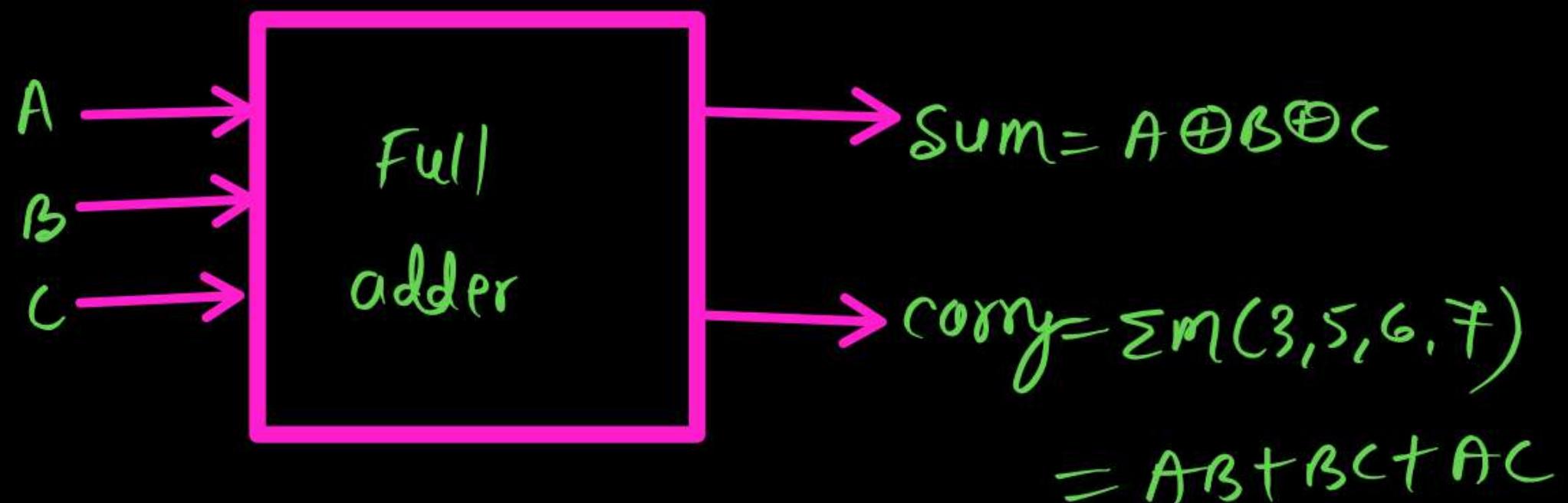
#Q. In the following circuit, Y can be expressed as



- (a) $Y = BC + A$
- (b) $Y = C$
- (c) $Y = AC + BC$
- (d) $Y = B$

#Q. How many inputs and outputs does a full adder have?

- (a) 3, 2
- (b) 2, 3
- (c) 3, 3
- (d) 2, 2



#Q. Consider the following :

Any **combinational circuit** can be built using

- 1. NAND gates
- 2. NOR gates
- 3. EX-OR gates
- 4. Multiplexers

→ Universal Logic

$$\textcircled{1} \quad \overline{AB} = \bar{A} + \bar{B}$$

$$\textcircled{2} \quad \overline{A+B} = \bar{A} \cdot \bar{B}$$

$$\textcircled{3} \quad \bar{A} + B$$

$$\textcircled{4} \quad A + \bar{B}$$

$$\textcircled{5} \quad \bar{A} \cdot B$$

$$\textcircled{6} \quad A \cdot \bar{B}$$

$\textcircled{7}$ Multiplexer

$\textcircled{8}$ Decoder + OR

Which of these are correct?

- (a) 1, 2 and 3
- (b) 1, 3 and 4
- (c) 2, 3 and 4
- (d) 1, 2 and 4

#Q. Match List-I (Operation) with List-II (Associated Device) and select the correct answer using the codes given below:

List-I

- A. Counting
- B. Decoding
- C. Data selection
- D. Code conversion

List-II

- 1. ROM
- 2. Multiplexer
- 3. Demultiplexer
- 4. Register

Codes: A B C D

- (a) 3 4 2 1
- (b) 3 4 1 2
- (c) 4 3 1 2
- (d) 4 3 2 1

#Q. It is required to construct a 2^n -to-1 multiplexer by using 2-to-1 multiplexers only.
How many of 2-to-1 multiplexers are needed?

- (a) n
- (b) 2^{2n}
- (c) 2^{n-1}
- (d) $2^n - 1$

$$2 \times L \text{ MUX} \xrightarrow{\frac{4}{2} + \frac{2}{2}} 4 \times 1 \text{ MUX}$$

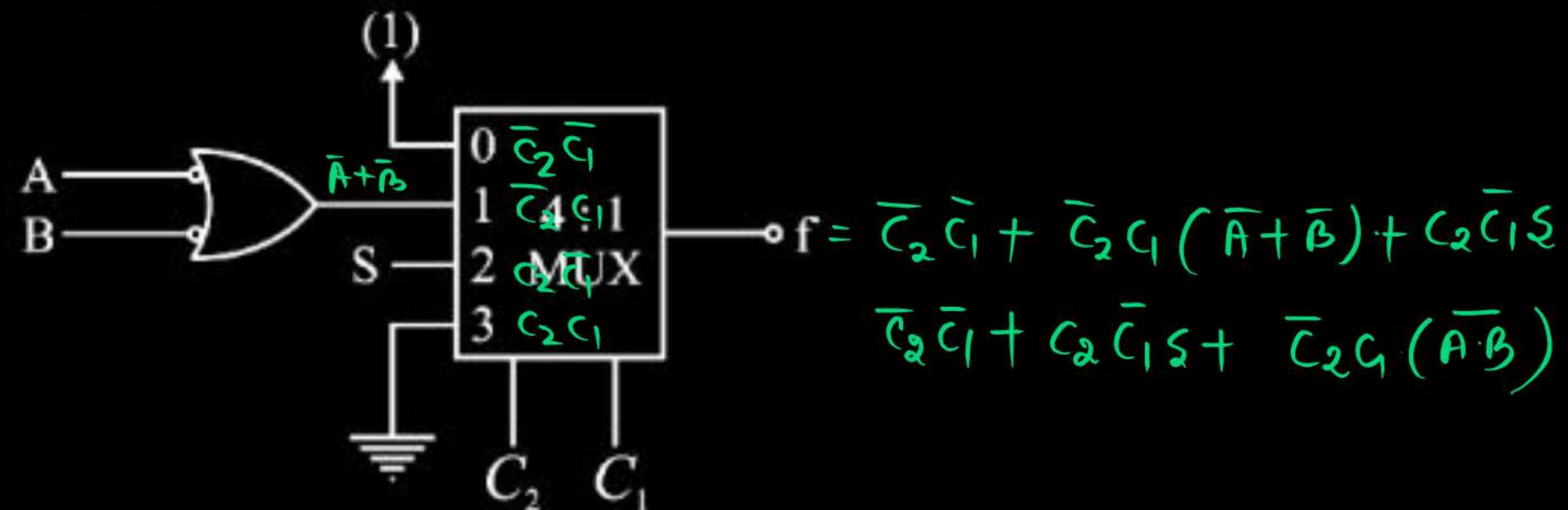
$$2+1 = ③$$

$$2 \times 1 \text{ MUX} \xrightarrow{\frac{8}{2} + \frac{4}{2} + \frac{2}{2}} 8 \times L \text{ MUX}$$

$$4+2+1 = ⑦$$

$$2 \times 1 \text{ MUX} \xrightarrow{2^n - 1} 2^n \times L \text{ MUX}$$

#Q. Consider the following circuit :



Which one of the following gives the function implemented by the MUX-based digital circuit?

- (a) $f = C_2 \cdot \bar{C}_1 \cdot S + \bar{C}_2 \cdot C_1 \cdot (\bar{A} + \bar{B})$
- (b) $f = \bar{C}_2 \cdot \bar{C}_1 + C_2 \cdot C_1 + C_2 \cdot \bar{C}_1 \cdot S + \bar{C}_2 \cdot C_1 \cdot \overline{AB}$
- (c) $f = \overline{AB} + S$
- (d) $\cancel{f = \bar{C}_2 \cdot \bar{C}_1 + C_2 \cdot \bar{C}_1 \cdot S + \bar{C}_2 \cdot C_1 \cdot \overline{AB}}$

#Q. What are the output bits S (Sum) and C (Carry) of a Half Adder having inputs A = \textcircled{P} W
1 and B = 1 ?

S C

- (a) 1 1
- (b) 1 0
- (c) 0 1
- (d) 0 0

$$\begin{array}{r} A \\ + B \\ \hline \end{array} \quad \begin{array}{r} | \\ + | \\ \hline 0 \\ | \\ \curvearrowright \text{sum} \\ \curvearrowleft \text{carry} \end{array}$$

#Q. The logic function $A + BC$ is the simplified form of which of the following?

- (a) $AB + BC$
- (b) $\bar{A}B + A\bar{B}C$
- (c) \overline{ABC}
- (d) $(A + B)(A + C)$

$$A + BC = (A + B)(A + C)$$

#Q. If a, b, c are 3 input variables, then Boolean function $y = ab + bc + ca$ represents

1. A 3 input majority gate
2. A 3 input minority gate
3. Carry output of a full adder
4. Product circuit for a, b and c

→ carry of Full adder

Which of the above statements are correct?

- | | |
|-------------|-------------|
| (a) 2 and 3 | (b) 2 and 4 |
| (c) 1 and 3 | (d) 1 and 4 |

Majority input
GATE

A	B	C	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$y = \{m(3, 5, 6, 7)\}$$

#Q. The truth table for the function, $f(ABCD) = \sum m(0, 1, 3, 4, 8, 9)$ is

	0	1	0	0	0	1	1	1	1
A	0	0	0	0	1	1	1	1	1
B	0	0	1	1	0	0	1	1	1
C	0	1	1	0	1	0	1	0	1
d	1	0	0	1	0	1	0	1	0
F	W	X	Y	0	Z	0	0	0	0

$F = \bar{A}\bar{B}\bar{C}W + \bar{A}\bar{B}Cx + \bar{A}B\bar{C}y + A\bar{B}\bar{C}z$
 $F = \bar{A}\bar{B}\bar{C}W + \bar{A}\bar{B}Cx + \bar{A}B\bar{C}D + A\bar{B}\bar{C}\cdot 1$

$\sum m(0,1)$ $\sum m(3)$

where W, X, Y, Z are given by (d is the complement of D)

- (a) $D, d, 1, 1$
- (b) $1, d, D, 1$
- (c) $1, 1, D, d$
- (d) $1, D, d, 1$

#Q. A 1-bit full adder takes 20ns to generate carry-out bit and 40ns for the sum bit. What is the maximum rate of addition per second when four 1-bit full adders are cascade ?

(a) 10^7

(b) 1.25×10^7

(c) 6.25×10^6

(d) 10^5

$$T = (n-1)T_{\text{carry}} + \text{Max}\{T_{\text{sum}}, T_{\text{carry}}\}$$

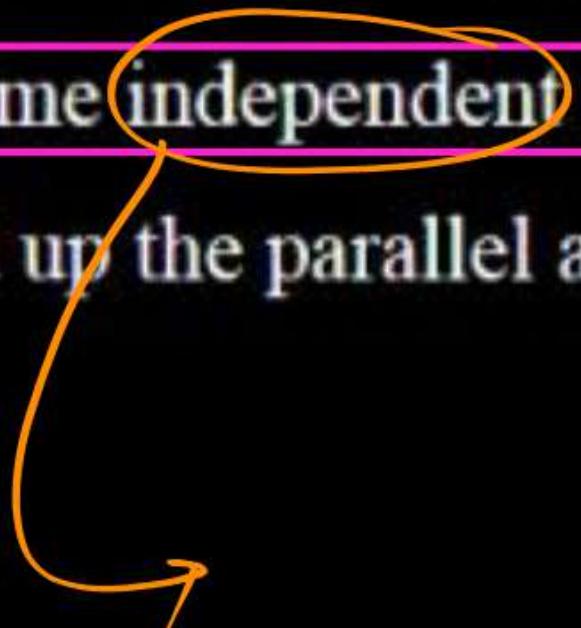
$$T = 3 \times 20 \text{ ns} + 40 \text{ ns}$$

$$T = 100 \text{ ns}$$

$$\frac{1}{T} = \frac{1}{100 \times 10^{-9}} = \frac{10^9}{100} = \frac{1000 \times 10^6}{100} = 10^7$$

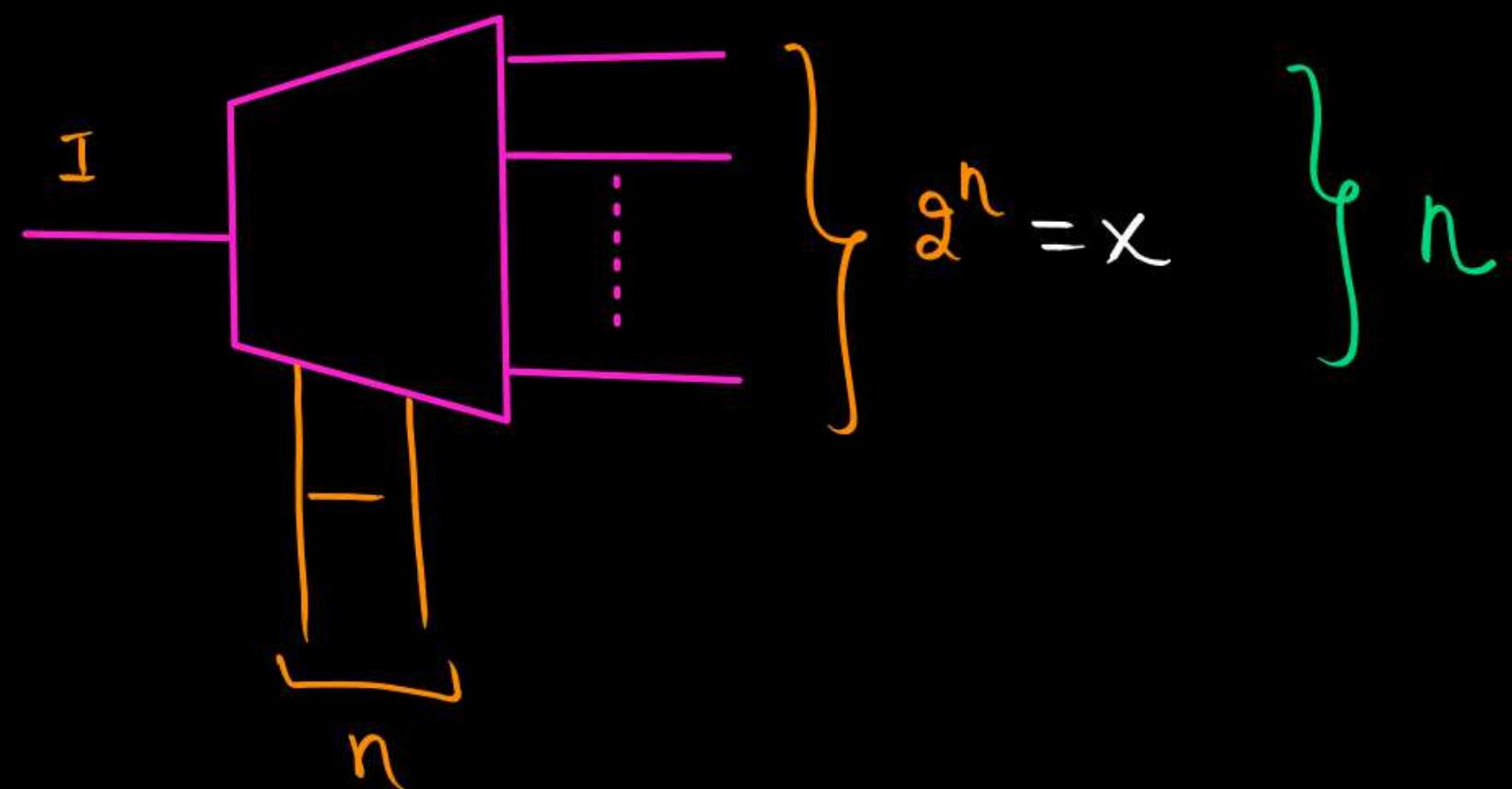
#Q. Which one of the following statements is **not correct** ?

- (a) A full adder can be constructed using two half-adders and an OR gate.
- (b) Two four bit parallel adders can be cascaded to construct 8-bit parallel adder.
- (c) Ripple carry adder has addition time **independent** of the number of bits.
- (d) Carry look ahead is used to speed up the parallel addition.



#Q. What is the number of selection lines required in a single input n-output de-multiplexer?

- (a) 2
- (b) n
- (c) 2^n
- (d) $\log_2 n$



$$\log_2 x$$

$$\log_2 n$$

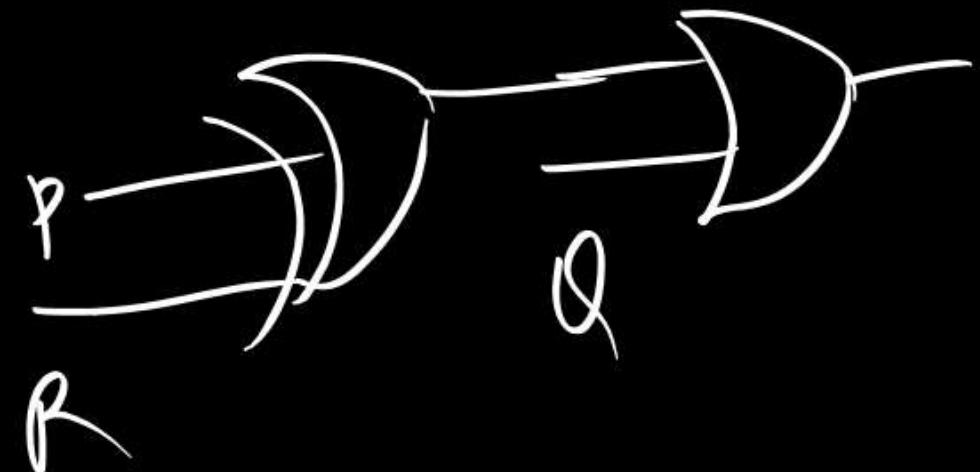
#Q. The Boolean expression $X(P, Q, R) = \pi(0, 5)$ is to be realized using only two 2-input gates. Which are these gates?

- (a) AND and OR
- (b) NAND and OR
- (c) AND and XOR
- (d) OR and XOR

P Q R	00	01	11	10
0	0	1	1	1
1	1	0	0	0

$$Q + \bar{P}R + P\bar{R}$$

$$Q + (P \oplus R)$$



#Q. What is the Boolean expression for the truth table shown below?

A	0	0	0	0	1	1	1	1
B	0	0	1	1	0	0	1	1
C	0	1	0	1	0	1	0	1
f	0	0	0	1	0	0	1	0

(a) $B(A+C)(\bar{A}+\bar{C})$

(b) $B(A+\bar{C})(\bar{A}+C)$

(c) $\bar{B}(A+C)(\bar{A}+C)$

(d) $\bar{B}(A+C)(\bar{A}+\bar{C})$

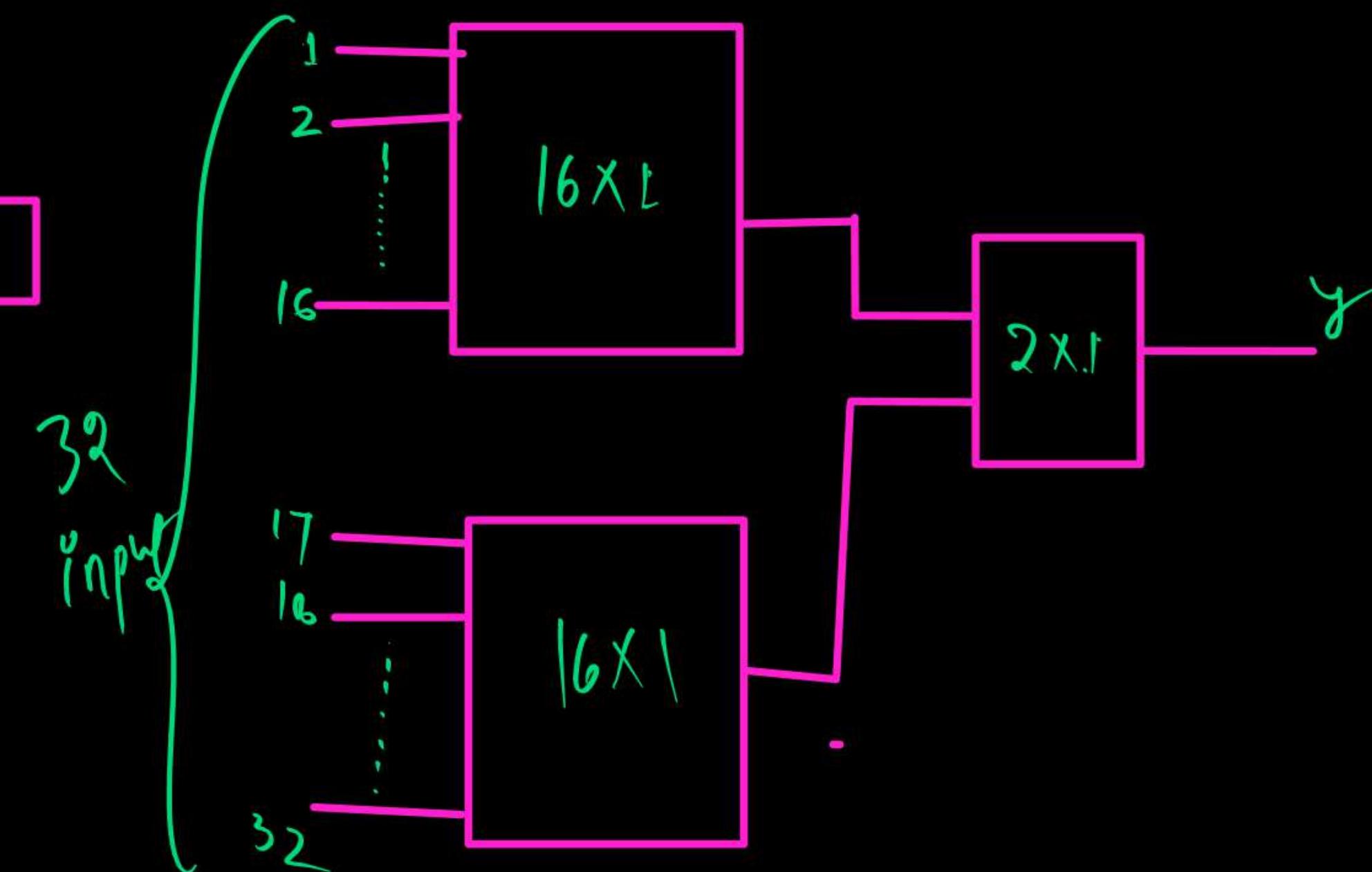
$$\bar{A}BC + AB\bar{C}$$

$$B(\bar{A}C + A\bar{C})$$

$$B(A+C)(\bar{A}+\bar{C})$$

#Q. When two 16-input multiplexers drive a 2-input MUX, what is the result?

- (a) 2-input MUX
- (b) 4-input MUX
- (c) 16-input MUX
- (d) 32-input MUX



#Q. Consider the following statements:

For 3 input variables a, b, c; a Boolean function $y = ab + bc + ca$ represents

1. A 3-input majority gate
2. A 3-input minority gate
3. Carry output of a full adder
4. Product circuit for a, b and c

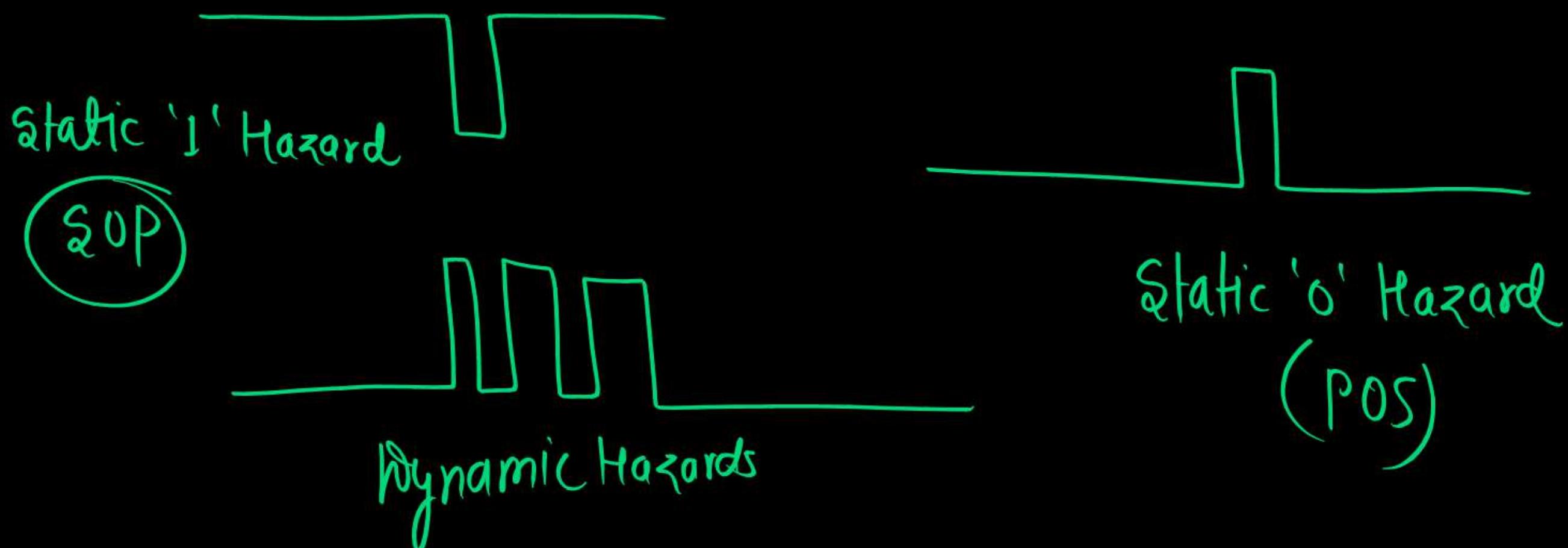
Which of the above statements are correct?

- (a) 1 and 4 only (b) 2 and 3 only
(c) 1 and 3 only (d) 3 and 4 only

#Q. Which one of the following statements is correct?

SOP

- (a) Static 1 hazard may occur in a 2-level AND-OR gate network.
- (b) Static 0 hazard may occur in a 2-level AND-OR gate network.
- (c) Dynamic hazards may occur in a 2-level GRAND gate network.
- (d) Essential hazards may occur in a combinational logic circuit.



#Q. A digital multiplexer can be used for which of the following?

1. Parallel to serial conversion
2. Many-to-one switch
3. To generate memory chip select.
4. For code conversion.



Select the correct answer using the code given below:

- | | |
|------------------|------------------|
| (a) 1, 3 and 4 | (b) 2, 3 and 4 |
| (c) 1 and 2 only | (d) 2 and 3 only |

#Q. Which of the following circuits come under the class of combinational logic circuits?

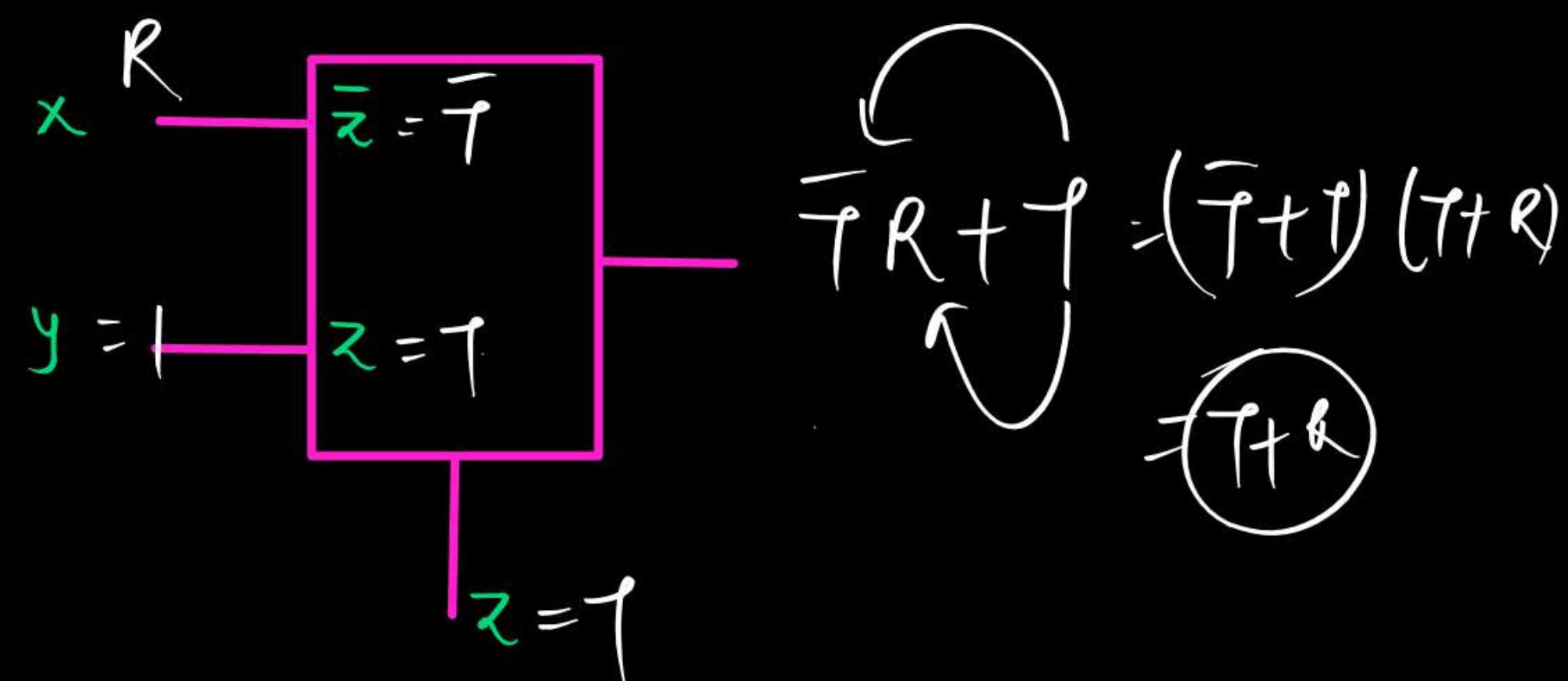
- ✓ 1. Full adder ✓ 2. Full subtractor
- ✓ 3. Half adder 4. J-K flip flop
- 5. Counter

Select the correct answer from the codes given below:

- (a) 1 only (b) 3 and 4
- (c) 4 and 5 (d) 1, 2 and 3

#Q. Consider a multiplexer with X and Y as data inputs and Z as control input. Z = 0 selects input X and Z = 1 selects input Y. What are the connections required to realize the 2 variable Boolean function $f = T + R$. without using any additional hardware?

- (a) R to X, 1 to Y, T to Z
- (b) T to X, R to Y, T to Z
- (c) T to X, R to Y, 0 to Z
- (d) R to X, 0 to Y, T to Z



#Q. ~~HW~~ With which decoder it is possible to obtain many code conversions?

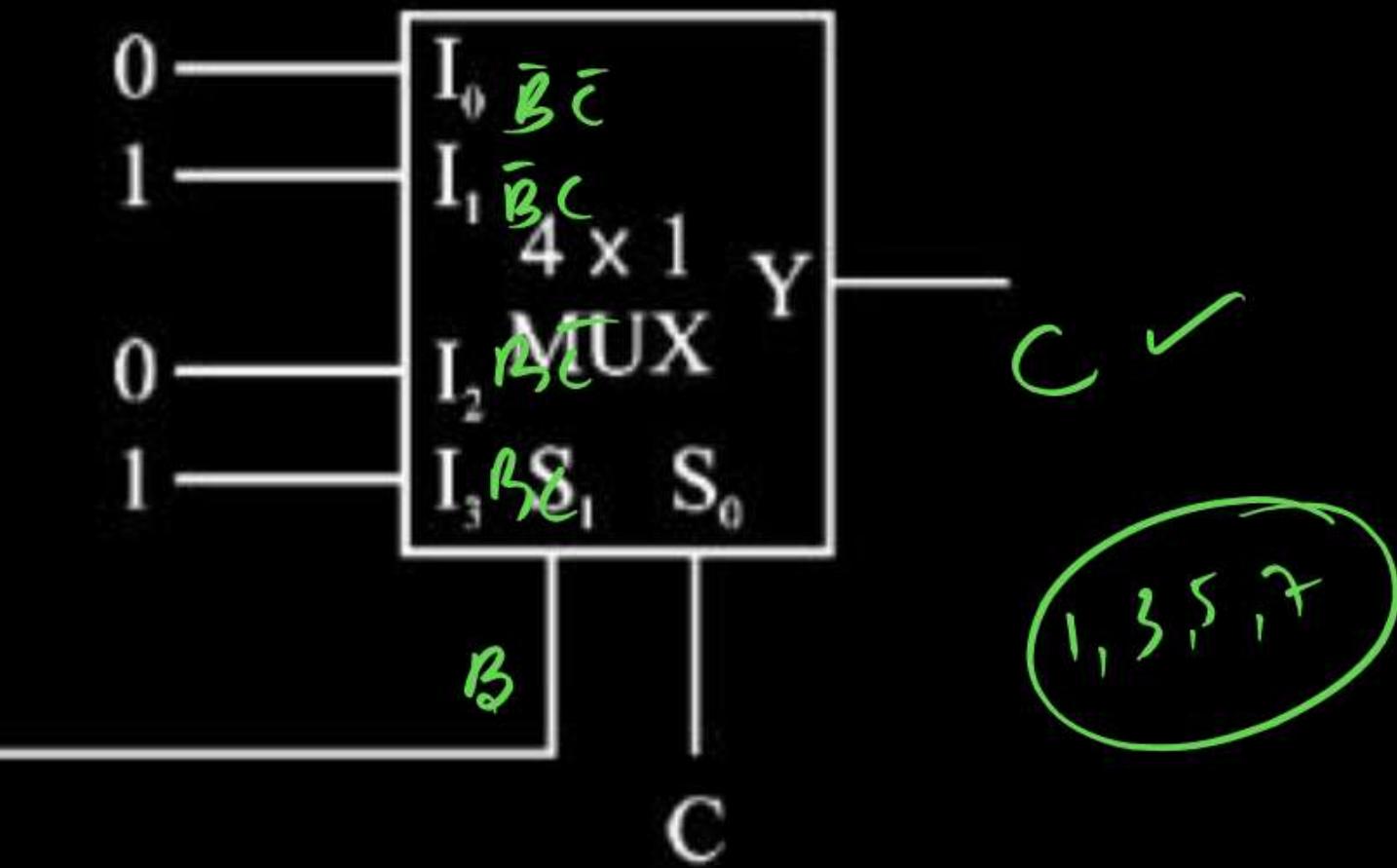
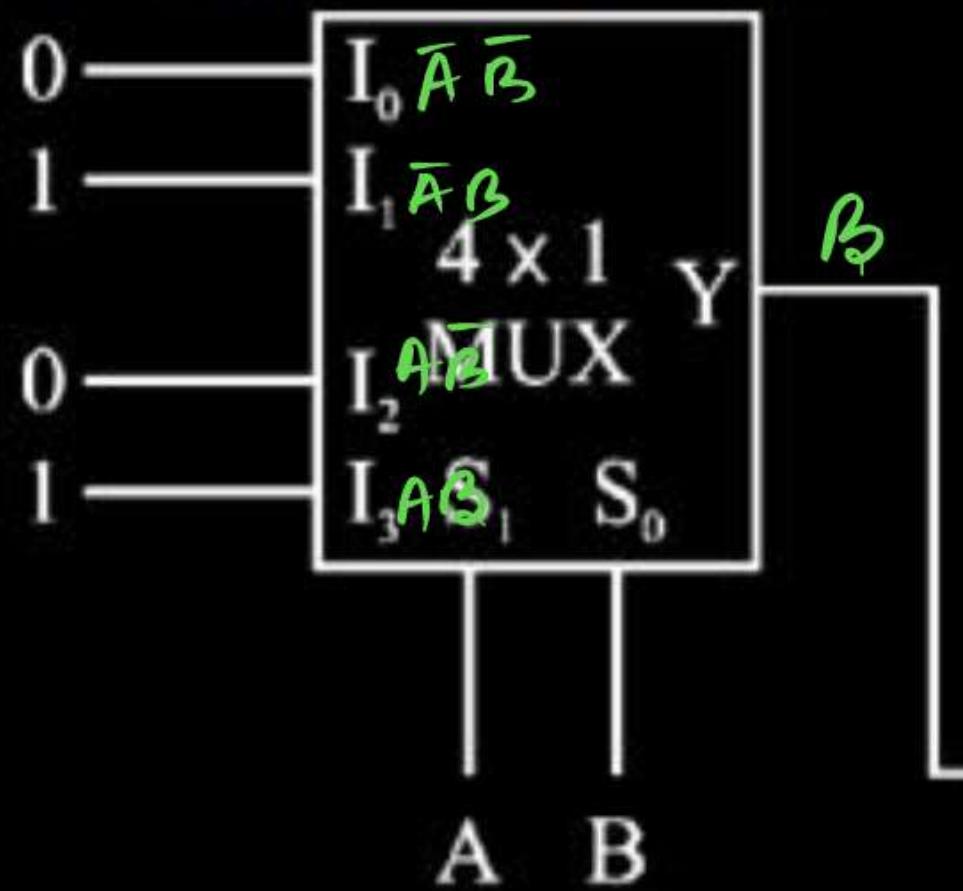
- (a) 2 line to 4 line
- (b) 3 line to 8 line
- (c) Not possible with any decoder
- (d) 4 line to 16 line decoder

#Q. ~~A~~^{HW} 3×8 decoder with two enable inputs is to be used to address 8 blocks of memory.

What will be the size of each memory block when addressed from a sixteen bit bus with two MSBs used to enable the decoder?

- (a) 2 K
- (b) 4 K
- (c) 16 K
- (d) 64 K

#Q. In the below circuit, X is given by



- (a) $X = A\bar{B}C + \bar{A}BC\bar{C} + \bar{A}\bar{B}C + ABC$
- (b) $X = \bar{A}BC + A\bar{B}C + ABC\bar{C} + \bar{A}BC$
- (c) $X = AB + BC + AC$
- (d) $X = \overline{AB} + \overline{BC} + \overline{AC}$

Karnaugh Map for X :

00	01	11	10
0	1	1	1
1	0	0	0

#Q. The Boolean expression for the output of the below logic circuit is



- (a) $Y = \overline{A}\overline{B} + AB + \overline{C}$
- (b) $Y = \overline{A}B + A\overline{B} + \overline{C}$
- (c) $Y = A \oplus B + \overline{C}$
- (d) $Y = AB + \overline{C}$

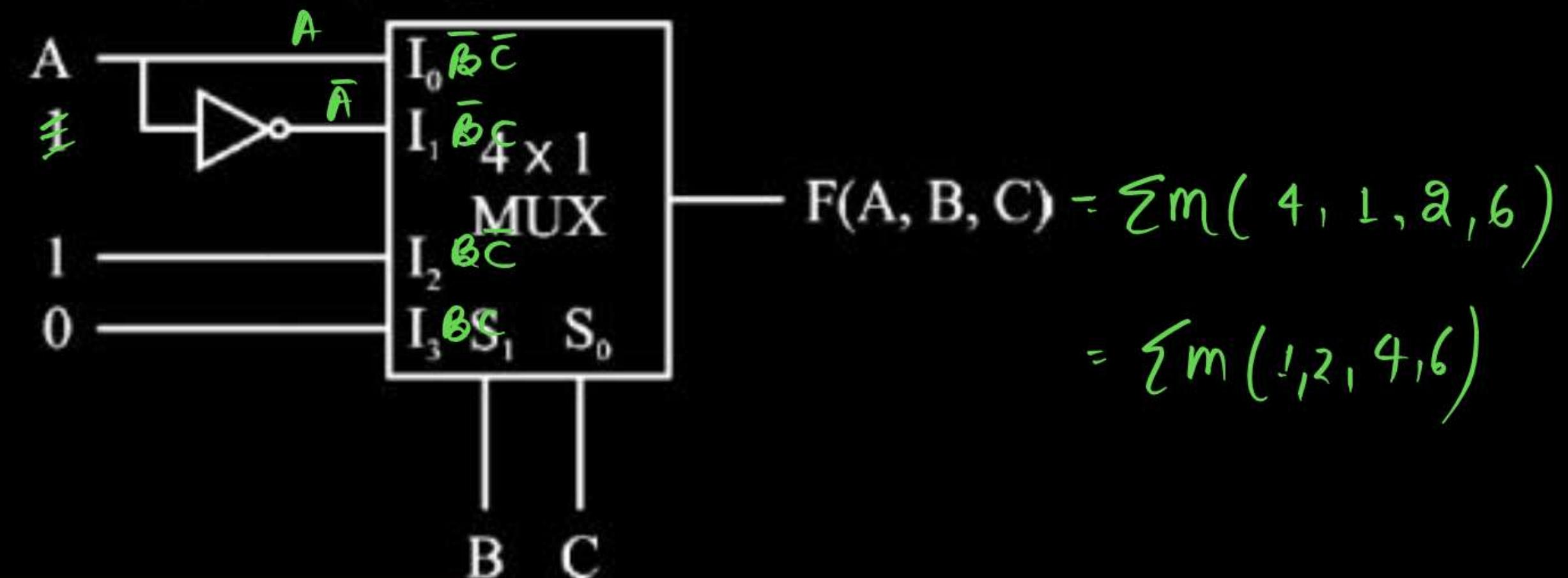
#Q. Consider the following statements:

1. A multiplexer is analogous to a rotary switch.
2. A decoder is a combinational logic circuit that converts binary information from ‘n’ input lines to a maximum of ‘n’ distinct elements at the output.
3. The Boolean expression for the output difference ‘D’ from a full subtractor is exactly the same as the output sum ‘S’ from a full adder.

Which of the above statements is/are correct?

- (a) 1 and 2 only (b) 1 only
(c) 1 and 3 only (d) 1, 2 and 3

#Q. A 4×1 mux is used to implement a 3 input Boolean function is as shown below.
The Boolean function (A, B, C) implemented is



(a) $F(A, B, C) = \sum m(1, 2, 4, 6)$

(b) $F(A, B, C) = \sum m(1, 2, 6)$

(c) $F(A, B, C) = \sum m(2, 4, 5, 6)$

(d) $F(A, B, C) = \sum m(1, 5, 6)$

#Q. A 3 - variable truth table has a high output for the inputs : 010, 011 and 110. The Boolean expression for sum of product (SOP) can be written as

- (a) $\bar{A}B + B\bar{C}$
- (b) $A\bar{B} + \bar{B}C$
- (c) $\overline{AB} + BC$
- (d) $AB + \overline{BC}$

A	B	C	Output
0	0	0	0
0	0	1	0
0	1	1	1
1	1	0	1

$$\bar{A}B + B\bar{C}$$

#Q. A binary full - subtractor

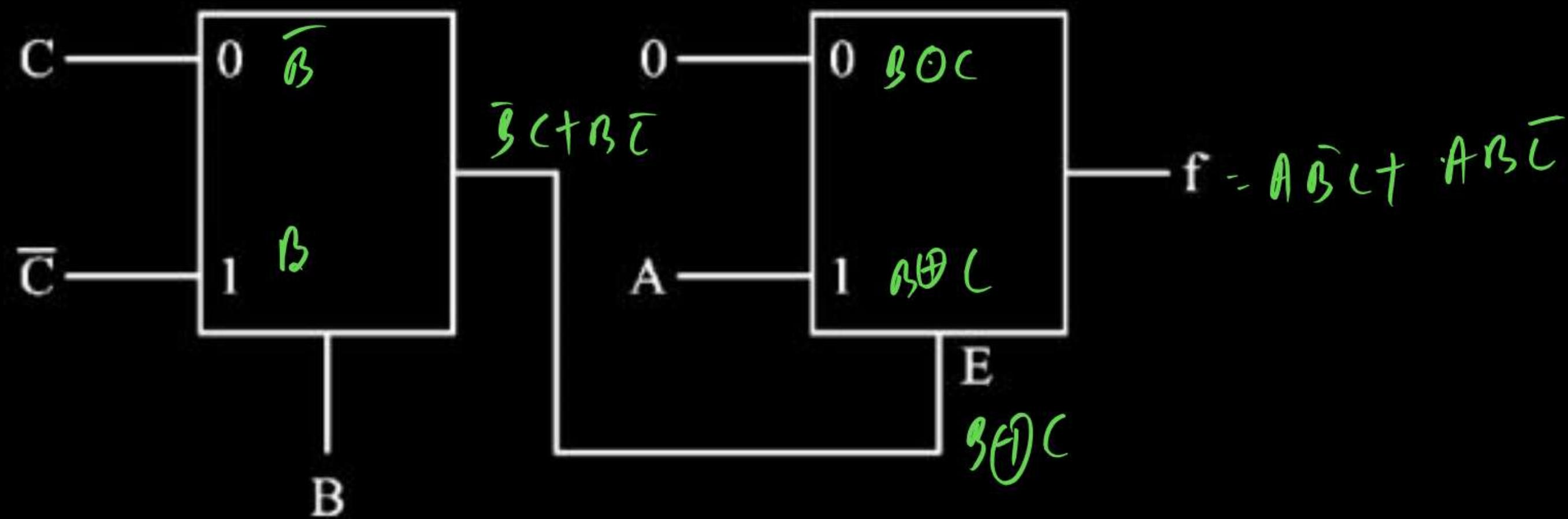
- (a) Consists of two cascaded half - subtractors
- (b) Contains two half - subtractors and one OR gate
- (c) Can subtract any binary number
- (d) Can be made out of a full – adder

#Q. An array multiplier is used to find the product of a 3 bit number with a 4 bit number. How many 4 bits adders are required to perform multiplication?

- (a) 1
- (b) 2
- (c) 3
- (d) 4

$$\begin{array}{r} A \rightarrow A_2 \ A_1 \ A_0 \\ \beta \rightarrow \beta_2 \beta_1 \beta_0 \\ \hline \end{array}$$

#Q. The Boolean function 'f' implemented as shown in the figure using two input multiplexers is



- (a) $A\bar{B}C + ABC$
- (b) $ABC + A\bar{B}\bar{C}$
- (c) $\bar{A}BC + ABC$
- (d) $\bar{A}\bar{B}C + \bar{A}BC$

#Q. A binary-to-BCD encoder has four inputs D_0 , C_0 , B_0 and A_0 and five outputs D, C, B, A and VALID. The outputs D, C, B and A give the proper BCD value of the input and the VALID output is 1 if the input combination is a valid decimal code. If the input combination is an invalid decimal code, the VALID output becomes 0 and all of the D, C, B and A outputs show 0 values. If only NOT gates and 2-input OR and AND gates are available, the minimum number of gates required to implement the above circuit is

- (a) 10
- (b) 9
- (c) 8
- (d) 7

#Q. A half adder can be constructed using

- (a) One XOR and one OR gate with their outputs connected in parallel
- (b) One XOR and one OR gate with their outputs connected in series
- (c) One XOR gate and one AND gate
- (d) Two XNOR gates only

Q. For realizing a binary half-subtractor having two inputs A and B, the correct set of logical expressions for the outputs D (A minus B) and X (borrow) are

1. The difference output $D = \bar{A}B + A\bar{B}$
 2. The borrow output $B = A\bar{B}$

Which of the above statements is/are correct?

#Q. Consider the following statements with respect to combinational circuit

1. The output at any time depends only on the present combination of inputs.
2. It does not employ storage elements
3. It performs an operation that can be specified logically by a set of Boolean functions.

Which of the above statements are correct?

- (a) 1 and 2 only (b) 1 and 3 only
(c) 2 and 3 only (d) 1, 2 and 3

#Q. Consider the following statements :

A multiplexer

1. selects one of the several inputs and transmit it to a single output.
2. routes the data from a single input to one of many outputs.
3. converts parallel data into serial data
4. is a combinational circuit

Which of the above statements are correct ?

- (a) 1 and 3 only (b) 2 and 4 only
(c) 1, 3 and 4 only (d) 2, 3 and 4 only

#Q. What are the two types of basic adder circuits?

- (a) Half adder and full adder
- (b) Half adder and parallel adder
- (c) Asynchronous adder and synchronous adder
- (d) One's complement adder and two's complement adder

#Q. Consider the following statements.

1. An 8-input MUX can be used to implement any 4 variable functions.
2. A 3-line to 8-line DEMUX can be used to implement any 4 variable functions.
3. A 64-input MUX can be built using nine 8-input MUXes.
4. A 6-line to 64-line DEMUX can be built using nine 3-line to 8-line DEMUXes.

Which of the above statements are correct?

- (a) 1, 2, 3 and 4 (b) 1, 2 and 4 only
(c) 3 and 4 only (d) 1, 2 and 3 only

#Q. For an n-bit binary adder, what is the number of gates through which a carry has to propagate from input to output

- (a) n
- (b) $2n$
- (c) n^2
- (d) $n + 1$

#Q. Which of the following circuits converts/convert a binary number on the input to a one-hot encoding at the output?

1. 3-to-8 binary decoder
2. 8-to-3 binary encoder
3. Comparator

Select the correct answer using the code given below.

- | | |
|------------|----------------|
| (a) 1 only | (b) 2 only |
| (c) 3 only | (d) 1, 2 and 3 |

#Q. A circuit outputs a digit in the form of 4 bits 0 is represented by 0000, 1 is represented by 0001, ..., 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and output as 1, if the digit is ≥ 5 , and 0 otherwise. It only AND, OR and NOT gates may be used, what is the minimum number of gates required?

- (a) 4
- (b) 3
- (c) 2
- (d) 1

#Q. How many 3-to-8 line decoders with an enabler input are needed to construct a 6-to-64 line decoder without using any other logic gates?

- (a) 11
- (b) 10
- (c) 9
- (d) 8

#Q. If only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables, what is the maximum size of the multiplexer needed?

- (a) 2^{n-2} line to 1 line
- (b) 2^{n-1} line to 1 line
- (c) 2^{n+1} line to 1 line
- (d) 2^{n+2} line to 1 line

#Q. A product of sums (POS) expression leads to what kind of logic circuit ?

- (a) OR-AND circuit
- (b) NOR-NOR circuit
- (c) AND-OR-INVERT circuit
- (d) NAND-NAND circuit

#Q. A logic circuit that accepts several data inputs and allows only one of them at a time to get through to the output is called

- (a) Multiplexer
- (b) De-multiplexer
- (c) Transmitter
- (d) Receiver

#Q. A, B and C_{in} are the three inputs of a full adder circuit and D_0, D_1, \dots, D_7 are the inputs of 8 : 1 multiplexer. S_2 (MSB), S_1 and S_0 (LSB) are the selection lines of the multiplexer. To implement the expression of sum of full adder circuit using this multiplexer, the connections of the input ports and selection lines are

- (a) $D_0 = D_3 = D_5 = D_6 = 0, D_1 = D_2 = D_4 = D_7 = 1, S_2 = A, S_1 = B$ and $S_0 = C_{in}$
- (b) $D_0 = D_3 = D_5 = D_6 = 1, D_1 = D_2 = D_4 = D_7 = 0, S_2 = C_{in}, S_1 = B$ and $S_0 = A$
- (c) $D_0 = D_2 = D_3 = D_6 = 0, D_1 = D_4 = D_5 = D_7 = 1, S_2 = A, S_1 = B$ and $S_0 = C_{in}$
- (d) $D_0 = D_1 = D_5 = D_7 = 1, D_2 = D_3 = D_4 = D_6 = 0, S_2 = C_{in}, S_1 = B$ and $S_0 = A$

Thank you
GW
Soldiers!



Electronics and Communication Engineering



Digital Electronics
Lecture 05
Digital Logic



By- CHANDAN JHA SIR



Topics to be Covered

1. Sequential Circuit

Parallel Adder [Ripple carry adder]

n bit

① $(n-1)$ FA + 1 HA

② $n \cdot$ FA

③ $(2n-1)$ HA + $(n-1)$ OR GATE

$$T = (n-1)T_{carry} + \max\{T_{sum}, T_{carry}\}$$

$$T = (n-1) \{ T_{AND} + T_{OR} \} + 2 T_{X-OR}$$

Look ahead carry adder

fastest adder among all the adder.

carry Block delay = $2T$

CARRY BLOCK

complete operation = $4T$

No. of AND = $\frac{n(n+1)}{2}$

No. of OR = n

Sequential circuit

- ✓ Latches
- ✓ FF
- ✓ Designing of FF
- ✓ Registers
- ✓ counters
- ✓ Designing of counter.

#Q. Which of the following statements are correct?

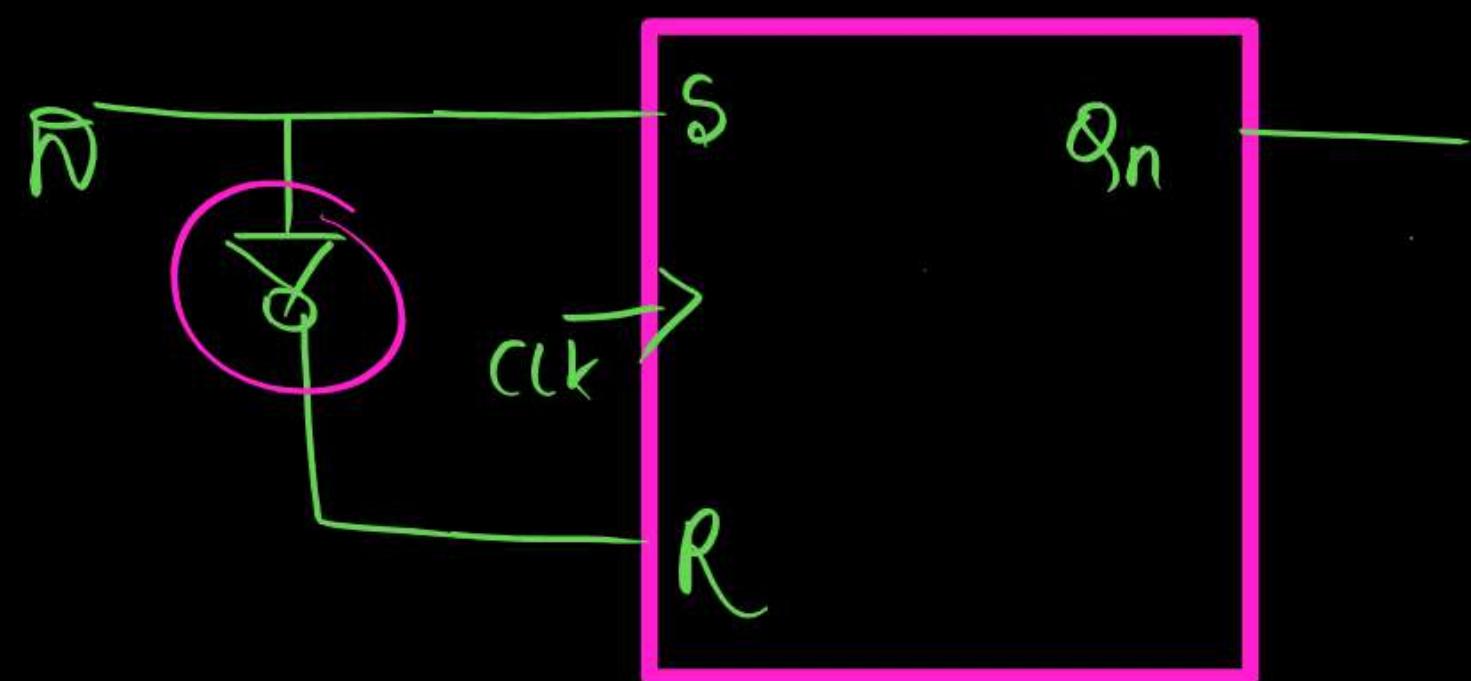
1. A flip-flop is used to store 1 bit of information. ✓
 2. Race-around condition occurs in a J-K flip-flops when both the inputs are 1. ✓
 3. Master-slave configuration is used in flip-flops to store 2 bits of information. ✗
 4. A transparent latch consists of a D-type flip-flop. ✓
- (a) 1, 2 and 3 (b) 1, 3 and 4
(c) 1, 2 and 4 (d) 2, 3 and 4

#Q. For one of the following conditions, clocked J-K flip-flop can be used as DIVIDE BY 2 circuit where the pulse train to be divided is applied at clock input

- (a) J = 1, K = 1 and the flip-flop should have active HIGH inputs
- (b) J = 1, K = 1 and the flip-flop should have active LOW inputs
- (c) J = 0, K = 0 and the flip-flop should have active HIGH inputs
- (d) J = 1, K = 1 and the flip-flop should be a negative edge triggered one

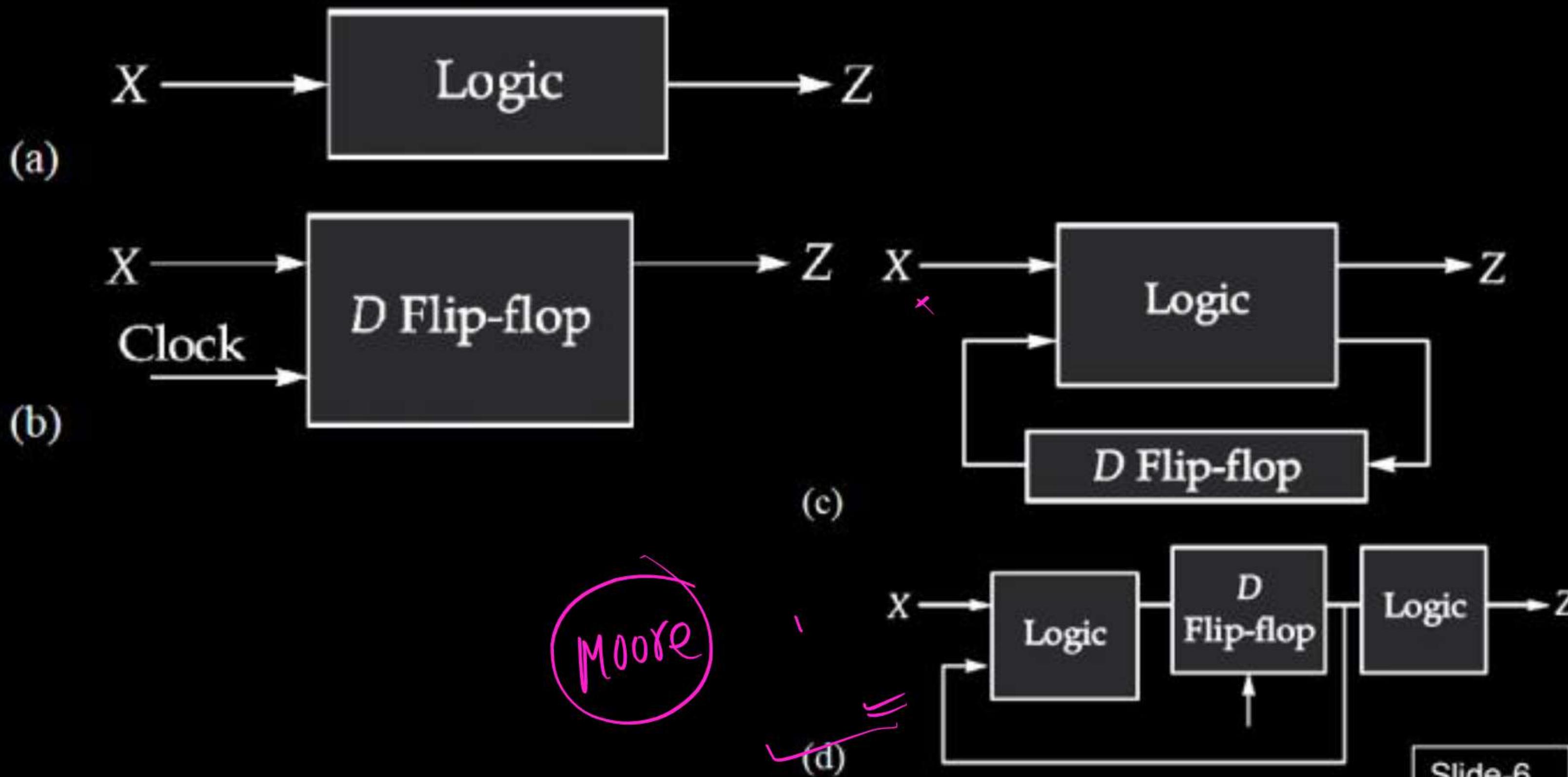
#Q. A S-R flip flop with a clock input can be converted to a 'D' flip flop using

- (a) Two inverters ✗
- (b) the flip flop output (Q & \bar{Q}) connected to its inputs (S & R)
- ~~(c) One inverter~~
- (d) Not possible



$$\begin{aligned}
 Q_{n+1} &= S + \bar{R}Q_n \\
 Q_{n+1} &= \bar{R} + \bar{R}Q_n \\
 Q_{n+1} &= \bar{R} + \bar{R}Q_n \\
 &\Rightarrow D(1 + Q_n) \\
 &= D
 \end{aligned}$$

#Q. Which of the following represents the Moore model for sequential circuits?



#Q. A certain JK FF has $t_{pd} = 12$ ns. The largest MOD counter that can be constructed from such FFs and still operate to 10 MHz is

- (a) 16
- ~~(b) 256~~
- (c) 8
- (d) 128

$$f_{clk} \leq \frac{1}{n \cdot t_{pd_{ff}}}$$

$$10 \times 10^6 \leq \frac{1}{n \cdot 12 \times 10^{-9}}$$

n=8

$$\begin{aligned} \text{Mod} &= 2^n \\ &= 2^6 = 256 \end{aligned}$$

$$n \leq \frac{1}{10 \times 10^6 \times 12 \times 10^{-9}}$$

$$n \leq \frac{1000}{10 \times 12} = 8 \text{ something}$$

#Q. The characteristic equation of the T-FF is given by

(a) $Q^+ = \bar{T}Q$

(b) $Q^+ = T\bar{Q}$

(c) $Q^+ = TQ$

(d) $Q^+ = T\bar{Q} + Q\bar{T}$

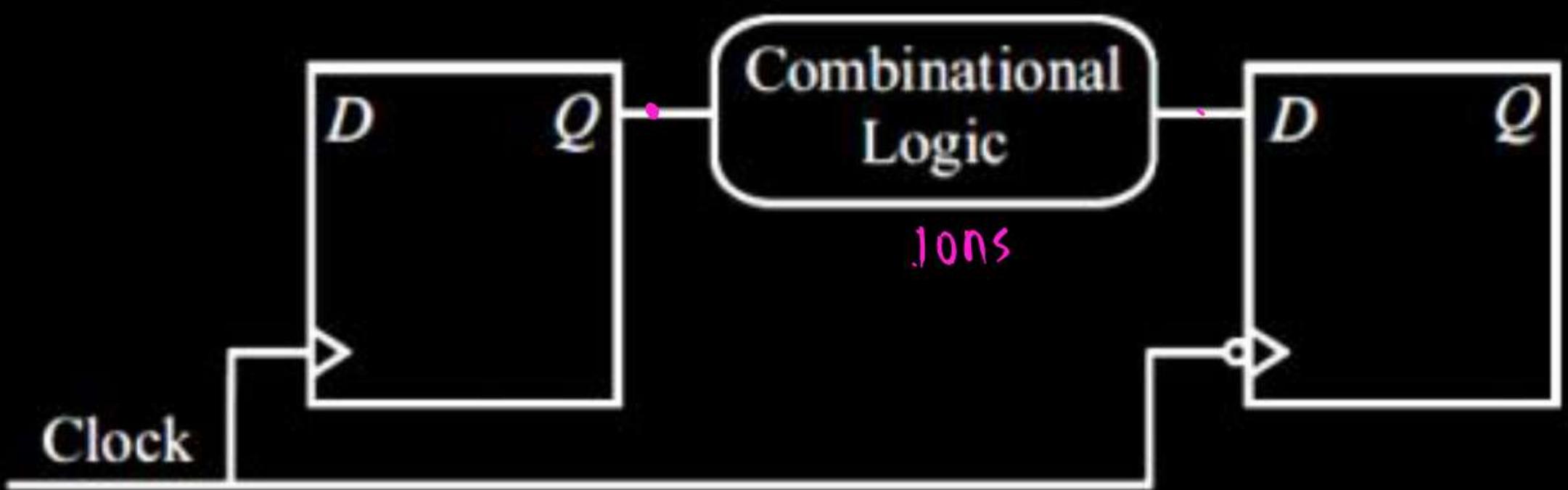
$$Q_{n+1} = S + \bar{R}Q_n$$

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$Q_{n+1} = R$$

$$Q_{n+1} = T \oplus Q_n$$

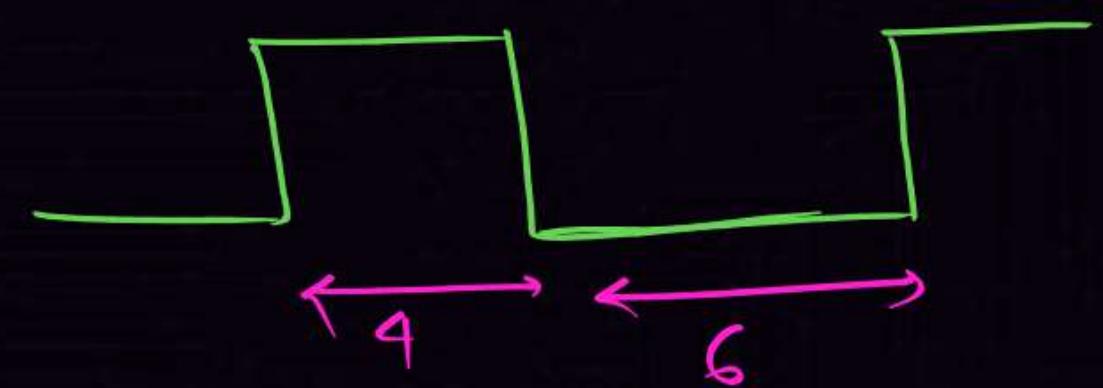
#Q. What is the maximum clock frequency at which following circuit can be operated without timing violations? Assume that the combinational logic delay is 10 ns and the clock duty cycle varies from 40% to 60%.



- (a) 100 MHz
- (b) 50 MHz
- (c) 40 MHz
- (d) 25 MHz

Duty cycle $\Rightarrow \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100$

40%



40% of $T = 10 \text{ ns}$

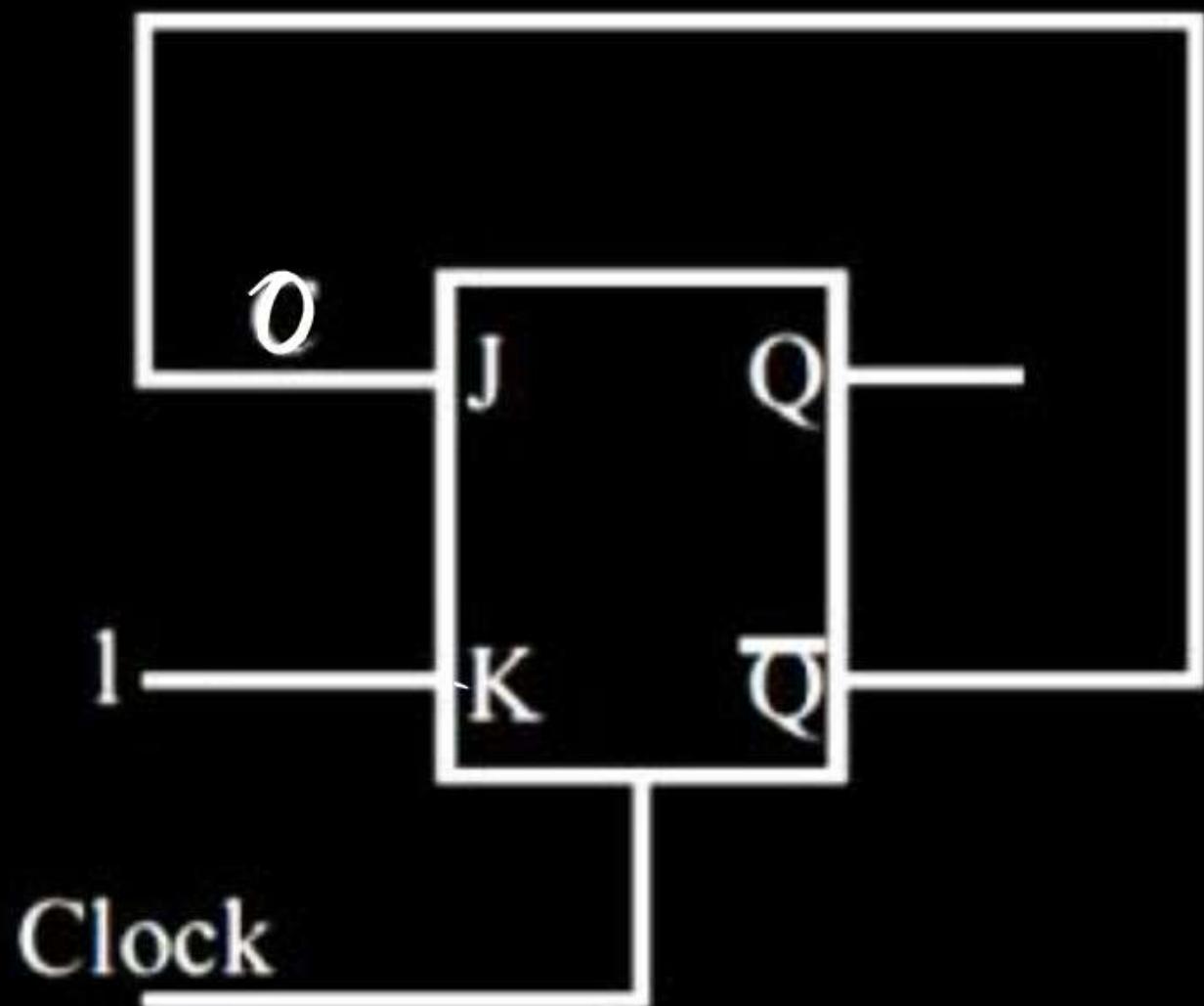
$$\frac{40}{100} \times T = 10 \times 10^{-9}$$

$$T = \frac{2.5}{40} \times 10^{-9} \times 10^6$$

$$T = 25 \times 10^{-9} = 25 \text{ ns}$$

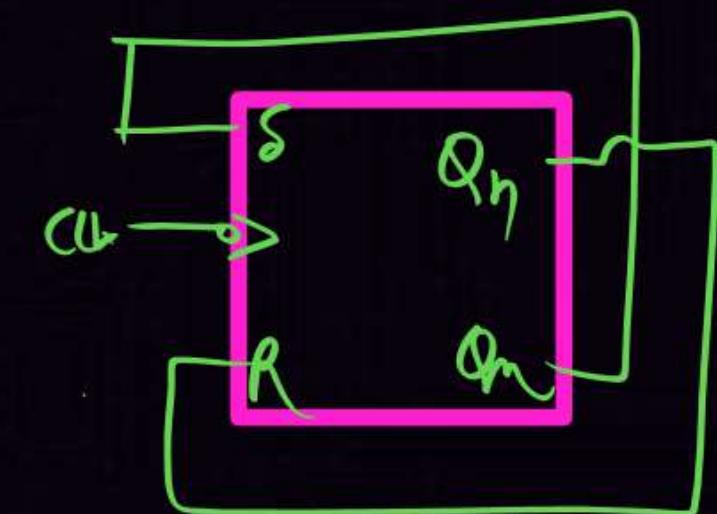
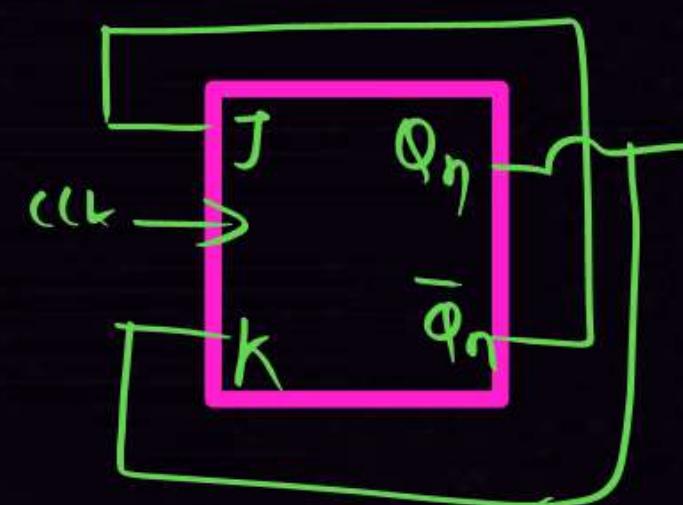
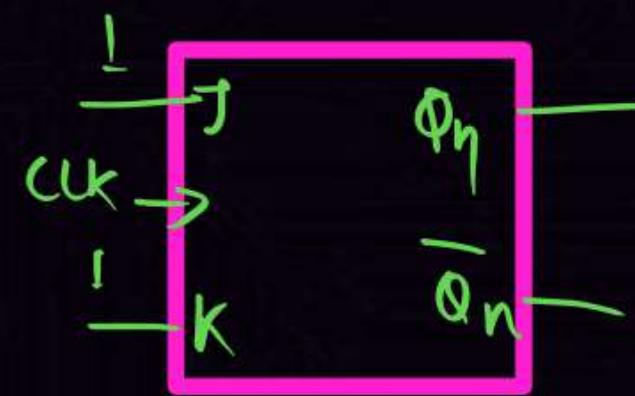
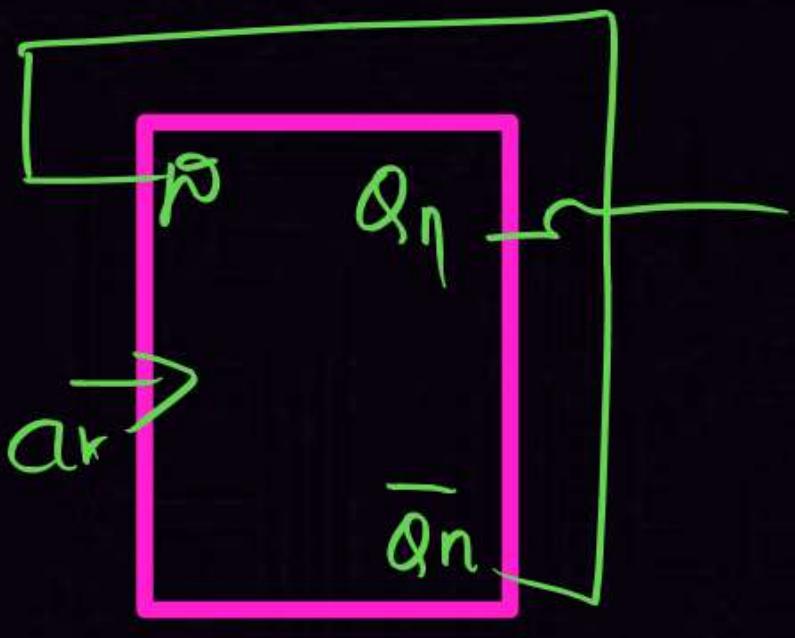
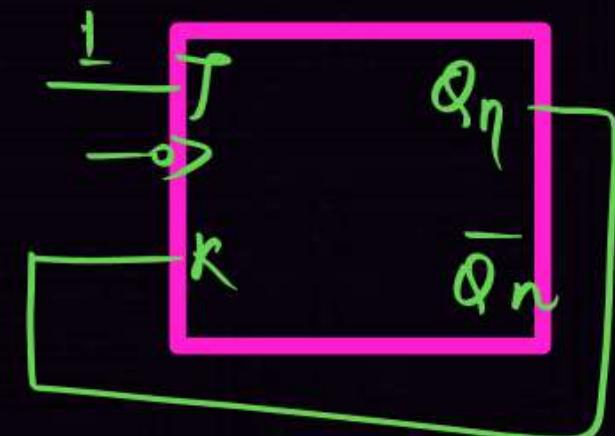
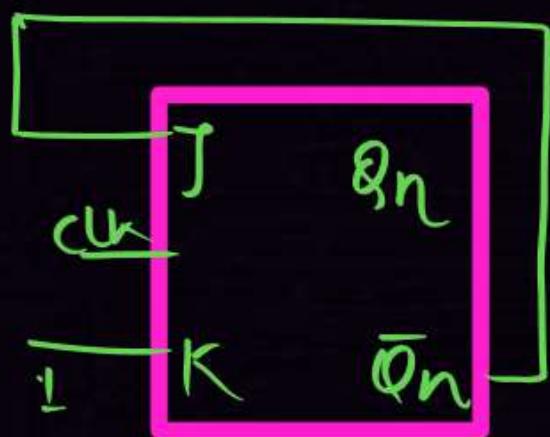
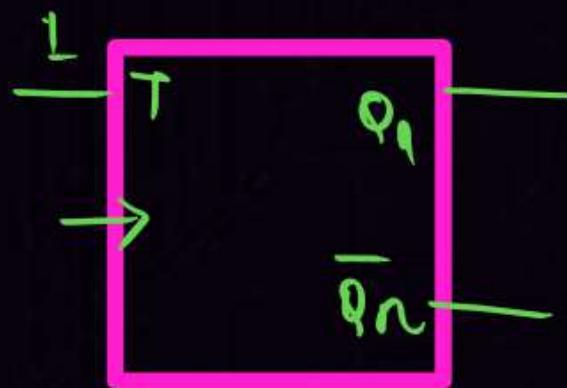
$$f = \frac{1}{T} = \frac{1}{25 \times 10^{-9}} \\ = \frac{10^6}{25} \times 10^6 \\ = 40 \text{ MHz}$$

#Q. In a JK flip-flop we have $J = Q'$ and $K = 1$. Assuming that the flip-flop was initially cleared and clocked for 6 pulses, the sequence at the Q output will be



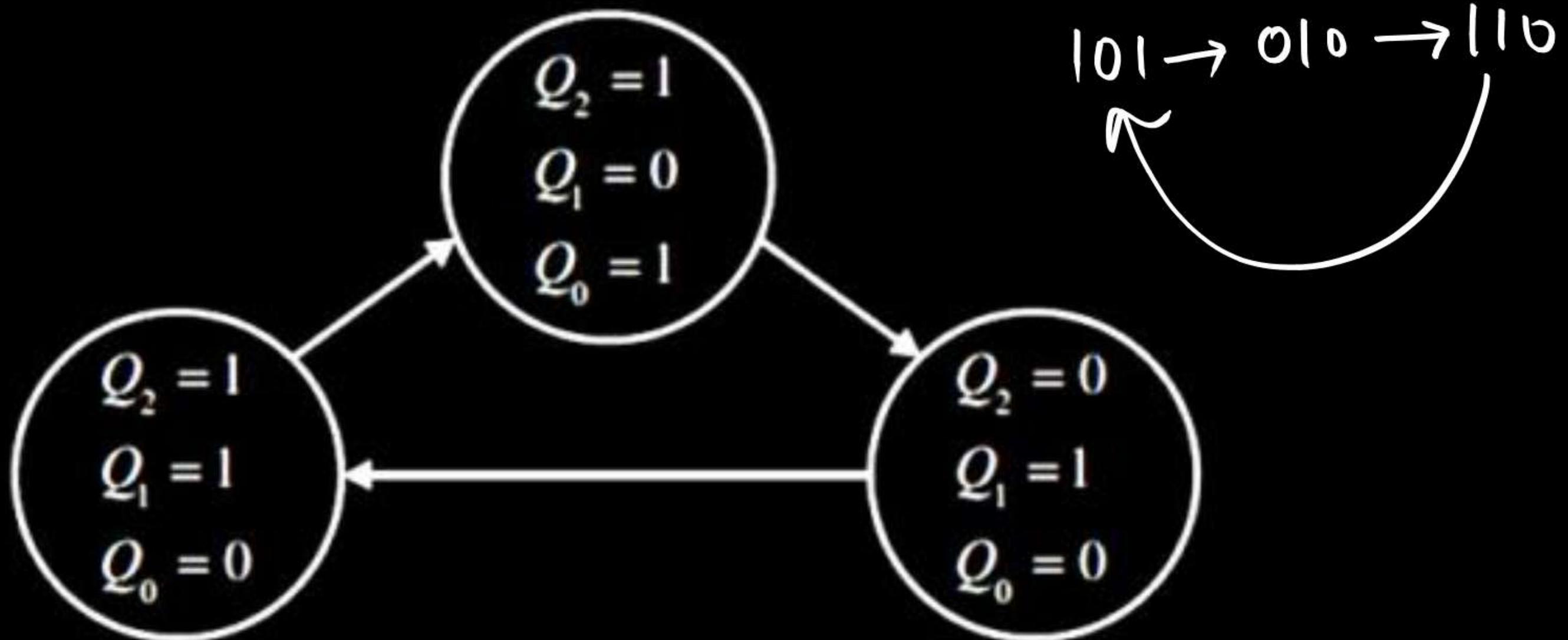
$0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow 0$

- (a) 010000
- (b) 011001
- (c) 010010
- ~~(d)~~ 010101

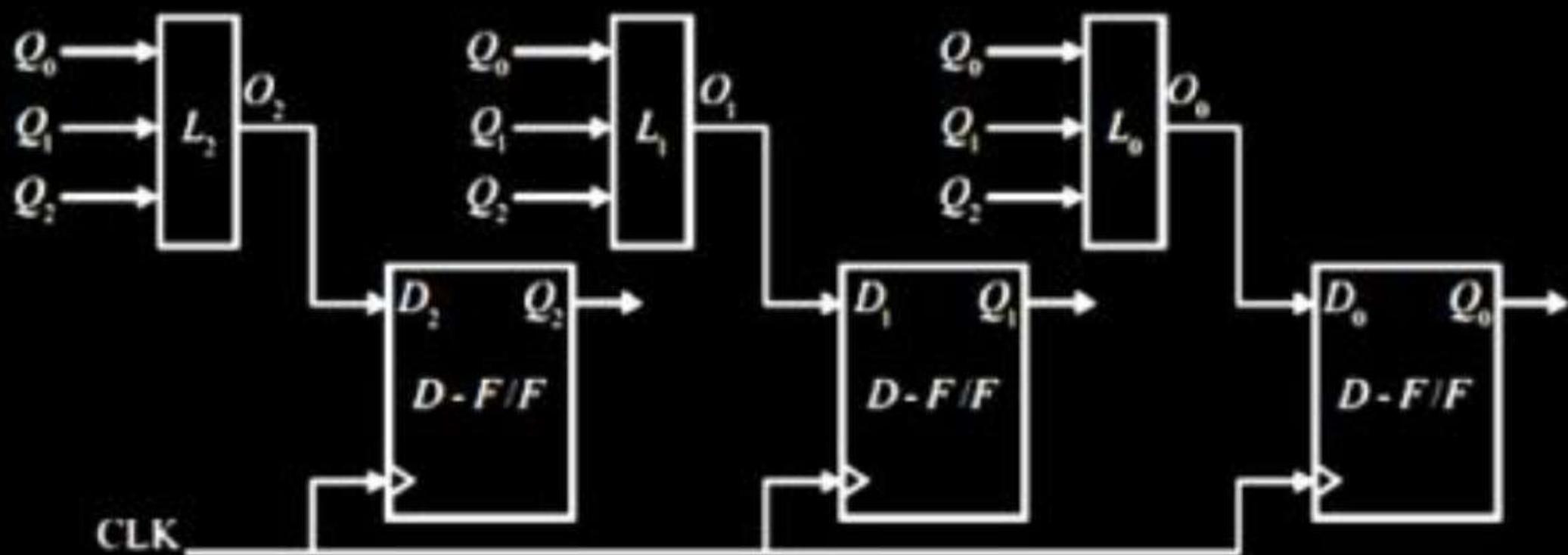


$Q_{n+1} = \bar{Q}_n$ Toggle Mode

#Q. The state transition diagram for a sequence generator is shown in figure



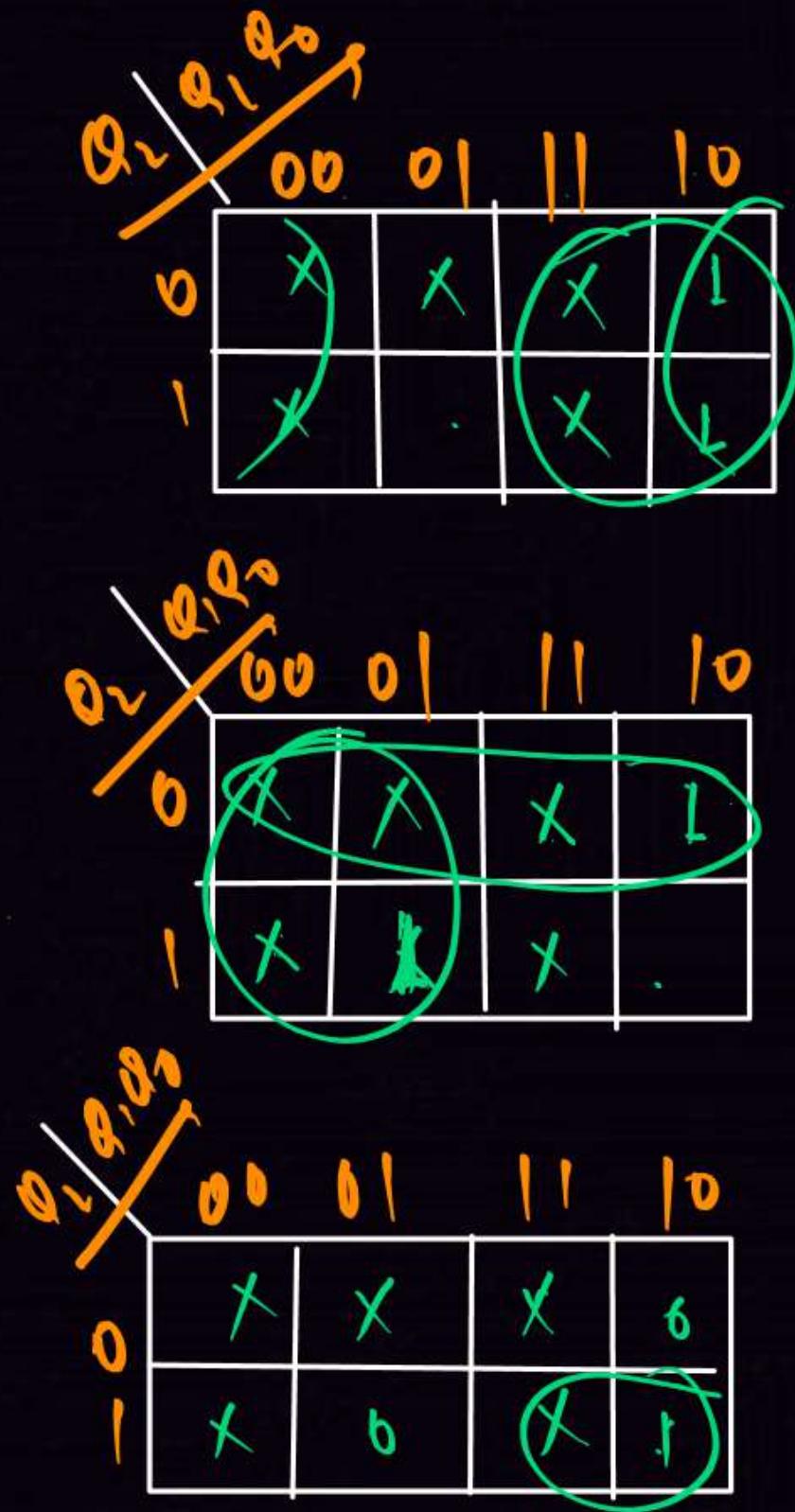
It is designed using D F/Fs and combinational logic blocks L_1, L_2 and L_3 and is initialized at $(Q_2 = 1, Q_1 = 0, Q_0 = 1)$



The minimized expressions for O_0 , O_1 and O_2 are,

- (A) $O_2 = Q_2 \quad O_1 = Q_1 \quad O_0 = Q_0$
- (B) $O_2 = Q_1 \bar{Q}_0 \quad O_1 = \bar{Q}_0 Q_1 \bar{Q}_2 + Q_0 \bar{Q}_1 Q_2 \quad O_0 = \bar{Q}_0 Q_1 Q_2$
- ~~(C)~~ $O_2 = Q_1 \quad O_1 = Q_0 + \bar{Q}_2 \quad O_0 = Q_1 Q_2$
- (D) None of above

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	D_2	D_1	D_0
0	0	0	X	X	X	X	X	X
0	0	1	X	X	X	X	X	X
0	1	0	1	1	0	1	1	0
0	1	1	X	X	Y	X	X	X
1	0	0	X	X	X	X	X	X
1	0	1	0	1	0	0	1	0
1	1	0	1	0	1	1	0	1
1	1	1	X	X	X	X	X	X



$$D_2 = \overline{Q_0}$$

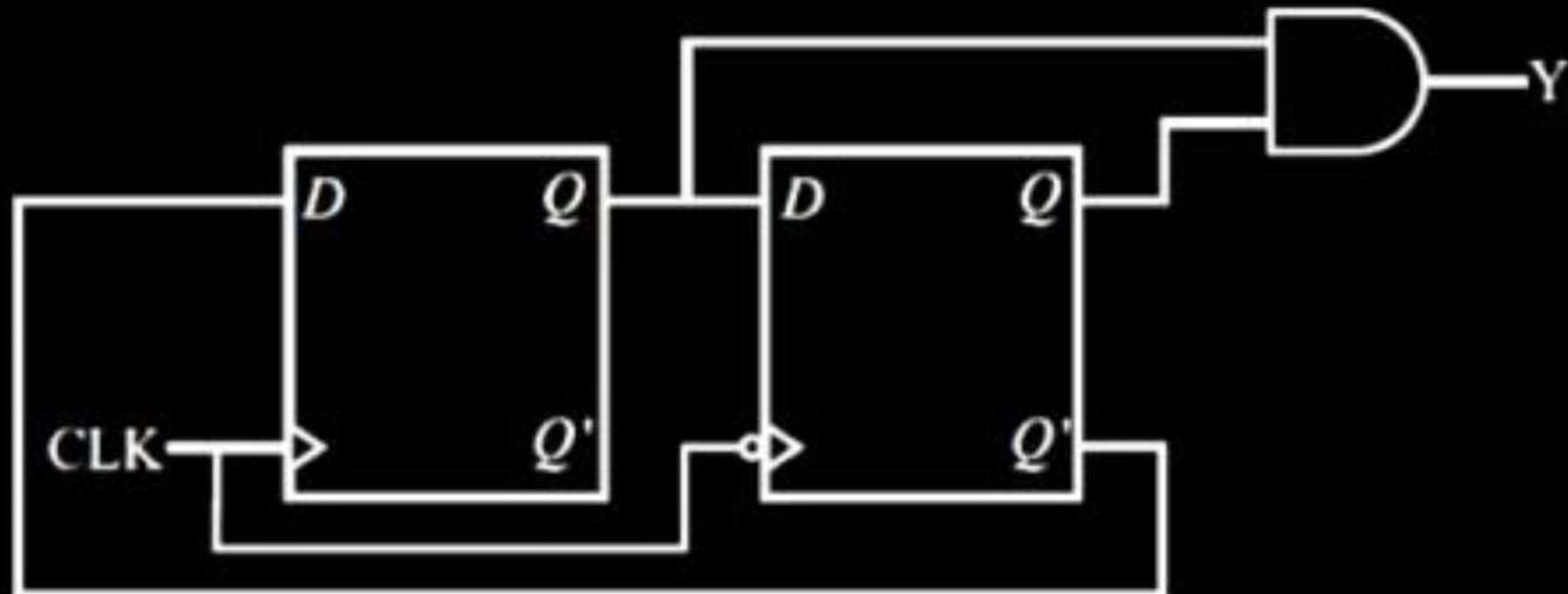
$$D_2 = Q_1$$

$$D_1 = \overline{Q_2} + \overline{Q_1}$$

$$D_1 = \overline{Q_2} + Q_0$$

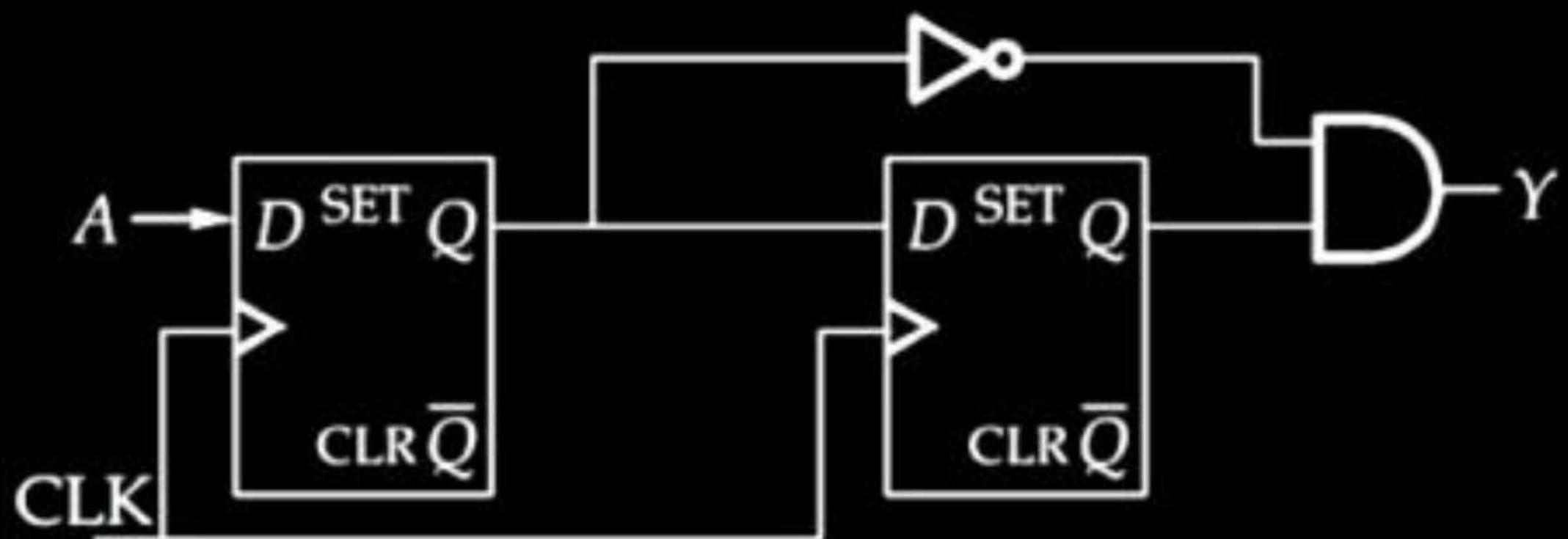
$$D_0 = Q_2 Q_1$$

#Q. What is the frequency and duty cycle of output Y, when clk frequency is 1 MHz
@ 50% duty cycle?



- (a) 500 kHz @ 50% duty cycle
- (b) 500 kHz @ 25% duty cycle
- (c) 250 kHz @ 50% duty cycle
- (d) 250 kHz @ 25% duty cycle

#Q. What is the functionality of following digital circuit? A is input data, CLK is system clock and Y is output.



- (a) Falling edge detection of input A
- (b) Clock division by 2
- (c) Rising edge detection of input A
- (d) Clock division by 4

#Q. A 1 MHz clock signal is applied to a J-K flip-flop with $J = K = 1$. What is the frequency of the flip-flop output signal ?

- (a) 2 MHz
- (b) 500 kHz
- (c) 260 kHz
- (d) 500 MHz

#Q. Assertion (A) : D-latch and edge-triggered D flip-flop (FF) are functionally different.

Reason (R): In D-latch the output (O) cannot change while enable (EN) is High.
In D-FF the output can change only on the active edge of CLK.

- (a) Both A and R are true and R is the correct explanation of A
- (b) Both A and R are true but R is NOT the ' correct explanation of A
- (c) A is true but R is false
- (d) A is false but R is true

#Q. Assertion (A): D-flip flops are used to construct a buffer register.

Reason (R) : Buffer registers are used to store a binary word temporarily.

- (a) Both A and R are true and R is the correct explanation of A
- (b) Both A and R are true but R is NOT the correct explanation of A
- (c) A is true but R is false
- (d) A is false but R is true

#Q. D flip-flop can be made from a J-K flip-flop by making

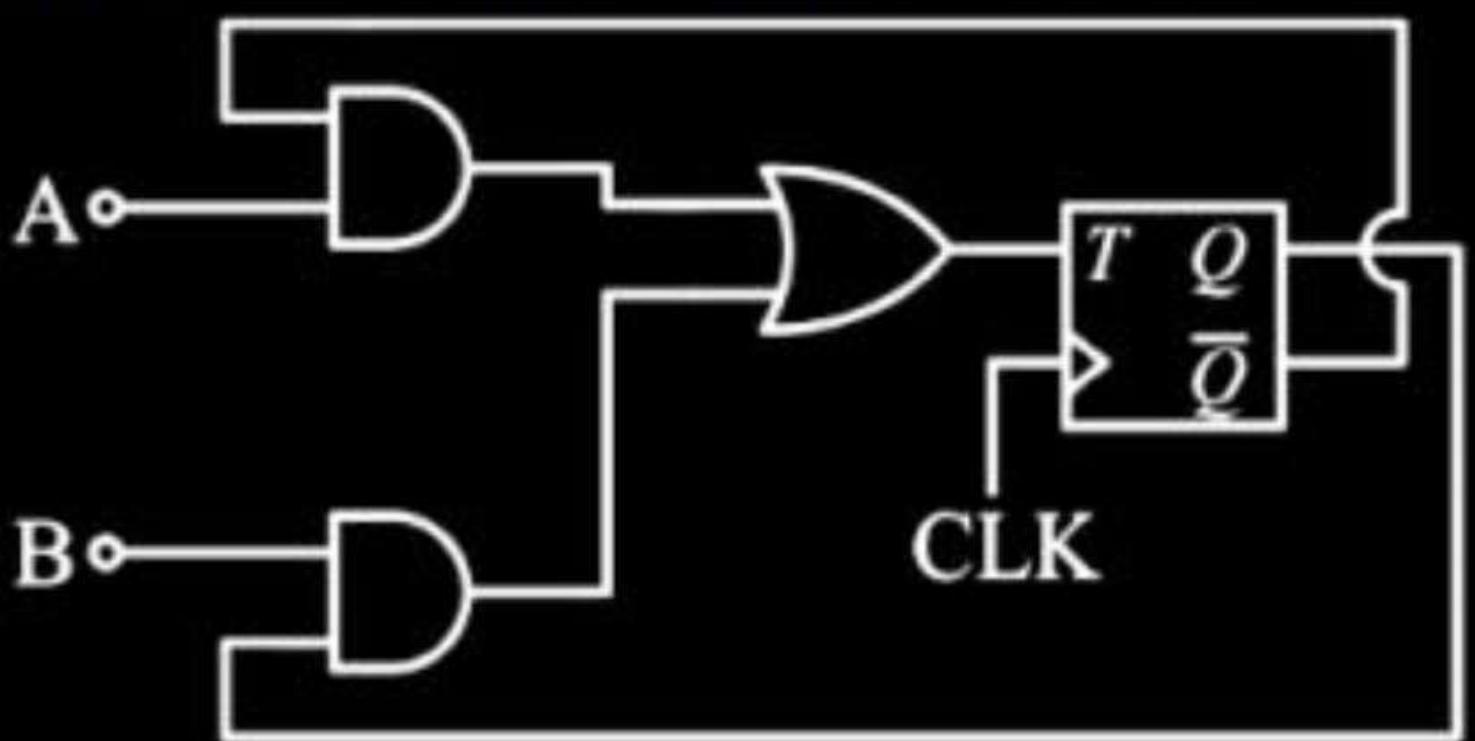
- (a) $J = K$
- (b) $J = K = 1$
- (c) $J = 0, K = 1$
- (d) $J = \bar{K}$

#Q. For a JK flip-flop, Q_n is output at time step t_n .

Which of the following Boolean expressions represents Q_{n+1} ?

- (a) $J_n \bar{Q}_n + \bar{K}_n Q_n$
- (b) $J_n Q_n + K_n \bar{Q}_n$
- (c) $\bar{J}_n Q_n + K_n \bar{Q}_n$
- (d) $J_n Q_n + \bar{K}_n \bar{Q}_n$

#Q. What is represented by the digital circuit given below?



- (a) An SR flip-flop with $A = S$ and $B = R$
- (b) A JK flip-flop with $A = K$ and $B = J$
- (c) A JK flip-flop with $A = J$ and $B = K$
- (d) An SR flip-flop with $A = R$ and $B = S$

#Q. Match List-I (Logic circuit / function) with List-II (Circuit realization) and select the correct answer using the code given below the lists :

List-I

A. D flip-flop

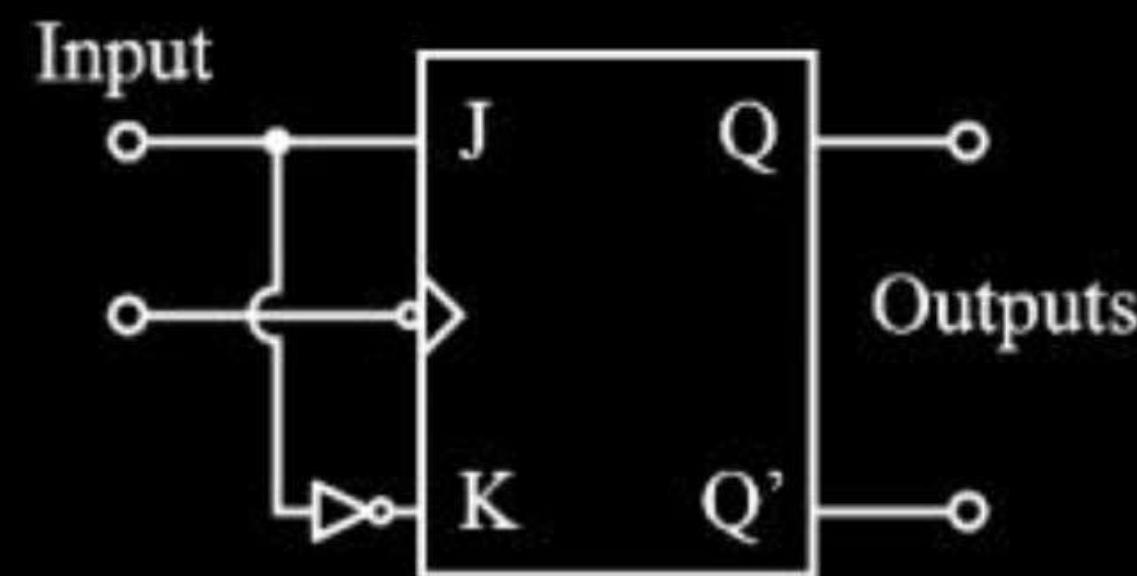
B. T flip-flop

List-II

1.

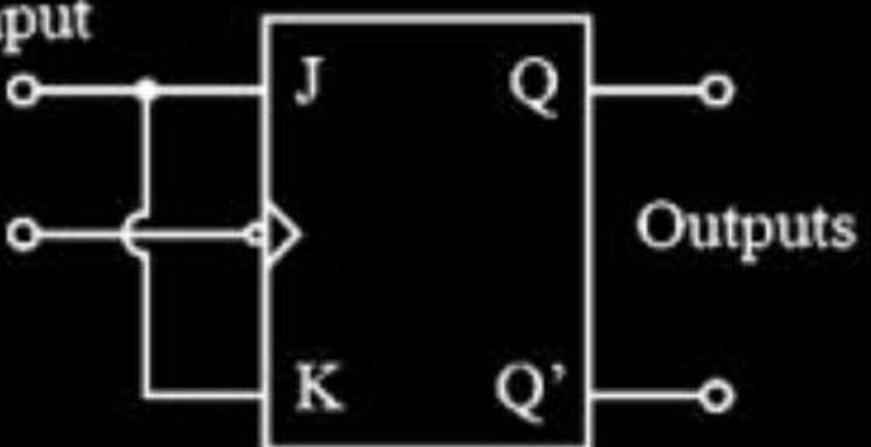


2.



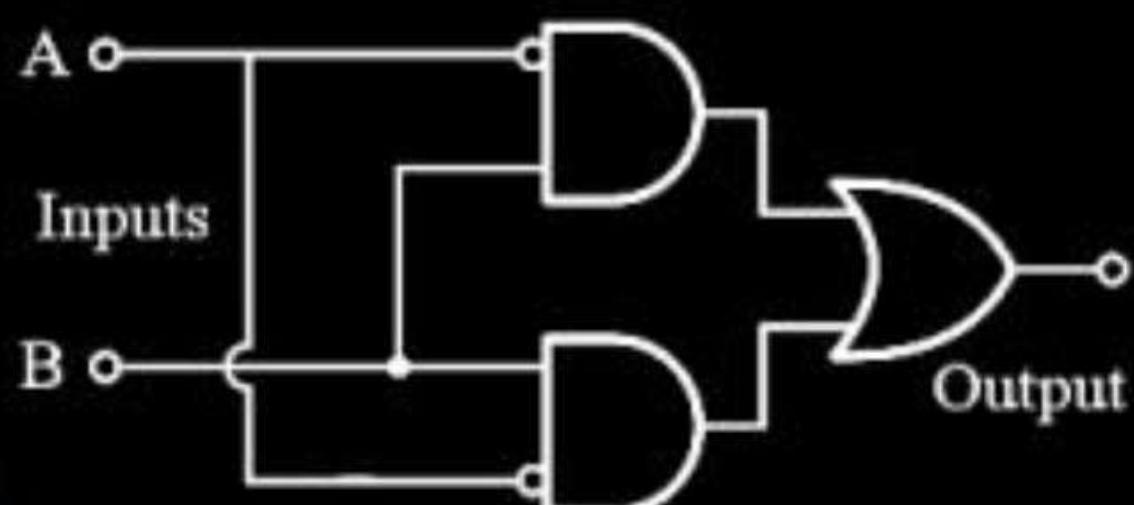
C. Exclusive OR

3.



D. Half-adder

4.



Codes: A B C D

- (a) 3 2 4 1
- (b) 2 3 4 1
- (c) 1 3 4 2
- (d) 2 4 3 1

#Q. A J-K flip-flop can be made from an S-R flip-flop by using two additional

- (a) AND gates
- (b) OR gates
- (c) NOT gates
- (d) NOR gates

#Q. Consider the following statements in Johnson counter:

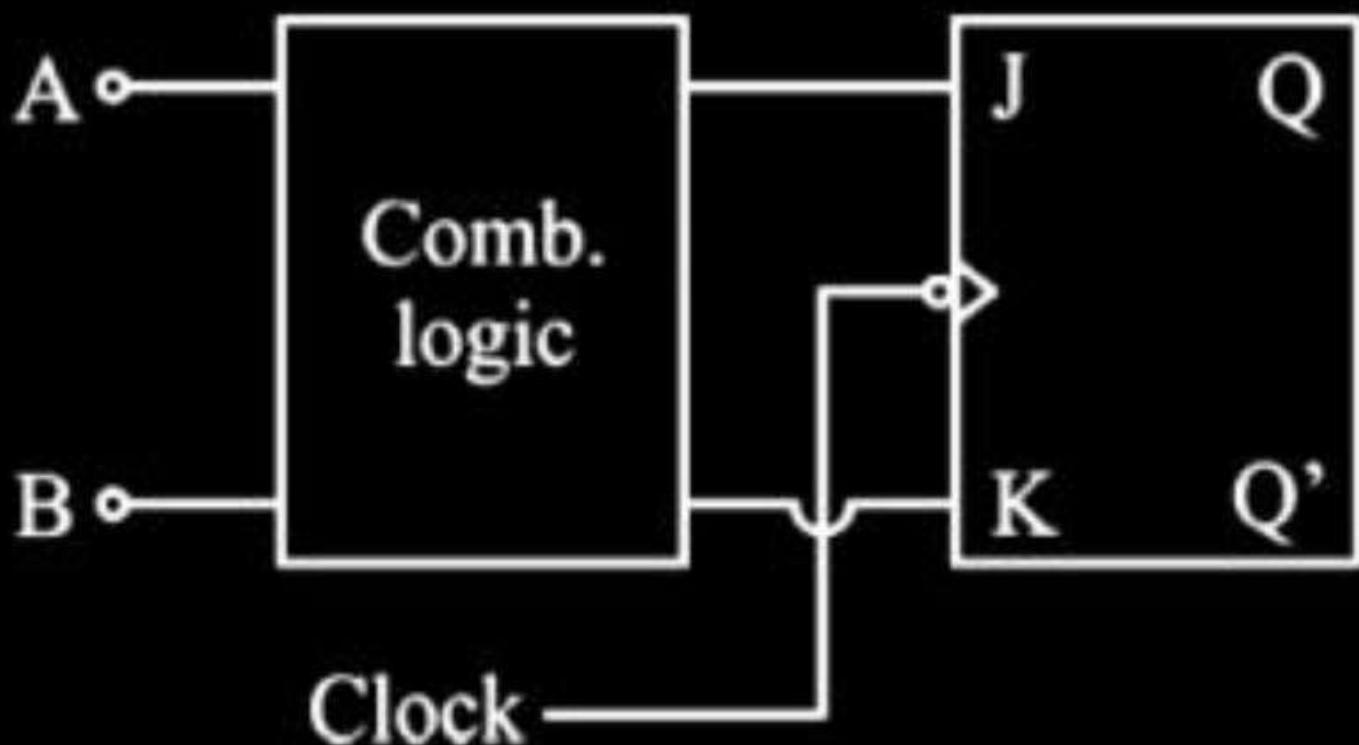
1. A MOD-6 Johnson counter requires 3 FFs.
2. Johnson counter requires decoding gates.
3. To decode each count, one logic gate is used. Each gate requires only two inputs regardless of the number of FFs.

Which of these statements are correct?

- | | |
|-------------|----------------|
| (a) 1 and 2 | (b) 2 and 3 |
| (c) 1 and 3 | (d) 1, 2 and 3 |

#Q. The following truth table has to be realized with the circuit shown in the figure:

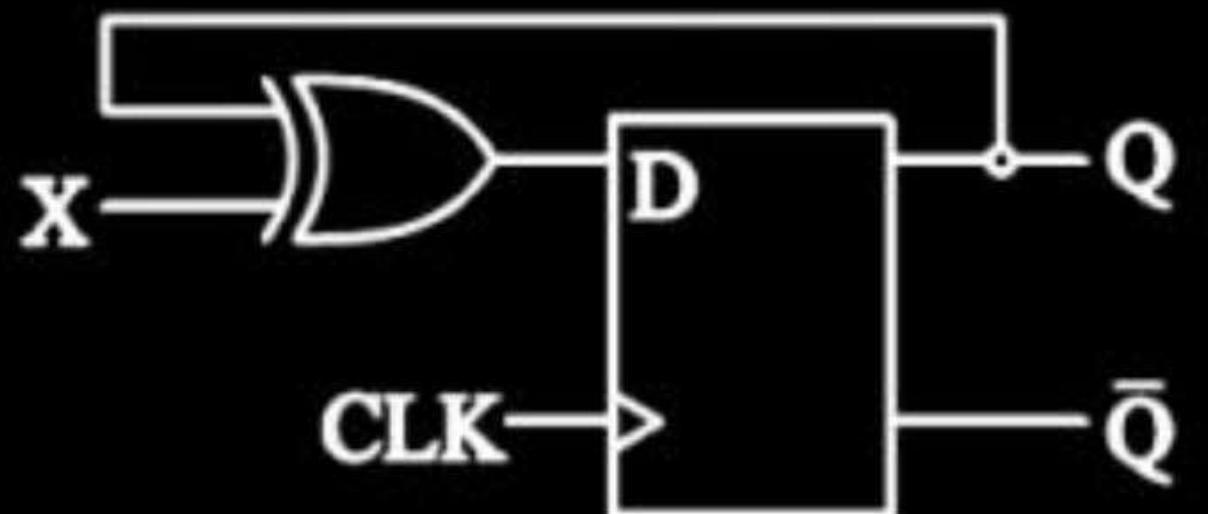
A	B	Q_{n+1}
0	0	Q'_n
0	1	1
1	0	Q_n
1	1	0



What is the output of the combinational logic circuit to the J input?

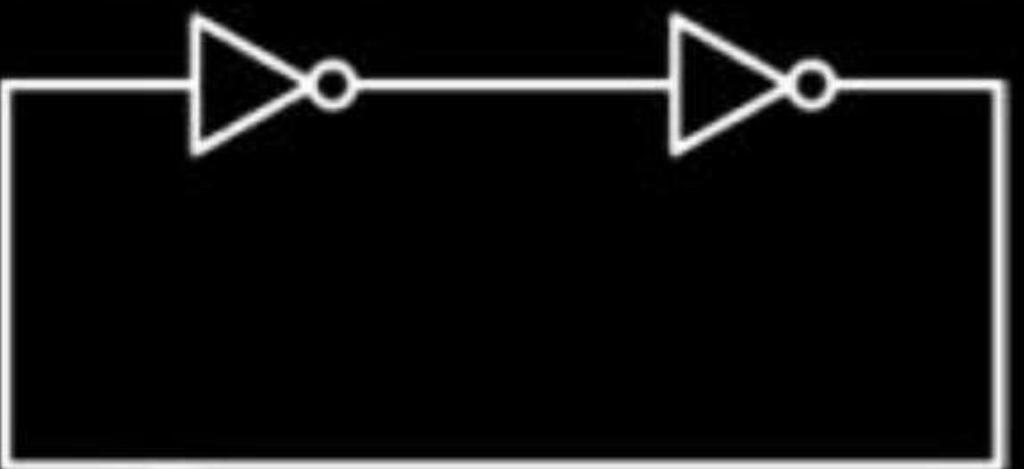
- (a) \overline{AB}
- (b) \overline{A}
- (c) \overline{B}
- (d) AB

#Q. The digital circuit as shown below represents to which one of the following?



- (a) JK flip-flop
- (b) Clocked RS flip-flop
- (c) T flip-flop
- (d) Ring counter

#Q. The digital circuit using two inverters as shown in the figure below acts as



- (a) A bistable multivibrator
- (b) A astable multivibrator
- (c) A monostable multivibrator
- (d) An oscillator

#Q. Which of the following is correct for a gated D-type flip flop ?

- (a) The output is either SET or RESET as soon as the D input goes HIGH or LOW.
- (b) The output complement follows the input when enabled.
- (c) Only one of the inputs can be HIGH at a time.
- (d) The output toggles if one of the inputs is held HIGH.

#Q. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature?

- (a) Asynchronous operation
- (b) Low input voltage
- (c) Gate impedance
- (d) Cross coupling

#Q. **Statement (I)** : As applied to flip-flops, asynchronous inputs are overriding inputs.

Statement (II) : Direct inputs of flip-flops are effective even in the absence of the control/clock input.

- (a) Both Statement (I) and Statement (II) are individually true and Statement (II) is the correct explanation of Statement (I).
- (b) Both Statement (I) and Statement (II) are individually true but Statement (II) is not the correct explanation of Statement (I).
- (c) Statement (I) is true but Statement (II) is false.
- (d) Statement (I) is false but Statement (II) is true.

#Q. Race-around condition occurs in

- (a) Multiplexer
- (b) ROM
- (c) Flip-flops
- (d) Voltage regulator

#Q. Consider the following statements :

1. Race-around condition occurs in a JK flipflop when the inputs are 1, 1.
2. A flip-flop is used to store one bit of information.
3. A transparent latch consists of D-type flipflops.
4. Master-slave configuration is used in a flipflop to store 2-bits of information.

Which of the above statements are correct?

- (a) 1, 2 and 3 only (b) 1, 2 and 4 only
(c) 3 and 4 only (d) 1, 2, 3 and 4

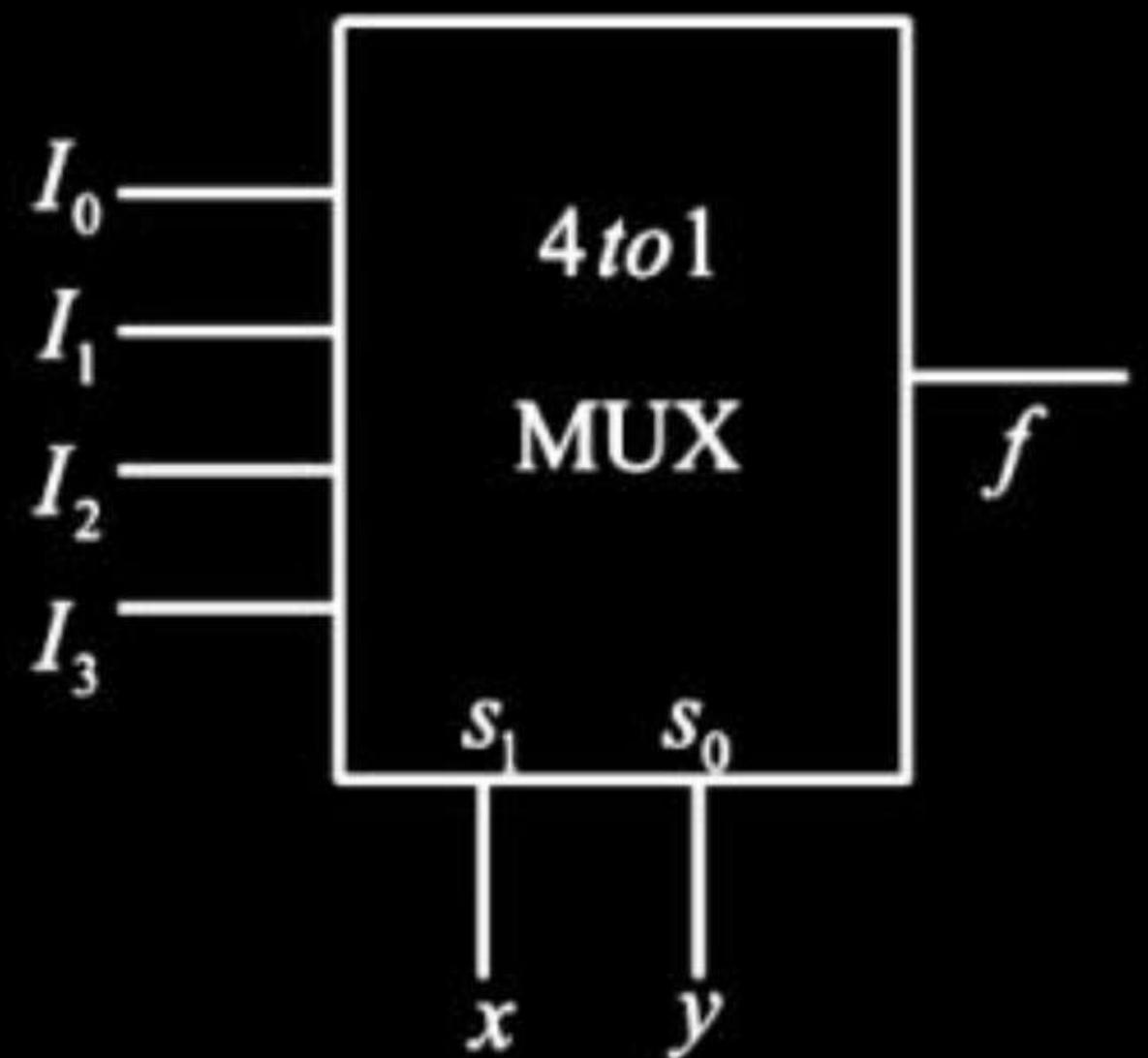
#Q. Consider the following circuits:

1. Full adder
2. Half adder
3. JK flip-flop
4. Counter

Which of the above circuits are classified as sequential logic circuits?

- (a) 1 and 2
- (b) 3 and 4
- (c) 2 and 3
- (d) 1 and 4

#Q. Which logic inputs should be given to the input lines I_0, I_1, I_2 and I_3 if the MUX is to behave two input XNOR gate?



- (a) 01110
- (b) 1001
- (c) 1010
- (d) 1111

#Q. The time delay in a look-ahead carry adder is independent of

- (a) Number of operands only
- (b) Propagation delay only
- (c) Number of bits in the operand only
- (d) Bits in the operand, number of operands and propagation delay

#Q. Consider the following statements:

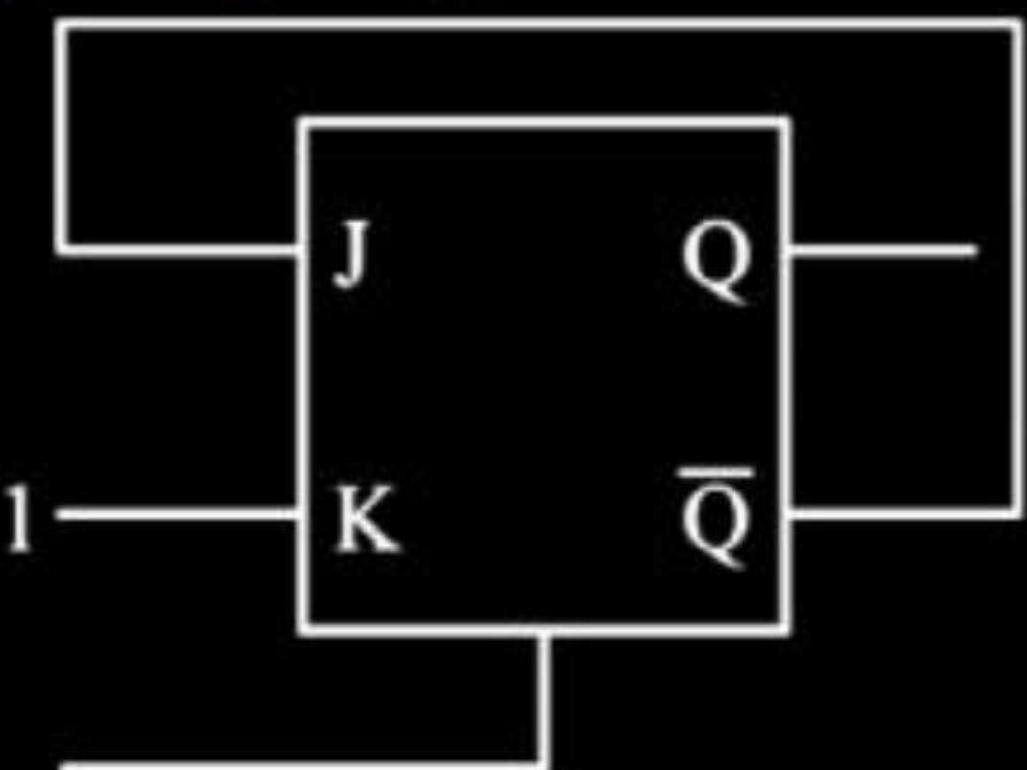
For a master-slave J-K flip-flop,

1. The toggle frequency is the maximum clock frequency at which the flip-flop will toggle reliably
2. The data input must precede the clock triggering edge transition time by some minimum time.
3. The data input must remain fixed for a given time after the clock triggering edge transition time for reliable operation.
4. Propagation delay time is equal to the rise time and fall time of the data.

Which of the statements given above are correct?

- (a) 1, 2 and 3 (b) 1, 2 and 4
(c) 1, 3 and 4 (d) 2, 3 and 4

#Q. Consider the following J-K flip-flop.



In the above J-K flip-flop, $J = \bar{Q}$ and $K = 1$. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

- (a) 01000
- (b) 011001
- (c) 010010
- (d) 010101

#Q. Match List-I (Type of flip-flop) with List-II (Symbol) and select the correct answer using the codes given below the lists:

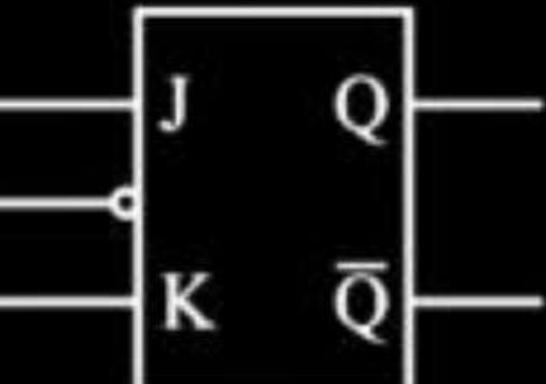
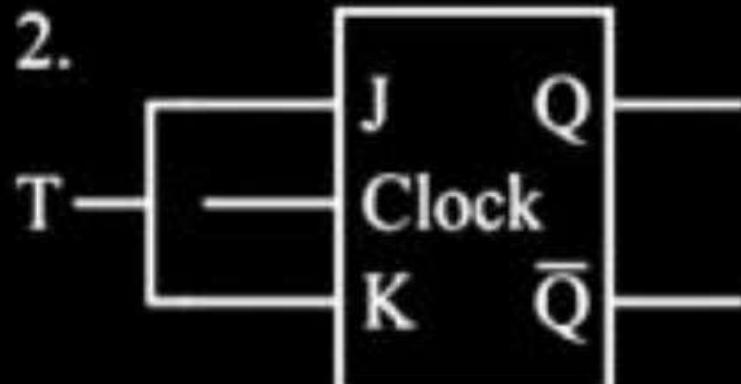
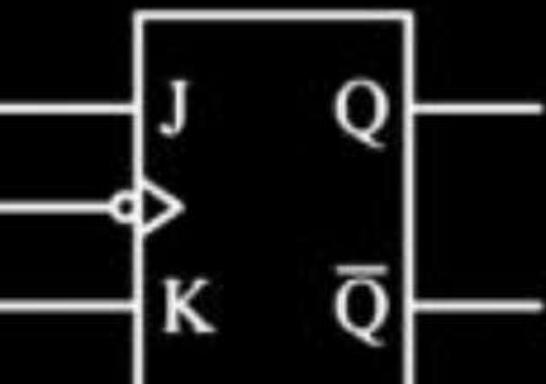
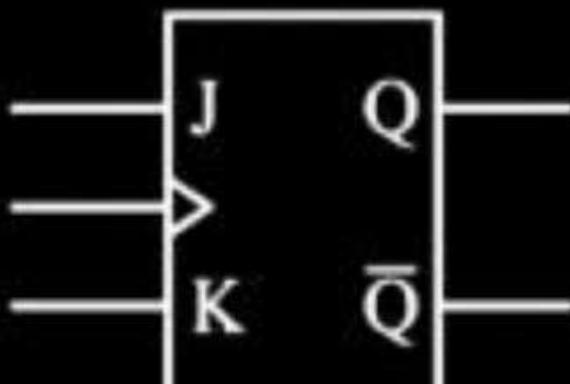
List-I

- A. T flip-flop
- B. Level-triggered JK flip-flop
- C. Leading edge-triggered JK flip-flop
- D. Trailing edge-triggered JK flip-flop

Codes: A B C D

- (a) 1 2 3 4
- (b) 2 1 3 4
- (c) 1 2 4 3
- (d) 2 1 4 3

List-II

- 1. 
- 2. 
- 3. 
- 4. 

#Q. Which one of the following equations satisfies the JK flip-flop truth table?

- (a) $Q_{n+1} = J_n \bar{Q}_n + \bar{K}_n Q_n$
- (b) $Q_{n+1} = \bar{J}_n \bar{Q}_n + \bar{K}_n Q_n$
- (c) $Q_{n+1} = J_n Q_n + K_n Q_n$
- (d) $Q_{n+1} = \bar{J}_n \bar{Q}_n + \bar{K}_n \bar{Q}_n$

#Q. A master slave configuration consists of two identical flip-flop connected in such a way that the output of the master is input to the slave. Which one of the following is correct?

- (a) Master is level triggered and slave is edge triggered.
- (b) Master is edge triggered and slave is level triggered
- (c) Master is positive edge triggered and slave is negative edge triggered.
- (d) Master is negative edge triggered and slave is positive edge triggered.

#Q. A 1 ms pulse can be converted into a 10ms pulse by using which one of the following?

- (a) An astable multivibrator
- (b) A mono stable multivibrator
- (c) A bi stable multivibrator
- (d) A J-K flip-flop

#Q. Which of the following flip-flop is used as a latch?

- (a) J K flip-flop
- (b) R S flip-flop
- (c) T flip-flop
- (d) D flip-flop

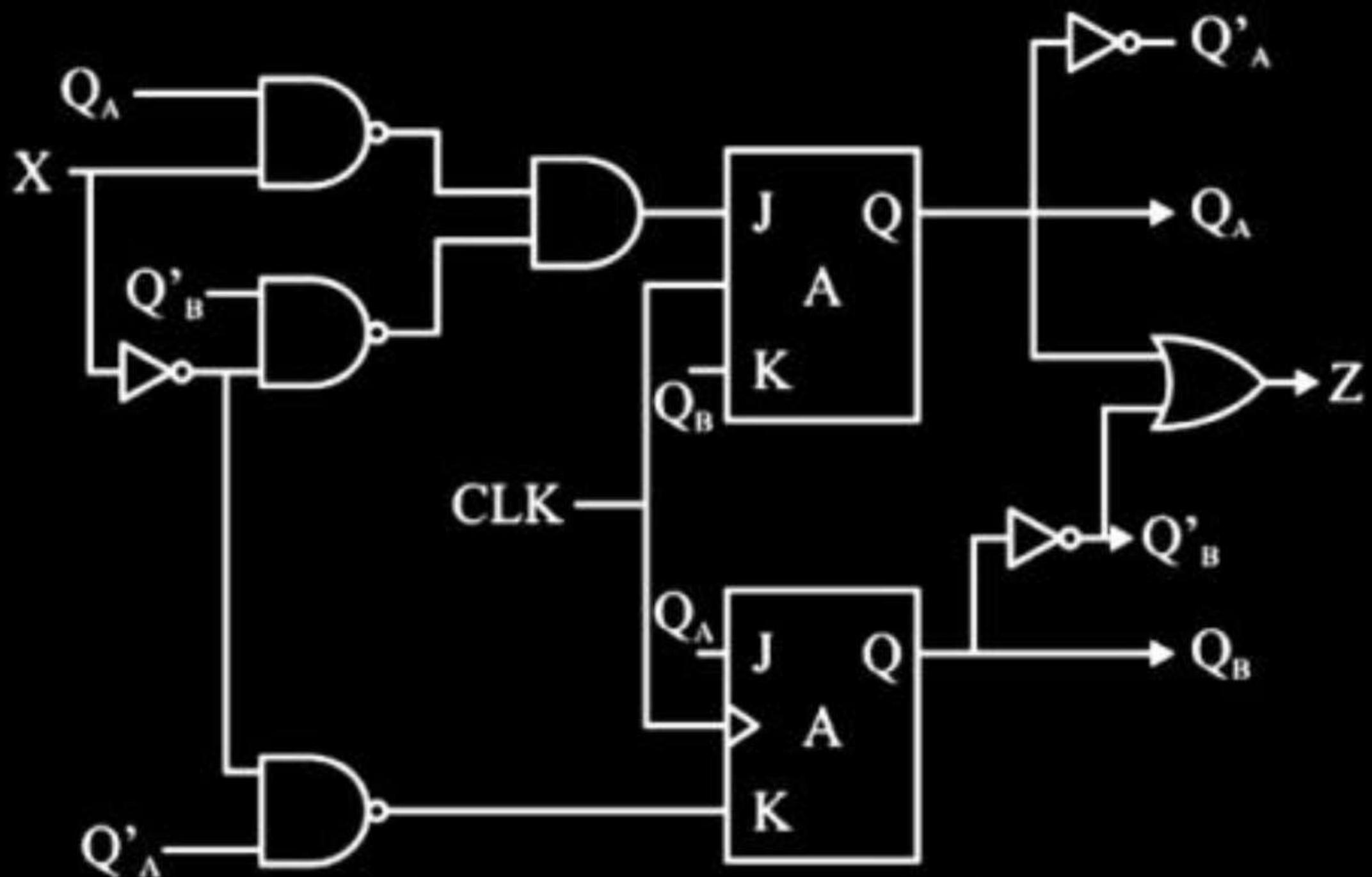
#Q. Which of the following conditions should be satisfied to call an astable multivibrator circuit using discrete components as a digital circuit?

1. A flip-flop is always a digital circuit.
2. Only when we assign 1 and 0 to the high and low levels of the output, a flip-flop is called a digital circuit
3. Only if the power supply voltage is maintained at +5 V or -5 V, it is called a digital circuit.
4. Only if it is in IC form, following the technology of IC manufacture, it is called a digital circuit.

Select the correct answer from the codes given below:

- | | |
|------------|------------------|
| (a) 1 only | (b) 2 and 3 only |
| (c) 2 only | (d) 3 and 4 |

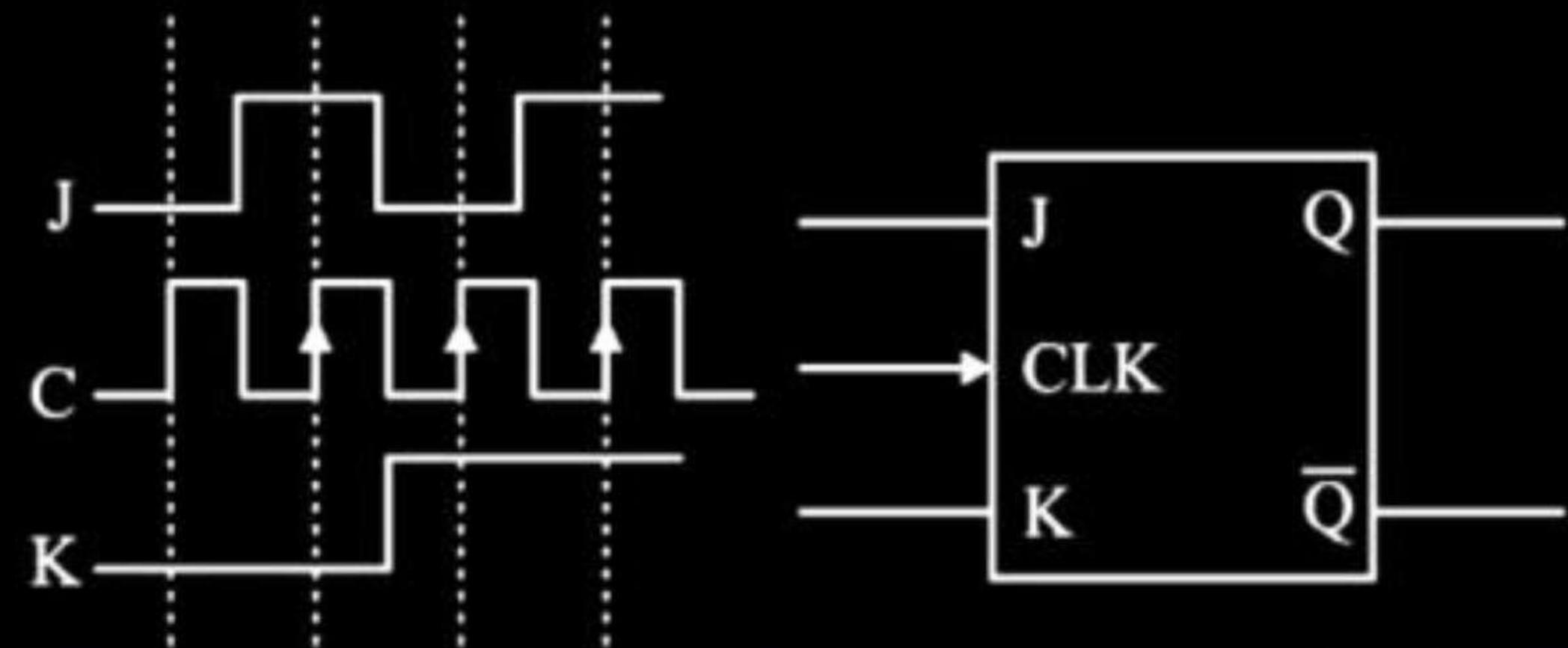
#Q.



Analyze the sequential circuit shown above in figure. Assuming that initial sequence would lead to state 11. What is the initial sequence?

- (a) 1 - 1
- (b) 1 - 0
- (c) 0 - 0
- (d) state 11 is unreachable.

#Q.



The J-K flip-flop shown above is initially reset so that $Q = 0$. If a sequence of four clock pulses is then applied, with the J and K inputs as given in the figure, the resulting sequence of values that appear at the output Q starting with its initial state, is given by:

- (a) 01011
- (b) 01010
- (c) 00110
- (d) 00101

#Q.

X	Y	Q _{n+1}
0	0	1
0	1	Q _n
1	0	\bar{Q}_n
1	1	0

An X-Y flip flop, whose characteristic table is given above is to be implemented using JK flip flop. This can be done by making

- (a) J = X, K = \bar{Y}
- (b) J = \bar{X} , K = Y
- (c) J = Y, K = \bar{X}
- (d) J = \bar{Y} , K = X

#Q. If both inputs of S-R NAND latch are low, the output will be

- (a) Unpredictable
- (b) Toggle
- (c) Reset
- (d) Remain same

#Q. A bistable multi-vibrator that functions as a voltage comparator with hysteresis is called

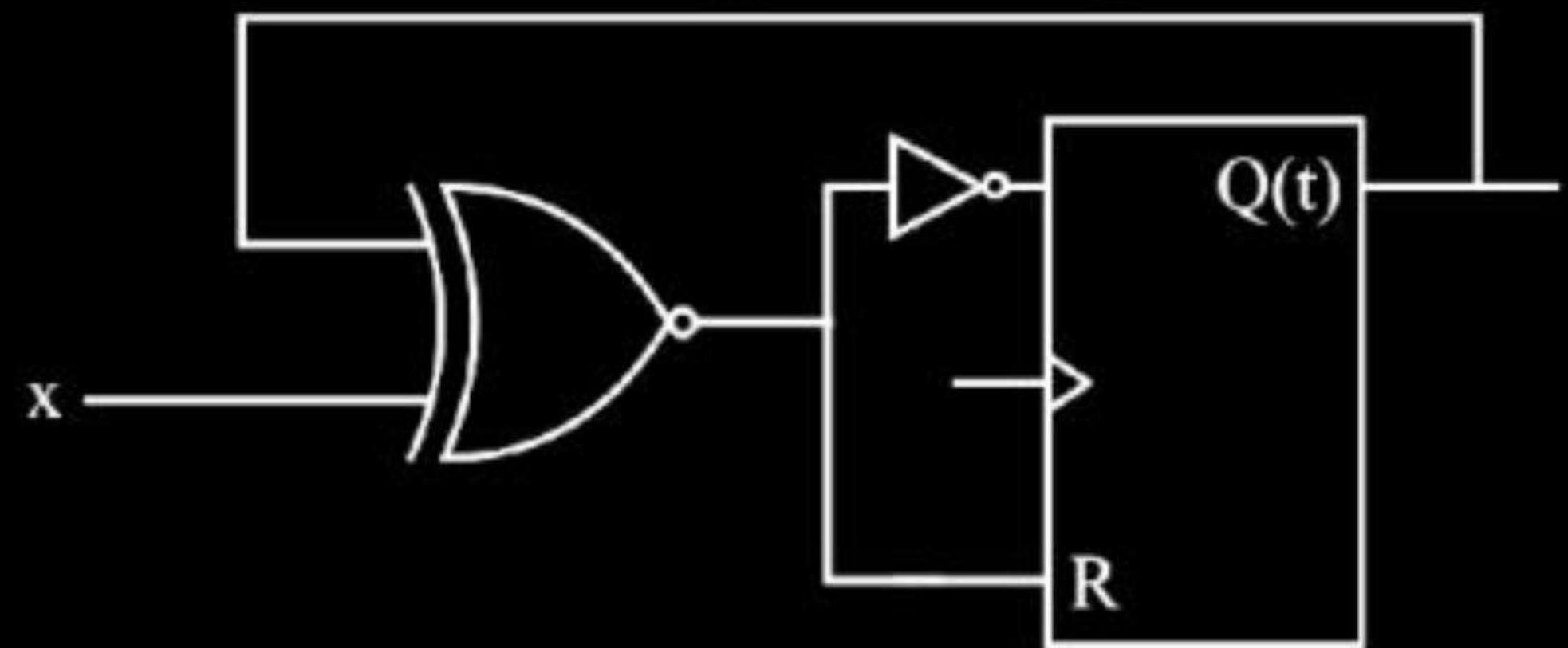
- (a) T flip-flop
- (b) D flip-flop
- (c) J-K flip-flop
- (d) Schmitt trigger

#Q. The output Q_n of a J-K flip-flop is zero. It changes to 1 when a clock pulse is applied. The input J_n and K_n are respectively (\times represents don't care condition)

- (a) 1 and \times
- (b) 0 and \times
- (c) \times and 0
- (d) \times and 1

#Q.

Consider the circuit shown in the figure. The expression for the next state $Q(t+1)$ is



- (a) $x \cdot Q(t)$
- (b) $x \oplus Q(t)$
- (c) $x \bar{Q}(t)$
- (d) $x \odot Q(t)$

#Q. The right side of a state equation represents

- (a) Next state of flip-flop
- (b) Present state of flip-flop
- (c) Present state condition that makes the next state equal to 1
- (d) None of the above

#Q. The outputs Q and \bar{Q} of master slave S-R flip-flops are connected to its R and S inputs respectively. The output Q when clock pulses are applied will be

- (a) Permanently 0
- (b) Permanently 1
- (c) Fixed 0 or 1
- (d) Complementing with every clock pulse

#Q. For an SR flip-flop, S and R are made equal to 1. What is the value of Q?

- (a) Unchanged
- (b) Clear to 0
- (c) Set to 1
- (d) Indeterminate

#Q. D input of a clocked D-flip flop receives an input $A \oplus Q_n$ where A is an external logic input and Q_n is the output of the n^{th} D-FF before the clock appeals. The circuit works as

- (a) Ex OR gate
- (b) T-FF
- (c) D-FF
- (d) JK-FF

#Q. Which one of the following statements best describes the operation of a negative-edge-triggered D flip-flop?

- (a) The logic level at the D input is transferred to Q on NGT of CLK
- (b) The Q output is always identical to the CLK input if the D input is high
- (c) The Q output is always identical to the D input when CLK = PGT
- (d) The Q output is always identical to the D input.

#Q. A flip-flop is a

- (a) Combinational logic circuit and edge sensitive
- (b) Sequential logic circuit and edge sensitive
- (c) Combinational logic circuit and level sensitive
- (d) Sequential logic circuit and level sensitive

#Q. If the input to a T flip-flop is a 100 MHz signal, the final output of three T flip-flops in a cascade is

- (a) 1000 MHz
- (b) 520 MHz
- (c) 333 MHz
- (d) 12.5MHz

#Q. In a master-slave JK flip-flop

- (a) both master and slave are positive-edge-triggered
- (b) both master and slave are negative-edge-triggered
- (c) master is positive-edge-triggered and slave is negative-edge-triggered
- (d) master is negative-edge-triggered and slave is positive-edge-triggered

#Q. Master Slave flip-flop is also called

- (a) Pulse triggered flip-flop
- (b) Latch
- (c) Level triggered flip-flop
- (d) Buffer

#Q. The data sheet of a certain flip-flop specifies that the minimum HIGH time $t_w(H)$ for the clock pulse is 16 nano-seconds and the minimum LOW time $t_w(L)$ is 29 nanoseconds. What is the maximum operating frequency for the given flip-flop?

- (a) 62.50 MHz
- (b) 31.25 MHz
- (c) 22.22 MHz
- (d) 11.11 MHz

Thank you
GW
Soldiers!



Electronics and Communication Engineering

Computer Science



Digital Electronics

Digital Logic

Lecture- 06

By- CHANDAN JHA SIR



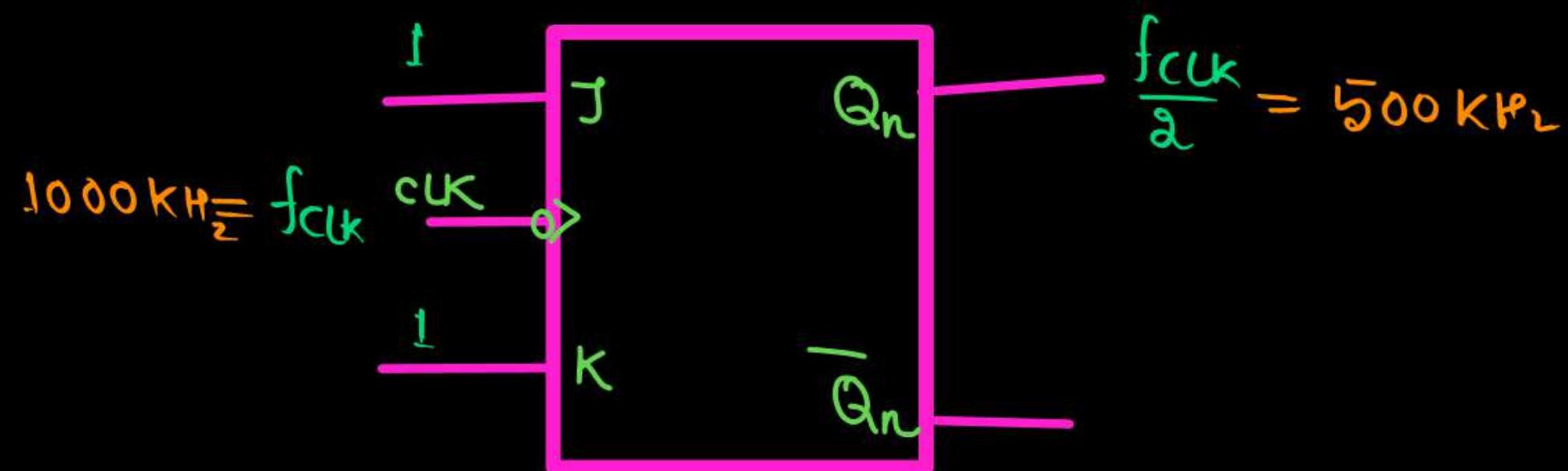


Topics to be Covered

1. Sequential Circuit

#Q. A 1 MHz clock signal is applied to a J-K flip-flop with $J = K = 1$. What is the frequency of the flip-flop output signal ?

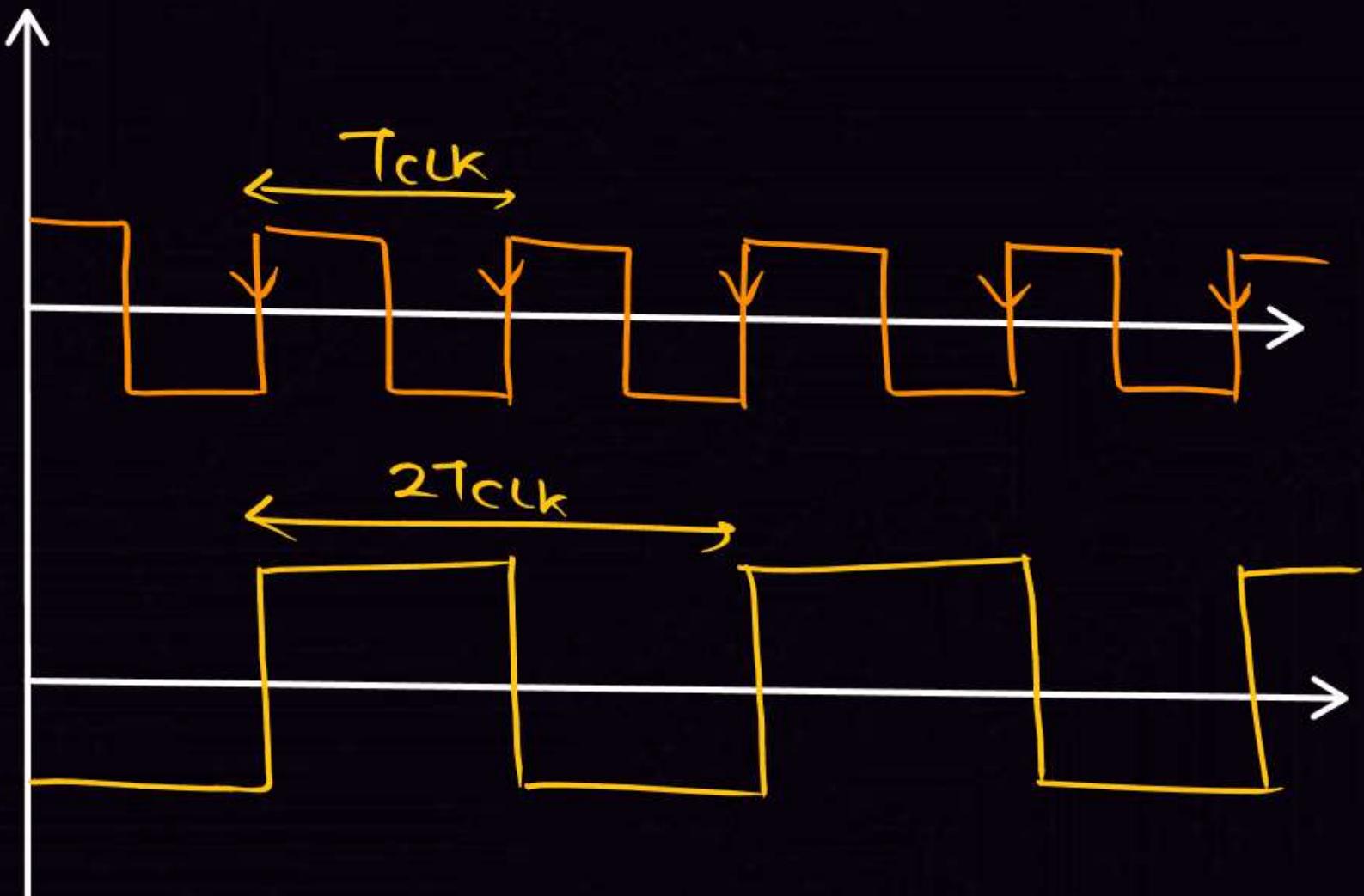
- (a) 2 MHz
- (b) 500 kHz**
- (c) 260 kHz
- (d) 500 MHz



$$f_{\text{clk}} = \frac{1}{T_{\text{clk}}}$$

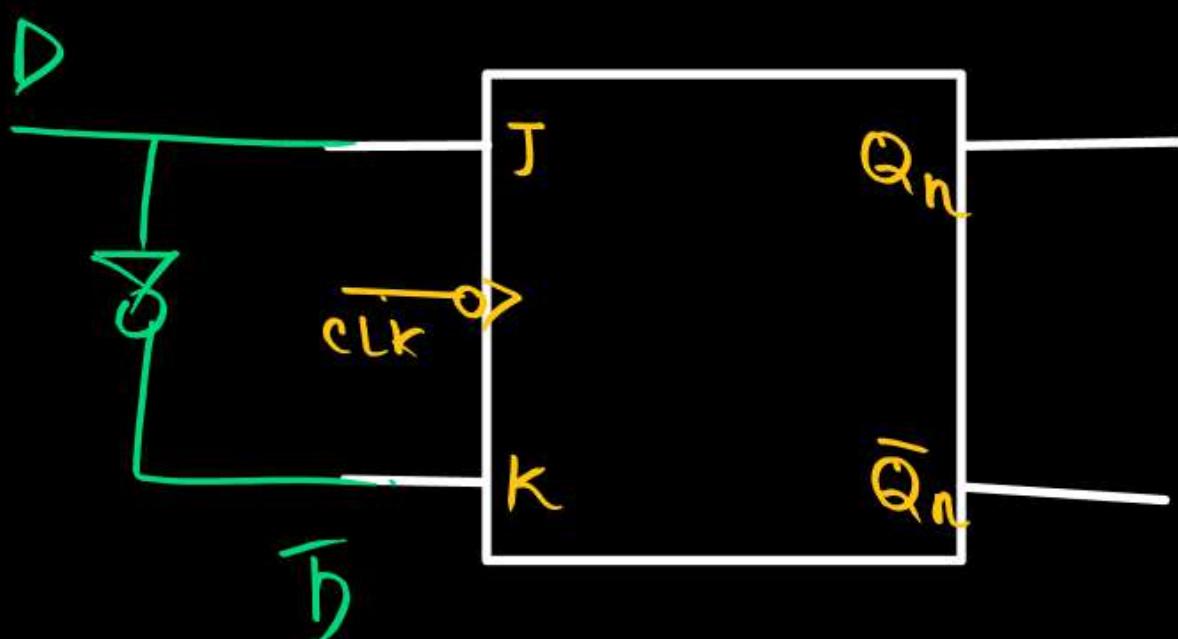
$$f_Q = \frac{1}{2T_{\text{clk}}} \quad Q$$

$$= \frac{f_{\text{clk}}}{2}$$



#Q. D flip-flop can be made from a J-K flip-flop by making

- (a) $J = K$
- (b) $J = K = 1$
- (c) $J = 0, K = 1$
- (d) $J = K$



$$Q_{n+1} = D$$

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$\begin{aligned} Q_{n+1} &= \bar{J}\bar{Q}_n + \bar{D}Q_n \\ &= \bar{D}(\bar{Q}_n + Q_n) \end{aligned}$$

$Q_{n+1} = \bar{D}$

✓

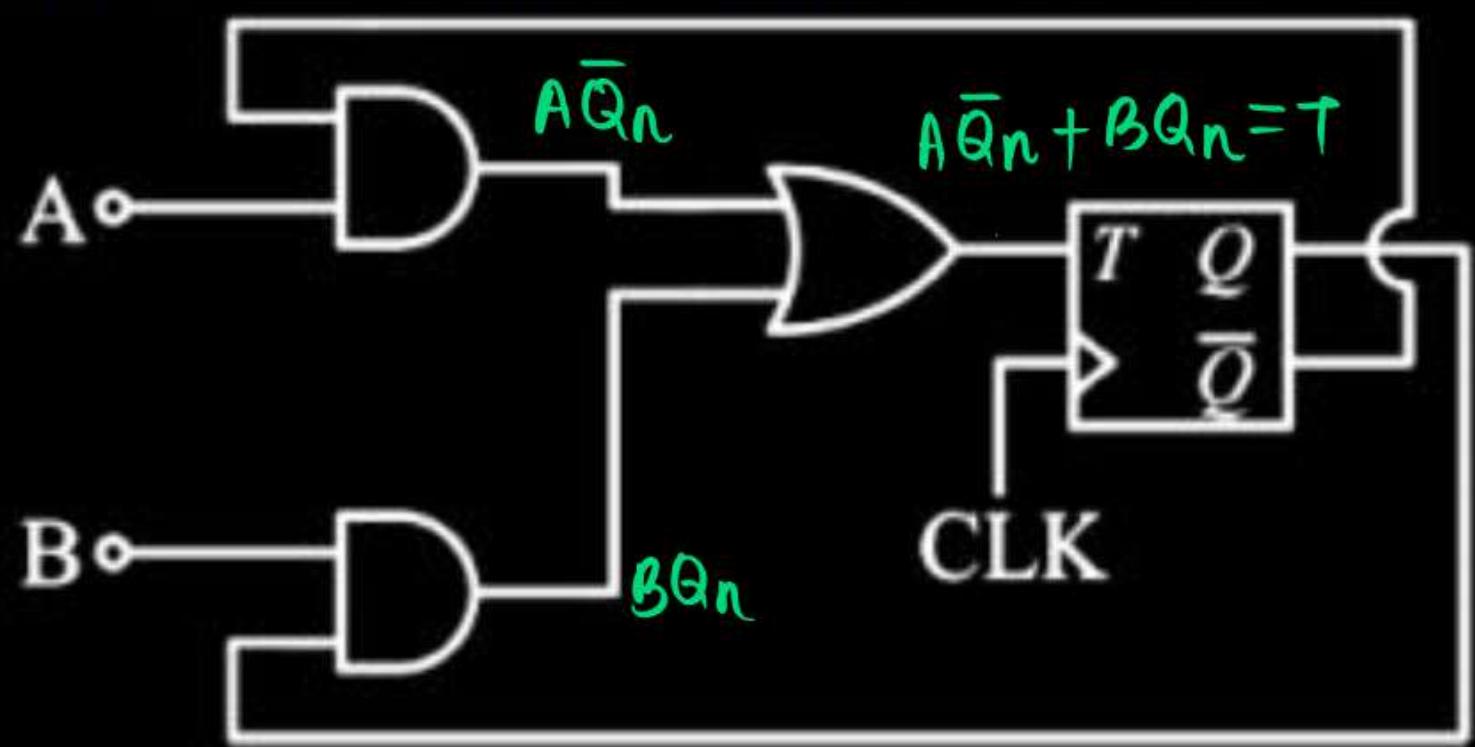
#Q. For a JK flip-flop, Q_n is output at time step t_n .

Which of the following Boolean expressions represents Q_{n+1} ?

- (a) $J_n \bar{Q}_n + \bar{K}_n Q_n$
- (b) $J_n Q_n + K_n \bar{Q}_n$
- (c) $\bar{J}_n Q_n + K_n \bar{Q}_n$
- (d) $J_n Q_n + \bar{K}_n \bar{Q}_n$

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

#Q. What is represented by the digital circuit given below?



- (a) An SR flip-flop with $A = S$ and $B = R$
- (b) A JK flip-flop with $A = K$ and $B = J$
- (c) A JK flip-flop with $A = J$ and $B = K$
- (d) An SR flip-flop with $A = R$ and $B = S$

$$Q_{n+1} = J \bar{Q}_n + K Q_n$$

$$Q_{n+1} = T \oplus Q_n$$

$$Q_{n+1} = (A \bar{Q}_n + B Q_n) \oplus Q_n$$

$$Q_{n+1} = (A\bar{Q}_n + BQ_n) \oplus Q_n$$

$$= \overline{A\bar{Q}_n + BQ_n} \cdot Q_n + (A\bar{Q}_n + BQ_n) \cdot \bar{Q}_n \quad Q_{n+1} = J\bar{Q}_n + KQ_n$$

$$= \overline{A\bar{Q}_n} \cdot \overline{BQ_n} \cdot Q_n + A\bar{Q}_n$$

$$= (\bar{A} + Q_n)(\bar{B} + \bar{Q}_n) \cdot Q_n + A\bar{Q}_n$$

$$= (\bar{A}\bar{B} + \bar{A}\bar{Q}_n + \bar{B}Q_n)Q_n + A\bar{Q}_n$$

$$= \bar{A}\bar{B}Q_n + \bar{B}Q_n + A\bar{Q}_n$$

$$= \bar{B}Q_n(\bar{A} + 1) + A\bar{Q}_n$$

$$= \bar{B}Q_n + A\bar{Q}_n$$

$$Q_{n+1} = A\bar{Q}_n + \bar{B}Q_n$$

$$J = A$$

$$K = B$$

#Q. Match List-I (Logic circuit / function) with List-II (Circuit realization) and select the correct answer using the code given below the lists :

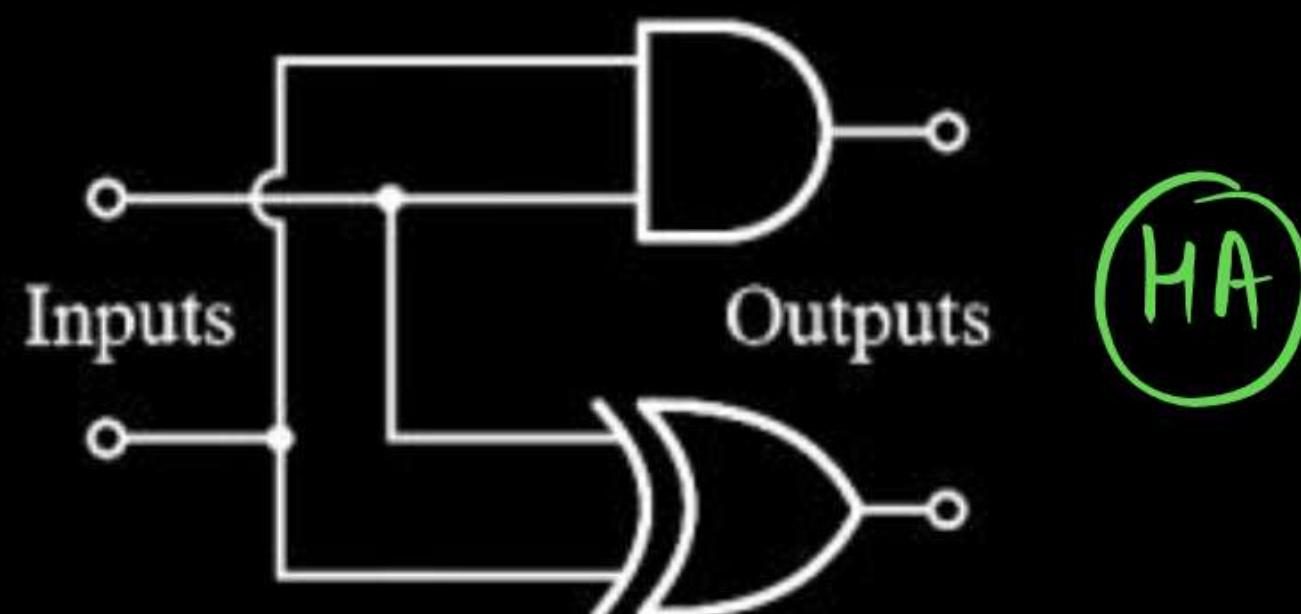
List-I

A. D flip-flop

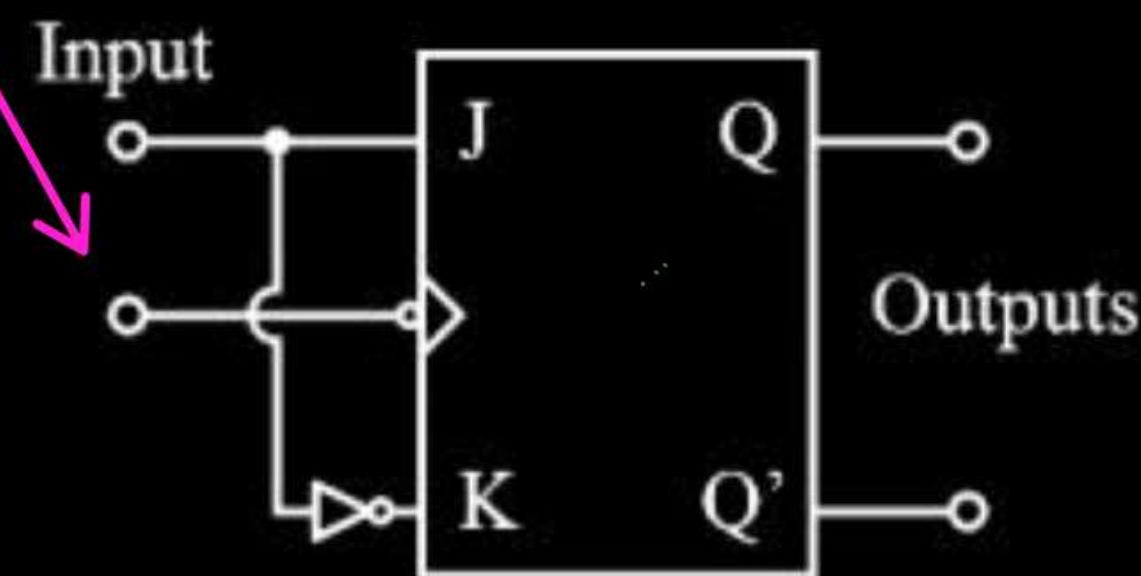
B. T flip-flop

List-II

1.

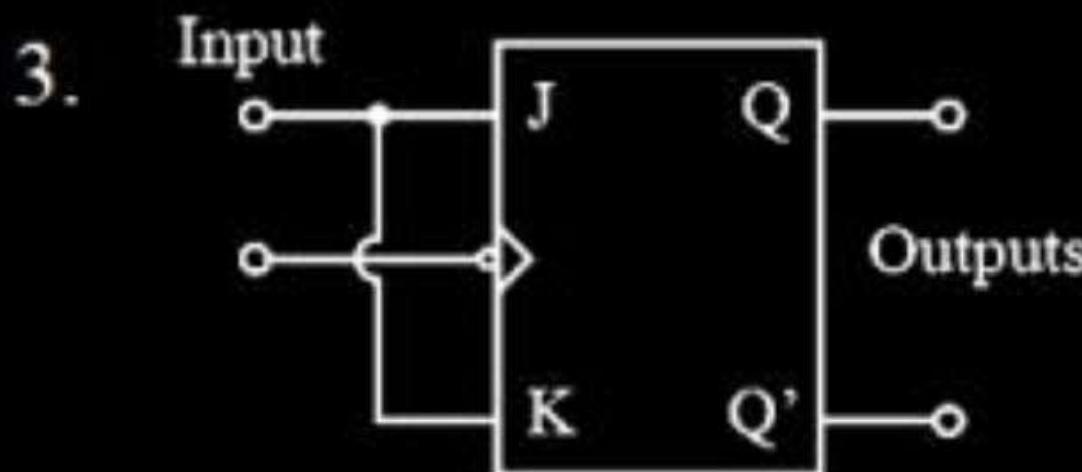


2.



C. Exclusive OR

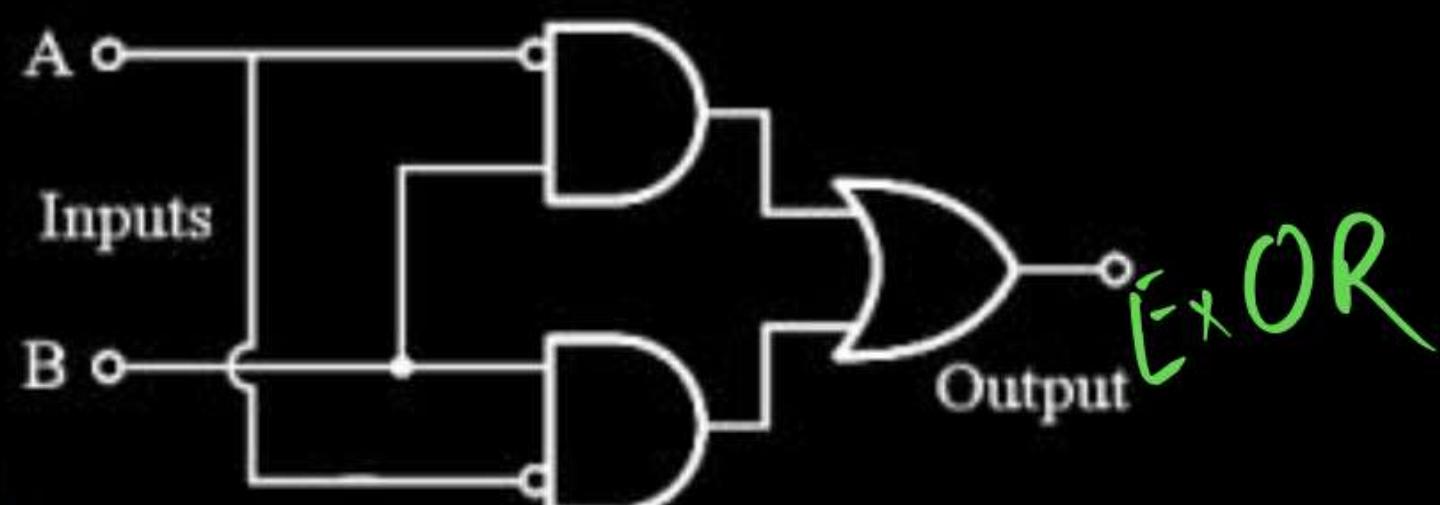
3.



T-FF

D. Half-adder

4.

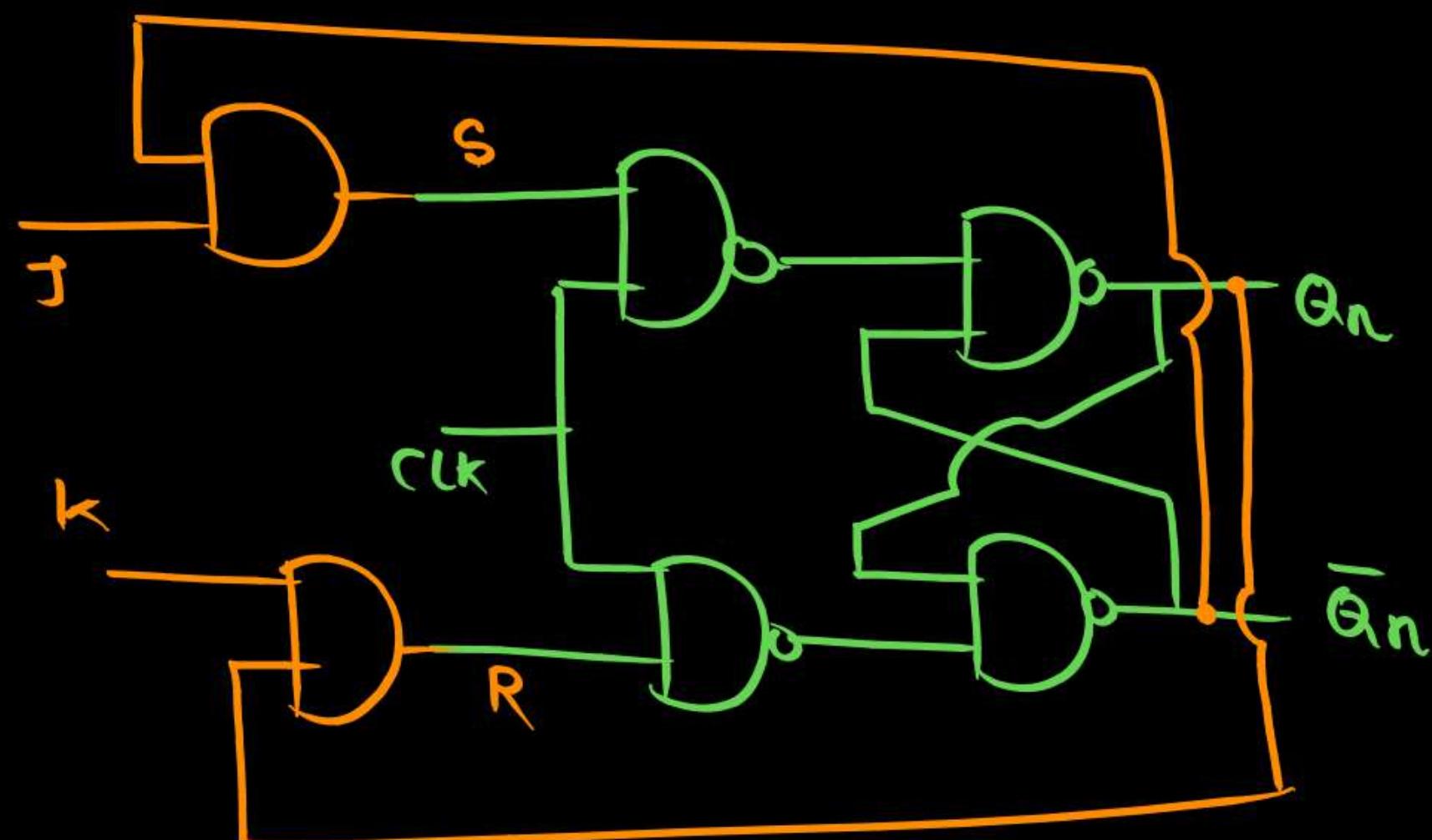


Codes: A B C D

- (a) 3 2 4 1 }
- (b)** 2 3 4 1
- (c) 1 3 4 2
- (d) 2 4 3 1

#Q. A J-K flip-flop can be made from an S-R flip-flop by using two additional

- (a) AND gates
- (b) OR gates
- (c) NOT gates
- (d) NOR gates

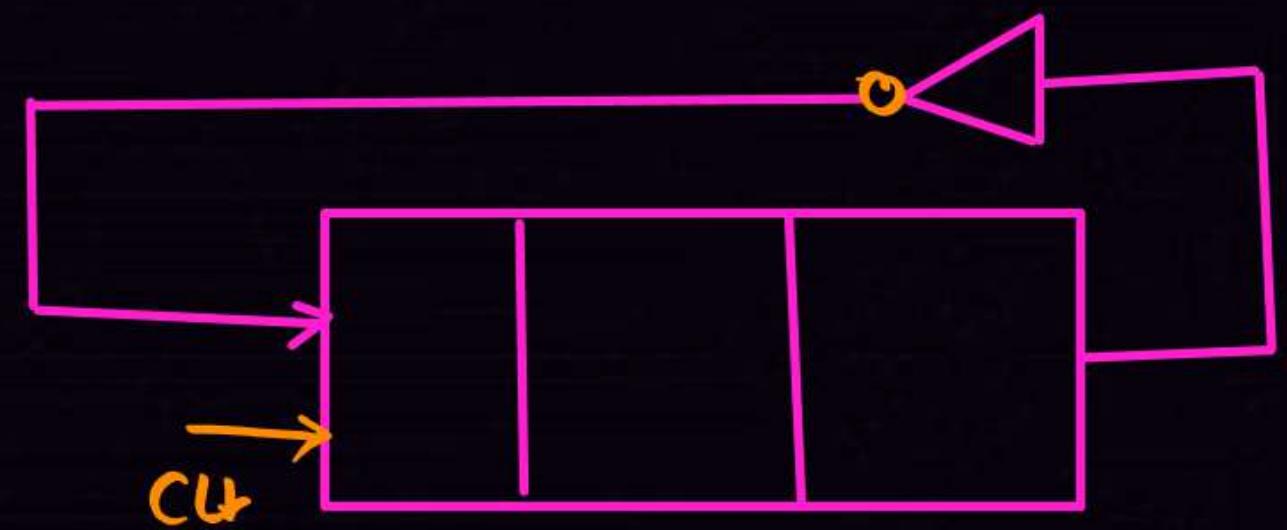


#Q. Consider the following statements in Johnson counter:

1. A MOD-6 Johnson counter requires 3 FFs. ✓
 2. Johnson counter requires decoding gates. ✓
 3. To decode each count, one logic gate is used. Each gate requires only two inputs regardless of the number of FFs.

Which of these statements are correct?

Johnson counter



000
100
110
111
011
001 }
6 Mod

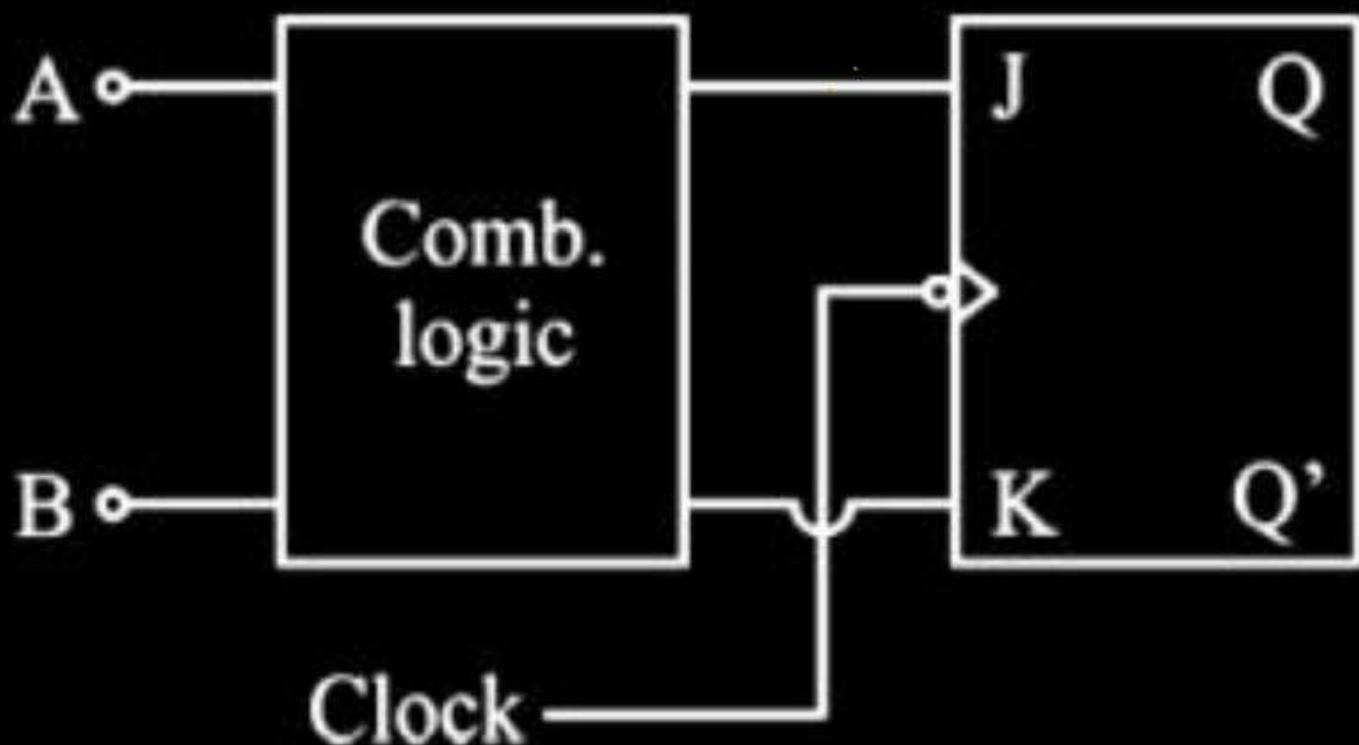
N-FF

MOD (Used state) = $2N$

Unused state = $2^N - 2N$

#Q. The following truth table has to be realized with the circuit shown in the figure:

A	B	Q_{n+1}
0	0	Q'_n
0	1	1
1	0	Q_n
1	1	0



What is the output of the combinational logic circuit to the J input?

- (a) \overline{AB}
- (b) \overline{A}
- (c) \overline{B}
- (d) AB

A	B	Q_n	Q_{n+1}	J	K
0	0	0	1	1	X
0	0	1	0	X	J
0	1	0	1	1	X
0	1	1	1	X	0
1	0	0	0	0	X
1	0	1	1	X	0
1	1	0	0	0	X
1	1	1	0	X	1

~~P W~~

P	Q _n	00	01	11	10
0	1	X	X	X	0
1		X	X		

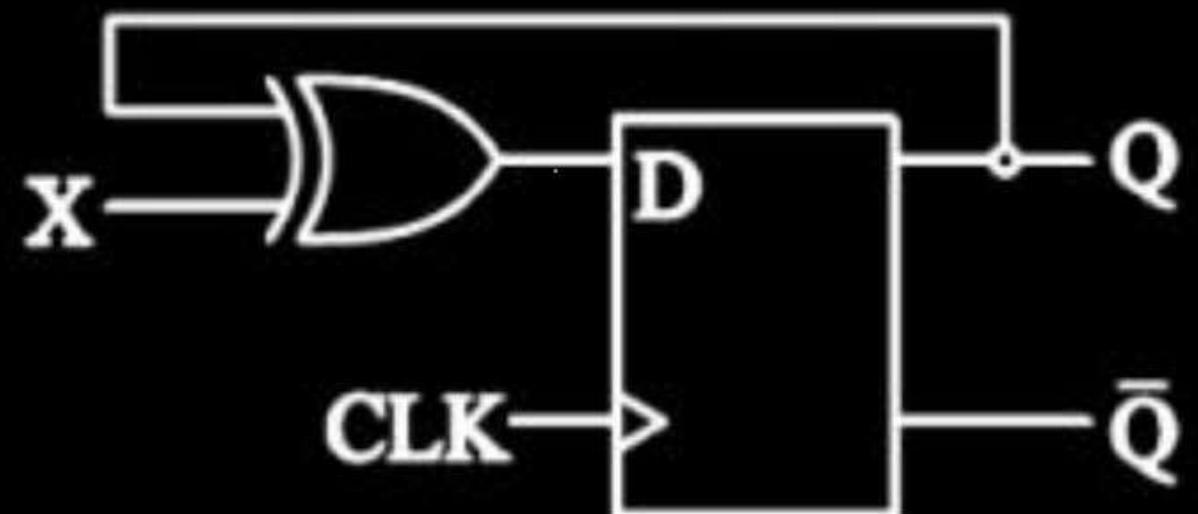
$J = \bar{A}$

~~P W~~

P	Q _n	00	01	11	10
0		X	1		X
1		X	1		X

$$K = \bar{A}\bar{B} + A\bar{B}$$

#Q. The digital circuit as shown below represents to which one of the following?



$$\bar{D} = X \oplus Q_n$$

- (a) JK flip-flop
- (b) Clocked RS flip-flop
- (c) T flip-flop
- (d) Ring counter

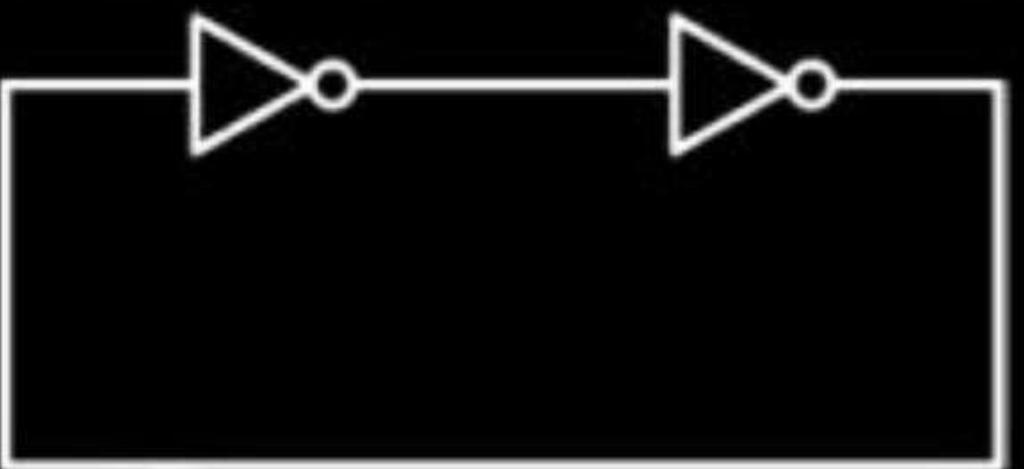
$$Q_{n+1} = \bar{D}$$

$$Q_{n+1} = X \oplus Q_n$$

$$X = 1$$

$$1 \oplus Q_n$$

#Q. The digital circuit using two inverters as shown in the figure below acts as



- (a) A bistable multivibrator
- (b) A astable multivibrator
- (c) A monostable multivibrator
- (d) An oscillator

#Q. Race-around condition occurs in

- (a) Multiplexer
- (b) ROM
- (c) Flip-flops
- (d) Voltage regulator

#Q. Consider the following circuits:

- 1. Full adder
- 2. Half adder
- 3. JK flip-flop
- 4. Counter

Which of the above circuits are classified as sequential logic circuits?

- (a) 1 and 2
- (b) 3 and 4
- (c) 2 and 3
- (d) 1 and 4

Q Design a synchronous counter by using T-FF which
count →

000 → 001 → 010 → 011 → 100 → 101 → 110 → 111 → 000

Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

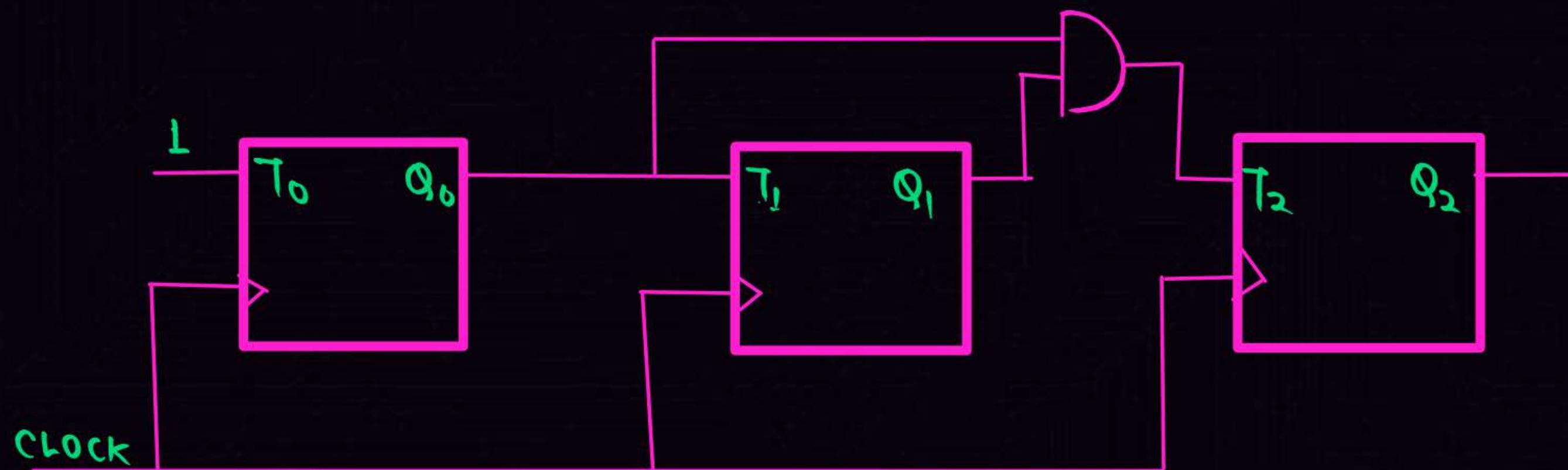
 $T_2 \Rightarrow$

Q_2	$Q_1^+ Q_0^+$	00	01	11	10
0				1	
1				1	

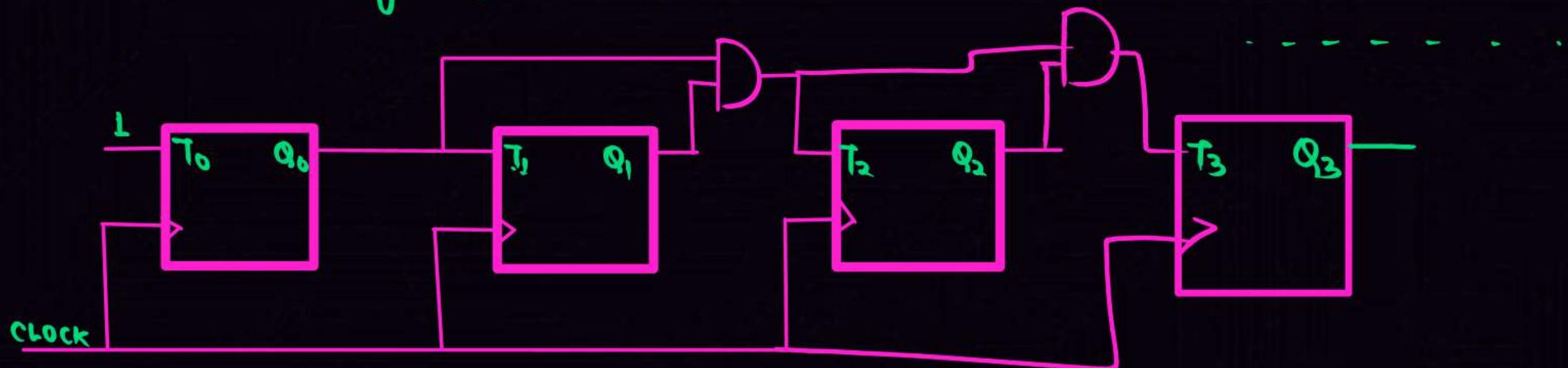
 $T_0 = 1$ $T_1 = Q_0$ $T_2 = Q_1 Q_0$

Q_2	$Q_1^+ Q_0^+$	00	01	11	10
0		1	1	1	
1		1	1	1	

 $T_1 = Q_0$



Series carry synchronous counter :-

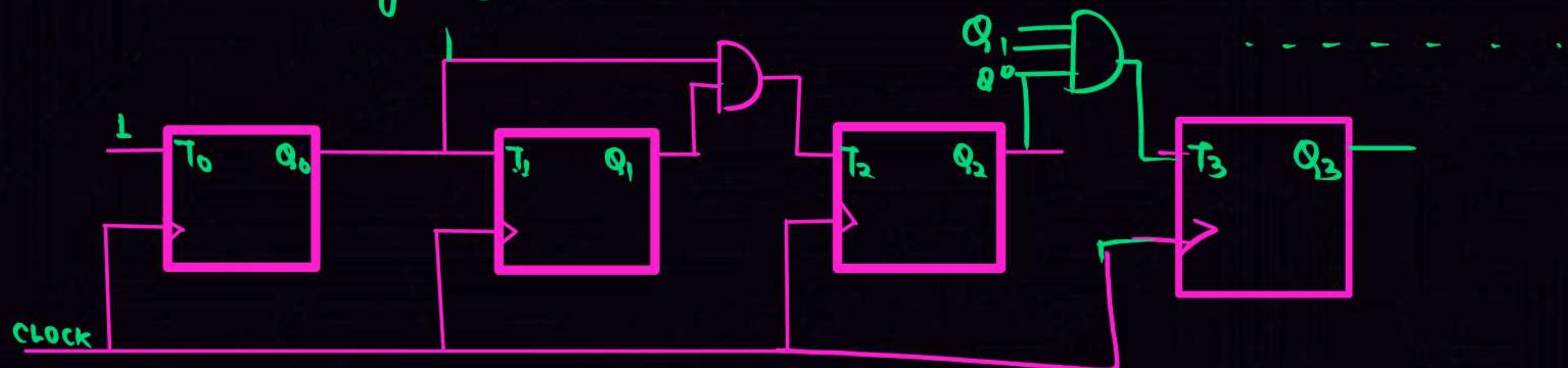


$$T_{CK} \geq \tau_{Pdff} + (n-2)\tau_{PdAND}$$

$$f_{CK} \leq \frac{1}{\tau_{Pdff} + (n-2)\tau_{PdAND}}$$

$$f_{max} = \frac{1}{\tau_{Pdff} + (n-2)\tau_{PdAND}}$$

Parallel carry synchronous counter :-

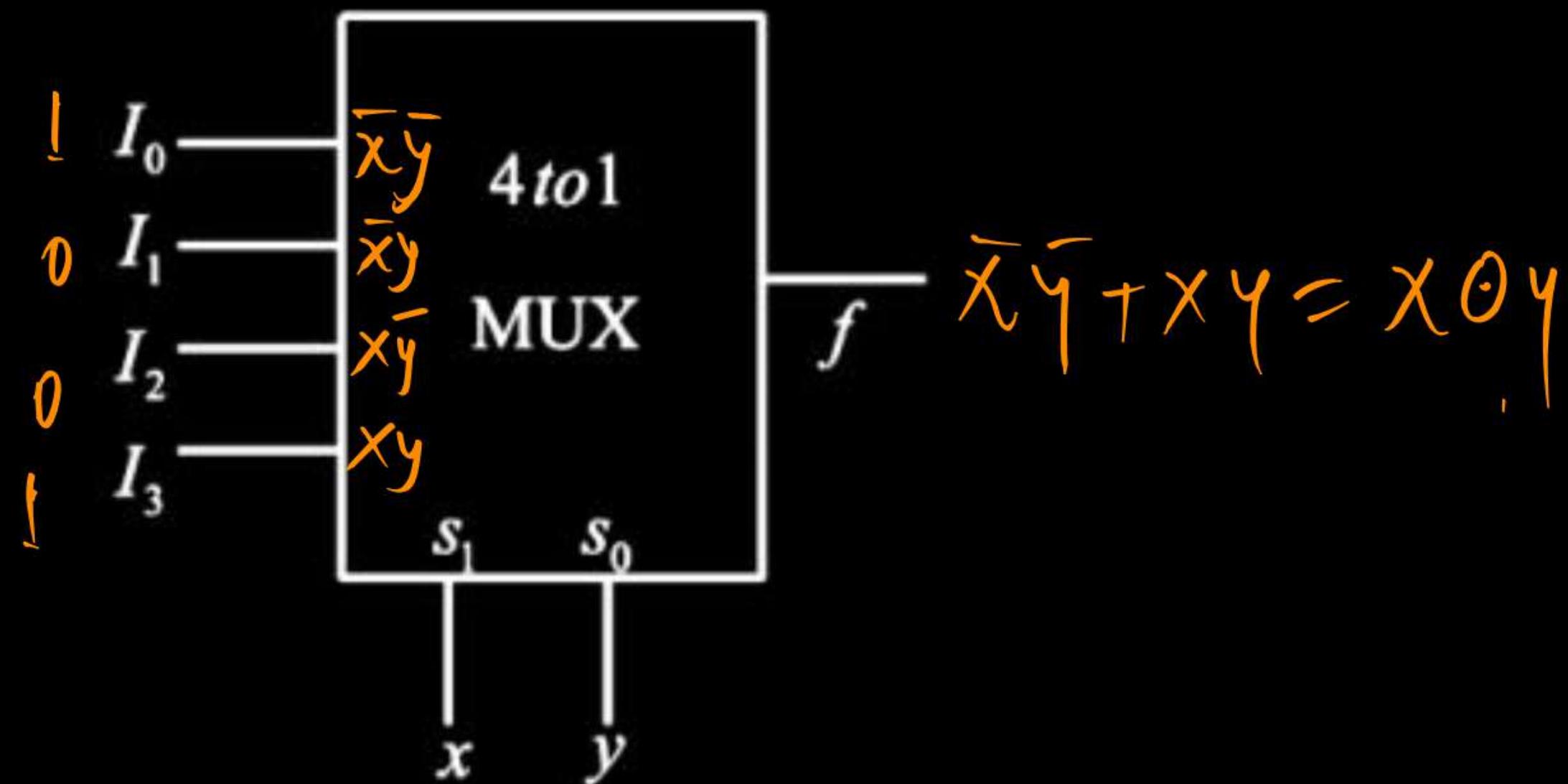


$$T_{CLK} \geq \tau_{Pdff} + \tau_{PdAND}$$

$$f_{CLK} \leq \frac{1}{\tau_{Pdff} + \tau_{PdAND}}$$

$$(f_{CLK})_{max} = \frac{1}{\tau_{Pdff} + \tau_{PdAND}}$$

#Q. Which logic inputs should be given to the input lines I_0, I_1, I_2 and I_3 if the MUX is to behave two input XNOR gate?

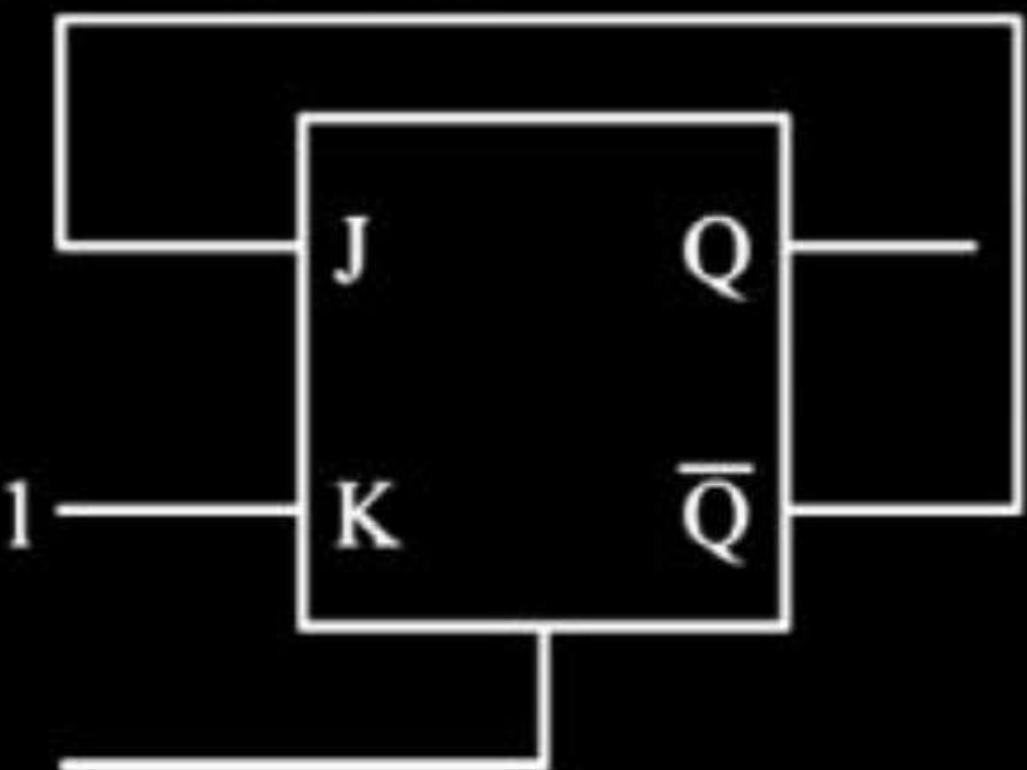


- (a) 01110
~~(b) 1001~~
(c) 1010
(d) 1111

#Q. The time delay in a look-ahead carry adder is independent of

- (a) Number of operands only
- (b) Propagation delay only
- ~~(c)~~ Number of bits in the operand only
- (d) Bits in the operand, number of operands and propagation delay

#Q. Consider the following J-K flip-flop.



Toggle Mode of the
FF

In the above J-K flip-flop, $J = \bar{Q}$ and $K = 1$. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

- (a) 01000
- (b) 011001
- (c) 010010
- (d) 010101

#Q. Match List-I (Type of flip-flop) with List-II (Symbol) and select the correct answer using the codes given below the lists:

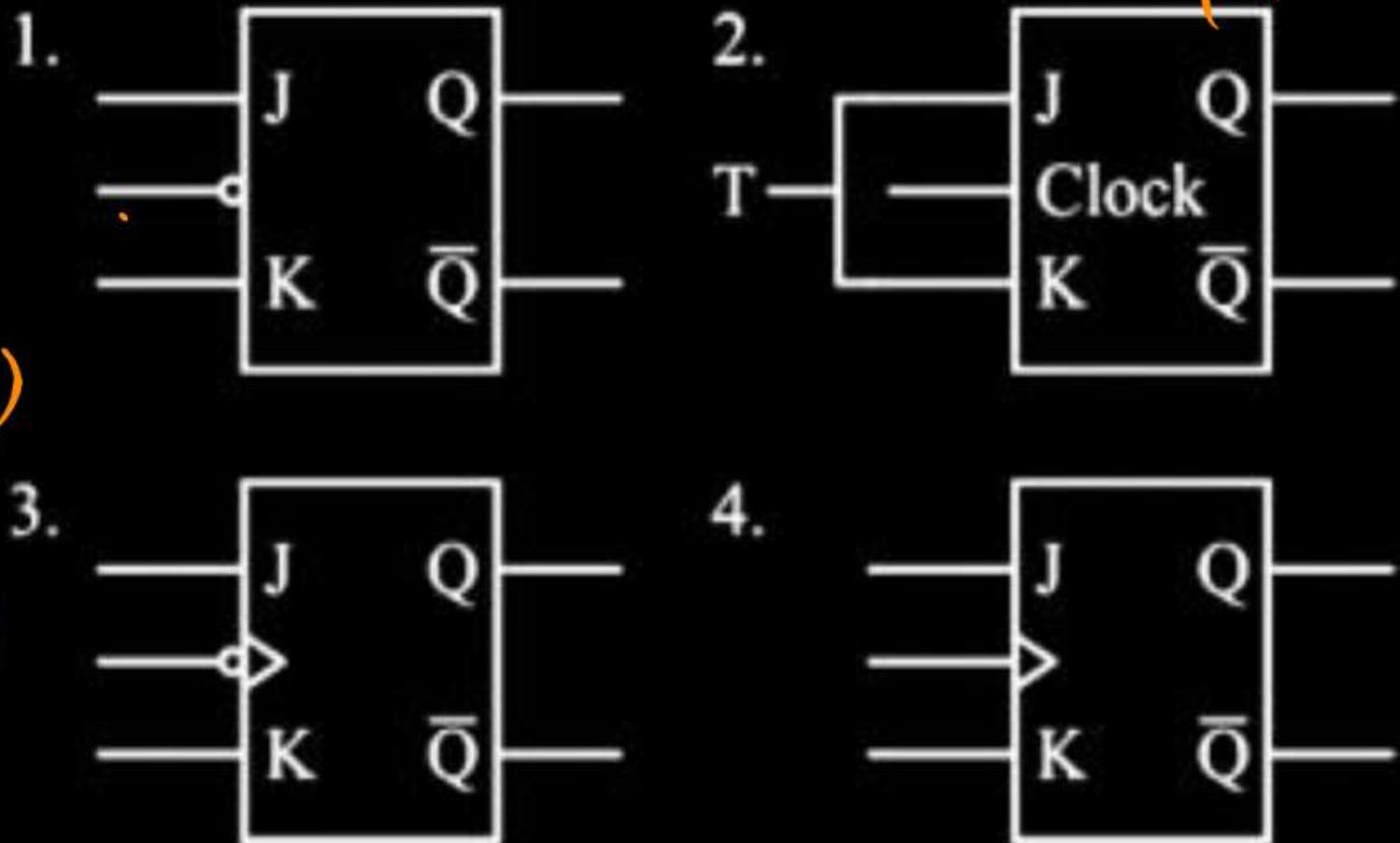
List-I

- A. T flip-flop
- B. Level-triggered JK flip-flop
- C. Leading edge-triggered JK flip-flop (4)
- D. Trailing edge-triggered JK flip-flop (3)

Codes: A B C D

- (a) 1 2 3 4
- (b) 2 1 3 4
- (c) 1 2 4 3
- (d) 2 1 4 3

List-II



Level triggered
T-flip-flop

#Q. Which one of the following equations satisfies the JK flip-flop truth table?

- (a) $Q_{n+1} = J_n \bar{Q}_n + \bar{K}_n Q_n$
- (b) $Q_{n+1} = \bar{J}_n \bar{Q}_n + \bar{K}_n Q_n$
- (c) $Q_{n+1} = J_n Q_n + K_n Q_n$
- (d) $Q_{n+1} = \bar{J}_n \bar{Q}_n + \bar{K}_n \bar{Q}_n$

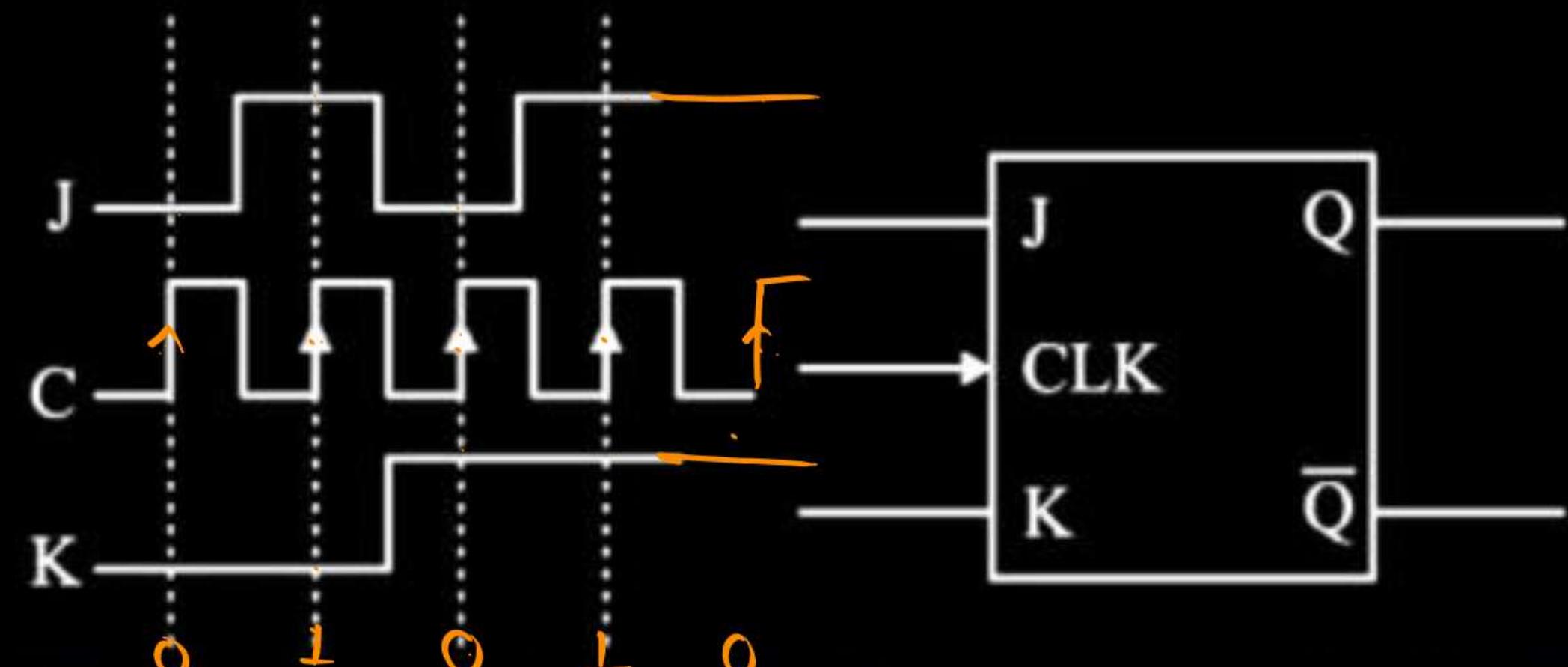
$$SR \rightarrow S + \bar{R}Q_n$$

$$JR \rightarrow J\bar{Q}_n + \bar{R}Q_n$$

$$R \rightarrow Q_{n+1} = \bar{R}$$

$$T \rightarrow T \oplus Q_n$$

#Q.



The J-K flip-flop shown above is initially reset so that $Q = 0$. If a sequence of four clock pulses is then applied, with the J and K inputs as given in the figure, the resulting sequence of values that appear at the output Q starting with its initial state, is given by:

- (a) 01011
- (b) 01010
- (c) 00110
- (d) 00101

#Q.

X	Y	Q _{n+1}
0	0	1
0	1	Q _n
1	0	\bar{Q}_n
1	1	0

An X-Y flip flop, whose characteristic table is given above is to be implemented using JK flip flop. This can be done by making

- (a) J = X, K = \bar{Y}
- (b) J = \bar{X} , K = Y
- (c) J = Y, K = \bar{X}
- (d) J = \bar{Y} , K = X

X	Y	Q_n	Q_{n+1}	J	K
0	0	0	1	1	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	1	X	0
1	0	0	1	1	X
1	0	1	0	X	1
1	1	0	0	0	X
1	1	1	0	X	1

+ Y8m

	00	01	11	10
0	-	X	X	
1	1	X	X	

$$J = \bar{Y}$$

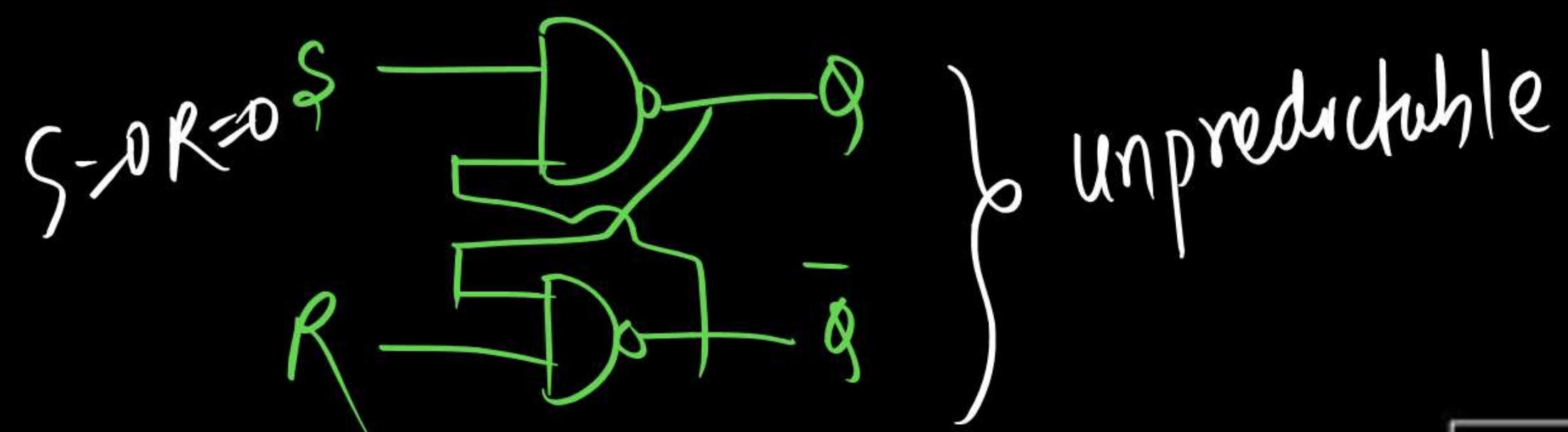
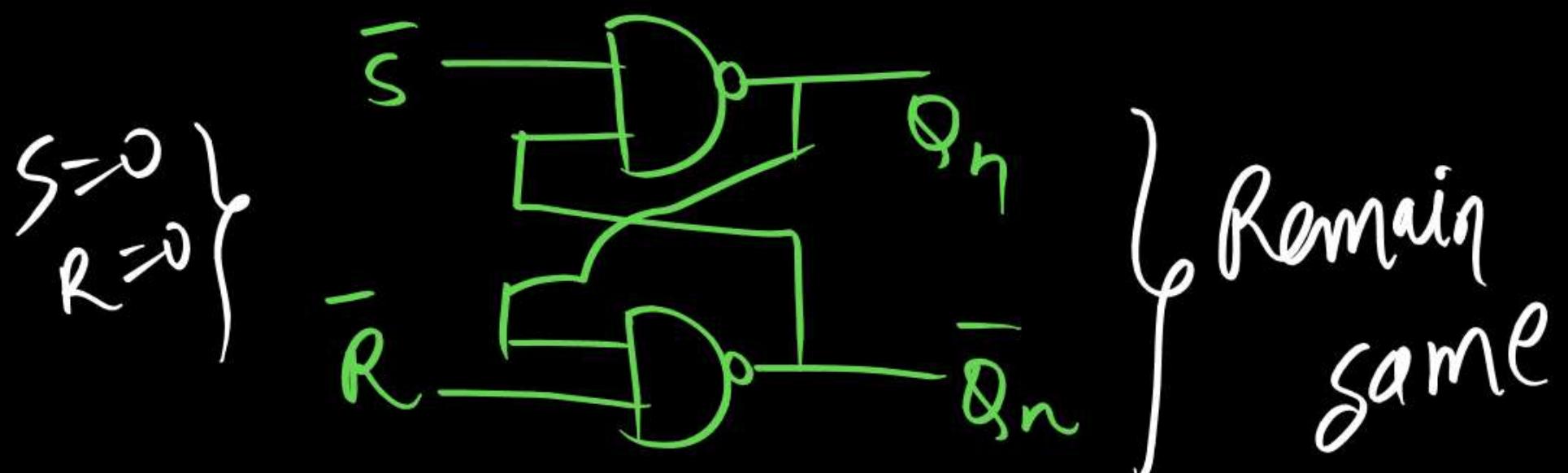
+ Y8o

	00	01	11	10
0	X	.	.	X
1	X	1	1	X

$$K = X$$

#Q. If both inputs of S-R NAND latch are low, the output will be

- (a) Unpredictable
- (b) Toggle
- (c) Reset
- (d) Remain same



#Q. A bistable multi-vibrator that functions as a voltage comparator with hysteresis is called

- (a) T flip-flop
- (b) D flip-flop
- (c) J-K flip-flop
- (d) Schmitt trigger

#Q. The output Q_n of a J-K flip-flop is zero. It changes to 1 when a clock pulse is applied. The input J_n and K_n are respectively (\times represents don't care condition)

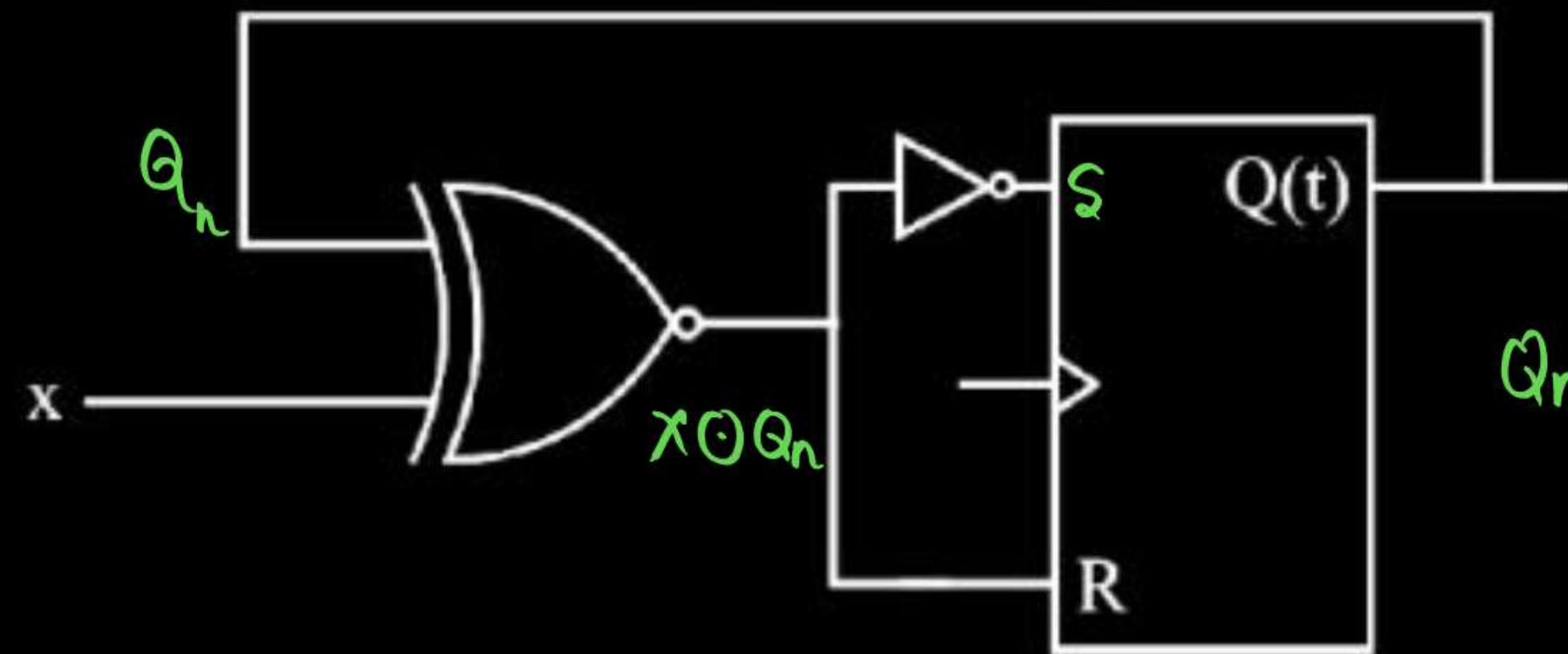
- (a) 1 and \times
(b) 0 and \times
(c) \times and 0
(d) \times and 1

Q_n	Q_{n+1}	J	K
0	0	0	\times
0	1	1	\times
1	0	\times	1
1	1	\times	0

$J=1$ $K=\times$

#Q.

Consider the circuit shown in the figure. The expression for the next state $Q(t+1)$ is



- (a) $x \oplus Q(t)$
- ~~(b)~~ $x \oplus Q(t)$
- (c) $x \bar{Q}(t)$
- (d) $x \odot Q(t)$

$$\begin{aligned}
 Q_{n+1} &= S + \bar{R} Q_n \\
 &= (x \oplus Q_n) + (x \oplus Q_n) \bar{Q}_n \\
 &= x \oplus Q_n [1 + \bar{Q}_n] \\
 &= x \oplus Q_n
 \end{aligned}$$

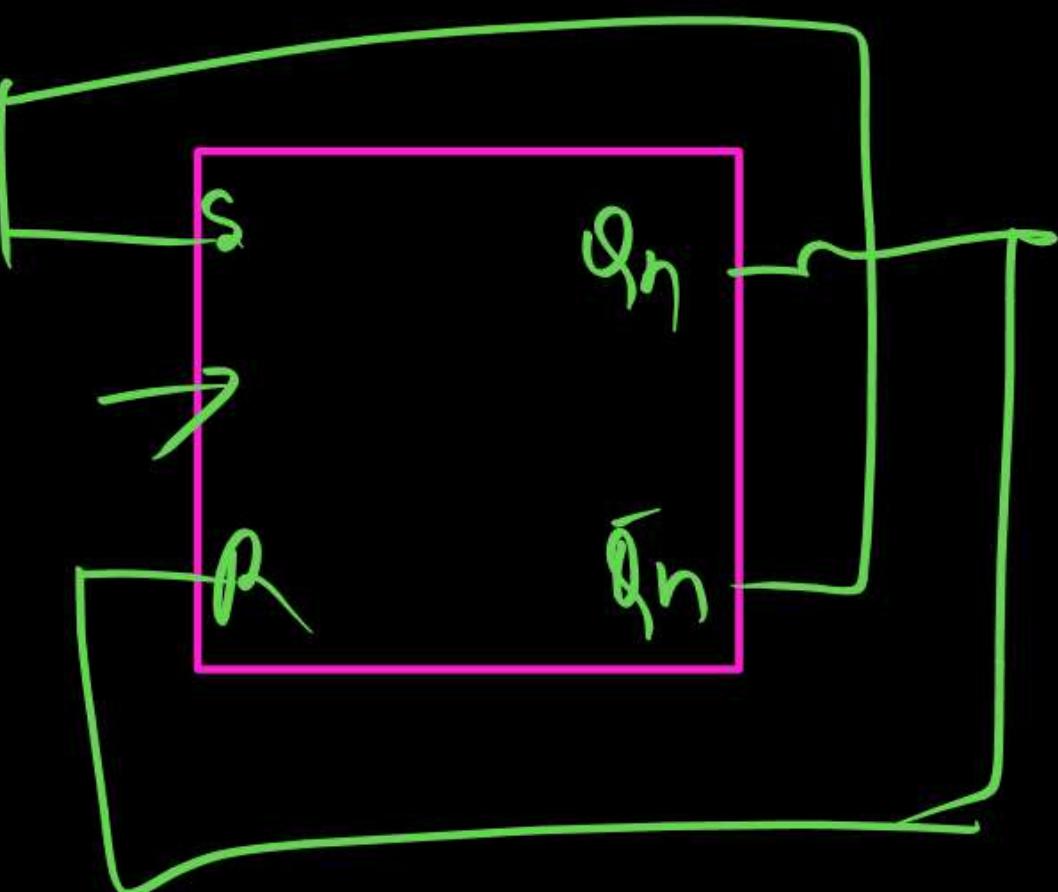
#Q. The right side of a state equation represents

- (a) ✓ Next state of flip-flop
- (b) Present state of flip-flop
- (c) Present state condition that makes the next state equal to 1
- (d) None of the above

$$Q_{n+1} = \underline{\underline{}}$$

#Q. The outputs Q and \bar{Q} of master slave S-R flip-flops are connected to its R and S inputs respectively. The output Q when clock pulses are applied will be

- (a) Permanently 0
- (b) Permanently 1
- (c) Fixed 0 or 1
- (d) Complementing with every clock pulse

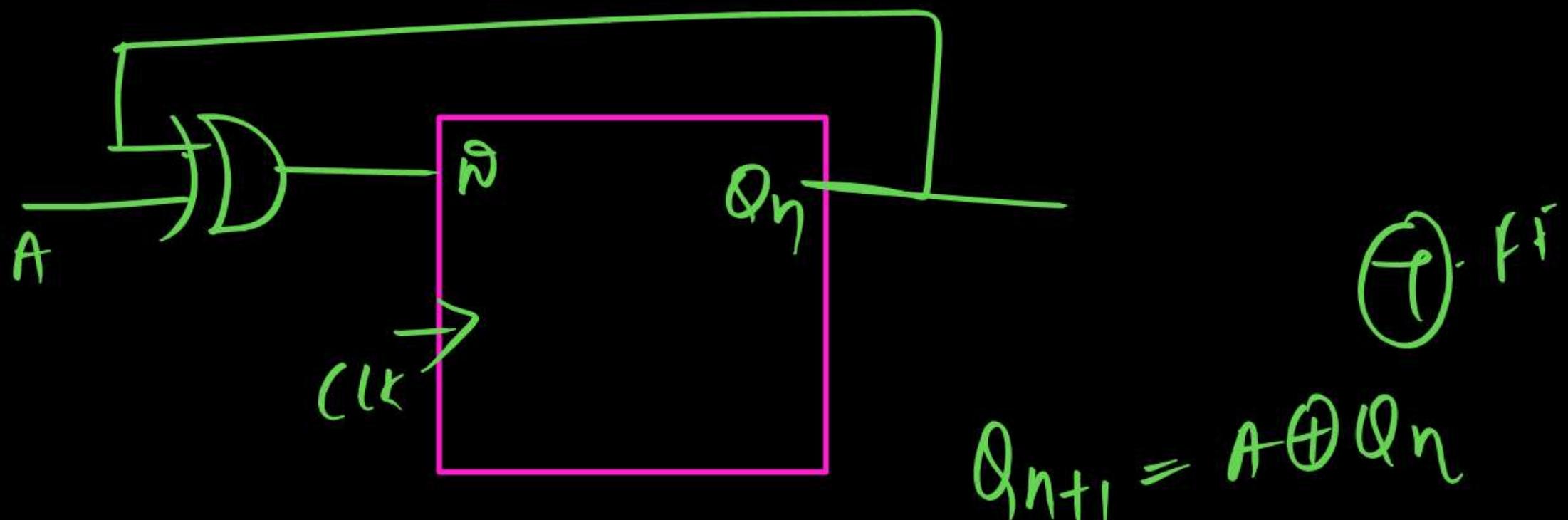


#Q. For an SR flip-flop, S and R are made equal to 1. What is the value of Q?

- (a) Unchanged
- (b) Clear to 0
- (c) Set to 1
- (d) Indeterminate

#Q. D input of a clocked D-flip flop receives an input $A \oplus Q_n$ where A is an external logic input and Q_n is the output of the n^{th} D-FF before the clock appeals. The circuit works as

- (a) Ex OR gate
- (b) T-FF**
- (c) D-FF
- (d) JK-FF



#Q. Which one of the following statements best describes the operation of a negative-edge-triggered D flip-flop?

- (a) The logic level at the D input is transferred to Q on NGT of CLK
- (b) The Q output is always identical to the CLK input if the D input is high
- (c) The Q output is always identical to the D input when CLK = PGT
- (d) The Q output is always identical to the D input.

#Q. A flip-flop is a

- (a) Combinational logic circuit and edge sensitive
- (b) Sequential logic circuit and edge sensitive
- (c) Combinational logic circuit and level sensitive
- (d) Sequential logic circuit and level sensitive

#Q. If the input to a T flip-flop is a 100 MHz signal, the final output of three T flip-flops in a cascade is

- (a) 1000 MHz
- (b) 520 MHz
- (c) 333 MHz
- (d) 12.5 MHz

$$\begin{aligned}f_{\text{out}} &= \frac{f_{\text{in}}}{\text{MOD}} \\&= \frac{100 \times 10^6}{2^3} \\&= \underline{12.5 \text{ MHz}}\end{aligned}$$

#Q. In a master-slave JK flip-flop

- (a) both master and slave are positive-edge-triggered ✗
- (b) both master and slave are negative-edge-triggered ✗
- (c) master is positive-edge-triggered and slave is negative-edge-triggered
- (d) master is negative-edge-triggered and slave is positive-edge-triggered ✗

#Q. Master Slave flip-flop is also called

- (a) Pulse triggered flip-flop
- (b) Latch
- (c) Level triggered flip-flop
- (d) Buffer

Thank you
GW
Soldiers!



Electronics and Communication Engineering

COMPUTER SCIENCE



Digital Electronics

LECTURE- 07

DIGITAL LOGIC

By- CHANDAN JHA SIR





1. Number Systems

↳ Base conversion

↳ Magnitude Representation

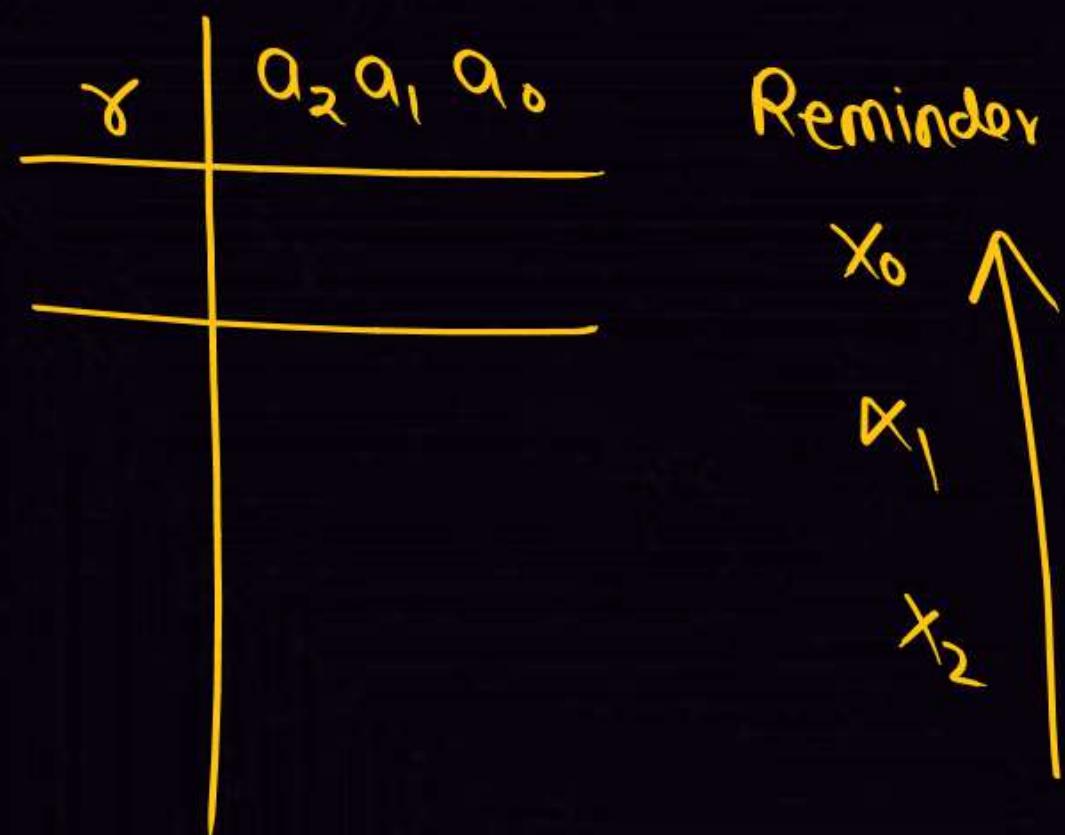
↳ Any Base to Decimal conversion

$$(a_3 r^3 + a_2 r^2 + a_1 r^1 + a_0 r^0 + a_{-1} r^{-1} + a_{-2} r^{-2} + a_{-3} r^{-3})_r = (?)_{10}$$

$$(a_3 \times r^3 + a_2 \times r^2 + a_1 \times r^1 + a_0 \times r^0 + a_{-1} \times r^{-1} + a_{-2} \times r^{-2} + a_{-3} \times r^{-3})_{10} =$$

↪ Decimal to any other Base

$$(a_2 a_1 a_0 \cdot a_{-1} a_{-2})_{10} = (?)_r$$



$$(x_2 x_1 x_0 \cdot y_0 y_1 y_2)_r \text{ All}$$

$0 \cdot a_{-1} a_{-2} \times r = y_0 \cdot a_{-3} a_{-4}$
 $0 \cdot a_{-3} a_{-4} \times r = y_1 \cdot a_{-5} a_{-6}$
 $0 \cdot a_{-5} a_{-6} \times r = y_2 \cdot a_{-7} a_{-8}$



#Q. How many 1's are present in the binary representation of $3 \times 512 + 7 \times 64 + 5 \times 8 + 3$?

- (a) 8
- ~~(b)~~ 9
- (c) 10
- (d) 11

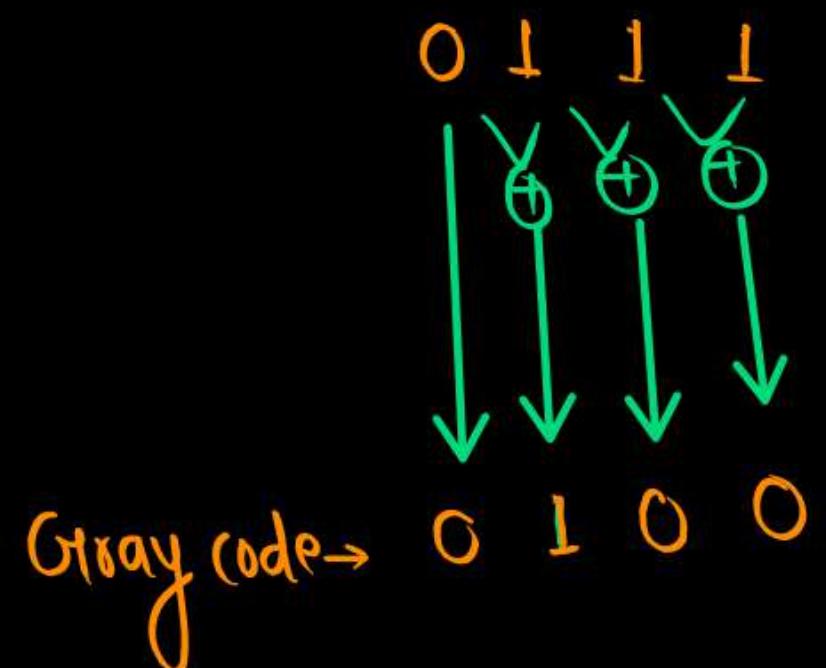
$$\begin{aligned}
 2^0 &\rightarrow 1 \rightarrow 1 \\
 2^1 &\rightarrow 10 \\
 2^2 &= 100 \\
 2^3 &= 1000 \\
 2^4 &= 10000
 \end{aligned}$$

$$\begin{aligned}
 &(2+1)2^9 + (4+2+1)2^6 + (4+1)2^3 + 2 + 1 \\
 &= 2^{10} + 2^9 + 2^8 + 2^7 + 2^6 + 2^5 + 2^3 + 2^1 + 2^0
 \end{aligned}$$

9

#Q. Gray code for number 7 is

- (a) 1100
- (b) 1001
- (c) 0110
- ~~(d) 0100~~



#Q. Given the decimal number - 19, an eight bit two's complement representation is given by

- (a) 11101110
- (b) 11101101
- (c) 11101100
- (d) None of these

0 0 0 1 0 0 1 1 ←
↑ ↑ | 0 1 | 0 1 → +19

#Q. Which of the following binary number is equal to octal number 66.3?

- (a) 101101.100
- (b) 1101111.111
- (c) 111111.1111
- (d) 110110.011

$$\begin{array}{r} 2 | 66 \\ \quad \quad \quad \uparrow \\ \quad \quad \quad . \\ \quad \quad \quad 6 \times 8^0 + 6 \times 8^1 + 3 \times 8^{-1} \end{array}$$

$$0.375 \times 2 = 0.75 \Rightarrow 0$$

$$0.75 \times 2 = 1.5 \Rightarrow 1$$

$$0.5 \times 2 = 1.0 \Rightarrow 1$$

$$\left(48 + 6 + \frac{3}{8} \right)_{10}$$

$$\left(54.375 \right)_{10}$$

$$(66.3)_8 = (\quad)_2$$

$$\downarrow$$

$$(\quad)_{10} \longrightarrow (\quad)_2$$

$$(66.3)_8 = (\quad)_2$$

$\swarrow_2^3 \qquad \searrow_2^1$

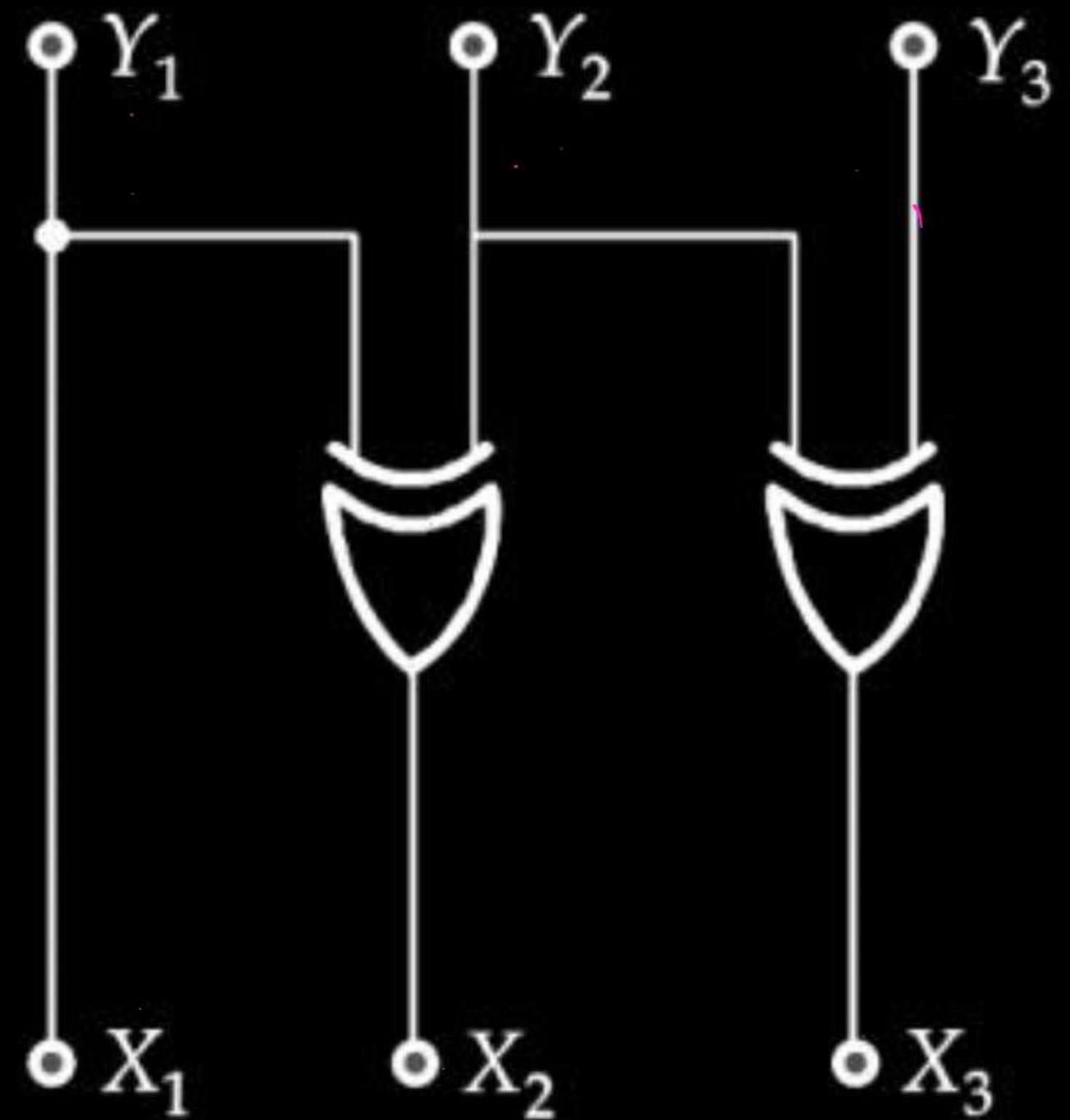


Each no. will be written by 3 bits of binary

$$(110110.011)_2$$

A₁

#Q. The logic circuit given below converts a binary code $Y_1Y_2Y_3$ into



- (a) Excess -3 code
- (b) Gray code
- (c) BCD code
- (d) Hamming code

#Q. The greatest negative number which can be stored in a computer that has 8-bit word length and uses 2's complement arithmetic is

- (a) - 256
- (b) - 255
- ~~(c)~~ - 128
- (d) - 127

$$\text{Range} = -2^{n-1} \text{ to } 2^{n-1} - 1$$

$$-2^{8-1} \text{ to } 2^{8-1} - 1$$

$$-2^7 \text{ to } 2^7 - 1$$

$$-2^7 = -128$$

#Q. If $(146)_x + (313)_{x-2} = (246)_8$, then the value of base x is

- (a) 5
- (b) 6
- (c) ~~7~~
- (d) 9

$$x^2 + 4x + 6 + 3(x-2)^2 + 1 \cdot (x-2) + 3 = 2 \times 8^2 + 4 \times 8^1 + 6$$

$$4x^2 - 7x + 19 = 128 + 32 + 6$$

$$x = 9$$

#Q. The Gray code for $(A5)_{16}$ is equivalent to

- (a) 10010101
- (b) 11010101
- (c) 11011111
- (d) 11011011
- (e) None

$$(A5)_{16} = \begin{smallmatrix} 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 \end{smallmatrix}$$

$$\begin{smallmatrix} 1 & 1 & 1 & 0 & 1 & 1 \end{smallmatrix}$$

#Q. Which of the following statement is wrong?

- (a) $(1000.64)_8 = (100000000.1101)_2$
- (b) $(512.512)_8 = (4022.224)_5$
- (c) $(2202)_6 = (426)_{11}$
- (d) $(0.23)_4 = (0.1011)_2$

#Q. If $(2.3)_{\text{base}4} + (1.2)_{\text{base}4} = (\text{Y})_{\text{base}4}$; What is the value of Y ?

- (a) 10.1
- (b) 10.01
- (c) 10.2
- (d) 1.02

$$\begin{array}{r} 1 \\ (2.3)_4 \\ + (1.2)_4 \\ \hline \underline{(10.1)}_4 \end{array}$$

#Q. The number of 1's in 8-bits representation of -127 in 2's complement form is m and that in 1's complement form is n. What is the value of m : n ?

- (a) ~~2 : 1~~
- (b) 1 : 2
- (c) 3 : 1
- (d) 1 : 3

$$\begin{matrix} m = 2 \\ n = 1 \end{matrix}$$

$$\begin{matrix} -127 \\ \rightarrow \end{matrix}$$

$$\begin{matrix} 127 \\ \rightarrow \end{matrix} \begin{matrix} 01111111 \\ 10000001 \rightarrow 2^7 \end{matrix}$$

$$\begin{matrix} -127 \\ \rightarrow \end{matrix} \begin{matrix} 10000000 \\ 1's \end{matrix}$$

$$m : n$$

$$2 : 1$$

#Q. What is the Gray code word for the binary 101011 ?

- (a) 101011
- (b) 110101
- (c) 011111
- (d) 111110

111110

#Q. What is the addition of $(-64)_{10}$ and $(80)_{16}$?

- (a) $(-16)_{10}$
- (b) $(16)_{16}$
- (c) $(1100000)_2$
- ~~(d)~~ $(01000000)_2$

$$(80)_{16} = (\quad)_{10}$$

$$8 \times 16 = 128$$

$$\begin{array}{r} 128 \\ - 64 \\ \hline \end{array} \qquad \qquad \qquad \begin{array}{r} \downarrow 000000 \\ \hline \end{array}$$

#Q. $(24)_8$ is expressed in Gray code as which one of the following?

- (a) 11000
- (b) 10100
- (c) ~~11110~~
- (d) 11111

$$(24)_8 \rightarrow 010\ 100$$

0 1 1 1 0

#Q. Two 2's complement numbers having sign bits 'x' and 'y' are added and the sign bit of the result is 'z'. Which Boolean function indicates the occurrence of the overflow?

- (a) xyz
- (b) $\bar{x}\bar{y}\bar{z}$
- (c) $\bar{x}\bar{y}z + xy\bar{z}$
- (d) $xy + yz + zx$

$$\begin{array}{r} x \quad 0 \\ y \quad 0 \\ \hline z \quad 1 \end{array}$$
$$\begin{array}{r} x \quad 1 \\ y \quad 1 \\ \hline z \quad 0 \end{array}$$



#Q. Consider the following statements:

1. Taking 2's complement is equivalent to sign change.
2. In the 2's complement representation the most significant bit (MSB) is zero for a positive number
3. In a 4 bit binary representation of a binary number A, $A + 1$'s complement of A = 2^4 .

Which of the above statements are correct ?

- (a) 1 and 2 only (b) 1 and 3 only
 (c) 2 and 3 only (d) 1, 2 and 3

#Q. The hexadecimal representation of 657_8 is:

- (a) 1 AF H
- (b) D 78 H
- (c) D 71 H
- (d) 32 F H

$$(657)_8 = (?)_{16}$$

000 110 101 111

$$(1AF)_{16}$$

#Q. If (73_x) (in base x number system) is equal to (54_y) (in base y number system),
the possible values of x and y are:

- (a) 8 and 16
- (b) 10 and 12
- (c) 9 and 13
- ~~(d)~~ 8 and 11

$$(73)_x = (54)_y$$

$$7x + 3 = 5y + 4$$

#Q. Two numbers are represented in signed 2's complement form as

$$P = 11101101 \text{ and } Q = 11100110 \rightarrow -26$$

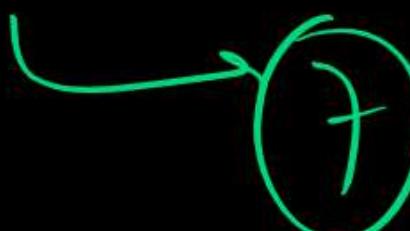
$\begin{array}{r} 11101101 \\ + 11100110 \\ \hline 00000111 \end{array}$

If Q is subtracted from P, the value obtained in signed 2's complement form is

- (a) 100000111
- ~~(b) 00000111~~
- (c) 11111001
- (d) 011111001

$$P = -19 \quad Q = -26$$

$$P - Q = -19 - (-26) = 07$$

00000111


#Q. If $(11X1Y)_8 = (12C9)_{16}$ then the values X and Y are

- (a) 5 and 7
- (b) 3 and 1
- (c) 7 and 5
- (d) 1 and 5

#Q. Binary data is being represented in size of byte and in 2's complement form.
The number of 0's present in representation of (-127)_{DECIMAL} is

- (a) 8
- (b) 7
- (c) 6
- (d) 5

$$\begin{array}{r} +127 \rightarrow 0111111 \\ -127 \quad 1000000 \end{array}$$

#Q. The BCD code for a decimal number $(874)_{10}$ is

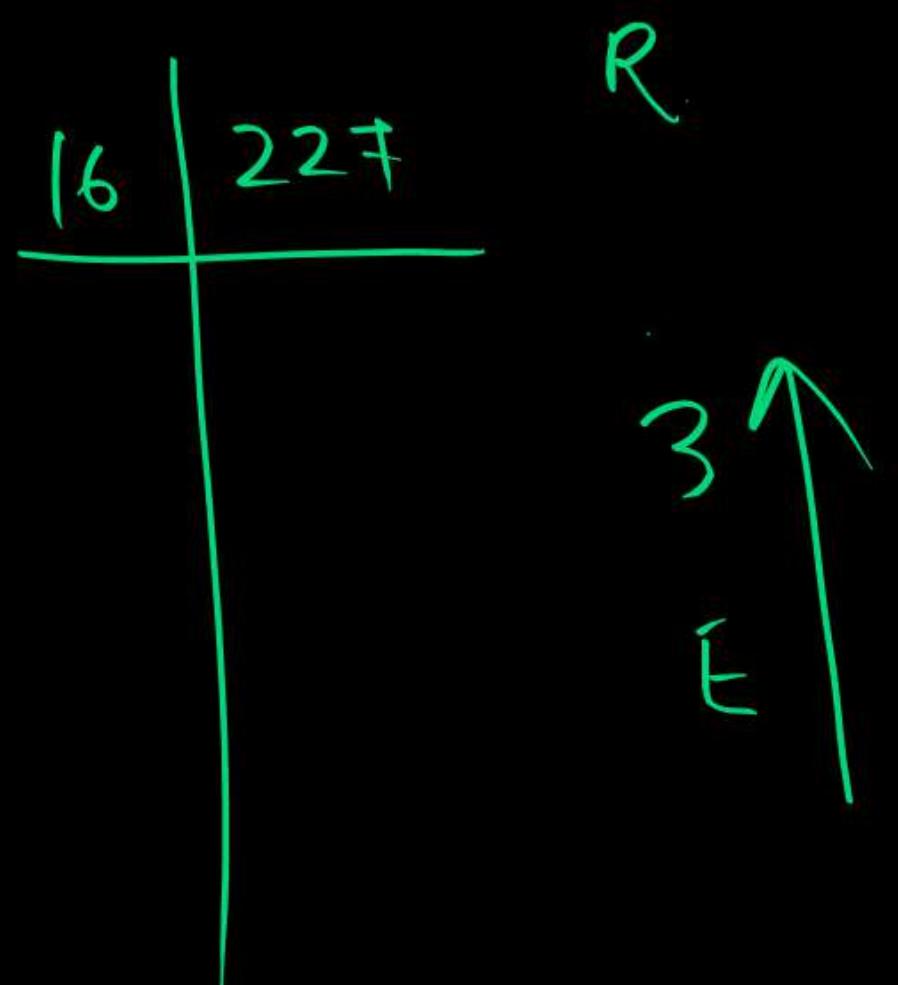
- (a) ~~(100001110100)_{BCD}~~
- (b) $(010001111000)_{BCD}$
- (c) $(100001000111)_{BCD}$
- (d) $(011110000100)_{BCD}$

1000 0111 0100

#Q. Hexadecimal conversion of decimal number 227 will be

- (a) A3
- (b) E3
- (c) CC
- (d) C3

$$(227)_{10} = (?)_{16}$$



#Q. A seven - bit Hamming code is received as 1111101. What is the correct code?

- (a) 1101111
- (b) 1011111
- ~~(c) 1111111~~
- (d) 1111011

#Q. The decimal equivalent of binary number 10110.11 is

- (a) 16.75
- (b) 20.75
- (c) 16.50
- (d) 22.75

(22.75)

#Q. The decimal equivalent of Binary 110.001 is

- (a) 6.25
- (b) 6.125
- (c) 62.5
- (d) 0.612

$$(6.125)$$

#Q. Given $(125)_R = (203)_5$. The value of radix R will

- (a) 16
- (b) 10
- (c) 8
- (d) 6

$$R^2 + 2R + 5 = 5 \cdot 0 + 3$$

$$R^2 + 2R - 48 = 0$$

$$R = -2 \pm \sqrt{4 + 48 \times 4}$$

2

$$R = -2 + \sqrt{4 + 48 \times 1}$$

2

R=6

#Q. Which one of the following is the correct answer when 11011_2 is subtracted from 11101_2 by using the 1's complement method?

- (a) 01001
- (b) 10001
- (c) 00011
- (d) 00010

Hint $P + (-Q)$

#Q. The 2's complement representation of -17 is

- (a) 100001
- (b) 101111
- (c) 110011
- (d) 101110

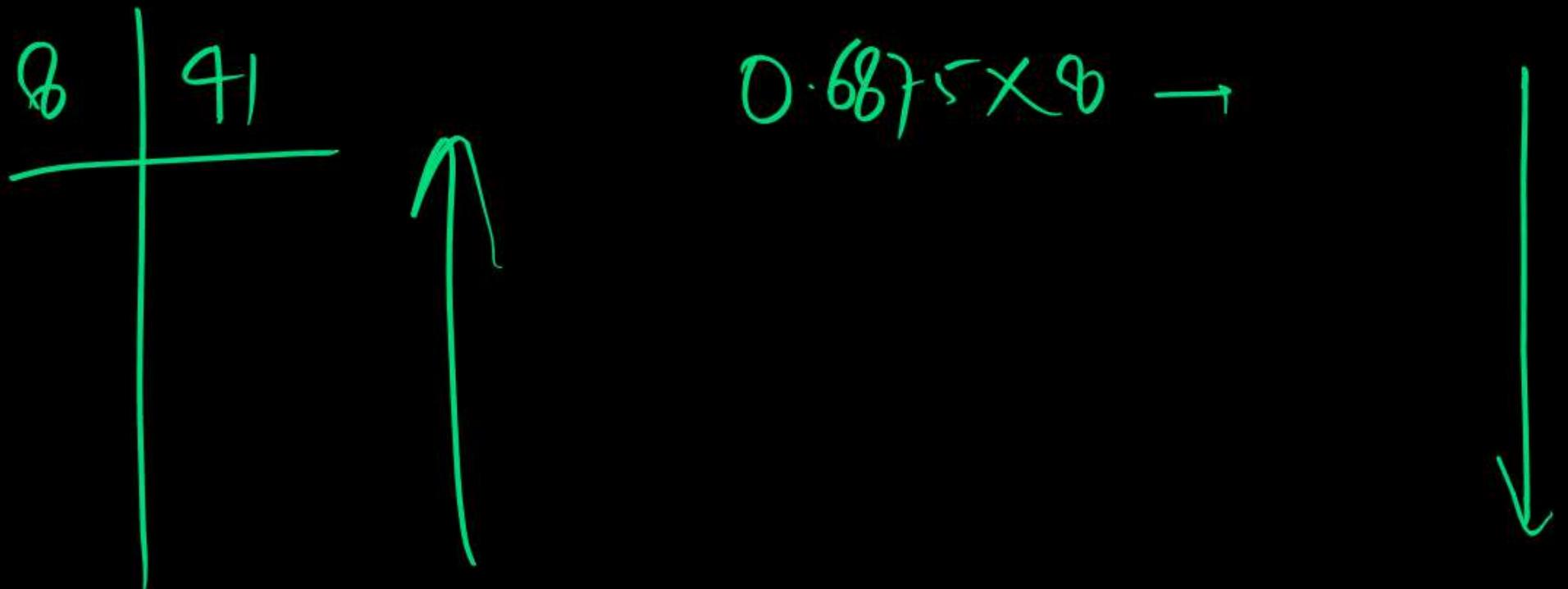
8

#Q. An Excess-3 code arithmetic operation is used to perform the

- (a) Binary addition
- (b) Binary subtraction
- (c) BCD addition
- (d) BCD subtraction

#Q. Convert the decimal 41.6875 into octal

- (a) 51.54
- (b) 51.13
- (c) 54.13
- (d) 51.51



#Q. The subtraction of two hexadecimal numbers $84_{16} - 2A_{16}$ results in

- (a) $2B_{16}$
- (b) $3A_{16}$
- (c) $4B_{16}$
- (d) $5A_{16}$

#Q. What is the base of the numbers for the following operation to be correct ?

$$\frac{(54)_b}{(4)_b} = (13)_b$$

- (a) 2
- (b) 4
- (c) 8
- (d) 16

#Q. The addition of the two numbers $(1A8)_{16} + (67B)_{16}$ will be

- (a) $(889)_{16}$
- (b) $(832)_{16}$
- (c) $(823)_{16}$
- (d) $(723)_{16}$

#Q. Add 8 and 9 in BCD code.

- (a) 00010111
- (b) 00010001
- (c) 01110111
- (d) 10001001

#Q. Convert the binary number 11000110 to Gray code.

- (a) 00100101
- (b) 10100100
- (c) 11100110
- (d) 10100101

#Q. The decimal value of the signed binary number 10101010 expressed in 2's complement will be

- (a) -42
- (b) -86
- (c) -116
- (d) -170

#Q. Convert $(329.54)_{10}$ to hexadecimal.

- (a) $(149.8A3D70A)_{16}$
- (b) $(219.8A3D70A)_{16}$
- (c) $(149.8A70AD)_{16}$
- (d) $(219.8A70AD)_{16}$

#Q. The most personal computers (PCs) compatible computer systems use a 20-bit address code to identify each of over 1 million memory locations. What is the 5-digit hexadecimal address of the 500th memory location?

- (a) 001F3
- (b) 001F4
- (c) 001F5
- (d) 001F6

Thank you
GW
Soldiers!



Electronics and Communication Engineering

COMPUTER SCIENCE



Digital Electronics

Lecture - 08
DIGITAL LOGIC



By- CHANDAN JHA SIR

Today's Goal

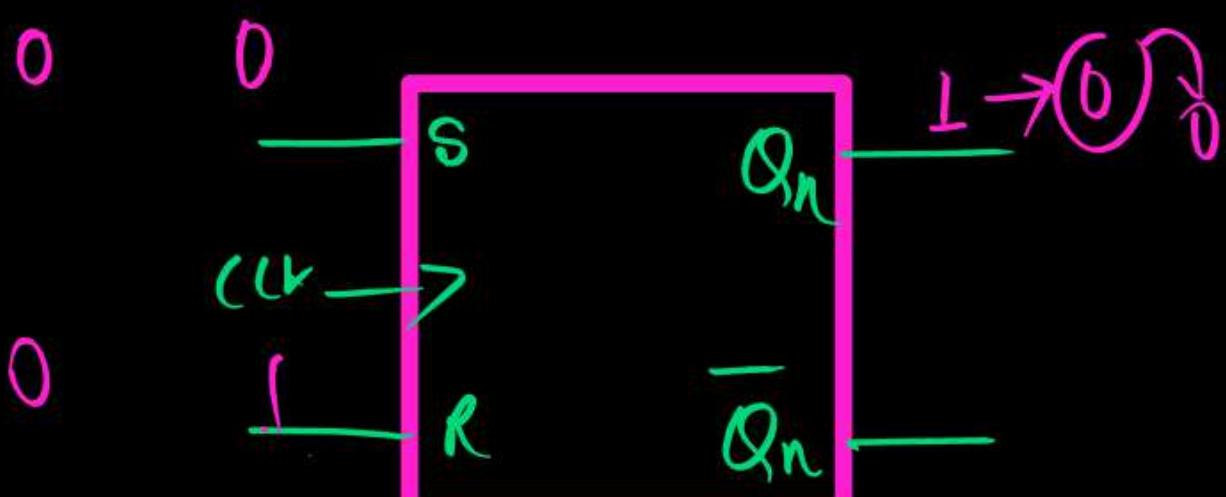
Todays Goal : →

Questions on sequential circuit

Question (MCQ)

In a S-R flip-flop, the present output is $Q = 1$. Then after applying input $S = 0, R = 1$ and then $S = 0, R = 0$, output will be:

- | A $Q = 0$
- | B $Q = 1$
- | C $Q \rightarrow$ invalid state
- | D None of these



$$\begin{array}{ll} S=0 & R=1 \\ S=0 & R=0 \end{array} \quad Q_{n+1}=0 \quad Q_{n+1}=0$$

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

Question (MCQ)



Which of the following is true?

- A $S = 1, R = 1$, is a valid state input for S-R ff
- B $J = 1, K = 1$ is an invalid state input for J-K ff
- C Input $(0, 0)$ is hold state input for both S-R as well as JK ff
- D None of these

Question (MCQ)



A flip flop has characteristic equation

$$Q(n+1) = \bar{A}\bar{Q} + \bar{B}Q$$

Then it will be in toggle mode of operation if

| A A = 1, B = 1

| B ~~A~~ A = 0, B = 1

| C A = 1, B = 0

| D A = 0, B = 0

$$Q_{n+1} = \bar{Q}_n$$

Toggle mode

$$Q_{n+1} = \bar{A}\bar{Q} + \bar{B}Q$$

$$Q_{n+1} = \bar{Q}$$

$$\bar{A} = 1 \quad \bar{B} = 0$$

$$A = 0 \quad B = 1$$

Question (MCQ)

In J-K FF, to change output from 0 to 1 input is changed from

| A | $J = 0, K = 0$ to $J = 0, K = 1$ ✗

| B | $J = 0, K = 1$ to $J = 1, K = 0$ ✓

| C | $J = 0, K = 1$ to $J = 0, K = 0$ ✗

| D | $J = 1, K = 0$ to $J = 0, K = 1$ ✗

$0 \rightarrow$

$J=0 \quad R=1$

$J=1 \quad K=0$

$J=1 \quad K=1$

$0 \rightarrow$

$J \quad K$

Q_n	Q_{n+1}	J	K
0	0	0	✗
0	1	1	✗
1	0	✗	1
1	1	✗	0

Diagram illustrating the state transition of a J-K flip-flop. The current state is Q_n (green). The next state Q_{n+1} (green) is determined by the inputs J and K (orange). The truth table shows four possible states: (0,0), (0,1), (1,0), and (1,1). The inputs $J=0, K=1$ (highlighted with a box and circled) result in a transition from (0,0) to (1,0), which is highlighted with a dashed box and circled. Other transitions are marked with a red '✗'.

Question (MCQ)



Which of the following statement is true?

- | A Master-Slave ff is used to avoid race-around condition.
- | B Edge triggered J-K FF has problem of race-around condition when $J = 1, K = 1$
- | C Race-around condition occurs in S-R ff with $S = 1, R = 1$
- | D None of these

Question (MCQ)

To solve the problem of invalid state at input $S = 1$ and $R = 1$ in S-R ff, S and R are replaced by

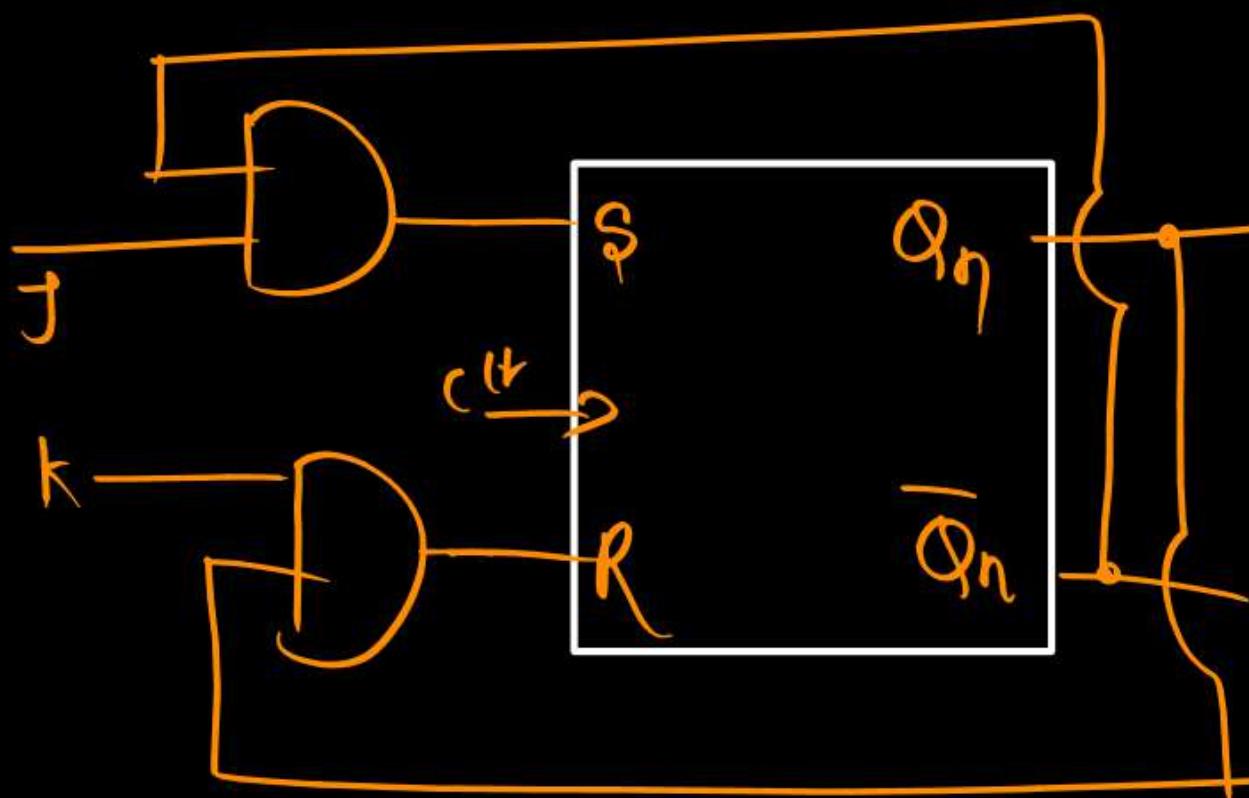
| A $S = J\bar{Q}, R = \bar{K}Q$

$$S = J\bar{Q}_n \quad R = KQ_n$$

| B ~~$S = J\bar{Q}, R = KQ$~~

| C $S = JQ, R = \bar{K}Q$

| D $S = JQ, R = KQ$



Question (MCQ)

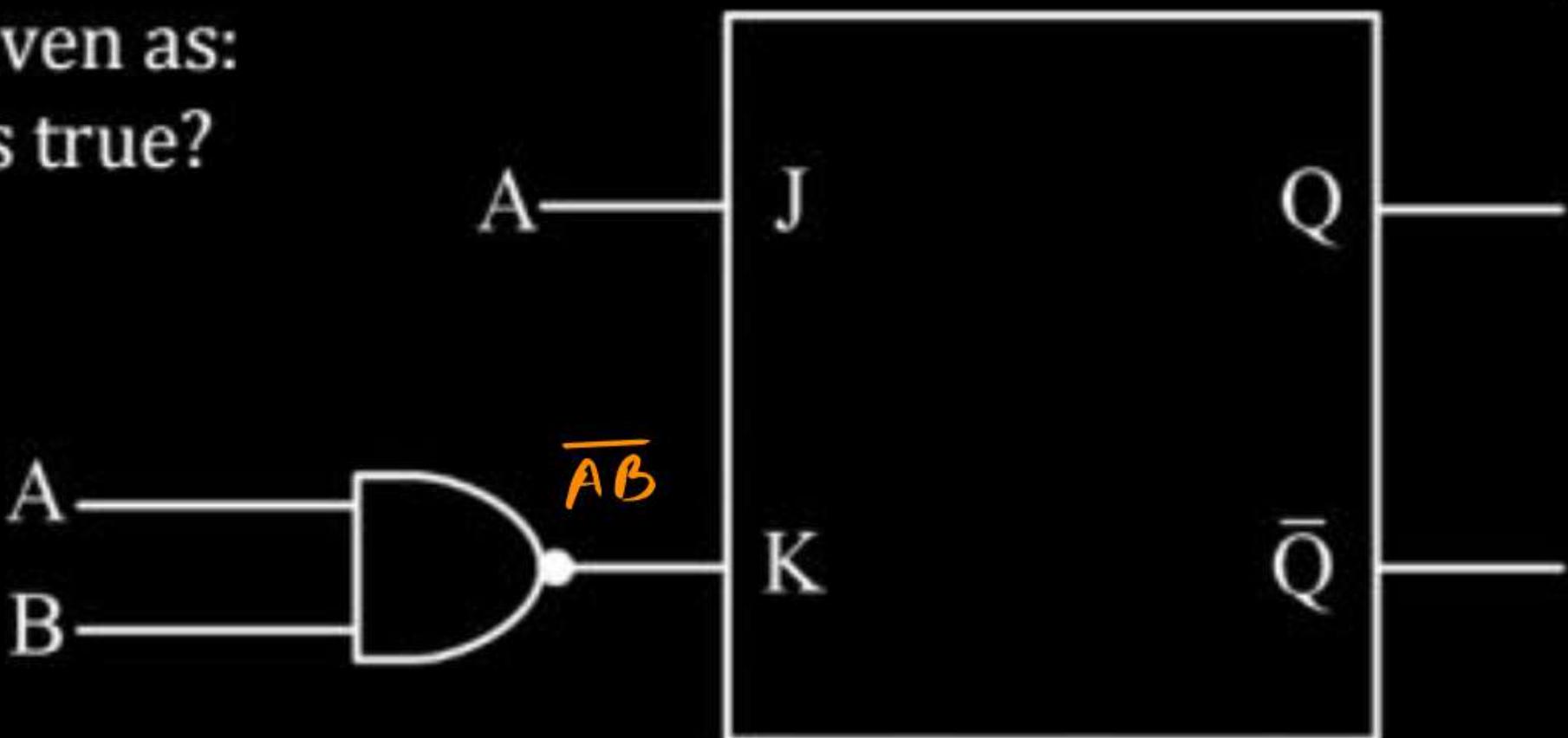
In J-K FF, J and K inputs are given as:
Then which of the following is true?

| A ~~$Q(n+1) = A\bar{Q} + AB$~~

| B $Q(n+1) = A\bar{Q} + \bar{B}Q$

| C $Q(n+1) = A \oplus B \oplus Q$

| D $Q(n+1) = A \oplus B$



$$\begin{aligned}Q_{n+1} &= J\bar{Q}_n + \bar{K}Q_n & J=A & K=\bar{A}B \\&= A\bar{Q}_n + ABQ_n & & \bar{K}=AB \\&= A[\bar{Q}_n + BQ_n] = A[(\bar{Q}_n + B) \cdot (\bar{Q}_n + Q_n)] = A\bar{Q}_n + AB\end{aligned}$$

Question (MCQ)

Which of the following is true?

$$\begin{array}{ll} S=0 & R=0 \\ S=0 & R=1 \\ S=1 & R=0 \end{array}$$

$$S = R = 1$$

$$Q_{n+1} = X$$

$$Q_{n+1} = 1 + 0^Q.$$

$$= 1$$

| A $Q(n+1) = S + \bar{R}Q$ is valid for all S and R values

| B $Q(n+1) = J\bar{Q} + \bar{K}Q$ is valid only when $J \cdot K = 1$ \times

| C $Q(n+1) = S + \bar{R}Q$ is valid when $S \cdot R = 1$ \times

| D $Q(n+1) = S + \bar{R}Q$ is valid when $S \cdot R = 0$

Question (MCQ)



A counter sequence is given as:

2 - 3 - 1 - 0 - 4 - 7, then MOD no. of the counter is

| A 7

| B 8

| C 5

| D 4

Question (MCQ)



A sequential circuit is as given below:

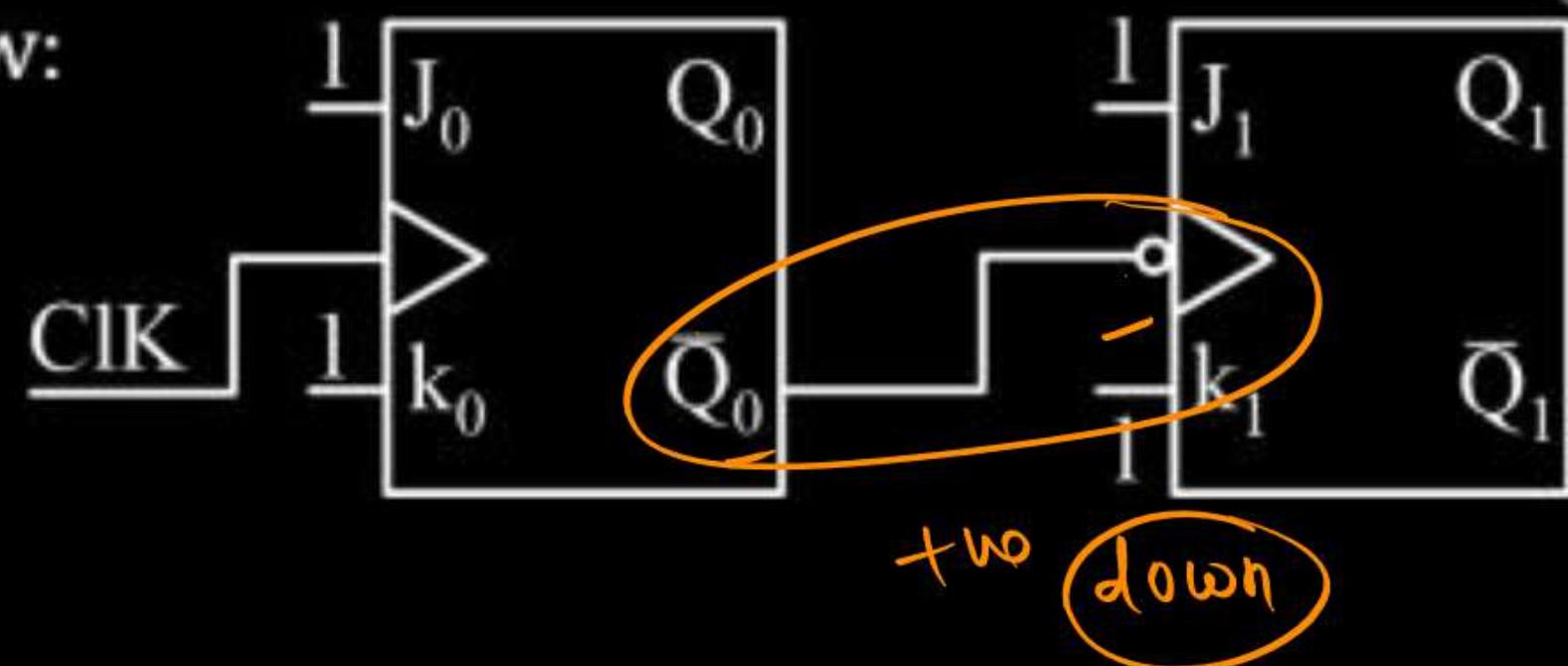
The above circuit is

| A MOD -4 up counter

| B MOD-4 down counter

| C MOD-4 neither up nor down counter

| D MOD-2 counter

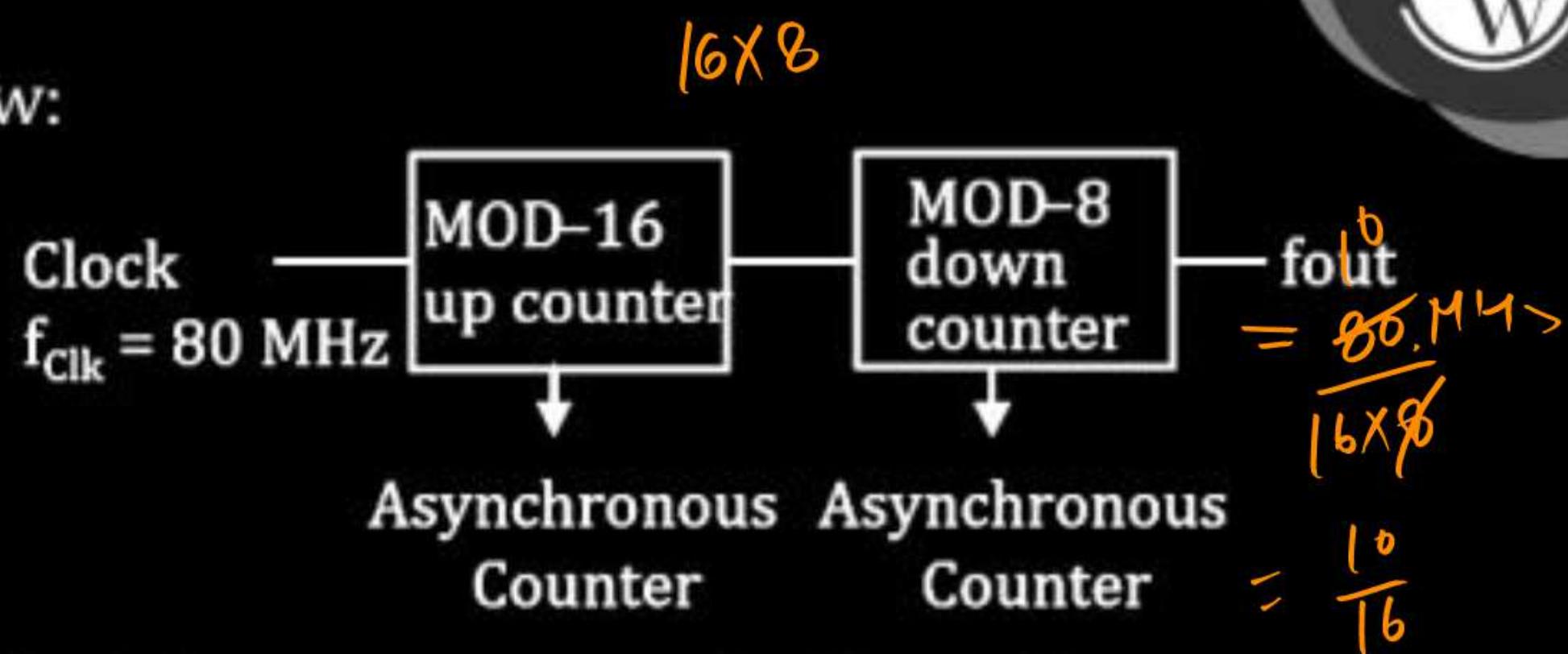


4- MOD down

Question (MCQ)

A sequential circuit as given below:

The value of f_{out} will be



- A Can not be calculated as one block is up-counter and other is down counter
- B 5 MHz
- C 0.625 MHz
- D 3.33 MHz

Question (MCQ)



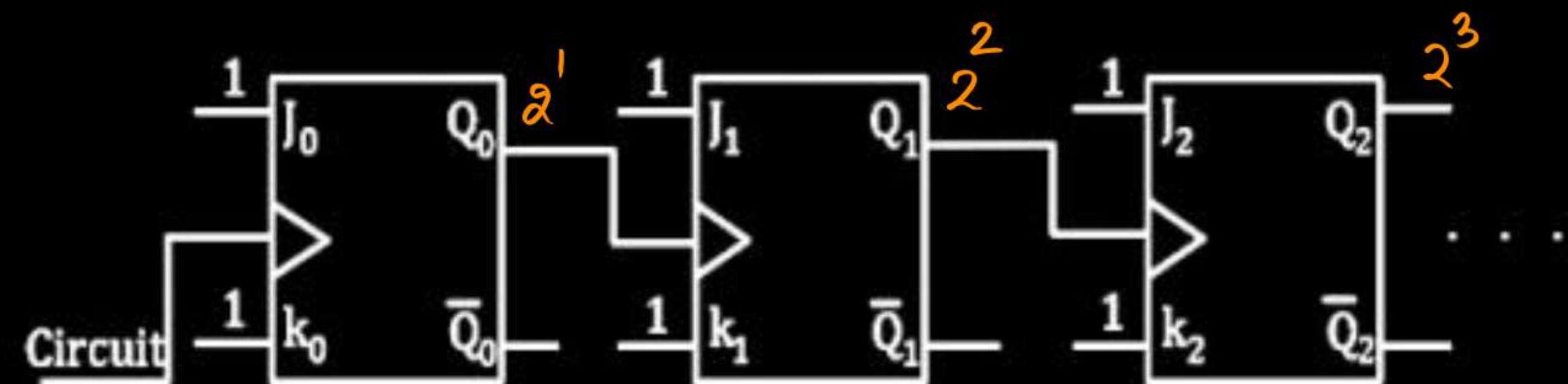
MOD-12 counter can be designed

- | A cascading two MOD-6 counter
- | B cascading MOD-4 counter, and MOD-8 counter
- | C ~~cascading MOD-4 & mod-3 counter~~
- | D cascading MOD-3 & MOD-9 counter

Question (MCQ)

A sequential circuit is as given below has total 20 FFs connected. If input clock frequency is 128 MHz, at output of 16th FF frequency of the waveform will be:

- A 8 MHz
- B 12.8 MHz
- C 1.95 KHz.
- D 4 MHz



$$\begin{aligned} & \cancel{\frac{128 \times 1000 \text{ KHz}}{2^4 \times 2^9}} \\ & = \frac{1000 \text{ KHz}}{512} = 1.95 \text{ KHz} \end{aligned}$$

$$f_{\text{out}} = \frac{f_{\text{in}}}{2^{16}} = \frac{128 \text{ MHz}}{2^{16}}$$

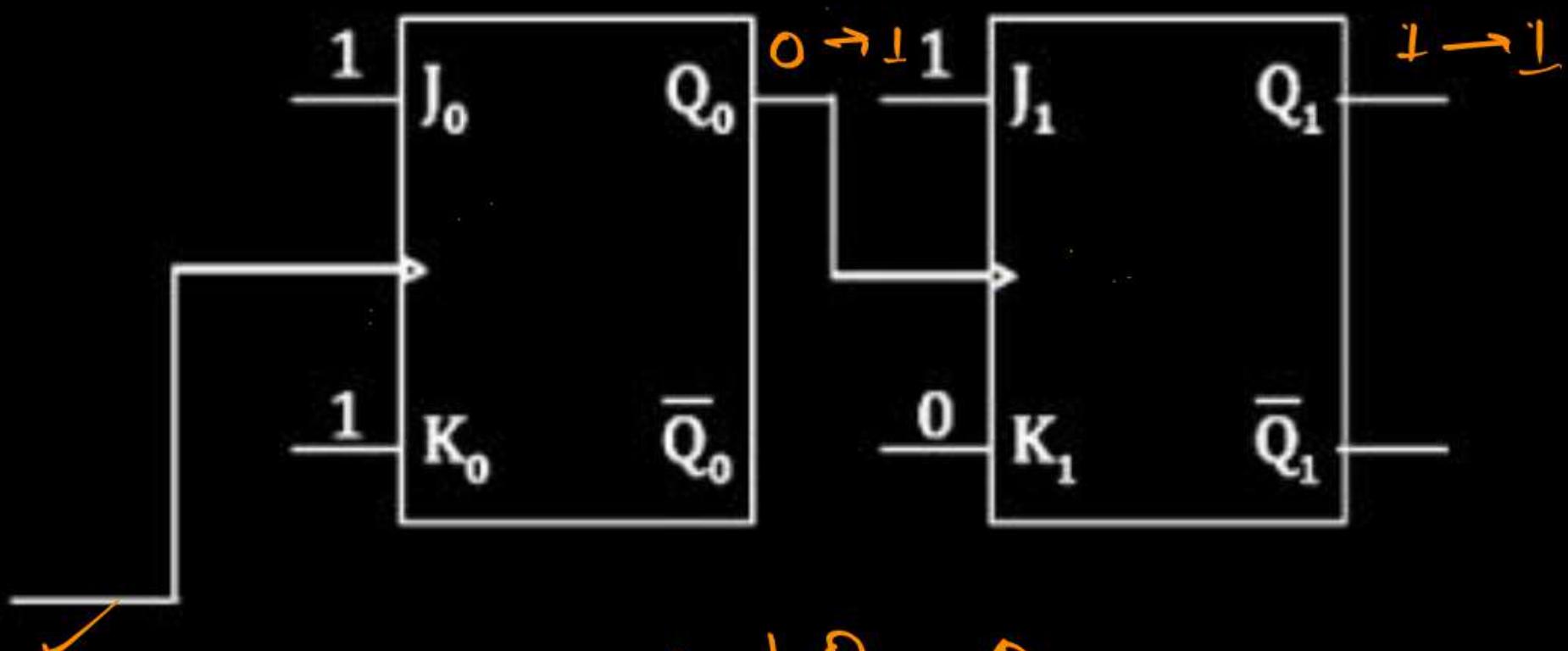
Question (MCQ)

A sequential circuit is as given below:

$0 \rightarrow 1$

Both the FFs are at reset state initially, then MOD-no. of the counter is

- A MOD-4 counter
- B MOD-3 counter
- C MOD-2 counter
- D None of these



CLK	Q ₀	Q ₁
0	0	0
1	1	1
2	0	1
3	1	1

Question (MCQ)

A sequential circuit is as given below:

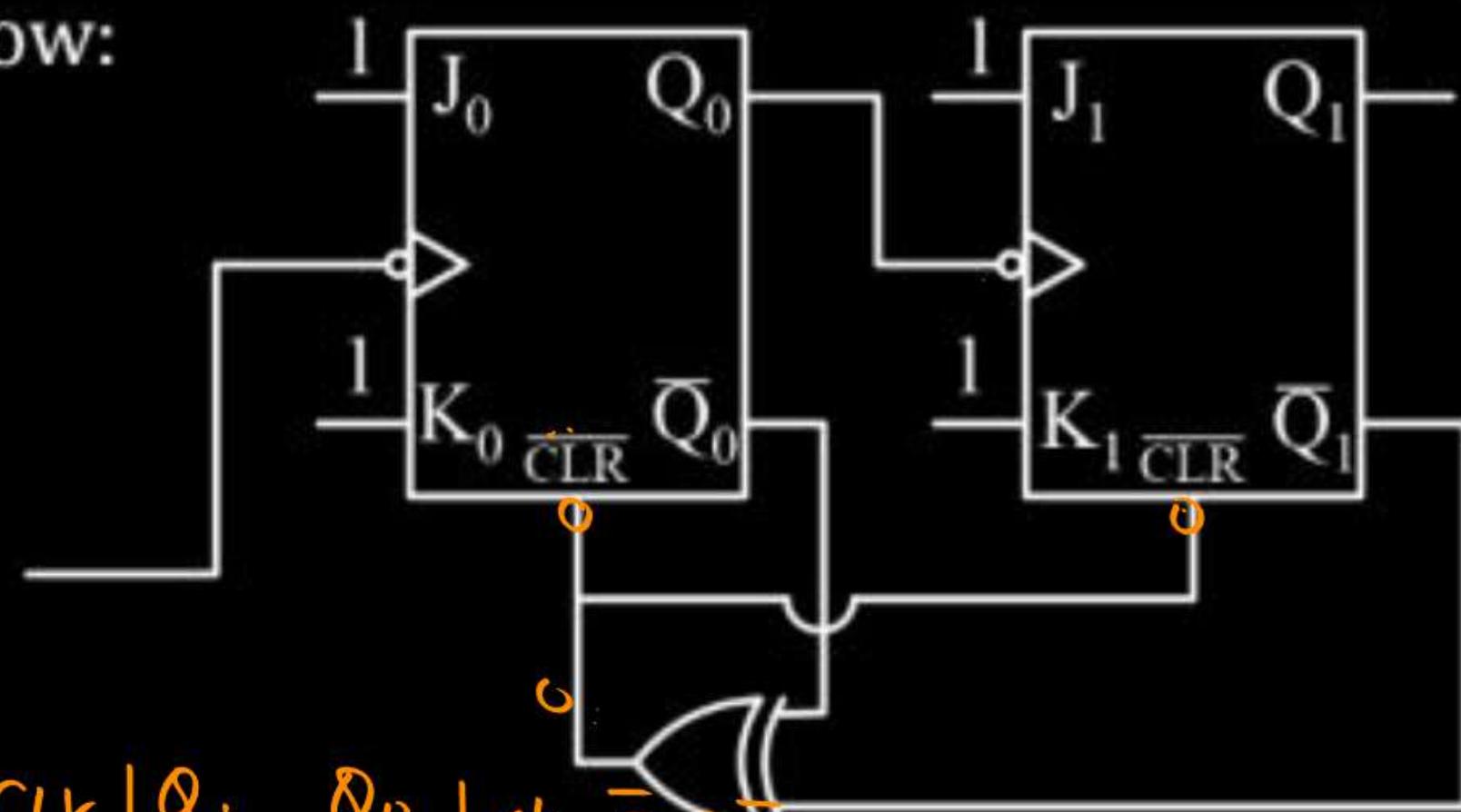
The counter is _____.

[A] MOD-4 UP counter

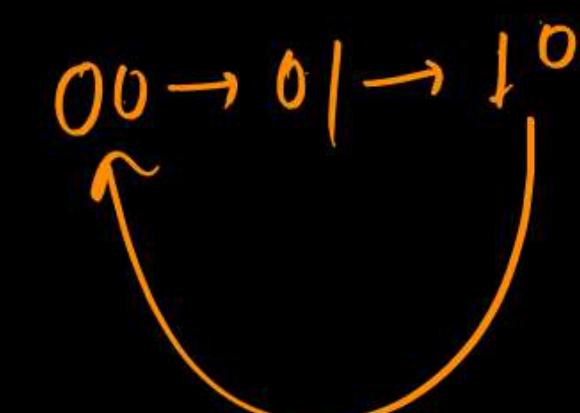
[B] MOD-3 Down counter

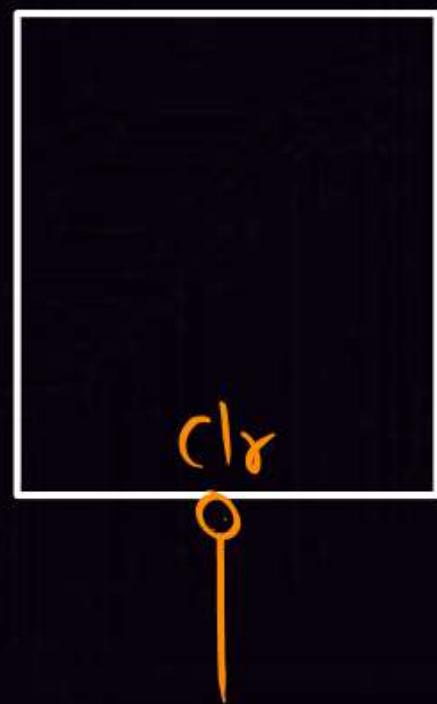
[C] MOD-3 UP counter

[D] MOD-4 Down counter



Clk	Q ₁	Q ₀	Clk = $\bar{Q}_1 \oplus \bar{Q}_0$
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0





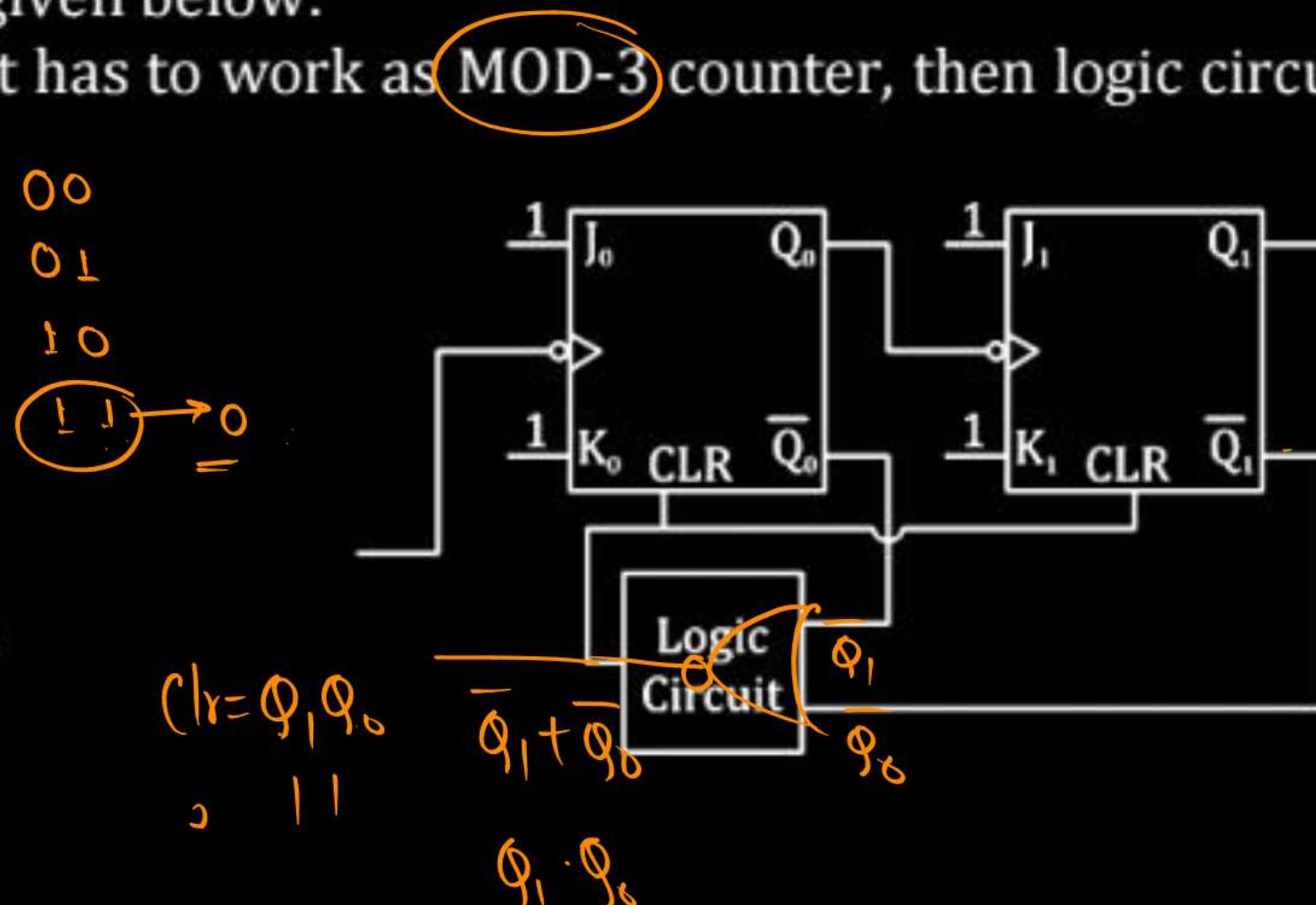
Active low

Question (MCQ)

A sequential circuit is as given below:

If above sequential circuit has to work as MOD-3 counter, then logic circuit will be:

- [A] Two input OR gate
- [B] Two input AND gate
- [C] Two input NAND gate
- [D] Two input NOR gate



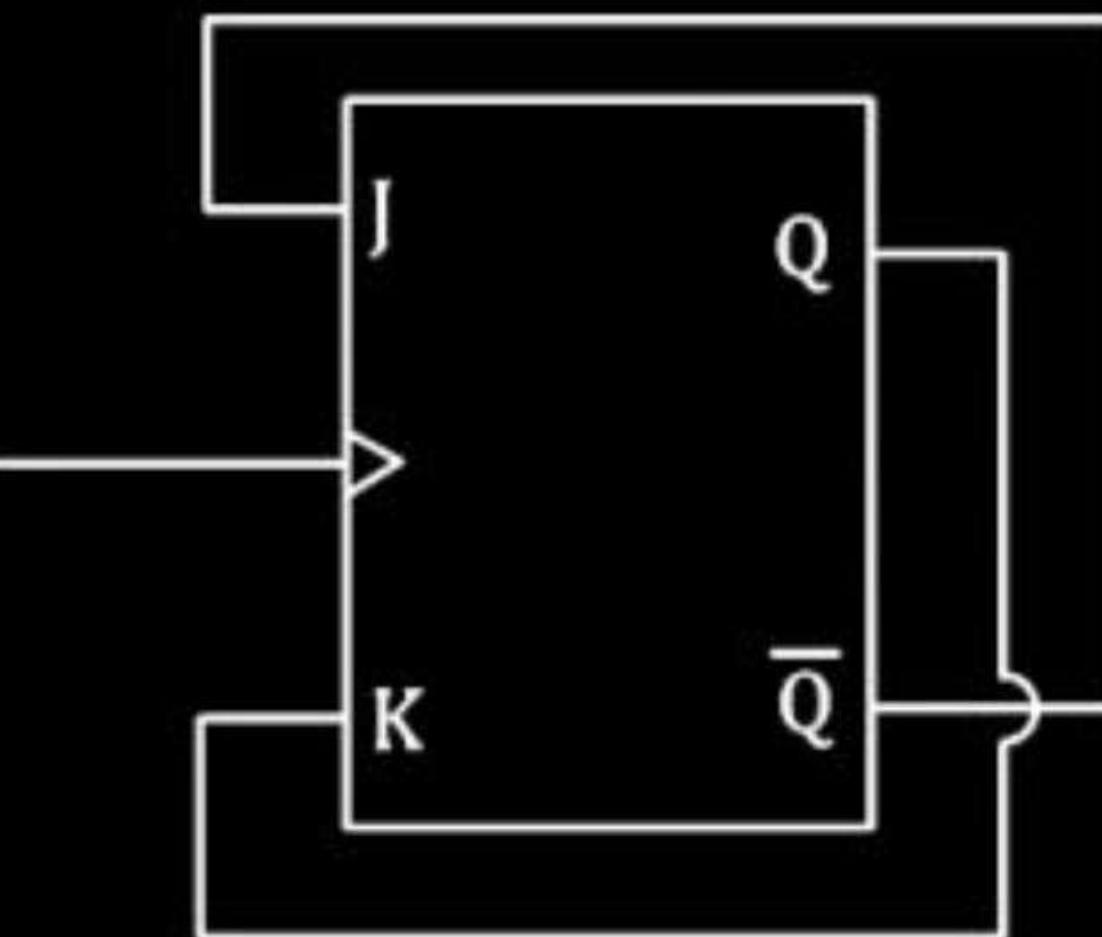
Question (MCQ)



Let's consider the circuit given below:

Counter is at $Q = 0$ initially, then after applying clock pulses the sequence generated at \bar{Q} will be

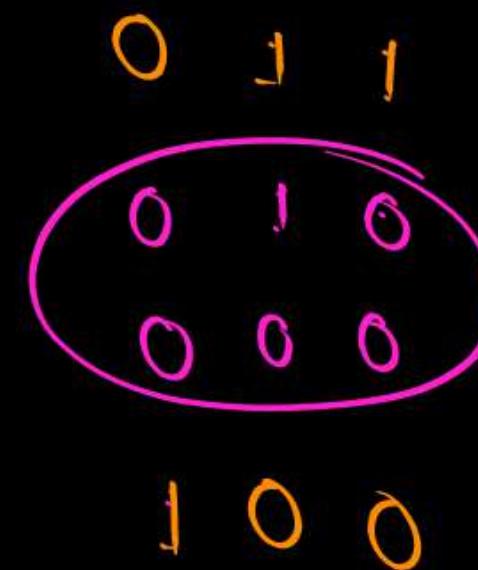
- A 1010101010.....
- B 110011001100....
- C 0110001010011...
- D 01011011101....



Question (MCQ)

We have MOD-8 asynchronous counter, counting in up-sequence. Delay of each FF is t_d . Initially it is at $(011)_2$ and 1-clock is applied then decoding errors that will appear →

- A ~~$(010)_2$ & $(000)_2$~~
- B $(000)_2$ & $(101)_2$
- C $(101)_2$ & $(010)_2$
- D $(010)_2$ & $(110)_2$



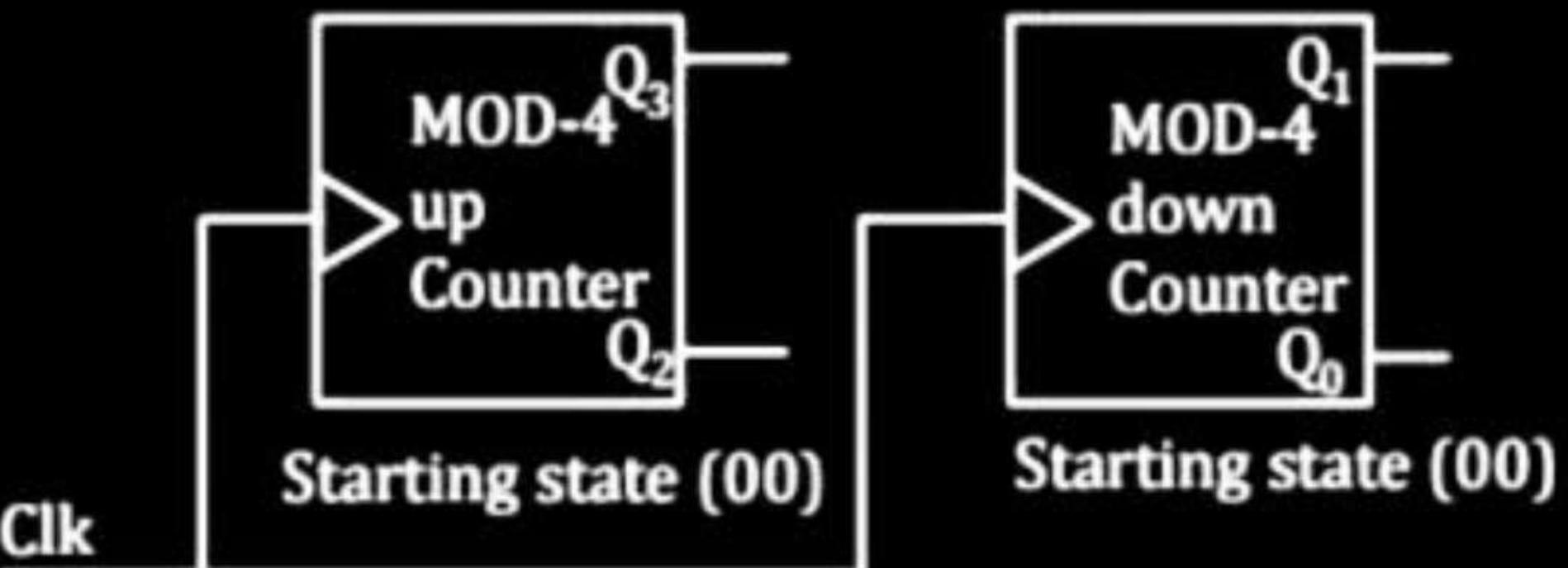
Question (MCQ)

A sequential circuit is as given below:

After applying clock pulses, which count sequence will not appear at output $Q_3Q_2Q_1Q_0$?

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	1
0	0	0	0

- [A] $(0)_{10}$
- [B] $(7)_{10}$
- [C] $(10)_{10}$
- [D] ~~$(11)_{10}$~~



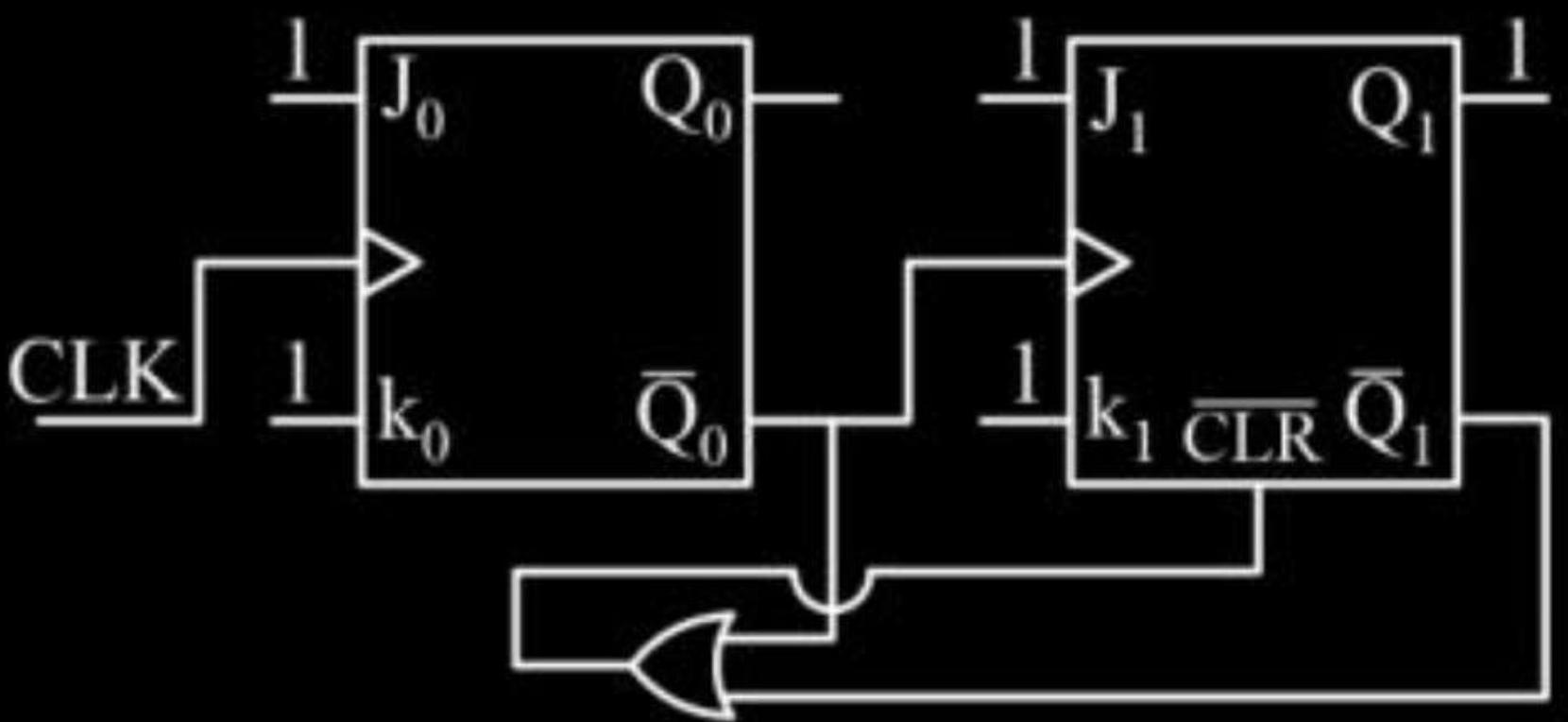
Question (MCQ)



We have sequential circuit as given below:

The above circuit is

- A MOD-3 counter
- B MOD-2 counter
- C MOD-4 counter
- D None of these



Question (MCQ)

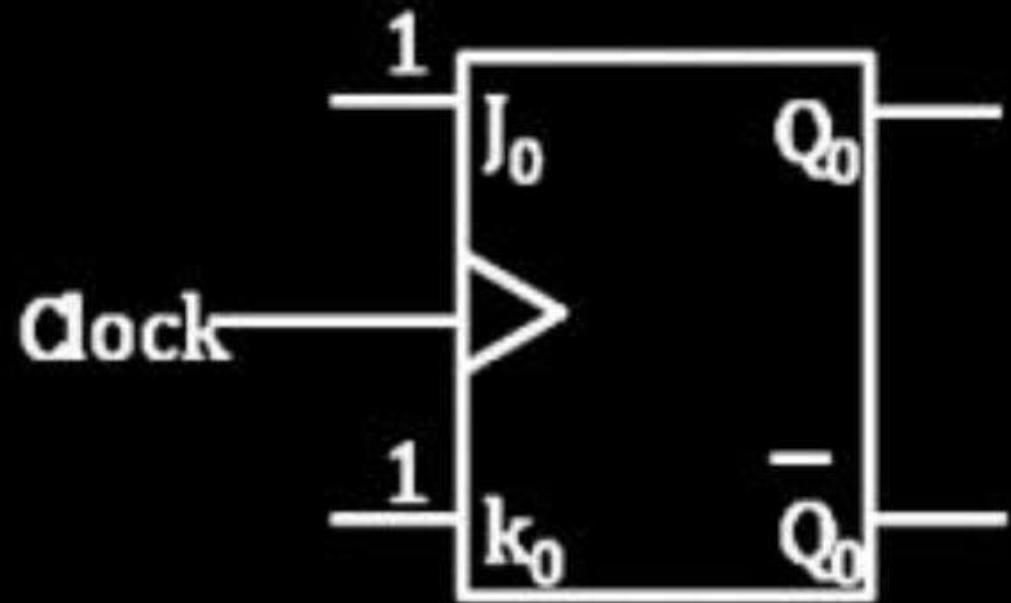
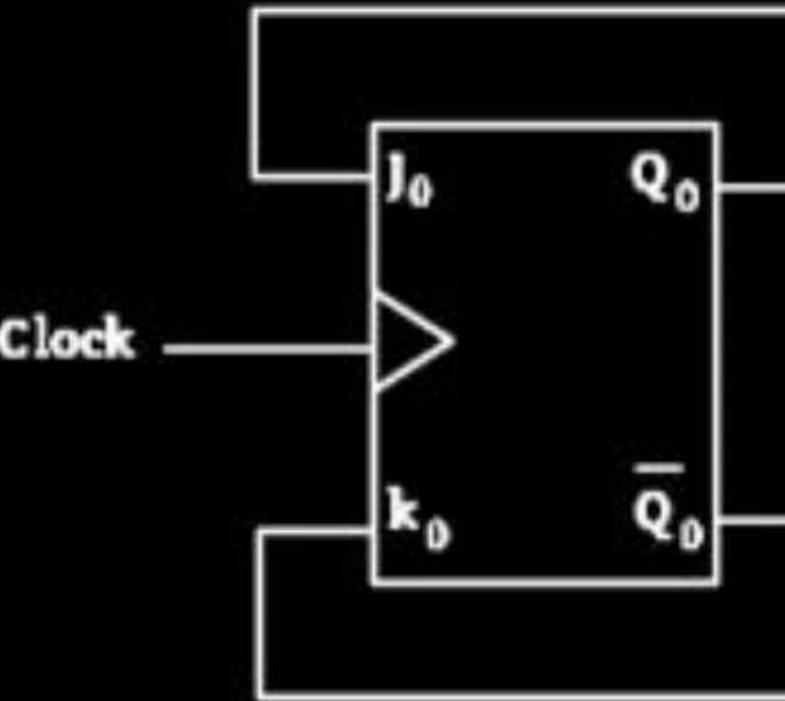
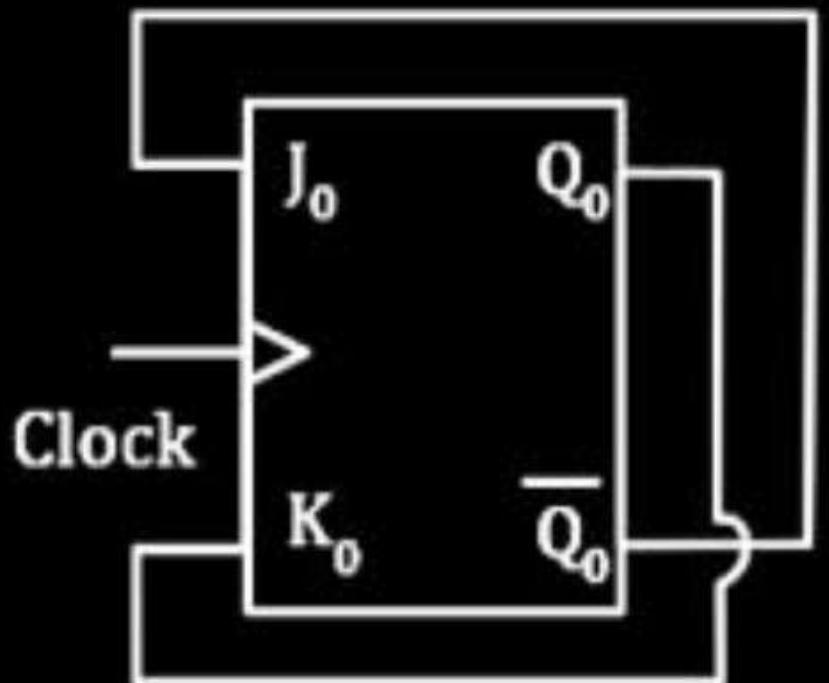
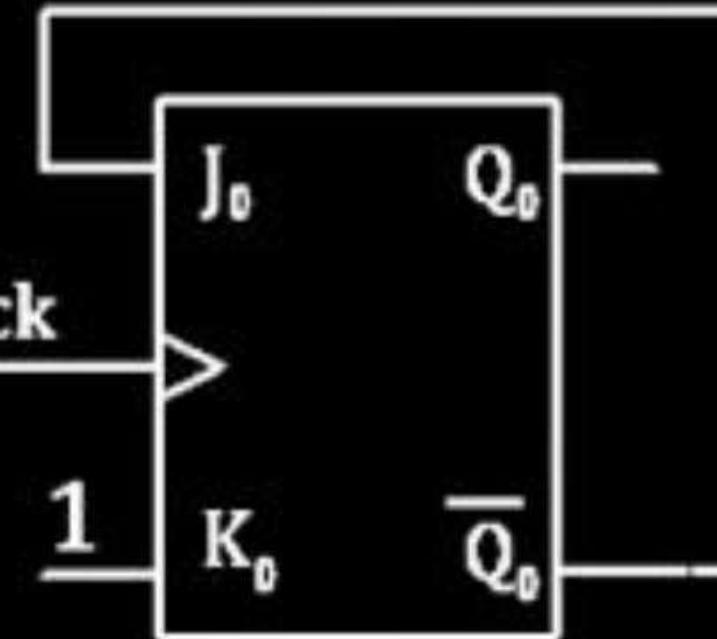


Which of the following is true about decoding error in asynchronous counter?

- A** It is removed by using additional signaling
- B** It can be avoided using strobe signal
- C** Decoding error is present in asynchronous as well as in synchronous counter
- D** None of these

Question**(MSQ)**

Which of the following circuit represents toggle mode of operation?

| A**| B****| C****| D**

Question (MSQ)



A FF is given as:

Characteristic equation of above FF is

$$Q(n+1) = A \odot B \oplus Q(n)$$

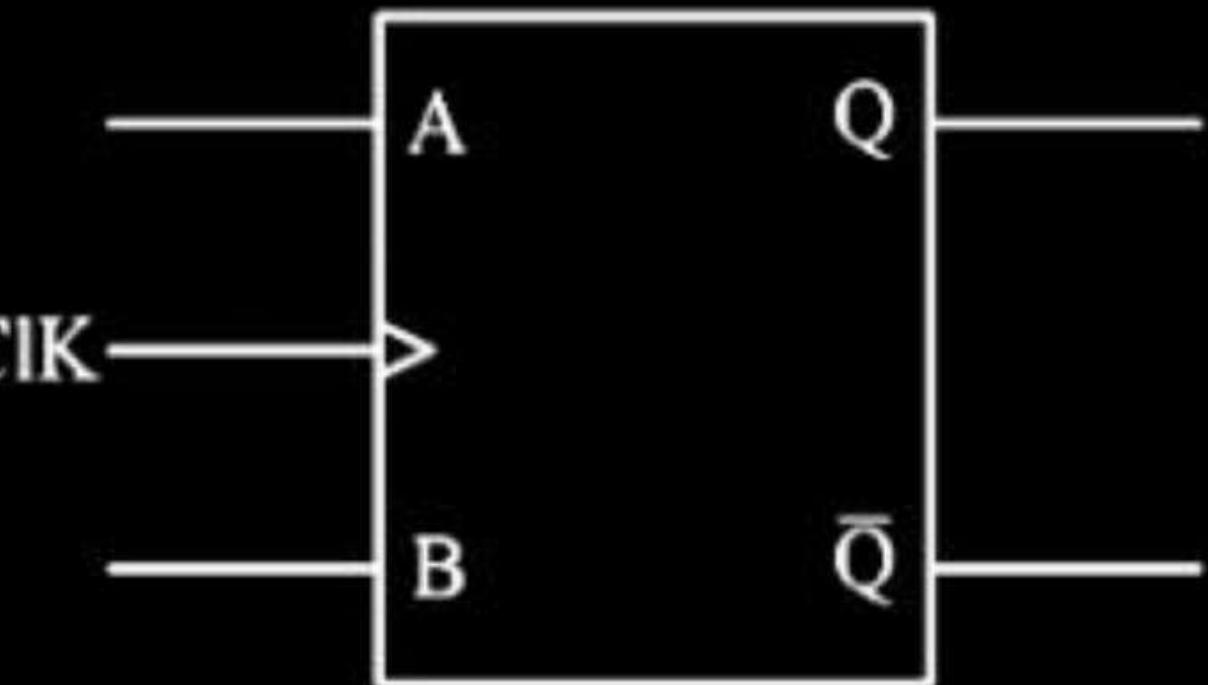
To convert this FF into T-FF, A & B will be:

| A A = T, B = 1

| B A = \bar{T} , B = 1

| C A = \bar{T} , B = 0

| D A = 0, B = \bar{T}



Question (MCQ)



To convert J-K FF into D-FF, J-K input will be

| A | J = \bar{D} , K = D

| B | J = K = D

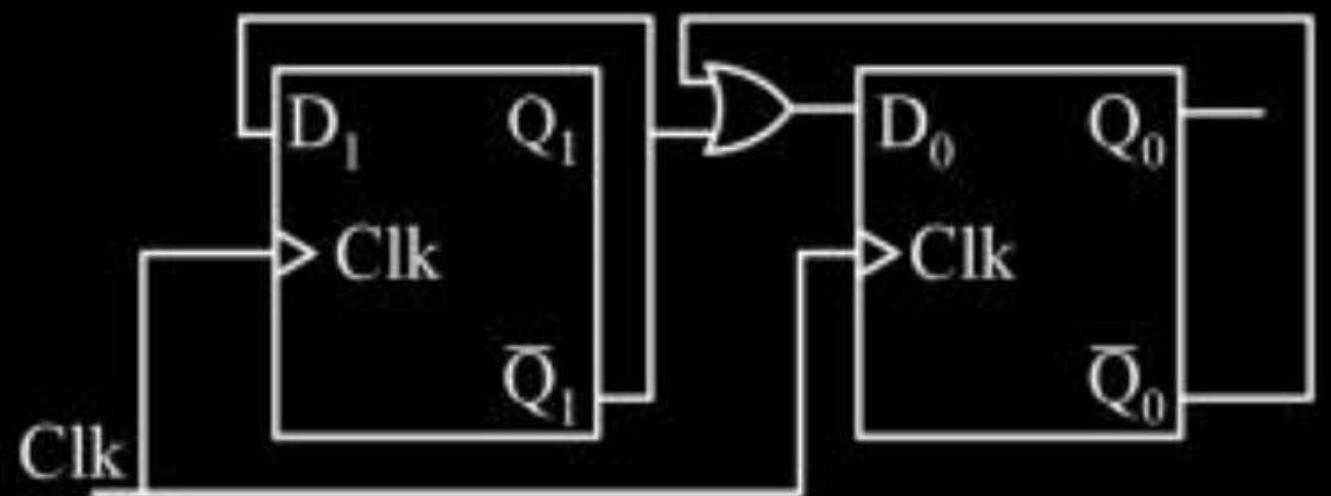
| C | J = D, K = \bar{D}

| D | J = K = \bar{D}

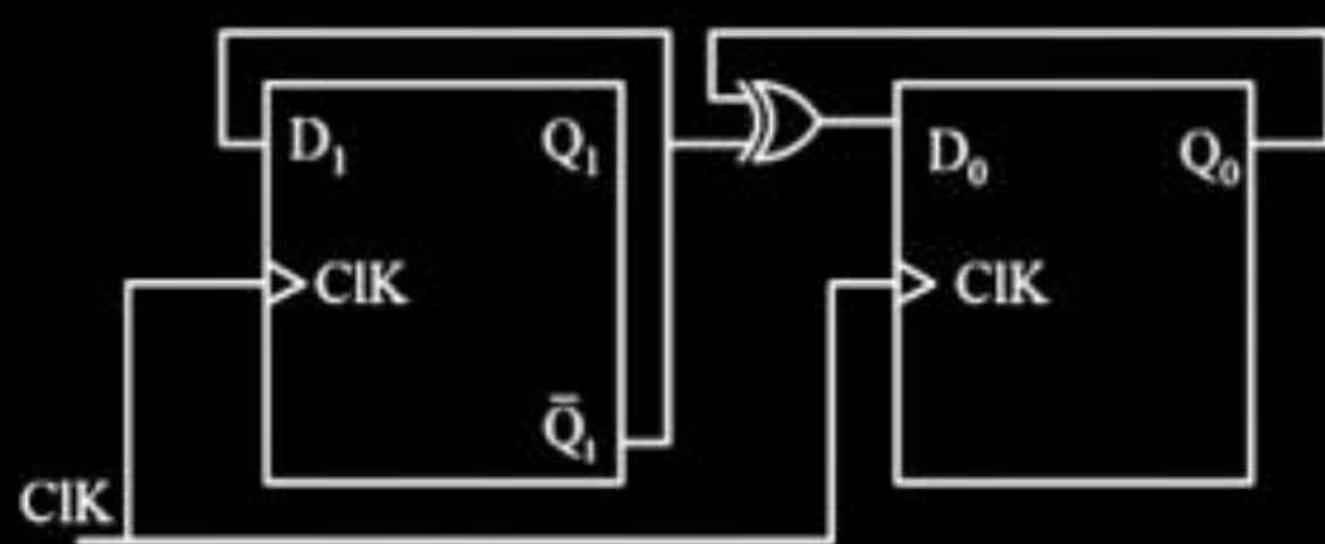
Question (MCQ)

To design a counter with counting sequence 0 - 3 - 1 - 2 - 0 the circuit will be

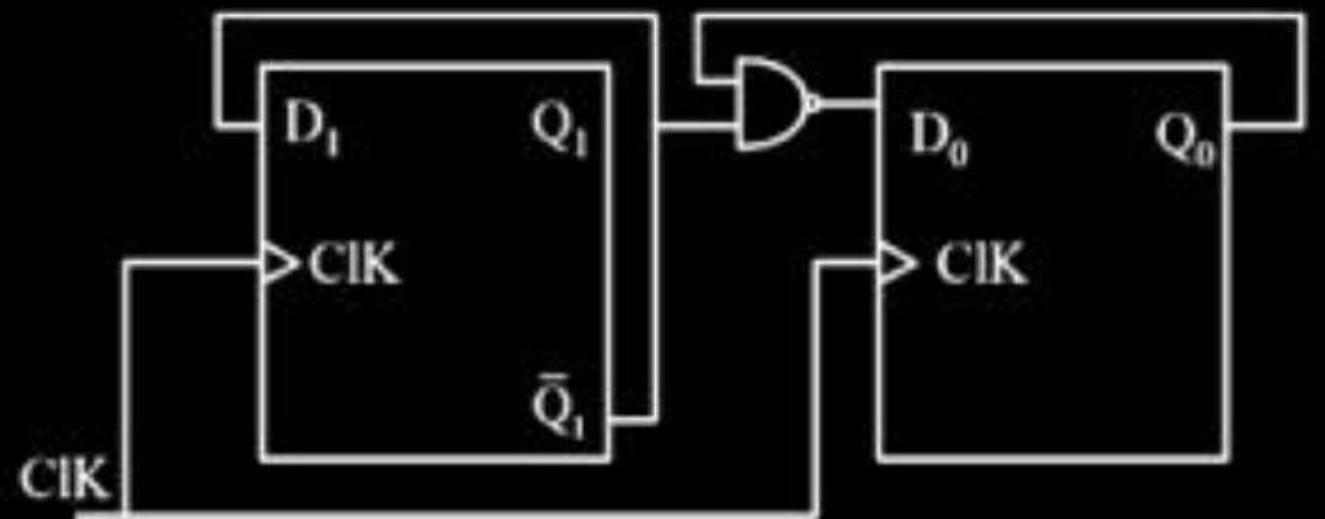
[A]



[B]



[C]



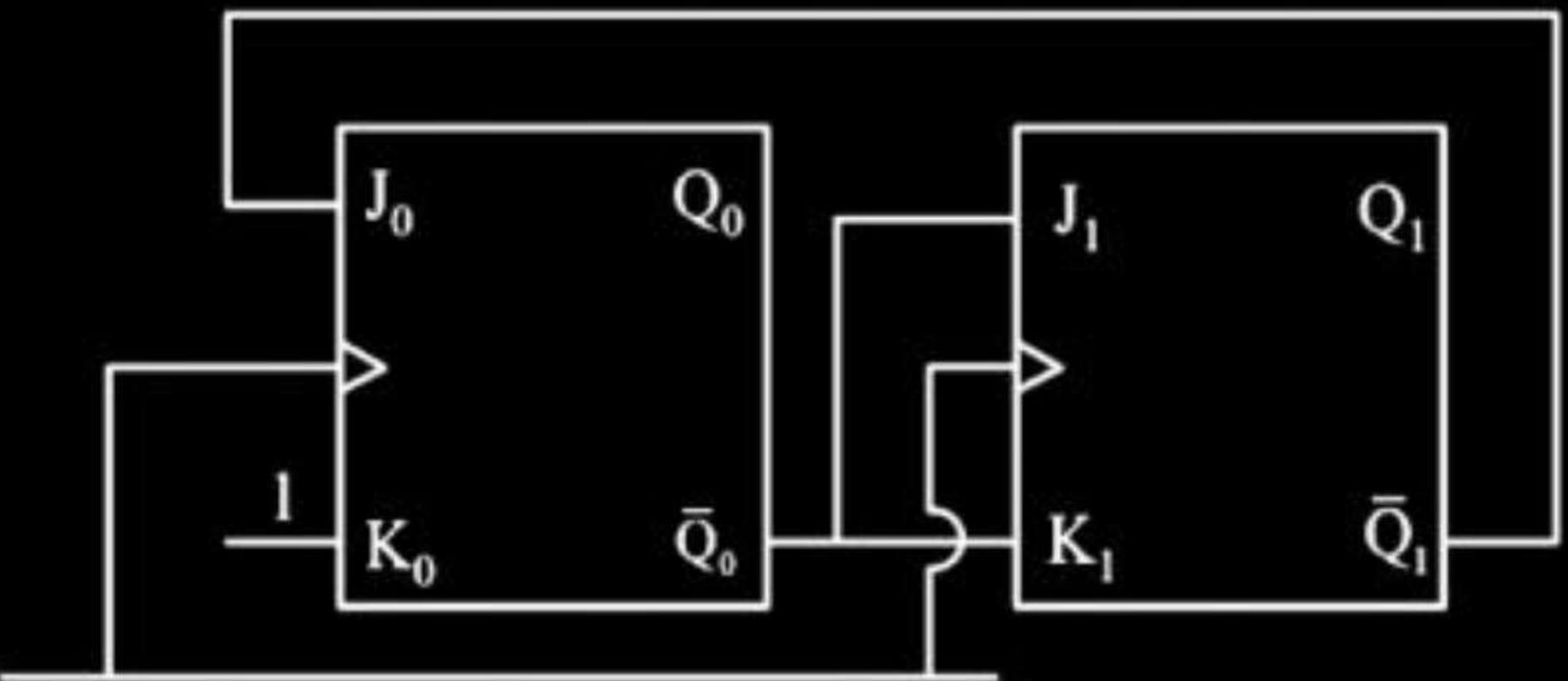
[D] None of these

Question (MCQ)

A sequential circuit is as given below:

Initially counter is at $Q_1Q_0 = (11)_2$, then after applying clock next state will be

- [A] $(01)_2$
- [B] $(10)_2$
- [C] $(00)_2$
- [D] None of these



Question (MCQ)



We have a T-FF, to convert it into D-FF, input T must be

| A $D \odot Q$

| B $D \oplus Q$

| C D

| D \bar{D}

Question (MCQ)



Which of the following is true?

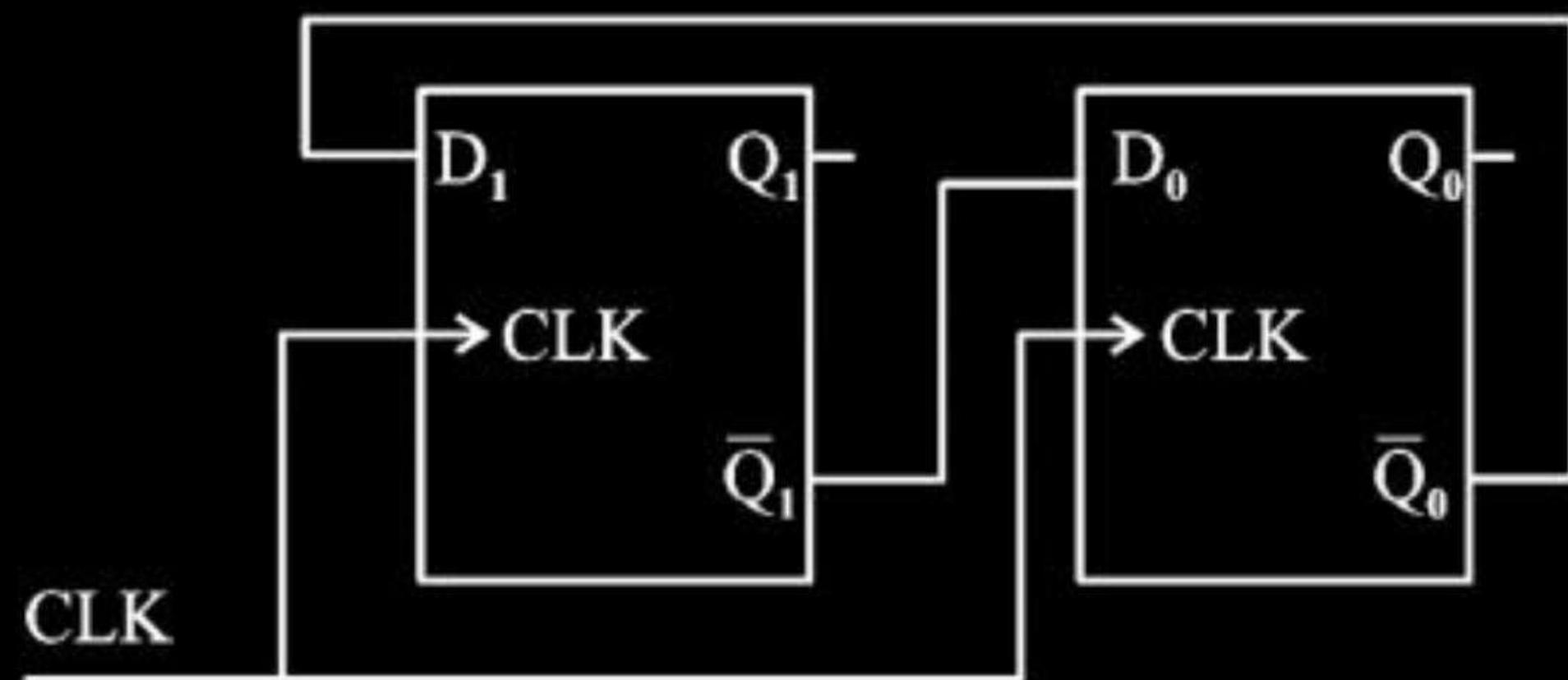
- A** Johnson counter has more unused states compared to ring counter
- B** Duty cycle in case of ring counter is $1/2n$.
- C** Duty cycle in case of Johnson counter is $1/2n$.
- D** MOD no. of Johnson counter = 2 MOD no. of ring counter.

Question

(NAT)



A sequential CKT is as given below:



Starting state of the counter is $Q_1Q_0 = (10)_2$. Its clock frequency is 5 MHz, then at o/p of Q_0 the frequency of the waveform is _____ MHz.

Question (MCQ)



2-bit Johnson counter generate the sequence:

$Q_1 Q_0$ [Q₁-MSB, Q₀ - LSB]:

| A 00-10-11-01-00

| B 00-11-10-01-00

| C 00-01-11-00

| D 00-11-01-10-00

Question (MCQ)

In a 3-bit Johnson counter, connections are interchanges as given below:

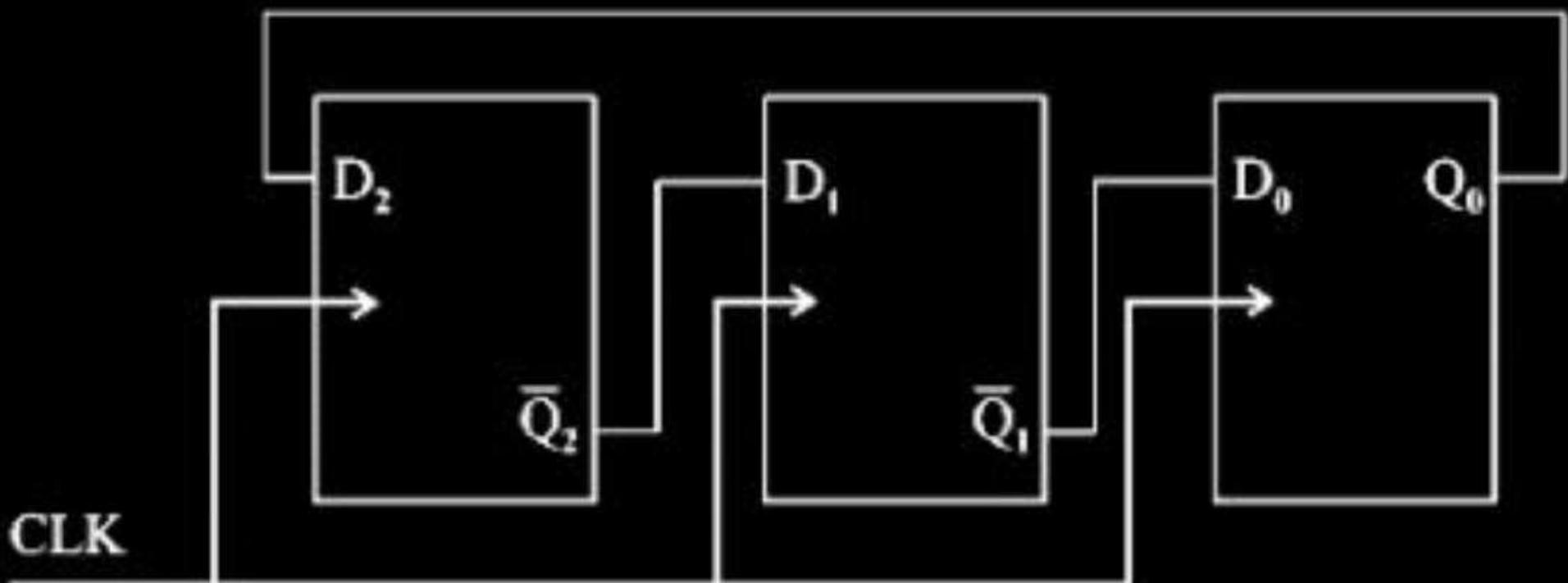
If starting state is $Q_2Q_1Q_0 = (100)_2$, the next state after applying clock will be:

A $(110)_2$

B $(001)_2$

C $(101)_2$

D $(000)_2$



Question (MCQ)



For 8-bit SISO register, to serially out the data from register, number of clock pulses required is

[A] 8

[B] 7

[C] 6

[D] 0

Question (MCQ)



The order of the speed of registers based on time taken to store the data and time taken to retrieve the stored data is:

- [A] SIPO > SISO > PISO > PIPO
- [B] PIPO > SIPO = PISO > SISO
- [C] SISO > SIPO = PISO > PIPO
- [D] PIPO > PISO > SIPO > SISO

Question (MCQ)

A SIPO register is connected as shown:

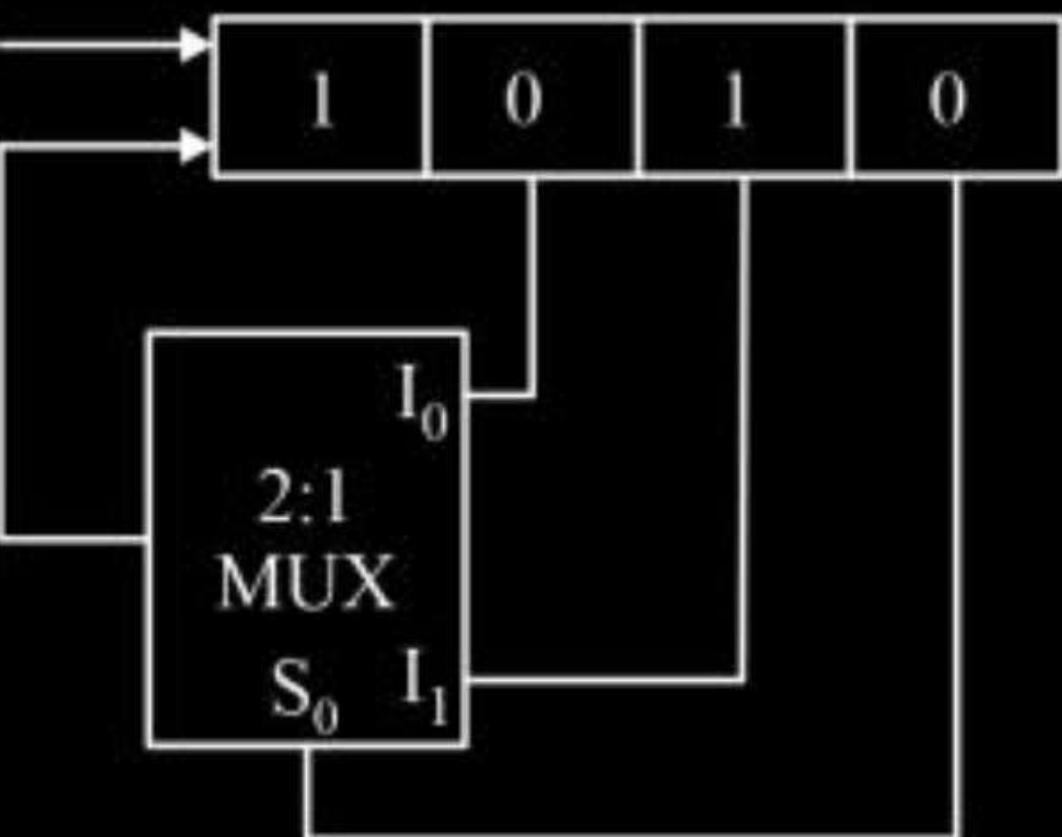
After three clock pulses output of register will be:

| A $(0010)_2$

| B $(0101)_2$

| C $(0001)_2$

| D $(1010)_2$



Question (MCQ)



In a 4-bit SIPO register has starting content of $(1100)_2$ as shown:

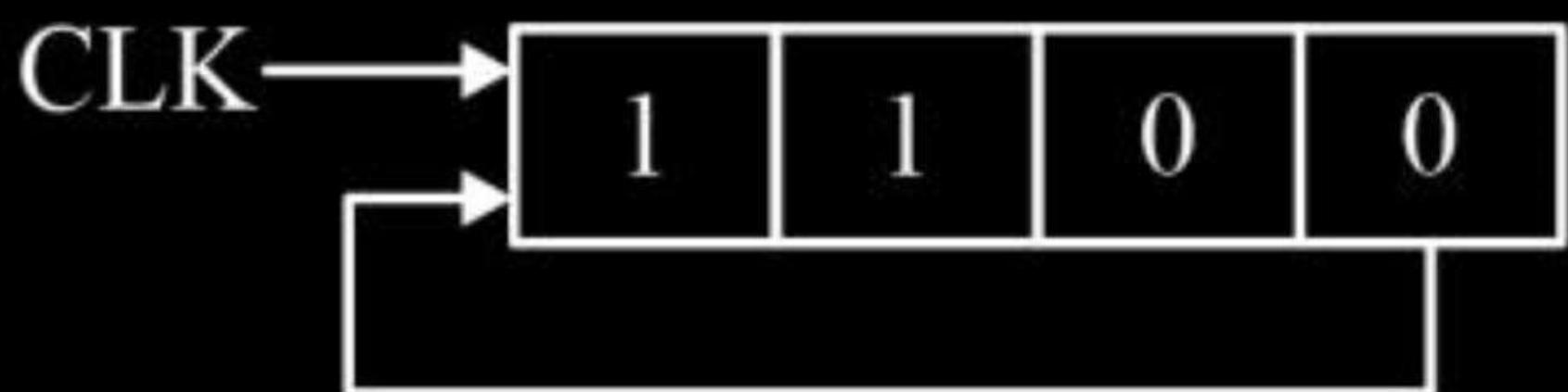
All the used FFs are replaced by T-FF then after 2 clock pulses the content of the register will be:

| A $(1010)_2$

| B $(1111)_2$

| C $(0000)_2$

| D None of these



Question (MCQ)



SISO register is an example of

- | A Asynchronous circuit (counter)
- | B Synchronous circuit (counter)
- | C Asynchronous circuit as well as synchronous circuit
- | D None of these

Question (MCQ)



Johnson counter is an example of

- | A Asynchronous counter
- | B Synchronous counter
- | C Asynchronous circuit as well as synchronous circuit
- | D None of these

Thank you
GW
Soldiers!



Electronics and Communication Engineering

COMPUTER SCIENCE



Digital Electronics

Lecture- 09

Digital Logic



By- CHANDAN JHA SIR



Topics to be Covered

1. Analog to Digital Converters
2. Digital to Analog Converters

ADC.

$$\text{Resolution} = \frac{V_r}{2^{n-1}}$$

$V_r \rightarrow$ Reference Voltage

$n \rightarrow$ no. of bits

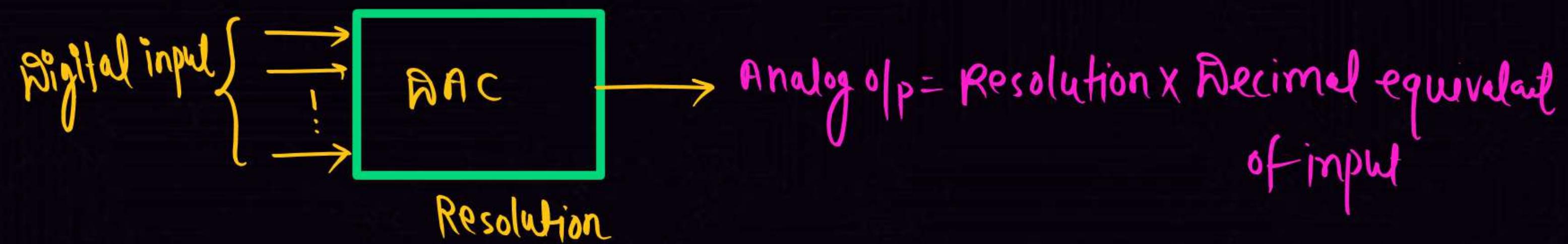
$$\% \text{ Resolution} = \frac{R}{V_{FS}} \times 100$$

$V_{FS} \rightarrow$ Full scale Voltage

$$\% R = \frac{1}{2^{n-1}} \times 100$$

$$V_{FS} \approx V_r$$

$$\% \text{ Accuracy} = \frac{\text{Error}}{V_{FS}} \times 100$$



Analog to Digital converter

① Counter type ADC [Ramp type ADC]

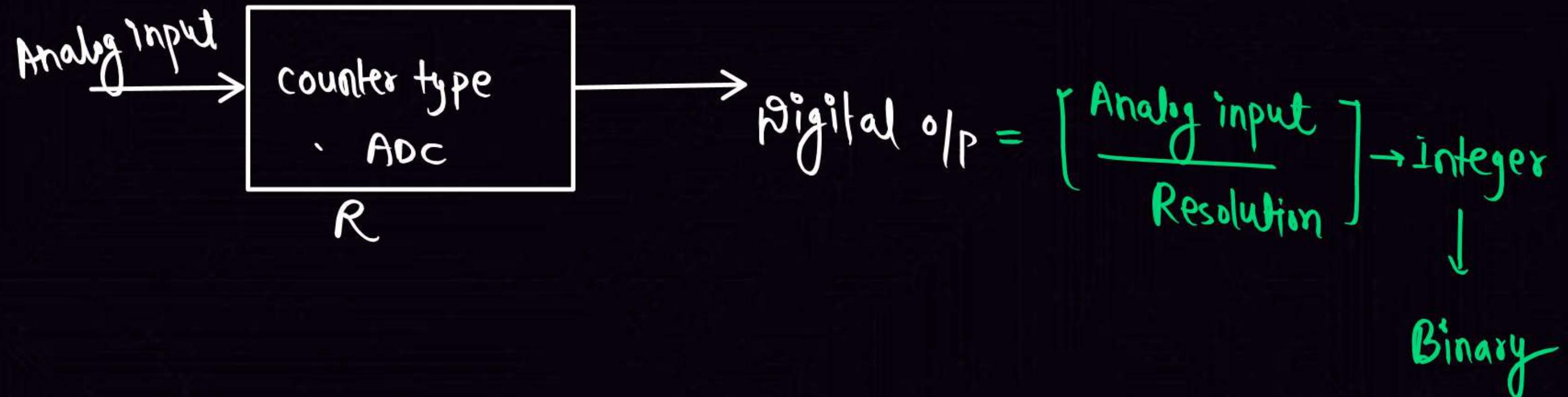
(a) conversion time depends on analog input,
analog input ↑ conversion time ↑

(b) minimum conversion time = $1 \cdot T_{clk}$

maximum conversion time = $(2^n - 1) \cdot T_{clk}$

Average conversion time = $(2^{n-1}) \cdot T_{clk}$

(c)



② Successive approximation Register type ADC (SAR)

(a) Conversion time is independant of analog input

(b) $\max = \min = \text{average} = \begin{cases} n \cdot T_{\text{clk}} & \text{without SOC \& EOC} \\ (n+2)T_{\text{clk}} & \text{with SOC \& EOC} \end{cases}$

③ Flash type ADC

(a) It is fastest ADC among all the ADC.

(b) No clock requirement.

(c) No. of comparators = $2^n - 1$

No of Resistors = 2^n

Encoder = $2^n \times n$ priority

④ Dual slope type ADC

- (a) It is also known 'integrator type ADC'.
- (b) It is slowest ADC among all the ADC but most accurate.
- (c) minimum conversion = $2^n \cdot T_{CK}$

$$\text{maximum conversion} = (2^{n+1})T_{CK}$$

Digital to analog converter

- ① Weighted Resistor type DAC
- ② R-2R type DAC

① Weighted Resistor type DAC

Analog Output = Resolution × Decimal Equivalent × Grain

$$\text{Resolution} = \frac{V_r}{2^{n-1}}$$

② R-2R type

Analog o/p = Resolution × Decimal Equivalent × Gain

$$\text{Resolution} = \frac{V_r}{2^n}$$

NOTE :- Only DAC mention.

Analog o/p = Resolution \times Decimal Equivalent \times Gain

$$\text{Resolution} = \frac{V_r}{2^n - 1}$$

Logic family

① Propagation Delay (τ_{pd})

↳ fastest



$\tau_{pd} = \frac{\tau_{PHL} + \tau_{PLH}}{2}$

Emitter coupled logic

② Power dissipation

$$P_{diss} = V_{CE} \times I_{cavg}$$

Less $P_{diss} \rightarrow$ CMOS

③ Figure of Merit (FOM)

↳ speed power product

$$FOM = \tau_{pd} \times P_{diss}$$



$I^2L \rightarrow$ Integrated Injected Logic

Best FOM

④ Fanout :-

→ Number of logic driven by similar type of Logic are called Fanout.

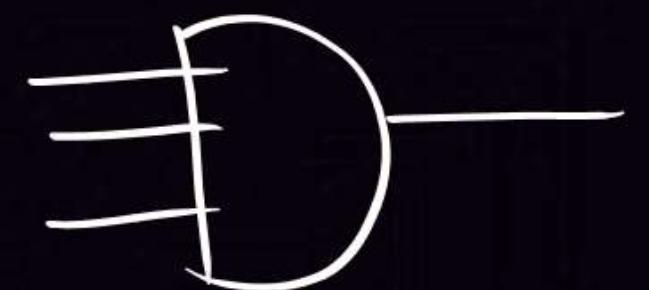
Largest → CMOS.

⑤ Fan in :-

→ Number of input terminal



$\text{Fanin} = 2$



$\text{Fanin} = 3$

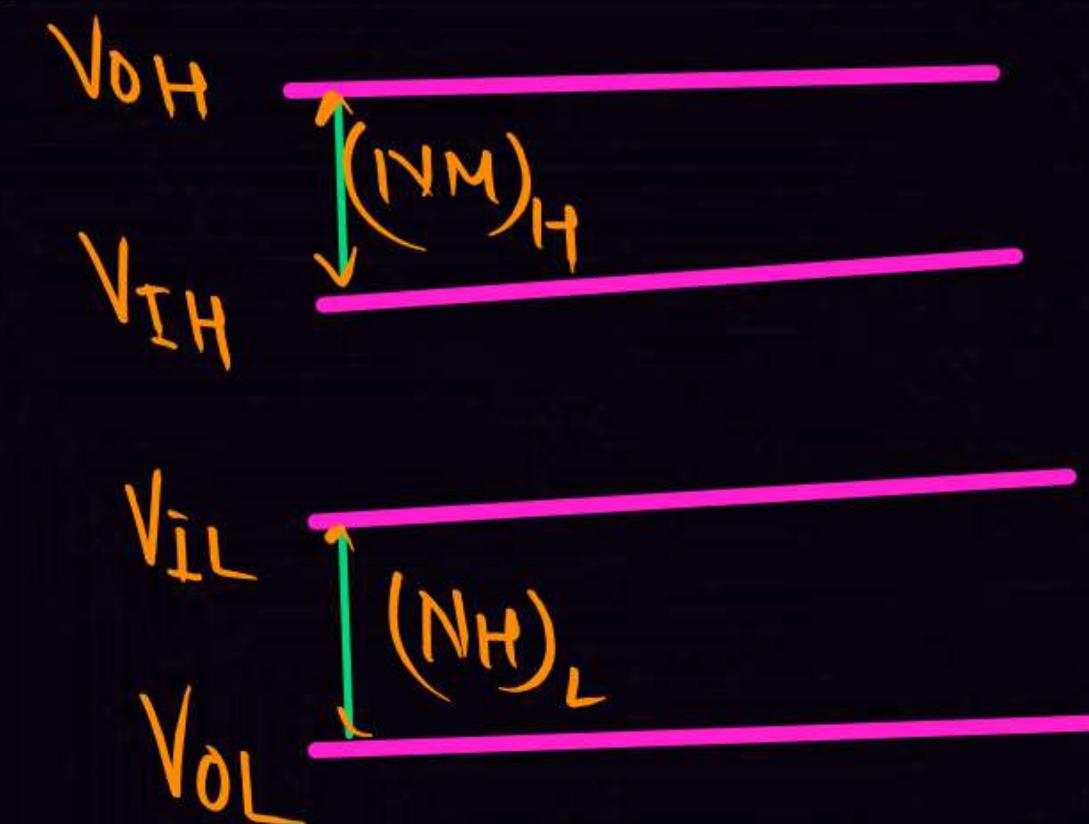
⑥ Noise Margin :-

Best Noise Margin \rightarrow HTL

High threshold Logic

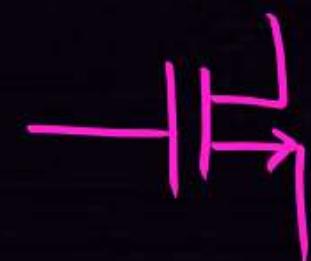
Maximum noise added to the input which will not affect the output are called Noise Margin.

$$\text{V}_{OH} > \text{V}_{IH} > \text{V}_{IL} > \text{V}_{OL}$$



$$\left\{ \begin{array}{l} (\text{NM})_H = \text{V}_{OH} - \text{V}_{IH} \\ (\text{NM})_L = \text{V}_{IL} - \text{V}_{OL} \\ \text{NM} = \text{Min} \{ (\text{NM})_H, (\text{NM})_L \} \end{array} \right.$$

N-MOS



input = 1 ON \rightarrow S.C

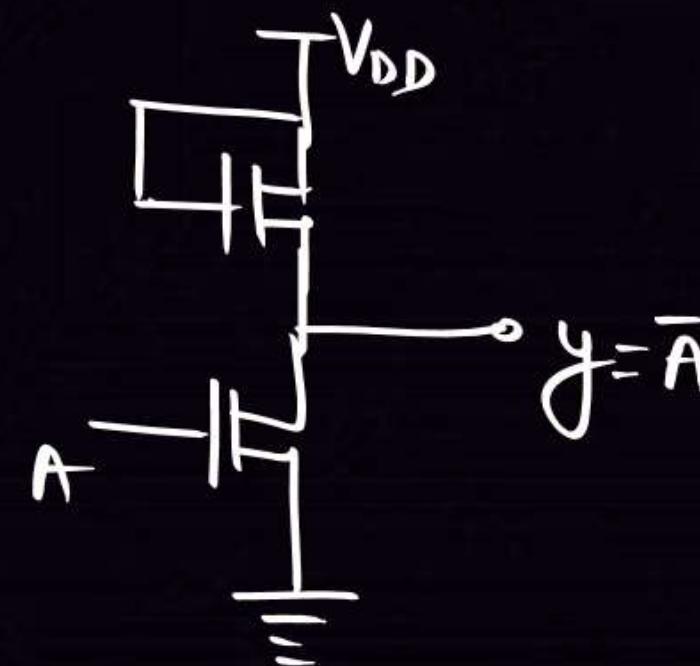
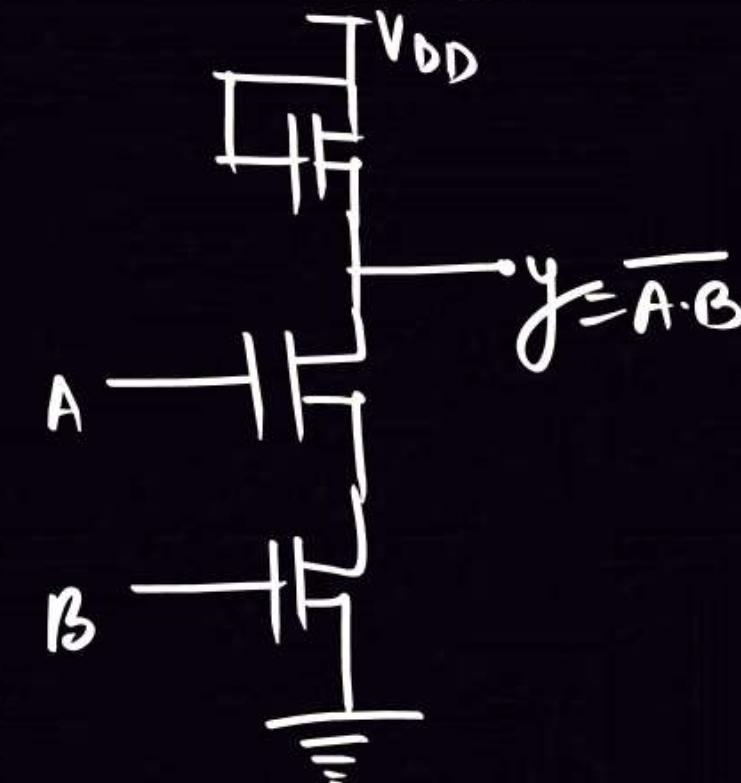
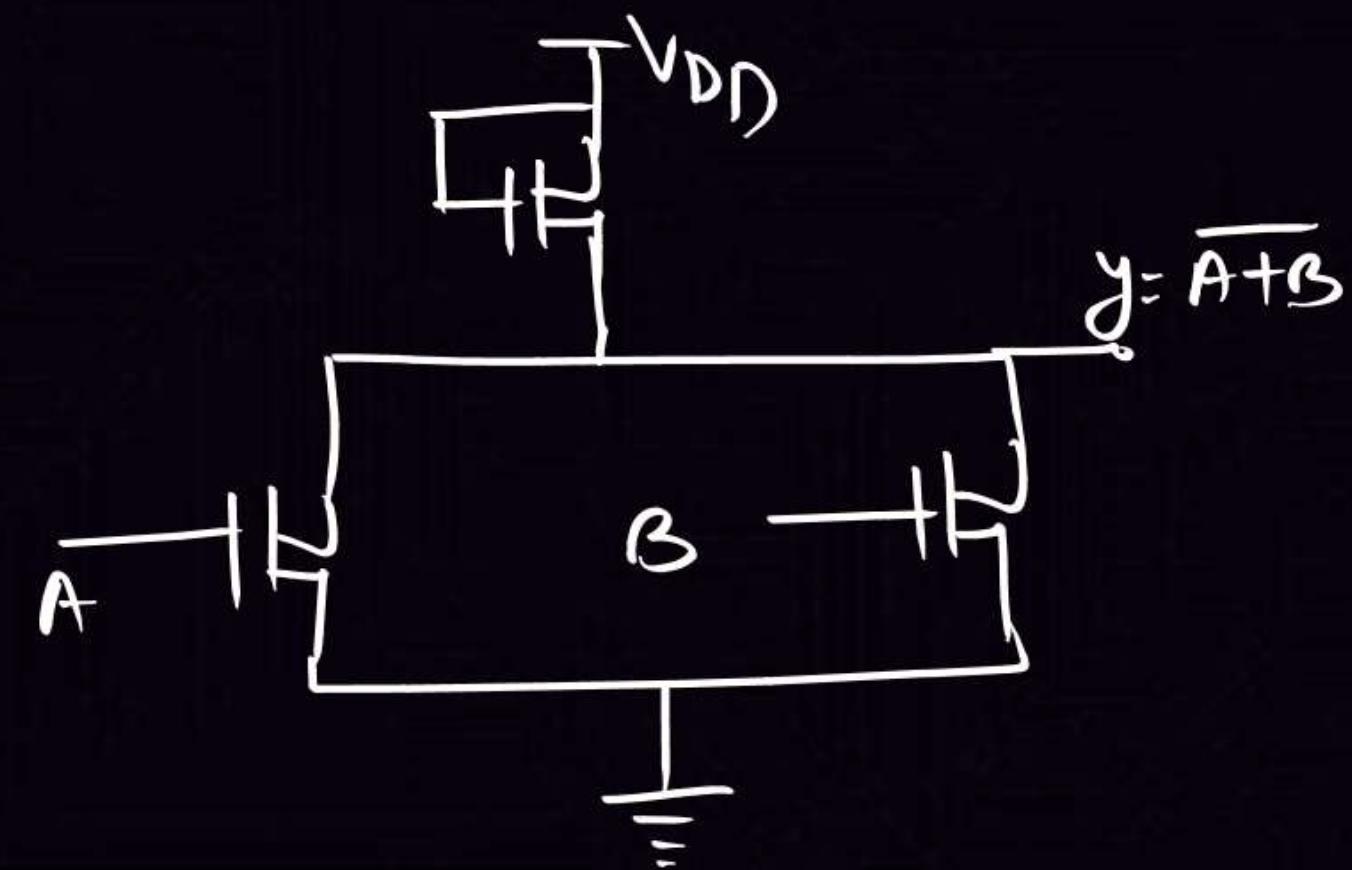
input = 0 OFF \rightarrow O.C

P-MOS



input = 1 OFF \rightarrow O.C

input = 0 ON \rightarrow S.C

NOT GATE.NAND GATE.NOR GATE.

#Q. The A/D converter used in a digital voltmeter could be (1) successive approximation type (2) Flash converter type (3) Dual slope converter type. The correct sequence in the increasing order of their conversion times is

- (a) 1, 2, 3
- ~~(b) 2, 1, 3~~ 2, 1, 3
- (c) 3, 2, 1 ✗
- (d) 3, 1, 2 ✗

#Q. Number of comparators needed to build a 6-bit simultaneous A/D converter is

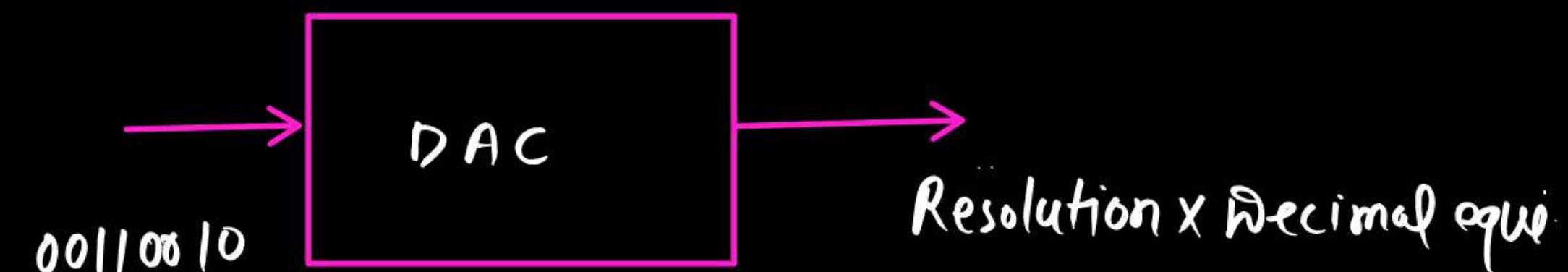
- (a) 63
- (b) 64
- (c) 7
- (d) 6

Flash type ADC

$$\begin{aligned}\text{comparator} &= 2^n - 1 \\ &= 2^6 - 1 \\ &= 64 - 1 \\ &= \underline{\underline{63}}\end{aligned}$$

#Q. The 8 bit DAC produces 1.0 V for a digital input of 00110010. What is the largest output it can produce?

- (a) 5 V
- (b) -5 V
- (c) 5.5 V
- (d) ~~5.10 V~~



$$\begin{aligned}
 & 32 + 16 + 2 \\
 & 50 \rightarrow 1V \\
 & \downarrow \\
 & 1111111 \\
 & 255 \rightarrow \frac{1}{50} R \\
 & \frac{1}{50} \times 255 V = 5.1 V
 \end{aligned}$$

#Q. The fastest ADC among the following is

- (a) Successive approximation type
- (b) Dual slope type
- (c) Sigma-Delta ADC
- ~~(d) Flash Converter~~

#Q. The number of comparators required in an 8-bit flash type A/D converter is

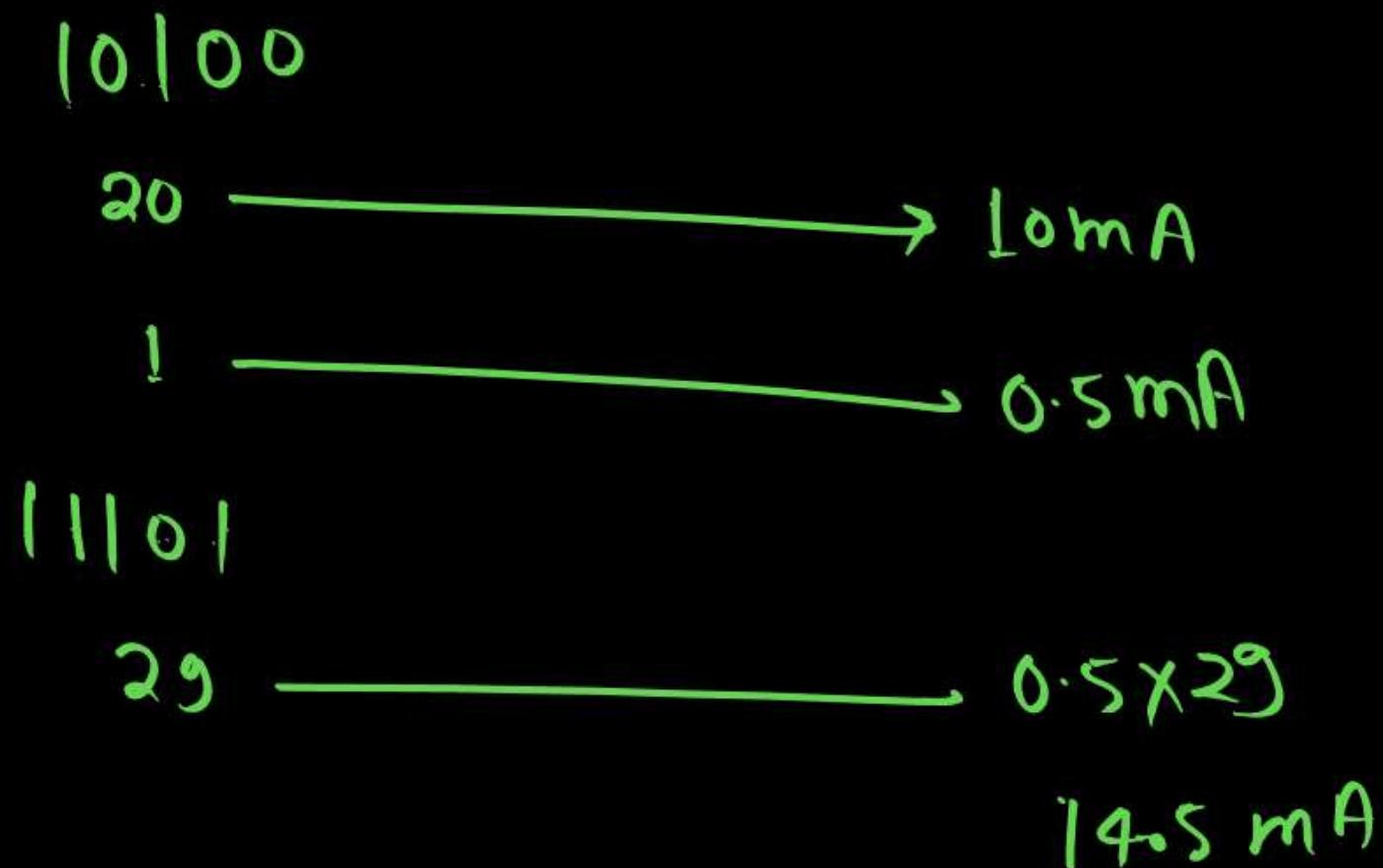
- (a) 256
- (b) 255
- (c) 9
- (d) 8

$$2^n - 1$$
$$2^8 - 1 = 255$$

(B)

#Q. A 5 bit DAC has a current output. For a digital input of 10100, an output current of 10 mA is produced. What will be the output current for a digital input of 11101?

- (a) 14.5 mA
- (b) 10 mA
- (c) 100 mA
- (d) Not possible to calculate



#Q. A 12 bit ADC is operating with $1 \mu\text{s}$ clock period and the total conversion time is seen to be $14 \mu\text{s}$. The ADC must be of

- (a) Flash type
- (b) Counting type
- (c) Integrating type
- ~~(d)~~ Successive approximation type

#Q. The number of comparators needed in a 8-bit flash type A to D converter is

- (a) 8
- (b) 16
- ~~(c) 255~~
- (d) 256

$$2^{n-1} = 2^8 - 1 = 256 - 1$$

= 255

#Q. A 10-bit DAC has a step size of **10 mV**. What is its Full scale output voltage and the percentage resolution?

- (a) 10.24 V, 0.2%
- (b) 10.23 V, 0.5%
- (c) 10.23 V, 0.1%
- (d) 10.24 V, 0.1%

$$R = \frac{V_{FS}}{2^{n-1}}$$

$$10\text{mV} \times 2^{10-1} = V_{FS}$$

$$10 \times 10^3 \times 2^{10-1} = V_{FS}$$

$$10 \times 10^3 \times 1023$$

$$\underline{10.23V}$$

$$\therefore R = \frac{1}{2^{10-1}} \times 10^3$$

$$= \frac{1}{1023} \times 10^3$$

$$= 0.999V$$

#Q. For a 10-bit digital ramp ADC using **500 kHz clock**, the maximum conversion time is

- (a) 2048 μ s
- (b) 2064 μ s
- (c) 2046 μ s
- (d) 2084 μ s

$$\tau_{clk} = \frac{1}{500} \cdot 10^{-3}$$

$$\tau_{clk} = \underline{\underline{2 \mu s}}$$

$$\begin{aligned} \text{max} &\Rightarrow (2^n - 1) \tau_{clk} \\ &= (2^{10} - 1) \times 2 \mu s \\ &= 1023 \times 2 \mu s \\ &= 2046 \mu s \end{aligned}$$

#Q. The resolution of a 12 bit Analog to Digital converter in percent is

- (a) 0.01220
- (b) 0.02441
- (c) 0.04882
- (d) 0.09760

$$\% R = \frac{1}{2^n - 1} \times 10^4$$

$$\therefore \frac{1}{2^{12} - 1} \times 10^4$$

#Q. What is the analog output for a 4-bit R-2R ladder DAC when input is $(1000)_2$,
for $V_{ref} = 5 \text{ V}$?

- (a) 2.3333 V
- (b) 2.4444 V
- ~~(c) 2.5556 V~~
- (d) 2.6667 V

$$\begin{aligned}V_0 &= R \times D \times G \\&= R \times D \\&= \frac{V_r}{2^n} \times B \\&= \frac{5}{2^4} \times 8 = 2.5 \\&=\end{aligned}$$

#Q. A analog output voltage for the input 1001 to a 4-bit D/A converter for all possible inputs assuming the proportionality factor $K = 1$ will be

- (a) 9
- (b) 6
- (c) 3
- (d) 1

$$\begin{array}{ccc} 1001 & \xrightarrow{\quad} & K \times D \\ D(9) & \xrightarrow{\quad} & 1 \times 9 = 9V \end{array}$$

#Q. What is the value of the full scale output for an 8-bit digital to analog converter for 0 V to 10 V range ?

- (a) 6.961 V
- (b) 7.891 V
- (c) 8.961 V
- ~~(d)~~ 9.961 V

$$R = \frac{10}{2^8} = \frac{10}{256}$$

1111111

255

$$V_d = R \times D$$

$$= \frac{10}{256} \times 255$$

$$= 9.961 V$$

#Q. An analog voltage of 3.41 V is converted into 8-bit digital form by an A/D converter with a reference voltage of 5 V. The digital output is

- (a) ~~1001 1001 1~~ X
- (b) ~~1111 0001~~ X
- (c) ~~1011 0111~~ X
- (d) ~~128 32 8 4 2~~
~~1010 1110~~ ✓

$$R = \frac{5}{2^8 - 1} = \frac{5}{255}$$

$$\frac{V_a}{R} = \frac{3.41}{R} = \frac{3.41 \times 255}{5}$$

$$= 173.91 \Rightarrow \overline{174}$$

Binary

#Q. A 12-bit ADC is operating with a $1 \mu\text{s}$ clock period and total conversion time is seen to be $14 \mu\text{s}$. The ADC must be of

- (a) Flash type
- (b) Counting type
- (c) Integrating type
- ~~(d)~~ Successive approximately type

#Q. A 12-bit A/D converter has a full-scale analog input of 5 V. Its resolution is

- (a) 1.22 mV
- (b) 2.44 mV
- (c) 3.66 mV
- (d) 4.88 mV

$$R = \frac{V_F}{2^n}$$

$$R = \frac{V_{FS}}{2^n}$$

$$R = \frac{5}{2^{12}} = 1.22\text{mV} \checkmark$$

#Q. An 8-bit DAC produces $V_{out} = 0.05$ V for a digital input of 00000001. The full scale output will be nearly

- (a) 12.8 V
- (b) 17.8 V
- (c) 22.8 V
- (d) 27.8 V

$$R = 0.05$$

1111111

255

$$0.05 \times 255$$

#Q. The resolution of 6-bit DAC will be nearly

- (a) 4.6%
- (b) 3.2%
- (c) 1.6%
- (d) 1.2%

$$\% R = \frac{1}{2^n - 1} \times 10^0$$

$$= \frac{1}{2^6 - 1} \times 10^0 \\ = \frac{1}{63} \times 10^0 = 1.587\%$$

Thank you
GW
Soldiers!

