

OVERALL ANALYSIS

Solution Report

All

Correct Answers

Wrong Answers

Not Attempted Questions

Q.1)

Suppose we want to read 5000 bytes in programmed I/O mode of transfer, where the bus width is 16 bits. Each time an interrupt occurs, it takes 10 microseconds to service it (i.e. transfer 16 bits). The CPU time required to read 5000 bytes is milliseconds.

Max Marks: 1

Correct Answer

Solution: (25)

Answer: is 25 milliseconds.

Explanation:

2 byte transfer requires a minimum of 10 microseconds.
So, 5000 bytes transfer will require: $10 / 2 * 5000 = 25,000$ microseconds
= 25 milliseconds.

Q.2)

Suppose we have a memory and a direct-mapped cache with the following characteristics.

Memory is byte addressable

Memory addresses are 16 bits (i.e., the total memory size is $2^{16} = 65536$ bytes)

The cache has 8 rows (i.e., 8 cache lines)

Each cache row (line) holds 16 bytes of data

If 16 address bits are allocated to the offset, index, and tag parts of the address used to reference the cache, then the number of bits in offset, index, and tag respectively

Max Marks: 1

A

9,3 and 4

B

4,3 and 9

Correct Option

Solution: (B)

Answer:B

Explanation:

The cache has 8 rows (i.e., 8 cache lines) \Rightarrow 3 bits for identifying the block
Each cache row (line) holds 16 bytes of data \Rightarrow 4 bits are required for offset

16 bit Address

Tag Bits	Index	Offset
9	3	4

Offset-4, index-3, Tag-9

C

4,9 and 3

D

4,4 and 8

Q.3)

Suppose that in 1000 memory references there are 40 misses in L1 cache and 10 misses in L2 cache. If the miss penalty of L2 is 200 clock cycles, hit time of L1 is 1 clock cycle, and hit time of L2 is 15 clock cycles, the average memory access time will be clock cycles. Assume that cache follows the global missrate.

Max Marks: 1

Correct Answer

Solution: (1.68)

$$\begin{aligned} \text{AMAT} &= 1 + 0.04^*(15 + 0.01*200) \\ &= 1 + 0.04*(17) \\ &= 1 + 0.68 \\ &= 1.68 \end{aligned}$$

Q.4)

Which of the following is false for interrupt-driven data transfer?

Max Marks: 1

A

It is faster than asynchronous data transfer.

B

It is slower than DMA mode of data transfer.

C

An interrupt signal can arrive at specific times.

Correct Option

Solution: (C)

Answer: C

Explanation:

Since in interrupt-driven data transfer, the CPU does not have to check the status of the I/O device continuously, the data transfer rate is faster than asynchronous transfer. However, a program needs to be executed (the interrupt service subroutine) that limits the maximum speed of transfer; hence it is slower than DMA where no program execution is involved.

An interrupt signal can arrive any time (not at specific times), but is typically acknowledged at the end of the instruction cycle.



Typically, an interrupt is acknowledged after completion of the instruction that is being executed by the CPU.

Q.5)

Max Marks: 1

We know that some versions of the Pentium 4 microprocessor have two 8 Kbyte, Level 1 caches – one for data and one for instructions. However, a design team is considering another option – a single, 16 Kbyte cache that holds both instructions and data.

Additional specs for the 16 Kbyte cache include:

- Each block will hold 32 bytes of data (not including tag, valid bit, etc.)
- The cache would be 2-way set associative
- Physical addresses are 32 bits
- Data is addressed to the word and words are 32 bits

Then the number of bits are required for the TAG bits with each block entry?



16



20



21

Correct Option

Solution: (c)**Answer:** C**Explanation:**

Cache size = 16KB

Each cache block can hold 32B

Number of blocks in cache is = 16KB / 32B = 1024/2 = 512

Index:

Given 2-way set associative cache

Number of sets = 512/2 = 256 Sets

Number of bits = 8

Offset:Data is addressed to the word and words are 32 bits \Rightarrow 1 word = 4B

Number of words in a block = 32B / 4B = 8

Number of bits required = 3

Therefore 3 bits of offset

Physical addresses are 32 bits

Number of TAG bits are $32 - (8+3) = 21$

Tag Bits	Index	Offset
21	8	3



17

Q.6)

Max Marks: 1

If a direct mapped cache has a hit rate of 95%, a hit time of 4 ns, and a miss penalty of 100 ns. If replacing the cache with a 2-way set associative increases the hit rate to 97%, but increases the hit time to 5 ns, what is the new AMAT?



Correct Answer

Solution: (8)**Answer:** 8**Explanation:**AMAT = Hit time + Miss rate \times Miss penalty = 5 + 0.03 \times 100 = 8 ns**Q.7)**

Max Marks: 1

A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Then the number of bits required for the tag, offset, Index respectively



10,7 and 2



10,2 and 7



8, 4 and 7



8, 7 and 4

Correct Option

Solution: (D)**Answer:** D**Explanation:**

The cache is divided into 16 sets of 4 lines each. Therefore, 4 bits are needed to identify the set number.

Main memory consists of $4K = 2^{12}$ blocks. Therefore, the set plus tag lengths must be 12 bits and therefore the tag length is 8 bits. Each block contains 128 words. Therefore, 7 bits are needed to specify the word

Tag bits 8, offset 7 and set 4bits

Main memory address	TAG	SET	WORD
	8	4	7

Q.8)

Which of the following statements is true for cache misses?

Max Marks: 1

- A Compulsory miss can be reduced by decreasing the cache block size.
- B Capacity miss can be reduced by decreasing the total size of the cache.
- C Conflict miss can be reduced by decreasing the value of cache associativity.
- D Compulsory miss can be reduced by prefetching cache blocks.

Correct Option

Solution: (D)

Answer:D

Explanation:

Compulsory miss: when a block of main memory is trying to occupy fresh empty line of cache and the very first access to a memory Block that must be brought into cache is called compulsory miss

Capacity Miss: Capacity misses occur when the cache is too small to hold all concurrently used data.

Compulsory miss can be reduced by decreasing the cache block size. False

Capacity miss can be reduced by decreasing the total size of the cache. False

Conflict miss can be reduced by decreasing the value of cache associativity. False

Compulsory miss can be reduced by prefetching cache blocks. True

Q.9)

How is the address of the interrupt service routine (ISR) typically determined by the CPU?

Max Marks: 1

- A The CPU checks the status of the I/O devices to determine who has sent the interrupt.
- B The interrupting device pushes an identifying interrupt vector on the data bus upon receiving the INTA signal.

Correct Option

Solution: (B)

Answer: B

Explanation:

(a) is not practical for multiple interrupt sources. Also, the INTR is a single signal line; it cannot carry identification information. The common practice is to have the interrupting device put a unique interrupt vector on the data bus when the CPU acknowledges the interrupt.

- C The INTR signal contains a unique code for identification.
- D None of the above.

Q.10)

Here is a series of address references given as word addresses: 1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17. The number of misses for a two-way set-associative cache with one-word blocks and a total size of 16 words. Assume LRU replacement.

Max Marks: 1



Correct Answer

Solution: (12)

Explanation:

#of sets = 16 blocks /2blocks per set = 8

Address reference	Binary address	Hit/Miss	Assigned cache set
1	0001	Miss	001
4	0100	Miss	100
8	1000	Miss	000
5	0101	Miss	101
20	10100	Miss	100
17	10001	Miss	001
19	10011	Miss	011
56	111000	Miss	000
9	1001	Miss	001
11	1011	Miss	011
4	0100	Hit	100

45	101011	MISS	011
5	0101	Hit	101
6	0110	Miss	110
9	1001	Hit	001
17	10001	Hit	001

Q.11)

Max Marks: 2

Consider a computer with the following characteristics: total of 1Mbyte of main memory; word size of 1 byte; block size of 16 bytes; and cache size of 64 Kbytes. For the main memory address of CABBE, give the corresponding tag, cache line address, and word offsets for a direct mapped cache.

C,AB, BE

C,ABB, E

Correct Option

Solution: (B)

Answer:B

Explanation:

Because the block size is 16 bytes and the word size is 1 byte, this means there are 16 words per block. We will need 4 bits to indicate which word we want out of a block.

Each cache line/slot matches a memory block. That means each cache line contains 16 bytes. If the cache is 64Kbytes then 64Kbytes/16 = 4096 cache lines.

To address these 4096 cache lines, we need 12 bits ($2^{12} = 4096$).

Consequently, given a 20 bit (1 MByte) main memory address:

Bits 0-3 indicate the word offset (4 bits).

Bits 4-15 indicate the cache line/slot (12 bits).

Bits 16-19 indicate the tag (remaining bits).

CABBE = 1100 1010 1011 1011 1110

Tag = 1100 = C

Line = 1010 1011 1011 = ABB

Word offset = 1110 = E

Tag	Line	Offset
1100	1010 1011 1011	1110

CA,BB, E

None of these

Q.12)

Max Marks: 2

A computer system uses 16-bit memory addresses. It has a 2K-byte cache organized in a direct-mapped manner with 64 bytes per cache block. Assume that the size of each memory word is 1 byte. When a program is executed, the processor reads data sequentially from the following word addresses: 128, 144, 2176, 2180, 128, 2176 All the addresses are shown in decimal values. Assume that the cache is initially empty. For each of the above addresses, the number of hits are

Correct Answer

Solution: (2)

Answer: 2

Explanation:

Block size = 64 bytes = 2^6 bytes = 2^6 words (since 1 word = 1 byte)

Therefore, Number of bits in the Word field = 6

Cache size = 2K-byte = 2^{11} bytes

Number of cache blocks = Cache size / Block size = $2^{11}/2^6 = 2^5$

Therefore, Number of bits in the Block field = 5

Total number of address bits = 16

Therefore, Number of bits in the Tag field = $16 - 6 - 5 = 5$

For a given 16-bit address, the 5 most significant bits represent the Tag, the next 5 bits represent the Block, and the 6 least significant bits represent the Word.

Access # 1: Address = $(128)_{10} = (0000000010000000)_2$

(Note: Address is shown as a 16-bit number, because the computer uses 16-bit addresses) For this address, Tag = 00000, Block = 00010, Word = 000000 Since the cache is empty before this access, this will be a cache miss After this access, Tag field for cache block 00010 is set to 00000

Access # 2: Address = $(144)_{10} = (0000000010010000)_2$

For this address, Tag = 00000, Block = 00010, Word = 010000 Since tag field for cache block 00010 is 00000 before this access, this will be a cache hit (because address tag = block tag)

Access # 3: Address = $(2176)_{10} = (0000100010000000)_2$

For this address, Tag = 00001, Block = 00010, Word = 000000 Since tag field for cache block 00010 is 00000 before this access, this will be a cache miss (address tag ≠ block tag) After this access, Tag field for cache block 00010 is set to 00001

Access # 4: Address = $(2180)_{10} = (000010001000100)_2$

For this address, Tag = 00001, Block = 00010, Word = 000100 Since tag field for cache block 00010 is 00001 before this access, this will be a cache hit (address tag = block tag)

Access # 5: Address = $(128)_{10} = (0000000010000000)_2$

For this address, Tag = 00000, Block = 00010, Word = 000000 Since tag field for cache block 00010 is 00001 before this access, this will be a cache miss (address tag ≠ block tag)

tag) After this access, Tag field for cache block 00010 is set to 00000

Access # 6: Address = $(2176)_{10} = (0000100010000000)_2$

For this address, Tag = 00001, Block = 00010, Word = 000000 Since tag field for cache block 00010 is 00001 before this access, this will be a cache miss (address tag ≠ block tag) After this access, Tag field for cache block 00010 is set to 00001

Number of hits = 2

Q.13)

Max Marks: 2

Consider a machine with a byte addressable main memory of 2^{16} bytes and block size of 8 bytes. Assume that a direct mapped cache consisting of 32 lines is used with this machine. Into what line would bytes with each of the following address will be stored?
0001 0001 0001 1011

A

Line 3

Correct Option

Solution: (A)

Answer: A

Explanation:

Byte addressable main memory of 2^{16} bytes and block size is 8 bytes
Cache consisting of 32 lines to represent cache block bits required.

TAG	LINE	WORD
8	5	3

Given address is

0001 0001 0001 1011 $\Rightarrow (0001\ 0001)\ (00011)011$

First 3 bits from right to left will represent offset, next 5 bits will represent cache line number.

Total 32 cache lines, 00011 decimal equivalent is 3 $\Rightarrow 3 \bmod 32 = 3$

The given address will represent the 3rd line of the cache

B

Line 6

C

Line 17

D

None of these

Q.14)

Max Marks: 2

Consider three processors with three cache configurations:

Processor 1: Direct-mapped i-cache and d-cache with one-word blocks Instruction miss-rate = 4%, data miss-rate = 6%

Processor 2: Direct-mapped i-cache and d-cache with four-word blocks Instruction miss-rate = 2%, data miss-rate = 4%

Processor 3: Two-way set associative i-cache and d-cache with four-word blocks Instruction miss-rate = 2%, data miss-rate = 3%

For these processors, 50% of the instructions contain a data reference. Assume that the cache penalty is 6 + Block size in words. Determine which processor spends the most cycles on cache misses

A

Processor 1

Correct Option

Solution: (A)

Answer: A

Explanation:

For Processor 1: Miss penalty = 6 + 1 = 7 cycles

Stall cycles per instruction = $4\% \times 7 + 50\% \times 6\% \times 7 = 0.28 + 0.21 = 0.49$

For Processors 2: Miss penalty = 6 + 4 = 10 cycles

Stall cycles per instruction = $2\% \times 10 + 50\% \times 4\% \times 10 = 0.2 + 0.2 = 0.4$

For Processor 3: Miss penalty = 6 + 4 = 10 cycles

Stall cycles per instruction = $2\% \times 10 + 50\% \times 3\% \times 10 = 0.2 + 0.15 = 0.35$

Therefore, Processor 1 spends the most cycles on cache misses.

B

Processor 2

C

Processor 3

D

None of them

Q.15)

Max Marks: 2

Consider a memory system that uses a 32-bit address to address at the byte level, plus a cache that uses a 64-byte line size. Assume a four-way set-associative cache with a tag field in the address of 9 bits. Then the size of the cache memory (excluding tag memory) in terms of megabytes.

A

Correct Answer

Solution: (32)

Answer: 32

Explanation:

Address is 32 bits and byte addressable

Cache line size = 64byte,

6 bits required to represent the cache line

Given four-way set-associative cache with a tag field in the address of 9 bits

Number of index bits = $32 - (9+6) = 17$ bits

32 bit Address		
TAG	Index	Word/Offset
9	17	6

Number of set in the cache is 2^{17}

Each set contains 4 cache lines = 4

Number of cache lines are $2^{17} * 4 = 2^{19}$

Each cache line contains 64B

Total cache size = $2^{19} \times 64B = 2^{25} B = 2^5 MB = 32MB$

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