



Kunal Jha  
 Course: GATE  
 Computer Science Engineering(CS)

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## COMPUTER ORGANIZATION AND ARCHITECTURE + OPERATING SYSTEM (GATE - 2021) - REPORTS

OVERALL ANALYSIS    COMPARISON REPORT    **SOLUTION REPORT**

ALL(33)    CORRECT(0)    INCORRECT(0)    SKIPPED(33)

Q. 1

Have any Doubt?



For the processes listed in the following table, which of the following scheduling schemes will give the highest average Turn Around Time?

Process	Arrival Time	Processing Time
A	0	3
B	1	6
C	4	4
D	6	2

**A** First Come First Serve

**B** Non-preemptive shortest job first

**C** Both (a) and (b)

**D** Round Robin with quantum value two

Correct Option

Solution :

(d)

Turn around time is the total time taken between the submission of a program/process/thread/task (Linux) for execution and the return of the complete output to the customer/user.

Turn around Time = Completion Time - Arrival Time

FCFS = First Come First Serve (A, B, C, D)

SJF = Non-preemptive Shortest Job First (A, B, D, C)

RR = Round Robin with Quantum value 2 (A(2), B(2), A(1), C(2), B(2), D(2), C(2), B(2))

Process	Arrival Time	Processing Time	FCFS	SJF	RR
A	0	3	3 - 0 = 3	3 - 0 = 3	5 - 0 = 5
B	1	6	9 - 1 = 8	9 - 1 = 8	15 - 1 = 14
C	4	4	13 - 4 = 9	11 - 6 = 5	13 - 4 = 9
D	6	2	15 - 6 = 9	15 - 4 = 11	11 - 6 = 5
Average			7.25	6.75	8.25

Hence option (d) has highest average turn around time.

### QUESTION ANALYTICS



Q. 2

Solution Video

Have any Doubt?



How many tag bits are required for a system that has a main memory with 4 GB of addressable locations and a 256 KB direct mapped cache with 64 bytes per block.

**A** 12

**B** 13

**C** 14

Correct Option

Solution :

(c)

Cache memory size = 256 KB

Main memory size = 4 GB =  $2^{32}$  byte

Block size = 64 B

Number of blocks = Number of lines

$$= \frac{256 \text{ KB}}{64 \text{ B}} = \frac{2^{18}}{2^6} = 2^{12} \text{ blocks/cache}$$

And, 12 bits are needed for index/line

Word offset =  $\log(64 \text{ B}) = 6$  bits

Addressing main memory requires =  $\log(2^{32}) = 32$  bits

Tag bits required =  $32 - (12 + 6) = 14$  bits

Option (c) is correct.

**D** 15

### QUESTION ANALYTICS



Q. 3

Have any Doubt?



Consider an operating system capable of loading and executing a single sequential user process at a time. The disk head scheduling algorithm used is First Come First Served (FCFS). If FCFS is replaced by Shortest Seek Time First (SSTF), claimed by the vendor to give 50% better benchmark results, what is the expected improvement in the I/O

Q. 3 Which of the following is replaced by Shortest Job First (SJF), whenever it is used to give better benchmark results, where the expected improvement in the performance of user programs (in percentage)?

A 50%

B 0%

Correct Option

Solution :

(b)  
Since Operating System can execute a single sequential user process at a time, the disk is accessed in FCFS manner always.  
The OS never has a choice to pick an I/O from multiple I/Os as there is always one I/O at a time.

C 25%

D 75%

QUESTION ANALYTICS



Q. 4

Have any Doubt ?



Which is the correct relation between number of available resource( $r$ ), maximum number of resources needed by each process( $n$ ) and number of processes( $p$ ):

A  $r \geq p \times (n - 1) + 1$

Correct Option

Solution :

(a)  
The formula for  $r \geq p \times (n - 1) + 1$ , is the correct relation between  $n, p, r$ .

B  $r \geq p \times (n + 1) + 1$

C  $r > p \times (n - 1) + 1$

D  $r > p \times (n + 1) + 1$

QUESTION ANALYTICS



Q. 5

Have any Doubt ?



Given memory partition of 100 K, 500 K, 200 K, 300 K and 600 K in order, if we have processes needs memory of 212 K, 417 K, 112 K and 405 K respectively, which of the following memory allocation technique(s) will be suitable to allocate memory for all the processes?

A First fit

B Best fit

Correct Option

Solution :

(b)  
If we use First fit, then request 405 K can't be satisfy because the request of 212 K will go to the partition of 500 K and 417 K will go to 600K. So, the request for 405 K can't be satisfy by using first fit.  
If we use best fit then the request for all will be satisfied.  
Random fit is also not suitable because in that case nothing will be in your hand and this technique may select first fit algorithm which is not suitable for the given request as we have seen above.  
Using worst fit also request can't be satisfied because 212 K will go to 600 K, 417 K will go to 500 K, then 405 K can't be satisfied.

C Worst fit

D Random fit

QUESTION ANALYTICS



Q. 6

FAQ

Solution Video

Have any Doubt ?



Consider a reduced 7-bit IEEE floating-point format, with 3 bits for the exponent and 3 bits for the significand (Mantissa). What will be the value which get stored in the system corresponding to  $(-0.5625)$ ?

A 1010001

Correct Option

Solution :

(a)  
Here, Sign bit = 1  
Also,  $0.5625 = (0.1001)$   
For normalized form,  
 $0.5625 = 1.001 \times 2^{-4}$   
Hence, Actual Exponent = -4  
Biased Exponent = Actual Exponent + Bias  
Bias = Largest signed integer possible with 3 bits = 3  
Biased Exponent =  $-4 + 3 = 2$  (010)  
Therefore, Binary representation will be (1010001).

**B** 0101001

**C** 1010101

**D** 1001000

QUESTION ANALYTICS



Q. 7

? FAQ ▶ Solution Video ⚡ Have any Doubt ? 📖

Given stage1 (IF), stage2 (ID), stage3 (EX), stage4 (Memory access (MA)), stage5 (WB). Consider the following sequence of instructions in the program:

100 :  $I_1$

101 :  $I_2$  (JMP 200)

103 :  $I_3$

:

200 :  $BI_1$

What will be Output sequence of the above Instruction mention if there are any stalls?

**A**  $I_1 \rightarrow I_2 \rightarrow \text{Delay(Stall)} \rightarrow BI_1$

Correct Option

Solution :

(a)  
 $I_1 \rightarrow I_2 \rightarrow \text{Delay(Stall)} \rightarrow BI_1$  as JMP instruction is received after ID (if no stage is mentioned take ID) of 2nd instruction but before that  $I_3$  is fetched due to Control Dependency thus due to this a stall is introduced.

**B**  $I_1 \rightarrow I_3 \rightarrow \text{Delay(Stall)} \rightarrow BI_1$

**C**  $I_2 \rightarrow I_3 \rightarrow \text{Delay(Stall)} \rightarrow BI_1$

**D**  $I_1 \rightarrow I_2 \rightarrow \text{Delay(Stall)} \rightarrow I_3$

QUESTION ANALYTICS



Q. 8

? FAQ ⚡ Have any Doubt ? 📖

Consider a system having demand paged system, where integers are stored in 4 bytes, page size is 256 bytes. Consider the below program.

```
int a[200] [200];
int i = 0;
int j = 0;
while (i + + < 200)
{
    J = 0;
    while(j++ < 200)
        a[i][j] = 0;
}
```

How many pages are needed to store the elements of an array?  
(Assuming all elements of the array are stored in contiguous memory location?)

**A** 1000

**B** 500

**C** 625

Correct Option

Solution :

(c)  
Number of elements =  $200 \times 200$   
Memory needed =  $200 \times 200 \times 4 \text{ B}$   
Number of pages needed =  $\frac{160000 \text{ B}}{256 \text{ B}} = 625$

**D** 450

QUESTION ANALYTICS



Q. 9

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The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds.  
The throughput increase of the pipeline is \_\_\_\_\_ %. (Upto 2 decimal places)

**C** 33.33 [33.30 - 33.35]

Correct Option

Solution :

33.33 [33.30 - 33.35]

Old design  
New design

$$\text{Throughput} = \frac{\left(\frac{1}{600}\right) - \left(\frac{1}{800}\right)}{\left(\frac{1}{800}\right)} = 33.33\%$$

QUESTION ANALYTICS



Q. 10

FAQ Solution Video Have any Doubt ?



Consider a machine with a byte addressable and 4 GB main memory divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache lines is used with this machine. The size of the tag field in bits is \_\_\_\_\_.

18

Correct Option

Solution :

18

$$\text{Number of blocks of main memory} = \frac{2^{32}}{2^5} = 2^{27}$$

$$\text{Number of lines in cache memory} = 512 = 2^9$$

So, number of TAG bits required =  $27 - 9 = 18$  bits.

QUESTION ANALYTICS



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Q. 11

Solution Video

Have any Doubt ?



Consider two processors  $P_1$  and  $P_2$  executing the same instruction set. Assume that under identical conditions, for the same input, a program running on  $P_2$  takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on  $P_1$ .

If the clock frequency of  $P_1$  is 1 GHz, then the clock frequency of  $P_2$  (in GHz) is \_\_\_\_\_. (Upto 1 decimal place)

1.6

Correct Option

**Solution :**

1.6

$$\text{1 cycle time for } P_1 = \frac{10^9}{1 \text{ GHz}} = 1 \text{ ns}$$

Assume  $P_1$  takes 5 cycles for a program then  $P_2$  takes 20% more means, 6 cycles.

$P_2$  Takes 25% less time means, if  $P_1$  takes 5 ns, then  $P_2$  takes 3.75 ns.

Assume  $P_2$  clock frequency is  $x$  GHz.

$$P_2 \text{ taken 6 cycles, so } \frac{6 \times 10^9}{x \text{ GHz}} = 3.75. \text{ i.e. } x = 1.6$$

QUESTION ANALYTICS



Q. 12

Solution Video

Have any Doubt ?



A hard disk with a transfer rate of 10 MB/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively.

If the size of the transfer is 20 KB, what is the percentage of processor time consumed for the transfer operation is \_\_\_\_\_. (Upto 1 decimal place)

0.1

Correct Option

**Solution :**

0.1

$$\text{Clock cycle time} = \frac{1}{600} \times 10^6$$

$$\text{For DMA initiation and completion} = \frac{900 + 300}{600 \times 10^6} = 2 \mu\text{s}$$

$$\text{Disk Transfer rate} = 10 \text{ MB/s}$$

$$\text{For 20 KB} = \frac{20 \text{ KB}}{10 \text{ MB}} = 2 \text{ ms} = 2000 \mu\text{s}$$

$$\text{Processor time consumed} = \frac{2}{2000} \times 100 = 0.1\%$$

QUESTION ANALYTICS



Q. 13

? FAQ    Solution Video

Have any Doubt ?



Consider a 4-stages pipeline with respective stage delays of (10 ns, 5 ns, 20 ns and 15 ns). What is the efficiency of the pipeline when the number of tasks are significantly larger than the number of stages \_\_\_\_%. (Upto 1 decimal place)

62.5

Correct Option

**Solution :**

62.5

$$\text{Efficiency} = \frac{\text{Given speed up}}{\text{Max speed up}} = \frac{S}{S_{\max}}$$

When the number of tasks 'n' are significantly larger than k, that is,  $n \gg k$

$$S_{\max} = K$$

$$S = \frac{10 + 5 + 20 + 15}{20} = 2.5$$

$$M = \frac{S}{K} = \frac{2.5}{4} = 62.5\%$$

QUESTION ANALYTICS



Q. 14

? FAQ

Have any Doubt ?



Which of the following is/are shared by all the threads in a process?

Child processes

Correct Option

B Pending alarms

Correct Option

C State

D Registers

YOUR ANSWER - NA

CORRECT ANSWER - a,b

STATUS - SKIPPED

**Solution :**

(a,b)

- I. Threads share:
  - Address space
  - Heap
  - Static data
  - Code segments
  - File descriptors
  - Global variables
  - Child processes
  - Pending alarms
  - Signals and signal handlers
  - Accounting information
- II. Threads have their own:
  - Program counter
  - Registers
  - Stack
  - State

Option (d) is correct.

QUESTION ANALYTICS



Q. 15

? FAQ

Have any Doubt ?



Consider the following statement regarding CISC computer with respect to RISC. Which of the following is/are true?

A It supports more addressing modes.

Correct Option

B It contains large instruction set.

Correct Option

C It is more suitable for general purpose system.

Correct Option

D It has more number of registers.

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

**Solution :**

(a, b, c)

All the statement are true except last one regarding CISC system as they support encoded form of control signal and they are cost effective.  
RISC structure has more number of registers.

QUESTION ANALYTICS



Q. 16

? FAQ

Have any Doubt ?



Consider the following Scheduling Strategies. Which of the following do not suffers from starvation?

A Longest Job First Scheduling

Correct Option

B Longest Remaining Time First Scheduling

Correct Option

C Shortest Job First Scheduling

D First Come First Serve Scheduling

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - b,d

STATUS - SKIPPED

**Solution :**

(b, d)

Longest remaining time first do not suffer from starvation as if longer process keep on coming, then memory will be full.  
First Come First Serve do not suffers from starvation because fixed time bound exist for execution of each process.

QUESTION ANALYTICS



Q. 17

Have any Doubt ?



A virtual memory system uses First In First Out (FIFO) page replacement policy and allocates a fixed number of frames to a process. Consider the following statements:

P : Increasing the number of page frames allocated to a process sometimes increases the page fault rate.  
Q : Some programs do not exhibit locality of reference.  
Which one of the following is TRUE?

A P, Q true and Q is the reason for P.

B P true and Q false.

C P, Q true and Q is not the reason for P.

Correct Option

Solution :

(c)  
Belady's Anomaly proves that it is possible to have more page faults when increasing the number of page frames while using the First In First Out (FIFO) page replacement algorithm.  
Locality of reference, also known as the principle of locality, is the phenomenon of the same value of related storage locations being frequently accessed.  
Both P and Q are true but Q is not the cause for P as page fault is related to pages present in frame not with pages nearly the page accessed recently.

D P false and Q true.

QUESTION ANALYTICS



Q. 18

? FAQ

▶ Solution Video

⌚ Have any Doubt ?



A cache has a hit rate of 95%, 128-byte lines, and a cache hit latency of 5 ns. The main memory takes 100 ns to return the first word (32 bits) of a line, and 10 ns to return each subsequent word. What is the Cache miss penalty of this system? (Assume that the cache waits until the line has been fetched into the cache and then re-executes the memory operation).

A 400 ns

B 410 ns

C 415 ns

Correct Option

Solution :

(c)  
In case of a miss, cache line is 128 bytes and main memory takes 100 ns to return the first word (32 bits) of a line, and 10 ns to return each subsequent word, therefore for first 4 bytes it takes 100 ns and for subsequent 124 bytes i.e. 31 words it takes  $31 \times 10 = 310$  ns.  
Therefore, Cache miss penalty = time taken to fetch a line from MM to cache + time taken to re-execute the operation  
 $= (100 + 310) \text{ ns} + 5 \text{ ns} = 415 \text{ ns}$

D 420 ns

QUESTION ANALYTICS



Q. 19

? FAQ

⌚ Have any Doubt ?



A single processor system has three resource types X, Y and Z, which are shared by three processes. There are 5 units of each resource type. Consider the following scenario, where the column alloc denotes the number of units of each resource type allocated to each process, and the column request denotes the number of units of each resource type requested by a process in order to complete execution. Which of these processes will finish LAST?

	Alloc	Request
$P_0$	X Y Z 1 2 1	X Y Z 1 0 3
$P_1$	2 0 1	0 1 2
$P_2$	2 2 1	1 2 0

A  $P_0$

B  $P_1$

C  $P_2$

Correct Option

Solution :

(c)  
(5, 4 and 3 instances of X, Y and Z respectively) are allocated, 0, 1 and 2 instances of X, Y and Z are left. Only needs of  $P_1$  can be satisfied. So  $P_1$  can finish its execution first. Once  $P_1$  is done, it releases 2, 1 and 3 units of X, Y and Z respectively. Among  $P_0$  and  $P_2$ , needs of  $P_0$  can only be satisfied. So  $P_0$  finishes its execution.  
Finally,  $P_2$  finishes its execution at last.

D None of the above, since the system is in a deadlock

QUESTION ANALYTICS



Q. 20

⌚ Have any Doubt ?



A file system with 300 GByte uses a file descriptor with 8 direct block address, 1 indirect block address and 1 doubly indirect block address. The size of each disk block is 128 Bytes and the size of each disk block address is 8 Bytes. The maximum possible file size in this file system is

**A** 3 Kbytes

Correct Option

**B** 35 Kbytes

Solution :

(b)

$$\text{Total number of possible addresses stored in a disk block} = \frac{128}{8} = 16$$

Maximum number of addressable bytes due to direct address block =  $8 \times 128$

Maximum number of addressable bytes due to 1 single indirect address block =  $16 \times 128$

Maximum number of addressable bytes due to 1 double indirect address block =  $16 \times 16 \times 128$

The maximum possible file size =  $8 \times 128 + 16 \times 128 + 16 \times 16 \times 128 = 35 \text{ KB}$ .

**C** 280 Bytes

**D** Dependent on the size of the disk

 QUESTION ANALYTICS

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Q. 21

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In  $X = (M + N \times O)/(P \times Q)$ , how many one-address instructions are required to evaluate it using ACC-CPU and variables are in the memory ?

A 6

B 7

C 8

Correct Option

**Solution :**

(c)

In One-address instructions, an accumulator register is required to perform all the instructions. Load and store operations are performed to fetch the values of operands from registers or memory to accumulators and to store the value of accumulator to a memory location. Instructions required to execute the code:

1. Load M : ACC  $\leftarrow M[M]$
2. Add N : ACC  $\leftarrow ACC + M[N]$
3. Mul O : ACC  $\leftarrow ACC \times M[O]$
4. Store T : M[T]  $\leftarrow ACC$
5. Load P : ACC  $\leftarrow M[P]$
6. Mul Q : ACC  $\leftarrow ACC \times M[Q]$
7. Div T : ACC  $\leftarrow M[T]/ACC$
8. Store X : M[X]  $\leftarrow ACC$

Total 8 instruction are required.

So, option (c) is correct.

D 10

QUESTION ANALYTICS

Q. 22

[Solution Video](#)    [Have any Doubt ?](#)

The register that stores the bits required to mask the interrupts is \_\_\_\_\_.

A Status register

B Interrupt service register

C Interrupt mask register

Correct Option

**Solution :**

(c)

The register that stores the bits required to mask the interrupts is Interrupt mask register. The register that stores the bits required for Status is Status register. The register that stores the bits required to service the interrupts is Interrupt service register. The register that stores the bits required to request the interrupts is Interrupt request register. So, option (c) is correct.

D Interrupt request register

QUESTION ANALYTICS

Q. 23

[FAQ](#)    [Solution Video](#)    [Have any Doubt ?](#)

A byte addressable computer has a memory capacity of  $2^m$  KB and can perform  $2^n$  operations. An instruction involving 3 operands and one operator needs maximum of

A  $3m$  bits

B  $3m + n$  bits

C  $m + n$  bits

D None of the above

Correct Option

**Solution :**

(d)

Note: Memory is byte addressable.

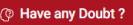
Operator	Operand 1	Operand 2	Operand 3
$n$ bit	$m + 10$ bit	$m + 10$ bit	$m + 10$ bit

$$\begin{aligned}\text{Total bits required} &= 3(m + 10) + n \\ &= (3m + n + 30) \text{ bits}\end{aligned}$$

QUESTION ANALYTICS



Q. 24

? FAQ  Have any Doubt ?



Match the items in List-I and List-II:

List-I

- A. Interrupts which can be delayed when a much highest priority interrupt has occurred.
- B. Unplanned interrupts which occur while executing a program.
- C. Source of interrupt is in phase with the system clock.

List-II

- 1. Normal
- 2. Synchronous
- 3. Maskable
- 4. Exception

Codes:

	A	B	C
(a)	2	1	3
(b)	2	4	3
(c)	3	1	2
(d)	3	4	2

A a

B b

C c

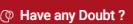
D d

Correct Option

QUESTION ANALYTICS



Q. 25

? FAQ  Have any Doubt ?



Consider the following program:

```
{
    printf("Hello");
    fork();
    printf("Hello");
    fork();
    fork();
}
```

How many times "Hello" will be printed? \_\_\_\_\_

3

Correct Option

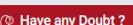
Solution :

3  
Total 3 times "Hello" is printed.

QUESTION ANALYTICS



Q. 26

 Have any Doubt ?



Consider a logical address space of 2 GB and page size is 8 KB, physical memory size is 512 MB. How many bits are required to access an entry in an inverted page table?

16

Correct Option

Solution :

16

Logical address space:

$$2 \text{ GB} = 2^{31} \text{ B}$$

$$\text{Page size} = 8 \text{ KB} = 2^{13} \text{ B}$$

$$\text{Physical address space} = 512 \text{ MB} = 2^{29} \text{ B}$$

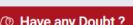
$$\text{Number of frames in physical memory/main memory} = 2^{(29 - 13)} = 2^{16}$$

$\Rightarrow$  16 bits required to access an entry in the inverted page table as number of entry in page table is same as number of frames in main memory.

QUESTION ANALYTICS



Q. 27

 Have any Doubt ?



A system uses virtual address space of size 2 GB and page size is 1 KB. The system has maximum 32 K physical pages. If each page table entry holds only a valid bit and the \_\_\_\_\_

4

Correct Option

**Solution :**

4

- Page size = 1 KB =  $2^{10}$  B  
 V.A.S. = 2 GB =  $2^{31}$  B
- $(31 - 10 = 21)$  bits are used for number of entries in page table.
  - Page table entry = Valid bit + Frame number (bits)
  - 32 K physical pages required 15 bits for frame number.  
 So page table entry =  $1 + 15 = 2$  Bytes
  - Page table size =  $2^{21} \times 2B = 2^{22} = 4$  MB

QUESTION ANALYTICS

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Q. 28

[FAQ](#)[Solution Video](#)[Have any Doubt ?](#)

Q

Suppose that a datapath is built with the following latencies:

Instruction memory = 1200 ps

Register file read = 130 ps

ALU = 600 ps

Data memory = 800 ps

Register file write = 400 ps

All other components = 0 ps

Assuming an average CPI of 1.4 cycles, calculate the speedup of the pipelined implementation over the single-cycle implementation \_\_\_\_\_. (Upto 1 decimal place)

2.6 [2.60 - 2.61]

Correct Option

**Solution :**

2.6 [2.60 - 2.61]

Instruction memory = 1200 ps  
 Register file read = 130 ps  
 ALU = 600 ps  
 Data memory = 800 ps  
 Register file write = 400 ps  
 All other components = 0 ps

Average CPI = 1.4 cycles

$$\text{Speedup} = \frac{CT_{(\text{old})}}{CT_{(\text{new})}}$$

$$= \frac{1200 + 130 + 600 + 800 + 400}{1200} = \frac{3130}{1200} = 2.6$$

QUESTION ANALYTICS

+

Q. 29

[FAQ](#)[Solution Video](#)[Have any Doubt ?](#)

Q

Consider a 16-bit register of floating format is used to store a floating-point number. Mantissa (M) is denoted as normalized signed magnitude fraction, exponent (E) is expressed as excess-64 form. Base of system is 2. How many bits are allocated for fractional Mantissa \_\_\_\_?

8

Correct Option

**Solution :**

8

As bias is given as excess-64, i.e. bias = 64 =  $2^n - 1$   
 $n - 1 = 6 \Rightarrow n = 7$   
 $S + E + M = 16 \Rightarrow 1 + 7 + M = 16$   
 $M = 8$

QUESTION ANALYTICS

+

Q. 30

[FAQ](#)[Solution Video](#)[Have any Doubt ?](#)

Q

Consider a pipeline X consist of 5 stages named as IF, ID, OF, EX and WB with the respective stage delays of 6 ns, 4 ns, 3 ns, 7 ns and 2 ns. The alternative pipeline Y contain the same number of stages but EX stage is divided into 3 sub stages (EX1, EX2 and EX3) each having delay of 2 ns. In the pipeline X and Y memory reference instructions are not overlapped so the penalty of memory reference instructions in the pipeline X is 4 cycles and the penalty in the pipeline Y is 6 cycles. If the program contain 35% of the instructions which are memory based instructions then the speed up ratio of X to speed up ratio of Y is \_\_\_\_\_. (Upto 2 decimal places)

1.15 [1.15 - 1.16]

Correct Option

**Solution :**  
1.15 [1.15 - 1.16]

QUESTION ANALYTICS

+



Kunal Jha

Course: GATE  
Computer Science Engineering(CS)

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## COMPUTER ORGANIZATION AND ARCHITECTURE + OPERATING SYSTEM (GATE - 2021) - REPORTS

OVERALL ANALYSIS

COMPARISON REPORT

SOLUTION REPORT

ALL(33)

CORRECT(0)

INCORRECT(0)

SKIPPED(33)

Q. 31

FAQ

Have any Doubt?



In resource allocation graph two situation exists that is some process is either allocated the resource or requests for the resource.

If in a resource allocation graph contains a cycle then which of the following is/are false:

(A) Starvation occurs.

Correct Option

(B) No deadlock.

Correct Option

(C) Whenever there exists a cyclic condition deadlock will occur.

Correct Option

(D) If several instances per resource type, there is a possibility of deadlock.

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

## Solution :

(a, b, c)

If graph contains a cycle

- If only one instance per resource type, then deadlock.
- If several instances per resource type, possibility of deadlock.

Since 2nd condition is given so option (d) will be chosen over option (a).

QUESTION ANALYTICS



Q. 32

FAQ



Which of the following is/are true of deadlock prevention and deadlock avoidance schemes?

(A) In deadlock prevention, the request for resources always granted if the resulting state is safe.

Correct Option

(B) In deadlock avoidance, the request for resources always granted if the resulting state is safe.

Correct Option

(C) Deadlock avoidance is less restrictive than deadlock prevention.

Correct Option

(D) Deadlock avoidance requires knowledge of resource requirements a priority.

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - b,c,d

STATUS - SKIPPED

## Solution :

(b, c, d)

Deadlock prevention deals only with preventing mutual exclusion, hold and wait, No preemption,

Circular wait.

Deadlock prevention scheme handles deadlock by making sure that one of the four necessary conditions don't occur. In deadlock prevention, the request for a resource may not be granted even if the resulting state is safe.

QUESTION ANALYTICS



Q. 33

FAQ

Have any Doubt?



The benefits of multithreaded programming is/are:

(A) Scalability

Correct Option

(B) Responsiveness

Correct Option

(C) Efficiency

Correct Option

(D) Resource sharing.

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c,d

STATUS - SKIPPED

## Solution :

(a, b, c, d)

The benefits of multithreaded programming are: Responsiveness (it allows program to continue running even part of it is blocked or is performing lengthy operation, thereby increases responsiveness to the user), Resource sharing (process share resource by through message passing), Scalability and Efficiency.

QUESTION ANALYTICS



