



Kunal Jha
 Course: GATE
 Computer Science Engineering(CS)

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COMPUTER ORGANIZATION AND ARCHITECTURE-1: (GATE - 2021) - REPORTS

OVERALL ANALYSIS COMPARISON REPORT **SOLUTION REPORT**

ALL(17) CORRECT(0) INCORRECT(0) SKIPPED(17)

Q. 1

Solution Video

Have any Doubt ?



Which of the following options represents the correct matching?

Addressing Mode	Description
1. Immediate	A. The address field refers to the address of a word in the memory, which in-turn contains the address of the operand.
2. Direct	B. The address field contains the address (in main memory) where the operand is stored.
3. Indirect	C. Operand value is present in the instruction itself (address field)
4. Register Direct	D. The address field of the operand is a register.

A 1 → A; 2 → D; 3 → C; 4 → B

B 1 → C; 2 → B; 3 → D; 4 → A

C 1 → C; 2 → B; 3 → A; 4 → D

Correct Option

Solution :
 (c)

D 1 → A; 2 → D; 3 → B; 4 → C

QUESTION ANALYTICS



Q. 2

FAQ Solution Video Have any Doubt ?



The following is the micro-operation sequence needed for the instruction "POP" i.e., "POP R1".

A. SP ← SP + 1

B. _____

C. Read

D. R1 ← HBR

Which of the following describes most appropriately, the second step (B) marked above with _____.

A PC ← PC + 1 (PC gets incremented by instruction length)

B MAR ← Address of operand in IR.

C PC ← Pop the return address from the stack.

D MAR ← SP (memory address register is assigned with the value of stack pointer)

Correct Option

Solution :

(d)

A. SP ← SP + 1

B. MAR ← SP

C. Read

D. R1 ← MBR

Memory Address Register is assigned the value of stack-pointer.

QUESTION ANALYTICS



Q. 3

FAQ Solution Video Have any Doubt ?



Which of the following is TRUE?

A In micro-programmed control unit, the logic of the control unit is specified in a memory.

Correct Option

Solution :

(a)

• In micro-programmed control unit, the logic of the control unit is specified in a memory.

• Hardwired control unit is faster than micro-programmed control unit.

B Hardwired control unit is slower in execution compared to micro-programmed control unit.

C For some control signal sequence there can not be any hardware control unit.

D To some control signal sequence there can not be any micro-programmed control unit.

Q. 4

[FAQ](#)
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An instruction pipeline was designed with five stages. Individually each of the stages will take 3.2 ns, 2.9 ns, 4.1 ns, 3.3 ns and 3.5 ns respectively. The pipeline latch latency is 0.9 ns. What is the minimum clock frequency of the pipeline?

 A 0.1 GHz B 0.2 GHz

Correct Option

Solution :(b) $\text{Max}(3.2, 2.9, 4.1, 3.3, 3.5)$

$$= 4.1 \text{ ns}$$

$$\text{Cycle time} = 4.1 \text{ ns} + 0.9 \text{ ns} (\text{latch latency})$$

$$= 5 \text{ ns}$$

$$\text{So, Clock frequency} = \frac{1}{5 \text{ ns}} = 0.2 \text{ GHz}$$

 C 0.3 GHz D 0.4 GHz

Q. 5

[FAQ](#)
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Which of the following operation is performed in the MEM stage for an ALU instructions in a 5-stage RISC instruction pipeline?

 A Transfer the resultant from the ALU to the memory location. B Load the address of the destination location from memory to ALU. C Write the resultant from the ALU to the destination register. D Copies the contents in EX/MEM pipeline register to MEM/WB pipeline register.

Correct Option

Solution :

(d)

Copies the contents in EX/MEM pipeline register to MEM/WB pipeline register.

Q. 6

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Consider an example of memory organization as shown in the figure below. Assume @ represents indirect address.

Memory Location Address	Content
0	10
1	23
2	25
3	20
4	12
5	3
6	1
7	2

Which value will be loaded into the accumulation when the instruction "LOAD @ 5" (here 5 is the address location) is executed?

 20

Correct Option

Solution :

20

Load @ 5.

Here @ is indirect address.

Here the content of 5 is the address of the actual data.

Actual data present at address 3 which is 20.

Q. 7

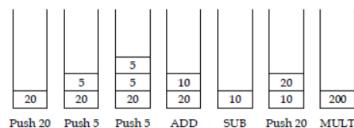
[FAQ](#)
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For a 0-address instruction format, what would be the top element of the stack following sequences of instructions?
PUSH 20; PUSH 5; PUSH 5; ADD; SUB; PUSH 20; MULTIPLY

 200

Correct Option

Solution :
200



QUESTION ANALYTICS

Q. 8

Solution Video

Have any Doubt ?



Which of the following addressing modes are suitable for program relocation at run time?

A Absolute addressing

B Based addressing

Correct Option

C Relative addressing

Correct Option

D Indirect addressing

YOUR ANSWER - NA

CORRECT ANSWER - b,c

STATUS - SKIPPED

Solution :

(b, c)

Relocation at run time is done in the displacement type of addressing mode so Based addressing and Relative Addressing.

QUESTION ANALYTICS



Q. 9

FAQ Solution Video

Have any Doubt ?



Which of the following is/are true about Excess-3 code?

A These are unweighted binary decimal codes.

Correct Option

B These are self-complementary codes.

Correct Option

C It considerably simplifies arithmetic operations.

Correct Option

D It can cause fault in transmission line due to the use of 0000 and 1111.

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)

Option (d) is false since excess-3 code does not use 0000 and 1111 and hence will not cause any fault. It is the advantage of excess-3 code.

QUESTION ANALYTICS



Q. 10

FAQ Solution Video

Have any Doubt ?



A system employs 8-stage instruction pipeline in which 10% instruction results in data dependency, 10% instruction results in control dependency, 5% instruction results in structural dependency. If the penalty for structural dependency is 2 clock and the penalty for control dependency is 2 and 1 clock for data dependency. What is the average instruction time?

A 1.1 cycles

B 1.3 cycles

C 1.4 cycles

Correct Option

Solution :

(c)

$$\begin{aligned} T_{avg} &= (1 + \# \text{ stalls/instruction}) \times \text{Cycle Time} \\ &= 1 + (10\% \times 1) + (10\% \times 2) + (5\% \times 2) \\ &= 1 + 0.1 + 0.2 + 0.1 \\ &= 1.4 \text{ cycles} \end{aligned}$$

D 1.5 cycles

QUESTION ANALYTICS





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CORRECT(0)

INCORRECT(0)

SKIPPED(17)

Q. 11

FAQ

Solution Video

Have any Doubt?

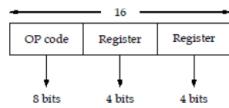


A 64

B 144

C 240

Correct Option

Solution:
(c)So, total number of 2-address instructions = $2^8 = 256$.

Given that number of 1-address instruction = 256.

We know that maximum number 1-address instruction 256.

$$(2^8 - x) \times 2^4 = 256$$

$$2^8 - x = 2^4$$

$$x = 256 - 16 = 240$$

D 256

QUESTION ANALYTICS



Q. 12

FAQ

Solution Video

Have any Doubt?

Consider a hypothetical control unit that supports 6 groups of mutually exclusive control signals. Assume that group G_1 and G_2 are using horizontal micro-programming whereas G_3 , G_4 , G_5 and G_6 are using vertical micro-programming.

Groups	G_1	G_2	G_3	G_4	G_5	G_6
Control Signals	32	45	66	33	13	21

The total number of bits used for control words are _____.

A 94 bits

B 99 bits

Correct Option

Solution:
(b)

- Group G_1 and G_2 use horizontal μ -programming.
Total bits are : $32 + 45 = 77$
- Group G_3 , G_4 , G_5 and G_6 are using vertical μ -programming.
Hence, total bits are

$$= [\log_2 66] + [\log_2 33] + [\log_2 13] + [\log_2 21] \\ = 7 + 6 + 4 + 5 = 22$$

$$\text{Total bits for control word} = 77 + 22 = 99$$

C 100 bits

D 101 bits

QUESTION ANALYTICS



Q. 13

FAQ

Solution Video

Have any Doubt?



Suppose that a task that has floating point operations with 30% of the time is consumed by floating point operations with a new hardware design. If the floating point module is speed up by a factor of 3. What is the overall speed up?

A 1.8

B 1.25

Correct Option

Solution:
(b)

By using Amdahl's law :

$$S = 3, f = 30\%$$

$$S_{\text{overall}} = \left[(1-f) + \frac{f}{S} \right]^{-1}$$

Here, f is most frequencies used operation frequency and S is speed up factor.

$$\begin{aligned} S_{\text{overall}} &= \left[(1-0.3) + \frac{0.3}{3} \right]^{-1} = [0.7 + 0.1]^{-1} \\ &= \frac{1}{0.8} = 1.25 \end{aligned}$$

C 1.35

D 1.6

QUESTION ANALYTICS

Q. 14

FAQ Solution Video

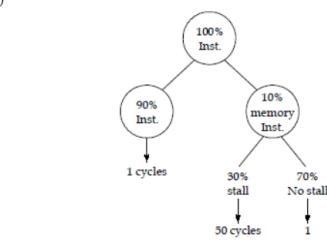
Have any Doubt?

Given an instruction pipeline running at 1 GHz that takes 5 cycles to finish an instruction. 30% memory instructions result in a stall of 50 cycles. Assume a base CPI without stalls as 1 and there are 10% memory instructions, the effective CPI is _____. (Upto 2 decimal places)

C 2.50 (2.45 - 2.55)

Correct Option

Solution:
2.50 (2.45 - 2.55)



$$\begin{aligned} \text{Effective CPI} &= 0.9 \times 1 + 0.1(0.3 \times 50 + 0.7 \times 1) \\ &= 0.9 + 0.1 \times 15.7 = 2.47 \end{aligned}$$

QUESTION ANALYTICS

Q. 15

Solution Video

Have any Doubt?

Given a non-pipelined architecture running at 2 GHz, that takes 5 cycles to finish an instruction. You want to make it pipelined with 5 stages. Due to hardware overhead the pipelined design will operate only at 1 GHz. 5% of instructions cause a stall of 20 cycles each during the IF (instruction fetch) stage due to cache miss. (Assume that there are no other hazards). What is the speed up obtained by the pipelined design over the non-pipelined design? (Upto 2 decimal places)

C 1.25 (1.20 - 1.30)

Correct Option

Solution:
1.25 (1.20 - 1.30)

$$\begin{aligned} \text{Speed up of pipeline} &= \frac{5 \times 0.5 \text{ ns}}{(1 + 0.05 \times 20) \times 1 \text{ ns}} \\ &= \frac{2.5}{2} = 1.25 \end{aligned}$$

QUESTION ANALYTICS

Q. 16

Solution Video

Have any Doubt?

Which information is/are not correct?

A Sign flag(s): If sign bit is 1 then the sign flag is set to 1 and if the sign bit is zero then flag is reset to zero.

B Zero flag(z): If the result of any arithmetic or logical operation is zero i.e. all the bits are zero then flag is set to 1 else it is set to zero.

C Auxiliary carry: (AC) this flag is set to 1 only when a carry is produced in the result.

Correct Option

D Carry flag(C): This flag is set to 1 only when any intermediate carry is produced. Else it is reset to 0

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - c,d

STATUS - SKIPPED

Solution :

(c, d)
Auxiliary carry: (AC) This flag is set to 1 only when any intermediate carry is produced. Else it is reset to 0.
Carry flag(C): This flag is set to 1 only when a carry is produced in the result i.e. the carry bit is 1 else if the carry bit is zero then the flag is reset to zero.

QUESTION ANALYTICS



Q. 17

FAQ Solution Video Have any Doubt ?



Which of the flowing statements about relative addressing mode is TRUE?

A It enables reduced instruction size.

Correct Option

B It enables easy relocation of data.

Correct Option

C It allows indexing of Arrays element with same instruction.

Correct Option

D It enables faster address calculation than absolute addressing mode.

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)

Only option (d) is false. Relative addressing cannot be faster than absolute addressing as absolute address must be calculated from relative address. With specialized hardware unit, this can perform equally as good as absolute addressing but not faster.

QUESTION ANALYTICS



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INCORRECT(0)

SKIPPED(33)

FAQ

Solution Video

Have any Doubt ?



Q. 1

FAQ

Solution Video

Have any Doubt ?



Assertion (A) : The DMA technique is more efficient than the interrupt-driven technique for high volume I/O data transfer.
 Reason (R) : The DMA technique does not make use of the interrupt mechanism.

 A Assertion (A) is true but Reason (R) is false. B Assertion (A) is false and Reason (R) is false. C Both Assertion (A) and Reason (R) is true and Reason (R) is the correct explanation of Assertion (A).

Correct Option

Solution :

(c)

The DMA technique does not make use of the interrupt mechanism, that's why it is more efficient than the interrupt-driven technique for high volume I/O data transfer.

 D Both Assertion (A) and Reason (R) is true and Reason (R) is not the correct explanation of Assertion (A).

QUESTION ANALYTICS



Q. 2

Solution Video

Have any Doubt ?



Match List-I with List-II and select the correct option accordingly.

List-I List-II

- | | |
|----------------------------|-----------------------------|
| A. Thrashing | 1. Direct Cache |
| B. Expand-OPcode technique | 2. Inclusion |
| C. Write Back Protocol | 3. Coherence |
| D. Write through Protocol | 4. Fixed Length Instruction |

Codes:

- | A | B | C | D |
|-------------|---|---|---|
| (a) 2 4 3 1 | | | |
| (b) 1 4 3 2 | | | |
| (c) 3 1 2 4 | | | |
| (d) 4 2 3 1 | | | |

 A a B b

Correct Option

Solution :

(b)

 C c D d

QUESTION ANALYTICS



Q. 3

FAQ

Solution Video

Have any Doubt ?



Which of the following best characterizes about memory mapped I/O?

 A Common bus is used but to differentiate between memory and I/O different control signals is used for memory and I/O. B Some of the address space is separated from the memory space and assigned them to I/O parts.

Correct Option

Solution :

(b)

Memory mapped I/O uses common bus and common control signals but having unique address space for I/O ports.

 C Additional hardware for bus is required to control the I/O bus and memory bus. D Both (a) and (b)

QUESTION ANALYTICS



Q. 4

[FAQ](#)[Solution Video](#)[Have any Doubt ?](#)

A processor overflow flag is represented as $OV(a, b, c)$ where arguments a is MSB of operand 1, b is MSB of operand 2 and c is the MSB of the result after computing a and b . The $OV(a, b, c)$ of PSW becomes 1 after

A $a'b'c + abc'$ **B** $a'b'c + abc$

Correct Option

Solution :

(b)

Overflow flag is active when there is a carry into the MSB and No carry out of MSB or vice-versa.

MSB of operand 1 (a)	MSB of operand 2 (b)	MSB of result (c)	Overflow
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
<hr/>			
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

So, whenever $a'b'c + abc'$, overflow flag is active.

Hence, option (b) is correct.

C $ab'c + abc$ **D** $a'b'c + abc$ 

Q. 5

[FAQ](#)[Solution Video](#)[Have any Doubt ?](#)

Which of the following is correct about vectored interrupt?

A Interrupt vector gives the branch address of an interrupting device.

Correct Option

Solution :

(a)

Interrupt Vector gives the branch address of an interrupting device.

B Polling technique is used to transfer the branch information.**C** Branch address is always assigned to a fixed memory location.**D** None of these

Q. 6

[Solution Video](#)[Have any Doubt ?](#)

A hypothetical CPU supports 400 instructions. Each instruction takes 4 cycles to accomplish the execution. The control unit is designed using vertical programming which has 150 control signals, 45 flags and 20 branch conditions. The number of bits required for Control Address Register (CAR) and Control Data Register (CDR) is

A 16 bit and 11 bit respectively**B** 10 bit and 28 bit respectively**C** 11 bit and 30 bit respectively

Correct Option

Solution :

(c)

$$\begin{aligned} \# \text{cycles/instruction} &= 4 \\ \text{Total } \# \text{ } \mu\text{-instruction} &= 400 \times 4 = 1600 \\ \# \text{f bit for CAR} &= [\log_2(1600)] = 11 \text{ bit} \end{aligned}$$

Branch Conditions	Flag	Control Signal	CM Address
5-bit	6-bit	8-bit	11-bit

$$\# \text{f bit for CDR} = 5 + 6 + 8 + 11 = 30 \text{ bit}$$

D 15 bit and 25 bit respectively

Q. 7

[FAQ](#)
[Solution Video](#)
[Have any Doubt?](#)


Consider a modified 8-bit floating point representation in which 1-bit for sign, 3-bit for exponent and 4-bit for significant. What will be representation for decimal value -12?

A 11111000

B 11101000

Correct Option

Solution :

(b)

Given, Decimal = -12

Number is negative, so

Sign bit = 1

Sign	Exponent	Significant
1-bit	3-bit	4-bit

- Now express 12 in binary form : 1100

Normalized form = 1.100×2^3

- For 3-bit exponent field, a bias of $(2^{3-1} - 1 = 3)$ is used.

- Add the bias to the exponent = $3 + 3 = 6 = (110)_2$.

Hence result will be

1	110	1000
Sign	Exponent	Significant

Hence, option (b) is correct.

C 11110000

D 11111100

Q. 8

[FAQ](#)
[Solution Video](#)
[Have any Doubt?](#)


A hypothetical processor uses a fixed 20-bit instruction length. The operand size are 8 bits. There are x number of 2-operand instructions and y number of 1-operand instructions. What is the maximum number of zero operand instructions that can be supported by this processor?

A $((2^4 - x) \times 2^8) - y) \times 2^8$

Correct Option

Solution :

(a)

of 2-operand instructions = x

of 1-operand instructions = y

of zero operand instruction

$$= ((2^4 - x) \times 2^8) - y) \times 2^8$$

B $((2^4 - x)/2^8) - y) \times 2^8$

C $((2^{20} - x) \times 2^8) - y) \times 2^8$

D $((2^8 - x) \times 2^8) - y) \times 2^8$

Q. 9

[FAQ](#)
[Solution Video](#)
[Have any Doubt?](#)


Consider a 4-stage pipeline system. Assume that there is no cycle time overhead of pipelining. An application is executing on this pipeline system. What is the speedup achieved with respect to non-pipelined execution if 42% of the instruction incurred 3 pipeline stall cycles _____ (Upto 2 decimal places)

A 1.76 [1.70 - 1.78]

Correct Option

Solution :

1.76 [1.70 - 1.78]

$$\text{Speed-up} = \frac{\text{Execution time of non pipeline}}{\text{Execution time of pipe line}}$$

$$\text{Speed up factor} = \frac{4}{0.42 \times 4 + 0.58 \times 1} = \frac{4}{2.26} = 1.76$$

Q. 10

[FAQ](#)
[Solution Video](#)
[Have any Doubt?](#)


Consider a 5 stage pipeline with Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Write Back (WB) and Memory Access (MA) having latencies 4 ns, 8 ns, 3 ns, 6 ns

and f is respectively. What is the average CPI of non-pipeline CPU when speed up achieved by pipeline is 5 _____? (Up to 2 decimal places)

1.50 [1.48 - 1.51]

Correct Option

Solution :

1.50 [1.48 - 1.51]

$$\text{Speed up} = \frac{T_{\text{non-pipeline}(N)}}{T_{\text{pipeline}(P)}}$$

$$5 = \frac{\text{CPI}_n \times \# \text{Instruction} \times \text{Cycle Time}_n}{\text{CPI}_p \times \# \text{Instruction} \times \text{Cycle Time}_p}$$

$$5 = \frac{\text{CPI}_n \times (4+8+3+6+9)}{1 \times \max[4, 8, 3, 6, 9]}$$

$$5 = \frac{\text{CPI}_n \times 30}{1 \times 9}$$

$$\text{CPI}_n = \frac{45}{30} = 1.5$$

 QUESTION ANALYTICS



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ALL(33) CORRECT(0) INCORRECT(0) SKIPPED(33)

Q. 11

? FAQ ▶ Solution Video ⚡ Have any Doubt ?

Consider a cache of $2y$ blocks and the main memory of $2y$ blocks. At what set location $(y + 4)^{\text{th}}$ block will be mapped in 2-way set associative _____.

4

Correct Option

Solution :

4

$$\text{Number of sets} = \frac{\text{Number of blocks in cache}}{k\text{-way}} = \frac{2y}{2} = y$$

Set location of y^{th} block = $y\%$ number of sets

$$\begin{aligned} \text{Set location of } (y + 4)^{\text{th}} \text{ block} \\ &= (y + 4)\% \text{ number of sets} \\ &= (y + 4)\% y = 4 \end{aligned}$$

QUESTION ANALYTICS

+

Q. 12

? FAQ ▶ Solution Video ⚡ Have any Doubt ?

Assume X and Y represents number of times a processor needs to refer to memory when it fetches and executes an indirect address mode instruction for single operand and for branch respectively. The value of $(X - Y)$ is _____.

1

Correct Option

Solution :

1

- X represents number of times memory referred for single operand.

$$X = 3 \left[\begin{array}{l} 1. \text{ Fetch instruction} \\ 2. \text{ Fetch operand reference [EA]} \\ 3. \text{ Fetch operand} \end{array} \right]$$

- Y represents for branch instruction

$$Y = 2 \left[\begin{array}{l} 1. \text{ Fetch instruction} \\ 2. \text{ Fetch from memory and placed EA into PC} \end{array} \right]$$

$$\text{So, } X - Y = 3 - 2 = 1$$

QUESTION ANALYTICS

+

Q. 13

? FAQ ▶ Solution Video ⚡ Have any Doubt ?

A processor supports 256 kW of memory and uses memory mapped I/O for I/O Port. Address to the I/O Port is assigned when 3 MSB bits of address is high. The number of memory address available for I/O port is _____.

32768

Correct Option

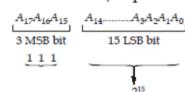
Solution :

32768

Given that 256 kW of memory used.

$$\begin{aligned} 256 \text{ kW} &= 2^8 \times 2^{10} \text{ W} \\ &= 2^{18} \text{ W} \end{aligned}$$

Whenever 3 MSB bit is high, that is used for I/O port.



When $A_{17}A_{16}A_{15}$ is high then remaining 2^{15} combinations of memory reserved for I/O Port.
 So, $2^{15} = 32768$

QUESTION ANALYTICS

+

Q. 14

? FAQ ▶ Solution Video ⚡ Have any Doubt ?

Assume a system has 3 control signals named as S_0, S_1 and S_2 , 3 different instructions I_1, I_2 and I_3 and 3 micro-operations T_1, T_2 and T_3 . The below table represents controls signals required at different micro-operations for the particular instruction.

μ -operation/instruction	I_1	I_2	I_3
T_1	S_0, S_1	S_0	S_0, S_1, S_2
T_2	S_2	S_2, S_1	S_2
T_3	S_0	S_1	S_2

Which of the below control signal equations are correct?

A $S_0 = T_1 + T_3 I_1$

Correct Option

B $S_0 = T_1(I_1 + I_2) + T_3 I_1$

C $S_1 = T_1(I_1 + I_2) + T_2 I_2 + T_3 I_2$

Correct Option

D $S_1 = T_1 I_1 + T_2(I_2 + I_2)$

YOUR ANSWER - NA

CORRECT ANSWER - a,c

STATUS - SKIPPED

Solution :

(a, c)

Only equation (a) and (c) for control signal S_0 and S_1 are correct.

Hence, answer will be 2.

QUESTION ANALYTICS



Q. 15

Solution Video

Have any Doubt ?



Which of the following are correct?

A Compulsory misses can be reduced by increasing the block size.

Correct Option

B The search concept used in associative memory is parallel search.

Correct Option

C Conflict misses can be reduced by increasing block size.

D Reducing block size will impact the spatial locality.

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,d

STATUS - SKIPPED

Solution :

(a, b, d)

(a) Larger blocks reduce compulsory misses by improving spatial locality. So, this statement is correct.

(b) Associative memory is suitable for parallel searches and is used where search time needs to be minimized.

(c) Conflict misses in fact will increase by increasing block size because there will be less number of lines. So, this statement is incorrect.

(d) is correct.

QUESTION ANALYTICS



Q. 16

Solution Video

Have any Doubt ?



Which of the following is pipelined CPU causes hazards?

A 2 consecutive instructions and 1 instruction uses the result of previous instructions.

Correct Option

B Conditional jump instruction.

Correct Option

C 2 consecutive instruction required ALU at the same time.

Correct Option

D None of these

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)

(a) → Data hazard

(b) → Control hazard

(c) → Structural hazard

(a), (b) and (c) all three statements causes hazards.

QUESTION ANALYTICS



Q. 17

Solution Video

Have any Doubt ?



Consider 4 stage instruction pipeline executed on a system:

	S_1	S_2	S_3	S_4
I_1	1	3	1	1
I_2	2	1	2	1
I_3	1	2	1	2
I_4	2	1	2	1

If all instructions are executed only once, what is the throughput or system?

A $\frac{4}{9}$ cycles

B $\frac{4}{10}$ cycles

C $\frac{4}{12}$ cycles

D $\frac{4}{11}$ cycles

Correct Option

Solution:
(d)

	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}	c_{11}
S_4						I_1	I_2	I_3	I_3	I_4	
S_3						I_1	I_2	I_3	I_4	I_4	
S_2		I_1	I_1	I_1	I_2	I_3	I_3	I_4			
S_1	I_1	I_2	I_2		I_3	I_4	I_4				

$$\text{Throughput} = \frac{\text{Number of task completed}}{\text{Total time taken to process the tasks}}$$

$$= \frac{4}{11} \text{ cycles}$$

QUESTION ANALYTICS

Q. 18

FAQ Solution Video Have any Doubt ?

Consider a n-way cache with ' x ' blocks of 64 words each. The main memory of the system is having 8 million words. Size of the tag field is 16 bits and additional memory required for tags is 1024 bytes. What will be the value of n and x respectively?

A 128 and 1024

B 128 and 256

C 8 and 158

D 256 and 512

Correct Option

Solution:
(d)

$$1 \text{ million words} = 10^6 \text{ words} = 2^{20} \text{ words}$$

$$8 \text{ million words} = 2^3 \times 2^{20} = 2^{23} \text{ word} = 23 \text{ bits}$$

Tag memory = Number of blocks \times Tag size

$$1024 \times 8 = x \times 16$$

$$x = 512 = 2^9$$

x blocks of 64 words each, so 6 bits required to represent word offset.



$$\text{Length of set offset} = 23 - (16 + 6) = 1$$

$$\text{Number of sets} = 2^1 = 2$$

$$n = \frac{\text{Number of blocks}}{\text{Number of sets}} = \frac{512}{2} = 256$$

QUESTION ANALYTICS

Q. 19

FAQ Solution Video Have any Doubt ?

Consider the following set of instructions executed for a program to be accomplished.

Instruction	Meaning
$I_1 : \text{STORE } M[100], R_1$	$M[100] \leftarrow R_1$
$I_2 : \text{MOV } R_2, M[700]$	$R_2 \leftarrow M[700]$
$I_3 : \text{DIV } R_1, R_2, R_1$	$R_1 \leftarrow R_2 / R_1$
$I_4 : \text{ADD } R_2, R_1, R_2$	$R_2 \leftarrow R_1 + R_2$
$I_5 : \text{STORE } M[500], R_2$	$M[500] \leftarrow R_2$
$I_6 : \text{STORE } M[200], R_1$	$M[200] \leftarrow R_1$

How many number of anti data dependency and true data dependency in the above instructions?

A 2 and 3

Correct Option

Solution:
(a)

Anti data dependency \rightarrow Write After Read Hazard (WAR)

True data dependency \rightarrow Read After Write Hazard (RAW)

	WAR hazards	RAW hazards (Adjacent)
1.	$I_3 - I_1(R_1)$	$I_1 - I_3(R_2)$

2.	$I_4 - I_5(R_2)$	2.	$I_4 - I_3(R_1)$
3.	$I_5 - I_4(R_2)$		

B 2 and 2

C 2 and 1

D 1 and 3

QUESTION ANALYTICS



Q. 20

? FAQ

▶ Solution Video

⌚ Have any Doubt ?



Consider an instruction pipeline as shown below:



A program having 100 instructions is executed in the pipelined processor. Instruction I_4 is the unconditional jump instruction and branch address is known after EX stage. The time needed to complete the execution of the program if the branch target address is 98th instruction is

A 96 ns

B 102 ns

C 105 ns

D 108 ns

Correct Option

Solution :

(d)

Let's take 100 instruction is $I_1, I_2, I_3, \dots, I_{98}, I_{99}, I_{100}$.

Instruction	1	2	3	4	5	6	7	8	9	10	11	12
I_1	IF	ID	EX	MO								
I_2		IF	ID	EX	MO							
I_3			IF	ID	EX	MO						
I_4				IF	ID	EX	MO					
I_5					IF	ID	EX					
I_6						IF	ID					
I_{98}							IF	ID	EX	MO		
I_{99}								IF	ID	EX	MO	
I_{100}									IF	ID	EX	MO

$$n = 9$$

$$\begin{aligned} \text{Total time required} &= (K + n - 1)t_p \\ &= (4 + 9 - 1)9 \text{ ns} = 108 \text{ ns} \end{aligned}$$

QUESTION ANALYTICS



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CORRECT(0)

INCORRECT(0)

SKIPPED(33)

Q. 21

FAQ

Solution Video

Have any Doubt?

A cache contains n blocks and main memory contains m blocks. If k -way associative mapping is used then what will be number of TAG bits

A $\log_2 \frac{mn}{k}$

B $\log_2 \frac{nk}{m}$

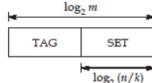
C $\log_2 \frac{m}{n}$

D $\log_2 \frac{mk}{n}$

Correct Option

Solution :
(d)

Number of sets = $\frac{n}{k}$



$$\begin{aligned} \text{Number of TAG bits} &= \log_2(m) - \left(\log_2 \frac{n}{k} \right) \\ &= \log_2(m) - \log_2 \frac{n}{k} \\ &= \log_2 \frac{mk}{n} \end{aligned}$$

QUESTION ANALYTICS



Q. 22

FAQ

Solution Video

Have any Doubt?

A hypothetical processor can execute a maximum of 10^6 instructions per second. System is word addressable and I/O device is connected through shared bus. An average instruction requires 8 machine cycles. Processor can execute 80% of its instruction that does not require any I/O instructions. If programmed I/O is used and each one-word I/O transfer requires the process to 4 instructions. What is the data transfer rate between I/O and processor?

A 1950 words/sec

B 3375 words/sec

C 2408 words/sec

D 50000 words/sec

Correct Option

Solution :
(d)

- 80% does not require I/O. So, 20% instructions required I/O.

Thus, maximum I/O instructions execution rate

$$= 10^6 \times 0.2$$

$$= 200000 \text{ instruction/sec}$$

- For 1-word transfer it requires to execute 4 instructions

$$1 \text{ word} = 4 \text{ instructions}$$

$$? = 200000 \text{ instructions}$$

$$\text{Data transfer rate} = \frac{200000}{4} = 50000 \text{ words/sec}$$

QUESTION ANALYTICS



Q. 23

Solution Video

Have any Doubt?

Suppose 2-way set associative cache with 2^m lines 2^p bytes per cache lines. Memory is byte addressable of 2^n bytes. What is the space required for storing tags (in bits)?A $2^{n-(m+p)}$ B $2^m \times (n - (m + p))$

C $2^m \times (n - ((m-1) + p))$

Correct Option

Solution:
(c)

$$\begin{aligned}\text{Number of sets} &= \frac{\text{Number of lines}}{\text{Set associativity}} \\ &= \frac{2^m}{2} = 2^{m-1}\end{aligned}$$

$$\begin{aligned}\text{Set offset} &= \log_2(2^{m-1}) = (m-1) \text{ bits} \\ \text{Word offset} &= \log_2(2^p) = p \text{ bits} \\ \text{Address field size} &= \log_2(2^n) = n \text{ bits} \\ \text{Tag bit per line} &= n - ((m-1) + p) \\ \text{Tag size} &= \text{Number of cache lines} \times \text{Number of tag bits per line} \\ &= 2^m \times (n - ((m-1) + p))\end{aligned}$$

D $2^p \times (n - (m+p))$

QUESTION ANALYTICS

Q. 24

? FAQ ► Solution Video

Have any Doubt ?



Consider the following instruction sequence with their meaning given below:

Instruction	Meaning of Instruction
$I_0 : MUL R_2, R_3, R_1$	$R_2 \leftarrow R_3 \times R_1$
$I_1 : DIV R_3, R_3, R_4$	$R_3 \leftarrow R_3 / R_4$
$I_2 : ADD R_2, R_3, R_2$	$R_2 \leftarrow R_3 + R_2$
$I_3 : SUB R_3, R_2, R_6$	$R_3 \leftarrow R_2 - R_6$

What is the number of Write After Read (WAR) and Write After Write (WAW) hazards for the above instruction sequence?

A 3, 2

Correct Option

Solution:
(a)

$$\begin{aligned}\text{WAW} &= I_0(R_2) \rightarrow I_2(R_2), I_1(R_3) \rightarrow I_3(R_3) \\ \text{WAR} &= I_0(R_3) \rightarrow I_1(R_3), I_0(R_3) \rightarrow I_3(R_3), I_2(R_3) \rightarrow I_3(R_3)\end{aligned}$$

B 2, 1

C 3, 1

D 1, 2

QUESTION ANALYTICS

Q. 25

? FAQ ► Solution Video

Have any Doubt ?



Consider a hypothetical system used in web applications. Application program refers the IO operation and ALU operations. IO operational unit is enhanced then it runs 4 times faster. In the application program 40% of instructions are ALU instructions. The performance gain in the enhanced system is _____. (Up to 2 decimal places)

1.80 (1.80 – 1.82)

Correct Option

Solution:

1.80 (1.80 – 1.82)

$$S = \left[(1-F) + \frac{F}{S} \right]^{-1}$$

$$S = \left[(1-0.6) + \frac{0.6}{4} \right]^{-1}$$

$$S = [0.4 + 0.15]^{-1}$$

$$S = 1.8$$

QUESTION ANALYTICS

Q. 26

? FAQ ► Solution Video

Have any Doubt ?



Consider the following program codes:

$I_1 : \text{Load } R_1, (R_2)$

$I_2 : \text{MUL } R_1, R_3$

$I_3 : \text{SUB } R_3, R_0$

$I_4 : \text{Load } (R_0), R_3$

$I_5 : \text{DIV } R_3, R_6$

$I_6 : \text{SUB } R_2, R_5$

$I_7 : \text{HALT}$

$I_8 : \text{ADD } R_2, R_4$

$I_9 : \text{LOAD } (R_3), R_0$

Assume the data transfer instruction size is 48 bit, ALU operation instruction size 40 bit and branch instruction size is 24 bit. The program starts from the location 5000 decimal onwards. Assume if the interrupt occurs during the execution of I_7 , the return address pushed onto the stack is _____.

5032

Correct Option

Solution :

5032

 $I_1 : 5000 - 5005$ $I_2 : 5006 - 5010$ $I_3 : 5011 - 5015$ $I_4 : 5016 - 5021$ $I_5 : 5022 - 5026$ $I_6 : 5027 - 5031$ $I_7 : 5032 - 5034$ $I_8 : 5035 - 5039$ $I_9 : 5040 - 5045$

Return address (5032) is pushed onto the stack.

QUESTION ANALYTICS



Q. 27

FAQ Solution Video

Have any Doubt ?



A hypothetical 6 stage pipeline processor is designed in which branch is predicted at 4th stage and each stage takes a cycle to compute its task. If P is the probability of an instruction being a branch instruction then the value of P such that speed up is atleast 3 is _____. (Upto 2 decimal places)

0.33 [0.30 - 0.34]

Correct Option

Solution :

0.33 [0.30 - 0.34]

$$\text{Speed up} = \frac{\text{Pipeline depth}}{1 + \text{Branch frequency} \times \text{Branch Penalty}} \geq 3$$

$$\frac{6}{1 + P \times 3} \geq 3$$

$$9P + 3 \leq 6$$

$$9P \leq 3$$

$$P \leq \frac{1}{3}$$

$$P \leq 0.33$$

QUESTION ANALYTICS



Q. 28

FAQ Solution Video

Have any Doubt ?



Direct Memory Access (DMA) takes 50 cycles for the initialization and 5 cycles for the transfer of each block. An interrupt program takes 3 cycles for every instruction and executed for every byte transferred. The block size of the system is 8 bytes. The speed up of DMA over interrupt program achieved when program of 15 instructions executed for transfer of 160 bytes is _____.

48

Correct Option

Solution :

48

If cycles required when program executed using DMA

$$= 50 + 5 \times \left(\frac{160}{8} \right) = 150 \text{ cycles}$$

If cycles required when program executed using interrupt program

$$= (3 \times 15) \times 160 = 7200$$

Speed up achieved by DMA over interrupt program

$$= \frac{7200}{150} = 48$$

QUESTION ANALYTICS



Q. 29

FAQ Solution Video

Have any Doubt ?



A cache memory is organized into 2 level cache L_1 and L_2 . The penalty for L_1 cache miss and L_2 cache miss are 55 and 25 respectively for 1000 memory references. The hit time of L_1 and L_2 are 10 and 18 clock cycles respectively. The penalty for L_2 cache miss to main memory is 100 clock cycles. The average memory access time will be _____. (Upto 2 decimal places)

13.46 (13.45 – 13.50)

Correct Option

Solution :

13.46 (13.45 – 13.50)

$$T_{\text{avg}} = \frac{\text{Hit Time } L_1 + \text{Miss Rate } L_1 \times (\text{Hit Time } L_2 + \text{Miss Rate } L_2 \times \text{Miss Penalty } L_2)}{\text{Miss Rate } L_1}$$

$$\text{Miss Rate, } L_1 = \frac{55}{1000} = 0.055$$

$$\text{Miss Rate, } L_2 = \frac{25}{55} = 0.45$$

$$T_{\text{avg}} = 10 + 0.055 \times (18 + 0.45 \times 100)$$

$$= 10 + 0.055 \times 63$$

$$= 13.46$$

Q. 30

[FAQ](#) [Solution Video](#) [Have any Doubt ?](#)

A device with data transfer rate 40 KB/sec is connected to a CPU, where data transfer time between interfaces to memory or CPU is neglected. If the interrupt overhead is 2 μ sec, then minimum performance gain of operating the device under interrupt mode over operating it under program controlled mode _____. (Assume data transferred Byte wise) (Upto 1 decimal place)

 12.5 (12.2 – 12.5)

Correct Option

Solution :

12.5 (12.2 – 12.5)

Execution time of programmed IO mode :

$$1 \text{ sec} \rightarrow 40 \text{ KB}$$

$$1B \rightarrow \frac{1}{40K} = 25 \mu \text{ sec}$$

$$\Rightarrow S = \frac{25}{2} = 12.5$$

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ALL(33) CORRECT(0) INCORRECT(0) SKIPPED(33)

Q. 31

Solution Video

Have any Doubt?



Which of the following statements about I/O modes are correct?

- A** CPU takes care of the I/O operation in the programmed I/O modes because the I/O devices are directly connected to the system bus. Correct Option
- B** DMA module has direct access to the main memory and control over the system bus for transfer of the data. Correct Option
- C** DMA is efficient for transferring bulk amount of data and programmed I/O is efficient for small amount of data transfer. Correct Option
- D** None of these

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)
 All of the above statements are correct.

QUESTION ANALYTICS



Q. 32

FAQ

Solution Video

Have any Doubt?



Consider a RISC processor with an ideal CPI, where 25% of the total instructions are load and store instruction. Time to accessing main memory is 100 clock cycles and accessing of the cache memory required 2 clock cycles and cache miss rate is 2%. Which of the following are correct?

- A** The effective Cycle Per Instruction (CPI) for the system with the cache is 3.5 CPI.
- B** The effective CPI for the system with the cache is 5 CPI. Correct Option
- C** CPI for handling cache misses is 2.9.
- D** CPI for the handling cache hits is 2.45. Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - b,d

STATUS - SKIPPED

Solution :

(b, d)
 LOAD and STORE take 2 memory access, 1 for IF and 1 for loading/storing.
 So total memory access for 100 instruction

$$\begin{aligned} &= 100 \text{ (IF)} + 1 \times 0.25 \times 100 \text{ (loading/storing)} \\ &= 100 + 25 = 125 \text{ memory access} \end{aligned}$$

Average memory access/instruction

$$= \frac{125}{100} = 1.25 \text{ memory access/instruction}$$

Cycles per instruction for handling cache misses

$$\begin{aligned} &= \text{Memory accesses per instruction} \times \text{Miss rate} \times \text{Cycles per miss} \\ &= 1.25 \times 0.02 \times 1.02 = 2.55 \text{ Cycles per instruction} \end{aligned}$$

Cycles per instruction for handling cache hits

$$\begin{aligned} &= \text{Memory accesses per instruction} \times \text{Hit rate} \times \text{Cycles per hit} \\ &= 1.25 \times 0.98 \times 2 = 2.45 \text{ Cycles per instruction} \end{aligned}$$

$$\begin{aligned} \text{Effective CPI} &= \text{Cycles for hits} + \text{Cycles for misses} \\ &= 2.55 + 2.45 = 5 \end{aligned}$$

QUESTION ANALYTICS



Q. 33

FAQ

Solution Video

Have any Doubt?



Consider a system with instruction set that uses a fixed 16 bits instruction length and length of address is 6 bits. There are 10 two address instruction and 8192 zero address instructions. Which of the following are correct?

- A** Maximum 512 zero address instructions can be supported in the system.
- B** Maximum 256 one address instructions can be supported in the system. Correct Option
- C** Maximum 8192 zero address instructions can be supported in the system. Correct Option

D Maximum 64 one address instructions can be supported in the system.

YOUR ANSWER - NA

CORRECT ANSWER - b,c

STATUS - SKIPPED

Solution :

(b, c)



$$\text{Total number of opcode} = 2^4 = 16$$

$$\text{Remaining opcodes for one address instruction} = (16 - 10) = 6$$

$$\text{Possible 1 address instruction} = 2^6 \times 6$$

Consider there are 'n' one address instruction.

$$\text{Remaining opcodes for zero address instruction} = 2^6 \times 6 - n$$

Possible zero address instruction

$$(2^6 \times 6 - n) \times 2^6 = 8192$$

$$\text{By solving we get, } n = 256$$

QUESTION ANALYTICS



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CORRECT(0)

INCORRECT(0)

SKIPPED(17)

Q. 1

Solution Video

Have any Doubt?



The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29,154 KB from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____.

A 675**B** 456

Correct Option

C 3246**D** 2915

QUESTION ANALYTICS



Q. 2

FAQ

Solution Video

Have any Doubt?



A CPU generally handles an interrupt by executing an interrupt service routine.

A As soon as interrupt is raised.**B** By checking the interrupt register at the end of fetch cycle.**C** By checking the interrupt register after finishing the execution of the current instruction.

Correct Option

D By checking the interrupt register at fixed intervals.

QUESTION ANALYTICS



Q. 3

FAQ

Solution Video

Have any Doubt?



Which of the following is TRUE?

A A direct mapped cache has higher hit time than a 4-way set associative cache with same number of sets.**B** Two 4 KB caches of same block size, but with different associativity will always have same hit rate.**C** A set associative cache has lower number of conflict misses than a direct mapped cache of same size.

Correct Option

D During a cache miss, there will be block replacements in a fully associative case if at least one of the cache location is empty.

QUESTION ANALYTICS



Q. 4

FAQ

Solution Video

Have any Doubt?



For a cache memory of given capacity, as block size increases, there is

A An increase in compulsory misses and a decrease in conflict misses.

B A decrease in compulsory misses and conflict misses.

C An increase in compulsory misses and conflict misses.

D A decrease in compulsory misses and increase in conflict misses.

Correct Option

Solution :

(d)

As the block size increases in cache memory then more number of words get fetched at a time and hence compulsory misses can be decrease but conflict misses increases since number of lines (in direct mapped cache) or number of sets (in set associative cache) will decrease leading to more number of blocks into same line or set.

QUESTION ANALYTICS



Q. 5

Solution Video

Have any Doubt ?



Which cache write mechanism allows updated memory location in the cache to remain out of data in memory. Until the block containing the updated memory location is replaced in the cache?

A Write through

B Write back

Correct Option

Solution :

(b)

In write back updating technique, block containing the data in cache and same block data in main memory may hold different data at a time. This happens due to Asynchronous Updating Technique.

C Both write through and write back

D None of the above

QUESTION ANALYTICS



Q. 6

FAQ

Solution Video

Have any Doubt ?



Consider the following statements for memory mapped I/O scheme.

- I. The I/O device and the memory have separate address space.
- II. The I/O device and the memory shares same address space.
- III. No special command for I/O is needed.

IV. Needs I/O or memory select line.
The number of the correct statements is/are _____.

2

Correct Option

Solution :

2

- In memory mapped I/O scheme, a part of memory space is used for I/O and is used as same as other address space. It does not require any special hardware or command.
- Statement II and III are correct.

QUESTION ANALYTICS



Q. 7

FAQ

Solution Video

Have any Doubt ?



Consider a write through cache memory having the hit ratio for the read operation 80% and access time of 50 ns. Main memory access time is 200 ns. CPU generates 70% read requests and remaining are used for write operation. What is the average memory access time when considering both read and write operation?

116

Correct Option

Solution :

116

$$\begin{aligned}T_{\text{avg read}} &= H_r T_c + (1 - H_r) T_m \\T_{\text{avg read}} &= 40 + 40 = 80 \text{ ns} \\T_{\text{avg write}} &= H_w T_m = 200 \text{ ns} \\T_{\text{avg write through}} &= f_r \times T_{\text{avg read}} + f_w \times T_{\text{avg write}} \\&= 0.7 \times 80 + 0.3 \times 200 = 116 \text{ ns}\end{aligned}$$

QUESTION ANALYTICS



Q. 8

Solution Video

Have any Doubt ?



External interrupt may arise because of

- A Timing device Correct Option
- B External source Correct Option
- C I/O device Correct Option
- D Illegal or erroneous use of instruction

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)

An external interrupt is a computer system interrupt that happens as a result of outside interference, whether that's from the user, from peripherals, from other hardware devices or through a network. These are different than internal interrupts that happen automatically as the machine reads through program instructions.

External Interrupt may be a case of which rises up due to an illegal use of instruction.

 QUESTION ANALYTICS



Q. 9

? FAQ

▶ Solution Video

⌚ Have any Doubt ?



Consider the following statements:

- (a) It increases the maximum I/O transfer rate.
- (b) It reduces the interface by the DMA controller in the CPU's memory access.
- (c) It is beneficially employed for I/O devices with shorter bursts of data transfer.
- (d) Cycle stealing is one of the type of addressing modes.

Which of the above statement(s) is/are true about cycle stealing in DMA?

- A a Correct Option
- B b Correct Option
- C c Correct Option
- D d

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)

 QUESTION ANALYTICS



Q. 10

? FAQ

▶ Solution Video

⌚ Have any Doubt ?



Which of the following statements are true?

- S_1 : Doubling the line size halves the number of tags in the cache.
- S_2 : Doubling the associativity increases the number of tags in the cache.
- S_3 : Doubling the line size usually reduce compulsory misses.

- A Only S_1 and S_3
- B Only S_1 and S_2
- C Only S_2 and S_3
- D All of the statements Correct Option

Solution :

(c)

- S_1 is correct.
- S_2 is correct tag bits increases when associativity is increased.
- S_3 is also correct.

 QUESTION ANALYTICS





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? FAQ ▶ Solution Video 🤔 Have any Doubt ?



Q. 11

Consider a computer system has a main memory consisting of 2M 16 bit words. It also has a 8K-word cache organized in the block set associative manner, with 4 blocks per set and 32 words per block. What is the number of bits in each of the TAG, SET and word field of main memory address format?

A 10, 6, 5

Correct Option

Solution :

(a)

TAG	SET offset	Word offset
-----	------------	-------------

- Word offset = 1 block = 32 words = 5 bit
- CM size = 8 K-word
- Number of lines = $\frac{\text{CM Size}}{\text{Block Size}} = \frac{2^{13}}{2^5} = 2^8$
- Number of set = $\frac{\text{Number of lines}}{\text{Number of blocks per set}} = \frac{2^8}{2^2} = 2^6$

2M word MM $\rightarrow \log_2 2M = 21$ bit

21 bit		
TAG	SET offset	Word offset

10 bit 6 bit 5 bit

B 12, 5, 5

C 8, 8, 6

D 8, 6, 8

QUESTION ANALYTICS



Q. 12

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A program is stored in a 16 MB main memory that is attached to a 4 KB direct mapped cache with a block size of 16 bytes. The program reads 4 data words A, B, C and D in that order 100 times (total 400 memory references). Let the physical addresses of A, B, C and D are 0x420424, 0x74042A, 0x740664, 0x740660 respectively. Assume that caches are initially empty and one word is 2 bytes. Consider the following statements:

- Every access to B will result in removal of A from the cache.
 - Out of the 400 memory references, there are exactly 201 cache misses.
 - Every access to D is a cache hit.
 - At the end of 400 memory references A, B, C and D are located inside the cache.
- Which of the above statements is/are TRUE?

A I and III only

Correct Option

Solution :

(b)

Physical address is broken as:

12 bits	8 bits	4 bits
Tag	Line offset	Block offset

A: 0x 420 42 4 \rightarrow line number 42
 B: 0x 740 42 A \rightarrow line number 42

Both A and B are in different block.

C: 0x 740 66 4 \rightarrow line number 66
 D: 0x 740 66 0 \rightarrow line number 66

Both C and D are in same block.

Note : Tag bits of A and B are different while line number is same. Thus every access to B, remove A.

Both C and D are having same line number as well as tag bits. Thus, fetching C also fetches D.

Hence, I is true,

II is true as 100 misses for A, 100 misses for B and 1 misses for both C and D.

Sequence:

A B C D A B C D A B C D
 miss miss miss hit miss miss hit hit miss miss hit hit

III is true.

IV is false as A will not be in the cache.

C III only

D I, II, III and IV

Q. 13

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Consider 2 MBPS I/O device interfaced to 64 bit CPU in a programmed-I/O mode. Data transmission between the CPU and I/O in word-wise. Interrupt overhead is 3 μ sec. What is the performance gain when the device is operating under interrupt-I/O over programmed-I/O mode?

 A 2 B 2.5 C 1.33

Correct Option

Solution :

(c)

Prog. I/O : CPU time depends on I/O speed.

$$\text{i.e., } 2 \text{ MB} = 1 \text{ sec}$$

$$8 \text{ B (1 word)} = ?$$

$$ET_{\text{Prog-I/O}} = \frac{8 \text{ B}}{2 \text{ MB}} \text{ sec} = 4 \mu\text{sec}$$

INT I/O : CPU time depends on interface latency.

$$ET_{\text{INT-I/O}} = 3 \mu\text{sec}$$

$$S = \frac{ET_{\text{Prog-I/O}}}{ET_{\text{INT-I/O}}} = \frac{4}{3} = 1.33$$

So, option (c) is the correct answer.

 D 2.66

Q. 14

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Assume in a system doubling the cache size reduces the miss rate by around 20%. If a memory system consists of a single external cache with an access time of 30 ns, size is 128 kB and a hit rate of 80% and a main memory with an access time of 60 ns. What is the expected percentage improvement in the effective access time if we change given cache size to 512 kB? (Upto 1 decimal place)

 C 10.2 (10.0 - 10.3)

Correct Option

Solution :

10.2 (10.0 - 10.3)

$$T_{\text{avg}} = H_c T_c + (1 - H_c) [T_m + T_c]$$

$$= 0.8 \times 30 + 0.2 (60 + 30)$$

$$= 24 + 18 = 42 \text{ ns}$$

$$T_{\text{avg new}} = 0.872 \times 30 + 0.128 (60 + 30)$$

$$= 26.16 + 11.52 = 37.68 \text{ ns}$$

$$\text{Expected improvement} = \frac{42 - 37.68}{42} = 0.102 = 10.2\%$$

Q. 15

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An interrupt driver I/O device that transfers data at 20 KB/sec. Consider interrupt processing takes 700 μ sec i.e., time to jump to ISR, execute it and return to main program. The fraction of processor time consumed by this I/O device if interrupts occur for every byte is _____. (Upto 2 decimal places)

 C 0.07 (0.06 - 0.08)

Correct Option

Solution :

0.07 (0.06 - 0.08)

$$\text{Data transfer} = 20 \text{ KB/sec}$$

$$1 \text{ sec} = 20 \text{ KB}$$

$$? \text{ sec} = 1 \text{ B}$$

$$= \frac{1}{20 \text{ K}} \text{ sec} = 0.05 \text{ msec} = 50 \mu\text{s}$$

Interrupt Processing Time = 700 μ s

So, percentage of processor time consumed by I/O device

$$= \frac{50 \mu\text{s}}{700 \mu\text{s}} = 0.07$$

0.16

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Consider the following statements:

- (a) Time taken for a single instruction on a pipelined CPU is less than or equal to time taken on a non-pipelined (identical) CPU.
- (b) In a uniform delay pipeline execution time for a single instruction is equal to the execution time in non-pipelined processor. (Assume no buffer delay).
- (c) Linear pipeline latency is always 1.
- (d) Non linear pipeline latency is always 1.

Which of the above statement(s) is/are correct?

A a

B b

Correct Option

C c

Correct Option

D d

YOUR ANSWER - NA

CORRECT ANSWER - b,c

STATUS - SKIPPED

Solution :

- (b, c)
- (a) For a single instruction time taken on pipeline CPU is always greater than or equal to the nonpipeline.
- (b) When all stages have same delay and buffer latency is zero then for a single instruction execution time of pipeline CPU is equal to the execution time of non-pipeline CPU.
- (c) True
- (d) False

QUESTION ANALYTICS



Q. 17

FAQ

Solution Video

Have any Doubt ?



Consider the following procedures. Assume that the pipeline registers have zero latency.

P_1 : 4 stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.

P_2 : 4 stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.

P_3 : 5 stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.

P_4 : 5 stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which procedure has clock frequency less than 1 GHz?

A P_1

Correct Option

B P_2

Correct Option

C P_3

D P_4

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,d

STATUS - SKIPPED

Solution :

(a, b, d)

It is given that pipeline registers have zero latency. Thus, Cycle time
= Maximum delay due to any stage + Delay due to its register
= Maximum delay due to any stage

P_1 :

$$\text{Cycle time} = \text{Max}\{1 \text{ ns}, 2 \text{ ns}, 2 \text{ ns}, 1 \text{ ns}\} = 2 \text{ ns}$$

$$\text{Clock frequency} = \frac{1}{\text{Cycle time}} = \frac{1}{2 \text{ ns}} = 0.5 \text{ gigahertz}$$

P_2 :

$$\text{Cycle time} = \text{Max}\{1 \text{ ns}, 1.5 \text{ ns}, 1.5 \text{ ns}, 1.5 \text{ ns}\} = 1.5 \text{ ns}$$

$$\text{Clock frequency} = \frac{1}{\text{Cycle time}} = \frac{1}{1.5 \text{ ns}} = 0.67 \text{ gigahertz}$$

P_3 :

$$\text{Cycle time} = \text{Max}\{0.5 \text{ ns}, 1 \text{ ns}, 1 \text{ ns}, 0.6 \text{ ns}, 1 \text{ ns}\} = 1 \text{ ns}$$

$$\text{Clock frequency} = \frac{1}{\text{Cycle time}} = \frac{1}{1 \text{ ns}} = 1 \text{ gigahertz}$$

P_4 :

$$\text{Cycle time} = \text{Max}\{0.5 \text{ ns}, 0.5 \text{ ns}, 1 \text{ ns}, 1 \text{ ns}, 1.1 \text{ ns}\} = 1.1 \text{ ns}$$

$$\text{Clock frequency} = \frac{1}{\text{Cycle time}} = \frac{1}{1.1 \text{ ns}} = 0.91 \text{ gigahertz}$$

QUESTION ANALYTICS



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