DIGITAL ELECTRONICS 12

COMPLETE DIGITAL ELECTRONICS IN 2 HOURS

GATE CRASH COURSE

Chandan sir

ABOUT ME

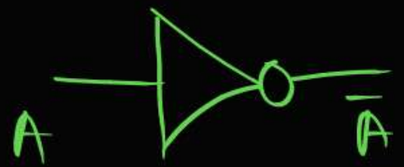
- Cleared Gate Multiple times with double Digit Rank (AIR 23, AIR 26)
- Qualified ISRO Exam
- Mentored More then 1 Lakhs+ Students (Offline & Online)
- More then 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs

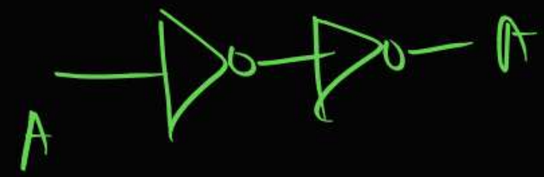
Chandan Jha

मंजिल यूँ ही नही मिलती राही को
जुनून सा दिल में जगाना पड़ता है,
पूछा चिड़िया से कि घोसला कैसे बनता है
वो बोली कि तिनका तिनका उठाना पड़ता है..

LOGIC GATE

NOT GATE





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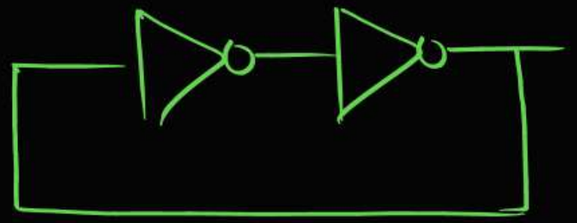
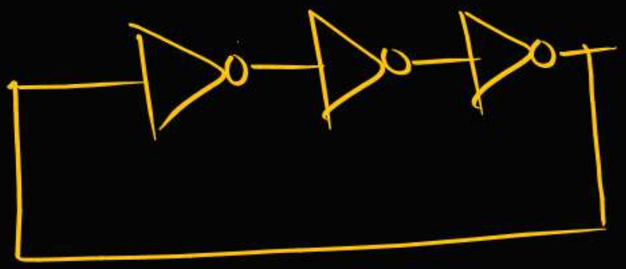


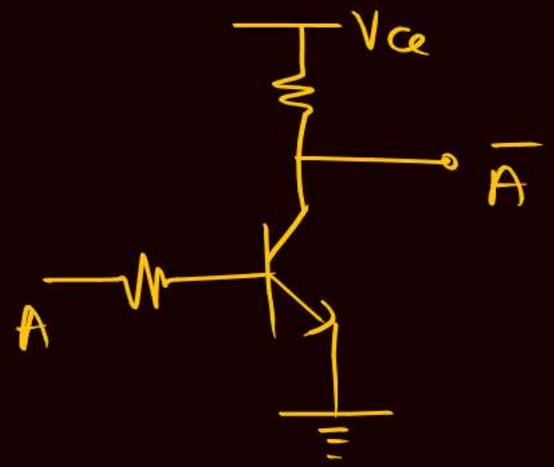
Basic memory element
Bistable Multivibrator



Astable Multivibrator
Square wave generato.

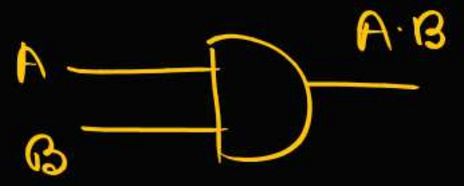
Clock gen.
free Runing Ckt
Ring oscillator

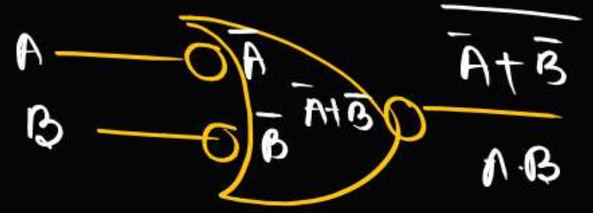
$$f = \frac{1}{2N \times t_{pd}}$$


Vcc
$\overline{A}$
A

LOGIC GATE

AND GATE





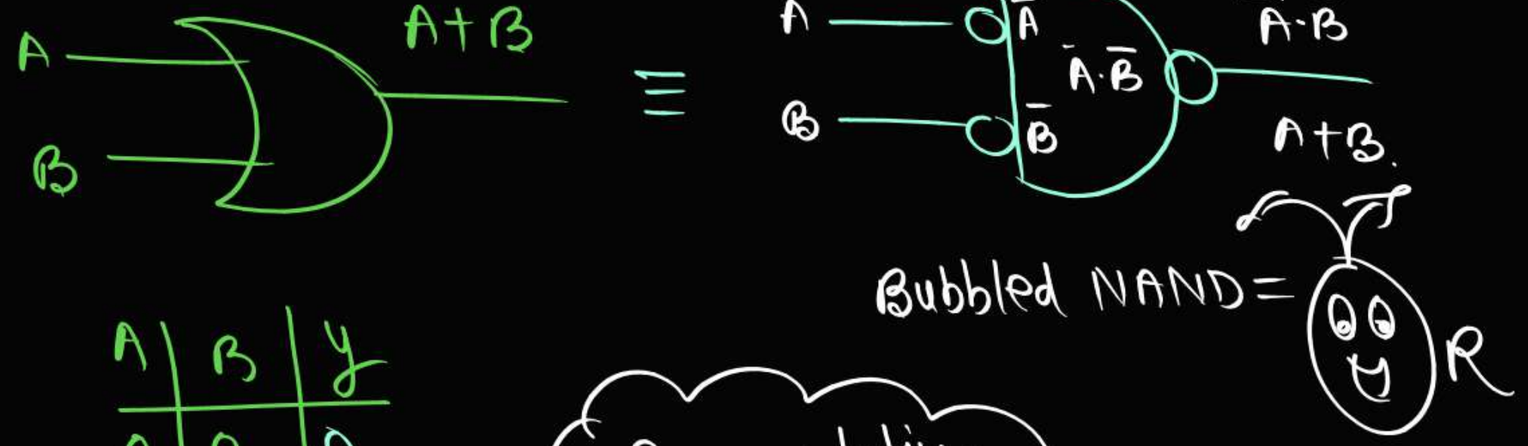
Bubbled NOR ≡ AND

Commutative
Associative Law ✓

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

LOGIC GATE

OR GATE



TTL ⟶ 1

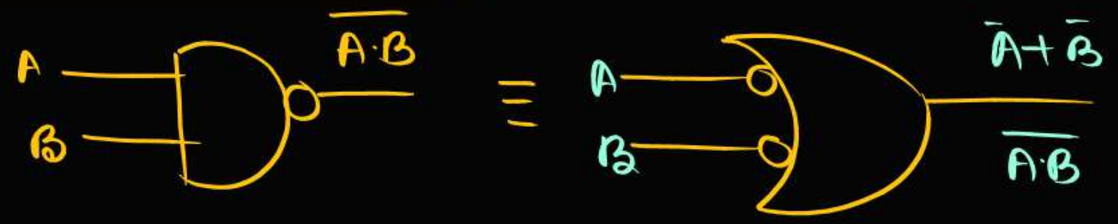
ECL ⟶ 0

A	B	y
0	0	0
0	1	1
1	0	1
1	1	1

Commutative
Associative Law ✓

LOGIC GATE

NAND GATE



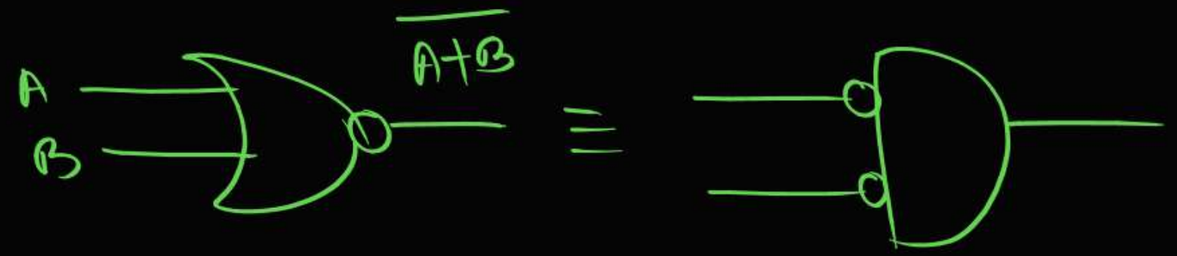
A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

Commutative Law ✓

Associative Law ✗

LOGIC GATE

NOR GATE



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Commutative Law ✓

Associative Law ✗

Universal Logic

NAND

NOR

- $\overline{A \cdot B}$
- $\overline{A+B}$
- $\bar{A}+B$
- $A+\bar{B}$
- $\bar{A} \cdot B$
- $A \cdot \bar{B}$
- MUX
- Decoder + OR

LOGIC GATE

XOR GATE

A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

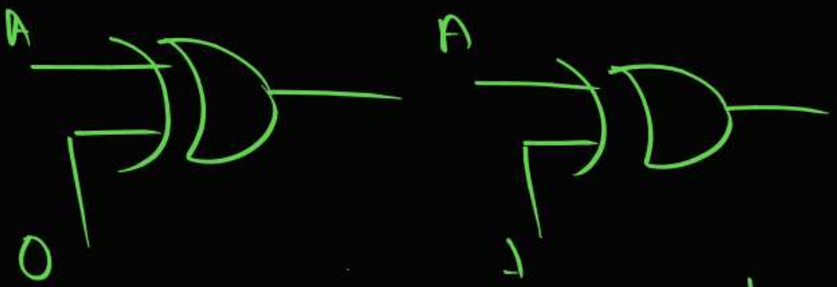
$A \oplus A = 0$

$A \oplus 0 = A$

$A \oplus \bar{A} = 1$

$A \oplus 1 = \bar{A}$

$A \oplus A \oplus \cdots \oplus A = \begin{cases} 0 & \text{Even no. of A} \\ A & \text{Odd no of A} \end{cases}$



Buffer

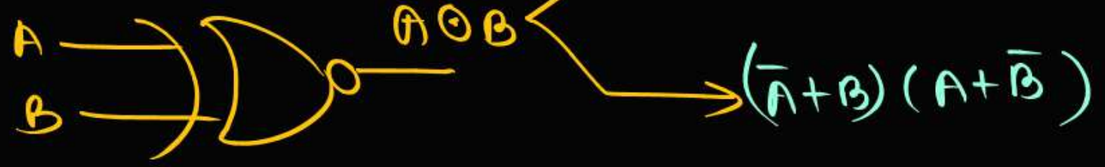
Inverter

$A \oplus B \oplus C = \Sigma m(1,2,4,7)$

$A \oplus B = \bar{A} \oplus \bar{B} = \bar{A} \odot B = A \odot \bar{B}$

LOGIC GATE

XNOR GATE



A	B	A⊙B
0	0	1
0	1	0
1	0	0
1	1	1

$A \odot A = 1$

$A \odot 1 = A$

$A \odot \bar{A} = 0$

$A \odot 0 = \bar{A}$

$A \odot B = \bar{A} \oplus B = A \oplus \bar{B} = \overline{A \oplus B} = \bar{A} \odot \bar{B}$

$\overline{A \oplus B} = A \odot B$

$(A \odot B) \odot C = A \oplus B \oplus C$

BOOLEAN ALGEBRA

THEOREM

- Distribution Theorem $A+BC=(A+B)(A+C)$
- Consensus Theorem $AB+\bar{A}C+BC=AB+\bar{A}C$
- Transpose Theorem $(A+B)(\bar{A}+C)=AC+\bar{A}B$
- D Morgan's Law $\overline{AB}=\bar{A}+\bar{B}$

$\overline{A+B}=\bar{A}\cdot\bar{B}$

K MAP

→ Gray code.

→ cyclic code

unity haming distance code.

Reflecting code.

Rule of minimization

#CJ_BABA_RULE

→ Kam se kam group banana hai and Bade se bada group banana hai.

kam group → terms will minimize

bada group → Variables minimize.

2^n → n Variable Reduce

"n" Variable: 2^k group $k \leq n$

how many Variables are present in that term → $n-k$

COMBINATIONAL CIRCUIT

COMPARATOR

"n" bit Comparator

Total combination $= 2^{2n}$

Equal combination $= 2^{n}$

Unequal combination $= 2^{2n} - 2^{n}$

Greater = Less $= \frac{2^{2n} - 2^{n}}{2}$

Seminimized.

$A > B \Rightarrow A_1\bar{B}_1 + (A_1 \odot B_1)A_0\bar{B}_0$

$A < B \Rightarrow \bar{A}_1 B_1 + (A_1 \odot B_1)\bar{A}_0 B_0$

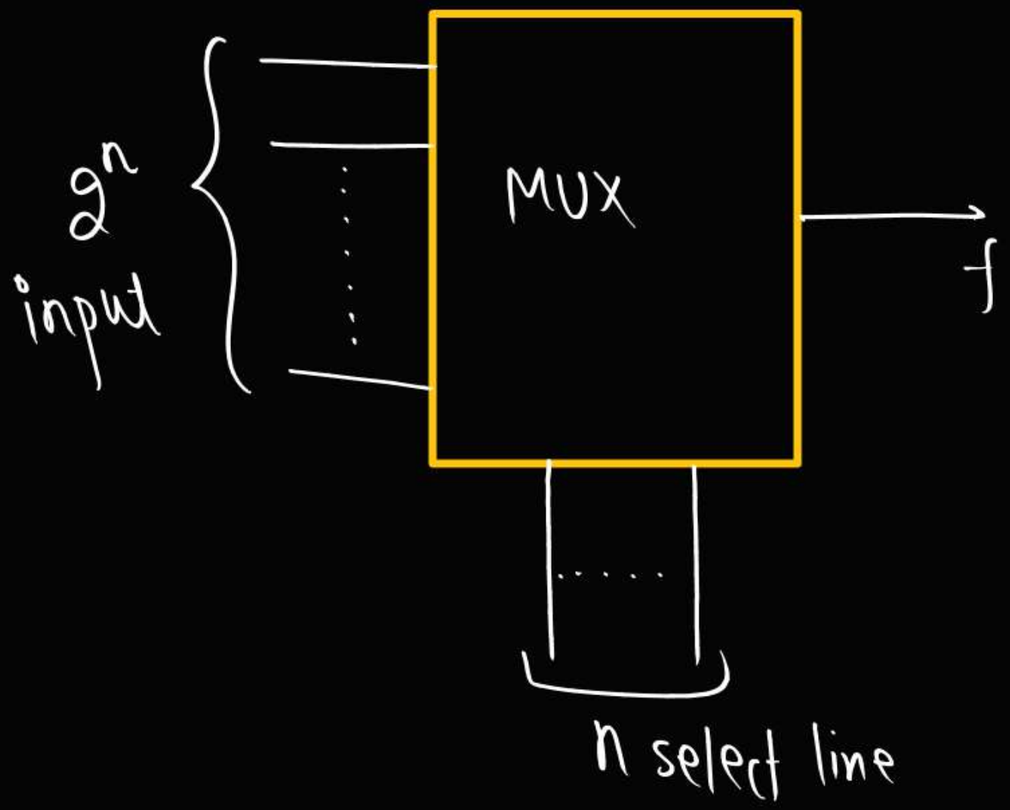
$A = B \Rightarrow (A_1 \odot B_1) \cdot (A_0 \odot B_0)$

COMBINATIONAL CIRCUIT

MULTIPLEXER

→ universal logic

→ AND-OR Logic



COMBINATIONAL CIRCUIT

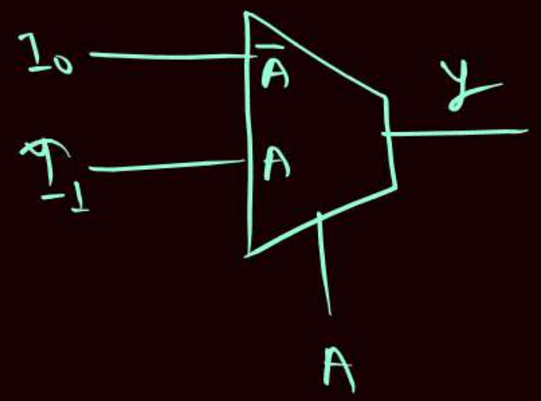
MULTIPLXER

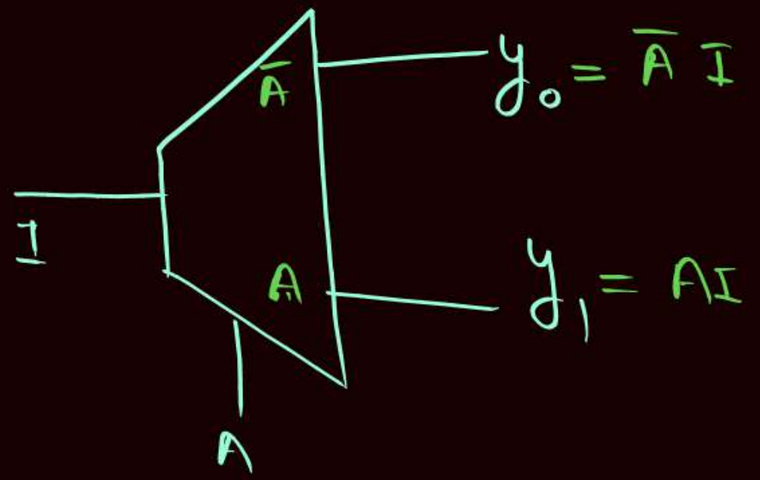
- Designing of Higher Order Mux
- MUX as Universal Logic
- Minimization
- Cascading of MUX
- Implementation of Function
- Delay in MUX

$4\times1 \xrightarrow[4+1=5]{\frac{16}{4}+\frac{4}{4}} 16\times1$ MUX

NOT, AND, OR → One 2×1 MUX

NAND, NOR, XOR, XNOR → Two 2×1 MUX

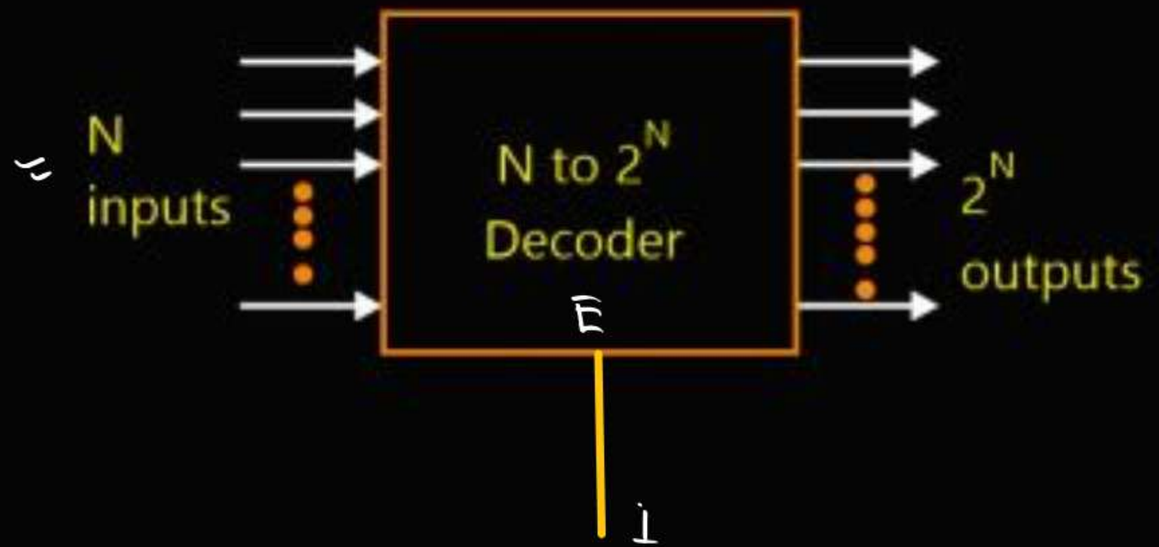

I_0
I_1
$\bar{A}$
A
Y
A


$\bar{I}$
$\bar{A}$
A
$y_0 = \bar{A}\,\bar{I}$
$y_1 = A\bar{I}$
A

COMBINATIONAL CIRCUIT

DECODER → A circuit which convert binary into any other code.

- 2 × 4 Decoder
- 3 × 8 Decoder
- 4 × 16 Decoder



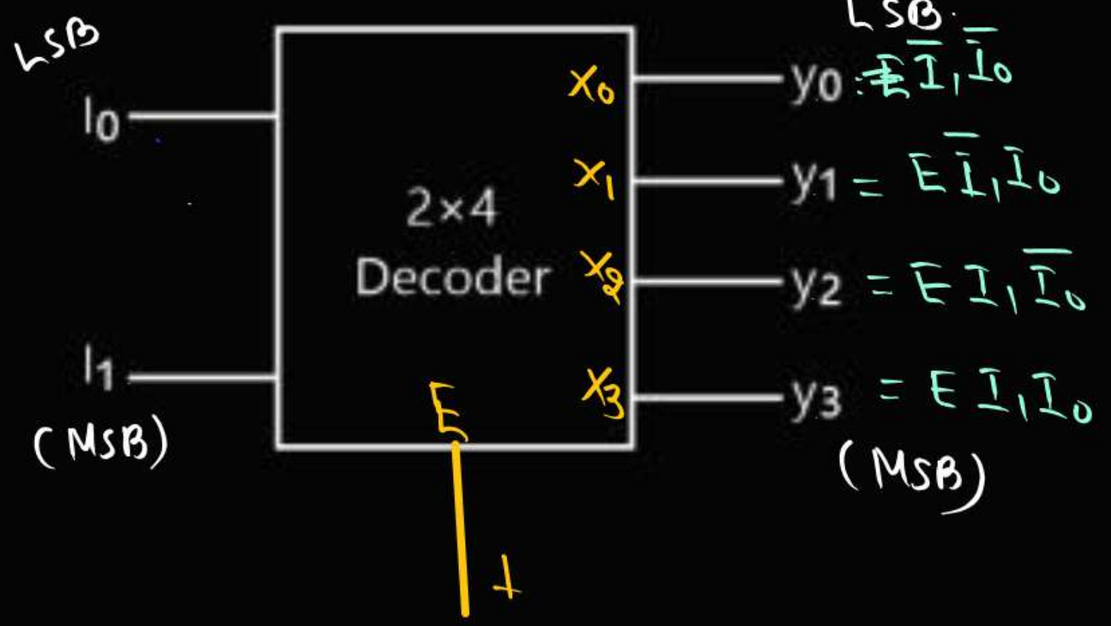
COMBINATIONAL CIRCUIT

inputs ↓ ⌜ outputs

2 X 4 DECODER

$y_0 = \bar{I}_1 \bar{I}_0$ $y_2 = I_1 \bar{I}_0$

$y_1 = \bar{I}_1 I_0$ $y_3 = I_1 I_0$

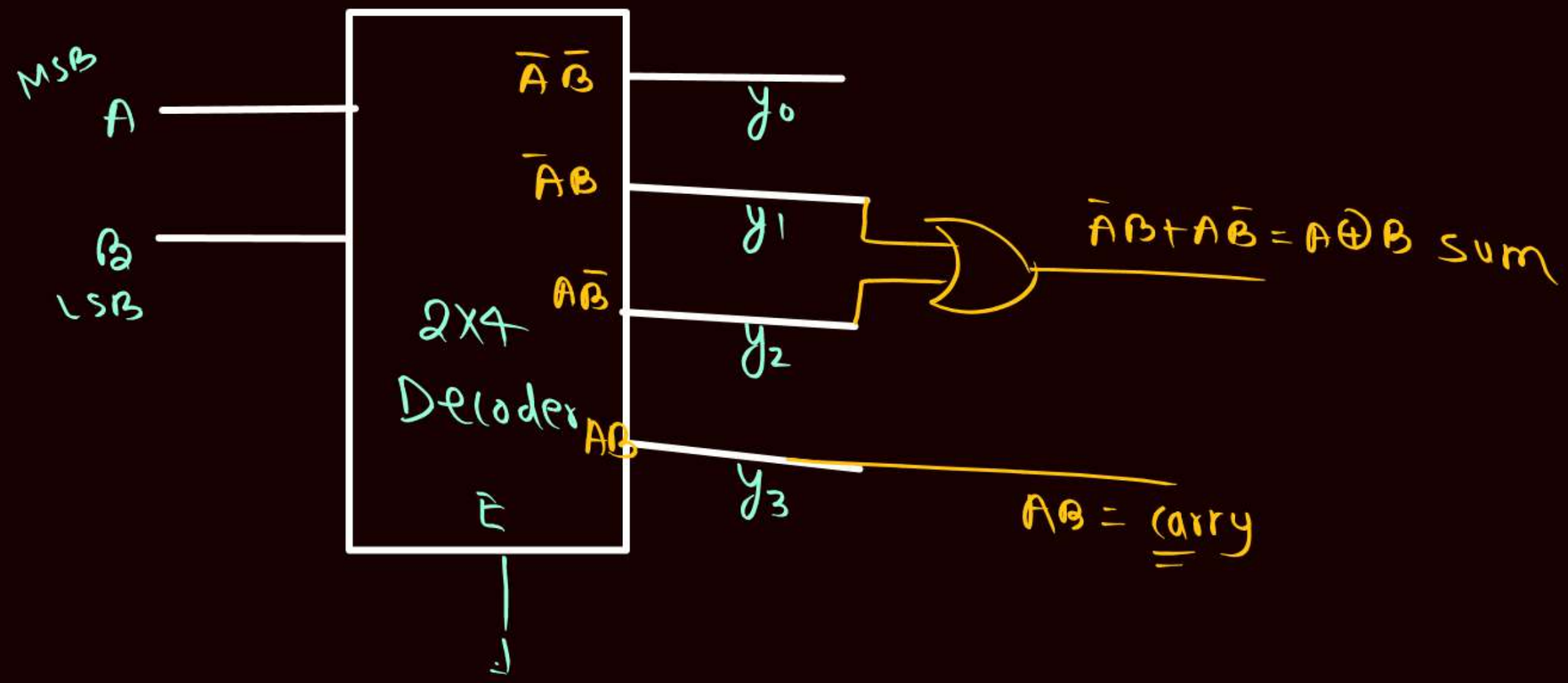


I_1	I_0	y_0	y_1	y_2	y_3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

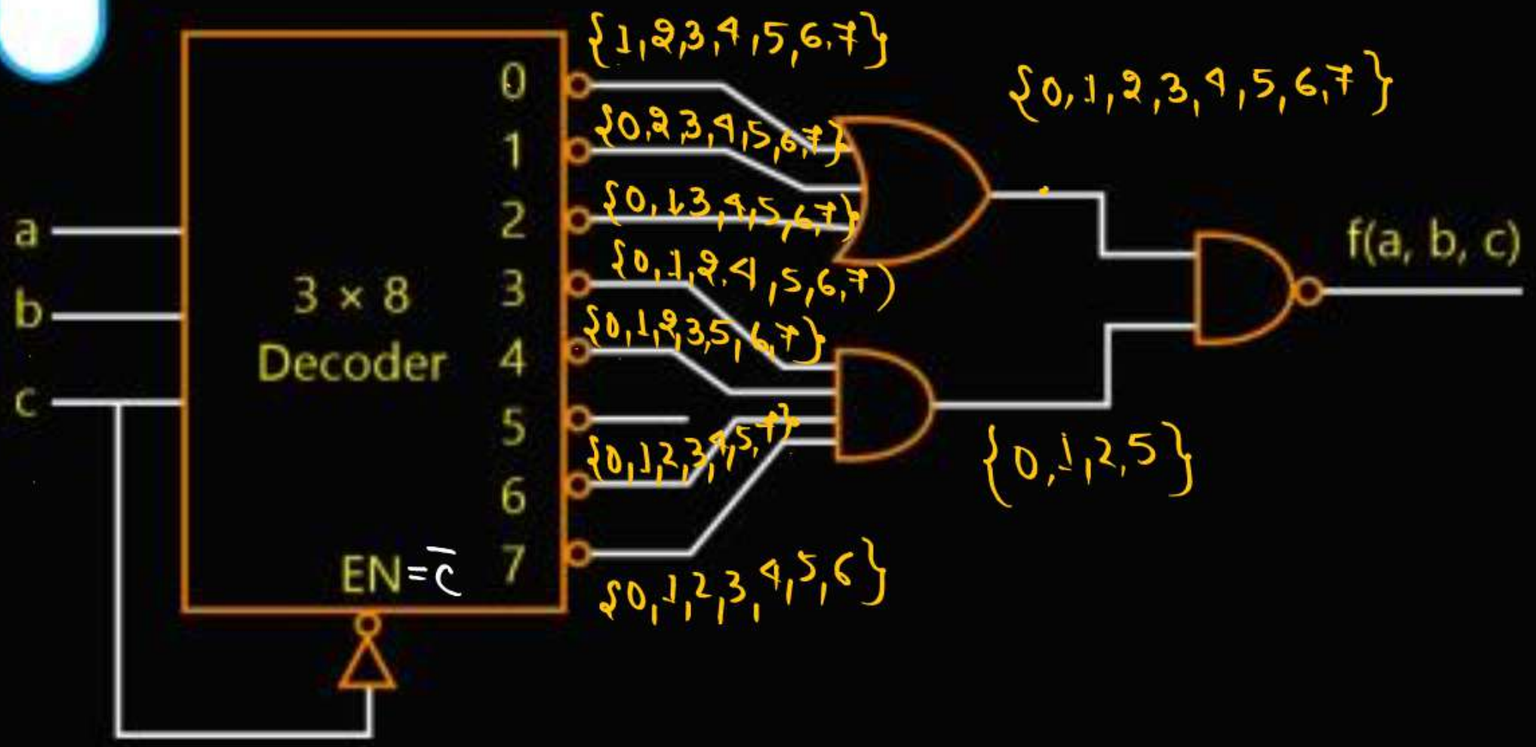
HA

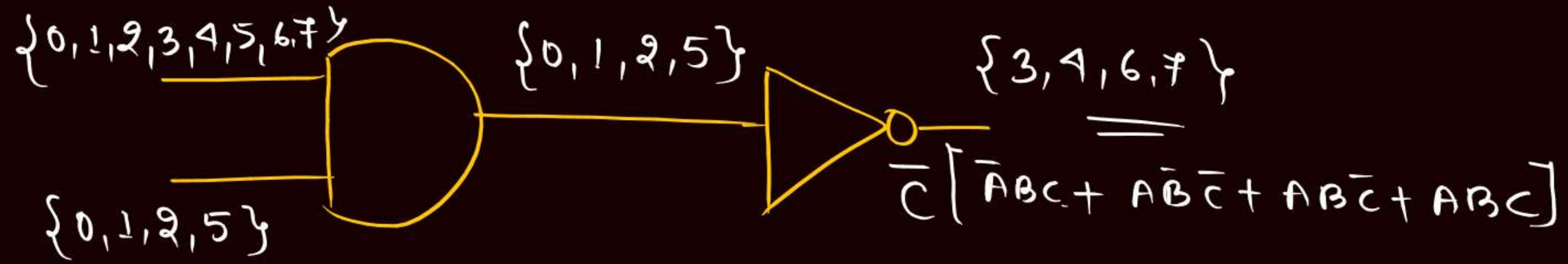
Sum = A ⊕ B

Carry = AB



Q. The Boolean expression f(a, b, c) in its canonical form for the decoder circuit shown below is-




{0,1,2,3,4,5,6,7}
{0,1,2,5}
{0,1,2,5}
{3,4,6,7}
$\overline{C}[\bar{A}BC + A\bar{B}\bar{C} + AB\bar{C} + ABC]$

HW

A logic circuit consist of two 2 × 4 decoders as shown in the figure. The output of decoder are as follow:

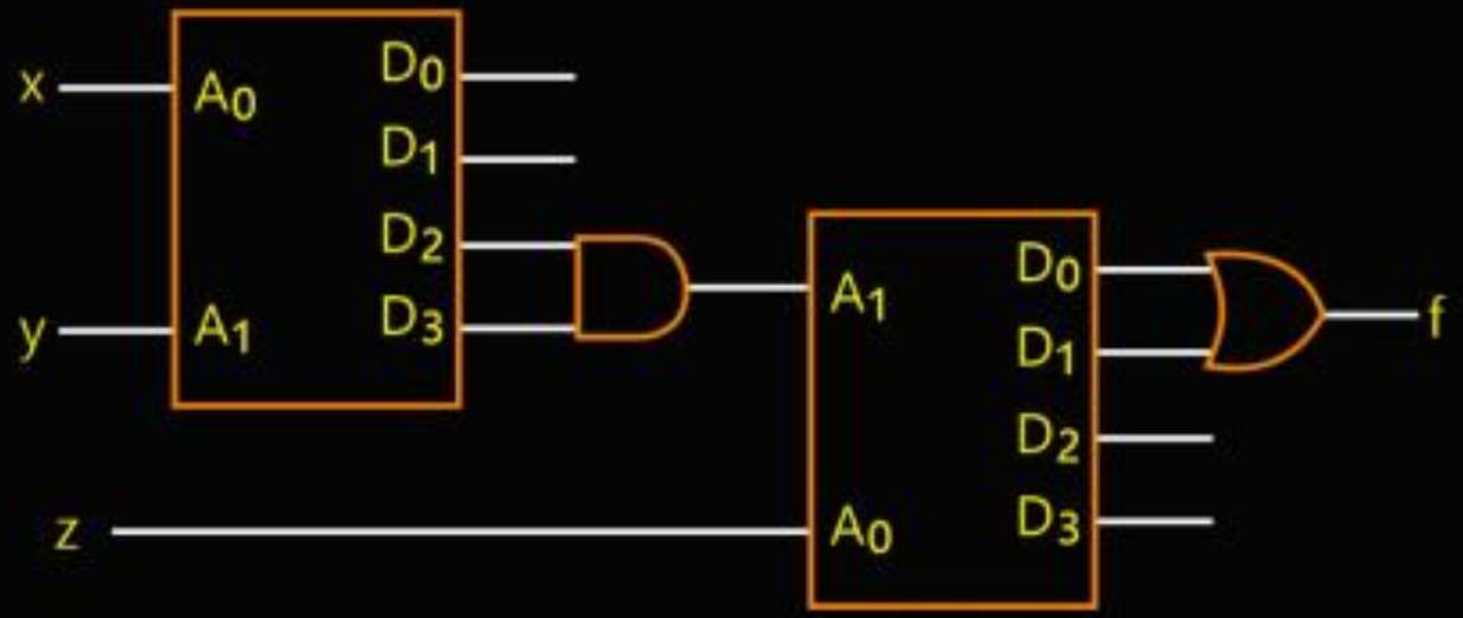
D0 = 1 when A0 = 0, A1 = 0

D1 = 1 when A0 = 1, A1 = 0

D2 = 1 when A0 = 0, A1 = 1

D3 = 1 when A0 = 1, A1 = 1

The value of f(x, y, z) is



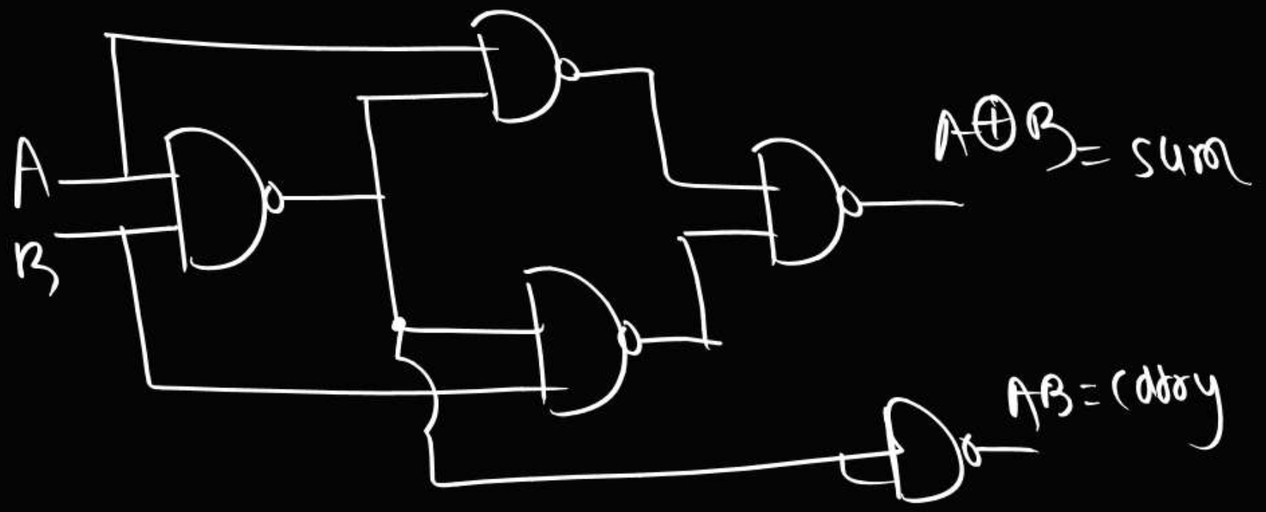
COMBINATIONAL CIRCUIT

HALF ADDER

$Sum = \bar{A}B + A\bar{B} = A \oplus B$

$Carry = AB$

NAND
NOR
} 5



COMBINATIONAL CIRCUIT

FULL ADDER

$$\text{Sum} = A \oplus B \oplus C$$

$$\text{Carry} = \Sigma m(3,5,6,7)$$

$$= AB + BC + AC$$

$$= (A \oplus B)C + AB$$

NAND = 9

COMBINATIONAL CIRCUIT

HALF SUBTRACTOR

NAND
NOR } (5)

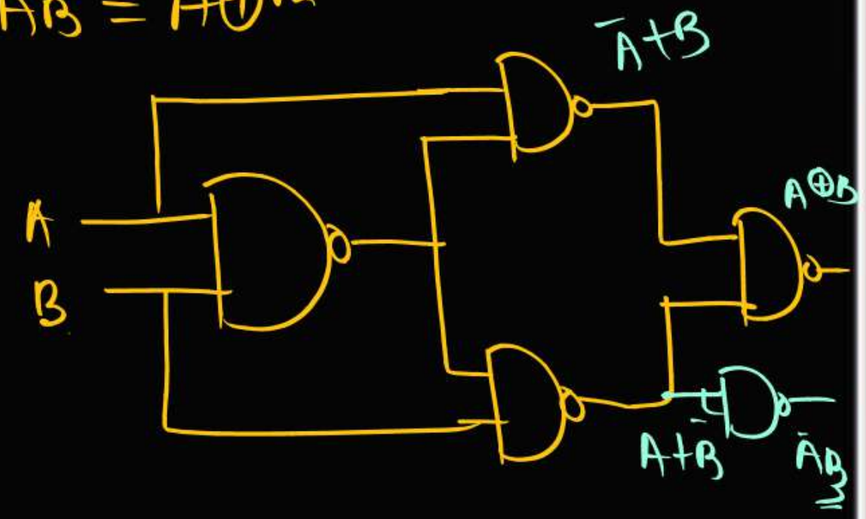
A	B	Diff	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$0-0=00 \qquad 1-0=01 \qquad 1-1=00 \qquad 0-1=11$$

Borrow, Difference

$$\text{Difference} = \bar{A}B + A\bar{B} = A \oplus B$$

$$\text{Borrow} = \bar{A}B$$



COMBINATIONAL CIRCUIT

HW

FULL SUBTRACTOR

→ NAND → 9

$(A-B)-C$

A	B	C	Diff	Borrow
0	0	0		
0	0	1		

COMBINATIONAL CIRCUIT

PARALLEL ADDER

Case(1) T_{sum}, T_{carry}

$$T = (n-1)T_{carry} + \text{Max}\{T_{sum}, T_{carry}\}$$

Case(2) XOR/AND/OR.

$$T = (n-1)\{T_{AND} + T_{OR}\} + T_{sum}$$

Case(3) when input to the parallel adder is given.

Figure I show a 4-bits ripple carry adder realized using full adders and Figure II shows the circuit of a full-adder (FA). The propagation delay of the XOR, AND and OR gates in Figure II are 20 ns, 15 ns and 10 ns respectively. Assume all the inputs to the 4-bit adder are initially reset to 0.

At t=0, the inputs to the 4-bit adder are changed to

X3X2X1X0 = 1100, Y3Y2Y1Y0 = 0100,

And Z0 = 1

The output of the ripple carry adder will be stable at t (in ns) =

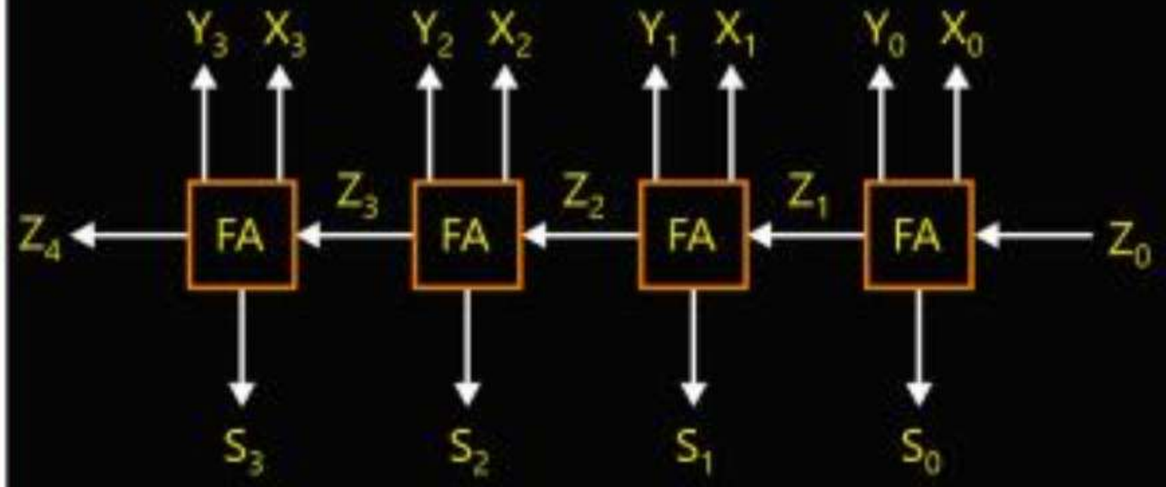


Figure-I

Ans = 50 ns.

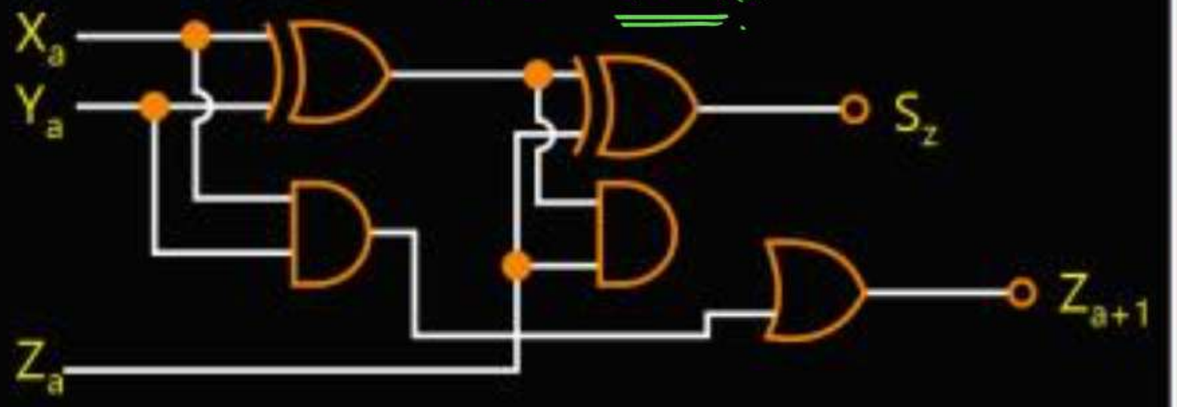
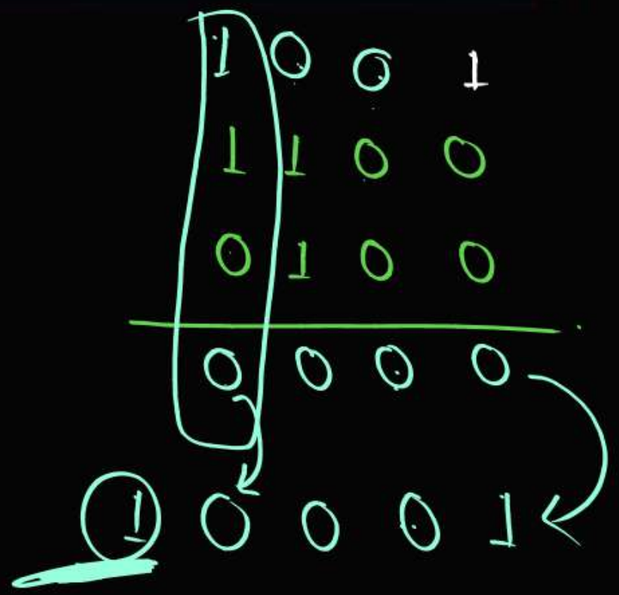
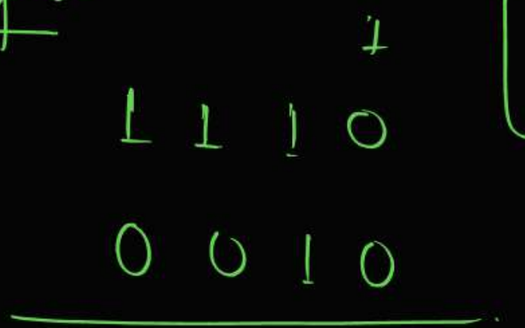


Figure-II

4 bit Parallel Adder



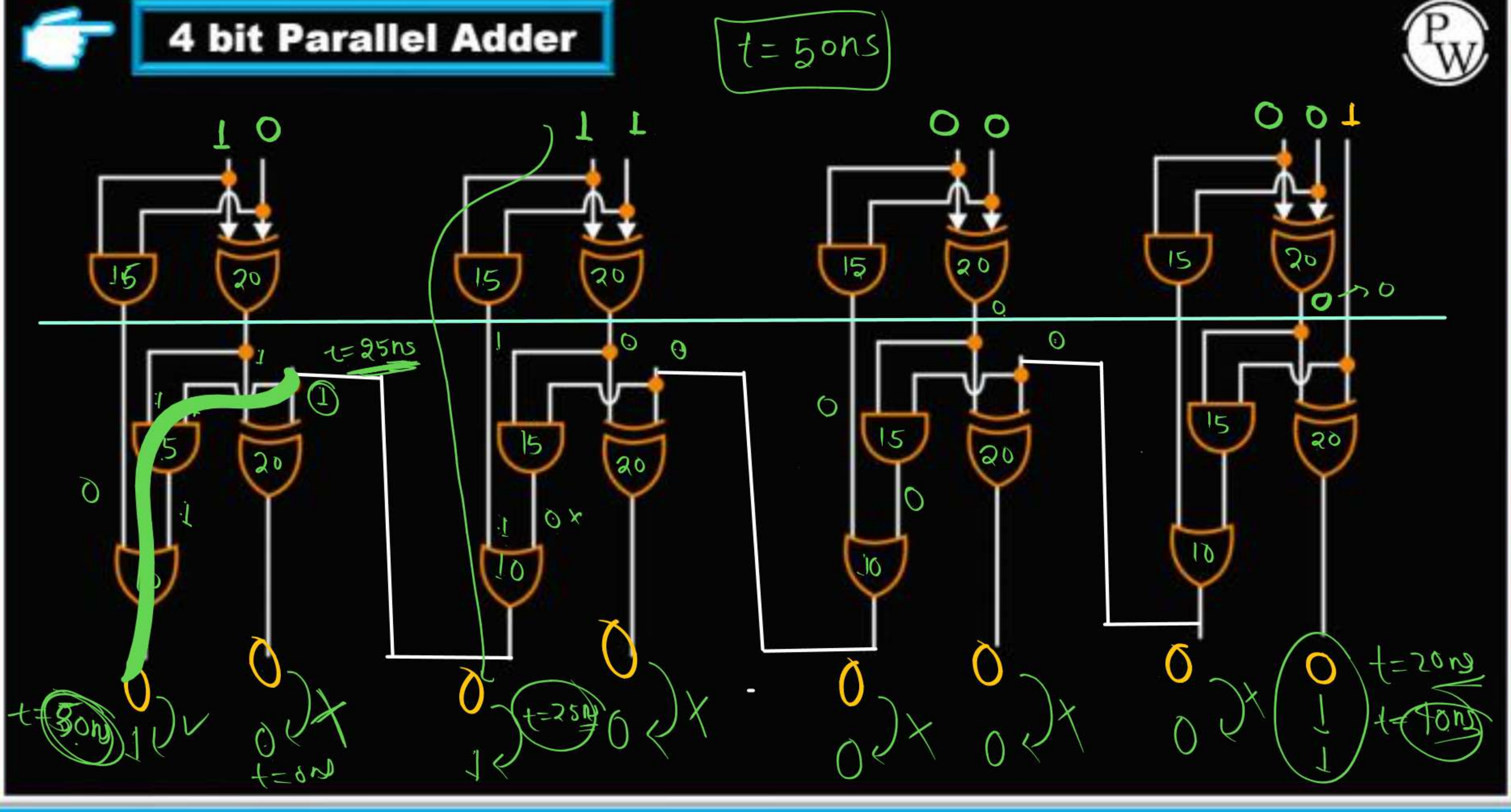
input



Comment Box

4 bit Parallel Adder

t = 50ns



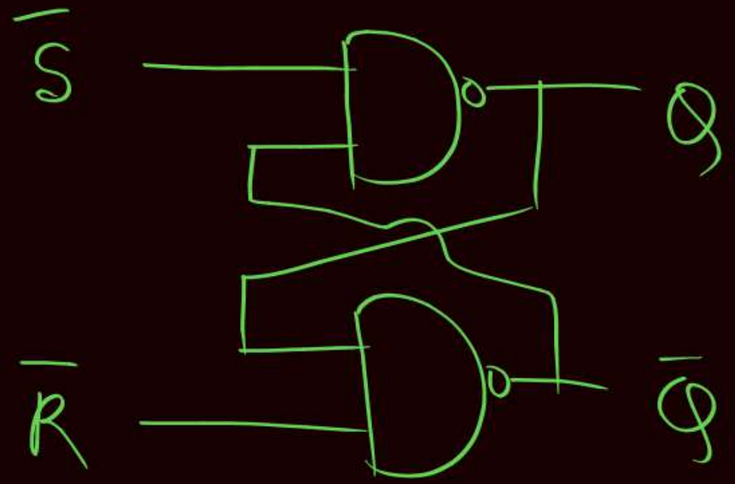
SEQUENTIAL CIRCUIT

FLIP FLOP

- Circuit Diagram
- Truth Table
- Characteristic Table
- Characteristic Equation
- Excitation Table

State Diagram

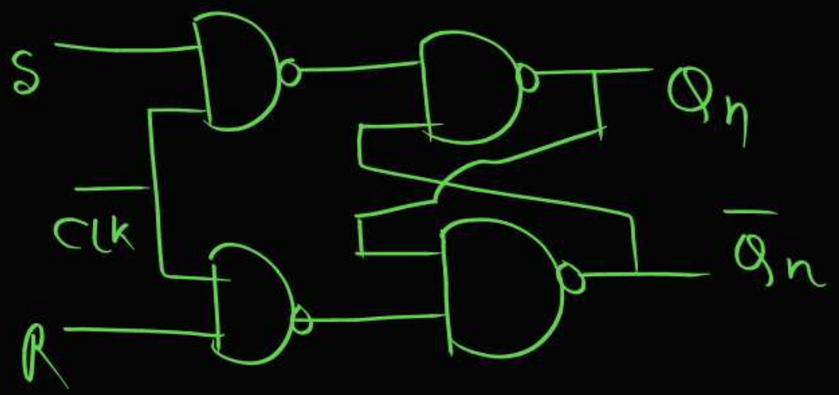
SR latch:



S	R	Q
0	0	Q
0	1	0
1	0	1
1	1	X

COMBINATIONAL CIRCUIT

SR FLIP FLOP



Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$$Q_{n+1} = S + \bar{R}Q_n$$

COMBINATIONAL CIRCUIT

JK FLIP FLOP

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

COMBINATIONAL CIRCUIT

D FLIP FLOP

D	Q_{n+1}
0	0
1	1

$Q_{n+1} = D$

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

COMBINATIONAL CIRCUIT

T FLIP FLOP

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

$$Q_{n+1} = T \oplus Q_n$$

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

SEQUENTIAL CIRCUIT

DESIGNING OF FLIP FLOP

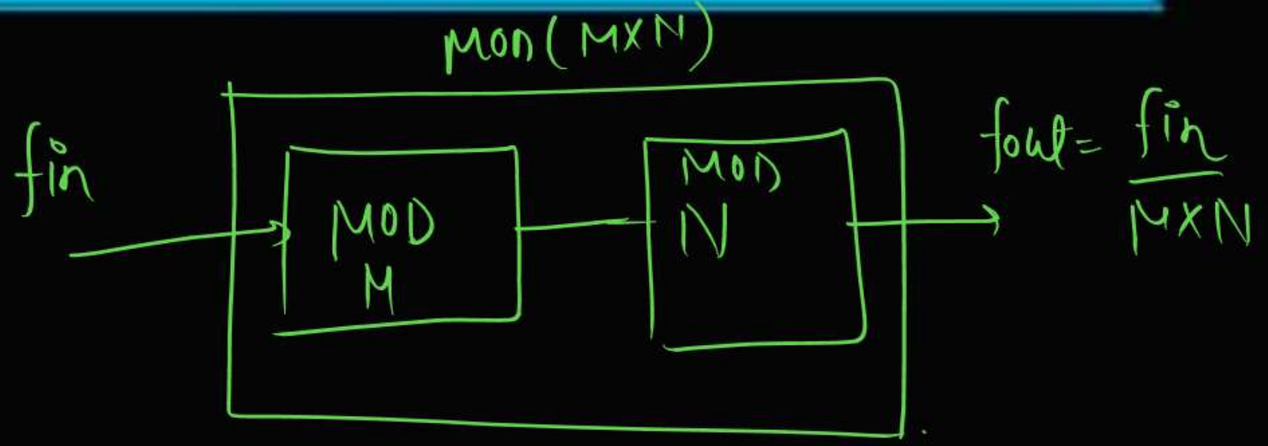
- Write the characteristic Table of Desired Flip Flop
- Write the excitation of Available Flip Flop
- Write the Logical Expression
- Minimization
- Hardware Implementation

4 X 3 = 12

COUNTERS

SYNCHRNOUS COUNTER

ASYNCHRNOUS COUNTER



COUNTERS

ASYNCHRNOUS COUNTER

$T_{clk} \geq n \cdot \tau_{pdff}$

$(f_{clk}) \leq \frac{1}{n \cdot \tau_{pdff}}$

+ve → Down

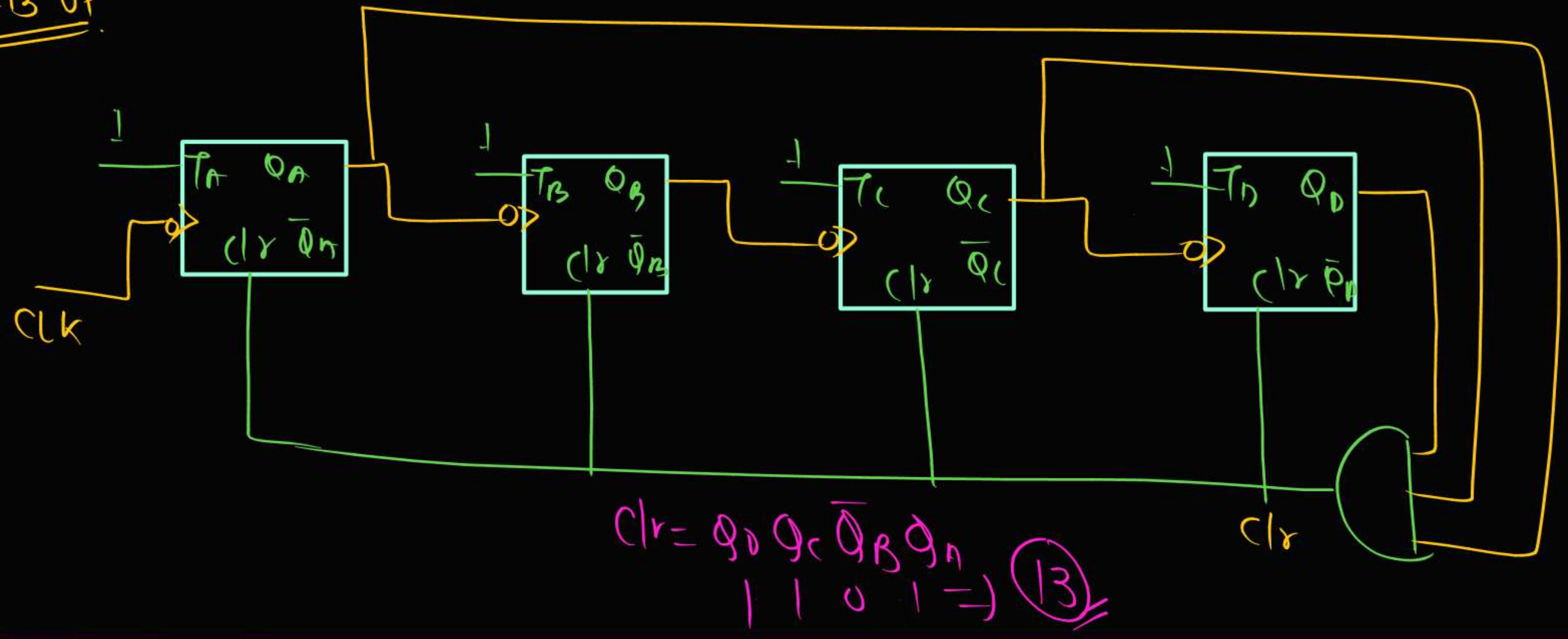
−ve → UP

COUNTERS

ER.CJHA@GMAIL.COM.
GATE/ESE by CJ sir.

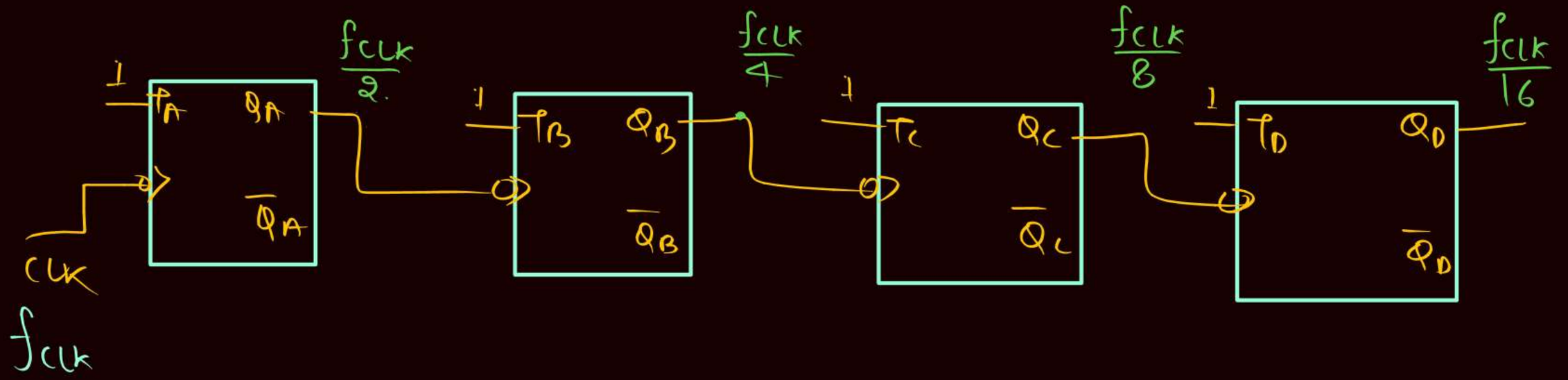
ASYNCHRNOUS COUNTER

MOD-13 UP.



$clr = Q_D Q_C \bar{Q}_B Q_A$

1 1 0 1 ⇒ (13)


1
T_A
Q_A
$\overline{Q}_A$
CLK
f_{CLK}
$\frac{f_{CLK}}{2}$
1
T_B
Q_B
$\overline{Q}_B$
$\frac{f_{CLK}}{4}$
1
T_C
Q_C
$\overline{Q}_C$
$\frac{f_{CLK}}{8}$
1
T_D
Q_D
$\overline{Q}_D$
$\frac{f_{CLK}}{16}$

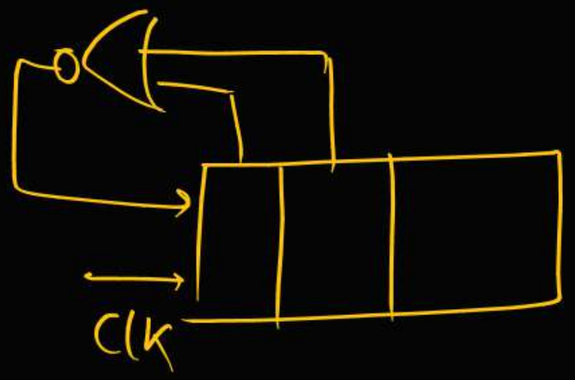
COUNTERS

SYNCHRNOUS COUNTER

Ring counter

n bit

→ MOD n.

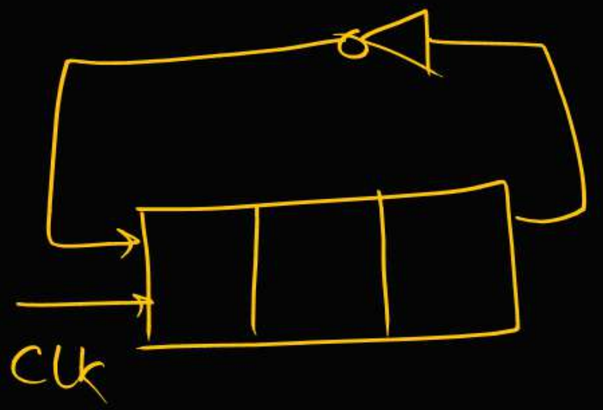


Johnson counter

'n' bit

→ MOD = 2n

Lockout problem



COUNTERS

SYNCHRNOUS COUNTER

Designing

Step 1 Write the present and next state.

step 2. Write the exictiation table.

step 3. Logical expression.

step 4. Minimization.

step 5. Hardware Implementation.

Series

$$f_{clk} \leq \frac{1}{\tau_{pd_{ff}} + (n-2)\tau_{pd_{AND}}}$$

Parallel

$$f_{clk} \leq \frac{1}{\tau_{pd_{ff}} + \tau_{pd_{AND}}}$$

NUMBER SYSTEM

BASE CONVERSION

Any Base to Decimal Conversion

$$(a_2 a_1 a_0 \cdot a_{-1} a_{-2})_r = (\quad)_{10}$$

$$\left[a_2 \times r^2 + a_1 \times r^1 + a_0 \times r^0 + a_{-1} \times r^{-1} + a_{-2} \times r^{-2}\right]_{10} = \text{Ans}$$

NUMBER SYSTEM

BASE CONVERSION

Decimal to Any Other Base Conversion

$(a_2 a_1 a_0 \cdot a_{-1} a_{-2})_{10} = (\quad)_r$

r	$a_2 a_1 a_0$	R
		x_0
		x_1
		x_2

$0 \cdot a_{-1} a_{-2} \times r =$

b_0

b_1

b_2

$(x_2 x_1 x_0 \cdot b_0 b_1 b_2)_r$

NUMBER SYSTEM

MAGNITUDE REPRESENTATION

- ✓ 1's ⟶ Range $-[2^{n-1}-1]$ to $+[2^{n-1}-1]$
- ✓ 2's ⟶ Range ⟶ $-[2^{n-1}]$ to $[2^{n-1}-1]$

Q 11100100

2's complement

→ Decimal ?

Look ahead carry

↳ Carry block

- no. of AND $= \frac{n(n+1)}{2}$
- no. of OR $\Rightarrow n$

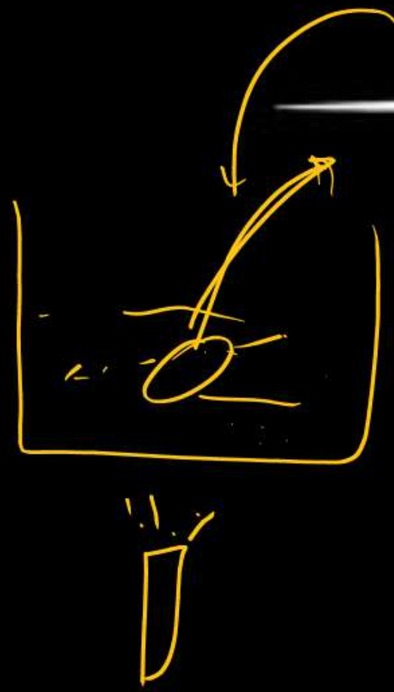
Propagation Delay

Only in carry Block

$2 T_{pd}$

Complete.

$4 T_{pd}$



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thank you