digital

1. Find the minimum product of sums of the following expression

   f=ABC+ABC

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1990

2. Find the minimum sum of products form of the logic function f(A,B,C,D)=Σm(0,2,8,10,15)+Σd(3,11,12,14) where m and d represent minterm and don't care term respectively.

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1991

3. Identify the logic function performed by the circuit shown in figure.

   (A)exclusive OR
   (B)exclusive NOR
   (C)NAND
   (D)NOR
   (E)None of the above

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1993

4. The logic expression for the output of the circuit shown in figure below is:

   (A) (AC)'+(BC)'+CD
   (B) A'C+B'C+CD
   (C) ABC+C'D'

(D) A'B'+B'C'+CD

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1994

5. What is the equivalent Boolean expression in product-of-sums form for the Karnaugh map given in Fig

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1996

6. Let $f(x, y, z) = x' + y'x + xz$ be a switching function. Which one of the following is valid?
   (A) y'z is a prime implicant of f
   (B) xz is a minterm of f
   (C) xz is an implicant of f
   (D) y is a prime implicant of f

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1997

7. Let * be defined as $x * y = x' + y$. Let $z = x * y$. Value of $z * x$ is
   (A) x'+y
   (B) x
   (C) 0
   (D) 1

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1997

8. dont worry skip it (nothing is missing here its just a numbering error)

9. Consider a logic circuit shown in figure below. The functions *f1*,*f2* and *f* (in canonical sum of products form in decimal notation) are :

   f1(w,x,y,z) = ∑(8,9,10)
   f2(w,x,y,z) = ∑ 7,8,12,13,14,15)
   f(w,x,y,z) = ∑ 8,9)
   The Function *f3* is
   a. ∑9,10
   b. ∑9
   c. ∑1,8,9
   d. ∑8,10,15

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1997

10. Which of the following operation is commutative but not associative
   (A) AND
   (B) OR
   (C) NAND
   (D) EXOR
   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1998

11. What happens when a bit-string is XORed with itself n-times as shown:

   [B⊕ (B⊕ (B⊕ (B…….. n times)]

   (A) complements when n is even
   (B) complements when n is odd
   (C) divides by 2^n always
   (D) remains unchanged when n is even
   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1998

12. The function represented by the Karnaugh map given below is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1998

13. Which of the following expressions is not equivalent to

(A) x NAND x

(B) x NOR x

(C) x NAND 1

(D) x NOR 1

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1999

14. Which of the following functions implements the Karnaugh map shown below?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1999

15. The simultaneous equations on the Boolean variables x, y, z and w,

have the following solution for x, y, z and w, respectively.

(A) 0 1 0 0
(B) 1 1 0 1
(C) 1 0 1 1
(D) 1 0 0 0

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2000

16. Which functions does NOT implement the Karnaugh map given below?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2000

17. Given the following Karnaugh map, which one of the following represents the minimal Sum-Of-Products of the map?

(A) xy + y'z
(B) wx'y' + xy + xz
(C) w'x + y'z + xy
(D) xz + y

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2001

18. Minimum sum of product expression for f(w, x, y, z) shown in Karnaugh-map below is

(A) xz + y'z
(B) xz' + zx'
(C) x'y + zx'
(D) None of these

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2002

19. Consider the following logic circuit whose inputs are functions f_1, f_2, f_3 and output is f

Given that

- $f_1(x,y,z)=\Sigma(0,1,3,5)$
- $f_2(x,y,z)=\Sigma(6,7)$, and
- $f(x,y,z)=\Sigma(1,4,5)$.

f_3 is?

1. $\Sigma(1,4,5)$
2. $\Sigma(6,7)$
3. $\Sigma(0,1,3,5)$
4. None of the above

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2002

20. Let f(A, B) = A' + B. Simplified expression for function f(f(x + y, y)z) is :
    (A) x' + z
    (B) xyz
    (C) xy' + z
    (D) None of these

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2002

21. **PART1** Express the function $f(x,y,z)=xy'+yz'$ with only one complement operation and one or more AND/OR operations. Draw the logic circuit implementing the expression obtained, using a single NOT gate and one or more AND/OR gates.

    Pending video

    PART2 Transform the following logic circuit (without expressing its switching function) into an equivalent logic circuit that employs only 6 NAND gates each with 2-inputs.
    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2002

22. The literal count of a boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of (xy + xz') is 4. What are the minimum possible literal counts of the product-of-sum and sum-of-product representations respectively of the function given by the following Karnaugh map ? Here, X denotes "don't
    care"

(A) (11, 9)
(B) (9, 13)
(C) (9, 10)
(D) (11, 11)

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2003

23. Consider the following circuit composed of XOR gates and non-inverting buffers.

The non-inverting buffers have delays δ_1=2ns and δ_2=4ns as shown in the figure. Both XOR gates and all wires have zero delays. Assume that all gate inputs, outputs, and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?

1. 1
2. 2
3. 3
4. 4

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2003

24. The Boolean function x'y' + xy + x'y is equivalent to

(A) x' + y'

(B) x + y

(C) x + y'

(D) x' + y

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

25. What is the minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate?
    1. 2
    2. 4
    3. 5
    4. 6

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

26. The function *AB'C + A'BC + ABC' + A'B'C + AB'C'* is equivalent to

(A) AC'+AB+A'C

(B) AB'+AC'+A'C

(C) A'B+AC'+AB'

(D) A'B+AC+AB'

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

27. Which are the essential prime implicants of the following Boolean function?

f(a, b, c) = a'c + ac' + b'c

(A) a'c and ac'

(B) a'c and b'c

(C) a'c only

(D) ac' and bc'

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

28. Which of the following expressions is equivalent to $(A \oplus B) \oplus C$

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

29. A two-way switch has three terminals a, b and c. In ON position (logic value 1), a is connected to b, and in OFF position, a is connected to c. Two of these two-way switches S1 and S2 are connected to a bulb as shown below.

Which of the following expressions, if true, will always result in the

lighting of the bulb ?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

30. Consider the following circuit.

Which one of the following is TRUE?
(A) f is independent of X
(B) f is independent of Y
(C) f is independent of Z
(D) None of X, Y, Z is redundant

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

31. The switching expression corresponding to f(A, B, C, D) = Σ (1, 4, 5, 9, 11,12) is

(A) BC'D' + A'C'D + AB'D

(B) ABC' + ACD + B'C'D

(C) ACD' + A'BC' + AC'D'

(D) A'BD + ACD' + BCD'

Pending (actually video lost)

32. Consider a Boolean function f (w, x, y, z). suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors i1 = (w1, x1, y1, z1) and i2 = (w2, x2, y2, z2) we

would like the function to remain true as the input changes from i1 to i2 (i1 and i2 differ in exactly one bit position), without becoming false momentarily. Let f (w, x, y, z) = ∑(5,7,11,12,13,15). Which of the following cube

covers of f will ensure that the required property is satisfied?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

33. Consider numbers represented in 4-bit gray code. Let h3h2h1h0 be the gray code representation of a number n and let g3g2g1g0 be the gray code of (n + 1) (modulo 16) value of the number. Which one of the following functions is correct?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

34. The boolean function for a combinational circuit with four inputs is represented by the following Karnaugh map.

Which of the product terms given below is an essential prime implicant of the function?

(A) QRS

(B) PQS

(C) PQ'S'

(D) Q'S'

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

35. What is the maximum number of different Boolean functions involving n Boolean variables?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

36. Consider the following Boolean function of four variables:

$f(w,x,y,z) = \sum(1,3,4,6,9,11,12,14)$

The function is:

(A) independent of one variables.
(B) independent of two variables.
(C) independent of three variables.
(D) dependent on all the variables.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

37. The following expression was to be realized using 2-input AND and OR gates. However, during the fabrication all 2-input AND gates were mistakenly substituted by 2-input NAND gates.
(a.b).c + (a'.c).d + (b.c).d + a. d
What is the function finally realized ?

(A) 1
(B) a’ + b’ + c’ + d’
(C) a’ + b + c’ + d’
(D) a’ + b’ + c + d’

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

38. Consider the following expression

ad’ + (ac)’ + bc’d
Which of the following Karnaugh Maps correctly represents the expression?

1. B.

C. D.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

39. Consider the following expression

Which of the following expressions does not correspond to the Karnaugh Map obtained for the given expression?

ANSWER- this is b part of 1.38 so refer the video solution of previous question. I have coverd both questions in same video

GATE-2007

40. Let f(w, x, y, z) = ∑(0, 4, 5, 7, 8, 9, 13, 15). Which of the following expressions are NOT equivalent to f?
(A) x’y’z’ + w’xy’ + wy’z + xz

(B) w'y'z' + wx'y' + xz
(C) w'y'z' + wx'y' + xyz + xy'z
(D) x'y'z' + wx'y' + w'y

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

41. Define the connective * for the Boolean variables X and Y as: X * Y = XY + X' Y'. Let Z = X * Y.

```
Consider the following expressions P, Q and R.
P: X = Y*Z
Q: Y = X*Z
R: X*Y*Z=1
```

Which of the following is TRUE?
(A) Only P and Q are valid
(B) Only Q and R are valid.
(C) Only P and R are valid.
(D) All P, Q, R are valid.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

42. The line T in the following figure is permanently connected to the ground.

Which of the following inputs (X1 X2 X3 X4) will detect the fault ?
(A) 0000
(B) 0111
(C) 1111
(D) None of these

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

43. cIn the Karnaugh map shown below, X denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2008

44. Given f1, f3 and f in canonical sum of products form (in decimal) for the circuit

f1=Σm(4,5,6,7,8)
f3=Σm(1,6,15)
f=Σm(1,6,8,15)
then f2 is:-
(A)Σm(4,6)
(B)Σm(4,8)
(C)Σm(6,8)
(D)Σm(4,6,8)

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2008

45. A set of Boolean connectives is functionally complete if all Boolean functions can be synthesized using those. Which of the following sets of connectives is NOT functionally complete?
(A) EX-NOR
(B) implication, negation
(C) OR, negation
(D) NAND

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2008

46.

Hindi [CLICK HERE]

English [CLICK HERE]

GATE-2008

47. Consider the following Boolean function of four variables
f(A, B, C, D) = Σ(2, 3, 6, 7, 8, 9, 10, 11, 12, 13)
The function is
(A) independent of one variable
(B) independent of two variables
(C) independent of three variable
(D) dependent on all the variables

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2008

48. What is the minimum number of gates required to implement the Boolean function (AB+C)if we have to use only 2-input NOR gates?
(A) 2
(B) 3
(C) 4
(D) 5

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2009

49. The minterm expansion of f(P, Q, R) = PQ + QR' + PR' is
(A) m2 + m4 + m6 + m7
(B) m0 + m1 + m3 + m5
(C) m0 + m1 + m6 + m7
(D) m2 + m3 + m4 + m5

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2010

50. The simplified SOP (Sum Of Product) form of the boolean expression (P + Q' + R') . (P + Q' + R) . (P + Q + R') is
(A) (P'.Q + R')
(B) (P + Q'.R')
(C) (P'.Q + R)
(D) (P.Q + R)

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2011

51. What is the boolean expression for the output f of the combinational logic circuit of NOR gates given below?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2010

52. Which one of the following circuits is NOT equivalent to a 2-input XNOR (exclusive NOR) gate?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2011

53. What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2012

54. The truth table

represents the Boolean function

(A) X

(B) X+Y

(C) X xor Y

(D) Y

Hindi [CLICK HERE]

English [CLICK HERE]

GATE-2012

55. Which one of the following expressions does NOT represent exclusive NOR of x and y?

(A) xy+x'y'

(B) x⊕y'

(C) x'⊕y

(D) x'⊕y'

Hindi [CLICK HERE]

English [CLICK HERE]

GATE-2013

56. Consider the following Boolean expression for F:

```
F(P, Q, R, S) = PQ + P'QR + P'QR'S
```

The minimal sum-of-products form of F is

(A) PQ + QR + QS

(B) P + Q + R + S

(C) P' + Q' + R' + S'

(D) P'R + P'R'S + P

Hindi [CLICK HERE]

English [CLICK HERE]

GATE-2014

57. The dual of a Boolean function f(x1, x2, … , xn, +, · , ′), written as F_D, is the same expression as that of F with + and . swapped. F is said to be self-dual if F = F_D. The number of self-dual functions with n Boolean variables is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

58. Consider the following minterm expression for F :
F(P,Q,R,S) = ∑ (0, 2, 5, 7, 8, 10, 13, 15)
The minterms 2, 7, 8 and 13 are ‘do not care’ terms. The minimal sum-of-products form for F is :

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

59. Let ⊕ denote the Exclusive OR (XOR) operation. Let ‘1’ and ‘0’ denote the binary constants. Consider the following Boolean expression for F over two variables P and Q:
F(P, Q) =((1 ⊕ P) ⊕ (P ⊕ Q)) ⊕ ((P ⊕ Q) ⊕ (Q ⊕ 0))
The equivalent expression for F is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

60. Consider the operations
f(X, Y, Z) = X’YZ + XY’ + Y’Z’ and g(X, Y, Z) = X′YZ + X′YZ′ + XY
Which one of the following is correct?

(A) Both {f} and {g} are functionally complete
(B) Only {f} is functionally complete
(C) Only {g} is functionally complete

(D) Neither {f} nor {g} is functionally complete

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2015

61. The number of min-terms after minimizing the following Boolean expression is _____.

```
[D' + AB' + A'C + AC'D + A'C'D]'
```

(A) 1
(B) 2
(C) 3
(D) 4

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2015

62. The total number of prime implicants of the function f(w, x, y, z) = Σ(0, 2, 4, 5, 6, 10) is _____.

(A) 2
(B) 3
(C) 4
(D) 5

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2015

63. Given the function F = P′ + QR, where F is a function in three Boolean variables P, Q and R and P′ = !P, consider the following statements.

```
S1: F = Σ (4, 5, 6)
S2: F = Σ (0, 1, 2, 3, 7)
S3: F = Π (4, 5, 6)
S4: F = Π (0, 1, 2, 3, 7)
```

Which of the following is true?

(A) S1-False, S2-True, S3-True, S4-False

(B) S1-True, S2-False, S3-False, S4-True
(C) S1-False, S2-False, S3-True, S4-True
(D) S1-True, S2-True, S3-False, S4-False

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2015

64. Consider the Boolean operator # with the following properties

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2016

65. Let, $x1 \oplus x2 \oplus x3 \oplus x4 = 0$ where x1, x2, x3, x4 are Boolean variables, and $\oplus$ is the XOR operator. Which one of the following must always be TRUE ?
(A) x1x2x3x4 = 0
(B) x1x3+x2 = 0
(C) $x'1 \oplus x'3 = x'2 \oplus x'4$
(D) x1+x2+x3+x4 = 0

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2016

66. Consider the Karnaugh map given below, where X represents " don't care" and blank represents 0.

Assume for all inputs (a, c, d) the respective complements (a', b', c', d')are also available. The above logic is implemented 2-input NOR gates only.
The minimum number of gates required is _____.

Hindi [CLICK HERE]

English [CLICK HERE]

GATE-2017

67. Given $f(w, x, y, z) = \Sigma_m(0,1,2,3,7,8,10) + \Sigma_d(5,6,11,15)$, where d represents the don't-care condition in Karnaugh maps. Which of the following is a minimum product-of-sums(POS) form of f(w,x,y,z)?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2017

68. If w, x, y, z are boolean variables, then which of the following is INCORRECT?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2017

69. Let $\oplus$ and $\odot$ denote the Exclusive OR and Exclusive NOR operations, respectively. Which one of the following is NOT CORRECT?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2018

70. Consider the minterm list form of a Boolean function F given below.
$F(P, Q, R, S) = \Sigma m(0, 2, 5, 7, 9, 11) + d(3, 8, 10, 12, 14)$
Here, m denotes a minterm and d denotes a don't care term. The number of essential prime implicants of the function F is _____ .

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2018

71. Which one of the following is NOT a valid identity?

(A) $(x \oplus y) \oplus z = x \oplus (y \oplus z)$

(B) $(x + y) \oplus z = x \oplus (y + z)$

(C) $x \oplus y = x + y$, if $xy = 0$

(D) $x \oplus y = (xy + x'y')'$

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2019

72. What is the minimum number of 2-input NOR gates required to implement 4-variable function expressed in sum-of-minterms from as f = Σ(0, 2, 5, 7, 8, 10, 13, 15)? Assume that all the inputs and their complements are available_____ .

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2019

73. Consider three 4-variable functions f_1, f_2 and f_3, which are expressed in sum-of-minterms

$f_1 = \Sigma(0, 2, 5, 8, 14)$

$f_2 = \Sigma(2, 3, 6, 8, 14, 15)$

$f_3 = \Sigma(2, 7, 11, 14)$

For the following circuit with one AND gate and one XOR gate, the output function f can be expressed as:

(A) Σ(7, 8, 11)

(B) Σ(2, 14)

(C) Σ(0, 2, 3, 5, 6, 7, 8, 11, 14)

(D) Σ(2, 7, 8, 11, 14)

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2019

74. Consider the Boolean function z(a,b,c).

Which one of the following minterm lists represents the circuit given above?

(A) z = ∑(0, 1, 3, 7)
(B) z = ∑(1, 4, 5, 6, 7)
(C) z = ∑(2, 4, 5, 6, 7)
(D) z = ∑(2, 3, 5)

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2020

1. pending
2. Show with the help of a block diagram how the Boolean function

   f=AB+BC+CA

   can be realized using only a 4:1 multiplexer

   Hindi [CLICK HERE]
   English [CLICK HERE]

GATE-1990

3. Consider the circuit given below which has a four bit binary

number $b_3b_2b_1b_0$ as input and a five bit binary number $d_4d_3d_2d_1d_0$ as output. The circuit implements:

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1996

4. Consider the circuit in below figure. *f* implements

   (A) (ABC)' + A'BC' + ABC
   (B) A + B + C
   (C) A $\oplus$ B $\oplus$ C
   (D) AB + BC + CA

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1996

5. A logic network has two data inputs A and B, and two control inputs C0and C1. It implements the function F according to the following table.

   Implement the circuit using one 4 to 1Multiplexer, one 2−input Exclusive OR gate, one 2−input AND gate, one 2−input OR gate and one Inverter.

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1996

6. A multiplexor with a 4-bit data select input is a
   (A) 4:1 multiplexor
   (B) 2:1 multiplexor
   (C) 16:1 multiplexor
   (D) 8:1 multiplexor

   GATE-1998

7. The number of full and half-adder's required to add 16-bit number is:
   (A) 8 half-adder's, 8 full-adder's
   (B) 1 half-adder, 15 full-adder's
   (C) 16 half-adder's, 0 full-adder
   (D) 4 half-adder's, 12 full-adder's

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1999

8. Which of the following sets of component(s) is/are sufficient to implement any arbitrary boolean function?
   a) XOR gates, NOT gates
   b) 2 to 1 multiplexers
   c) AND gates, XOR gates
   d) Three-input gates that output (A.B)+C for the inputs A, B and C.
   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1999

9. Consider the circuit shown below. The output of a 2:1 Mux is given by the function (ac' + bc).

   Which of the following is true?
   (A) f = x1'+ x1x
   (B) f = x1'x2 + x1x2′
   (C) f = x1x2 + x1'x2′
   (D) f = x1 + x2′
   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-2001

10. Consider the following multiplexor where I0, I1, I2, I3 are four data input lines selected by two address line combinations A1A0 = 00, 01, 10, 11 respectively and f is "the output of the multiplexor. EN is the enable

input.

The function f(x, y, z) implemented by the above circuit is :
(A) xyz'
(B) xy + z
(C) x + z
(D) None of these
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2002

11. Consider the ALU shown below.

If the operands are in 2's complement representation, which of the following operations can be performed by suitably setting the control lines K and C0 only (+ and – denote addition and subtraction respectively) ?
(A) A + B, and A – B, but not A + 1
(B) A + B, and A + 1, but not A – B
(C) A + B, but not A – B, or A + 1
(D) A + B, and A – B, and A + 1
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2003

12. A 4-bit carry lookahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.
(A) 4 time units
(B) 6 time units
(C) 10 time units
(D) 12 time units

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

13. A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, …, 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit ≥ 5, and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?
(A) 2
(B) 3
(C) 4
(D) 5

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

14. Consider a multiplexer with X and Y as data inputs and Z as control input. Z = 0 selects input X, and Z = 1 selects input Y. What are the connections required to realize the 2-variable Boolean function f = T + R, without using any additional hardware ?
(A) R to X, 1 to Y, T to Z
(B) T to X, R to Y, T to Z
(C) T to X, R to Y, 0 to Z
(D) R to X, 0 to Y, T to Z
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

15. The circuit shown below implements a 2-input NOR gate using two 2-4 MUX (control signal 1 selects the upper input). What are the values of signals x, y and z?

(A) 1, 0, B
(B) 1, 0, A

(C) 0, 1, B
(D) 0, 1, A

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

16. The majority function is a Boolean function f(x, y, z) that takes the value 1 whenever a majority of the variables x, y, z and 1. In the circuit diagram for the majority function shown below, the logic gates for the boxes labeled P and Q are, respectively,
(A) XOR, AND
(B) XOR, XOR
(C) OR, OR
(D) OR, AND

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

17. Consider the circuit below. Which one of the following options correctly represents f (x, y, z)?

(A) xz' + xy + y'z
(B) xz' + xy + (yz)'
(C) xz + xy + (yz)'
(D) xz + xy' + y'z

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

18. Given two three bit numbers a2a1a0 and b2b1b0 and c, the carry in, the function that represents the carry generate function when these two

numbers are added is:

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

19. We consider the addition of two 2's complement numbers $b_{n-1}b_{n-2}\ldots b_0$ and $a_{n-1}a_{n-2}\ldots a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2}\ldots c_0$ and the carry-out by c_{out}. Which one of the following options correctly identifies the overflow condition?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

20. In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:
$P_i = A_i \oplus B_i$ and $G_i = A_i.B_i$

The expressions for the sum bit S_i and the carry bit C_{i+1} of the look-ahead carry adder are given by:
$S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_i.C_i$, where C_0 is the input carry.

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S3, S2, S1, S0 and C4 as its outputs are respectively:
(A) 6, 3
(B) 10, 4
(C) 6, 4
(D) 10, 5
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

21. The following circuit implements a two-input AND gate using two 2-1 multiplexers. What are the values of X_1, X_2, X_3 ?

(A) X_1=b, X_2=0, X_3=a

(B) X_1=b, X_2=1, X_3=b

(C) X_1=a, X_2=b, X_3=1

(D) X_1=a, X_2=0, X_3=b

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

22. How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

(A) 7
(B) 8
(C) 9
(D) 10

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

23. Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

(A) 2^n line to 1 line
(B) 2^{n+1} line to 1 line
(C) 2^{n-1} line to 1 line
(D) 2^{n-2} line to 1 line

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

24. What Boolean function does the circuit below realize ?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2008

25. The Boolean expression for the output ‘f’ of the multiplexer shown below is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2010

26. In the following truth table, V = 1 if and only if the input is valid.

What function does the truth table represent?
(A) Priority encoder
(B) Decoder
(C) Multiplexer
(D) Demultiplexer
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2013

27. Consider a 4-to-1 multiplexer with two select lines S1 and S0, given below

The minimal sum-of-products form of the Boolean expression for the output F of the multiplexer is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

28. Consider the following combinational function block involving four Boolean variables x,y,a,b where x,a,b are inputs and y is the output.

```
f(x, a, b, y)
{
  if(x is 1) y = a;
  else y = b;
}
```

Which one of the following digital logic blocks is the most suitable for implementing this function?

(A)Full adder

(B)Priority encoder

(C)Multiplexor

(D)Flip-flop

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

29. A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. The total propagation time of this 4-bit binary adder in microseconds is_____.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2015

30. Consider the two cascaded 2-to-1 multiplexers as shown in the figure.

The minimal sum of products form of the output X is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2016

31. Consider a carry lookahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is
(A) $\Theta(1)$
(B) $\Theta(\text{Log } (n))$
(C) $\Theta(\sqrt{n})$
(D) $\Theta(n)$

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2016

32. Consider an eight-bit ripple-carry adder for computing the sum of A and B, where A and B are integers represented in 2's complement form. If the decimal value of A is one, the decimal value of B that leads to the longest latency for the sum to stabilize is _____

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2016

33. When two 8-bit numbers $A_7 \ldots A_0$ and $B_7 \ldots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using ripple-carry adder. the sum bits obtained are $S_7 \ldots S_0$ and the carry bits are $C_7 \ldots C_0$. An overflow is said to have occurred if

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2017

1. pending vid

2. For the synchronous counter shown in Fig, write the truth table of Q0,Q1, and Q2 after each pulse, starting from Q0=Q1=Q2=0 and determine the counting sequence and also the modulus of the counter.given initial state Q2 Q1 Q0=000

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1990

3. Find the maximum clock frequency at which the counter in the figure below can be operated. Assume that the propagation delay through each flip flop and each AND gate is 10ns. Also, assume that the setup time for the JK inputs of the flip flops is negligible.

   Hindi [CLICK HERE]
   English [CLICK HERE]

GATE-1991

4. For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in figure is:

   (A)Shift Register
   (B)Mod- 3 Counter
   (C)Mod- 6 Counter
   (D)Mod- 2 Counter
   (E)None of the above

   Hindi [CLICK HERE]
   English [CLICK HERE]

GATE-1993

5. The number of flip flop required to construct a binary modulo N counter v is _____.
   pending vid

6. Consider the synchronous sequential circuit in the below figure

   PART a
   Draw a state diagram, which is implemented by the circuit. Use the following names for the states corresponding to the values of flip-flops as given below.

   .....
   ....

PART b

Given that the initial state of the circuit is S4, identify the set of states, which are not reachable. Given that the initial state of the circuit is S4, identify the set of states, which are not reachable.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1996

7. The following arrangement of master-slave flip flops has the initial state of P, Q as 0, 1 (respectively). After three clock cycles the output state P, Q is (respectively),

(A) 1, 0
(B) 1, 1
(C) 0, 0
(D) 0,1

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2000

8. Consider the following circuit with initial state Q0 = Q1 = 0. The D Flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.

   Consider the following timing diagrams of X and C; the clock period of C <= 40 nanosecond. Which one is the correct plot of Y?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2001

9. Consider the circuit given below with initial state Q0 =1, Q1 = Q2 = 0. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$

   Which one of the following is the correct state sequence of the circuit?
   (A) 1,3,4,6,7,5,2
   (B) 1,2,5,3,7,6,4
   (C) 1,2,7,3,5,6,4
   (D) 1,6,5,7,2,3,4

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-2001

10. The Finite state machine described by the following state diagram with A as starting state, where an arc label is x / y and x stands for 1-bit input and y stands for 2- bit output

    (A) Outputs the sum of the present and the previous bits of the input.
    (B) Outputs 01 whenever the input sequence contains 11.
    (C) Outputs 00 whenever the input sequence contains 10.
    (D) None of these
    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2002

11. A 1-input, 2-output synchronous sequential circuit behaves as follows :
    Let zk, nk denote the number of 0's and 1's respectively in initial k bits of the input (zk + nk = k). The circuit outputs 00 until one of the following conditions holds.

    zk - nk = 2. In this case, the output at the k-th and all subsequent clock ticks is 10.
    nk - zk = 2. In this case, the output at the k-th and all subsequent clock ticks is 01.

    What is the minimum number of states required in the state transition graph of the above circuit?
    (A) 5
    (B) 6

(C) 7
(D) 8

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2003

12. In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in
(A) Q = 0, Q' = 1
(B) Q = 1, Q' = 0
(C) Q = 1, Q' = 1
(D) Indeterminate states

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

13. Consider the partial implementation of a 2-bitt counter using T flip-flops following the sequence 0-2-3-1-0, as shown below

To complete the circuit, the input X should be
(A) Q2′
(B) Q2 + Q1
(C) (Q1 $\oplus$ Q2)'
(D) Q1 $\oplus$ Q2

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

14. The following diagram represents a finite state machine which takes as input a binary number from the least significant bit.

Which one of the following is TRUE?
(A) It computes 1's complement of the input number

(B) It computes 2's complement of the input number
(C) It increments the input number
(D) It decrements the input number

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

15. How many pulses are needed to change the contents of a 8-bit up counter from 10101100 to 00100111 (rightmost bit is the LSB)?
(A) 134
(B) 133
(C) 124
(D) 123

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

16. Which of the following input sequences will always generate a 1 at the output z at the end of the third cycle?

(A)

A	B	C
0	0	0
1	0	1
1	1	1

(B)

A	B	C
1	0	1
1	1	0
1	1	1

(C)

A	B	C
0	1	1
1	0	1
1	1	1

(D)

A	B	C
0	0	1
1	1	0
1	1	1

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

17. Consider the following circuit involving a positive edge triggered D FF.

Consider the following timing diagram. Let Ai represent the logic level on the line A in the i-th clock period.

Let A' represent the complement of A. The correct output sequence on Y over the clock periods 1 through 5 is
(A) A0 A1 A1′ A3 A4
(B) A0 A1 A2′ A3 A4
(C) A1 A2 A2′ A3 A4
(D) A1 A2′ A3 A4 A5′
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

18. Consider the following circuit:

The flip-flops are positive edge triggered D FFs. Each state is designated as a two bit string Q0Q1. Let the initial state be 00. The state transition sequence is:

1.
2.

3.
4.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

19. Consider the circuit in the diagram. The $\oplus$ operator represents Ex-OR. The D flipflops are initialized to zeroes (cleared).

    The following data: 100110000 is supplied to the “data” terminal in nine clock cycles. After that the values of q2q1q0 are:
    (A) 000
    (B) 001
    (C) 010
    (D) 101
    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2006

20. You are given a free running clock with a duty cycle of 50% and a digital waveform f which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of f by 180°?

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2006

21. For a state machine with the following state diagram the expression for

the next state S+ in terms of the current state S and the input variables x and y is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

22. Which of the following input sequences for a cross-coupled R-S flip-flop realized with two NAND gates may lead to an oscillation ?
(A) 11, 00
(B) 01, 10
(C) 10, 01
(D) 00, 11

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

23. What is the final value stored in the linear feedback shift register if the input is 101101?

(A) 0110
(B) 1011
(C) 1101
(D) 1111

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

24. The control signal functions of a 4-bit binary counter are given below (where X is “don’t care”)

The counter is connected as follows:

Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence:

(A) 0, 3, 4
(B) 0, 3, 4, 5
(C) 0, 1, 2, 3, 4
(D) 0, 1, 2, 3, 4, 5

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

25. Consider the following state diagram and its realization by a JK flip flop

The combinational circuit generates J and K in terms of x, y and Q.The Boolean expressions for J and K are :

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2008

26. Given the following state table of an FSM with two states A and B,one input and one output.

PRESENT - STATE		Input	Next State		Output
A	B		A	B	
0	0	0	0	0	1
0	1	0	1	0	0
1	0	0	0	1	0

1	1	0	1	0	0
0	0	1	0	1	0
0	1	1	0	0	1
1	0	1	0	1	1
1	1	1	0	0	1

If the initial state is A=0,B=0 what is the minimum length of an input string which will take the machine to the state A=0,B=1 with output=1.

(A)3
(B)4
(C)5
(D)6

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2009

27. In the sequential circuit shown below,if the initial value of the output Q1Q0 is 00,what are the next four values of Q1Q0?

(A) 11, 10, 01, 00
(B) 10, 11, 01, 00
(C) 10, 00, 01, 11
(D) 11, 10, 00, 01

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2010

28. The minimum number of D flip-flops needed to design a mod-258 counter is.
(A) 9
(B) 8
(C) 512
(D) 258

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2011

29. Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.

    If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

    (A) 000
    (B) 001
    (C) 010
    (D) 011

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2011

30. {PART 2 and continuation of previous question}If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?

    (A) 3
    (B) 4
    (C) 5
    (D) 6

    Hindi [CLICK HERE] same video as question no 3.29
    English [CLICK HERE]

    GATE-2011

31. Let k = 2n. A circuit is built by giving the output of an n-bit binary counter as input to an n-to-2n bit decoder. This circuit is equivalent to a

    (A) k-bit binary up counter.
    (B) k-bit binary down counter.
    (C) k-bit ring counter.
    (D) k-bit Johnson counter.

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

32.

The above sequential circuit is built using JK flip-flops is initialized with Q2Q1Q0 = 000. The state sequence for this circuit for the next 3 clock cycle is

(A) 001, 010, 011
(B) 111, 110, 101
(C) 100, 110, 111
(D) 100, 011, 001

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

33. Consider a 4 bit Johnson counter with an initial value of 0000. The counting sequence of this counter is:

(A) 0, 1, 3, 7, 15, 14, 12, 8, 0
(B) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
(C) 0, 2, 4, 6, 8, 10, 12, 14, 0
(D) 0, 8, 12, 14, 15, 7, 3, 1, 0

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2015

34. A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flipflop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that J = K = 1 is the toggle mode and J = K = 0 is the

state-holding mode of the JK flip-flop. Both the flip-flops have non-zero propagation delays.

(A) 0110110…
(B) 0100100…
(C) 011101110…
(D) 011001100…

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2015

35. The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0,…) is _____

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2015

36. We want to design a synchronous counter that counts the sequence 0-1-0-2-0-3 and then repeats. The minimum number of J-K flip-flops required to implement this counter is_____.

ANSWER :- I have covered along with question 3.35 so refer video solution of previous question

GATE-2016

37. Consider a combination of T and D flip-flops connected as shown below. The output of the D flipflop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.

Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs
(A) Q_1 Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively

(B) Q_1 Q_0 after the 3rd cycle are 11 and after the 4th cycle are 01 respectively
(C) Q_1 Q_0 after the 3rd cycle are 00 and after the 4th cycle are 11 respectively
(D) Q_1 Q_0 after the 3rd cycle are 01 and after the 4th cycle are 01 respectively
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2017

38. The next state table of a 2 bit saturating up-counter is given below.

The counter is built as synchronous sequential circuit using T flip-flops.The value for T_1 and T_0 are
(A) $T_1 = Q_0Q_1$ $T_0 = Q'_0Q'_1$
(B) $T_1 = Q'_1Q_0$ $T_0 = Q'_1 + Q'_0$
(C) $T_1 = Q_1 + Q_0$ $T_0 = Q'_1 + Q'_0$
(D) $T_1 = Q'_1Q_0$ $T_0 = Q_1 + Q_0$

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2017

39. Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.

The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of “in” is _____ .
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2018

1. Consider the number given by the decimal expression:

   $$163*9+162*7+16*5+3$$

   The number of 1's in the unsigned binary representation of the number is _____

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1991

2. Topic removed from syllabus

3. When two 4-bit numbers A = a3 a2 a1 a0 and B=b3 b2 b1 b0 are multiplied, the bit c1 of the product C is given by _____

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1991

4. A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16.

   PART 1
   The range of the exponent is _____

   PART 2
   The range of the exponent is _____, if the scale factor is represented in excess-64 format.

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1990

5. Consider n-bit (including sign bit) 2's complement representation of integer number. The range of integer values, N, that can be represented is _____≤ N ≤ _____ .

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1994

6. The number of 1's in the binary representation of (3∗4096+15∗256+5∗16+3) are:

   (A)8
   (B)9
   (C)10
   (D)12

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1995

7. What is the minimum size of ROM required to store the complete truth table of an 8-bit x 8-bit multiplier?
   (A) 32 K x 16 bits
   (B) 64 K x 16 bits
   (C) 16 K x 32 bits
   (D) 64 K x 32 bits

   [video solution covers 2 questions from **cao subject** - q.no. 2.9-gate 2004 and question no and 2.23-Gate 2012 this one is exactly similar to 2.9]

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1996

8. Booth's algorithm for integer multiplication gives worst performance when the multiplier pattern is
   (A) 101010 ……1010
   (B) 100000 ……0001
   (C) 111111 ……1111
   (D) 011111 ……1110

   Hindi [CLICK HERE]
   English [CLICK HERE]

   GATE-1996

9. Consider the following floating point number representation

   The exponent is in 2's complement representation and mantissa is in the sign magnitude representation. The range of the magnitude of the normalized numbers in this representation is

a). 0 to 1
b). 0.5 to 1
c). 2^{-23} to 0.5
d). 0.5 to $(1-2^{-23})$

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1996

10. Given √(224)r=(13)r. The value of the radix r is:

(A)10
(B)8
(C)5
(D)6

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1997

11. Booth's coding in 8 bits for the decimal number −57 is:

(A)0−100+1000
(B)0−100+100−1
(C)0−1+100−10+1
(D)00−10+100−1

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1999

12. Zero has two representations in:

a) Sign magnitude
b) 1's complement
c) 2's complement
d) None of the above

(A) Only a
(B) a and b
(C) a and c
(D) a, b and c

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-1999

13. The number 43 in 2's complement representation is

(A) 01010101
(B) 11010101
(C) 00101011
(D) 10101011

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2000

14. Consider the values A = 2.0 x 10^30, B =-2.0 x 10^30, C= 1.0, and the sequence

```
X: = A + B
Y: = A + C
X: = X + C

Y: = Y + B
```

executed on a computer where floating-point numbers are represented with 32 bits. The values for X and Y will be
(A) X = 1.0, Y = 1.0
(B) X = 1.0, Y = 0.0
(C) X = 0.0, Y = 1.0
(D) X = 0.0, Y = 0.0
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2000

15. The 2's complement representation of $(-539)_{10}$ in hexadecimal is

(A) ABE
(B) DBC
(C) DE5
(D) 9E7

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2001

16. In 2' s complement addition, overflow

(A) is flagged whenever there is carry from sign bit addition
(B) cannot occur when a positive value is added to a negative value
(C) is flagged when the carries from sign bit and previous bit match
(D) none of the above

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2002

Videos got mixed (hin video on eng channel and …..)

17. The decimal value 0.25

(A) is equivalent to the binary value 0.1
(B) is equivalent to the binary value 0.01
(C) is equivalent to the binary value 0.00111….
(D) cannot be represented precisely in binary

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2002

18. The 2' s complement representation of the decimal value – 15 is

(A) 1111
(B) 11111
(C) 111111

(D) 10001

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2002

19. Sign extension is a step in

(A) floating point multiplication
(B) signed 16 bit integer addition
(C) arithmetic left shift
(D) converting a signed integer from one size to another

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2002

20. Assuming all numbers are in 2's complement representation, which of the following numbers is divisible by 11111011?

(A) 11100111
(B) 11100100
(C) 11010111
(D) 11011011

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2003

21. The following is a scheme for floating point number representation using 16 bits.

Let s,e, and m be the numbers represented in binary in the sign, exponent, and mantissa fields respectively. Then the floating point number represented is:

What is the maximum difference between two successive real numbers

representable in this system?

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2003

22. If 73x (in base-x number system) is equal to 54y (in base-y number system), the possible values of x and y are

(A) 8, 16
(B) 10, 12
(C) 9, 13
(D) 8, 11

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

23. What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

(113. + -111.) + 7.51
113. + (-111. + 7.51)

(A) 9.51 and 10.0 respectively
(B) 10.0 and 9.51 respectively
(C) 9.51 and 9.51 respectively
(D) 10.0 and 10.0 respectively

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

24. Let A = 1111 1010 and B = 0000 1010 be two 8-bit 2's complement numbers. Their product in 2's complement is

(A) 1100 0100
(B) 1001 1100
(C) 1010 0101
(D) 1101 0101

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

25. The number $(123456)_8$ is equivalent to

(A) $(A72E)_{16}$ and $(22130232)_4$
(B) $(A72E)_{16}$ and $(22131122)_4$
(C) $(A73E)_{16}$ and $(22130232)_4$
(D) $(A62E)_{16}$ and $(22120232)_4$

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2004

26. The range of integers that can be represented by an n bit 2's complement number system is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

27. The hexadecimal representation of 657_8 is
(A) 1AF
(B) D78
(C) D71
(D) 32F

Video lost

28. Using Booth's Algorithm for multiplication, the multiplier −57 will be recoded as:-

(A)0 -1 00 1 0 0 -1
(B)1 1 0 0 0 1 1 1
(C)0 -1 0 0 10 0 0
(D)0 1 0 0 -1 0 0 1

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

29. $(34.4)_8 \times (23.4)_8$ evaluates to

A) $(1053.6)_8$
B) $(1053.2)_8$
C) $(1024.2)_8$
D) None of these

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

30. Consider the following floating-point format.

Mantissa is a pure fraction in sign-magnitude form.The decimal number 0.239×2^{13} has the following hexadecimal representation (without normalization and rounding off):

(A) 0D 24

(B) 0D 4D

(C) 4D 0D

(D) 4D 3D

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2005

31. Consider the following floating point format

Mantissa is a pure fraction in sign-magnitude form. The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field. The normalized representation of the above number (0.239×2^{13}) is:

(A) 0A 20
(B) 11 34
(C) 4D D0
(D) 4A E8

ANSWER I have covered it along with question 4.31, so refer video solution of previous question

GATE-2005

32. The addition of 4-bit, two's complement, binary numbers 1101 and 0100 results in

(A) 0001 and an overflow
(B) 1001 and no overflow
(C) 0001 and no overflow
(D) 1001 and an overflow

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

33. When multiplicand Y is multiplied by multiplier X = xn – 1 xn-2 …. x0 using bit-pair recoding in Booth's algorithm, partial products are generated according to the following table.

The partial products for rows 5 and 8 are
(A) 2Y and Y
(B) -2Y and 2Y
(C) -2Y and 0
(D) 0 and Y

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2006

34. (C012.25)H – (10111001110.101)B =

(A) (135103.412)o
(B) (564411.412)o
(C) (564411.205)o

(D) (135103.205)o

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2007

35. The following bit pattern represents a floating point number in IEEE 754 single precision format

    1 10000011 10100000000000000000000

    The value of the number in decimal form is

    (A) -10
    (B) -13
    (C) -26
    (D) None of these

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2008

36. In the IEEE floating point representation, the hexadecimal value 0 × 00000000 corresponds to

    (A) the normalized value 2^-127
    (B) the normalized value 2^-126
    (C) the normalized value +0
    (D) the special value +0

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2008

37. Let r denote number system radix. The only value(s) of r that satisfy the equation

    is/are

    (A) decimal 10
    (B) decimal 11
    (C) decimal 10 and 11
    (D) any value > 2

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2008

38. The two numbers given below are multiplied using the Booth's algorithm.

    Multiplicand : 0101 1010 1110 1110
    Multiplier: 0111 0111 1011 1101

    How many additions/Subtractions are required for the multiplication of the above two numbers?

    (A) 6
    (B) 8
    (C) 10
    (D) 12

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2008

39. $(1217)_8$ is equivalent to

    (A) $(1217)_{16}$
    (B) $(028F)_{16}$
    (C) $(2297)_{10}$
    (D) $(0B17)_{16}$

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2009

40. P is a 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$.The 2's complement representation of 8*P

    (A) $(C3D8)_{16}$
    (B) $(187B)_{16}$
    (C) $(F878)_{16}$
    (D) $(987B)_{16}$

    Hindi [CLICK HERE]

English [CLICK HERE]

GATE-2010

41. The decimal value 0.5 in IEEE single precision floating point representation has

(A) fraction bits of 000…000 and exponent value of 0
(B) fraction bits of 000…000 and exponent value of −1
(C) fraction bits of 100…000 and exponent value of 0
(D) no exact representation
Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2012

42. The smallest integer that can be represented by an 8-bit number in 2's complement form is

(A) -256
(B) -128
(C) -127
(D) 0

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2013

43. The base (or radix) of the number system such that the following equation holds is_____.

```
312/20 = 13.1
```

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

44. Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions is _____ .

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2014

45. The value of a float type variable is represented using the single-precision 32-bit floating point format IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for mantissa. A float type variable X is assigned the decimal value of −14.25. The representation of X in hexadecimal notation is

    (A) C1640000H
    (B) 416C0000H
    (C) 41640000H
    (D) C16C0000H

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2014

46. consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions is _____.

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2015

47. The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is_____.

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2016

48. Let X be the number of distinct 16-bit integers in 2's complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation. Then X −Y is _____

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2016

49. The n-bit fixed-point representation of an unsigned real number X uses f bits for the fraction part. Let i = n − f. The range of decimal values for X in this representation is

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2017

50. Given the following binary number in 32 bit (single precision) IEEE-754 format:

    00111110011011010000000000000000

    The decimal value closest to this floating-point number is:

    (A) 1.45 X 10^1
    (B) 1.45 X 10^-1
    (C) 2.27 X 10^-1
    (D) 2.27 X 10^1

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2017

51. The representation of the value of a 16-bit unsigned integer X in a hexadecimal number system is BCA9. The representation of the value of X in octal number system is:

    (A) 571244
    (B) 736251
    (C) 571247
    (D) 136251

    Hindi [CLICK HERE]
    English [CLICK HERE]

    GATE-2017

52. Consider the unsigned 8-bit fixed point binary number representation, below,

    b7 b6 b5 b4 b3 . b2 b1 b0

    where the position of the binary point is between b3 and b2 . Assume b7 is the most significant bit. Some of the decimal numbers listed below cannot be represented exactly in the above representation:

(i) 31.500
(ii) 0.875
(iii) 12.100
(iv) 3.001

Which one of the following statements is true?

(A) None of (i), (ii), (iii), (iv) can be exactly represented
(B) Only (ii) cannot be exactly represented
(C) Only (iii) and (iv) cannot be exactly represented
(D) Only (i) and (ii) cannot be exactly represented

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2018

53. In 16-bit 2's complement representation, the decimal number −28 is:

(A) 1111 1111 0001 1100
(B) 0000 0000 1110 0100
(C) 1111 1111 1110 0100
(D) 1000 0000 1110 0100

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2019

54. Consider Z = X − Y where X, Y and Z are all in sign-magnitude form. X and Y are each represented in n bits. To avoid overflow, the representation of Z would require a minimum of:

(A) n bits
(B) n−1 bits
(C) n+1 bits
(D) n+2 bits

Hindi [CLICK HERE]
English [CLICK HERE]

GATE-2019

55. Consider three registers R1, R2, and R3 that store numbers in IEEE−754 single precision floating point format. Assume that R1 and R2 contain the values (in hexadecimal notation) 0x42200000 and 0xC1200000, respectively.

If R3 = R1 / R2, what is the value stored in R3 ?
(A) 0x40800000
(B) 0xC0800000
(C) 0x83400000
(D) 0xC8500000

Hindi [CLICK HERE]
English [CLICK HERE]