EC/EE/CS & IT/IN

Digital Electronics

Latches & SR Flip Flops

LECTURE NO. 7

Chandan Jha Sir (CJ Sir)

निगाहों में मंज़िल थी, गिरे और
गिरकर सम्भालते रहे
हवाओं ने बहुत कोशिश की,
मगर चिराग़ अंशियाँ में भी
जलते रहे

SUCCESS

LATCHES & SR FF

SEQUENTIAL CIRCUIT

Latches
Flip-Flop

Registers
Counter

1. A circuit with feedback and memory are called sequential circuit.

2. Output of the sequential circuit depends on previous output as well as present state of input.

{ Dynamic circuit }

LATCHES & SR FF

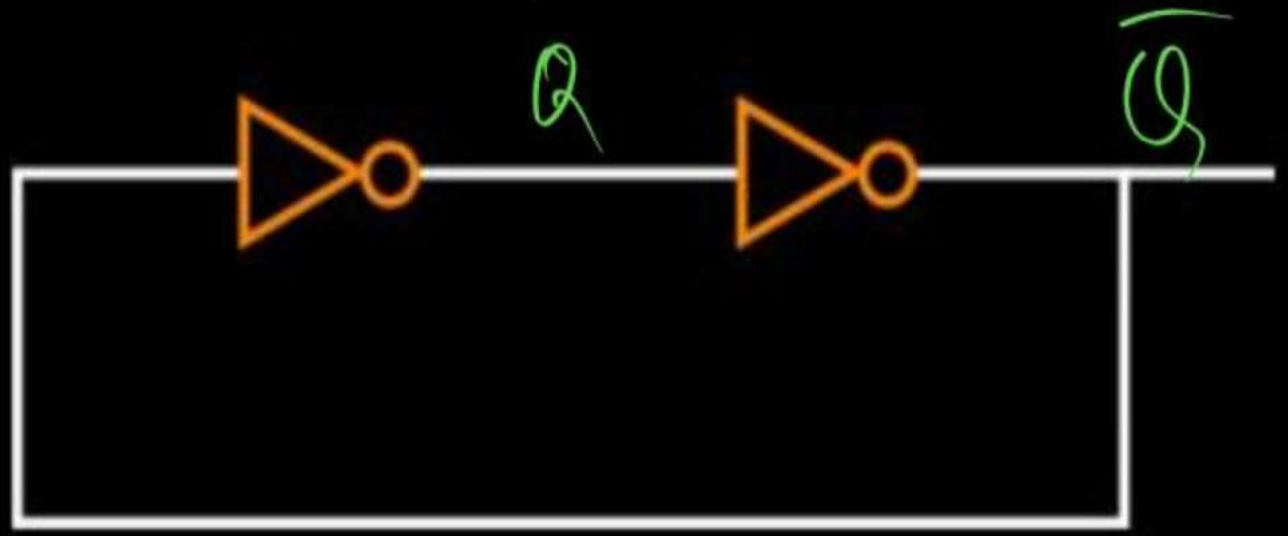
LATCHES

Even

- Basic memory element
- Latches are level triggered
- Latches has two output which is complement of each other

LATCHES & SR FF

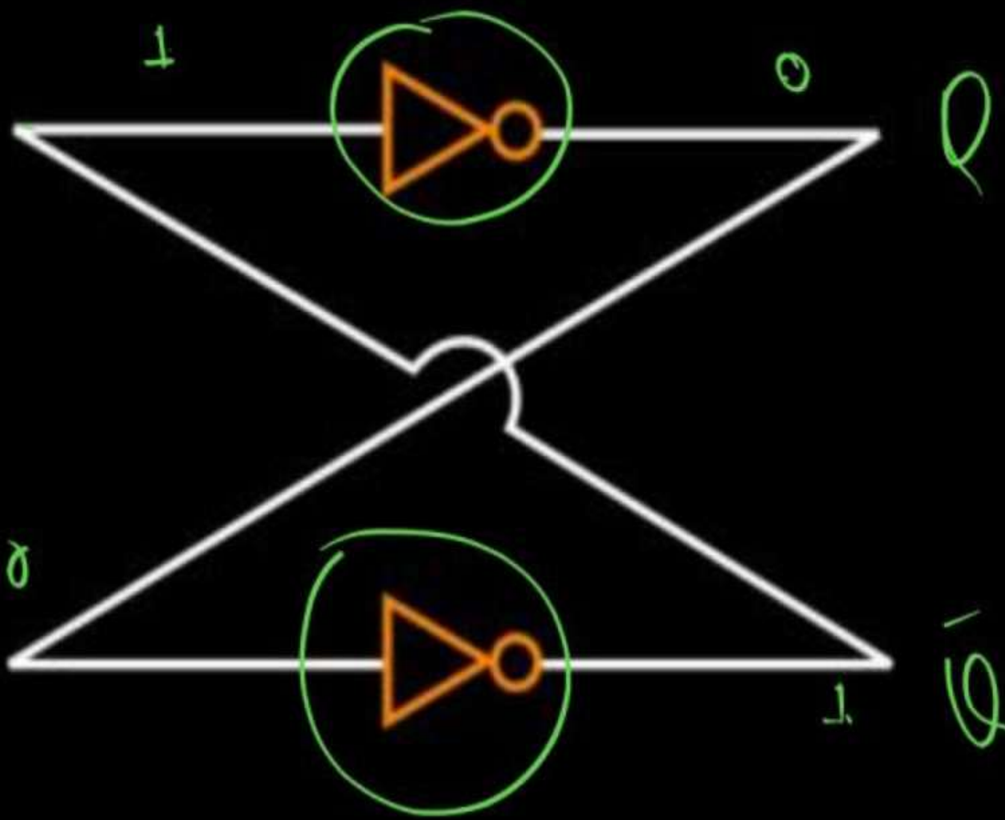
LATCHES



" Basic memory element "

LATCHES & SR FF

LATCHES

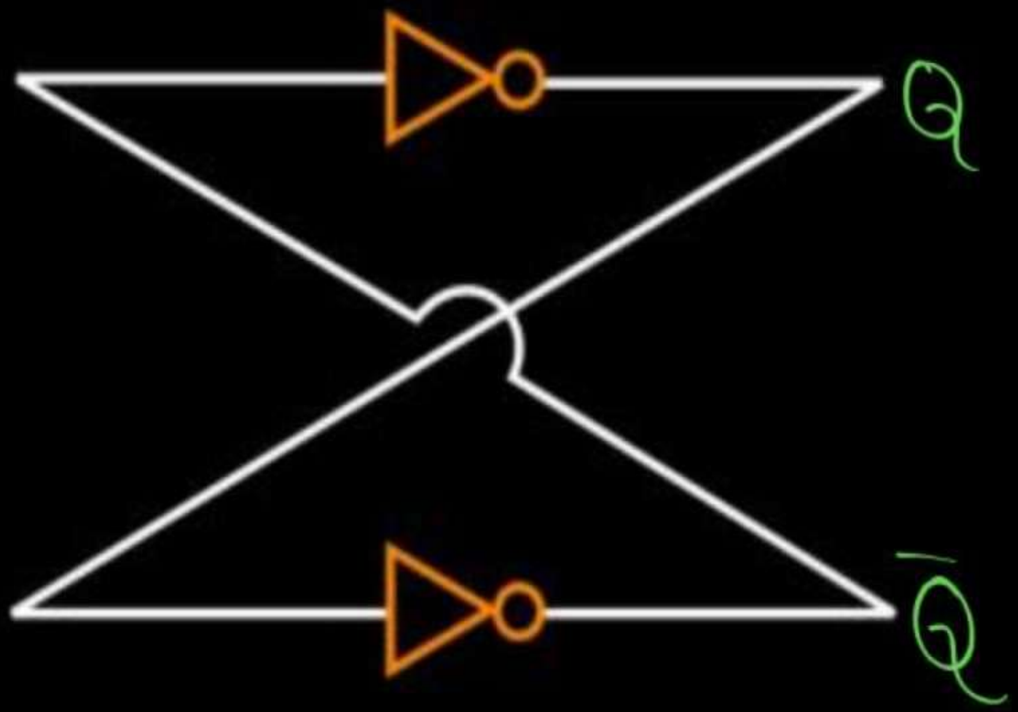


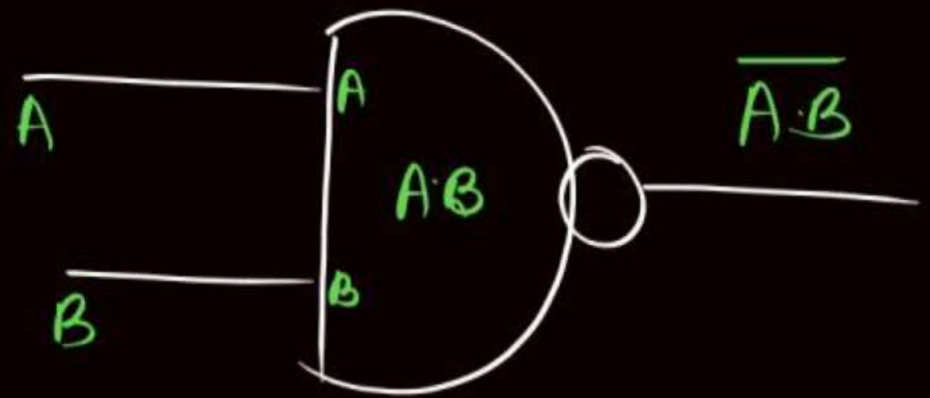
NAND

NOR

LATCHES & SR FF

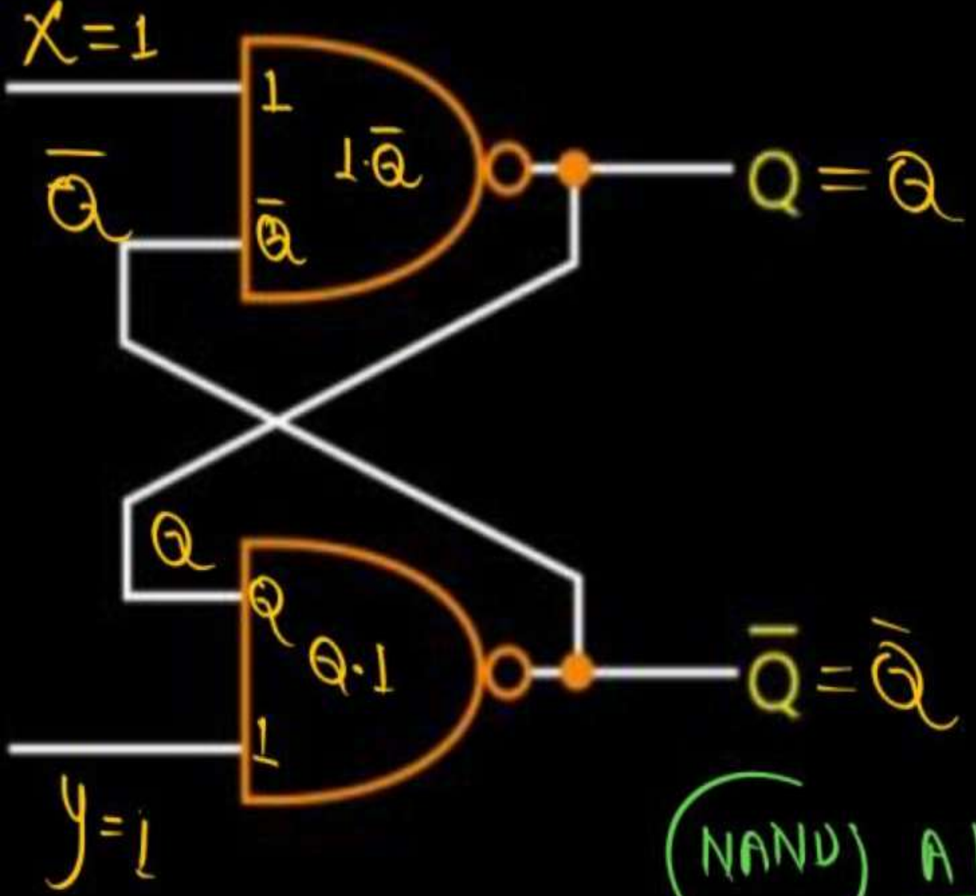
LATCHES




A
B
A
B
A·B
$\overline{A \cdot B}$

LATCHES & FLIP FLOP

$1 \cdot \bar{Q} = \bar{Q}$



NAND

A	B	y
0	0	1
0	1	1
1	0	1
1	1	0

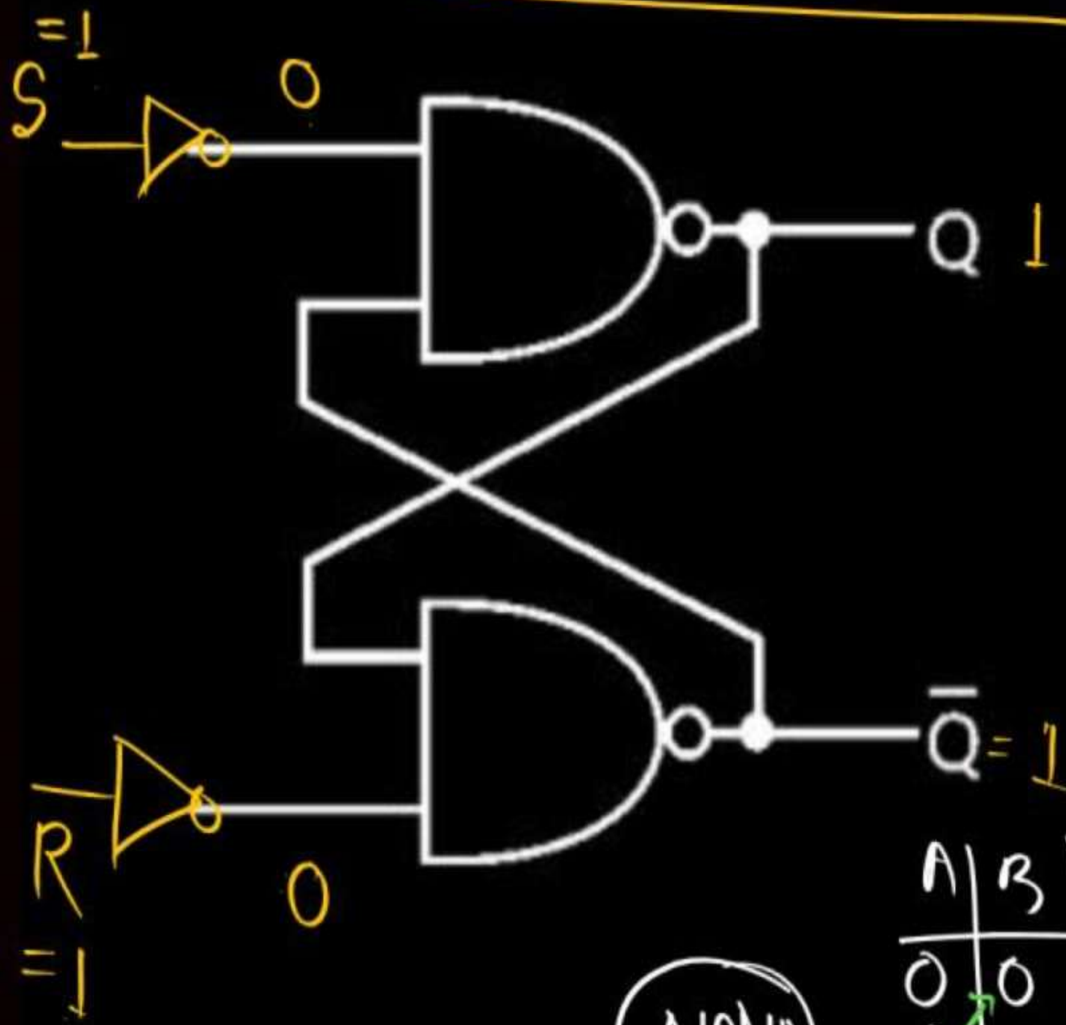
गलत है मैं नहीं खेल रहा

forbidden
don't care

X	Y	Q	$\bar{Q}$	
0	0	1	1	Invalid
0	1	1	0	
1	0	0	1	
1	1	Q	$\bar{Q}$	HOLD/ MEMORY

LATCHES & FLIP FLOP

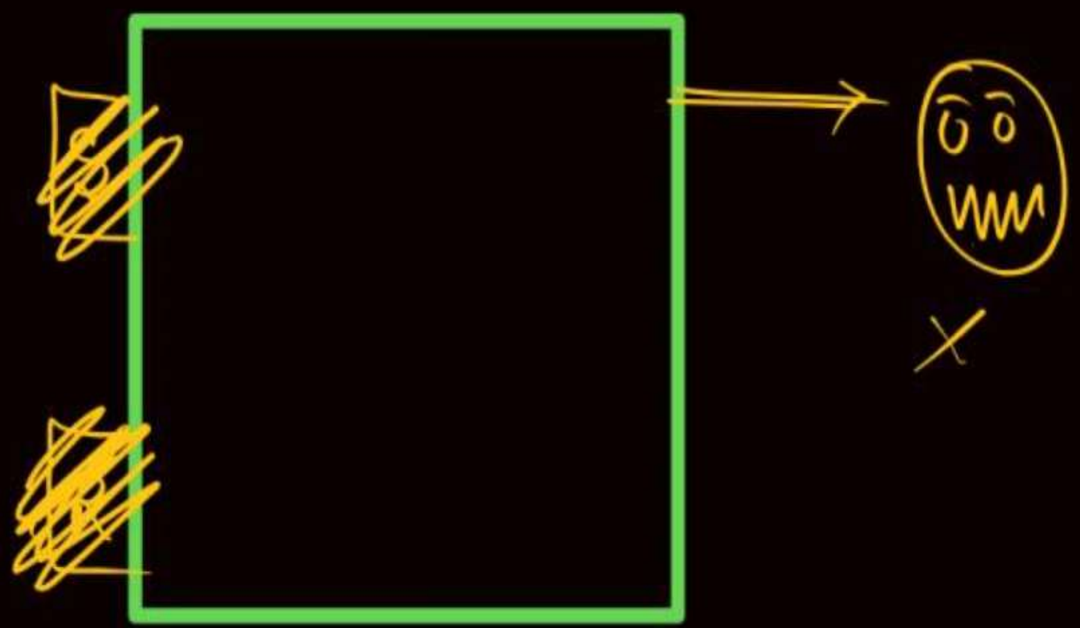
SET- RESET LATCH.

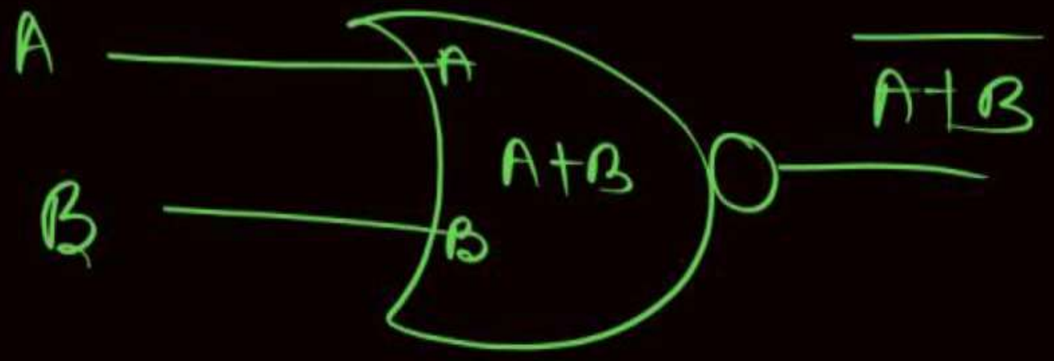


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

	Set	Reset	o/p	
	S	R	Q	$\bar{Q}$
HOLD	0	0	q	$\bar{q}$
Reset	0	1	0	1
Set	1	0	1	0
Invalid	1	1	1	1

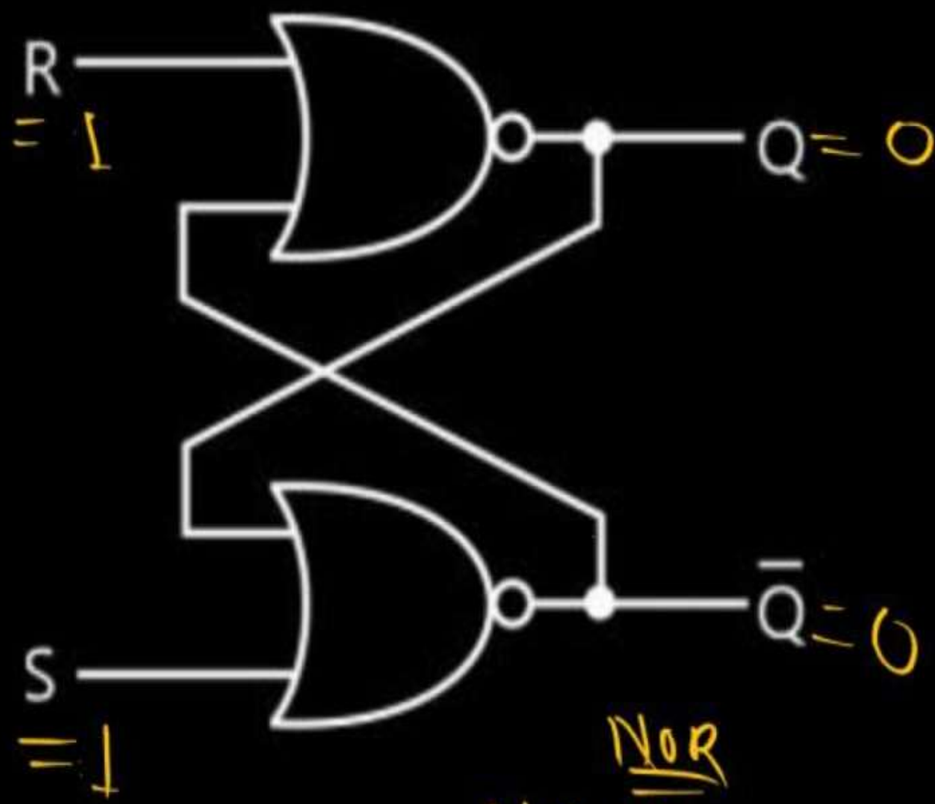
SR Latch




A
B
A
B
A+B
$\overline{A+B}$

LATCHES & FLIP FLOP

R-S Latch



S	R	Q	Q̄
0	0	Q	Q̄
0	1	0	1
1	0	1	0
1	1	X	X

HOLD

Reset

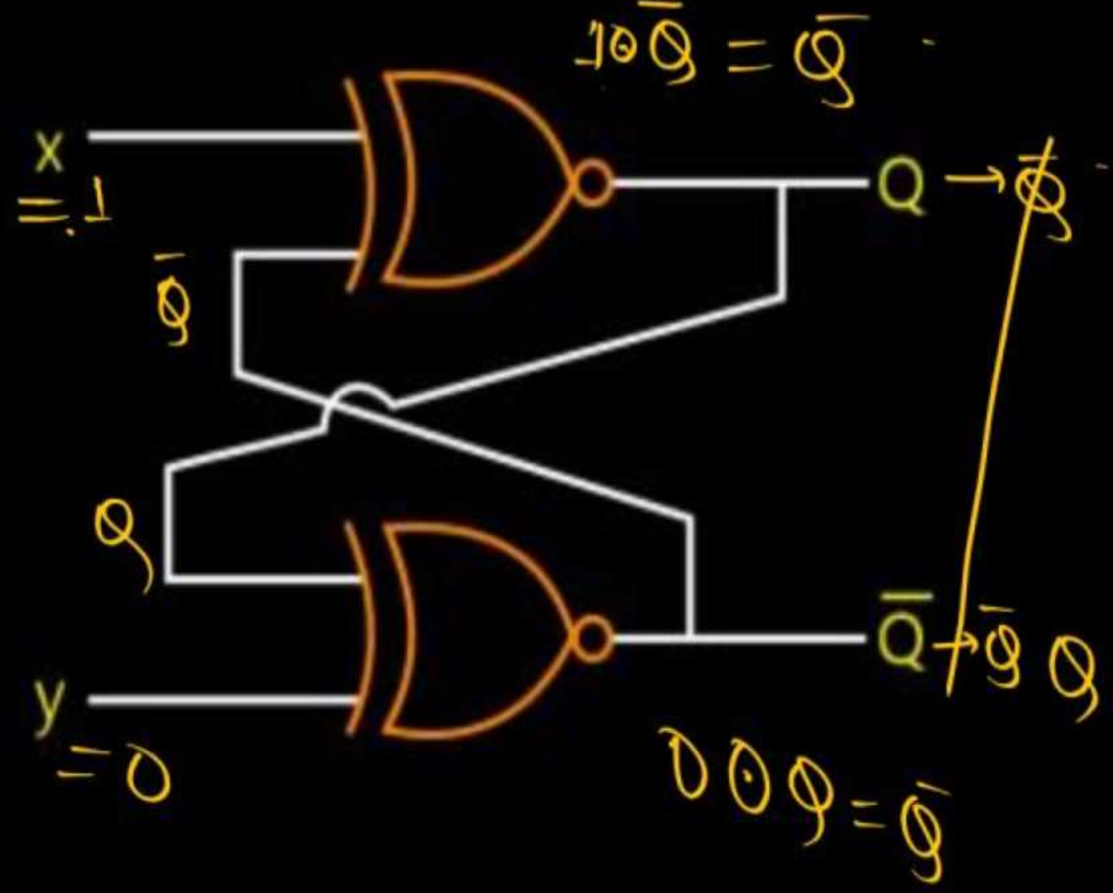
Set

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

LATCHES & FLIP FLOP

$$\begin{cases} Q \odot Q = 1 & Q \odot \bar{Q} = 0 \\ Q \odot 1 = Q & Q \odot 0 = \bar{Q} \\ \bar{Q} \odot 1 = \bar{Q} & \bar{Q} \odot 0 = Q \end{cases}$$

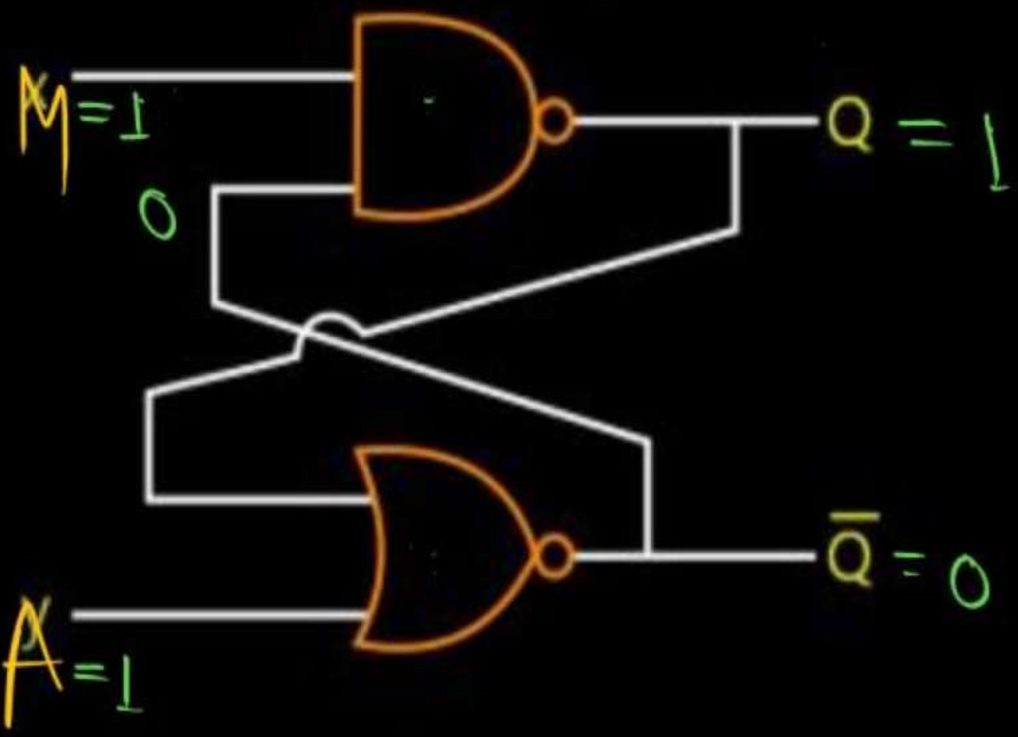


X	Y	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	Q	Q
1	0	$\bar{Q}$	$\bar{Q}$
1	1	$\bar{Q}$	Q

Toggle

LATCHES & FLIP FLOP

MA Latch



NAND

a	b	y
0	0	1
0	1	1
1	0	1
1	1	0

NOR

A	B	y
0	0	1
0	1	0
1	0	0
1	1	0

~~M~~	~~A~~	Q	$\bar{Q}$
0	0	1	0
0	1	1	0
1	0	q	$\bar{q}$
1	1	1	0

QUESTION

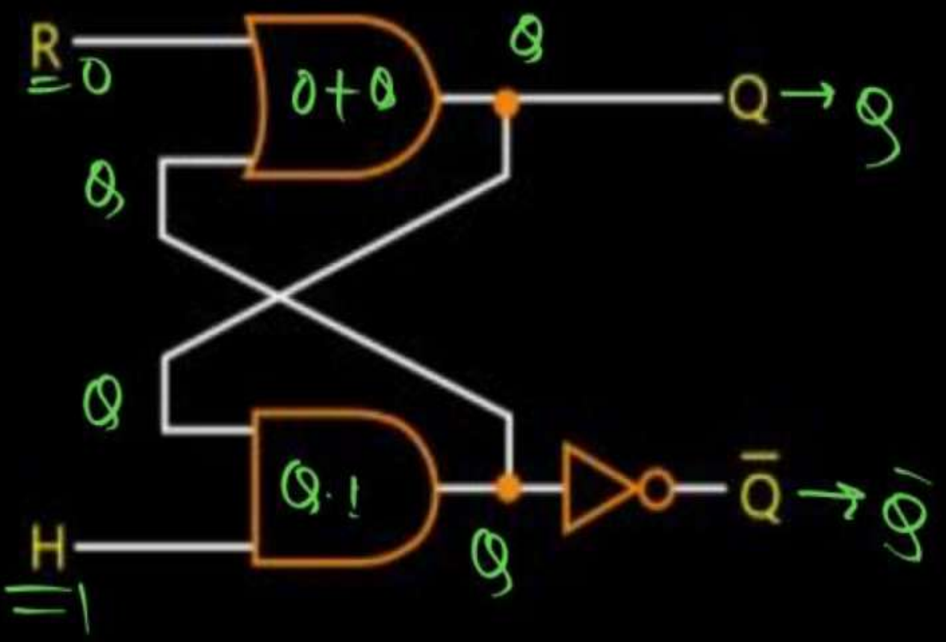
Consider a latch circuit shown in figure below. Which of the following set of input is invalid for circuit?

A. R=0 H=0 → $Q=0$ $\bar{Q}=1$ Valid

B. R=0 H=1 → $Q=Q$ $\bar{Q}=\bar{Q}$ Hold (Valid)

C. R=1 H=0 → $Q=1$ $\bar{Q}=1$ Invalid

D. R=1 H=1 → $Q=1$ $\bar{Q}=0$ Valid



E. Sir, Mai Gajni hu.

OR

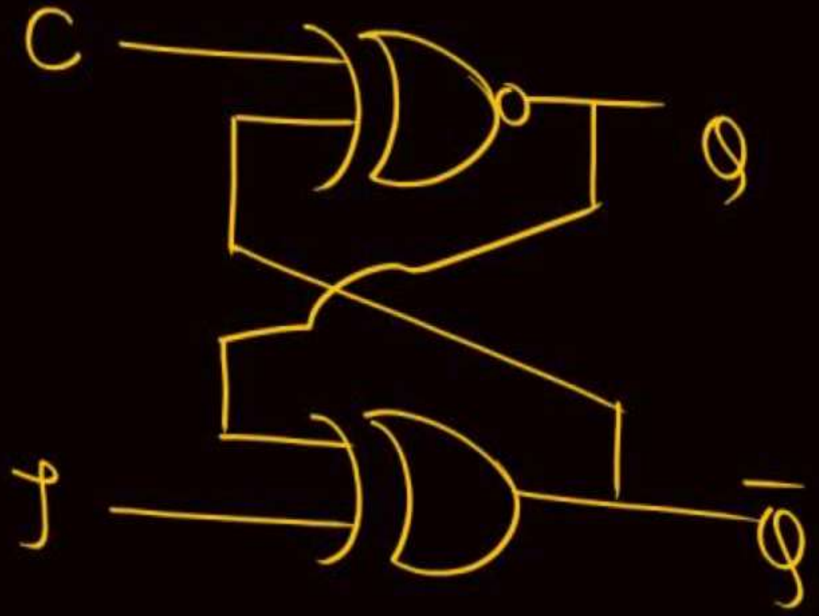
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

CJ latch

H.W



QUESTION

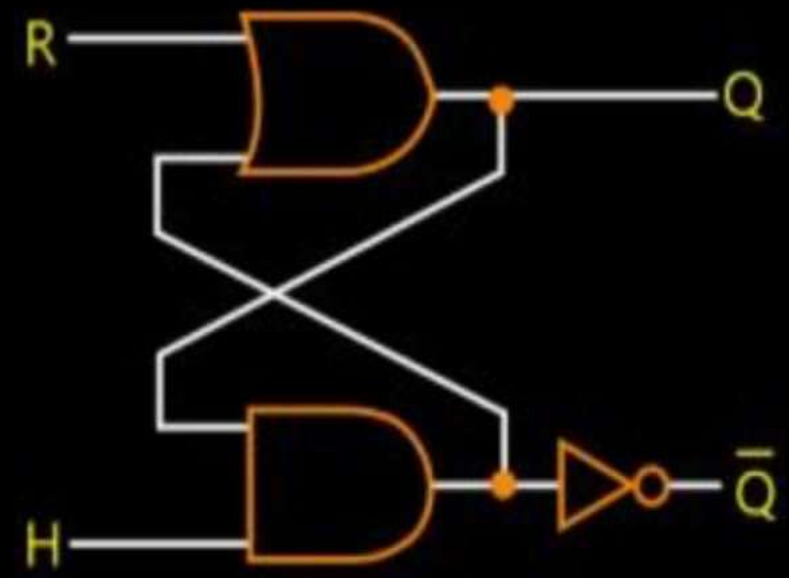
Consider a latch circuit shown in figure below. Which of the following set of input is invalid for circuit?

A. R=0 H=0

B. R=0 H=1

C. R=1 H=0

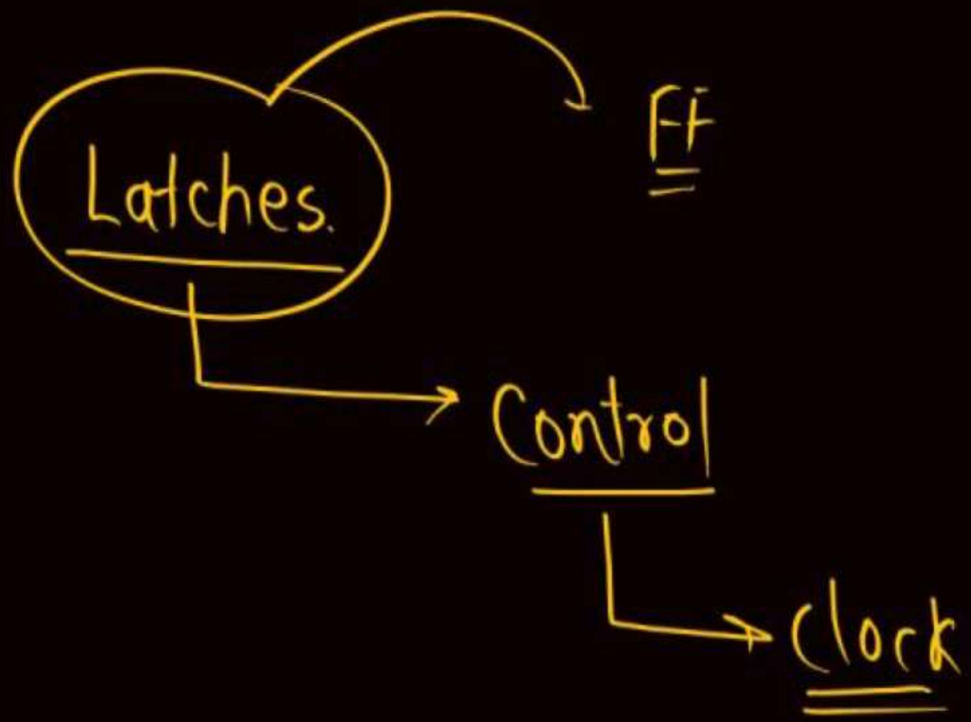
D. R=1 H=1

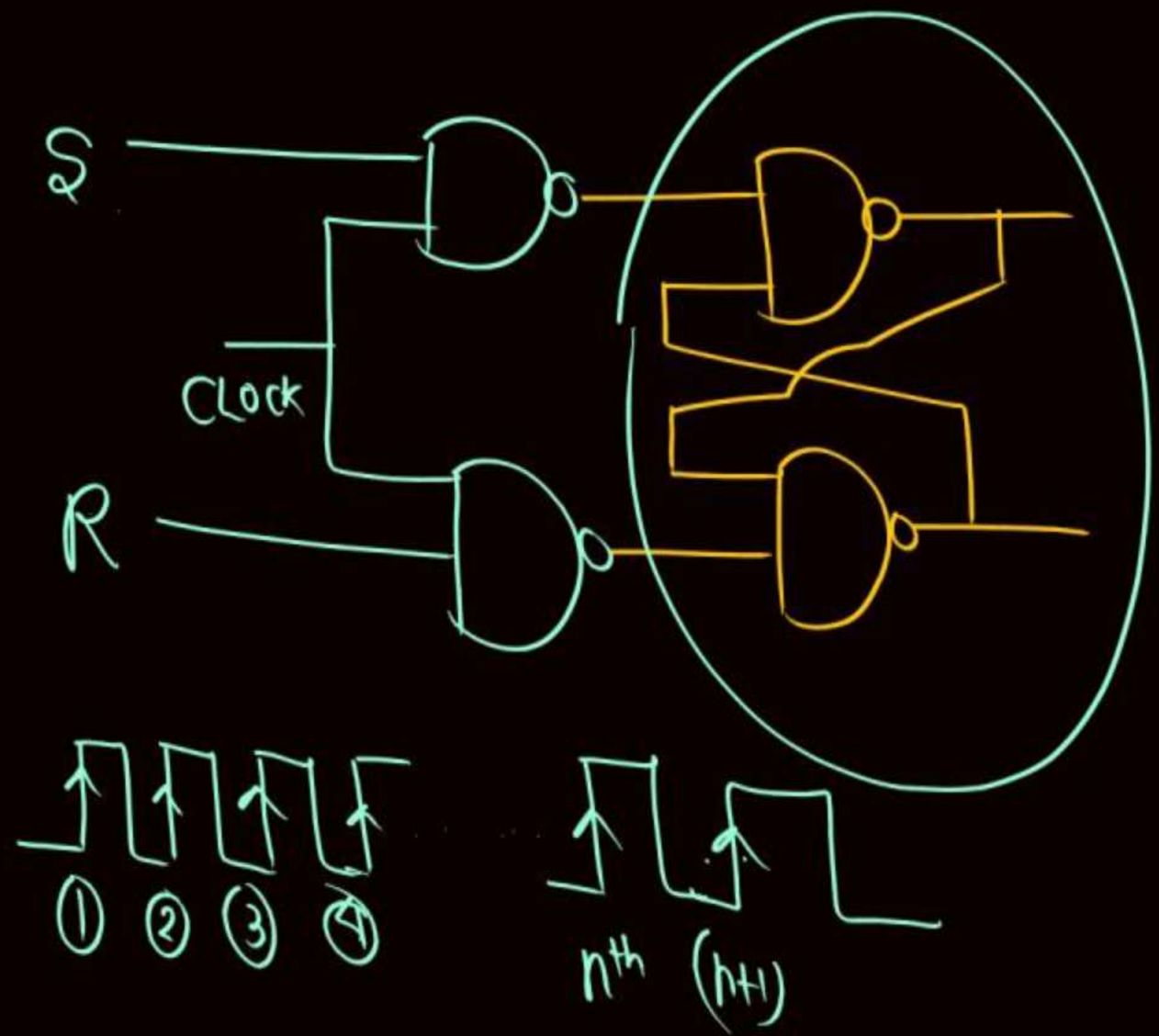


ABOUT ME

- Cleared Gate Multiple times with double Digit Rank (AIR 23, AIR 26)
- Qualified ISRO Exam
- Mentored More then 1 Lakhs+ Students (Offline & Online)
- More then 250+ Motivational Seminar in various Engineering College including NITs & Some of IITs

Chandan Jha


Latches.
FF
Control
Clock



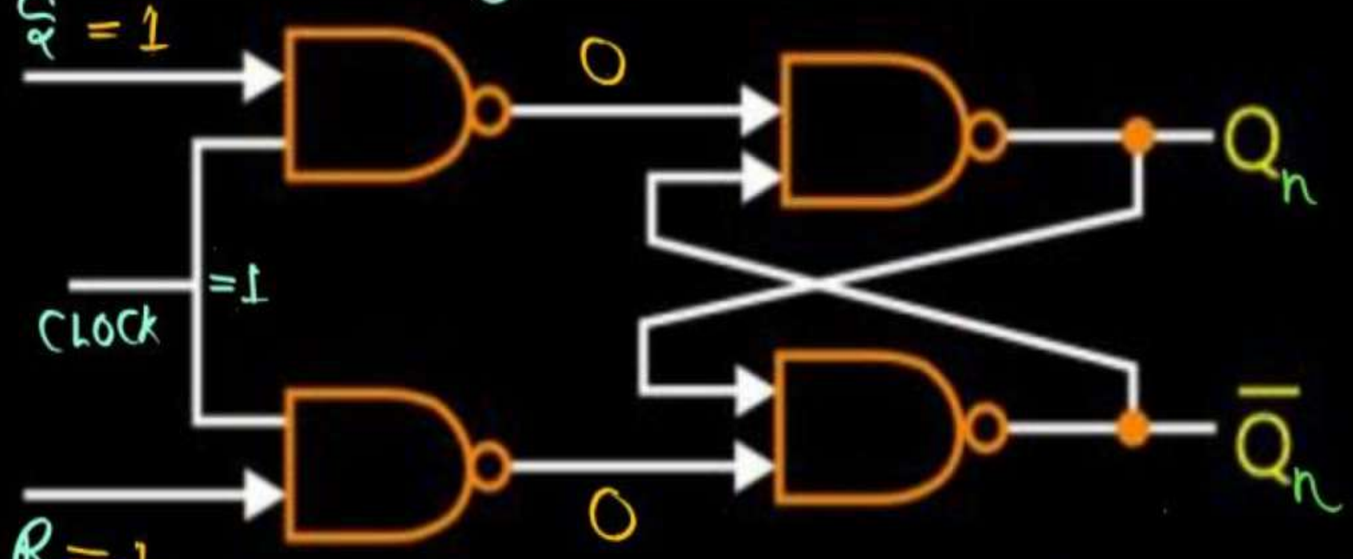
n^{th}	$(n+1)^{th}$
Q_n	Q_{n+1}

① Circuit Diagram
② Truth table
③ characteristic Table
④ characteristic Equation
⑤ Excitation Table
⑥ State Diagram

inputs	P.S Q_n	N.S Q_{n+1}

LATCHES & FLIP FLOP

① Circuit Diagram



Q_{n+1}

1

1

② Truth Table

S	R	Q_{n+1}	$\bar{Q}_{n+1}$	
0	0	Q_n	$\bar{Q}_n$	→ HOLD
0	1	0	1	RESET
1	0	1	0	SET
1	1	x	x	Invalid / forbidden / don't care, ये नहीं होना चाहिए

LATCHES & FLIP FLOP

③ Characteristic Table :→

	S	R	Q_n	Q_{n+1}
0	0	0	0	0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	0
4	1	0	0	1
5	1	0	1	1
6	1	1	0	X
7	1	1	1	X

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

$$Q_{n+1}(S,R,Q_n) = \Sigma m(1,4,5) + \Sigma d(6,7)$$

LATCHES & SR FF

④ Characterstic Equation

$$Q_{n+1}(S,R,Q_n) = \Sigma m(1,4,5) + \Sigma d(6,7)$$

S \ RQn	$\bar{R}\bar{Q}_n$ (00)	$\bar{R}Q_n$ (01)	RQ_n (11)	$R\bar{Q}_n$ (10)
0		1		
1	1	1	X	X

$$Q_{n+1} = S + \bar{R}Q_n$$

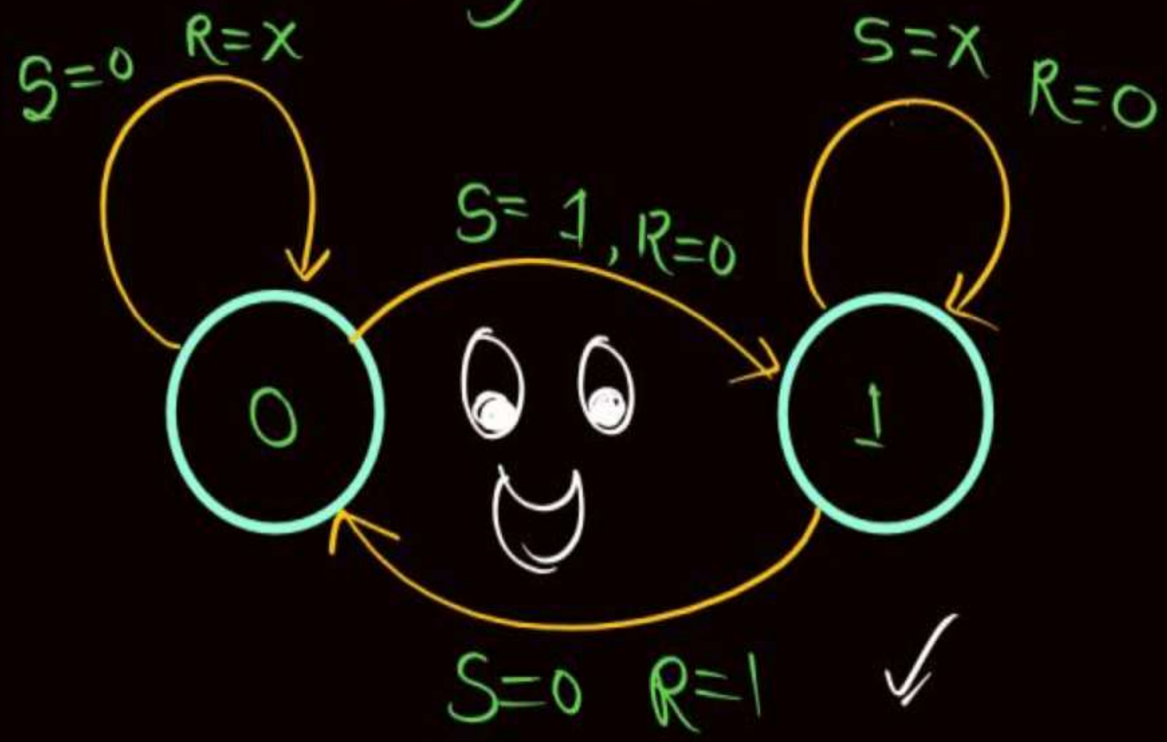
⑤ Excitation Table.

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

C.T.

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

⑥ State Diagram



E.T

Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

RECAPE

Circuit Diagram

↓

Truth Table

↓

Char. Table ⟶ Excitation Table ⟶ State Diagram

↓

Char. Equation

#Maza

#DEC

Truth table

C	J	Q_{n+1}
0	0	Q_n
0	1	$\overline{Q_n}$
1	0	1
1	1	Q_n

① Char. T

② Char. Eq

③ Excitation Table

④ State Diagram


THANK
YOU!