

# DIGITAL CIRCUITS

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# DIGITAL CIRCUITS

*Unique way of covering the syllabus*

## Syllabus

### 1. Basics

- Boolean Algebra
- Logic Gates
- K – Map
- Number systems

### 2. Combinational Circuits

- Arithmetic circuits
- Multiplexer and D- multiplexer
- Decoder and Encoder
- Compactor
- Code converter
- Parity generator and checkers

### 3. Sequential Circuits

- Flip Flops
- Registers
- Counters
- State machines

## UNIQUE WAY OF TEACHING

- BUILDING THE STRONG CONCEPT
- SOLVING BASIC PROBLEM TO MAKE MORE STRONG IN CONCEPTS
- SOLVING PRVIOUS GATE and ESE PROBLEMS

# **Preparation strategy**

**1. Class notes**

**2. Previous papers of GATE**

- ECE
- EEE
- IN
- CS

**3. Previous papers of ESE**

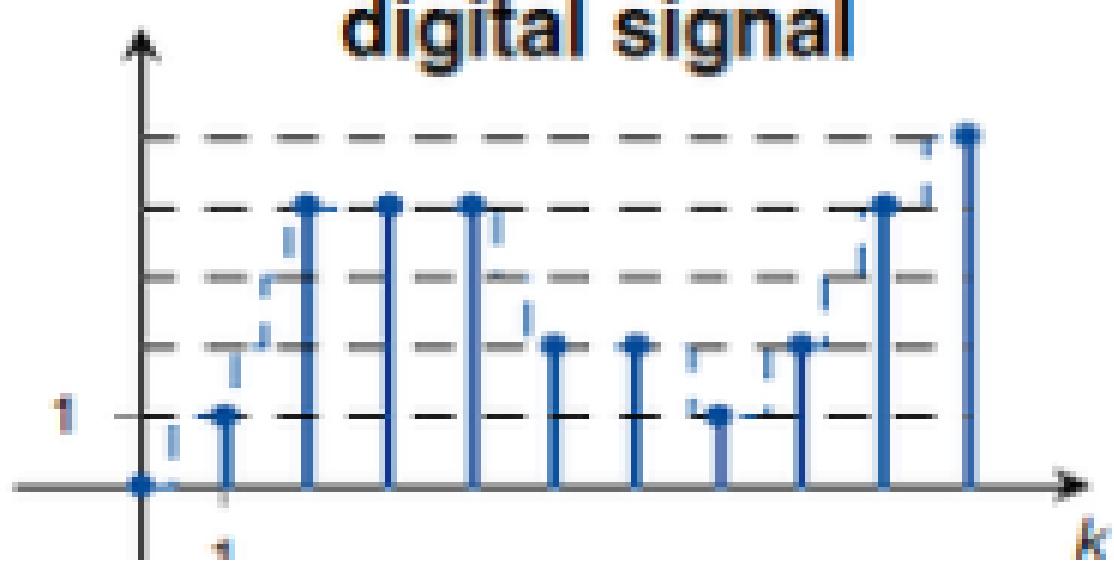
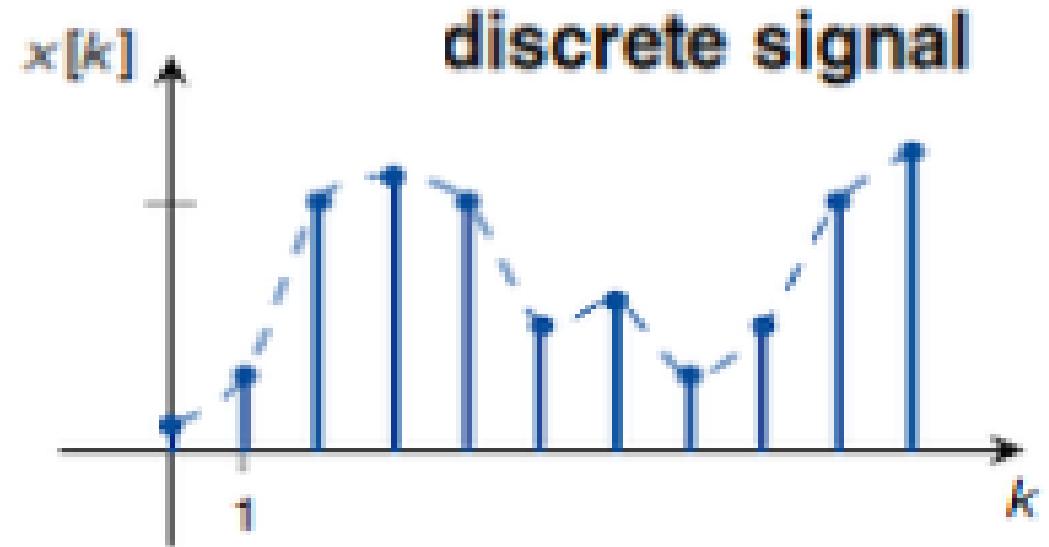
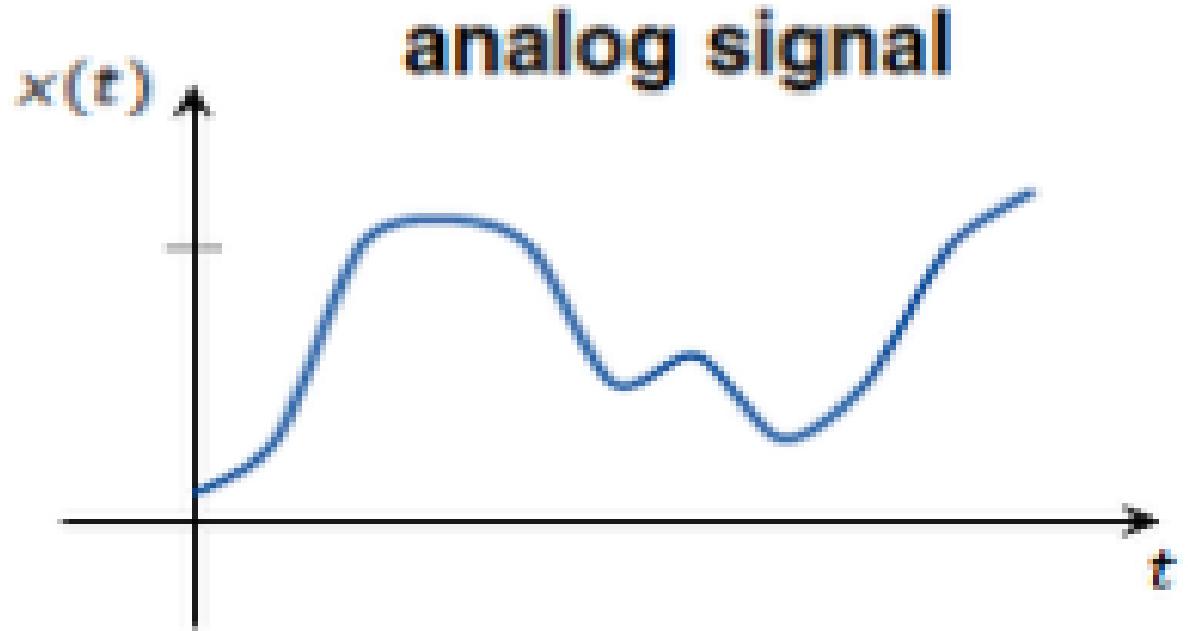
- ECE
- EEE

**SOLVE ALL THE DPPs**

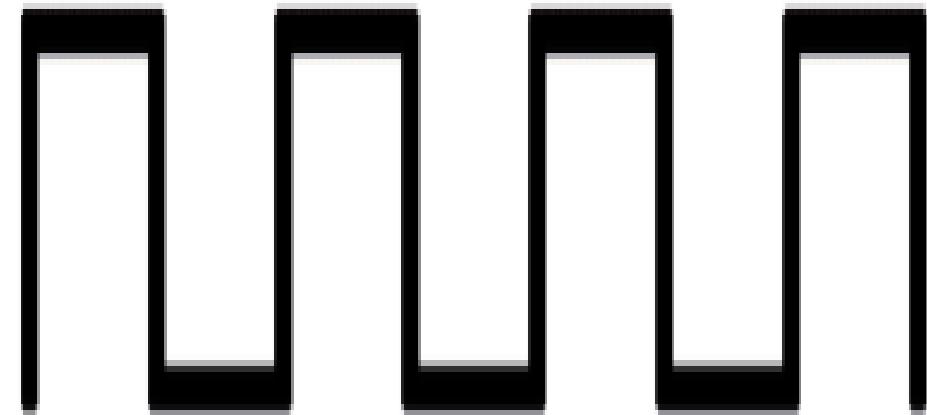
# Analog Signal :

If the signal amplitude take any value i.e infinite number of possibilities then is called as analog signal

Amplitude	Time	Signal
Continuous	Continuous	Analog signal
Continuous	Discrete	Discrete signal
Discrete	Discrete	Digital signal



Digital



- If the digital signals takes only two possible amplitudes , then it is called as **Binary Digital Signal**
- The system which process the analog signals is called as analog system .
- The system which process the digital signals is called as digital system .

# Logic Systems

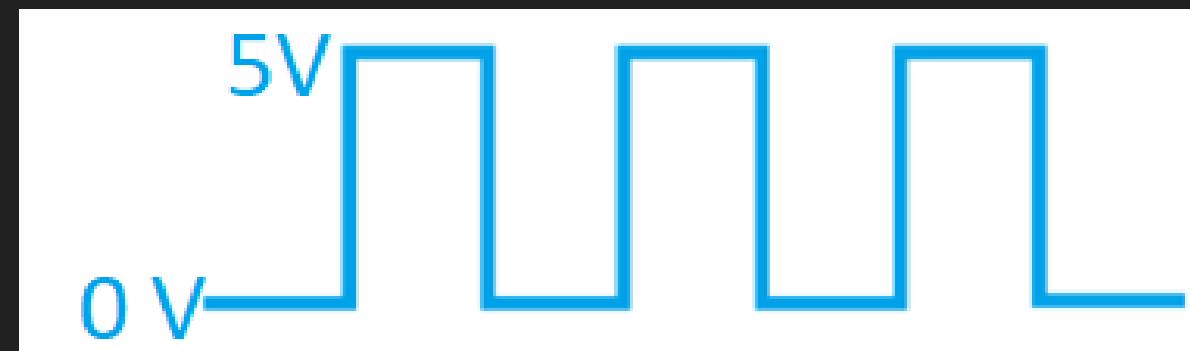
## 1. Positive logic system

High voltage corresponds to logic “ 1 ”

Maximum positive value is taken as logic ‘ 1 ’

+5V ----> logic “1”

0V ----> logic “0 ”



# Logic Systems

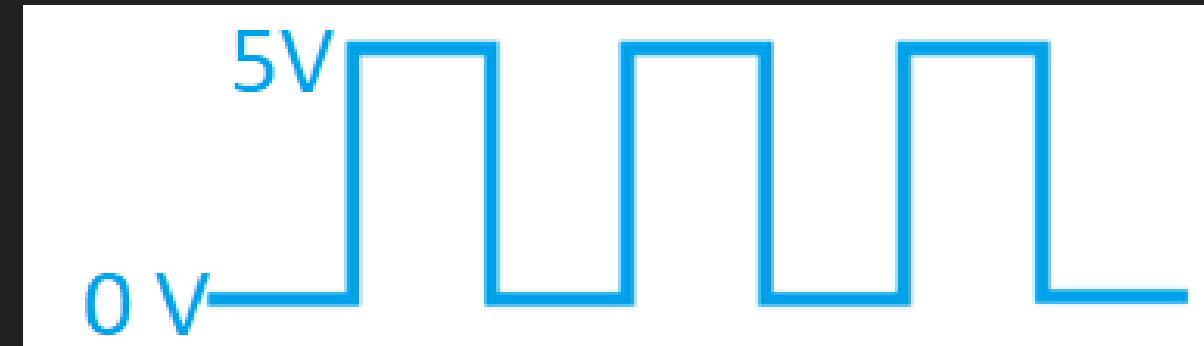
## 2. Negative logic system

High voltage corresponds to logic “ 0 ”

Maximum positive value is taken as logic ‘0 ‘

+5V ----> logic “0”

0V ----> logic “1 “



A

B

Digital  
system

Y

A	B	Y
0V	0V	0V
0V	5V	0V
5V	0V	0V
5V	5V	5V

## POSITIVE LOGIC SYSTEM

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

## NEGATIVE LOGIC SYSTEM

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

A positive logic system is converted into negative logic system by using the concept of duality

Finding the dual of a given Boolean expression

1.  $*$   $\leftrightarrow$   $+$

2.  $0 \leftrightarrow 1$

3. Keep the variables as it is

# Boolean Algebra

- It is an analysis tool that is used for analyzing and designing of various digital system
- The i/p vs o/p relationship in digital system is known as logic expression

## OR -Operation

$$A + 0 = A$$

$$1 + A = 1$$

$$A + A = A$$

$$A + \bar{A} = 1$$

## AND-Operation

$$A * 1 = A$$

$$A * 0 = 0$$

$$A * A = A$$

$$A * \bar{A} = 0$$

# Laws of Boolean Algebra

## 1. Commutative Law

$$A + B = B + A$$

$$A * B = B * A$$

## 2. Associative Law

$$A + B + C = (A + B) + C = (B + C) + A = (C + A) + B$$

$$A * B * C = (A * B) * C = (B * C) * A = (C * A) * B$$

### 3.Distributive Law

$$A(B+C) = AB + AC$$

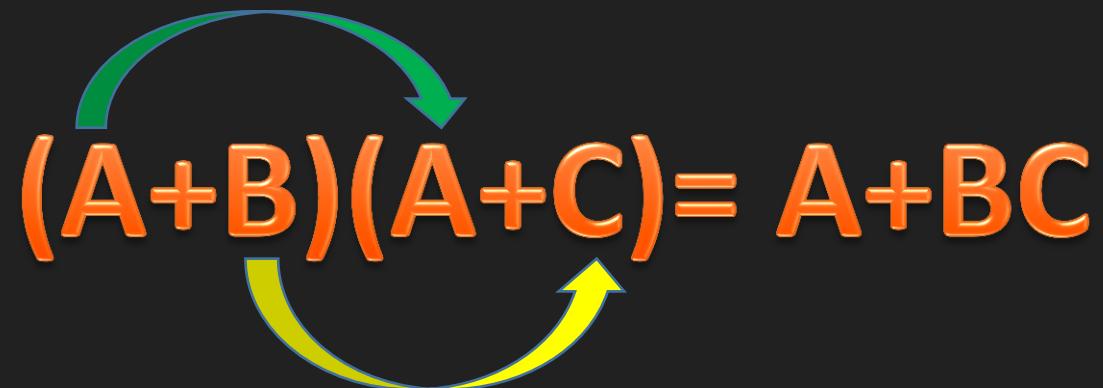
$$A+BC = (A+B)(A+C)$$

### 4. D- Morgan's Law

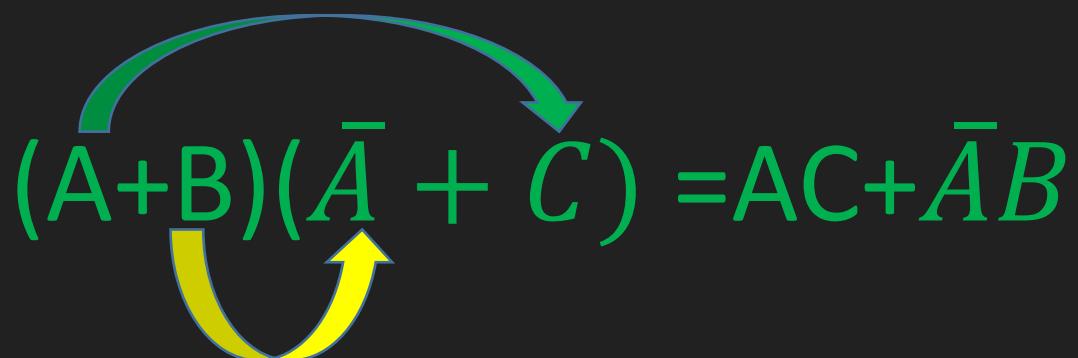
$$\overline{AB} = \bar{A} + \bar{B}$$

$$\overline{A + B} = \bar{A}\bar{B}$$

## 5. Transposition theorem ( T- 1)

$$(A+B)(A+C) = A+BC$$


## 6. Transposition theorem ( T- 2)

$$(A+B)(\bar{A} + C) = AC + \bar{A}B$$


# Problems

Q)  $F = A + BC$ . find  $\overline{F}$ .

$$F_D = A(B+C) \rightarrow \text{Dual}$$

$$\overline{F} = \overline{A}(\overline{B}+\overline{C}).$$

$$Q) \quad F = (A+B)\bar{C} \quad , \quad \text{find } \bar{F}$$

$$F_D = (AB) + \bar{C}$$

$$\bar{F} = \bar{A}\bar{B} + C$$

$$Q) \quad a \left[ b + z(x+\bar{a}) \right] = f \quad \left| \begin{array}{l} = (\underline{\bar{a}+a})(\bar{a}+\bar{x}\bar{b}) + \bar{b}\bar{z} \\ = \bar{a} + \bar{x}\bar{b} + \bar{b}\bar{z} \end{array} \right.$$

$$f_D = a + b[z + x\bar{a}]$$

$$\bar{f} = \bar{a} + \bar{b}[\bar{z} + \bar{x}a]$$

$$\bar{f} = \bar{a} + \bar{b} \bar{z} + \bar{x}a\bar{b}$$

$$= \bar{a} + a\underline{\bar{x}\bar{b}} + \bar{b}\bar{z}$$

$$Q) A + \overline{A}B = (A + \overline{A})(A + B) = A + B.$$

$$Q) A + \overline{A}\overline{B} = (A + \overline{A})(A + \overline{B}) = A + \overline{B}.$$

$$Q) \overline{A} + AB = \overline{A} + B.$$

$$Q) \overline{A} + A\overline{B} = \overline{A} + \overline{B}.$$

$$Q) \quad \overline{a(b+c) + \bar{a}b} \\ = \bar{a} + \bar{b}\bar{c}[a+1] \\ = \bar{a} + \bar{b}\bar{c}$$

$$f = a(b+c) + \bar{a}b$$

$$f_D = a + (bc)(\bar{a}+b)$$

$$\bar{f} = \bar{a} + (\underline{\bar{b}\bar{c}})(\underline{a+\bar{b}})$$

$$= \bar{a} + \underline{a\bar{b}\bar{c}} + \underline{\bar{b}\bar{c}}$$

# Consensus Theorem (RAJINIKANTH VALA)

$$AB + \overline{A}C + BC = AB + \overline{A}C.$$

Proof :

$$AB + \overline{A}C + BC \quad (1)$$

$$AB + \overline{A}C + BC [A + \overline{A}]$$

$$AB + \overline{A}C + \overline{A}BC + \overline{A}BC$$

$$AB(1+C) + \overline{A}C(1+B)$$

$$AB + \overline{A}C.$$

$$Q) \quad A\overline{B} + AC + BC = \overline{A}\overline{B} + BC.$$

$$Q) \quad \underline{\overline{AB}} + \overline{BC} + \underline{\overline{CA}} = \overline{A}\overline{B} + \overline{C}A.$$

$$Q) \quad (A+B)(\overline{A}+C)(B+C) = (A+B)(\overline{A}+C)$$

$$Q) \quad \underline{AB} + \overline{A}\underline{CD} + \underline{BCD} = AB + \overline{ACD}$$

$$Q) \quad ABC + \overline{A}D + \overline{B}D + CD.$$

$$A + \overline{A}B = (A + \overline{A})(A + B)$$

$$ABC + D(\overline{A} + \overline{B}) + CD.$$

$$ABC + D\overline{AB} + CD.$$

$$(AB) = x.$$

$$\underline{ABC} + \overline{\underline{AB}}D + CD.$$

$$xC + \overline{x}D + CD.$$

$$= xC + \overline{x}D = ABC + \overline{AB}D.$$

✓

=

$$Q) f = \overline{A}B + \overline{B}C + \underline{\overline{C}A} + A\overline{B} + AC + B + \overline{C}$$

$$= \overline{A}B + \overline{B}C + A\overline{B} + AC + B + \overline{C}[1 + A]$$

$$= \overline{A}B + \overline{B}C + A\overline{B} + AC + B + \overline{C}$$

$$= \overline{A}B + \overline{B}C + B + \underline{A} + \overline{C} + \underline{A}$$

$$= B[1 + \bar{A}] + A + \overline{C} + \overline{B}$$

$$= B + A + \overline{C} + \overline{B} = 1 + A + \overline{C} = 1$$

$$\overline{C} + \overline{B} C.$$

$$(\overline{C} + \overline{B}) (\overline{C} + C)$$

Q) If  $X^* Y = \overline{XY}$ , then the minimized expression of  $[(\underline{(x+y)*y}) * z]$  is ..

$$(x+y)*y = \overline{(x+y)y} = \overline{xy+y} = \overline{y(1+x)} = \overline{y}$$

$$\overline{y}*z = \overline{\overline{y}z} = \underline{\underline{y+z}}$$

Q) If  $f(A, B) = \bar{A} + B$ , then the simplified expression of  
 $f[(f(x+y, y)), z]$  is .....

$$f(x+y, y) = \overline{x+y} + y = \overline{x}\overline{y} + y = (y+x)(\overline{y}+y) = y\overline{x}$$

$$f(\overline{x+y}, z) = \overline{\overline{x+y}} + z = xy + z$$

Q) Minimize the following Boolean expression  $(\underline{A + B + C})(\underline{A + B + \bar{C}})(A + \bar{B} + C)$

$$[(\underline{\underline{A + B}}) + \underline{0}] [\underline{\underline{A + (\bar{B} + C)}}]$$

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$$A + B(\bar{B} + C)$$

$$\underline{A + BC}$$

Q) Minimize the following Boolean expression  $xy + \overline{x}ywz$

$$\begin{array}{c} xy = A \mid A + \overline{A} w z \\ (A + \overline{A})(A + w z) \end{array}$$

$$\overline{xy + wz}$$

Q) Minimize the following Boolean expression  $v + \bar{v}w + \bar{v}\bar{w}x + \bar{v}\bar{w}\bar{x}g = v + \omega + x + g$

$$v + \omega + \bar{v}\bar{\omega} \left[ \underline{x + \bar{x}g} \right]$$

$$v + \omega + \bar{v}\bar{\omega} [x + g]$$

$$\bar{v+\omega} = \bar{v} \cdot \bar{\omega}$$

$$\begin{array}{c} \rightarrow \\ \curvearrowleft \end{array} (v+\omega) + (\bar{v+\omega}) (x+g) \rightarrow$$

$$\underline{\underline{v + \omega + x + g}}$$

$$\left| \begin{array}{l} A + \underline{\bar{A}B} = \\ - \\ = \cancel{(A + \cancel{\bar{A}})} (A + B) \end{array} \right.$$

Q) Minimize the following Boolean expression  $A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D$

$$A + B + C + D$$


# Boolean function representation

**Canonical form :** Each minterm ( maxterms ) contains all the Boolean variables

$$F(A, B, C) = ABC + \bar{A}BC + AB\bar{C} \quad \text{-----> SOP}$$

$$F(A, B, C) = (A+B+C)(A+\bar{B}+C)(\bar{A}+B+\bar{C}) \quad \text{-----> POS}$$

**Minimal Form :** The minimized form of Boolean expression

$$F(A, B, C) = BC + AB$$

$$F(A, B, C) = (A+B)(A+\bar{B})(\bar{A}+\bar{C})$$

**Literal** : A Boolean variable either in normal form (or ) complimented form is known as literal

$$f = \frac{ABC}{③} + \frac{\bar{A}\bar{B}}{②} + \frac{\bar{A}\bar{C}}{②}$$

$A \quad \bar{A}$

**Minterm** : Each term in canonical SOP representation is known as minterm

$$f = \underbrace{ABC}_{③} + \underbrace{\bar{A}\bar{B}\bar{C}}_{③} + \underbrace{A\bar{B}\bar{C}}$$

SOP

**Maxterm**: Each term in canonical POS representation is known as maxterm

$$f = (A+B+C) (\bar{A}+\bar{B}+\bar{C}) (A+\bar{B}+\bar{C}) \rightarrow \text{POS}$$

③

A

B

C

# Digital System

Y

With n- variable number of possible input combinations =  $2^n$

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

# Sum of Product ( + ve logic S/m )

A--> logic high → ‘ 1 ‘

$\bar{A}$  --> logic Low → ‘ 0 ‘

$$Y = \sum m(0, \underline{2}, 3, 5, 7) \checkmark$$

$$Y = \underline{\bar{A} \bar{B} \bar{C}} + \underline{\bar{A} B \bar{C}} + \underline{\bar{A} B C} + \underline{A \bar{B} C} + \underline{A B C}$$

$$y = m_0 + m_2 + m_3 + m_5 + m_7$$

# Product of Sum( - ve logic S/m )

A--> logic Low → ‘ 0 ‘

$\bar{A}$  --> logic high → ‘ 1 ‘

$$Y = \overline{ABC} (1, \underline{4}, 6)$$

$$Y = (A + B + \bar{C}) (\bar{A} + B + C) (\bar{A} + \bar{B} + C)$$

$$Y = \underline{\underline{M_1 \cdot M_4 \cdot M_6}}$$

# Note :

1. Maximum possible minterms =  $2^n$
2. Maximum possible maxterms =  $2^n$
3. Number of minterm's + number of maxterm's =  $2^n$
4. The sum of all the minterms = **ONE**

$$\sum_{i=0}^{2^n - 1} m_i = m_0 + m_1 + m_2 + m_3 = 1$$

5. The product of all maxterms = ZERO

$$\prod_{i=0}^{2^n - 1} M_i = M_0 M_1 M_2 M_3 = 0$$

6. Minterm's and maxterm's of same index are compliment to each other

---

$$\overline{m_i} = M_i$$

$$\overline{m_4} = M_4$$

$$\overline{M_{10}} = m_{10}$$

7. The product of two minterms of different index is .....

$$m_i \cdot m_j = (\bar{A}B)(A\bar{B}) = 0$$

$$m_i \cdot m_i = (\bar{A}B)(\bar{A}B) = \bar{A}B = m_i$$

$$m_i \cdot m_j = 0 \quad \text{if } i \neq j$$

$$= m_i \quad \text{if } i = j$$

8. The sum of two arbitrary maxterms of different index is .....

$$M_1 + M_2 = (A+\bar{B}) + (\bar{A}+B) = 1$$

$$M_i + M_j = M_i \quad \begin{cases} M_i + M_j = 1 & \text{if } i \neq j \\ = M_i & \text{if } i = j \end{cases}$$

Q) Find the Minterms and Maxterms of the following

$$f(A, B, C) = AB + \bar{A}BC + \bar{C} \longrightarrow \begin{array}{c} \text{SOP} \\ \downarrow \end{array}$$

$$f(A, B, C) = AB - + \overline{\bar{A}BC} + --C$$

minterms

6	110	011	001 → 1
7	111	3	011 → 3
			101 → 5
			111 → 7

$$f(A, B, C) = \sum m(1, 3, 5, 6, 7)$$

$$= \prod M(0, 2, 4)$$

Q) Find the Minterms and Maxterms of the following

$$f(A, B, C) = (\underline{B + C})(\underline{\bar{A}})(\bar{A} + \bar{B} + C)$$

$\rightarrow$  POS  $\rightarrow$  maxterms.

True logic S/m

0	0 0 0	4	1 0 0	6.	1 1 0
4	1 0 0	5	1 0 1		
	1 1 0	6			
	1 1 1				

$$\begin{aligned} A &\rightarrow 0 \\ \bar{A} &\rightarrow 1 \end{aligned}$$

$$f(A, B, C) = \prod M(0, 4, 5, 6, 7) = \sum m(1, 2, 3)$$

Q) Find the Minterms and Maxterms of the following

$$f(A, B, C) = \bar{A}B + A\bar{C} + B + ABC$$

010	100	010	111
011	110	011	

$$f = \sum m (2, 3, 4, 6, \neq)$$

$$= \pi M (0, 1, 5).$$

Q) Find the Minterms and Maxterms of the following

$$f(A, B, C) = A + B + \bar{A}B + C$$

$$\begin{aligned} f(A, B, C) &= \sum m (1, 2, 3, 4, 5, 6, 7) \\ &= \overline{\pi M (0)} . \end{aligned}$$

Q) Find the Minterns and Maxterms of the following

$$f(\underline{A, B, C, D}) = AB + \bar{A}BC + B\bar{C}$$

$\overline{AB} - -$	$\overline{\bar{A}BC} -$	$- \overline{B\bar{C}} -$
12 ← 11 00	6	0 10 0 → 4
13 ← 11 01	7	0 10 1 → 5
14 ← 11 10		1 10 0 → 12
15 ← 11 11		1 10 1 → 13

$$f(A, B, C, D) = \Sigma m(4, 5, 6, 7, 12, 13, 14, 15)$$

$$= \pi M(0, 1, 2, 3, 8, 9, 10, 11)$$

Q) Find the Minterms and Maxterms of the following

$$f(A, B, C) = B + \bar{A}BC + \bar{A}\bar{C}$$

$$\begin{aligned} f(A, B, C) &= \sum m (0, 2, 3, 6, 7) \\ &= \overline{\prod M} (1, 4, 5) \end{aligned}$$

Q) Find the Minterms and Maxterms of the following

$$f(A, B, C) = (\bar{B} + \bar{C})(\bar{A} + \bar{B})(A + B + C)(A)$$

$$\begin{array}{c|cc} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{array} \quad \begin{array}{c|cc} 1 & 1 & 0 \\ 1 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 0 & 0 \end{array} \quad \begin{array}{c|ccc} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 1 \end{array}$$

$$f(A, B, C) = \pi m (0, 1, 2, 3, 6, 7)$$

$$= \sum m (4, 5)$$

Q)  $f(P, Q, R) = \overline{P} + QR$

- 1.  $f = \Sigma m(4, 5, 6)$
- 2.  $f = \Sigma m(0, 1, 2, 3, 7) \checkmark$
- 3.  $f = \Pi M(4, 5, 6) \checkmark$
- 4.  $f = \Pi M(0, 1, 3, 7)$

which of the following statements are correct

Q)  $f(P, Q, R, S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$

the function is equivalent to

a)  $PQ + QR + QS$

b)  $P + Q + R + S$

c)  $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$

d)  $\bar{P}R + \bar{P}\bar{R}S + P$

$$\begin{aligned}f &= PQ + \bar{P}QR + \bar{P}Q\bar{R}S \\&= PQ + \bar{P}Q[R + \bar{R}S] \\&= PQ + \bar{P}Q[R + S] \\&= Q[P + \bar{P}(R + S)] \\&= Q[(P + \bar{P})(P + R + S)] \\&= Q[P + R + S].\end{aligned}$$

$$Q) f_1(A, B, C) = \sum m(2, 3, 6) \text{ and}$$

$$f_2(A, B, C) = \sum m(1, 2, 5, 7) \quad \text{Then } f_3 = \underline{f_1 f_2}$$

$$f_4 = f_1 + f_2$$

$$m_i \cdot m_j = \bullet, \quad i \neq j$$

$$= m_i, \quad i = j$$

$$f_4 = f_1 + f_2.$$

$$f_4 = \sum m(1, 2, 3, 5, 6, 7)$$

$$f_1 = m_2 + m_3 + m_6.$$

$$f_2 = m_1 + m_2 + m_5 + m_7.$$

$$f_3 = f_1 \cdot f_2 = m_2 = \sum m(2)$$



1. By using 2- Boolean variables total number of possible Boolean functions = 16
2. By using n- Boolean variables total number of possible Boolean functions =  $2^{2^n}$
3. By using 2- Boolean variables total number of possible Boolean functions having at most 3-minterms =  $4C_0 + 4C_1 + 4C_2 + 4C_3 = 15$
4. By using 2- Boolean variables total number of possible Boolean functions having at most 3- maxterms = 15
5. By using 2- Boolean variables total number of possible Boolean functions having 3- minterms =  $4C_3 = 4$
6. By using n- Boolean variables total number of possible Boolean functions having 2- minterms =  $2^n C_2$
7. By using 5- Boolean variables total number of possible Boolean functions having at most 3- minterms =  $32C_0 + 32C_1 + 32C_2 + 32C_3$

Q)  $Y(A, B, C) = \sum m(1, 4, 6, 7)$  identify the correct statements

$Y(A, B, C) = \pi M(0, 2, 3, 5)$

1.  $Y = m_1 + m_4 + m_6 + m_7$  ✓

2.  $Y = M_0 M_2 M_3 M_5$  ✓

3.  $Y = \overline{m_0 + m_2 + m_3 + m_5}$  ✓

4.  $Y = \overline{M_1 M_4 M_6 M_7} = \overline{M_1} + \overline{M_4} + \overline{M_6} + \overline{M_7}$   
 $= m_1 + m_4 + m_6 + m_7$

5.  $Y = \overline{m_0} \overline{m_2} \overline{m_3} \overline{m_5}$

6.  $Y = \overline{m_0} \cdot \overline{m_2} \overline{m_3} \overline{m_5}$

$Y = M_0 M_2 M_3 M_5$

6.  $Y = \overline{M_1} + \overline{M_4} + \overline{M_6} + \overline{M_7}$   
 $= m_1 + m_4 + m_6 + m_7$

7.  $Y = \underline{m_0} m_2 m_3 m_5$  ✗

8.  $Y = M_1 + M_4 + M_6 + M_7$  ✗

9.  $\cancel{Y = \overline{m_1 m_4 m_6 m_7} = \overline{m_1} + \overline{m_4} + \overline{m_6} + \overline{m_7}}$   
 $= m_1 + m_4 + m_6 + m_7$

10.  $Y = \overline{M_0} + \overline{M_2} + \overline{M_3} + \overline{M_5}$

$Y = \overline{M_0} \cdot \overline{M_2} \overline{M_3} \overline{M_5}$

$= m_0 m_2 m_3 m_5$  ✗

# Duals

1.	$\overline{0} = 1$	$\overline{1} = 0$
2.	$0 \cdot 1 = 0$	$1 + 0 = 1$
3.	$0 \cdot 0 = 0$	$1 + 1 = 1$
4.	$1 \cdot 1 = 1$	$0 + 0 = 0$
5.	$A \cdot 0 = 0$	$A + 1 = 1$
6.	$A \cdot 1 = A$	$A + 0 = A$
7.	$A \cdot A = A$	$A + A = A$
8.	$A \cdot \overline{A} = 0$	$A + \overline{A} = 1$
9.	$A \cdot B = B \cdot A$	$A + B = B + A$
10.	$A \cdot (B \cdot C) = (A \cdot B) \cdot C$	$A + (B + C) = (A + B) + C$
11.	$A \cdot (B + C) = AB + AC$	$A + BC = (A + B)(A + C)$
12.	$A(A + B) = A$	$A + AB = A$
13.	$A(A \cdot B) = A \cdot B$	$A + A+B = A+B$

14.

$$\overline{AB} = \overline{A} + \overline{B}$$

$$\overline{A+B} = \overline{A}\overline{B}$$

15.

$$(A+B)(\overline{A}+C)(B+C) = (A+B)(\overline{A}+C)$$

$$AB + \overline{A}C + BC = AB + \overline{A}C$$

16.

$$(A+C)(\overline{A}+B) = AB + \overline{A}C$$

$$AC + \overline{A}B = (A+B)(\overline{A}+C)$$

17.

$$A + \overline{B}C = (A+\overline{B})(A+C)$$

$$A(\overline{B}+C) = A\overline{B} + AC$$

18.

$$(A+B)(C+D) = AC + AD + BC + BD$$

$$AB + CD = (A+C)(A+D)(B+C)(B+D)$$

19.

$$A + B = AB + \overline{A}B + A\overline{B}$$

$$AB = (A+B)(\overline{A}+B)(A+\overline{B})$$

20.

$$A + B[C + \overline{D+E}] = A + B\overline{C}DE$$

$$A[B + C(\overline{D+E})] = A \cdot (B + \overline{C} + D + E)$$

21.

$$\overline{AB} + \overline{A} + \overline{AB} = 0$$

$$\overline{A+B} \cdot \overline{A}(A+B) = 1$$

22.

$$AB + \overline{A}\overline{C} + A\overline{B}C (AB + C) = 1$$

$$(A+B)(\overline{A+C})[(A+\overline{B}+C) + (A+B)C] = 0$$

23.

$$ABD + ABCD = ABD$$

$$(A+B+D)(A+B+C+D) = A+B+D$$

24.

$$\overline{\overline{AB} + ABC} + A(B + A\overline{B}) = 0$$

$$(\overline{A+\overline{B}})(A+B+C) \cdot (A+B(A+\overline{B})) = 1$$

25.

$$A + \overline{B}C (A + \overline{B}C) = A + \overline{B}C$$

$$A \cdot [\overline{B} + C + A \cdot (\overline{B} + C)] = A \cdot (\overline{B} + C)$$

Q) If  $\underline{A * B} = \underline{AB + \bar{A}\bar{B}}$

MSQ

Let  $C = \underline{A * B}$ , then

- a)  $\underline{B * C} = A$  ✓
- b)  $\underline{A * C} = B$  ✓
- c)  $A * (B * C) = 1$  ✓
- d)  $A * B = B * A$  ✓

$$A * A = AA + \bar{A}\bar{A}$$

$$= A + \bar{A} = 1$$

$$\begin{aligned} B * C &= BC + \bar{B}\bar{C} \\ &= B\left[\underline{A * B}\right] + \bar{B}\left[\underline{\bar{A} * \bar{B}}\right] \\ &= B\left[AB + \bar{A}\bar{B}\right] + \bar{B}\left[\underline{AB + \bar{A}\bar{B}}\right] \\ &= AB + \bar{B}\left[\underbrace{(A + \bar{B})}_{1} \underbrace{(A + B)}_{1}\right] \\ &= AB + \bar{B}\left[\underline{AB + \bar{A}\bar{B}}\right] \\ &= AB + \bar{B} + A\bar{B} = A \end{aligned}$$

$$\begin{aligned}
 A * C &= AC + \overline{A} \overline{C} \\
 &= A[A \cdot B] + \overline{A} \left[ \overline{A * B} \right] \\
 &= A[AB + \overline{A} \overline{B}] + \overline{A} \left[ AB + \overline{A} \overline{B} \right] \\
 &= AB + \overline{A} \left[ (\overline{A} + \overline{B})(A + B) \right] \\
 &= AB + \overline{A} \left[ \overline{A}B + A\overline{B} \right] \\
 &= AB + \overline{A}B = \underline{\underline{B}}
 \end{aligned}$$

## Self Dual Expression

If one time dual of the Boolean expression result the same expression, then it is called as self dual expression

$$f = AB + BC + AC$$

$$\begin{aligned} f_D &= (A+B)(B+C)(A+C) \\ &= (B+AC)(A+C). \end{aligned}$$

$$f_D = AB + BC + AC$$

$$(A+B)(B+C)$$

$$AB + AC + BC + BC.$$

$$B[1 + C + A] + AC$$

$$B + AC$$

## Conditions for the given expression is self dual

1. The number of minterms = number of maxterms

$$\text{number of minterms} + \text{number of maxterms} = 2^n$$

$$\text{number of minterms} = \text{number of maxterms} = 2^{n-1}$$

2. If  $m_i$  belongs to  $f$ , then  $m_{2^n-i-1}$  should belong to  $\bar{f}$

Q) Verify the given Boolean functions are self dual or not

$$f(A, B, C) = AB + BC + CA$$

✓  $f = AB + BC + CA$

$$f = \sum m(3, 5, 6, 7)$$

$$f = \pi M(0, 1, 2, 4)$$

$$\overline{f} = \sum m(0, 1, 2, 4)$$

$$m_3 \rightarrow f$$

$$m_{2^n-1-i} = m_{2^3-1-3} = m_4$$

$$m_2 \rightarrow \overline{f}$$

$$m_1 \rightarrow \overline{\overline{f}}$$

$$m_0 \rightarrow \overline{\overline{f}}$$

Q) Verify the given Boolean functions are self dual or not

$$f(A, B, C) = m(1, 2, 4, 7)$$

$$\overline{f} = \sum m(5, 3, 5, 6)$$

$$\underline{\underline{m_{2^n-1-i}}}$$

Self dual



Q) Verify the given Boolean functions are self dual or not

$$f(A, B, C) = m(0, 1, 2, 5)$$

$$\overline{f}(A, B, C) = \sum m(3, 4, \underline{6}, 7)$$

X

$$m_{2-1-i}$$

## Note:

1.Number of Boolean functions =  $2^{2^n}$

2.Maximum Number of minterms =  $2^n$

3.Maximum Number of maxterms =  $2^n$

4.Number of self dual expressions =  $2^{2^{n-1}}$

Q) A logic circuit have 3 inputs A , B , C and output Y . Output Y is logic 1 for the following

1. A and C are true
2. B and C are false
3. A, B and C are true
4. A, B and C are false

then the minimized expression Y is-----

$$Y = AC + \overline{B}\overline{C} + \overbrace{A\overline{B}C + \overline{A}\overline{B}\overline{C}}^{\cdot}$$

$$Y = AC [1 + B] + \overline{B}\overline{C} [1 + \overline{A}] \cdot$$

$$Y = AC + \overline{B}\overline{C} \cdot$$

Q) A logic circuit have 3 inputs A, B and C. Output is F. F is logic 1 when majority number of inputs are at logic 1, then the minimized expression for F is

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

$$A+A = A$$

$$F = \sum m(3, 5, 6, 7)$$

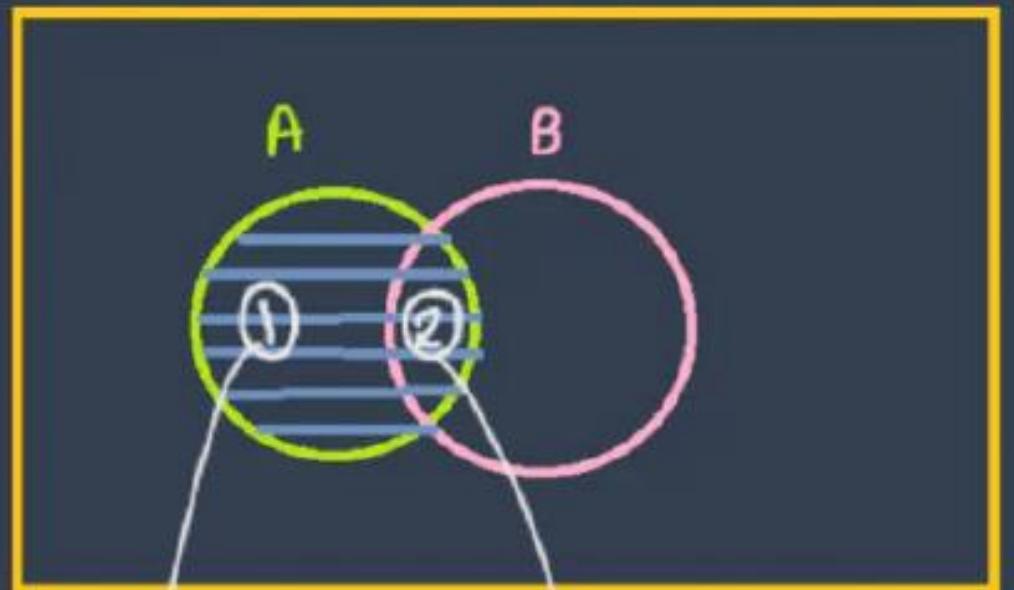
$$F = \overline{ABC} + A\overline{B}C + AB\overline{C} + \underline{\overline{ABC}}$$

$$F = \overline{A}\overline{BC} + \underline{\overline{ABC}} + A\overline{B}C + \overline{ABC} + \overline{AB}\overline{C}$$

$$F = BC + AC + AB$$

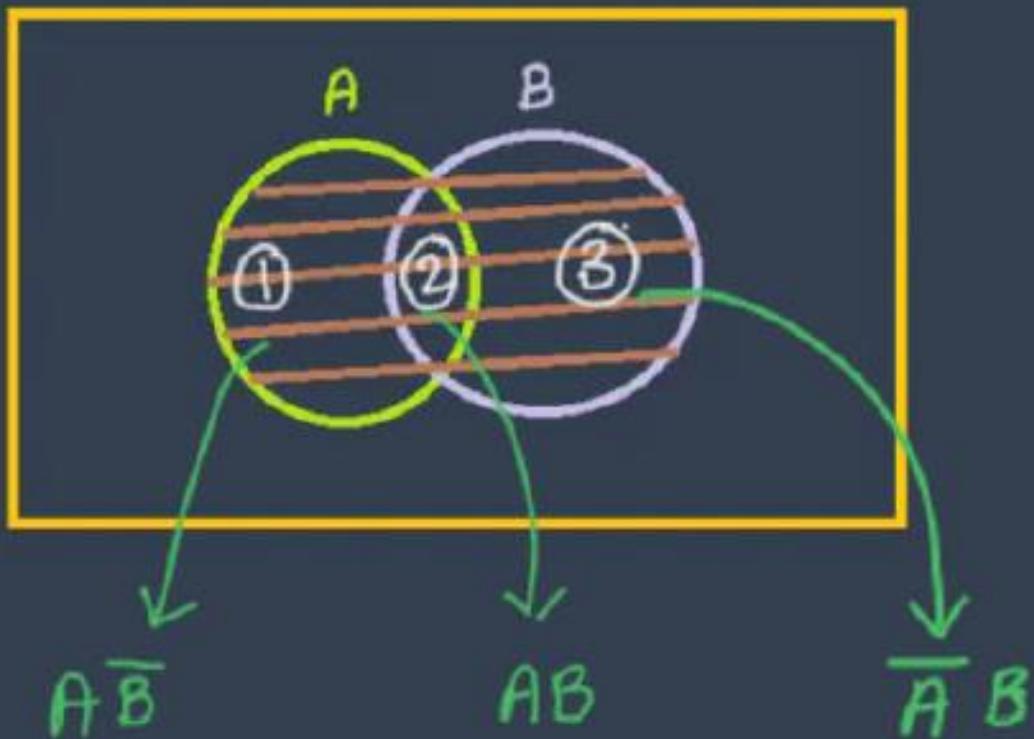
$$F = AB + BC + AC$$

Q) For the given venn diagrams , find the minimized logical expression



$$f = A\bar{B} + AB = A$$

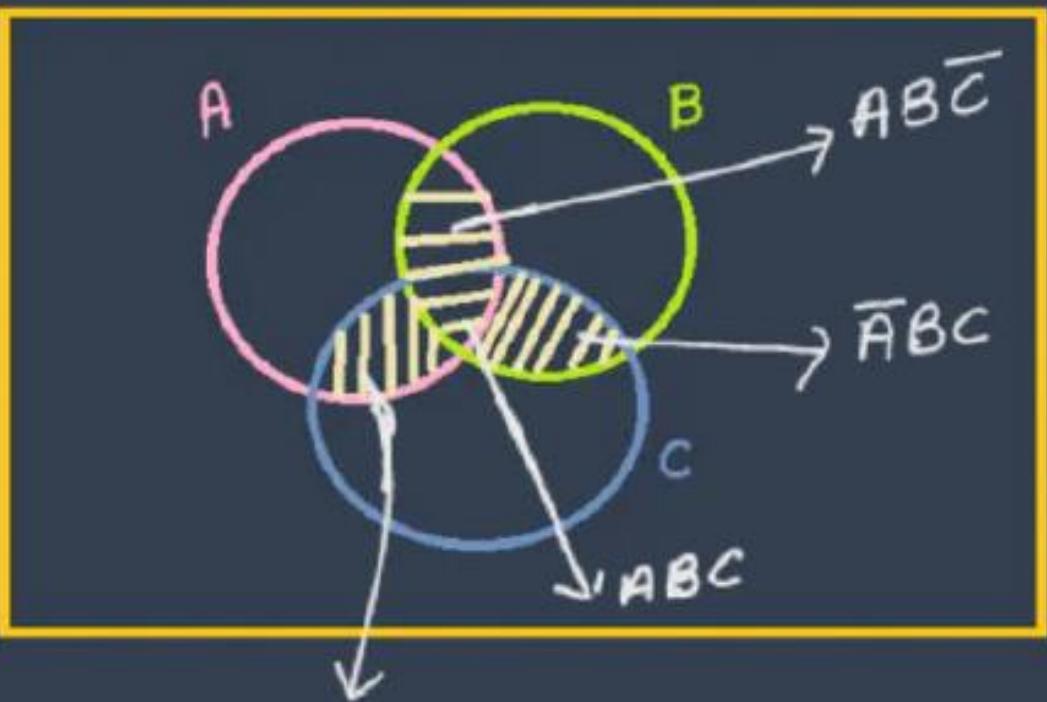
Q) For the given venn diagrams , find the minimized logical expression



$$Y = \overbrace{A\bar{B}} + \overbrace{AB} + \overbrace{\bar{A}B}$$

$$Y = A + B$$

Q) For the given venn diagrams , find the minimized logical expression



$$A\bar{B}C$$

$$Y = AB\bar{C} + \bar{A}BC + A\bar{B}C + ABC.$$

$$Y = AB + BC + AC.$$

# Logic Gates

Logic gates are basic building blocks of digital circuits

Basic Gates	Universal Gates	Derived Gates
<b>AND GATE</b>	<b>NAND GATE</b>	<b>EX- OR GATE</b>
<b>OR GATE</b>	<b>NOR</b>	<b>EX-NOR GATE</b>
<b>NOT</b>		

# NOT Gate

Symbol



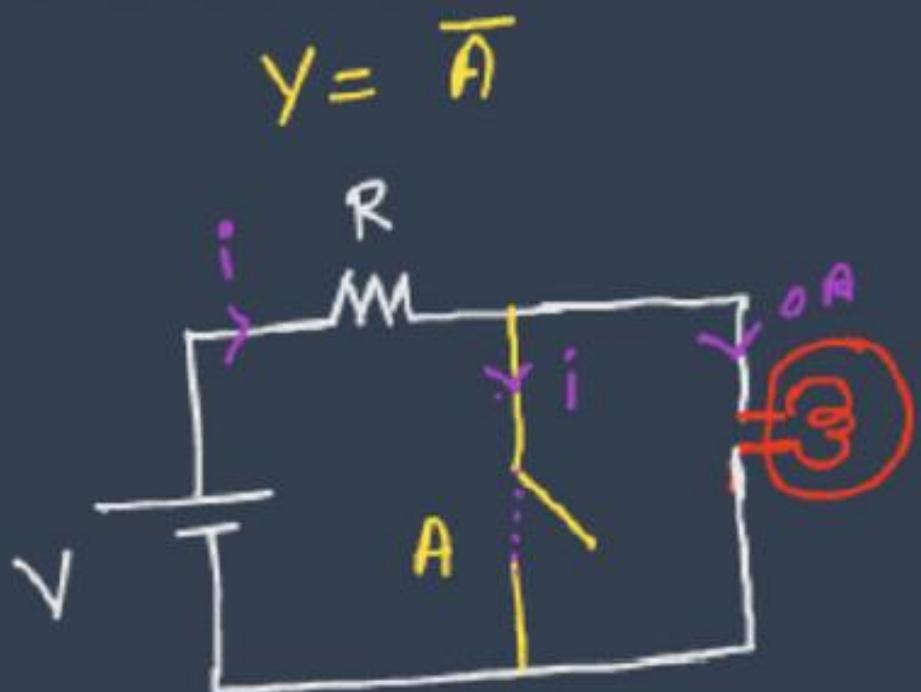
Truth table

$A$	$y$
0	1
1	0

Boolean expression

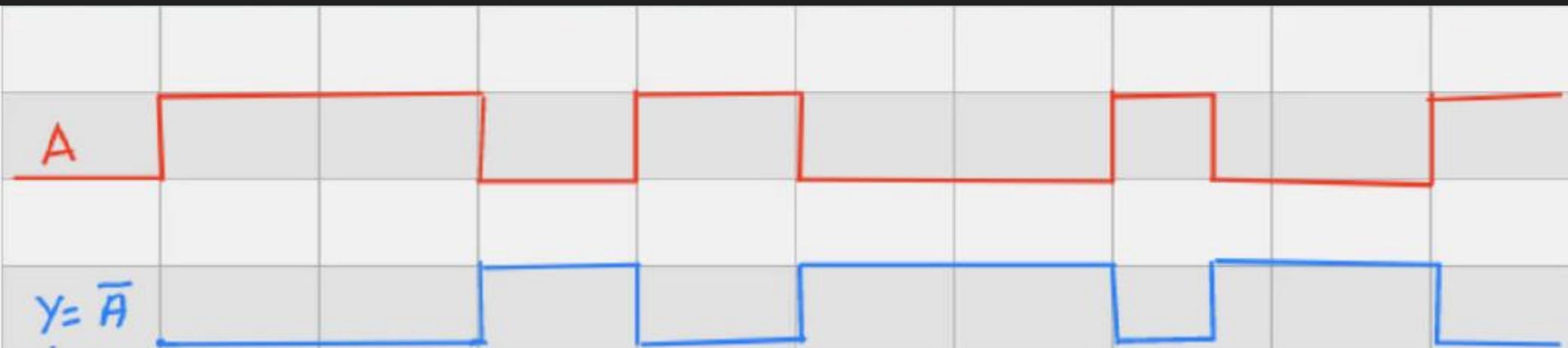
$$y = \bar{A}$$

## Switching circuit



A	Y
Off	on
On	off

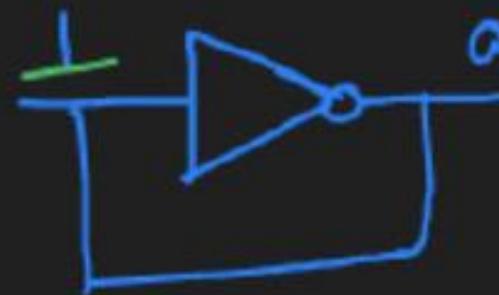
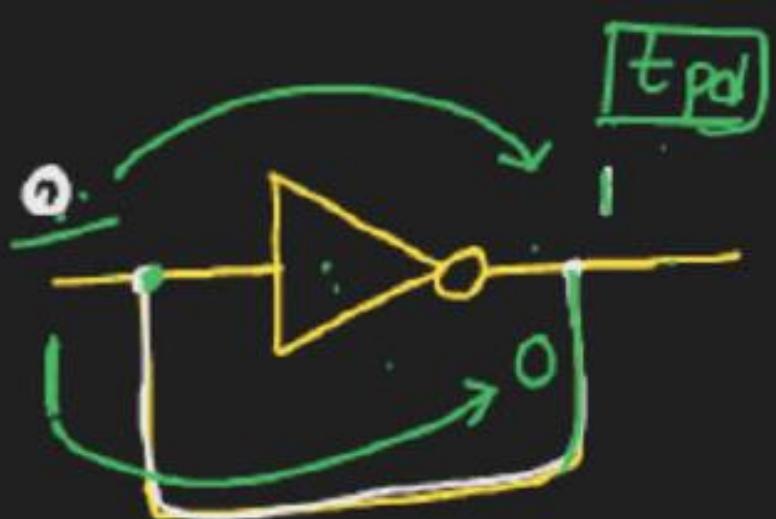
# Timing Diagram





→ Bistable multivibrator

→ Basic memory circuit



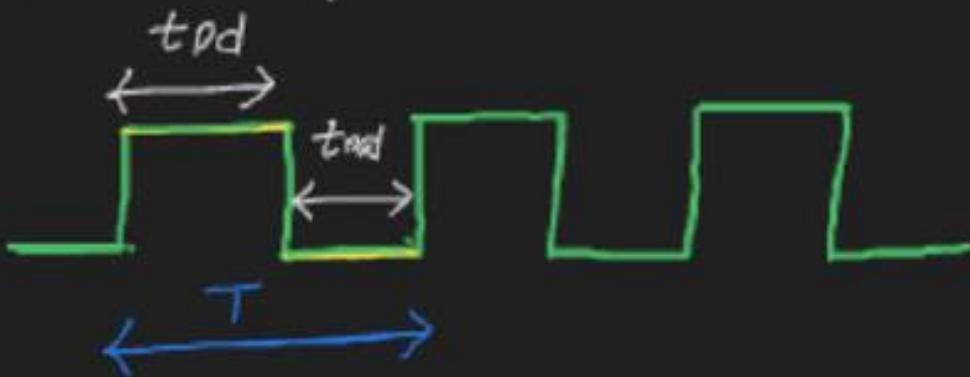
unstable

→ Astable multivibrator

→ Square wave generator

→ Clock generator

→ Ring oscillator

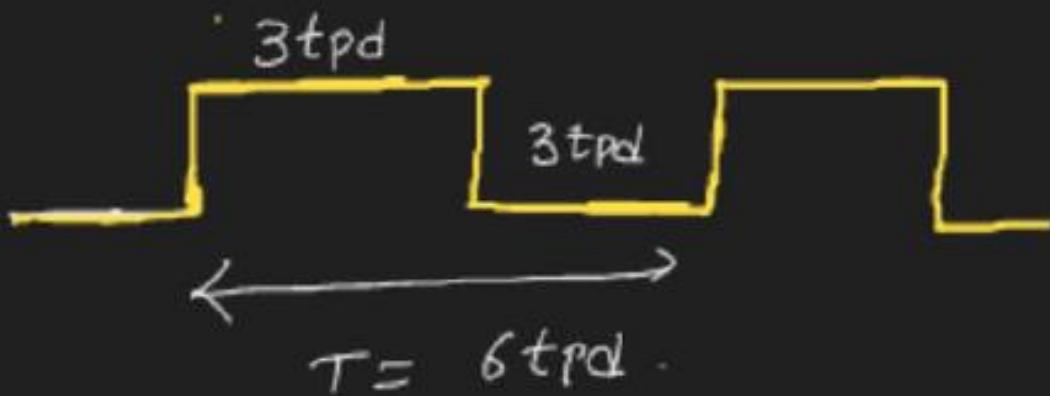
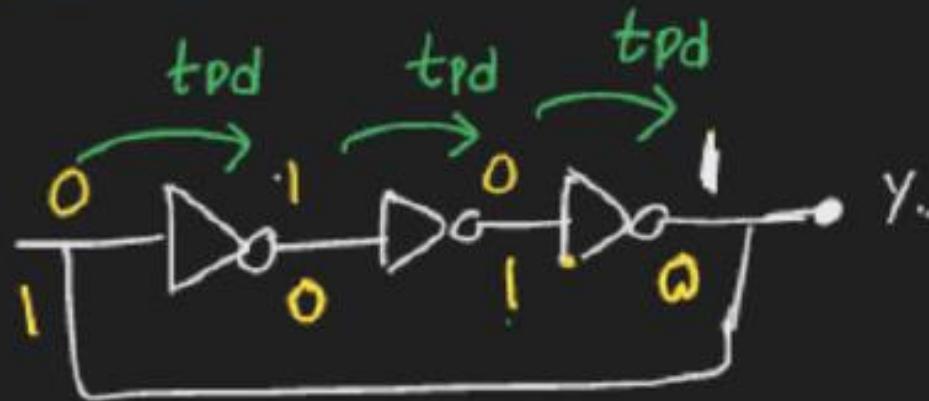


$$T = 2 \text{tpd}$$

tpd - Propagation delay.

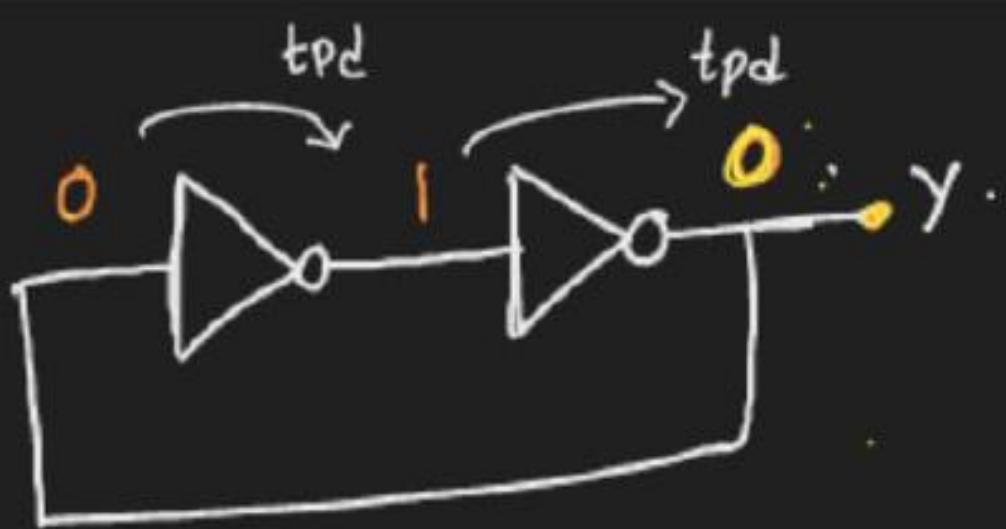
$$T = 2(1) \text{tpd}$$

→ for n- NOT Gate,  $T = 2n \text{ tpd}$ .



$$T = 2n \text{ tpd}.$$

$$f = \frac{1}{T} = \frac{1}{2n \text{ tpd}}.$$

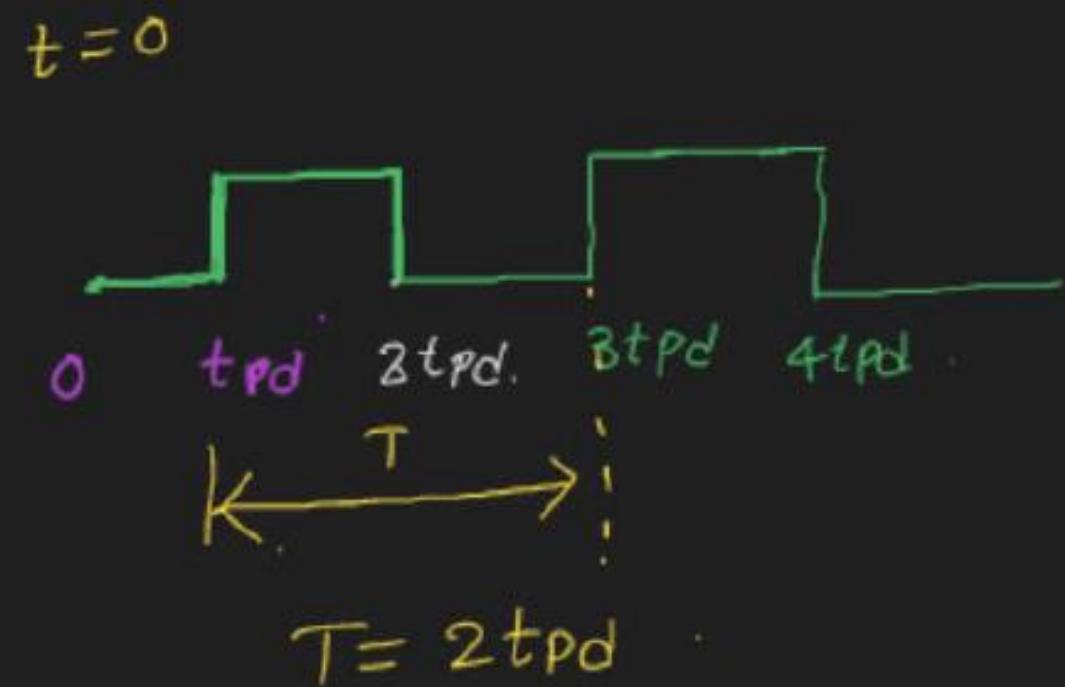
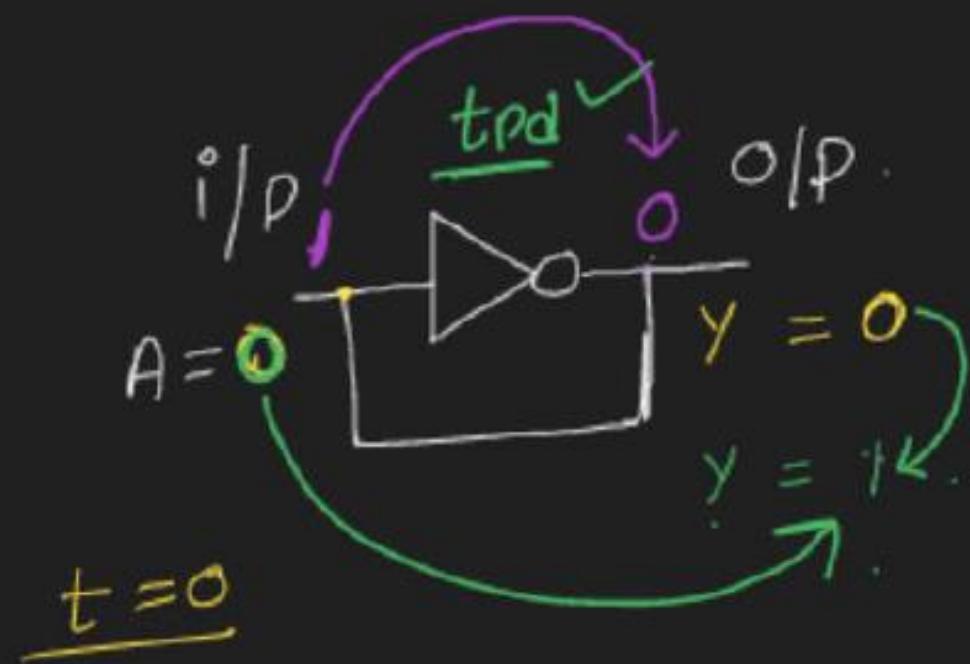


Bistable

$$\underline{f = 0}$$



DC

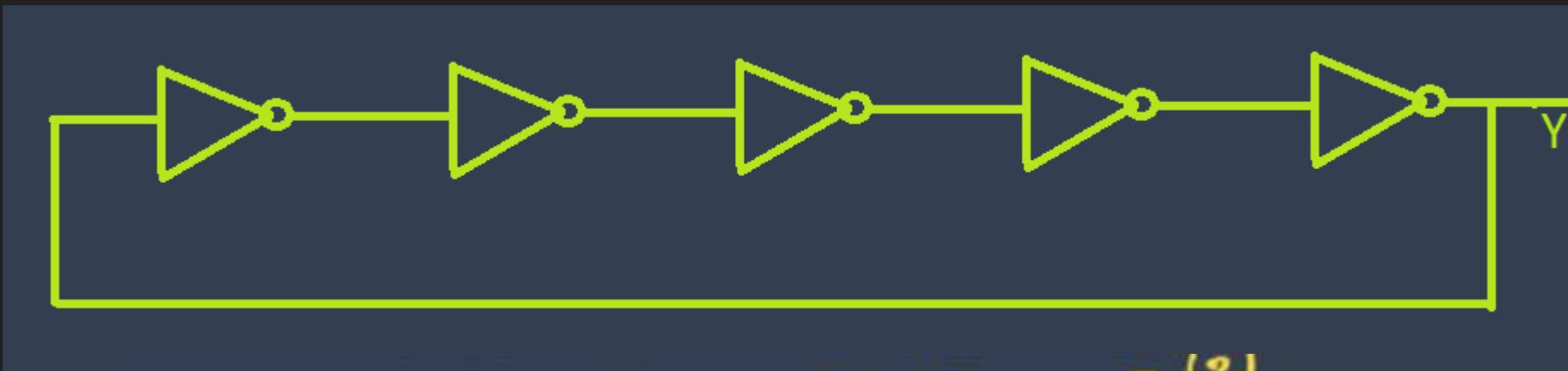


## NOTE:

1. If the number of inverters in the feedback path is even then ---->  
**BISTABLE MULTIVIBRATOR**
  
2. If the number of inverters in the feedback is odd then --->  
**ASTABLE MULTIVIBRATOR**



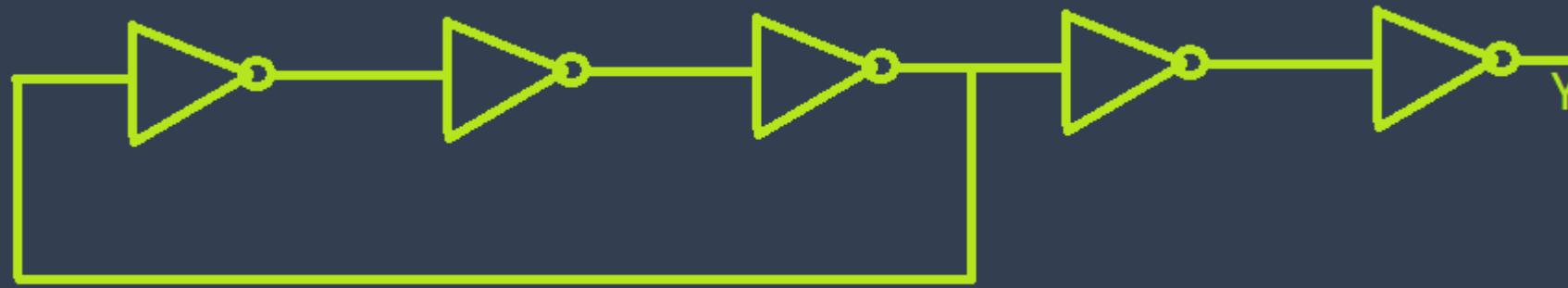
Q) The ring oscillator shown in fig , if the propagation delay of each NOT gate is 100 psec , then the frequency of generated square wave is



$$T = 2n \cdot t_{pd} = 2(5) (100 \times 10^{-12})$$

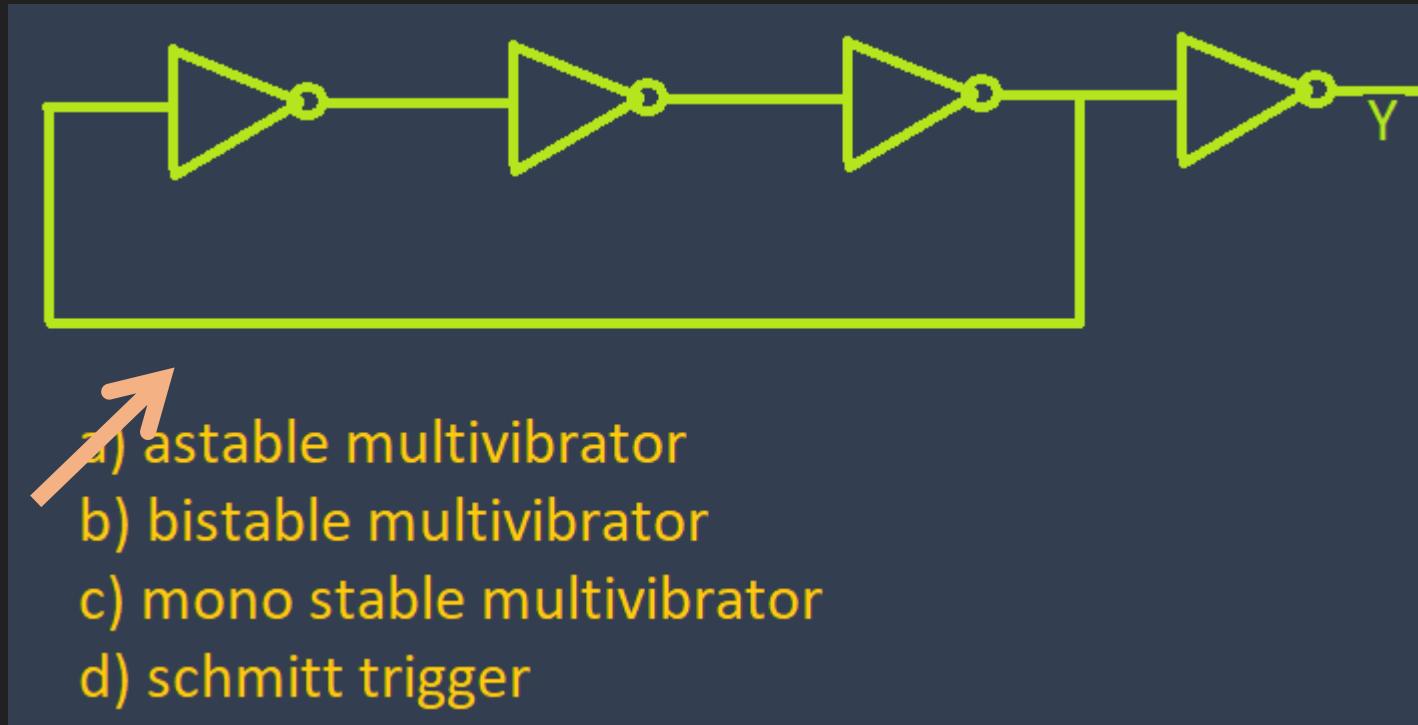
$$f = \frac{1}{10^3 \times 10^{-12}} = 1 \text{ GHz}$$

Q) The circuit shown in the figure acts as



- a) astable multivibrator ✓
- b) bistable multivibrator
- c) mono stable multivibrator
- d) schmitt trigger

Q) The circuit shown in the figure acts as



- a) astable multivibrator
- b) bistable multivibrator
- c) mono stable multivibrator
- d) schmitt trigger

# AND Gate

Symbol



$$Y = \sum m(3) = AB \rightarrow SOP$$

$$Y = \prod M(0, 1, 2)$$

$$Y = (A+B)(A+\overline{B})(\overline{A}+B) \rightarrow POS$$

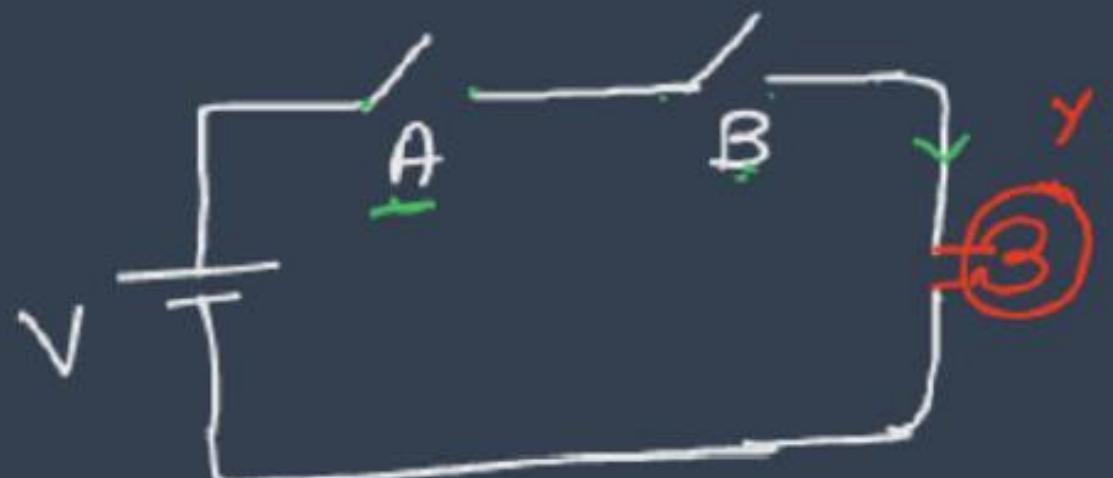
Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

If any one of the input is '0' then the output is '0'

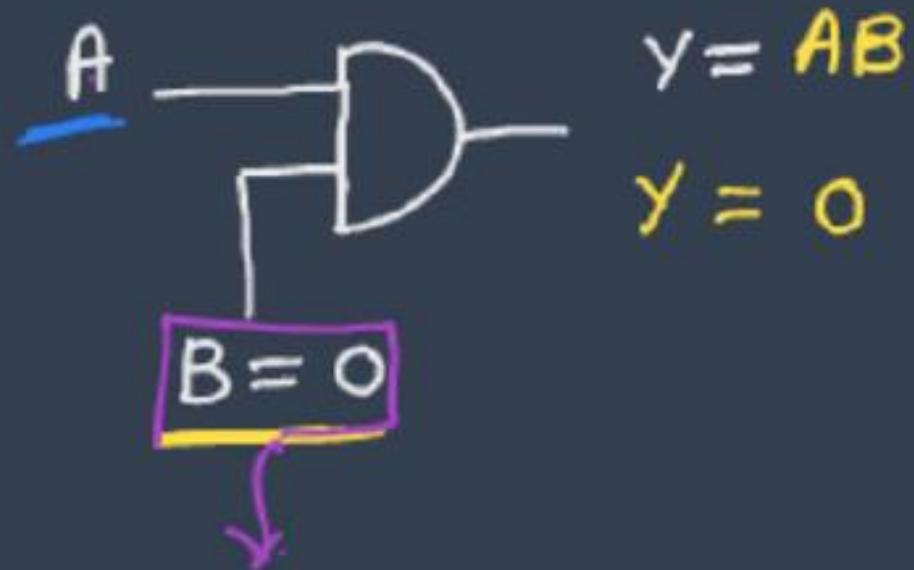
## Switching Circuit

$$Y = AB$$

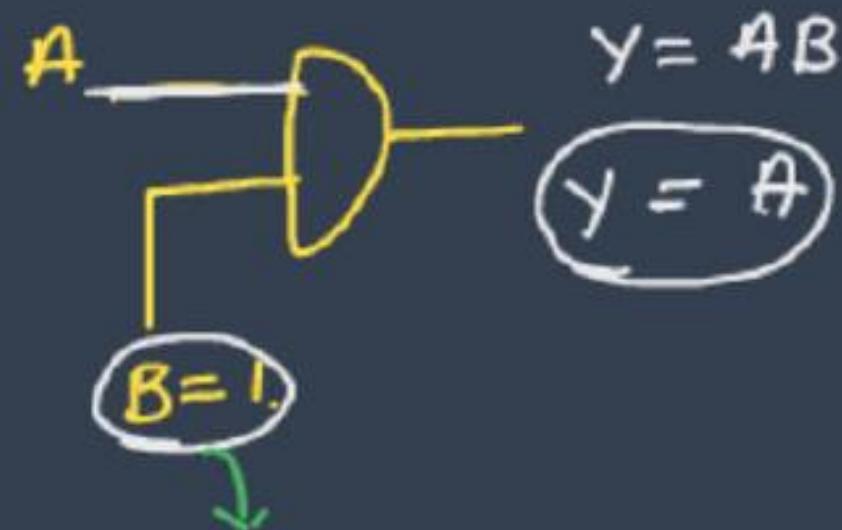


A	B	Y
Off	Off	off
Off	On	off
On	Off	off
On	On	on

## Enable input and Disable input



Disable i/p



Enable i/p

Commutative Law

$$AB = BA$$

A  
B

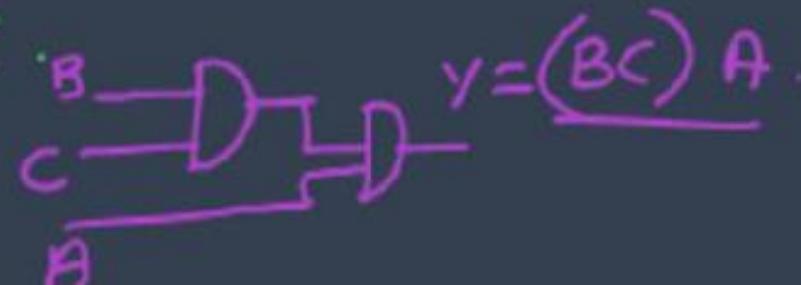
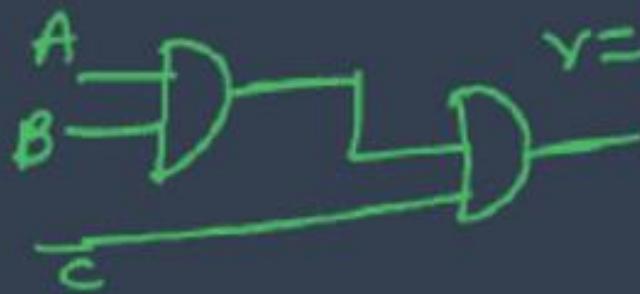


$$\boxed{AB = BA}$$

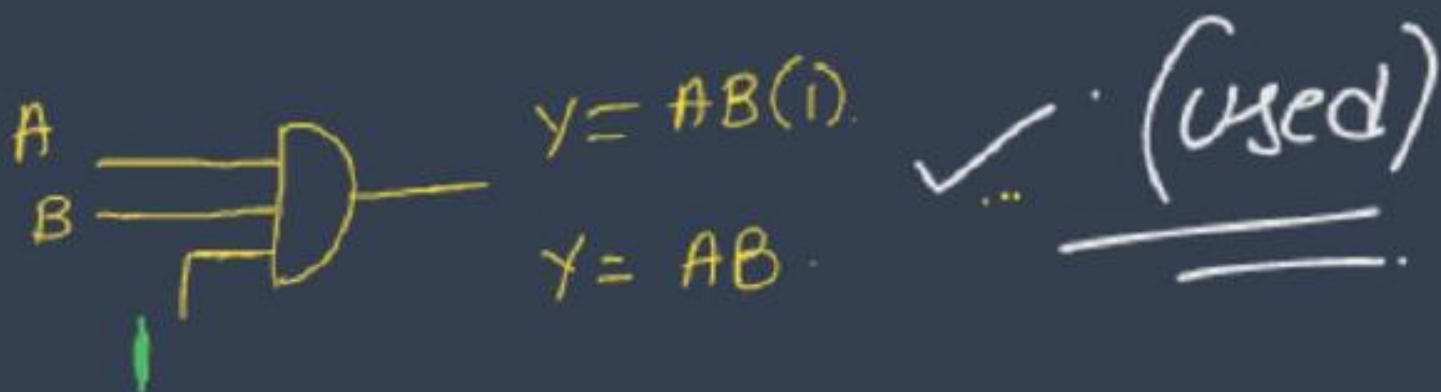
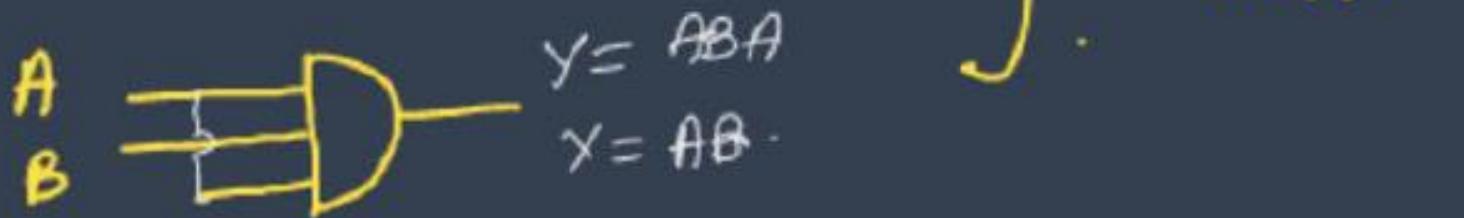
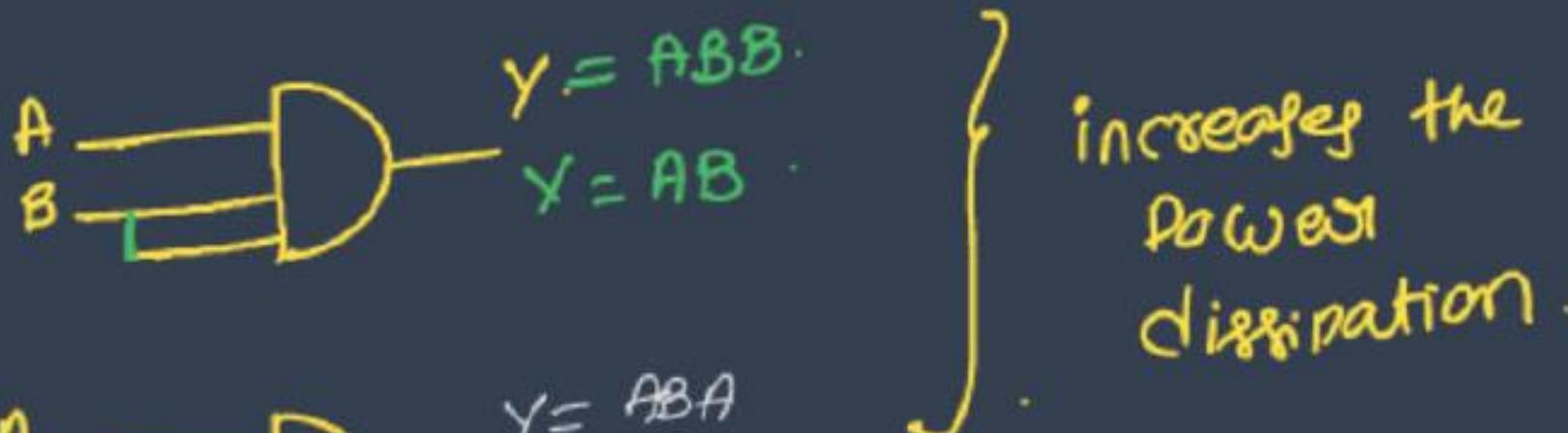
Associative Law

$$ABC = (AB)C = (AC)B = (BC)A \quad \checkmark$$

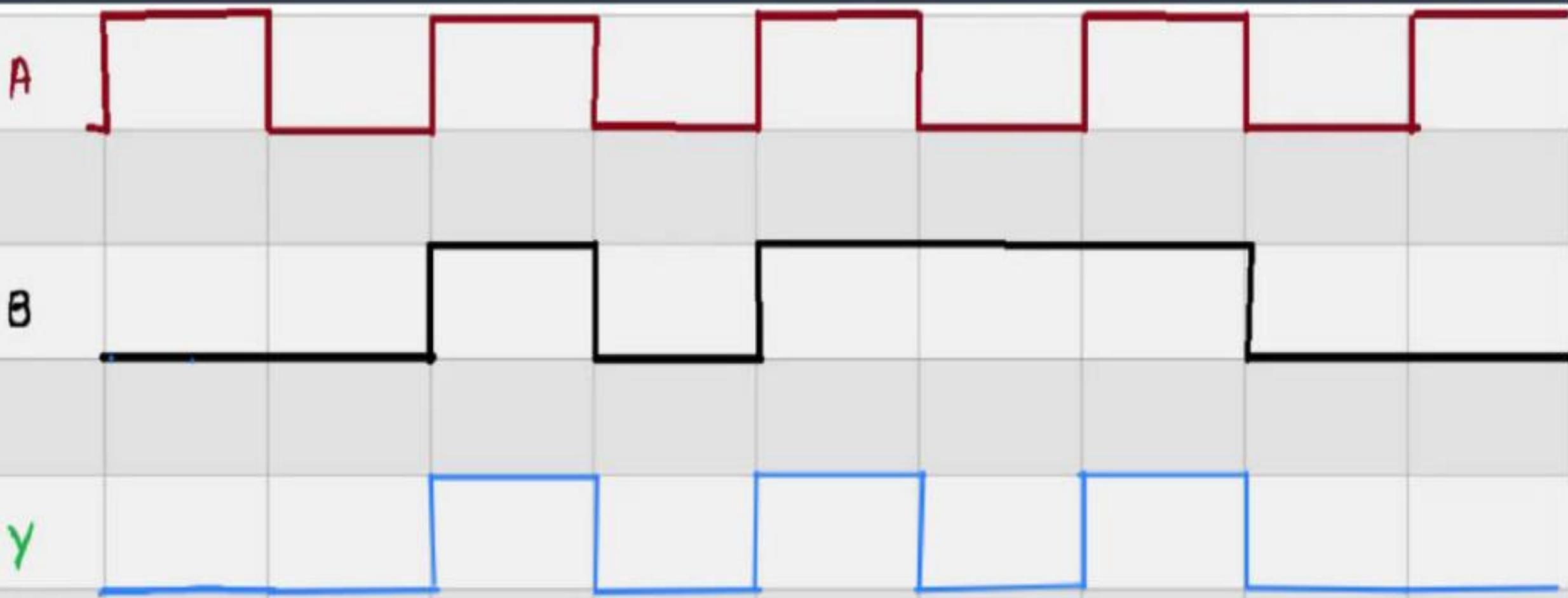
A  
B  
C



## Unused input in AND Gate



# Timing Diagram



# OR Gate

Symbol


$$y = A + B$$
$$y = \Sigma m(1, 2, 3)$$
$$y = \overline{A}B + A\overline{B} + AB$$
$$y = \text{TM}(0)$$
$$y = (A + B)$$

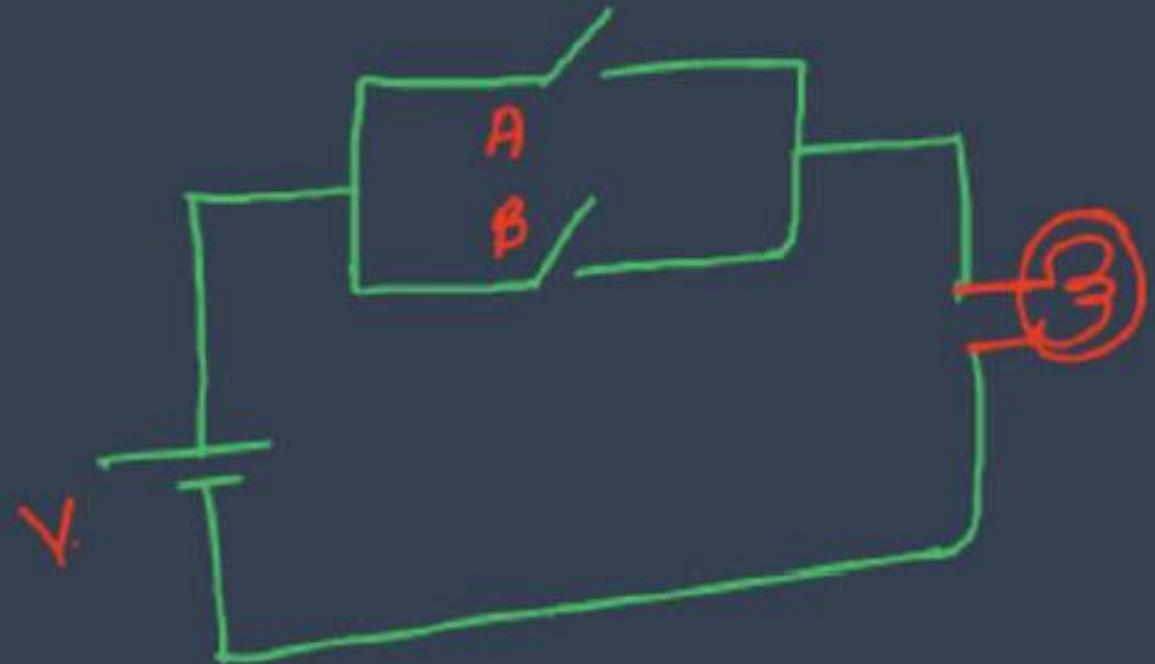
Truth table

A	B	y
0	0	0
0	1	1
1	0	1
1	1	1

If any one of the input is '1' then the output is '1'

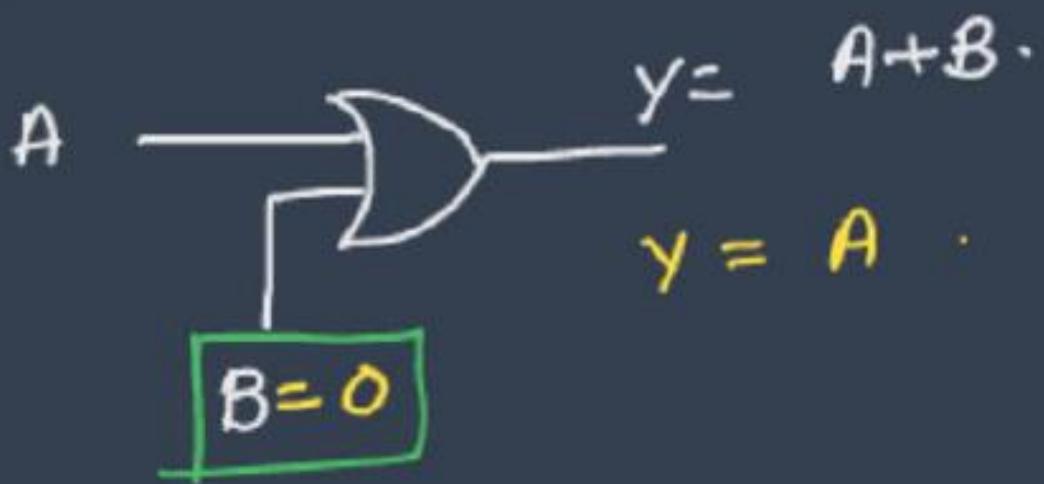
## Switching Circuit

$$y = A + B$$

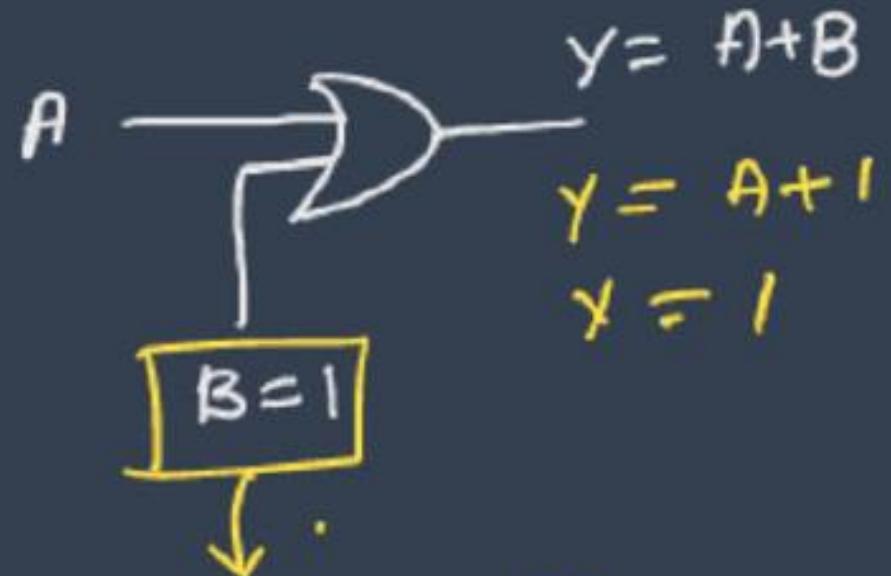


A	B	Y
Off	Off	off.
Off	On	on.
On	Off	on.
On	On	on.

## Enable input and Disable input



Enable IP



Disable IP

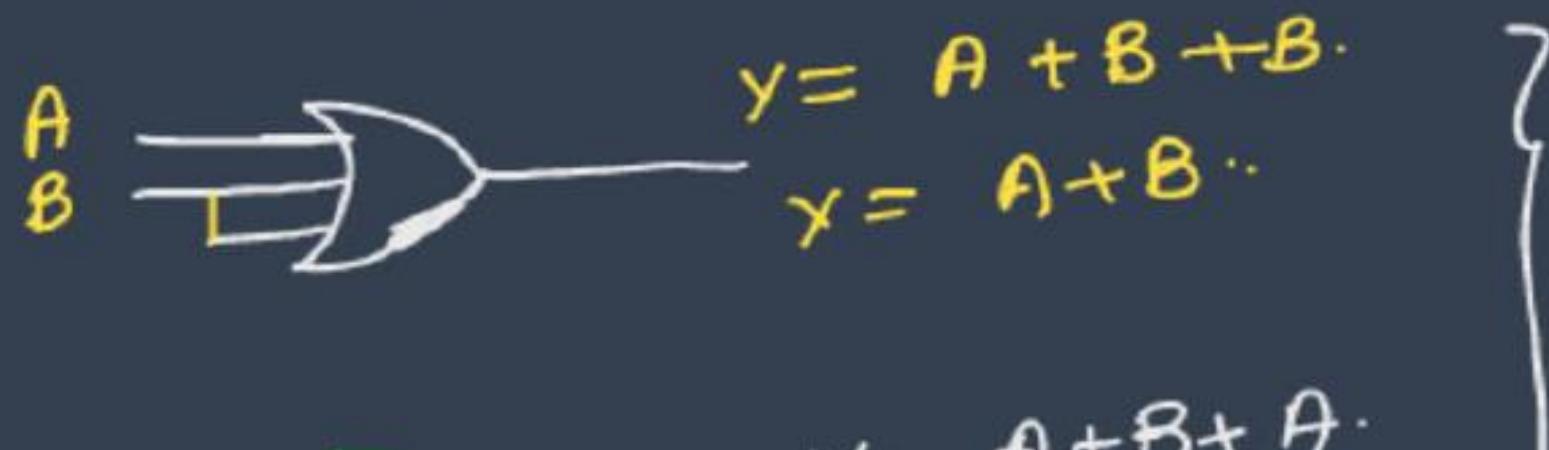
Commutative Law

$$y = A + B = B + A \quad \checkmark$$

Associative Law

$$y = A + B + C = (A + B) + C = A + (B + C) \quad \checkmark$$

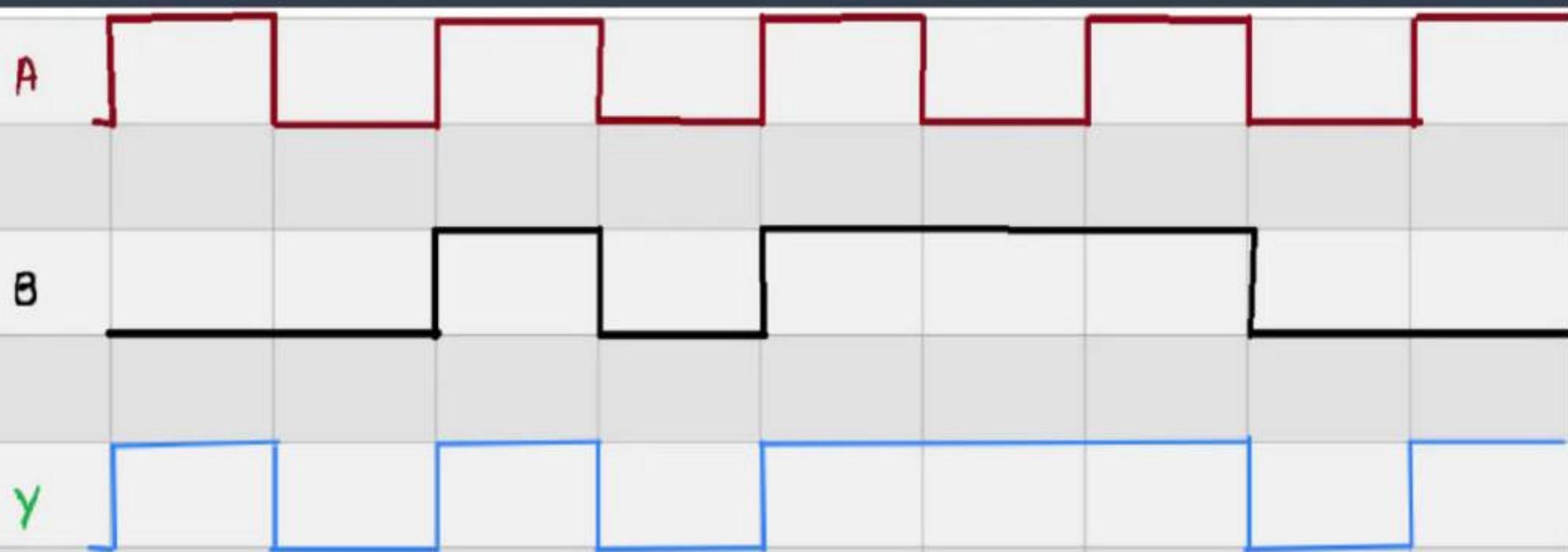
## Unused input in OR Gate



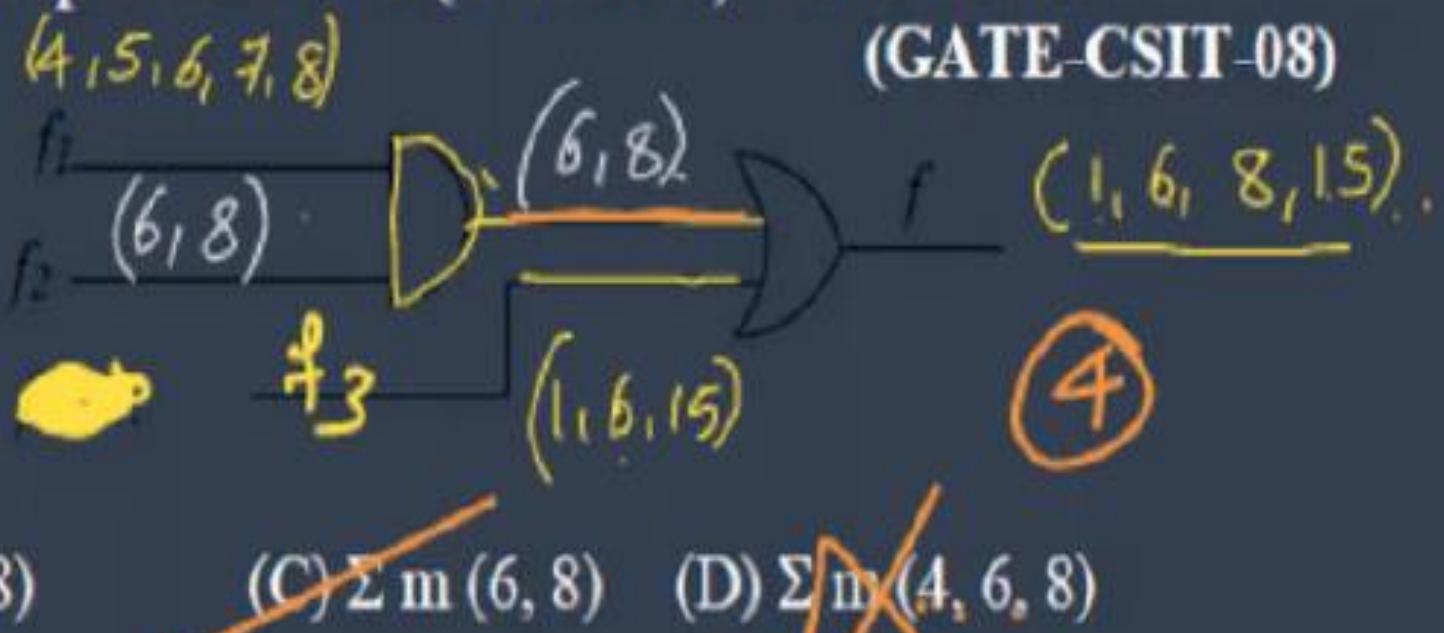
increasing  
the power  
dissipation .



## Timing Diagram



Given  $f_1$ ,  $f_2$ , and  $f$  in canonical sum of products form (in decimal) for the circuit.



The product – of – sum expression for given truth table is: (IES-1992)

X	Y	Z
0	0	1
0	1	0
1	0	1
1	1	0

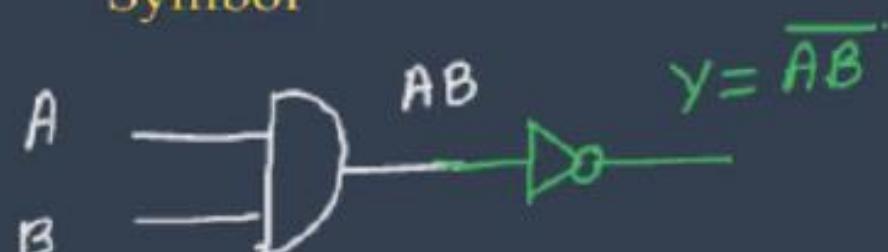
pos

$$Z = (x + \bar{y})(\bar{x} + \bar{y})$$

- (a)  $(\bar{X} + \bar{Y})(X + Y)$
- (b)  $(X + \bar{Y})(\bar{X} + \bar{Y})$  ✓
- (c)  $(X + \bar{Y})(\bar{X} + \bar{Y})$  ✓
- (d) None of the above

# NAND Gate (AND + NOT)

Symbol



$$y = \overline{\Sigma m(0, 1, 2)}$$
$$y = \overline{A}\overline{B} + \overline{A}B + A\overline{B}$$
$$y = \overline{\prod M(3)}$$
$$y = (\overline{A} + \overline{B})$$

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

If any one of the input is '0' then the output is '1'

Switching Circuit

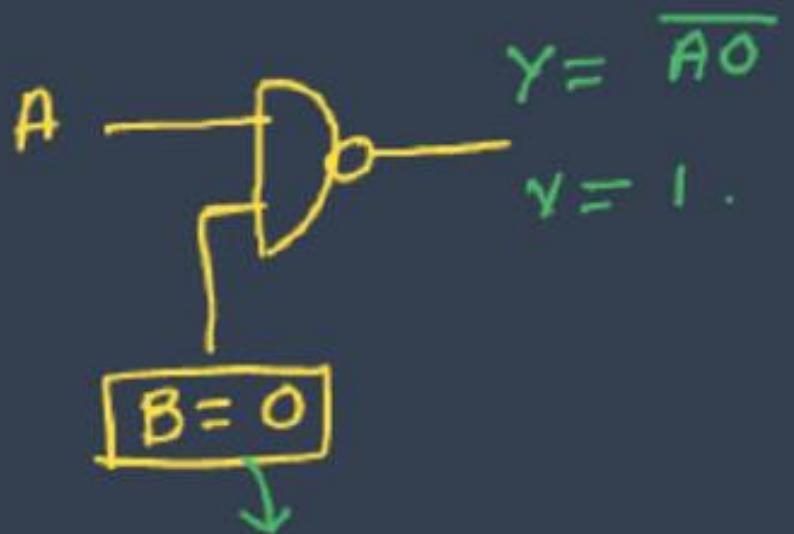
$$y = \overline{AB} = \overline{x}$$

$$x = AB$$

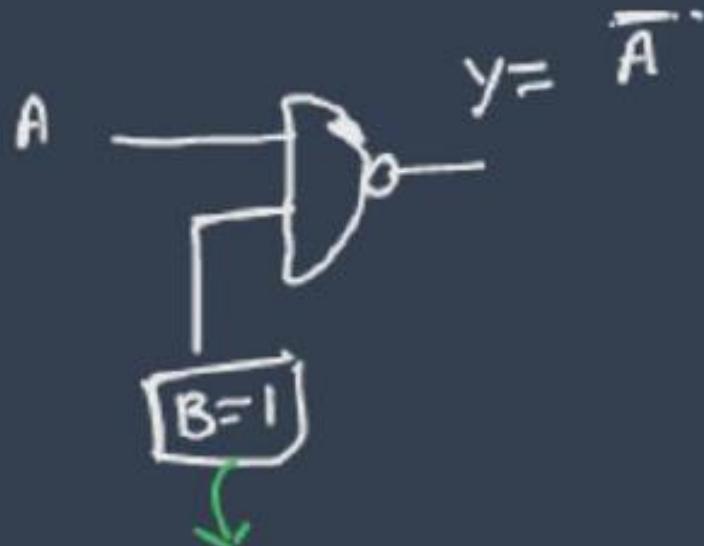


A	B	y
Off	Off	on
Off	On	on
On	Off	on
On	On	off

## Enable input and Disable input



disable input.



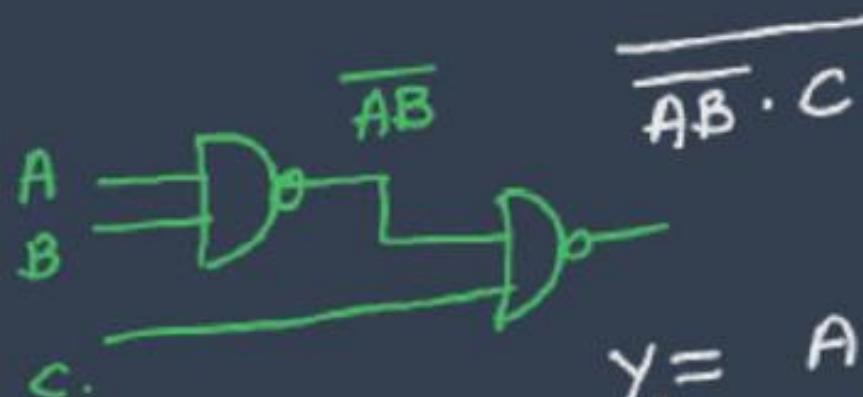
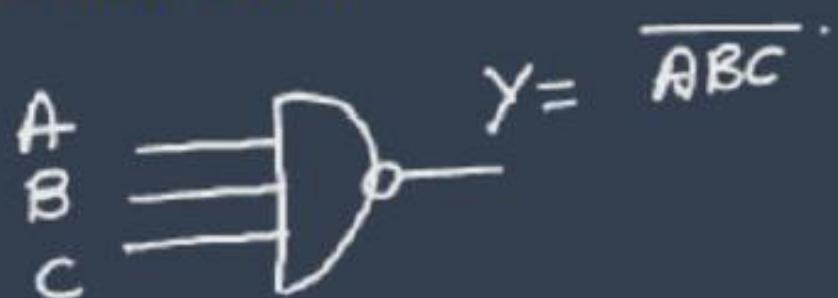
Enable input.

## Commutative Law



$$\overline{AB} = \overline{BA}$$

## Associative Law



$$Y = \overline{A} + \overline{B} + \overline{C}$$

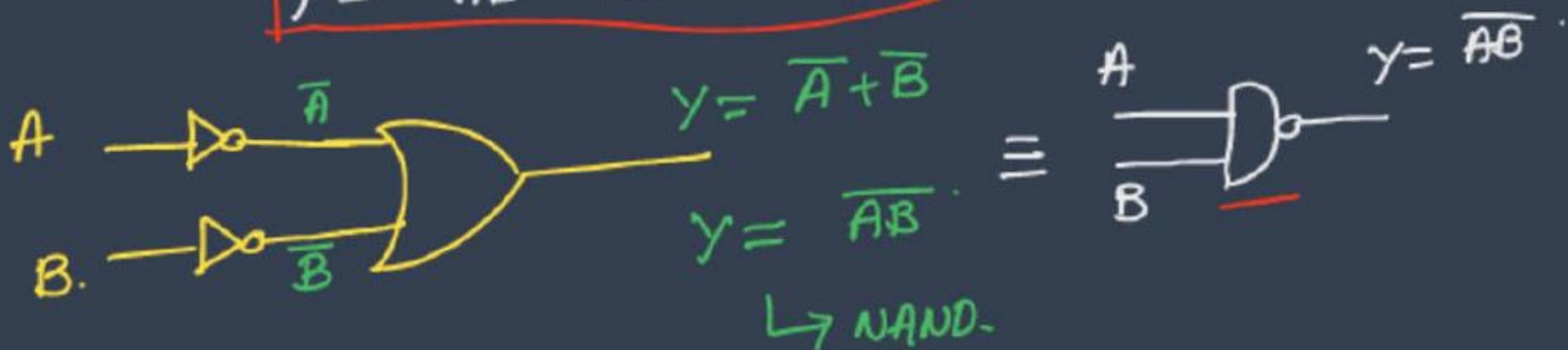
$$\overline{ABC} \neq \overline{(\overline{AB})C}$$

Not satisfying  
Associative law

## Alternative Logic

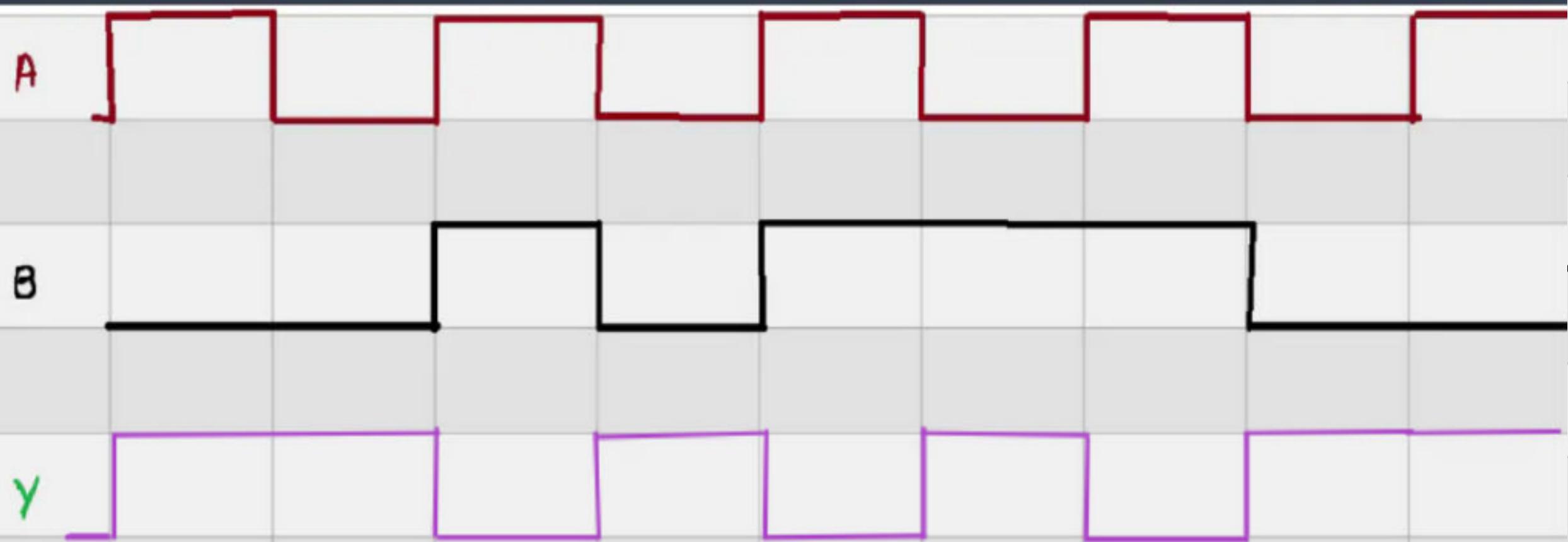
$$\overline{AB} = \overline{A} + \overline{B}$$

$$Y = \overline{AB} = \overline{A} + \overline{B}$$



NAND Gate  $\equiv$  Bubbled OR-Gate

## Timing Diagram



# NOR Gate (OR + NOT)



$$y = \sum m(0) = \overline{A}\overline{B}$$

$$Y = \pi M(1, 2, 3)$$

$$Y = (\overline{A} \cdot B)(A \cdot \overline{B})(\overline{A} \cdot \overline{B})$$

Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If any one of the input is '1' then the output is '0'

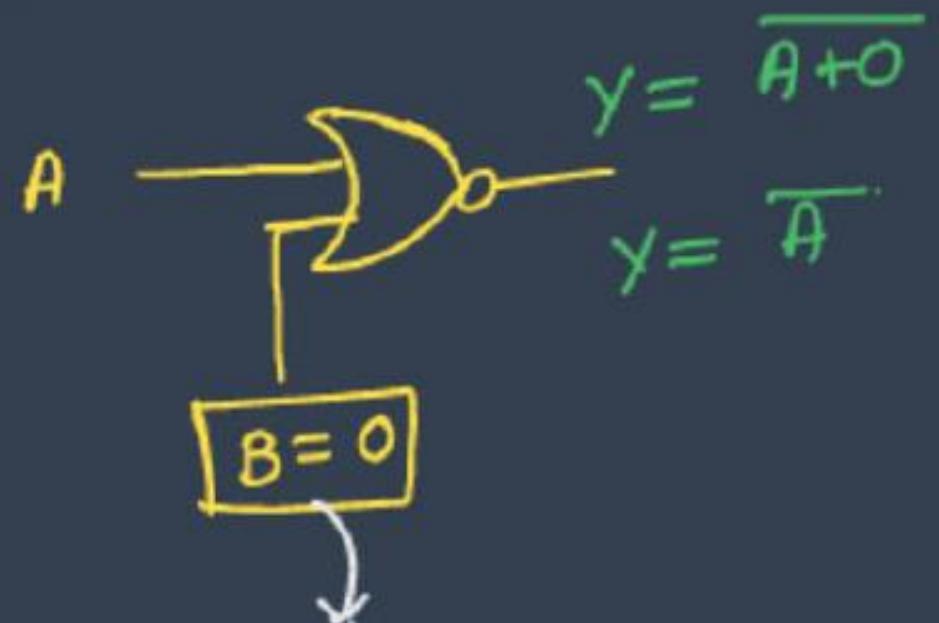
## Switching Circuit

$$Y = \overline{A+B}$$

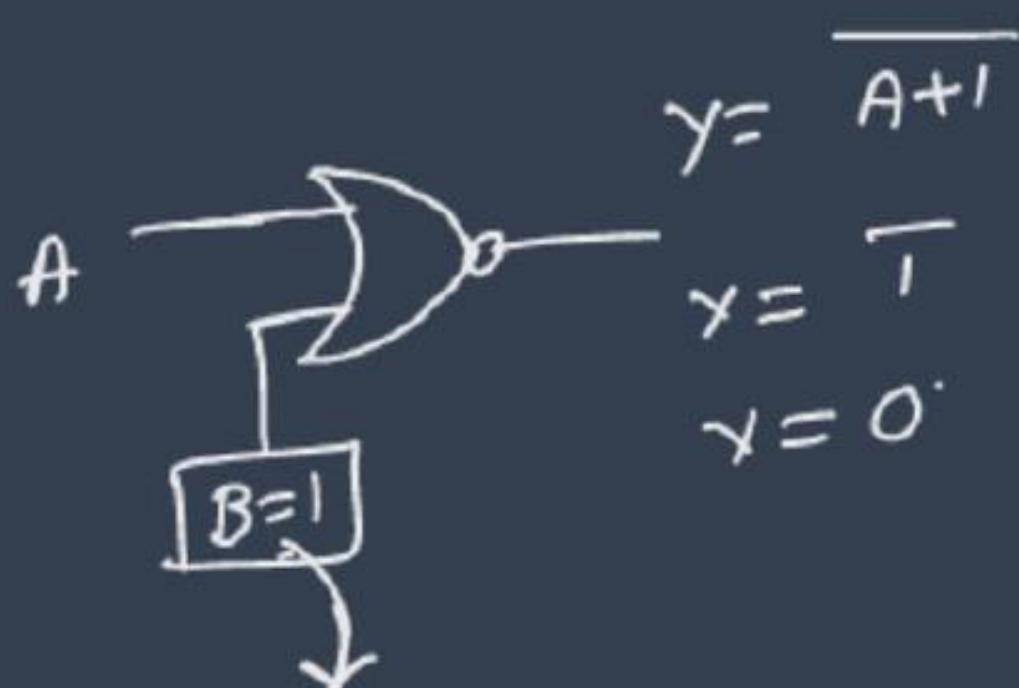


A	B	Y
Off	Off	on
Off	On	off
On	Off	off
On	On	off

## Enable input and Disable input



Enable i/p



Disable i/p  
=

## Commutative Law

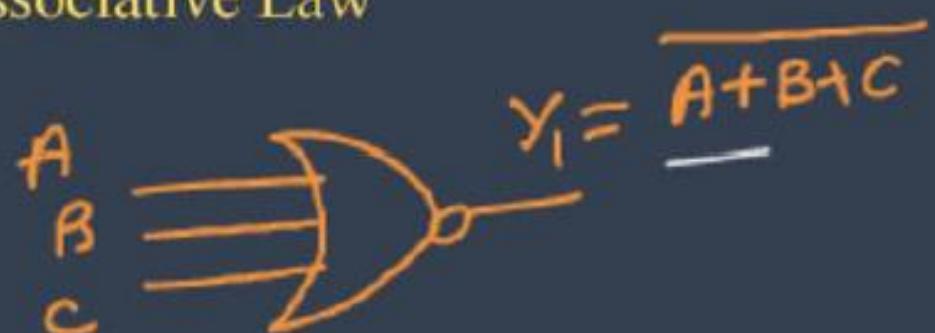
$$\overline{A+B} = \overline{B+A}$$

✓

$$A+B+C = \overline{\overline{(A+B)}+C} = A+(B+C)$$

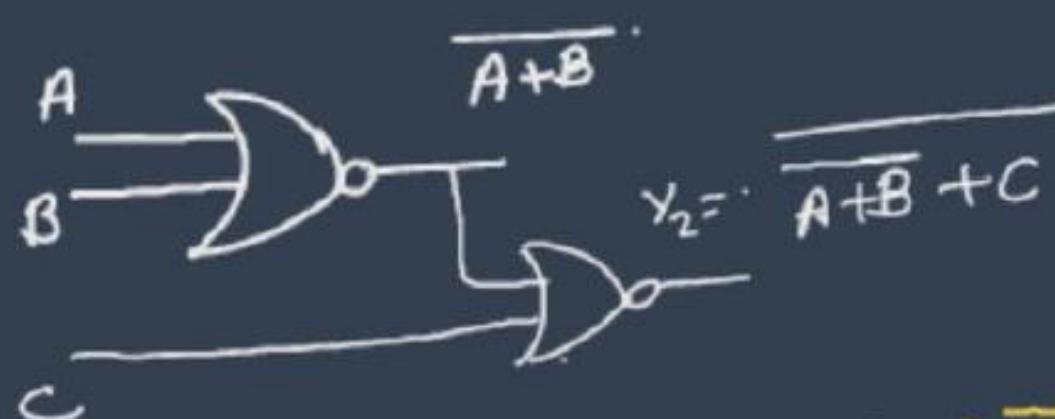
$$\overline{A+B+C} \neq \overline{\overline{(A+B)}+C}$$

## Associative Law



$$Y_1 = \overline{A}\overline{B}\overline{C}$$

$\boxed{Y_1 \neq Y_2}$

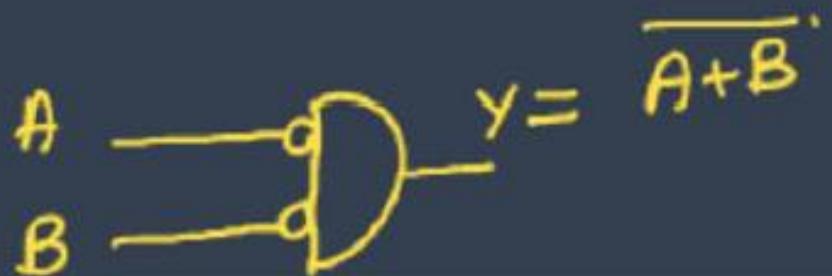


$$Y_2 = (A+B)\overline{C}$$

Not satisfy associative law.

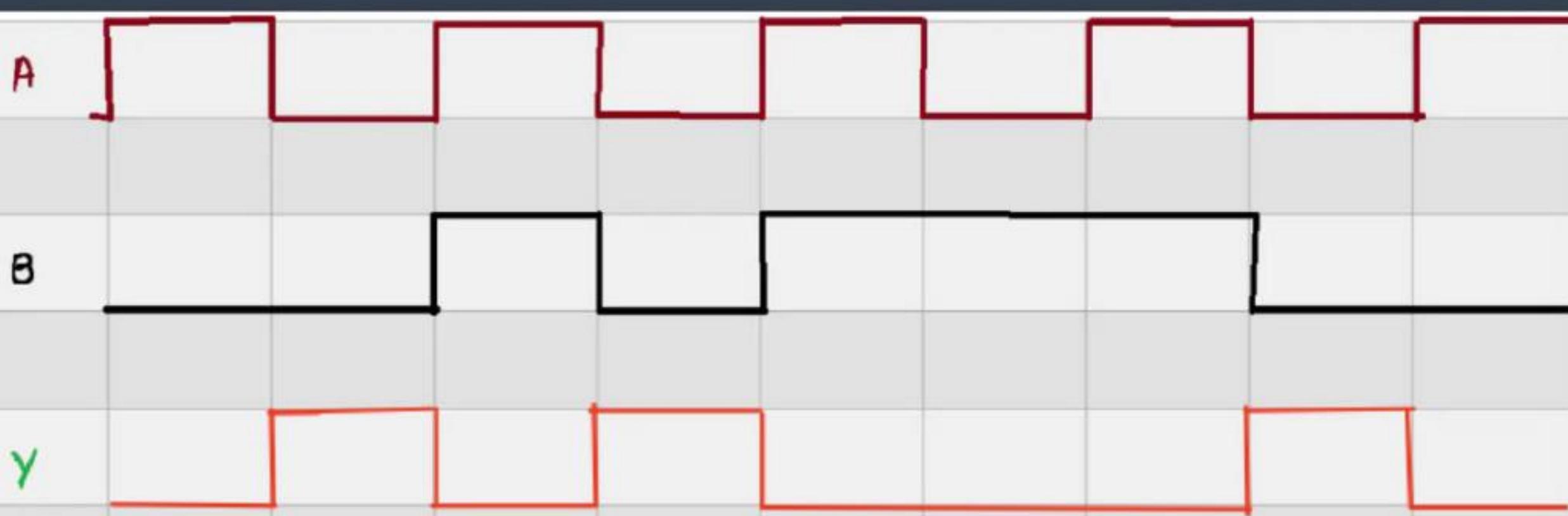
## Alternative Logic

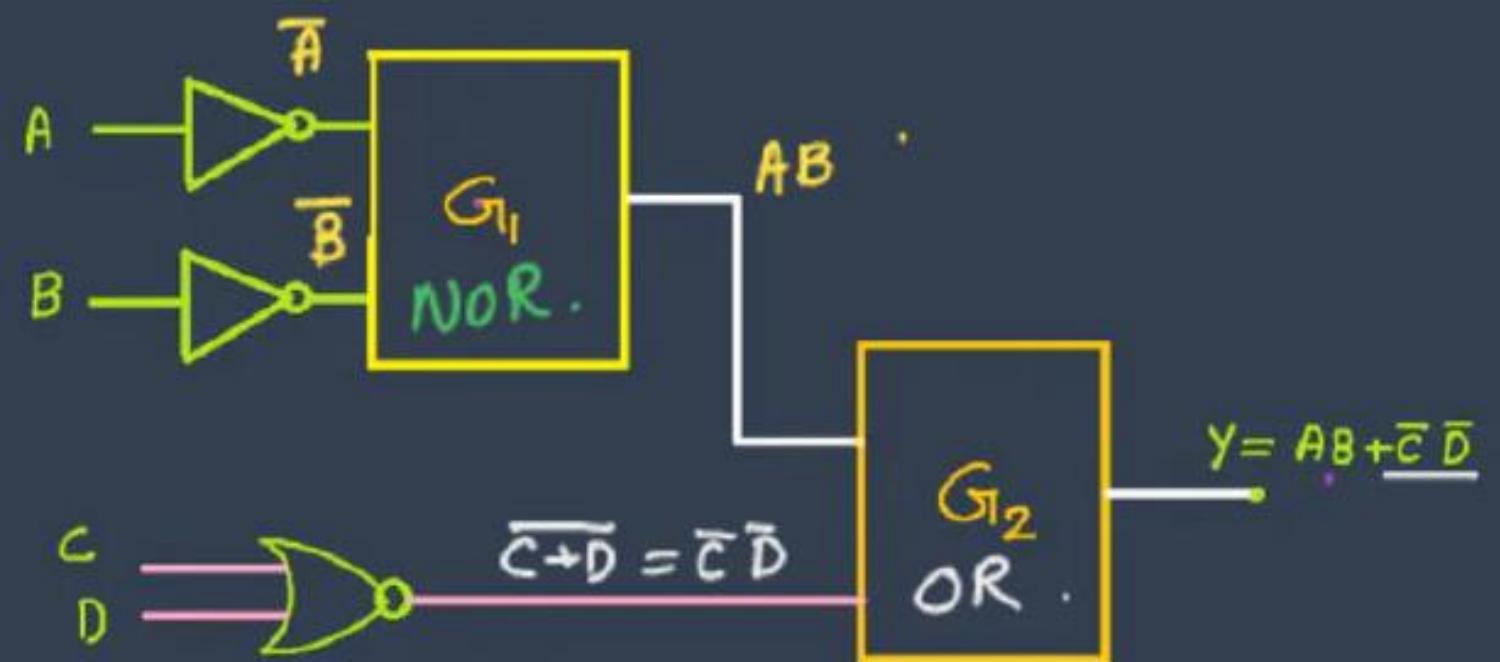
$$y = \overline{A+B} = \overline{A} \cdot \overline{B}$$



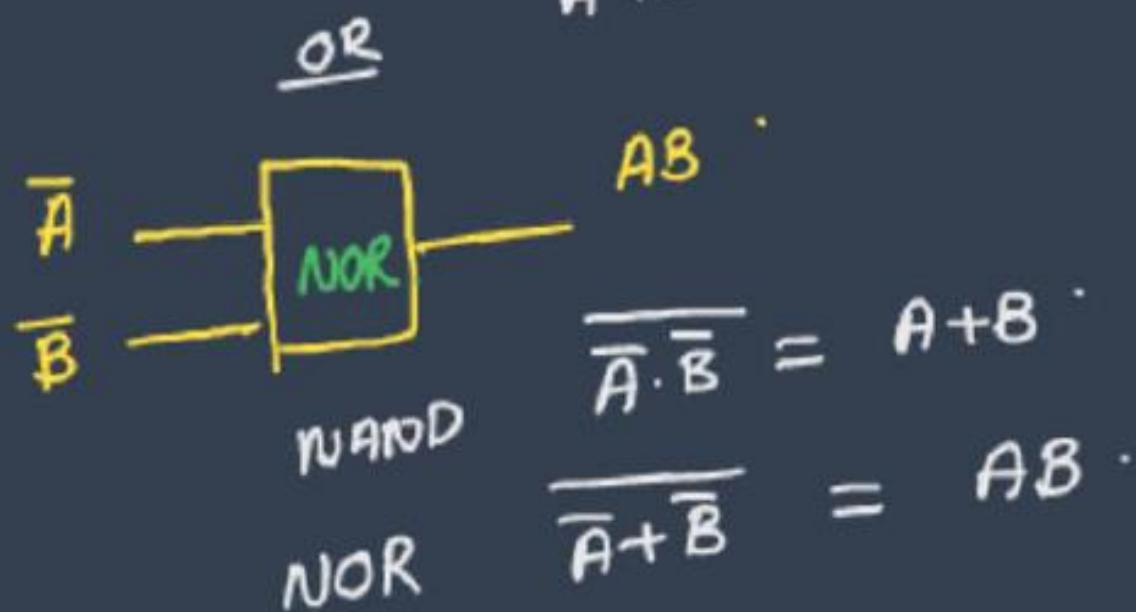
NOR Gate  $\equiv$  Bubbled AND Gate

## Timing Diagram

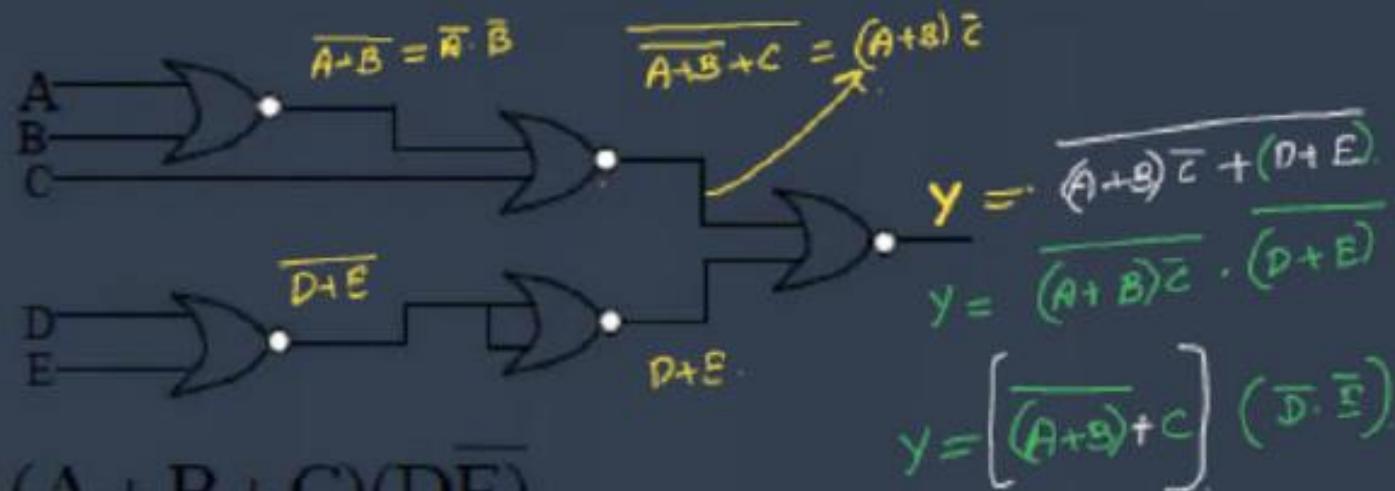




then gates  $G_1$  &  $G_2$  are



The circuit shown in figure realizes the function:



- (a)  $(A+B+C)(D\bar{E})$
- (b)  $(A+(\overline{B}+\overline{C})(\overline{D}\bar{E})$
- (c)  $(A+B+C)(\overline{D}\bar{E})$
- (d)  $(\overline{A+B}+C)(\overline{D}\bar{E}) \checkmark$

Q) The binary operator # is defined as  $X \# Y = \bar{X} + \bar{Y}$ , then which of the following is true

$$S_1 : P \# Q \# R = P \# (Q \# R) \quad \cancel{\times}.$$

$$S_2 : \underline{Q \# R} = R \# Q \quad \checkmark$$

$$\begin{array}{r} \overline{xy} \\ \underline{=} \end{array}$$

NAND satisfy only commutative law.

S<sub>2</sub> - true

# EX-OR Gate

Symbol



$$Y = A \oplus B$$

$$Y = \sum m(1, 2)$$

$$Y = \overline{A}B + A\overline{B}$$

$$Y = \pi M(0, 3)$$

$$Y = (A+B)(\overline{A}+\overline{B})$$

Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

If odd number of one's present , then the output is 1

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$y(A, B, C) = \sum m(1, 2, 4, 7).$$

$$y(A, B, C, D) = \sum m(1, 2, 4, 7, 8, 11, 13, 14)$$

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

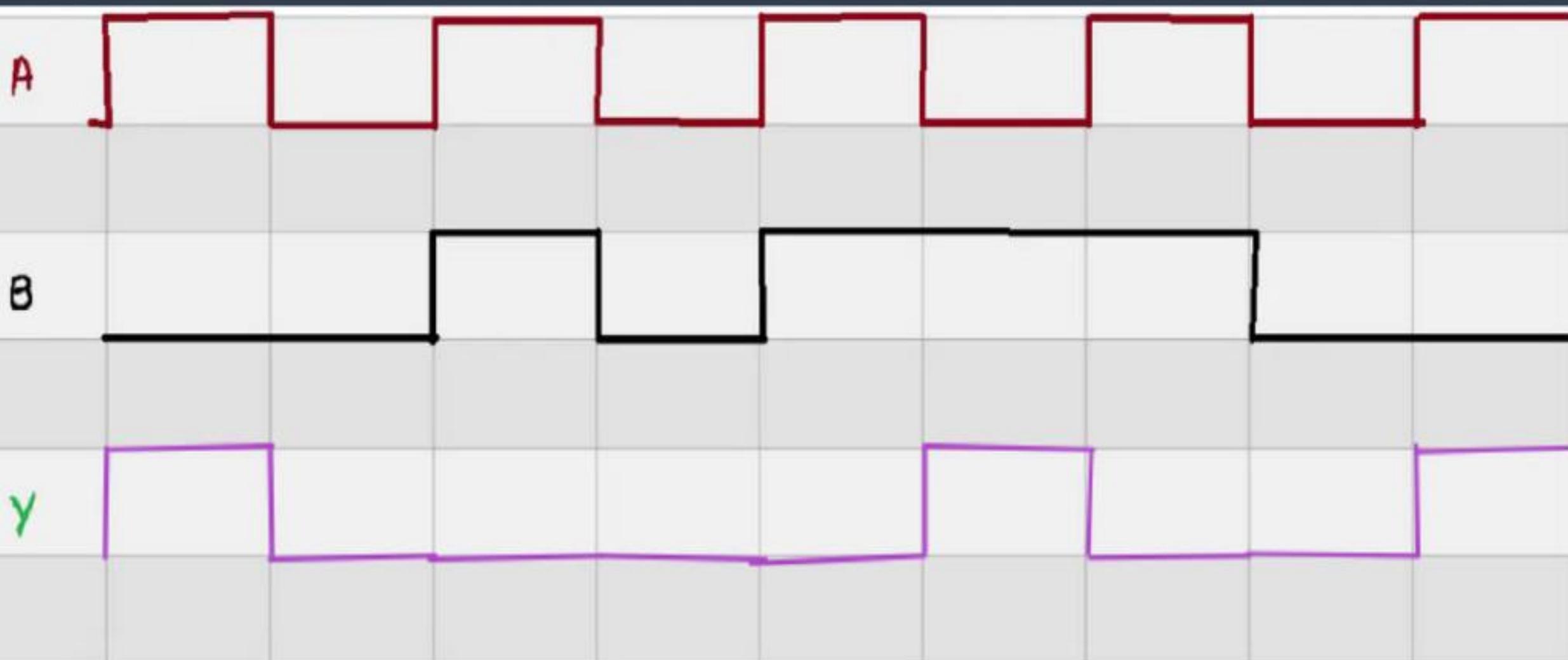
Switching Circuit

$$y = \bar{A}B + A\bar{B} = (\underline{\bar{A} + B})(\underline{\bar{A} + \bar{B}}) = (\bar{A} + B)(\bar{A}\bar{B})$$

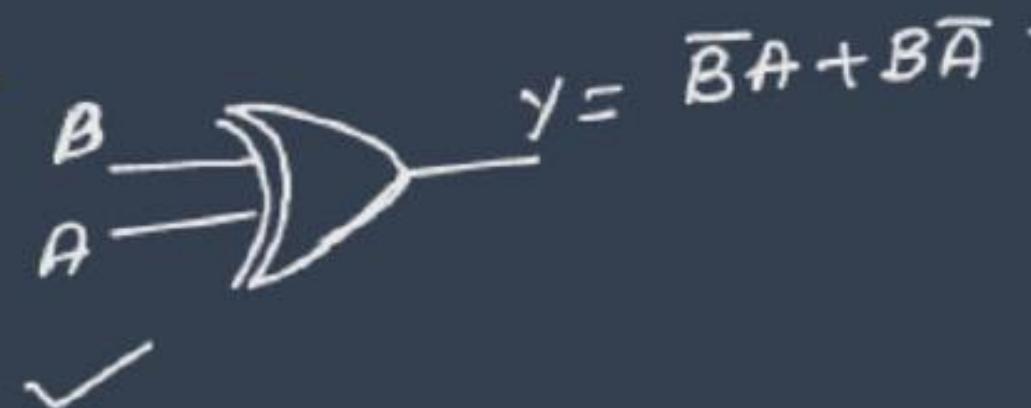
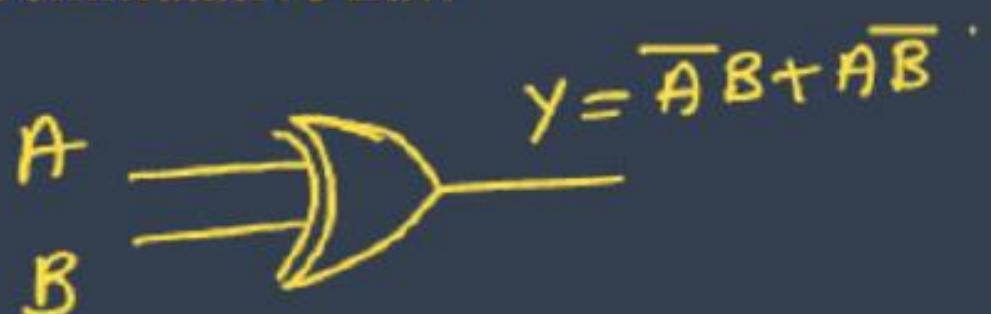


A	B	Y
Off	Off	off
Off	On	on
On	Off	on
On	On	off

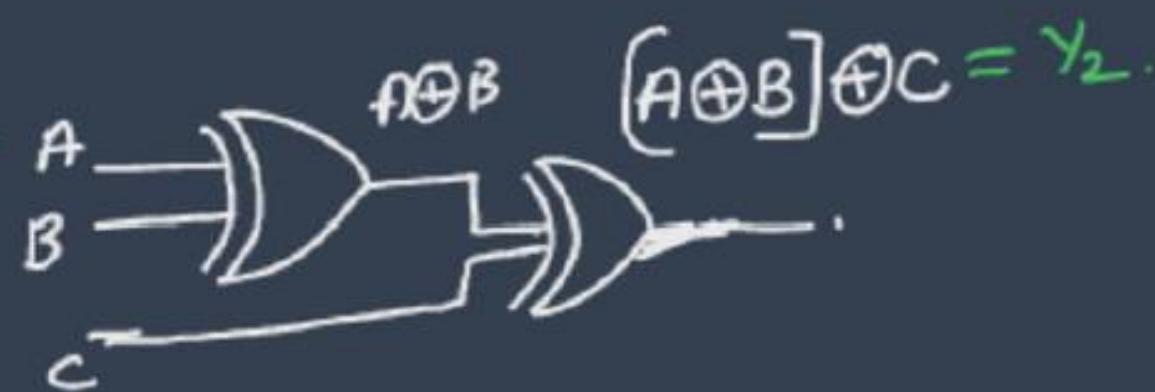
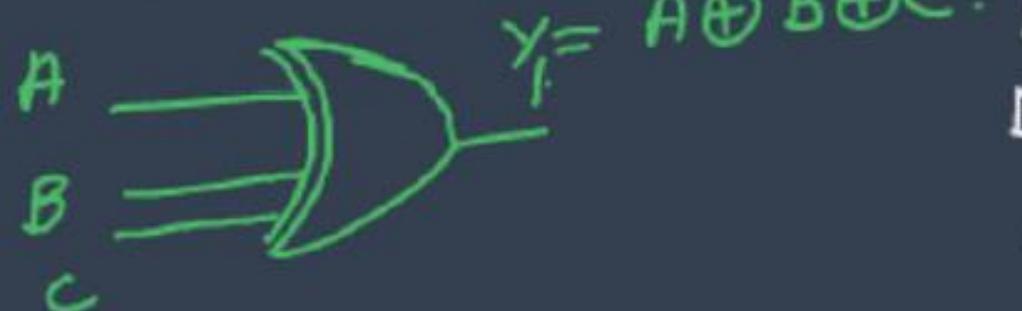
## Timing Diagram



### Commutative Law



### Associative Law

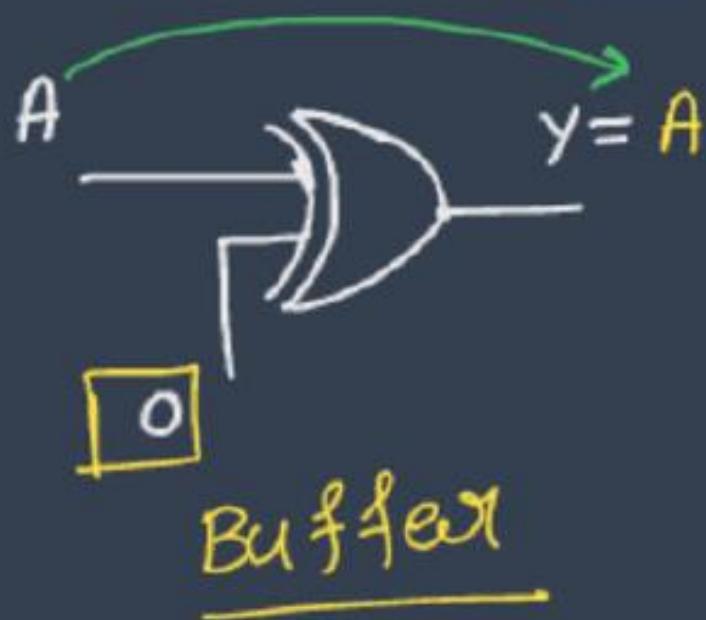


Satisfies Associative law

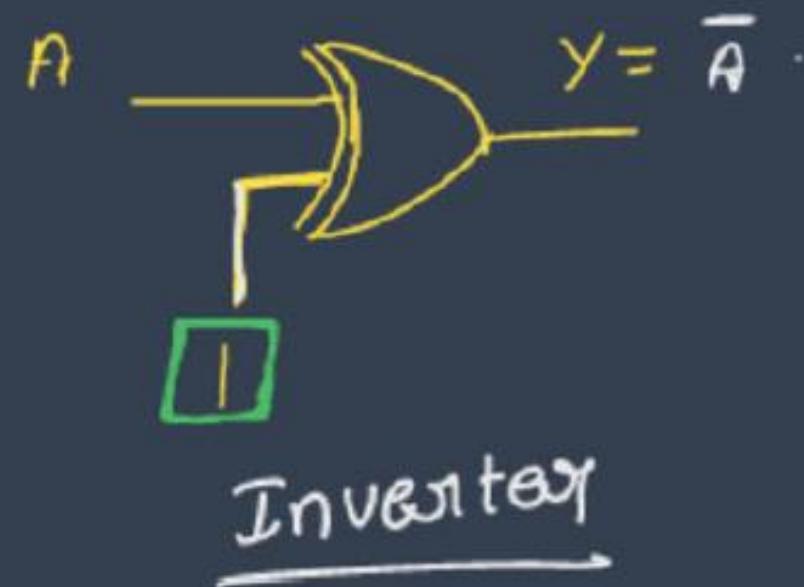
$$\begin{aligned}
 \text{y}_1 &= A \oplus B \oplus C = \sum m(1, 2, 4, 7) \\
 \text{y}_2 &= (A \oplus B) \oplus C = (\underline{A \oplus B}) \bar{C} + \overline{(A \oplus B)} C \\
 &= (\underline{A \bar{B} + \bar{A}B}) \bar{C} + [\underline{\bar{A}\bar{B} + \bar{A}B}] C \\
 &= A\bar{B}\bar{C} + \bar{A}B\bar{C} + (\bar{A} + B)(A + \bar{B})C \\
 &= A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC \\
 &\quad | \qquad \qquad \qquad 001 \qquad 111
 \end{aligned}$$

$$\text{y}_2 = \sum m(1, 2, 4, 7)$$

## EX- OR Gate as Buffer



## EX- OR Gate as Inverter



# Properties of EX- OR Gate

$$1. A \oplus 0 = A$$

$$2. A \oplus 1 = \bar{A}$$

$$3. A \oplus A = 0$$

$$4. A \oplus \bar{A} = 1$$

$$5. A \oplus A \oplus A \oplus A \dots \dots \dots n \text{ times} = \begin{cases} A, & n - \text{odd} \\ 0, & n - \text{even} \end{cases}$$

$$6. A \oplus \bar{A}B = A + B$$

$$7. AB \oplus BC = B(A \oplus C)$$

$$A \oplus \underline{\overline{A}B} = \overline{A}(\underline{\overline{A}B}) + A(\overline{\overline{A}B})$$

$$= \overline{A}B + A[A + \overline{B}]$$

$$= \overline{A}B + A\overline{B} + A$$

$$= \boxed{\overline{A}B + A}$$

$$= A + B$$

$$A \oplus B = \overline{A}B + A\overline{B}$$

Q) Simplify the following

$$F = x \oplus y \oplus xy$$

$$F = x \oplus y[1 \oplus x]$$

$$= x \oplus y[\bar{x}]$$

$$= x \oplus \bar{x}y$$

$$= x + \bar{x}y$$

$$= x + y$$

Q) Simplify the following

$$F = \bar{A}B \oplus A\bar{B}$$

$$A \oplus B = \bar{A}B + A\bar{B}$$

$$\begin{aligned} F &= \overline{\bar{A}B} \quad A\bar{B} + \overline{A}B \quad \overline{A\bar{B}} \\ &= (\bar{A} + \bar{B})(A\bar{B}) + \overline{A}B (\bar{A} + B) \\ &= \bar{A}\bar{B} + A\bar{B} \quad + \quad \overline{A}B + \bar{A}B \\ &= \bar{A}\bar{B} + A\bar{B} \end{aligned}$$

$$F = A \oplus B$$

# EX-NOR Gate (Ex-OR + NOT)

Symbol



$$Y = \sum m(0, 3) = \overline{A}\overline{B} + AB$$

$$Y = \prod M(1, 2) = (A + \overline{B})(\overline{A} + B)$$

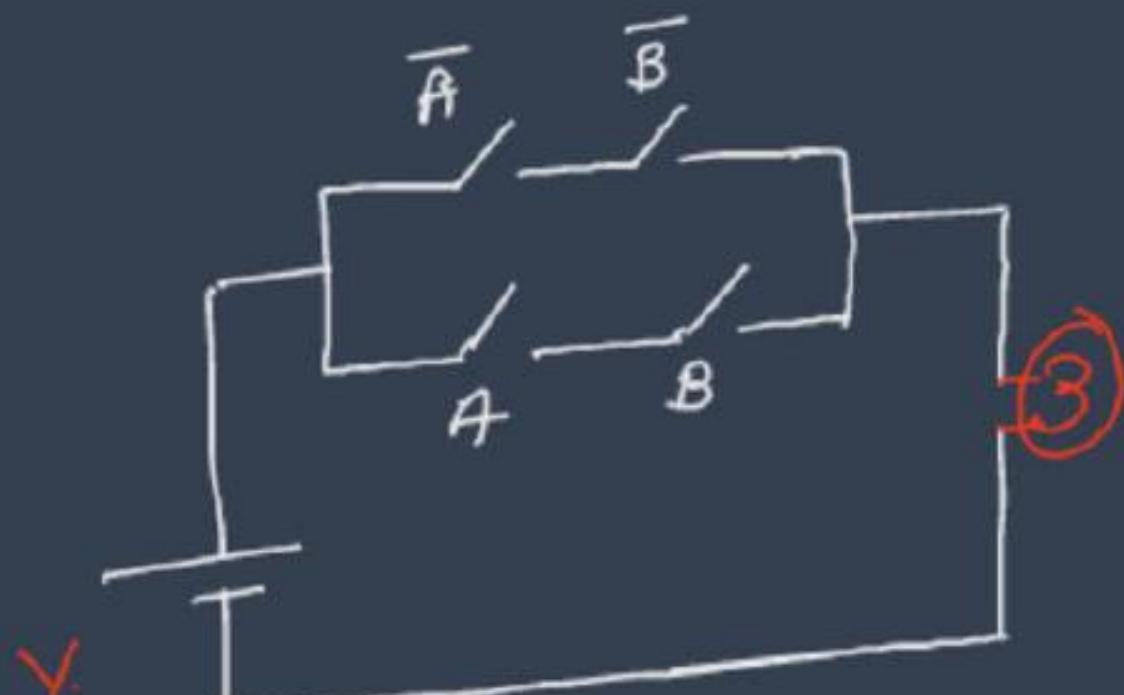
Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

If even number of one's present , then the output is 1

Switching Circuit

$$Y = \bar{A}\bar{B} + AB = (\bar{A}+B)(A+\bar{B})$$



A	B	Y
Off	Off	on.
Off	On	off.
On	Off	off.
On	On	on.

A	B	C	$Y = A \odot B \odot C$	$Y = A \oplus B \oplus C$	$Y = (A \odot B)$	$Y = (A \odot B) \odot C$	$Y = (A \odot C)$	$Y = (A \odot C) \odot B$
0	0	0	1	0	1	0	1	0
0	0	1	0	1	1	1	0	1
0	1	0	0	1	0	1	1	1
0	1	1	1	0	0	0	0	0
1	0	0	0	1	0	1	0	1
1	0	1	1	0	0	0	1	0
1	1	0	1	0	1	0	0	0
1	1	1	0	1	1	1	1	1

$$A \odot B \odot C = \sum m(0, 3, 5, , 6)$$

$$A \oplus B \oplus C = \sum m(1, 2, 4, 7)$$

$$(A \odot B) \odot C = \sum m(1, 2, 4, 7)$$

$$(A \odot C) \odot B = \sum m(1, 2, 4, 7)$$

$$A \oplus B \oplus C = (A \odot B) \odot C = (A \odot C) \odot B$$

Commutative Law

$$A \odot B = B \odot A.$$

Associative Law

$$A \odot B \odot C \neq (A \odot B) \odot C.$$

✗.

NAND

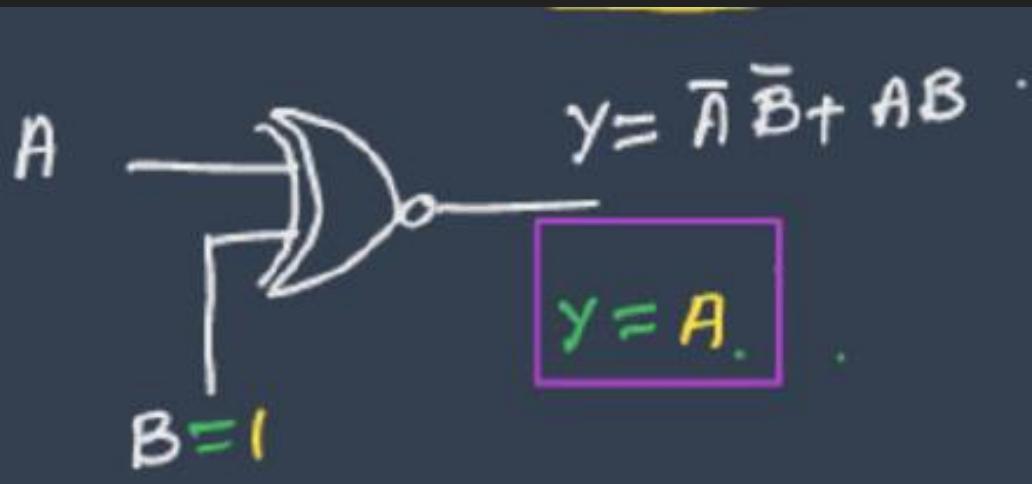
NOR

Ex- NOR.

→ not satisfy  
Associative  
draw  $\equiv$

## EX- NOR Gate as Buffer

## EX- NOR Gate as Inverter



## Timing Diagram



# Properties of EX- NOR Gate

$$1. A \odot 0 = \bar{A}$$

$$2. A \odot 1 = A$$

$$3. A \odot A = 1$$

$$4. A \odot \bar{A} = 0$$

$$5. A \odot A \odot A \odot A \dots\dots n\text{-times} = 1 \\ = A \quad \begin{array}{l} n\text{-even} \\ n\text{-odd} \end{array}$$

$$6. \overline{A \odot B} = A \oplus B$$

$$7. A \oplus \bar{B} = A \odot B$$

$$8. \bar{A} \oplus B = A \odot B$$

$$9. \bar{A} \oplus \bar{B} = A \oplus B$$

$$10. A \odot B = \bar{A} \oplus B = A \oplus \bar{B} = \bar{A} \odot \bar{B}$$

$$11. A \oplus B = A \odot \bar{B} = \bar{A} \odot B = \bar{A} \oplus \bar{B}$$

$$\begin{aligned}12. \overline{A \oplus B \oplus C} &= \bar{A} \odot \bar{B} \odot \bar{C} \\&= A \oplus B \odot C \\&= A \odot B \oplus C\end{aligned}$$

# EX- OR Gate

**OUTPUT = 1**

**For odd number of 1's**

**Odd number of 1's detector**

**Inequality detector**

**Anti coincident Gate**

# EX-NOR Gate

**OUTPUT = 1**

**For even number of 1's**

**Even number of 1's detector**

**Equality detector**

**Coincident Gate**

Q) Simplify the following

$$F = \underline{A \oplus A\bar{B}} \oplus \bar{A}$$

$$F = A \oplus A\bar{B} \oplus \bar{A}$$

$$F = A\bar{B} \oplus \underline{A \oplus \bar{A}}$$

$$F = (A\bar{B}) \oplus \underline{1}$$

$$F = \overline{A\bar{B}} = \bar{A} + B$$

$$F = A \oplus A\bar{B} \oplus \bar{A}$$

$$F = A[1 \oplus \bar{B}] \oplus \bar{A}$$

$$F = AB \oplus \bar{A}$$

$$F = \bar{A} \oplus AB$$

$$F = \bar{A} + AB$$

$$F = \bar{A} + B$$

Q) Simplify the following

$$F = A \oplus B \oplus A \oplus \bar{B}$$

$$F = [A \oplus B] \oplus [A \oplus \bar{B}]$$

$$= (A \oplus B) \oplus (A \odot B)$$

$$= (A \oplus B) \oplus (\overline{A \oplus B}) = 1.$$
  
$$x \oplus \bar{x} = 1.$$

$$F = \underline{\underline{A \oplus A \oplus B \oplus \bar{B}}}$$

$$F = 0 \oplus 1$$

$$\underline{\underline{F = 1}}$$

Q) Simplify the following

$$F = (A \oplus B) + (A \oplus \bar{B})$$

$$F = (\bar{A} \oplus B) + (\bar{A} \oplus \bar{B})$$

$$F = (\bar{A} \oplus B) + \overline{(\bar{A} \oplus B)}$$

$$F = x + \bar{x} = 1.$$

Q) Simplify the following

$$[(\underline{1 \oplus P}) \oplus (\underline{P \oplus Q})] \oplus [(\underline{P \oplus Q}) \oplus (\underline{Q \oplus 0})]$$

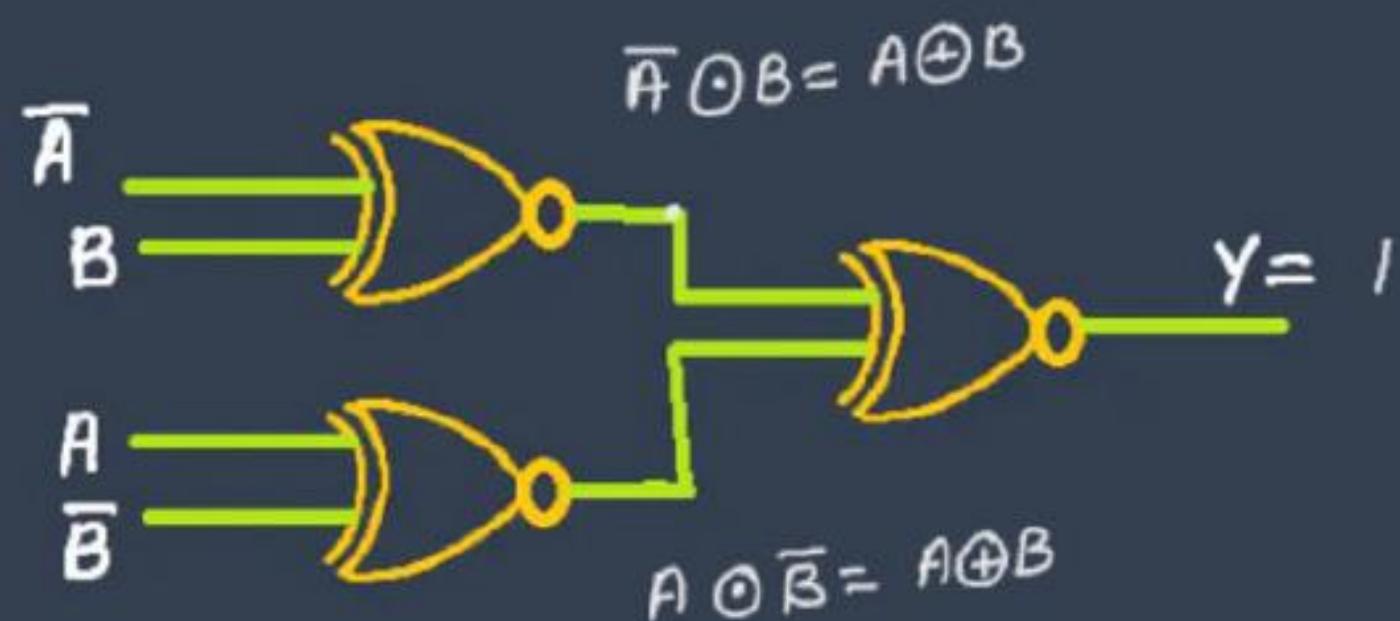
$$[\underline{\bar{P} \oplus P \oplus Q}] \oplus [P \oplus \underline{Q \oplus Q}]$$

$$(\underline{1 \oplus 0}) \oplus [\underline{P \oplus 0}]$$

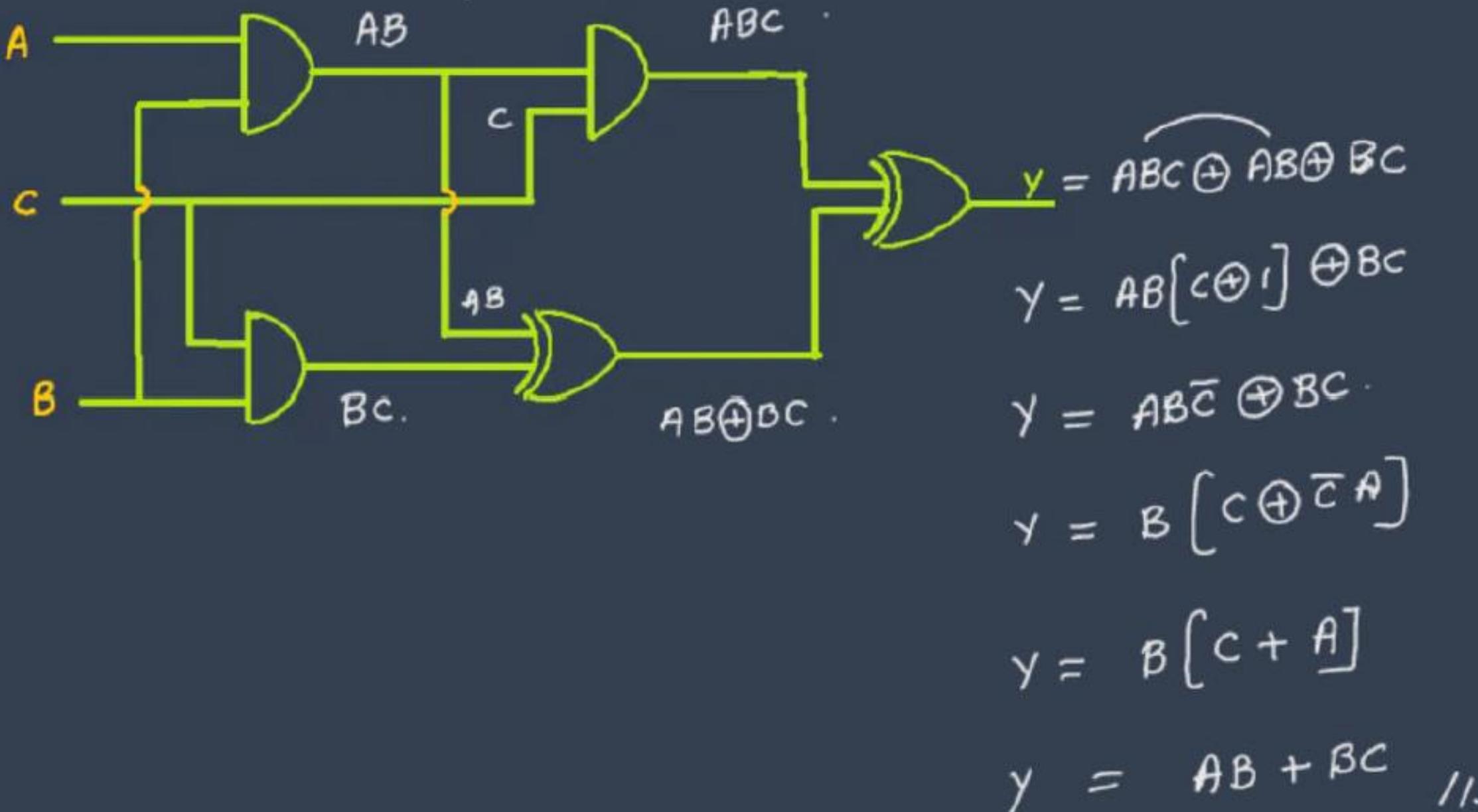
$$\bar{Q} \oplus P$$

$$P \oplus \bar{Q} = \underline{\underline{P \odot Q}}$$

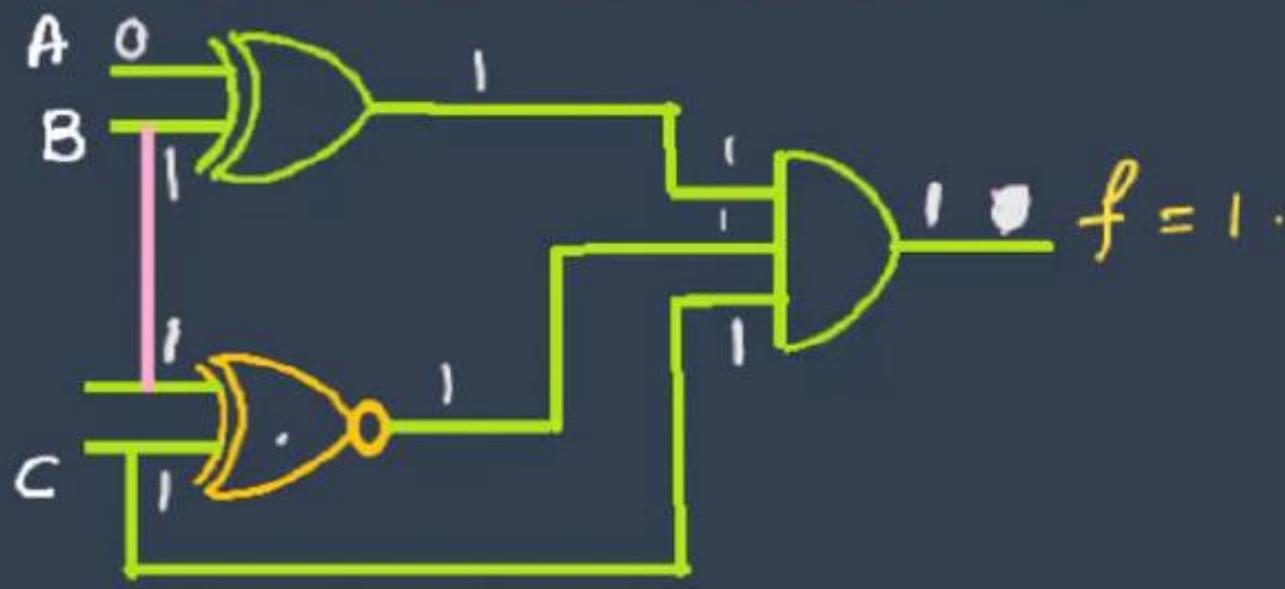
Q) The output Y =.....



Q) The output Y =.....



Q) if  $f = 1$ , the values of A, B and C are.....

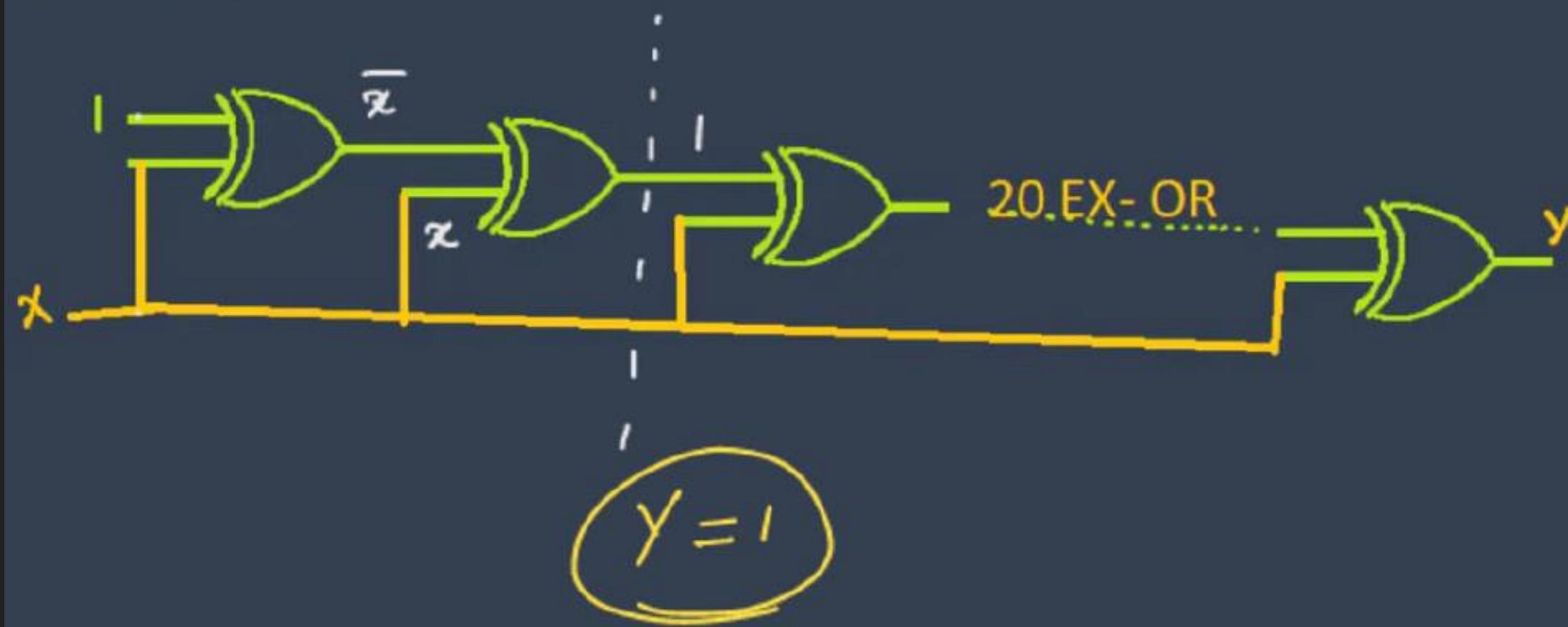


$$C = 1$$

$$B = 1$$

$$A = 0$$

Q) The output Y = .....



Q) Find the minterms of 3 variable EX-OR and EX-NOR gate

$$Y = A \oplus B \oplus C = \sum m (1, 2, 4, 7)$$

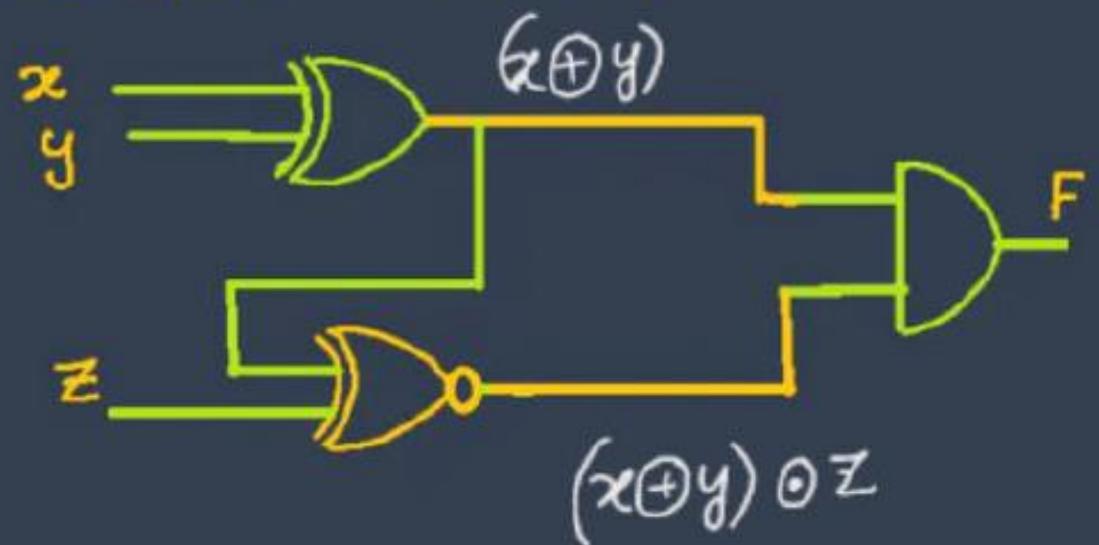
$$Y = A \ominus B \ominus C = \sum m (0, 3, 5, 6)$$

Q) Find the minterms of 4 variable EX-OR and EX-NOR gate

$$Y = A \oplus B \oplus C \oplus D = \sum m(1, 2, 4, 7, 8, 11, 13, 14)$$

$$Y = A \ominus B \ominus C \ominus D = \sum m(0, 3, 5, 6, 9, 10, 12, 15).$$

Q) The output F = .....



$$F = (x \oplus y) \odot z = x \odot y \odot z.$$

$$= \overline{(x \oplus y)} \bar{z} + (x \oplus y) z.$$

$$= (x \odot y) \bar{z} + \bar{x}yz + x\bar{y}z.$$

$$= \frac{\bar{x}\bar{y}\bar{z}}{0} + \frac{x\bar{y}\bar{z}}{6}, \quad \frac{\bar{x}yz}{3}, \quad \frac{x\bar{y}z}{5}.$$

# Logic Gate



$\equiv$



$\equiv$



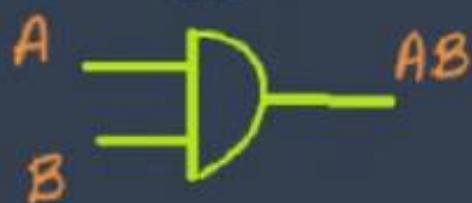
# Alternative Gate



$\equiv$



# Logic Gate



$\equiv$



$\equiv$

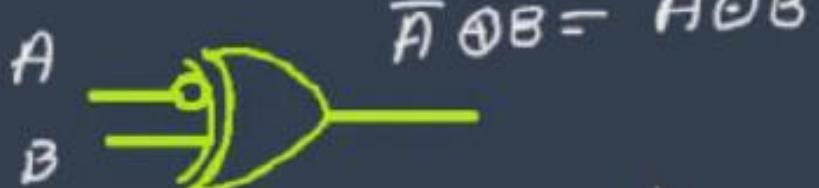


$\equiv$



$\equiv$

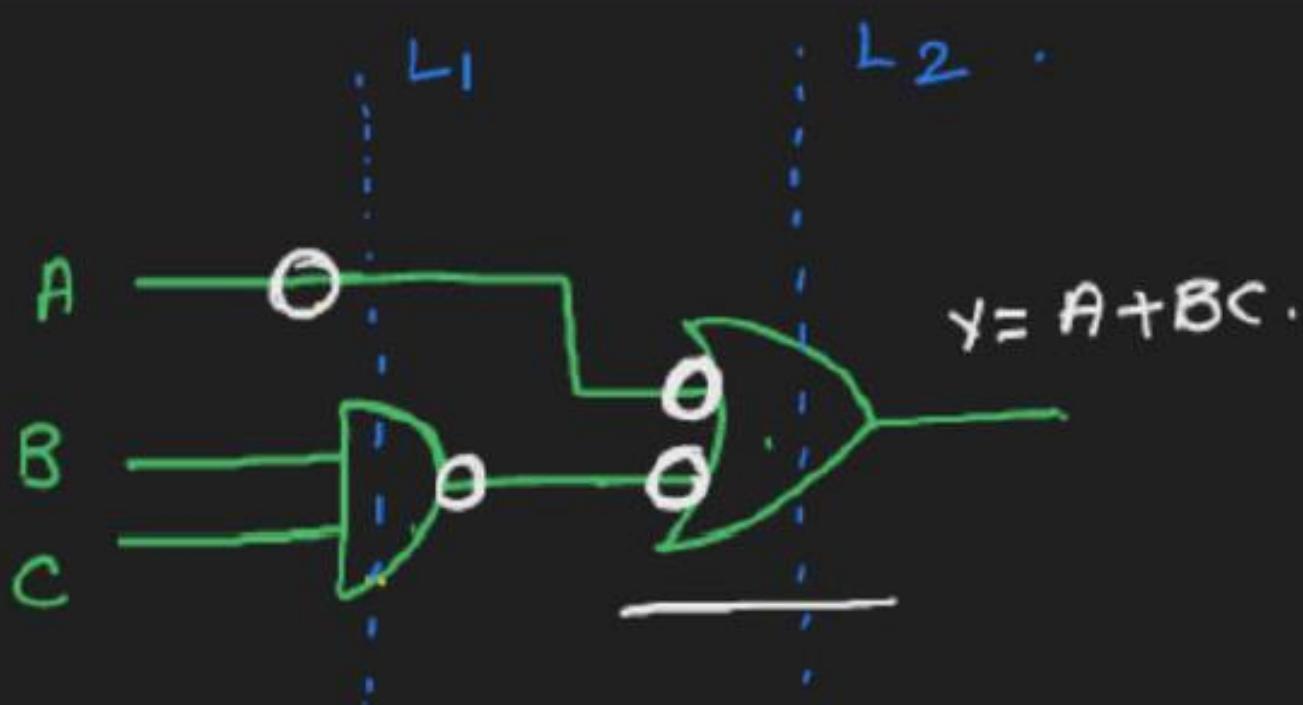
# Alternative Gate



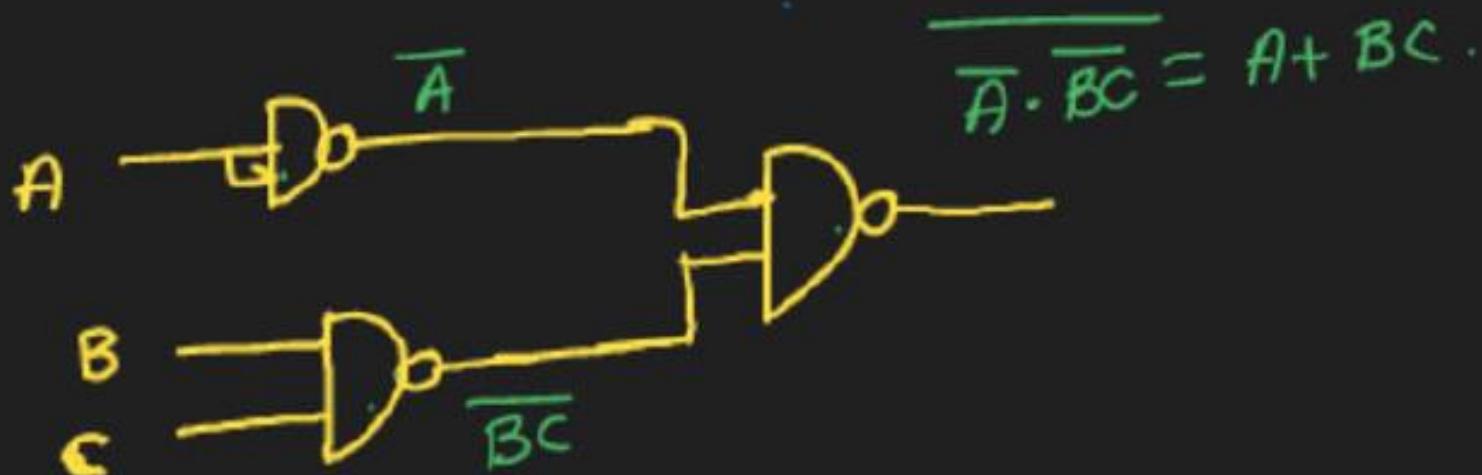
1. Bubbled AND gate → NOR gate.
2. Bubbled OR gate → NAND gate.
3. Bubbled NAND gate → OR gate.
4. Bubbled NOR gate → AND gate.

Q)  $Y = A + BC$  implement using NAND gates

✓

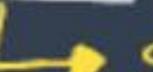


Two-level AND-OR logic  $\equiv$  NAND-NAND logic.

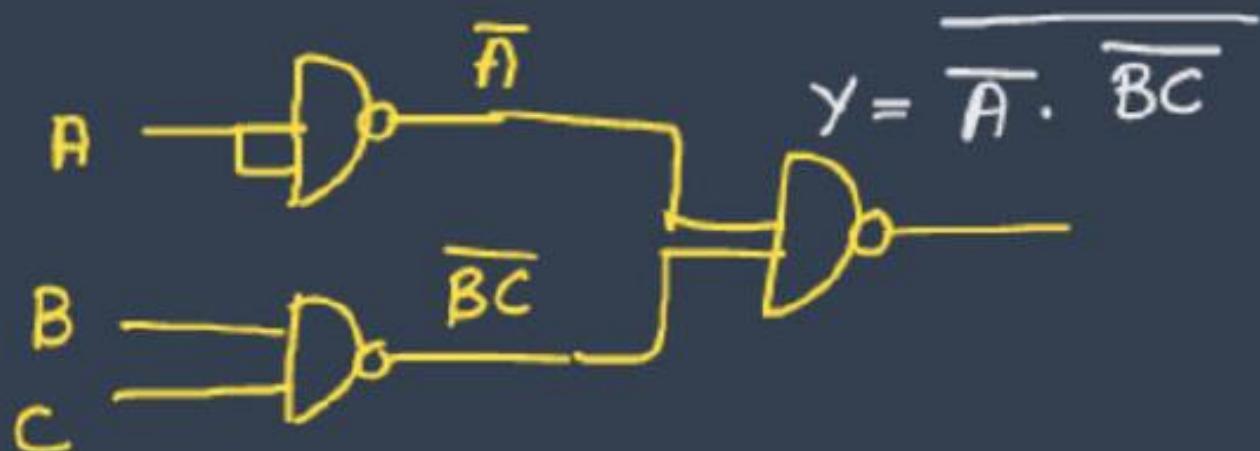


Q)  $Y = A + BC$  implement using NAND gates

$$Y = A + BC \rightarrow SOP$$

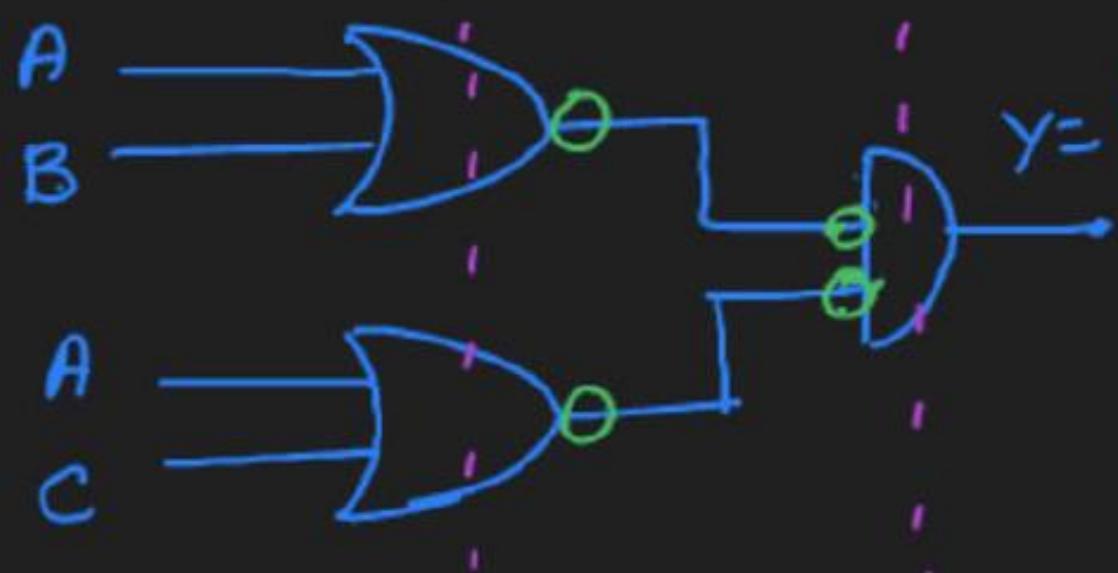
NAND   $\rightarrow SOP$

$$Y = \overline{\overline{A + BC}}$$
$$Y = \overline{\overline{\overline{A} \cdot \overline{BC}}}$$

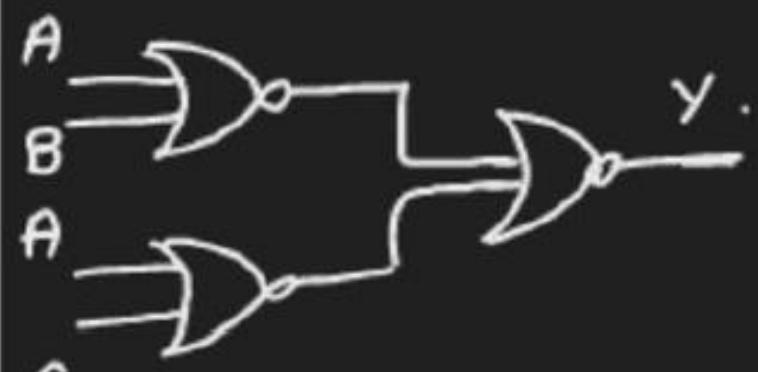


Q)  $Y = A + BC$  implement using NOR gates

$$Y = A + BC = \overline{\overline{A+B}} \cdot \overline{\overline{A+C}}$$



$$Y = (A+B)(A+C)$$



Two level OR-AND logic  $\equiv$  NOR-NOR logic.

Q)  $Y = A + BC$  implement using NOR gates

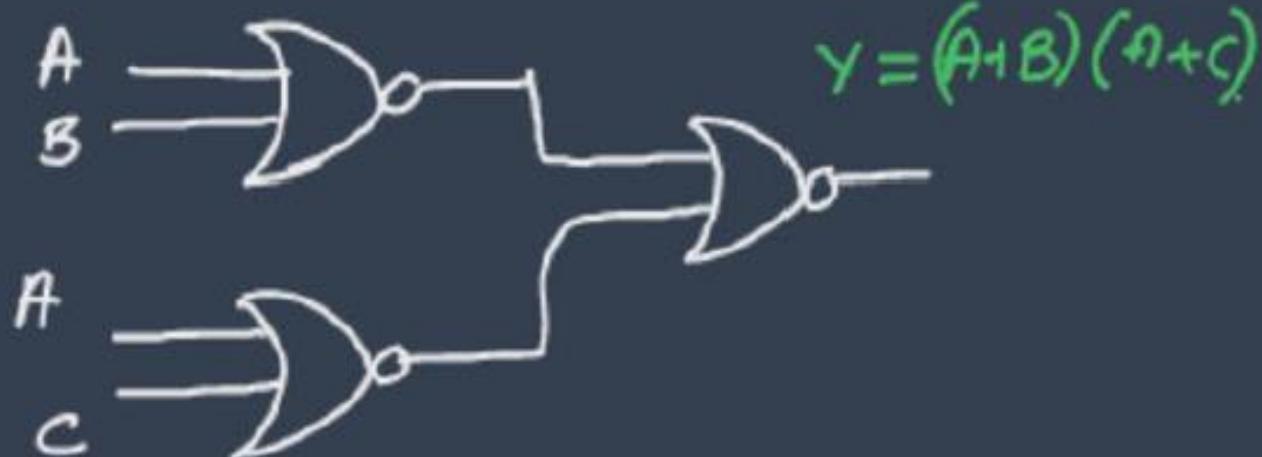
$$Y = A + BC \rightarrow SOP$$

NOR  $\rightarrow POS$

$$Y = (\bar{A} + B)(\bar{A} + C) \rightarrow POS$$

$$Y = \overline{\overline{(A+B)(A+C)}}$$

$$Y = \overline{\overline{(A+B)}} + \overline{\overline{(A+C)}}$$



Q)  $Y = (\bar{W} + \bar{X})(Y + Z)$  implement using NAND gates

$$Y = \overline{\omega x} (y + z)$$

$$\overline{\omega x} = 1$$

$$Y = \overline{\omega x} y + \overline{\omega x} z$$

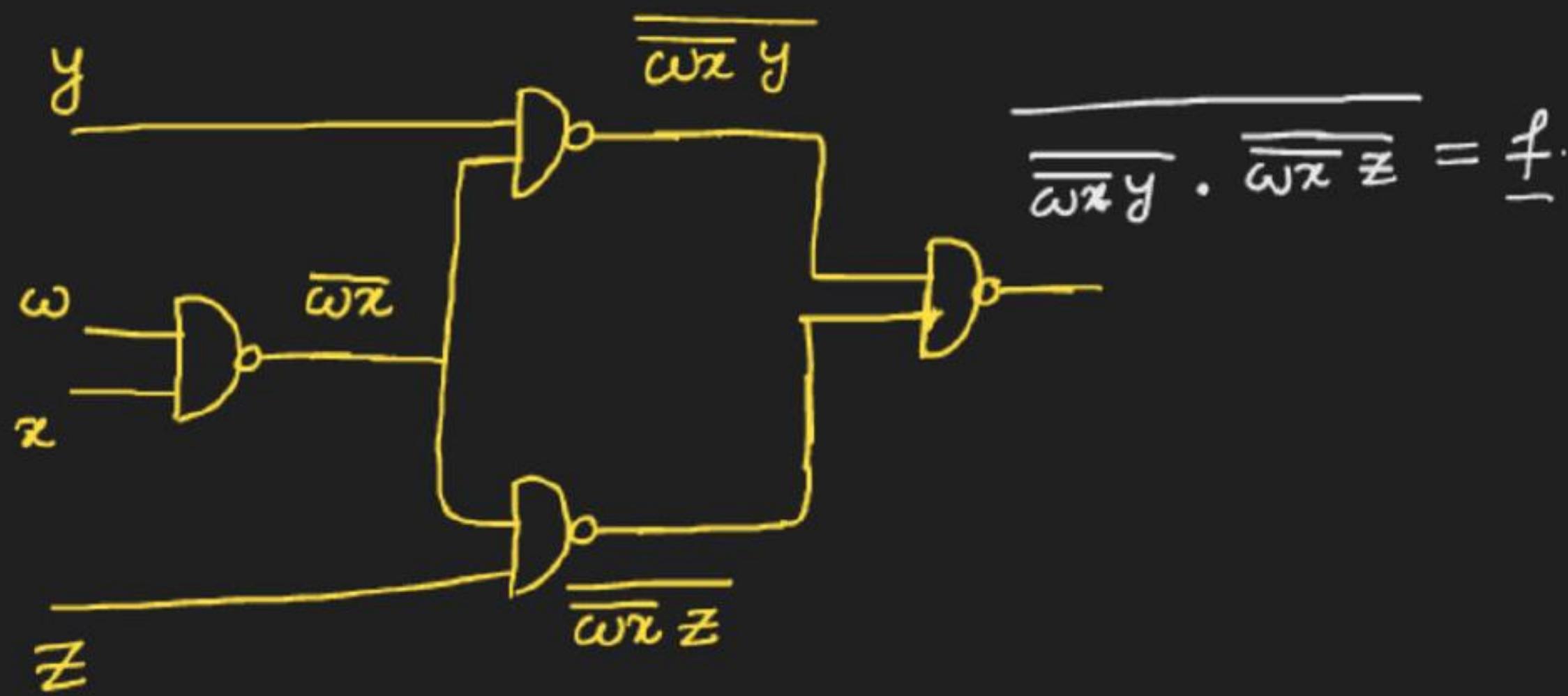
$$\overline{\overline{\omega x} \cdot y} = 1 + 1$$

$$Y = \overline{\omega x} y + \overline{\omega x} z$$

$$\overline{\overline{\omega x} \cdot z} \rightarrow 3$$

$$Y = \overline{\overline{\omega x} y} \cdot \overline{\overline{\omega x} z}$$

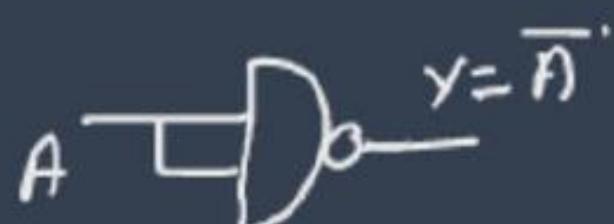
$$\overline{\overline{\omega x} y} \cdot \overline{\overline{\omega x} z} \rightarrow ④$$



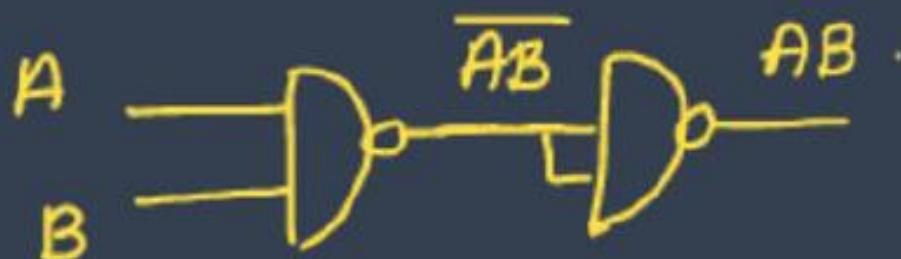
(4)

# NAND Gate as Universal Gate

1. NOT gate



2. AND gate



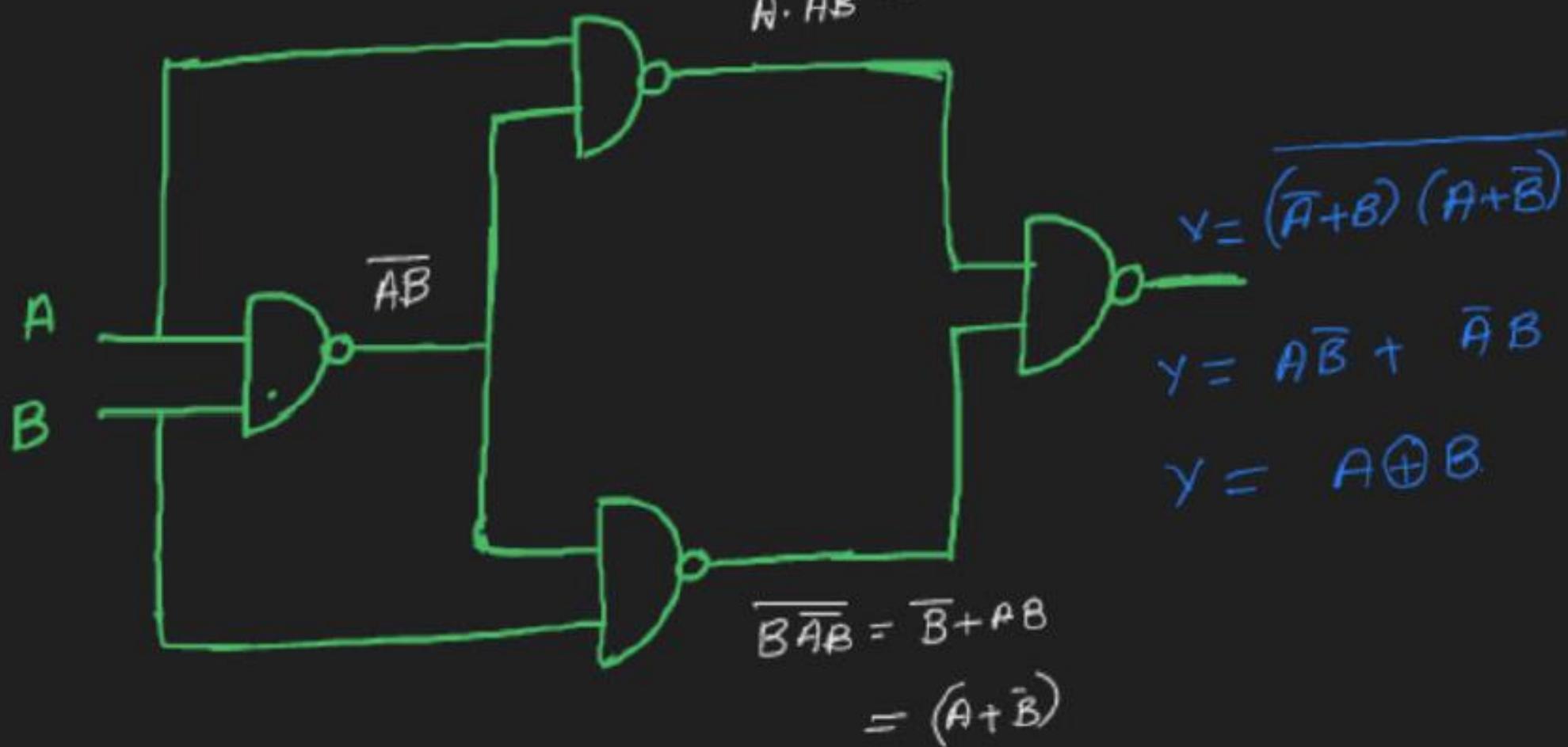
3. OR-gate



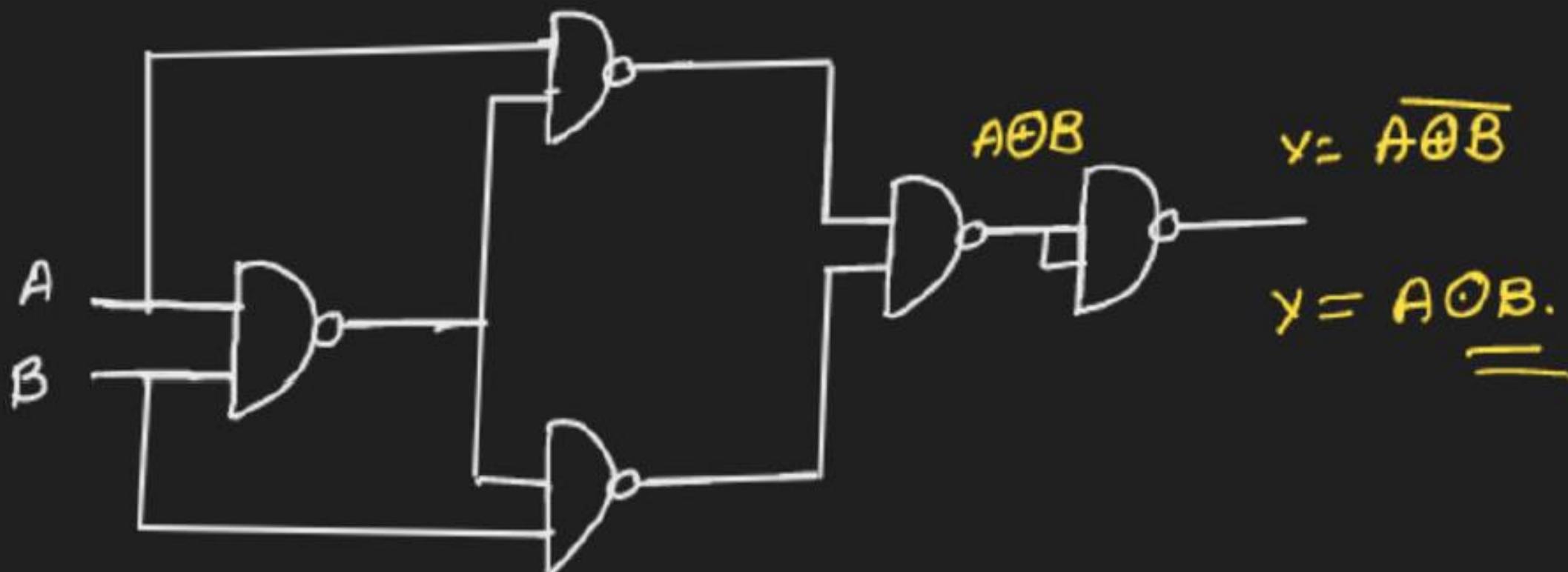
4. NOR-gate



## 5. Ex-OR gate



6.

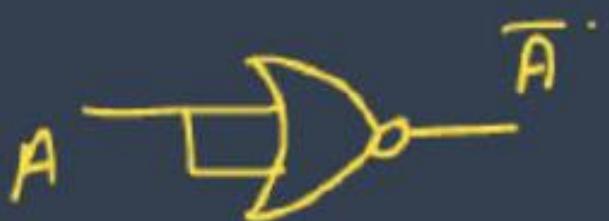
Ex-NOR Gate

$$y = A \overline{B}$$

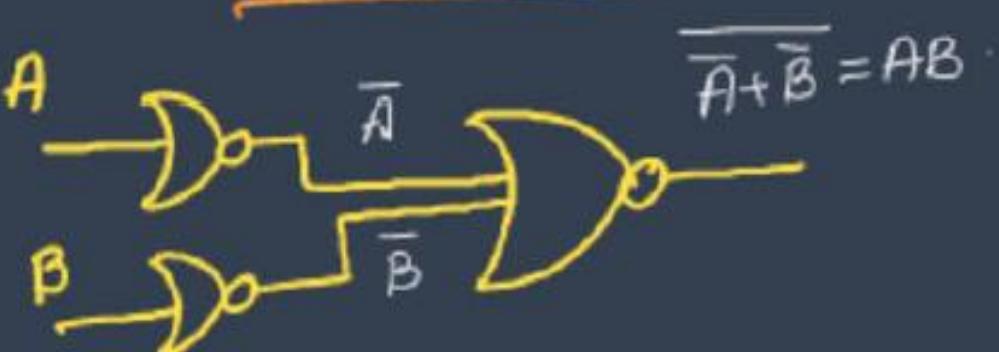
$$y = A \oplus B.$$

# NOR Gate as Universal Gate

1. NOT-Gate



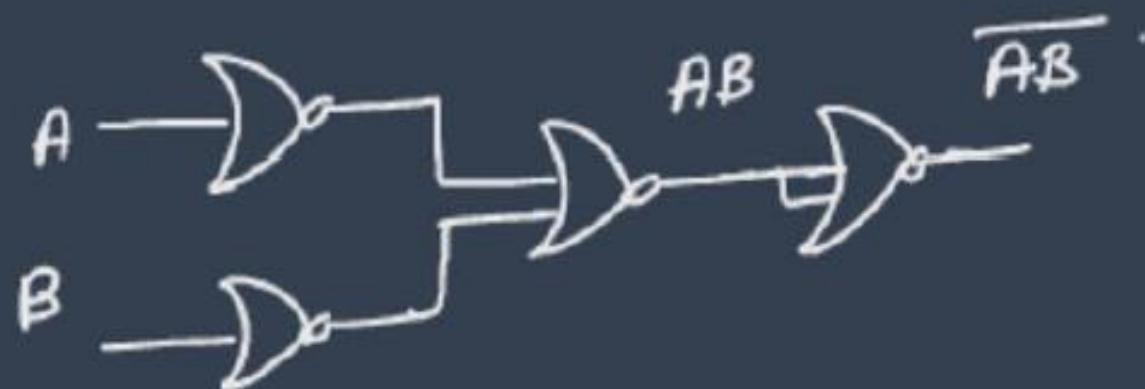
2. AND-Gate



3. OR-Gate



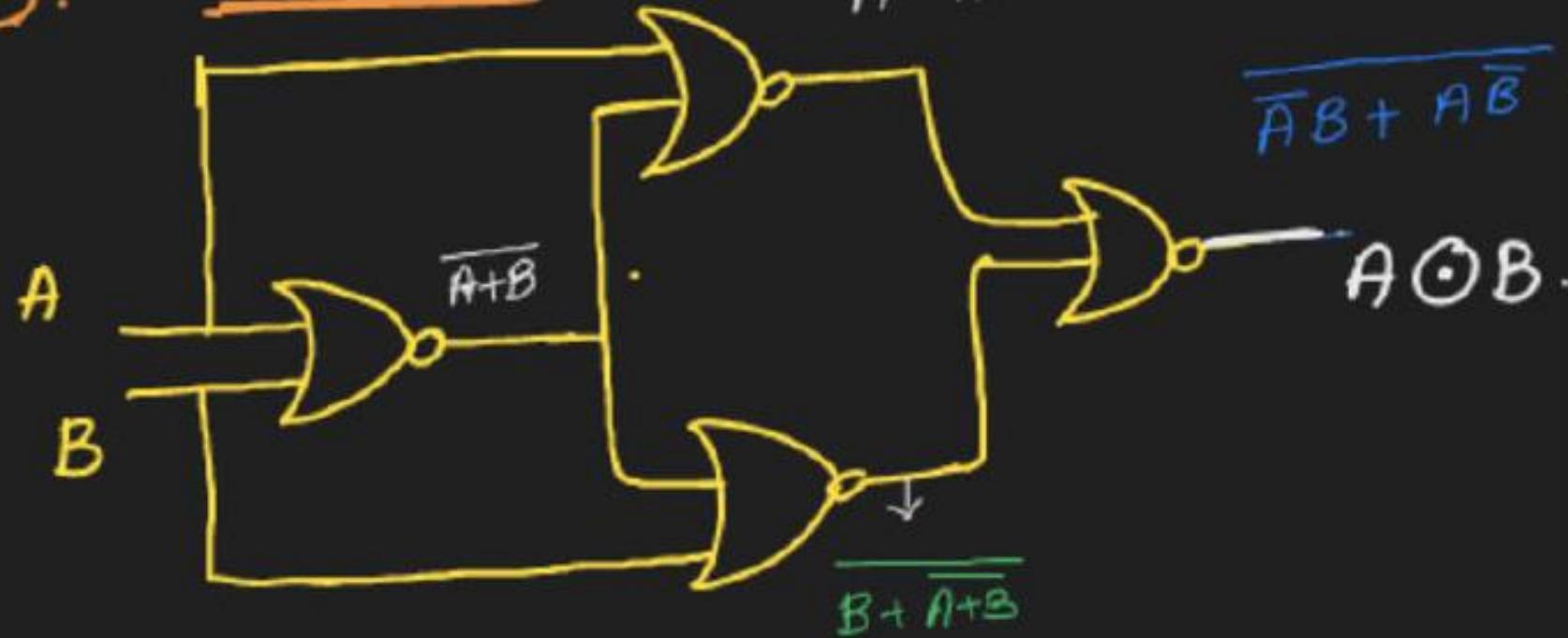
4. NAND-Gate



5.

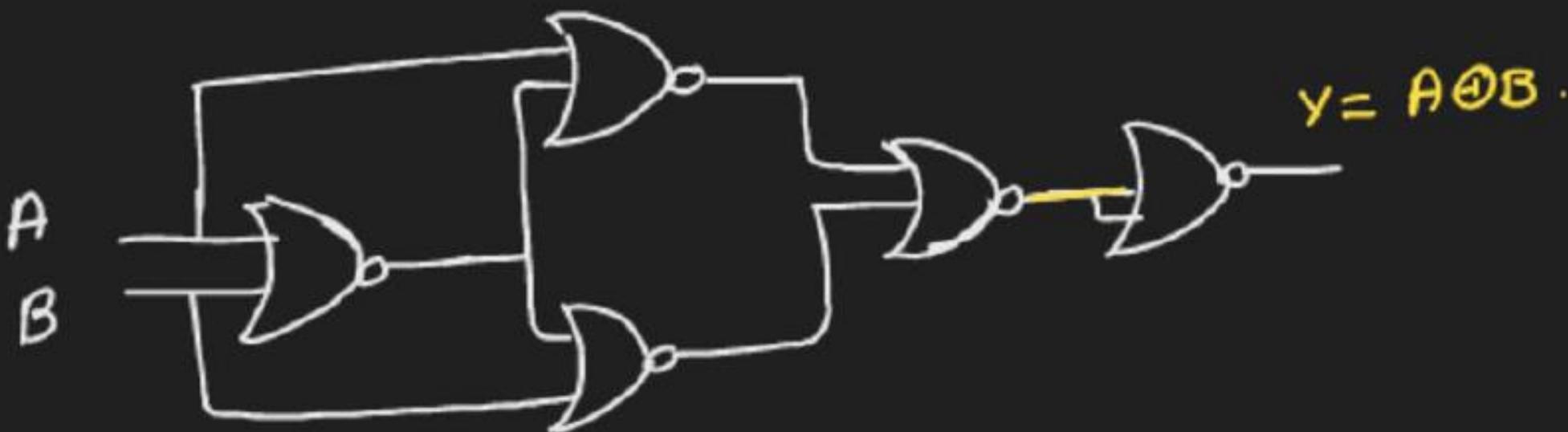
Ex-NOR

$$\overline{A + \overline{A+B}} = \overline{A} \cdot (A+B) = \overline{A}B$$



(4)

## 6. Ex-OR



⑤

	NAND GATES	NOR GATES
NOT	1	1
AND	2	3
OR	3	2
EX-OR	4	5
EX-NOR	5	4
NAND	1	4
NOR	4	1

The circuit shown below is to be used to implement the function  
 $Z = f(A, B) = \overline{A} + B$ .



What values are to be selected for I and J?

(IES-2006)

(IES-2010)

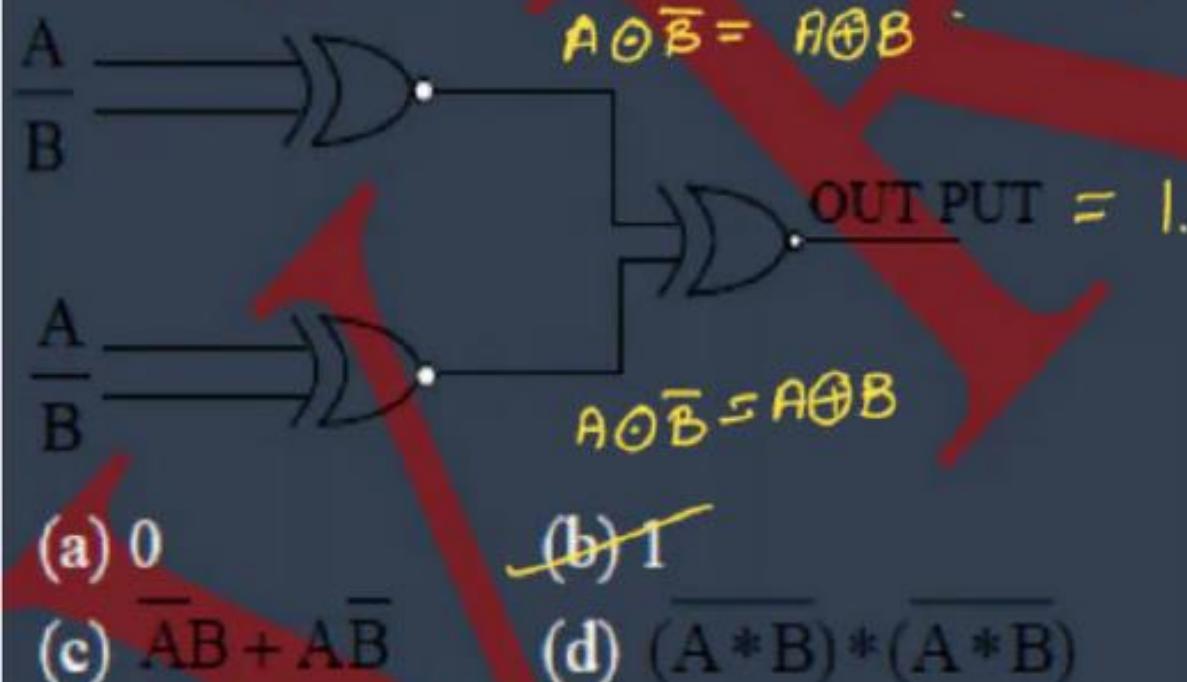
- (a)  $I = 0, J = B$
- (b)  $I = A, J = B$
- (c)  $\overline{I} = 1, J = B$
- (d)  $I = \overline{B}, J = 0$

$$\begin{aligned}Z &= (\overline{A} + I)(\overline{A} + J) = \overline{A}J + \overline{A}I + IJ \\&= \overline{A}J + \overline{A} + J = \overline{A} + J[1 + \overline{A}] \\&= \overline{A} + J\end{aligned}$$

$$I = 1.$$

$$J = B.$$

. The output of the circuit shown in the figure is equal to (IES-2008)

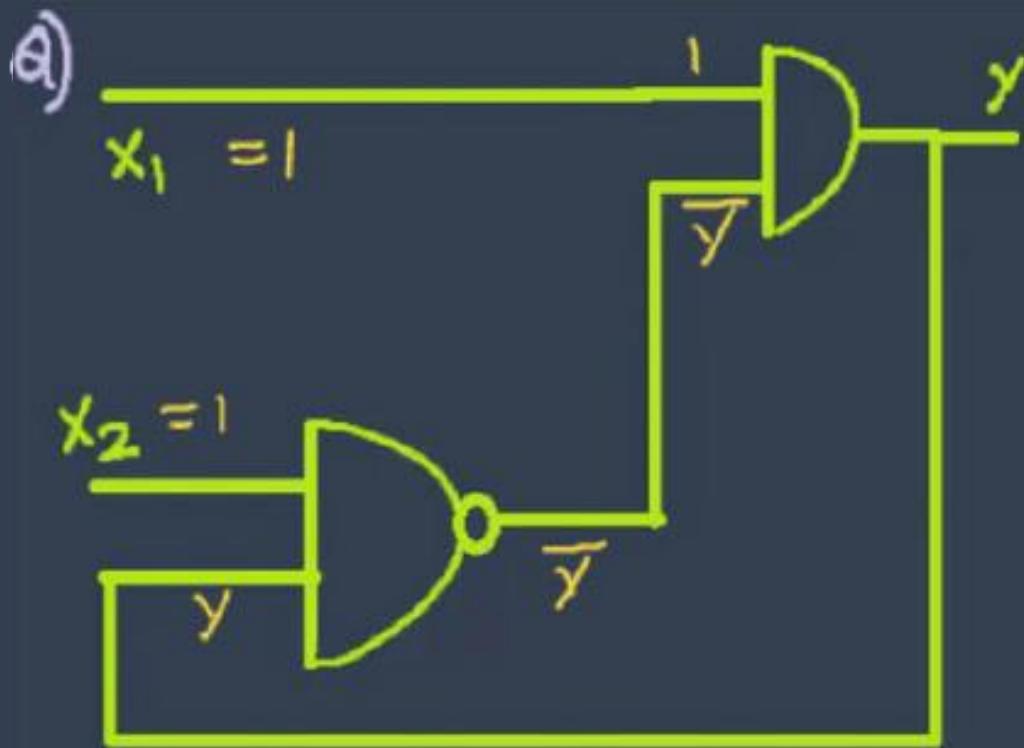




The output X of the above logic circuits is:

(IES-2009)

- (a)  $AB + CD + EF$  ✓
- (b)  $\overline{AB} + \overline{CD} + \overline{EF}$
- (c)  $(A + B)(C + D)(E + F)$
- (d)  $(\overline{A + B})(\overline{C + D})(\overline{E + F})$



If  $x_1 = x_2 = 1$  then  $y$  is

- a) 1
- b) 0
- c) initial value
- d) unstable. ✓

$$y = \bar{y}$$

if initially  $y=0$ ,

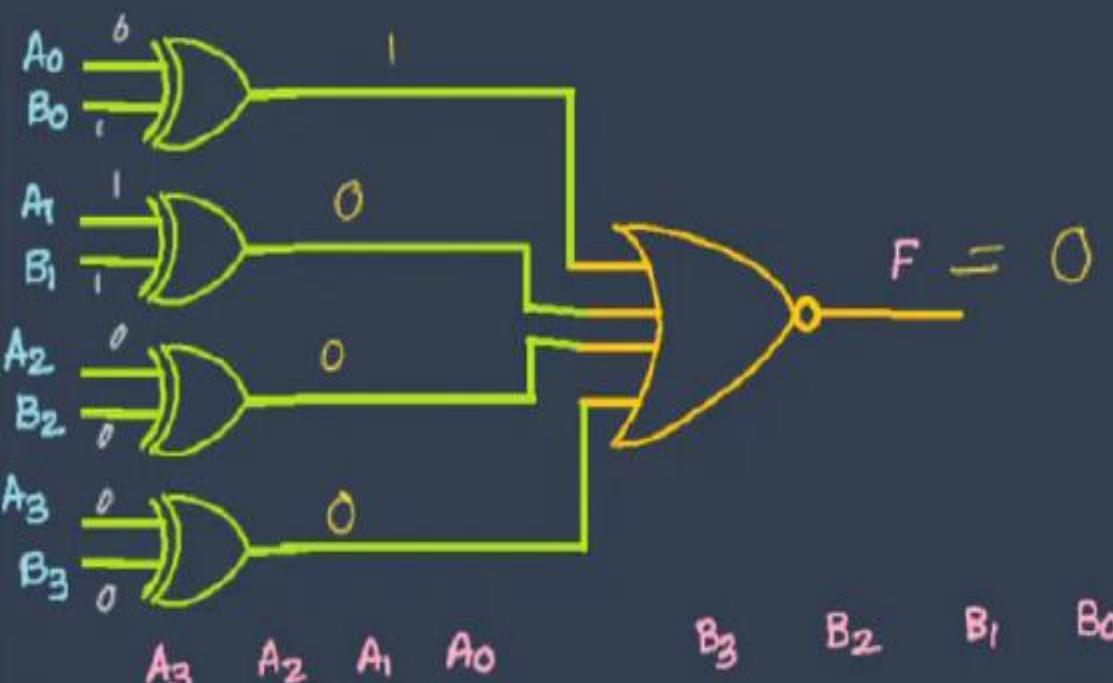
$$y = 1$$

if initially  $y=1$

$$y = 0$$

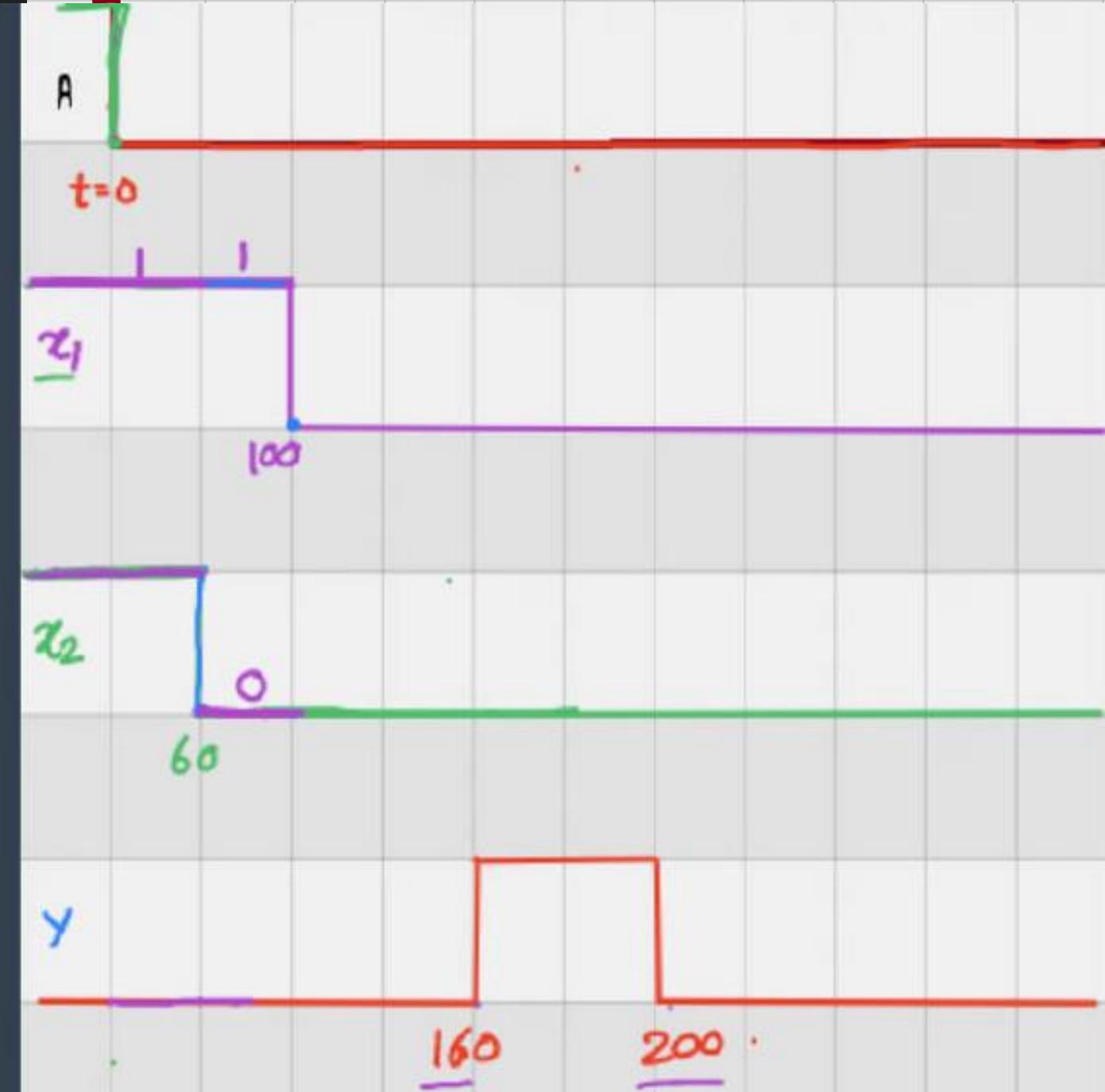
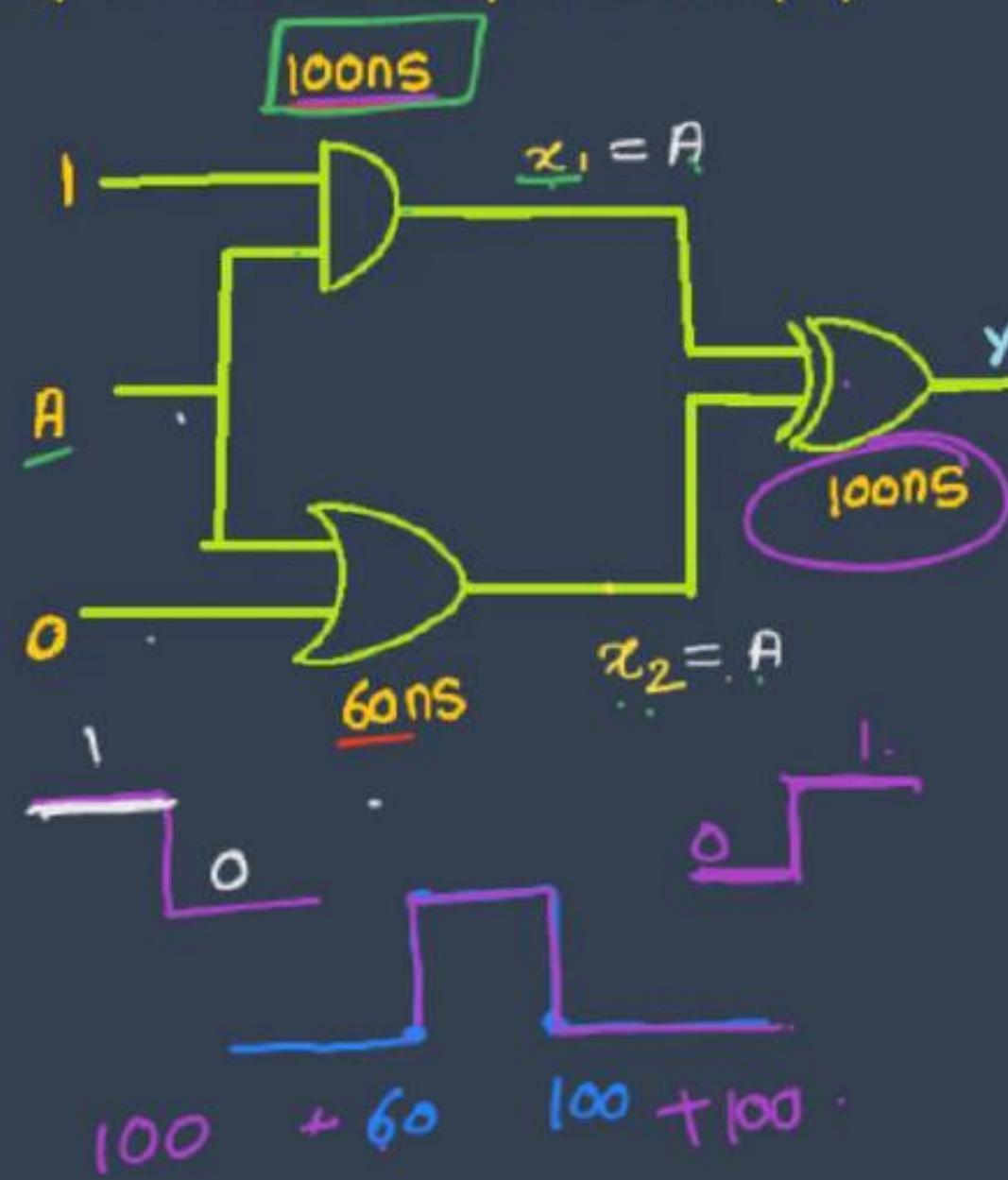


Q) if  $F = 0$  then the inputs

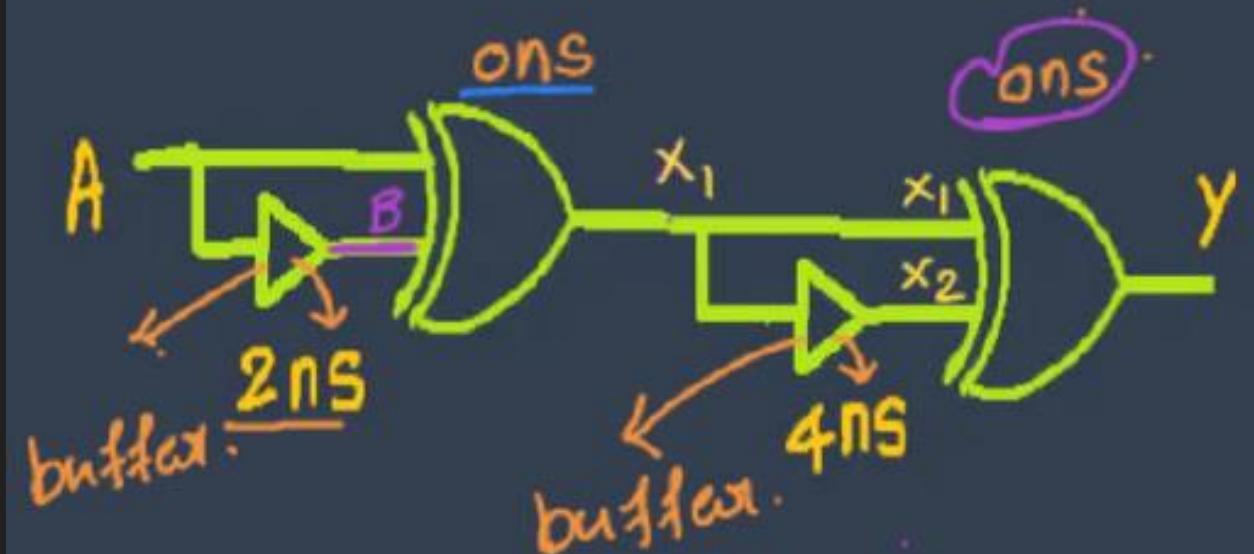


- |    | $A_3$ | $A_2$ | $A_1$ | $A_0$ | $B_3$ | $B_2$ | $B_1$ | $B_0$ |
|----|-------|-------|-------|-------|-------|-------|-------|-------|
| a) | 1     | 0     | 1     | 0     | 1     | 0     | 1     | 0     |
| b) | 0     | 1     | 0     | 1     | 0     | 1     | 0     | 1     |
| c) | 0     | 0     | 1     | 0     | 0     | 0     | 1     | 1     |
| d) | 0     | 1     | 0     | 0     | 0     | 1     | 0     | 0     |

Q) Draw the output wave (Y)



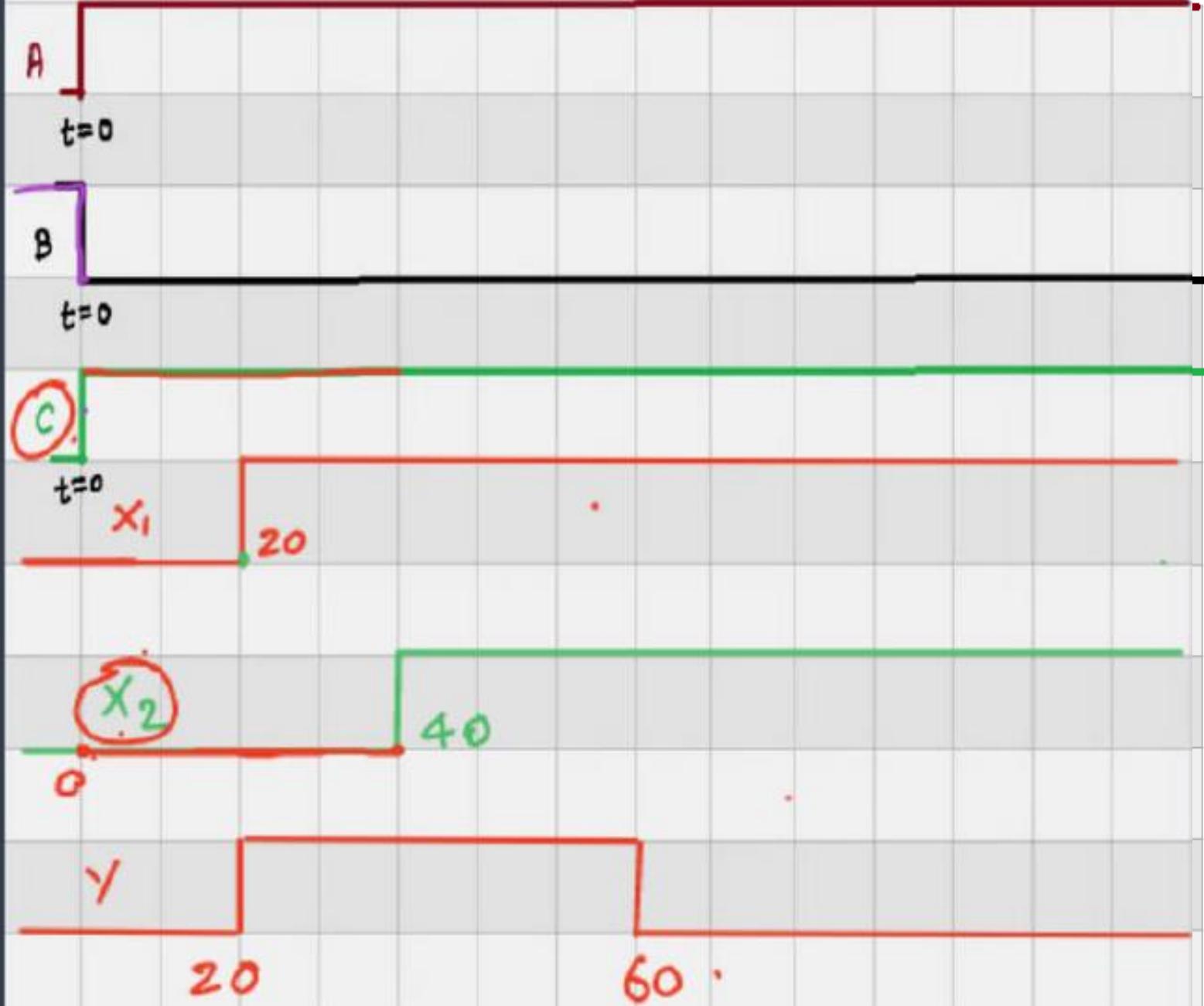
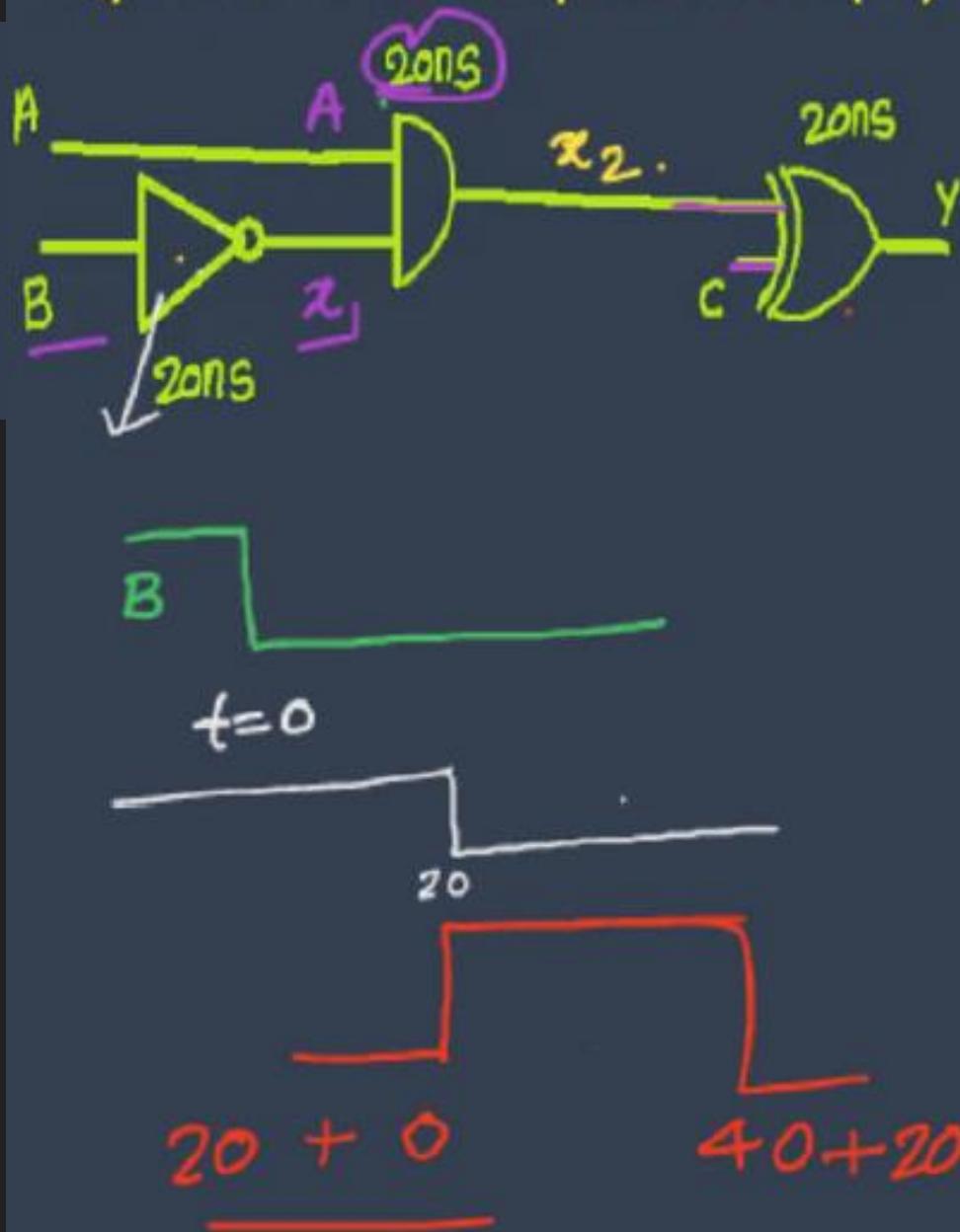
Q) How many transition's occurs in the output Y from 0 to 10 ns



④



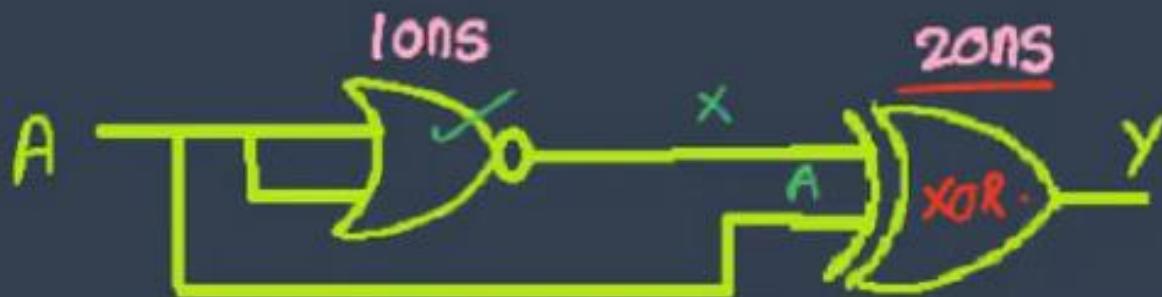
Q) Draw the output wave (Y)



Q) Draw the output wave ( Y )

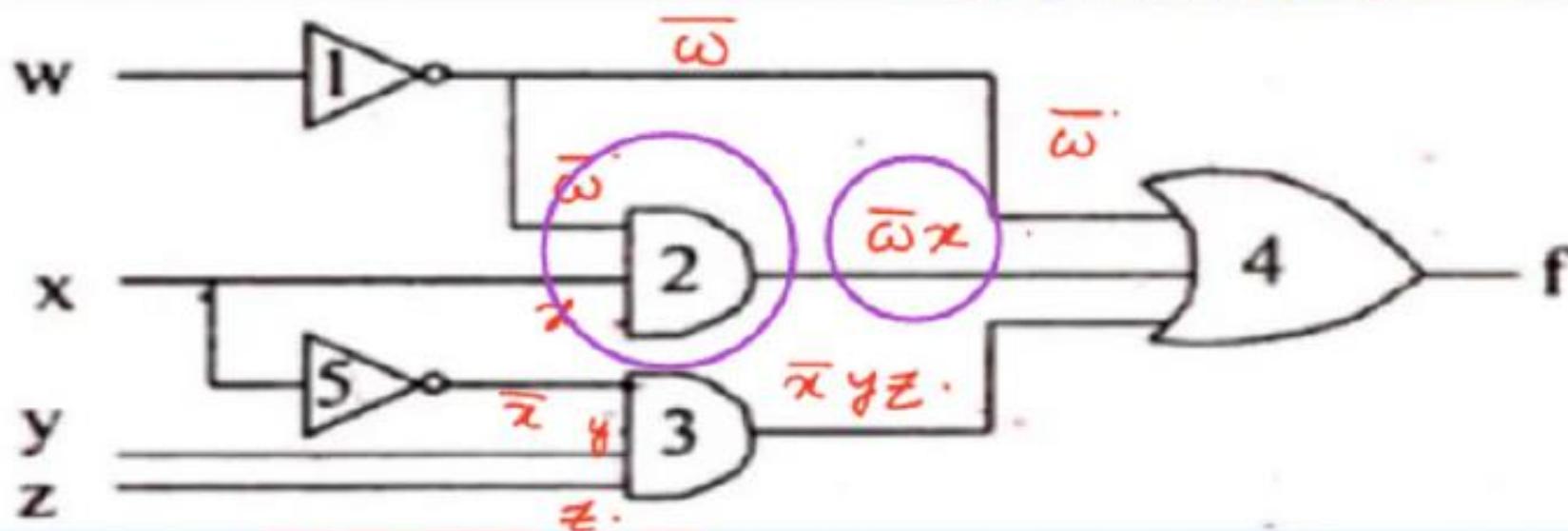


Q) Draw the output wave ( Y )



Consider the following gate network:

(IES 2011)



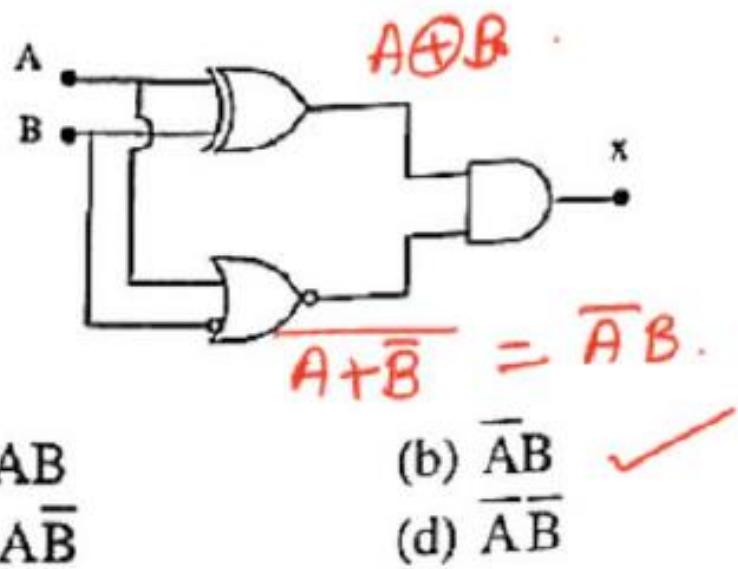
Which one of the following gates is redundant

- (a) Gate No. 1
- (b) Gate No. 2 ✓
- (c) Gate No. 3
- (d) Gate No. 4

$$f = \bar{w} + \cancel{\bar{w}x} + \bar{x}yz.$$

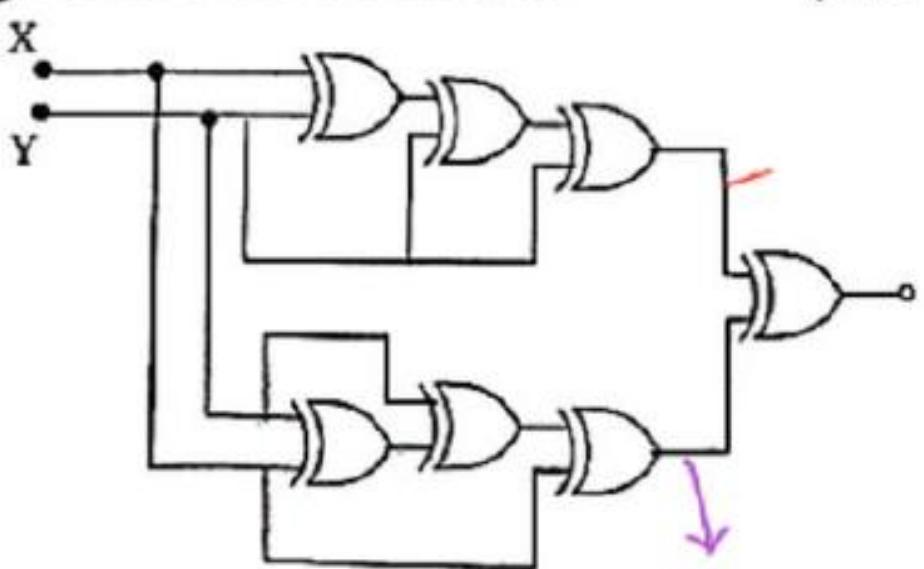
$$f = \bar{w}[1+x] + \bar{x}yz = \bar{w} + \bar{x}yz.$$

The output X of the circuit shown in the figure will be (IES-98)



$$X = \bar{A}\bar{B} [\bar{A}B + A\bar{B}]$$
$$X = \bar{A}\bar{B} + 0$$

The circuit shown in the figure below generates the function of  
(IES-10)



- (a)  $X \oplus Y$  ✓
- (b) 0
- (c)  $X\bar{Y} + YX + \bar{Y}X$
- (d)  $X \cdot \bar{Y}$

$$x \oplus y \oplus y \oplus y = x \oplus y \oplus 0 = x \oplus y$$

$$x \oplus y \oplus y \oplus x = 0$$

$$x \oplus y \oplus 0 = x \oplus y$$

Q) A 3 – input majority gate is defined by the logic function  $M(a, b, c) = ab + bc + ca$ , which one of the following gates is represented by the function  $M(\overline{M(a, b, c)}, \overline{M(a, b, \bar{c})}, \overline{c}) \dots$

- a) 3- input NAND gate
- b) 3- input EX-OR gate ✓
- c) 3- input NOR gate
- d) 3- input XNOR gate

$$M(x, y, z) = xy + yz + zx$$

$$x = \overline{M(a, b, c)} = \sum m(0, 1, 2, 4)$$

$$M(a, b, c) = ab + bc + ca$$

$\begin{matrix} 1 & 0 \\ 1 & 1 \\ 1 & 1 \end{matrix}$	$\begin{matrix} 0 & 1 & 1 \\ 0 & 1 & 1 \\ 1 & 1 & 1 \end{matrix}$	$\begin{matrix} 1 & 0 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{matrix}$
---	---	---

$$M(a, b, c) = \sum m(3, 5, 6, 7)$$

$$y = m(a, b, \bar{c}) = ab + b\bar{c} + a\bar{c}$$

$\begin{matrix} 1 & 1 & 0 \\ 1 & 1 & 1 \end{matrix}$	$\begin{matrix} 0 & 1 & 0 \\ 1 & 1 & 0 \end{matrix}$	$\begin{matrix} 1 & 0 & 0 \\ 1 & 1 & 0 \end{matrix}$
--	--	--

$$y = m(a, b, \bar{c}) = \sum m(2, 4, 6, 7)$$

$$z = \overline{\dots} c = \sum m(1, 3, 5, 7)$$

$\begin{matrix} 0 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \end{matrix}$
--

$$x = \Sigma m(0, 1, 2, 4)$$

$$y = \Sigma m(2, 4, 6, 7)$$

$$z = \Sigma m(1, 3, 5, 7)$$

$$M(x, y, z) = \underline{xy} + yz + zx.$$

$$= (2, 4) + (7) + (1)$$

$$M(x, y, z) = \Sigma m(1, 2, 4, \underline{\underline{7}})$$

3-i/p

XOR

=

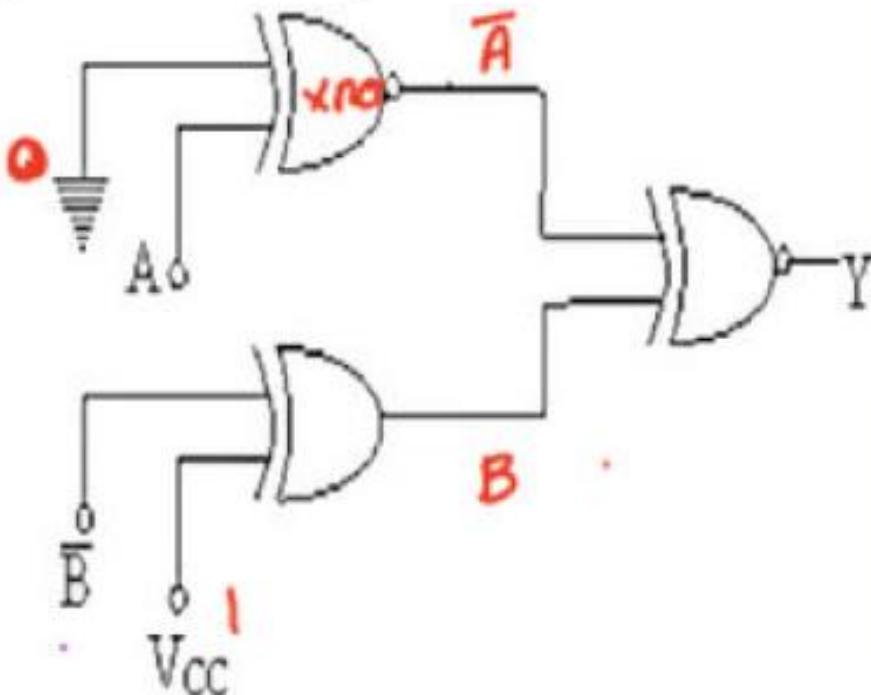
Consider the circuit shown below. The expression for the output Y is

(a)  $(\bar{A} + \bar{B})(A + \bar{B})$

(b)  $(\bar{A} + B)(A + \bar{B})$

(c)  $\bar{A} + \bar{B}$

(d)  $(A + B)(\bar{A} + \bar{B})$



$$= \bar{A} \oplus B = A \oplus B$$

$$Y = (\bar{A} + \bar{B})(A + B)$$

$$Y = \bar{A}B + A\bar{B}$$



Q) The following expression was to be realized using 2 input AND , OR gates , however during fabrication all 2 input AND gates are mistakenly substituted by 2 input NAND gates

$$\underline{(ab)c} + \underline{(\bar{a}c)}d + (bc)d + ad$$

what is the function realised finally

a) i                      b)  $\bar{a} + \bar{b} + \bar{c} + \bar{d}$

c)  $\bar{a} + b + \bar{c} + \bar{d}$  ✓

d)  $\bar{a} + \bar{b} + c + \bar{d}$

$$\overline{\overline{ab}}\overline{c} + \overline{\overline{(\bar{a}c)}}d + \overline{\overline{(bc)}}d + \overline{\overline{ad}}$$

$$ab + \bar{c} + \bar{a}c + \underline{\bar{d}} + bc + \underline{\bar{d}} + \bar{a} + \underline{\bar{d}}$$

$$\bar{a} + \bar{c} + \bar{d} + ab + bc = \bar{a} + b + \bar{c} + \bar{d} + bc = \bar{a} + b + \bar{c} + \bar{d}$$

# Functionally Complete (universal set)

- Any arbitrary function is said to be functionally complete , if it can give 3 basic operations ( and , or , not ) (or) NAND (or) NOR .
- NAND ,NOR gates are always functionally complete since any given Boolean function can be implemented .
- For a given function to verify whether it is functionally complete or not then substitute A , 0 , 1 in place of various Boolean variable's

<u>f :</u>	
<u>AND + NOT</u>	✓
<u>OR + NOT</u>	✓
<u>NAND</u>	✓
<u>NOR</u>	✓

Q) Verify whether the function is functionally complete or not

$$f(A, B, C) = \bar{A}B + C$$

AND, + NOT

$$f(\underline{A}, \underline{B}, \underline{C}) = \bar{A} \rightarrow \text{NOT}$$

OR + NOT

$$f(\underline{A}, \underline{B}, \underline{C}) = \bar{A}B + C = \frac{\bar{A} + C}{\bar{B}} \rightarrow \text{OR}$$

functionally complete

---

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A + \bar{B}$$

$$f(A, B) = \bar{B} \rightarrow \text{NOT}$$

$$f(\bar{A}, B) = \bar{A} + \bar{B} = \overline{AB} \rightarrow \underline{\text{NAND}}$$

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A\bar{B}$$



$$f(\bar{A}, B) = \bar{B} \quad \text{--- NOT.}$$

$$f(A, \bar{B}) = A\bar{\bar{B}} = AB \rightarrow \text{AND}$$

$$f(\bar{A}, \bar{B}) = \bar{A} \cdot \bar{B} = \overline{A+B} \rightarrow \text{NOR.}$$

functionally complete.

Q) Verify whether the function is functionally complete or not

$$f(A, B) = \underline{A \oplus B}$$

$$f(A, B) = \overline{A}B + A\overline{B}$$

AND  
OR.

$$f(0, 0) = \overline{A}(0) + A\overline{0} = A$$

$$f(1, 0) = \overline{1}B + 1\overline{B} = \overline{B} \rightarrow \text{NOT}$$

$$f(\overline{A}, B) = \overline{\overline{A}}B + \overline{A}\overline{B} = AB + \overline{A}\overline{B} \times$$

$$f(A, \overline{B}) = \overline{A}\overline{B} + A\overline{\overline{B}} = \overline{A}\overline{B} + AB \times$$

functionally incomplete.

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A \odot B$$

$$f(A, B) = \overline{A} \overline{B} + AB.$$

$$f(A, 0) = \overline{A} \overline{0} + A(0) = \overline{A} \rightarrow \text{NOT}.$$

functionally incomplete.

Q) Verify whether the function is functionally complete or not

$$f(x, y, z) = x\bar{y}z + x\bar{y} + \underline{\bar{y}z}$$

$$f(0, y, z) = 0 + 0 + \bar{y}\bar{z} = \overline{\bar{y} + \bar{z}} \rightarrow NOR.$$

functionally Complete

Q) Verify whether the function is functionally complete or not

$$f(x, y, z) = \bar{x}yz + \bar{x}y\bar{z} + xy\bar{z}$$

$$f(1, 1, 1) =$$

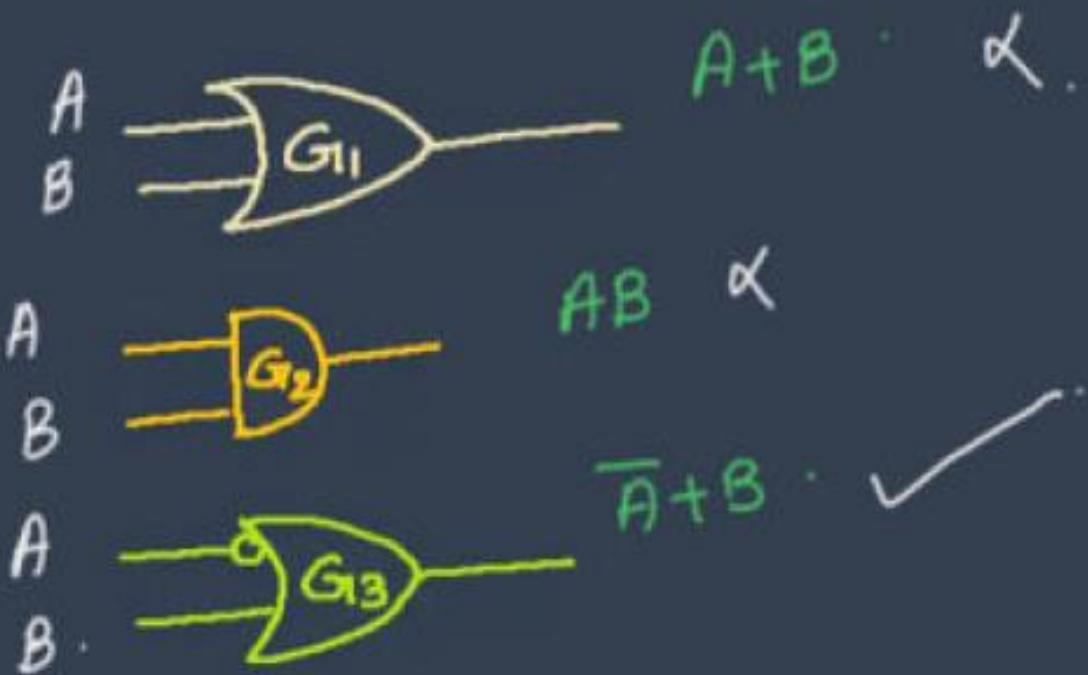
$$f(x, \bar{y}, 0) = \bar{x}\bar{y}(0) + \bar{x}\bar{y}(1) + x\bar{y}$$

$$= 0 + \bar{x}\bar{y} + x\bar{y} = \bar{y} \rightarrow NOT.$$

functionally incomplete

Q) A universal logic gate can implement any boolean function by connecting sufficient number of them appropriately. 3 gates are shown in figure , identify the correct statements.

- a) G1 is a universal gate
- b) G2 is a universal gate
- c) G3 is a universal gate
- d) none



$$f(\bar{A}, B) = \bar{A} + B =$$



unacademy

# DIGITAL CIRCUITS

DPP - 1

The dual of Boolean theorem  $x(y+z) = xy+xz$  is

- (a)  $x + yz = xy + xz$
- (b)  $x(y+z) = (x+y)(x+z)$
- (c)  $\underline{x+yz} = (\underline{x+y})(\underline{x+z})$
- (d) None

Given Boolean theorem  $AB + A'C + BC = AB + A'C$  which of the following is true?

- (a)  $(A+B)(A'+C)(B+C) = (A+B)(A'+C)$  ✓
- (b)  $AB + A' C + BC = AB + BC$
- (c)  $AB + A' C + BC = (A+B)(A'+C)(B+C)$
- (d)  $(A+B)(A'+C)(B+C) = AB + A' C$

$(A' + B' + C')$ ' is equal to

(a)  $A' B' C'$

(b)  $ABC$

(c)  $A+B+C$

(d)  $A'+B'+C'$

$$\overline{(A' + B' + C')} = \underline{\underline{ABC}}.$$

$AB + A' C + BC$  is equivalent to

- (a)  $AB + BC$     (b)  ~~$AB + A' C$~~     (c)  $A' C + BC$     (d)  $AC$

The dual of a Boolean theorem is obtained by

- (a) interchanging all zeros and ones only
- (b) changing all zeros to ones only
- (c) changing all ones to zeros only
- (d) interchanging operators and identity elements

$$\cdot \longleftrightarrow +$$

$$0 \longleftrightarrow 1$$

In Boolean Algebra '1' is called

- (a) Additive identity    (b) Multiplicative identity    (c) Either 1 or 2    (d) None

$$1 \cdot A = A$$

In Boolean Algebra '0' is called

- (a) Additive identity    (b) Multiplicative identity    (c) Both 1 and 2    (d) None

$$A + ( ) = A$$

↳ Additive identity.

$$A \cdot ( ) = A$$

↳ multiplicative identity.

The Boolean expression  $x + x' y$  is equal to

- (a)  $x$

- (b)  ~~$x+y$~~

- (c)  $y$

- (d)  $x + y'$

$$x + y$$

The Boolean expression  $(x+y)(x+z)$  is equal to

- (a)  $x+z$
- (b)  $x+y$
- (c)  ~~$x+yz$~~
- (d)  $y+xz$



If P, Q, R are Boolean variables, then

(GATE-CSIT-08)

$$(P + \bar{Q})(P \cdot \bar{Q} + P \cdot R)(\bar{P} \cdot \bar{R} + \bar{Q})$$

Simplifies to

(A)  $P \cdot \bar{Q}$

(B)  $P \cdot \bar{R}$

(C)  $P \cdot \bar{Q} + R$

(D)  $P \cdot \bar{R} + Q$

$$\underline{(P + \bar{Q})} (\underline{P\bar{Q}} + PR) (\bar{P}\bar{R} + \bar{Q})$$

$$(\underline{P\bar{Q}} + PR + \underline{P\bar{Q}} + P\bar{Q}R) (\bar{P}\bar{R} + \bar{Q})$$

$$\left( P\bar{Q} [1 + R] + PR \right) (\bar{P}\bar{R} + \bar{Q})$$

$$\begin{aligned} & (P\bar{Q} + P \cdot R) (\bar{P}\bar{R} + \bar{Q}) = 0 + P\bar{Q}\bar{R} + 0 + P\bar{Q}R \\ & = \underline{\underline{P\bar{Q}}} [\bar{R} + R] = P\bar{Q} \end{aligned}$$

In the following equations the equals sign means is equal to Which of the following is a positive logic?

- (a)  $0 = 0 \text{ V}$  and  $1 = +5 \text{ V}$  ✓
- (b)  $0 = 0 \text{ V}$  and  $1 = -5 \text{ V}$
- (c)  $0 = +5 \text{ V}$  and  $1 = 0 \text{ V}$
- (d) None of these

The voltage levels for positive logic system

- a) must necessarily be positive
- (c) may be positive or negative

- (b) must necessarily be negative
- (d) must necessarily be 0 V and 5 V

### Positive logic SIm

more +ve value is logic '1'

0V → logic '0'

5V → logic '1'

-10V → logic '0'

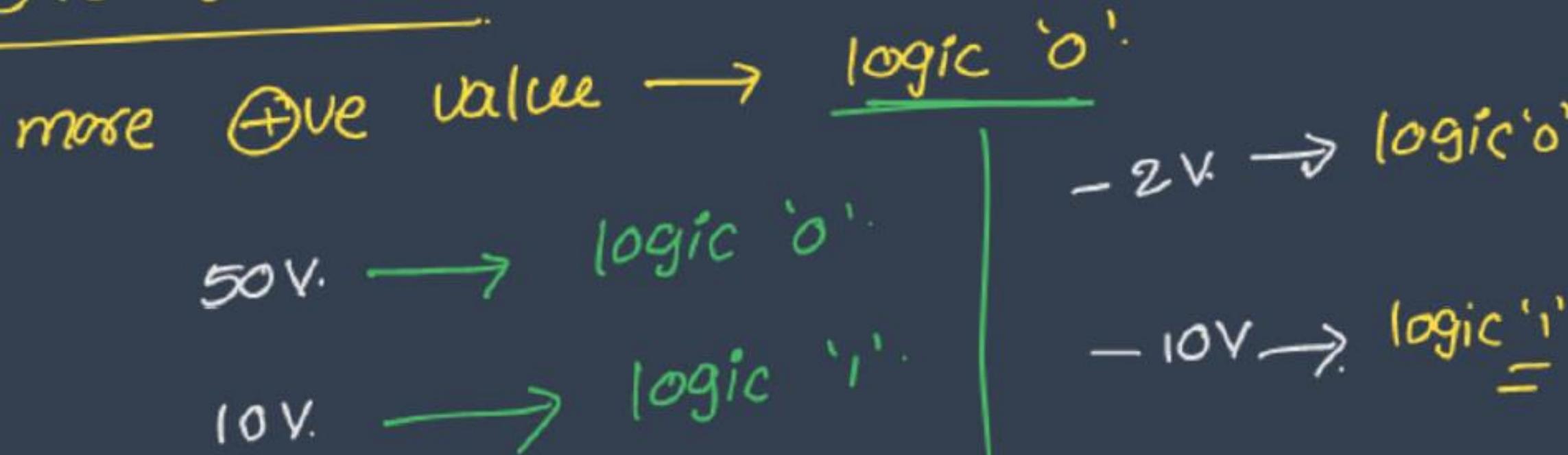
-2V → logic '1'

The voltage levels for negative logic system

- (a) must necessarily be negative ✗  
(c) need not be negative

- (b) must necessarily be positive  
(d) must necessarily be 0 V and -5 V

⊕ve logic S/m



The term  $AB + AC + B\bar{C}$  reduce to  
**(IES-1991)**

- (a)  $AB + CA$
- (b)  $AC + BC$
- (c)  $AC + B\bar{C}$  ✓
- (d)  $AB + \bar{B}\bar{C}$

If X, Y and Z are Boolean variables, then the expression

$$\underline{X(X + XY)} Z (X + Y + Z)$$

(IES-1991)

- (a)  $X + XY$       (b)  $X + Y + Z$   
(c)  $XYZ$       (d)  $XZ$  

$$x \cancel{x}[1 + \cancel{y}] \equiv [x + \cancel{y} + \cancel{z}]$$

$$x \cancel{z} [x + \cancel{y} + \cancel{z}]$$

$$x \cancel{z} + x \cancel{y} \cancel{z} + x \cancel{z}$$

$$x \cancel{z} [1 + \cancel{y} + 1] = x \cancel{z}$$

. What is dual of  $A + [B + (AC)] + D$   
**(IES-1992)**

- (a)  $A + [(B(A + C)] + D$
- (b)  $A[B + AC]D$
- (c)  $A + [B(A + C)]D$
- (d)  $A[B(A + C)]D$  ✓

$$A[B(A + C)]D.$$

What is dual of  $X + \bar{X}Y = X + Y$   
(IES-1992)

- (a)  $X + Y = XY$
- (b)  $\bar{X} + XY = XY$ .
- (c)  $X(\bar{X} + Y) = XY$  ✓
- (d)  $X(\bar{X} + Y) = X + Y$

Which one of the following is the dual form of the Boolean Identity?

$$\bar{A}B + \bar{A}C = (A + C)(\bar{A} + B)?$$

(IES-1996)

(a)  $AB + \bar{A}C = AC + \bar{A}B$

(b)  $(A + B) + (A + C) = (A + C)(A + B)$

(c)  $(\bar{A} + B)(\bar{A} + C) = AC + \bar{A}B$  ✓

(d)  $AB + \bar{A}C = AB + \bar{A}C + BC$

The complement of the Boolean expression  $\overline{AB}(\overline{BC} + \overline{AC})$  is  
(IES-1998)

- (a)  $(\overline{A} + \overline{B}) + (B + \overline{C})(\overline{A} + \overline{C})$
- (b)  $(\overline{A}.\overline{B}) + (B\overline{C} + \overline{A}\overline{C})$
- (c)  $(\overline{A} + \overline{B}).(B + \overline{C})(\overline{A} + \overline{C})$
- (d)  $(A + B).(\overline{B} + C)(A + C)$

$$f = AB(\overline{BC} + \overline{AC})$$

$$f = (\overline{A} + \overline{B}) + (B + \overline{C})(\overline{A} + \overline{C})$$

## The Boolean theorem

$AB + \bar{A}C + BC = AB + \bar{A}C$  corresponds to **(IES-1999)**

- (a)  $(A+B).(\bar{A}+C).(B+C) = (A+B).(\bar{A}+C)$  ✓
- (b)  $AB + \bar{A}C + BC = AB + BC$
- (c)  $AB + \bar{A}C + BC = AB + BC$
- (d)  $(A+B) . (\bar{A} + C).(B+C) = \underline{\underline{AB + \bar{A}C}}$

Which one of the following is equivalent to the Boolean expression  $Y = \overline{AB} + \overline{BC} + \overline{CA}$ ?

(IES-2001)

- (a)  $\overline{AB} + BC + CA$
- (b)  $(\overline{A} + \overline{B})(B + \overline{C})(\overline{A} + \overline{C})$
- (c)  $(A + B)(B + C)(C + A)$  ✓
- (d)  $\overline{(A + B)}(B + C)(C + A)$

$$\overline{(A+B)} + \overline{(B+C)} + \overline{(C+A)}$$
$$\overline{AB} + \overline{BC} + \overline{CA}$$

Consider the Boolean expression

$$X = ABCD + A\bar{B}CD +$$

$$\bar{A}CB\bar{D} + \bar{A}BCD$$

The simplified form of X is

(IES-2002)

- (a)  $\bar{C} + \bar{D}$
- (b)  $BC$
- (c)  $CD$
- (d)  $BC$

$$X = ABCD + A\bar{B}CD + \bar{A}CB\bar{D} + \bar{A}BCD.$$

$$X = CD \left[ \underline{AB + A\bar{B}} + \underline{\bar{A}\bar{B} + \bar{A}B} \right]$$

$$= CD [A + \bar{A}] = CD //.$$

The Boolean expression

$$(\bar{A}+B)(A+\bar{C})(B+\bar{C})$$

(IES-2003)

- Simplifies to
- (a)  $(A+B)\bar{C}$
  - (b)  $(A+\bar{B})\bar{C}$
  - (c)  $(\bar{A}+B)\bar{C}$
  - (d)  $(\bar{A}+\bar{B})\bar{C}$

T1  
13 + 24.

$$\neq = (\bar{A}+B) \underline{(\bar{C}+A)} (\bar{C}+\bar{B})$$

$$= (\bar{A}+B) (\bar{C} + A\bar{B})$$

$$= \bar{A}\bar{C} + B\bar{C} + 0$$

$$= \bar{C}(\bar{A}+B)$$

The Boolean function  $(x+y)(\bar{x}+z)(y+z)$  is equal to which one of the following expressions?

(IES-2005)

- (a)  $(x+y)(y+z)$
- (b)  $(\bar{x}+z)(y+z)$
- (c)  $(x+y)(\bar{x}+z)$
- (d)  $(x+y)(y+\bar{z})$

$$AB + \overline{A} C = (A+C)(\overline{A} + B) \dots$$

Which one of the following is the dual form of the Boolean identity given above?  
**(IES-2005)**

- (a)  $AB + \overline{A} C = AC + \overline{A} B$
- (b)  $(A+B)(\overline{A} + C) = (A+C)(\overline{A} + B)$
- (c)  $(A+B)(\overline{A} + C) = AC + \overline{A} B$  ✓
- (d)  $\overline{AB} + \overline{A} \overline{C} = AB + \overline{A} C + BC$

What does the Boolean expression  $AD + ABCD + ACD + \bar{A}B + \bar{A}\bar{B}$  on minimization result into?  
**(IES-2006)**

- (a)  $A+D$
- (b)  $AD+\bar{A}$  ✗
- (c)  $AD$
- (d)  $\bar{A}+D$  ✓

$$AD[1 + BC + C] + \bar{A}[B + \bar{B}]$$

$$\frac{AD + \bar{A}}{(\bar{A} + A)(\bar{A} + D)} = \underbrace{\bar{A} + D}_{=}$$

If A and B are Boolean variables, then what is  $(A+B).(A+\bar{B})$  equal to?

**(IES-2006)**

- (a) B
- ~~(b) A~~
- (c) A+B
- (d) AB

A

The Boolean function  $A+BC$  is a reduced form of which one of the following  
**(IES-2008)**

- (a)  $AB+BC$
- (b)  $\bar{A}B+A\bar{B}C$
- (c)  $(A+B).(A+C)$
- (d) None of the above

.. Which one of the following statements is not correct?

(IES-2008)

- (a)  $X + \bar{X} Y = X$
- (b)  $X(\bar{X} + Y) = XY$
- (c)  $XY + X\bar{Y} = X$
- (d)  $ZX + Z\bar{X} Y = ZX + ZY$

Which of the following Boolean algebra rules is correct? (IES-2009)

- (a)  $A \cdot \bar{A} = 1$  ✗
- (b)  $A + AB = A + AB$  ✓
- (c)  $A + \bar{A}B = AB$  ✗
- (d)  $\underline{A(A+B)} = B$  ✗

$A + B$

The Boolean expression

$$\overline{A + \overline{B} + C} + \overline{\overline{A} + \overline{B} + C} + \overline{A + \overline{B} + \overline{C}} + ABC$$

reduces to: (IES-2009)

- (a) A
- (b) B ✓
- (c) C
- (d)  $A + B + C$

$$\overbrace{\overline{ABC} + AB\overline{C} + \overline{ABC} + ABC}^{\overline{BC} + BC} = B.$$

The complement of the expression  $Y = ABC + A\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + \bar{A}BC$  is:  
**(IES-2010)**

- (a)  $(A + \bar{B})(A + \bar{C})$
- (b)  $(\bar{A} + B)(A + C)$
- (c)  $(A + \bar{B})(\bar{A} + C)$
- (d)  $(\bar{A} + \bar{B})(A + \bar{C})$  ✓

$$Y = AB + \bar{A}\bar{C}$$
$$\overline{Y} = (\bar{A} + \bar{B})(A + \bar{C})$$

The logic function  $f = \overline{x}.\overline{y} + \overline{x}.y$  is the same as (IES-2011)

- (a)  $f = (x + y)(\overline{x} + \overline{y})$
- (b)  $f = \overline{(\overline{x} + \overline{y})(x + y)}$
- (c)  $f = (x.y)(\overline{x}.\overline{y})$
- (d) None of the above

$$\begin{aligned}f &= (\overline{x} + y)(x + \overline{y}) \\&= \overline{x}\overline{y} + xy.\end{aligned}$$

If the Boolean expression  $\overline{PQ} + QR + \overline{PR}$  is minimized, the expression becomes :  
**(IES-2011)**

- (a)  $\overline{PQ} + QR$
- (b)  $\overline{PQ} + PR$
- (c)  $QR + PR$
- (d)  $\overline{PQ} + QR + PR$

In the negative logic system,

(IES-2001)

- (a) the more negative of the two logic levels represents a logic '1' state. ✓
- (b) the more negative of the two logic levels represents a logic '0' state.
- (c) all input and output voltage levels are negative.
- (d) the output is always complement of the intended logic function.



The Boolean equation

$X = [(A + \bar{B})(B + C)]B$  can be simplified to  
(IES-2012)

- (a)  $X = \bar{A}B$
- (b)  $X = A\bar{B}$
- (c)  $X = AB$  ✓
- (d)  $X = \bar{A}\bar{B}$

$$X = (\bar{B} + A)(B + C)B.$$

$$X = (\bar{B}C + AB)B.$$

$$= 0 + AB.$$

The correct expression is (IES-2012)

- (a)  $\overline{A}B + A\overline{B} = \overline{AB}(A + B)$
- (b)  $\overline{AB} + \overline{AB} = AB(\overline{A} + \overline{B})$
- (c)  $\overline{AB} + A\overline{B} = AB(\overline{A} + \overline{B})$
- (d)  $\overline{AB} + \overline{AB} = \overline{AB}(A + B)$

Simplified form of the logic expression  $(A + \overline{B} + C)(A + \overline{B} + \overline{C})(A + B + C)$  is  
**(IES-2012)**

- (a)  $\overline{A}\overline{B} + \overline{C}$
- (b)  $A + \overline{B}C$
- (c)  $A$
- (d)  $AB + \overline{C}$

Logic function  $(\bar{A} + B)(A + \bar{B})$  can be reduced to :

(IES-2013)

- (a) B
- (b)  $\bar{B}$
- (c) A
- (d)  $\bar{A}$

Logic function  $A\bar{B}D + A\bar{B}\bar{D}$  can be reduced to :

(IES-2013)

- (a)  $\bar{A}\bar{B}$
- (b)  $A\bar{B}$
- (c)  $\bar{B}\bar{D}$
- (d)  $A\bar{D}$

The logic function

$f(A, B, C, D) = (\bar{A} + BC)(B + CD)$  can be  
expressed to : (IES-2013)

- (a)  $\bar{A}B + BC + \bar{A}CD + BCD$  ✓
- (b)  $AB + A\bar{B} + A\bar{C}D + BCD$
- (c)  $AB + \bar{A}\bar{B} + \bar{A}CD + B\bar{C}D$
- (d)  $A\bar{B} + \bar{A}B + \bar{A}CD + BCD$

$$f = \bar{A}B + \bar{A}CD + BC + BCD.$$

The simplified form of the Boolean expression  $AB + A(B + C) + B(B + C)$  is given by

(IES - 2016)

- (a)  $AB + AC$
- (b)  $B + AC$
- (c)  $BC + AC$
- (d)  $AB + C$

$$\begin{aligned}f &= AB + AB + AC + B + BC \\&= AB + AC + BC + B \\&= B[A + C + 1] + AC \\&= B + AC.\end{aligned}$$

Simplified form of the Boolean expression

$$Y = \overline{(A \cdot B + \bar{C})}(\overline{A + B + C}) \text{ is } (\text{IES - 2016})$$

(a)  $\bar{A}\bar{C} + A\bar{C} + \bar{B}\bar{C} + \bar{B}C$

(b)  $(\bar{A} + \bar{B} + \bar{C})(A + B + C)$  ✓

(c)  $(\bar{A} + \bar{B})(A + \bar{C})$

(d)  $A(B+C)$

$$\overline{A+B} = \overline{A}\overline{B}$$

$$Y = \overline{(AB + \bar{C})}(\overline{A}\overline{B} + C)$$

$$= ABC + \bar{A}\bar{B}\bar{C}$$

$$Y = (\bar{A} + \bar{B} + \bar{C})(A + B + C)$$

Four logical expressions are given below:

$$1. \overline{A}.\overline{B}.\overline{C}.\overline{D}.\overline{E}.\overline{F}.\overline{G}.\overline{H}$$

$$2. \overline{AB}.CD.EF.GH$$

$$3. \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E} + \overline{F} + \overline{G} + \overline{H}$$

$$4. (\overline{A} + \overline{B})(\overline{C} + \overline{D})(\overline{E} + \overline{F})(\overline{G} + \overline{H})$$

Two of these expressions are equal. They  
are

(IES-96)

- (a) 1 and 2
- (b) 3 and 4
- (c) 1 and 3
- (d) 2 and 4

The expression  $(X+Y)(X+\bar{Y})(\bar{X}+Y)$  is equivalent to

**(IES-98)**

- (a)  $\bar{X}\bar{Y}$
- (b)  $\bar{X}Y$
- (c)  $X\bar{Y}$
- (d)  $XY$

In Boolean algebra, if  $F = (A + B)(\bar{A} + C)$ ,  
then

(IES-01)

- (a)  $F = AB + \bar{A}C$
- (b)  $F = AB + \bar{A}\bar{B}$
- (c)  $F = AC + \bar{A}B$
- (d)  $F = A\bar{A} + \bar{A}B$

The simplified form of a logic function  $Y =$

$$\overline{(A\bar{B})(\bar{A}B)} \text{ is } \quad \text{(IES-03)}$$

- (a)  $A + B$
- (b)  $AB$
- (c)  $\bar{A} + \bar{B}$
- (d)  $\bar{A}B + A\bar{B}$

The reduced form of the Boolean expression  
 $A[B + C(\overline{AB} + \overline{AC})]$  is (IES-03)

- (a)  $\overline{A}B$       (b)  $A\overline{B}$   
(c)  $AB$  ✓      (d)  $AB + B\overline{C}$

$$\begin{aligned}f &= A \left[ B + C \left( (\overline{A} + \overline{B})(\overline{A} + \overline{C}) \right) \right] \\&= A \left[ B + C \left( \overline{A} + \overline{B}\overline{C} \right) \right] \quad AB \\&= A \left[ B + \overline{A}C + \overline{J} \right]\end{aligned}$$

The function

$F = ABC + ABC + \bar{A}BC + \bar{A}\bar{B}\bar{C}$ ; can be  
reduced to which one of the following?

(IES-07)

- (a)  $F = A$
- (b)  $F = AB$
- (c)  $F = ABC$
- (d)  $F = B$

$$F = B \left[ A\bar{C} + AC + \bar{A}C + \bar{A}\bar{C} \right]$$

$$F = B$$

What is the simplified form of the Boolean expression  $(A \oplus B) \oplus C$ ? (IES-08)

$$T = (X + Y)(X + \bar{Y})(\bar{X} + Y)$$

- (c) XY ✓

$$T = (x + o)(\bar{x} + y)$$

$$T = x \cdot y.$$

The Boolean expression  $A \cdot B + \overline{A} \cdot \overline{B}$   
is logically equivalent to which of the  
following? (IES-08)

- (a)  $(A + \overline{B}) \cdot (\overline{A} + B)$    (b)  $(\overline{A} + \overline{B}) \cdot (A + B)$   
(c)  $\overline{(A + \overline{B}) \cdot (\overline{A} + B)}$    (d)  $\overline{(A + B)} \cdot \overline{(\overline{A} + \overline{B})}$

$$AB + \overline{A} \overline{B}$$

$$(A + \overline{B})(\overline{A} + B)$$

# DIGITAL CIRCUITS

DPP - 2

A switching function  $f(A,B,C,D) = A'B'CD + A'BC'D + A'BCD + AB'C'D + AB'CD$  can also be written as

- (a)  $\Sigma m(1,3,5,7,9)$  (b)  ~~$\Sigma m(3,5,7,9,11)$~~  (c)  $\Sigma m(3,5,9,11,13)$  (d)  $\Sigma m(5,7,9,11,13)$

$$f = \Sigma m(3, 5, 7, 8, 11)$$

The switching function  $f(A,B,C,D) = \Sigma m(5,9,11,14)$  can be written as

- (a)  $A' B C' D + A B' C' D + A B' C D + A B C D'$  ✓ (b)  $A' B' C' D + A B' C' D + A' B' C D + A B C D'$   
(c)  $A' B C' D + A' B C' D' + A B' C D' + A B C D$  (d) None

$$f = \overline{A} B \overline{C} D + A \overline{B} \overline{C} D + A \overline{B} C D + A B C \overline{D}$$

The switching function  $f(A,B,C) = (A+B'+C)(A'+B+C)(A+B'+C')$  can also be written as  
 (a)  $\Sigma m(2,3,6)$     (b)  $\Sigma m(0,1,4,5,7)$     (c)  $\Sigma m(1,2,5,6,7)$     (d)  $\Sigma m(0,2,4,6)$

$$f = \text{LCM}(2, 3, 6)$$

$$f = \sum m (0, 1, 4, 5, 7) \equiv$$

The other canonical form of  $f(A,B,C) = \Sigma m(0,1,5,7)$  is

- (a)  $\Pi M(2,3,4,6)$       (b)  $\Pi M(2,4,6,8)$       (c)  $\Pi M(2,5,6,7)$       (d)  $\Pi M(1,3,5,7)$

$$f = \Pi M (2, 3, 4, 6)$$

If a three variable switching function is expressed as the product of maxterms by  $f(A,B,C) = \prod M(0,3,5,6)$  then it can also be expressed as the sum of minterms by

- (a)  $\sum m(0,3,5,6)$       (b)  $\prod M(1,2,4,7)$       (c)  ~~$\sum m(1,2,4,7)$~~       (d)  $\prod M(1,2,4,7)$

The logic expression  $F = XY + XZ' + YZ$  is known as

- (a) SSOP form
- (b) SOP form
- (c) POS form
- (d) SPOS form

The logic expression  $F = (\underline{x+y+z})(\underline{x+y'})(\underline{y+z'})(\underline{x+z})$  is known as

(a) SOP form

(b) SSOP form

(c) SPOS form

(d) POS form

SSOP

The logic expression  $F = \Sigma m(0,3,6,7,10,12,15)$  is equivalent to

- (a)  $F = \prod M(0,3,6,7,10,12,15)$
- (c)  $F = \Sigma m(0,1,5,6,7,12,15)$

- (b)  ~~$F = \prod M(1,2,4,5,8,9,11,13,14)$~~
- (d)  $F = \Sigma m(1,2,4,5,8,9,11,13,14)$

A literal in Boolean algebra is a

- (a) Primed or unprimed Boolean variable ✓
- (b) Primed Boolean variable only
- (c) Unprimed Boolean variable only
- (d) None

$$A \quad (\alpha) \quad \overline{A}$$

Identify number of literals in the given Boolean function  $F = x'yz + xyz + xy'z$

(a) 5

(b) 4

(c) 3

(d) 6

$$x \cdot \bar{x} \rightarrow ①$$

A minterm is nothing but

- (a) Standard sum term
- (c) May be standard sum term or product term

- (b) Standard product term
- (d) None

$$F = \underline{\textcolor{orange}{xyz}} + \textcolor{orange}{x\bar{y}z} + \textcolor{orange}{\bar{x}\bar{y}z}$$

$xyz$

A maxterm is nothing but a

- (a) Standard sum term ✓
- (c) May be standard sum term or product term

- (b) Standard product term
- (d) None

$$f = \underbrace{(\bar{x} + y + z)}_{\downarrow} (x + \bar{y} + \bar{z})$$

The Boolean function expressed in standard sum of products form or standard product of sums form is called

- (a) Canonical form
- (b) Conical form
- (c) Both 1 and 2
- (d) None

Let \* be defined as  $x * y = \bar{x} + y$ . Let  $z = x * y$ . Value of  $z * x$  is

(GATE-CSIT-97)

(a)  $\bar{x} + y$

(b)  $x$

(c) 0

(d) 1

$$x * y = \bar{x} + y.$$

$$z = x * y.$$

$$\begin{aligned} z * x &= \bar{z} + x \\ &= \overline{(x * y)} + x \\ &= \overline{\bar{x} + y} + x \\ &= x\bar{y} + x = x. \end{aligned}$$

$$z * x =$$

The minterm expansion of  $f(P,Q,R) = PQ + Q\bar{R} + P\bar{R}$  is (GATE-CSIT-10)

- (A)  $m_2 + m_4 + m_6 + m_7$  ✓  
(C)  $m_0 + m_1 + m_6 + m_7$

- (B)  $m_0 + m_1 + m_3 + m_5$   
(D)  $m_2 + m_3 + m_4 + m_5$

$$PQ + Q\bar{R} + P\bar{R}$$

110	010	100
111	110	110

The number of input words in a truth table always equals ---- where 'n' is the number of input bits

- (a)  $2n$       (b)  $2n+1$       (c)  $2(n+1)$       (d)  $2^n$

$$\underbrace{2}_{\text{---}}^n.$$

The number of Boolean functions which can be generated with four variables is  
**(IES-1992)**

- (a) 4
- (b) 16
- (c) 256
- (d) 65,536

$$2^{2^n} = 2^{2^4} = 2^{16} = (2^6)(2^{10}) \\ = 64 \cdot (1024)$$

The number of switching functions of 3 variables is

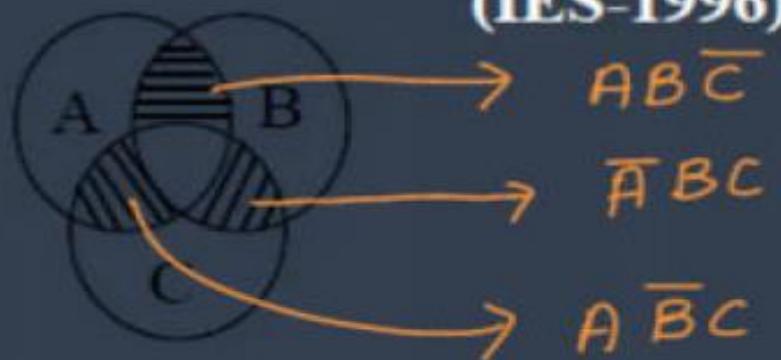
(IES-1993)

- (a) 8
- (b) 64
- (c) 128
- (d) 256 ✓

$$2^{2^3} = 2^8.$$

The Boolean expression for the shaded area in the given Venn diagram is

(IES-1996)



(a)  $AB + BC + CA$

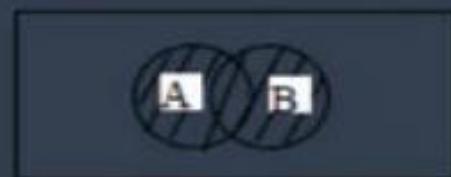
(b)  $AB\bar{C} + \bar{A}BC + A\bar{B}C$  ✓

(d)  $\bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$

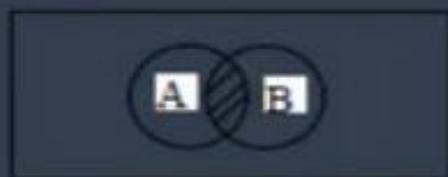
(c)  $ABC + \bar{A}\bar{B}\bar{C}$

The Venn diagram representing the Boolean expression  $A + (\bar{A}B)$  is  
**(IES-1998)**

(a) ✓



(b)



$$A + B$$

(c)



(d)



With 4 Boolean variables, how many Boolean expressions can be formed?

(IES – 2002)

- (a) 16
- (b) 256
- (c) 1024(1k)
- (d) 64K( $64 \times 1024$ )

The Boolean functions can be expressed in canonical SOP(Sum of products) and POS (product of sums) form. For the functions,  
two forms (IES-2008)

- (a)  $Y = \sum(1, 2, 6, 7)$  and  $Y = \prod(0, 2, 4)$
- (b)  ~~$Y = \sum(1, 4, 5, 6, 7)$  and  $Y = \prod(0, 2, 3)$~~
- (c)  $Y = \sum(1, 2, 5, 6, 7)$  and  $Y = \prod(0, 1, 3)$
- (d)  $Y = \sum(1, 2, 4, 5, 6, 7)$  and  
 $Y = \prod(0, 2, 3, 4)$

$$Y = A + \overline{B} C, \text{ Which are such}$$

$$Y = A + \overline{B} C.$$

1	00	001
1	01	101
1	10	
1	11	

Product of Max terms representation for the

Boolean function  $F = \overline{BD} + \overline{AD} + BD$  is  $\rightarrow$

$$\begin{array}{c|cc} 001 & 001 \\ 101 & 011 \end{array} \text{(IES - 2016)}$$

- (a)  $\prod M(1, 3, 5, 7)$
- (c)  $\prod M(0, 1, 2, 3)$

- (b)  $\prod M(0, 2, 4, 6)$
- (d)  $\prod M(4, 5, 6, 7)$

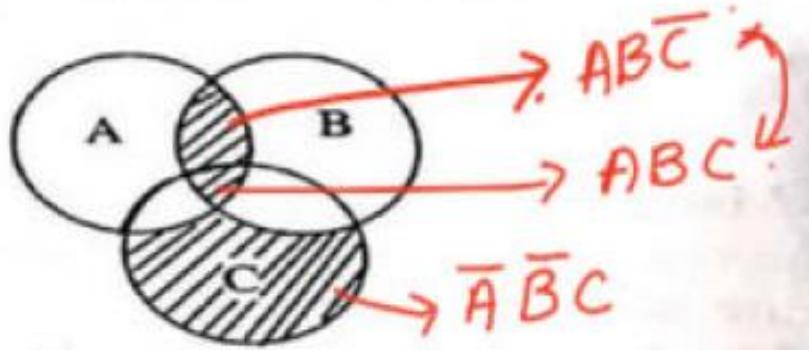
$$f(A, B, D) = \sum m(1, 3, 5, 7)$$

$$f(A, B, D) = \prod M(0, 2, 4, 6)$$

What is the function  $Y = A + \overline{B}C$  in Product-of-Sums (POS) form? (IES - 2016)

- (a)  $M_6 M_5 M_4 M_3$
- (b)  $M_3 M_2 M_1 M_0$
- (c)  $M_0 M_2 M_3$  ✓
- (d)  $M_4 M_3 M_2 M_1$

The Boolean expression for the shaded area in the Venn diagram shown is: (IES-11)



- (a)  $A + \bar{B} + C$       (b)  $AB + \bar{A} BC$   
(c)  $A \bar{B} C + \bar{A} BC$     (d)  $AB + \bar{A} \bar{B} C$

$$f = ABC\bar{C} + ABC + A\bar{B}\bar{C}$$

$$f = AB + A\bar{B}\bar{C}$$

Represent the Boolean expression  $F(A, B, C) = \Pi(\underline{0}, \underline{2}, \underline{4}, \underline{5})$  is standard POS Form.

$$F = (A + B + C) \quad (A + \bar{B} + C) \quad (\bar{A} + B + C) \quad (\bar{A} + \bar{B} + C)$$

Convert the following Boolean function into standard SOP and express it in terms of minterms.

$$Y(A, B, C) = AB + A\bar{C} + BC$$

110	100	011
111	110	111

$$Y = \Sigma m(3, 4, 6, 7)$$

$$Y = \bar{A}BC + A\bar{B}\bar{C} + A\bar{B}\bar{C} + ABC .$$

$$Y = AB\underline{(C + \bar{C})} + A(CB + \bar{B})\bar{C} + (A + \bar{A})BC .$$

Convert the following Boolean function into standard POS and express it in terms of maxterms.

$$f(A, B, C) = (A + B)(B + \overline{C})(A + C)$$

$$f(A, B, C) = \overline{(A + B + C)} \cdot \overline{(A + B + \overline{C})} \cdot \overline{(A + \overline{B} + C)}$$

$$= \pi M (0, 1, 5, 2)$$

Convert the following SOP expression to an equivalent POS expression.

$$f(A, B, C) = \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} C + \overline{A} B C + A \overline{B} C + A B C$$

$$f(A, B, C) = \sum m (0, 1, 3, 5, 7)$$

$$f(A, B, C) = \pi M (2, 4, 6)$$

$$f(A, B, C) = (A + \overline{B} + C) (\overline{A} + B + C) (\overline{A} + \overline{B} + C)$$

For the Boolean function  $F$  given in the truth table, find the following:

- (a) List the minterms of the function. ✓
- (b) List the minterms of  $F'$  ✓
- (c) Express  $F$  in sum of minterms in algebraic form.
- (d) Simplify the function to an expression with a minimum number of literals.

x	y	z	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

$$f = \sum m (2, 3, 6, 7)$$

$$F' = \sum m (0, 1, 4, 5)$$

$$f = \overline{x}y\bar{z} + \overline{x}yz + xy\bar{z} + xyz$$

$$f = \overline{x}y + yz + \underline{xy}$$

$$f = y$$

Express the following functions in sum of minterms and product of maxterms:

(a)  $F(A, B, C, D) = \overline{B}D + \overline{A}D + BD$

(b)  $F(x, y, z) = \underline{(xy + z)(xz + y)}$

$$f(A, B, C, D) = \overline{B}D + \overline{A}D + BD.$$

1	0001	0001	0101	5
3	0010	0010	0110	7
9	1001	0101	1101	13
11	1011	0111	1111	15

Express the complement of the following functions in sum of minterms:

(a)  $F(A, B, C, D) = \Sigma(0, 2, 6, 11, 13, 14)$

(b)  $F(x, y, z) = \Pi(0, 3, 6, 7)$

Convert the following to the other canonical form:

(a)  $F(x, y, z) = \Sigma(1, 3, 7)$

(b)  $F(A, B, C, D) = \Pi(0, 1, 2, 3, 4, 6, 12)$

The simplified expressions for Boolean function  $T_1$  &  $T_2$  respectively from the table given below are

A	B	C	$T_1$	$T_2$
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

- (a)  $\overline{A} + \overline{B}\overline{C}$ ,  $AB + AC$   
 (c)  $AB + C$ ,  $AB + AC$

- (b)  $\overline{AB} + \overline{AC}$ ,  $A + BC$  ✓  
 (d)  $A(B + C)$ ,  $AB + AC$

$$T_1 = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C}$$

$$T_1 = \overline{A}\overline{B} + \overline{A}\overline{C}$$

$$T_2 = \overline{A}BC + A\overline{B}\overline{C} + A\overline{B}C + A\overline{B}\overline{C} + ABC$$

$$T_2 = A + BC$$

What values of A, B, C and D satisfy the following simultaneous Boolean equations?

$$\bar{A} + AB = 0, AB = AC, AB + A\bar{C} + CD = \bar{CD}$$

(A) A=1, B=0, C=0, D=1 ✓

(B) A=1, B=1, C=0, D=0 ✗

(C) A=1, B=0, C=1, D=1 ✗

(D) A=1, B=0, C=0, D=0 ✓

[1995, 2 Marks]

$$\bar{A} + AB = 0$$

$$\bar{A} + B = 0$$

$$AB = AC$$

$$\boxed{B = C}$$

$$\overline{AB} + A\bar{C} + CD = \bar{C} + \bar{D}$$

$$0 + 1 + 0 = \bar{D} = 1.$$

$$0 \neq 0$$

$$0 + 1(1) + 0 = \bar{0} = 1.$$

Let \* be defined as  $x^*y = \bar{x} + y$ . Let  $z = x^*y$ .

value of  $z^*x$  is

- (A)  $\bar{x} + y$     (B)  ~~$x$~~     (C) 0    (D) 1

[1997, 2 Marks]

The simultaneous equations on the Boolean variables x, y, z and w, have the following solution for x, y, z and w, respectively:

$$\underline{x + y + z = 1}$$

$$\underline{xy = 0}$$

$$\textcircled{xz + w = 1}$$

$$xy + \bar{z} \bar{w} = 0$$

(A) 0 1 0 0 ✗

(B) 1 1 0 1 ✗

(C) 1 0 1 1 ✓

(D) 1 0 0 0 ✗

[2000, 2 Marks]

$$0 + 0 = 1$$

$$1 + 1 = 1$$

$$0 + 0$$

Let  $f(A,B) = A' + B$ . Simplified expression for function  $f(f(x+y, y), z)$  is

- (A)  $x' + z$
- (B)  $xyz$
- (C)  $xy' + z$
- (D) None of these

*[2002, 2 Marks]*

The Boolean function  $x'y' + \cancel{xy} + x'y$  is equivalent to

- (A)  $x' + y'$       (B)  $x + y$   
(C)  $x + y'$       (D)  $x' + y$

[2004, 1 Mark]

$$\underline{\underline{y + \bar{x}}}$$

The switching expression corresponding to  
 $f(A,B,C,D) = \sum(1, 4, 5, 9, 11, 12)$  is

- (A)  $BC'D' + A'C'D + AB'D$
- (B)  $ABC' + ACD + B'C'D$
- (C)  $ACD' + A'BC' + AC'D'$
- (D)  $A'BD + ACD' + BCD'$

*[2005, 1 Mark]*

Let  $f(w, x, y, z) = \sum(0, 4, 5, 7, 8, 9, 13, 15)$ .

Which of the following expressions are NOT equivalent to  $f$ ?

P.  $x'y'z' + w'xy' + wy'z + xz$

Q.  $w'y'z' + wx'y' + xz$

R.  $w'y'z' + wx'y' + xyz + xy'z$

S.  $x'y'z' + wx'y' + w'y$

(A) P only                    (B) Q and S

(C) R and S                    (D) S only

*[2007, 2 Marks]*

The minterm expansion of f

$(P, Q, R) PQ + Q\bar{R} + P\bar{R}$  is \_\_\_\_\_.

- (A)  $m_2 + m_4 + m_6 + m_7$
- (B)  $m_0 + m_1 + m_3 + m_5$
- (C)  $m_0 + m_1 + m_6 + m_7$
- (D)  $m_2 + m_3 + m_4 + m_5$

*[2010, 1 Mark]*

If P, Q, R are Boolean variables, then

$$(P + \bar{Q})(P\bar{Q} + P.R)(\bar{P}.R + \bar{Q})$$

Simplifies to

- (A)  $P\bar{Q}$       (B)  $P\bar{R}$   
(C)  $P\bar{Q} + R$       (D)  $P\bar{R} + Q$

[2008, 1 Mark]

The simplified SOP (Sum of Product) form of the Boolean expression.

$$(P + \overline{Q} + \overline{R})(P + \overline{Q} + R)(P + Q + \overline{R})$$

- (A)  $(\overline{P}Q + \overline{R})$       (B)  $P + \overline{Q}\overline{R}$   
(C)  $(\overline{P}Q + R)$       (D)  $(PQ + R)$

*[2011, 1 Mark]*

The truth table

X	Y	f(X,Y)
0	0	0
0	1	0
1	0	1
1	1	1

Represents the Boolean function

- (A)  $X$
- (B)  $X + Y$
- (C)  $X \oplus Y$
- (D)  $Y$

$$x\bar{y} + xy = x$$

[2012, 1 Mark]

The dual of a Boolean function  $F(x_1, x_2, \dots, x_n, +, \dots)$ , written as  $F^D$ , is the same expression as that of  $F$  with  $+$  and  $\cdot$  swapped.  $F$  is said to be self-dual if  $F = F^D$ . The number of self-dual functions with  $n$  Boolean variables is

- (A)  $2^n$       (B)  $2^{n-1}$       (C)  $2^{2^n}$       (D)  ~~$2^{2^{n-1}}$~~

[2014, 1 Mark]

$$2^{2^{n-1}}$$

Consider the following Boolean expression for  $F$ :

$$F(P, Q, R, S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$$

The minimal sum-of-products form of  $F$  is

- (A) ~~PQ + QR + QS~~      (B)  $P + Q + R + S$   
(C)  $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$       (D)  $\bar{P}R + \bar{P}RS + P$

$$\begin{aligned} F &= Q \left( P + \bar{P}R + \bar{P}\bar{R}S \right) \\ &= Q \left[ P + \bar{P} \left[ R + S \right] \right] \\ &= P\bar{Q} + R\bar{Q} + S\bar{Q}. \end{aligned}$$

The number of min-terms after minimizing the following Boolean expression is \_\_\_\_\_.

$$[D' + AB' + A'C + AC'D + A'C'D]' = \underline{\underline{ABCD}}$$

1

[2015, 2Marks]

$$[\overline{D} + A\overline{B} + \overline{A}C + A\overline{C}D + \overline{A}\overline{C}D]$$

$$[\overline{D} + A\overline{B} + \overline{A}C + \overline{C}D]$$

$$[\overline{D} + \overline{C} + \overline{A}C + A\overline{B}]$$

$$[\overline{D} + \overline{C} + \overline{A} + A\overline{B}]$$

$$\frac{[\overline{D} + \overline{C} + \overline{A} + A\overline{B}]}{[\overline{D} + \overline{C} + \overline{A} + \overline{B}]}$$

ABCD.

Consider the Boolean operator # with the following properties:

$$x \# 0 = x, x \# 1 = \bar{x}, x \# x = 0 \text{ and } x \#\bar{x} = 1.$$

Then  $x \# y$  is equivalent to

- (A)  $x\bar{y} + \bar{x}y$
- (B)  $x\bar{y} + \bar{x}\bar{y}$
- (C)  $\bar{x}y + xy$
- (D)  $xy + \bar{x}\bar{y}$

*[2016, 1 Mark]*

If w, x, y, z are Boolean variables, then which one of the following is INCORRECT?

- (A)  $wx + w(x + y) + x(x + y) = x + wy$
- (B)  $\overline{wx}(\overline{y} + \overline{z}) + \overline{wx} = \overline{w} + x + \overline{yz}$
- (C)  $(\overline{wx}(\overline{y} + \overline{x}\overline{z}) + \overline{wx})y = x\overline{y}$
- (D)  $(w+y)(wxy + wyz) = wxy + wyz$

*[2017, 2 Marks]*

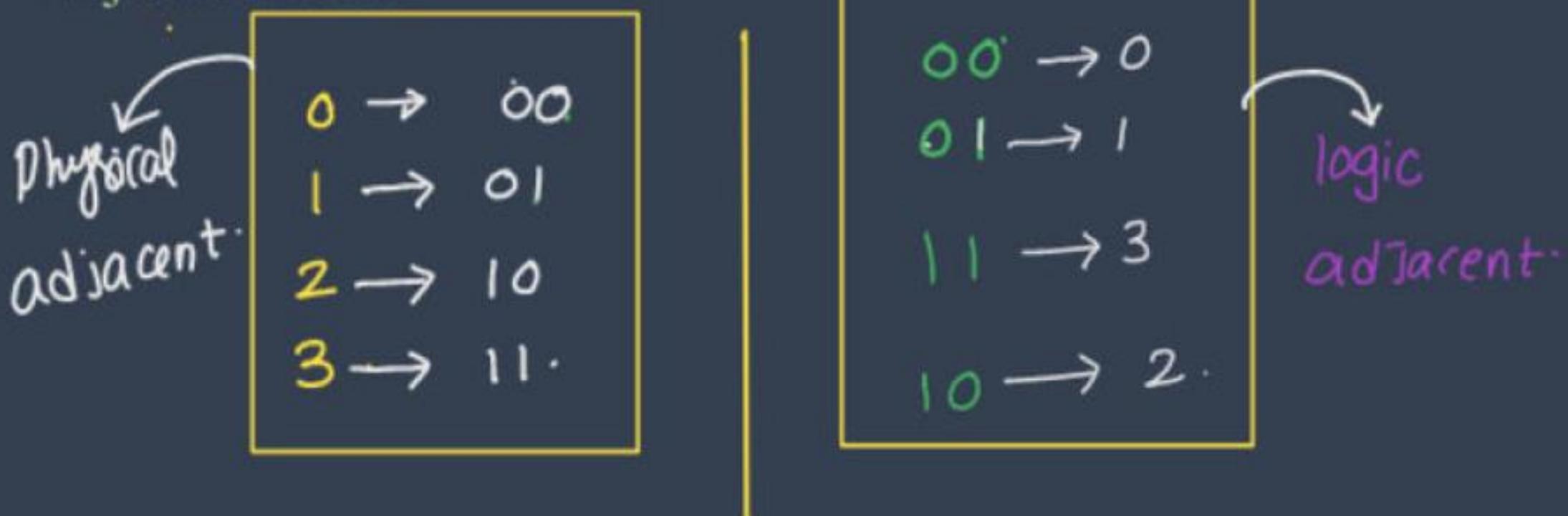
# Karnaugh Map(K- Map)

# K- Map

- It is a graphical technique to minimize the Boolean expressions, that may contain don't care combinations.
- K- map is a systematic method and suitable up to 5 variables .
- Gray code is used to formulate K-map, the minimization is based on the gray code property i.e. *Logical Adjacency*.
- K- map technique is used in 2 format's
  - 1.If we need the answer in SOP form , then the K-map is used in minterm mode
  - 2.If we need the answer in POS form ,then the K- map is used in Maxterm mode

# Logical Adjacency

- Two cells are said to be logical adjacent to each other , if there is only one bit change between them .
- For a n-variable K -map , for every cell there are ‘ n ‘ logical adjacent cells.



## 2- Variable K- Map

### Minterm mode

		B	O	I
		A	0	1
		$\bar{A}$	0	1
00	$\bar{A}\bar{B}$	1	0	1
01	$\bar{A}B$	1	0	1
10	$A\bar{B}$	1	0	1
11	$AB$	1	0	1

### Minterm mode

		$\bar{A}$	A	
		0	1	
		$\bar{B}$	0	1
00	$\bar{A}\bar{B}$	1	0	1
10	$A\bar{B}$	1	0	1
01	$\bar{A}B$	1	0	1
11	$AB$	1	0	1

### Maxterm mode

		B	$\bar{B}$	
		A	0	1
		$\bar{A}$	0	1
00	$A+B$	1	0	1
01	$A+\bar{B}$	1	0	1
10	$\bar{A}+B$	1	0	1
11	$\bar{A}+\bar{B}$	1	0	1

# 3-Variable K-Map

Minterm mode

		BC	$\bar{B}\bar{C}$
		00	01
		11	10
A		000 $\bar{A}\bar{B}\bar{C}$	001 $\bar{A}\bar{B}C$
$\bar{A}$		011 $\bar{A}BC$	010 $\bar{A}B\bar{C}$
A		100 $A\bar{B}\bar{C}$	101 $A\bar{B}C$
$\bar{A}$		111 $ABC$	110 $A\bar{B}\bar{C}$

Minterm mode

		AC	$\bar{A}\bar{C}$
		00	01
		11	10
B		000 $\bar{A}\bar{B}\bar{C}$	001 $\bar{A}B\bar{C}$
$\bar{B}$		010 $A\bar{B}\bar{C}$	011 $A\bar{B}C$
B		101 $ABC$	111 $A\bar{B}\bar{C}$
$\bar{B}$		110 $AB\bar{C}$	111 $ABC$

# 3-Variable K-Map

Maxterm mode

AB		$A+B$	$\bar{A}+\bar{B}$	$\bar{A}+B$	
		00	01	11	
		000	010	110	100
$A$	$B$	$A+B+C$	$A+\bar{B}+C$	$\bar{A}+\bar{B}+C$	$\bar{A}+B+C$
0	0	0	2	6	4
$\bar{A}$	$\bar{B}$	$\bar{A}+\bar{B}+\bar{C}$	$\bar{A}+\bar{B}+C$	$\bar{A}+B+\bar{C}$	$\bar{A}+B+C$
1	1	1	3	7	5

## 4- Variable K-map (A B C D)

		$\bar{A}C$	$\bar{A}\bar{C}$	$\bar{A}C$	$A\bar{C}$	$A\bar{C}$
		$BD$	$\bar{B}D$	$\bar{B}D$	$BD$	$BD$
$\bar{B}\bar{D}$	00	0000 $\bar{A}\bar{B}\bar{C}\bar{D}$	0010 ✓ $\bar{A}\bar{B}CD$	1010 $A\bar{B}CD$	1000 $A\bar{B}\bar{C}\bar{D}$	1000 $A\bar{B}\bar{C}\bar{D}$
$\bar{B}D$	01	0001 $\bar{A}\bar{B}\bar{C}D$	0011 $\bar{A}\bar{B}\bar{C}D$	1011 $A\bar{B}CD$	1001 $A\bar{B}\bar{C}D$	1001 $A\bar{B}\bar{C}D$
$B\bar{D}$	11	0101 $\bar{A}B\bar{C}D$	0111 $\bar{A}BCD$	1111 $ABCD$	1101 $AB\bar{C}D$	1101 $AB\bar{C}D$
$B\bar{D}$	10	0100 ✓ $\bar{A}B\bar{C}\bar{D}$	0110 $\bar{A}BC\bar{D}$	1110 $ABC\bar{D}$	1100 $AB\bar{C}\bar{D}$	1100 $AB\bar{C}\bar{D}$

Adjacent cell for 8 – { 0 , 10 , 9 , 12 }

Adjacent cell for 2 – { 0 , 3, 6,10,}

Adjacent cell for 11 – { 3, 10 , 9 , 15 }

Adjacent cell for 15 – { 7 , 13 , 11 , 14}

Adjacent cell for  $0 = \{1, 2, 4, 8\}$

Adjacent cell for 6 = { 4, 7, 2, 14 }

Adjacent cell for 14 = { 6, 10, 12, 15 }

Adjacent cell for 3 = { 1, 11, 7, 2 }

# 4- Variable K-map

		$\bar{C}D$	$C\bar{D}$	$CD$	$C\bar{D}$
		$00$	$01$	$11$	$10$
$\bar{A}\bar{B}$	$00$	$0000$ $\bar{A}\bar{B}\bar{C}\bar{D}$	$0001$ $\bar{A}\bar{B}C\bar{D}$	$0011$ $\bar{A}\bar{B}CD$	$0010$ $\bar{A}\bar{B}C\bar{D}$
	$01$	$0100$ $\bar{A}B\bar{C}\bar{D}$	$0101$ $\bar{A}B C\bar{D}$	$0111$ $\bar{A}B CD$	$0110$ $\bar{A}B C\bar{D}$
$A\bar{B}$	$11$	$1100$ $A\bar{B}\bar{C}\bar{D}$	$1101$ $A\bar{B} C\bar{D}$	$1111$ $A\bar{B} CD$	$1110$ $A\bar{B} C\bar{D}$
	$10$	$1000$ $A\bar{B}\bar{C}\bar{D}$	$1001$ $A\bar{B} C\bar{D}$	$1011$ $A\bar{B} CD$	$1010$ $A\bar{B} C\bar{D}$

Adjacent cell for  $_8 - \{ 0, 10, 9, 12 \}$

Adjacent cell for  $2 - \{ 0, 3, 6, 10, \}$

Adjacent cell for  $11 - \{ 3, 10, 9, 15 \}$

Adjacent cell for  $15 - \{ 7, 13, 11, 14 \}$

Adjacent cell for  $0 - \{ 1, 2, 4, 8, \}$

Adjacent cell for  $6 - \{ 4, 7, 2, 14 \}$

Adjacent cell for  $14 - \{ 6, 10, 12, 15 \}$

Adjacent cell for  $3 - \{ 1, 11, 7, 2 \}$

## 4-Variable K-map (Maxterm mode)

		CD	$C+D$	$C+\bar{D}$	$\bar{C}+\bar{D}$	$\bar{C}+D$
		00	01	11	10	
AB	00	$A+B+C+D$	$A+B+C+\bar{D}$	$A+B+\bar{C}+\bar{D}$	$A+B+\bar{C}+D$	
	01	$A+\bar{B}+C+D$	$A+\bar{B}+C+\bar{D}$	$A+\bar{B}+\bar{C}+\bar{D}$	$A+\bar{B}+\bar{C}+D$	
$\bar{A}+\bar{B}$	11	$\bar{A}+\bar{B}+C+D$	$\bar{A}+\bar{B}+C+\bar{D}$	$\bar{A}+\bar{B}+\bar{C}+\bar{D}$	$\bar{A}+\bar{B}+\bar{C}+D$	
	10	$\bar{A}+B+C+D$	$\bar{A}+B+C+\bar{D}$	$\bar{A}+B+\bar{C}+\bar{D}$	$\bar{A}+B+\bar{C}+D$	

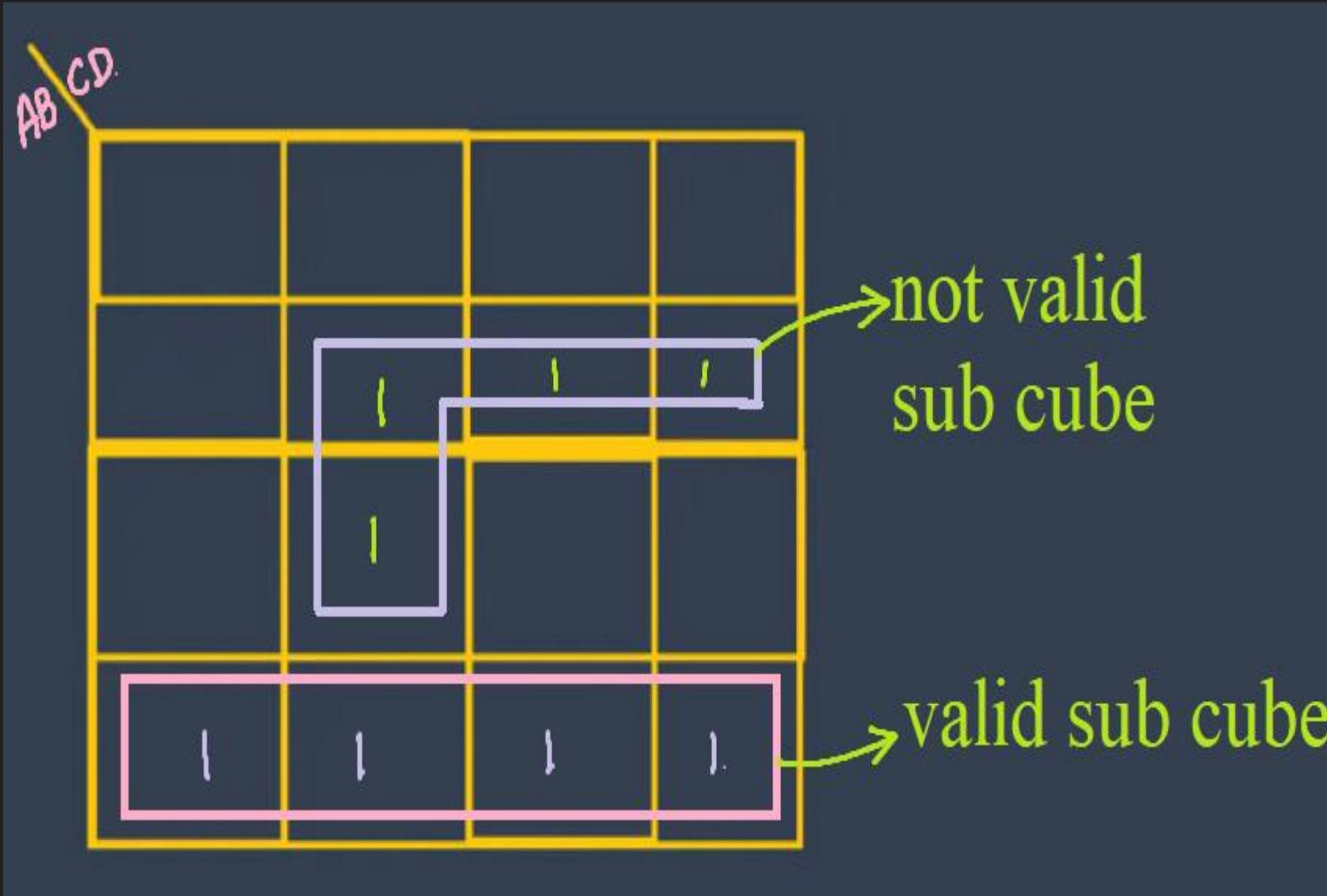
# Minimization Steps

1. Place the corresponding minterm/maxterms in the corresponding cells.
2. Using the valid sub cube property go for bigger size grouping .
3. Don't care combination's may not be covered , it depends on the K-map.
4. Remove the redundant groups if any present .

## **Sub cube**

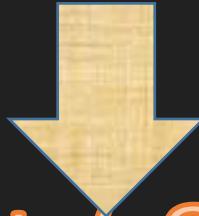
A collection of  $2^m$  number of cells in a K- map is said to be forming a valid sub cube , provided inside the collection  $2^m$  number of cells every cell is logical adjacent to m number of cells .

## 4- Variable K-map

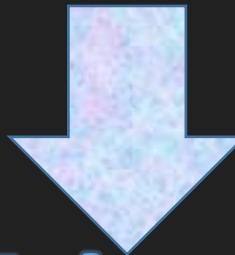


# Priority of grouping

( 16-cells )



Octet ( 8-cells )



Quad ( 4-cells )

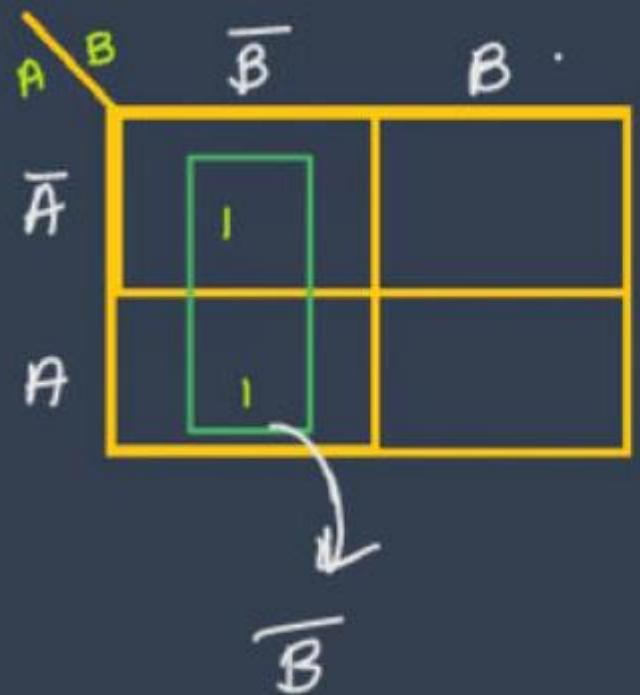


Pair ( 2-cells )

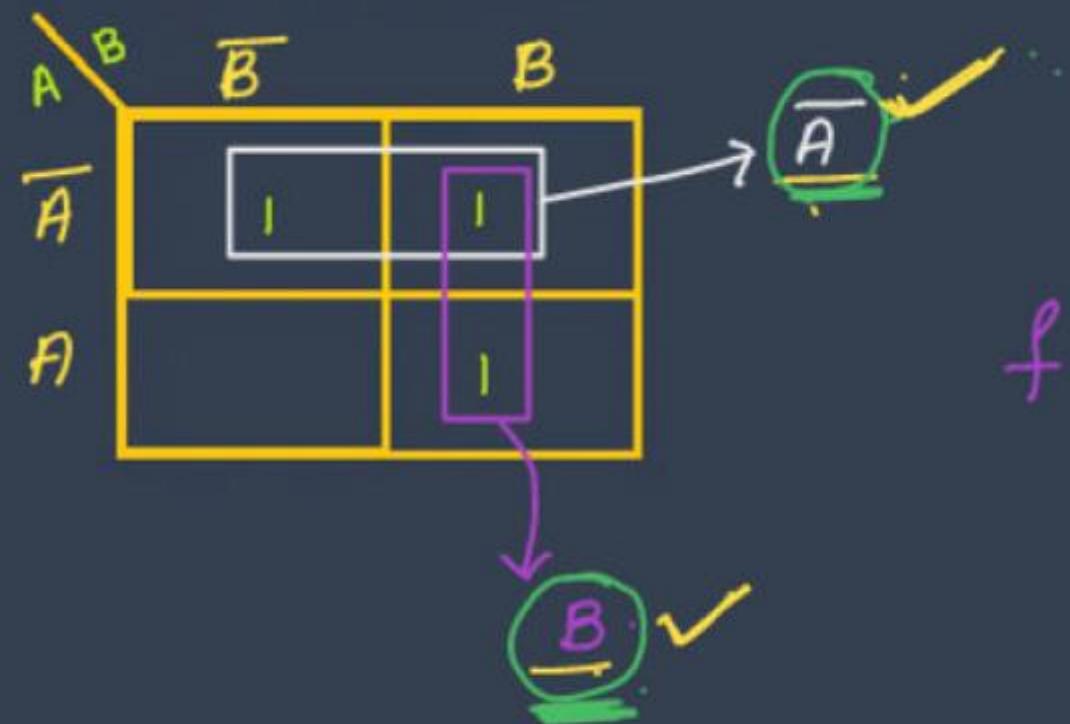
Q) Minimize the following



Q) Minimize the following



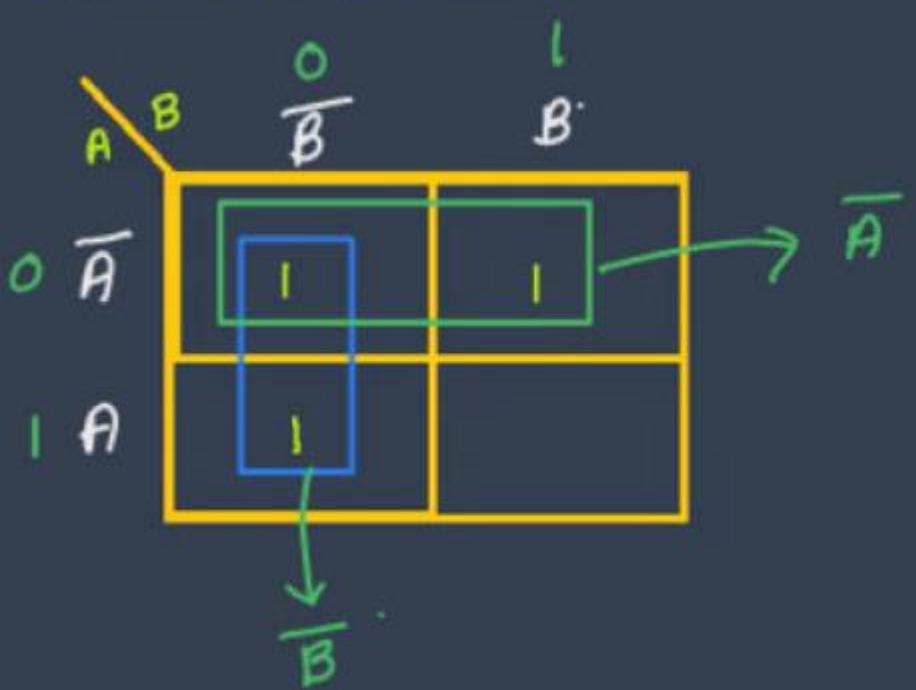
Q) Minimize the following



SOP

$$f = \bar{A} + B$$

Q) Minimize the following



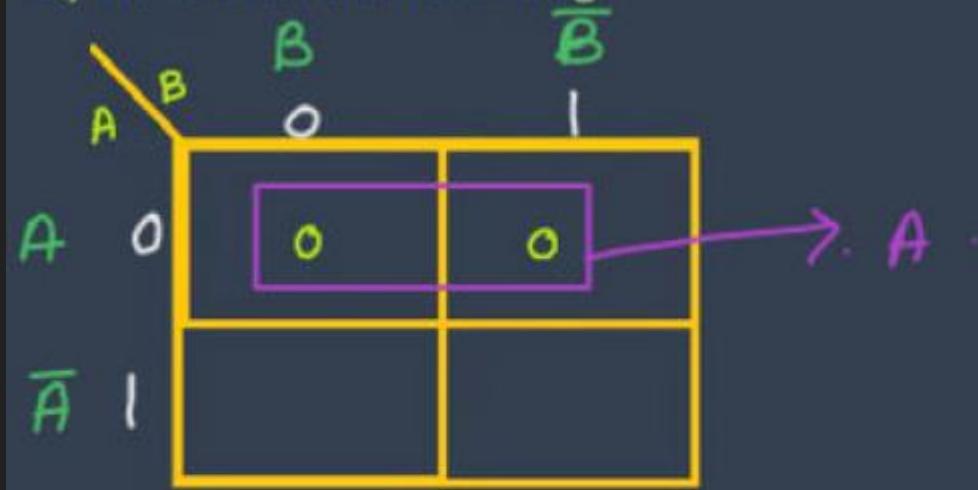
$$f = \overline{A} + \overline{B}$$

Q) Minimize the following



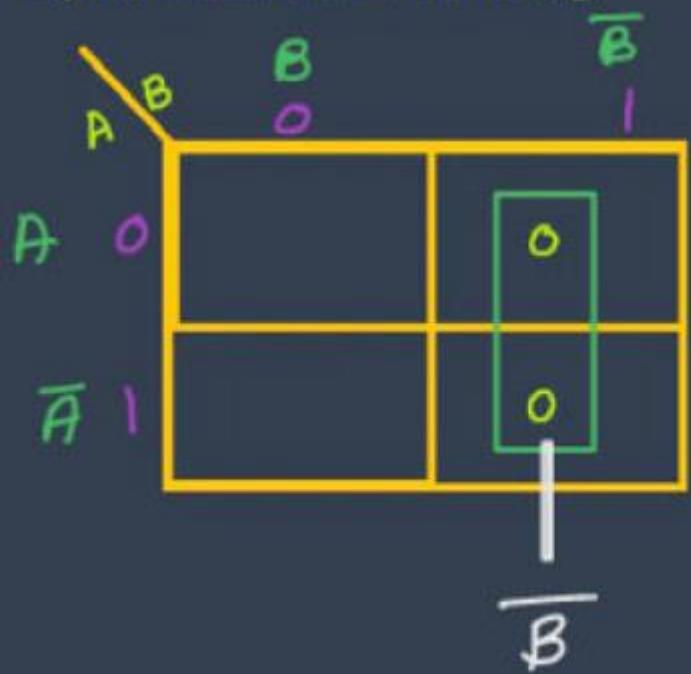
$$\rightarrow f = \underline{l}.$$

Q) Minimize the following

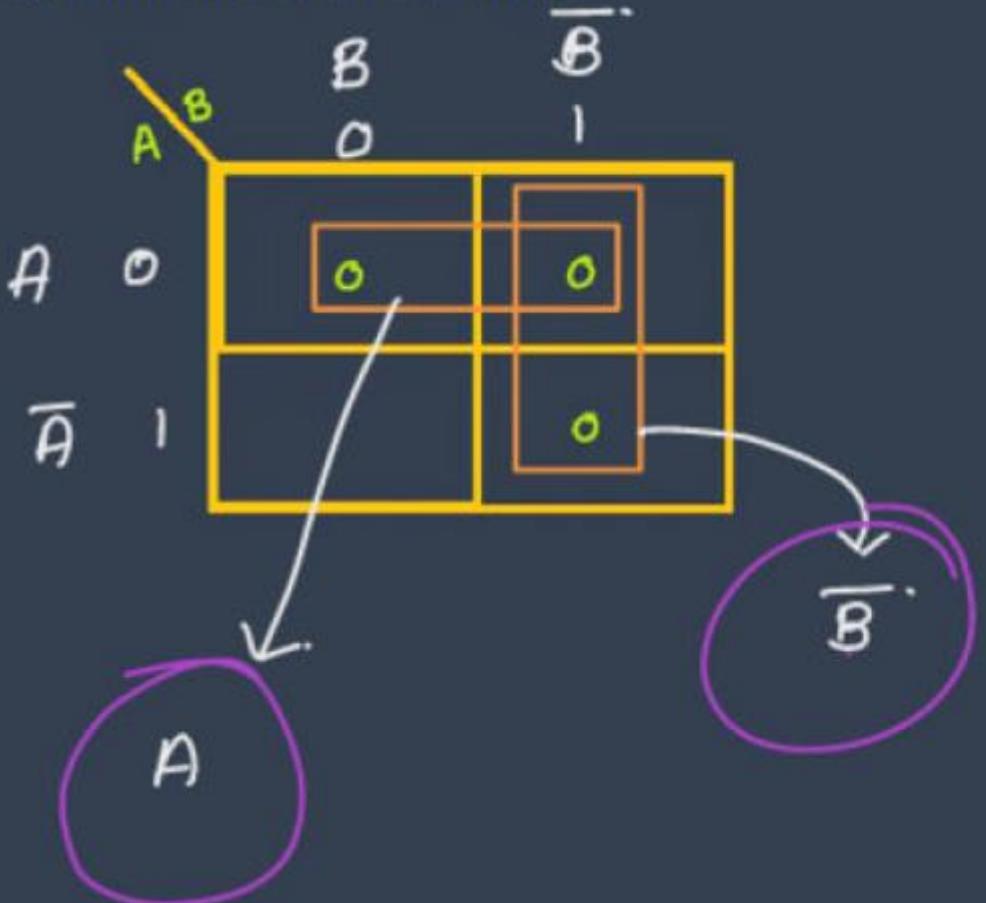


$A$

Q) Minimize the following



Q) Minimize the following



$$f = \underline{(A)(\bar{B})}$$

Q) Minimize the following

	B	$\bar{B}$
A	0	0
$\bar{A}$	0	0

$$f = 0$$

minimise

$$\begin{aligned} f &= \underline{(A+B)(A+\bar{B})(\bar{A}+B)(\bar{A}+\bar{B})} \quad \checkmark \\ &= (A+0)(\bar{A}+0) = A\bar{A} = 0 \end{aligned}$$

Q) Minimize the following

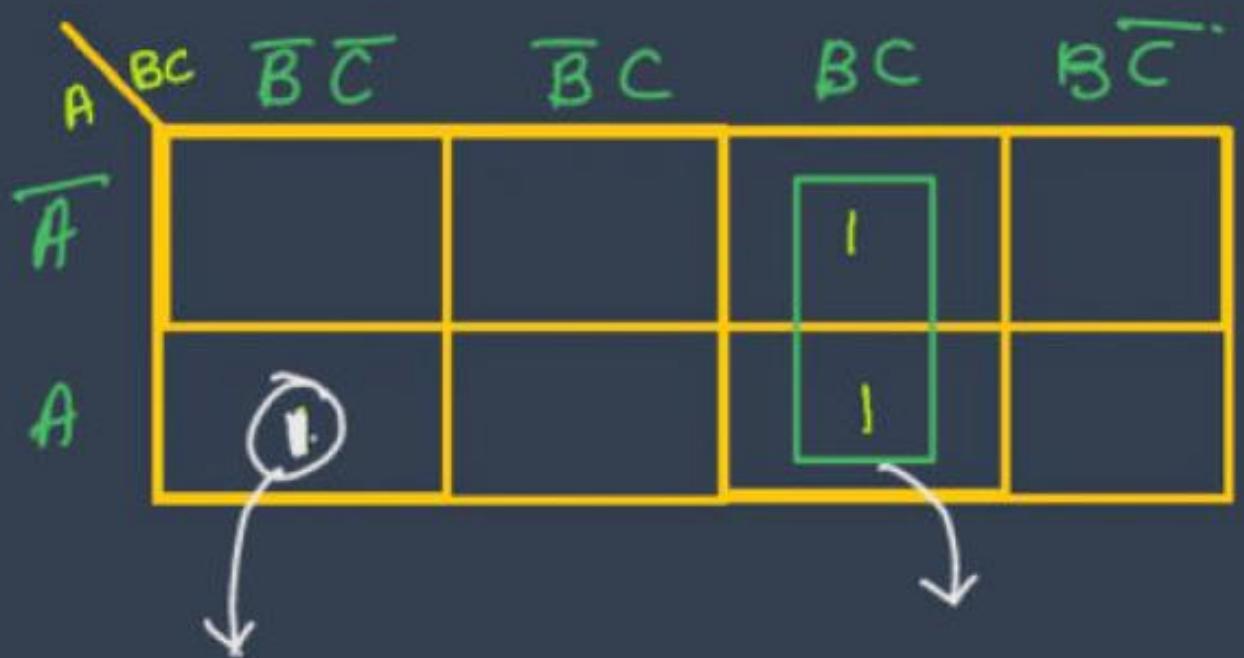


→.

$AC$

$$f = A C + \bar{A} \bar{C}$$

Q) Minimize the following



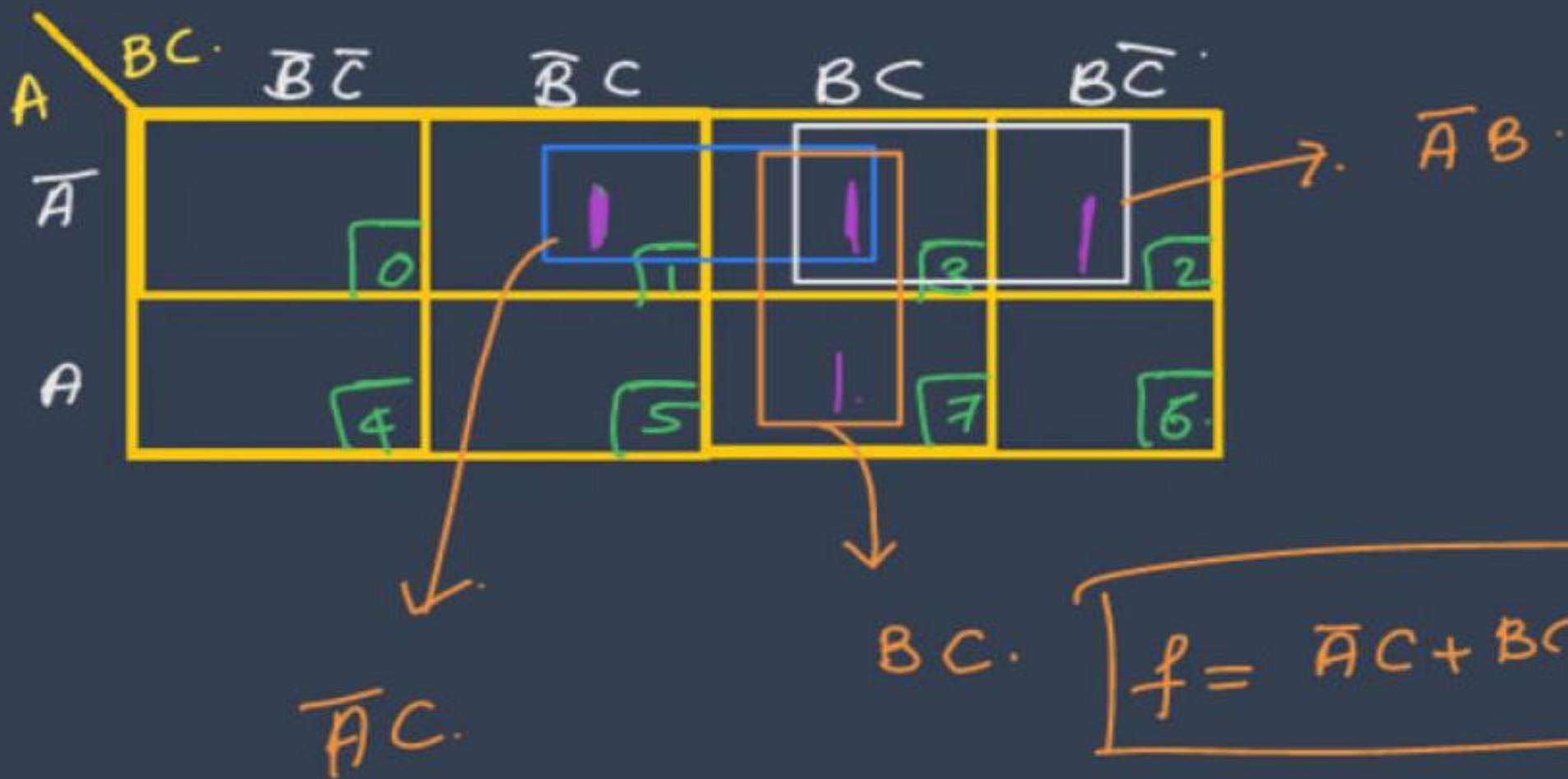
$$A\bar{B}\bar{C}$$

$$BC$$

$$f = A\bar{B}\bar{C} + BC$$

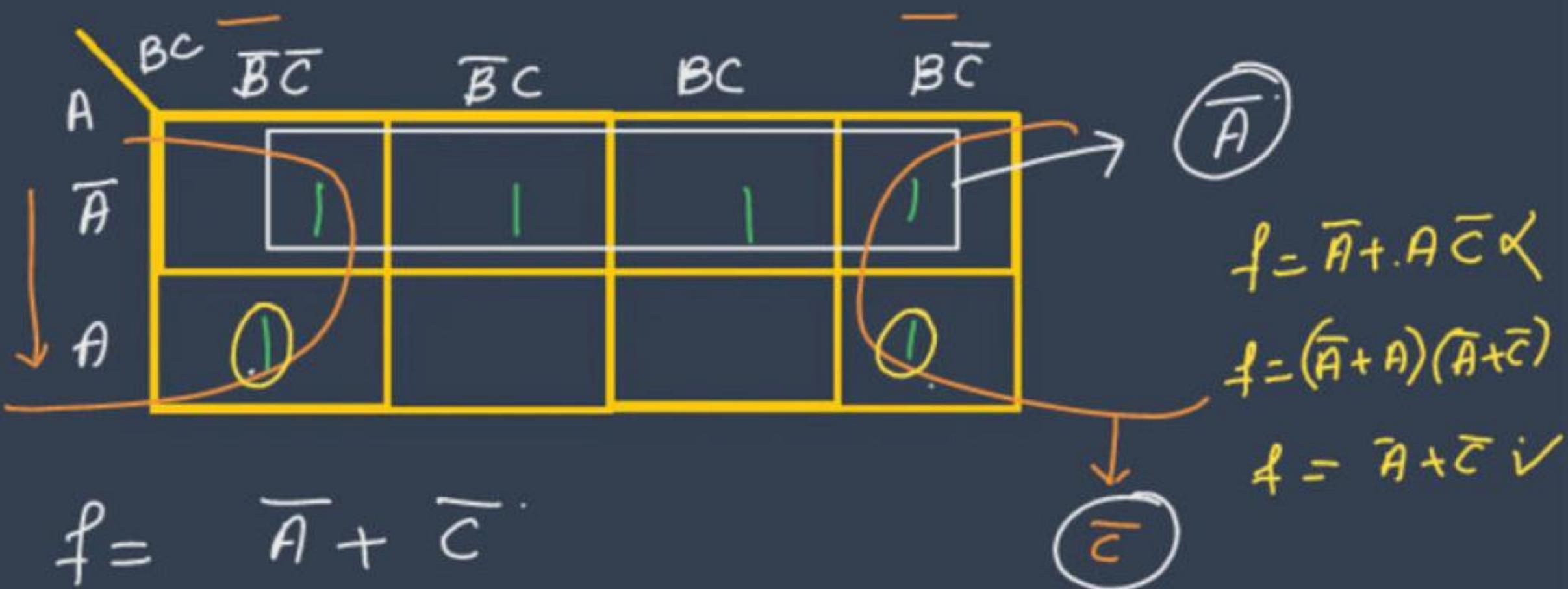
Q)  $F(A, B, C) = \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$

001    010    011    111

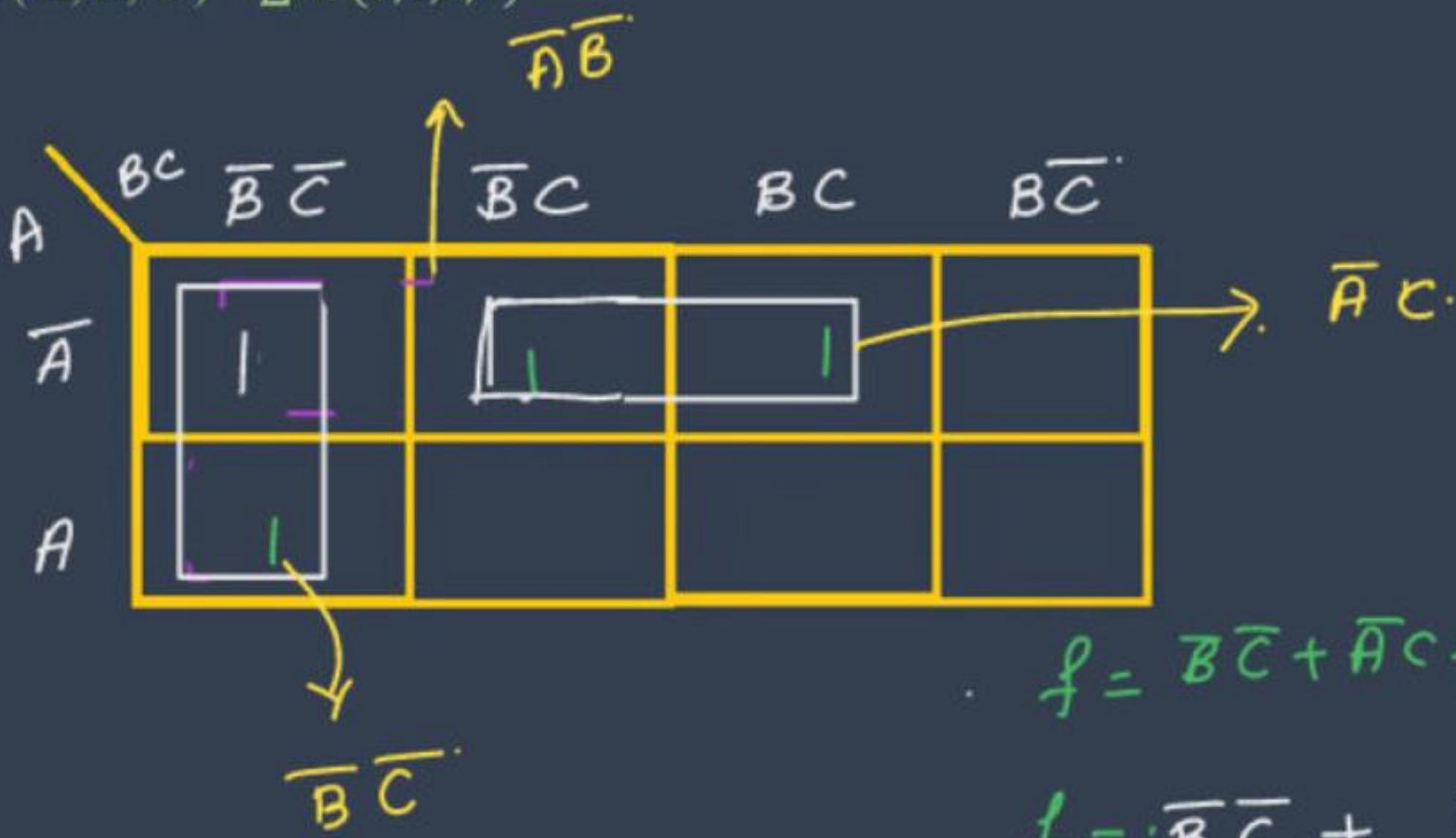


$f = \bar{A}C + BC + \bar{A}B$

$$Q) F(A, B, C) = \sum m(0, 1, 2, 3, 4, 6)$$



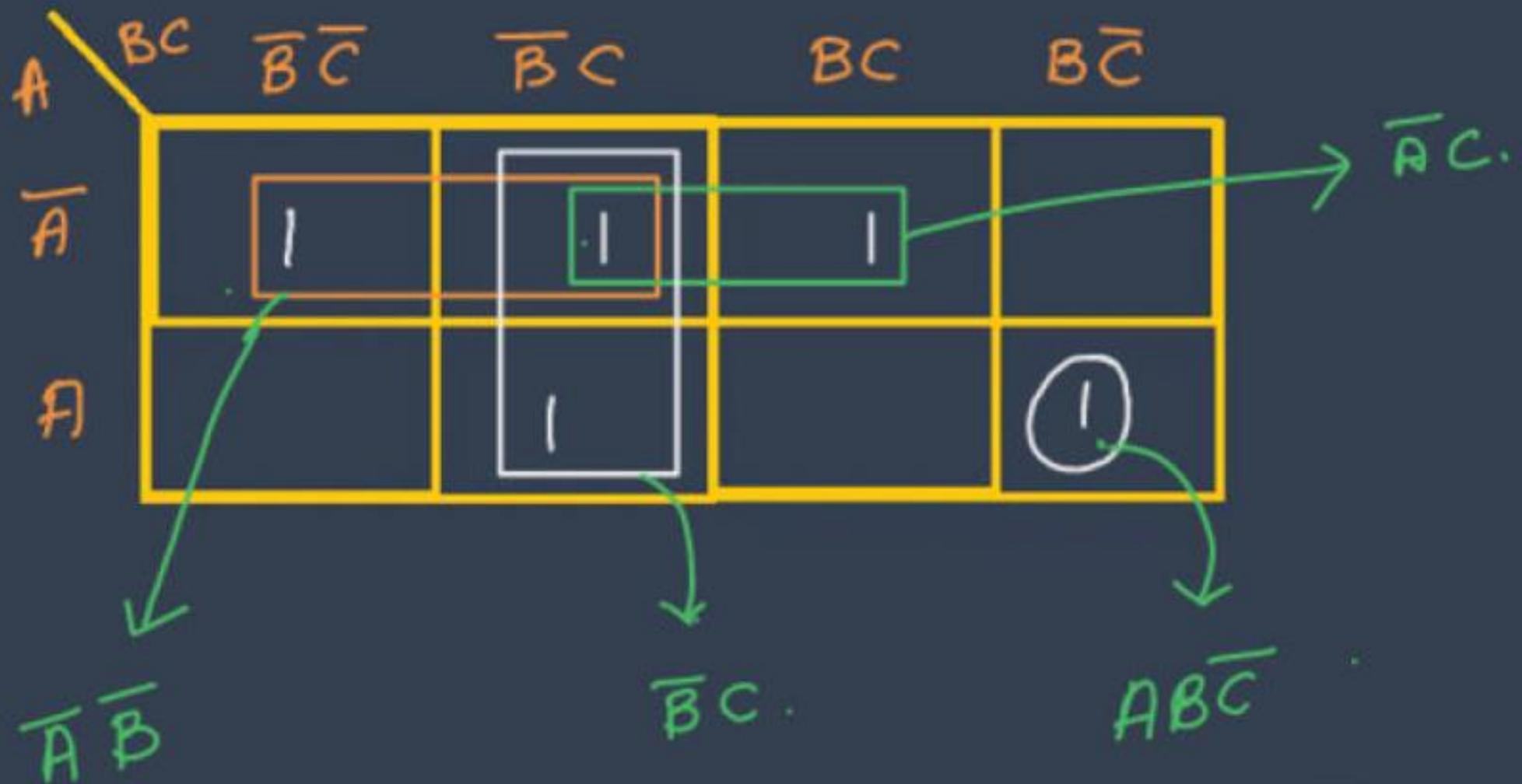
$$Q) F(A, B, C) = \sum m(0, 1, 3, 4)$$



$$f = B\bar{C} + \bar{A}C + \cancel{\bar{A}\bar{B}}$$

$$f = \bar{B}\bar{C} + \bar{A}C \checkmark$$

$$Q) F(A, B, C) = \sum m(0, 1, 3, 5, 6)$$



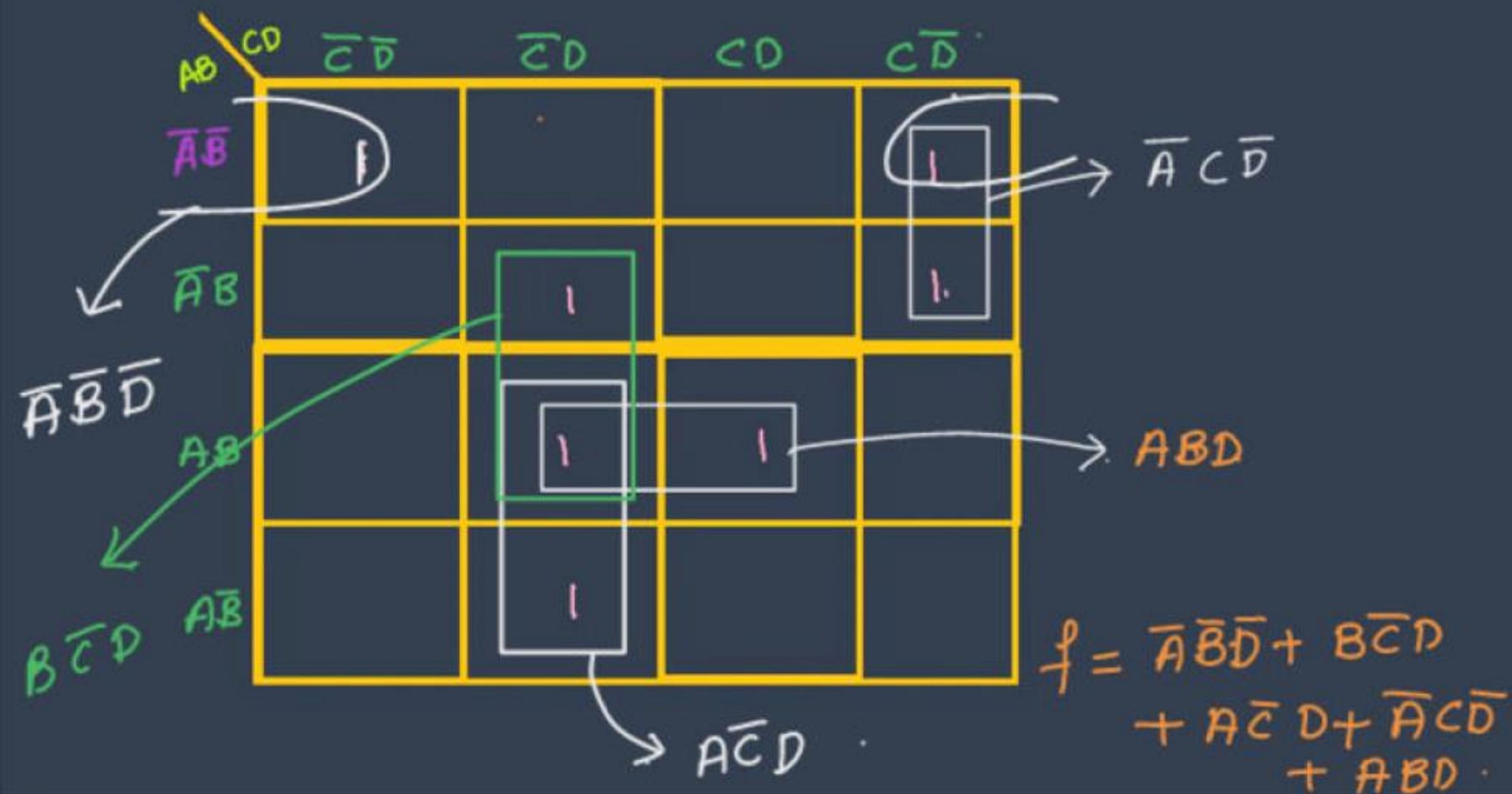
$$f = \bar{A}\bar{B} + \bar{B}C + \bar{A}C + AB\bar{C}$$

$$Q) F = (A, B, C) = \prod M(2, 4, 7)$$

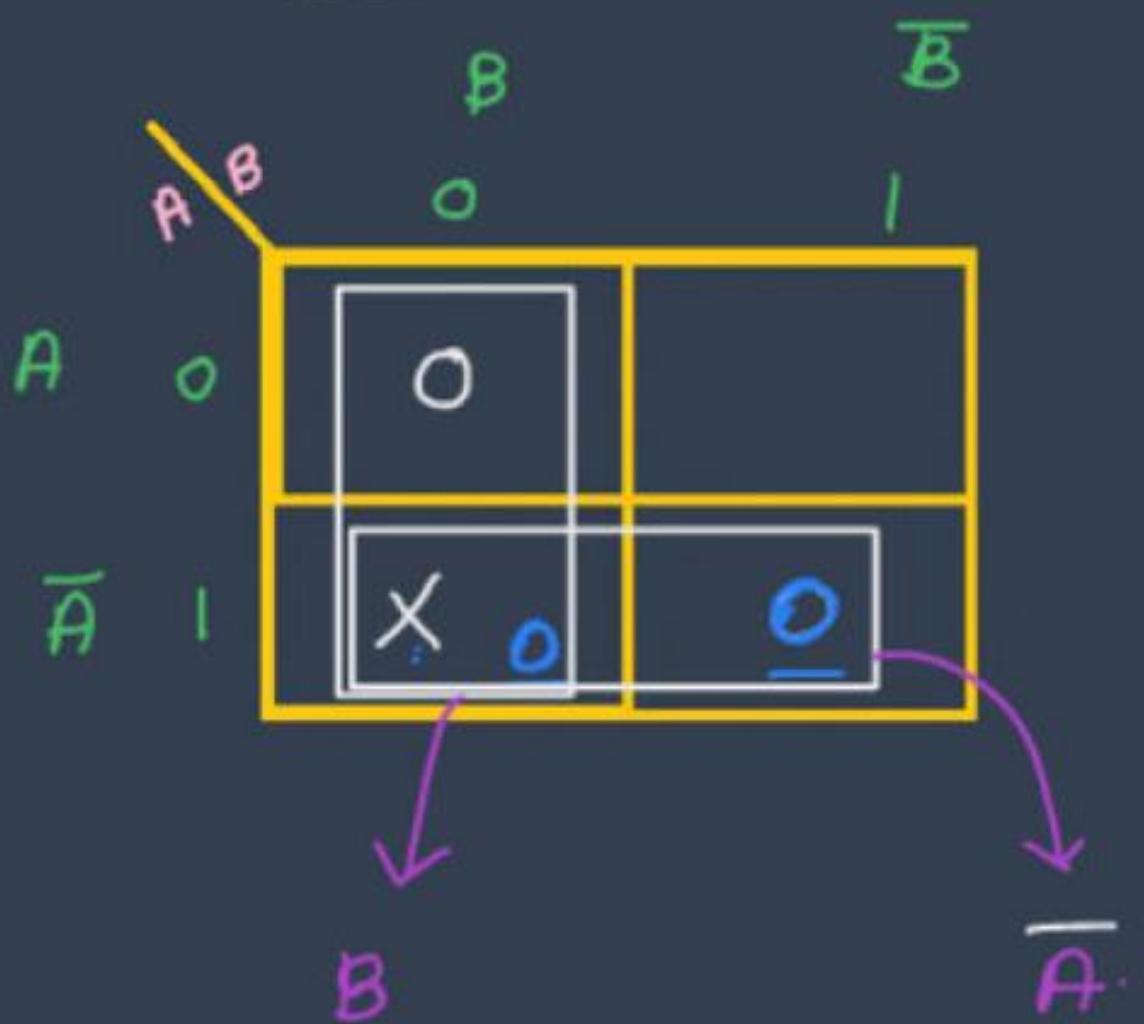
	$B + C$	$B + \bar{C}$	$\bar{B} + \bar{C}$	$\bar{B} + C$
$A$	00	01	11	10
$\bar{A}$	0	0	0	1

$$f = (\bar{A} + B + C)(\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + C)$$

Q) Minimize the following



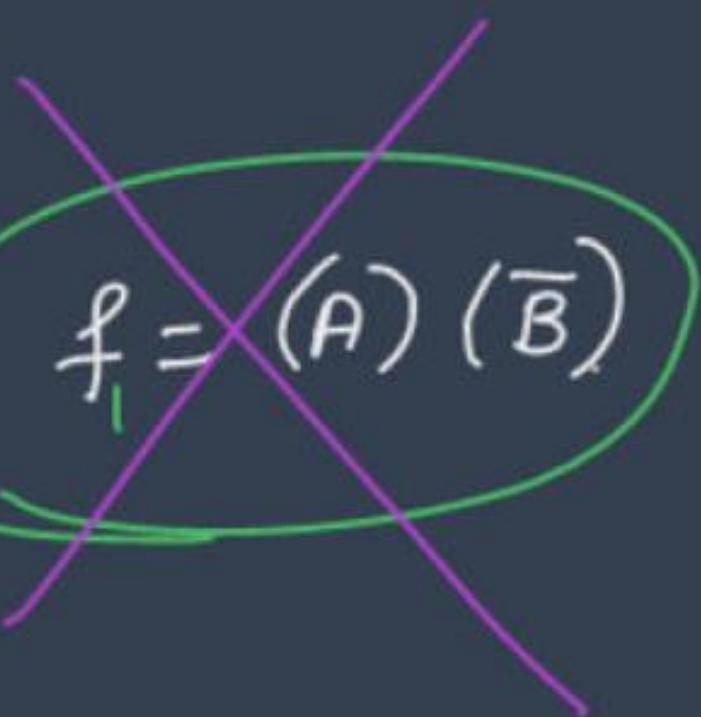
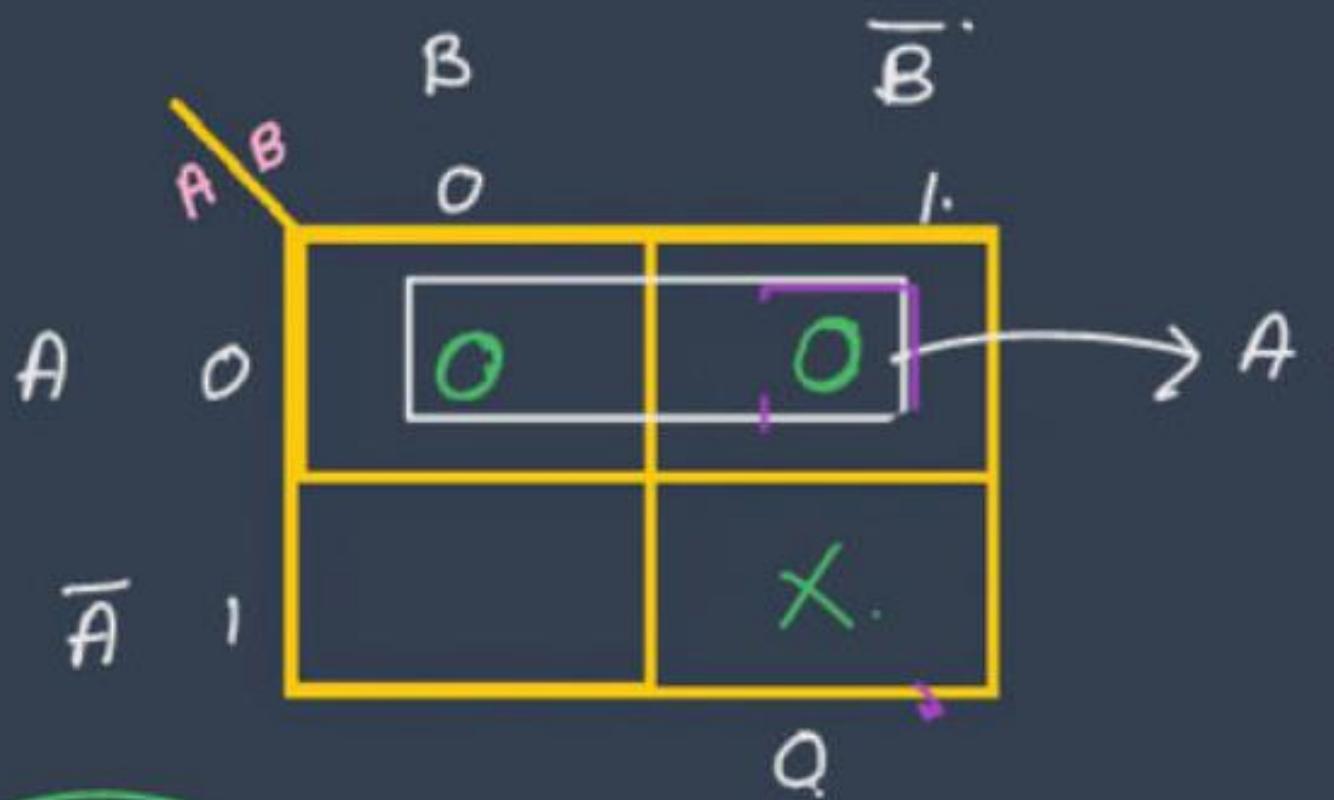
$$Q) F(A, B) = \underbrace{\prod M(0, 3)}_{d(2)} + \underbrace{\prod d(2)}$$



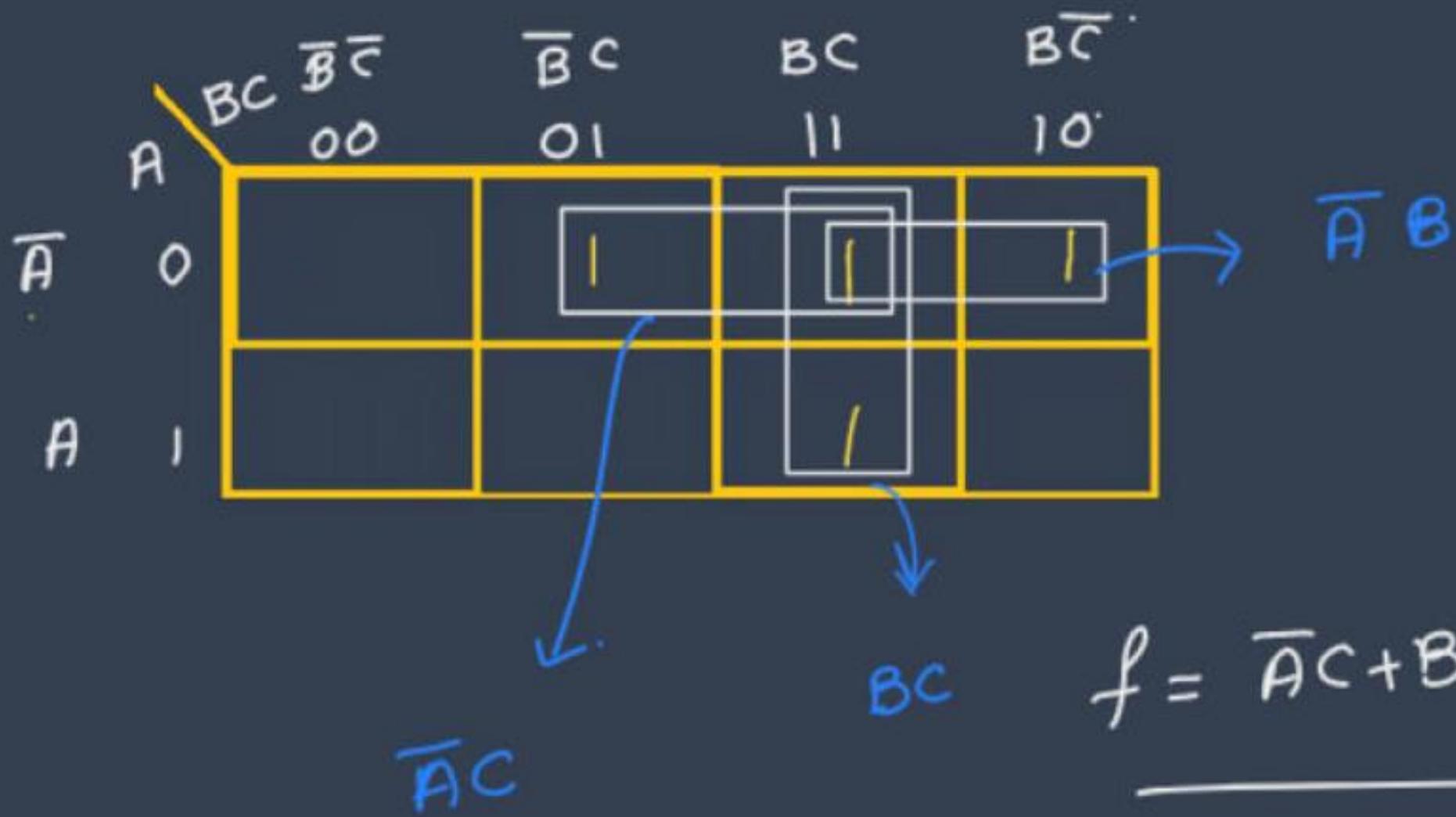
$$f = (\bar{A}) \cdot (\bar{B}).$$

$$X = \underline{o(\sigma r)}$$

$$Q) F(A, B) = \prod M(0, 1) + \prod d(3)$$

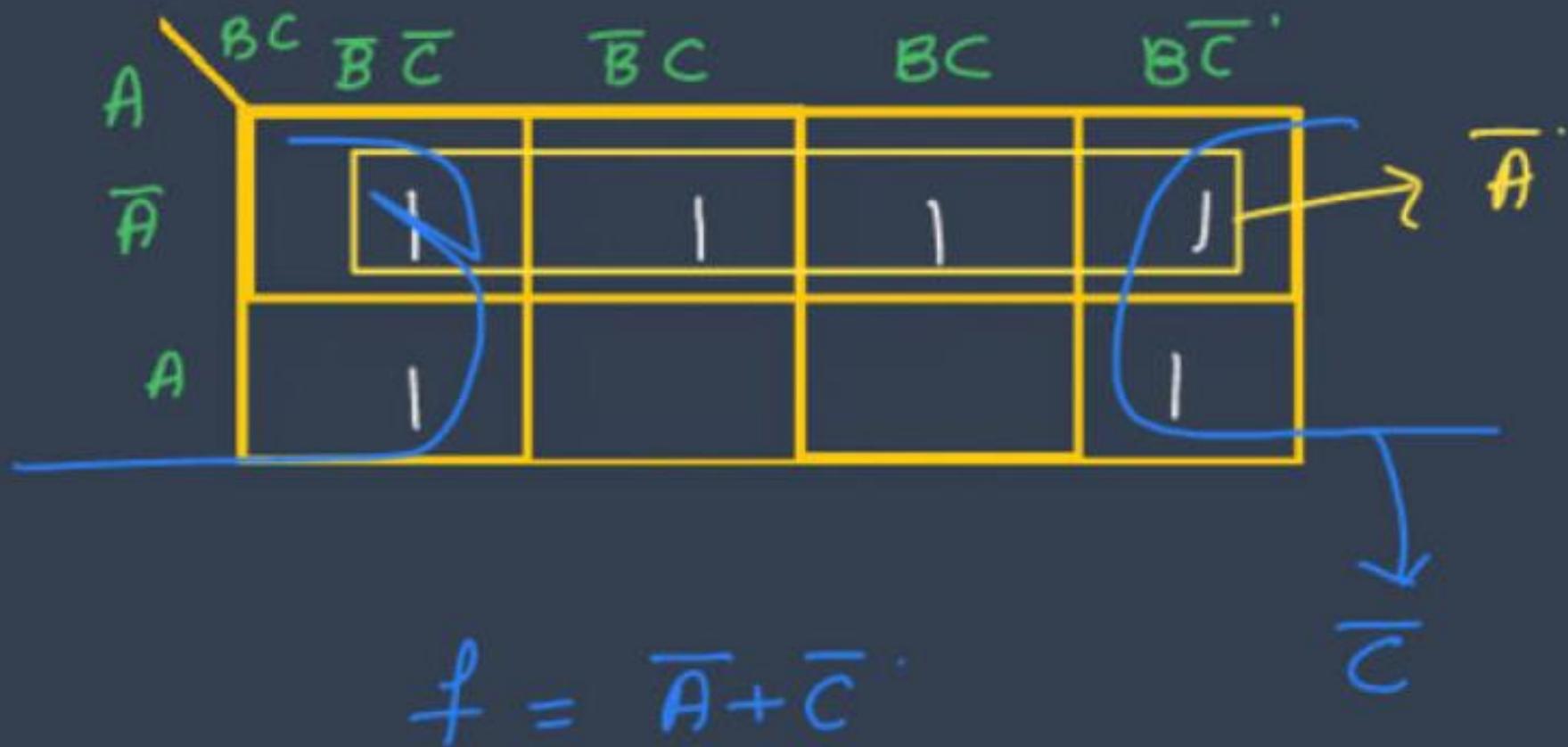


$$Q) F(A, B, C) = \underline{\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC}$$



$$f = \overline{A'C} + BC + \overline{AB}$$

$$Q)F = \sum m(0,1,2,3,4,6)$$



Q) Minimize the following

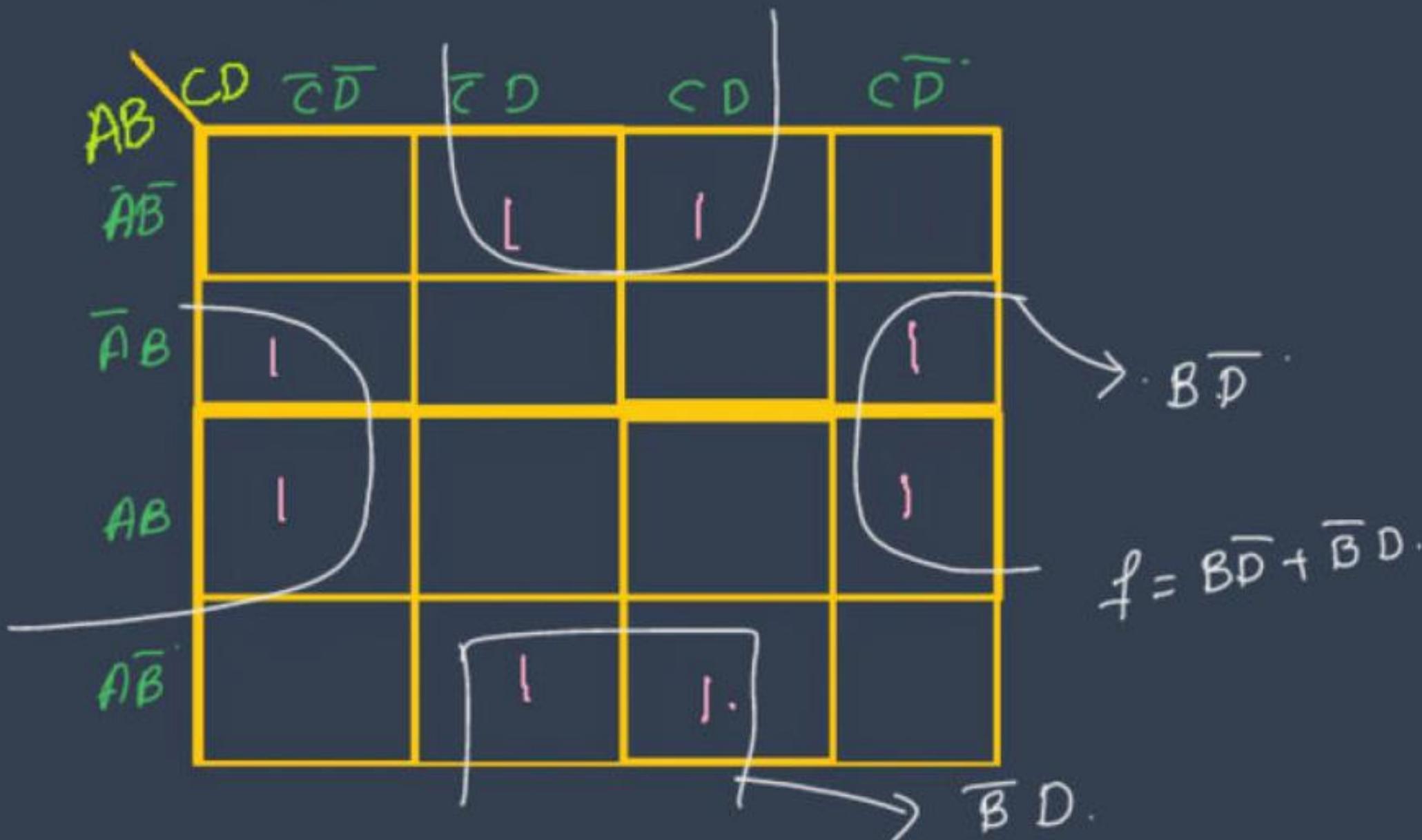
$AB$	$CD$	$\bar{C}\bar{D}$	$\bar{C}D$	$C\bar{D}$	$CD$
$\bar{A}\bar{B}$	1				1
$\bar{A}B$		1	1		
$A\bar{B}$		1	1		
$A\bar{B}$	1				

$$f = BD + \bar{B}\bar{D}$$

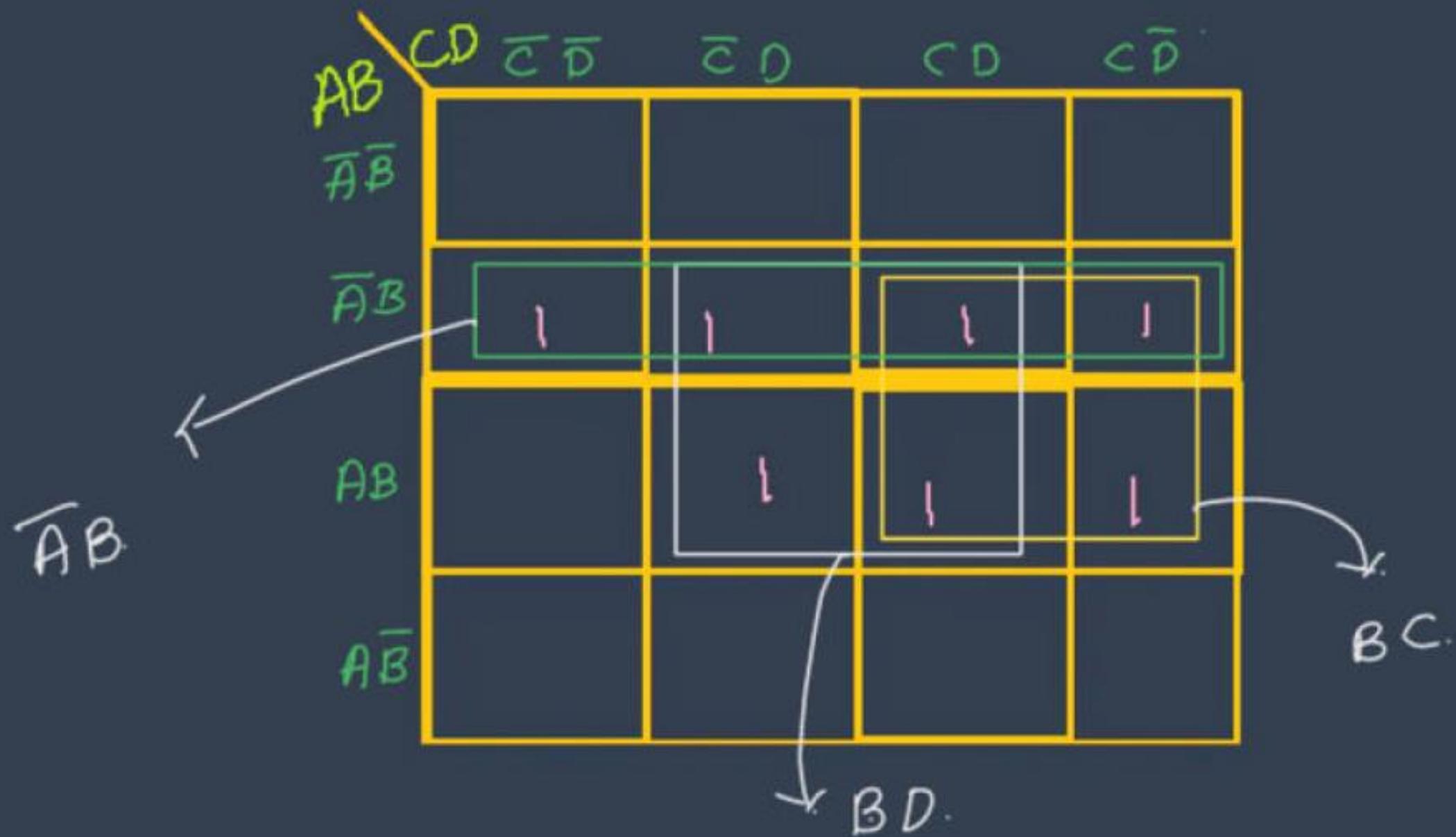
$BD$

$\bar{B}\bar{D}$

Q) Minimize the following



Q) Minimize the following

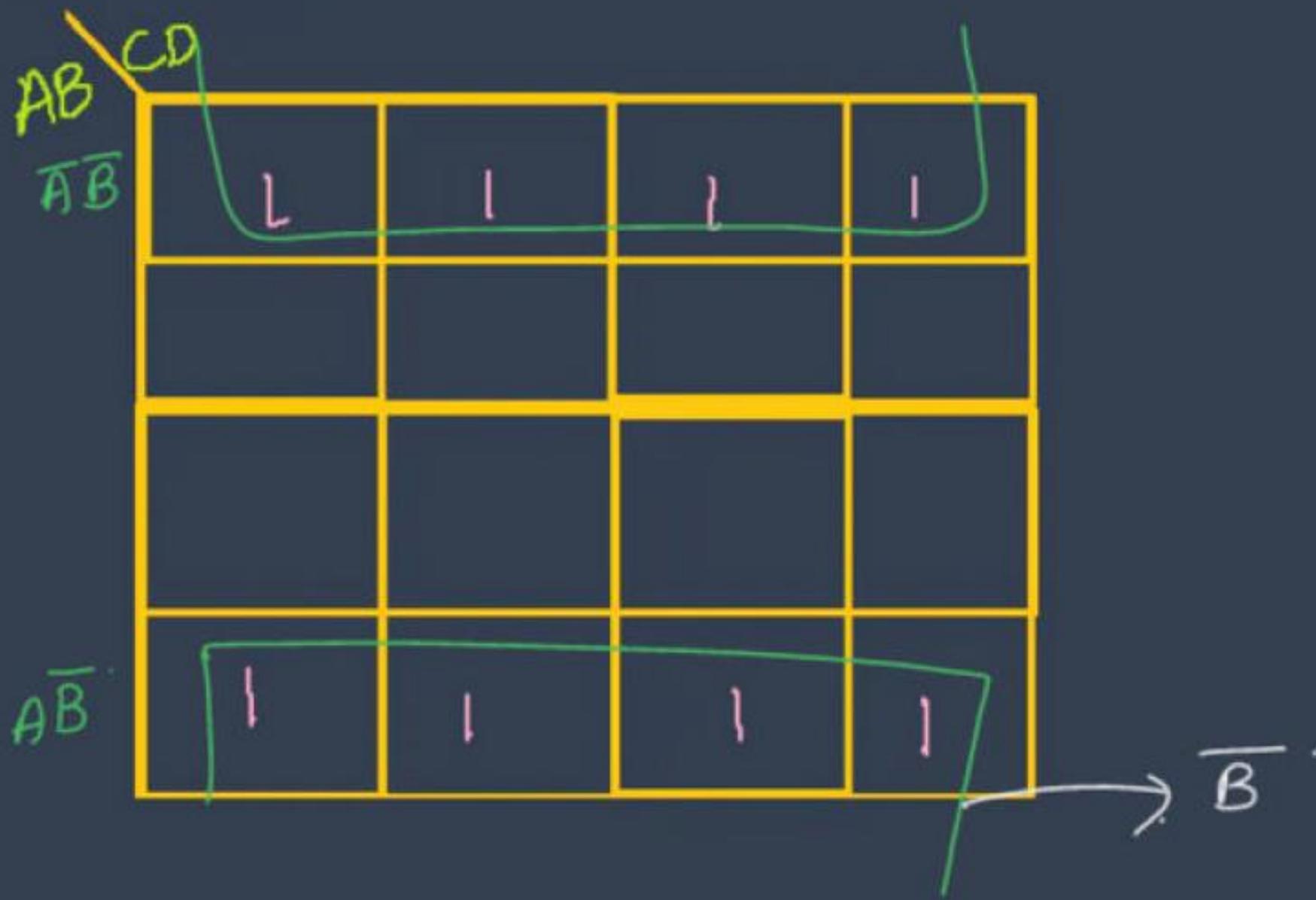


Q) Minimize the following

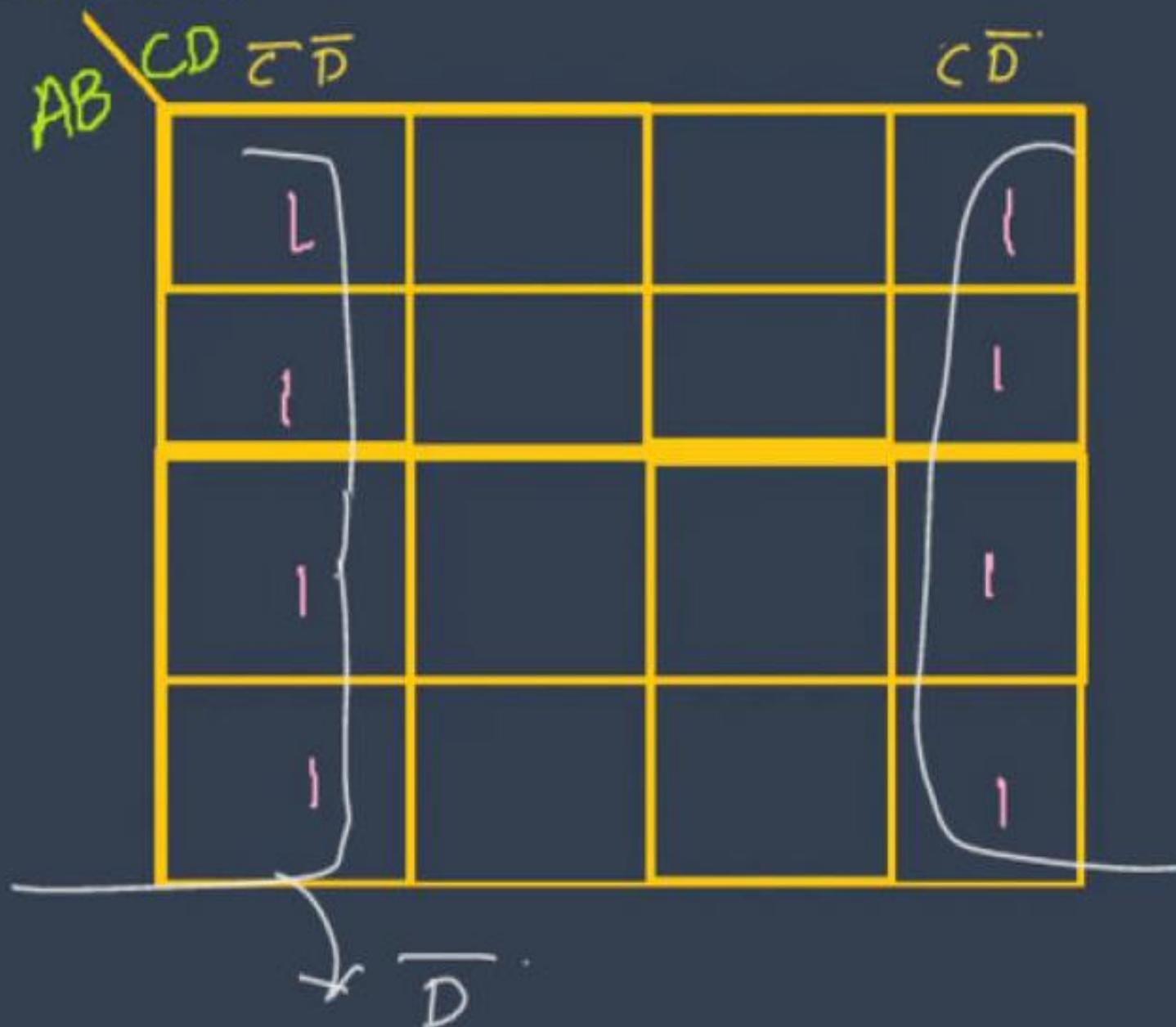
$AB$	$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	$AB$
$CD$	$\bar{C}\bar{D}$	$\bar{C}D$	$CD$	$C\bar{D}$
1	1	1	1	1
1	1	1	1	1

Diagram illustrating the minimization of a Boolean function using a Karnaugh map. The columns represent the product terms  $AB$ ,  $\bar{A}\bar{B}$ ,  $\bar{A}B$ ,  $A\bar{B}$ , and  $AB$ . The rows represent the product terms  $CD$ ,  $\bar{C}\bar{D}$ ,  $\bar{C}D$ ,  $CD$ , and  $C\bar{D}$ . The map shows minterms 1 at positions  $(\bar{A}, \bar{B}, \bar{C}, \bar{D})$ ,  $(\bar{A}, B, \bar{C}, \bar{D})$ ,  $(A, \bar{B}, \bar{C}, \bar{D})$ ,  $(A, B, \bar{C}, \bar{D})$ ,  $(\bar{A}, \bar{B}, C, \bar{D})$ ,  $(\bar{A}, B, C, \bar{D})$ ,  $(A, \bar{B}, C, \bar{D})$ , and  $(A, B, C, \bar{D})$ . A green bracket groups the first four minterms, and another green bracket groups the last four minterms. A curved arrow labeled  $B$  points from the bottom right corner of the grouped minterms to the  $B$  column, indicating that the function can be simplified to  $B$ .

Q) Minimize the following



Q) Minimize the following

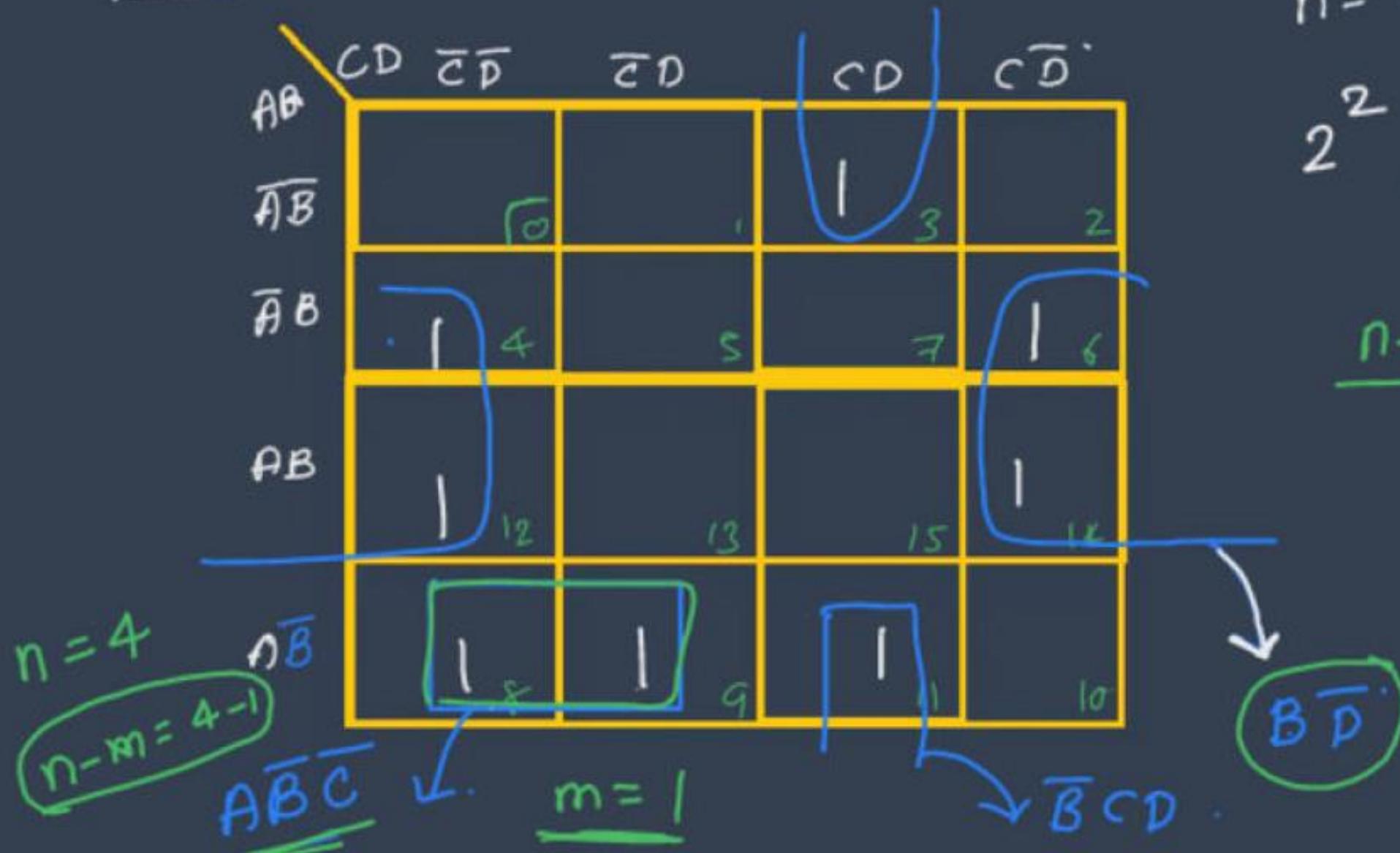


$$Q) F(A, B, C, D) = \sum m(3, 4, 6, 8, 9, 11, 12, 14)$$

$$n=4$$

$$2^2, m=2$$

n-m



$$Q) F(A, B, C, D) = \prod M(3, 4, 6, 8, 9, 11, 12, 14)$$

$$f = (A + B + C)(B + \bar{C} + \bar{D}) \\ (\bar{B} + D)$$

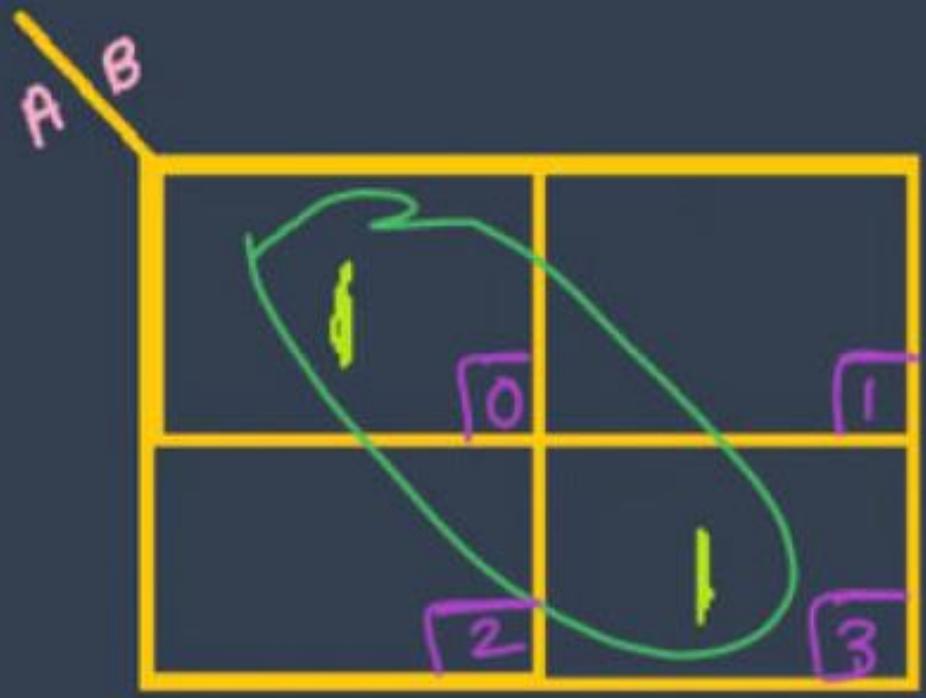
		$C + D$	$C + \bar{D}$	$\bar{C} + \bar{D}$	$\bar{C} + D$
		00	01	11	10
$A + B$	00			0	
$A + \bar{B}$	01	0			0
$\bar{A} + \bar{B}$	11	0			0
$\bar{A} + B$	10	0	0	0	

Handwritten annotations:

- Region 00: Labeled 0
- Region 01: Labeled 0
- Region 11: Labeled 0
- Region 10: Labeled 0
- Region 00 (row A+B=00): Labeled 0
- Region 01 (row A+B=01): Labeled 0
- Region 11 (row A+B=11): Labeled 0
- Region 10 (row A+B=10): Labeled 0
- Region 00 (column CD=00): Labeled 0
- Region 01 (column CD=01): Labeled 0
- Region 11 (column CD=11): Labeled 0
- Region 10 (column CD=10): Labeled 0
- Region 00 (row A+B=00, column CD=00): Labeled 0
- Region 01 (row A+B=01, column CD=01): Labeled 0
- Region 11 (row A+B=11, column CD=11): Labeled 0
- Region 10 (row A+B=10, column CD=10): Labeled 0
- Region 00 (row A+B=00, column CD=00, column C+D=00): Labeled 0
- Region 01 (row A+B=01, column CD=01, column C+D=01): Labeled 0
- Region 11 (row A+B=11, column CD=11, column C+D=11): Labeled 0
- Region 10 (row A+B=10, column CD=10, column C+D=10): Labeled 0
- Region 00 (row A+B=00, column CD=00, column C+D=00, column C+D=01): Labeled 0
- Region 01 (row A+B=01, column CD=01, column C+D=01, column C+D=11): Labeled 0
- Region 11 (row A+B=11, column CD=11, column C+D=11, column C+D=10): Labeled 0
- Region 10 (row A+B=10, column CD=10, column C+D=10, column C+D=10): Labeled 0
- Region 00 (row A+B=00, column CD=00, column C+D=00, column C+D=01, column C+D=11): Labeled 0
- Region 01 (row A+B=01, column CD=01, column C+D=01, column C+D=11, column C+D=10): Labeled 0
- Region 11 (row A+B=11, column CD=11, column C+D=11, column C+D=10, column C+D=10): Labeled 0
- Region 10 (row A+B=10, column CD=10, column C+D=10, column C+D=10, column C+D=10): Labeled 0

## Note :

- For a n-variable Boolean expression, the maximum number of literals = n
- For a n - variable k-map if grouping is done by considering  $2^m$  number of cells , then the resulting term from that group contains (n-m) number of literals
- 8 *cells* –  $2^3$  cells → Octet -----> 3 variables eliminated
- 4 *cells* –  $2^2$  cells → Quad -----> 2 variables eliminated
- 2 *cells* –  $2^1$  cells → Pair -----> 1 variables eliminated



$$f = \sum m(0, 3)$$

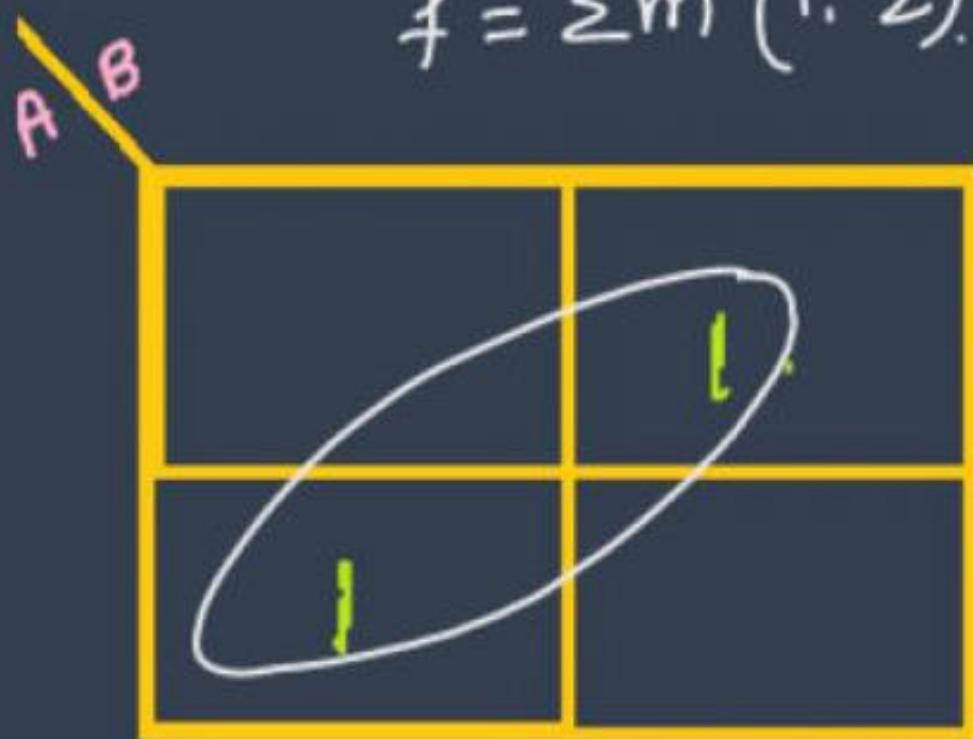
XOR

$A \oplus B$

$A \ominus B$

XOR.

$$f = \sum m(1, 2)$$



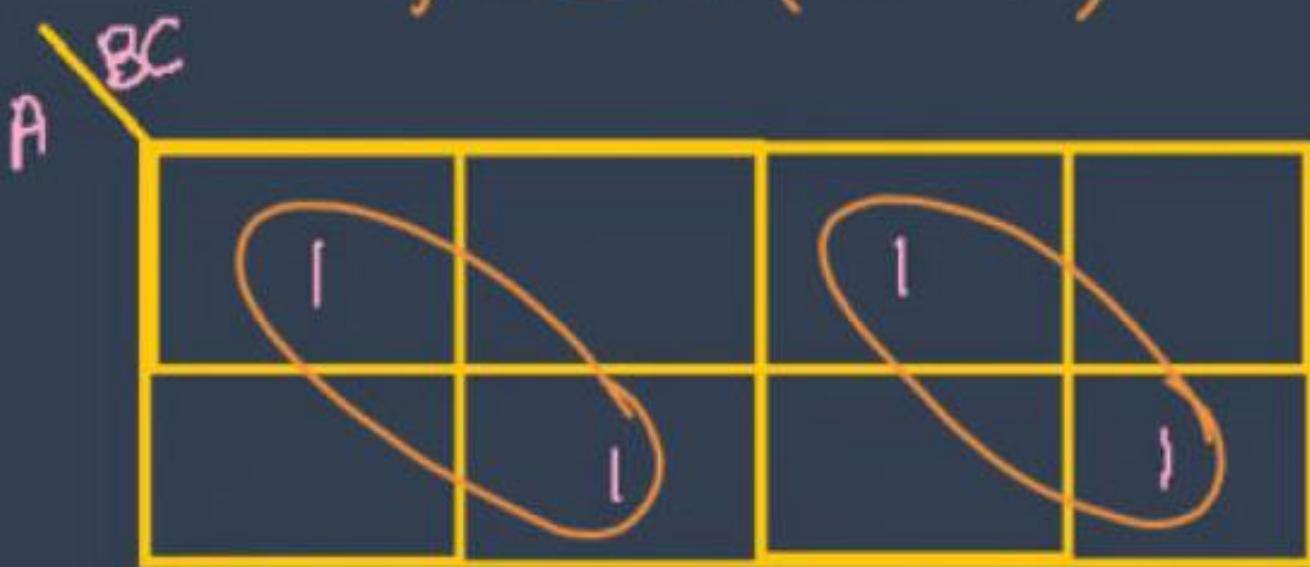


$$f = \sum m(1, 2, 4, 7)$$

$$f = A \oplus B \oplus C$$

$$f = A \oplus B \oplus C$$

$$f = \sum m(0, 3, 5, 6)$$



<del>AB</del>	<del>CD</del>			
		1		
			1	
				1
		1		

$$f = A \oplus B \oplus C \oplus D.$$

$$f = A \oplus B \oplus C \oplus D.$$

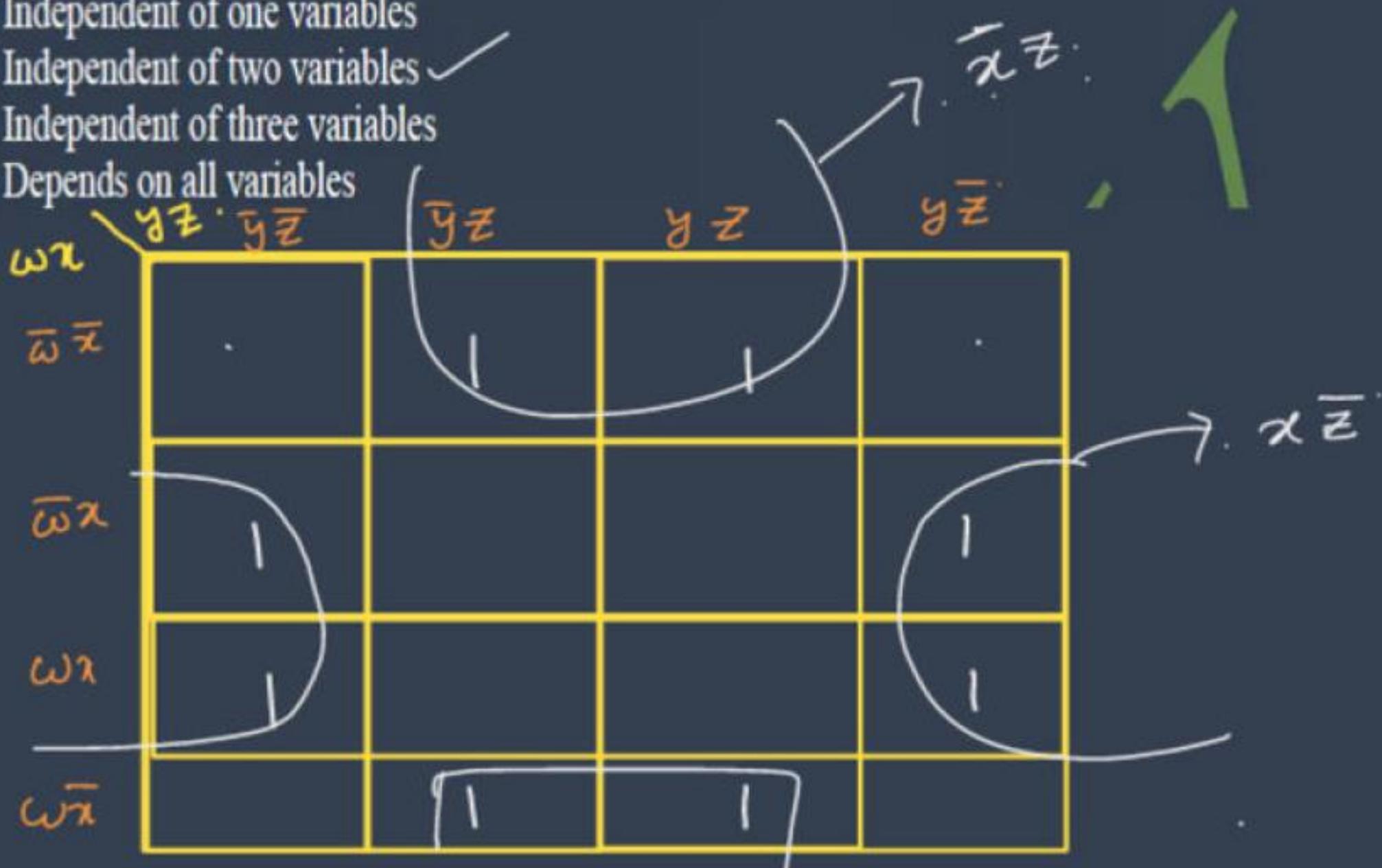
<del>AB</del>	<del>CD</del>			
			1	
		1		
				1
		1		

$$F(w, x, y, z) = \Sigma (1, 3, 4, 6, 9, 11, 12, 14)$$

the function is

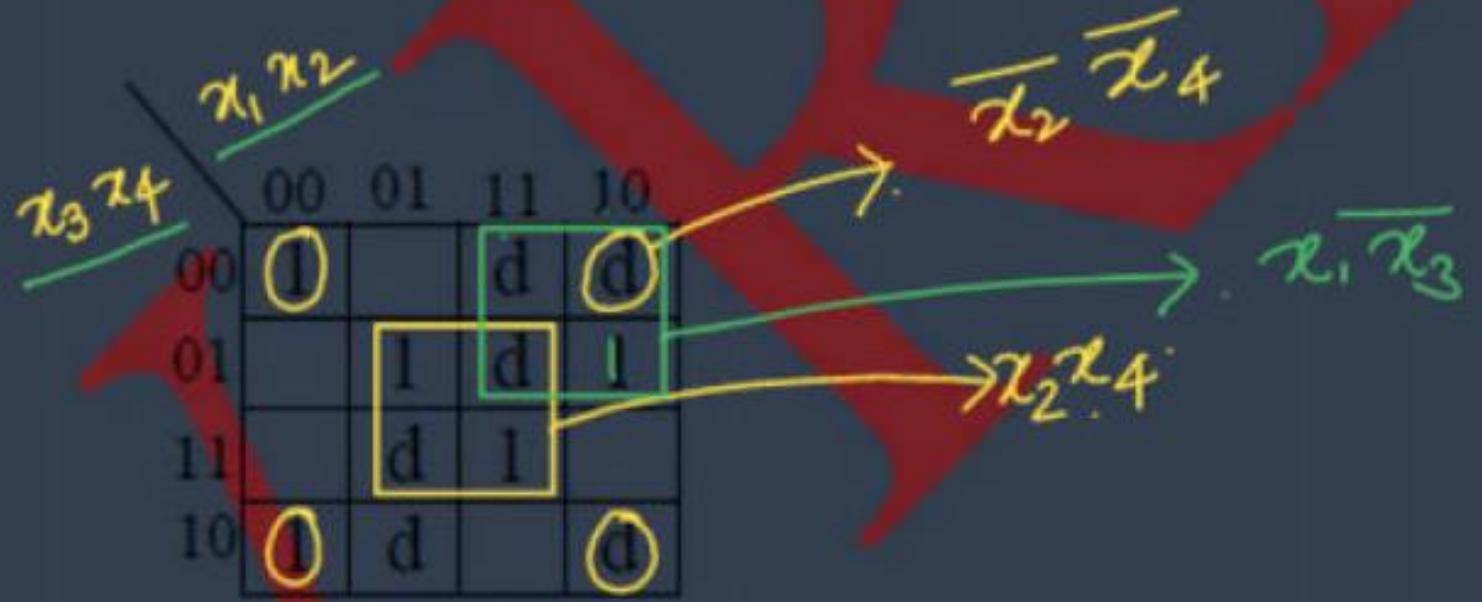
(GATE-CSIT-07)

- (a) Independent of one variables
- (b) Independent of two variables ✓
- (c) Independent of three variables
- (d) Depends on all variables



Consider the Karnaugh map given below:

The function represented by this map can be simplified to the minimal form as  
(IES-1997)



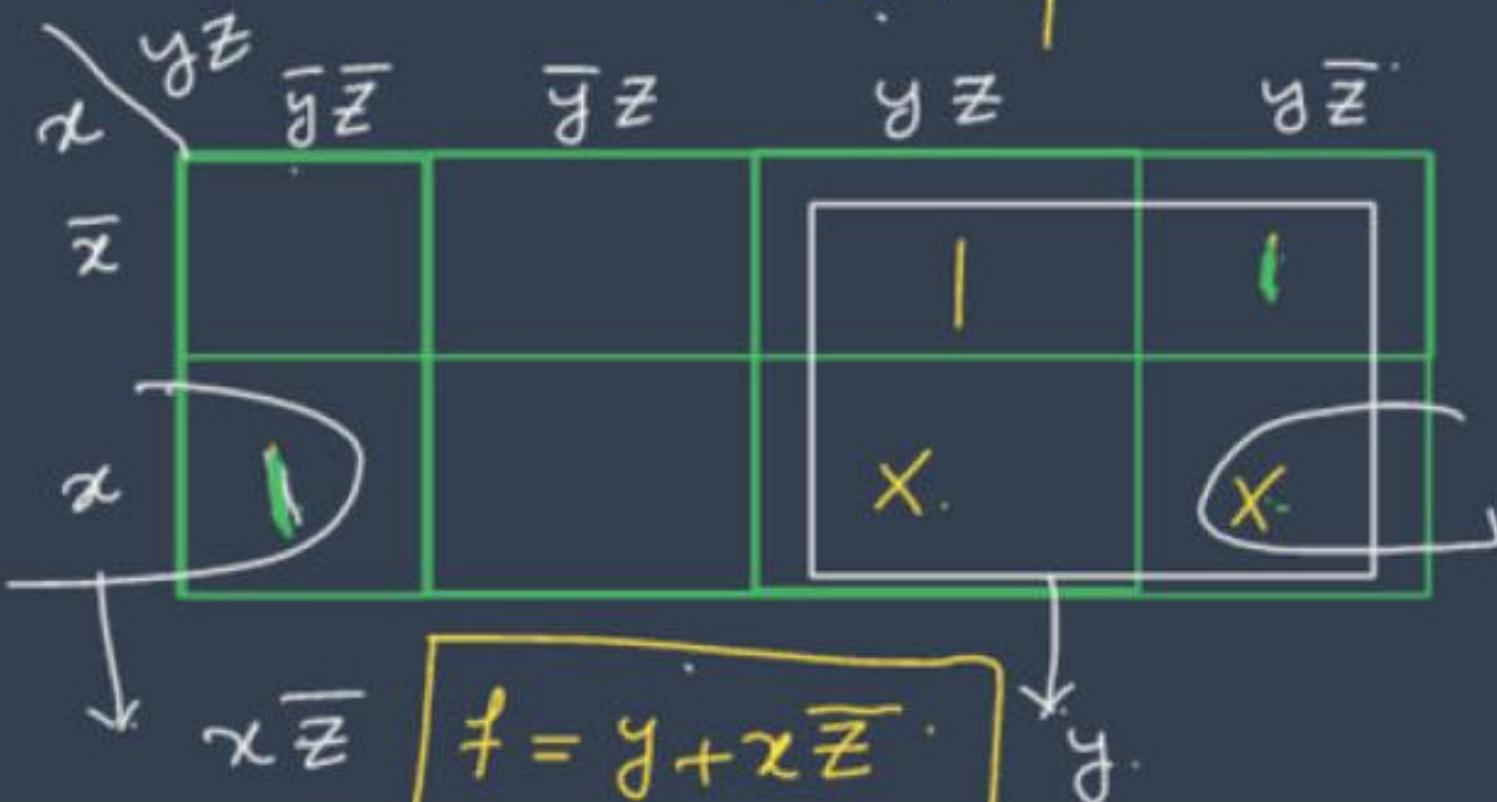
- (a)  $X_1 \bar{X}_2 \bar{X}_4 + X_2 X_4 + X_1 \bar{X}_3$
- (b)  $X_1 X_2 X_4 + X_2 X_4 + X_1 \bar{X}_2 \bar{X}_3 \bar{X}_4$
- (c)  $X_2 X_4 + \bar{X}_2 \bar{X}_4 + X_1 \bar{X}_3$  ✓
- (d)  $X_1 \bar{X}_2 \bar{X}_4 + \bar{X}_1 X_2 \bar{X}_3 X_4 + X_1 X_2 X_3 X_4 + X_1 \bar{X}_2 \bar{X}_3 \bar{X}_4$

Q) A logic circuit implement  $F = \bar{x}y + x\bar{y}\bar{z}$ , it is found that  $x = y = 1$  can never occur, considering this as fact, the minimized expression of F is.....

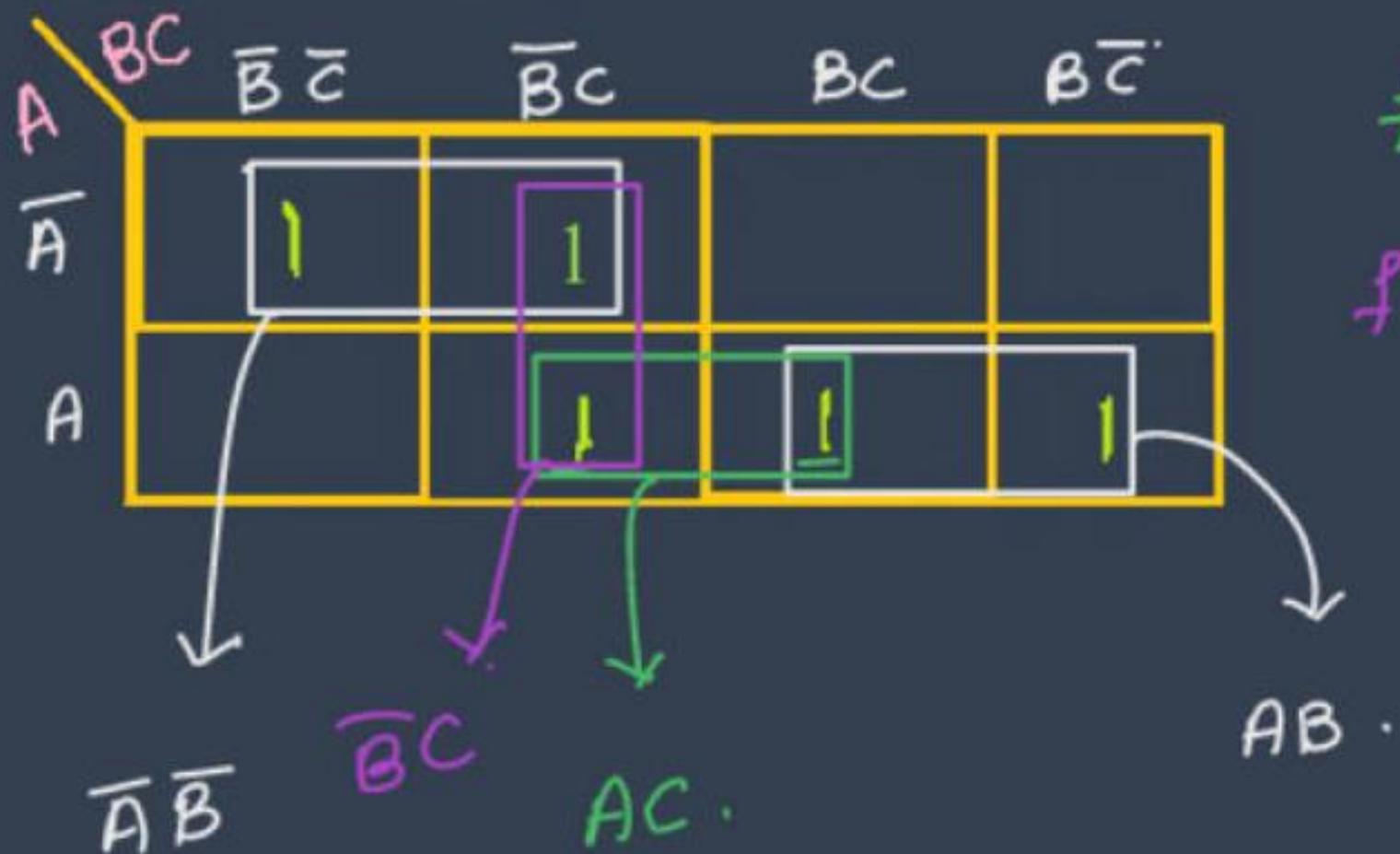
$x$	$y$	$z$	$f$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	X
1	1	1	X

$$f = \bar{x}y + x\bar{y}\bar{z}$$

010	100
011	.



Q) Minimize the following



$$f = \underline{\bar{A}\bar{B}} + \underline{AB} + \underline{AC} \quad (\text{or})$$

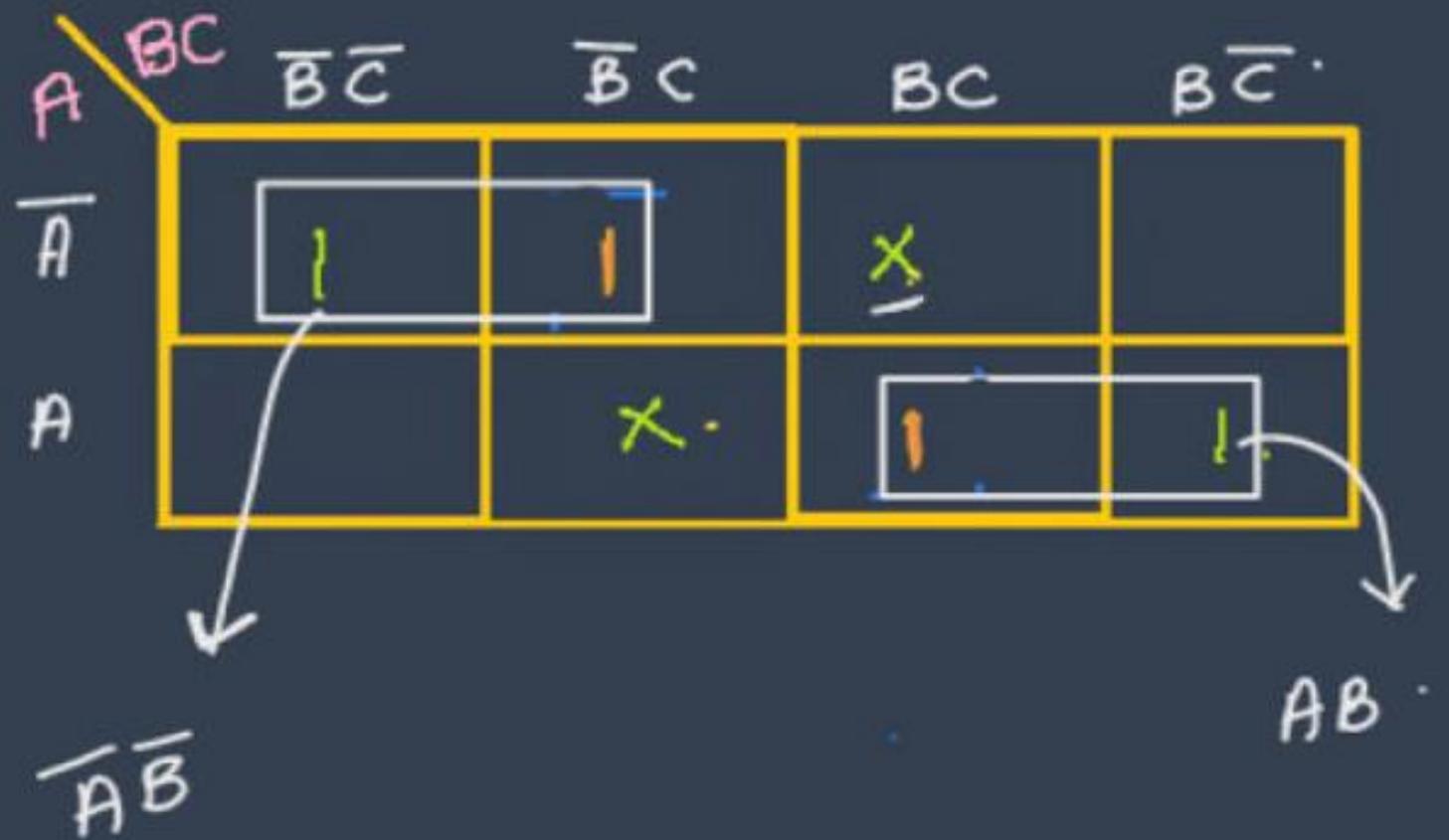
$$f = \underline{\bar{A}\bar{B}} + \underline{AB} + \underline{B\bar{C}}$$

$\bar{A}\bar{B}$  .

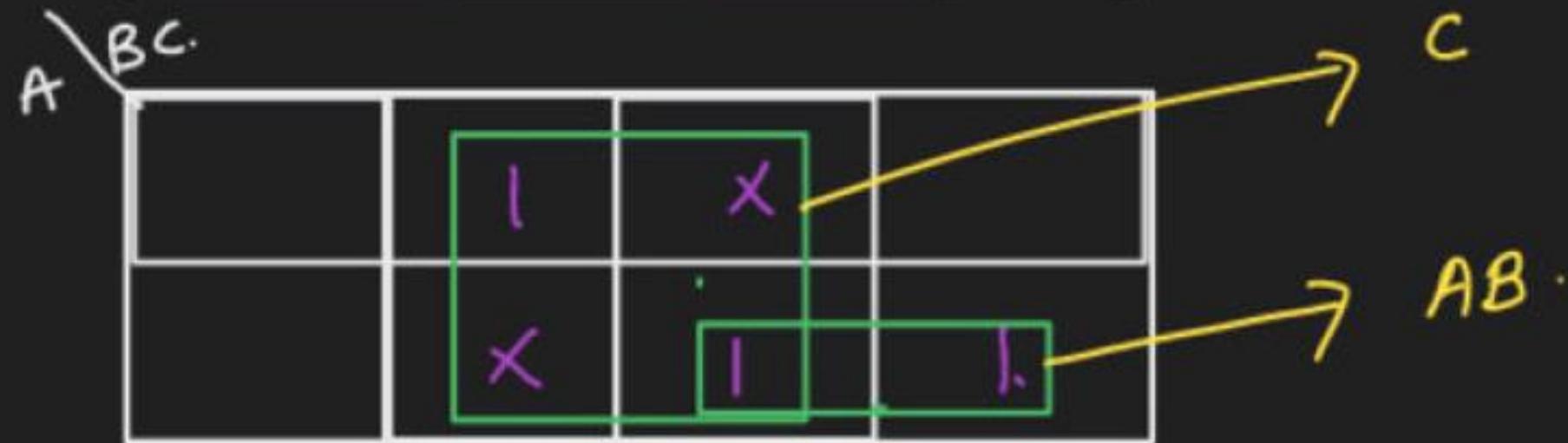
**NOTE:**

Minimal expression may not be **Unique**

Q) Minimize the following



$$f = \overline{A}\overline{B} + AB$$



# Minterm :

Each product term in the canonical SOP expression is called a minterm

# Maxterm :

Each sum term in the canonical POS expression is called a maxterm

## Implicant ,Prime Implicant , Essential Prime Implicant

**Implicant :** Each minterm in canonical SOP expression is known as Implicant .

**Prime Implicant ( PI ):**

Prime Implicant is a product term , obtained by combining maximum possible cells in the K-Map. While doing so make sure that a smaller group is not completely inside a bigger group .

**Essential Prime Implicant ( EPI ) :**

A prime Implicant is an EPI , if and only if it contains at least one minterm which is not covered by multiple groups .

**All EPI's are PI's , but vice versa not true**

$$\text{EPI} \leq \text{PI}$$

# False Minterms

The maxterms are called as False Minterms

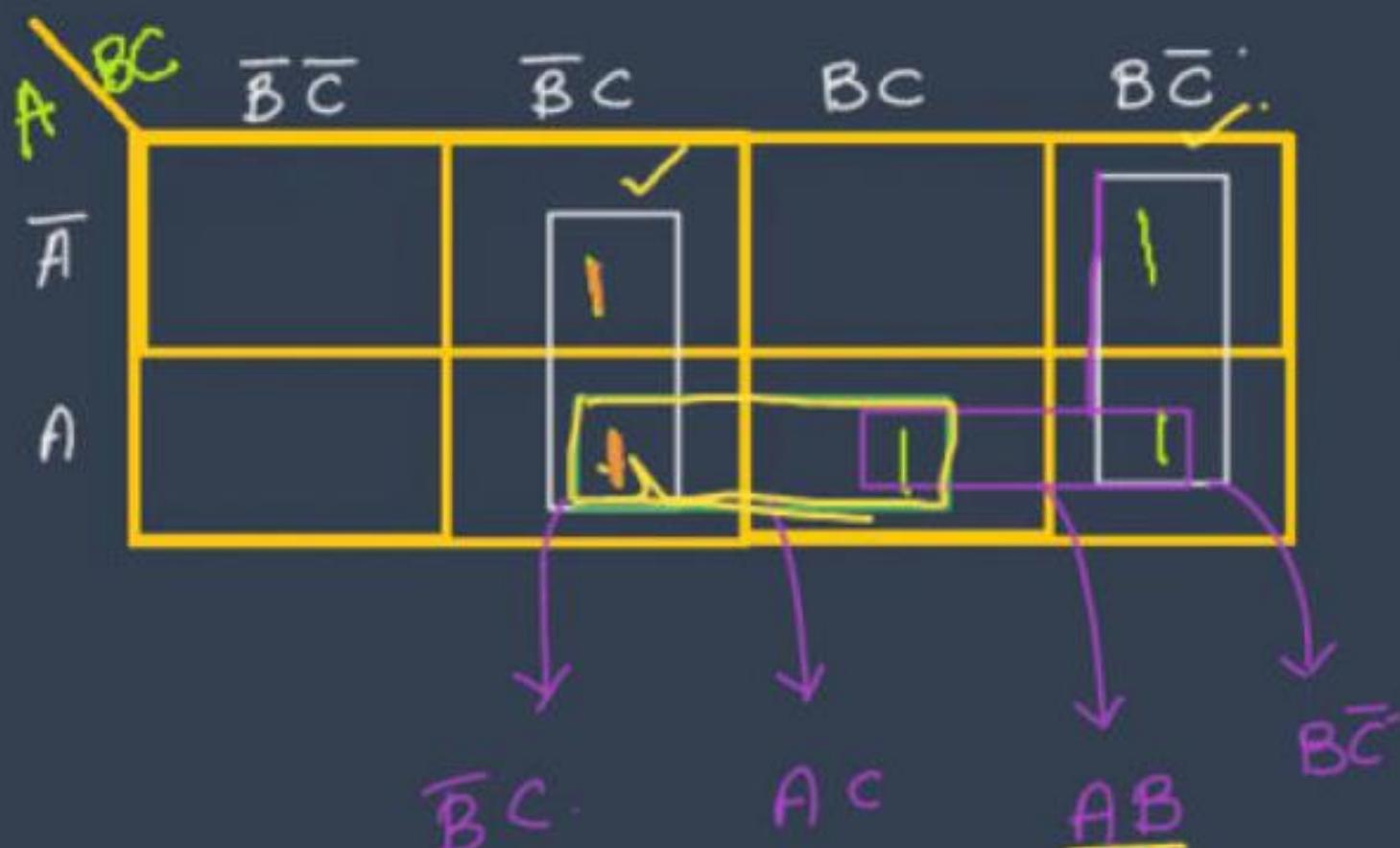
## False Prime Implicants

Prime Implicants obtained using the maxterms are called as False Prime Implicants

### Essential false Prime Implicants

A False Prime Implicant is said to be an Essential False Prime Implicants , if and only if it contains at least one maxterm which is not covered by multiple groups

Q) Find the number of Prime Implicants and Essential Prime Implicants



$$\underline{\text{PI}} = 4$$

$\bar{B}C$ ,  $\cancel{AC}$ ,  $\cancel{AB}$ ,  $\underline{B\bar{C}}$

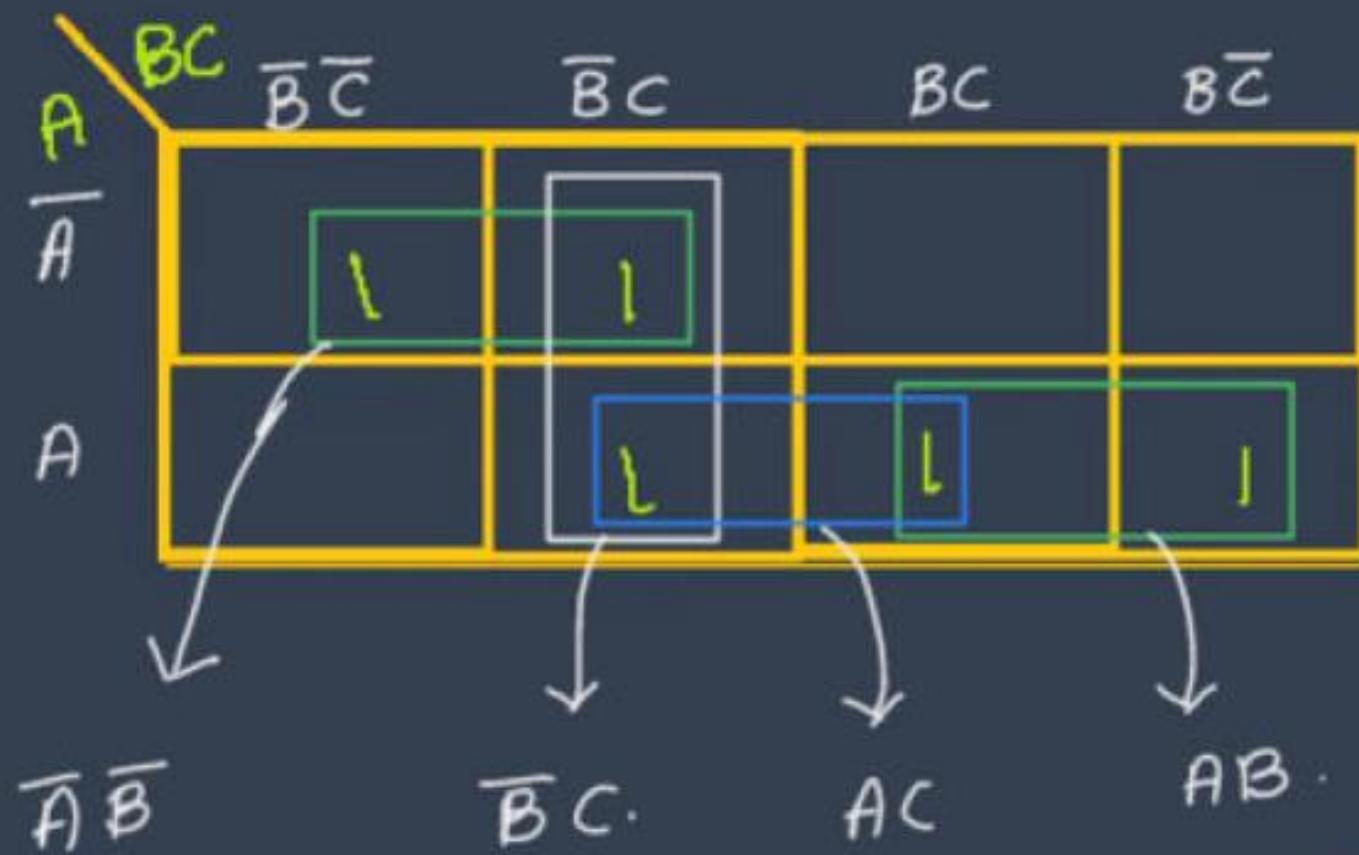
$$\underline{\text{EPI}} = 2$$

$\bar{B}C$ ,  $B\bar{C}$

$$f = \bar{B}C + B\bar{C} + AC \quad (\alpha)$$

$$f = \bar{B}C + B\bar{C} + AB$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



$$f = \bar{A}\bar{B} + AB + \bar{B}C \quad (\text{or})$$

$$= \bar{A}\bar{B} + AB + AC$$

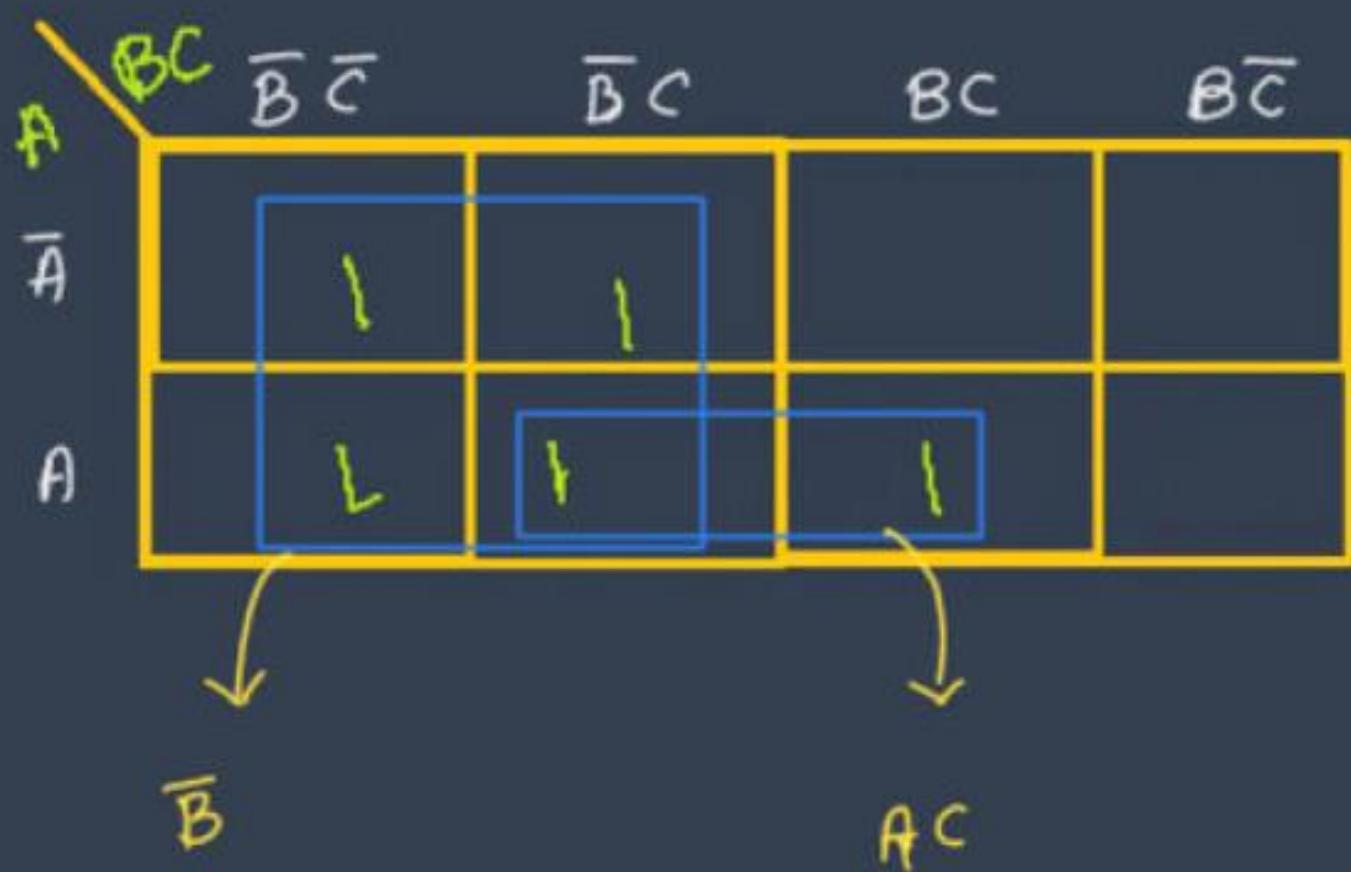
PI

$\bar{A}\bar{B}$ ,  $\bar{B}C$ ,  $AC$ ,  $AB$ .

EPI

$\bar{A}\bar{B}$ ,  $AB$

Q) Find the number of Prime Implicants and Essential Prime Implicants



PI

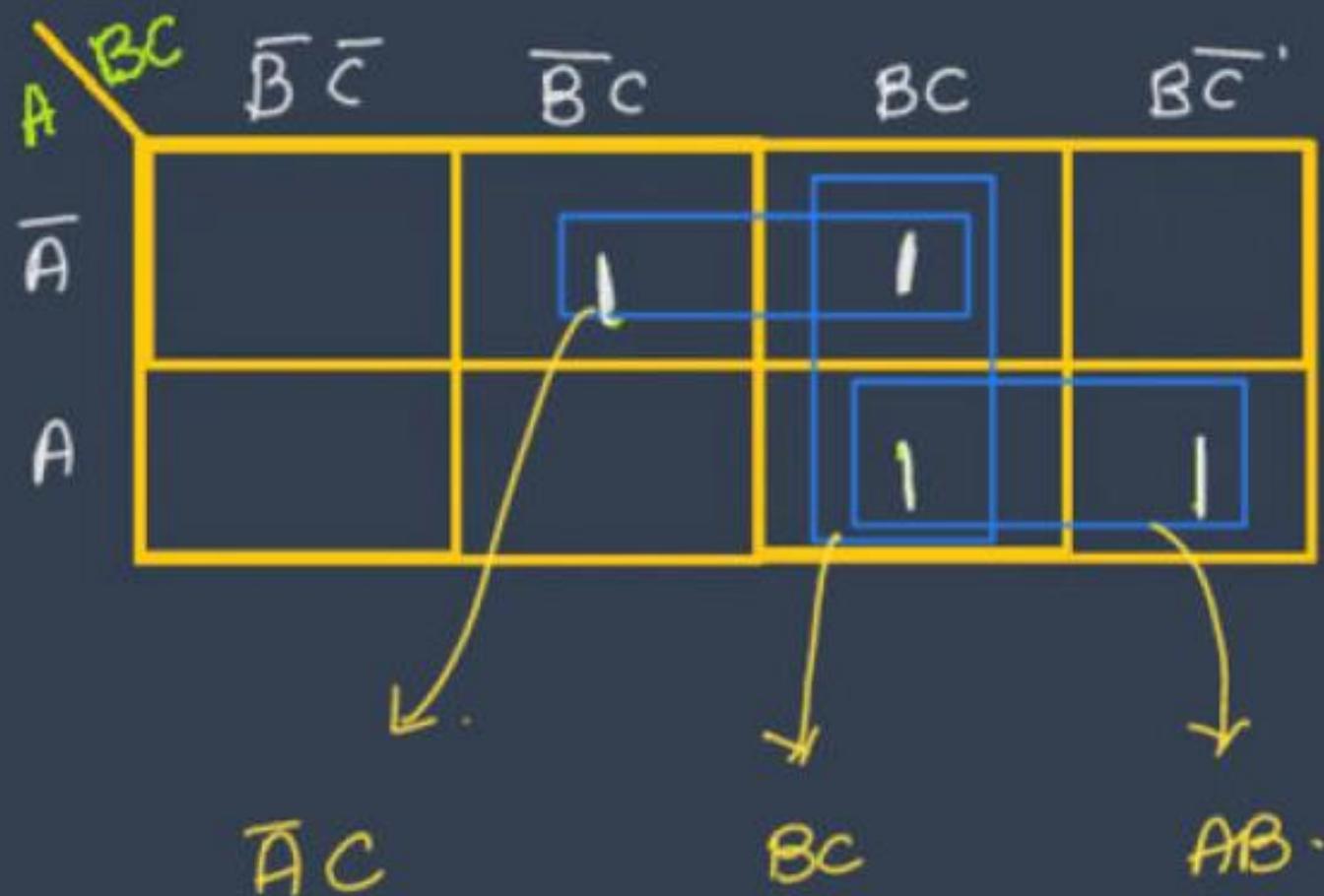
$\bar{B}$ ,  $AC$ .

EPI

$\bar{B}$ ,  $AC$ .

$$f = \bar{B} + AC + 0$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



PI

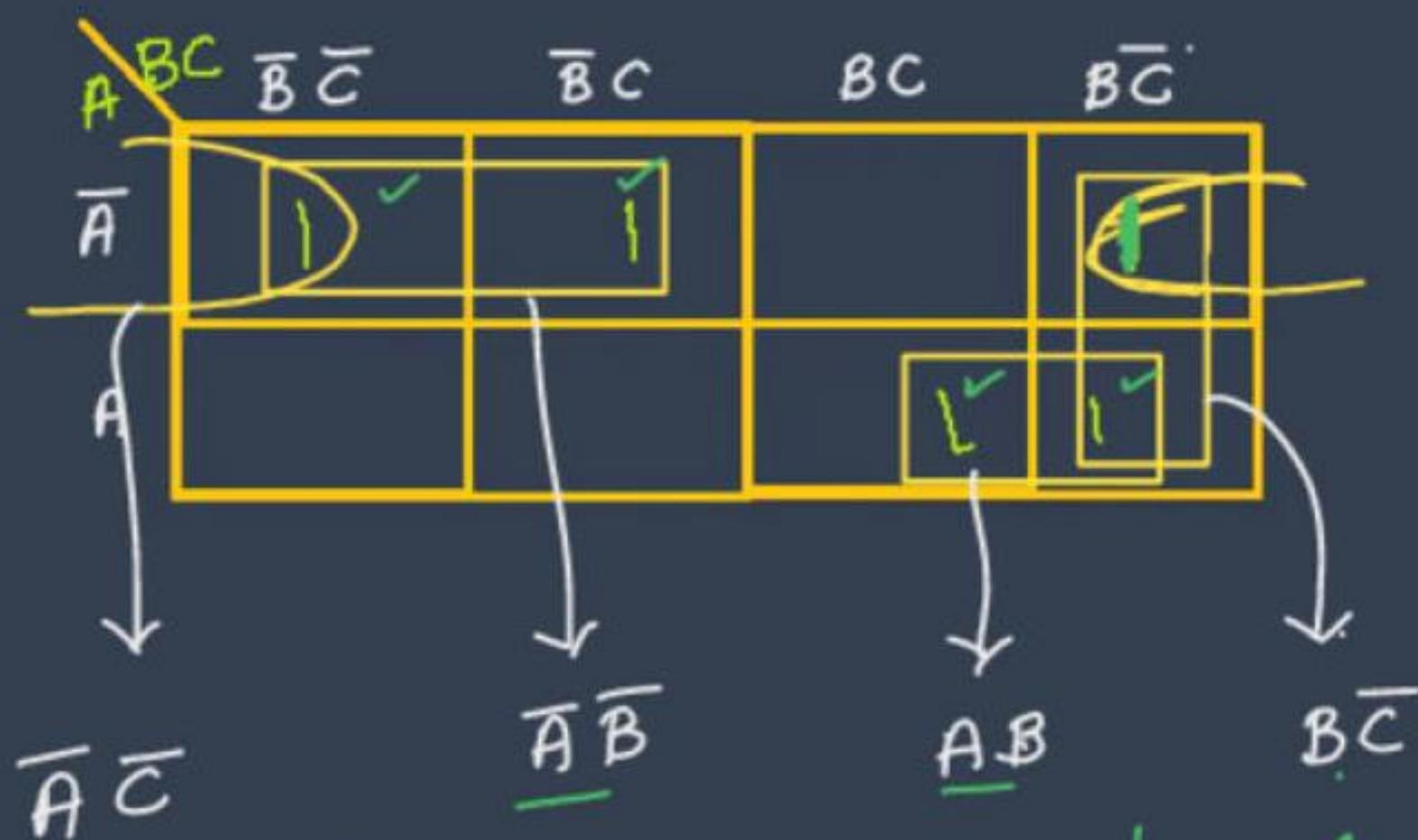
$\bar{A}C, BC, AB$

EPI

$\bar{A}C, AB$

$$f = \bar{A}C + AB + 0$$

Q) Find the number of Prime Implicants and Essential Prime Implicants

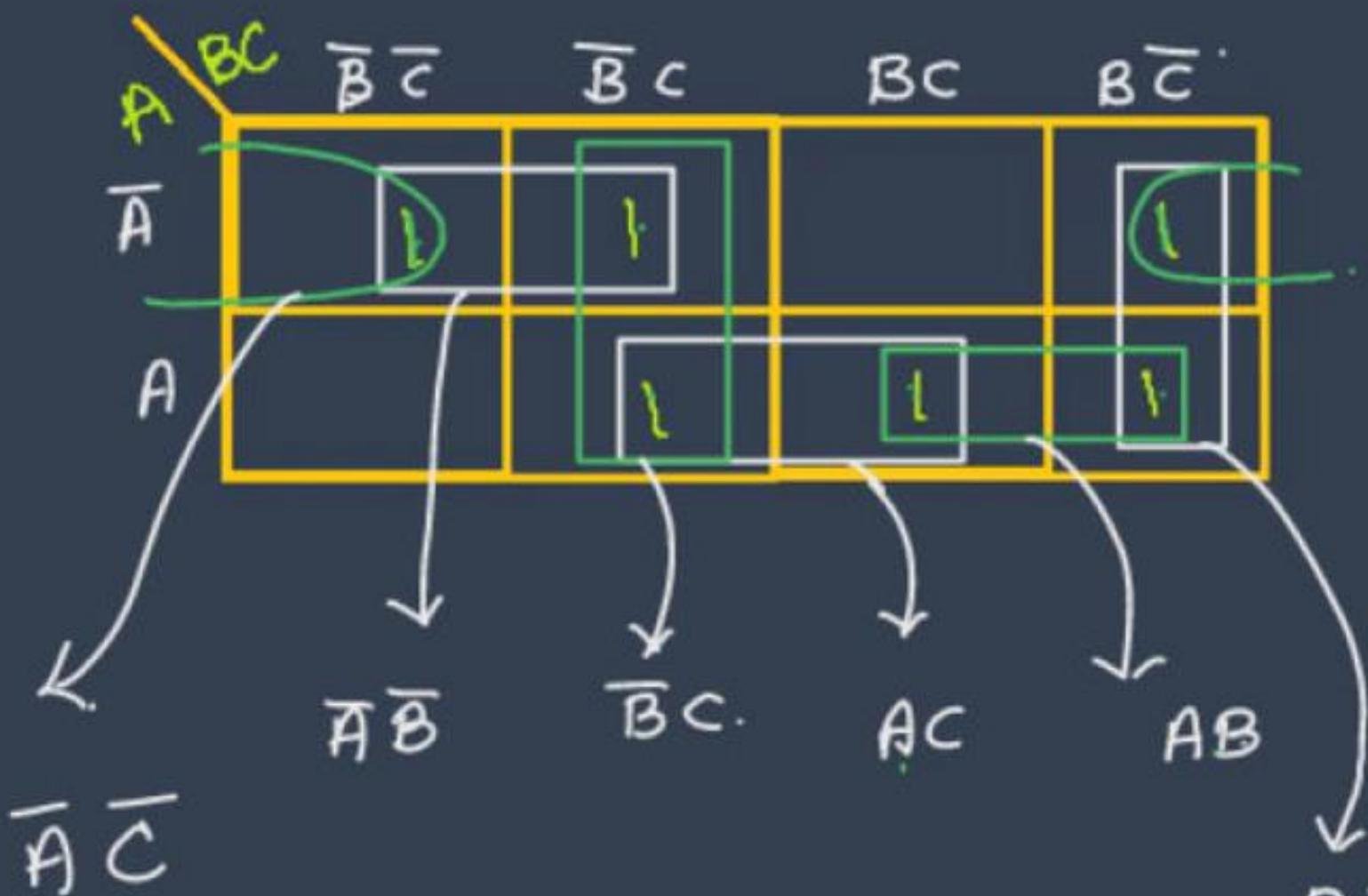


PI  
 $\bar{A}\bar{C}, \bar{A}\bar{B}, AB, BC'$

EPI  
 $\bar{A}\bar{B}, AB$

$$f = \bar{A}\bar{B} + AB + BC' \quad | \text{(or)} \quad f = \bar{A}\bar{B} + AB + \bar{A}\bar{C}$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



PI

$\bar{A}\bar{C}$ ,  $\bar{A}\bar{B}$ ,  $\bar{B}C$ ,  $AC$   
 ~~$\bar{A}B$~~   $BC$

EPI = 0

$$f = \bar{A}\bar{B} + AC + BC$$

$$f = \bar{A}\bar{C} + \bar{B}C + AB$$

Q) Find the number of Prime Implicants and Essential Prime Implicants

$A$	$\bar{B}C$	$\bar{B}\bar{C}$	$\bar{B} c$	$Bc$	$B\bar{C}$
$\bar{A}$			L	I	
$A$		L		I	

PI

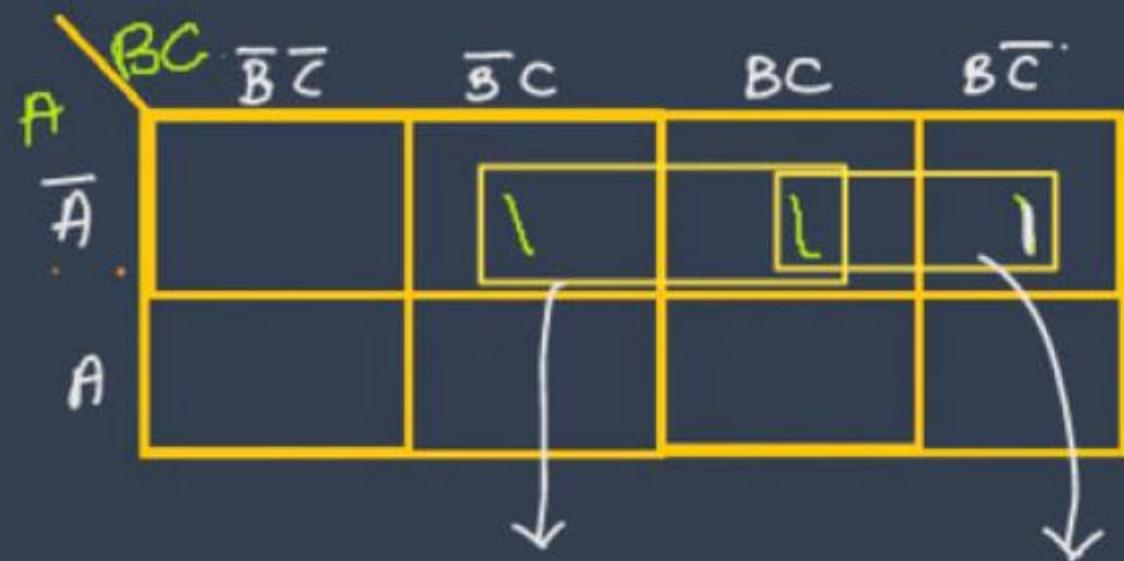
c

EPI

c.

$$f = c$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



PI

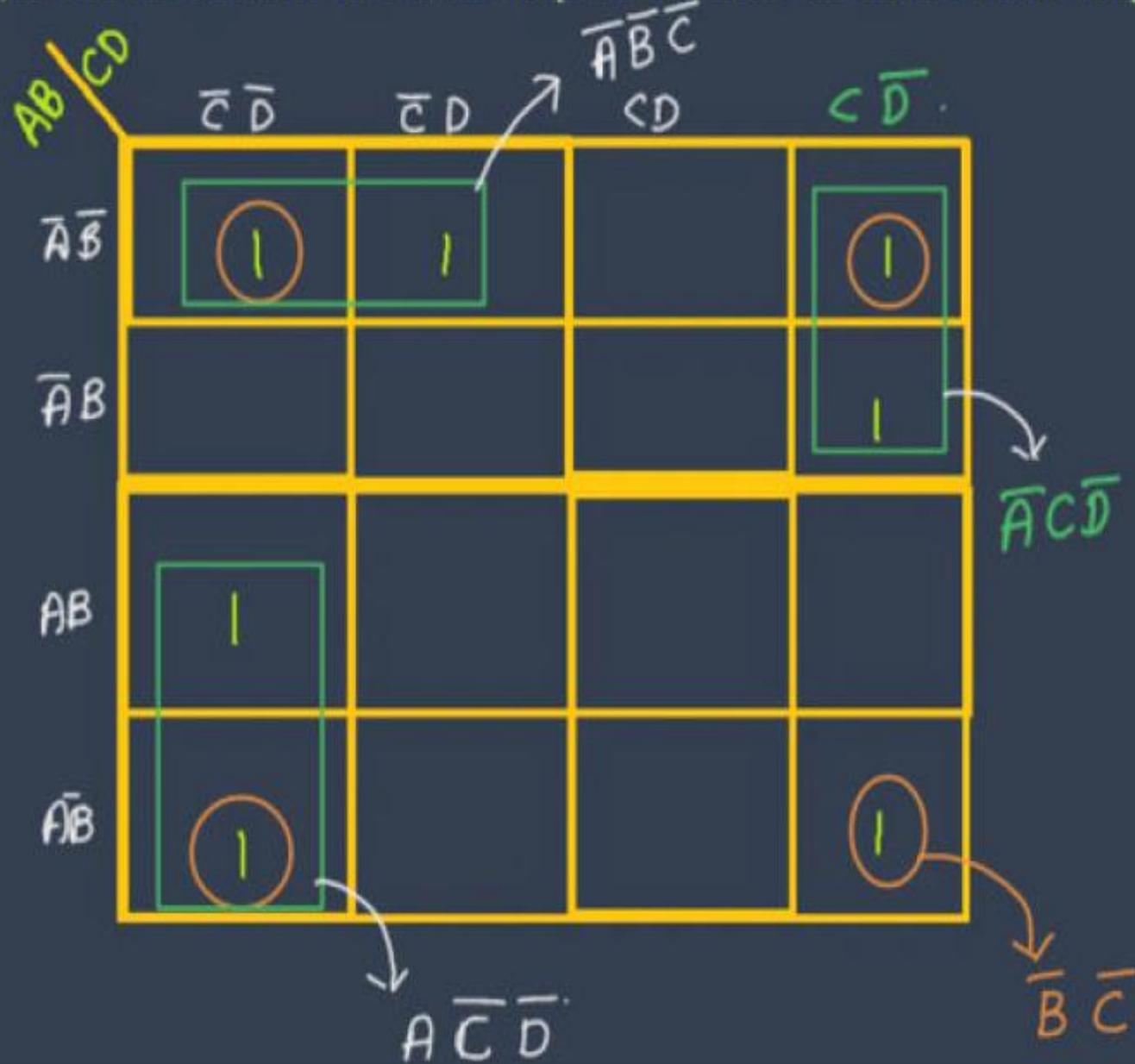
$\bar{A}C$ ,  $\bar{A}B$ .

EPI

$\bar{A}C$ ,  $\bar{A}B$ .

$$f = \bar{A}C + \bar{A}B$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



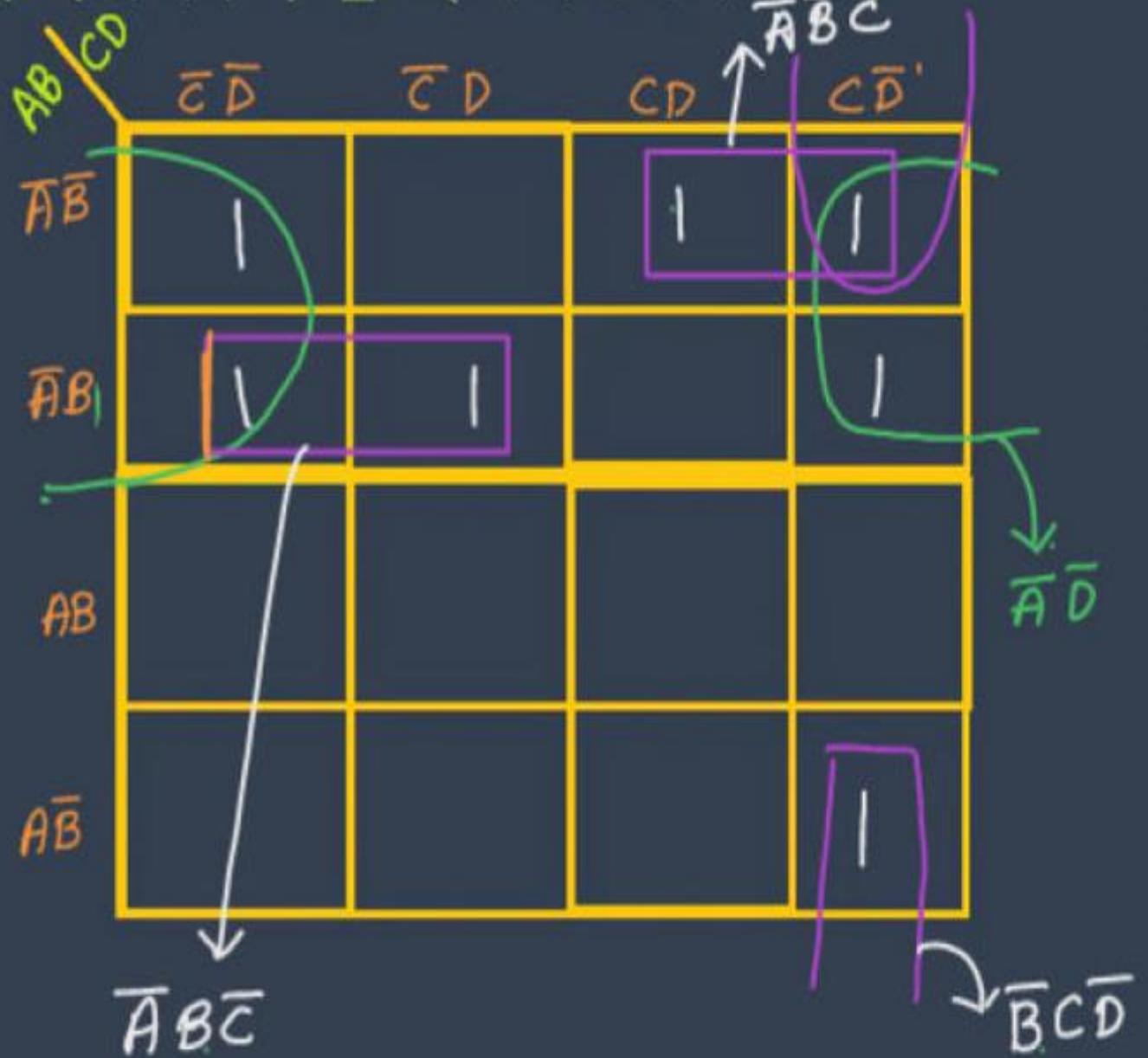
PI

$\bar{B}\bar{C}$ ,  $A\bar{C}\bar{D}$ ,  $\bar{A}C\bar{D}$   
 $\bar{A}\bar{B}\bar{C}$

EPI

$\bar{B}\bar{C}$ ,  $A\bar{C}\bar{D}$ ,  $\bar{A}C\bar{D}$   
 $\bar{A}\bar{B}\bar{C}$ .

$$Q) F(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 6, 10)$$



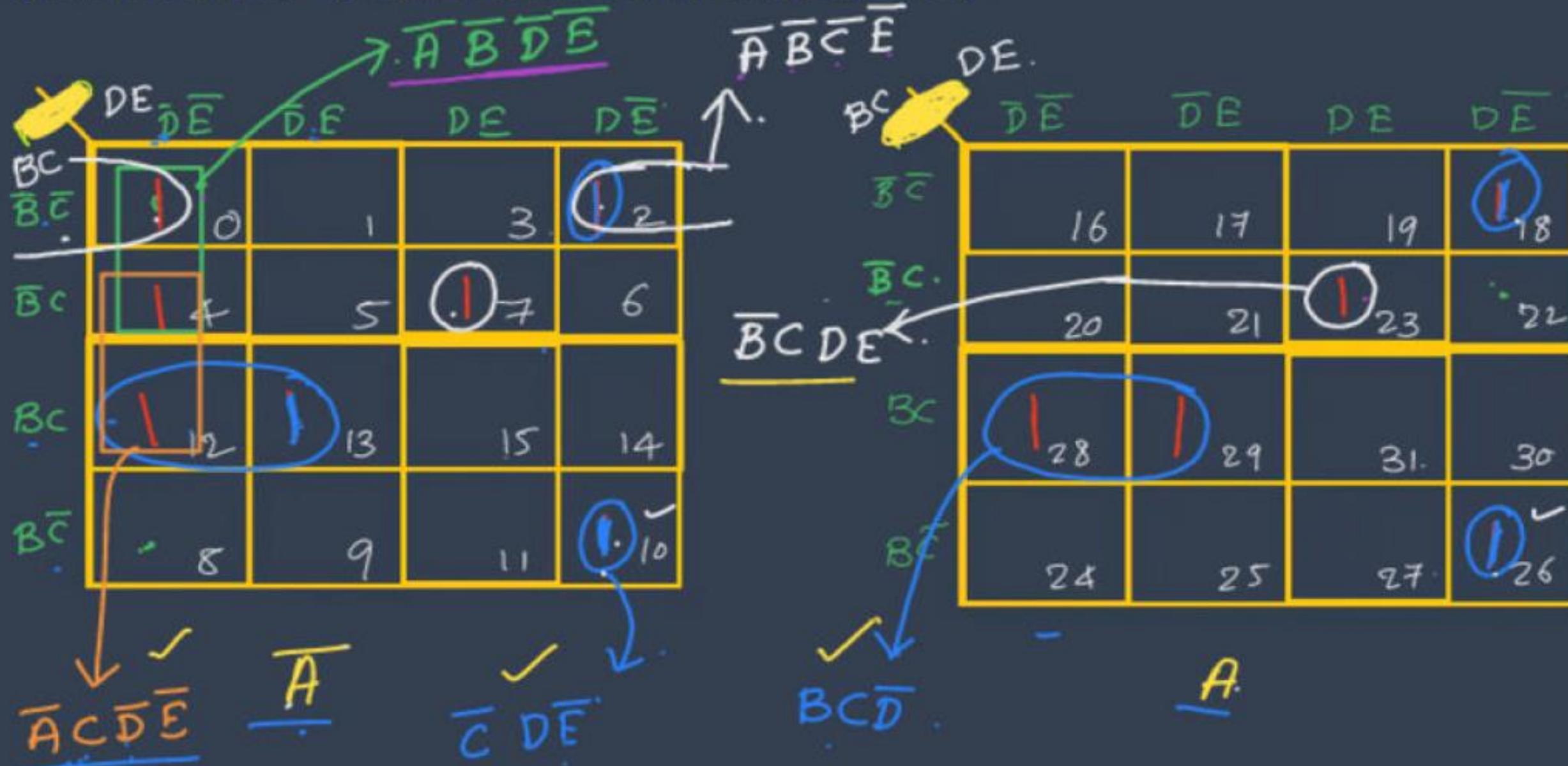
PI  
 $\overline{A}\overline{D}, \overline{A}B\overline{C}, \overline{B}C\overline{D}, \overline{A}\overline{B}C$

EPI  
 $\overline{A}D, \overline{A}B\overline{C}, \overline{B}C\overline{D}$   
 $\overline{A}\overline{B}C$ .

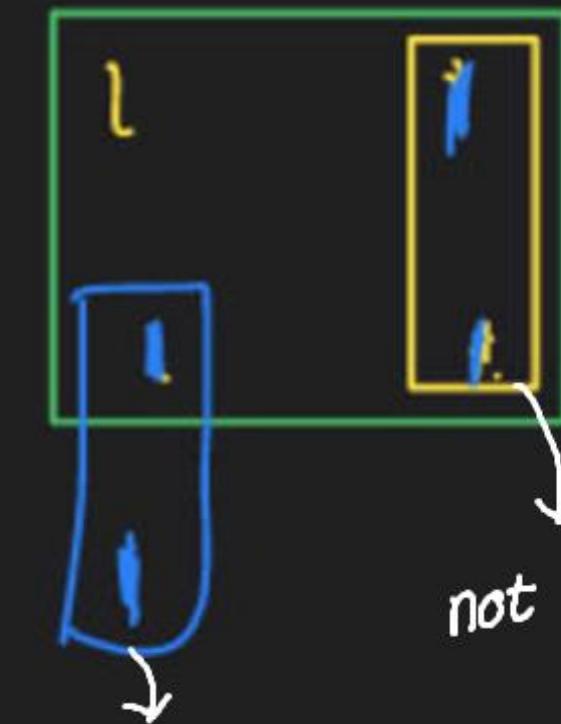
# NOTE:

- The minimal expression = ( All EPI's ) + ( Optional PI's )
- If all PI's are EPI's , then the minimal expression is unique
- The sufficient condition for a K-map to have unique solution is the number of PI's = number of EPI's

$$Q) F(A, B, C, D, E) = \sum m(0, 2, 4, 7, 10, 12, 13, 18, 23, 26, 28, 29)$$



$$\begin{array}{c}
 \text{PI} \\
 \overline{A} C \bar{D} \bar{E}, \\
 \bar{C} D \bar{E}, \\
 B C \bar{D}, \\
 \overline{B} C D E \\
 \hline
 \overline{A} \bar{B} \bar{D} \bar{E} \\
 \bar{A} \bar{B} \bar{C} \bar{E}.
 \end{array}
 \quad \left| \quad
 \begin{array}{c}
 \text{EPI} \\
 \bar{C} D \bar{E} \\
 B C \bar{D} \\
 \overline{B} C D E
 \end{array}
 \right.$$



*not allowed.*

*allowed.*

How many minterms (excluding redundant terms) does the minimal switching function

$f(y, w, x, y, z) = \underline{xy} + \underline{yz}$  originally have?

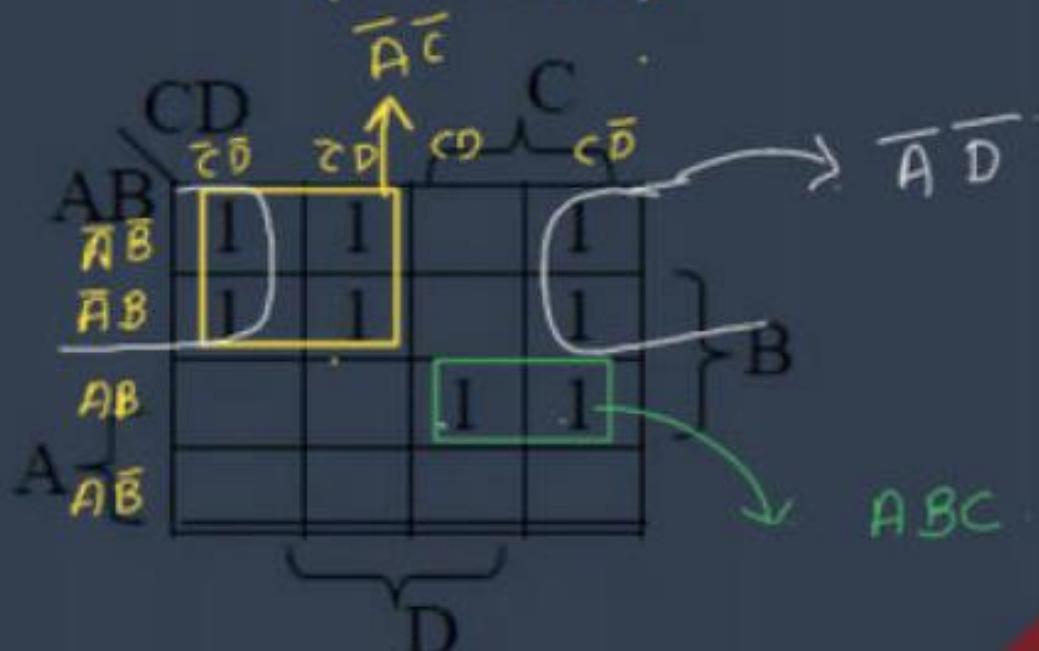
- (a) 16      (b) 20 ✓  
(c) 24 ✗      (d) 32

$wx$	$yz$	$\bar{y}\bar{z}$	$\bar{y}z$	$y\bar{z}$	$yz$
$\bar{w}\bar{x}$		1			
$\bar{w}x$	1	1 1	1	1	
$w\bar{x}$	1	1 1	1	1	
$w\bar{x}$		1			

(IES-1998)

$wx$	$yz$	$\bar{y}\bar{z}$	$\bar{y}z$	$y\bar{z}$	$yz$
$\bar{w}\bar{x}$		1			
$\bar{w}x$	1	1 1	1	1	
$w\bar{x}$	1	1 1	1	1	
$w\bar{x}$		1			

The simplified Boolean expression from the Karnaugh map given in the figure is  
**(IES-1995)**



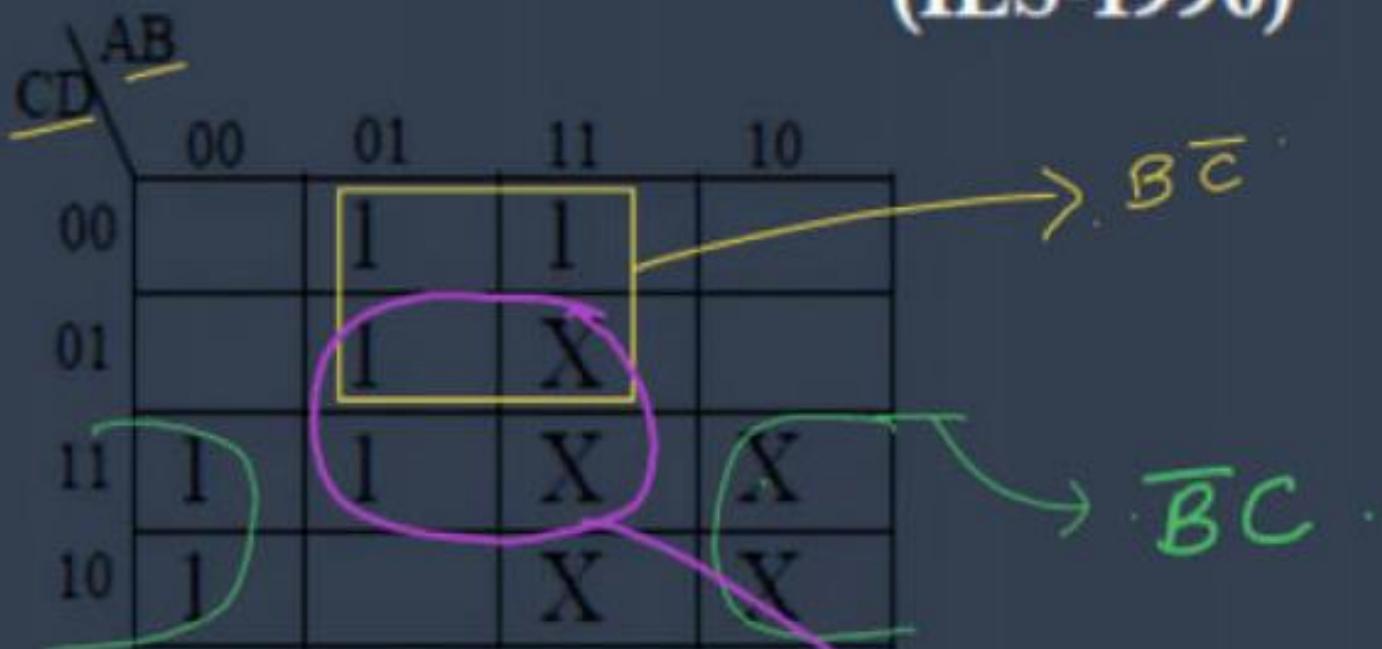
$$\overline{AC} + \overline{AD} + ABC \quad \checkmark$$

(b)  $\overline{AB} + \overline{AD} + ABC$

(c)  $AC + ACD + ABC + BCD\bar{D}$

(d)  $\overline{AB} + \overline{CD} + \overline{AD}$

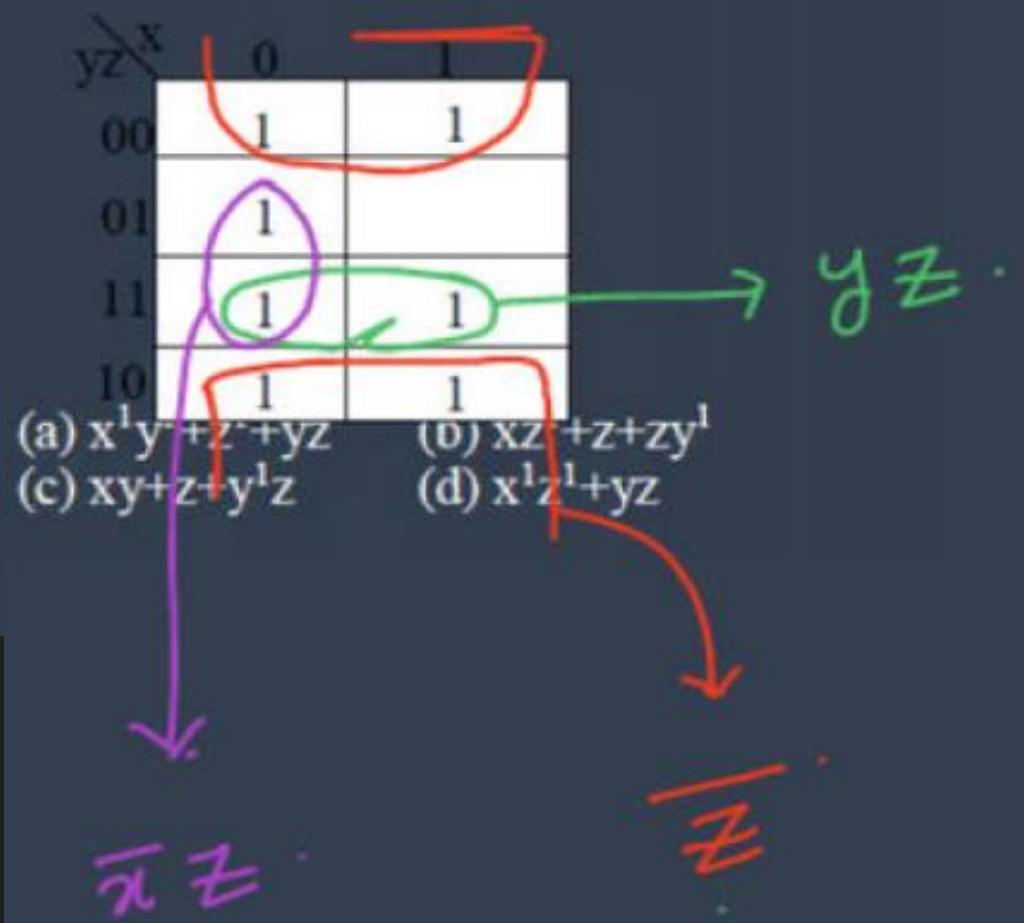
The minimized expression for the given K – map is ( X: don't care)  
(IES-1996)



- (a)  $\bar{C}B + BD + CD$  ✗
- (b)  $AB + \underline{C \bar{B}} + \underline{B \bar{C}}$
- (c)  $C \bar{B} + AC + B \bar{C}$
- (d)  $\bar{C}B + BD + C \bar{B}$  ✓

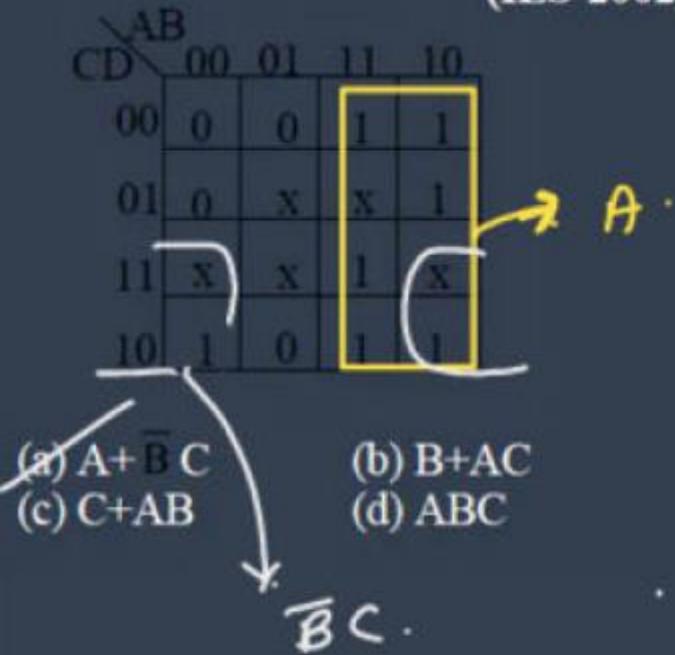
- a)  $\bar{B}C + B\bar{C} + BD$  ✓
- b)  $\bar{B}C + B\bar{C} + CD$  ✓

For the Karnaugh map shown in the given figure, the minimum Boolean function is  
(IES-2001)

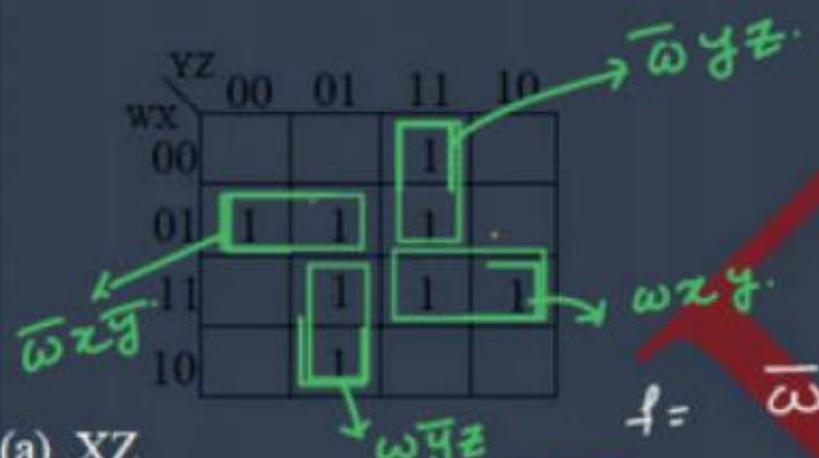


figure, the minimum Boolean function is

The minimized expression for the given Kmap(x: don't care) is  
(IES-2002)



What is the minimized logic expression corresponding to the given Karnaugh Map?  
(IES-2005)



- (a) XZ
- (b)  $\bar{W}X\bar{Y} + \bar{W}YZ + W\bar{Y}Z + WXY$  ✓
- (c)  $\bar{W}X\bar{Y} + \bar{W}YZ + WY\bar{Z} + W\bar{X}\bar{Y}$
- (d)  $XZ + \bar{W}YZ + WXY + WXY + W\bar{Y}Z$  ✗

$$f = \cancel{\bar{W}X\bar{Y}} + \bar{W}\bar{Y}Z + WXY + \bar{W}Y\bar{Z} + \underline{\underline{XZ}}$$
$$f = \bar{W}X\bar{Y} + \bar{W}\bar{Y}Z + WXY + \bar{W}Y\bar{Z}$$

43. When the Boolean function

$F(X_1X_2X_3) = \sum(0, 1, 2, 3) + \sum_{\phi}(4, 5, 6, 7)$  is minimized, what does one get?

(IES-2007)

- (a) 1
- (b) 0
- (c)  $X_1$
- (d)  $X_3$

A Karnaugh map for three variables  $X_1$ ,  $X_2$ , and  $X_3$ . The columns represent  $X_2X_3$  and the rows represent  $X_1$ . The map shows the following minterms marked with a green '1': (0,0,0), (0,0,1), (0,1,0), and (1,1,1). The other cells are marked with a green 'X'.

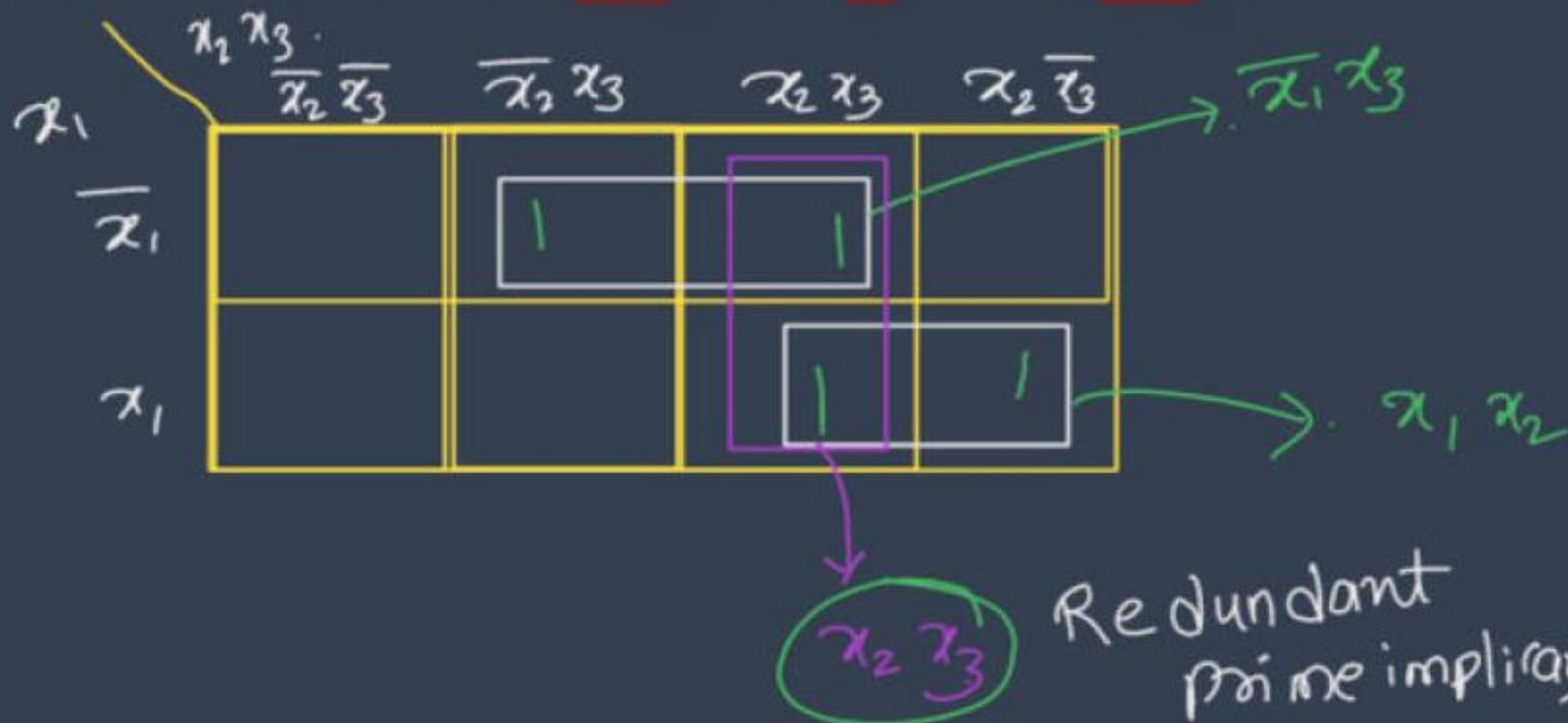
$X_2X_3$	00	01	10	11
$X_1$	0	1	1	1
0	X	X	X	X
1	1	1	1	1

An arrow points from the bottom-right corner of the Karnaugh map to the expression  $\bar{X}_1$ .

By inspecting the Karnaugh map plot of the switching function  $F(X_1 X_2 X_3) = \sum(1, 3, 6, 7)$  can say that the redundant prime implicant is

(IES-2007)

- (a)  $\bar{X}_1 X_3$
- (b)  $X_2 X_3$
- (c)  $X_1 X_2$
- (d)  $X_3$



For a function F, the Karnaugh map is shown in the figure below. Then minimal representation of F is (IES-10)

A	BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1	1	1	
A		1	1		

- (a)  $AB + \bar{C}$       (b)  $C + \bar{A}B$  ✓  
(c)  $A + B + C$       (d)  $A + \bar{B}C$

Consider the following expressions:

1.  $Y = f(A, B, C, D)$   
 $= \Sigma(1, 2, 4, 7, 8, 11, 13, 14)$  ✓
2.  $Y = f(A, B, C, D)$   
 $= \Sigma(3, 5, 7, 10, 11, 12, 13, 14)$
3.  $Y = f(A, B, C, D)$   
 $= \Pi(0, 3, 5, 6, 9, 10, 12, 15)$  ✓
4.  $Y = f(A, B, C, D)$   
 $= \Pi(0, 1, 2, 4, 6, 8, 9, 15)$

Which of these expressions are equivalents  
of the expression (IES-14)

$$Y = A \oplus B \oplus C \oplus D?$$

- (a) 1 and 2      (b) 1 and 4  
(c) 2 and 3      (d) 1 and 3 ✓

$$Y = \Sigma m (1, 2, 4, 7, 8, 11, 13, 14)$$

$$Y = \Pi M (0, 3, 5, 6, 9, 10, 12, 15)$$

A combinational circuit has input A, B and C and its Karnaugh Map is as shown. The output of the circuit is given by (IES-97)

		A\B	00	01	11	10
		C	0	1		1
		0	1		1	
		1				

- (a)  $(\bar{A}B + A\bar{B})C$       (b)  $(\bar{A}B + A\bar{B})\bar{C}$   
(c)  $\bar{A}\bar{B}\bar{C}$       ~~(d)  $A \oplus B \oplus C$~~

For a four variable K-Map, if each cell is assigned one integer value in range 0-15 then which is the cells adjacent to the cell corresponding to decimal value 7 ?

(IES-15)

- (a) 3, 5, 6 and 8
- (b) 3, 5, 10 and 11
- (c) 3, 5, 6 and 15
- (d) 4, 6, 8 and 15

0	1	3	2
4	5	7	6
12	13	15	14
8	9	11	10

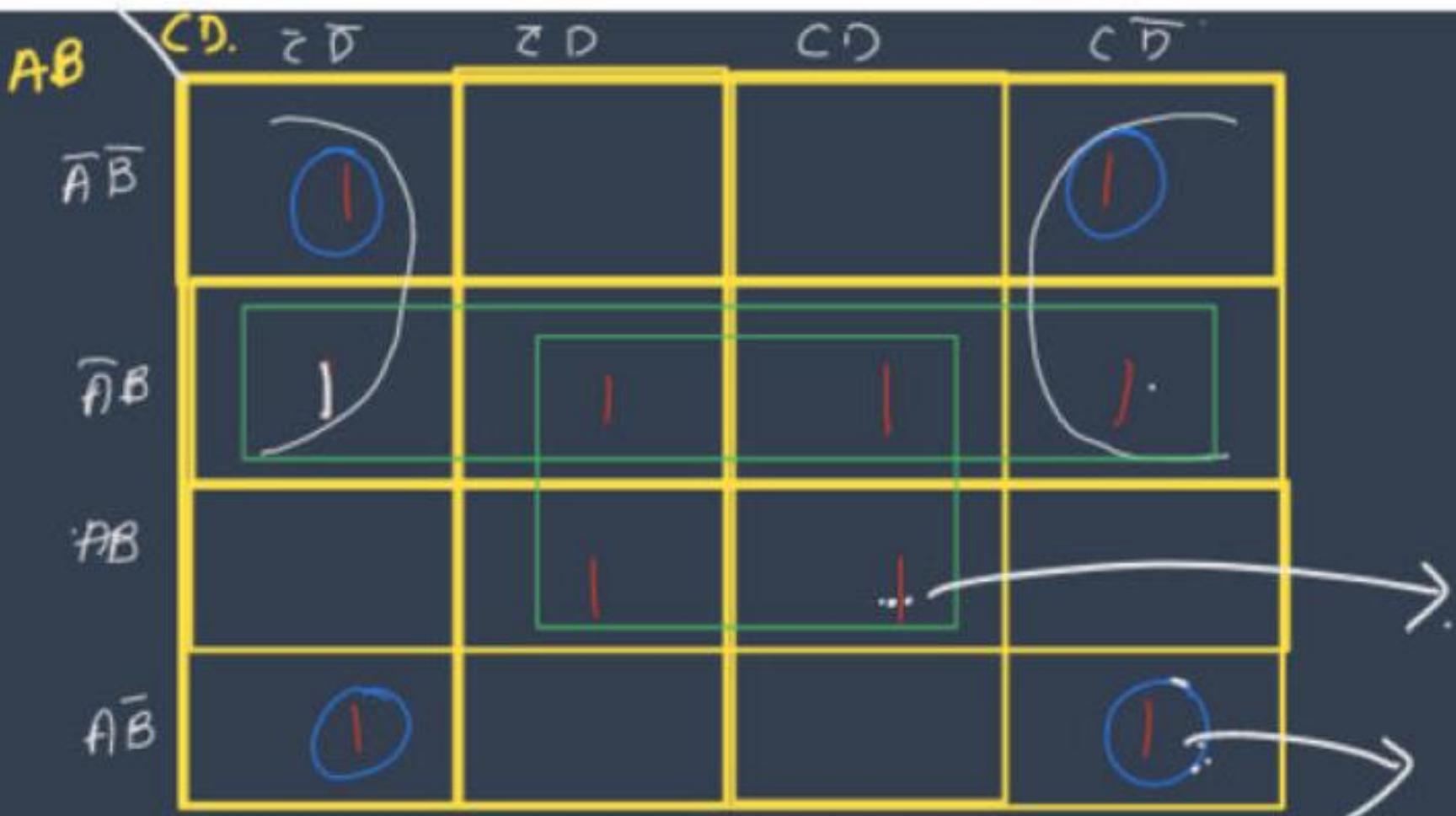
Find the number of EPI's in the following function F

$$F(W,X,Y,Z) = \sum m(0, 2, 5, 7, 8, 10, 12, 14, 15)$$

For the following function  $F(A, B, C, D) = \sum m(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$  the number of essential prime implicants and non-essential prime implicants respectively are?

- (a) 1,3  
(c) 3, 1

- (b) 2,2 ✓  
(d) 2,3



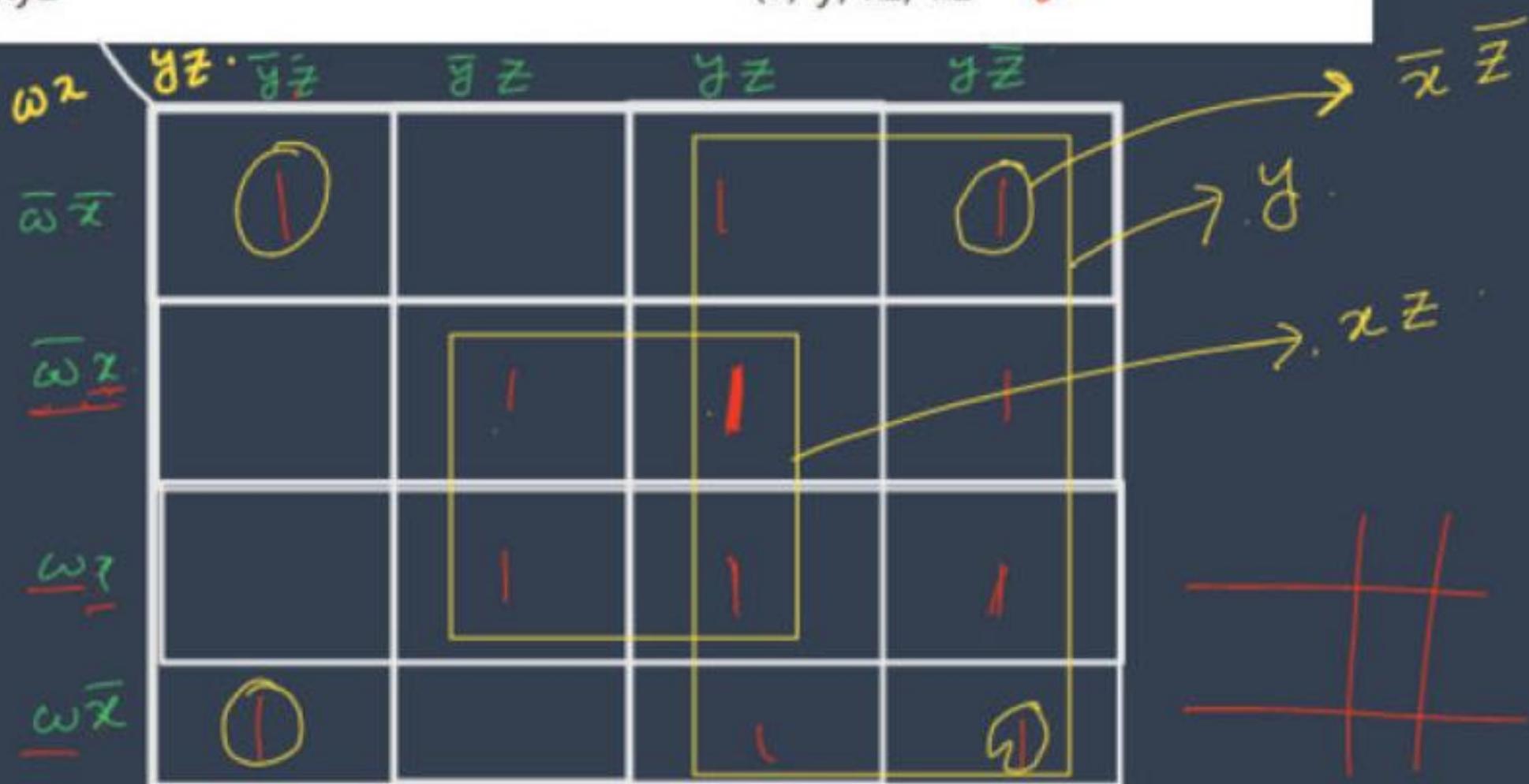
$$PI = 4 \quad \checkmark$$

$$EPI = 2 \quad \checkmark$$

Consider the Boolean function,  $F(w, x, y, z) = \underline{wy} + \underline{x}\underline{y} + \underline{\underline{wxyz}} + \underline{\underline{wxy}} + \underline{xz} + \underline{\underline{xyz}}$ . Which one of the following is the complete set of essential prime implicants?

- (a)  $w, y, xz, \underline{xz}$   
 (c)  $y, xyz$

- (b)  $w, y, xz$   
 (d)  $y, xz, \underline{xz}$



The number of essential prime Implicants of the given minterms  
 $F(A,B,C,D) = \sum m(0,1,4,5,8,11,12,13,15)$  is \_\_\_\_\_.

The minimized SOP expression of the given minterms  
 $F(A, B, C, D) = \sum m(0, 1, 4, 5, 7, 8, 9, 12, 13, 14, 15)$  is

- (a)  $F = \bar{C} + AB + BD$
- (b)  $F = \bar{C} + AB$
- (c)  $F = (A + D) \cdot B$
- (d)  $F = \bar{C} + BD$

Given the Boolean function F in the three variables A,B and C as  $F(A,B,C) = \sum m(2,5,7)$   
then the minimized POS expression is

- (a)  $F = (\bar{A} + C)(A + B)(A + \bar{C})$
- (b)  $F = (\bar{A} + C)(B + C)(A + \bar{C})$
- (c) Both (a) and (b)
- (d) None

K-map of a Boolean function is given below, after simplification choose the correct option.

		CD	00	01	11	10
		AB	00	01	11	10
AB	00	1	1	1	1	
	01	1	1	1	1	
	11	1	1	0	1	
	10	1	1	1	1	

(a)  $\bar{A} + \bar{B}$

(c)  $\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$

(b)  $\bar{A} + \bar{B} + \bar{C}$

(d)  $\bar{A} + \bar{B} + \bar{C} + \bar{D}$

$$\text{Simplify } f(A,B,C,D) = \sum m(0,1,4,5,9,11,14,15) + \sum d(10,13)$$

(a)  $\overline{\overline{AC}} + AC$

(b)  $\overline{\overline{AC}} + \overline{\overline{D}}$

(c)  $\overline{\overline{AC}} + \overline{BC} + \overline{\overline{D}}$

(d)  $\overline{\overline{AC}} + AC + \overline{\overline{D}}$

For the  $k$ -map shown below, the minimized logical expression in SOP form is

$AB \backslash CD$	00	01	11	10
00	1	1		1
01				
11			1	1
10	1		1	1

- a.  $\bar{A}\bar{B}\bar{C} + AC + \bar{B}CD + \bar{A}\bar{B}\bar{D}$
- b.   $\bar{A}\bar{B}\bar{C} + \bar{B}\bar{D} + AC$
- c.  $\bar{A}\bar{B}\bar{C} + AC + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D$
- d.  $\bar{A}\bar{B}\bar{C} + AC + \bar{A}\bar{B}\bar{D}$

Consider a function  $F = A \oplus B \oplus C \oplus D$ . The total number of essential prime implicants of the given function will be \_\_\_\_\_.

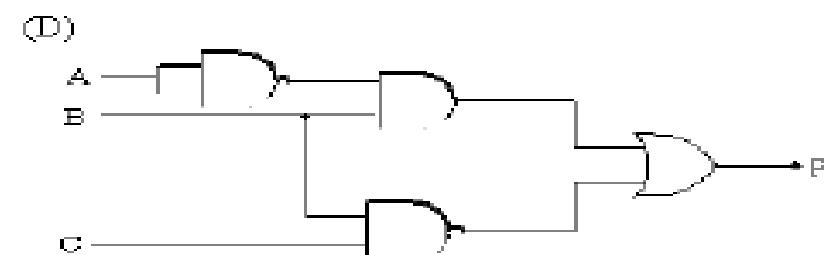
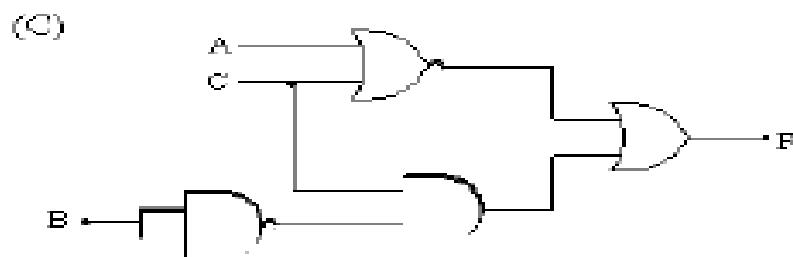
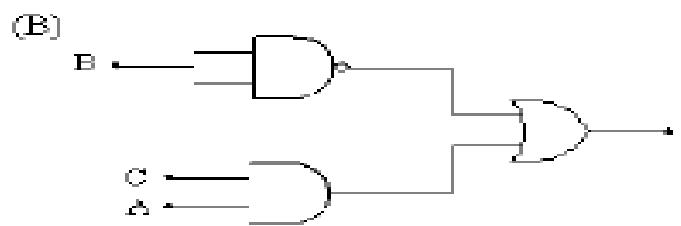
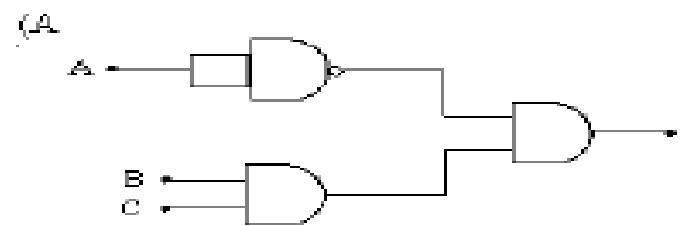
A logical function is given as  $F(A, B, C, D) = \Sigma m (0, 4, 5, 10, 11, 13, 15)$ .

The number of Essential Prime Implicants in the minimized expression will be

.....

Which of the following logic circuit is realization of the function F whose Karnaugh map is as shown below

		AB	00	01	11	10
C	0	1	1			
	1	1			1	



The total number of possible minimal expressions for the four variable Boolean function:

$$F(A,B,C,D) = \sum m(0,2,3,5,7,8,9,10,11,13,15) \text{ is } \underline{\hspace{2cm}}$$

Simplified form of the Boolean function

$F(A, B, C, D, E) = \Sigma m(0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$  is

(A)  $F = \overline{A}\overline{B}\overline{E} + \overline{B}D\overline{E} + ADE$

(B)  $F = \overline{A}\overline{B}\overline{C} + B\overline{D}E + ACE$

(C)  $F = \overline{A}\overline{B}\overline{E} + BCE + ACE$

(D)  $F = \overline{A}\overline{B}\overline{E} + B\overline{D}E + ACE$

A logic circuit implements the following Boolean function

$F(W, X, Y, Z) = \Sigma m(2, 3, 6, 7, 8, 12)$  It is found that the input combination for which  $W = Y$  can never occur. Then minimal expression for F is

- (A)  $WY + \overline{Y}Z$       (B)  $\overline{Y} + Z$   
 (C)  $W\overline{Y} + Z$       (D)  $Y + \overline{Z}$

**Answer : D**

# DIGITAL CIRCUITS

## DPP - 3

The SOP form of logical expression is most suitable for designing logic circuit using only

- (a) NOR gates
- (b) NAND gates
- (c) AND gates
- (d) X-OR gates

The POS form of logical expression is most suitable for designing logic circuits using only

- (a) X-OR gates
- (b) AND gates
- (c) NAND gates
- (d) NOR gates

The sum of products form can be realized by using ----- logic

- (a) NAND-NAND
- (b) AND-OR
- (c) Either 1 or 2
- (d) None

Let \* be defined as  $x * y = \bar{x} + y$ , Let  $z = x * y$ . Value of  $z * x$  is

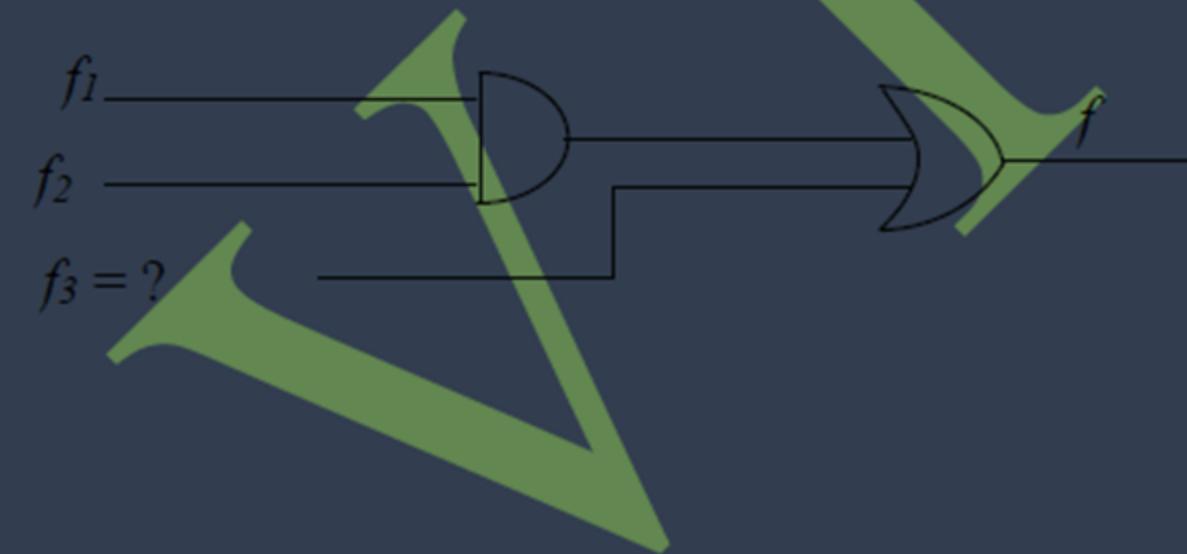
(a)  $\bar{x} + y$

(b)  $x$

(c) 0

(d) 1

Consider the logic circuit shown in the below figure. The functions  $f_1$ ,  $f_2$  and  $f$ (in canonical sum of products from in decimal notations) are: **(GATE-CSIT-97)**



$$f_1(w, x, y, z) = \sum 8, 9, 10$$

$$f_2(w, x, y, z) = \sum 7, 8, 12, 13, 14, 15$$

$$f(w, x, y, z) = \sum 8, 9$$

The function  $f_3$  is

- (a)  $\sum 9, 10$
- (b)  $\sum 9$
- (c)  $\sum 1, 8, 9$
- (d)  $\sum 8, 10, 15$

The simultaneous equations on the Boolean variables x, y, z and w,

(GATE-CSIT-2000)

$$x + y + z = 1$$

$$xy = 0$$

$$xz + w = 1$$

$$xy + \overline{z}\overline{w} = 0$$

have the following for x, y, z and w, respectively.

(a) 0100

(b) 1101

(c) 1011

(d) 1000

Consider the following circuit composed of XOR gates and non-inverting buffers.  
**(GATE-CSIT-03)**



The non-inverting buffers have delays  $\delta_1 = 2$  ns and  $\delta_2 = 4$  ns as shown in the figure. Both XOR gates and all wires have zero delay. Assume that all gate inputs, outputs and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A, how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?



- (a) 1      (b) 2      (c) 3      (d) 4

$F(w, x, y, z) = \Sigma (1, 3, 4, 6, 9, 11, 12, 14)$  the function is

(GATE-CSIT-07)

- (a) Independent of one variables
- (b) Independent of two variables
- (c) Independent of three variables
- (d) Depends on all variables

Let  $f(w,x,y,z) = \Sigma (0,4,5,7,8,9,13,15)$ . Which of the following expressions are NOT equivalent to  $f$ ? **(GATE-CSIT-07)**

- (P)  $x'y'z' + w'xy' + wy'z + xz$
- (Q)  $w'y'z' + wx'y' + xz$
- (R)  $w'y'z' + wx'y' + xyz + xy'z$
- (S)  $x'y'z' + wx'y' + w'y$
- (A) P only
- (B) Q and S
- (C) R and S
- (D) S only

. Define the connective \* for the Boolean variables X and Y as:  $X * Y = XY + X'Y'$ .

Let  $Z = X * Y$ . Consider the following expressions P, Q and R. (GATE-CSIT-07)

$$P : X = Y * Z$$

$$Q : Y = X * Z$$

$$R : X * Y * Z = 1$$

Which of the following is TRUE?

- (A) Only P and Q are valid.
- (C) Only P and R are valid.

- (B) Only Q and R are valid.
- (D) All P, Q, R are valid.

Given  $f_1$ ,  $f_2$ , and  $f$  in canonical sum of products form (in decimal) for the circuit.

(GATE-CSIT-08)

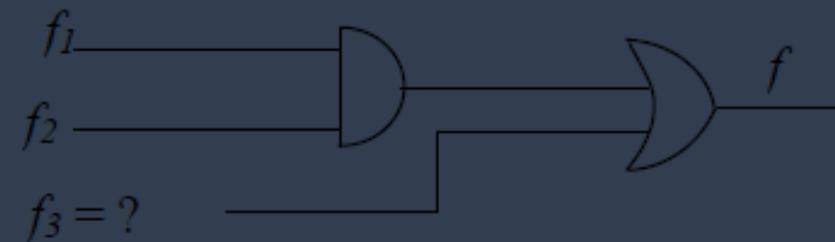
$$f_1 = \sum m(4, 5, 6, 7, 8)$$

$$f_3 = \sum m(1, 6, 15)$$

$$f = \sum m(1, 6, 8, 15)$$

Then  $f_2$  is

- (A)  $\sum m(4, 6)$       (B)  $\sum m(4, 8)$       (C)  $\sum m(6, 8)$     (D)  $\sum m(4, 6, 8)$

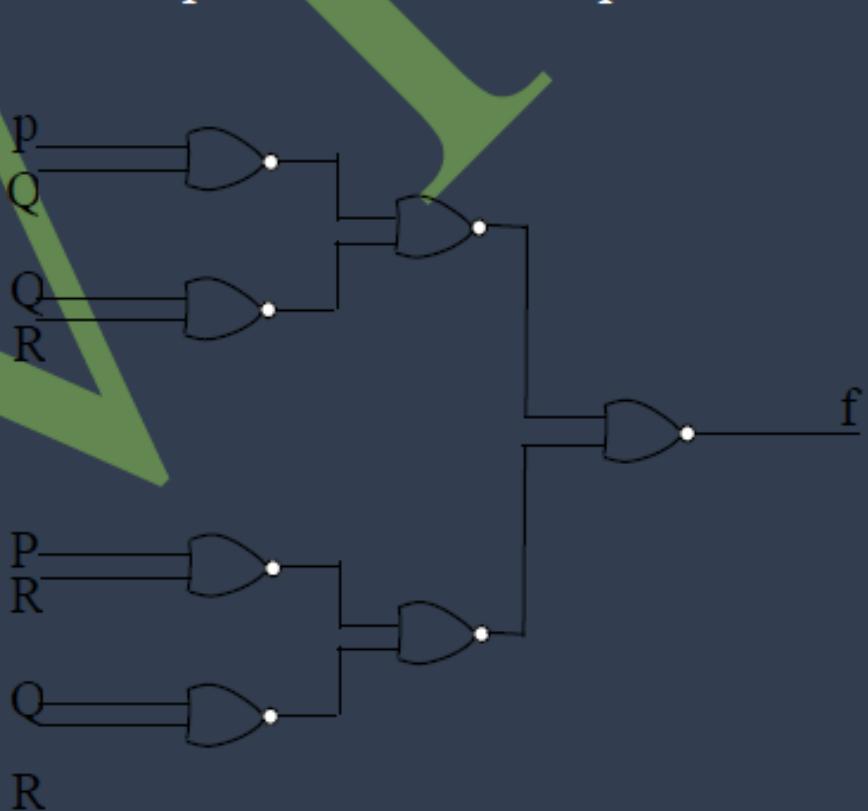


What is the minimum number of gates required to implement the Boolean function  
 $(AB + C)$  if we have to use only 2-input NOR gates ?

(GATE-CSIT-09)

- (A) 2
- (B) 3
- (C) 4
- (D) 5

What is the Boolean expression for the output  $f$  of the combinational logic circuit of NOR gates given below? (GATE-CSIT-10)



- (A)  $\overline{O+R}$       (B)  $\overline{P+O}$       (C)  $\overline{P+R}$       (D)  $\overline{P+O+R}$

Which logic gate is similar to the function of two series switches?

- a) AND gate
- (b) OR gate
- (c) NAND gate
- (d) None

$Y = (AB)'$  is the Boolean function for ---- gate

- a) AND gate
- (b) NAND gate
- (c) OR gate
- (d) NOR gate

The output Boolean expression for the exclusive OR gate is

- a)  $(A+B)'$
- b)  $Y = AB + A' B'$
- c)  $Y = (A + B)(A' + B')$
- d) None of these

XOR gates are ideal for testing parity because even-parity words produce a ---- output and odd parity words produce a ----- output

- a) low, high
- (b) low, low
- (c) high, high
- (d) high, low

Which gate corresponds to the action of parallel switches?

- a) AND gate
- (b) OR gate
- (c) NOR gate
- (d) NAND gate

The output of the following circuit is given by

- a) 1
- b) 0
- c)  $x$
- d)  $x'$



An AND gate has 7 inputs. How many words are there in its truth table?

- a) 7
- (b) 49
- (c) 81
- (d) 128

The number of input words in a truth table always equals ---- where 'n' is the number of input bits

- (a)  $2n$
- (b)  $2n+1$
- (c)  $2(n+1)$
- (d)  $2^n$

A gate can have -----input signals and ----- output signals

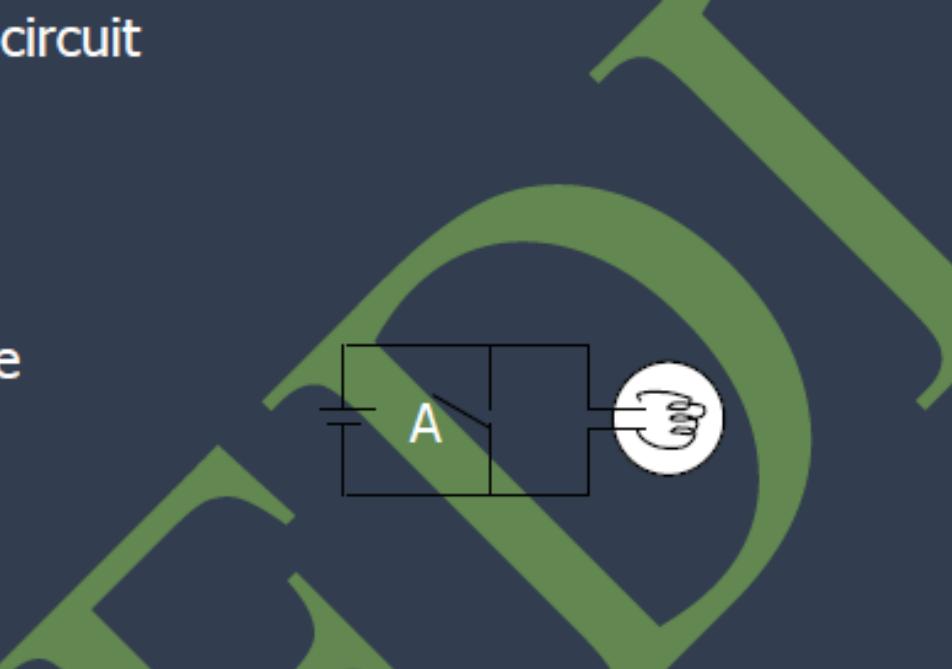
- a) one, one
- (b) two, two
- (c) one or more, one
- (d) two or more, two or more

Q) An OR gate has 6 inputs. How many input words are there in its truth table?

- a) 6
- (b) 36
- (c) 64
- (d) 64,000,000

Identify the operation of the circuit

- a) NOT gate
- b) AND
- c) OR
- d) None



Which of the following operations is not associative

- (a) NOR
- (b) OR
- (c) X-OR
- (d) None

The working of a staircase switch is a typical example of the logical operation.

- (a) OR
- (b) NOR
- (c) XOR
- (d) XNOR

In which of the following gates the output is 1 if at least one input is 0 or all inputs are zeros?

- (a) NOT
- (b) AND
- (c) OR
- (d) NAND

In which of the following gates the output is 0 if at least one input is 1?

- (a) NOT
- (b) AND
- (c) NOR
- (d) NAND

Let X and Y be the inputs and Z be the output of a NAND gate. The value of Z is given by

- (a)  $(XY)'$
- (b)  $X+Y$
- (c)  $XY$
- (d) none of these.

Let X and Y be the inputs and Z be the output of a XOR gate. The value of Z is given by

- (a)  $(XY)'$
- (b)  $XY' + X'Y$
- (c)  $XY$
- (d) None of these.

The NAND can function as NOT gate if

- (a) inputs are connected together
- (b) inputs are left open
- (c) one input is set to 0
- (d) none

What is the minimum number of two-input NAND gates used to perform the function of two-input OR gate?

- (a) one
- (b) two
- (c) three
- (d) four

Which of the following gates are added to the inputs of the OR gate to convert it to the NAND gate ?

- (a) NOT
- (b) AND
- (c) OR
- (d) XOR

What logic function is produced by adding inverters to the input of an AND gate?

(a) NAND

(b) NOR

(c) XOR

(d) AND

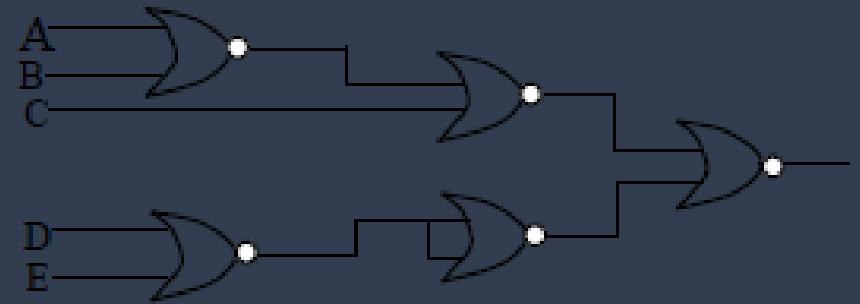
Which of the following gates is known as coincidence detector?

- (a) AND gate
- (b) OR gate
- (c) NOT gate
- (d) NAND gate

The operation  $x \oplus y$  represents  
**(IES-1991)**

- (a)  $x - y$
- (b)  $\overline{x} \overline{y} + \overline{x} y$
- (c)  $x \overline{y} + \overline{x} \overline{y}$
- (d)  $x - \overline{y}$

The circuit shown in figure realizes the function:



- (a)  $(A + B + C)(D\bar{E})$
- (b)  $(A + (\bar{B} + C))(\bar{D}E)$
- (c)  $(A + B + C)(\bar{D}\bar{E})$
- (d)  $(\bar{A} + \bar{B}) + C)(\bar{D}\bar{E})$

The product – of – sum expression for given truth table is: (IES-1992)

X	Y	Z
0	0	1
0	1	0
1	0	1
1	1	0

- (a)  $(\bar{X} + \bar{Y})(X + Y)$
- (b)  $(X + \bar{Y})(\bar{X} + \bar{Y})$
- (c)  $(X + \bar{Y})(\bar{X} + Y)$
- (d) None of the above

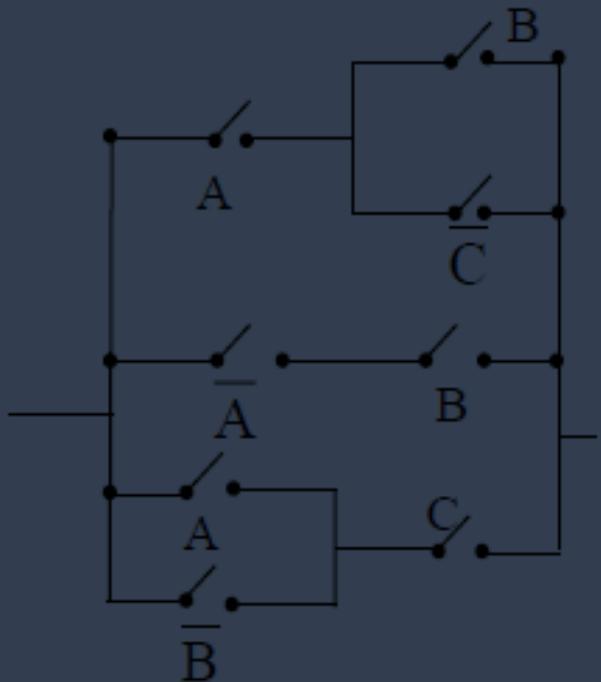
What is Boolean expression for a gating network that will have output 0 only, when X = 1, Y = 1, Z = 1, X = 0, Y = 0, Z = 0; X = 1, Y = 0, Z = 0?

**(IES-1992)**

- (a)  $XYZ + \overline{XYZ} + X\overline{YZ}$
- (b)  $(XYZ)(\overline{X} + \overline{Y} + Z)(X + \overline{Y} + Z)$
- (c)  $(\overline{X} + \overline{Y} + \overline{Z})(X + Y + Z)(\overline{X} + Y + Z)$
- (d)  $\overline{XYZ} + XYZ + \overline{XYZ}$

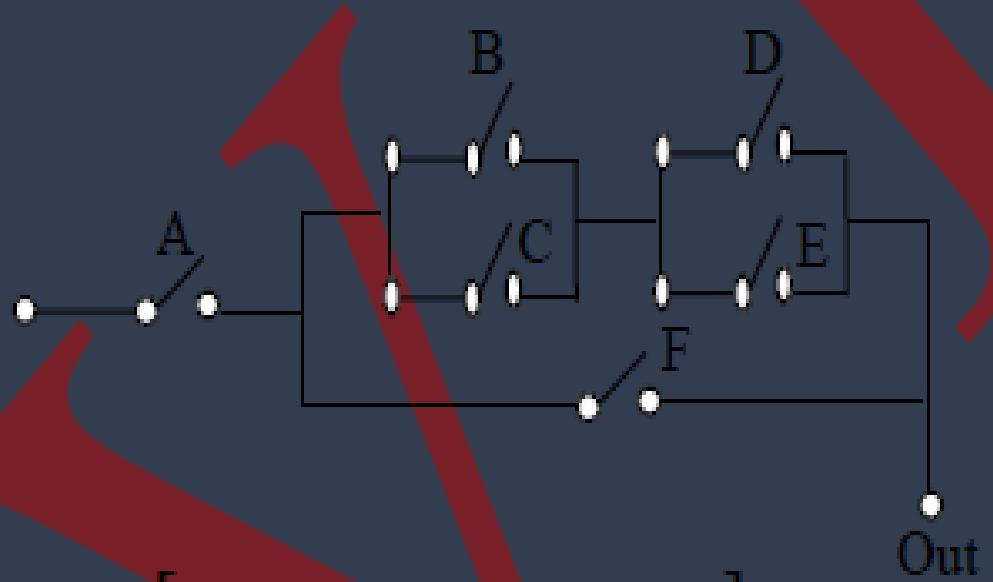
The minimum Boolean for the following circuit is

(IES-1993)



- (a)  $AB + AC + BC$
- (b)  $A + BC$
- (c)  $A + B$
- (d)  $A + B + C$

What Boolean function does the following circuit represent? (IES-1995)



- (a)  $A[F + (B+C)(D+E)]$
- (b)  $A[F + (B+C)DE]$
- (c)  $A[F + (BC+DE)]$
- (d)  $A[F(B+C) + (D+E)]$

How many minterms (excluding redundant terms) does the minimal switching function

$f(v, w, x, y, z) = x + \bar{y}z$  originally have?



(IES-1998)

Match List-I with List-II and select the correct answer using the codes given below the lists: (IES-2003)

**List-I**

- A.  $A \oplus B = 0$
- B.  $\overline{A + B} = 0$
- C.  $\overline{A} \cdot B = 0$
- D.  $A \oplus B = 1$

**Codes:**

	A	B	C	D
(a)	3	2	1	4
(b)	2	3	4	1
(c)	3	2	4	1
(d)	2	3	1	4

The minimum number of NAND gates required to implement the Boolean function

$A + A\bar{B} + A\bar{B}C$  is equal to (IES-2003)

- (a) zero
- (b) 1
- (c) 4
- (d) 7

Match List-I(Boolean Logic Function) with List-II(Inverse of Function) and select the correct answer using the code given below the lists:

(IES-2007)

List-I

- A.  $ab+bc+ca+abc$
- B.  $ab+\bar{a}\bar{b}+\bar{c}$
- C.  $a+bc$
- D.  $(\bar{a}+\bar{b}+\bar{c})(\bar{a}+\bar{b}+\bar{c})(\bar{a}+\bar{b}+c)$

List-II

- 1.  $\bar{a}(\bar{b}+\bar{c})$
- 2.  $\bar{a}\bar{b}+\bar{b}\bar{c}+\bar{c}\bar{a}$
- 3.  $(a \oplus b)c$
- 4.  $abc + \bar{a}bc + a\bar{b}c$

Codes:

	A	B	C	D
(a)	3	2	1	4
(b)	2	3	1	4
(c)	3	2	4	1
(d)	2	3	4	1

What are the ultimate purposes of minimizing logic expressions?

1. To get a small size expression
2. To reduce the number of variables in the given expression
3. To implement the function of the logic expression with least hardware
4. To reduce the expression for making it feasible for hardware implementation.

Select the correct answer from the codes given below.(IES-2009)

- |            |             |
|------------|-------------|
| (a) 1 only | (b) 2 and 3 |
| (c) 3 only | (d) 3 and 4 |

Match List – I with List – II and select the correct answer using the code given below the lists : (IES-2011)

**List – I**

- A. AND gate
- B. OR gate
- C. NOT gate

**List – II**

- 1. Boolean complementation
- 2. Boolean addition
- 3. Boolean multiplication

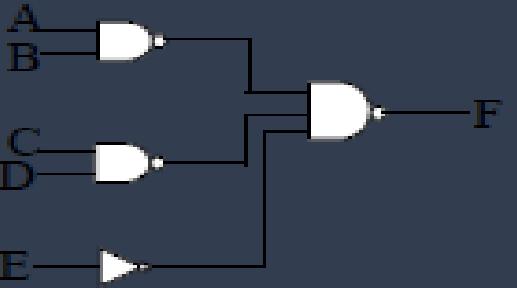
Code:

	A	B	C
(a)	3	1	2
(b)	1	2	3
(c)	3	2	1
(d)	1	3	2

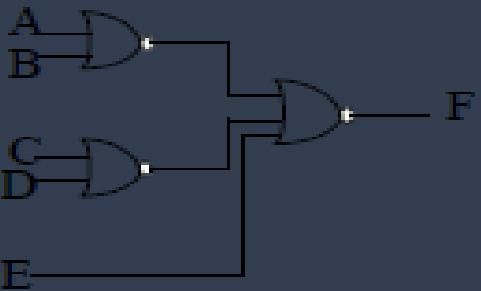
The Boolean function  $F = AB + CD + E$  can be realized as

(IES-1991)

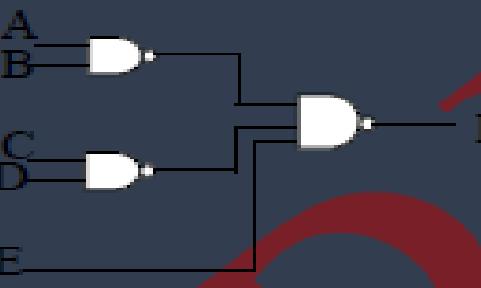
(a)



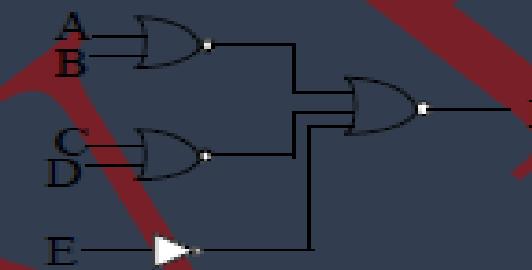
(b)



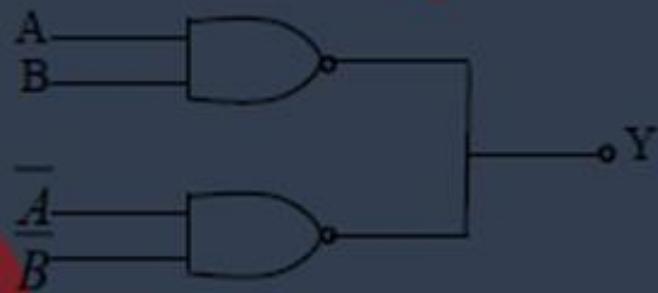
(c)



(d)

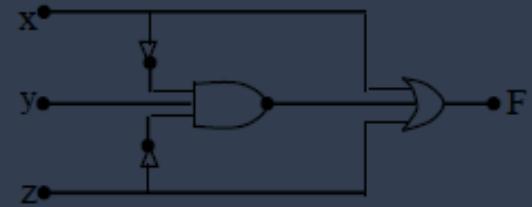


The open collector wired circuit shown below functions as: (IES-1992)



- (a) EX - NOR
- (b) AND
- (c) EX - OR
- (d) NOR

The minimized version for the logic circuit shown in the figure is :  
(IES-1992)



- (a)   
A NOR gate with three inputs: x, y, and z. The output is labeled F. A white square is placed next to the circuit.  
(b)   
A NOR gate with three inputs: x, y, and z. The output is labeled F.  
(c)   
A NOR gate with three inputs: x, y, and z. The output is unlabeled.  
(d)   
A NOR gate with three inputs: x, y, and z. The output is unlabeled.

Which of the following is a coincidence logic circuit: (IES-1992)

(a)



(b)



(c)



(d)



Which one of the following represents coincidence logic?

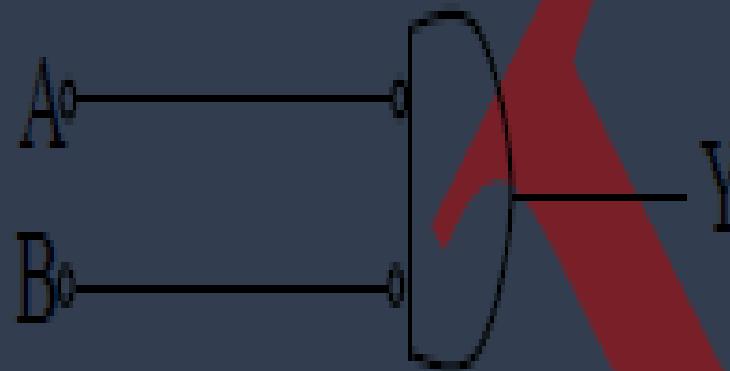
(IES-1993)

- (a)  A logic circuit diagram showing two inputs, A and B. Input A is connected to the input of an AND gate. Input B is connected to one input of an OR gate. The output of the AND gate is connected to one input of an OR gate. The other input of the OR gate is connected to ground. The output of the OR gate is labeled F.
- (b)  A logic circuit diagram showing two inputs, A and B. Input A is connected to the input of an AND gate. Input B is connected to one input of an OR gate. The output of the AND gate is connected to one input of an OR gate. The other input of the OR gate is connected to the output of an inverter. The output of the inverter is connected to ground. The output of the OR gate is labeled F.
- (c)  A logic circuit diagram showing two inputs, A and B. Input A is connected to the input of an AND gate. Input B is connected to one input of an OR gate. The output of the AND gate is connected to one input of an OR gate. The other input of the OR gate is connected to the output of an inverter. The output of the inverter is connected to the input of the AND gate. The output of the OR gate is labeled F.
- (d)  A logic circuit diagram showing two inputs, A and B. Input A is connected to the input of an AND gate. Input B is connected to one input of an OR gate. The output of the AND gate is connected to one input of an OR gate. The other input of the OR gate is connected to the output of an inverter. The output of the inverter is connected to the input of the AND gate. The output of the OR gate is labeled F.

The gate whose output is LOW if and only if all the inputs are HIGH, is  
(IES-1993)

- (a) NAND
- (b) NOR
- (c) OR
- (d) AND

The negative logic AND gate shown in the given figure is equivalent to a positive logic  
(IES-1993)



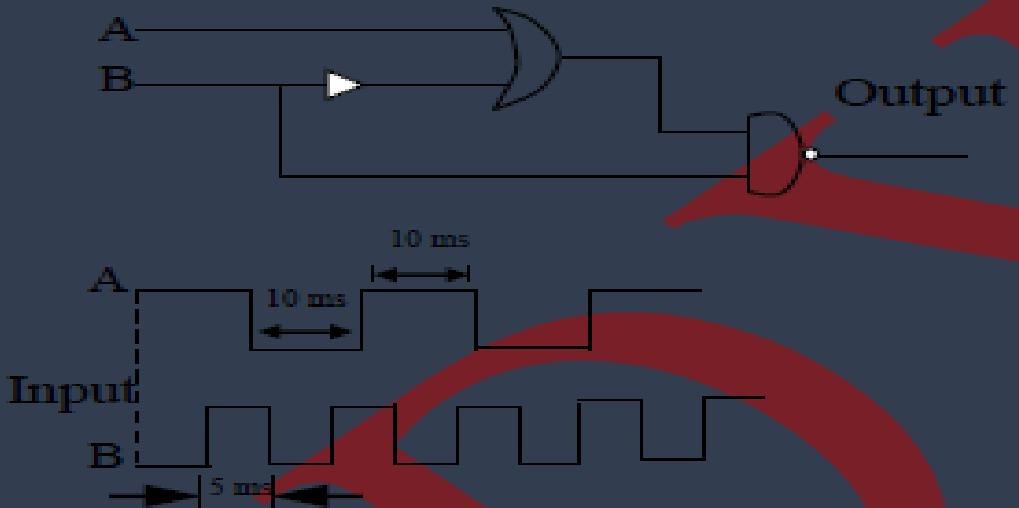
- (a) AND gate
- (b) OR gate
- (c) NAND gate
- (d) NOR gate

Which one of the following is equivalent to AND-OR realization?

(IES-1994)

- (a) NAND-NOR realization
- (b) NOR-NOR realization
- (c) NOR-NAND realization
- (d) NAND-NAND realization

The output (X) wave form for the above combination circuit for the inputs at A and B(waveform shown in the figure) will be (IES-1994)



- (a)   
10ms 10ms 10ms
- (b)   
15ms 5 ms 15ms 5 ms 15ms
- (c)   
15ms 5 ms 15ms 5 ms 15ms
- (d)   
10ms 5 ms 10ms 5 ms 10ms 5 ms 10ms

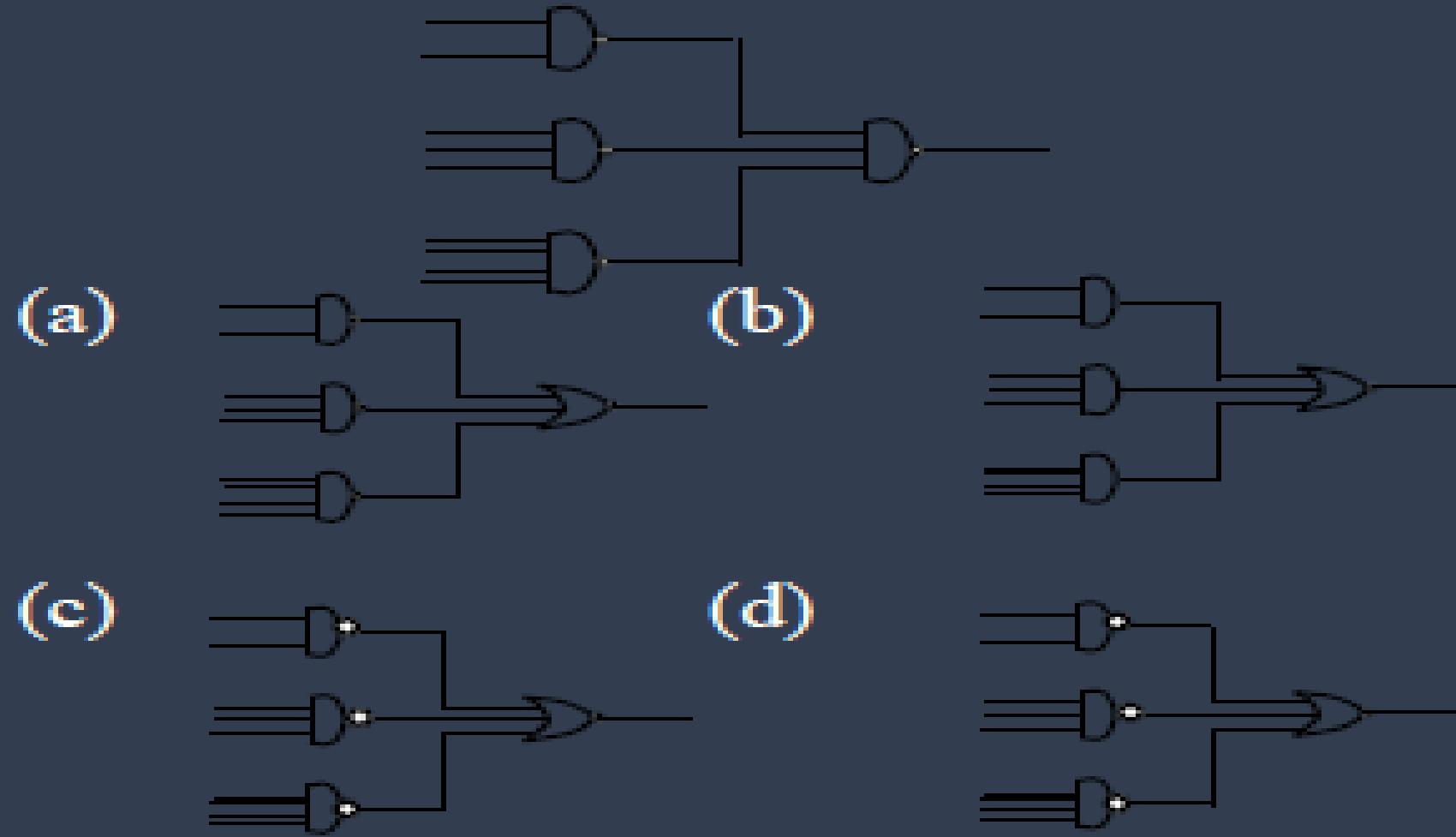
Q. Which one of the following sets of gates are best suited for parity checking and parity generation?  
**(IES-1995)**

- (a) AND, OR, NOT gates
- (b) X-OR X-NOR gates
- (c) NAND gates
- (d) NOR gates

The output of a logic gate is 1 when all its inputs are at logic 0. The gate is either  
**(IES-1995)**

- (a) A NAND or an EX-OR
- (b) an OR or an EX-OR
- (c) an AND or an EX-OR
- (d) a NOR or an EX-NOR

The circuit shown in figure 1 is equivalent to:  
**(IES-1995)**



The logic circuit shown in the given figure can be minimized to (IES-1995)

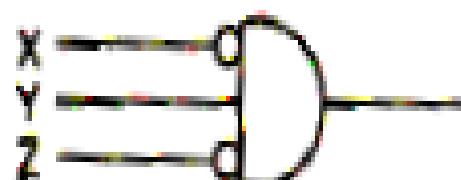
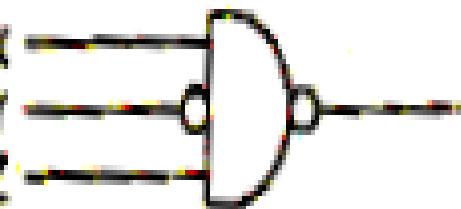
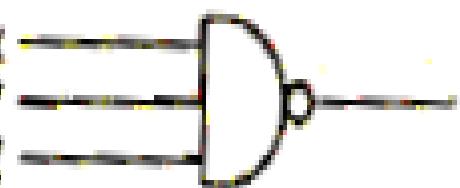
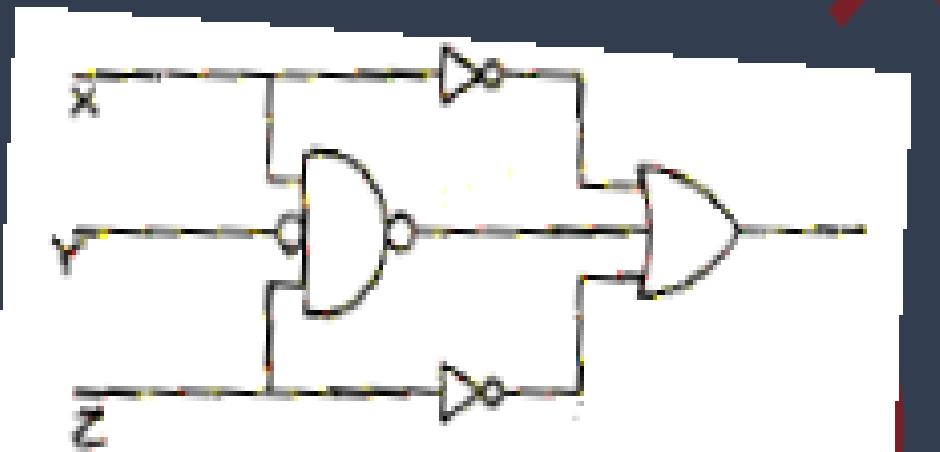


- (a)   
This circuit shows the input  $X$  connected to the inverter's input. The inverter's output is the final output, which is the negation of  $X$ .
- (b)   
This circuit shows the inputs  $X$  and  $Y$  connected to the OR gate's inputs. The OR gate's output is the final output.
- (c)   
This circuit shows the inputs  $X$  and  $Y$  connected to the AND gate's inputs. The AND gate's output is the final output.
- (d)   
This circuit shows the input  $X$  connected to the inverter's input. The inverter's output is the final output, which is the negation of  $X$ .

A three – input NAND gate is to be used as an inverter. Which one of the following measures will achieve better results? (IES-1996)

- (a) The two inputs not used are kept open
- (b) The two inputs not used are connected to ground (0 level)
- (c) The two inputs not used are connected to logic (1 level)
- (d) None of the above

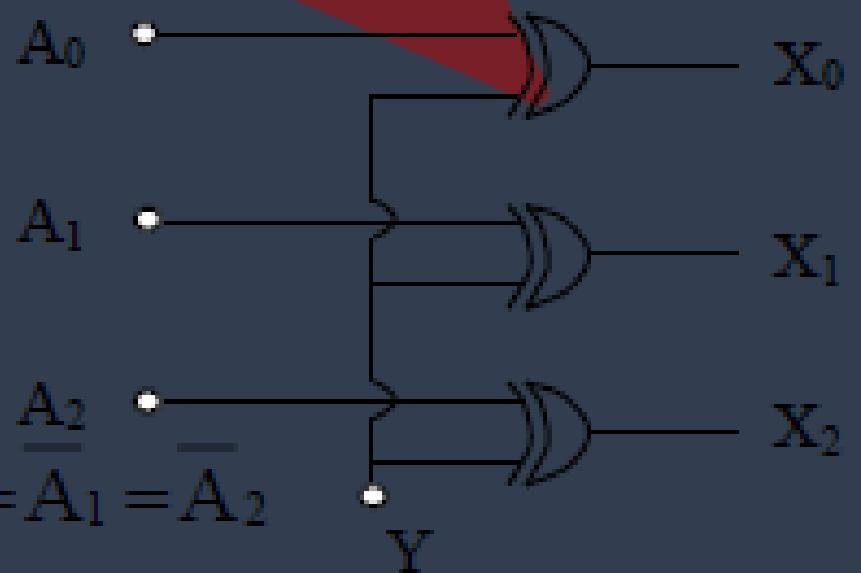
The minimized logic circuit for the circuit shown in fig. is (IES-1996)



(a)

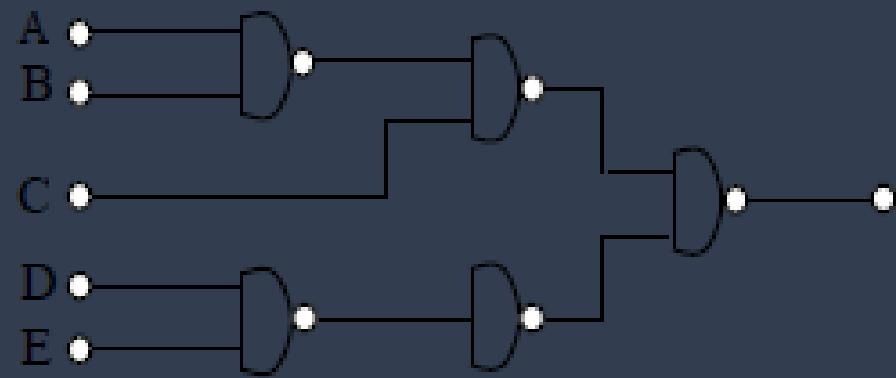
(c)

In the figure shown,  $X_2X_1X_0$  will be 1's complement of  $A_2A_1A_0$  if  
**(IES-1996)**



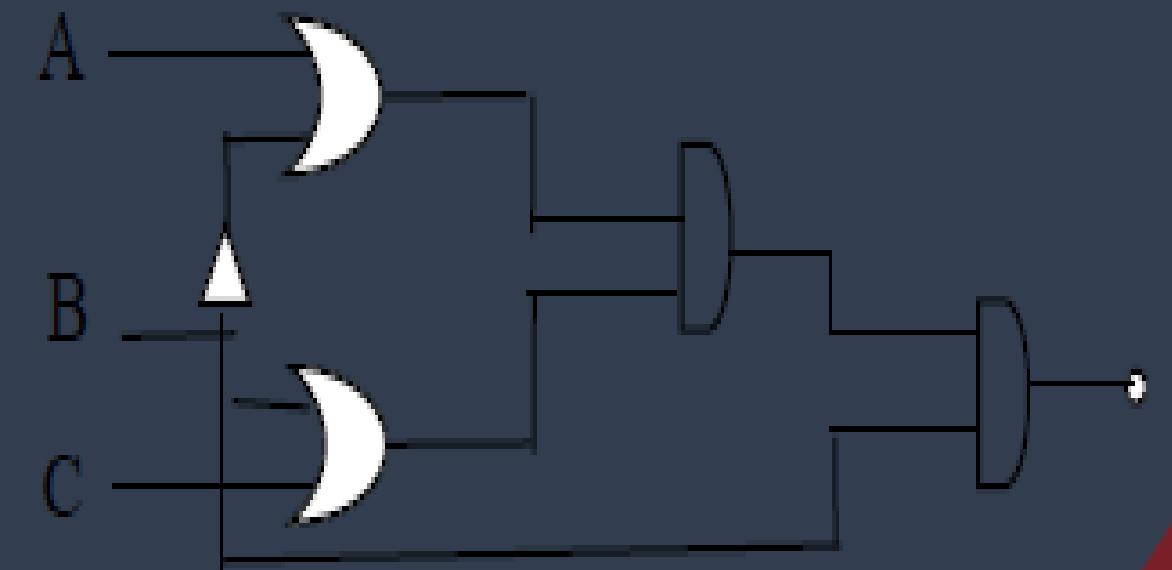
- $\bar{A}_0 = \bar{A}_1 = \bar{A}_2$
- (a)  $Y = 0$
  - (b)  $Y = 1$
  - (c)  $Y = \bar{A}_0 = \bar{A}_1 = \bar{A}_2$
  - (d)  $Y = A_0 = A_1 = A_2$

The circuit shown in the following figure realizes the function (IES-1996)



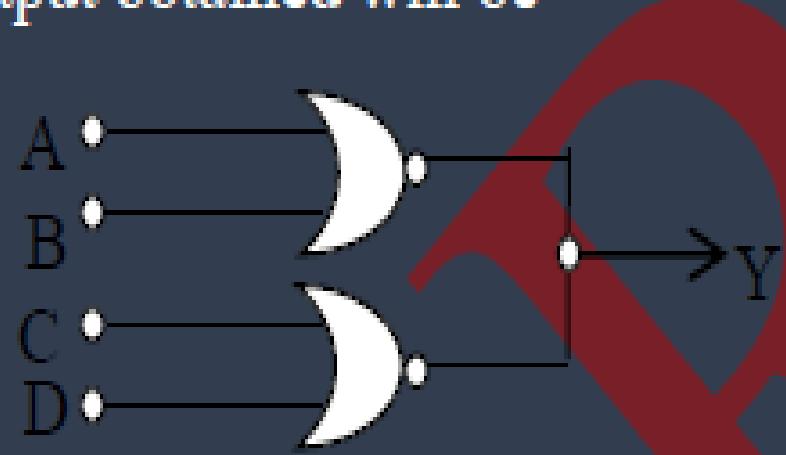
- (a)  $(\bar{A} + \bar{B})C + \bar{D}\bar{E}$
- (b)  $(A+B)C + D + E$
- (c)  $AB + C = DE$
- (d)  $AB + C(D+E)$

Q. The output X of the logic circuit shown in the figure is (IES-1997)



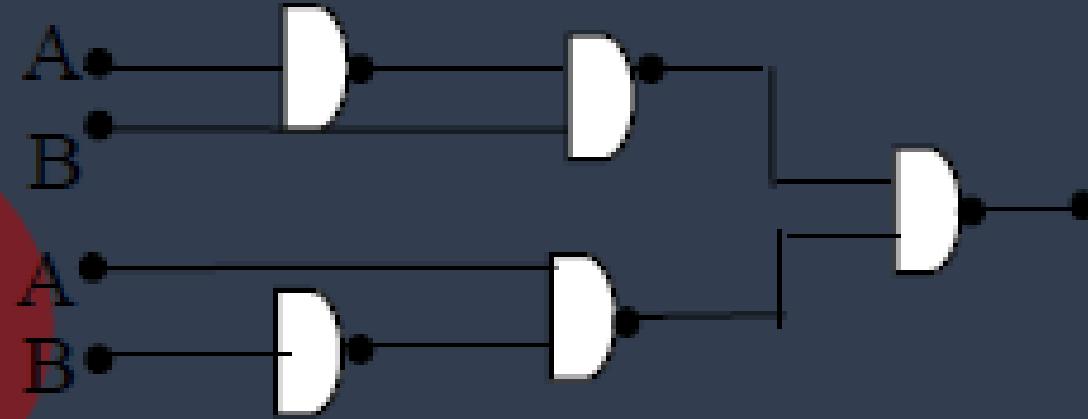
- (a)  $A + BC$
- (b)  $BC$
- (c)  $AB$
- (d)  $AB + C$

When two gates with open collector outputs are tied together as shown in the figure, the output obtained will be  
(IES-1997)



- (a)  $\overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$
- (b)  $\overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$
- (c)  $\overline{(\overline{A} + \overline{B})(\overline{C} + \overline{D})}$
- (d)  $\overline{\overline{A + B + C + D}}$

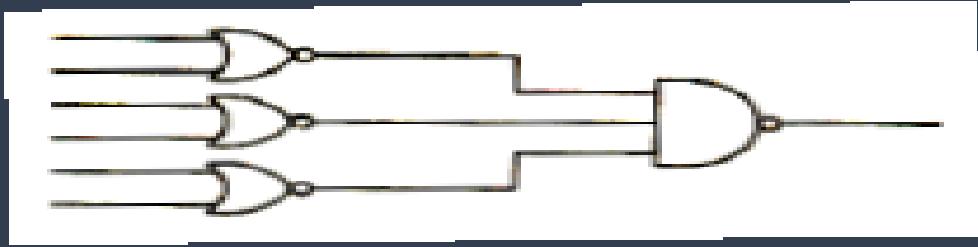
The circuit shown in the figure is functionally equivalent to  
**(IES-1997)**



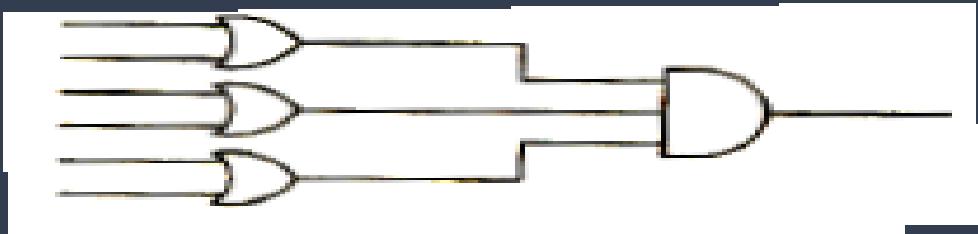
- (a) NOR gate
- (b) OR gate
- (c) EX - OR gate
- (d) NAND gate

The circuit shown in fig. 1 is equivalent to

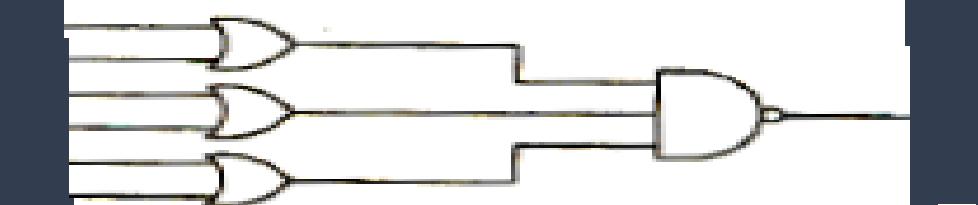
(IES-1998)



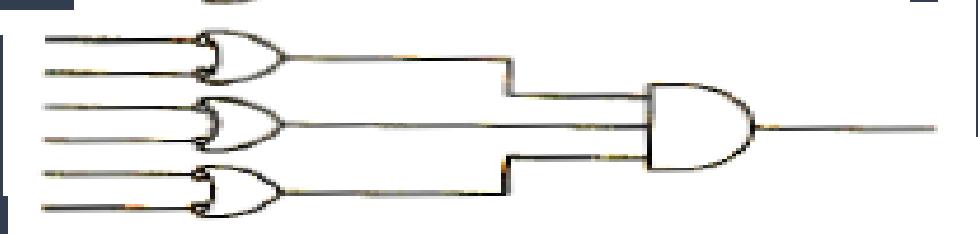
(a)



(b)



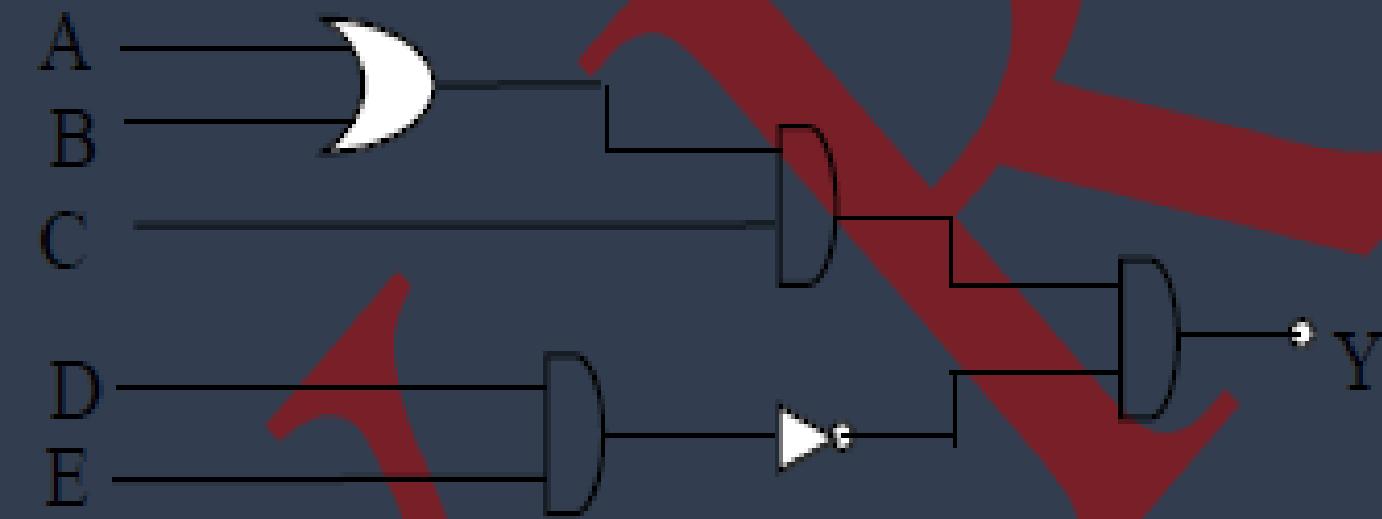
(c)



(d)

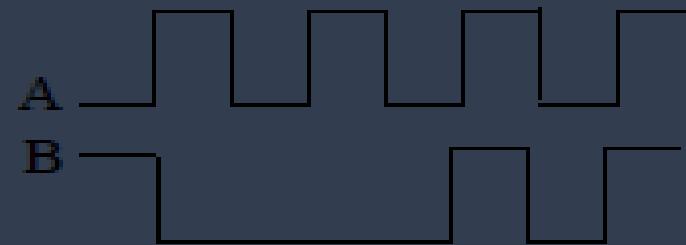


The output  $Y$  of the circuit shown in the figure is (IES-1998)



- (a)  $(A+B) C+DE$
- (b)  $AB+C(D+E)$
- (c)  $(A+B) C+D+E$
- (d)  $(AB+C)DE$

The given figure shows a NAND gate with input waveforms A and B.



The correct output waveform X of the gate is

(IES-1999)

- (a) A horizontal line at 1 level, followed by a sharp drop to 0 level.
- (b) A horizontal line at 0 level, followed by a sharp rise to 1 level, followed by another sharp rise to 1 level.
- (c) A horizontal line at 0 level, followed by a sharp rise to 1 level, followed by a small pulse down to 0 level, followed by a sharp rise back to 1 level.
- (d) A horizontal line at 1 level, followed by a sharp drop to 0 level, followed by a sharp rise to 1 level.

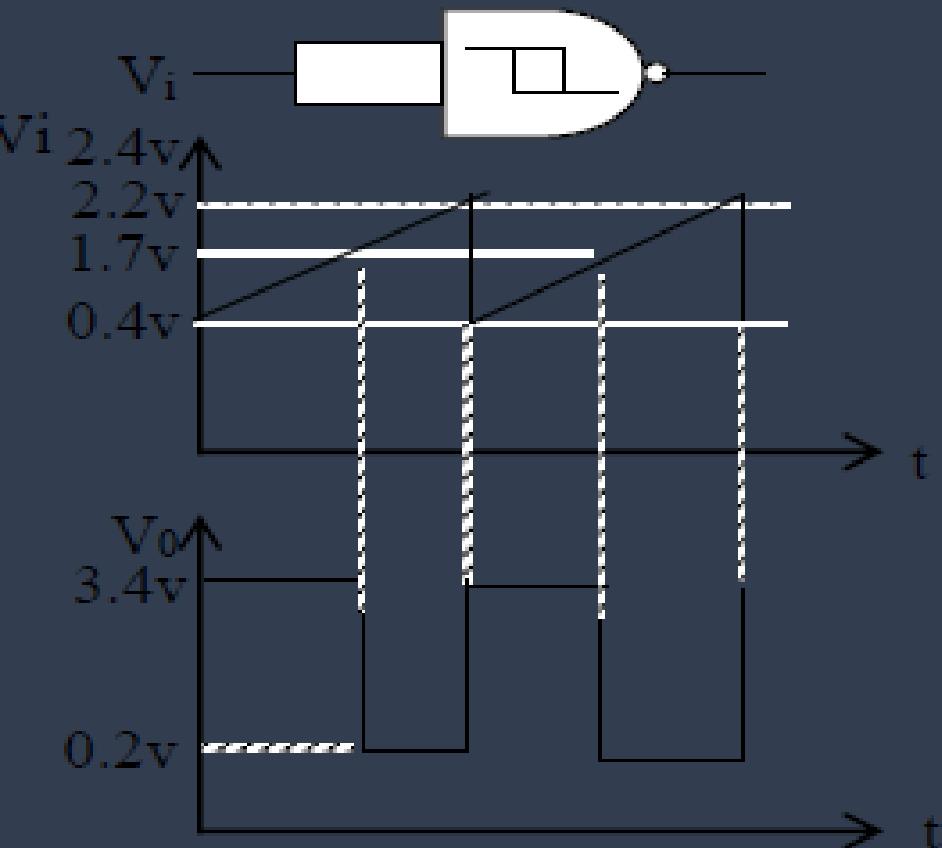
The output Y of the given circuit is  
(IES-1999)



- (a) 1
- (c) X

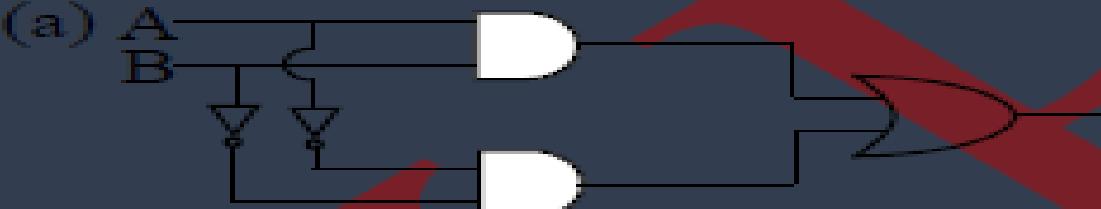
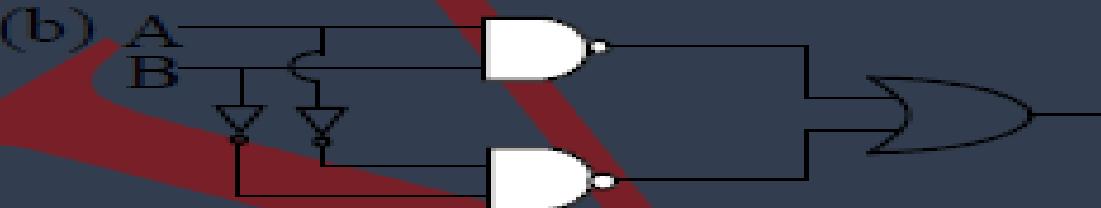
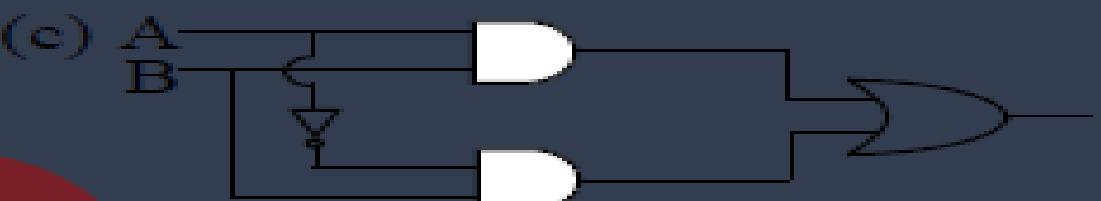
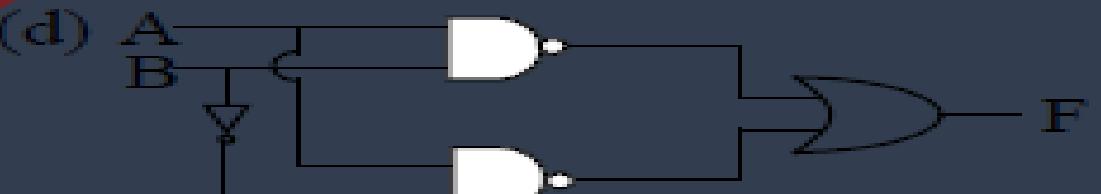
- (b) zero
- (d)  $\bar{X}$

The input waveform  $V_i$  and the output waveform  $V_o$  of a Schmitt NAND are shown in the given figures. The duty cycle of the output waveform will be  
(IES-1999)

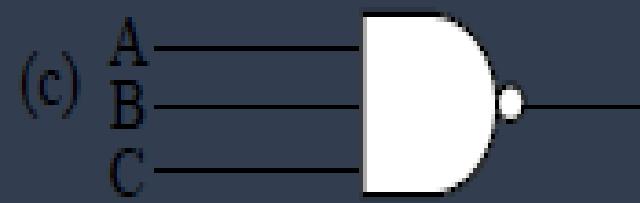
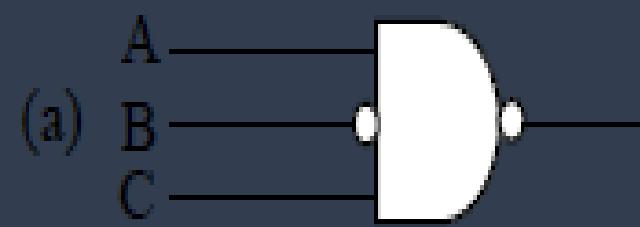
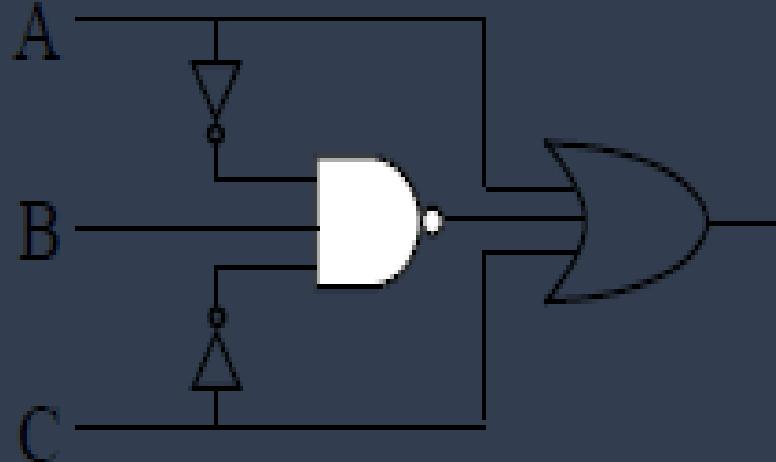


- (a) 100%
- (b) 85.5%
- (c) 72.2%
- (d) 25%

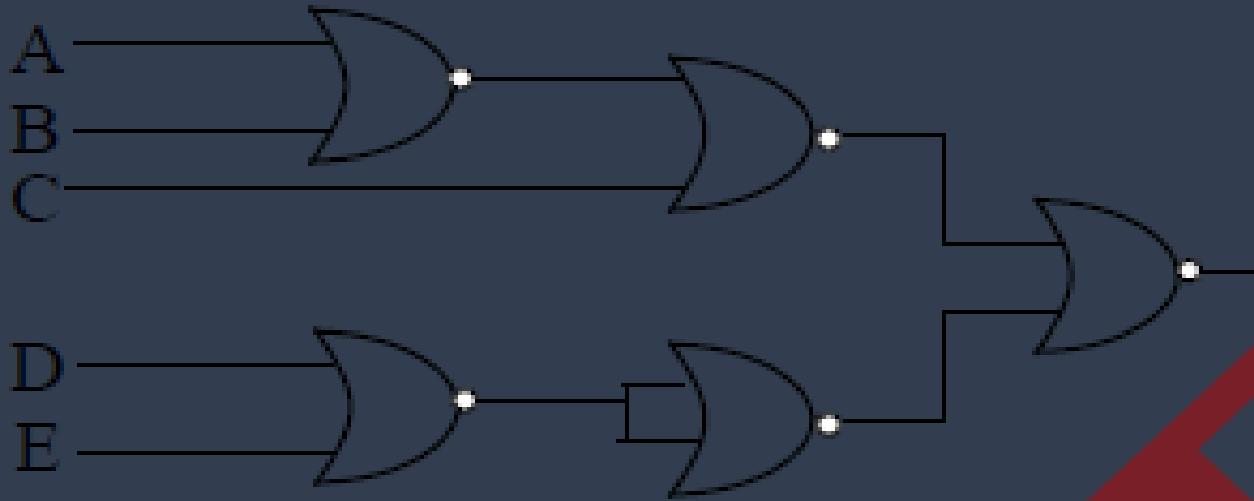
Which one of the following figures represents the coincidence logic?  
(IES-2000)

- (a)  A logic diagram with inputs A and B. Input A is connected to the first input of a top AND gate and the second input of a bottom AND gate. Input B is connected to the second input of the top AND gate and the first input of the bottom AND gate. The outputs of both AND gates are connected to the inputs of an OR gate, whose output is labeled F.
- (b)  A logic diagram with inputs A and B. Input A is connected to the first input of a top AND gate and the second input of a bottom AND gate. Input B is connected to the second input of the top AND gate and the first input of the bottom AND gate. The outputs of both AND gates are connected to the inputs of an OR gate, whose output is labeled F.
- (c)  A logic diagram with inputs A and B. Input A is connected to the first input of a top AND gate and the second input of a bottom AND gate. Input B is connected to the second input of the top AND gate and the first input of the bottom AND gate. The outputs of both AND gates are connected to the inputs of an OR gate, whose output is labeled F.
- (d)  A logic diagram with inputs A and B. Input A is connected to the first input of a top AND gate and the second input of a bottom AND gate. Input B is connected to the second input of the top AND gate and the first input of the bottom AND gate. The outputs of both AND gates are connected to the inputs of an OR gate, whose output is labeled F.

Which one of the following circuits is the minimized logic circuit for the circuit shown in figure? (IES-2000)



The circuit shown in the given figure realizes the function. (IES-2000)



- (a)  $(\overline{A + B} + C)(\overline{D} \overline{E})$
- (b)  $(\overline{A + B} + C)(D \overline{E})$
- (c)  $(A + \overline{B + C})(\overline{D} E)$
- (d)  $(A + B + \overline{C})(\overline{D} \overline{E})$

The logic operations of two combinational circuits given in figure-I and figure-II are  
**(IES-2000)**

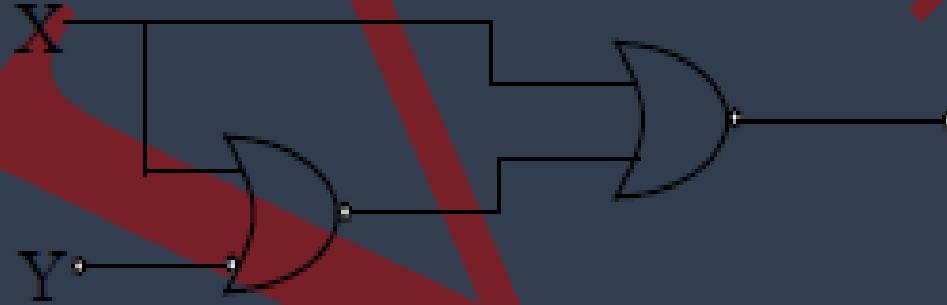


Figure I

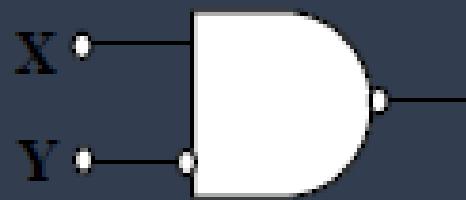


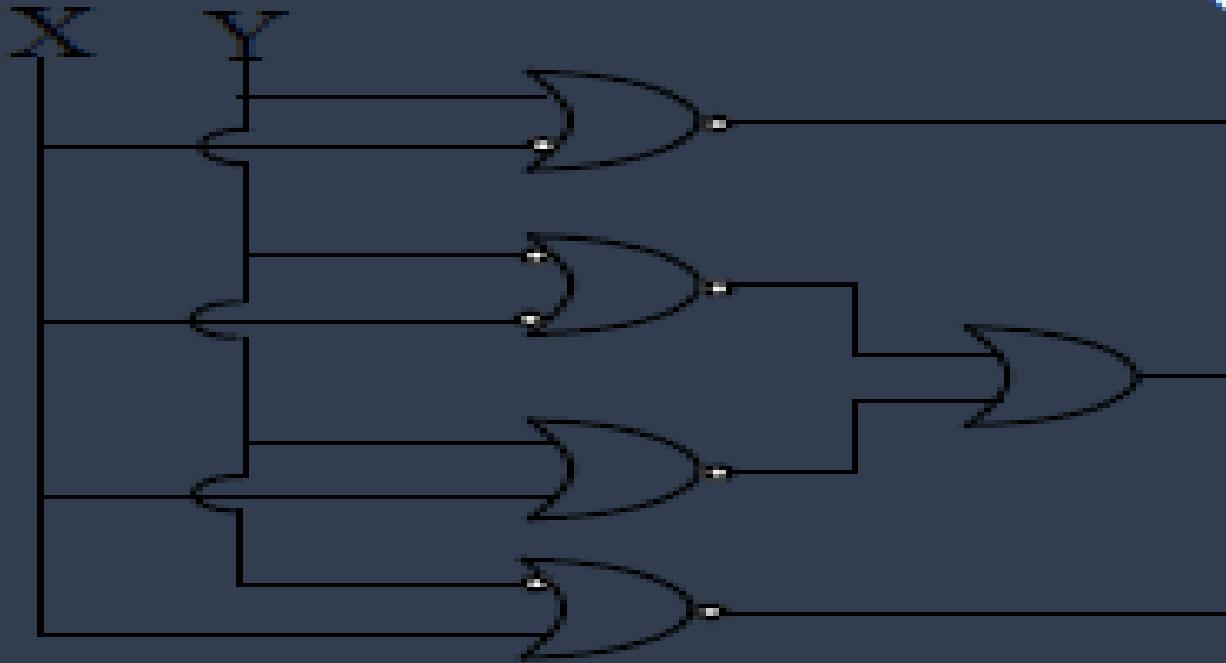
Figure II

- (a) entirely different
- (b) identical
- (c) complementary
- (d) dual

If the output of a logic gate is ‘1’ when all its inputs are at logic ‘0’ the gate is either.  
**(IES-2001)**

- (a) a NAND or NOR
- (b) and AND or an EX-NOR
- (c) an OR or a NAND
- (d) an EX-OR or an EX-NOR

The circuit shown in the given figure is  
(IES-2001)

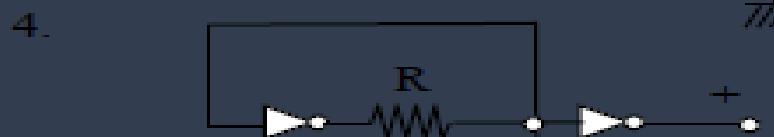
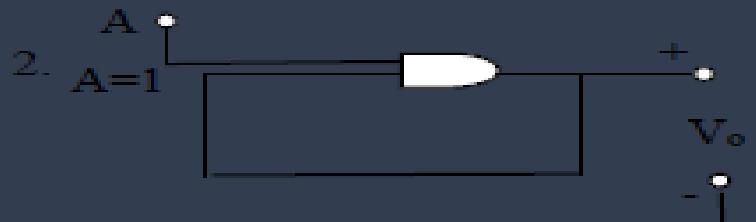


- (a) an adder circuit
- (b) a subtractor circuit
- (c) a comparator circuit
- (d) a parity generator circuit

How is inversion achieved using EX – OR gate? (IES-2002)

- (a) Giving input signal to the two input lines of the gate tied together.
- (b) Giving input to one input line and logic zero to the other line.
- (c) Giving input to one input line and logic one to the other line.
- (d) Inversion cannot be achieved using EX- OR gate.

Consider the following circuits (Assume all gates to have a finite propagation delay). Which of these circuits generate a periodic square wave output? (IES-2002)



- (a) 1 and 2      (b) 3 and 4  
(c) 2, 3 and 4    (d) 1, 2, 3 and 4

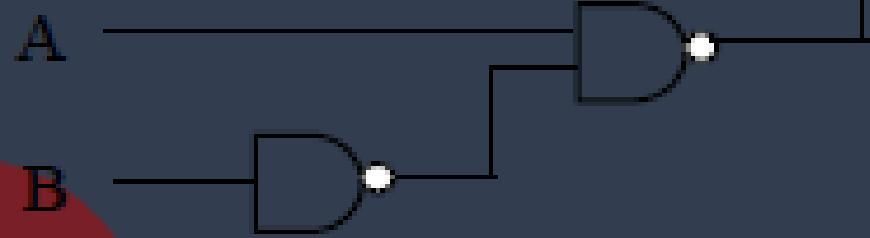
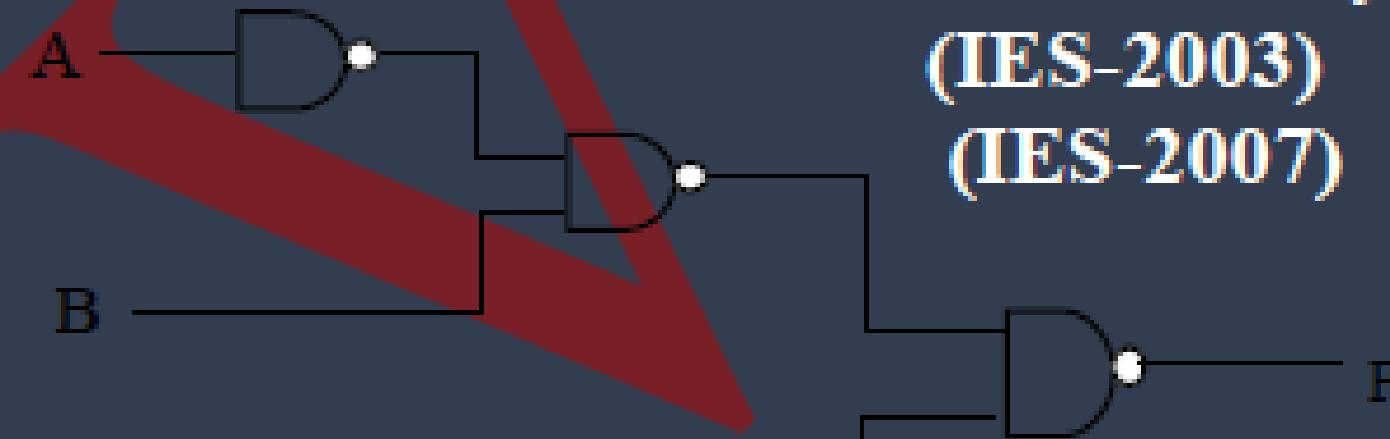
Q. The output of a logic gate is '1' when all its inputs '0'. Then the gate is either  
**(IES-2003)**

- (a) A NAND or an EX-OR gate
- (b) A NOR or an EX-NOR gate.
- (c) An OR or an EX-NOR gate.
- (d) An AND or an EX-OR gate.

The circuit shown below is functionally equivalent to

(IES-2003)

(IES-2007)



- (a) NOR gate      (b) OR gate
- (c) EX-OR gate      (d) NAND gate

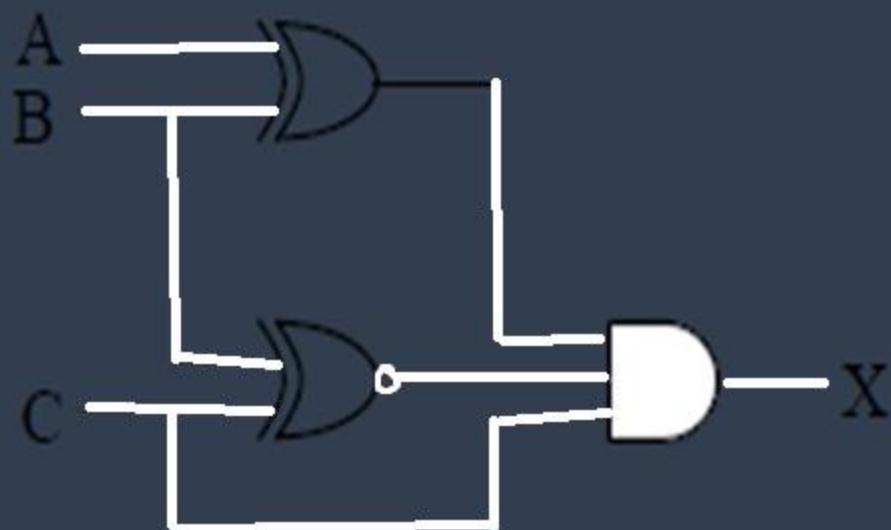
Assume that only  $x$  and  $y$  logic inputs are available, and their complements  $\bar{x}$  and  $\bar{y}$  are not available. What is the minimum number of 2-input NAND gates required to implement  $x \oplus y$ ? (IES-2004)

- (a) 2
- (b) 3 (IES-2007)
- (c) 4
- (d) 5

Consider the following logic circuit:

What is the required input condition (A, B, C) to make the output  
above logic circuit? (IES-2004)

(IES-2008)



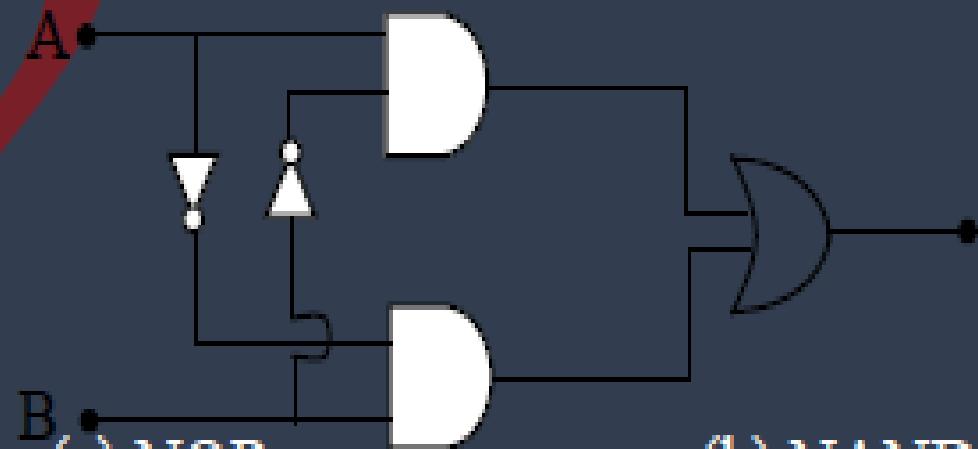
$X = 1$ , for the

The Boolean expression  $Y(A, B, C) = A + BC$  is to be realized using 2-input gates of only one type. What is the minimum number of ~~gates required for the realization?~~(IES-2006)

- (a) 1
- (b) 2
- (c) 3
- (d) 4 or more

Which one of the following logical operations is performed by the digital circuit shown below?

(IES-2006)

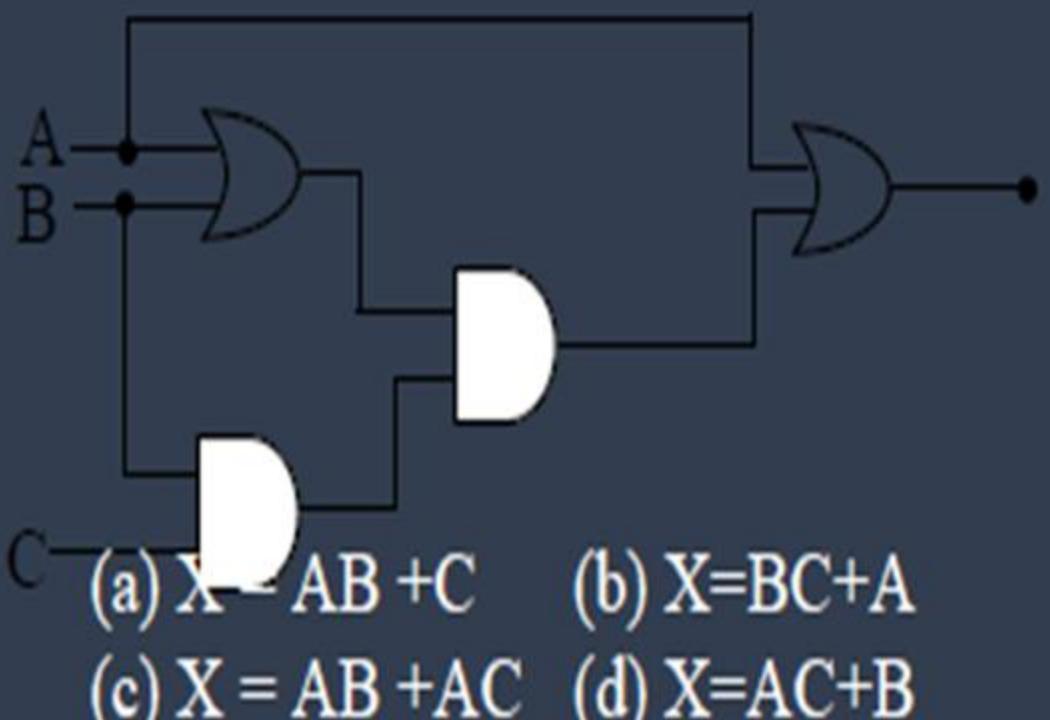


- (a) NOR
- (b) NAND
- (c) EX-OR
- (d) OR

. What is the Boolean expression  $A \oplus B$  equivalent to? (IES-2006)

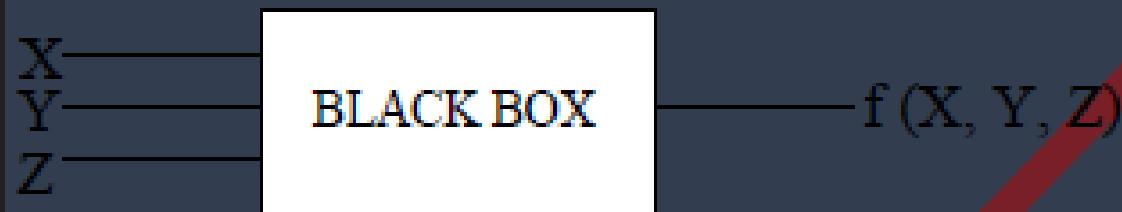
- (a)  $AB + \bar{A} \bar{B}$
- (b)  $\bar{A} B + A \bar{B}$
- (c)  $B$
- (d)  $\bar{A}$

For the logic circuit given above, what is the simplified Boolean function?  
(IES-2007)



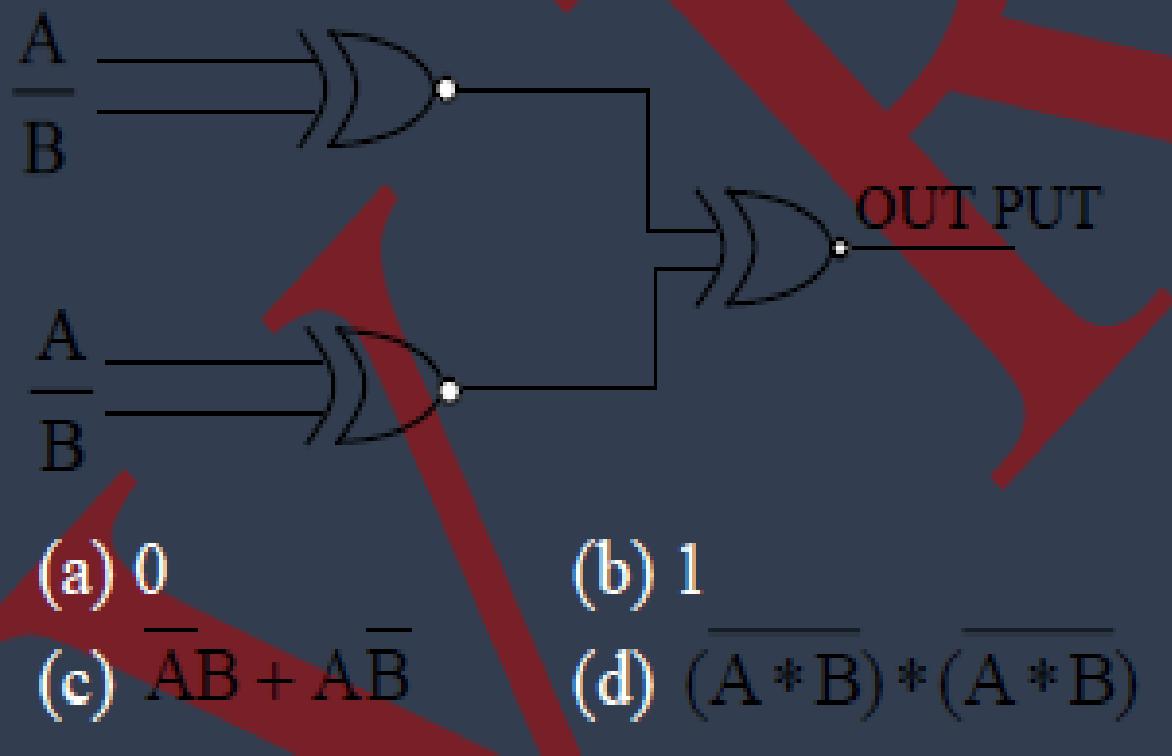
The black box in the below figure consists of a minimum complexity circuit that uses only AND, OR and NOT gates.

The function  $f(x, y, z) = 1$  whenever  $x, y$  are different and 0 otherwise. In addition the 3 inputs  $x, y, z$  are never all the same value. Which one of the following equations leads to the correct design for the minimum complexity circuit? (IES-2007)



- (a)  $X'Y + XY'$
- (b)  $X + Y'Z$
- (c)  $X'Y'Z' + XY'Z$
- (d)  $XY + Y'Z + Z'$

Q. The output of the circuit shown in the figure is equal to (IES-2008)



- (a) 0
- (b) 1
- (c)  $\overline{AB} + \overline{A}\overline{B}$
- (d)  $(\overline{A * B}) * (\overline{A * B})$

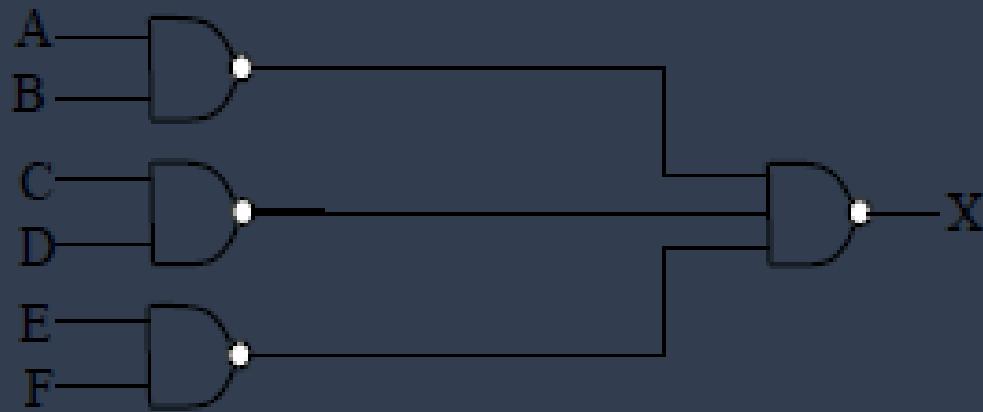
Which of the following are universal gates

(IES-2009)

- 1. NAND
- 2. NOR

3. XOR    Select the correct answer from the codes given below:

- (a) 1 and 2 only
- (b) 1 and 3 only
- (c) 2 and 3 only
- (d) 1, 2 and 3



The output X of the above logic circuits is:

(IES-2009)

- (a)  $AB + CD + EF$
- (b)  $\overline{AB} + \overline{CD} + \overline{EF}$
- (c)  $(A + B)(C + D)(E + F)$
- (d)  $(\overline{A + B})(\overline{C + D})(\overline{E + F})$

. Which of the following are universal gate?

- 1. AND    2. NAND    3. OR
  - 4. NOR    5. NOT
- (a) 1, 2, 3, 4 and 5
  - (b) 1, 3 and 4 only
  - (c) 2, 3 and 5 only
  - (d) 2 and 4 only

(IES-2011)

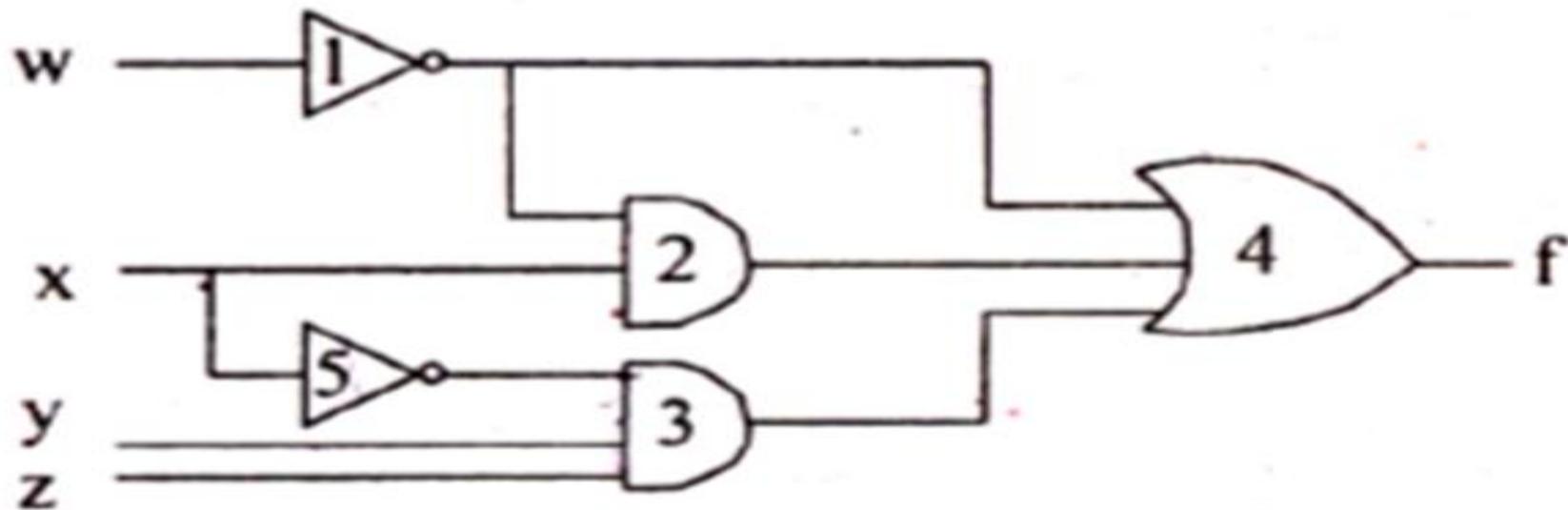
The logic function;  $\text{Out} = ab + bc + ca$  defines :

(IES-2011)

- 1. The output of a 3-inputs XOR gate
  - 2. The output of a 3-inputs majority gate
  - 3. The sum output of a full adder
  - 4. The carry output of a full adder
- (a) 1 and 2      (b) 2 and 3  
(c) 3 and 4      (d) 2 and 4

Consider the following gate network:

MES 2011



Which one of the following gates is redundant

- (a) Gate No. 1      (b) Gate No. 2
- (c) Gate No. 3      (d) Gate No. 4

The function  $(A \oplus B)$  is to be realized using only 2 input NAND gates. The minimum number of 2 – input NAND gates required for such a realization is

The minimum number of gates required to realize the function  $AB + \overline{C}$  (Using NAND gates only) is

(IES - 2015)

- (a) 2
- (b) 3
- (c) 4
- (d) 6

According to De Morgan's second theorem

- (a) A NAND gate is always complimentary to an AND gate
- (b) A NAND gate equivalent to a bubbled NAND gate
- (c) A NAND gate is equivalent to a bubbled AND gate
- (d) A NAND gate is equivalent to a bubbled OR gate.

There are four Boolean variables  $x_1, x_2, x_3$  and  $x_4$ . The following functions are defined on sets of them:

$$f(x_3, x_2, x_1) = \Sigma(3, 4, 5)$$

$$g(x_4, x_3, x_2) = \Sigma(1, 6, 7)$$

$$h(x_4, x_3, x_2, x_1) = fg.$$

Then  $h(x_4, x_3, x_2, x_1)$  is

(a) zero

(b)  $\Sigma(3, 12, 13)$

(c)  $\Sigma(3, 4, 5, 1, 6, 7)$

(d)  $\Sigma(3, 12, 15)$

Match List I with List II and select the correct answer using the codes given below the list:

**List I (Boolean identity)**

- A.  $Y \cdot (Y + Z)$
- B.  $Y + \bar{X} \cdot Z$
- C.  $Y \oplus Z$
- D.  $X + Y \cdot Z$

**List II (Boolean expression)**

- 1.  $(X + Z) \cdot (\bar{X} + Z)$
- 2.  $(Y)$
- 3.  $(Y + Z)$
- 4.  $(X+Z) \cdot (\bar{X} + \bar{Z})$

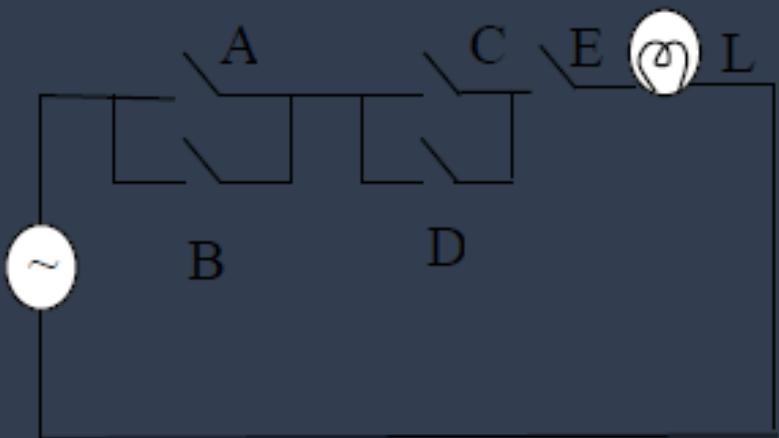
**Codes:**

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
(a)	1	2	4	3
(b)	2	3	1	4
(c)	2	3	4	1
(d)	3	2	1	4

(IES-EE - 95)

The switching circuit given in the figure can be expressed in binary logic notation

- (a)  $L = (A + B)(C + D)E$
- (b)  $L = AB + CD + E$
- (c)  $L = E + (A + B)(C + D)$
- (d)  $L = (AB + CD)E$



(IES-EE - 95)

Match List I with List II and select the correct answer using the codes given below the list:  
(IES-95)

List I	List II
(Boolean identity)	(Boolean expression)
A. $Y \cdot (Y + Z)$	1. $(X + Z)(\bar{X} + Z)$
B. $Y + \bar{X}Z$	2. $(Y)$
C. $Y \oplus Z$	3. $(Y + Z)$
D. $X + YZ$	4. $(X+Z) \cdot (\bar{X} + \bar{Z})$

*Codes:*

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
(a)	1	2	4	3
(b)	2	3	1	4
(c)	2	3	4	1
(d)	3	2	1	4

Match List-I (Expression-I) with List-II (Expression-II) and select the correct answer using the code given below the lists:

**List-I** (IES-08)

- A.  $ABC + AB\bar{C} + A\bar{B}C$
- B.  $\bar{A}B\bar{C} + AB\bar{C} + B\bar{C}$
- C.  $\bar{A}BC + A\bar{B}C + A\bar{B}\bar{C} + ABC$
- D.  $\bar{A}\bar{B} + \bar{A}B + ABC$

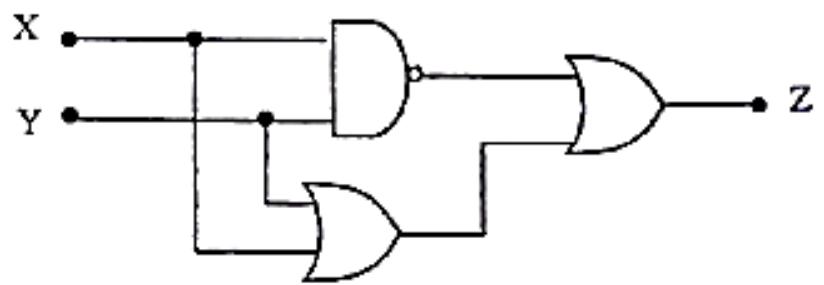
**List-II**

- 1.  $\bar{A} + BC$
- 2.  $A(B+C)$
- 3.  $B\bar{C}$
- 4.  $AB + BC + AC$

*Codes:*

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
(a)	2	1	4	3
(b)	4	3	2	1
(c)	2	3	4	1
(d)	4	1	2	3

Which of the following is the truth table of  
the given logic circuit? (IES-96)



(a)

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	1

(b)

X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

(c)

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

(d)

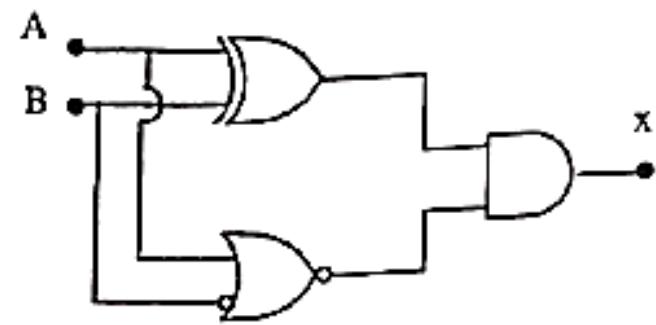
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	0

The output of an EX-OR gate with A and B as inputs will be

(IES-98)

- (a)  $AB + \overline{AB}$
- (b)  $(A + B)(\overline{A} + \overline{B})$
- (c)  $(A + B)\overline{AB}$
- (d)  $\overline{\overline{A} + \overline{B}} + AB$

The output X of the circuit shown in the figure will be (IES-98)



- (a)  $AB$
- (b)  $\overline{A}B$
- (c)  $A\overline{B}$
- (d)  $\overline{A}\overline{B}$

Consider the following statements:

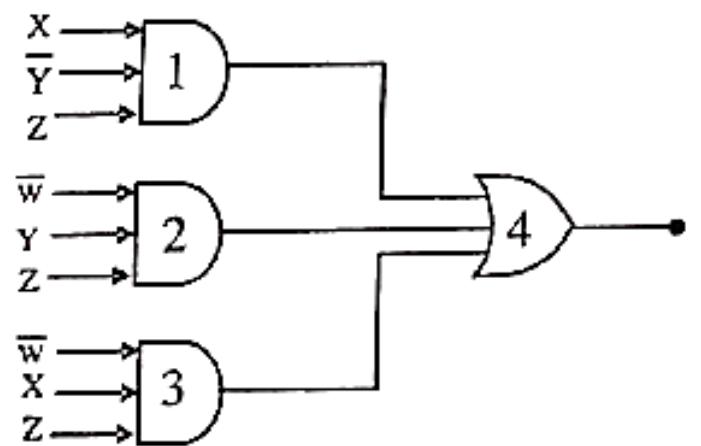
1. A NAND gate is equivalent to an OR gate with its inputs inverted
2. A NOR gate is equivalent to an AND gate with its inputs inverted
3. A NAND gate is equivalent to an OR gate with its output inverted
4. A NOR gate is equivalent to an AND gate with its output inverted

Which of these statements are correct?

(IES-99)

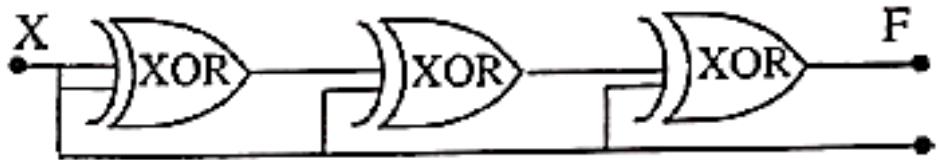
- |             |             |
|-------------|-------------|
| (a) 1 and 2 | (b) 2 and 3 |
| (c) 3 and 4 | (d) 1 and 4 |

Which one of the gate labeled 1, 2, 3 and 4 in the network shown in the figure is redundant? (IES-99)



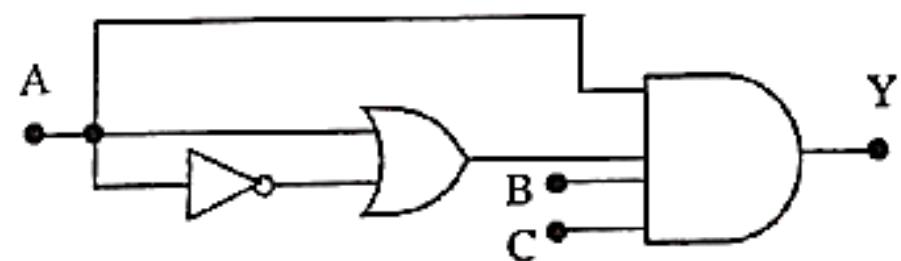
- (a) 1
- (b) 2
- (c) 3
- (d) 4

For the circuit shown in the below figure,  
the output F will be (IES-01)



- (a) 1
- (b) zero
- (c) X
- (d)  $\bar{X}$

The Boolean expression for the output Y in  
the logic circuit is (IES-02)



- (a)  $A \bar{B}C$
- (b)  $ABC$
- (c)  $\bar{A}\bar{B}C$
- (d)  $\bar{A}\bar{B}\bar{C}$

Consider the following:

Any combinational circuit can be built using

1. NAND gates
2. NOR gates
3. EX-OR gates
4. Multiplexers

Which of these are correct?

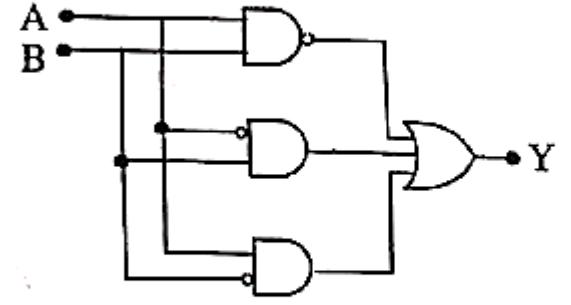
- (a) 1, 2 and 3      (b) 1, 3 and 4  
(c) 2, 3 and 4      (d) 1, 2 and 4

The AND function can be realized by using only n number of NOR gates. What is n equal to?

(IES-08)

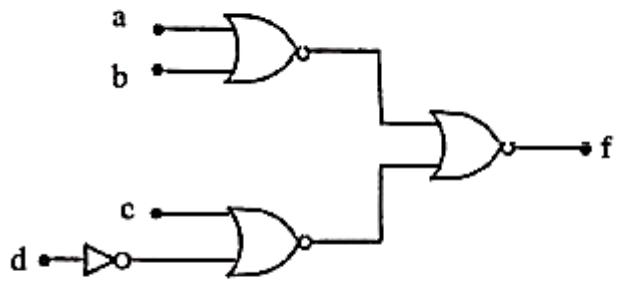
- (a) 2
- (b) 3
- (c) 4
- (d) 5

In the given circuit, the output Y equals  
which one of the following? (IES-08)



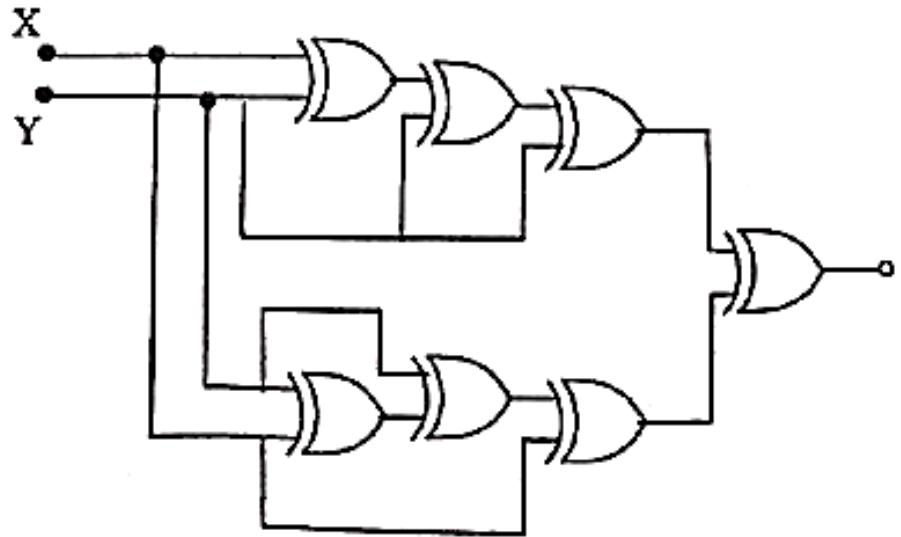
- (a)  $A+B$
- (b)  $\bar{A}\bar{B}+A\bar{B}$
- (c)  $AB$
- (d)  $\bar{A} + \bar{B}$

Which one of the following is the correct output (f) of the below circuit? (IES-09)



- (a)  $(a + b)(c + \bar{d})$
- (b)  $(\bar{a} + \bar{b})(c + \bar{d})$
- (c)  $(a + \bar{b})(c + \bar{d})$
- (d)  $(a + b)(\bar{c} + \bar{d})$

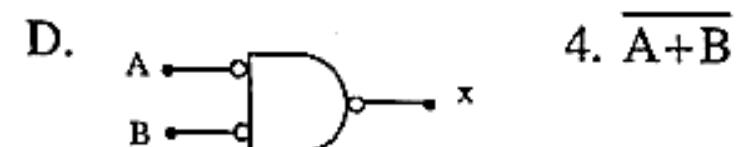
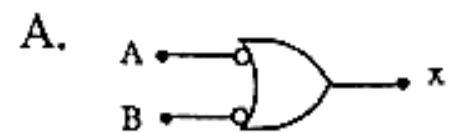
The circuit shown in the figure below generates the function of (IES-10)



- (a)  $X \oplus Y$
- (b) 0
- (c)  $X\bar{Y} + YX + \bar{Y}X$
- (d)  $X \cdot \bar{Y}$

Match List-I with List-II and select the correct answer using the codes given below the lists:  
(IES-10)

**List-I**



**List - II**

1.  $AB$

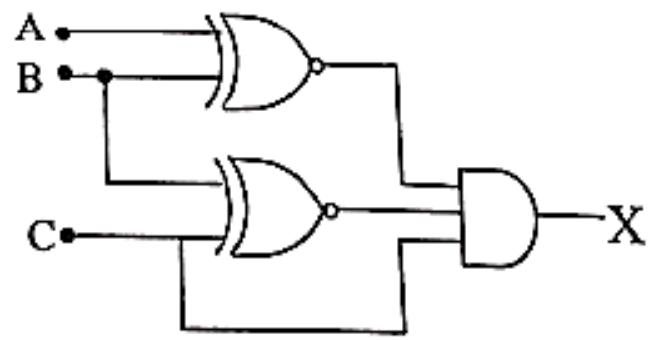
2.  $\overline{AB}$

3.  $A+B$

4.  $\overline{A+B}$

**Codes:**

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
(a)	3	1	4	2
(b)	2	1	4	3
(c)	3	4	1	3
(d)	2	4	1	3



For logic circuit shown, the required inputs A, B and C to make the output  $X = 1$  are, respectively.

(IES-11)

- (a) 1, 0 and 1
- (b) 0, 0 and 1
- (c) 1, 1 and 1
- (d) 0, 1 and 1

If the output of a logic gate is '1' when all its inputs are at logic '0', the gate is either

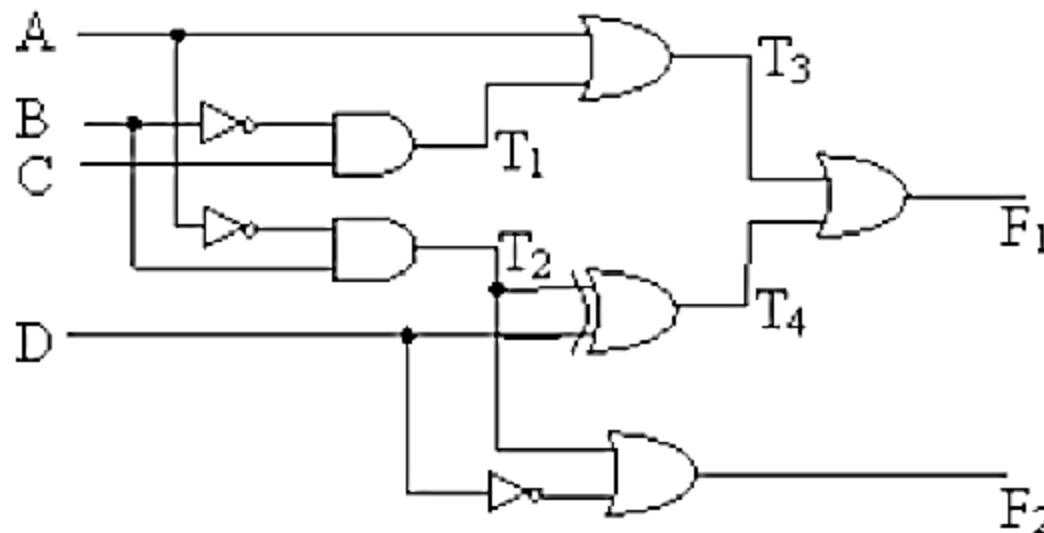
(IES-14)

- (a) A NAND or a NOR
- (b) An AND or an EX-NOR
- (c) An OR or a NAND
- (d) An EX-OR or an EX-NOR

Find the minimum number of 2—i/p NAND gates required to implement the above using a combinational logic circuit.

- (a) 9
- (b) 6
- (c) 7
- (d) 4

Consider the combinational circuit shown in Fig.

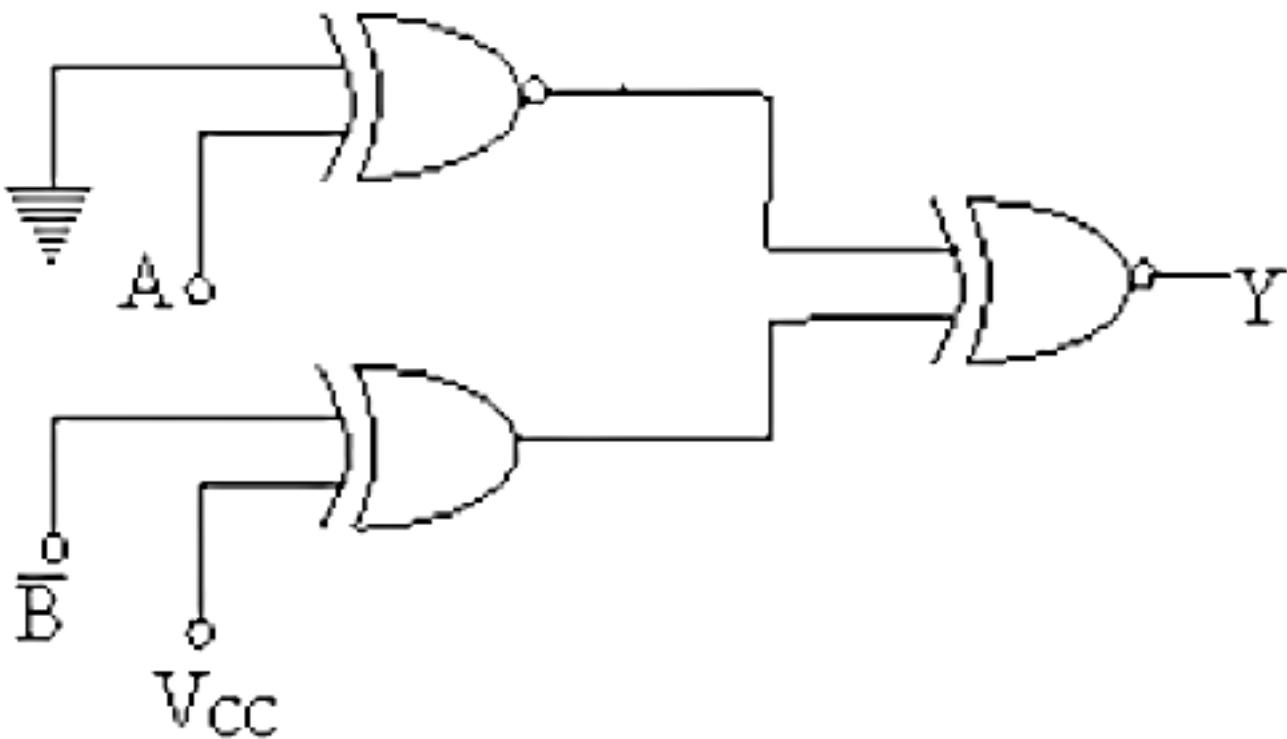


The expression for F<sub>1</sub> & F<sub>2</sub> respectively are

- (a)  $\overline{A} + \overline{B}C + \overline{B}\overline{D} + B\overline{D}$ ,  $\overline{\overline{AB}} + D$
- (b)  $A + \overline{B}C + \overline{B}\overline{D} + \overline{B}D$ ,  $\overline{AB} + D$
- (c)  $\overline{A} + \overline{B}C + \overline{B}\overline{D} + B\overline{D}$ ,  $\overline{\overline{AB}} + D$
- (d)  $A + \overline{B}C + \overline{B}\overline{D} + \overline{B}D$ ,  $\overline{AB} + \overline{D}$

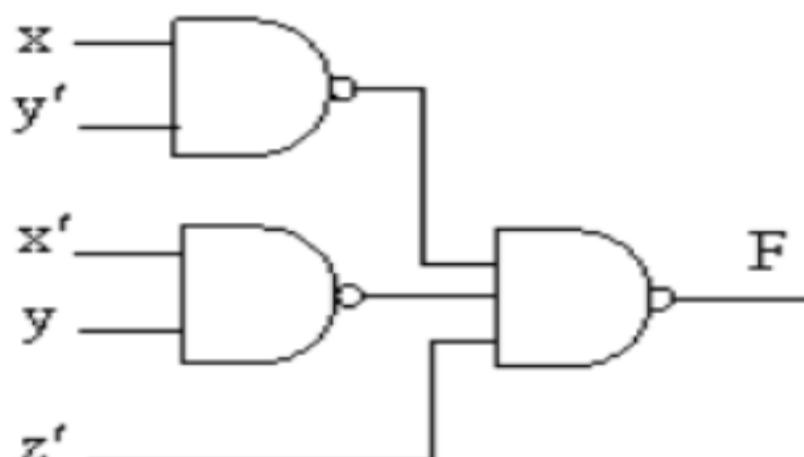
Consider the circuit shown below. The expression for the output Y is

- (a)  $(\bar{A} + \bar{B})(A + \bar{B})$
- (b)  $(\bar{A} + B)(A + \bar{B})$
- (c)  $\bar{A} + \bar{B}$
- (d)  $(A + B)(\bar{A} + \bar{B})$



Which of the following is the correct output expression for the following NAND-gate structure

- (a)  $F = \sum m(1, 2, 3, 4, 5, 7)$
- (b)  $F = \sum m(1, 2, 4, 5, 6)$
- (c)  $F = \sum m(1, 2, 4, 5, 7)$
- (d)  $F = 1$



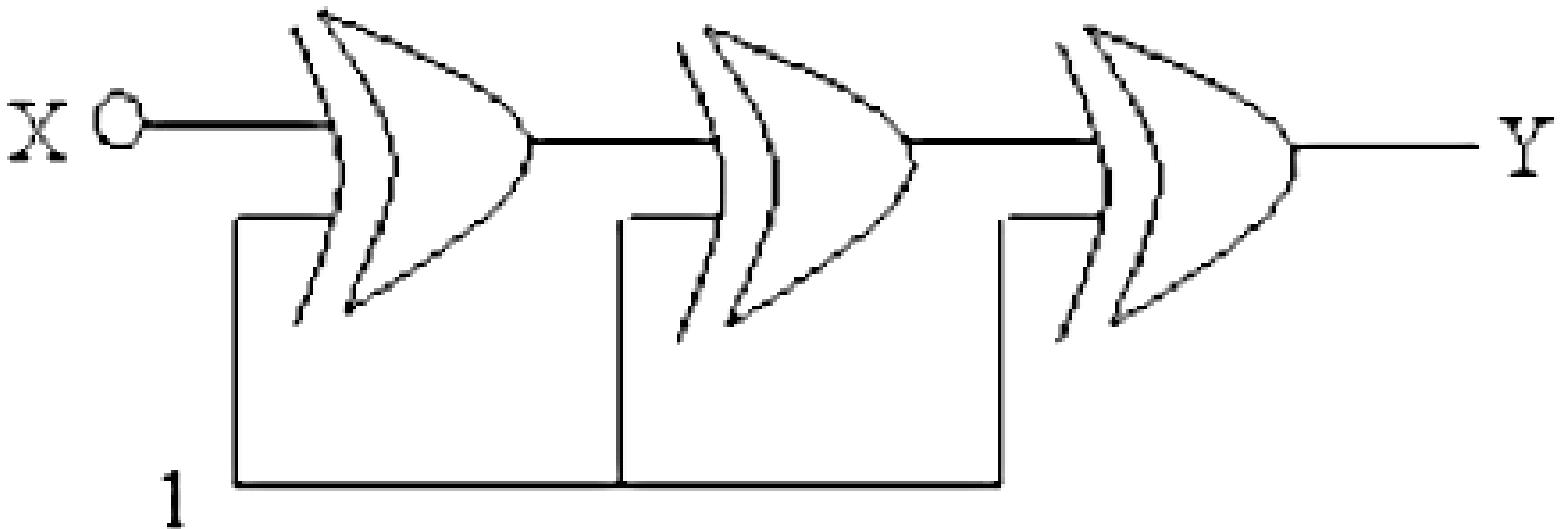
Minimum number of 2 - input NAND gates required to implement the function

$$F = (\overline{A} + \overline{B})(A + B)$$

- (a) 3
- (b) 4
- (c) 5
- (d) 6

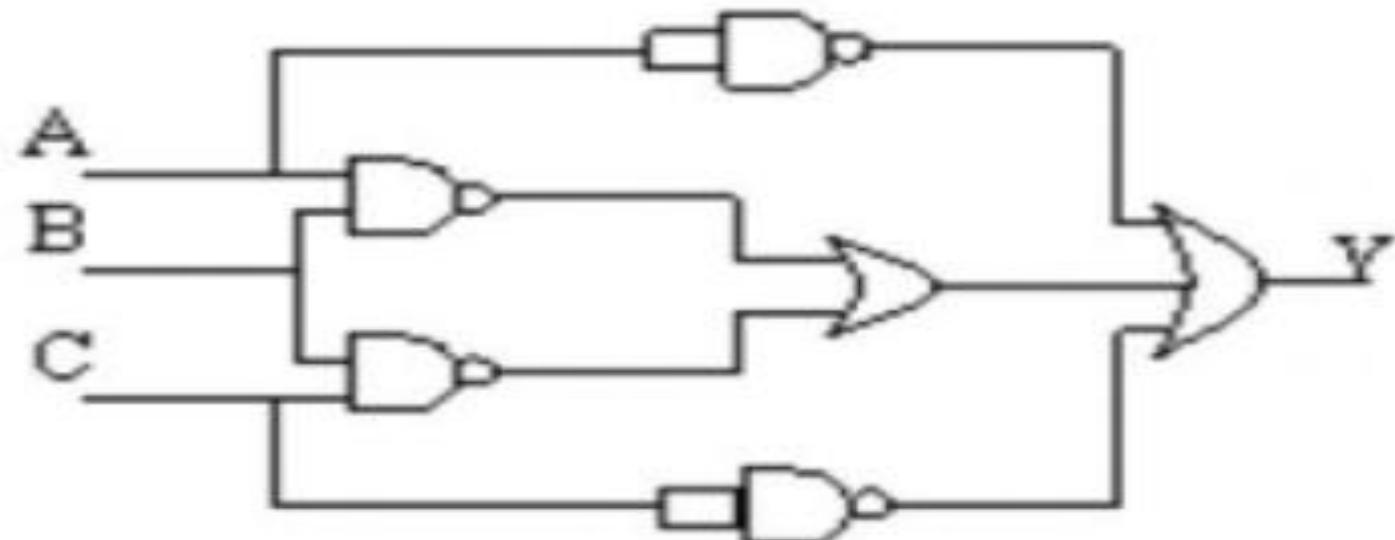
The output Y of the given circuit is

- (a) 1
- (b) Zero
- (c) X
- (d)  $\bar{X}$

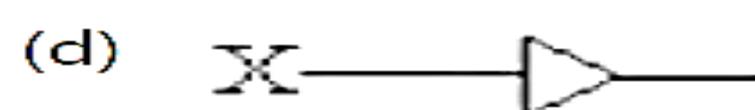
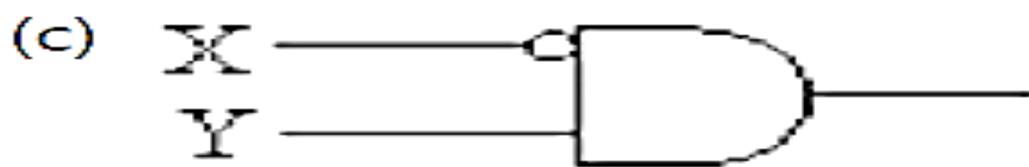
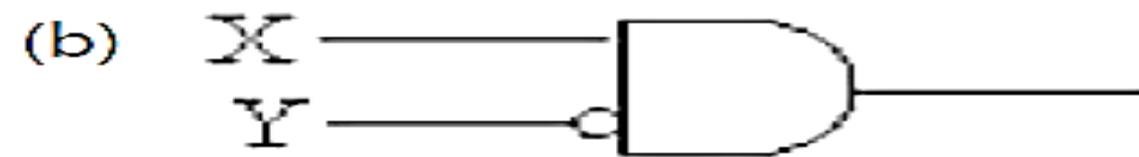
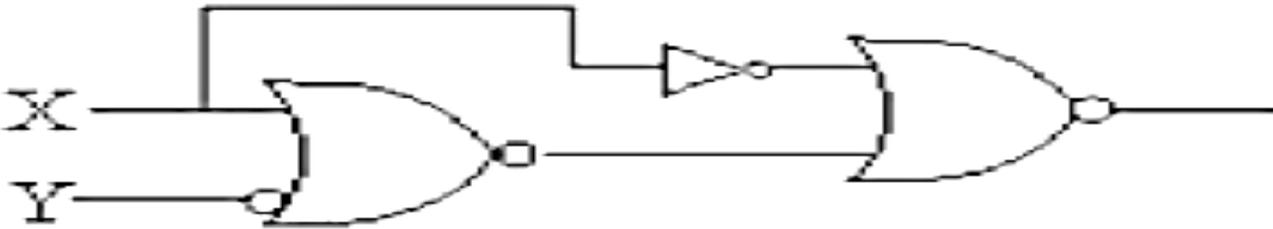


For the logic circuit shown in Figure, the output is equal to

- (a)  $\overline{ABC}$
- (b)  $\overline{A} + \overline{B} + \overline{C}$
- (c)  $\overline{AB} + \overline{BC} + \overline{A} + \overline{C}$
- (d)  $\overline{AB} + \overline{BC}$



The logic circuit shown below is equivalent to



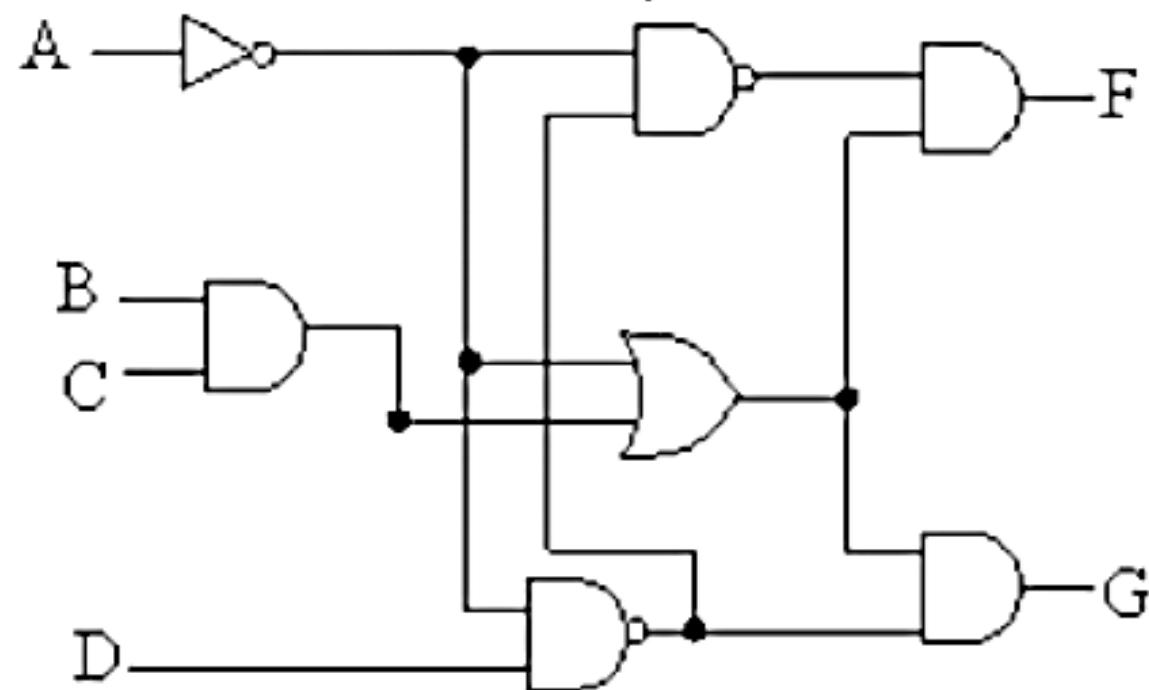
The simplified Boolean expression for output F in terms of the input variables in the circuit given below is

- (a)  $\overline{AD} + \overline{ABC}$

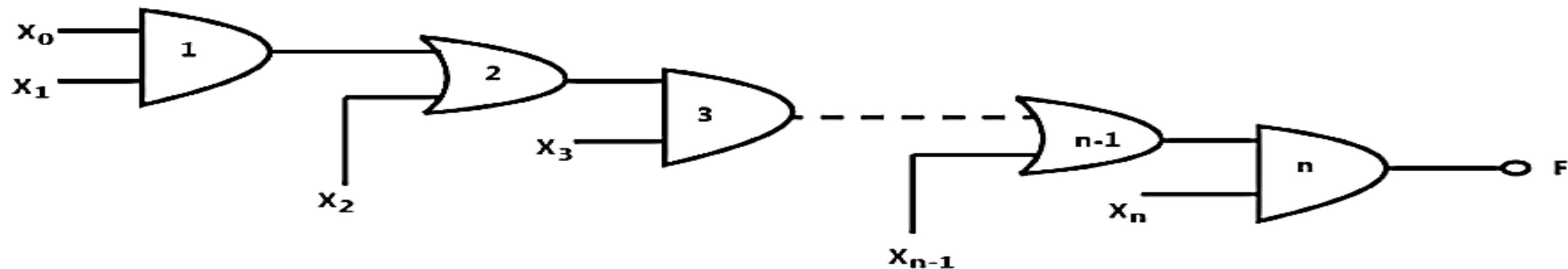
(b)  $\overline{\overline{AD}} + ABC$

(c)  $\overline{AB} + ADC$

(d)  $\overline{AD} + \overline{ABC}$

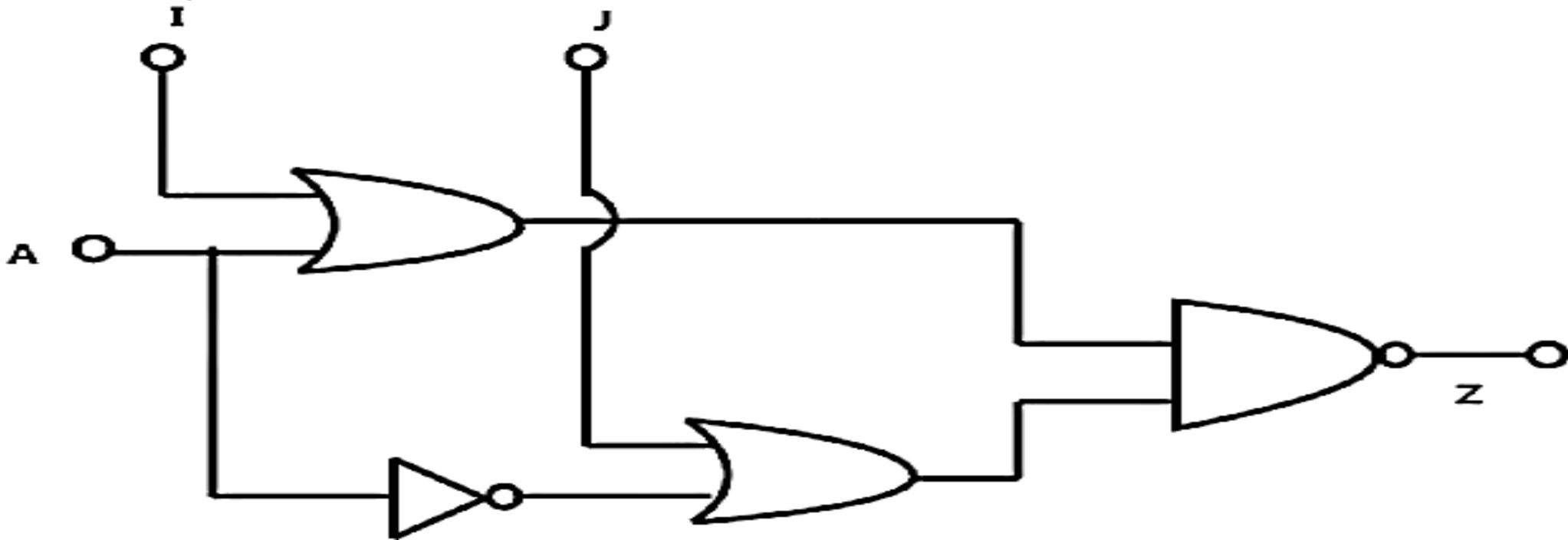


In the gate network shown below, find the output F.



- (a)  $X_0X_1X_3X_5 + X_2X_4X_5 \dots X_{n-1} + \dots X_{n-1}X_n$
- (b)  $X_0X_1X_3X_5 + X_2X_3X_4 \dots X_n + \dots X_{n-1}X_n$
- (c)  $X_0X_1X_3X_5 \dots X_n + X_2X_3X_5 \dots X_n + X_4X_5 \dots X_n + \dots X_{n-1}X_n$
- (d) None of these

If  $Z = F(A, B) = \overline{A} + B$ , then



- (a)  $I = 0$  and  $J = \overline{B}$   
(c)  $I = B$  and  $J = 1$

- (b)  $I = 1$  and  $J = B$   
(d)  $I = B$  and  $J = 0$

If  $F(A,B,C) = \sum m(0,1,2,3,5,6)$  then the minimized expression for the function F is

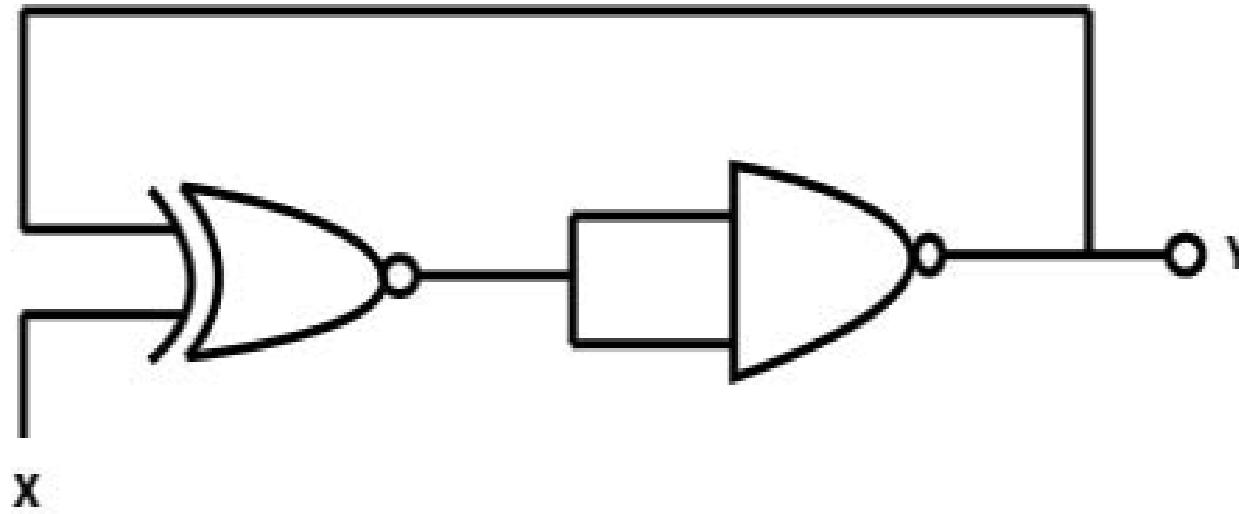
(a)  $A + (B \oplus C)$

(c)  $\overline{A} + (B \oplus C)$

(b)  $(A \oplus B) + C$

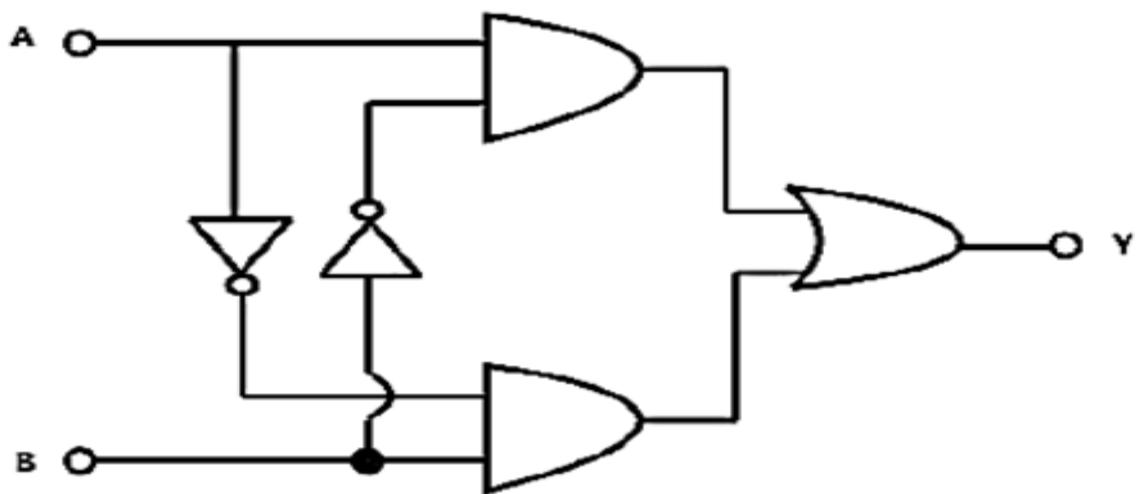
(d)  $\overline{ABC}$

All the logic gates in the circuit shown below have finite propagation delay. Circuit can be used as a clock generator, if  $X = \underline{\hspace{2cm}}$ .



Which of the following logical operations is performed by the digital circuit shown below?

- (a) NOR
- (b) NAND
- (c) EX-OR
- (d) OR



The logical operation performed by the given Boolean expression is  
 $wxyz + w'x'y'z' + w'xy'z + wx'yz'$

- (a)  $w \Theta x \Theta y \Theta z$
- (b)  $w \oplus x \oplus y \oplus z$
- (c)  $(w \Theta y).(x \Theta z)$
- (d)  $(w \oplus y).(x \oplus z)$

If  $A \oplus B = C$ , then which one of the following relation is NOT correct?

- (a)  $A \oplus C = B$
- (b)  $B \oplus C = A$
- (c)  $A \oplus B \oplus C = 0$
- (d)  $A \oplus B \oplus C = 1$

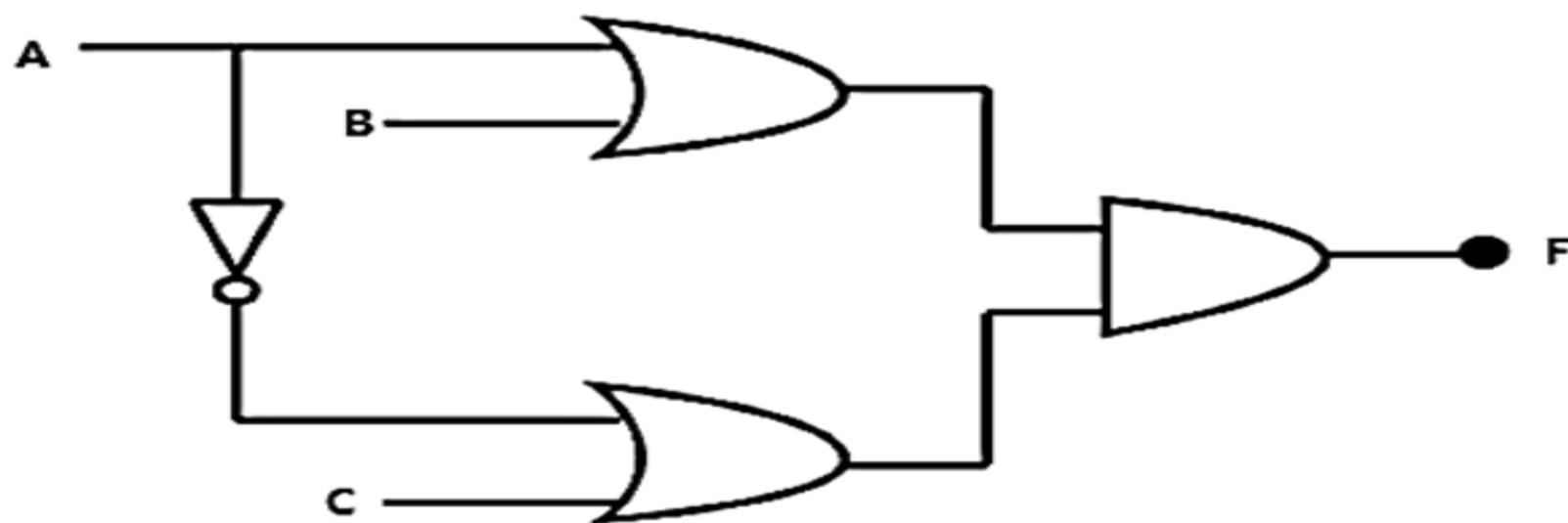
The minimized SOP logical expression of the given digital circuit is

(a)  $F = (A+B).C$

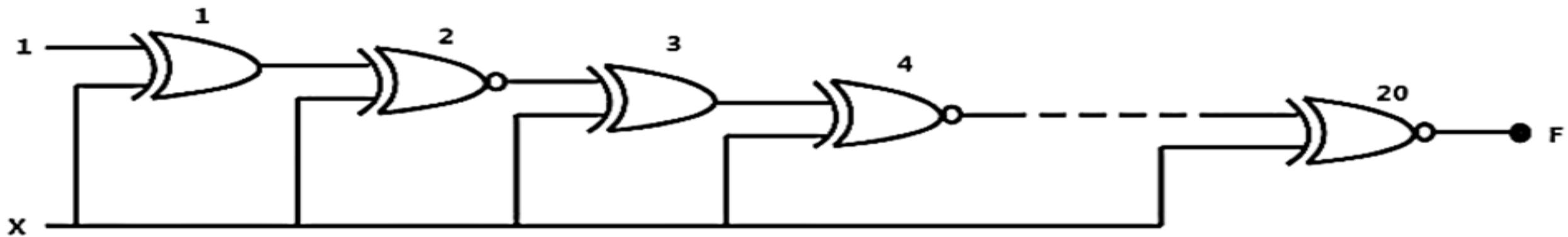
(b)  $F = (A+B).\left(\overline{A} + \overline{C}\right)$

(c)  $F = AC + \overline{AB}$

(d)  $F = AC + \overline{AB} + BC$



The output of the given following logic circuit is



- (a)  $X$
- (c) 0

- (b)  $\bar{X}$
- (d) 1

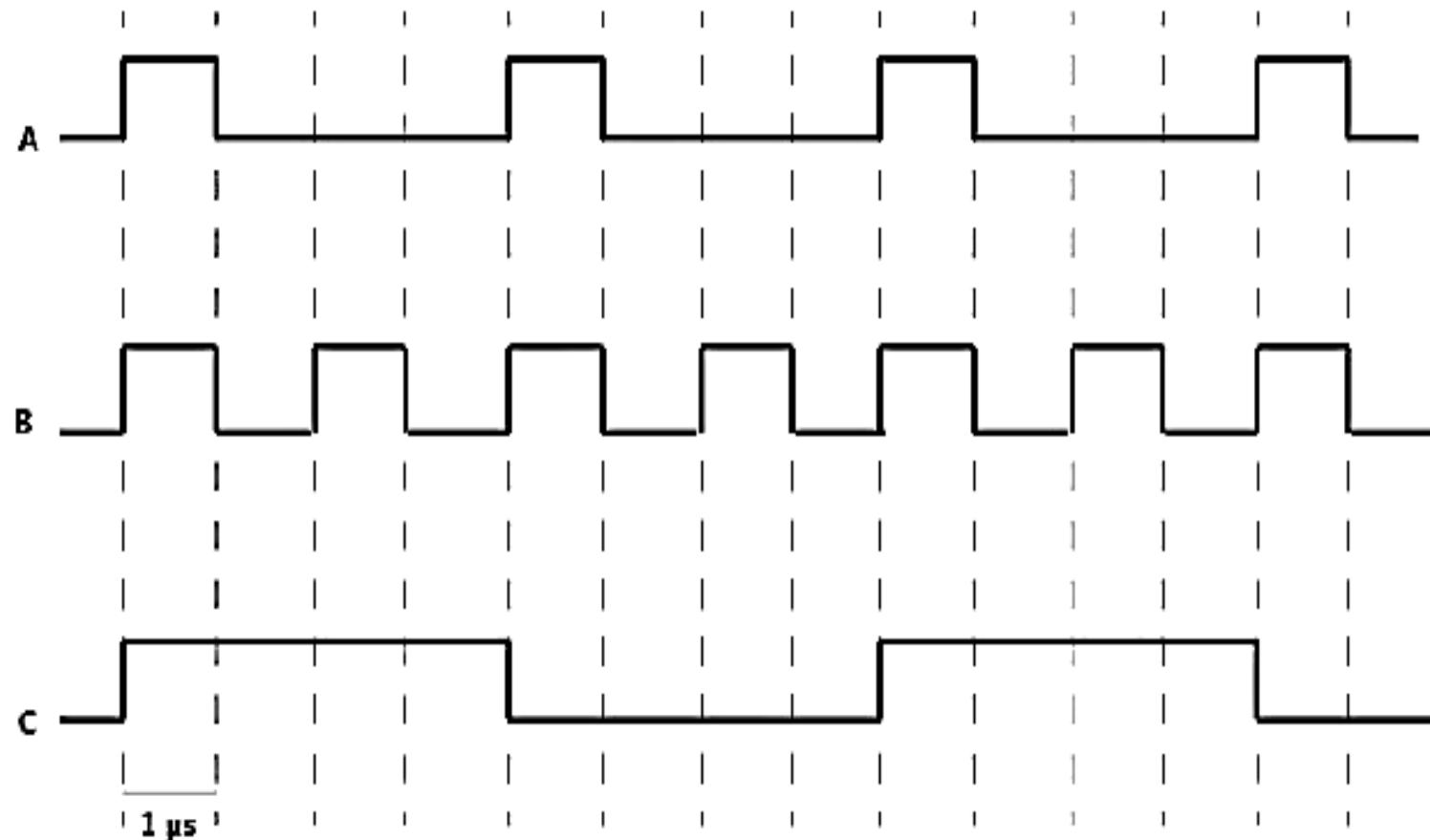
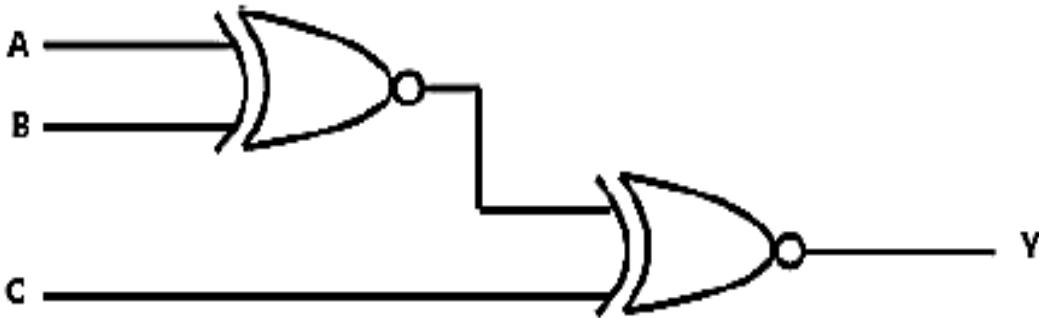
The minimum number of 2-input NAND gate required for the implementation of the given function  $F(A,B,C) = \overline{\overline{A} + BC}$  is \_\_\_\_\_.

The minimum number of 2-input NOR gate required for the implementation of the given following function  $F(A,B,C) = \overline{\overline{ABC}} + \overline{AC} + \overline{C}$  is \_\_\_\_\_.

For a two level combination of gates which of the following combination is Degenerate form

- (a) NAND - NAND
- (b) OR - NAND
- (c) NAND - NOR
- (d) NAND – AND

If the waveforms A, B, C shown in figure below are applied to the Ex-NOR gates. The frequency of output is \_\_\_ kHz.



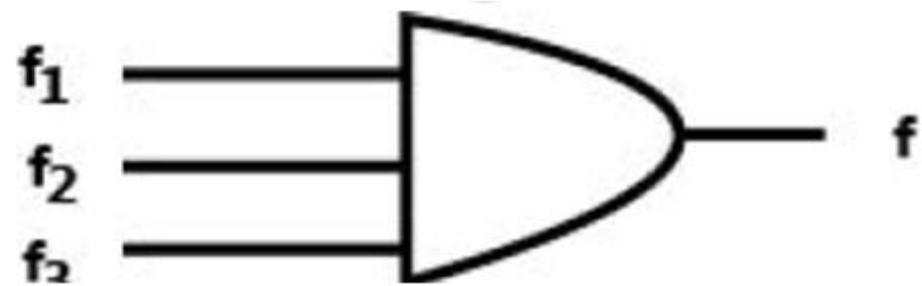
A car alarm system is to be designed considering 4 inputs, door closed (D), key in (K), seat pressure (S) and seat belt closed (B). The alarm (A) should sound if

1. the key is in and door is not closed or
2. the door is closed, the key is in, driver in the seat and seat belt is not closed.

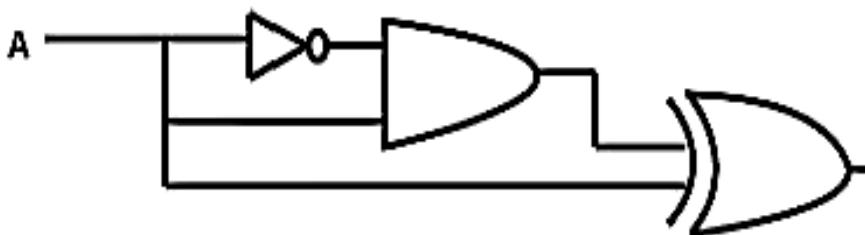
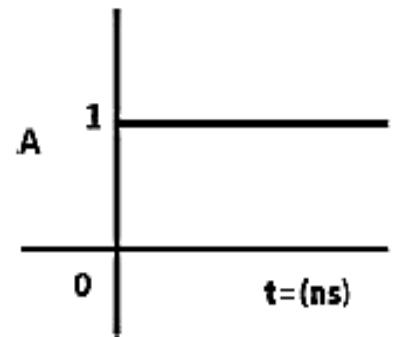
The system is to be designed with 2 input basic gates and inputs are available in basic form only. The number of gates required are

- |       |       |
|-------|-------|
| (a) 6 | (b) 7 |
| (c) 8 | (d) 9 |

Consider the logical functions given below  $f_1(A,B,C) = \sum(2,3,4)$ ,  $f_2(A,B,C) = \prod(0,1,3,6,7)$ . If  $f$  is logic zero, then maximum number of possible minterms in function  $f_3$  are \_\_\_\_.

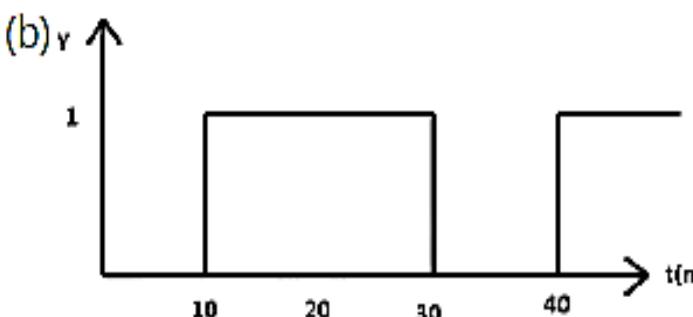


Consider the circuit shown in figure below

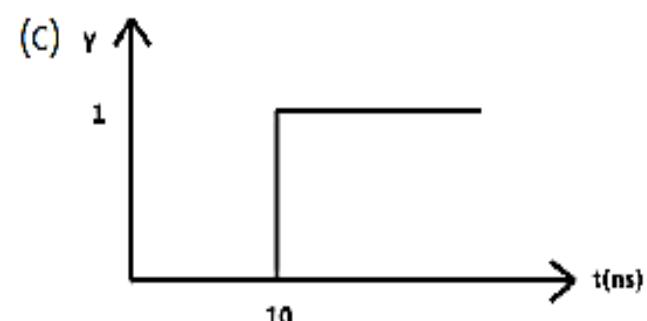


If propagation delay of NOT gate is 10 nsec, AND gate is 20 nsec and EX-OR gate is 10 nsec.  
If  $A$  is connected to  $V_{CC}$  at  $t = 0$ , then waveform for output  $Y$  is

(a)

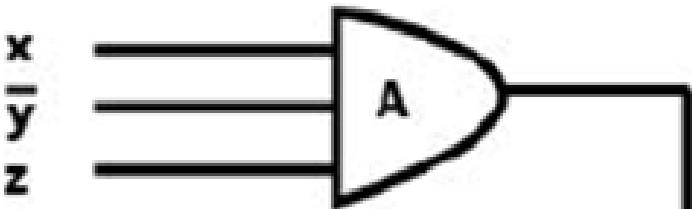


(c)



In the logic circuit shown below the redundant gate is

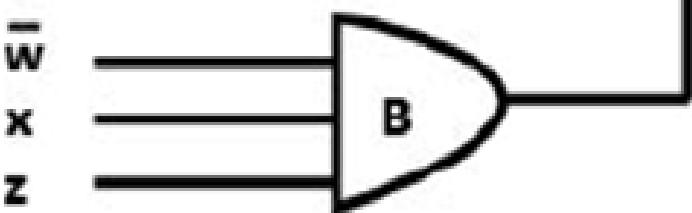
(a) A



(b) B



(c) C



(d) D

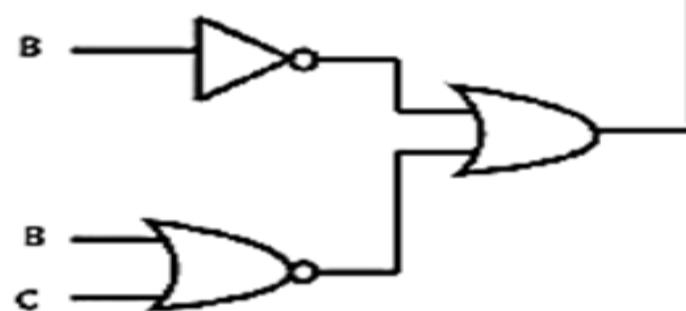
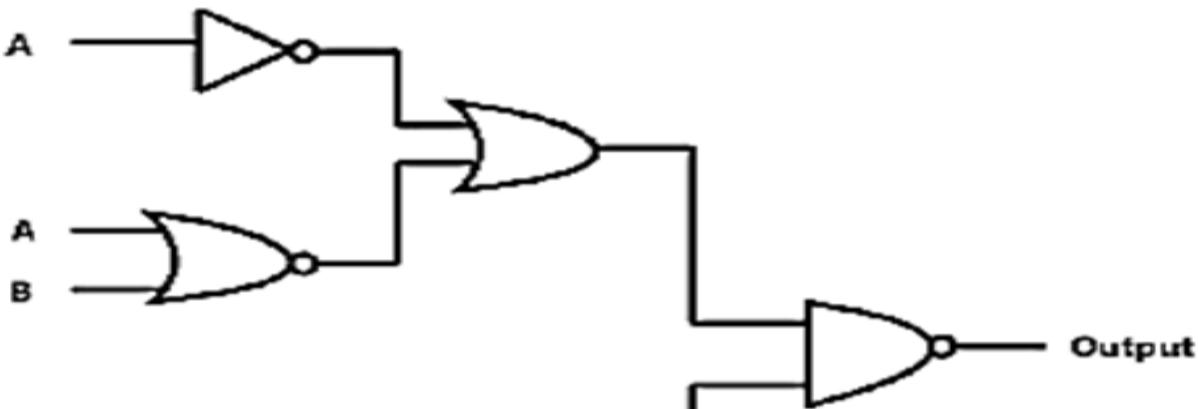
How many of the following gates given below follow associative law? EX-OR, NAND, AND, NOR, OR

(a) 5  
(c) 3

(b) 4  
(d) 6

The simplest possible logic diagram that implements the output of the logic diagram shown below is

- (a) AND gate
- (b) NAND gate
- (c) OR gate
- (d) NOR gate

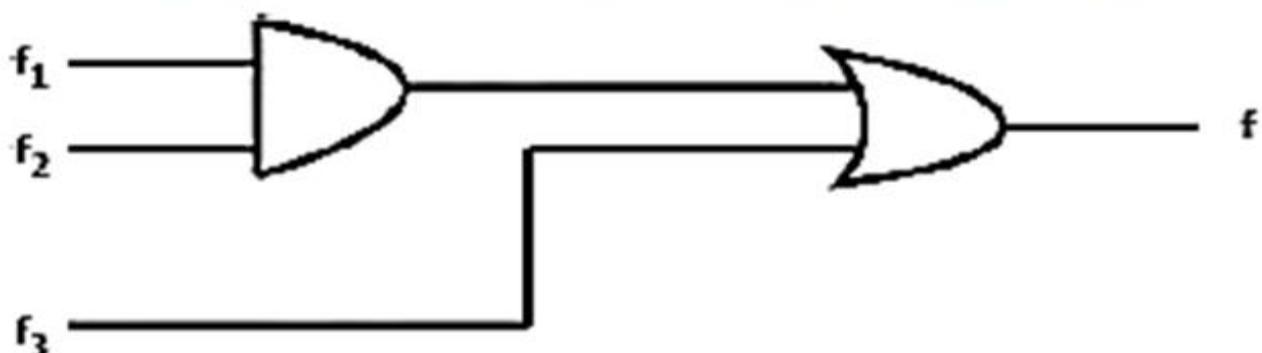


Consider the logic circuit shown in the figure given below. The function  $f_1$ ,  $f_2$ , and  $f$  (in sum of products form in decimal notation) are

$$f_2(w, x, y, z) = \sum m(2, 3, 4)$$

$$f_1(w, x, y, z) = \sum m(1, 4, 5, 6, 7, 8, 9)$$

$$f(w, x, y, z) = \sum m(4, 6)$$



Which of the following is the function  $f_3$ ?

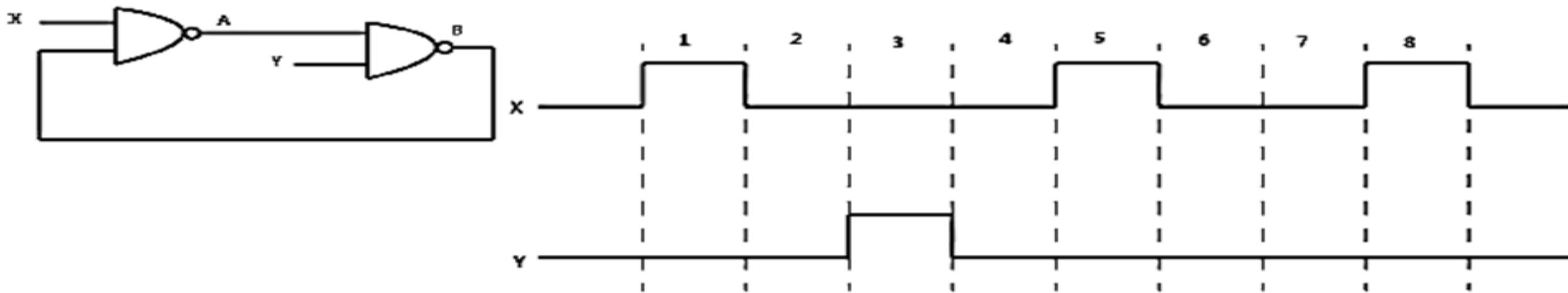
(a)  $\sum m(4, 6)$

(b)  $\sum m(4)$

(c)  $\sum m(6)$

(d)  $\sum m(4, 5, 6)$

Consider the digital circuit shown below Where, timing diagram is given below.



Value of A and B at 1, 3, 5 and 8 seconds are?

- (a) A = 0, 1, 0, 0, B = 1, 0, 1, 1
- (c) A = 1, 1, 0, 0, B = 1, 1, 0, 0

- (b) A = 1, 0, 1, 1, B = 0, 1, 0, 0
- (d) A = 0, 1, 0, 0, B = 0, 1, 0, 0

Using NAND gates only, \_\_\_\_\_ number of two input NAND gates are required to implement below operations.

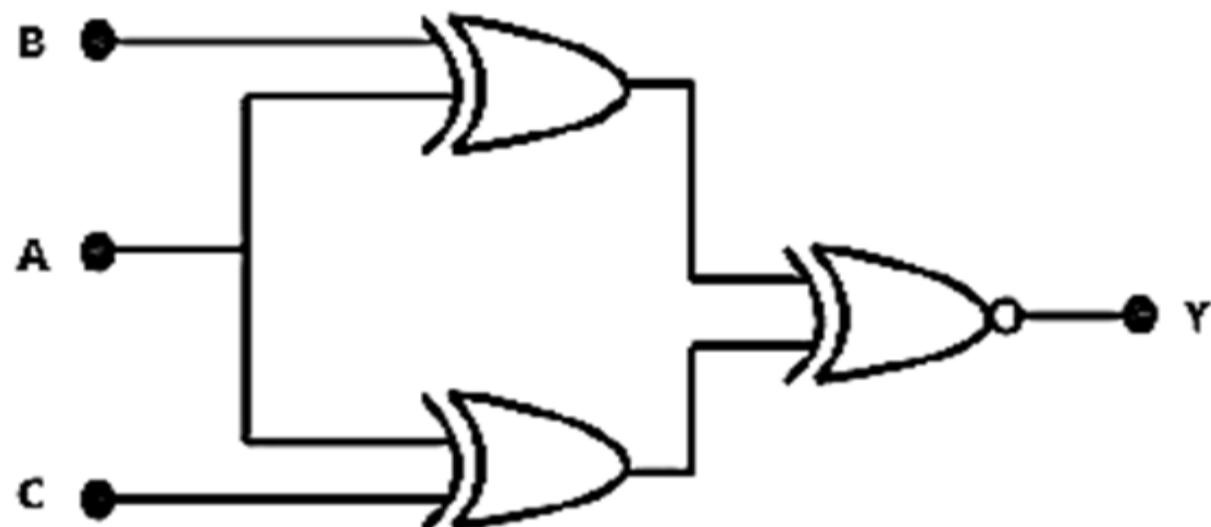
$$F = \overline{\overline{xy}} + \overline{xy} + \overline{yz}$$

Using NOR gates only, \_\_\_\_\_ number of 2 inputs NOR gates are required to implement below operations.

$$F = \overline{\overline{xy}} + \overline{xy} + \overline{yz}$$

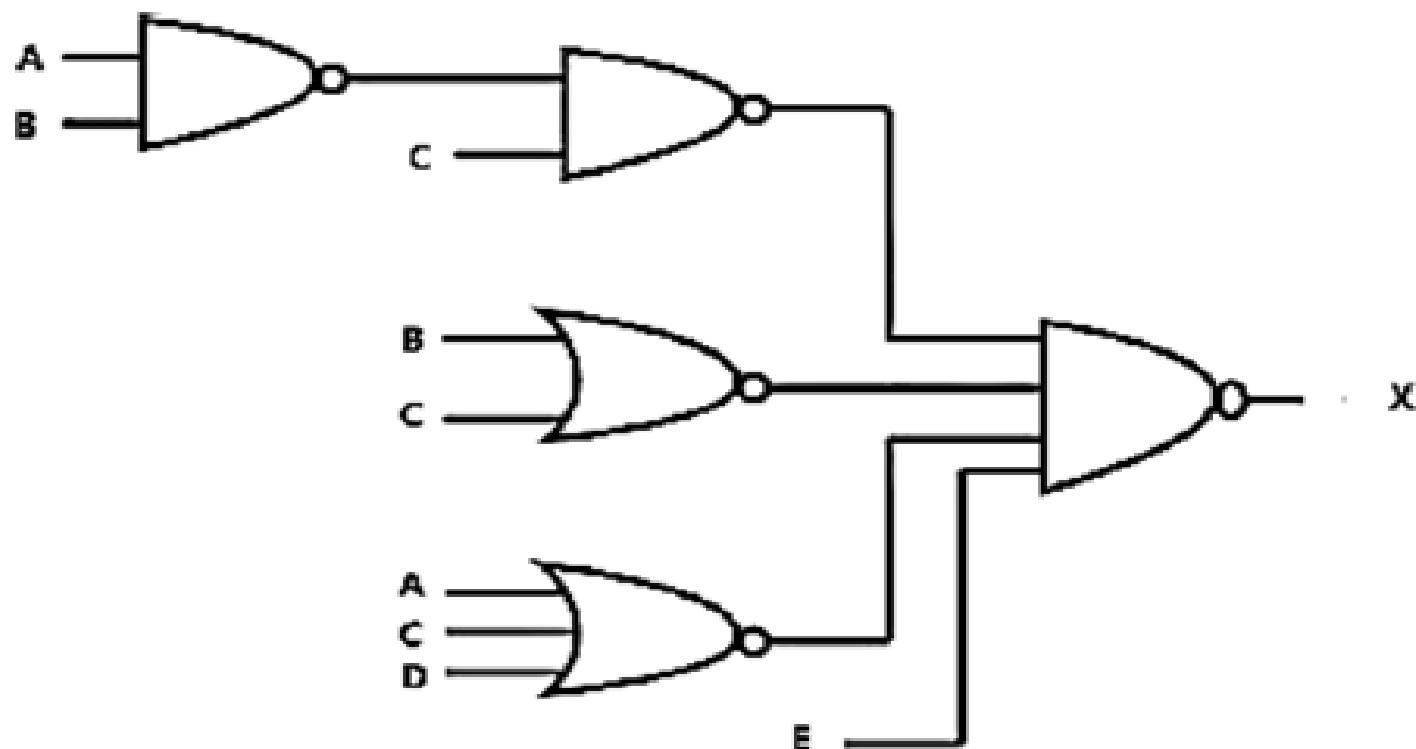
In the logic circuit shown in below figure, if inputs are A, B and C and the output is 'Y' then

- (a) 'Y' is independent of 'A'
- (b) Y = 0 for A = 1, B = 1, C = 1
- (c) 'Y' is independent of 'C'
- (d) Y = 1 for A = 1, B = 0 and C=1



The Boolean expression for the logic diagram given below is

(a)  $x = (A + B)C + BD + \bar{E}$



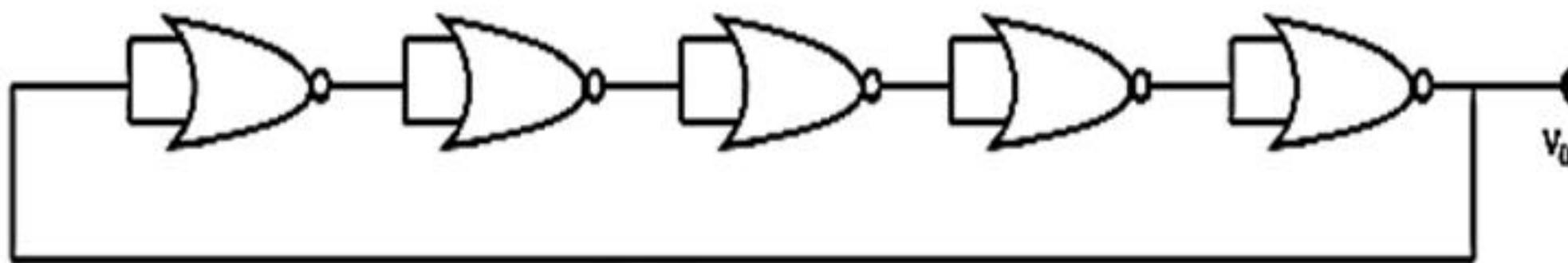
(b)  $x = (\bar{A} + B)C + \bar{B}\bar{D} + CE + \bar{E}$

(c)  $x = (\bar{A} + B)C + \bar{B}\bar{D} + CE + \bar{E}$

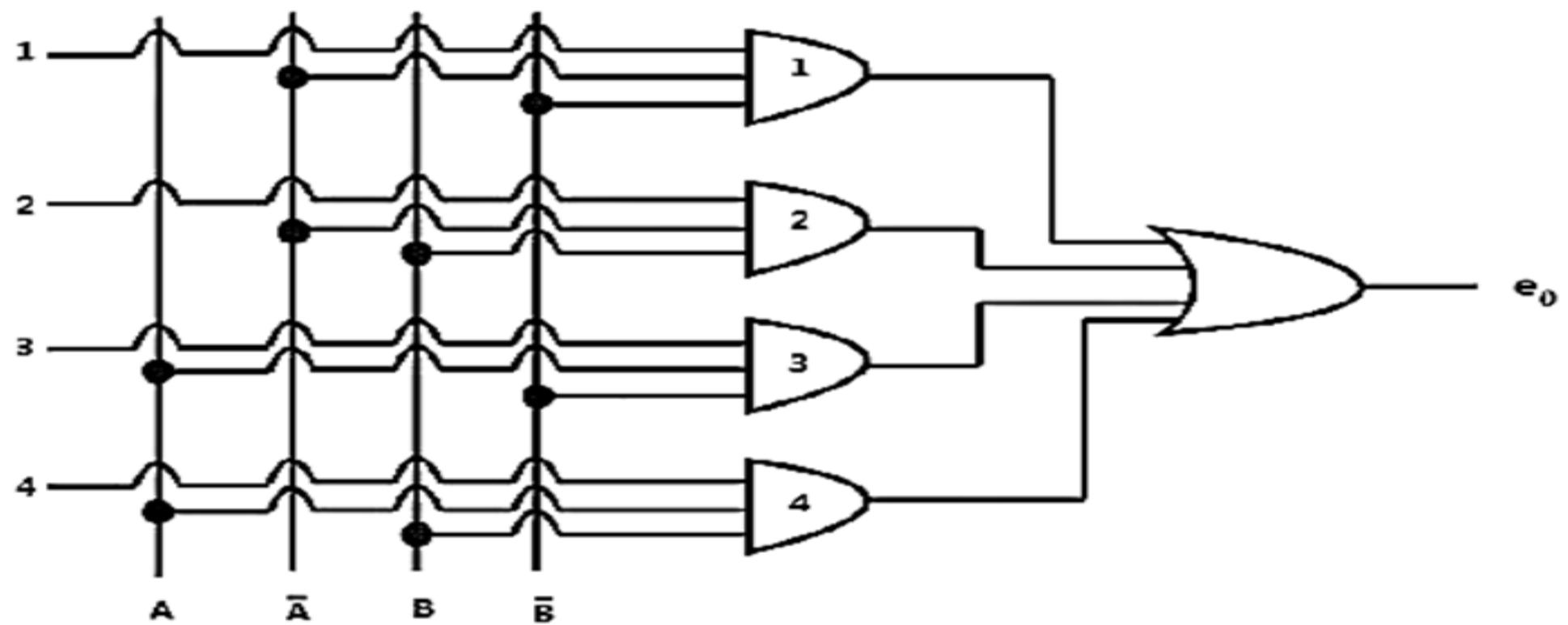
(d) None of these

Minimum number of two input gates (excluding XNOR) needed to realize one two input Ex-OR gate are \_\_

The average propagation delay of each NOR gate shown below is 10ns. The frequency or the output signal  $V_o$  is \_\_\_\_\_ MHz.

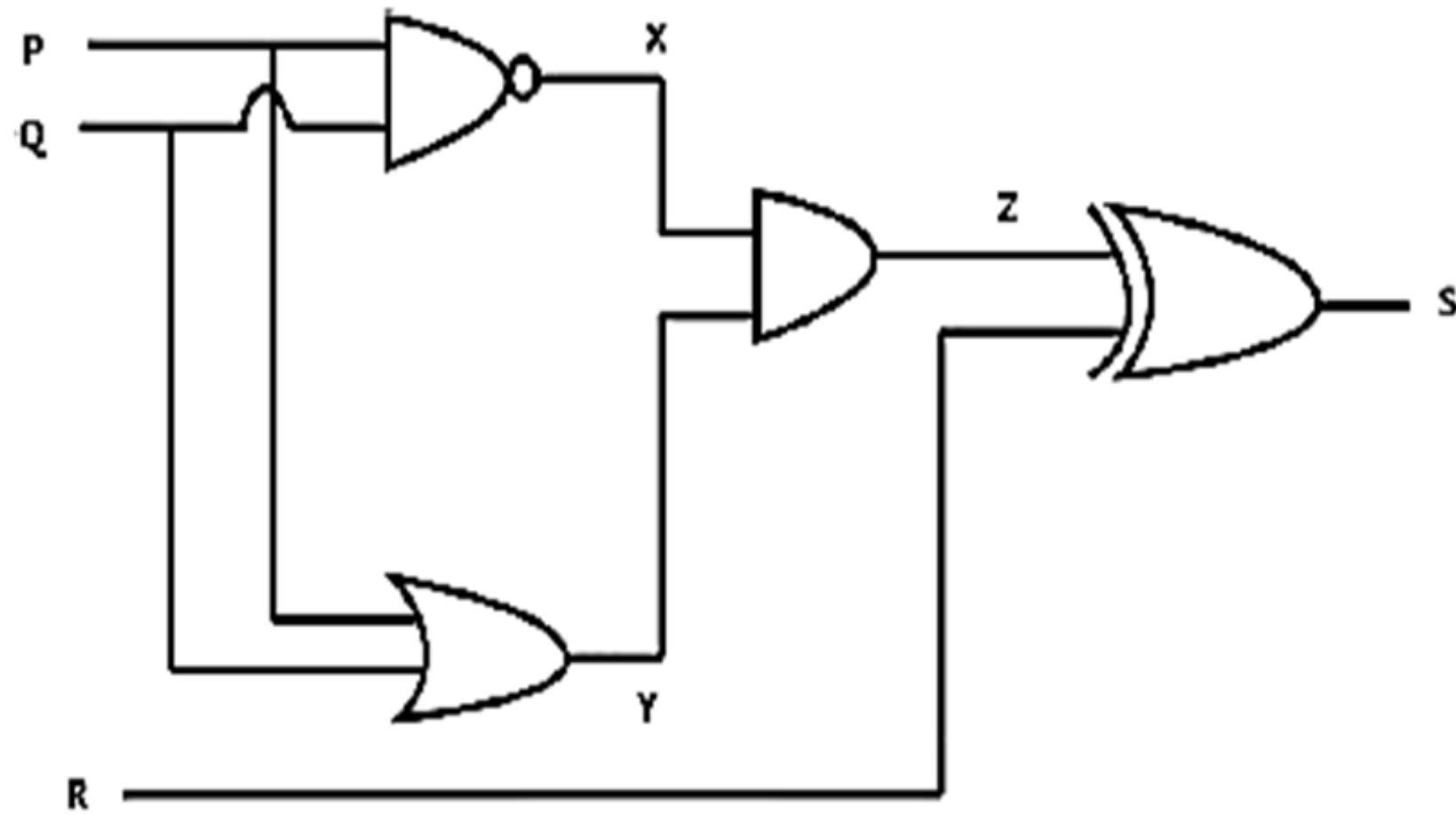


If input 2 and 3 are required to be enabled one by one then value of A and B are given by



- (a) AB = 00,  $\bar{AB} = 10$
- (b) AB = 01,  $\bar{AB} = 11$
- (c) AB = 01,  $\bar{AB} = 10$
- (d) AB = 00,  $\bar{AB} = 11$

Which of the following Boolean expression correctly represents the relation between P, Q, R and S



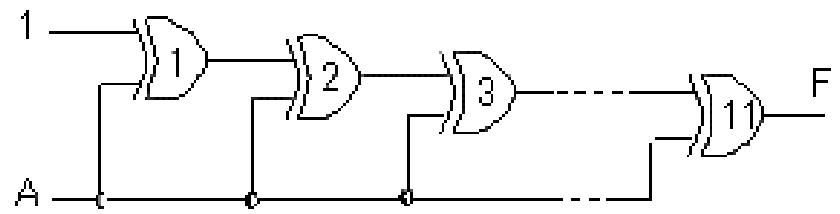
- (a)  $S = (P \text{ OR } Q) \text{ XOR } R$
- (c)  $S = (P \text{ NOR } Q) \text{ XOR } R$

- (b)  $S = (P \text{ AND } Q) \text{ XOR } R$
- (d)  $S = (P \text{ XOR } Q) \text{ XOR } R$

The minimum number of NAND gates required to implement the Boolean function,

$$Y = (\bar{B} + C)(\bar{A} + \bar{D}) \text{ are } \underline{\quad}$$

Determine the output of the following logic circuit.



(A) 1

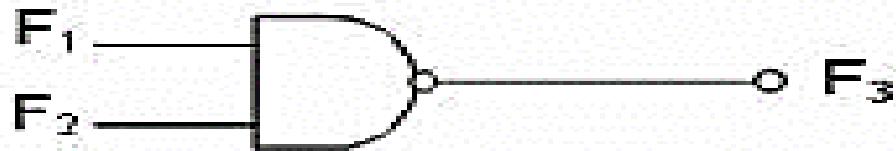
(B) 0

(C) A

(D)  $\bar{A}$

Minimum number of 2 input NAND gates required to implement a 2 input NOR gate is \_\_\_\_\_.

If  $F_1 = a \oplus b$  and  $F_2 = a + b$ , then the output of following logic gate is



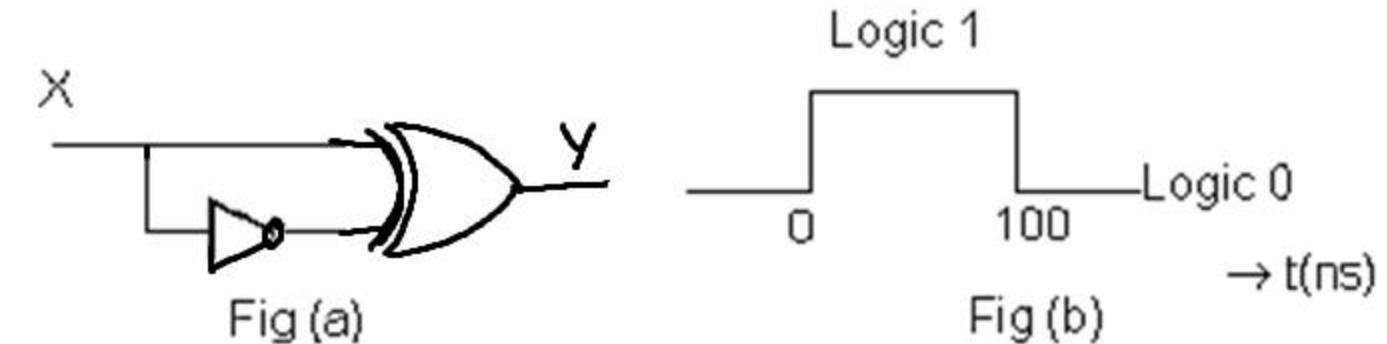
(A)  $ab$

(B)  $\bar{a} + b$

(C)  $a\bar{b}$

(D)  $a \oplus b$

Both the logic gates in the circuit(Fig(a)) below have propagation delay of 25 ns. If the waveform applied at input X is as shown in Fig(b), then output Y = 0 for total duration of \_\_\_\_\_ (in ns)



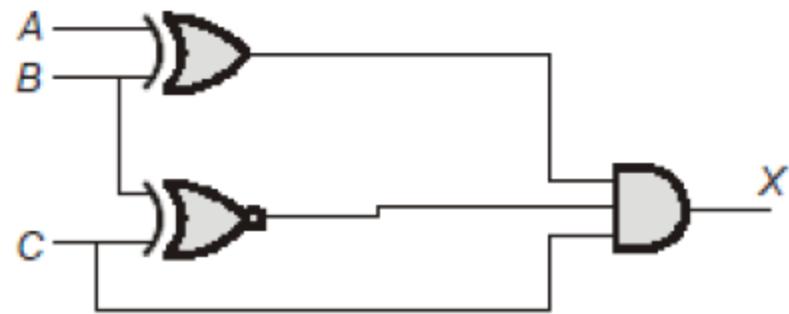
The truth table of a combinational circuit is given below

A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

The Boolean expression for Z is

- (a)  $(AB\bar{C}) + (\bar{A}\bar{B}\bar{C})$
- (b)  $(\bar{A} + \bar{B} + \bar{C}) + (A + B + C)$
- (c)  $\bar{C} + (A \oplus B)$
- (d)  $\bar{C} + (A \odot B)$

Find the correct input condition (ABC) which produce  $X = 1$  in the logic circuit shown below.



- a. 101
- b. 011
- c. 111
- d. 110

Which of the following examples expresses associative law of addition

- a.  $A + (B + C) = (A + B) + C$
- b.  $A + (B + C) = A + (BC)$
- c.  $A(BC) = (AB) + C$
- d.  $ABC = A + B + C$

If  $x$  and  $y$  are Boolean variables, then the minimized expression of  $x \oplus y \oplus xy$  will be

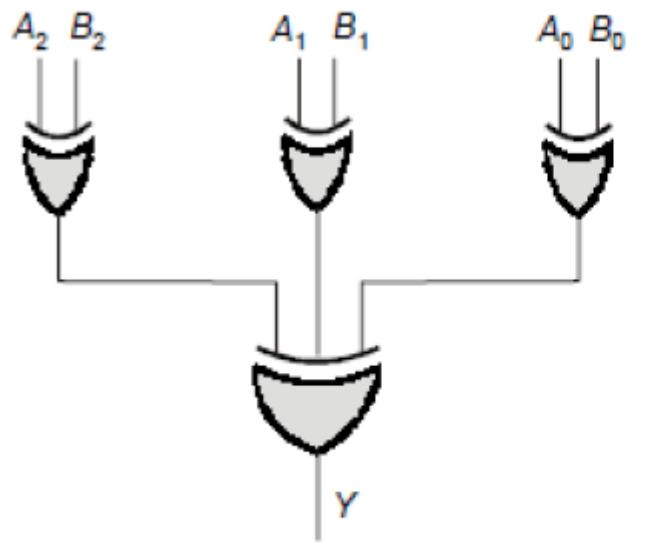
a.  $x + \bar{y}$

b.  $x + y$

c. 0

d. 1

The digital circuit shown below has two 3-bit inputs  $A_2 A_1 A_0$  and  $B_2 B_1 B_0$ .

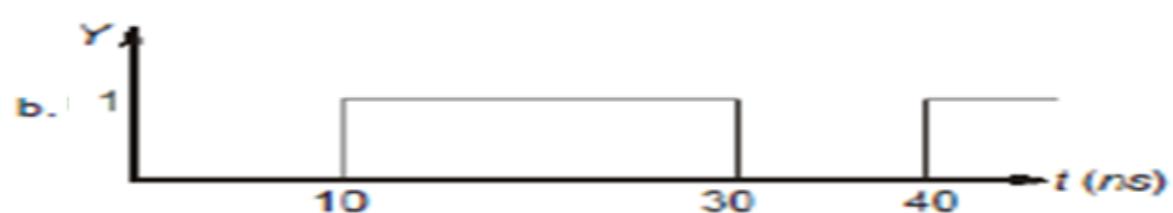
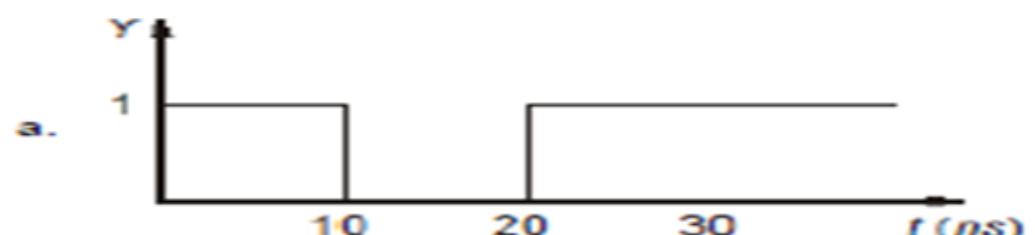


To obtain output  $Y = 1$ , the number of possible cases is \_\_\_\_\_.

Consider the circuit shown in figure below



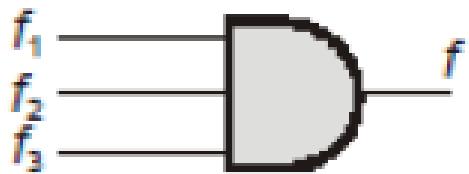
If propagation delay of NOT gate is 10 nsec, AND gate is 20 nsec and X-OR gate is 10 nsec. If A is connected to V<sub>CC</sub> at  $t = 0$ , then waveform for output Y is



Consider the logical functions given below.

$$f_1(A, B, C) = \Sigma(2, 3, 4)$$

$$f_2(A, B, C) = \pi(0, 1, 3, 6, 7)$$



If  $f$  is logic zero, then maximum number of possible minterms in function  $f_3$  are

\_\_\_\_\_.

Five soldiers **A, B, C, D** and **E** volunteer to perform an important military task if their following conditions are satisfied

- (i) either **A** or **B** or both must go
- (ii) either **C** or **E** but both must not go
- (iii) either both **A** and **C** go or neither goes
- (iv) If '**D**' goes, then '**E**' must also go
- (v) If '**B**' goes, then **A** and **C** must also go

The minimal combination of soldiers who can get the arrangement will be

Ans : ***AC $\bar{D}$  $\bar{E}$***

The minimum number of 2-input NAND gates required to implement the boolean function,

$$Y = (B + C)(\bar{A} + \bar{D}) \text{ are } \underline{\quad}.$$

The simplified form of the following Boolean expression is

$$f = (\overline{A} + B)(\overline{A} + B + D)\overline{D}$$

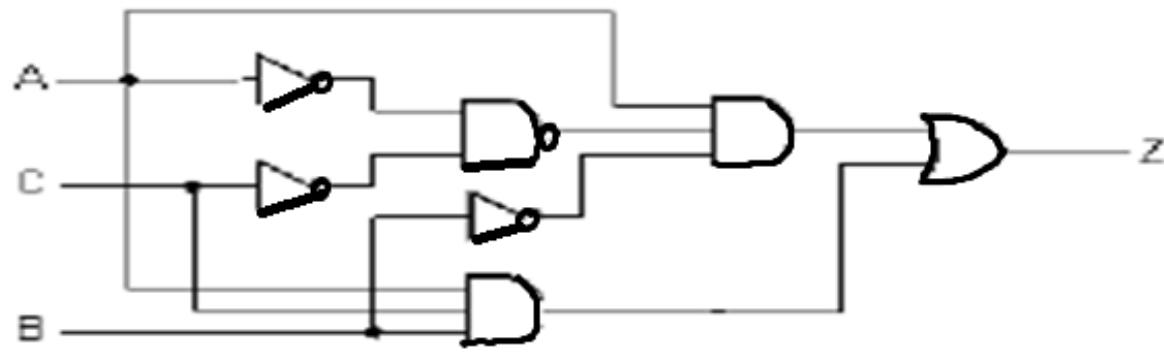
(A)  $f = \overline{A}\overline{D} + B\overline{D}$

(B)  $f = \overline{A} + B\overline{D}$

(C)  $f = B\overline{D}$

(D)  $f = \overline{A}\overline{D} + B$

Consider the logic circuit given below. The simplified version of this logic circuit is



- (A)
- (B)
- (C)
- (D)

Consider a logic circuit with three inputs A, B, C and an output Z that goes LOW only when A is HIGH while B and C are different. The simplified Boolean expression for Z in terms of inputs is

(A)  $A(B \oplus C)$

(B)  $A + (B \oplus C)$

(C)  $\bar{A} + (\overline{B \oplus C})$

(D)  $\bar{A} + (B \oplus C)$

Which of the following is NOT true ?

- (A)  $A + BC = (A+B)(A+C)$
- (B)  ~~$\overline{xy} + \overline{yz} + \overline{wxz} = \overline{xy} + \overline{yz}$~~
- (C)  $AB + \overline{A}C = (A+C)(\overline{A} + B)$
- (D)  $(A \uparrow B) \uparrow C = A \uparrow (B \uparrow C)$ ; " $\uparrow$ " represents NAND operation

Let  $X$  be the output of six input XOR gate. Then the number of minterms present in the Boolean expression for  $X$  is \_\_\_\_.

Consider the following Boolean function,

$$F(A, B, C) = (A + C + B)(A + \bar{B})(\bar{A} + B + \bar{C})$$

The canonical SOP (sum-of-product) expression for F is

- (A)  $F = m_0 + m_2 + m_3 + m_5$
- (B)  $F = m_0 + m_1 + m_3 + m_6$
- (C)  $F = m_1 + m_4 + m_6 + m_7$
- (D)  $F = m_2 + m_4 + m_5 + m_7$

The simplified expression of the Boolean function

$$F = \overline{AB}(\overline{CD} + \overline{EF})(\overline{AB} + \overline{CD})$$

(A)  $AB + (\overline{C} + \overline{D})(\overline{E} + \overline{F})$

(B)  $AB + (C + D)(E + F)$

(C)  $\overline{AB} + (\overline{C} + \overline{D})(E + F)$

(D)  $AB + (\overline{C} + \overline{D})(E + \overline{F})$

**Answer : D**

If  $xy = 0$ , then  $x \oplus y$  is equal to

(A)  $\bar{x} + \bar{y}$

(B)  $x+y$

(C)  $xy$

(D)  $\bar{x}\bar{y}$

The inputs to a 3-bit digital comparator are  $P = p_2p_1p_0$  and  $q = q_2q_1q_3$  and  $x_2 : p_2 \oplus q_2$ ,  $x_1 = p_1 \oplus q_1$ ,  $x_0 = p_0 \oplus q_0$ . The condition For  $P = Q$  is

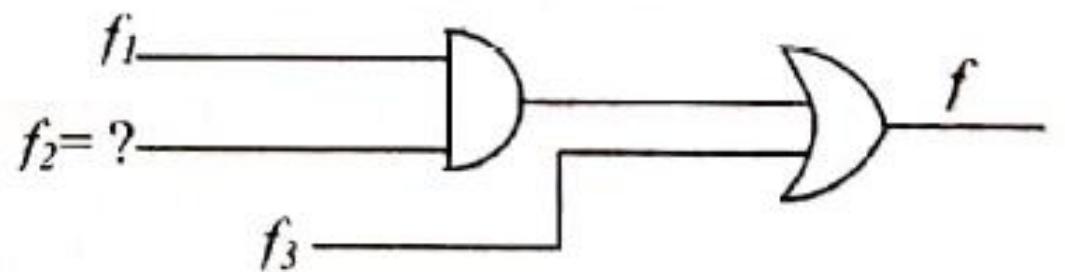
- (a)  $x_2x_1 + x_1x_0 + x_2x_0 = 1$
- (b)  $x_2 \cdot x_1 \cdot x_0 = 1$
- (c)  $x_2 + x_1 + x_0 = 1$
- (d)  $x_2x_1 + x_1x_0 + x_2x_0 = 1$

Given  $f_1$ ,  $f_3$ , and  $f$  in canonical sum of products form (in decimal) for the circuit.

$$f_1 = \sum m(4, 5, 6, 7, 8)$$

$$f_3 = \sum m(1, 15)$$

$$f = \sum m(1, 6, 8, 15) \quad \text{Then } f_2 \text{ is}$$



- (a)  $\sum m(4, 6)$
- (b)  $\sum m(4, 8)$
- (c)  $\sum m(6, 8)$
- (d)  $\sum m(4, 6, 8)$

Let,  $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$  where  $x_1, x_2, x_3, x_4$  are Boolean variables, and  $\oplus$  is the XOR operator. Which one of the following must always be TRUE?

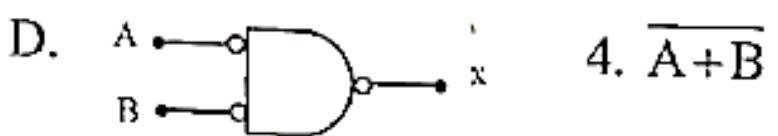
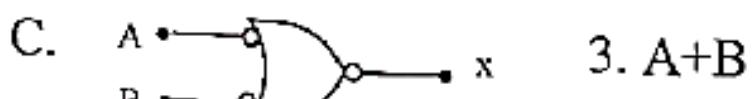
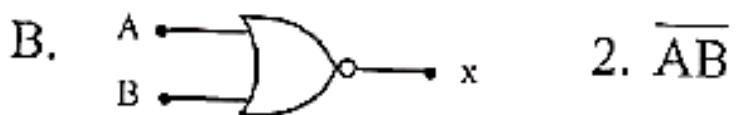
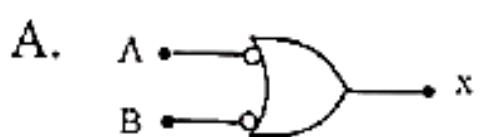
- (a)  $x_1 x_2 x_3 x_4 = 0$
- (b)  $x_1 x_3 + x_2 = 0$
- (c)  $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$
- (d)  $x_1 + x_2 + x_3 + x_4 = 0$

A 3 input majority gate is defined by the logic function  $M(a,b,c) = ab + bc + ca$ . Which one of the following gates is represented by the function  $M(\overline{M(a,b,c)}, M(a,b,\bar{c}), c)$ ?

- (a) 3-Input NAND gate
- (b) 3-Input OR gate
- (c) 3-Input NOR gate
- (d) 3-Input XNOR gate

Match List-I with List-II and select the correct answer using the codes given below the lists:

**List-I**



**List - II**

1. AB

2.  $\overline{AB}$

3. A+B

4.  $\overline{A+B}$

*Codes:*

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
(a)	3	1	4	2
(b)	2	1	4	3
(c)	3	4	1	3
(d)	2	4	1	3

Match List-I with List-II and select the correct answer using the codes given below the lists:

**List-I**

A.  $\underline{A \oplus B} = 0$

B.  $\overline{A + B} = 0$

C.  $\overline{A} \cdot B = 0$

D.  $A \oplus \overline{B} = 1$

**List-II**

1.  $A \neq B$

2.  $A = B$

3.  $A = 1 \text{ OR } B = 1$

4.  $A = 1 \text{ OR } B = 0$

*Codes:*

	A	B	C	D
(a)	3	2	1	4
(b)	2	3	4	1
(c)	3	2	4	1
(d)	2	3	1	4

Match List-I (Boolean Logic Function) with List-II (Inverse of Function) and select the correct answer using the code given below the lists:

**List-I**

A.  $ab + bc + ca + abc$

B.  $ab + \bar{a}\bar{b} + c$

C.  $a + bc$

D.  $(\bar{a} + \bar{b} + \bar{c})(a + \bar{b} + \bar{c})(\bar{a} + \bar{b} + c)$

**List-II**

1.  $\bar{a}(\bar{b} + \bar{c})$

2.  $\bar{a}\bar{b} + \bar{b}\bar{c} + \bar{c}\bar{a}$

3.  $(a \oplus b)c$

4.  $abc + \bar{a}bc + ab\bar{c}$

*Codes:*

<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
----------	----------	----------	----------

(a) 3 2 1 4

(b) 2 3 1 4

(c) 3 2 4 1

(d) 2 3 4 1

Match List – I with List – II and select the correct answer using the code given below the lists :

**List – I**

- A. AND gate
- B. OR gate
- C. NOT gate

**List – II**

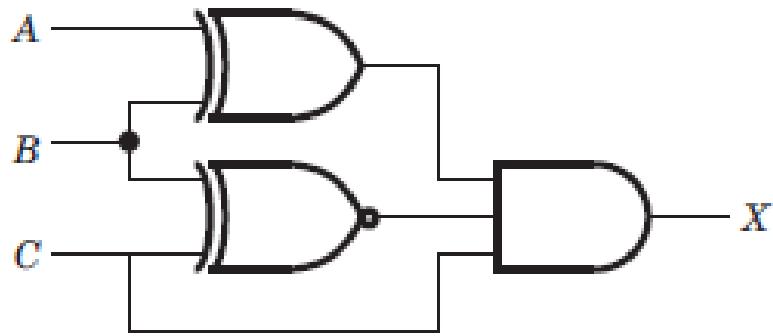
- 1. Boolean complementation
- 2. Boolean addition
- 3. Boolean multiplication

*Codes:*

A   B   C

- (a) 3    1    2
- (b) 1    2    3
- (c) 3    2    1
- (d) 1    3    2

In fig. the input condition, needed to produce  $X = 1$ , is



- (A)  $A = 1, B = 1, C = 0$
- (B)  $A = 1, B = 1, C = 1$
- (C)  $A = 0, B = 1, C = 1$
- (D)  $A = 1, B = 0, C = 0$

If the  $X$  and  $Y$  logic inputs are available and their complements  $\overline{X}$  and  $\overline{Y}$  are not available, the minimum number of two-input NAND required to implement  $X \oplus Y$  is

- (A) 4
- (B) 5
- (C) 6
- (D) 7

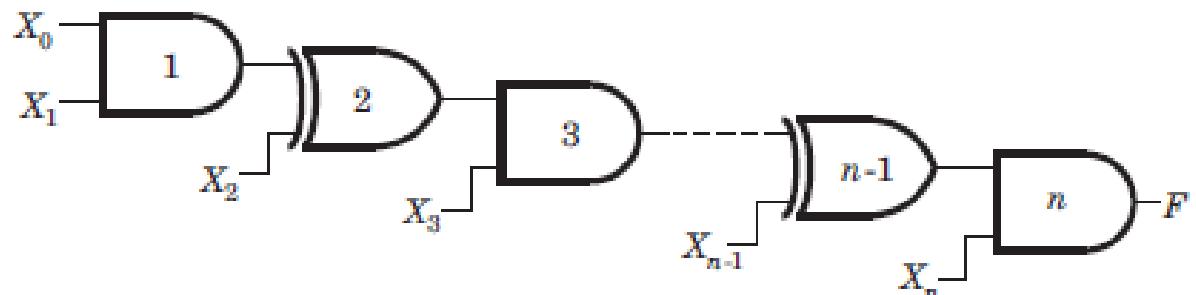
A Boolean function  $Z = A\bar{B}C$  is to be implemented using NAND and NOR gate. Each gate has unit cost. Only  $A$ ,  $B$  and  $C$  are available.

If both gate are available then minimum cost is



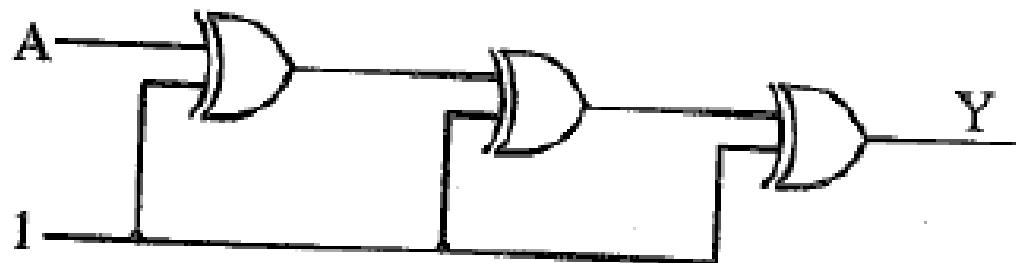
If NAND gate are available then minimum cost is

In the network of fig. f can be written as



- (A)  $X_0X_1X_3X_5 + X_2X_4X_5 \dots X_{n-1} + \dots X_{n-1}X_n$
- (B)  $X_0X_1X_3X_5 + X_2X_3X_4 \dots X_n + \dots X_{n-1}X_n$
- (C)  $X_0X_1X_3X_5 \dots X_n + X_2X_3X_5 \dots X_n + \dots + X_{n-1}X_n$
- (D)  $X_0X_1X_3X_5 \dots X_{n-1} + X_2X_3X_5 \dots X_n + \dots + X_{n-1}X_{n-2} + X_n$

The initial output of the following circuit is 1. If we apply 010101 at input A (first bit is zero), then what is the bit pattern generated at the output Y.



- (a) 010101
- (b) 101010
- (c) remains at 0
- (d) remains at '1'

The complement of the function

$$F = (A + \bar{B})(\bar{C} + D)(\bar{B} + C) \text{ is } \underline{\hspace{2cm}}$$

- (a)  $\bar{A}B + C\bar{D} + B\bar{C}$
- (b)  $A\bar{B} + \bar{C}D + \bar{B}C$
- (c)  $A\bar{B} + C\bar{D} + BC$
- (d)  $AB + BC + CD$

If  $F(A, B, C) = AB + AC + BC$ , then

$$F(\bar{A}, \bar{B}, C) \cdot F(\bar{A}, B, \bar{C}) \cdot F(A, \bar{B}, \bar{C}) = ?$$

- (a)  $\bar{A} \bar{B} \bar{C}$
- (b)  $\bar{A} \oplus \bar{B} \oplus \bar{C}$
- (c)  $\bar{A} \oplus \bar{B} \odot \bar{C}$
- (d)  $\bar{A} + \bar{B} + \bar{C}$

A circuit which is working as NAND gate with positive level logic system will work as ---- gate with negative level logic system.

- (a) NAND
- (b) NOR
- (c) AND
- (d) OR

The minimum number of two input NOR gates required to implement the simplified value of the following equation

$$f(w, x, y, z) = \sum m(0, 1, 2, 3, \overline{8, 9, 10}, 11)$$

- (a) One
- (b) Two
- (c) Three
- (d) Four

Let  $f(A, B) = A + B$ , simplified expression  
for function  $f(f(x + y, y), z)$  is

- (a)  $x + y + z$
- (b)  $xyz$
- (c)  $xy + z$
- (d) 1

The sum of all the minterms of a given Boolean function is equal to -----

- (a) zero
- (b) one
- (c) Two
- (d) Complement of the function

The product of all the maxterms of a given Boolean function is always equal to-----

- (a) Two
- (b) Complement of the function
- (c) One
- (d) Zero

To implement the simplified value of the following Boolean function, minimum of how many AND, NOT and OR gates are required?

$$f(A,B,C,D) = \overline{A} + A\overline{C} + \overline{A}\overline{B}C + AB\overline{C}D + ABCD$$

- (a) One 3-input OR gate , One 2-input AND and two NOT gates
- (b) One 3-input OR gate, Two 2-input AND and two NOT gates
- (c) Two 3-input OR gate, One 2-input AND and one NOT gates
- (d) One 3-input OR gate, One 2-input AND and one NOT gates

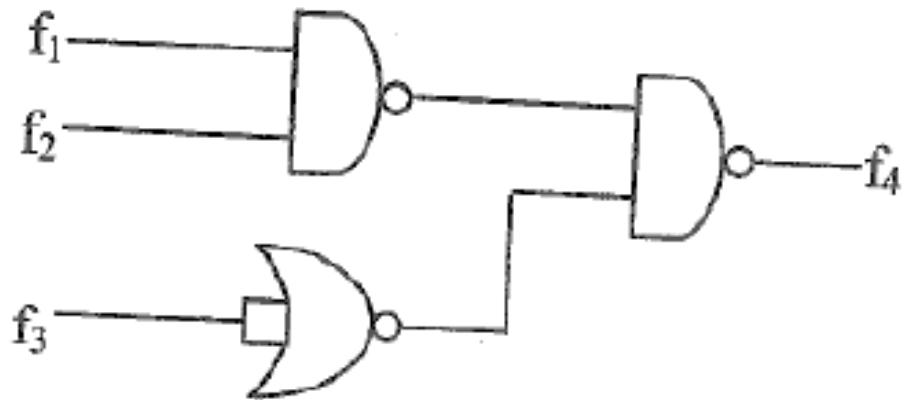
How many Boolean functions of the type  $f(x, y, z) = f(\bar{x}, \bar{y}, \bar{z})$  are available with three variables?

The logic expression  $Y = \Sigma m (0, 3, 6, 7, 10, 12, 15)$  is equivalent to

- (a)  $Y = \prod M (0, 3, 6, 7, 10, 12, 15)$
- (b)  $Y = \prod M (1, 2, 4, 5, 8, 9, 11, 13, 14)$
- (c)  $Y = \Sigma m (1, 2, 4, 5, 8, 9, 11, 13, 14)$
- (d)  $Y = \Sigma m (3, 0, 10, 12)$

**Pick up correct statements from the following:**

Consider the logic circuit shown in figure.



The functions  $f_1$ ,  $f_2$  and  $f_4$  are

$$f_1(w, x, y, z) = \sum m(8, 9, 10)$$

$$f_2(w, x, y, z) = \sum m(7, 8, 12, 13, 14, 15)$$

$$f_4(w, x, y, z) = \sum m(8, 9)$$

Then  $f_3(w, x, y, z)$  is

- |                       |                         |
|-----------------------|-------------------------|
| (a) $\sum m(9, 10)$   | (b) $\sum m(9)$         |
| (c) $\sum m(1, 8, 9)$ | (d) $\sum m(8, 10, 15)$ |

How many minimum number of NAND gates are required to implement the following Boolean equation, by taking inputs as A, B, C, D, E, F

$$F = \overline{A}C + \overline{D}F + \overline{B}C + \overline{E}F$$

- (a) 4
- (b) 5
- (c) 6
- (d) 7

Which of the following statements are correct?

1. The Dual of  $i^{\text{th}}$  minterms is maxterm  $(2^n - i - 1)$ .
  2. Sum of all minterms is always 0.
  3. Minterms and its corresponding Maxterms form a complement pair.
  4. Minterms are standard product terms.
- |             |             |
|-------------|-------------|
| (a) 1, 3, 4 | (b) 3, 4    |
| (c) 2, 3, 4 | (d) 1, 2, 4 |

Match List I with List II and select the correct answer using the codes given below the lists:

**List - I**                   **List - II**

- |                    |                         |
|--------------------|-------------------------|
| A. Boolean Algebra | 1. Minimization         |
| B. K-Map           | 2. Synchronous circuits |
| C. Clock           | 3. Error correction     |
| D. Parity          | 4. DeMorgan's theorem   |

**Codes:**

	<b>A</b>	<b>B</b>	<b>C</b>	<b>D</b>
(a)	4	1	2	3
(b)	4	3	2	1
(c)	3	4	2	1
(d)	4	2	1	3

# NUMBER SYSTEMS

Any number is associated with **Base** (or) **Radix** .

$(734)_{10}$

↓  
Base (or) Radix

$$(734)_{10} = 7(10^2) + 3(10^1) + 4(10^0)$$

$$(472.15) = 4(10^2) + 7(10^1) + 2(10^0) + 1(10^{-1}) + 5(10^{-2})$$

A number system with base ‘ b ’ , will have b different digits and they are from 0 to b -1 .

$(421)_4$  

$(243)_5$  

$(851)_9$  

➤ Base (b) is always a positive integer .

➤ In general  $b \geq 0$

<b>Base</b>	<b>Different digits</b>
2 ( Binary )	0 , 1
8( Octal )	0,1,2,3,4,5,6,7
10 ( Decimal )	0,1,2,3,4,5,6,7 ,8,9
16 (Hexadecimal)	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F

# Conversion of Number System

1. Decimal to Any Base

$$[N]_{10} \rightarrow [? ]_b$$

2. Any base to Decimal

$$[N]_b \rightarrow [? ]_{10}$$

3. one base to another base

$$[N]_{b_1} \rightarrow [? ]_{b_2}$$

4. Required base = ( Given Base )<sup>integer</sup>

# 1. Decimal to Other Base

- Integer part repeated division by the required base .
- Fractional part repeated multiplication by the required base .
- It is possible to obtain the equivalent of integer but may not possible for fractional part .

$$Q) (53.75)_{10} = (\underline{\hspace{2cm}} \underline{\hspace{2cm}})_2$$

$$(0.75)_{10} = (0.11)_2$$

$$\begin{array}{r} 53 \\ \hline 2 | 26 - 1 \\ \hline 2 | 13 - 0 \\ \hline 2 | 6 - 1 \\ \hline 2 | 3 - 0 \\ \hline 1 - 1 \end{array}$$

$$(53)_{10} = (110101)_2$$

$$\begin{array}{r} 0.75 \\ \times 2 \\ \hline 0.50 \\ - 0.50 \\ \hline 0.00 \end{array}$$

0.50

2

0.00

$$Q) (0.15)_{10} = (\underline{\underline{0.001001}})_2$$

$$\begin{array}{r} 0.15 \\ \times 2 \\ \hline 0.30 \\ \times 2 \\ \hline 0.60 \\ \times 2 \\ \hline 1.20 \end{array}$$

$$\begin{array}{r} 0.001001 \\ \hline 0.20 \\ \times 2 \\ \hline 0.40 \\ \times 2 \\ \hline 0.80 \\ \times 2 \\ \hline 1.60 \end{array}$$

$$0.60$$

$$Q) (53.75)_{10} = \underline{\hspace{2cm}}_4$$

$\begin{array}{r} 53 \\ \times 4 \\ \hline 13 - 1 \\ \hline 3 - 1 \end{array}$	$\begin{array}{r} 0.75 \\ \times 4 \\ \hline 3.00 \end{array}$
--	--

$(311.3)_4$

$$Q) (39.5)_{10} = (\underline{\hspace{1cm} \hspace{1cm} \hspace{1cm}})_8$$

$$\begin{array}{r} 39 \\ 8 \longdiv{39} \\ \underline{-4} \quad 7 \end{array}$$

$$\begin{array}{r} 0.5 \\ \times 8 \\ \hline \textcircled{4} \cdot 0 \end{array}$$

$$(47.4)_8$$

$$Q) (39.5)_{10} = \underline{\hspace{2cm}}_{16}$$

$$\begin{array}{r} 16 \longdiv{39.} \\ \underline{-2\phantom{9}.} \\ 19 \\ \underline{\times 16} \\ 8.0 \end{array}$$

$$(27.8)_{16}.$$

## 2. Any base to Decimal

$$(x_2x_1x_0 \ . \ x_{-1}x_{-2}x_{-3})_b = (?)_{10}$$

Simply expand the polynomial and do addition in base 10 form

$$x_2(b^2) + x_1(b^1) + x_0(b^0) + x_{-1}(b^{-1}) + x_{-2}(b^{-2}) + x_{-3}(b^{-3})$$

$$Q) \ (311.30)_4 = \underline{\hspace{1cm}} \ (----)_{10}$$

$$= 3(4^2) + 1(4^1) + 1(4^0) + 3(\bar{4}^1) + 0(\bar{4}^2)$$

$$= (53.75)_{10}$$

Q) Find the minimum decimal equivalent of  $(3AB26)_x$

Sol:

$$= 3(x^4) + \underline{A}(x^3) + \underline{B}(x^2) + 2(x^1) + 6(x^0) \rightarrow \underline{\text{min}}$$

$$= 3(12^4) + 10(12^3) + 11(12^2) + 2(12) + 6.$$

$$= 8102$$

$$\left. \begin{array}{l} x > 11 \\ \hline x_{\min} = 12 \end{array} \right|$$

$$Q) (137.4)_8 = \underline{\hspace{2cm}}_{10}$$

$$= 1(8^2) + 3(8) + 7 + 4(8^{-1})$$

$$= (95.5)_{10}.$$

$$Q) \quad (DAD)_{16} = \quad (- - - -)_{10}$$

$$(DAD)_{16} = D(16^2) + A(16^1) + D(1).$$

$$= (3501)_{10}.$$

$$Q) (ECE)_{16} = (- - - -)_{10}$$

$$(ECE)_{16} = 14(16^2) + 12(16) + 14$$

$$= \underline{\underline{3790}}_{10}.$$

$$Q) (EEE)_{16} = \underline{\hspace{2cm}} (----)_{10}$$

$$(EEE)_{16} = 14(16^2) + 14(16) + 14$$

$$= 3822$$

Q) Find b if  $(\sqrt{41})_b = (5)_{10}$

$$(41)_b = (25)_{10}$$

$$4b + 1 = 2(10) + 5$$

$$\boxed{b = 6}$$

### 3. One base to another base

$$[N]_{b_1} \rightarrow [?]_{b_2}$$

1. Convert the given number to the decimal system
2. After that convert to required base

Q) Find the value of x if  $(193)_x = (623)_8$

$$\underline{(193)_x} = (\quad)_{10}$$

$$(623)_8 = (\quad)_{10}$$

$$x^2 + 9x + 3 = 6(8^2) + 2(8) + 3$$

$$x^2 + 9x - 400 = 0 \quad \boxed{x = 16} \quad \checkmark$$

$$(x+25)(x-16) = 0 \quad x = -25 \quad \times$$

Q) Find  $b_1$  and  $b_2$  if  $(235)_{b_1} = (565)_{10} = (1065)_{b_2}$

$$(235)_{b_1} = (565)_{10}$$

$$2(b_1^2) + 3(b_1) + 5 = 565$$

$$2b_1^2 + 3b_1 - 560 = 0$$

$$b_1 = 16$$

$$(1065)_{b_2} = (565)_{10}$$

$$1(b_2^3) + 0(b_2^2) + 6b_2 + 5 = 565$$

$$b_2^3 + 6b_2 - 560 = 0$$

$$b_2 = 8$$

Q) The solution to the quadratic equation  $x^2 - 11x + 22 = 0$  is  $x=3$  and  $x=6$ , what is the base of the system

$$x^2 - 11x + 22 = (x - 3)(x - 6)$$

$$(3)_b = (3 \cdot)_{10}$$

$$(x^2 - 11x + 22)_b = (\underline{x^2 - 9x + 18})_{10}$$

$$3(b^0) = 3$$

$$(6)_b = (6 \cdot)_{10}$$

$$(-11)_b = (-9)_{10} \quad \textcircled{1}$$

$$b+1 = 9$$

$$(22)_b = (18)_{10} \quad \textcircled{2}$$

$$\boxed{b = 8}$$

4. Required base = (*Given Base*)<sup>*integer*</sup>

$$Q) (1011|010110.010110010)_2 = (-\underline{-} \underline{-} \underline{-})_8$$

$$\begin{array}{r} 1 | 3 \quad 2 | 6 \cdot 2 \quad 6 \quad 2 \\ \qquad \qquad \qquad 8 = 2^3 \end{array}$$

$$n=3$$

$$(1326 \cdot 262)_8$$

Q)  $(1011010110.010110010)_2 = (\underline{\hspace{1cm} \hspace{1cm} \hspace{1cm} \hspace{1cm}})_4$   
 $\underline{2} \quad \underline{3} \quad | \quad | \quad | \quad 2 \cdot | \quad | \quad | \quad 2 \quad | \quad 0 \quad -$   
 $n=2$ .

$$(23|12 \cdot 11240)_4.$$

Q)  $(10|1101|0110.0101|1001|0)_2 = (\underline{\hspace{1cm} \hspace{1cm} \hspace{1cm} \hspace{1cm}})_{16}$

$\begin{array}{c} 2 | & 13 | & 6 & \cdot & 5 | & 9 | & 0 \\ & D & & & & & \end{array}$

$n=4$

$$(206.590)_{16}$$

Q)  $(22|1012|10|12.20|11022)_3 = (\underline{\hspace{1cm}} \underline{\hspace{1cm}} \underline{\hspace{1cm}} \underline{\hspace{1cm}})_9$

$$(22)_3 = 2(3) + 2 = (8)_{10} = (8)_9$$

$$(10)_3 = 1(3) = (3)_{10} = (3)_9$$

$$(12)_3 = 1(3) + 2 = (5)_{10} = (5)_9$$

$$(10)_3 = (3)_9.$$

$$(12)_3 = (5)_9.$$

$$(20)_3 = 2(3) = (6)_{10} = (6)_9$$

$$(11)_3 = 3 + 1 = (4)_{10} = (4)_9$$

$$(02)_3 = (2)_{10} = (2)_9.$$

$$(20)_3 = (6)_{10} = (6)_9.$$

$$(83535 \cdot 6426)_9$$

Q) (32|10|33|21|01.22|10)<sub>4</sub> = (-----)<sub>16</sub>

n = 2

$$(32)_4 = 3(4) + 2 = (14)_{10} = (E)_{16}$$

$$(22)_4 = 2(4) + 2 = (10)_{10} = (A)_{16}$$

$$(10)_4 = 4 + 0 = (4)_{10} = (4)_{16}$$

$$(10)_4 = 4 = (4)_{10} = (4)_{16}$$

$$(33)_4 = 3(4) + 3 = (15)_{10} = (F)_{16}$$

$$(E\ A\ F\ 9\ 1\ .\ A\ 4)_{16}$$

$$(21)_4 = 2(4) + 1 = (9)_{10} = (9)_{16}$$

$$(01)_4 = 0 + 1 = (1)_{10} = (1)_{16}$$

Q) Find the number of solutions of 'Y' exists for  $(123)_5 = \underline{(X8)}_Y$

$$1(5^2) + 2(5) + 3(1) = x(y) + 8$$

$$y > x$$

$$y > 8$$

$$xy = 30$$

$$x=1,$$

$$y=30$$

$$x=2$$

$$y=15$$

$$x=3$$

$$y=10$$

$$x=5$$

$$y=6$$



$$x=30, y=1$$

$$x=15, y=2$$

$$x=10, y=3$$

$$x=6, y=5$$



Q) Find the number of solutions of 'X' exists for  $(123)_x = (12X)_3$

$$(123)_3^x.$$

$$\underline{(123)_x} = \underline{\underline{(12x)_3}}$$

No solution  
will exist

$$x > 3 \quad ①$$

$$\underline{x=3.1}$$



Q) Find the base of the following system such the given operation is valid

$$24+14=41$$

$$(24)_b + (14)_b = (41)_b.$$

$$2b+4 + b+4 = 4b+1$$

$$\boxed{b = 7.}$$

Q) Find the base of the following system such the given operation is valid

$$\underline{(66)}_b$$

$$\frac{66}{6} = 11$$

$$b > 6$$

$$b = \cancel{7}$$

$$\frac{(66)_b}{(6)_b} = (11)_b$$

$$b = \cancel{7}, 8, 9, 10, \dots$$

$$\frac{6b+6}{6} = b+1$$

$$b=1$$

$$\boxed{b+1 = b+1} \quad \checkmark \quad \checkmark$$

$$b=2$$

⋮

Q) Find the base of the following system such the given operation is valid

$$\underline{\sqrt{121} = 11}$$

$$\underline{(121)_b}$$

$$(121)_b = (121)_b \quad b = 3$$

$$1b^2 + 2b + 1 = 1b^2 + 2b + 1.$$

$$\underline{\underline{b=3}}$$

Q) Find the base of the following system such the given operation is valid

$$(\sqrt{41})_b = (5)_b$$

$$(\sqrt{4b+1})_{10} =$$

$$(5)_b = (5)_{10}$$

$$(\sqrt{4b+1})_{10} = (5)_{10}$$

$$4b+1 = 25$$

$$b = 6$$

# Complement Analysis

$[N]_r$

1. r's Complement

2. (r-1)'s Complement

**Binary (r=2)**

1's Complement

2's Complement

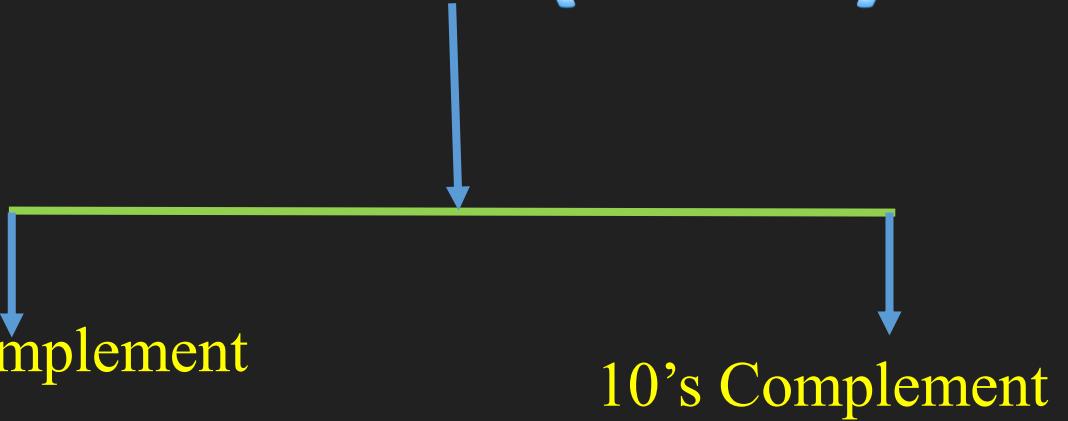
**Octal (r=8)**

7's Complement

8's Complement

**Decimal ( $r=10$ )**

**Hexadecimal ( $r=16$ )**



## r' s Complement

$r'$  s Complement of the number ( $N$ ) =  $r^n - N$

$r$  -----> Radix

$n$  -----> number of integer digits

$N$  -----> given number

## (r-1) ' s Complement

$(r-1) ' s \text{ Complement} \text{ of the number } (N) = r^n - r^{-m} - N$

r -----> Radix

n -----> number of integer digits

m -----> number of decimal digits

N -----> given number

$(r-1)^s$  Complement of the number ( $N$ )  $= r^n - r^{-m} - N$

$r^s$  Complement of the number ( $N$ )  $= (r-1)^s$  complement  $+ r^{-m}$

if  $m=0$

$r^s$  Complement of the number ( $N$ )  $= (r-1)^s$  complement  $+ 1$

Q) Find the 10's complement of  $(327.452)_{10}$

$$\begin{aligned} \text{9's complement} &= 10^n - 10^m - N \\ &= \underline{10^3 - 10^3} - 327.452 \\ &= \underline{1000 - 0.001} - 327.452 \\ &= 999.999 - 327.452 \\ &= 672.547 \end{aligned}$$

$$10\text{'s complement} = 10^n - N$$

$$= (10)^3 - 327.452$$

$$= 672.548$$

$$\left( \underline{3} \underline{2} \underline{7} \cdot \underline{4} \underline{5} \underline{2} \right)_{10}$$

q's complement = 999. 999 - 327. 452

999. 999.

327. 452

672. 547

$(327.452)_{10}$

999.9910

10's complement = 327.452.

672.548

$$(327 \cdot 452)_8$$

$$\begin{array}{rcl} 8\text{'s complement} & = & \begin{array}{r} 7 \cdot 7 \cdot 7 \cdot 7 \cdot 8 \\ 327 \cdot 452 \\ \hline 450 \cdot 326 \\ \hline \end{array} \\ & & \end{array}$$

$$\begin{array}{rcl} 7\text{'s complement} & = & \begin{array}{r} 450 \cdot 325 \\ \hline \end{array} \\ & & \end{array}$$

Q) Find the 9's complement of  $(327.452)_{10}$

$$9\text{'s complement} = 672.547$$

Q) Find the 10's complement of  $(784732179)_{10}$

10's complement = 215267821.

Q) Find the 2's complement of  $(101100)_2$

$$\begin{array}{rcl} \text{1's complement} & = & 010011 \\ & & \underline{+ 1} \\ & = & \underline{\underline{010100}} \end{array}$$

$$\begin{array}{rcl} \text{2's complement} & = & \underline{\underline{010100}} \\ & & \leftarrow 101100 \end{array}$$

$$2\text{'s complement} = \underline{\underline{010100}}$$

Q) Find the 2's complement and 1's complement of (0.0110)<sub>2</sub>

$$1\text{'s complement} = \gamma^n - \gamma^{-m} - n$$

$$\begin{array}{r} \text{1's complement} \\ \text{2's complement} \\ \hline 1.0000 \\ 0.0001 \\ \hline 0.1111 \end{array} = 2^0 - 2^{-4} - \underline{\underline{0.0110}}$$

$$= 1 - \underline{\underline{0.0001}} - 0.0110$$

$$= \underline{\underline{0.1111}} - 0.0110$$

$$= \underline{\underline{0.1001}}$$

$$\begin{array}{r} 0.1111 \\ 0.0110 \\ \hline \end{array}$$

0.0625

$\times 2$

0.1250

$\times 2$

0.2500

$\times 2$

0.5

$\times 2$

0.0001

1.

Q) Find the 9's and 10's complement of  $(52520)_{10}$

$$\begin{array}{r} \text{9's complement} = 47479 \\ \quad \quad \quad + 1 \\ \hline \end{array}$$

$$\begin{array}{r} \text{10's complement} = \underline{\quad \quad \quad 47480} \\ \quad \quad \quad - 1 \\ \hline \end{array}$$

$$\begin{array}{r} 999910 \\ 52520 \\ \hline \end{array}$$

$$\begin{array}{r} . \\ . \\ . \\ 47480 \\ \hline \end{array}$$

Q) Find the 9's and 10's complement of  $(0.3267)_{10}$

$$\begin{aligned} \text{9's Complement} &= 0.9999 - 0.3267 \\ &= 0.6732 \end{aligned}$$

$$\text{10's Complement} = 0.6733$$

Q) Find 1's and 2's complement of  $(10100100111)_2$

1's complement = 01011011000

2's complement = 01011011001

Q) Find 8's and 9's complement of  $(278421)_9$

$$\begin{aligned} \text{8's complement} &= 888888 - 278421 \\ &= 610467 \end{aligned}$$

$$\text{9's complement} = 610468$$

Q) Find F's and 16's complement of  $(792410)_{16}$

$$\begin{aligned} \text{F's complement} &= \text{FFFFEFF} - 792410 \\ &= 86DBEF \cdot \quad \underline{16-16=0} \\ &\quad + 1 \end{aligned}$$

$$\begin{aligned} \text{16's complement} &= \overline{86DBFO} \end{aligned}$$

Q) Find 1's and 2's complement of  $(11000100)_2$

1's complement = 00111011.

2's complement = 00111100

Q) Find 1's and 2's complement of  $(11010.11)_2$

$$1's \text{ Complement} = 00101.00$$

$$2's \text{ Complement} = 00101.01$$

Q) Find 8's complement of  $(2670)_8$

$$\begin{array}{rcl} \text{8's Complement} & = & 7778 - 2670 \\ & = & \underline{\quad 5110 \quad} \end{array}$$

Q) Find 10's complement of  $(7492)_{10}$

10's complement = 2608

Q) Find 16's complement of  $(9623)_{16}$

$$16\text{'s Complement} = \text{FFF } (16) - 9623$$

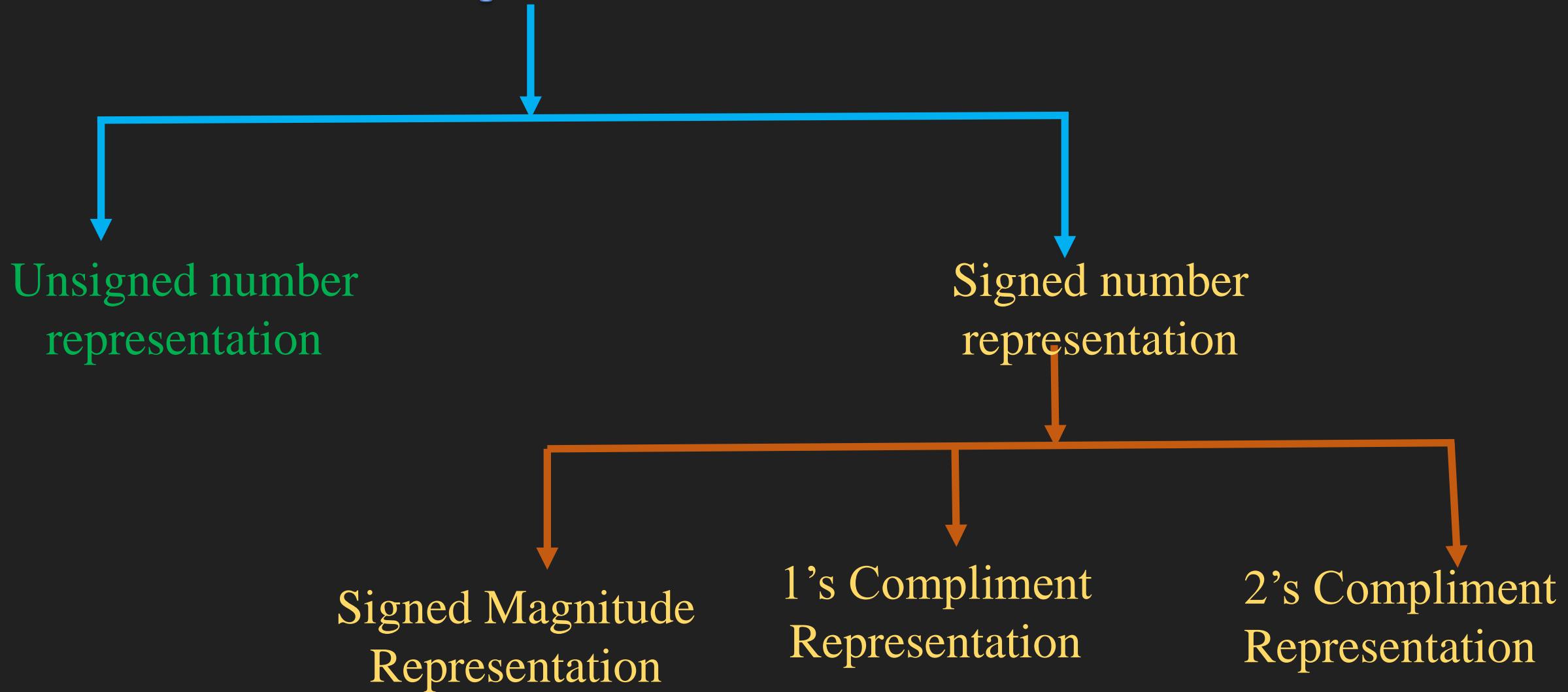
$$= \frac{69DD}{\text{---}}$$

$$= \frac{(16)^4}{10} - \underline{\underline{(9623)_{16}}} \quad \cdot$$

$$= \frac{(65536)_{10}}{10} - (9623)_{16}.$$

= .

# Data Representation



# Unsigned Number Representation

- Strictly applicable for positive numbers
- There is no sign bit concept

+ 5 -----> 101

- 5 -----> 

Decimal number	Unsigned number representation (4)
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

Range with 4 bits = 0 to 15

Range with n- bits = 0 to  $2^n - 1$

# Signed Number Representation

- 1.Signed magnitude representation
- 2.1' s compliment representation
- 3.2's compliment representation

# Signed Magnitude representation

- Valid for both positive and negative numbers .
- Sign bit concept is used .



Sign bit = 0 , for  $\oplus$ Ve number  
= 1, for  $\ominus$  ve number

$+5 =$ 

0	1	0	1
---	---	---	---

 $-5 =$ 

1	1	0	1
---	---	---	---

 $+5 =$ 

0	0	0	0	0	1	0	1.
---	---	---	---	---	---	---	----

 $-5 =$ 

1	0	0	0	0	1	0	1
---	---	---	---	---	---	---	---

Decimal number	Signed Magnitude Representation (4)
+0	0 000
+1	0 001
+2	0 010
+3	0 011
+4	0 100
+5	0 101
+6	0 110
+7	0 111
-0	1 000
-1	1 001
-2	1 010
-3	1 011
-4	1 100
-5	1 101
-6	1 110
-7	1 111

Range with 4 bits = -7 to +7

Range with 5 bits = -15 to +15

Range with n-bits =  $-(2^{n-1} - 1)$  to  $(2^{n-1} - 1)$



# 1's Compliment Representation

- In this  $\oplus$ Ve numbers are represented as normal binary number with MSB ‘0’

## Representation of $\ominus$ ve number

1. Write the binary equivalent of magnitude
2. Take its 1's compliment

$$+6 = \begin{array}{|c|c|c|c|} \hline 0 & | & | & 0 \\ \hline \end{array} \checkmark = + [ \begin{smallmatrix} 110 \end{smallmatrix} ] = +6$$

$$-6 = \begin{array}{|c|c|c|c|} \hline 1 & 0 & 0 & 1 \\ \hline \end{array} = - [ \begin{smallmatrix} 1's \text{ comp } (001) \end{smallmatrix} ].$$

$$- [ \begin{smallmatrix} 110 \end{smallmatrix} ] = -6.$$

$$+6 = \begin{array}{|c|c|c|c|c|c|c|c|} \hline 0 & 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ \hline \end{array} \quad +6 = 00000110$$

$$-6 = 11111001$$

$$-6 = \begin{array}{|c|c|c|c|c|c|c|c|} \hline 1 & 1 & 1 & 1 & 1 & 0 & 0 & 1 \\ \hline \end{array}$$

← →

Decimal number	1's Compliment Representation (4)
+0	0000 ✓
+1	0001
+2	0010 ✓
+3	0011 ✓
+4	0100 ✓
+5	0101 ✓
+6	0110 ✓
+7	0111
-0	1111
-1	1110
-2	1101
-3	1100
-4	1011
-5	1010
-6	1001
-7	1000

Range with 4 bits = -7 to +7

Range with 5- bits = -15 to +15

Range with n- bits =

$$-(2^{n-1} - 1) \text{ to } +(2^{n-1} - 1)$$

# 2's Compliment Representation

- In this  $\oplus$ Ve numbers are represented as normal binary number with MSB ‘0’

## Representation of $\ominus$ ve number

1. Write the binary equivalent of magnitude
2. Take its 2’s compliment

+6 =

$x_3$	$x_2$	$x_1$	$x_0$
0	1	1	0

- 6 =

$x_3$	$x_2$	$x_1$	$x_0$
1	0	1	0

+6 =

0	0	0	0	0	1	1	0
---	---	---	---	---	---	---	---

- 6 =

1	1	1	1	1	0	1	0
---	---	---	---	---	---	---	---

Decimal number	2's Compliment Representation (4)
+0	0 000
+1	0 001
+2	0 010
+3	0 011
+4	0 100
+5	0 101 ✓
+6	0 110
+7	0 111
-0	—
-1	1 111
-2	1 110
-3	1 101
-4	1 100
-5	1 011
-6	1 010
-7	1 001
-8	1 000 ✓

Range with 4 bits = (-8) to (+7).

Range with 5- bits = (-16) to +(15)

Range with n- bits =  $-(2^{n-1})$  to  $+(2^{n-1} - 1)$

Q) Find the Decimal equivalent of the unsigned numbers given below

a) 01101

b) 11101

a) 01101 = 13 .

b) 11101 = 29 .

Q) Find the Decimal equivalent of the Signed magnitude numbers given below

a) 01101

b) 11101

a) 01101 = + 13

b) 11101 = - [1101] = - 13

Q) Find the Decimal equivalent of the 1's Compliment numbers given below

a) 01101

b) 11101

a) 01101 = + [1101] = + 13 .

b) 11101 = - [1's complement of (1101)]

= - [0010]

= - 2 .

Q) Find the Decimal equivalent of the 2's Compliment numbers given below

a) 01101

b) 11101

$$a) \text{ 01101} = + [1101] = + 13 .$$

$$\begin{aligned} b) \text{ 11101} &= - \left[ \text{2's complement of } (1101) \right] \\ &= - [0011] \\ &= - 3 . \end{aligned}$$

Q) Find the 2's Compliment of the following

$$-2 = 11110$$

$$-4 = 111100$$

$$-8 = 1111000$$

$$-16 = 1110000$$

$$\underline{-2^n = 10000 \dots n-3 zeros.}$$

$$+2 = 10$$
$$\begin{array}{r} 2 = 10 \\ - 1 \\ \hline 10 \end{array}$$

$$+8 = 1000$$
$$\begin{array}{r} 2^3 = 1000 \\ - 1 \\ \hline 1000 \end{array}$$

$$+4 = 100$$
$$\begin{array}{r} 2^2 = 100 \\ - 1 \\ \hline 100 \end{array}$$

## NOTE :

The minimum number of bits required for  $-2^n$  , using 2's compliment representation = (n+1)

Q) 1's compliment of the numbers given below , find the decimal equivalents

a) 01001 = +9

b) 001001 = +9

c) 0001001 = +9

d) 11001 = - [ 1's comp (1001) ] = - [ 0110 ] = -6

e) 111001 = -6

f) 1111001 = -6

Q) 2's compliment of the numbers given below , find the decimal equivalents

a) 01001 = + 9

b) 001001 = + 9

c) 0001001 = + 9

d) 11001 = - [2's complement (1001)] = - [011] = - 7

e) 111001 = - 7

f) 1111001 = - 7

Q) A number in 4-bit 2's compliment is  $x_3x_2x_1x_0$ , this number when stored using 8-bits will be

- a) 0000  $x_3x_2x_1x_0$
- b) 1111  $x_3x_2x_1x_0$
- c)  $x_3x_3x_3x_3x_2x_1x_0$  ✓
- d)  $\overline{x_3}\ \overline{x_2}\ \overline{x_1}\ \overline{x_0}\ x_3x_2x_1x_0$

# Binary Subtraction using 1's compliment

1. Represent the given numbers in the 1's compliment form
2.  $Y = A - B = A + [-B] = A + (\text{1's Complement of } B)$
3. Add the two numbers
4. If carry is generated ,then the result is positive and in the true form , add carry to the LSB
5. If carry is not generated , then the result is negative , and in the 1's compliment form

Q) Perform the following operation for the given numbers using 1's compliment form .

a)  $8 - 4$

$$8 = 1000$$

$$+4 = 0100$$

$$-4 = 1011$$

$$8 = 1000$$

$$-4 = 1011$$

$$\begin{array}{r} \boxed{Cy=1} & 0011 \\ & 111 \\ \hline 0100 & \checkmark \end{array}$$

b)  $4 - 8$

$$4 = 00100$$

$$+8 = 01000$$

$$-8 = 10111$$

$$4 = 00100$$

$$\begin{array}{r} -8 = 10111 \\ \hline 11011 \end{array}$$

Cy=0

$$\text{Result} = -[\text{iscomp}(1011)] = -4$$

# Binary Subtraction using 2's compliment

1. Represent the given numbers in the 2's compliment form
2. Add the two numbers
3. If carry is generated ,ignore it .
- 4 .If MSB is 0, then the result is positive and in the true form .
5. If MSB is 1, then the result is negative and is in 2's compliment form .

Q) Perform the following operation for the given numbers using 2's compliment form .

a)  $46 - 14$

$$46 = \underline{0101110}$$

$$+ 14 = \underline{\underline{001110}}$$

$$-14 = \underline{\underline{110010}}$$

$$46 = \underline{0101110}$$

$$\begin{array}{r} -14 = \underline{\underline{01110010}} \\ \hline 32 = \underline{\underline{01000000}} = \underline{32} \end{array}$$

b)  $-75 + 26$

$$26 = \underline{\underline{0011010}}$$

$$+ 75 = \underline{\underline{01001011}}$$

$$-75 = \underline{10110101}$$

$$+ 26 = \underline{\underline{00011010}}$$

$$\begin{array}{r} Cy=0 \\ \hline \underline{\underline{10011111}} \end{array}$$

$$Ans = -[0110001] = -\underline{\underline{49}}$$

Q) Simplify the following using 2's compliment form

9+4

$C_{in} = 0$

$$x = 9 = \boxed{0}1001$$

$$y = 4 = \boxed{0}0100$$

$$\begin{array}{r} & 01001 \\ + & 00100 \\ \hline & 01101 \end{array}$$

$C_{in}$  — Carry in to the MSB

$C_{out}$  — carry out from the MSB

$$z = C_{out} = 0$$

$$C_{in} \oplus C_{out} = 0$$

$x y z$

0 0 0

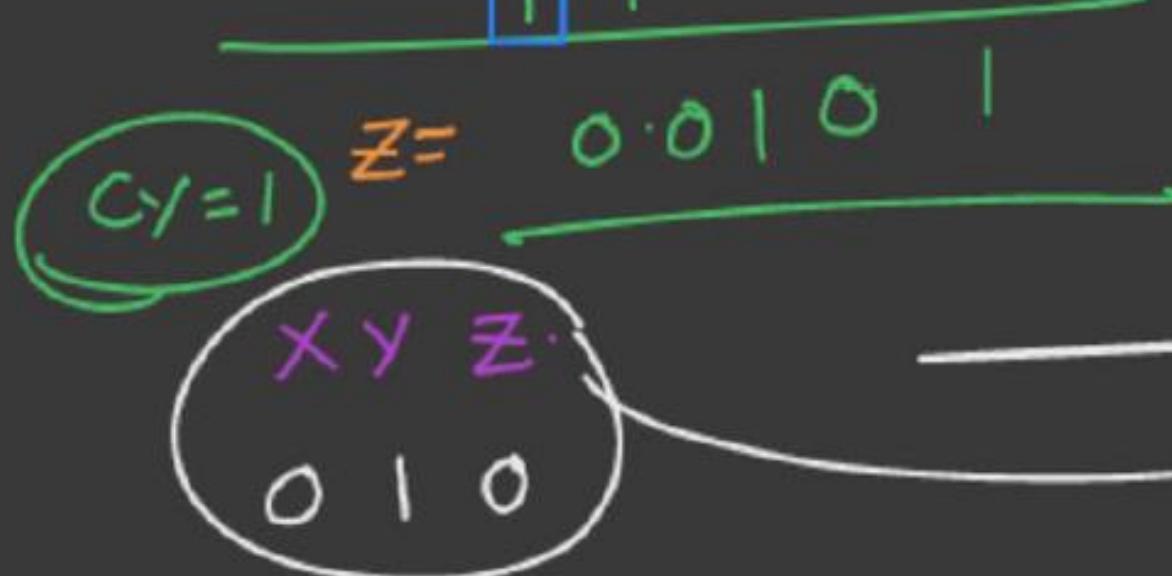
No overflow

Q) Simplify the following using 2's complement form

9 - 4

$$x = 9 = \boxed{0}1001$$

$$y = -4 = \boxed{1}1100$$



$$4 = 00100$$

$$Cin = 1$$

$$Cout = 1$$

$$Cin \oplus Cout = 0$$

No overflow

Q) Simplify the following using 2's compliment form

$$-9 + 4$$

$$x = -9 = \boxed{1}0111$$

$$y = 4 = \boxed{0}0100$$

---

$$z = \underline{\underline{1 \ 1011}}$$

$$q = 01001.$$

$$Cin = 0$$

$$Cout = 0$$

$$Cin \oplus Cout = 0$$

NO overflow

$$Ans = -[0101] = -5$$

X Y Z

---

1 0 1

No overflow

Q) Simplify the following using 2's compliment form

-9 - 4

$$-9 = 10111$$

$$\begin{array}{r} -4 = 11100 \\ \hline \end{array}$$

10011

$$Cin = 1$$

$$Cont = 1.$$

$$Cin \oplus Cont = 0$$

NO overflow

$$Ans = -[1101] = \underline{-13}$$

Q) Simplify the following using 2's complement form

$$\underline{9+8} = \underline{\underline{17}}$$

$x \times z$

$\begin{array}{r} 0 \\ 0 \\ \hline 1 \end{array}$

overflow

$$9 = \begin{array}{r} 0 \\ 1 \\ 0 \\ 0 \\ 1 \\ \hline \end{array} \quad \checkmark$$
$$8 = \begin{array}{r} 0 \\ 1 \\ 0 \\ 0 \\ 0 \\ \hline \end{array} \quad \checkmark$$
$$\begin{array}{r} & 1 \\ & 0 \\ & 0 \\ & 0 \\ & 1 \\ \hline \end{array}$$

-16 to 15..

$$\text{Ans} = - \left[ \text{2's complement } (0001) \right]$$
$$= - [ \quad 1111 ] = \underline{\underline{-15}}$$

$c_{in} = 1$

$c_{out} = 0$

$c_{in} \oplus c_{out} = 1$

overflow -

$$q = 001001$$

x y z  
0 0 0

$$g = 001000$$

no

$$\begin{array}{r} & & & & \\ \hline & 0 & 1 & 0 & 0 & 0 & 1 \\ \hline \end{array}$$

✓

$$Cin = 0$$

$$Cont = 0$$

$$Cin + Cont = 0$$

no overflow

$$Ans = + [10001] = + \underline{17}$$

Q) Simplify the following using 2's complement form

$$\begin{array}{r} -9 \\ -8 \\ \hline = -17 \end{array}$$

$$\begin{array}{r} xyz \\ -9 \\ \hline -9 = 10111 \end{array}$$

$$\begin{array}{r} 110 \\ -8 \\ \hline -8 = 11000 \end{array}$$

$$cy=1$$



ignore

$$01111$$

c<sub>in</sub> = 0

c<sub>out</sub> = 1

c<sub>in</sub> ⊕ c<sub>out</sub> = 1.

Overflow

$$9 = 01001$$

$$8 = 01000$$

Range

$$-2^{n-1} \text{ to } +2^{n-1}$$

$$\begin{array}{r} ans = + [111] \\ \hline = +15 \end{array}$$

$$-2^4 \cdot to +2^4 - 1$$

$$\underline{-16 to 15}$$

$\begin{matrix} XYZ \\ 111 \end{matrix}$

$$-q =$$

$11\ 0111$

$$-8 =$$

$11\ 1000$

          |

101111

$C_y = 1$

$\downarrow$

Ignore

$A_{\text{sg}} = - \left[ 2^{\text{'s comp}} (0111) \right]$

$= - [10001] = \underline{-17}$

$q = 001001$

$s = 001000$

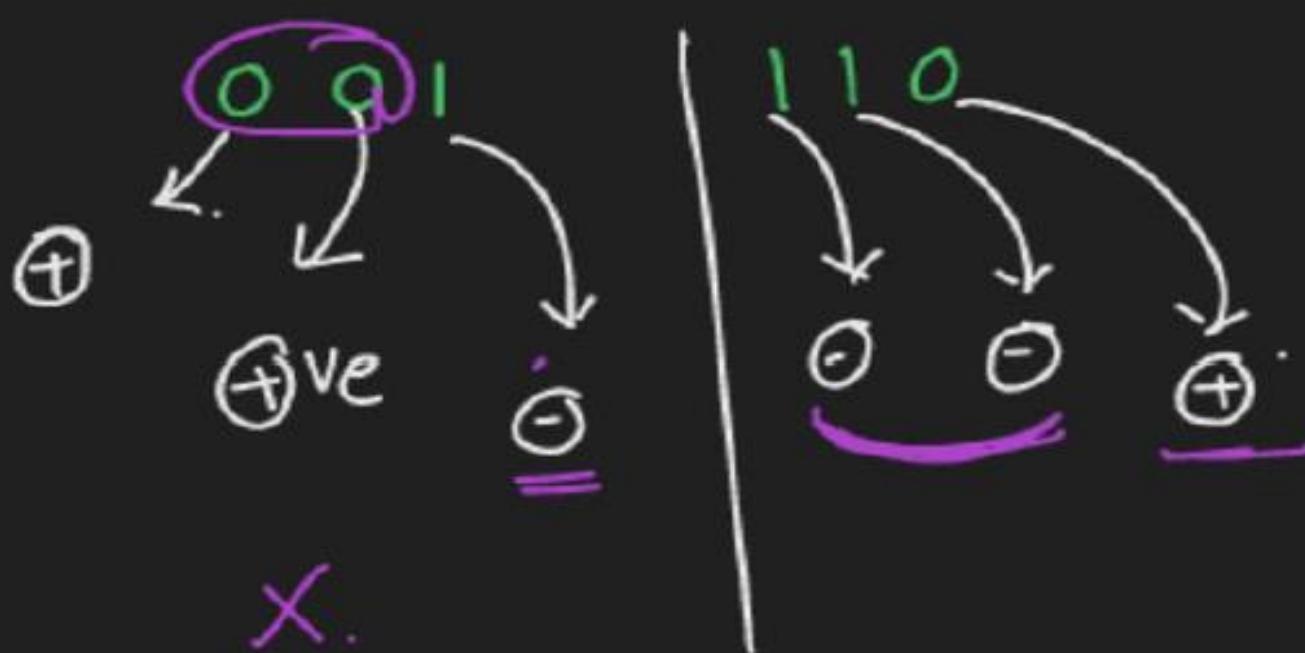
$C_{in} = 1$

$C_{out} = 1$

$C_{in} \oplus C_{out} = 0$

No overflow

$$\text{Overflow} = \bar{x}\bar{y}\bar{z} + xy\bar{z}$$



# Overflow

Over flow occurs in signed arithmetic operations if two same sign numbers are added and result exceeds with given number of bits.

Over flow can be detected by using 2- methods

1. by using carry bits
2. by using sign bit

# 1. By using carry bits

$C_{in}$  ----- *carry into MSB*

$C_{out}$  ----- *carry out from MSB*

if

$C_{in} \oplus C_{out} = 0$  , no overflow occurs

$C_{in} \oplus C_{out} = 1$  , over flow occurs

## 2. By using sign bit

X -----> Sign bit of 1<sup>st</sup> number

Y -----> Sign bit of 2<sup>nd</sup> number

Z-----> Sign bit of Resultant

$$\begin{array}{c} XYZ \\ \bar{X}\bar{Y}Z \end{array}$$

Over flow =  $XYZ + \bar{X}\bar{Y}Z$

# Overflow

Over flow occurs in signed arithmetic operations if two same sign numbers are added and result exceeds with given number of bits.

Over flow can be detected by using 2- methods

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# 1. By using carry bits

$C_{in}$  ----- *carry into MSB*

$C_{out}$  ----- *carry out from MSB*

if  $C_{in} \oplus C_{out} = 0$  , no overflow occurs

$C_{in} \oplus C_{out} = 1$  , over flow occurs

## 2. By using sign bit

X -----> Sign bit of 1<sup>st</sup> number

Y -----> Sign bit of 2<sup>nd</sup> number

Z-----> Sign bit of Resultant

$$\begin{array}{c} XYZ \\ \bar{X}\bar{Y}Z \end{array}$$

$$\text{Over flow} = XYZ + \bar{X}\bar{Y}Z$$

## NOTE :

TO AVOID THE OVERFLOW , INCREASE THE NUMBER OF BITS .

Q) Let x be the sign bit of  $N_1$ , y be the sign bit of  $N_2$ , and z be the sign bit of  $N_1 + N_2$ , then the condition for overflow .

- a)  $x \neq y \neq z$
- b)  $x \neq y = z$
- c)  $x = y \neq z$
- d)  $x = y = z$

Q) Two numbers represented in signed 2's complement form as  $P = 11101101$  ,  $Q = 11100110$  , if Q is subtracted from P , then the value obtained in signed 2's compliment from is

- a) 100000111
- b) 00000111
- c) 11111001
- d) 111111001

$$\begin{array}{r} P = \quad 1 \ 1 \ 1 \quad 0 \ 1 \quad 1 \ 0 \ 1 \\ -Q = \quad 0 \ 0 \ 0 \quad 1 \ 1 \quad 0 \ 1 \ 0 \\ \hline \quad 0 \ 0 \ 0 \quad 0 \ 1 \ 1 \ 1 \\ \hline \end{array}$$

# BINARY CODES

# Numeric Codes

- 1.BCD Code
- 2.Excess-3 Code
- 3.Gray Code
- 4.Self-complementing code
- 5.Cyclic Code
- 6.Reflective Code

# 1. BCD (Binary Coded Decimal) Code :

In this code each decimal number is represented by a separate group of 4- bits.

The image shows a handwritten mathematical equation. On the left, the decimal number  $(2\ 3\ 4\ 5)_{10}$  is written in red. To its right, an equals sign follows a plus sign ( $= +$ ). To the right of the equals sign, four binary numbers are listed under a single horizontal line:  $0010$ ,  $0011$ ,  $0100$ , and  $0101$ . Each of these four binary numbers has a green checkmark above it. A purple oval encloses the first binary number,  $0010$ , and a yellow bar highlights the second digit of this number,  $0010$ .

- It uses only 0 to 9
- 0 to 9 are valid BCD Code
- 10, 11, 12, 13, 14, 15 are invalid BCD Code
- Coding method is very simple but it requires more number of bits .

Eg. of BCD Codes

8 4 2 1
2 4 2 1
3 3 2 1
4 2 2 1
5 2 1 1
5 3 1 1
5 4 2 1
6 3 1 1
7 4 2 1
7 4 $\bar{2}$ $\bar{1}$
8 4 $\bar{2}$ $\bar{1}$

$$\begin{array}{c|c} \begin{array}{c} 2421 \\ \hline 0111 \\ |110 \end{array} & \begin{array}{c} 3321 \\ \hline 1100 \end{array} \\ \hline & \begin{array}{c} 5421 \\ \hline 0110 \end{array} \end{array}$$
$$\begin{array}{c} 7421 \\ \hline |010 \end{array} \quad \begin{array}{c} 74\bar{2}\bar{1} \\ \hline 0000-3 \\ 0011 \rightarrow 0 \end{array}$$

# BCD Addition

1. Express the given numbers in BCD form
2. Add the corresponding digits of the decimal numbers of each group .
3. If there is no carry and the sum term is not illegal code , no correction is needed
4. If there is a carry out of one group to next group , (or) if the sum term is an illegal code , then add  $6_{10}$  ( 0110) to the sum term of that group and the resulting carry is added to the next group .

Q) Perform the following using BCD addition

$$25 + 13$$

$$25 = 0010 \quad 0101$$

$$13 = 0001 \quad 0011$$

$$\begin{array}{r} 0010 \\ + 0001 \\ \hline 0011 \end{array} \quad \begin{array}{r} 0101 \\ + 0011 \\ \hline 1010 \end{array}$$

3      8

Q) Perform the following using BCD addition

$$679.6 + 536.8$$

$$679.6 = 0110 \quad 0111 \quad 1001 \cdot 0110$$

$$\begin{array}{r} 536.8 = 0101 \quad 0011 \\ \hline \end{array}$$

$$\begin{array}{r} 0 \cdot 1011 \quad 1010 \quad 1111 \cdot 1110 \\ 0110 \quad 0110 \quad 0110 \cdot 0110 \\ \hline \end{array}$$

$$\begin{array}{r} 1 \quad 1111 \quad 1111 \\ \hline 0001 \quad 0010 \quad 0001 \quad 0110 \cdot 0100 \\ \hline \end{array}$$

$$\begin{array}{r} 1 \\ 2 \\ \hline 6 \cdot 4 \\ \hline \end{array}$$

# BCD Subtraction

1. Express the given numbers in BCD form
2. Subtract the corresponding digits of the decimal numbers of each group .
3. If there is no barrow no correction is needed.
4. If there is a barrow from the next group , then  $6_{10}$  ( 0110) is subtracted from the difference term of this group .

Q) Perform the following using BCD subtraction

38-15

Q) Perform the following using BCD subtraction

$$206.7 - 147.8$$

# EXCESS-3 CODE

The EX-3 code can be derived from the natural BCD code by adding 3 to each coded number.

	2	3	4	5	
	3	3	3	3	
	5	6	7	8	
	0101	0110	0111	1000	

**Valid EX -3 : 3,4,5,6,7,8,9,10,11,12**

**Invalid EX-3 : 0 ,1,2,,13,14,15**

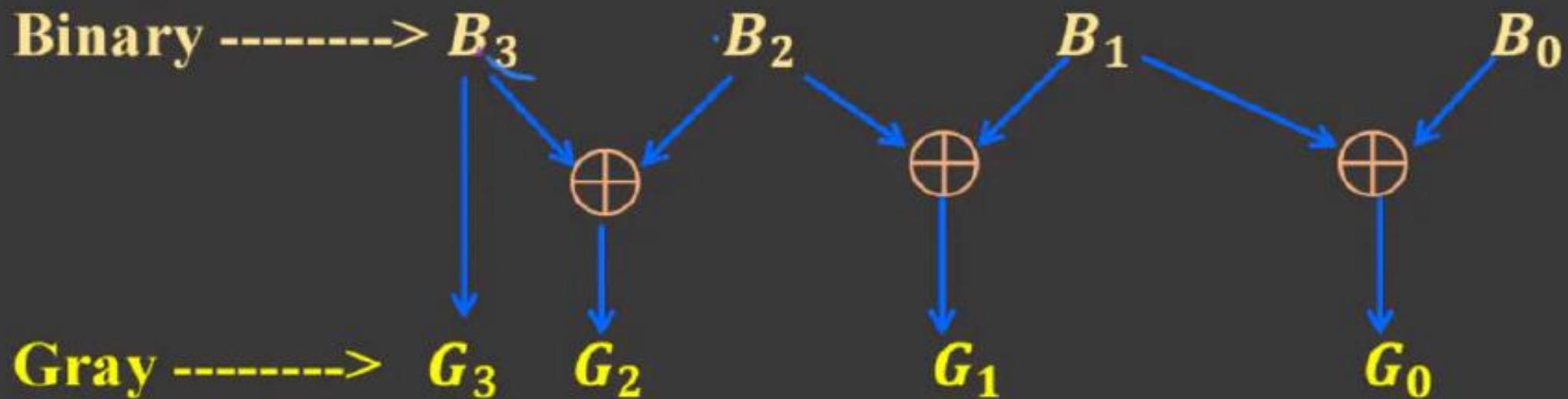
# Gray Code

Gray code is a non-weighted code, successive decimal numbers are differ by only one bit .

- Non- weighted code
- Unit distance code
- Cyclic code
- Reflective code
- Minimum error code

Decimal	1- bit Gray code	2- bit Gray code	3- bit Gray code
0	0	0 0	0 0 0
1	1	0 1	0 0 1
2		1 1	0 1 1
3		1 0	0 1 0
4			1 1 0
5			1 1 1
6			1 0 1
7			1 0 0

# Binary to Gray Code



Q) Find the Gray code of the following

110010

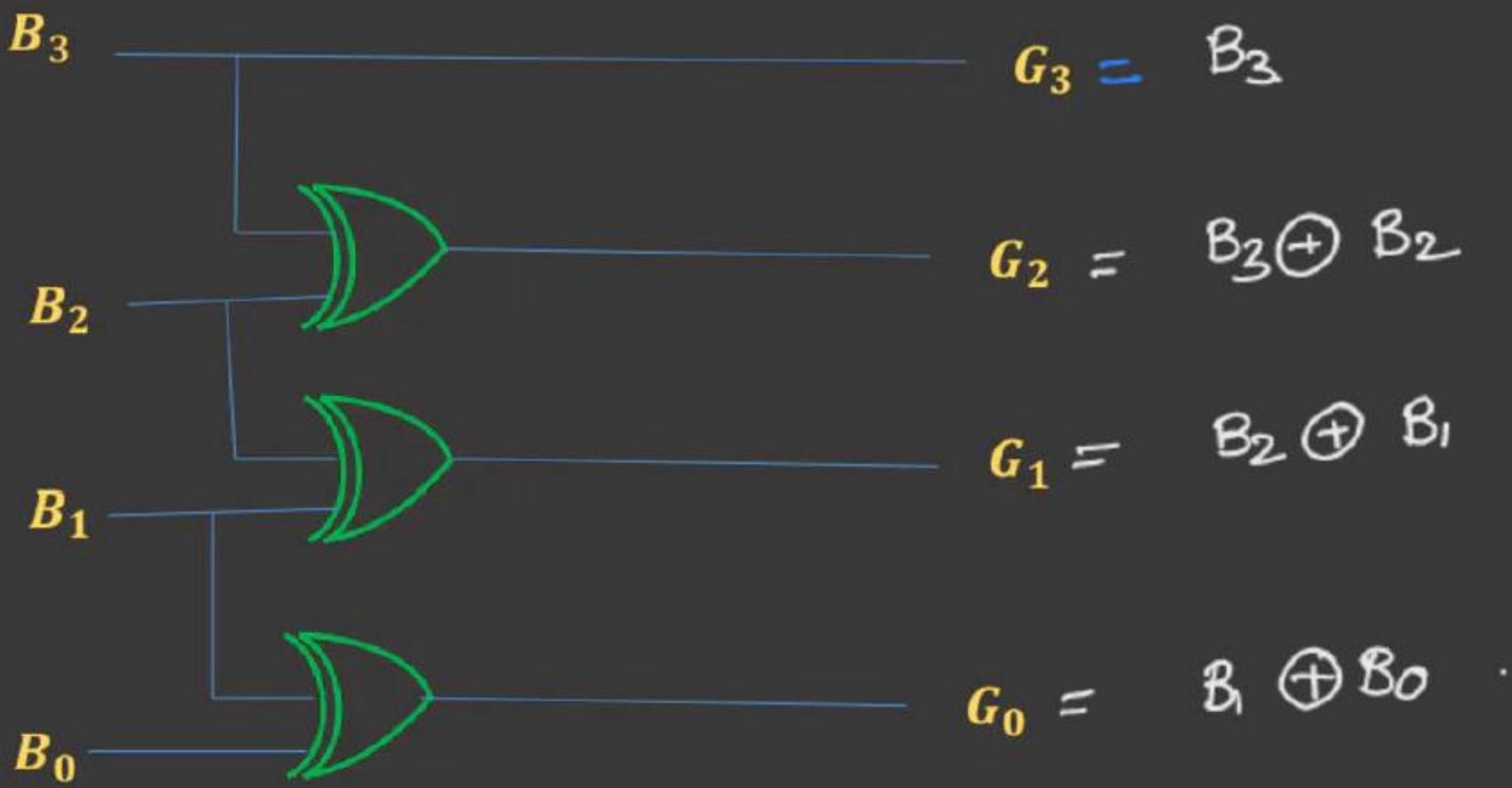
Gray = 101011.

Q) Find the Gray code of the following

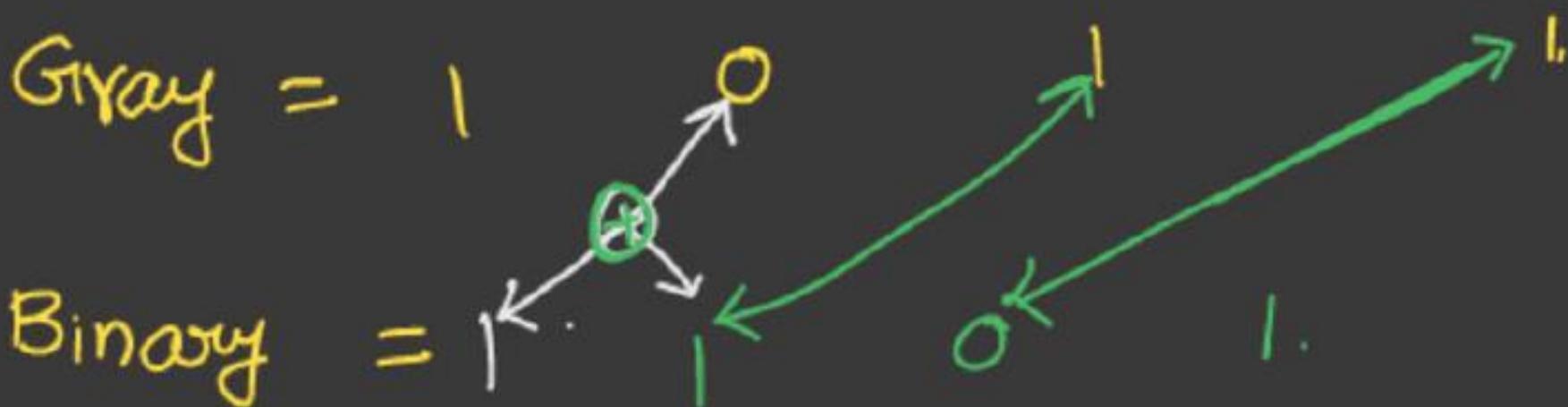
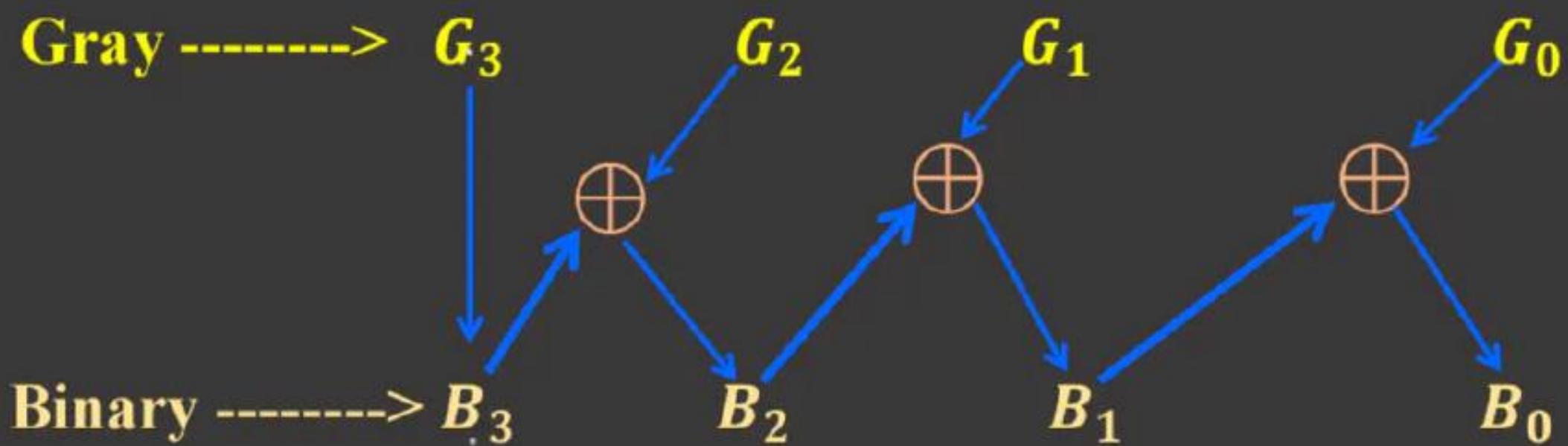
1 1 0 0 1 0

Gray = 1 0 1 0 1 1.

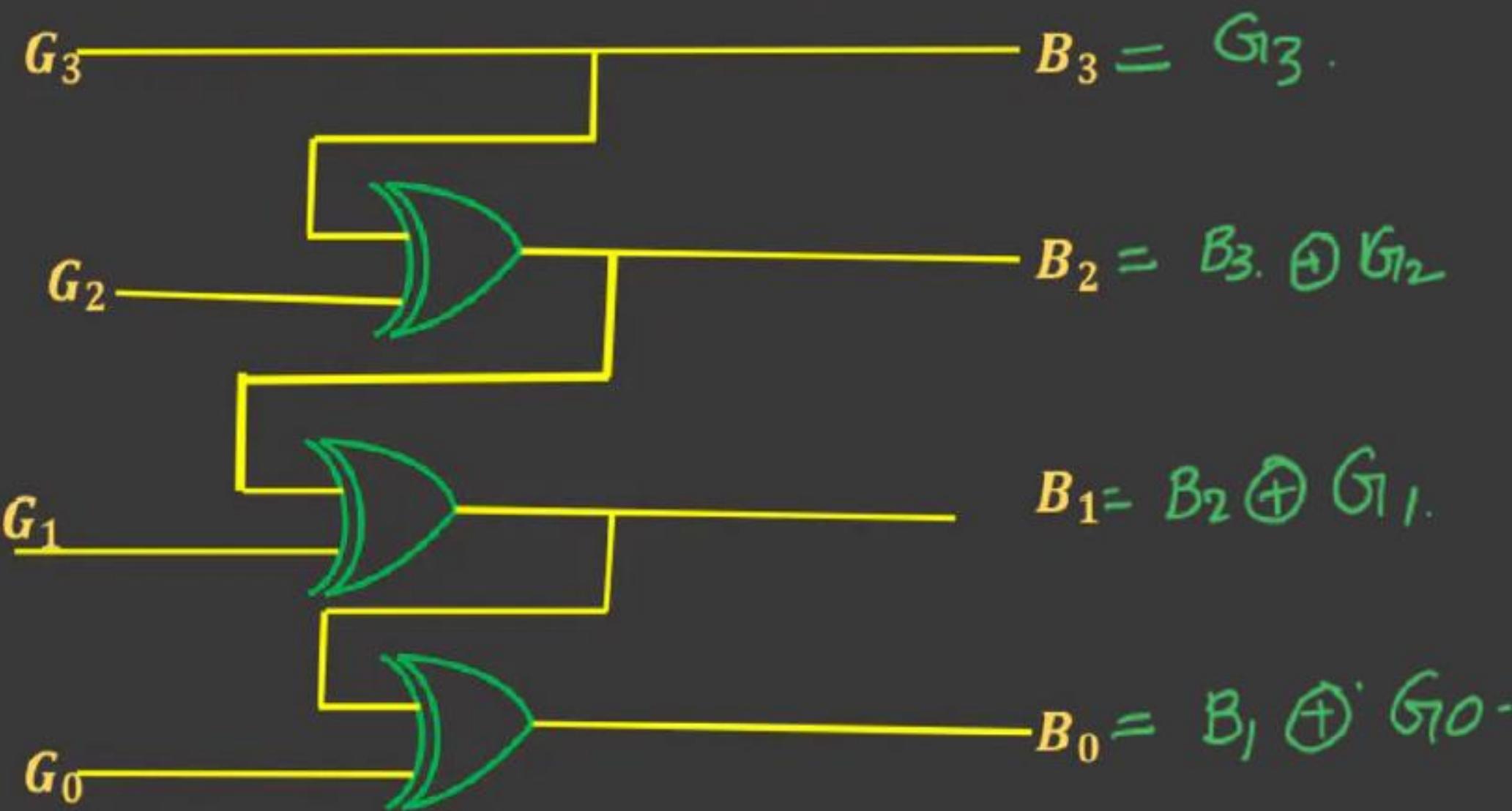
# Logic gate



# Gray to Binary Code



# Grey Code to Binary Code



Q) find the binary code of the following

1 0 1 0 1 1

Binary = 1 10010.

Q) find the binary code of the following

1 1 1 0 0 1 . 1 0

Binary = 1.0 + 1 + 0 + 1

# Self Complementing Codes

- A code is said to be self complementing, if the 1' complement of a number N is equal to the 9's complement of the number.
- For a code to be self complementing, the sum of all its weights must be 9 .

Eg. of Self Complementing Codes

2	4	2	1
5	2	1	1
4	3	1	1
3	3	2	1
XS-3			

# Combinational Logic Circuit

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For more details contact me @ **93980 21419**

# Combinational Logic Circuit

- The present output depends on present input only
- In combinational circuits feedback and clock is not present

# Adders/ Subtractor

- HA
- HS
- FA
- FS
- Parallel Adder
  - / Ripple carry Adder
- Carry look ahead Adder
- Binary Multiplier
- Magnitude Comparators
- Multiplexer
- Demultiplexers
- Decoder
- Encoder
- Priority Encoder
- Parity Generator & Parity Checker

# Half Adder

For the addition of two single bits



$$\text{Sum} = \sum m(1, 2) = \overline{A}B + A\overline{B} = A \oplus B$$

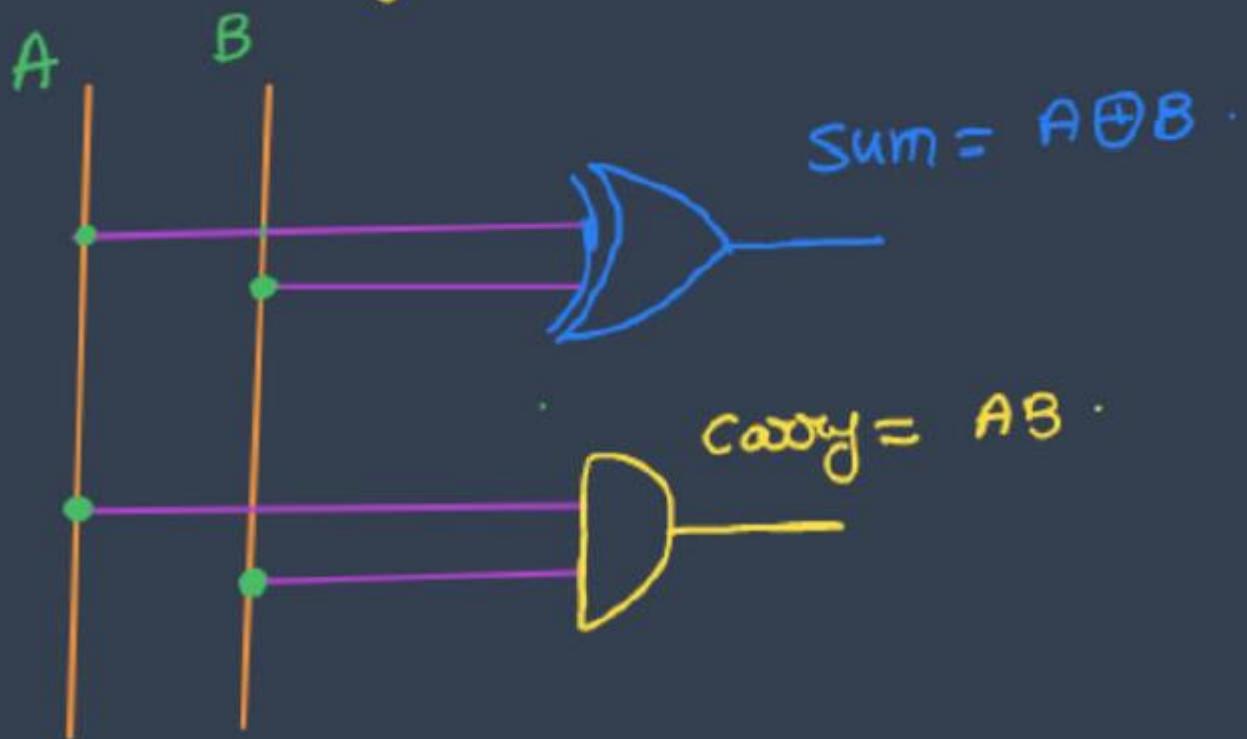
$$\text{Carry} = \sum m(3) = AB$$

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

# Logic Circuit

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = AB$$

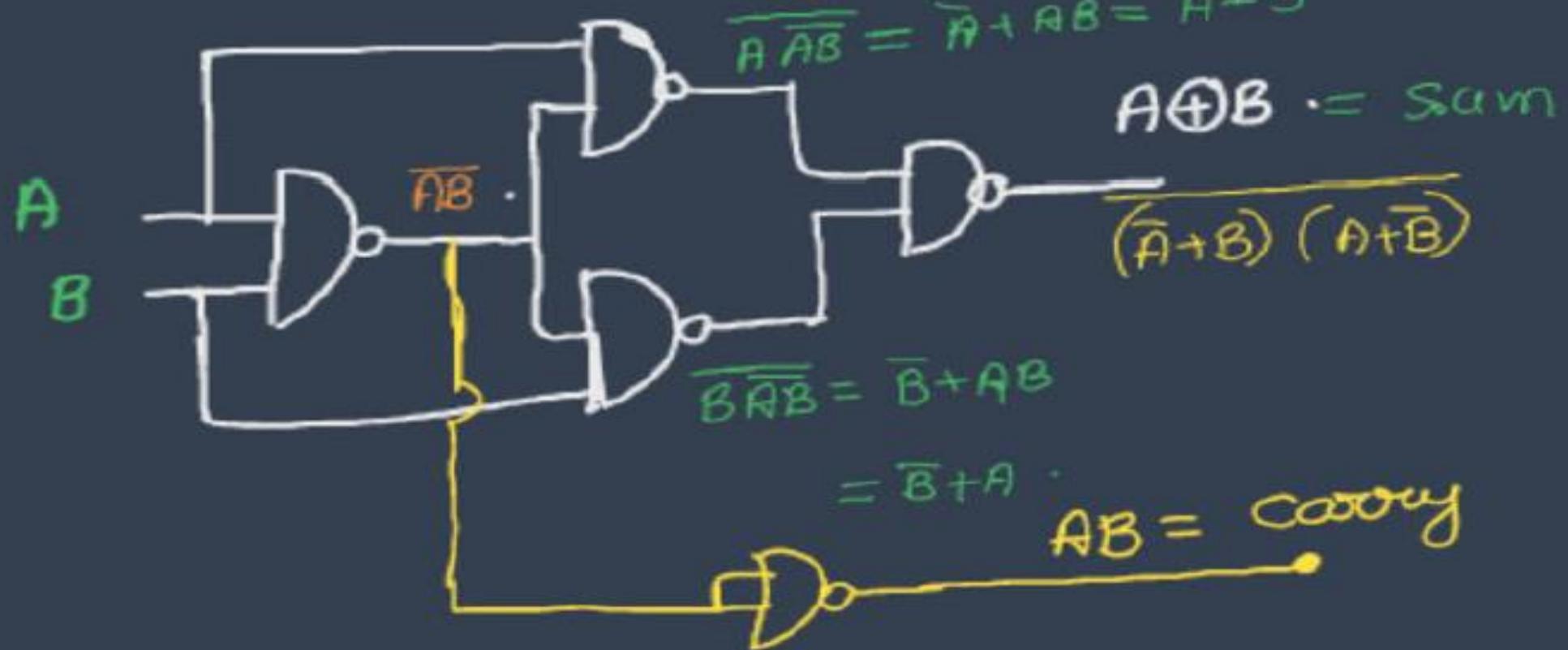


# Half Adder using NAND Gates

$$\text{Sum} = A \oplus B$$

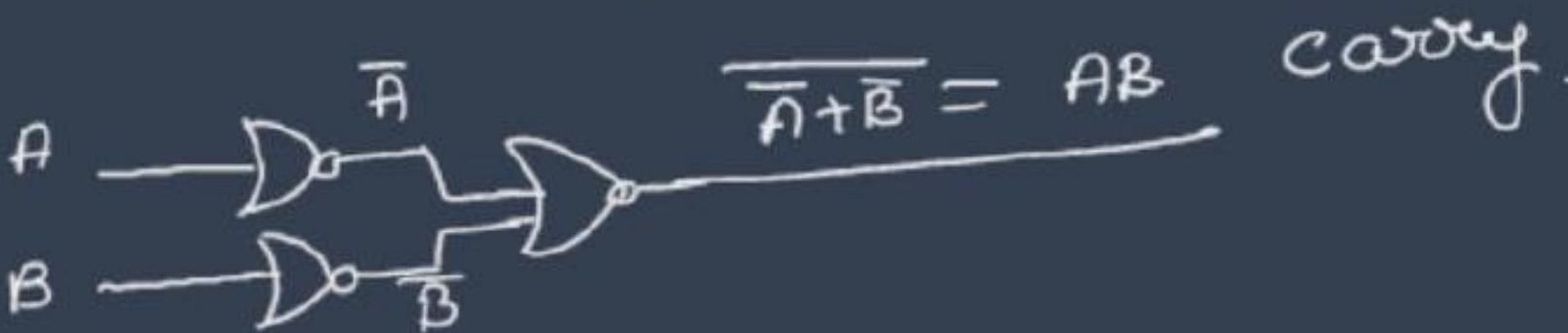
$$\text{Carry} = AB$$

$$\overline{A \overline{AB}} = \overline{A} + \overline{AB} = \overline{A} + S$$



# Half Adder using NOR Gates

$$\overline{A + \overline{A}B} = \overline{A} \cdot (\overline{A} + B) = \overline{A}B$$



⑧

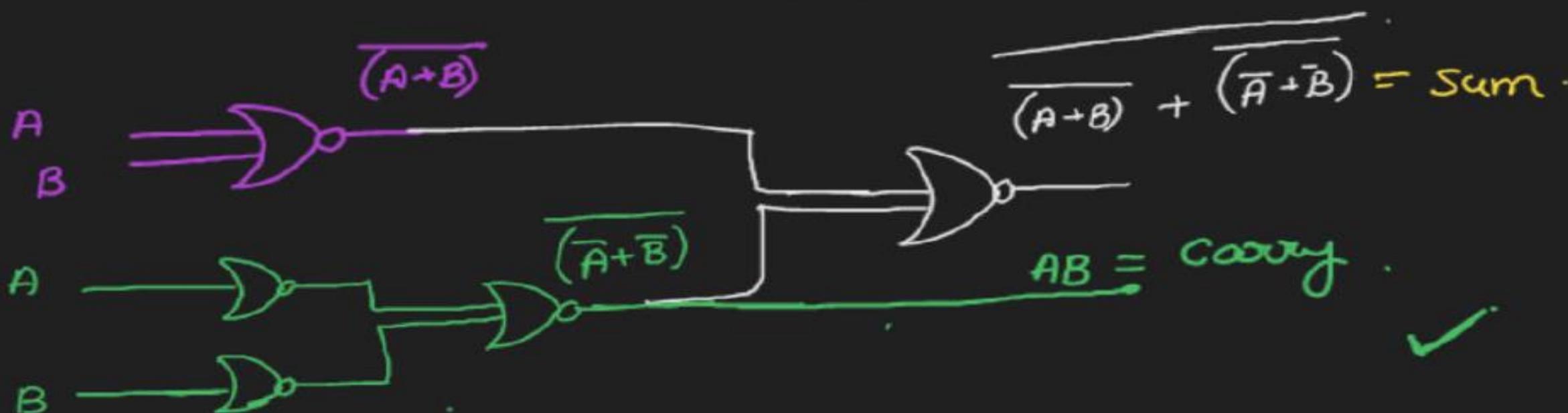
✗

# Half Adder using NOR Gates

$$\text{Sum} = A \oplus B = \overline{A \odot B}$$

$$= \overline{\overline{A} \overline{B}} + \overline{AB}$$

$$\text{Sum.} = \overline{(A+B)} + \overline{(\overline{A} + \overline{B})}$$



# Half Subtractor ( $A - B$ )

For the subtraction of two single bits



$$\text{Diff} = \sum m(1, 2) = A \oplus B$$

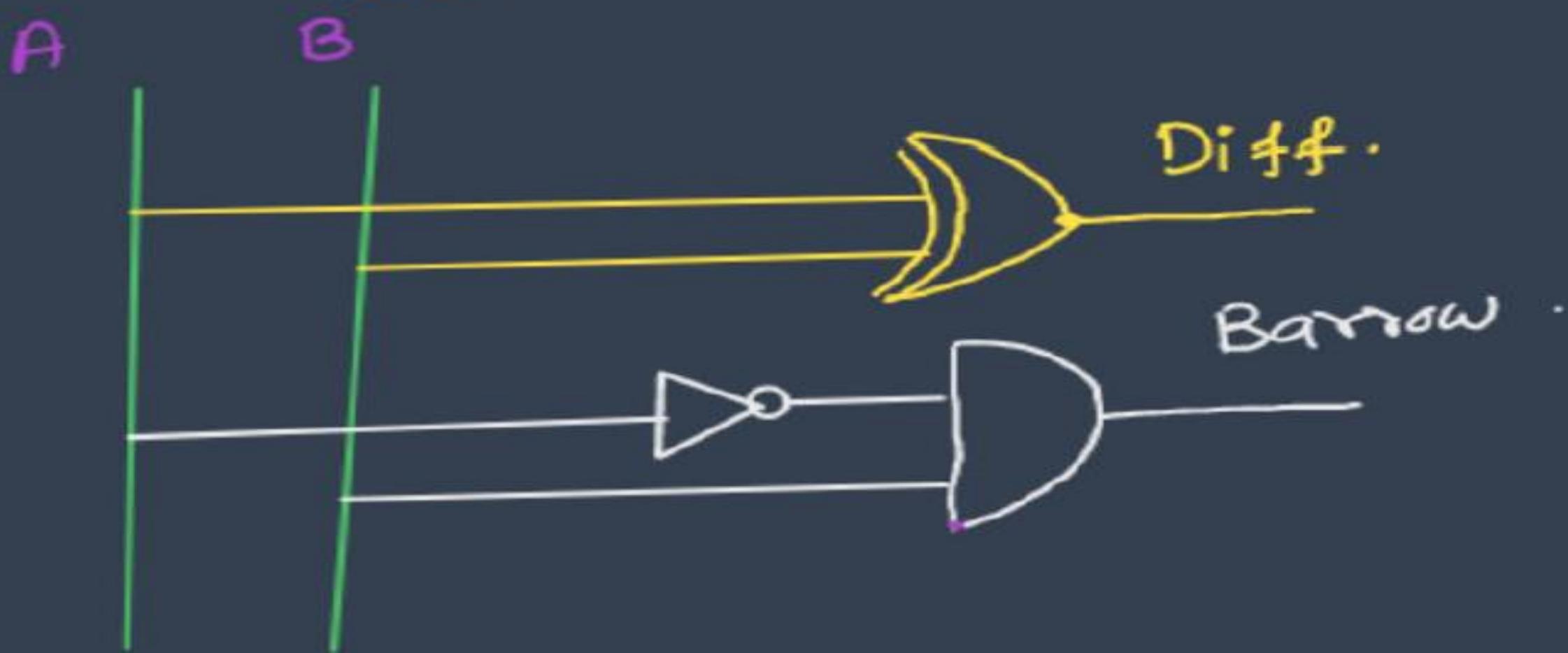
$$\text{Barrow} = \sum m(1) = \overline{A}B$$

A	B	Difference	Barrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

# Logic Circuit

$$\text{Diff} = A \oplus B$$

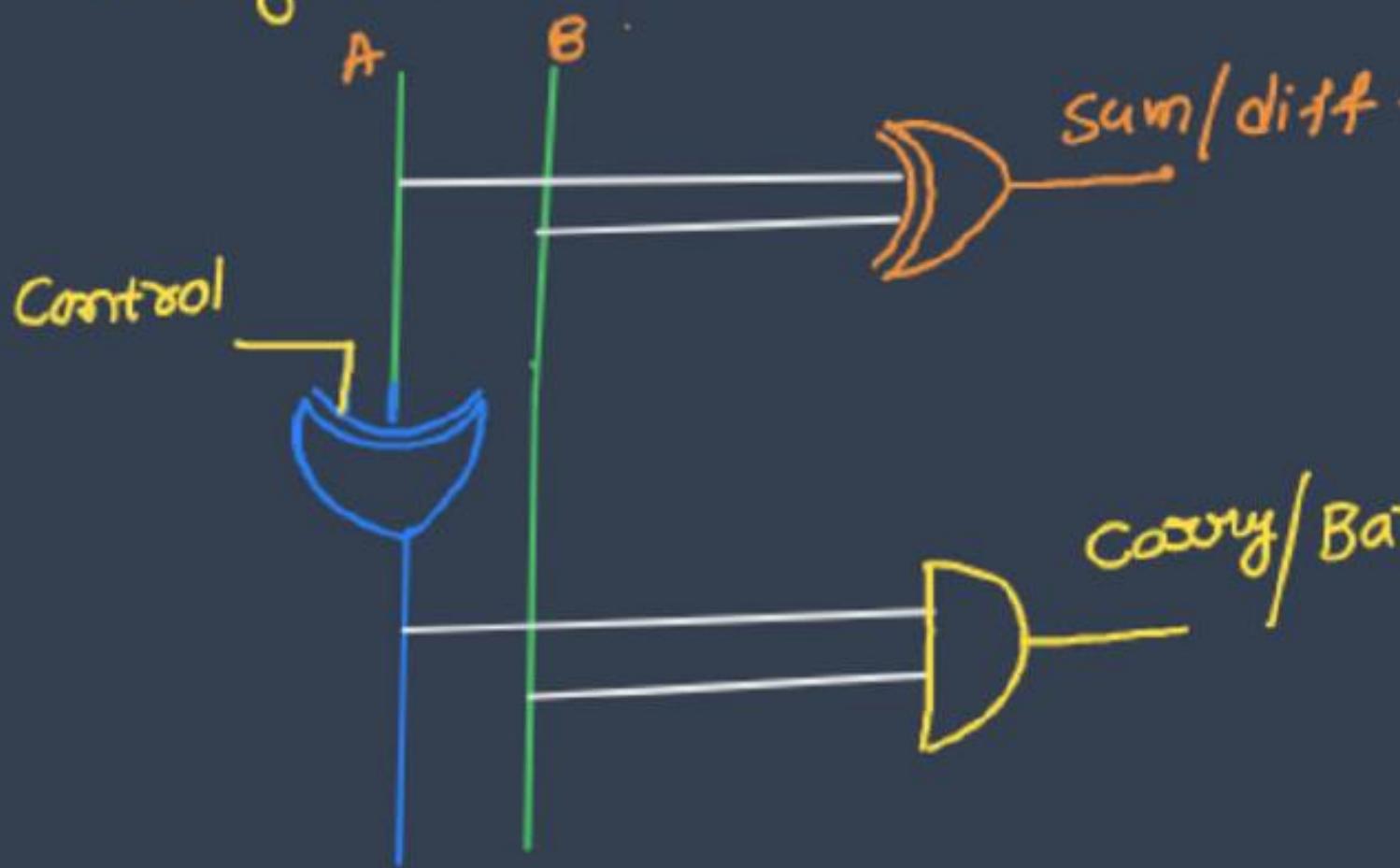
$$\text{Borrow} = \cdot \overline{A} B \cdot$$



# Half Adder / Half Subtractor

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = AB$$



$$\text{Diff} = A \oplus B$$

$$\text{Borrow} = \bar{A}B$$



Control = 0,  $Y = A$   
 Control = 1,  $Y = \bar{A}$

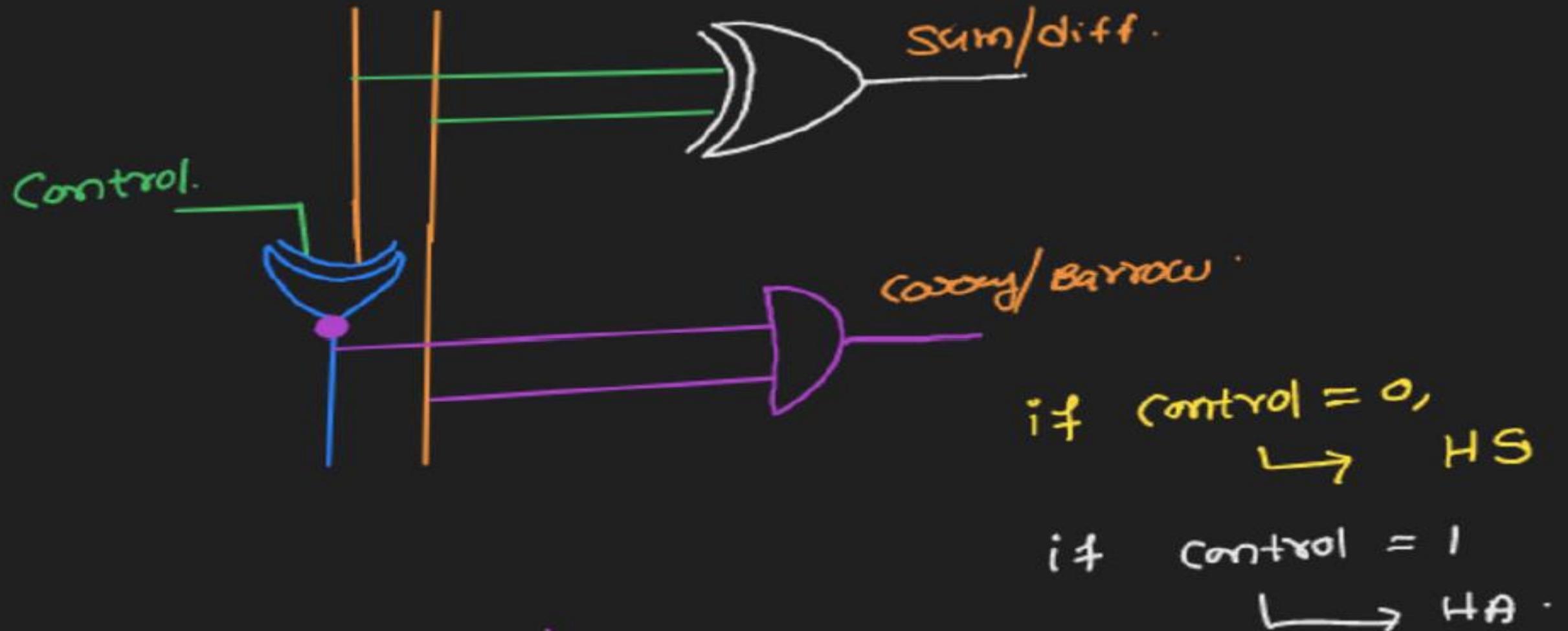
Carry / Borrow if Control = 0

$\hookrightarrow$  HA

if Control = 1.

$\hookrightarrow$  HS

# Half Adder / Half Subtractor

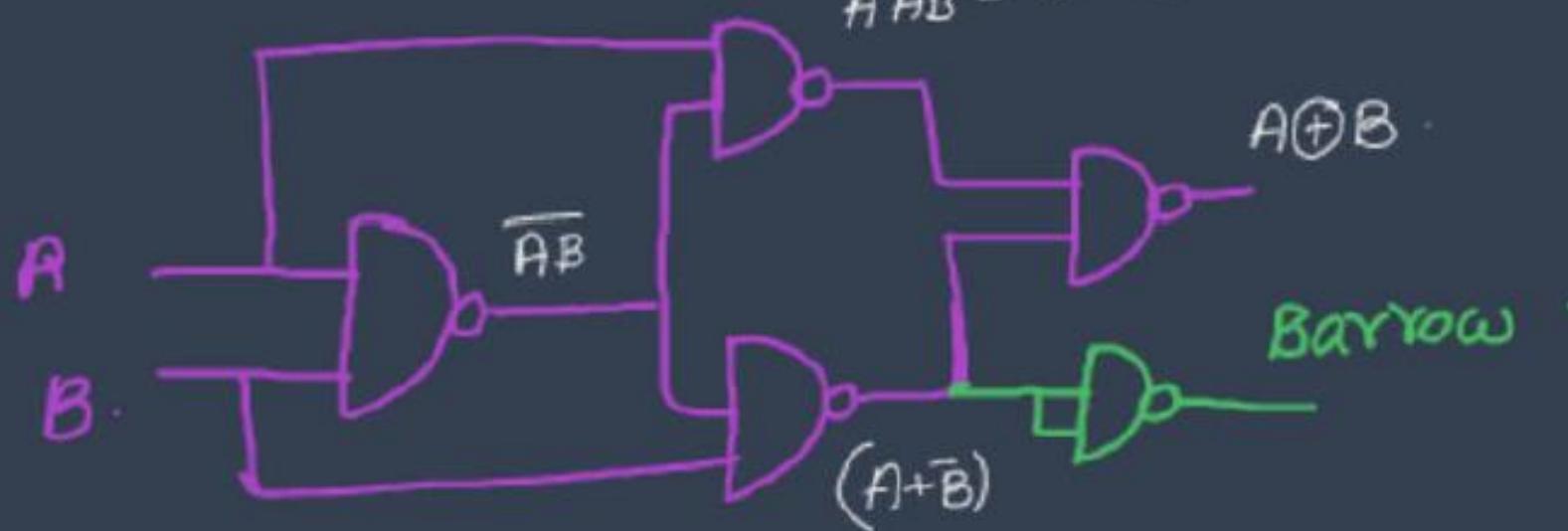


# Half Subtractor using NAND Gates

$$\text{Diff} = A \oplus B$$

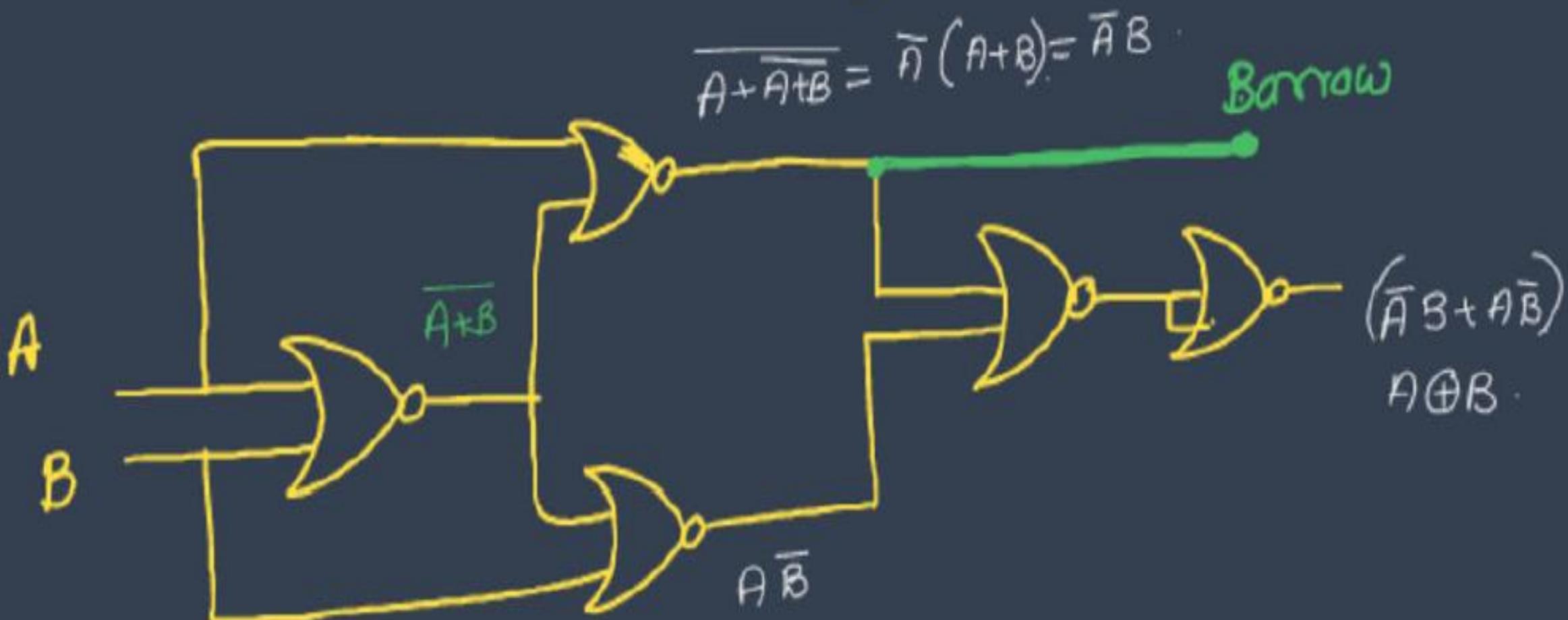
$$\text{Borrow} = \overline{A}B$$

$$\overline{\overline{A}\overline{B}} = \overline{A} + \overline{B} = \overline{A} + B$$



$$\overline{A + \overline{B}} = \overline{A}B$$

# Half Subtractor using NOR Gates



# Full Adder



$$\text{Sum} = \sum m(1, 2, 4, 7) = A \oplus B \oplus C$$

$$\text{Carry} = \sum m(3, 5, 6, 7)$$

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$\begin{aligned}
 \text{Coxxy} &= \sum m(3, 5, 6, 7) \\
 &= \overbrace{\overline{A}BC + A\overline{B}C + AB\overline{C}}^{\text{m}(3, 5, 6)} + ABC. \\
 &= AB + BC + AC.
 \end{aligned}$$

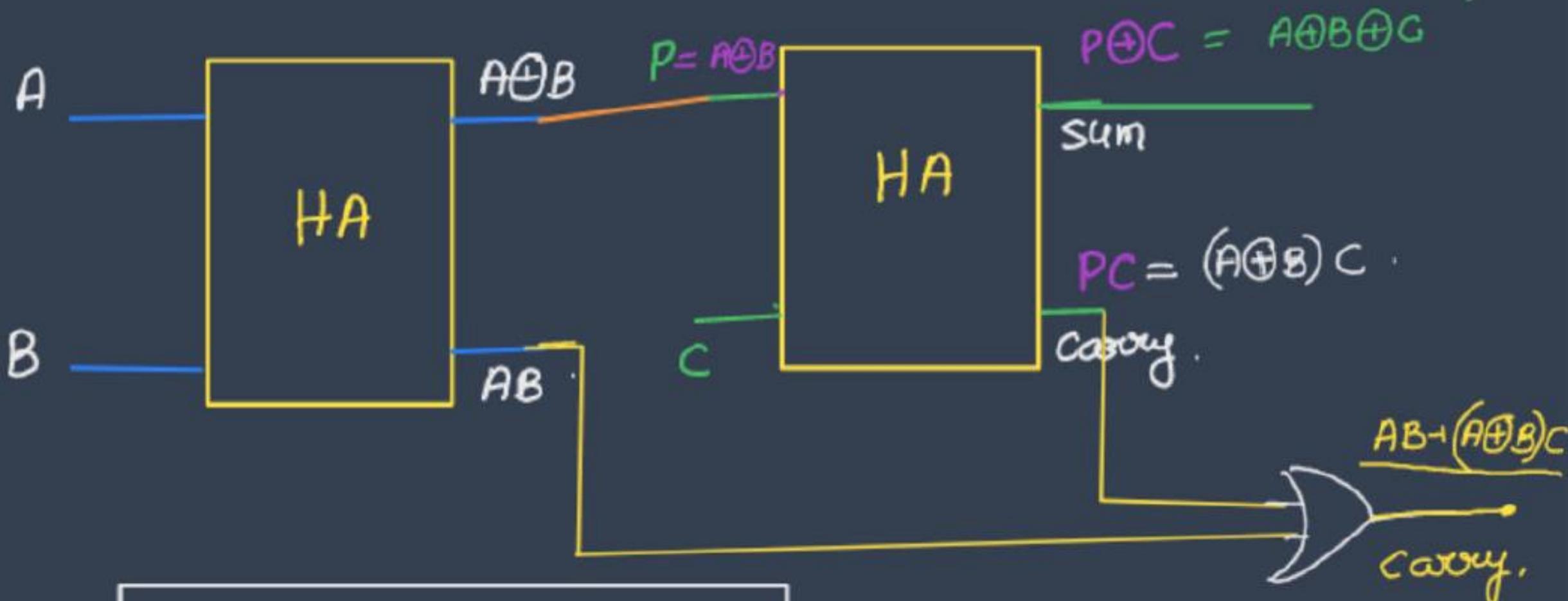
$$\begin{aligned}
 \text{Coxxy} &= \overbrace{\overline{A}BC + A\overline{B}C + AB\overline{C}}^{\text{m}(3, 5, 6)} + ABC. \\
 &= AB + (\overline{A}B + A\overline{B})C.
 \end{aligned}$$

$$\boxed{\text{Coxxy} = AB + (A \oplus B)C.}$$

# Logic Circuit

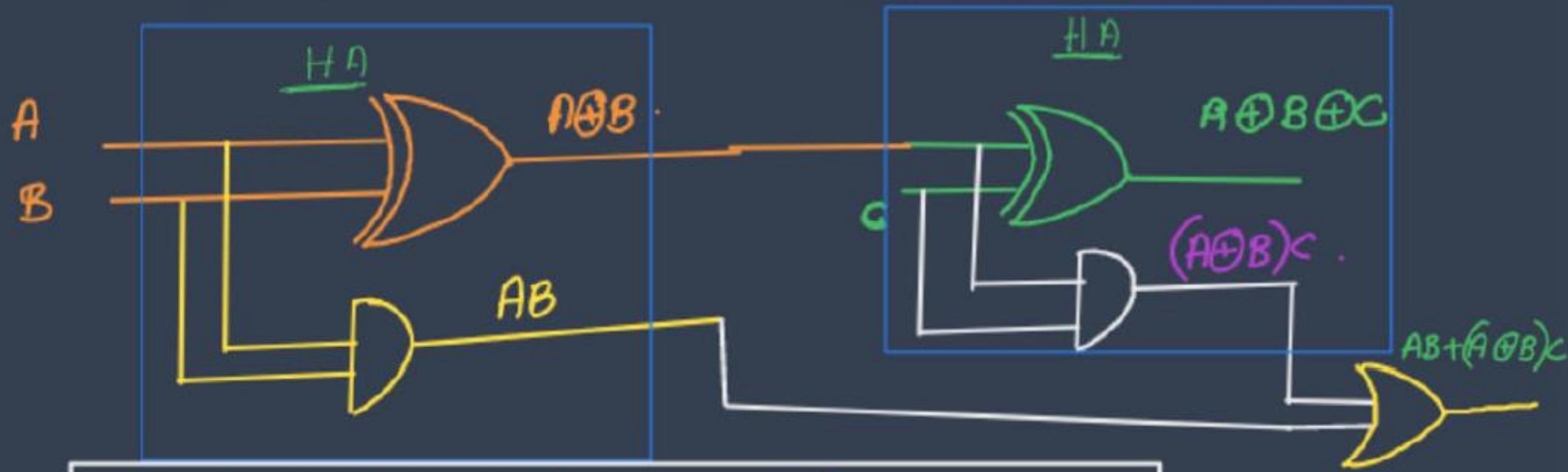


# Full Adder with two Half Adders



$$1 - FA = 2 - HA + 1 - OR$$

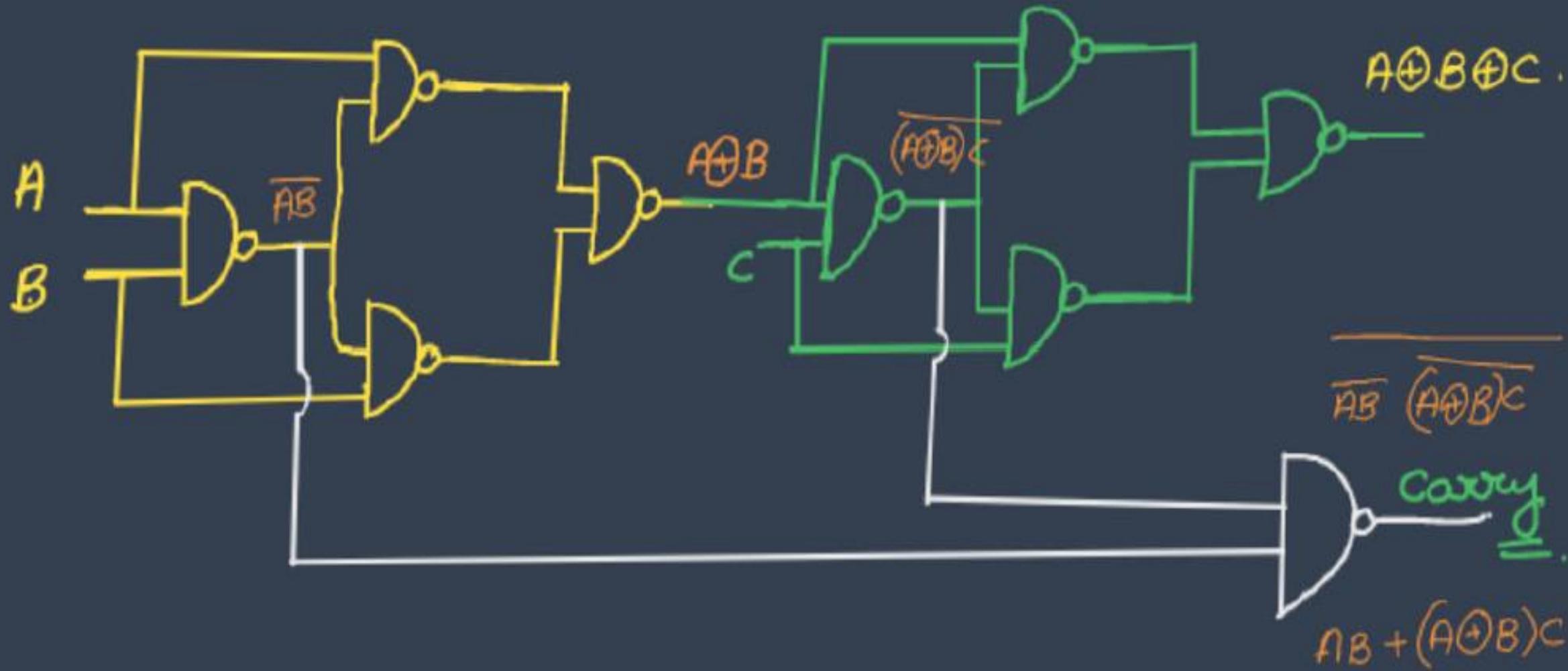
# Full Adder with two Half Adders



$$1 - FA = 2 - HA + 1 - OR$$

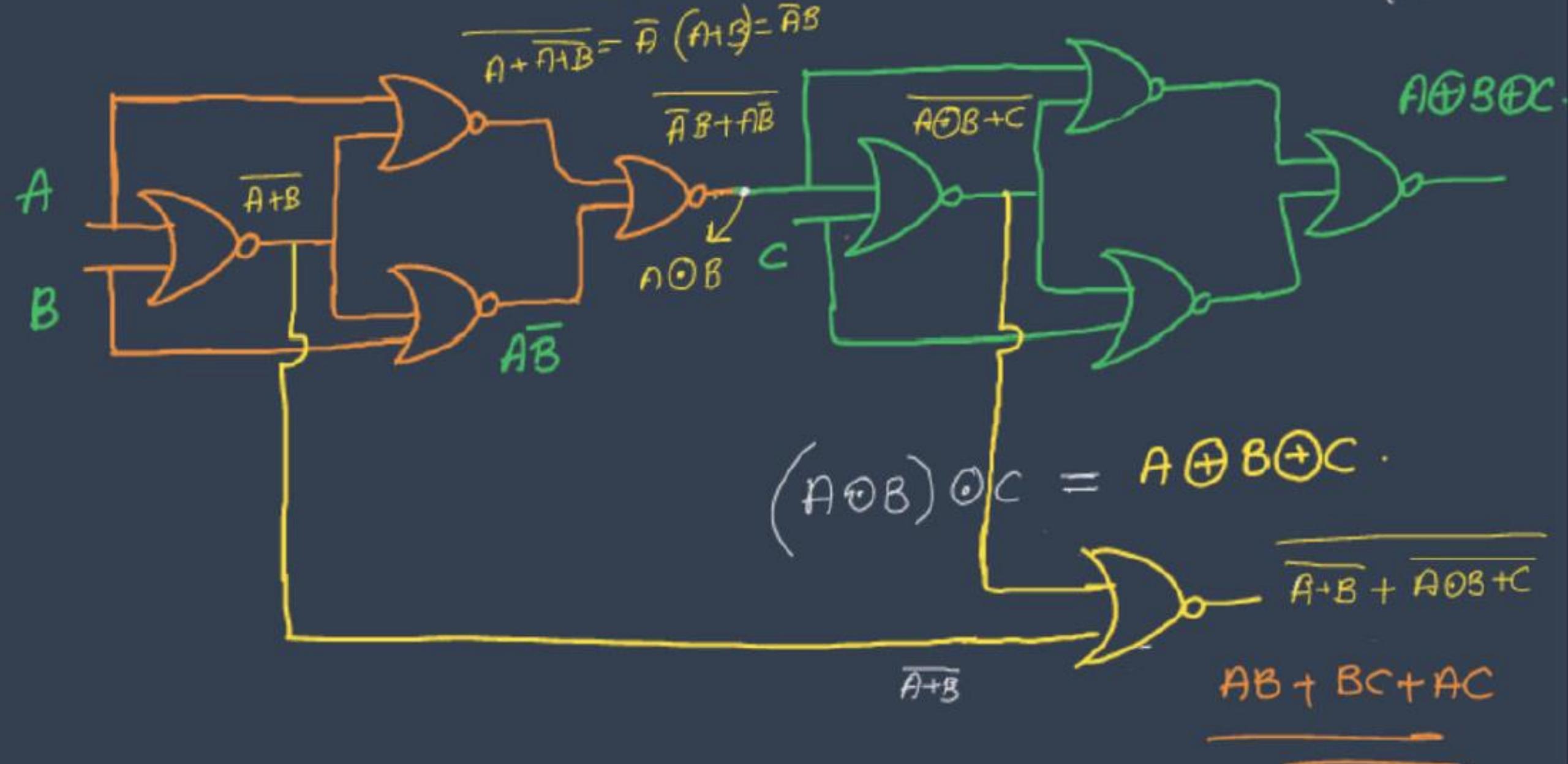
$$1 - FA = 2 - XOR + 2 - AND + 1 - OR$$

# Full Adder using NAND Gates



# Full Adder using NOR Gates

POC.



# Full Subtractor ( $A - B - C$ )

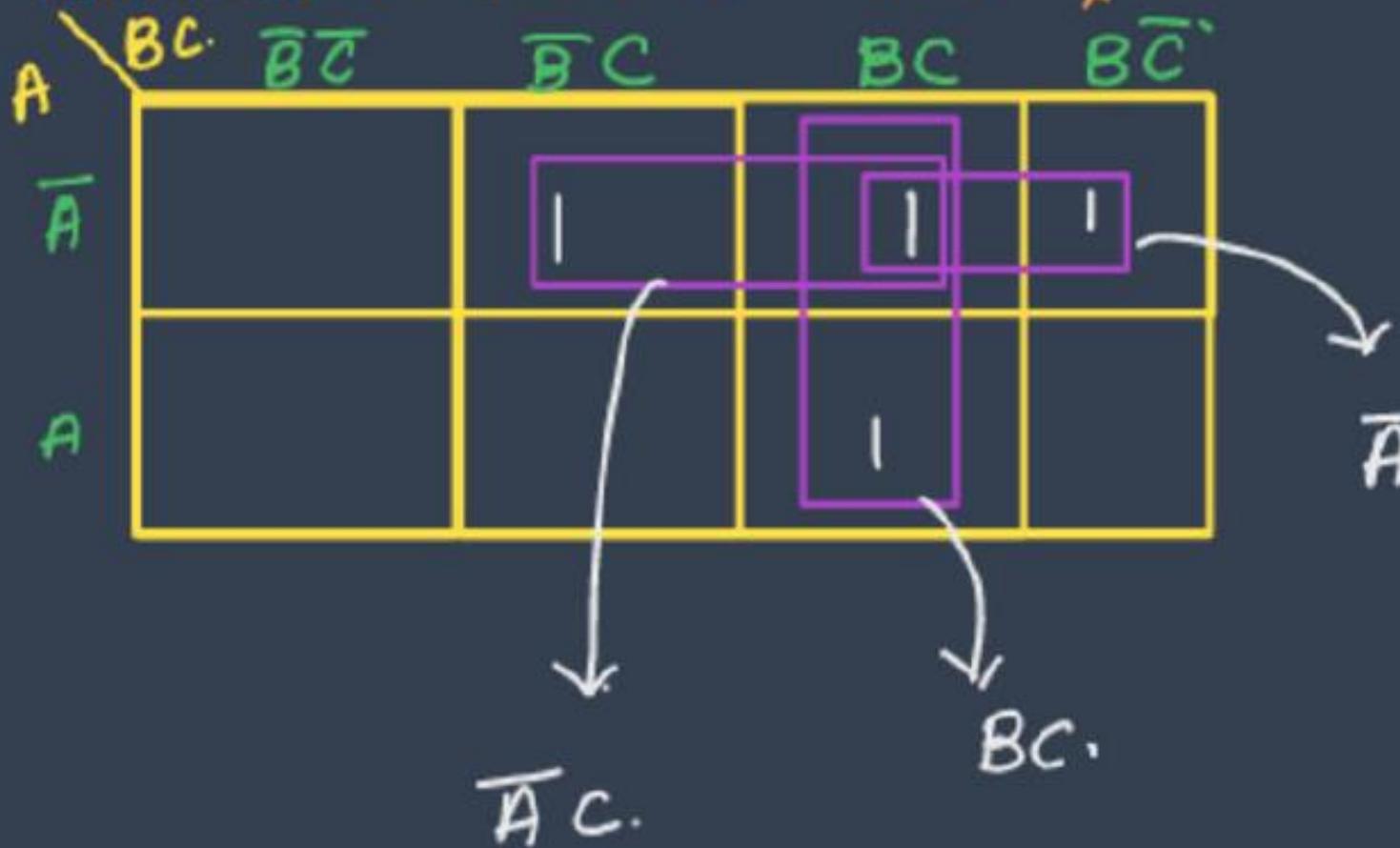


$$\text{Diff} = \sum m(1, 2, 4, 7) = A \oplus B \oplus C$$

$$\text{Barrow} = \sum m(1, 2, 3, 7)$$

A	B	C	Difference	Barrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$\text{Barrow} = \sum m (1, 2, 3, 7)$$



$$\text{Barrow} = \bar{A}B + BC + \bar{A}C.$$

Barrow =  $\sum m(1, 2, 3, 7)$

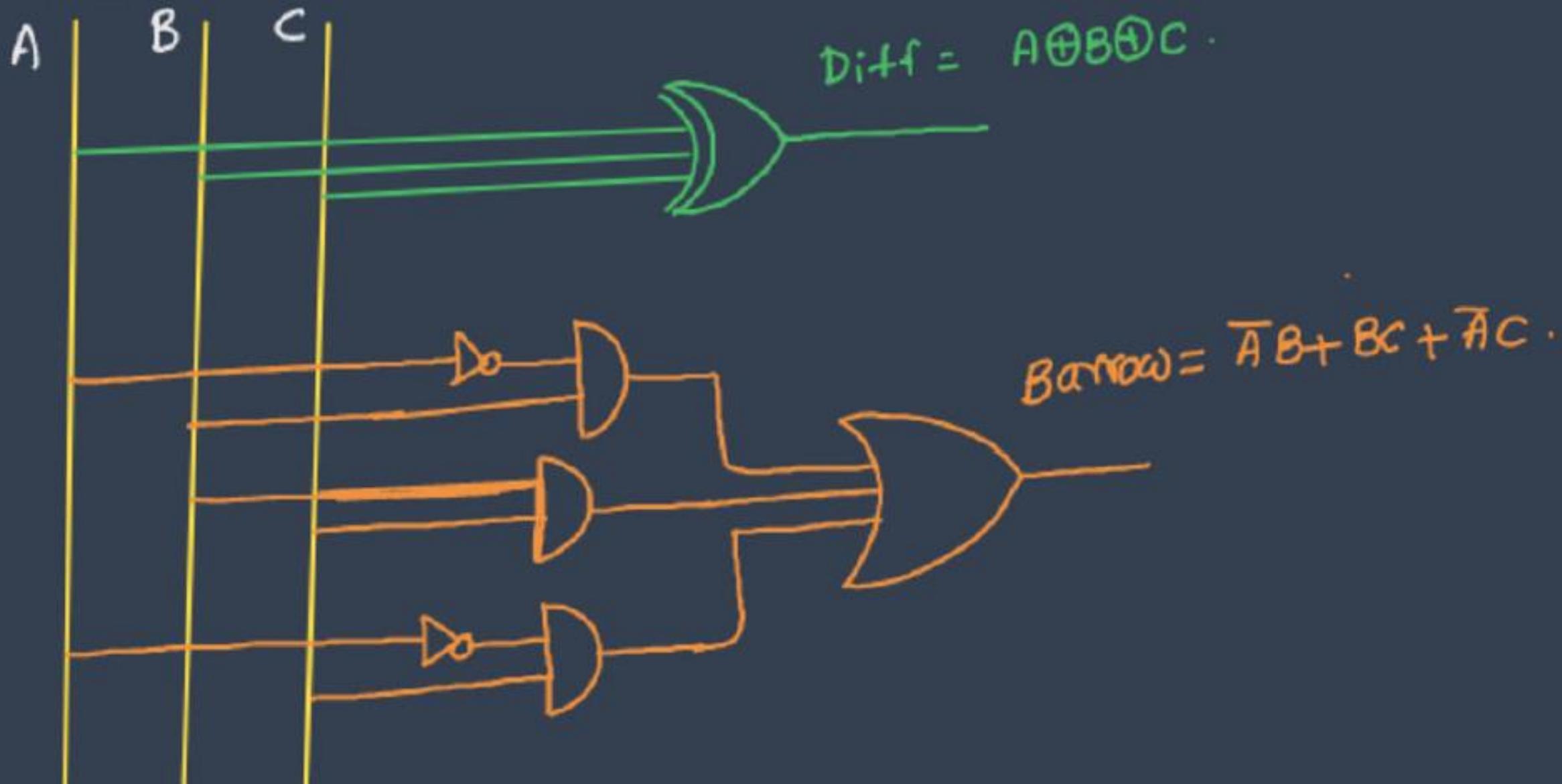
$$= \overline{A}\overline{B}C + \overbrace{\overline{A}B\overline{C} + \overline{A}Bc + A\overline{B}C}^{\text{circled terms}}.$$

$$= \overline{A}B + (\overline{A}\overline{B} + AB)c.$$

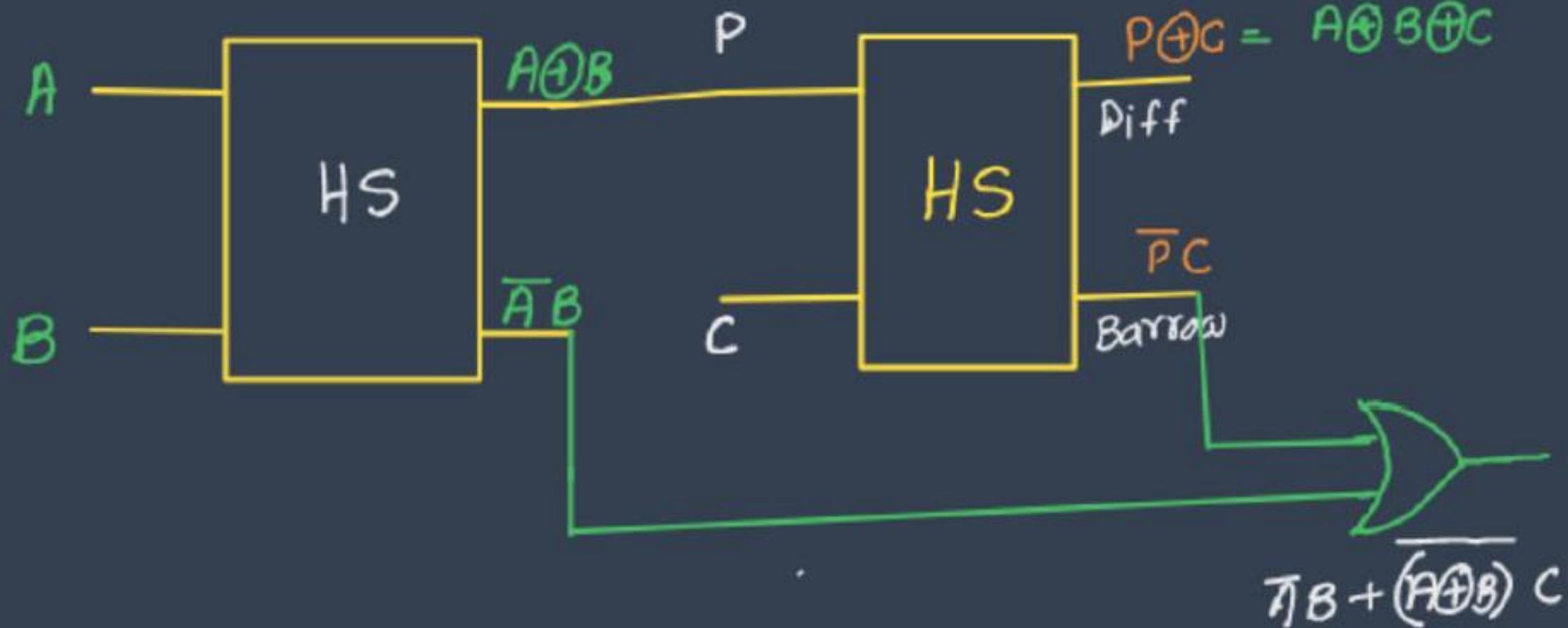
$$= \overline{A}B + (A \oplus B)c.$$

$$\boxed{\text{Barrow} = \overline{A}B + \overline{(A \oplus B)}c}$$

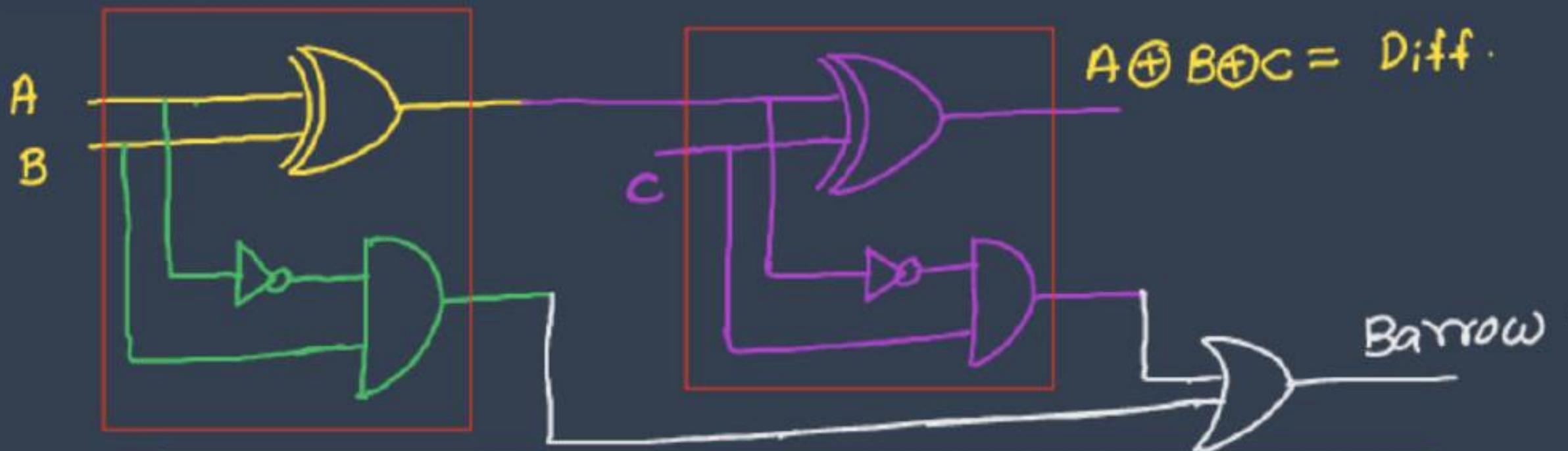
# Logic Circuit ( A-B-C ) .



# Full Subtractor with two Half Subtractors



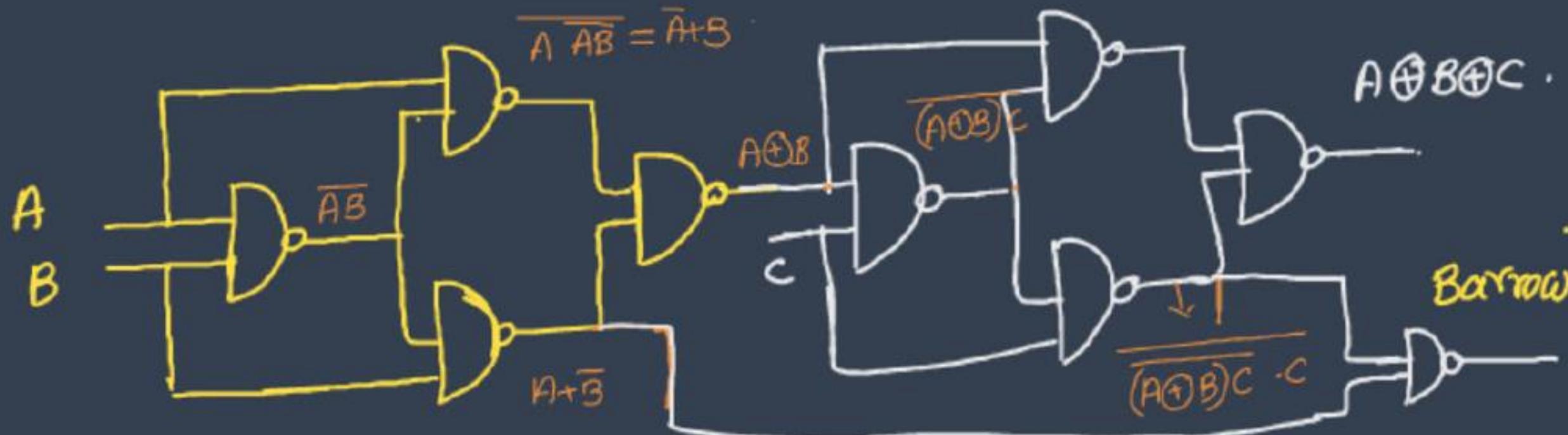
# Full Subtractor with two Half Subtractors



$$1 - FS = 2 - HS + 1 - OR$$

$$1 - FS = 2 - XOR + 2 - AND + 2 - NOT + 1 - OR$$

# Full Subtractor using NAND Gates



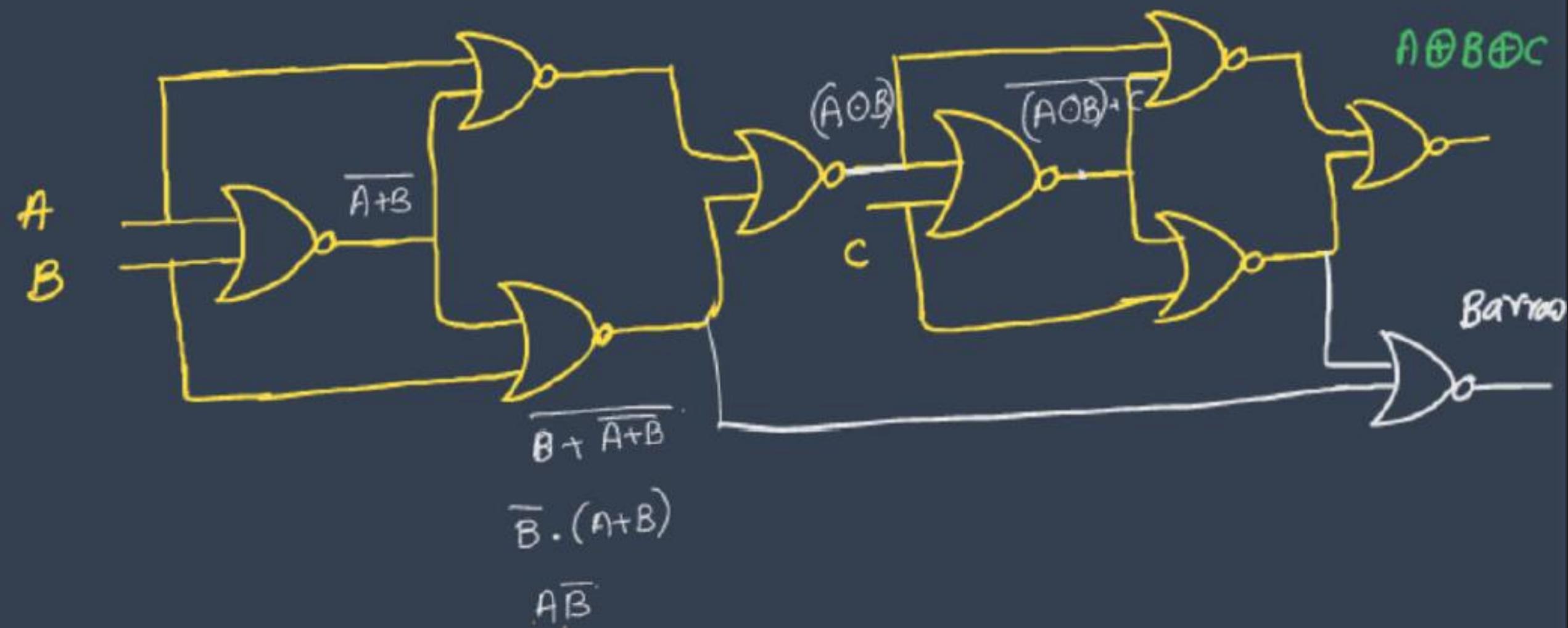
$$\overline{(A + \overline{B})(A \oplus B + \overline{C})}$$

$$\overline{\overline{AB}} + \overline{(A \oplus B)C}$$

$$A \oplus B + \overline{C}$$

$$(A \oplus B)C \rightarrow \overline{C}$$

# Full Subtractor using NOR Gates



FS : A- B- C

$$\text{Diff} = A \oplus B \oplus C.$$

$$\text{Barrow} = \overline{A}B + (\overline{A} \oplus B)C = \overline{A}B + BC + C\overline{A}$$

FS : B- C- A

$$\text{Diff} = A \oplus B \oplus C$$

$$\text{Barrow} = A\overline{B} + \overline{B}C + AC$$

FS : C- A- B

$$\text{Diff} = A \oplus B \oplus C$$

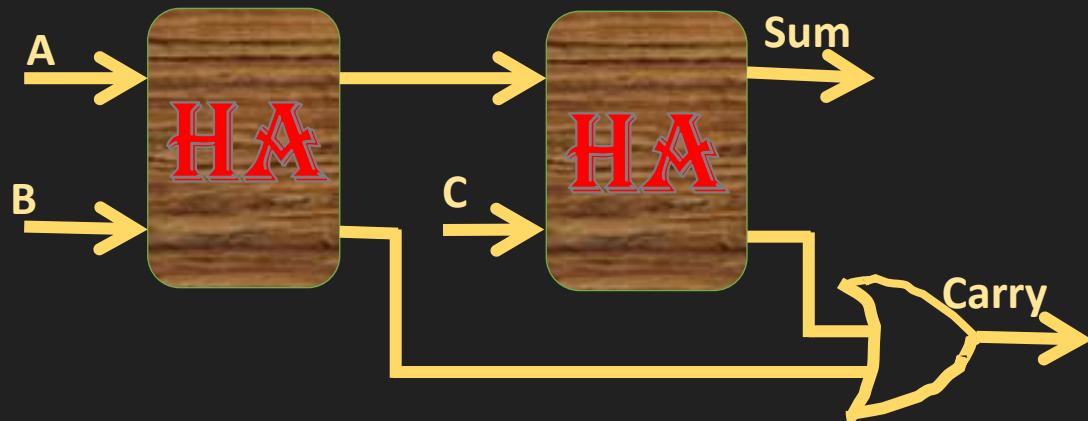
$$\text{Barrow} = AB + B\overline{C} + A\overline{C}$$

## HA

1. Logical expression for Sum =  $A \oplus B$
2. Logical expression for Carry =  $AB$
3. Minimum number of NAND Gates = 5
4. Minimum number of NOR Gates = 5

## FA

1. Logical expression for Sum =  $A \oplus B \oplus C$
2. Logical expression for Carry =  $AB + (A \oplus B)C$
3. Minimum number of NAND Gates = 9
4. Minimum number of NOR Gates = 9

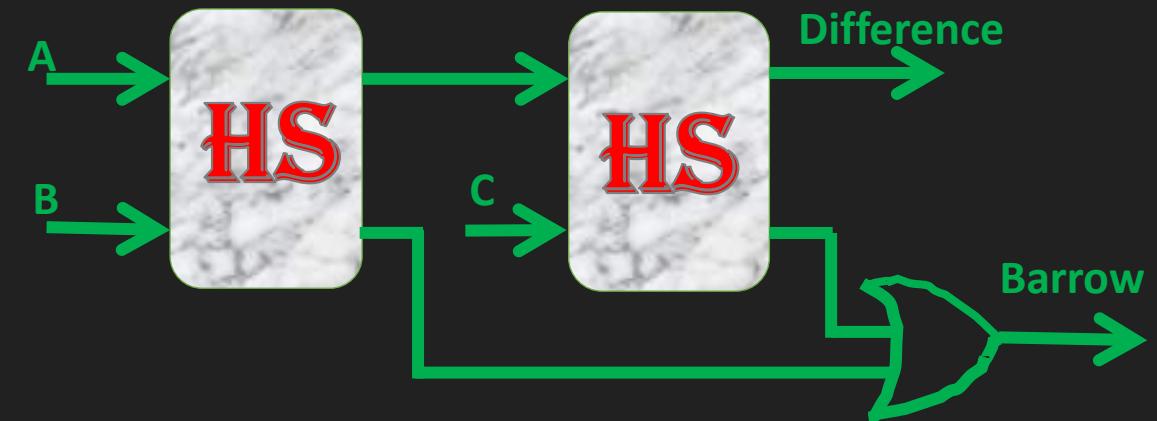


## HS

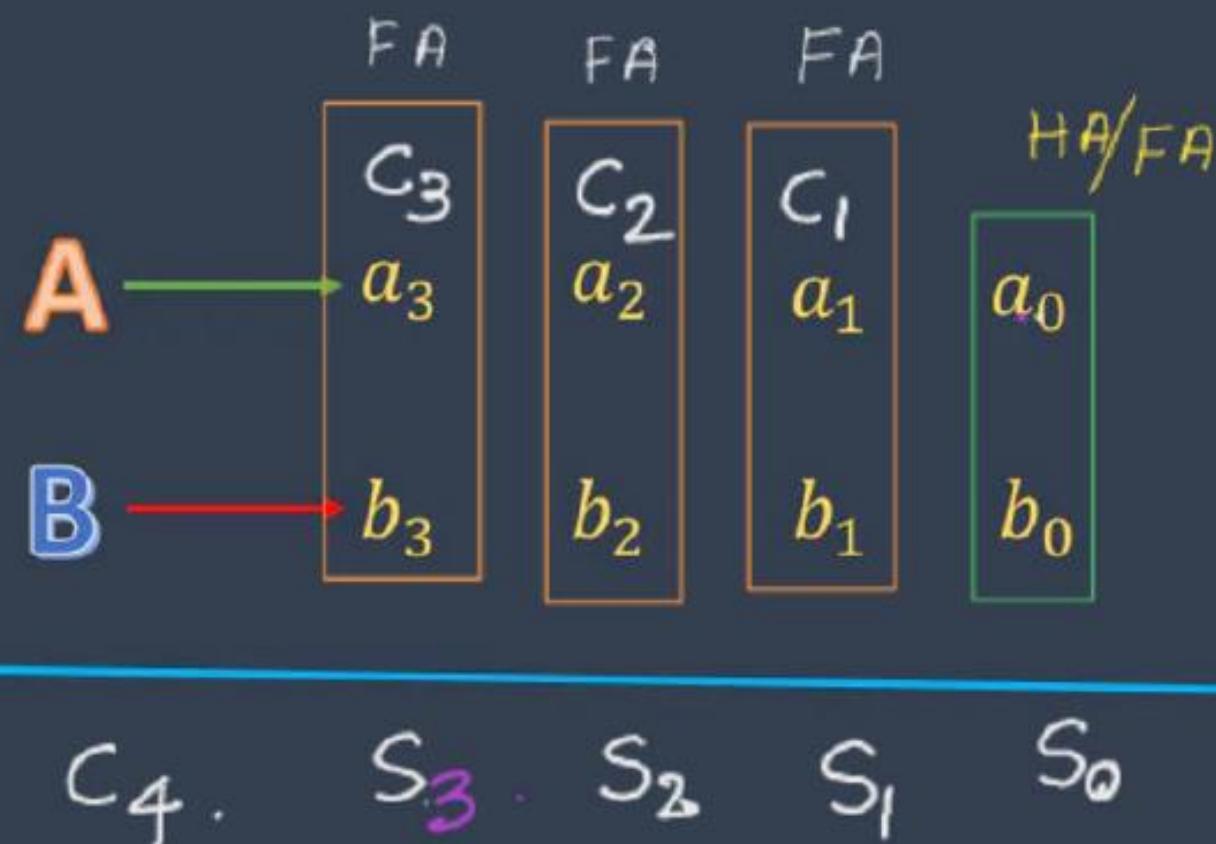
1. Logical expression for Difference =  $A \oplus B$
2. Logical expression for Barrow =  $\bar{A}B$
3. Minimum number of NAND Gates = 5
4. Minimum number of NOR Gates = 5

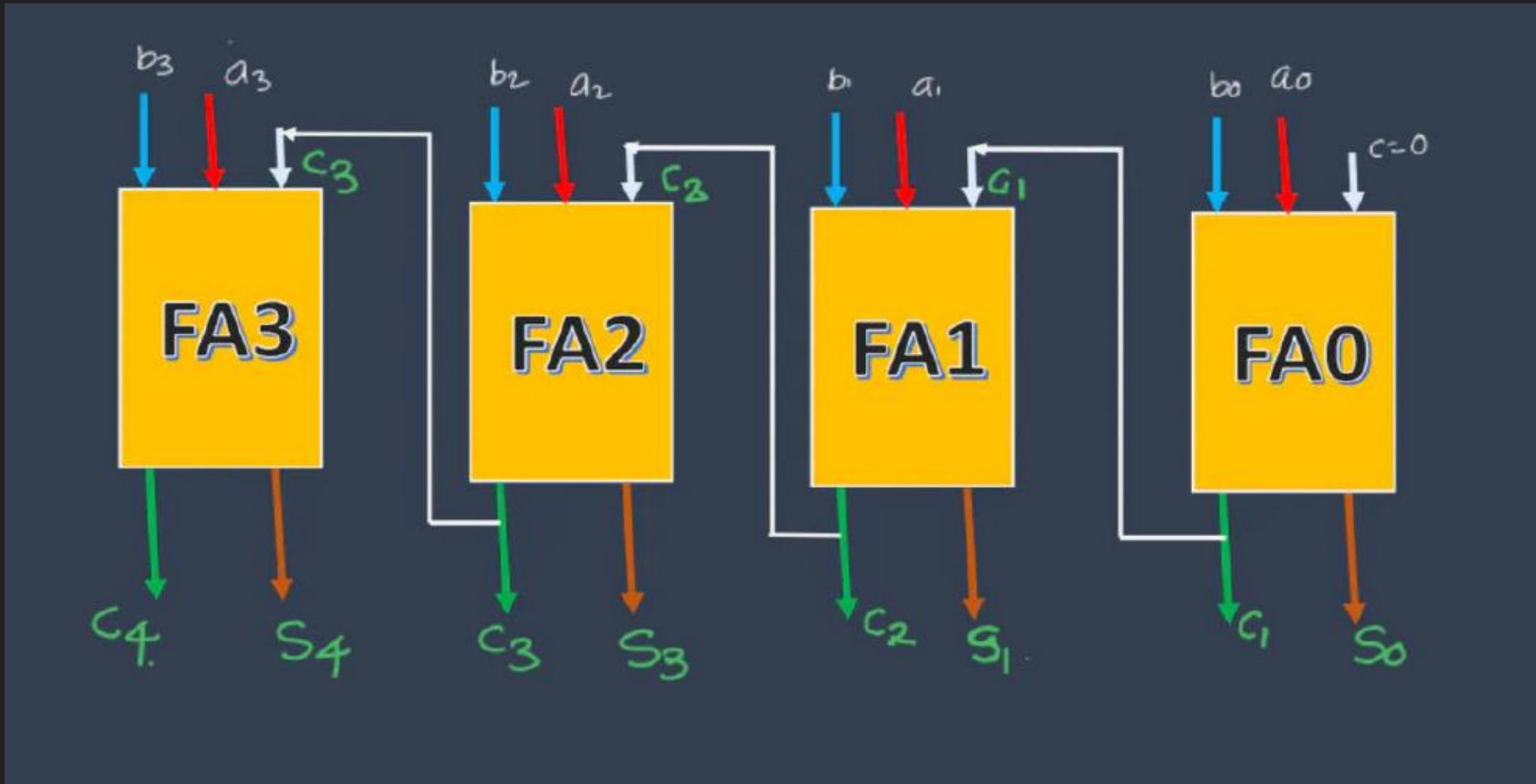
## FS

1. Logical expression for Difference =  $A \oplus B \oplus C$
2. Logical expression for Barrow =  $\bar{A}B + (\bar{A} \oplus B)C$
3. Minimum number of NAND Gates = 9
4. Minimum number of NOR Gates = 9



# Ripple Carry Adder (Parallel Adder)





## Note :

To implement 4-bit parallel adder

$$\longrightarrow 3 \text{ FA} + 1 \text{ HA}$$

$$\longrightarrow 4 \text{ FA}$$

$$\longrightarrow 7 \text{ HA} + 3 \text{-OR}$$

$$\longrightarrow 7 \text{-XOR} + 7 \text{-AND} + 3 \text{-OR}$$

$$1 \text{ FA} = 2 \text{ HA} + 1 \text{ OR}$$

$$1 \text{ HA} = 1 \text{-XOR} + 1 \text{-AND}$$

To implement n-bit parallel adder

$$\longrightarrow n \text{ - FA}$$

$$\longrightarrow (n-1) \text{ FA} + 1 \text{ - HA}$$

$$\longrightarrow (2n-1) \text{ HA} + (n-1) \text{-OR}$$

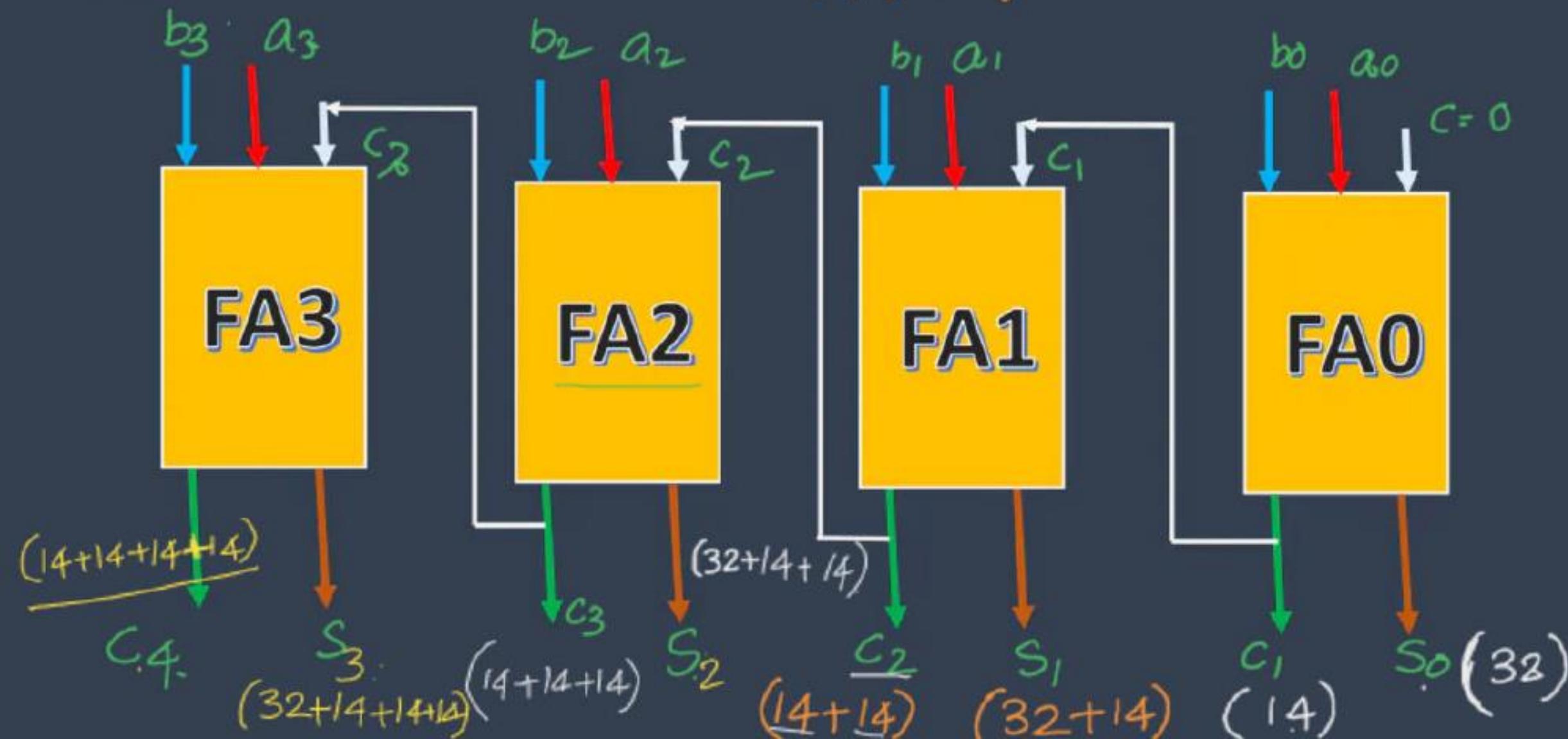
$$\longrightarrow (2n-1) \text{ XOR} + (2n-1) \text{ AND} + (n-1) \text{ OR}$$

# Delay Analysis

Case : 1  $(tpd)_{sum} > (tpd)_{carry}$

$$(tpd)_{sum} = 32\text{ns}$$

$$(tpd)_{carry} = 14\text{ns}$$



$$\text{Sum delay} = \underline{32 + 14 + 14 + 14} = 74 \text{ ns.}$$

$$\text{Carry delay} = \underline{14 + 14 + 14 + 14} = 56 \text{ ns.}$$

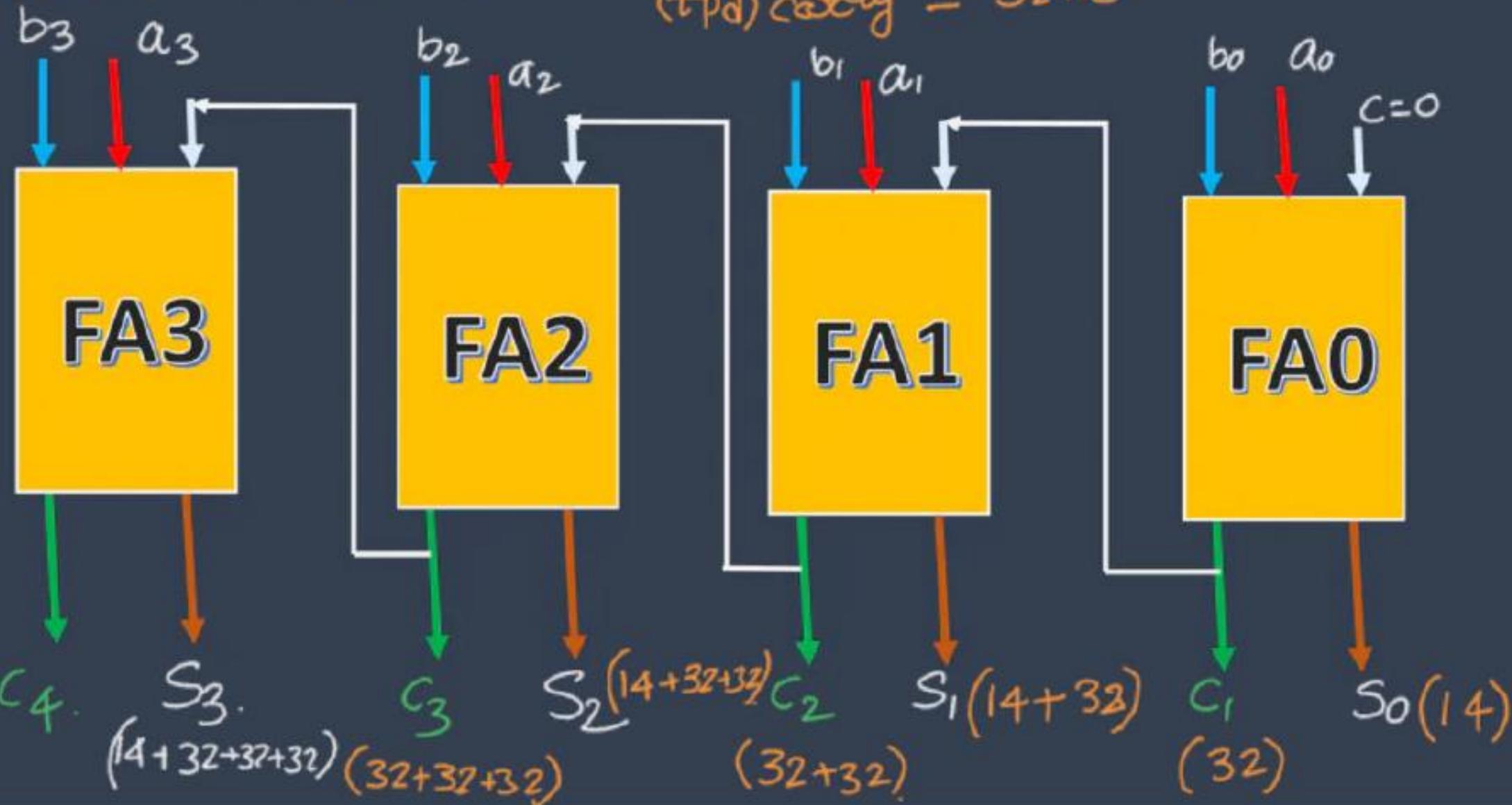
$$\begin{aligned}\text{over all delay} &= \max[\text{sum, carry}] \\ &= 74 \text{ ns.}\end{aligned}$$

# Delay Analysis

Case : 2  $(tpd)_{sum} < (tpd)_{carry}$

$$(tpd)_{sum} = 14 \text{ ns}$$

$$(tpd)_{carry} = 32 \text{ ns}$$



$$\text{Sum delay} = \underline{14} + \underline{32 + 32 + 32} = 110 \text{ ns}.$$

$$\text{carry delay} = \underline{\textcircled{32}} + \underline{32 + 32 + 32} = 128 \text{ ns}$$

$$\text{overall delay} = \max [\text{sum}, \text{carry}]$$

$$= \underline{\underline{128 \text{ ns}}}$$

In general for n- bit Parallel Adder

✓ Delay =  $(n-1) (t_{pd})_{carry} + \max[\text{sum, carry}]$ .

Q) A 16-bit RCA is realized using 16 identical FAs , if the  $(tpd)_{carry} = 12\text{ns}$  ,  $(tpd)_{sum} = 15\text{ns}$  , then the overall delay is ----- ns

$$\begin{aligned}\text{overall delay} &= (n-1)(tpd)_{carry} + \max[\text{sum}, \text{carry}] \\ &= \underline{\underline{195 \text{ ns}}}\end{aligned}$$

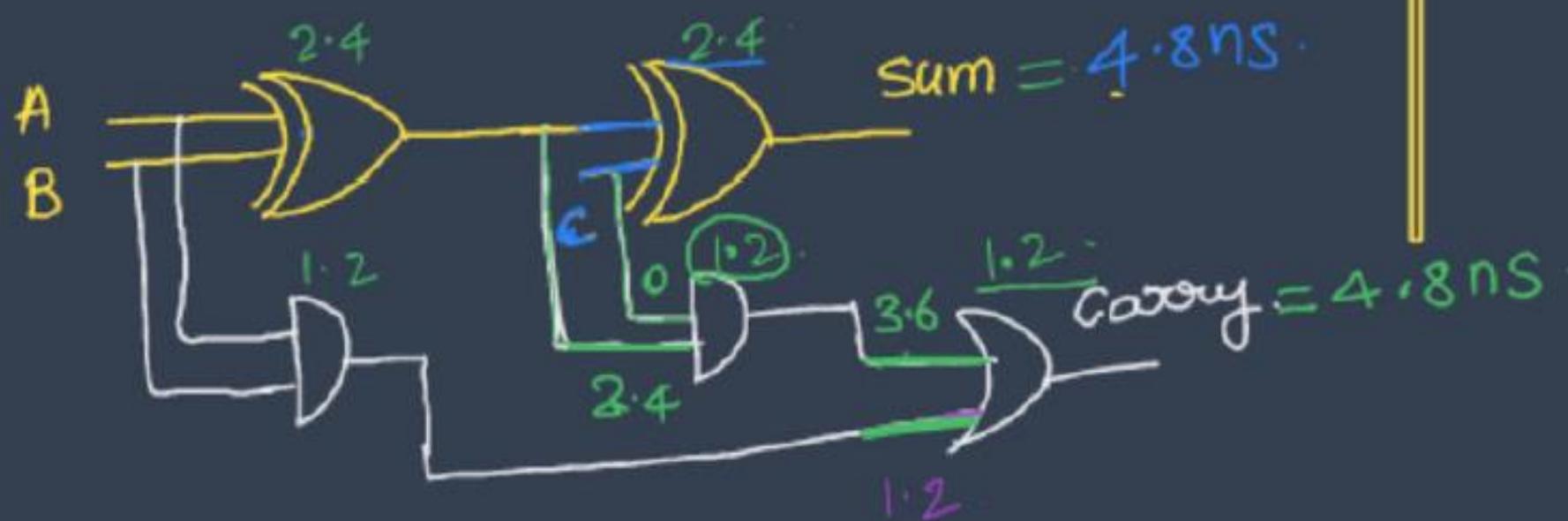
Q) A 4-bit RCA is implemented using 4FAs , if the propagation delay of XOR – Gate is twice the delay of AND/OR Gate , then the overall delay of 4- bit RCA if the delay of AND/OR Gate is  $1.2 \mu\text{sec}$

$$(t_{pd})_{\text{AND}} = (t_{pd})_{\text{OR}} = 1.2 \mu\text{s}$$

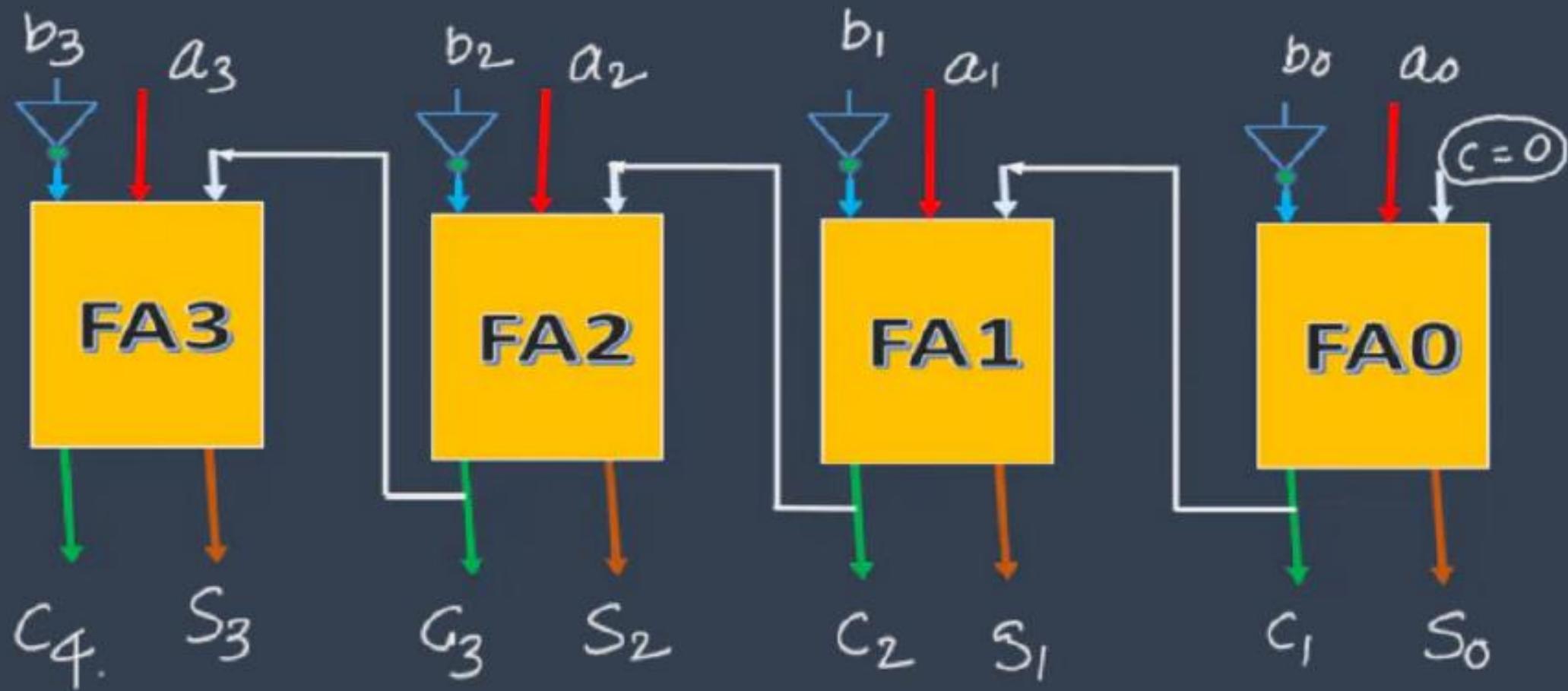
$$(t_{pd})_{\text{XOR}} = 2.4 \mu\text{s}$$

$$\text{Delay} = 4 \times 4.8$$

$$= 19.2 \mu\text{s}$$

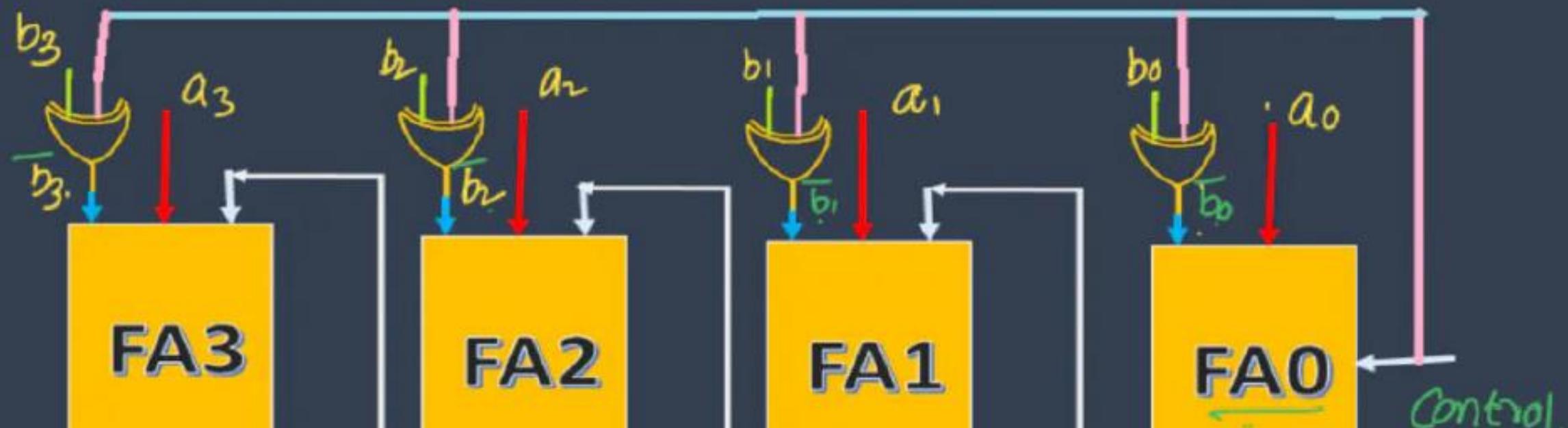


# Parallel Subtractor



# Parallel Adder/ Subtractor

$$a_0 + \underline{\overline{b}_0 + 1}$$



if control = 0

Parallel adder

if control = 1

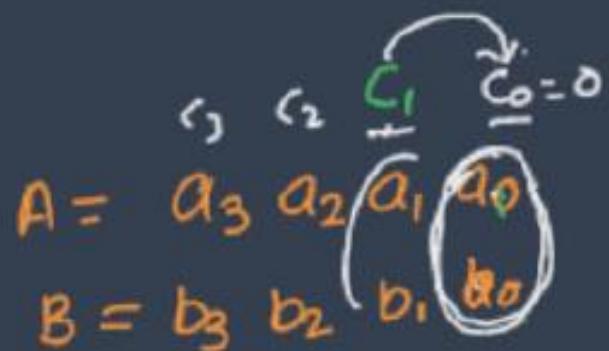
Parallel Subtractor

# Look Ahead Carry Adder

- In this adder ,the carry dependency of Ripple Carry Adder (RCA) is eliminated
- This is the fastest adder among all
- This adder have the maximum complexity

$$\text{Carry} = \underline{\underline{AB}} + \underline{\underline{(A \oplus B)C}}$$

$$\text{Sum} = A \oplus B \oplus C$$



$\checkmark P_i = A \oplus B \rightarrow$  Carry propagator

$\checkmark G_i = AB \rightarrow$  Carry generator.

$$S_i = P_i \oplus C_i$$

C<sub>i</sub>

$$S_0 = a_0 \oplus b_0 \oplus c_0$$

$$S_i = \underline{\underline{a_i \oplus b_i \oplus c_i}}$$

$$C_{i+1} = G_i + P_i C_i$$

$$P_0 = \underline{A_0 \oplus B_0}$$

$$P_1 = \underline{A_1 \oplus B_1}$$

$$P_2 = \underline{A_2 \oplus B_2}$$

$$P_3 = A_3 \oplus B_3$$

$$G_{10} = \underline{A_0 B_0}$$

$$G_{11} = A_1 B_1$$

$$G_{12} = A_2 B_2$$

$$G_{13} = A_3 B_3$$

$$S_0 = P_0 \oplus \underline{C_0}$$

$$S_1 = P_1 \oplus \underline{C_1}$$

$$S_2 = \textcircled{P_2} \oplus \underline{C_2}$$

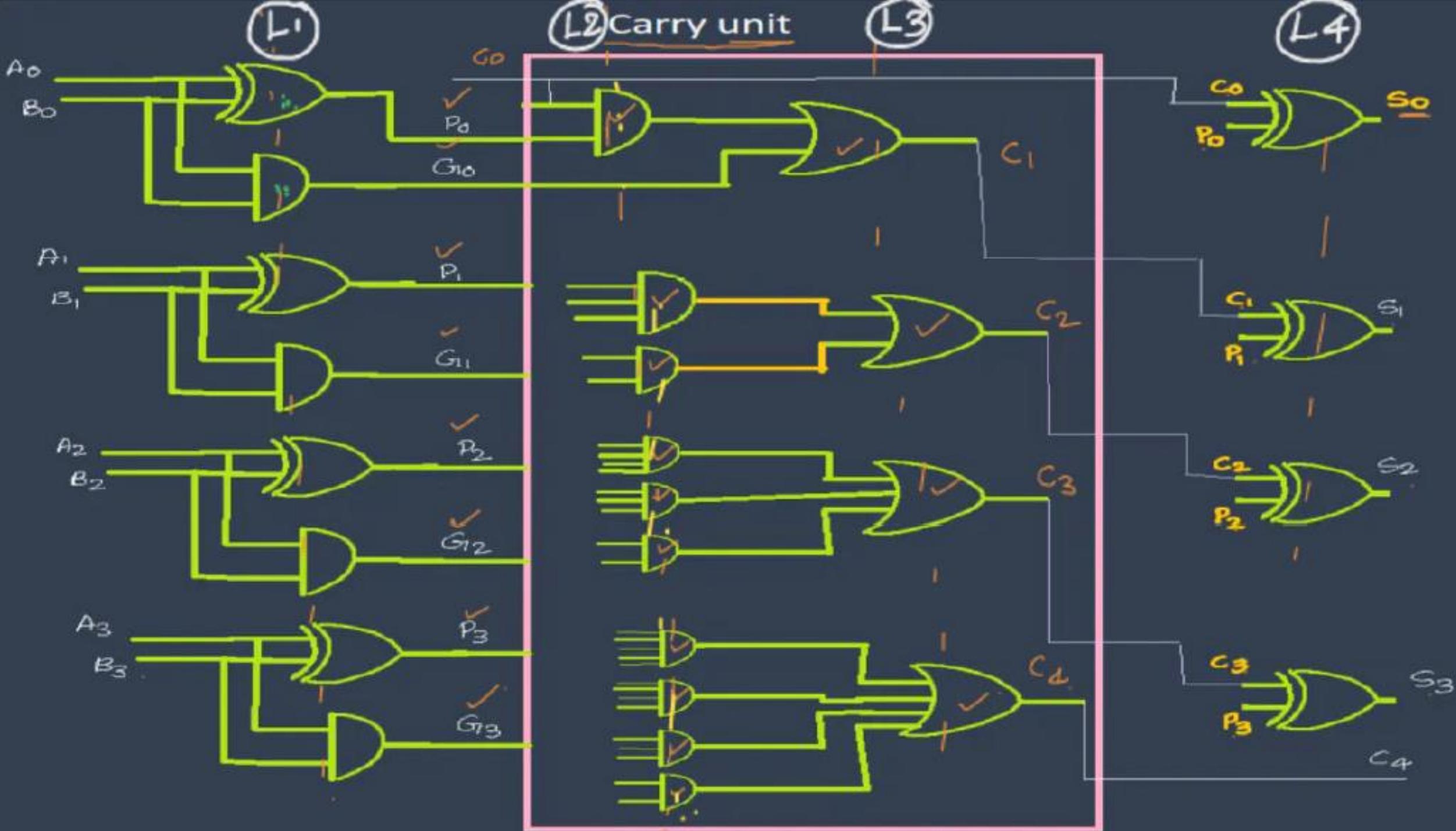
$$S_3 = P_3 \oplus C_3$$

$$C_1 = \underline{\underline{G_{10}}} + \underline{\underline{P_0 C_0}}$$

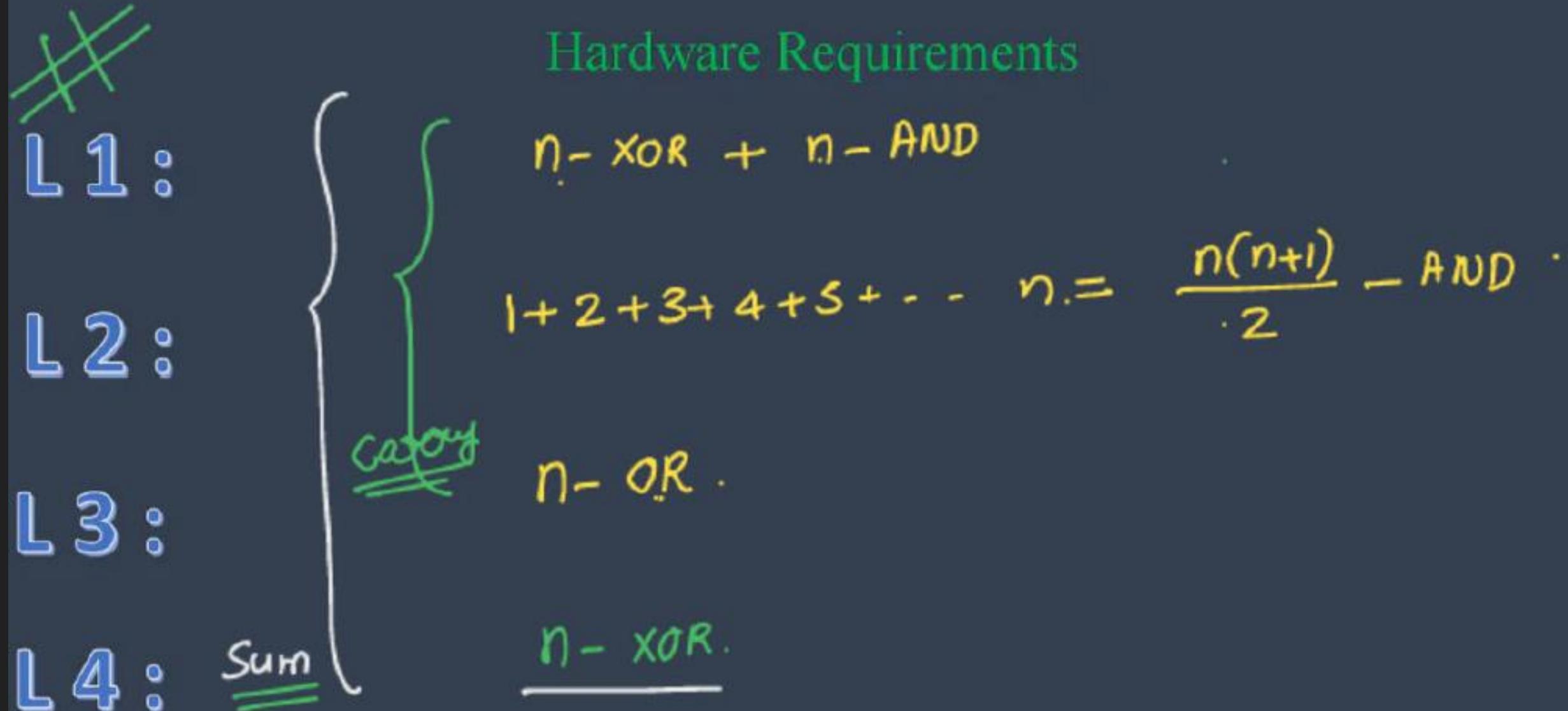
$$C_2 = G_{11} + P_1 C_1 = \underline{\underline{G_{11}}} + \underline{\underline{P_1 G_{10}}} + \underline{\underline{P_1 P_0 C_0}}$$

$$C_3 = G_{12} + P_2 C_2 = G_{12} + P_2 G_{11} + P_2 P_1 G_{10} + P_2 P_1 P_0 C_0$$

$$C_4 = G_{13} + P_3 C_3 = G_{13} + P_3 G_{12} + P_3 P_2 G_{11} + P_3 P_2 P_1 G_{10} + P_3 P_2 P_1 P_0 C_0$$



- In case of Carry look ahead adder for carry  $3\text{tpd}$  and for sum  $4\text{tpd}$
- Dependency of carry is eliminated



Total number of gates for carry =

$$= 3n + \frac{n(n+1)}{2} \quad \checkmark$$

Total number of gates for sum =

$$= 4n + \frac{n(n+1)}{2} \quad \checkmark$$

# Delay Analysis

$$\text{Carry} = \text{Max}[\text{xOR}, \text{AND}] + (t_{pd})_{\text{AND}} + (t_{pd})_{\text{xOR}}$$

$$\text{Sum} = \text{Max}[\text{xOR}, \text{AND}] + (t_{pd})_{\text{AND}} + (t_{pd})_{\text{xOR}} + (t_{pd})_{\text{xOR}}$$

Q) The minimum number of gates required for the implementation 4-bit look ahead carry generator are -----

$$\text{Carry} = 3n + \frac{n(n+1)}{2} = 22$$

$$\text{Sum} = 4n + \frac{n(n+1)}{2} = 26$$

Q) During the implementation of carry look ahead adder , if carry generator (  $G_i$  ) and carry propagator (  $P_i$  ) are available, then the minimum number of gates required are

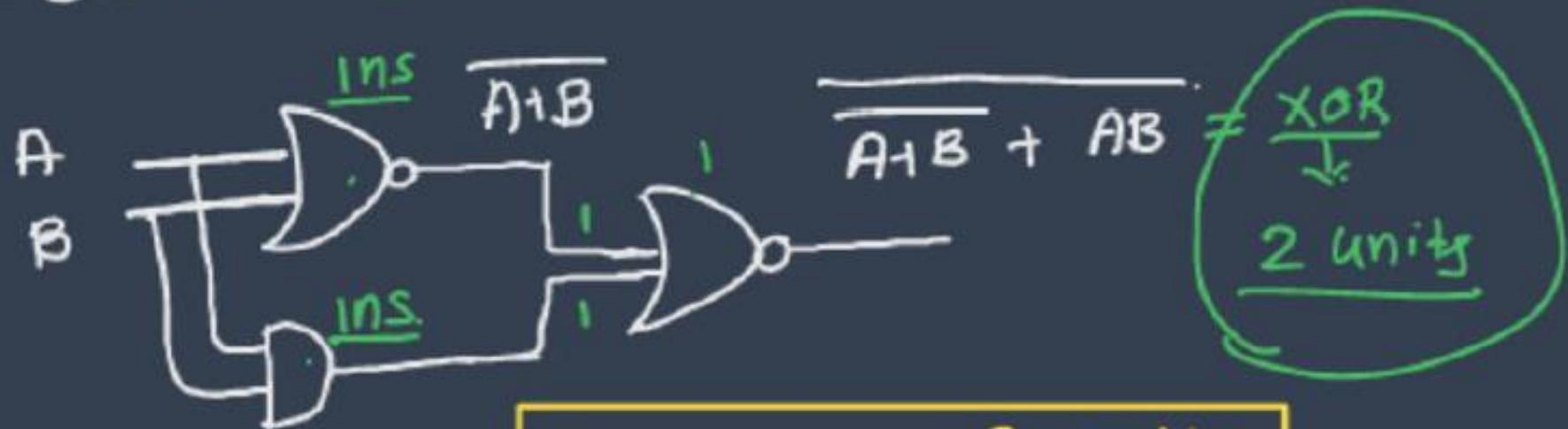
$$\text{Carry} = n + \frac{n(n+1)}{2}.$$

$$\text{Sum} = 2n + \frac{n(n+1)}{2}.$$

Q) In 4-bit look ahead carry adder is implemented with the following gates NOT , AND, OR , NAND , NOR calculate the minimum time required to generate sum if each gate has 1 unit delay.

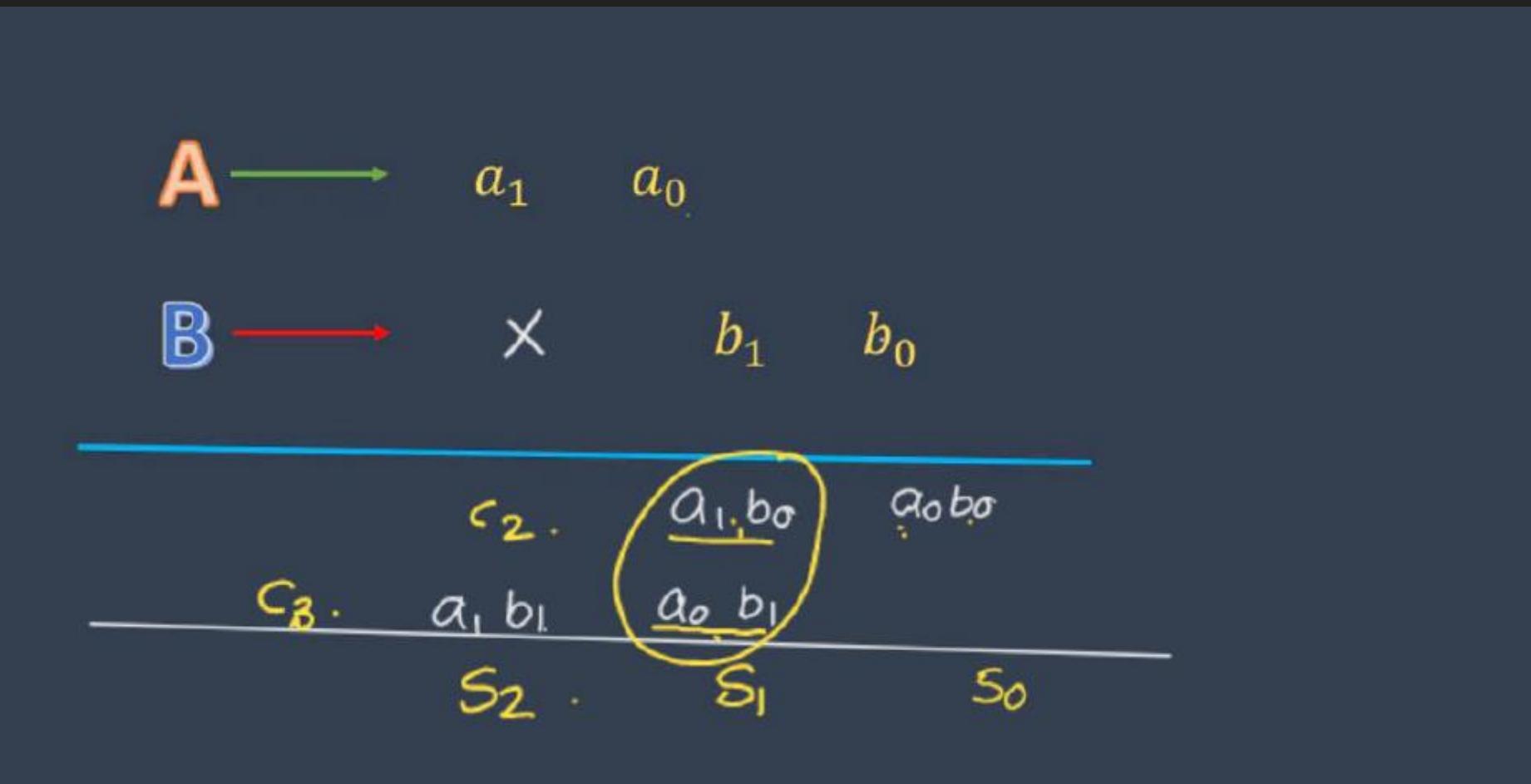
$$\text{Sum} = \max[\text{xOR}, \underline{\text{AND}}] + (t_{pd})_{\text{NAND}} + (t_{pd})_{\text{OR}} + (t_{pd})_{\text{xOR}}$$

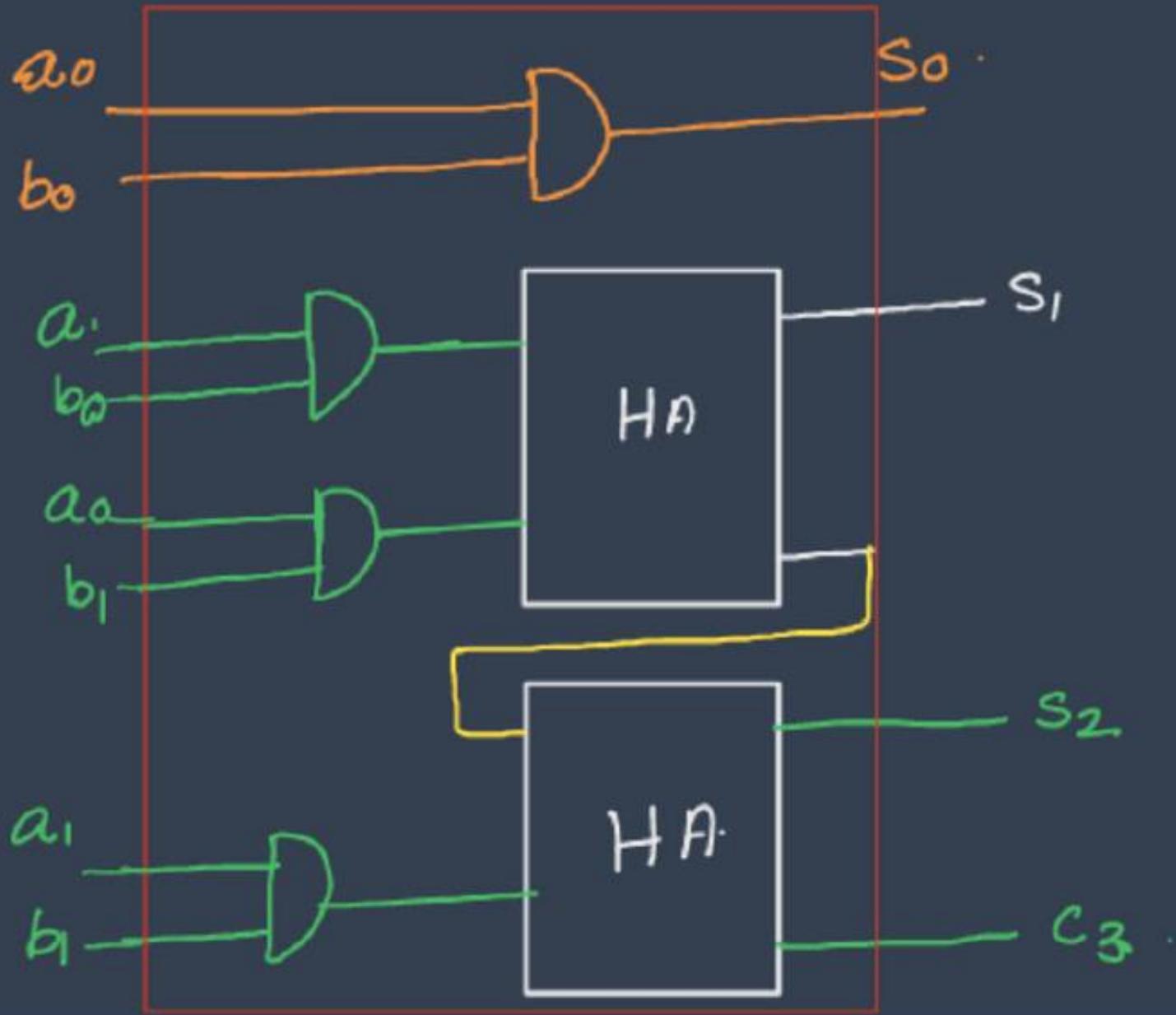
$$A \oplus B = \overline{\overline{A} \overline{B}} = \overline{\overline{A} \overline{B} + AB} = \overline{\overline{A+B} + AB}$$



$$\boxed{\text{Sum} = 6 \text{ units.}}$$

# Binary Multiplier





$$\begin{array}{cccc}
 \textcolor{brown}{A} & \longrightarrow & a_2 & a_1 & a_0 \\
 \\[10pt]
 \textcolor{blue}{B} & \longrightarrow & b_1 & b_0 \\
 \\[10pt]
 \hline
 & a_2 b_0 & \textcircled{a_1 b_0} & a_0 b_0 \\
 & b_1 a_1 & \textcircled{b_1 \bar{a}_0} & \\
 \hline
 c_4 & s_3 & s_2 & s_1 & s_0
 \end{array}$$

Number of AND gates required =  $m \times n$

Number of Adders required =  $m+n-2$

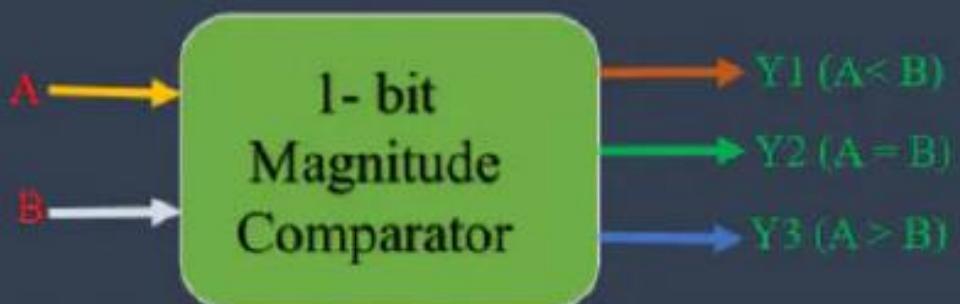
$m \longrightarrow$  number of bits in A

$n \longrightarrow$  number of bits in B

# Magnitude Comparator

To compare the magnitude of two binary numbers

# 1-bit magnitude comparator



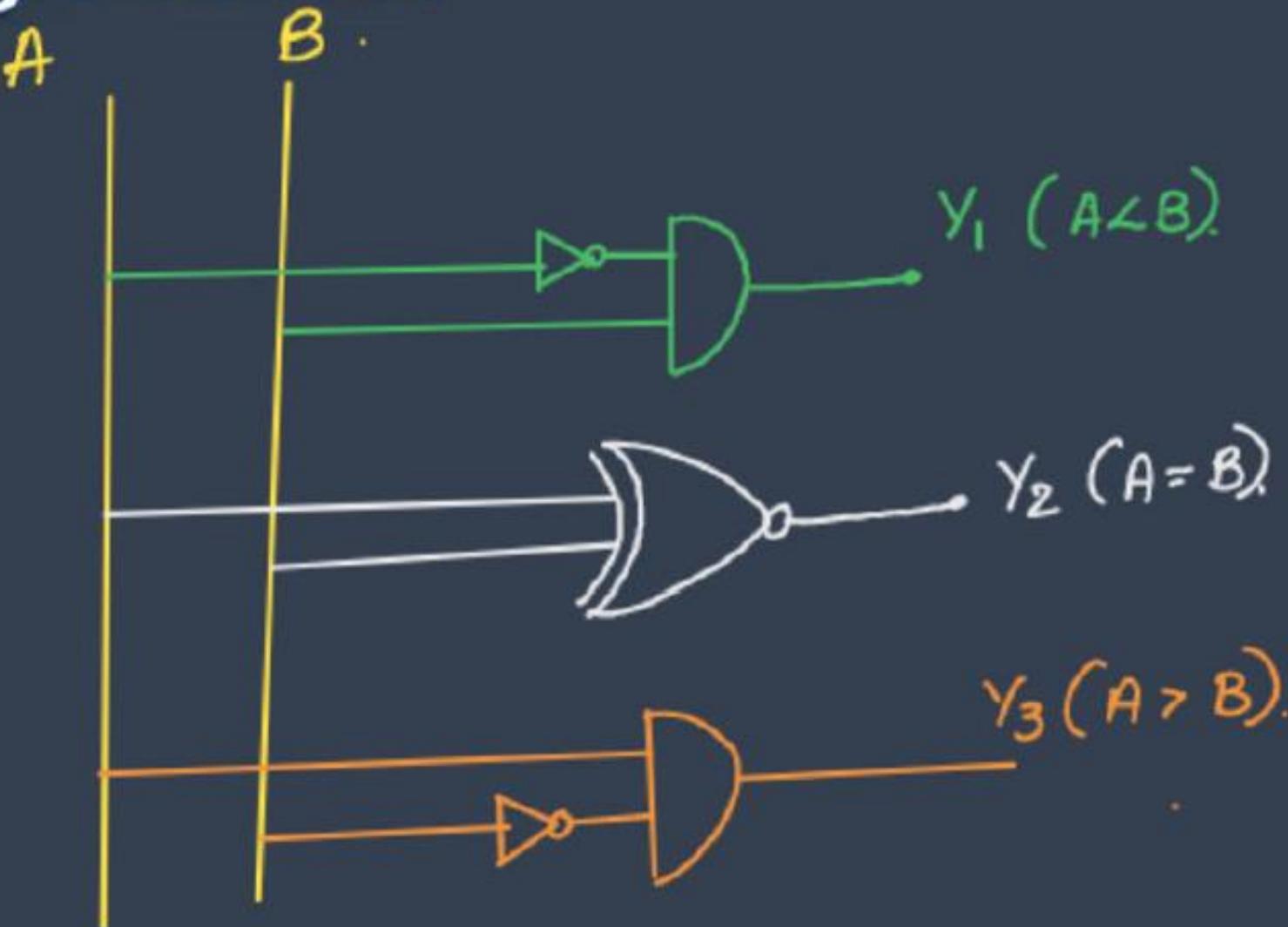
A	B	$Y_1$ (A < B)	$Y_2$ (A = B)	$Y_3$ (A > B)
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

$$Y_1 (A < B) = \overline{A}B$$

$$Y_2 (A = B) = \overline{A}\overline{B} + AB \\ = A \oplus B$$

$$Y_3 (A > B) = A\overline{B}$$

# Logic circuit



# 1- Bit magnitude Comparator

Total number of input combinations = 4

Lesser than combinations = 1

Greater than combinations = 1

Equal combinations = 2

# 2-bit Magnitude Comparator



A	B	$Y_1$ (A < B)	$Y_2$ (A = B)	$Y_3$ (A > B)
00	00	0	1	0
00	01	1	0	0
00	10	1	0	0
00	11	1	0	0
01	00	0	0	1
01	01	0	1	0
01	10	1	0	0
01	11	1	0	0
10	00	0	0	1
10	01	0	0	1
10	10	0	1	0
10	11	1	0	0
11	00	0	0	1
11	01	0	0	1
11	10	0	0	1
11	11	0	1	0

For 2-bit Magnitude Comparator

$$Y_1 (A < B) = \underline{\bar{a}_1 b_1} + (\underline{\bar{a}_1 \odot b_1}) \underline{\bar{a}_0 b_0}$$

$$Y_2 (A = B) = (\underline{\bar{a}_1 \odot b_1}) (\underline{\bar{a}_0 \odot b_0})$$

$$Y_3 (A > B) = \underline{a_1 \bar{b}_1} + (\underline{a_1 \odot b_1}) \underline{a_0 \bar{b}_0}$$

# For n- bit Magnitude Comparator

Total number of input combinations =  $2^{2n}$

Lesser than combinations =  $\frac{2^{2n} - 2^n}{2}$

Greater than combinations =  $\frac{2^{2n} - 2^n}{2}$

Equal combinations =  $2^n$

For 3-bit Magnitude Comparator

$$A = a_2 \ a_1 \ a_0$$

$$B = b_2 \ b_1 \ b_0$$

$$Y_1 (A < B) = \overline{a}_2 b_2 + (a_2 \odot b_2) \overline{a}_1 b_1 + (a_2 \odot b_2) (a_1 \odot b_1) \overline{a}_0 b_0$$

$$Y_2 (A = B) = (a_2 \odot b_2) (a_1 \odot b_1) (a_0 \odot b_0)$$

$$Y_3 (A > B) = a_2 \overline{b}_2 + (a_2 \odot b_2) a_1 \overline{b}_1 + (a_2 \odot b_2) (a_1 \odot b_1) a_0 \overline{b}_0$$

For 4-bit Magnitude Comparator

$$A = a_3 \ a_2 \ a_1 \ a_0$$
$$B = b_3 \ b_2 \ b_1 \ b_0$$

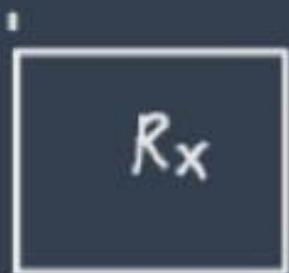
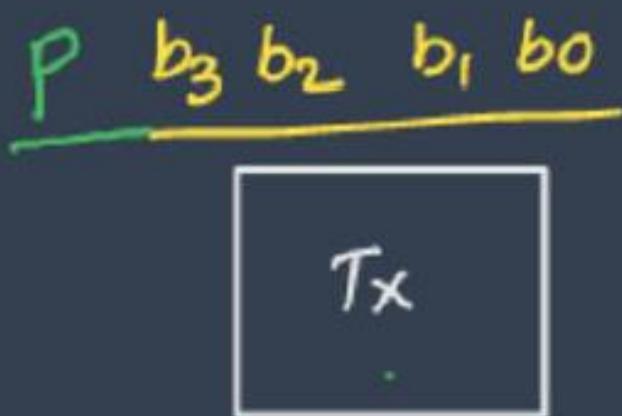
$$Y_1 (A < B) = \overline{a}_3 b_3 + (a_3 \oplus b_3)(\overline{a}_2 b_2) + (a_3 \oplus b_3)(a_2 \oplus b_2)(\overline{a}_1 b_1) \\ + (a_3 \oplus b_3)(a_2 \oplus b_2)(a_1 \oplus b_1)(\overline{a}_0 b_0).$$

$$Y_2 (A = B) = \\ = (a_3 \oplus b_3)(a_2 \oplus b_2)(a_1 \oplus b_1)(a_0 \oplus b_0).$$

$$Y_3 (A > B) = a_3 \overline{b}_3 + (a_3 \oplus b_3)(a_2 \overline{b}_2) + (a_3 \oplus b_3)(a_2 \oplus b_2)(\overline{a}_1 b_1) \\ + (a_3 \oplus b_3)(a_2 \oplus b_2)(a_1 \oplus b_1)(a_0 \overline{b}_0)$$

# PARITY BIT

A parity bit is used for the purpose of detecting errors during transmission of binary information. A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker.



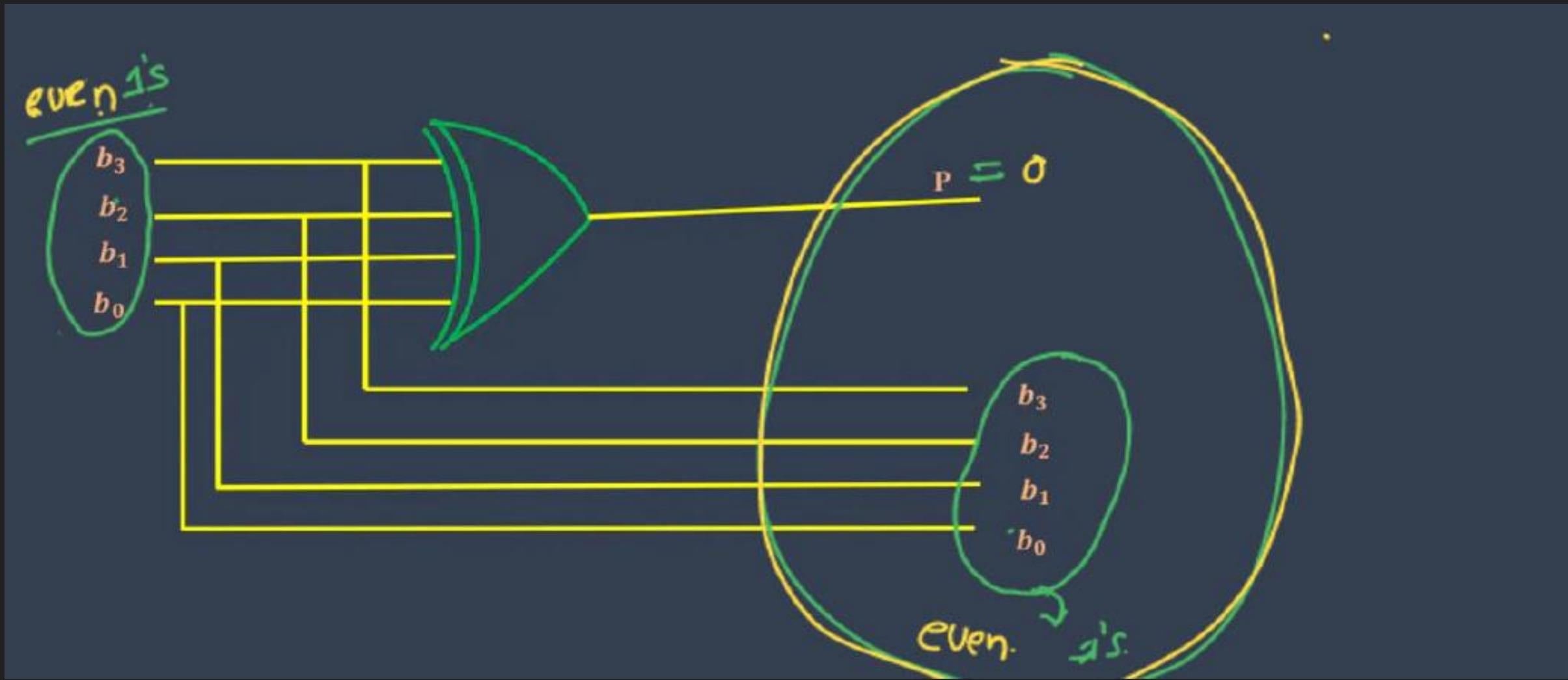
1. even parity.
2. odd parity

# Even parity

In case of even parity , the added parity bit will make the total number of 1's an even number .

3- bit message	Message with even parity	
	message	Parity
0 0 0	0 0 0	0
0 0 1	0 0 1	1
0 1 0	0 1 0	1
0 1 1	0 1 1	0
1 0 0	1 0 0	1
1 0 1	1 0 1	0
1 1 0	1 1 0	0
1 1 1	1 1 1	1.

# Even Parity Generator

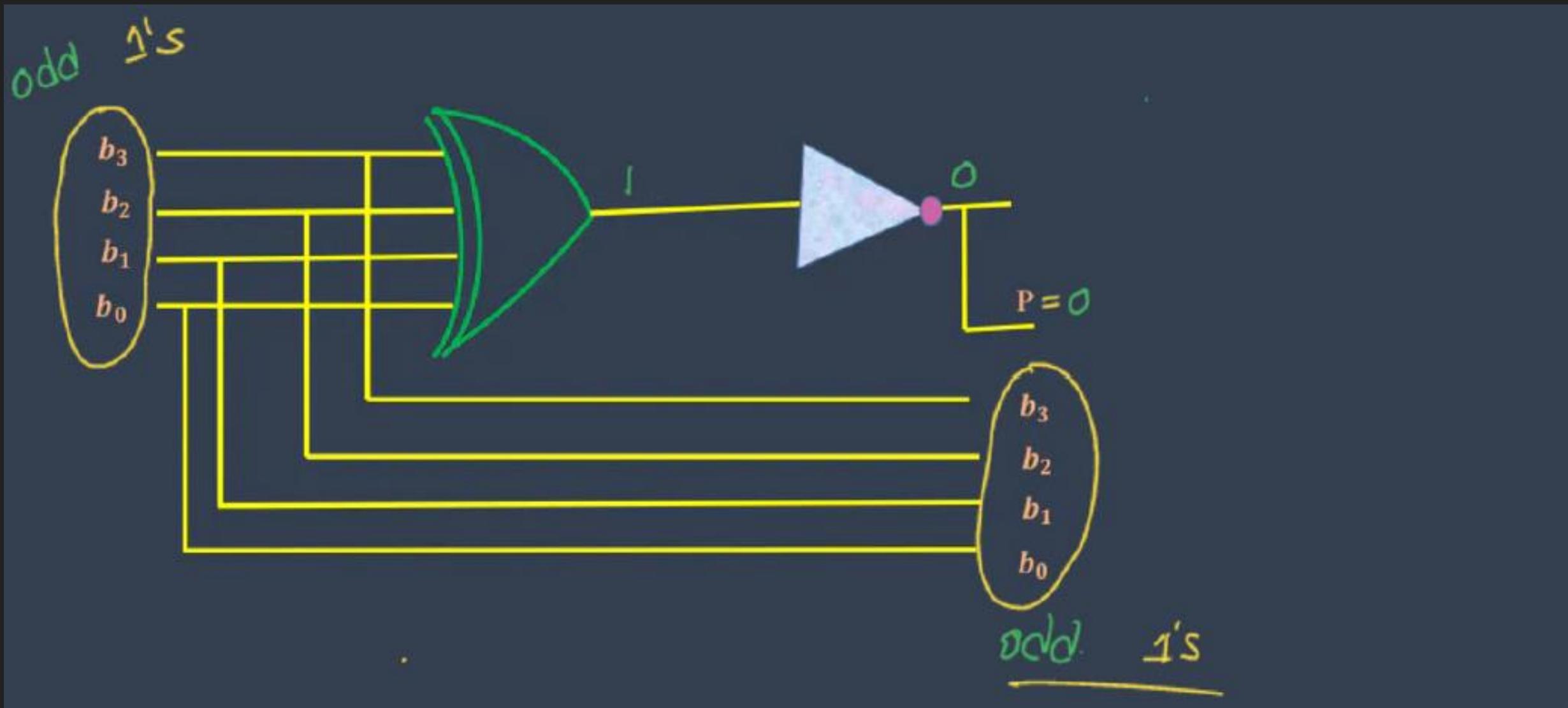


# Odd parity

In case of odd parity , the added parity bit will make the total number of 1's an odd number .

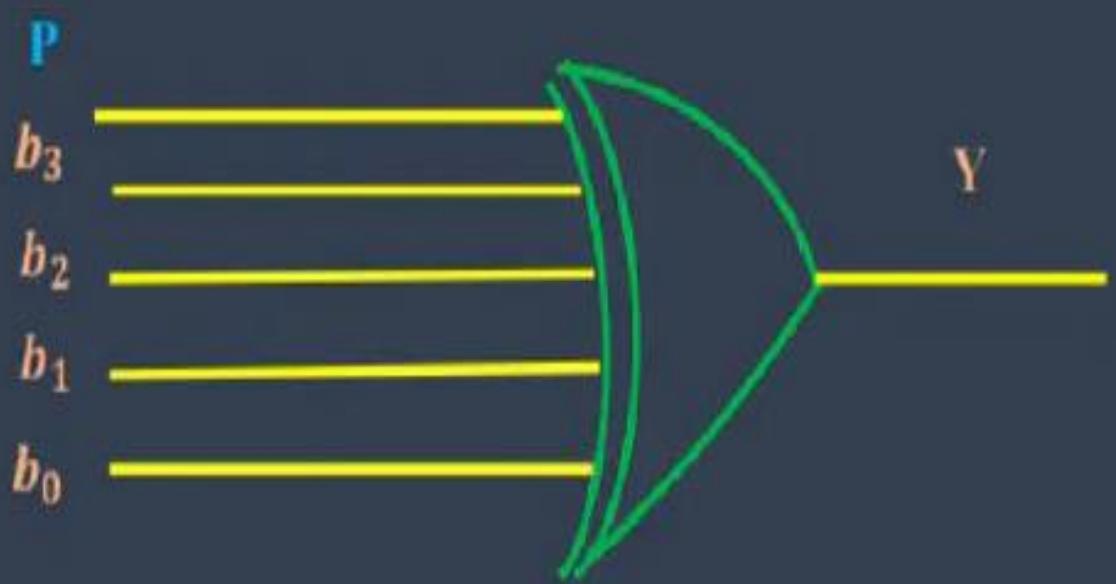
3- bit message	Message with odd parity	
	message	Parity
000	000	1
001	001	0
010	010	0
011	011	1
100	100	0
101	101	1
110	110	1
111	111	0

# Even Parity Generator



# Parity Checker

"Hamming code"



$Y=0 \rightarrow$  even parity

$=1 \rightarrow$  odd parity

# Hazards

Hazards are unwanted transients that occurs due to unequal propagation delay of the paths .

# Hazards



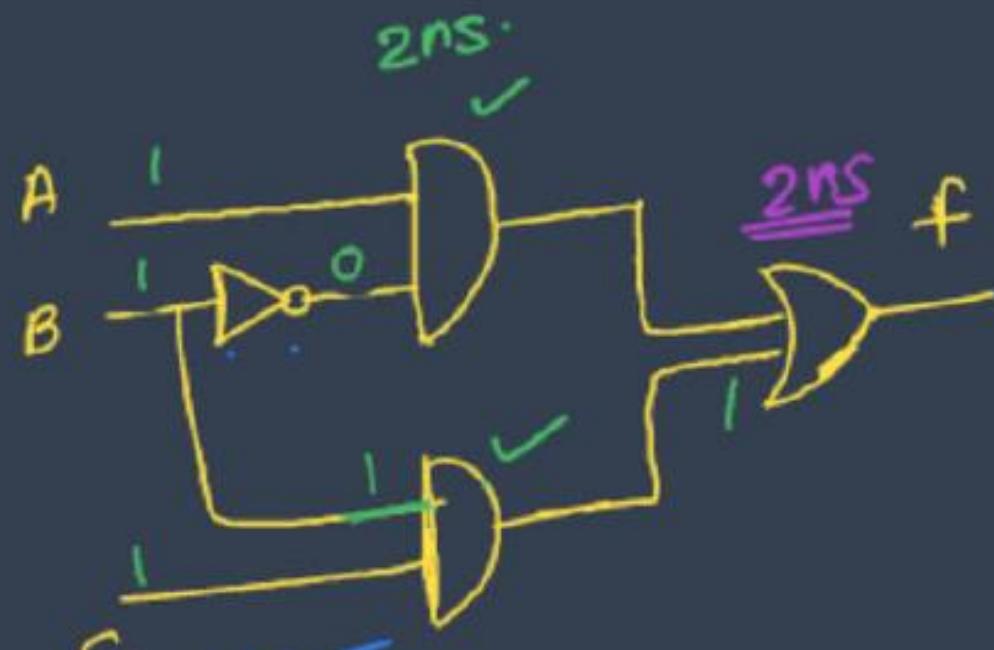
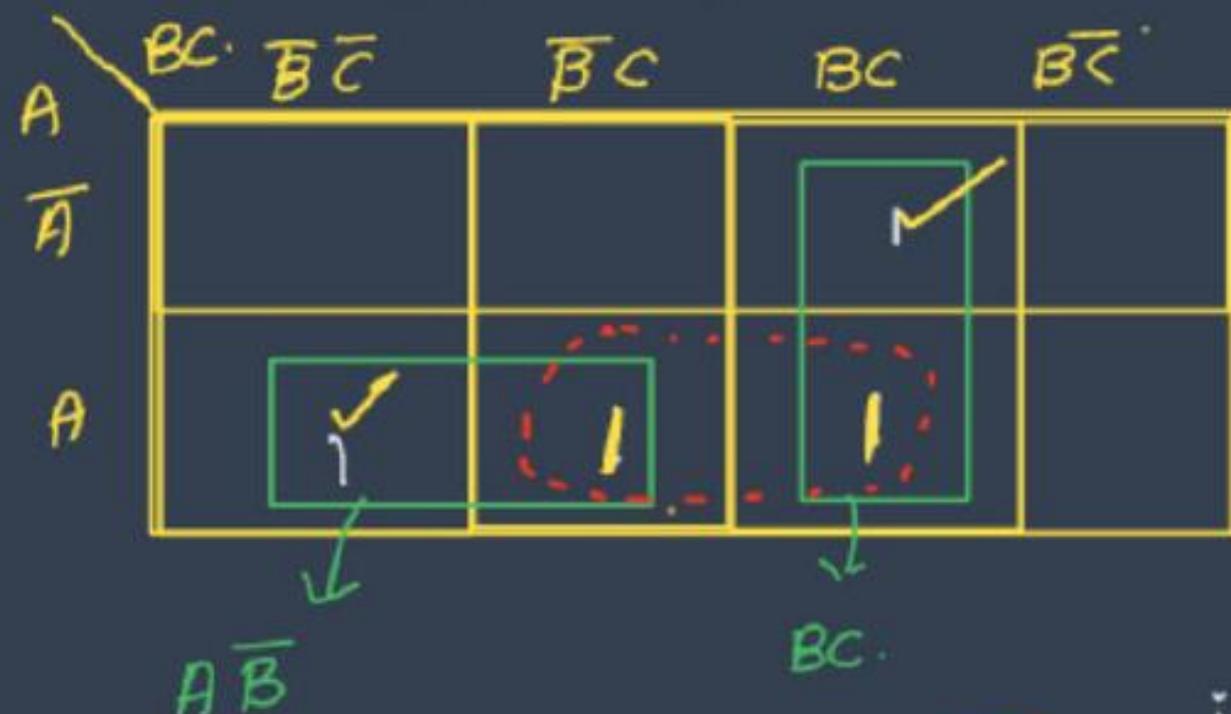
➤ Static 1 Hazards will occurs in two level AND- OR circuit (SOP)

**Static 1 Hazard**

➤ Static 0 Hazards will occurs in two level OR- AND circuit (POS)

**Static 0 Hazard**

Q)  $F(A, B, C) = \sum(3, 4, 5, 6)$  f



$$f = A\bar{B} + BC + AC$$

$i-f$   $A = C = 1$

$B = 0$

$f = 1$

$B = 1$

$f = 1$



$A=1$

$\checkmark B$

$\checkmark$

$C=1$

$\bar{B}$

2

$A\bar{B}$

4

$BC$

2

Static - I Hazard

$f_1$

4

6

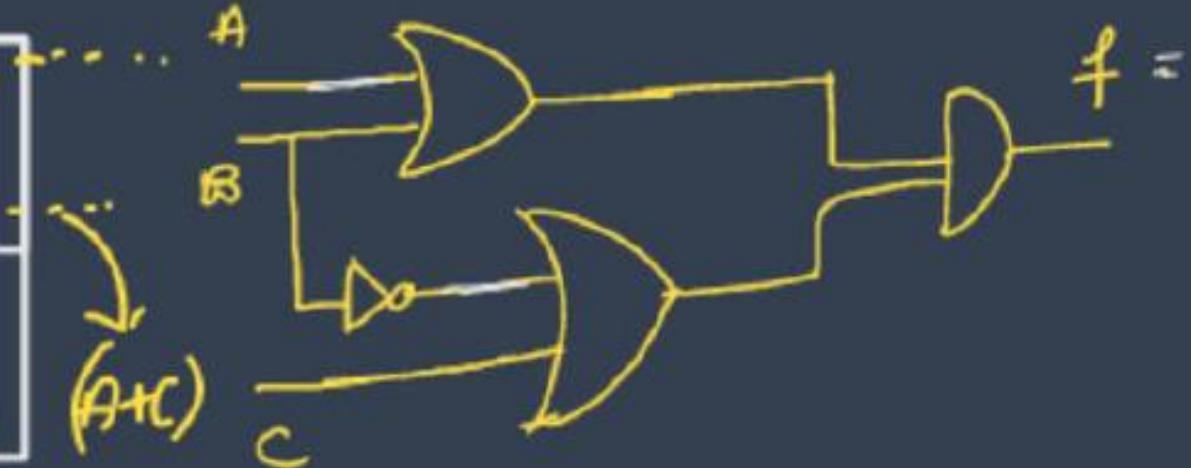
$AC$

$f_1 = 1$



$$Q) F(A, B, C) = \prod M(0, 1, 2, 6)$$

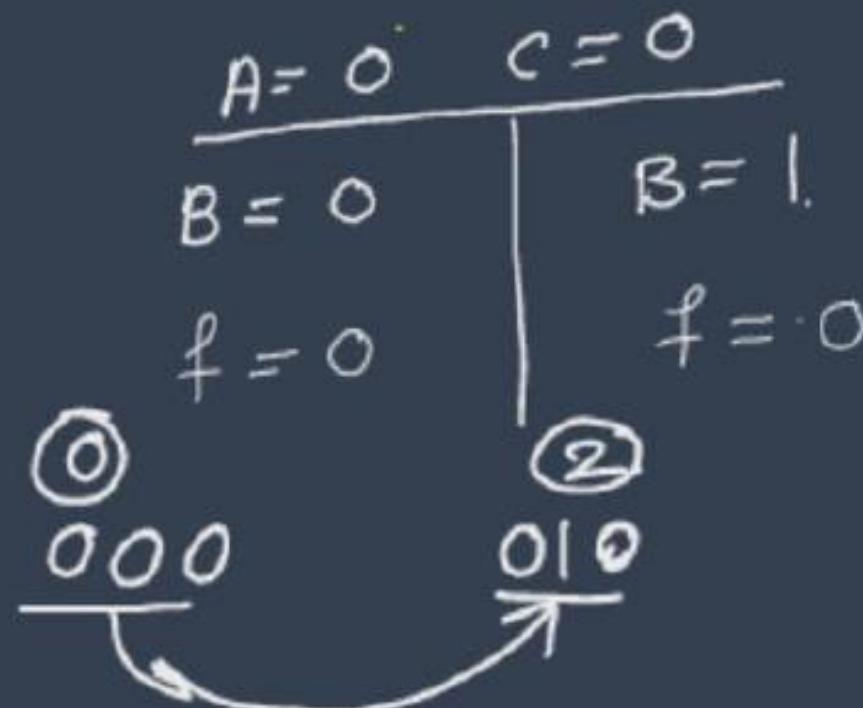
	$BC$	$B+C$	$B \cdot \bar{C}$	$\bar{B} + \bar{C}$
$A$	00	01	11	10
$\bar{A}$	10	00	00	00
$(A+B)$	11	11	10	10
$\bar{B}+C$	01	10	00	11



$$(A+B)$$

$$f_1 = \underline{(A+B)} (\bar{B}+C)$$

$$f_2 = (A+B) (\bar{B}+C) (A+C)$$



$A = 0$

$B$

$C = 0$

$(A + B)$

$\bar{B}$

$(\bar{B} + C)$

$f_1$

$(A + C)$

$f = 0$

2

2

4

4

6

Static - 0 Hazard

➤ Static hazards can be eliminated by adding the redundant term

# Multiplexer (MUX)

- Data selector
- Many to one
- Universal logic gate
- Parallel to serial converter

## The general structure of a Mux

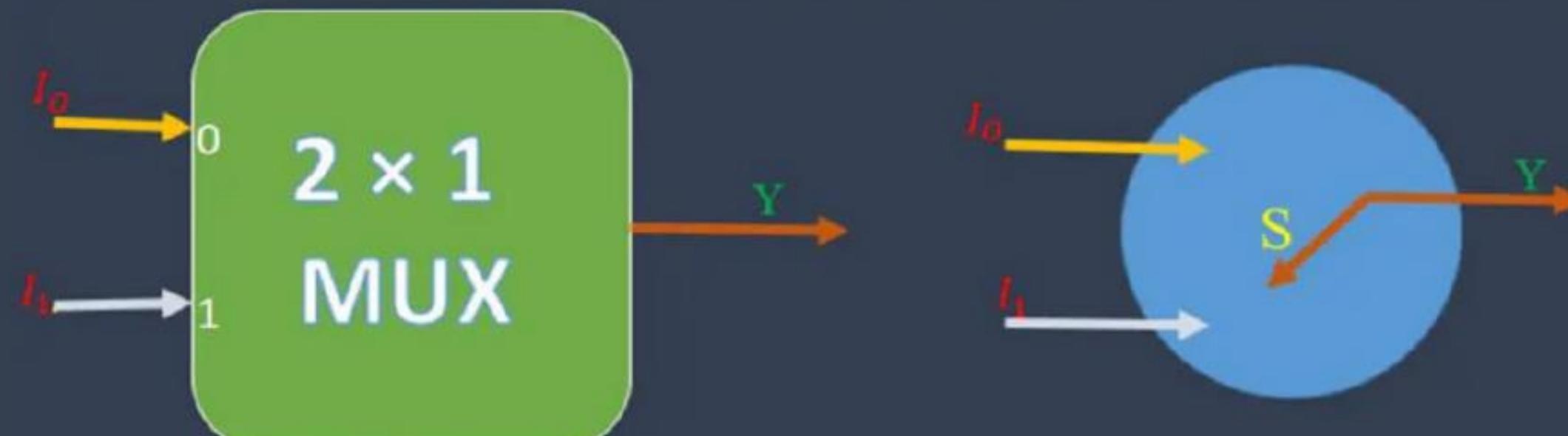
$$2^n \times 1$$

$2^n$  -----> number of data inputs

$n$  -----> number of select inputs

$1$  -----> number of outputs

# $2 \times 1$ MUX

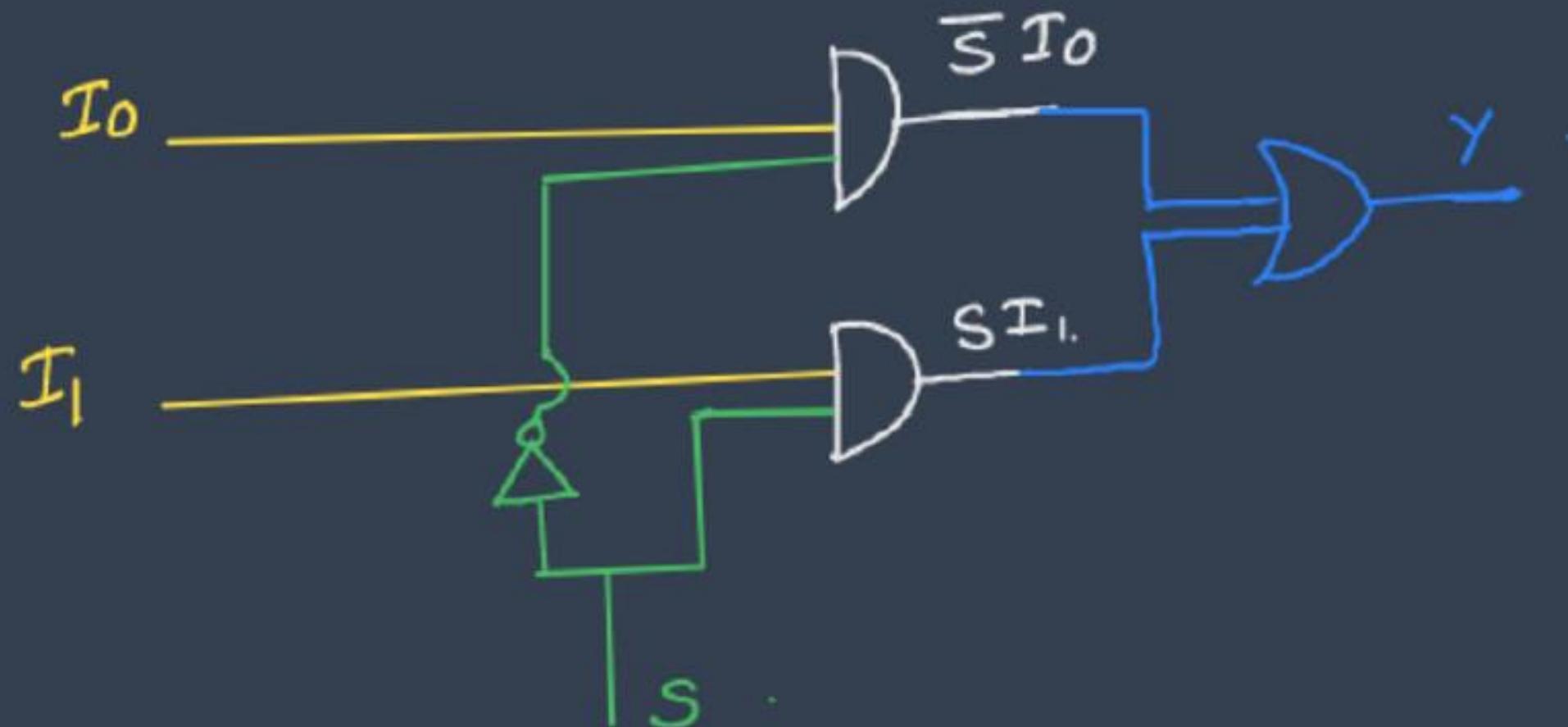


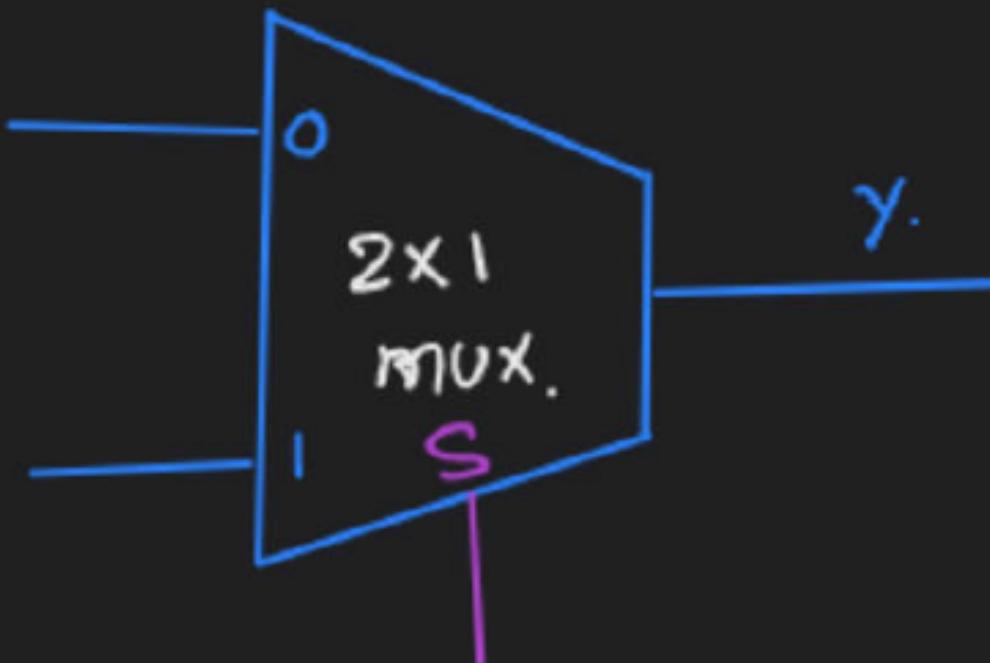
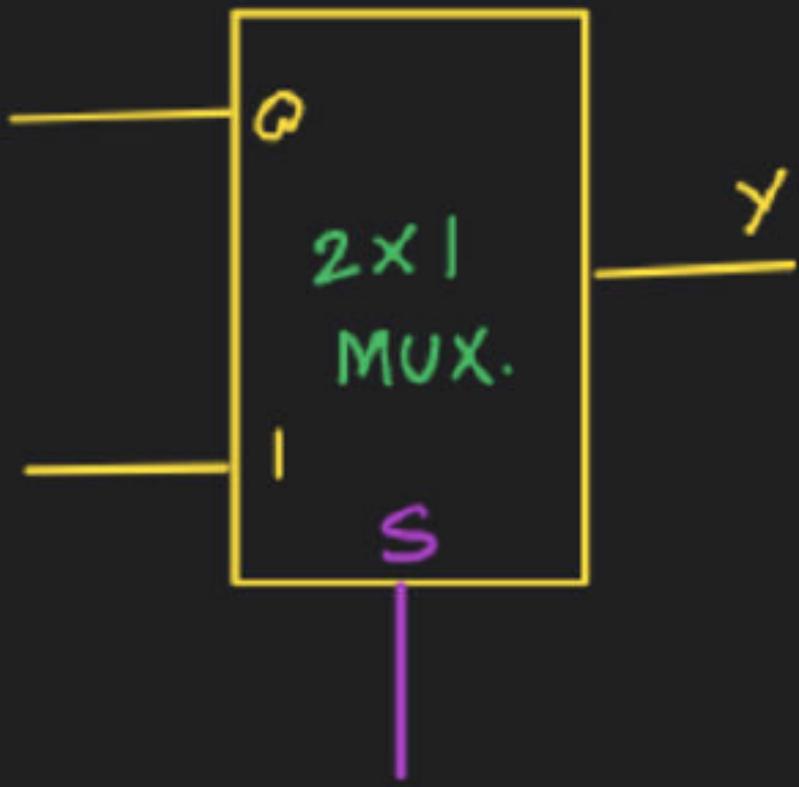
$$Y = \bar{S} I_0 + S I_1$$

$S$	$Y$
0	$I_0$
1	$I_1$

# Logic circuit

$$Y = \overline{S} I_0 + S I_1$$





# $4 \times 1$ MUX



$S_1$	$S_0$	$Y$
0	0	$I_0$
0	1	$I_1$
1	0	$I_2$
1	1	$I_3$

$$y = \overline{S_1} \overline{S_0} I_0 + \overline{S_1} S_0 I_1 + S_1 \overline{S_0} I_2 + S_1 S_0 I_3$$

Q) Find the minterms



$$Y = \underline{\bar{A}\bar{B}\bar{C}(0)} + \bar{A}\bar{B}C(1) + \bar{A}B\bar{C}(1)$$
$$+ \underline{\bar{A}BC(0)} + A\bar{B}\bar{C}(1) + \underline{A\bar{B}C(0)}$$
$$+ AB\bar{C}(1) + ABC(1)$$
$$Y = \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + ABC$$
$$Y = \sum m(1, 2, 4, 6, 7)$$

Q) Find the logic expression

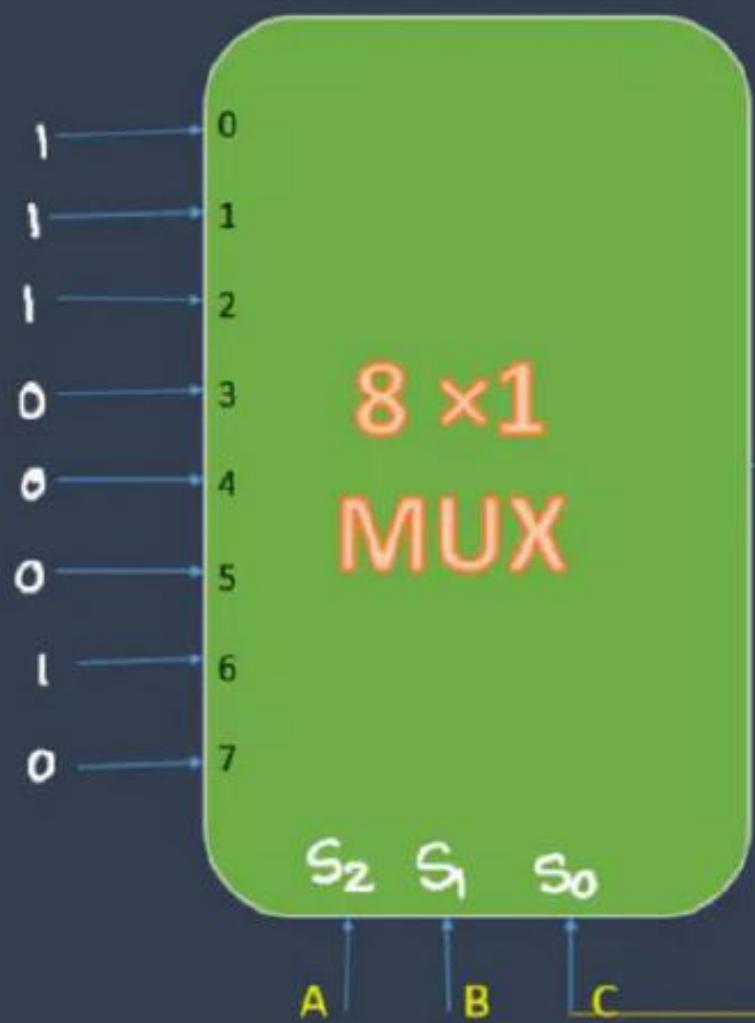


$$Y = \overline{P} \overline{Q} \cdot \bar{R} + \overline{P} Q \cdot \bar{\bar{R}} + P \bar{Q} \cdot \bar{\bar{\bar{R}}} + P Q \cdot \bar{\bar{\bar{\bar{R}}}} .$$

$$Y = \sum m(1, 2, 4, 7)$$

$$Y = P \oplus Q \oplus R .$$

Q) Find the logic expression



$$X = \sum m(0_1, 1_1, 2_1, 6_1)$$

$$X = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + AB\overline{C}$$

$$Y = X + \overline{C}$$

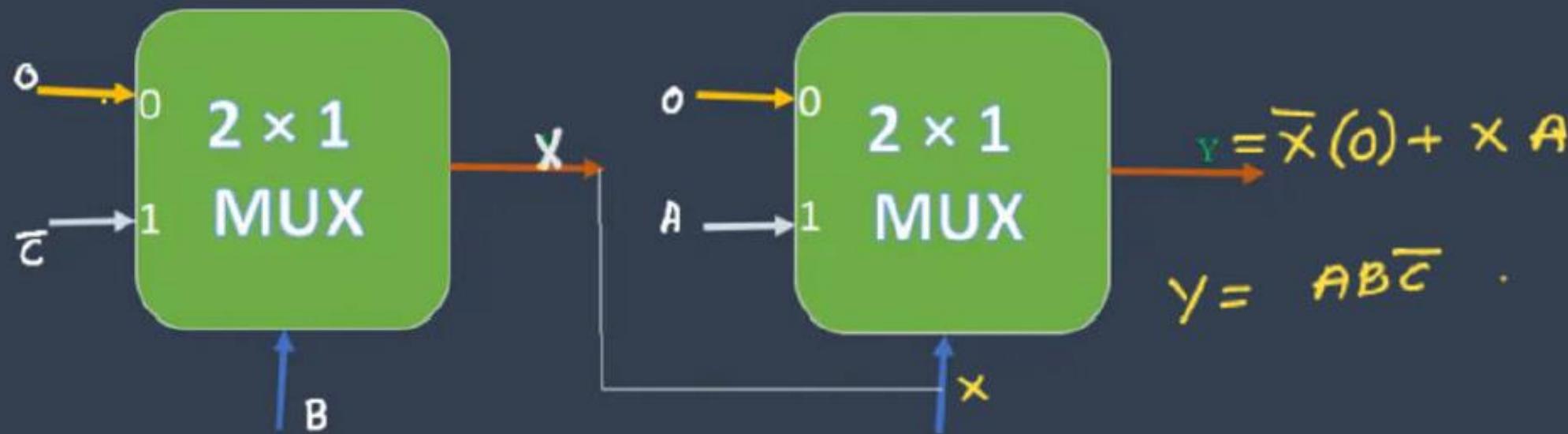
$$Y = \overline{A}\overline{B}\overline{C} + \underline{\overline{A}\overline{B}C} + \overline{A}B\overline{C} + AB\overline{C} + \overline{C}$$

$$Y = \overline{C} \left[ \underline{\overline{A}\overline{B}} + \underline{\overline{A}B} + \underline{AB} + \underline{!} \right] + \overline{A}\overline{B}C$$

$$Y = \overline{C} + \overline{A}\overline{B}C = (\overline{C} + \overline{A}\overline{B})(\overline{C} + C)$$

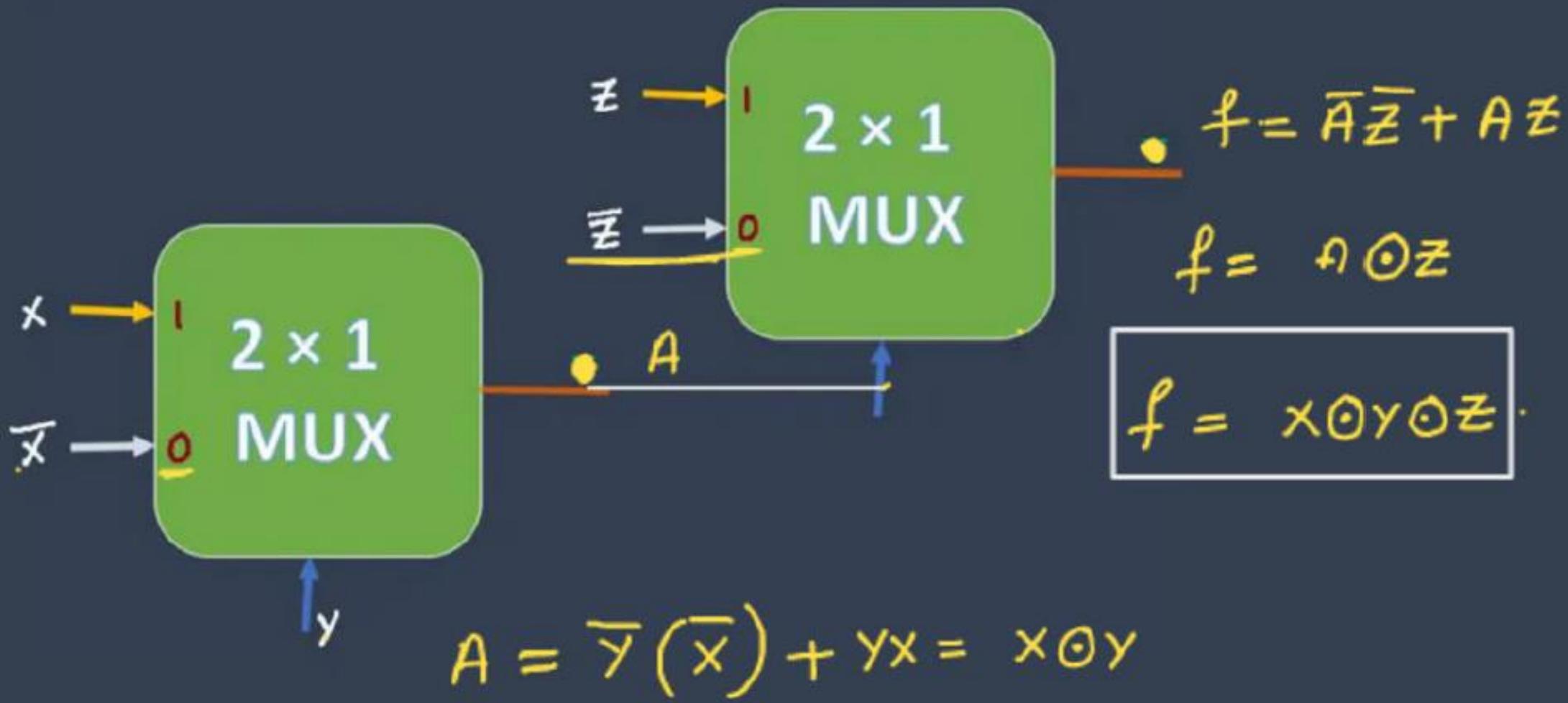
$$Y = \overline{A}\overline{B} + \overline{C}$$

Q) Find the logic expression

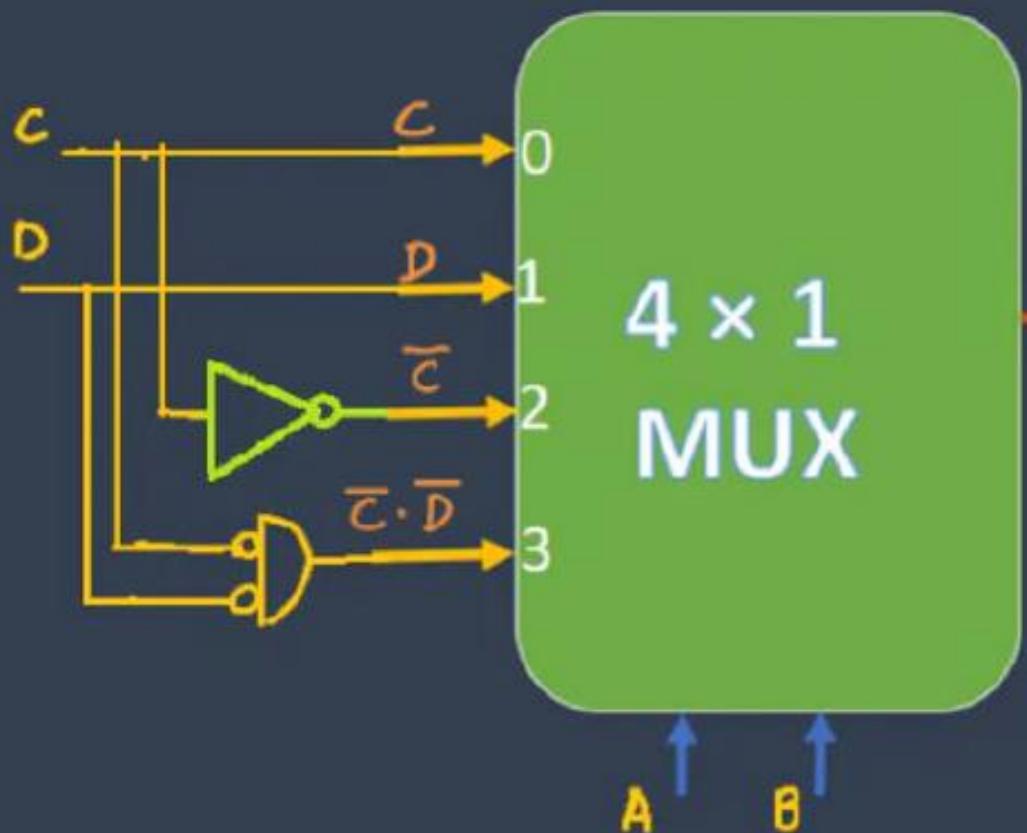


$$X = \bar{B}(0) + B\bar{C} = B\bar{C}$$

Q) Find the logic expression



Q) Find the minterms

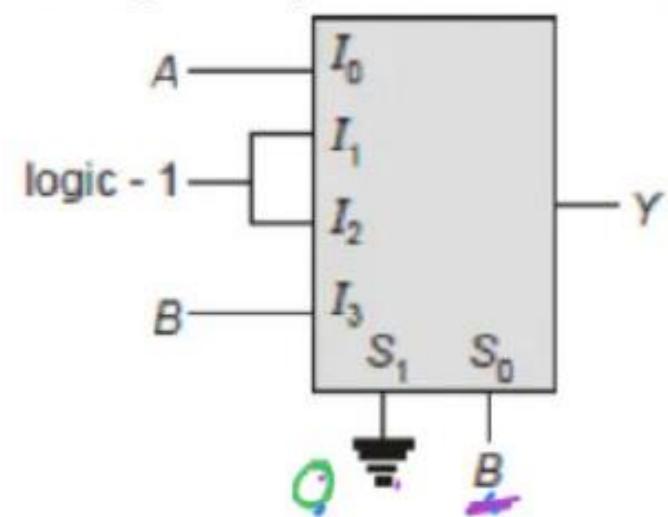


$$Y = \bar{A}\bar{B}C + \bar{A}BD + A\bar{B}\bar{C} + AB\bar{C}\bar{D}$$

0010	0101	1000	1100
0011	0111	1001	

$$Y = \sum m(2, 3, 5, 7, 8, 9, 12)$$

The logical expression of the output of the  $4 \times 1$  multiplexer shown below is



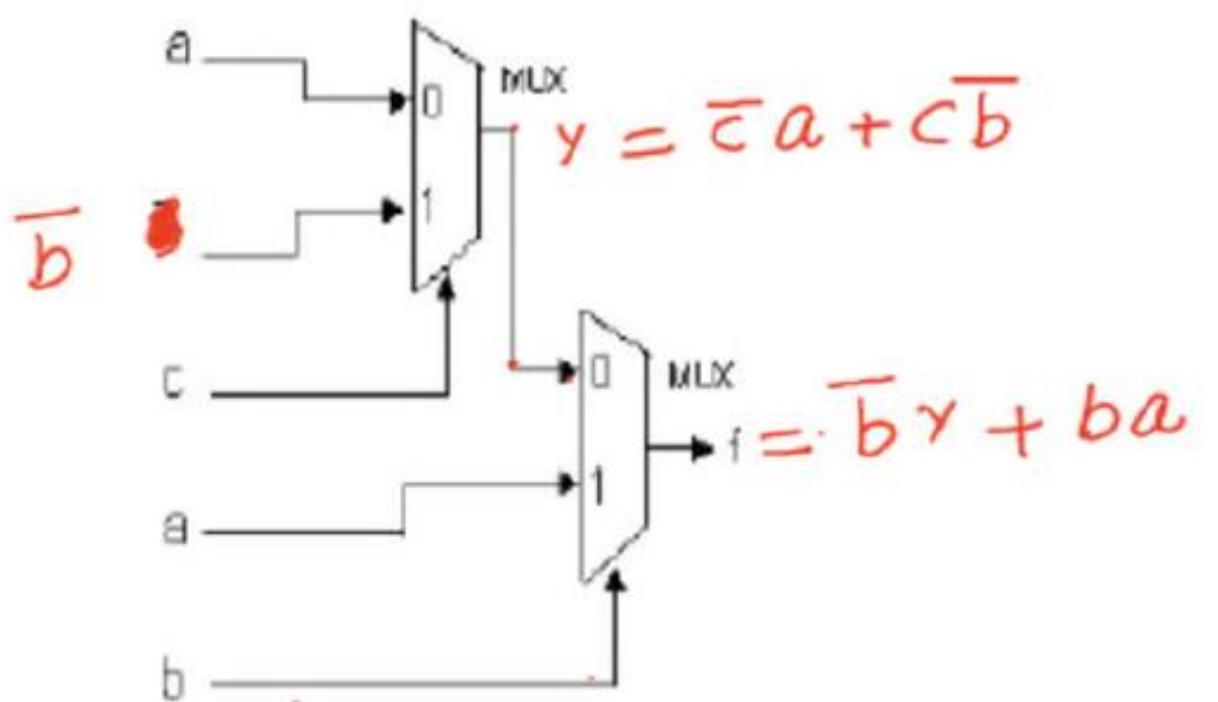
$S_1$	$S_0$	$Y$
0	0	$I_0$
0	1	$I_1$

- a.  $AB$
- b.  $\bar{A} + B$  ✓
- c.  $A \oplus B$
- d.  $AB + \bar{B}$

$$Y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1$$

$$Y = \bar{B} A + B I_1 = \underline{B + \bar{B} A} = \underline{A + B}$$

Consider the circuit below. Which one of the following options correctly represents  $f(a,b,c)$ ?



(A)  $\bar{ab} + ab + \bar{bc}$

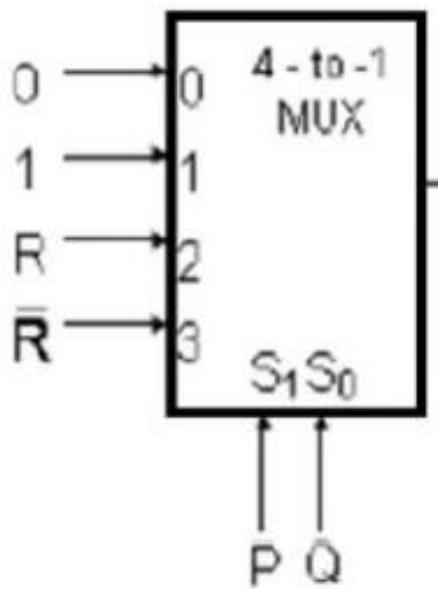
(B)  $ac + ab + \bar{bc}$

(C)  $ac + a\bar{b} + \bar{bc}$

(D)  $ac + ab + \bar{bc}$

$$\begin{aligned}
 f &= ab + \bar{b}(\bar{a}\bar{c} + \bar{b}c) \\
 f &= ab + a\bar{b}\bar{c} + \bar{b}c \quad \checkmark \\
 f &= ab + \bar{b}(c + a\bar{c}) \\
 &= ab + \bar{b}(c + a) \\
 f &= ab + a\bar{b} + \bar{b}c \\
 &\quad \text{(or)} \\
 f &= ab + \bar{b}c + a\bar{c}
 \end{aligned}$$

Consider the 4-to-1 multiplexer with two select lines  $S_1$  and  $S_0$  as given below.



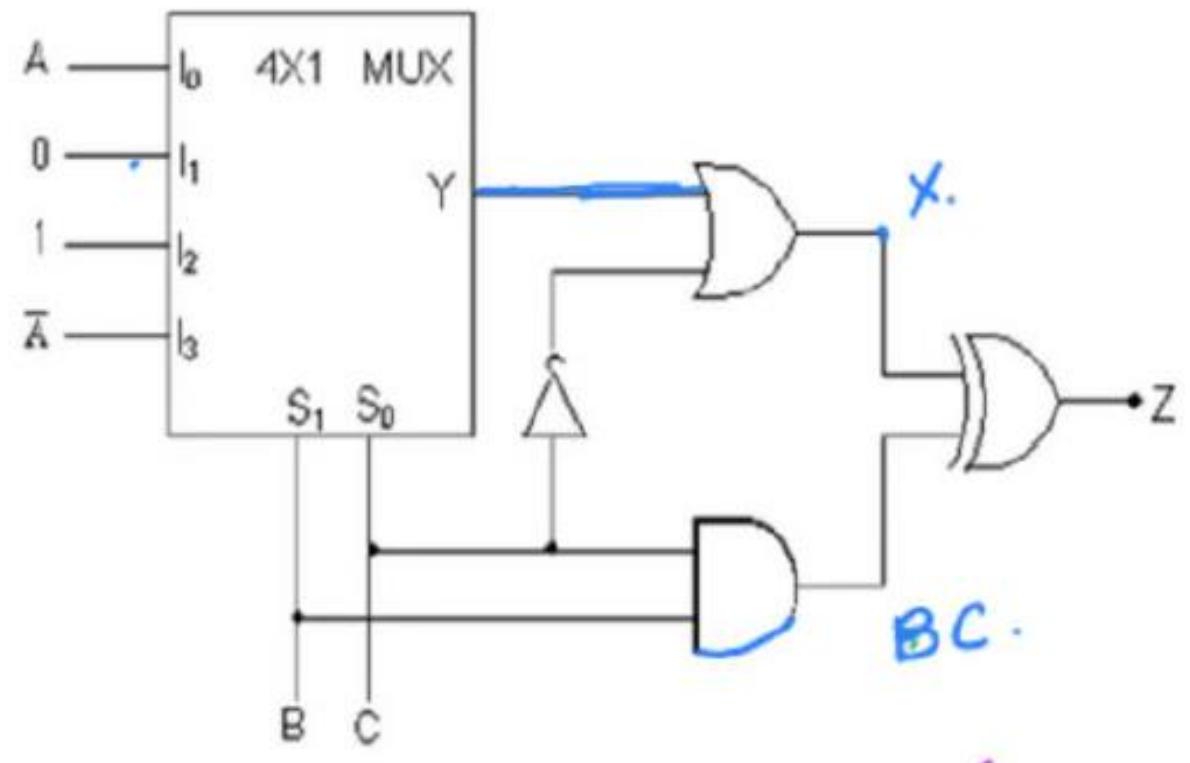
$$F = \overline{P}\overline{Q}(0) + \overline{P}Q(1) + P\overline{Q}(R) + PQ(\overline{R})$$
$$F = \overline{P}Q + P\overline{Q}R + PQ\overline{R}$$

0   0	1   0	1   1
0   1		

The output of the multiplexer can be expressed as

- (A)  $F(P,Q,R) = \Sigma m(1,3,4,5)$
- (B)  $F(P,Q,R) = \Sigma m(1,4,5,6)$
- (C)  $F(P,Q,R) = \Sigma m(2,5,6)$
- (D)  $F(P,Q,R) = \Sigma m(2,3,5,6)$  ✓

A combinational circuit using 4-to-1-line multiplexer is shown in the following diagram. The simplified expression for  $Z$  is



(A)  $A\bar{C} + B$

~~(B)  $AB + \bar{C}$~~

(C)  $A\bar{B} + C$

(D)  $AC + \bar{B}$

$$X = A\bar{B}\bar{C} + B\bar{C} + \bar{A}BC + \bar{C}$$

$$X = \bar{C} [A\bar{B} + B\bar{C} + 1] + \bar{A}BC$$

$$X = \bar{C} + \bar{A}BC$$

$X = \bar{C} + \bar{A}B$

$$Z = BC \oplus (\bar{C} + \bar{A}B)$$

$$Z = BC(\overline{\bar{C} + \bar{A}B}) + \overline{BC}(\bar{C} + \bar{A}B)$$

$$Z = BC(C \cdot (A + \bar{B})) + (\bar{B} + \bar{C})(\bar{C} + \bar{A}B)$$

$$Z = ABC + 0 + \bar{B}\bar{C} + 0 + \bar{C} + \bar{A}BC$$



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ALERT

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ELECTRICAL ENGINEERING



B V REDDY



VISHAL SONI



SURESH VSR



QAISAR HAFIZ



ANKIT GOYAL



TRINADH REDDY



SIDDHARTH  
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START DATE

4th jan  
2020

FOR 10% DISCOUNT

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START DATE

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START DATE

21  
DEC  
2020

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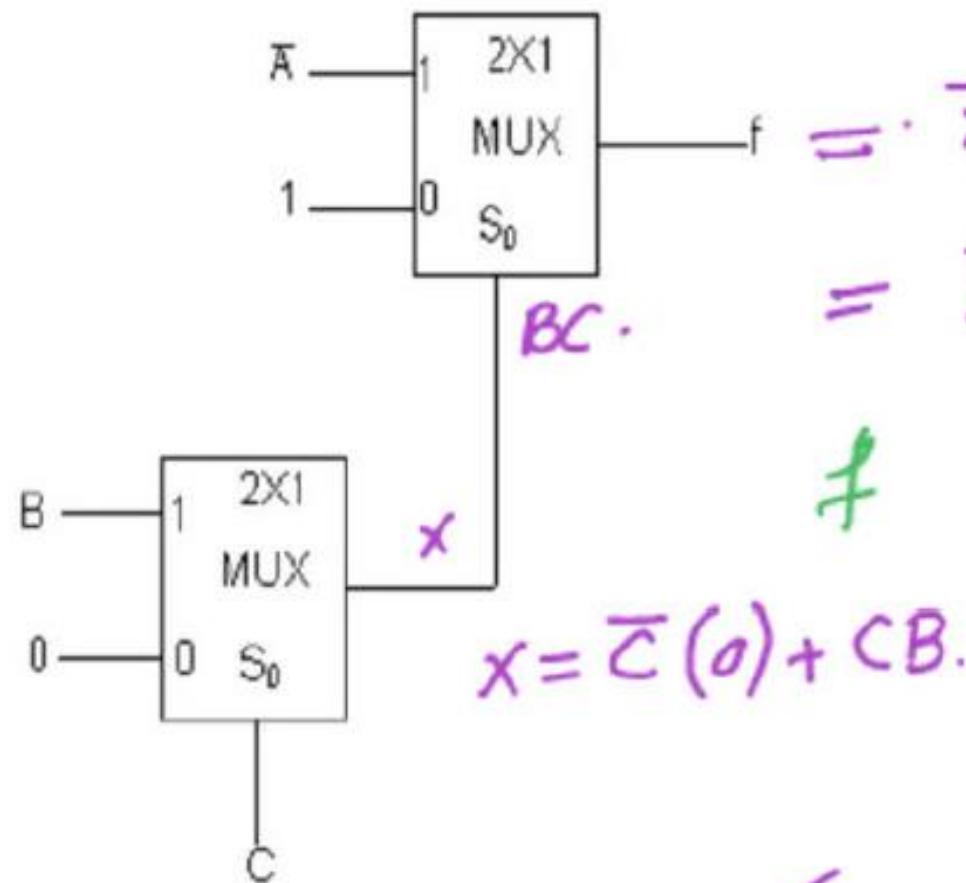
USE CODE  
**BVREDDY**

$$Z = ABC + \overline{B}\overline{C} + \overline{C} + \overline{A}B\overline{C}$$

$$Z = ABC + \overline{C} \left[ \overline{B} + 1 + \overline{A}B \right]$$

$$\boxed{Z = AB + \overline{C}}$$

The network shown below acts as



(A) NOR gate

(C) OR gate

(D) Ex-OR gate

(B) NAND gate

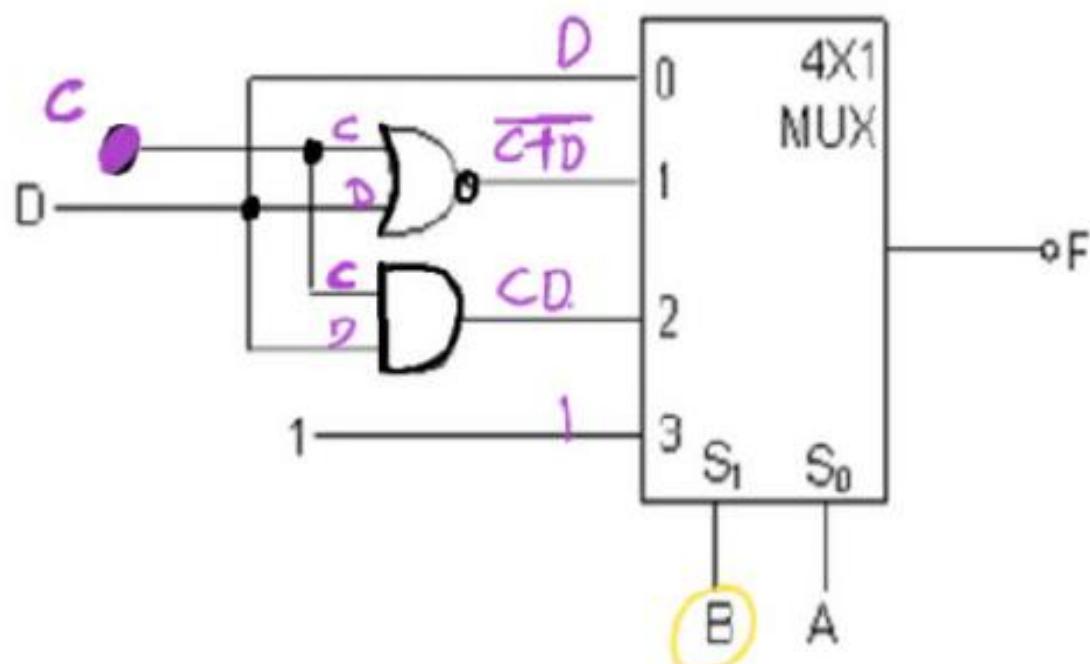
$$\begin{aligned}f &= \overline{x}(1) + x(\overline{A}) \\&= \overline{BC} + BC\overline{A} \\&\neq \overline{ABC} + \overline{BC}\end{aligned}$$

$$f = \overline{BC} + BC\overline{A}$$

$$f = (\overline{BC} + BC)(\overline{BC} + \overline{A})$$

$$f = \overline{\overline{A} + \overline{B} + \overline{C}} = \overline{ABC}$$

The Boolean function realized by the following circuit is



(A)  $F(A, B, C, D) = \Sigma m(0, 2, 4, 5, 9, 10, 11)$

(B)  $F(A, B, C, D) = \Sigma m(1, 3, 7, 8, 12, 13, 14, 15)$  ✓

(C)  $F(A, B, C, D) = \Sigma m(1, 8, 14, 15)$

(D)  $F(A, B, C, D) = \Sigma m(0, 2, 6, 8, 14, 15)$

$$= \bar{B} \bar{A} D + \bar{B} A (\bar{C} \cdot \bar{D}) + B \bar{A} C D + B A$$

$$f = AB + \bar{A} \bar{B} D + A \bar{B} \bar{C} \bar{D} + \bar{A} B C D.$$

<u>1100</u>	<u>0001</u>	<u>1000</u>	<u>0111</u>
<u>1101</u>	<u>0011</u>		
<u>1110</u>			
<u>1111</u>			

Q) Design a logic circuit  $f(A, B, C) = \sum m(0, 1, 3, 6, 7)$  using  $4 \times 1$  MUX

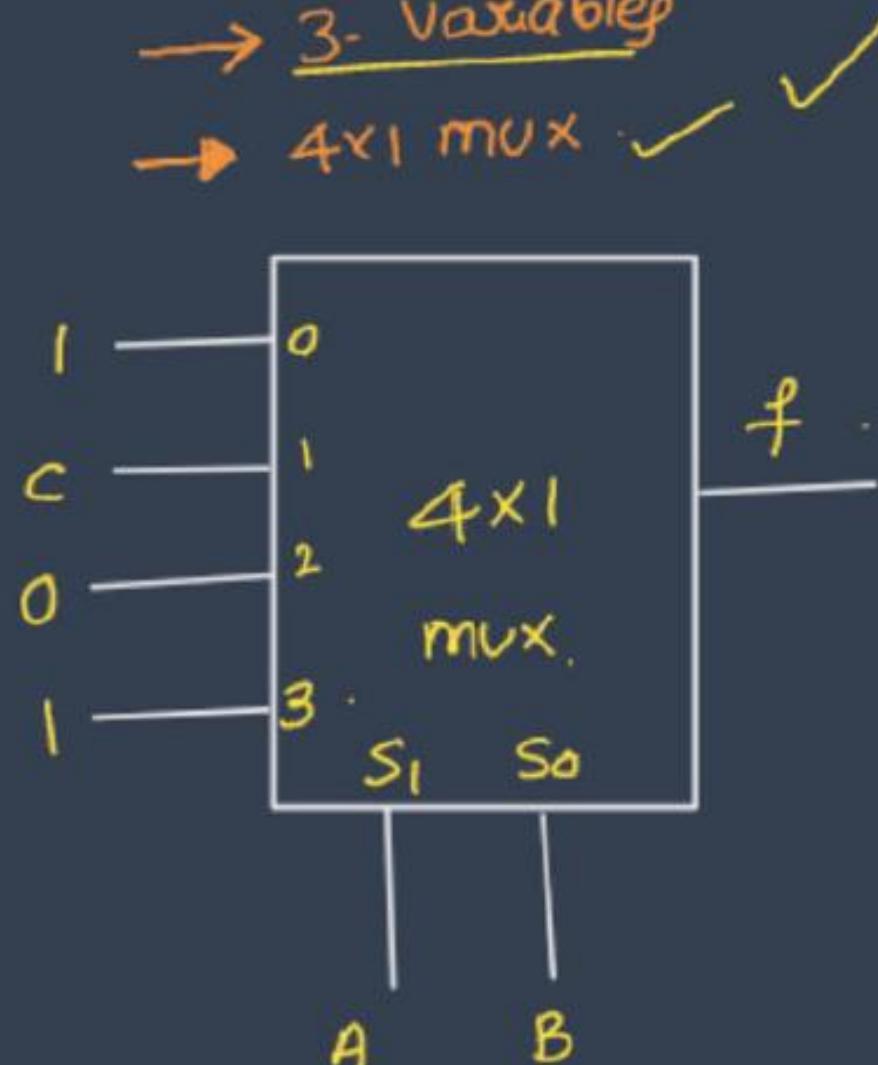
- i. AB as select lines ✓
- ii. BC as select lines ✓
- iii. AC as select lines

→ 3-variable

→  $4 \times 1$  mux ✓

$\bar{A} \bar{B}(0)$	$\bar{A} B(1)$	$A \bar{B}(2)$	$A B(3)$
$\bar{A} \bar{B} \bar{C}$ 0	$\bar{A} B \bar{C}$ 1	$A \bar{B} \bar{C}$ 4	$A B \bar{C}$ 6
$\bar{A} \bar{B} C$ 2	$\bar{A} B C$ 3	$A \bar{B} C$ 5	$A B C$ 7

$$\bar{C} + C = 1 \quad | \quad 0 + C = C \quad | \quad 0 + 0 = 0 \quad | \quad \bar{C} + C = 1$$



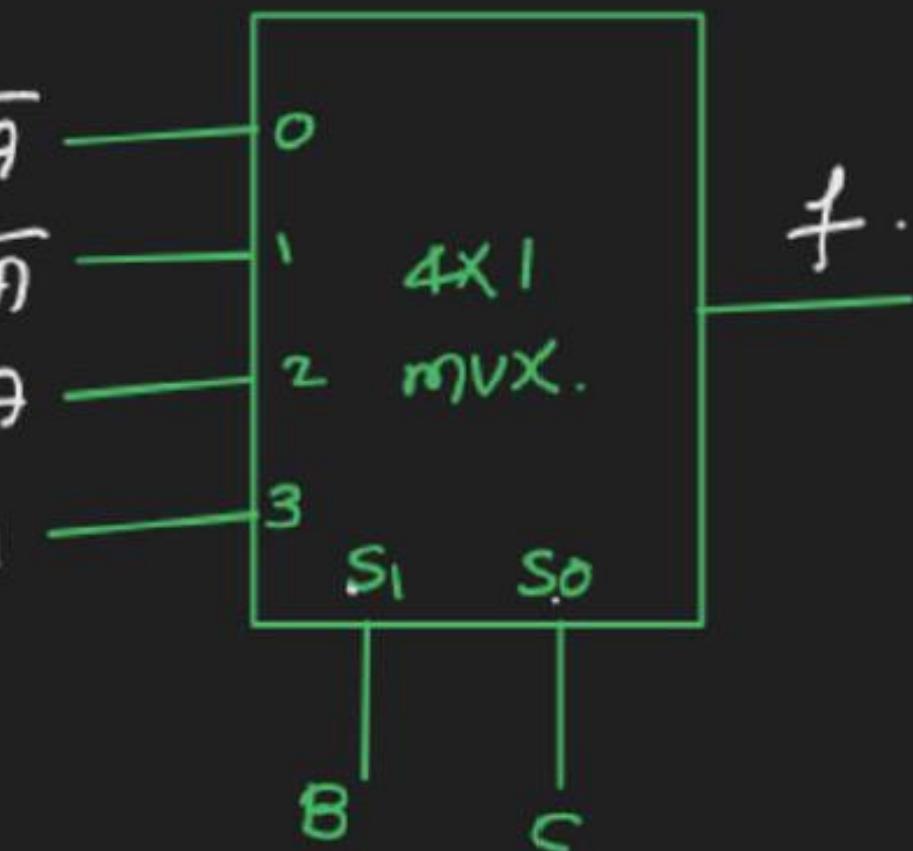
II BC as select lines.

0      1      2      3  
 $\bar{B}\bar{C}$      $\bar{B}C$      $B\bar{C}$      $BC$

$\bar{A}$	$\bar{A}\bar{B}\bar{C}$ 0	$\bar{A}BC$ 1	$\bar{A}B\bar{C}$ 2	$\bar{A}BC$ 3
$A$	$A\bar{B}\bar{C}$ 4	$A\bar{B}C$ 5	$ABC$ 6	$ABC$ 7
$\bar{A}$	$\bar{A}$	$\bar{A}$	$A$	$A$

msb      mlsb

D



→ 3. Variables.

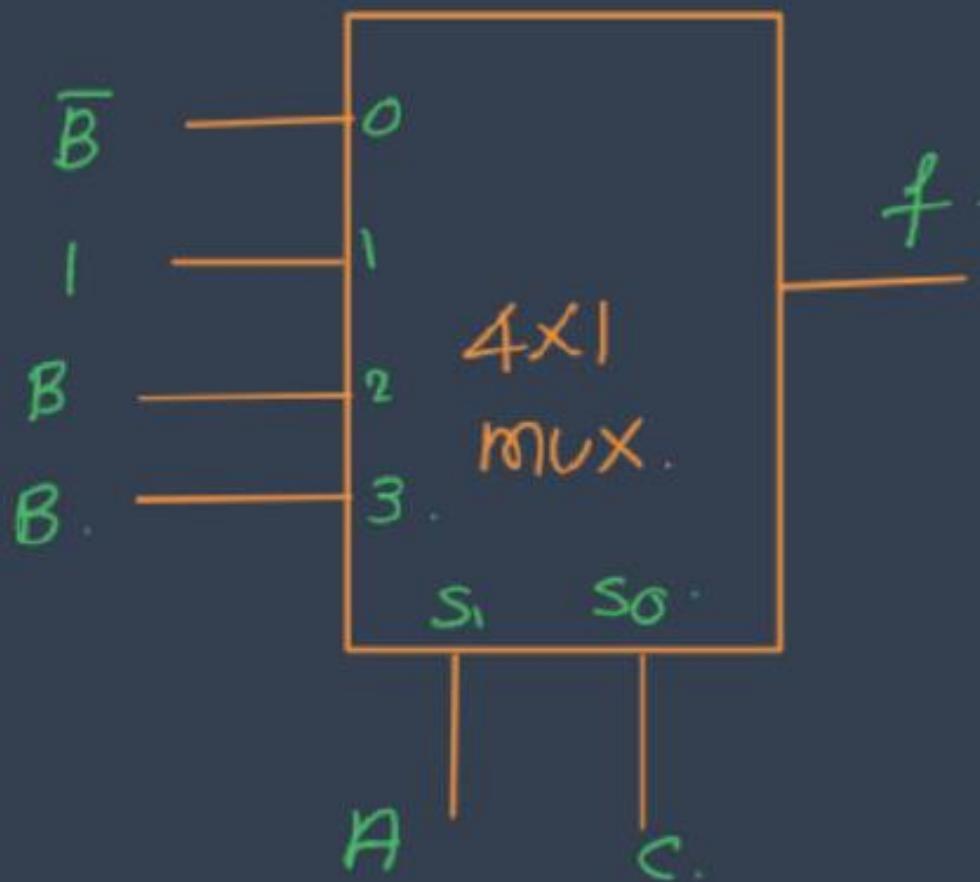
→ one 4x1 mux + NOT gate

iii) AC as Select lines.

$\bar{A}\bar{C}$	$\bar{A}C$	$A\bar{C}$	$AC$	
$\bar{B}$	$\bar{A}\bar{B}\bar{C}$ 0	$\bar{A}\bar{B}C$ 1	$A\bar{B}\bar{C}$ 4	$A\bar{B}C$ 5
B	$\bar{A}BC$ 2	$\bar{A}BC$ 3	$AB\bar{C}$ 6	$ABC$ 7
$\bar{B}$	1		B	B

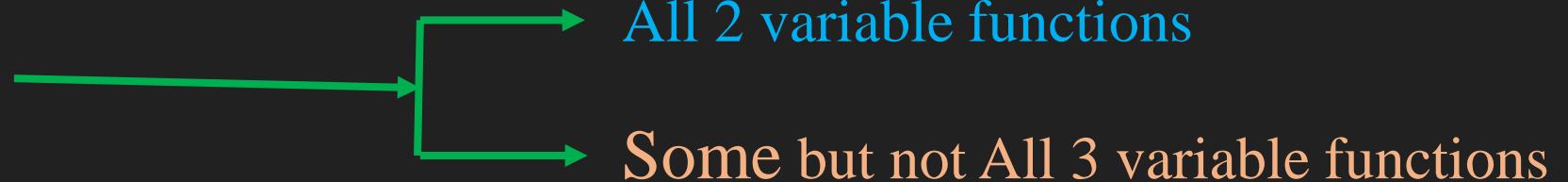
→ 3 variables

→ one  $4 \times 1$  mux + NOT gate.



# Note :

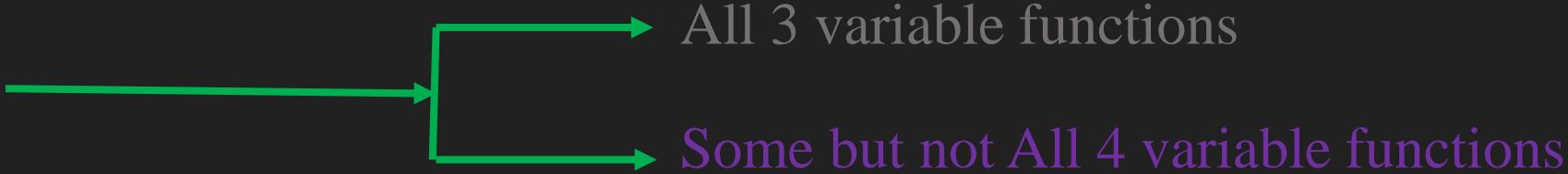
1. By using one  $4 \times 1$  Mux



2. By using one  $4 \times 1$  Mux + NOT Gate



3. By using one  $8 \times 1$  Mux



4. By using one  $8 \times 1$  Mux + NOT Gate



5. n- variable function

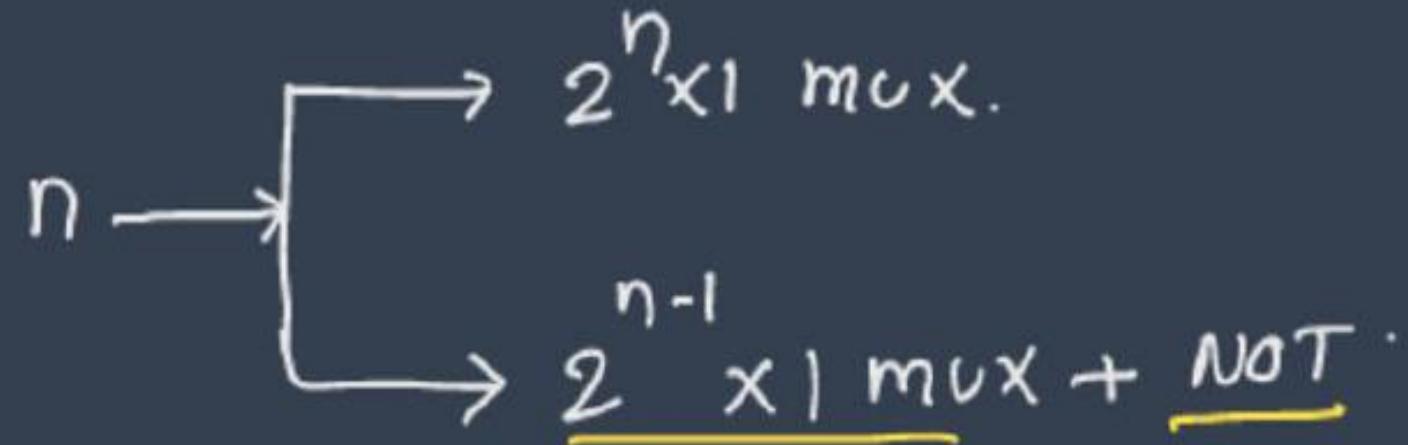


One  $2^n \times 1$  MUX

One  $2^{n-1} \times 1$  MUX + one NOT Gate

Q) Suppose only one mux and one inverter are allowed to be used to implement Boolean function of  $n$ - variables , what is the minimum size of the mux needed

- a)  $2^n \times 1$  MUX
- b)  $2^{n+1} \times 1$  MUX
- c)  $2^{n-1} \times 1$  MUX ✓
- d)  $2^{n-2} \times 1$  MUX



Q) Without using any additional circuitry an  $8 \times 1$  mux can be used to obtain

- a) Some but not all Boolean functions of 3 variables MSQ.
- b) All functions of 3 variable & none of 4- variables
- c) All function's of 4 variables
- d) All functions of 3 variables and some but not all functions of 4 variables

If the logical expressions of the outputs in the circuits shown in Figures A and B are same, then select the correct combination of signals to be connected to the inputs of multiplexer (i.e.  $I_0$ ,  $I_1$ ,  $I_2$ ,  $I_3$ ) using the codes given below the Figures.

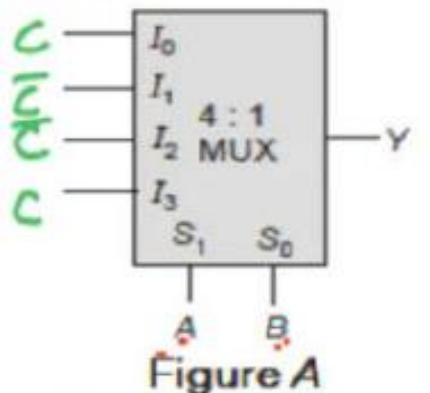


Figure A

$$Y = \sum m(1, 2, 4, 7)$$

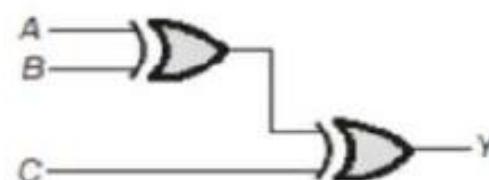


Figure B

Codes:

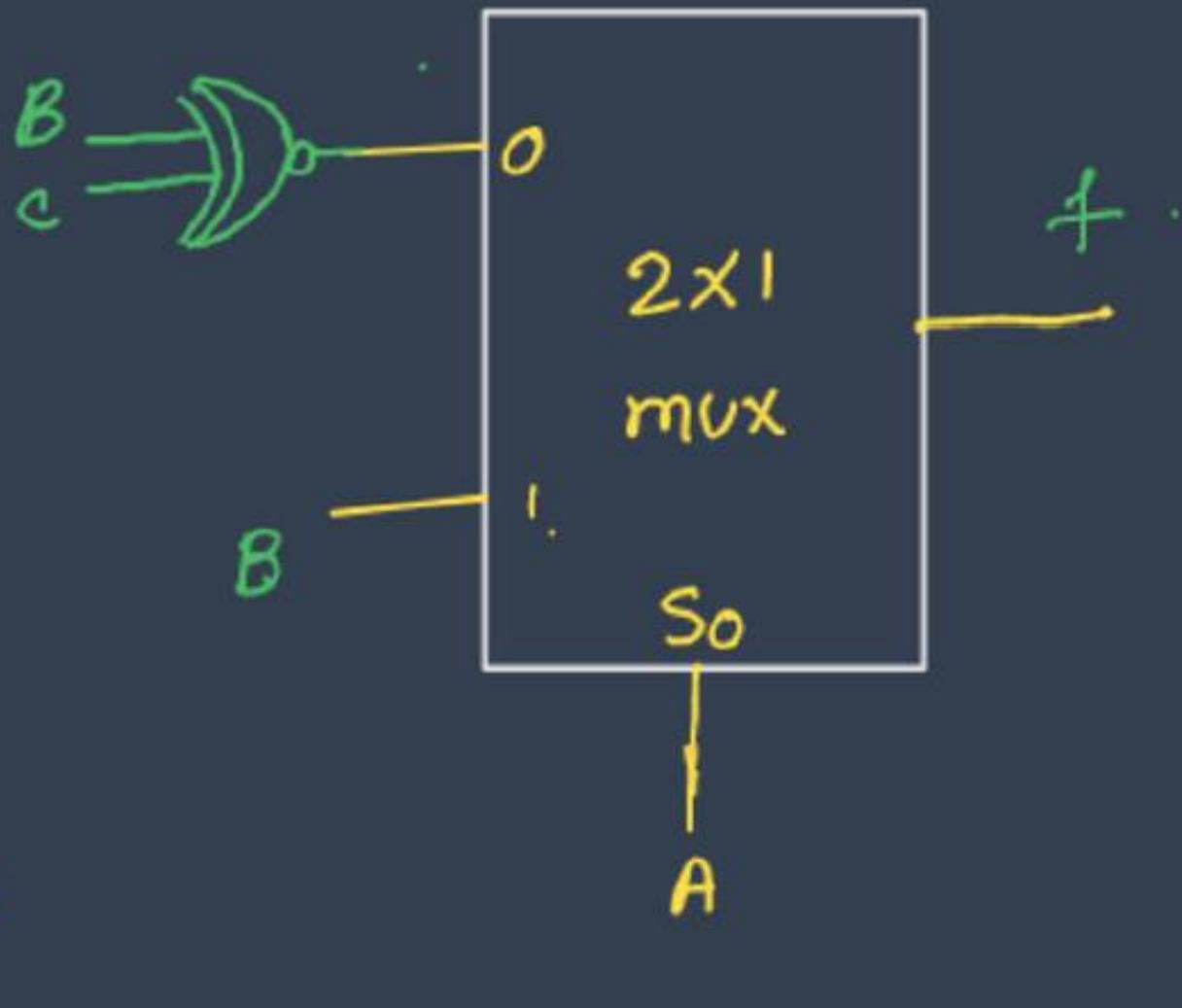
- |     | $I_0$     | $I_1$     | $I_2$     | $I_3$     |
|-----|-----------|-----------|-----------|-----------|
| (a) | 0         | $C$       | $\bar{C}$ | 1         |
| (b) | $\bar{C}$ | $C$       | $C$       | $\bar{C}$ |
| (c) | $C$       | $\bar{C}$ | $\bar{C}$ | $C$       |
| (d) | 1         | $C$       | $C$       | $\bar{C}$ |



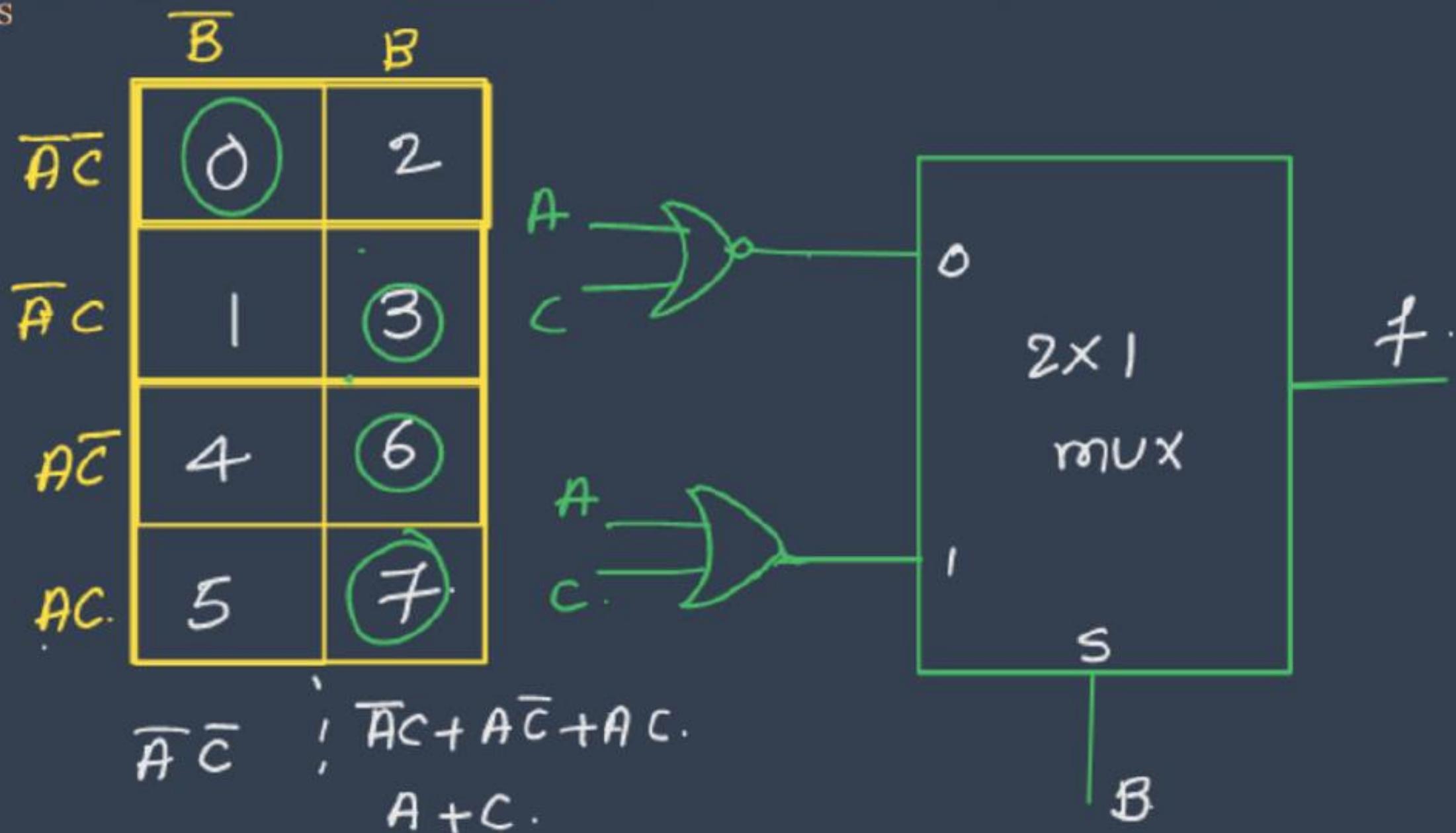
$\bar{A}\bar{B}$	$\bar{A}B$	$A\bar{B}$	$AB$
$\bar{C}$	0	2	4
$C$	1	3	5
$\bar{C}$			7
$C$			

Q) Design a logic circuit  $F(A, B, C) = \sum m(0, 3, 6, 7)$  using  $2 \times 1$  MUX by using A as select lines

$\bar{A}$	$A$
$\bar{B} \bar{C}$	0 4
$\bar{B} C$	1 5
$B \bar{C}$	2 6
$B C$	3 7
$\bar{B} \bar{C} + BC$	
$\bar{B} \bar{C} + BC$	
B	

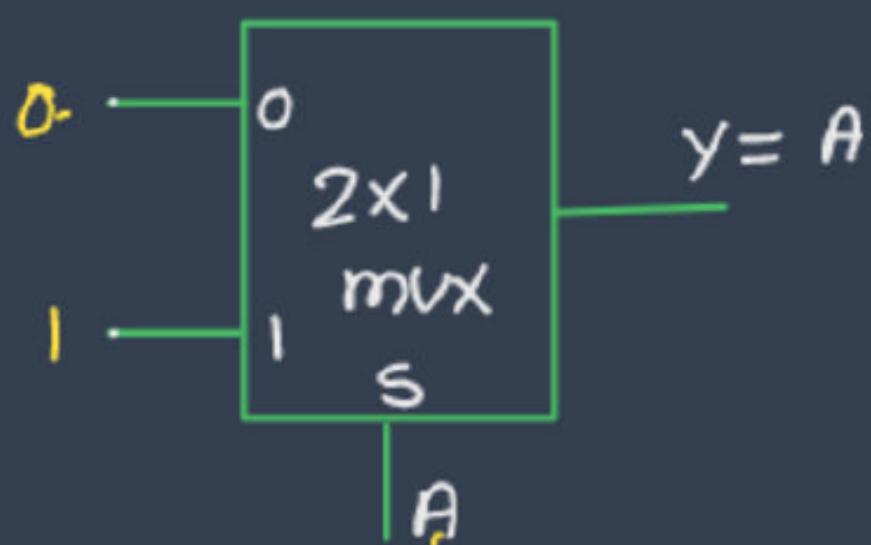


Q) Design a logic circuit  $F(A, B, C) = \sum m(0, 3, 6, 7)$  using  $2 \times 1$  MUX by using B as select lines



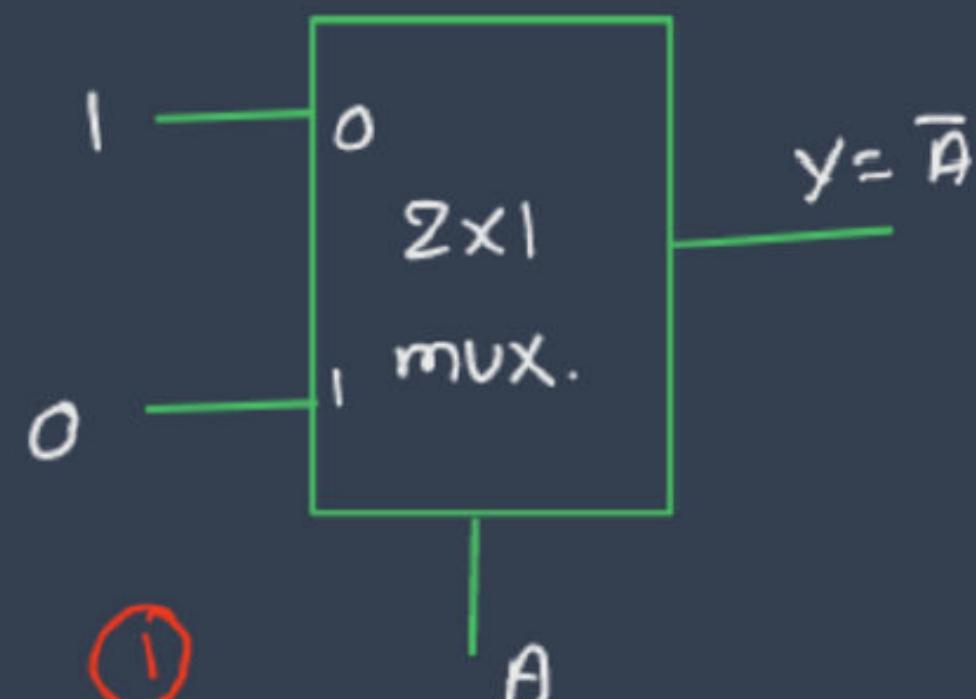
# MUX as Universal Gate

1. Buffer.



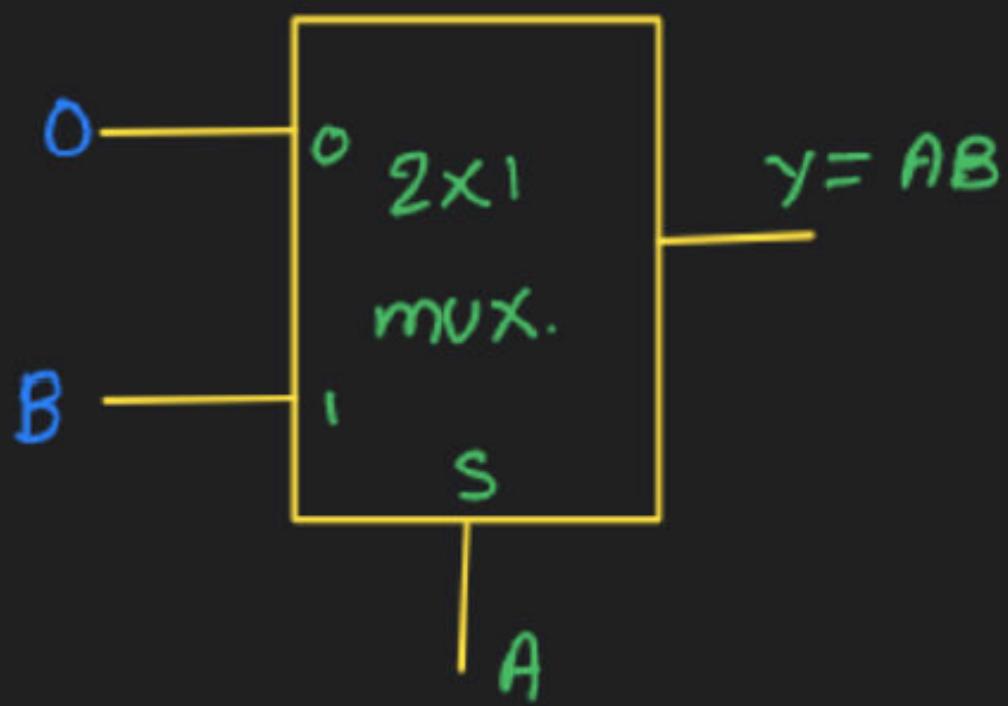
①

2. NOT Gate.



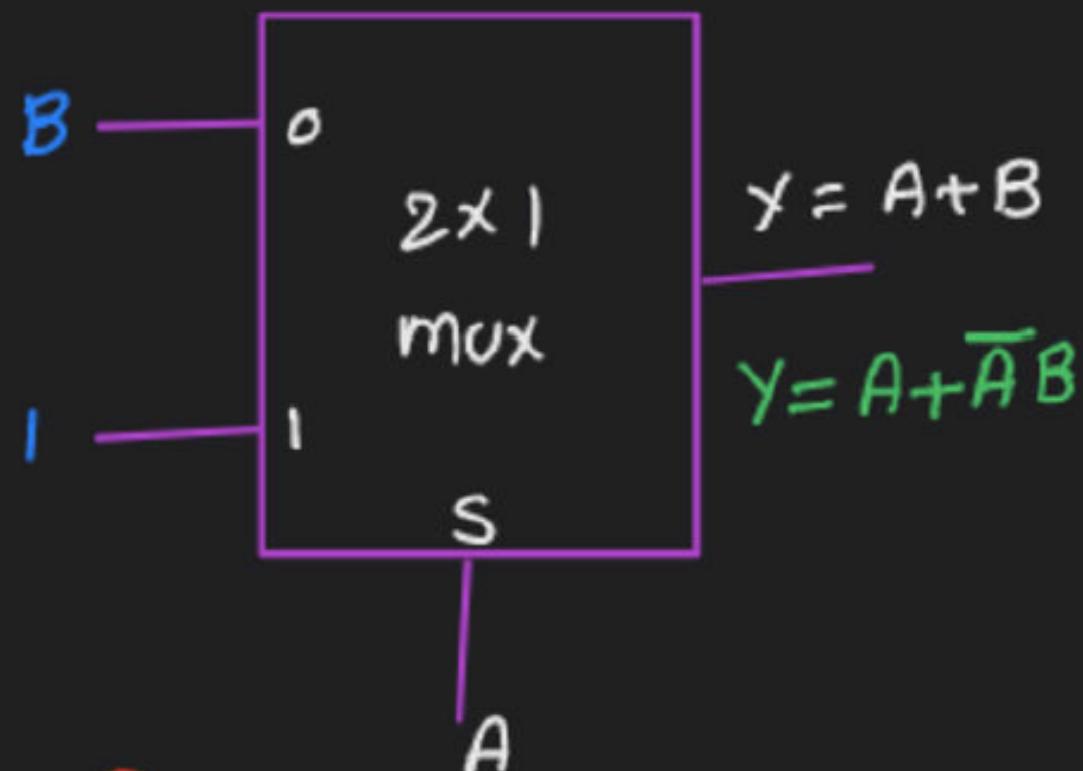
①

### 3. AND Gate



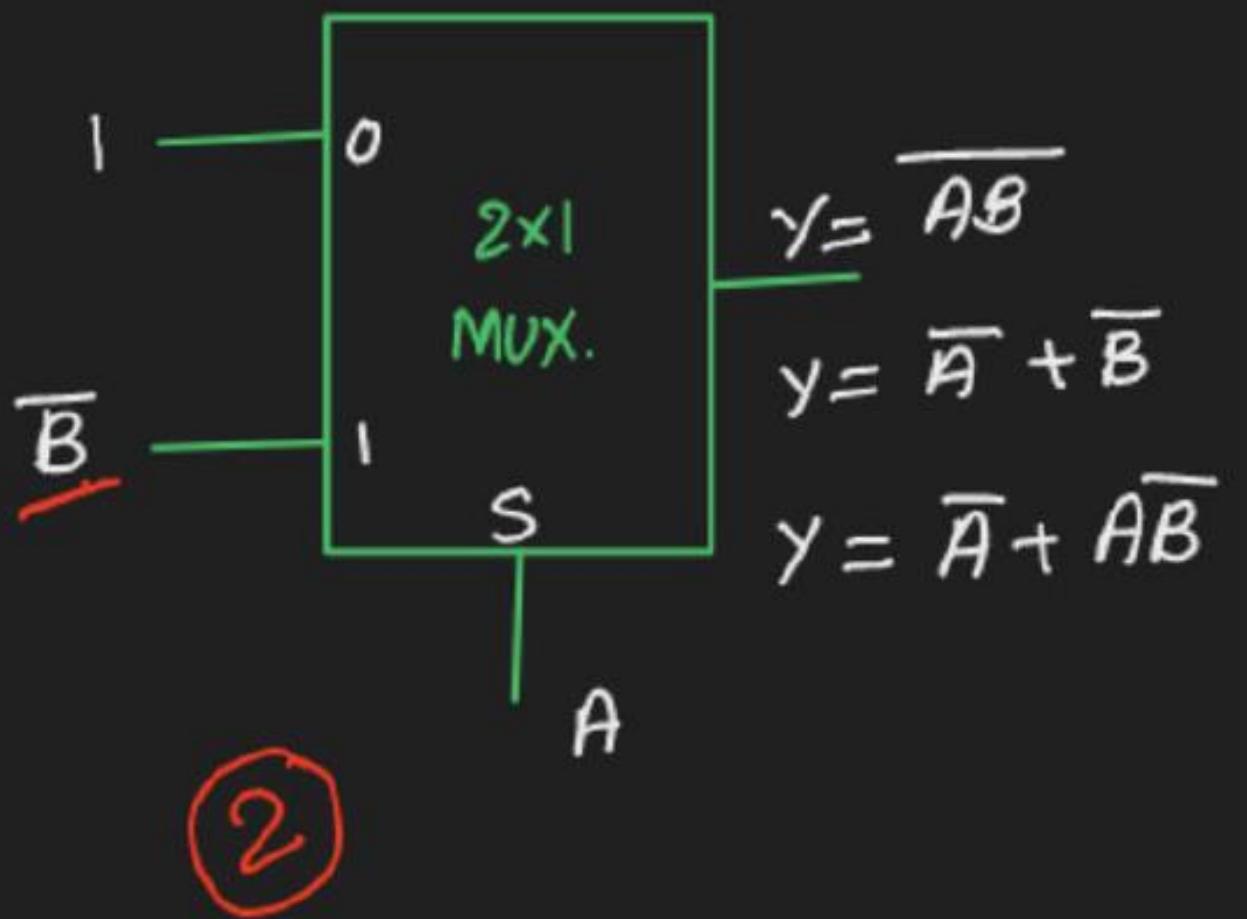
①

### 4. OR-Gate

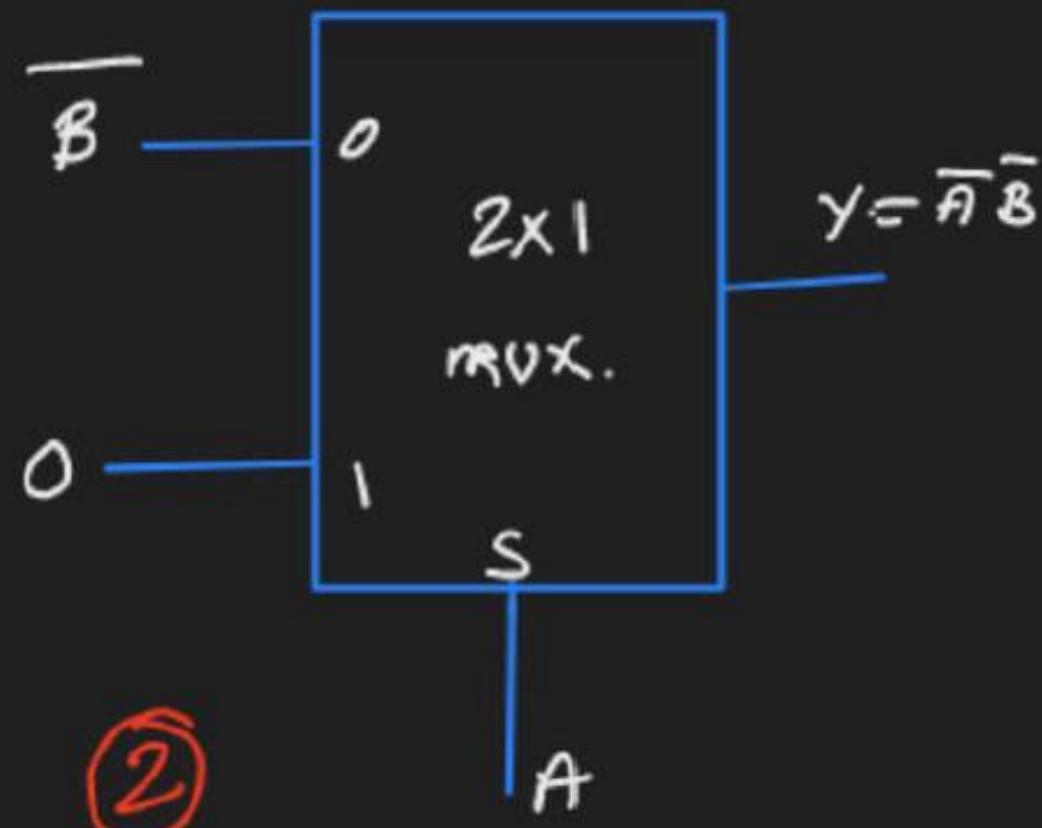


①

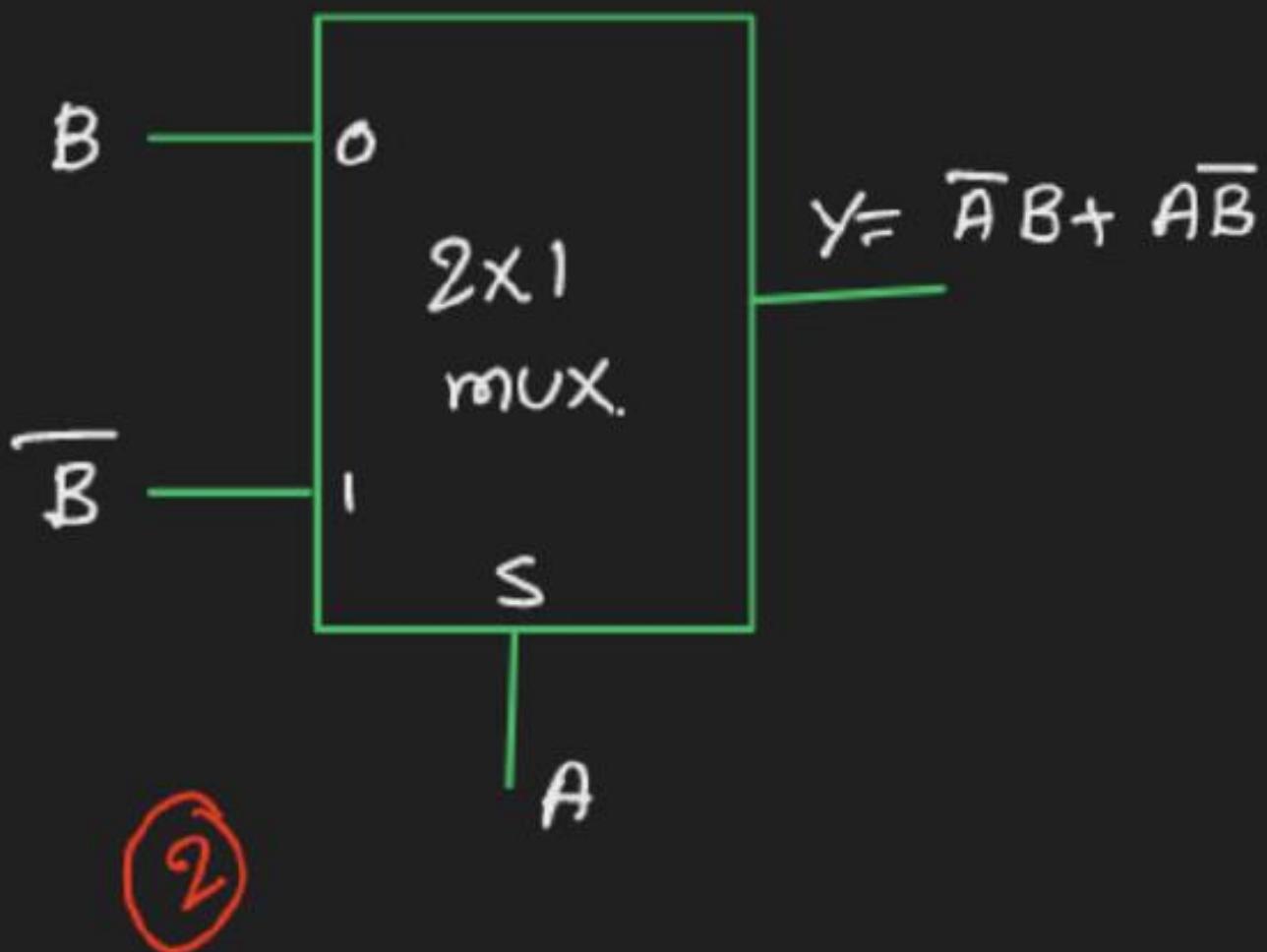
## 5. NAND Gate



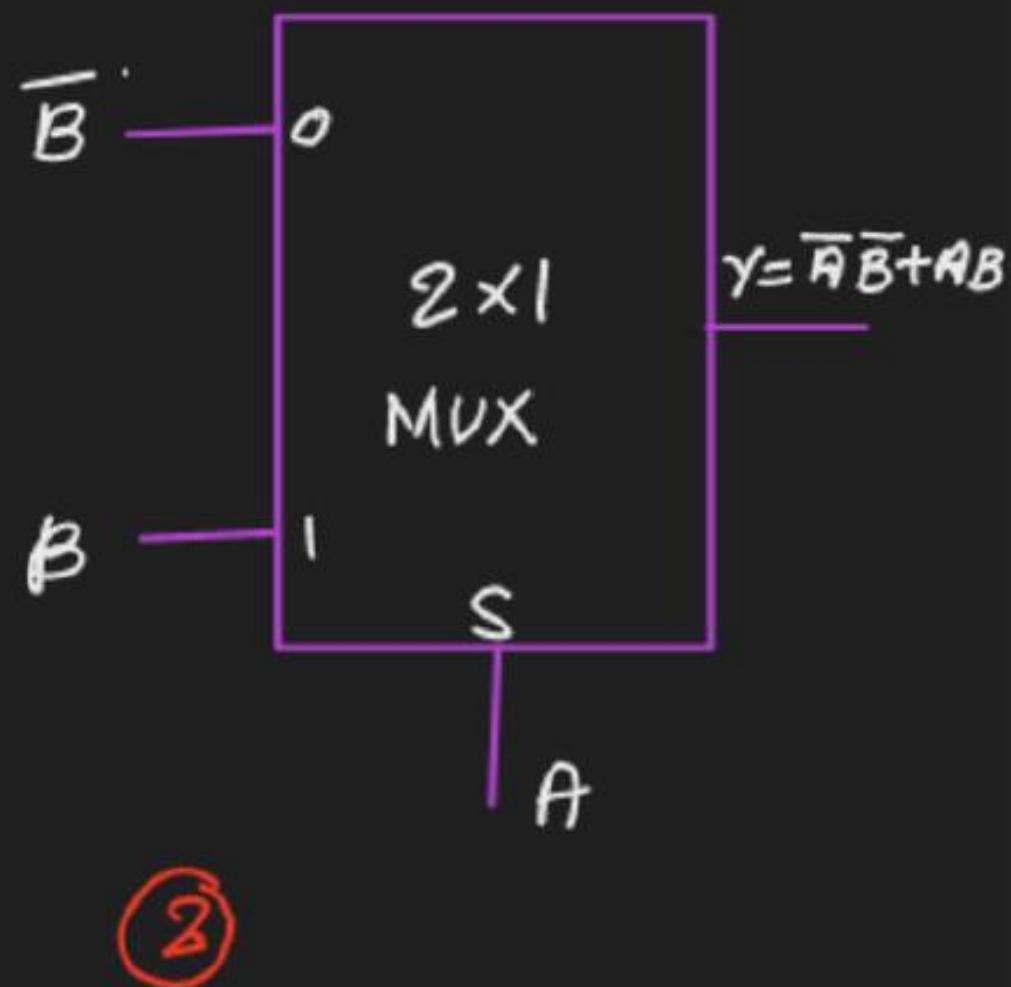
## 6. NOR Gate



## 7. XOR Gate

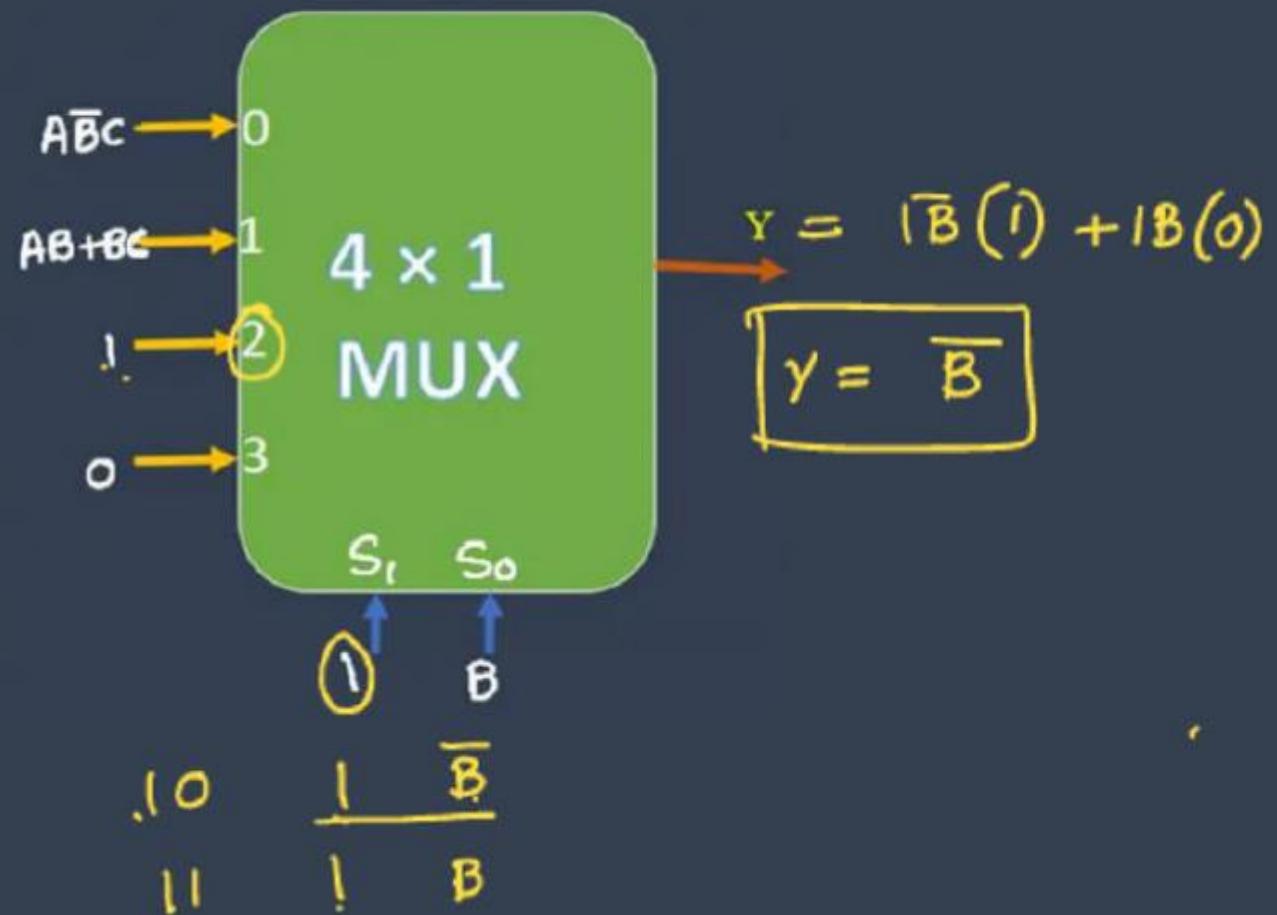


## 8. XNOR Gate

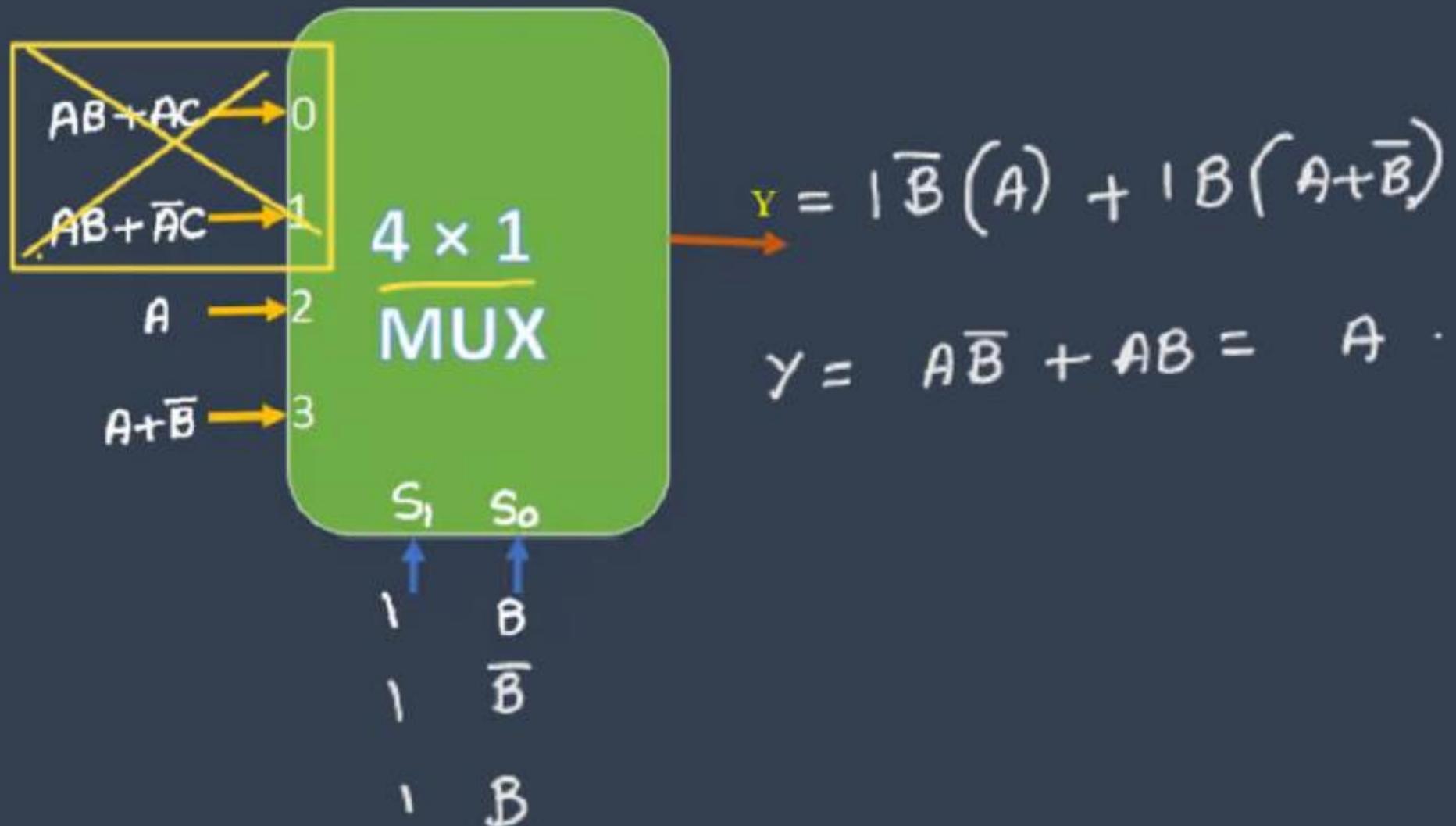


Logic Gate	Number of MUX required
<b>BUFFER</b>	1
<b>NOT</b>	1
<b>AND</b>	1
<b>OR</b>	1
<b>NAND</b>	2
<b>NOR</b>	2
<b>EX-OR</b>	2
<b>EX-NOR</b>	2

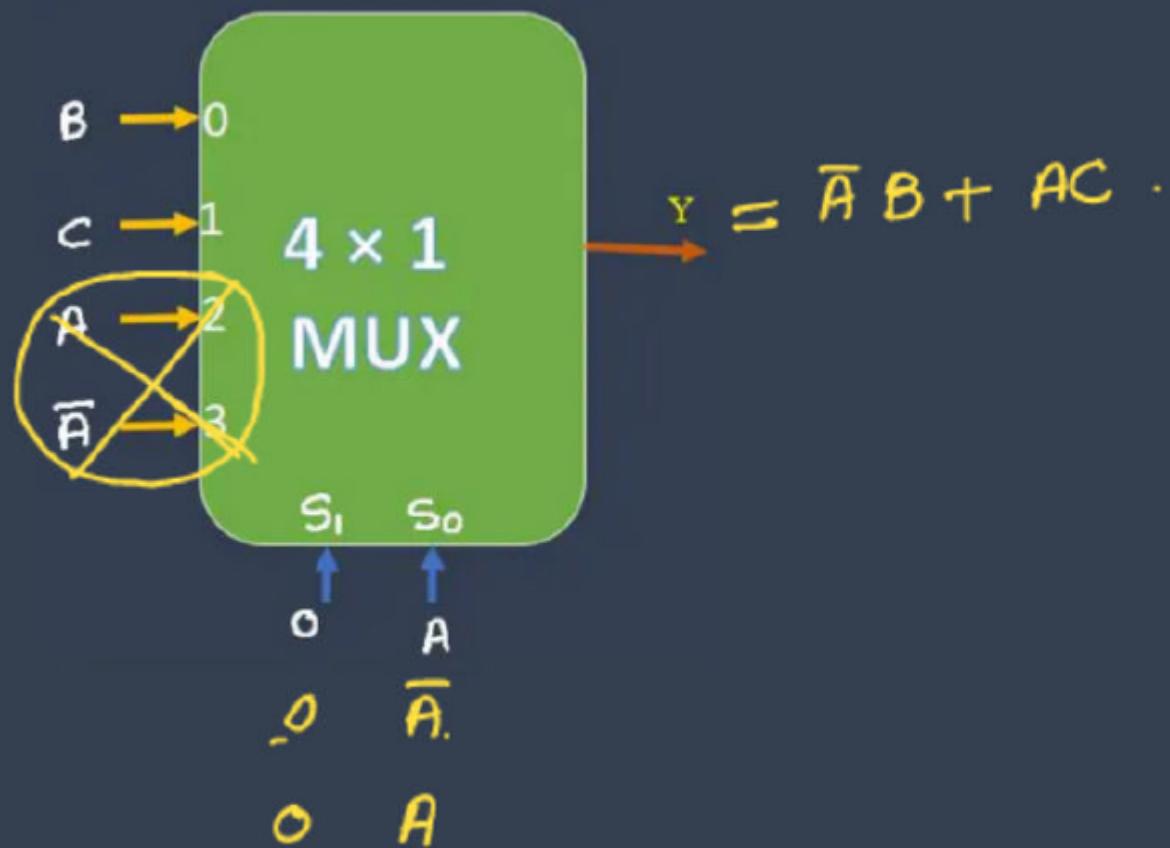
Q) Find the logic expression



Q) Find the logic expression

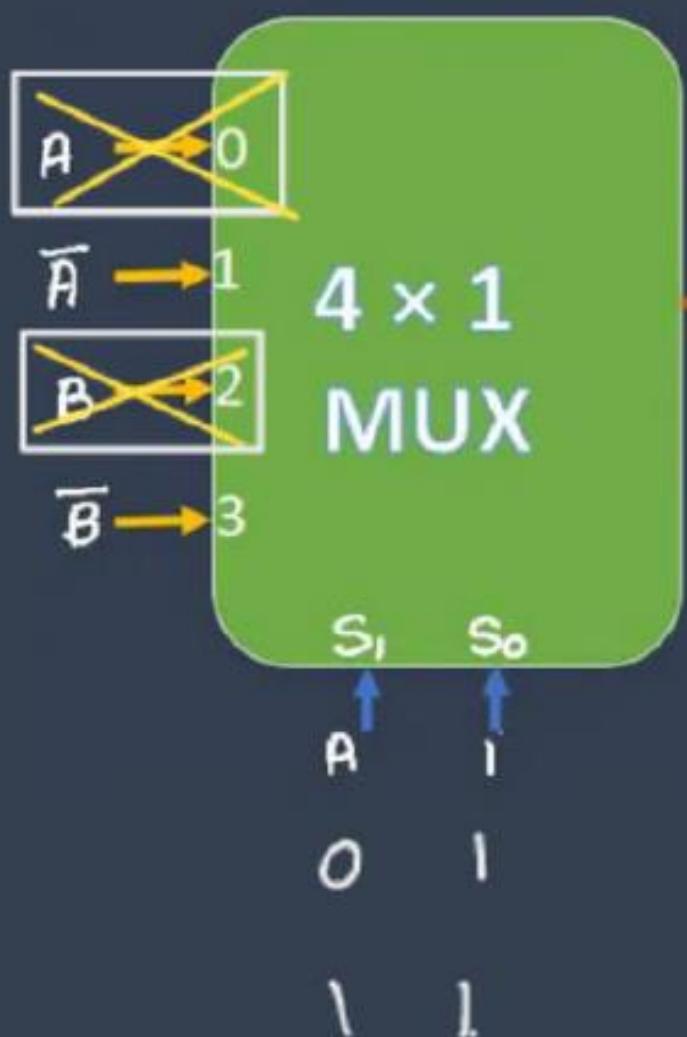


Q) Find the logic expression



$$Y = \bar{A}B + AC$$

Q) Find the logic expression



$$Y = \bar{A} \bar{A} + A \bar{B}$$

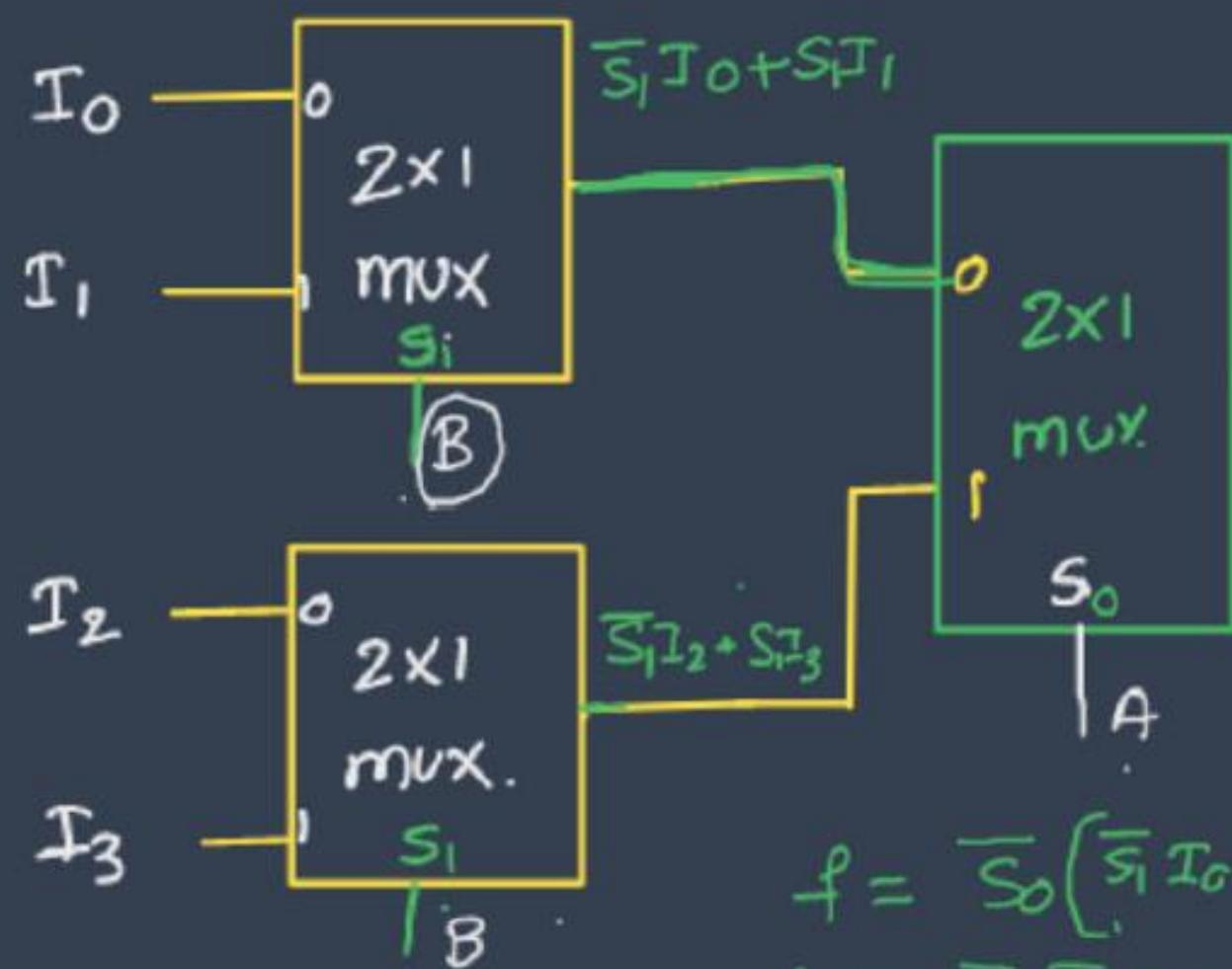
$$Y = \bar{A} + A \bar{B}$$

$$Y = \bar{A} + \bar{B}$$

$$Y = \overline{AB}$$

# Implementation of Higher order MUX using lower order MUX

Q) Design  $4 \times 1$  MUX using  $2 \times 1$  MUX



$$f(A, B)$$

$$f = \bar{A}\bar{B}I_0 + \bar{A}B\bar{I}_1 + A\bar{B}I_2 + AB\bar{I}_3$$

$$f = \bar{S}_0(\bar{S}_1 I_0 + S_1 I_1) + S_0(\bar{S}_1 I_2 + S_1 I_3)$$

$$f = \bar{S}_1 \bar{S}_0 I_0 + (\bar{S}_0 S_1 I_1) + (\bar{S}_1 S_0 I_2) + S_0 S_1 I_3$$

Q) Design  $8 \times 1$  MUX using  $2 \times 1$  MUX

$$\frac{8}{2} = 4 \quad L_1 \rightarrow C.$$

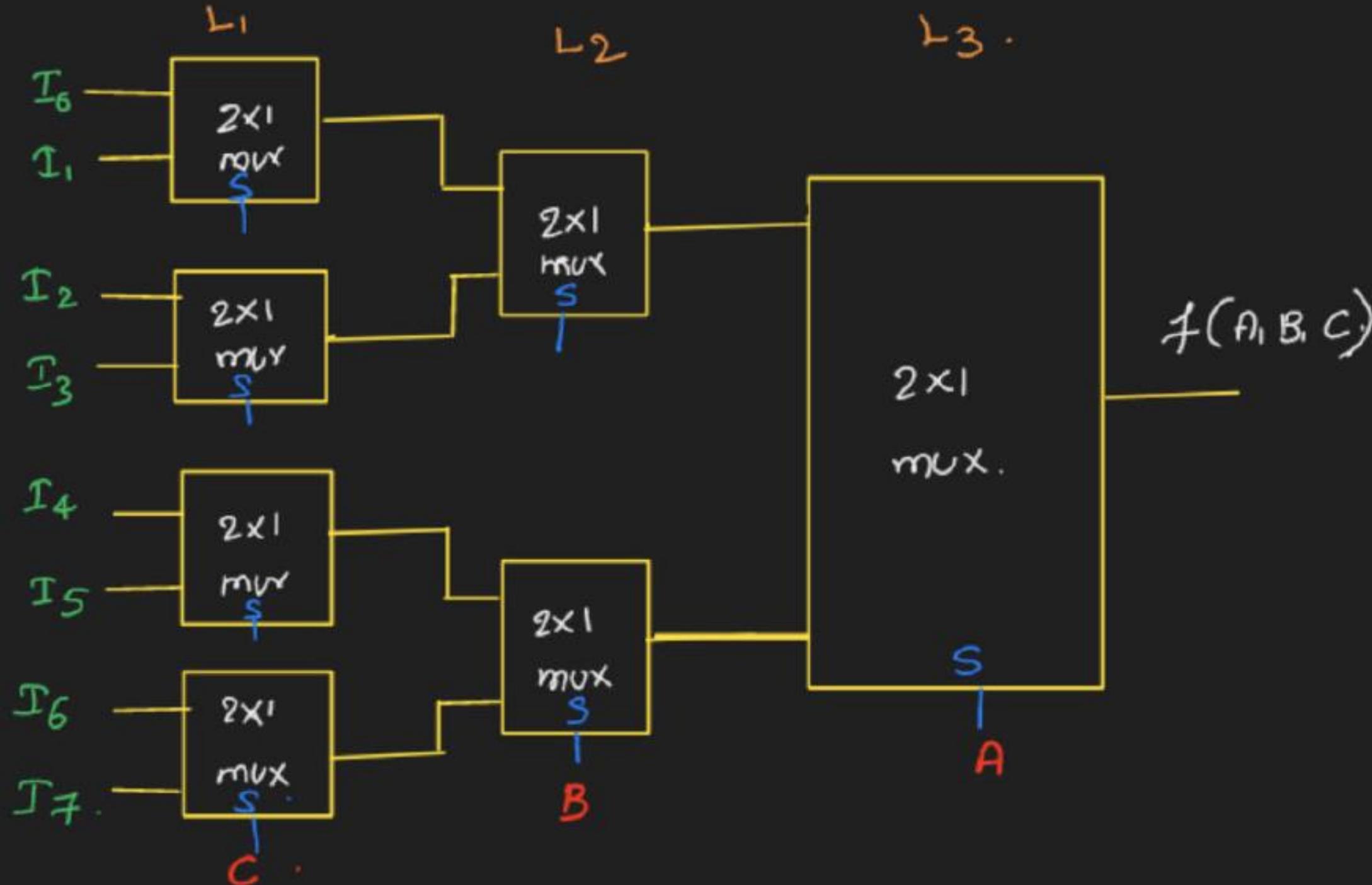
$$\frac{4}{2} = 2 \quad L_2 \rightarrow B$$

$$\frac{2}{2} = 1. \quad L_3 \rightarrow A$$

---

(1)

$$f(A, B, C)$$

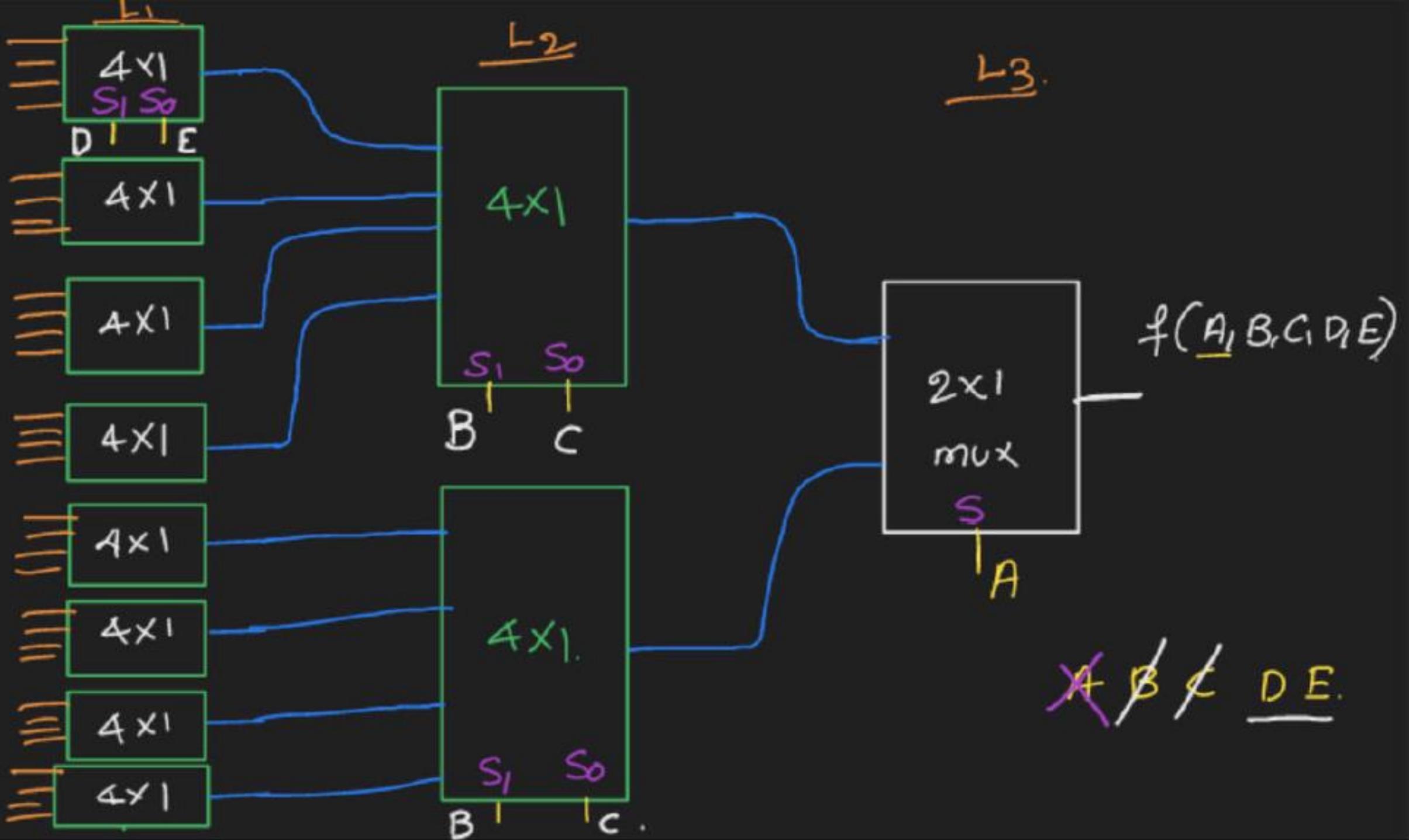


Q) Design  $32 \times 1$  MUX using  $4 \times 1$  MUX

$$\frac{32}{4} = 8 \quad L_1 \checkmark$$

$$\frac{8}{4} = 2 \quad L_2 \checkmark$$

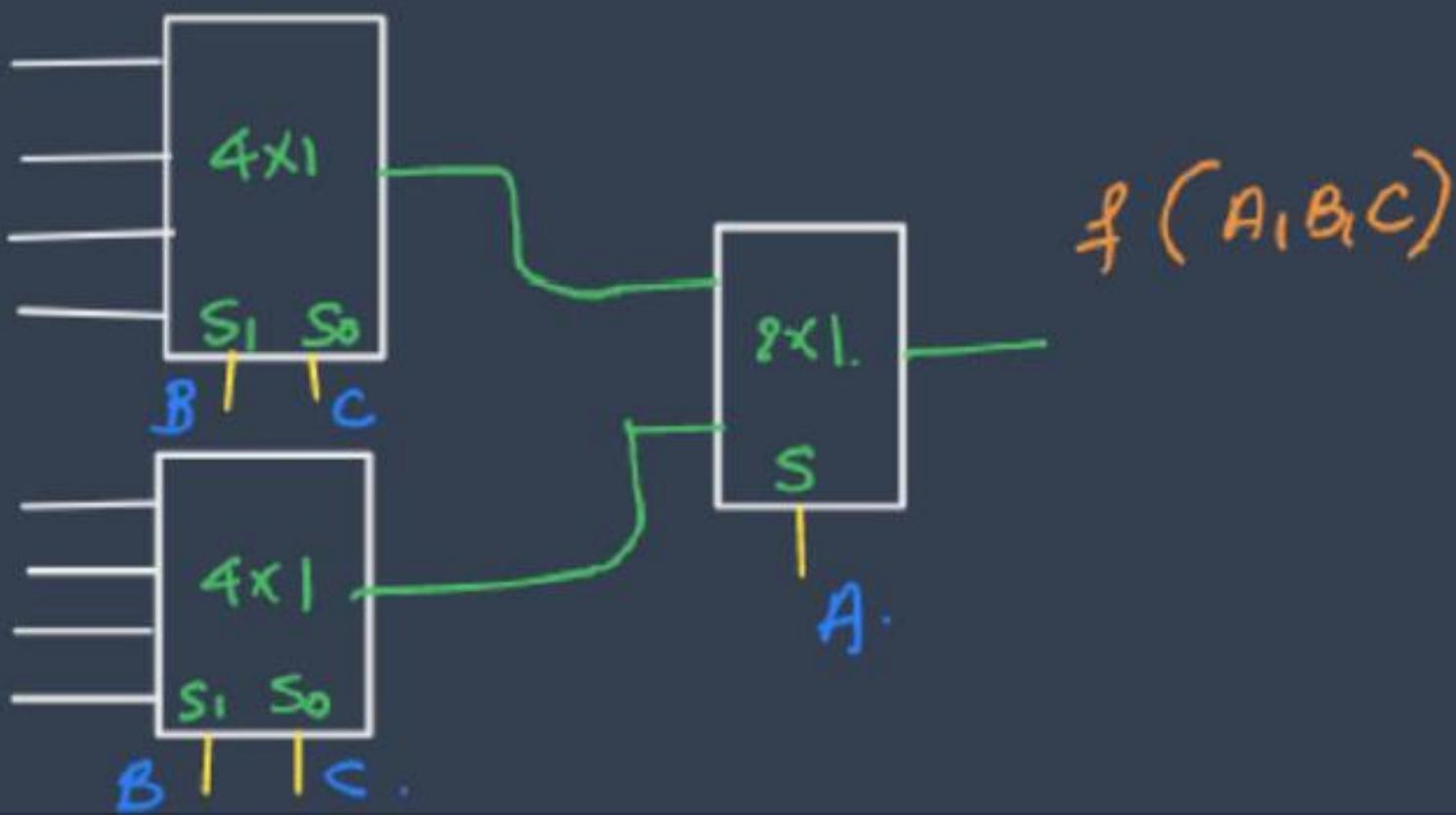
$$\frac{2}{4} = ? \quad (2 \times 1) \quad L_3 \quad (\text{MSB})$$



Q) Design  $8 \times 1$  MUX using  $4 \times 1$  MUX

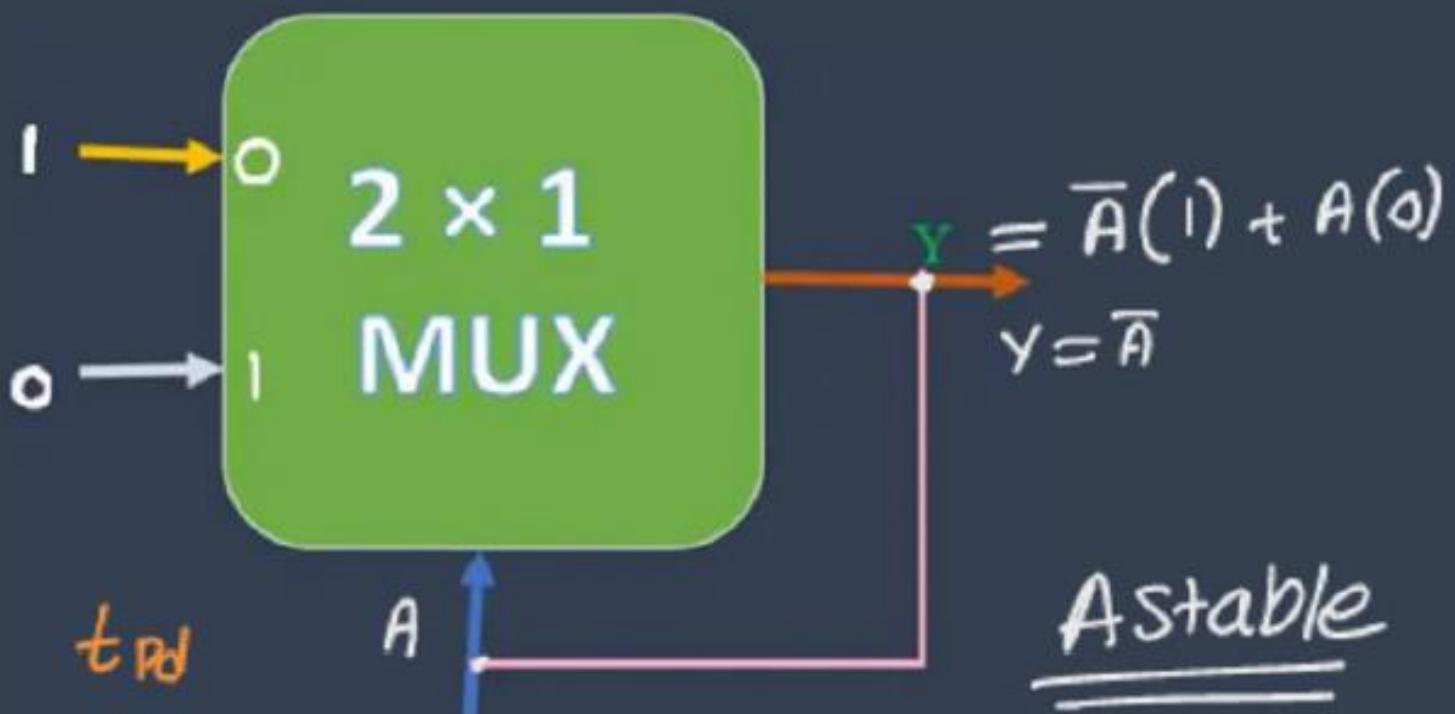
$$\frac{8}{4} = 2 \quad L_1$$

$$\frac{2}{4} = (2 \times 1) \quad L_2.$$



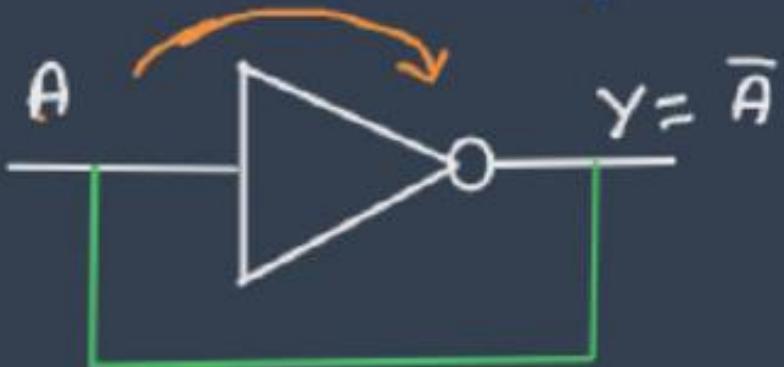
# Delay Analysis of MUX

Q) Draw the output waveform of the circuit , if the delay of the MUX is  $t_{pd}$

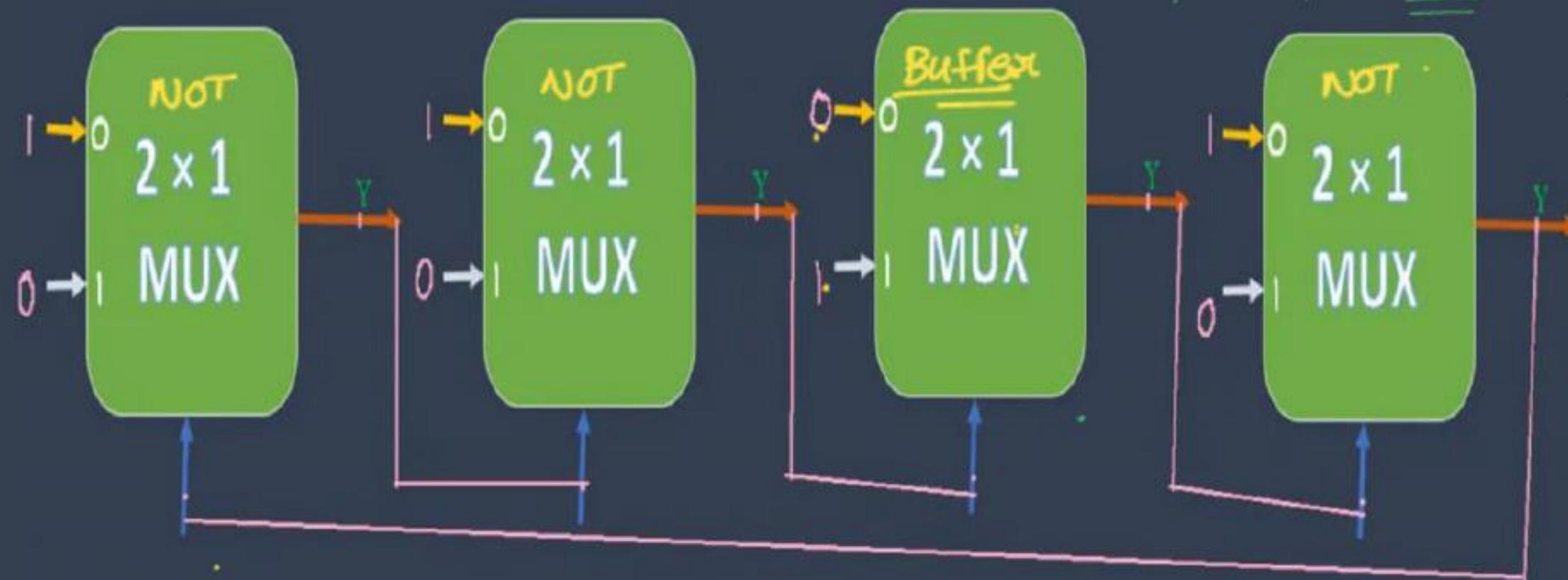
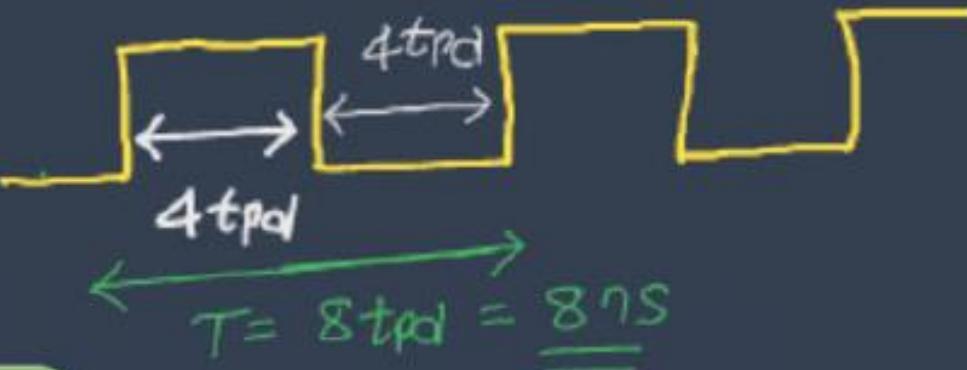
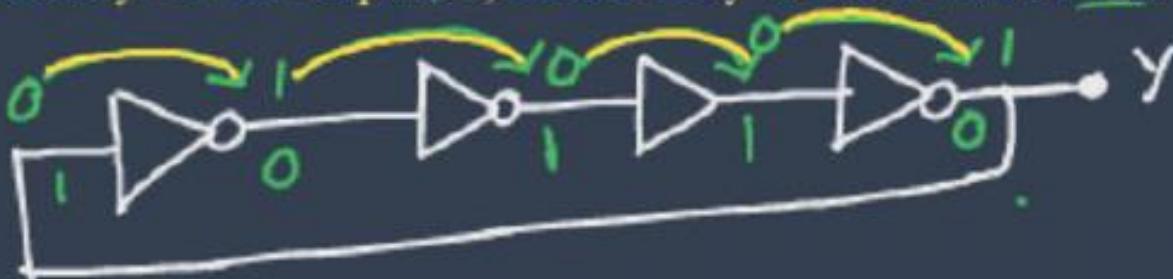


$$f = \frac{1}{\tau} = \frac{1}{2t_{pd}}$$

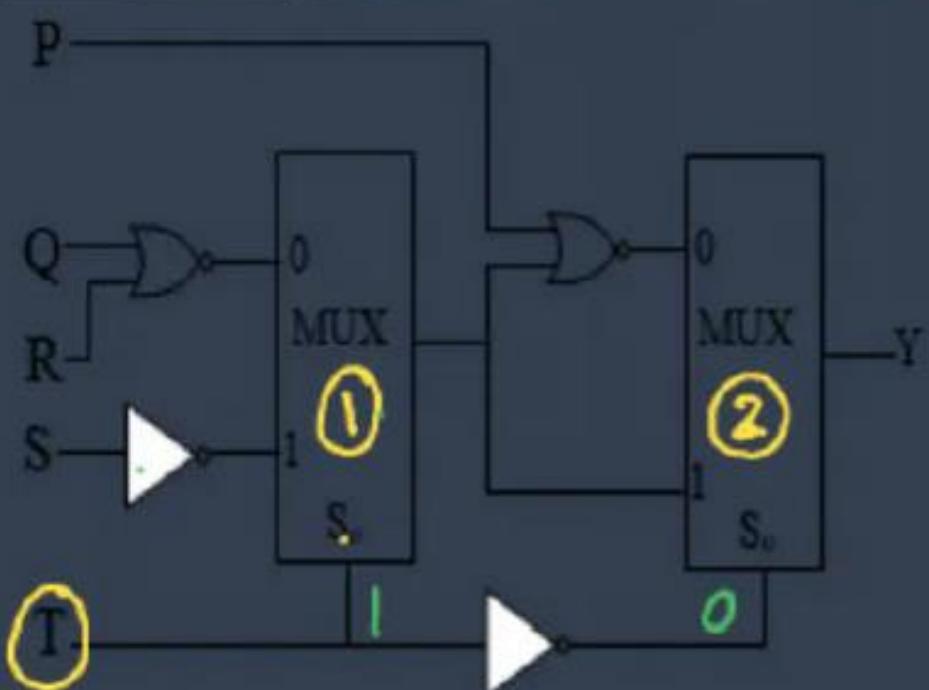
A Stable



Q) Find the delay of the output Y, if the delay of each mux is 1ns



For the circuit shown in figure, the delays of NOR gates, multiplexer and inverters are 2ns, 1.5ns and 1ns, respectively. If all the inputs P,Q,R,S and T are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is 6 ns



$$\underline{T=0}$$

$$\text{Delay} = (t_{pd})_{\text{NOR}} + (t_{pd})_{\text{MUX1}} + (t_{pd})_{\text{MUX2}}$$

$$= 2 + 1.5 + 1.5 = 5 \text{ ns}$$

$$\underline{T=1}$$

$$\text{Delay} = (t_{pd})_{\text{NOT}} + (t_{pd})_{\text{MUX1}} + (t_{pd})_{\text{NOR}} + (t_{pd})_{\text{MUX2}}$$

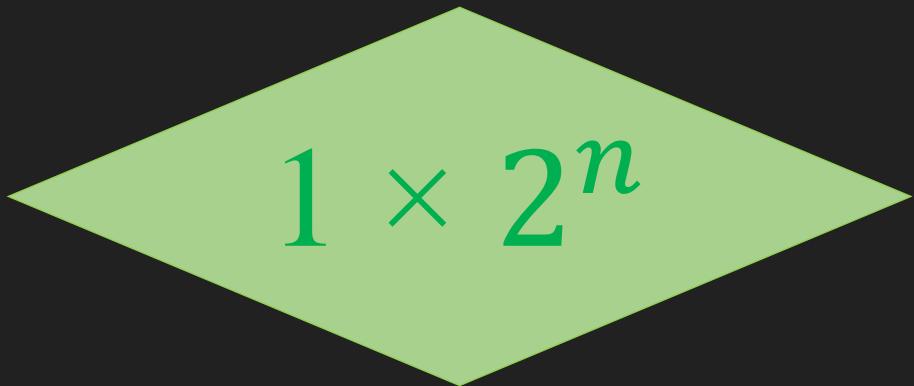
$$= \underline{\underline{6 \text{ ns}}}$$

# Demultiplexer

A demultiplexer is a circuit that receives information on a single line and transmits to one of the  $2^n$  possible output lines , according to the selection lines

- One input to many output
- Data distributor
- One to many circuit

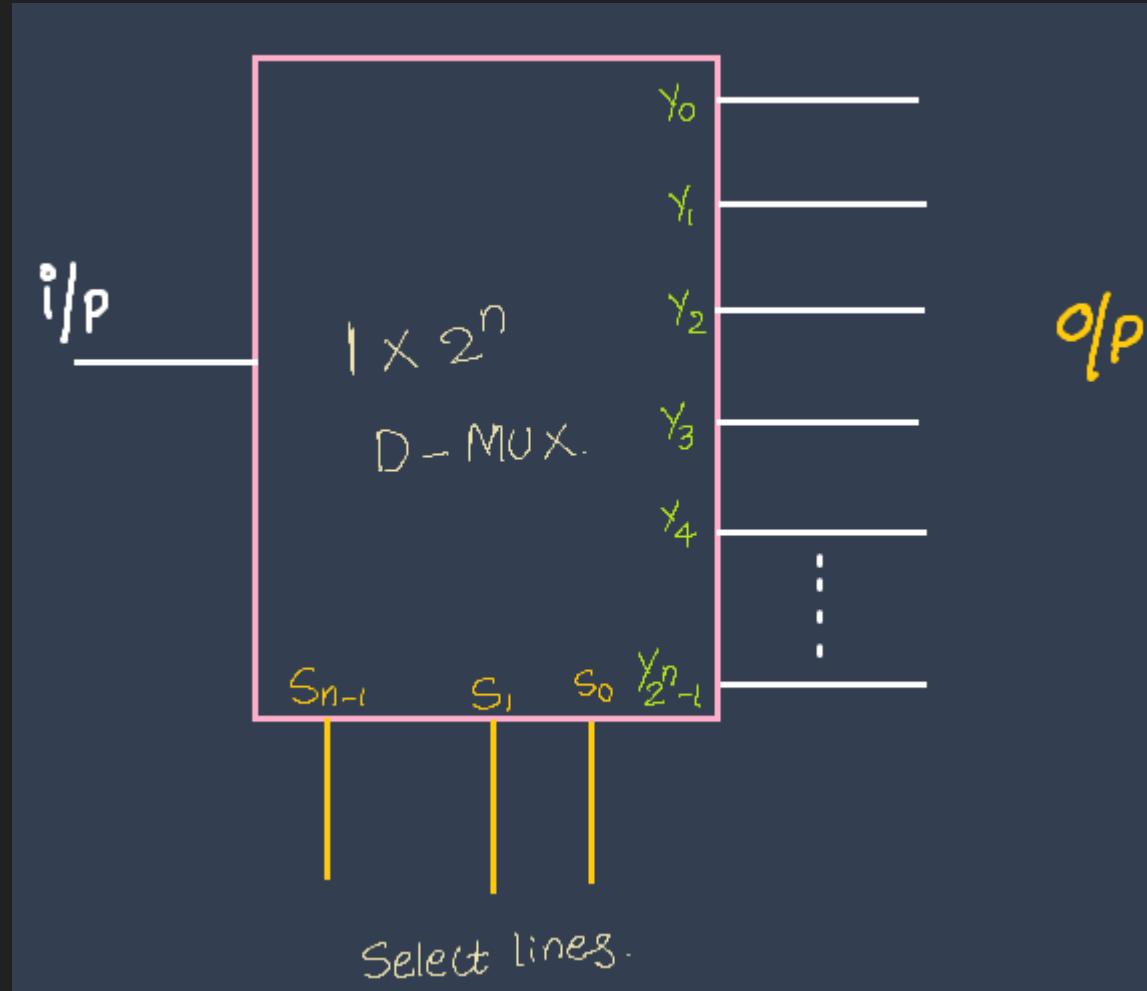
## General structure



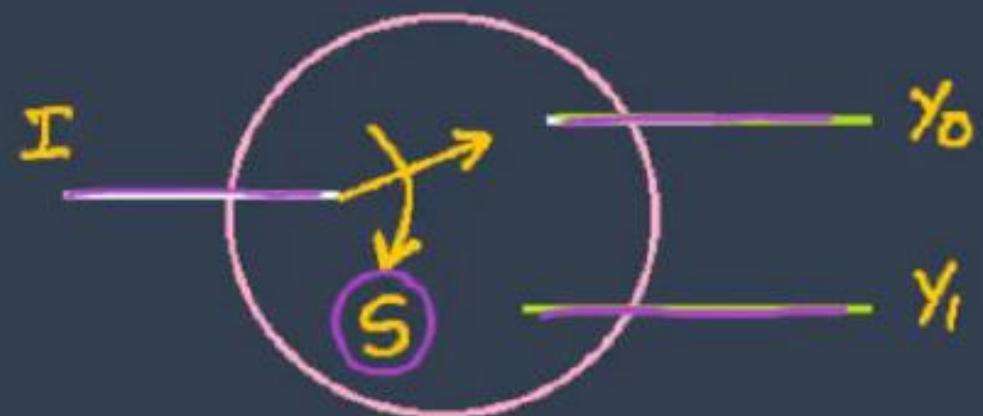
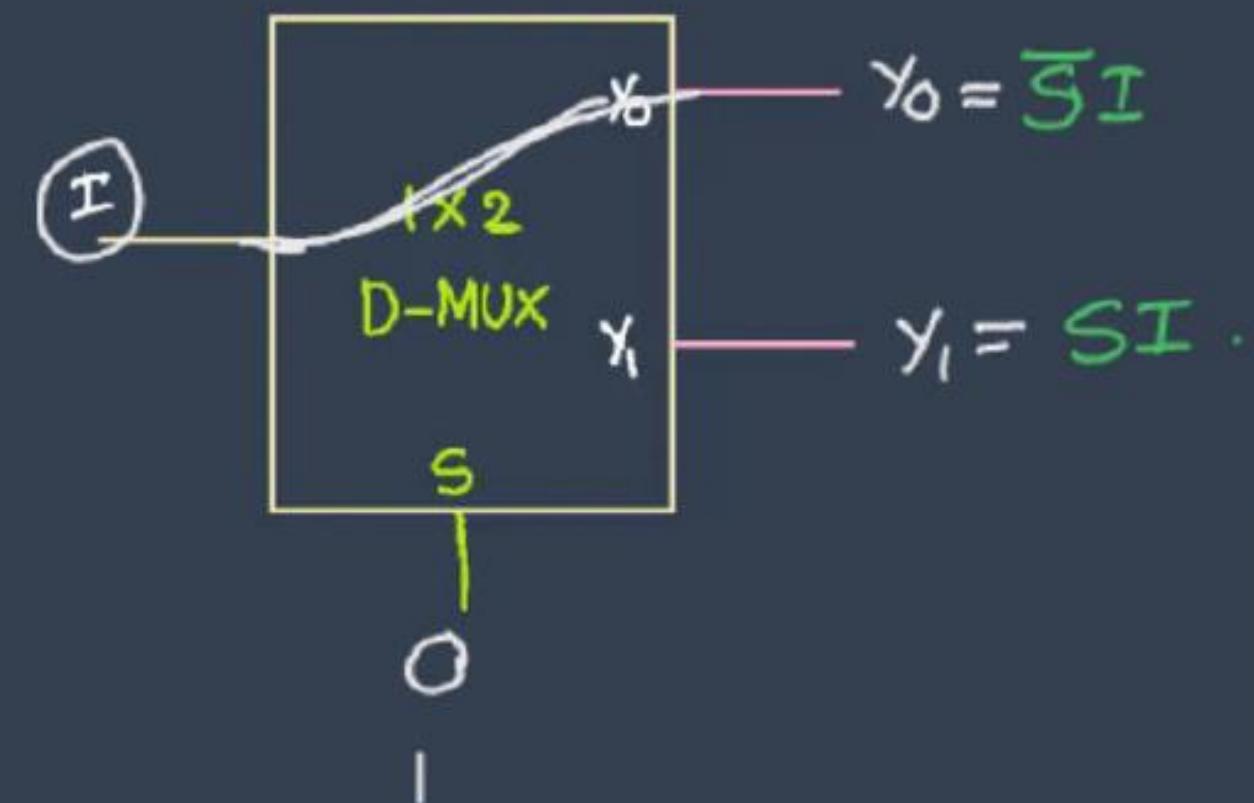
$n$  -----> number of select lines

$2^n$  -----> number of output lines

1 -----> number of inputs



# $1 \times 2$ DEMUX



$S$	$Y_0$	$Y_1$
0	I	0
1	0	I

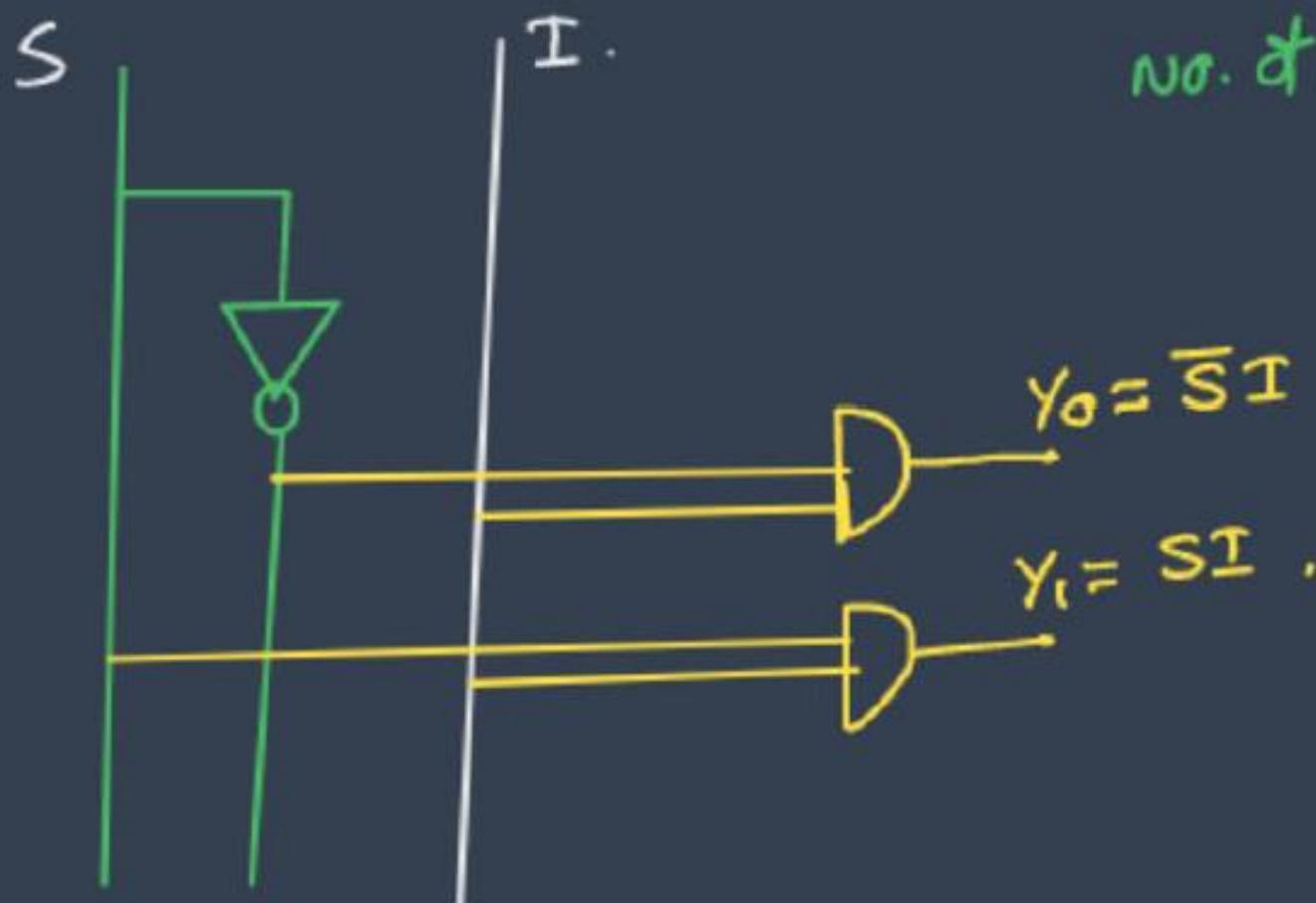
# Logic circuit

$$y_0 = \overline{S}T$$

$$y_1 = ST.$$

No. of AND gates = 2

No. of NOT gates = 1.

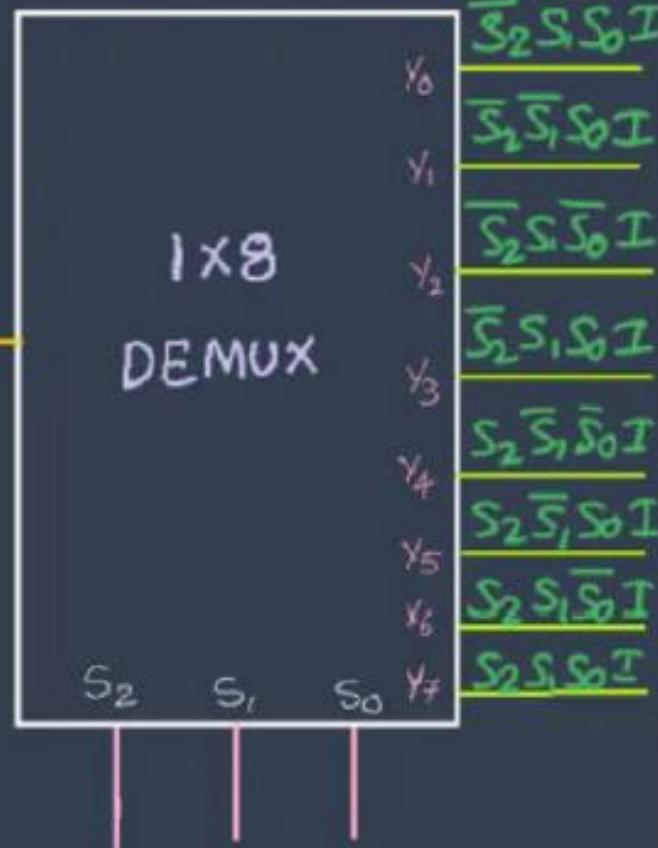


# $1 \times 4$ Demultiplexers



# 1 × 8 DEMUX

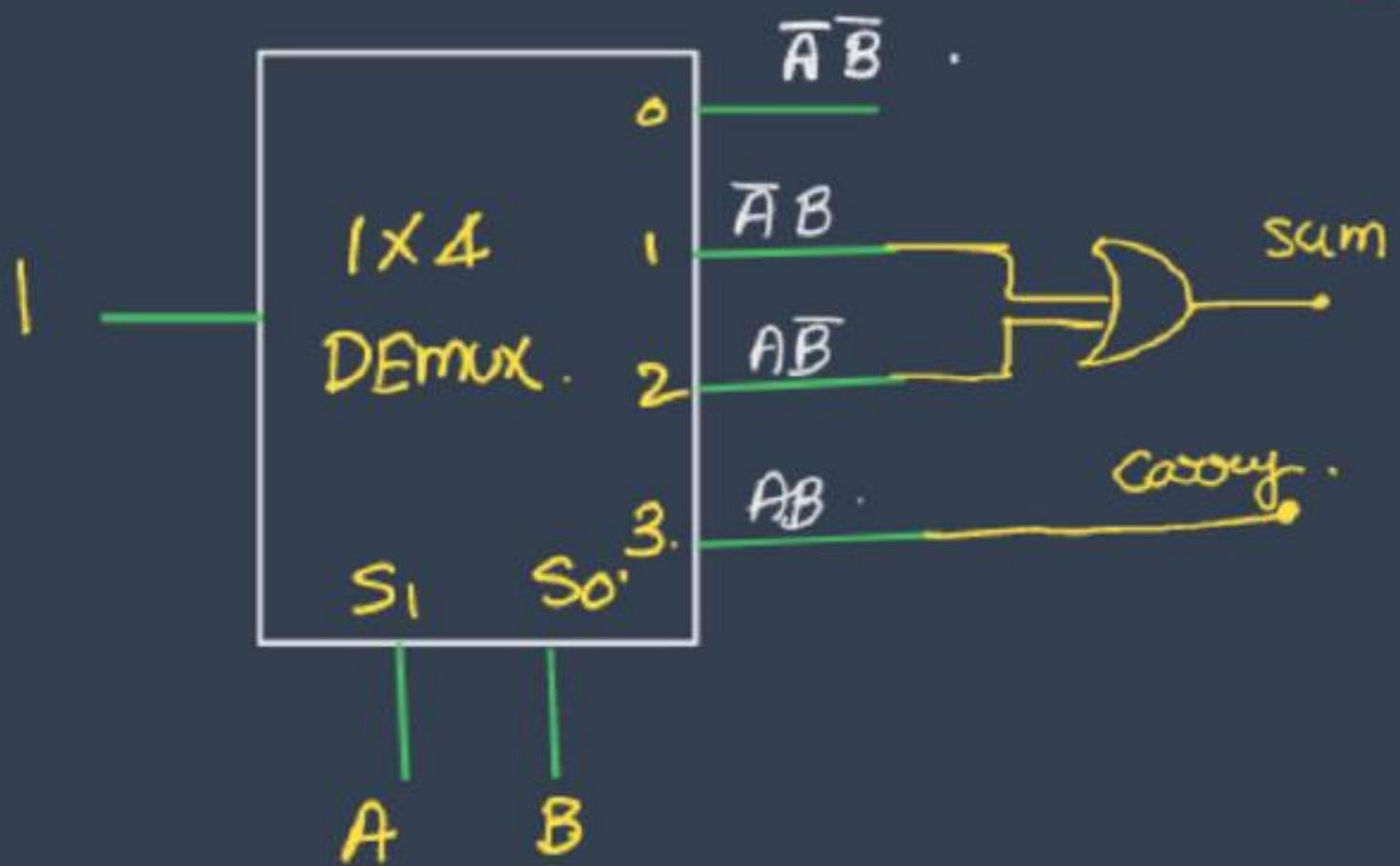
I



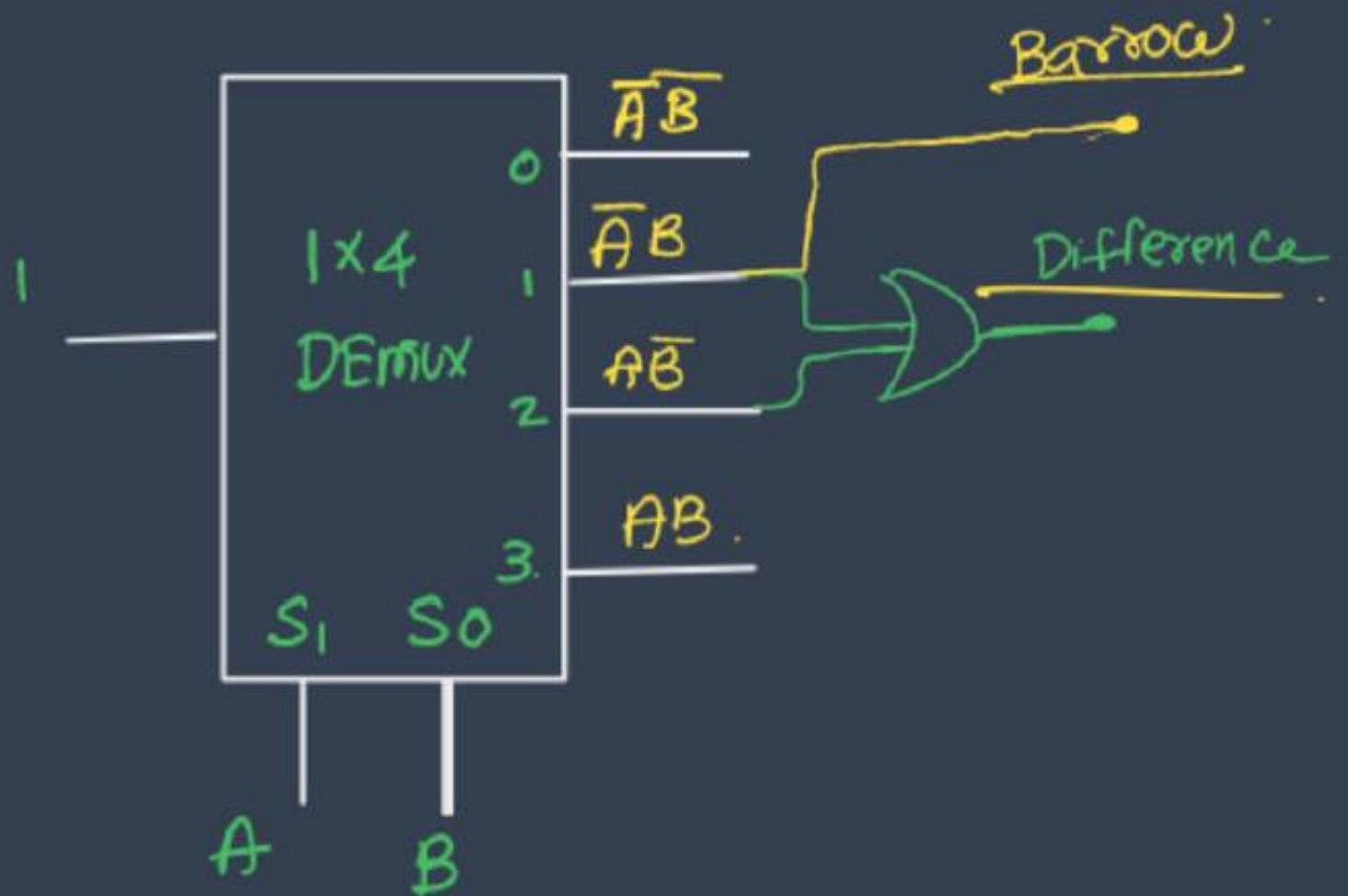
S2	S1	S0	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0	0	0	I
0	0	1	0	0	0	0	0	0	I	0
0	1	0	0	0	0	0	0	+	0	0
0	1	1	0	0	0	0	I	0	0	0
1	0	0	0	0	0	+	0	0	0	0
1	0	1	0	0	+	0	0	0	0	0
1	1	0	0	I	0	0	0	0	0	0
1	1	1	I	0	0	0	0	0	0	0

Q) Implement HA using  $1 \times 4$  Demux

$$\begin{aligned} S &= A \oplus B \\ C &= AB \end{aligned}$$



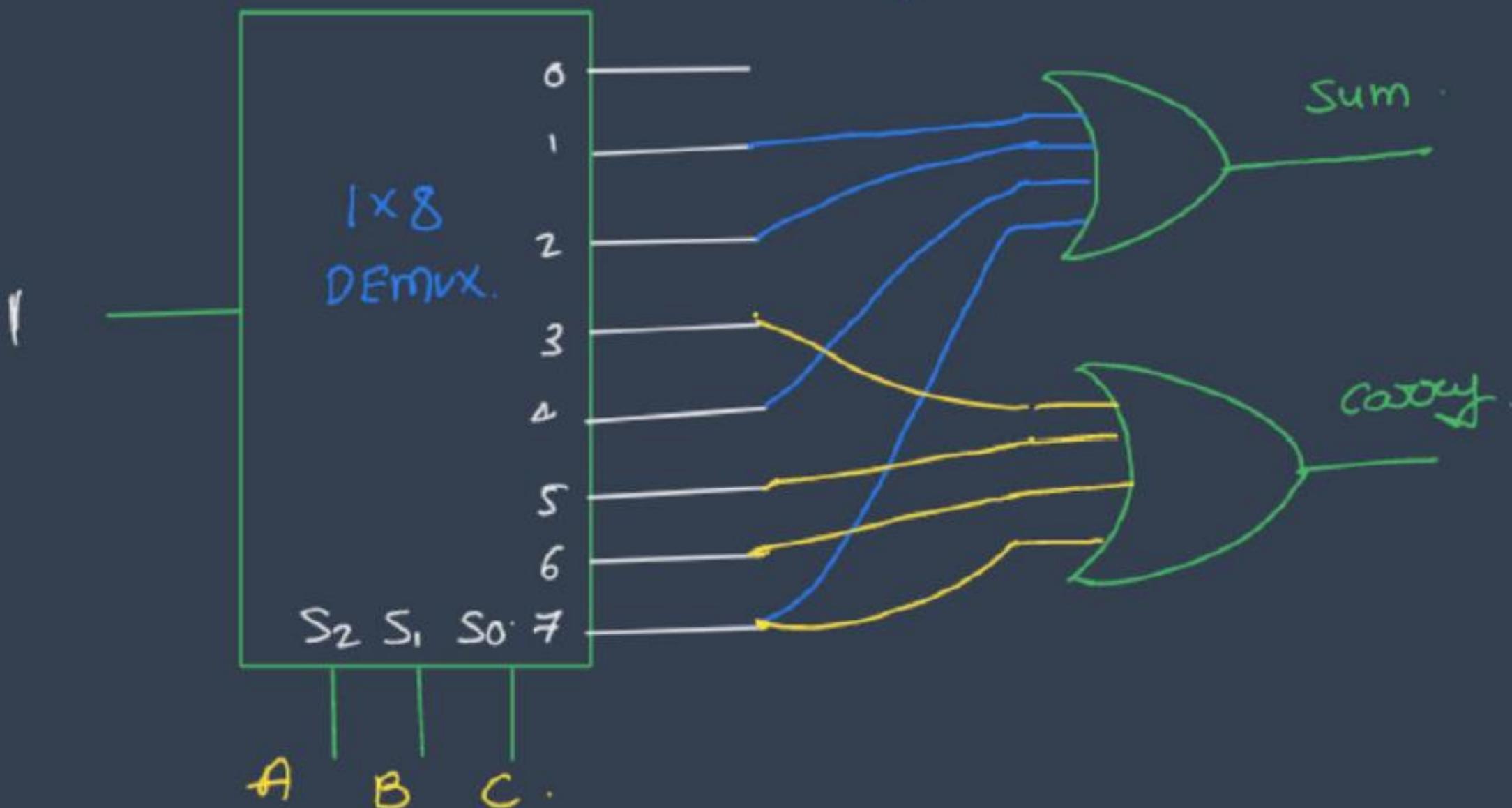
Q) Implement HS using  $1 \times 4$  Demux



Q) Implement FA using  $1 \times 8$  Demux

$$\text{Sum} = \sum m(1, 2, 4, 7)$$

$$\text{carry} = \sum m(3, 5, 6, 7).$$



# Implementation of higher order Demux using lower order Demux

Q) Implement  $1 \times 4$  Demux using  $1 \times 2$  Demux

$$\frac{4}{2} = 2$$

L2

$$\frac{2}{2} = 1$$

L1

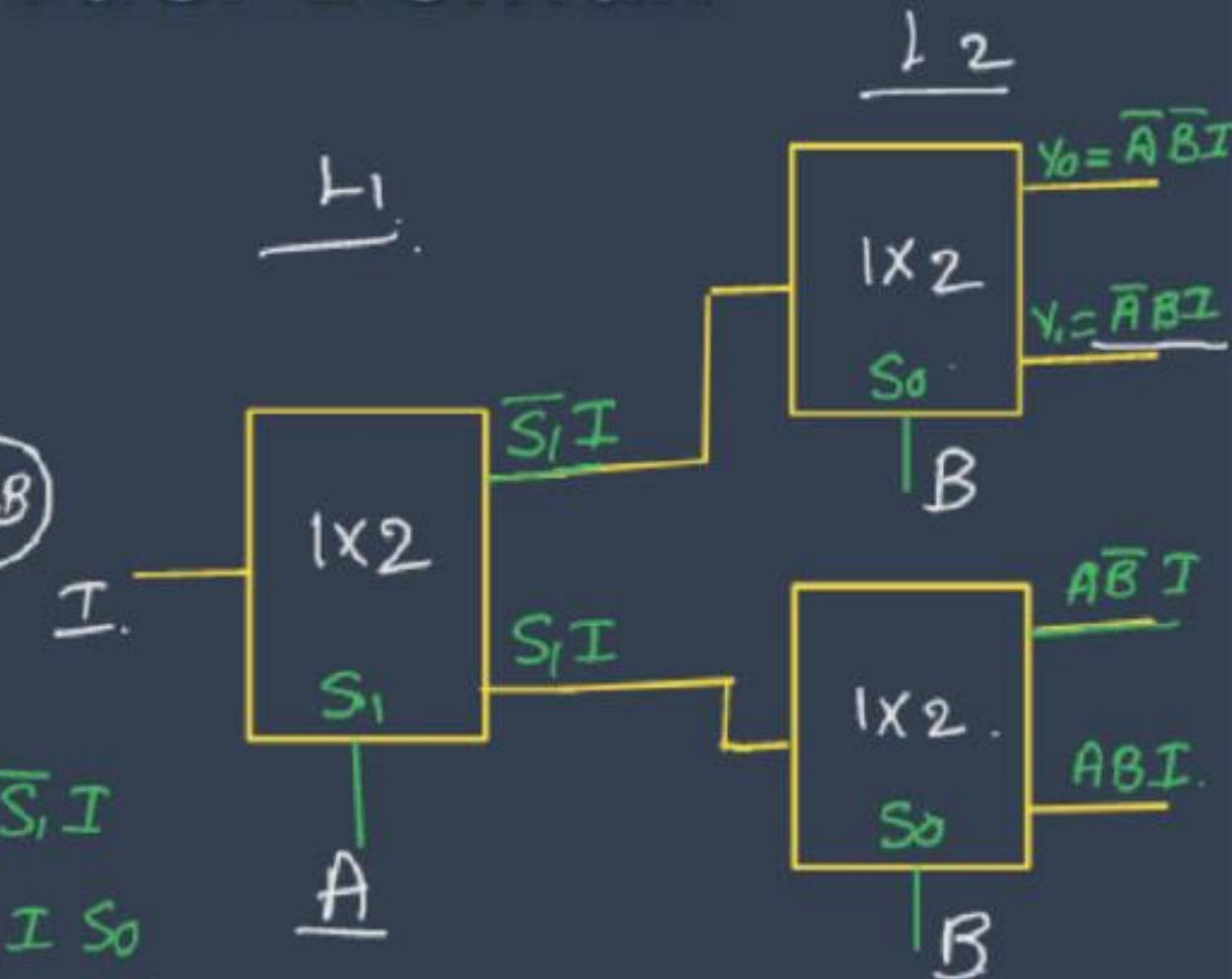
MSB

$$y_2 = \overline{s}_0 s_1 I$$

③

$$y_0 = \overline{s}_0 \overline{s}_1 I$$

$$y_1 = \overline{s}_1 I s_0$$



Q) Implement  $1 \times 16$  Demux using  $1 \times 2$  Demux

$$\frac{16}{2} = 8 \quad \textcircled{L_4} \quad (\text{LSB})$$

$$\frac{8}{2} = 4 \quad \textcircled{L_3}$$

$$\frac{4}{2} = 2 \quad \textcircled{L_2}$$

$$\frac{2}{2} = 1 \quad \textcircled{L_1} \quad (\text{MSB})$$

---

(15)

Q) Implement  $1 \times 8$  Demux using  $1 \times 4$  Demux

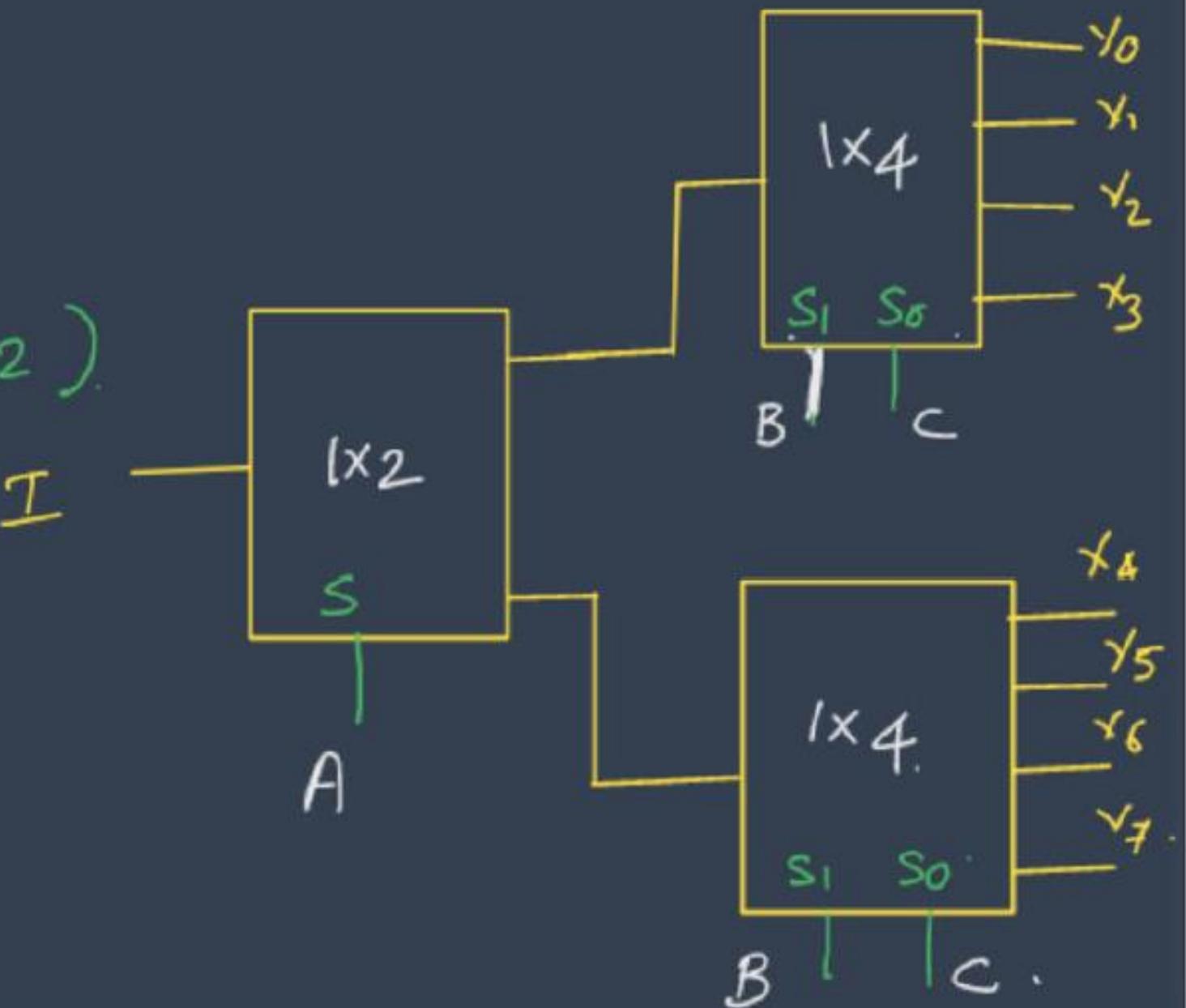
$$\frac{8}{4} = 2$$

$$\frac{2}{4} = ? (1 \times 2)$$

$$f(A, \underline{B}, C)$$

---

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# Decoder

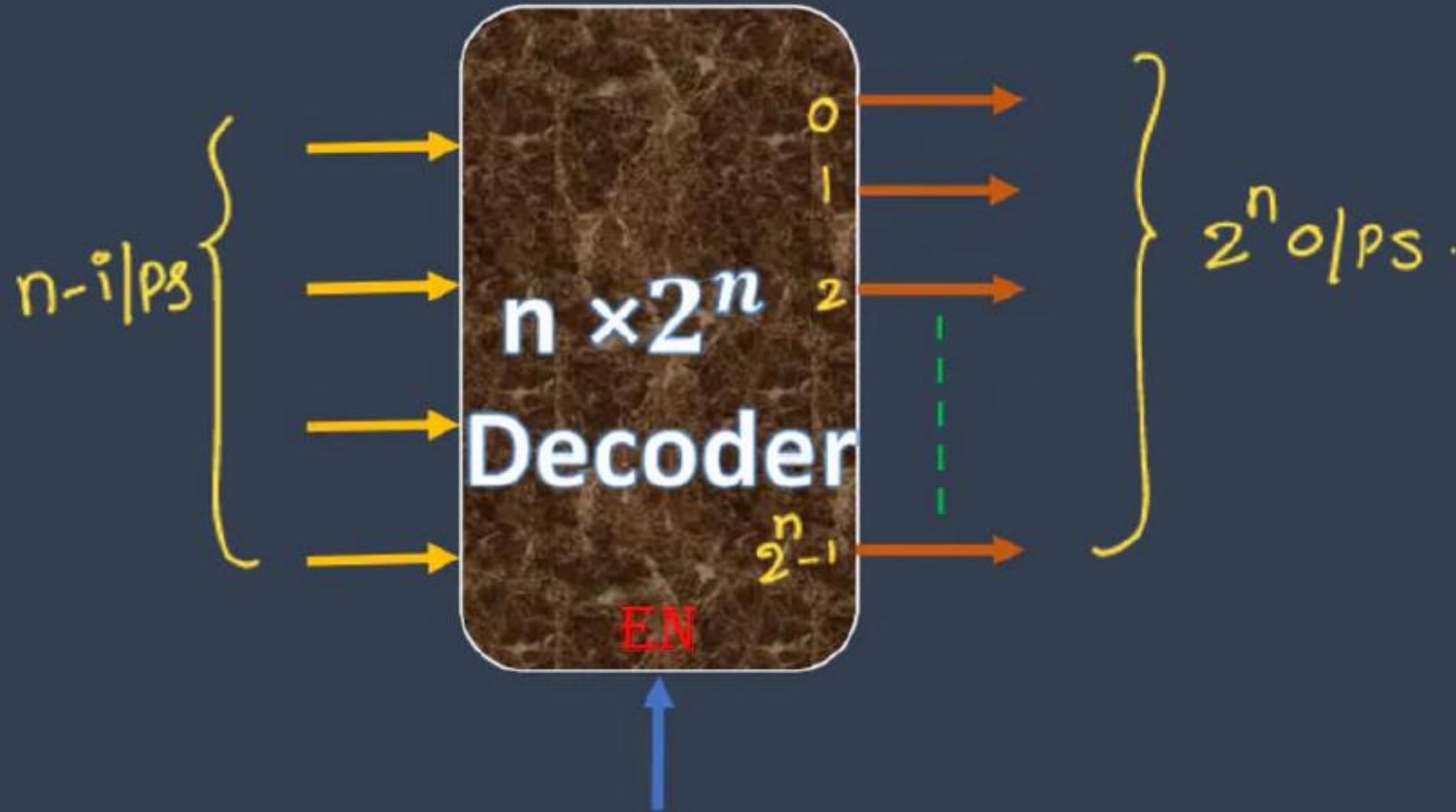
Decoder is a multi input ,multi output logic circuit which converts coded input into coded output , where the input and output codes are different

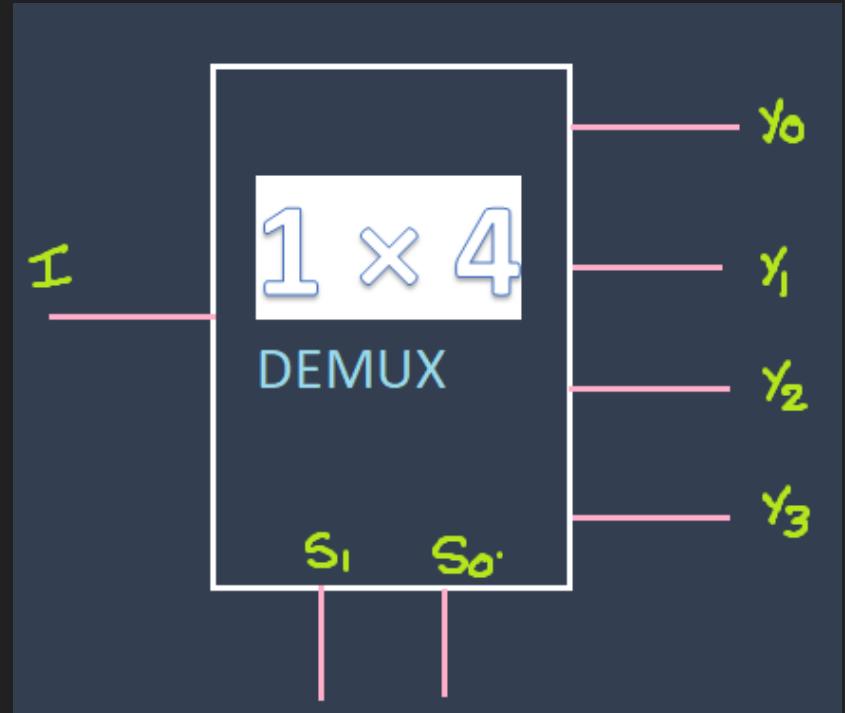
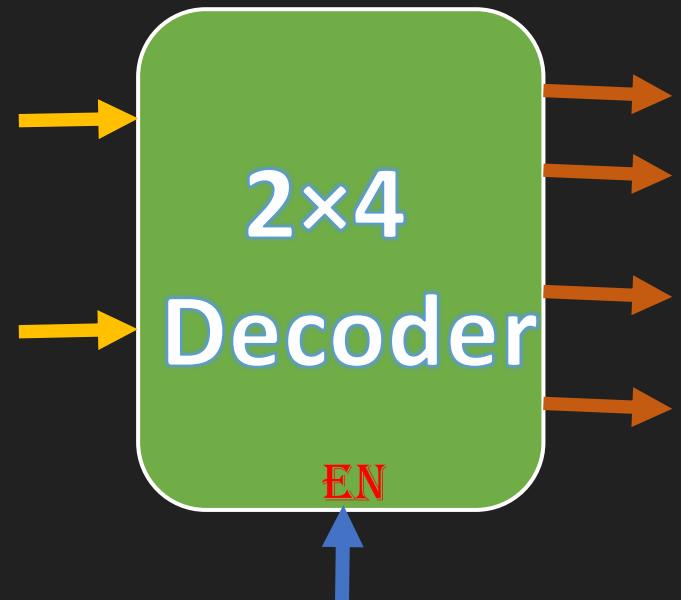
## General structure

$$n \times 2^n$$

$n$  -----> number of inputs

$2^n$  -----> number of outputs



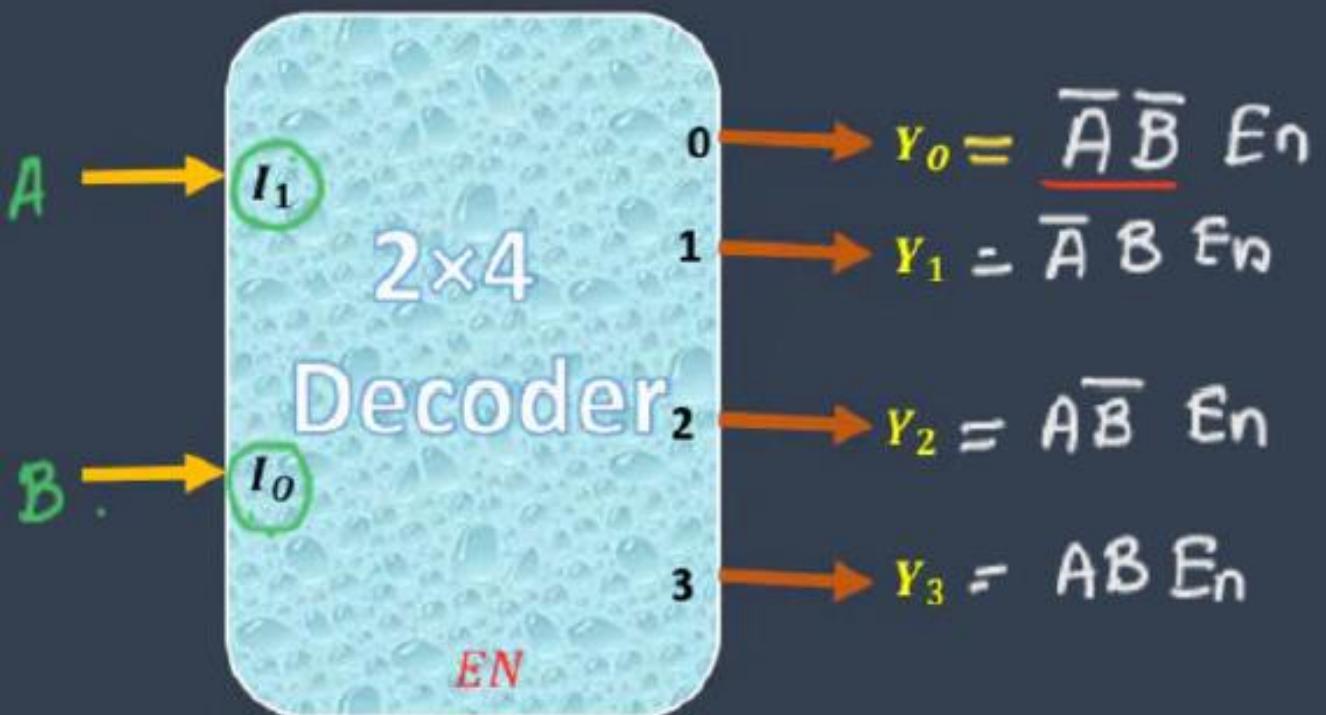


Inputs  $\longleftrightarrow$  Enable

Select lines  $\longleftrightarrow$  Inputs

Decoder is a special case of Demux , in which the select lines or Demux are treated as input's to the decoder and input of Demux is treated as Enable input of the Decoder

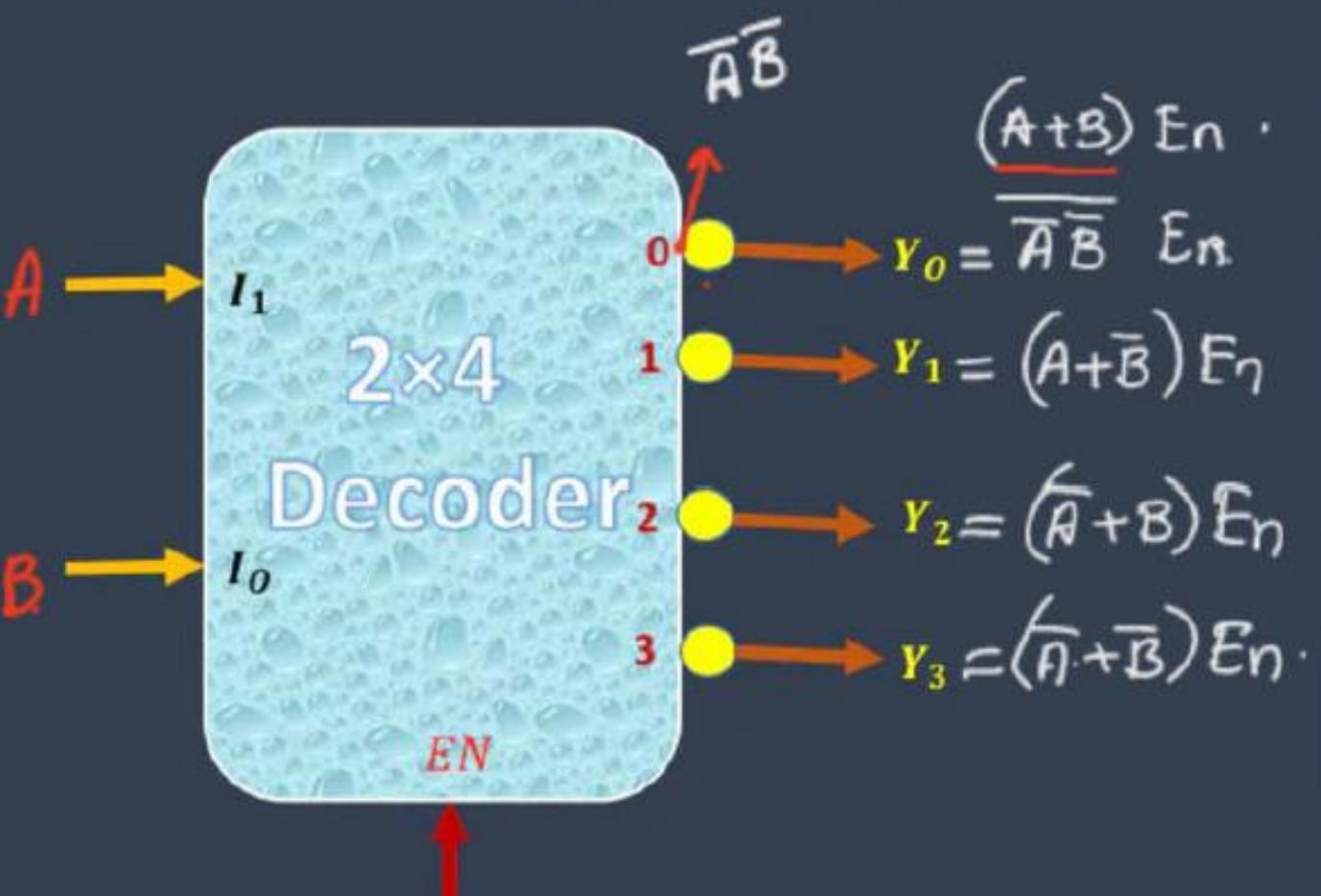
# Active High Decoder



If  $\underline{EN} = 1$ , decoder works.  
 $= 0$ , decoder is disable.

En	A	B	$Y_3$	$Y_2$	$Y_1$	$Y_0$
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

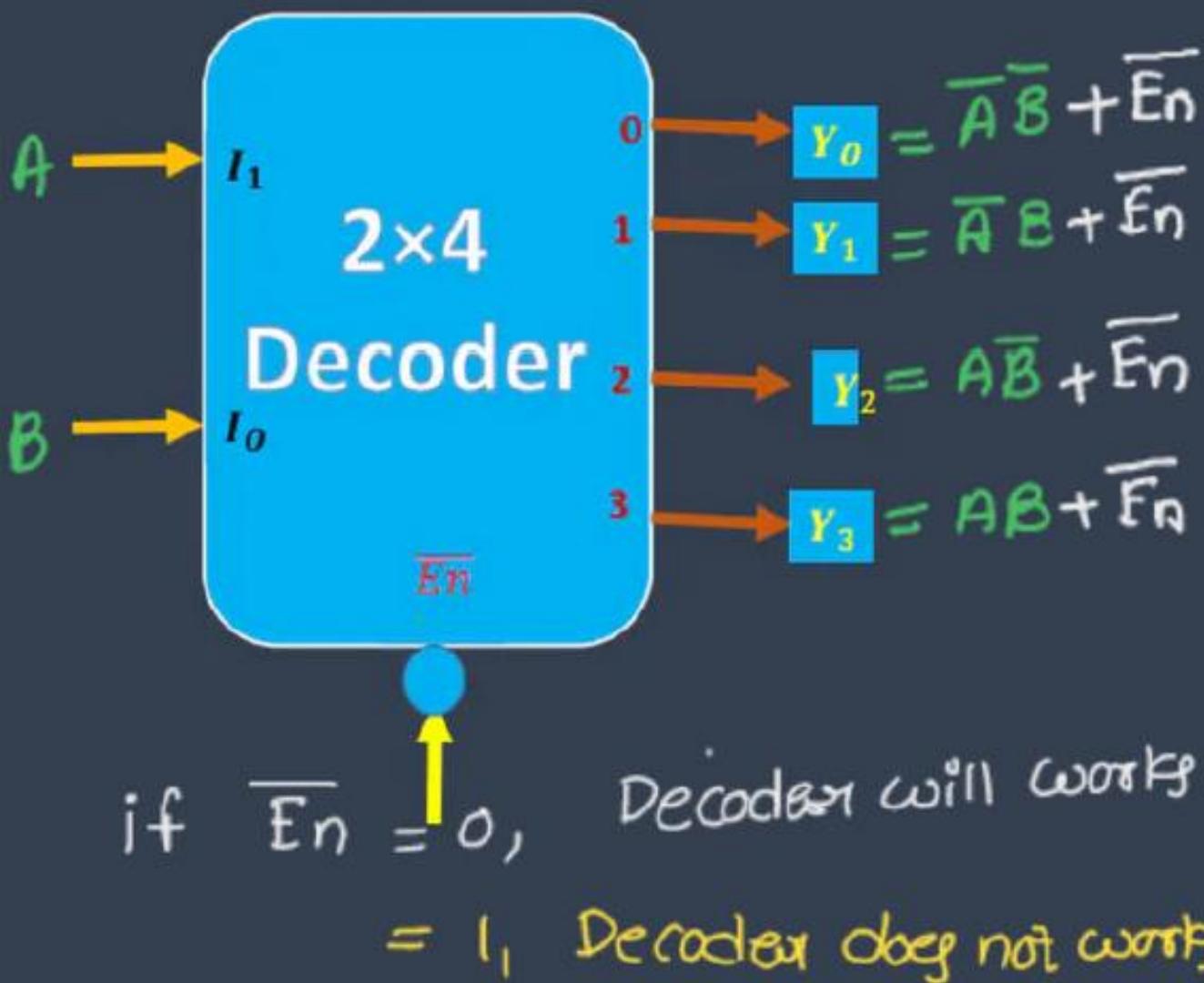
# Active High Decoder



$EN = 1$ , decoder will work.  
 $= 0$ ,  $\therefore$  does not work.

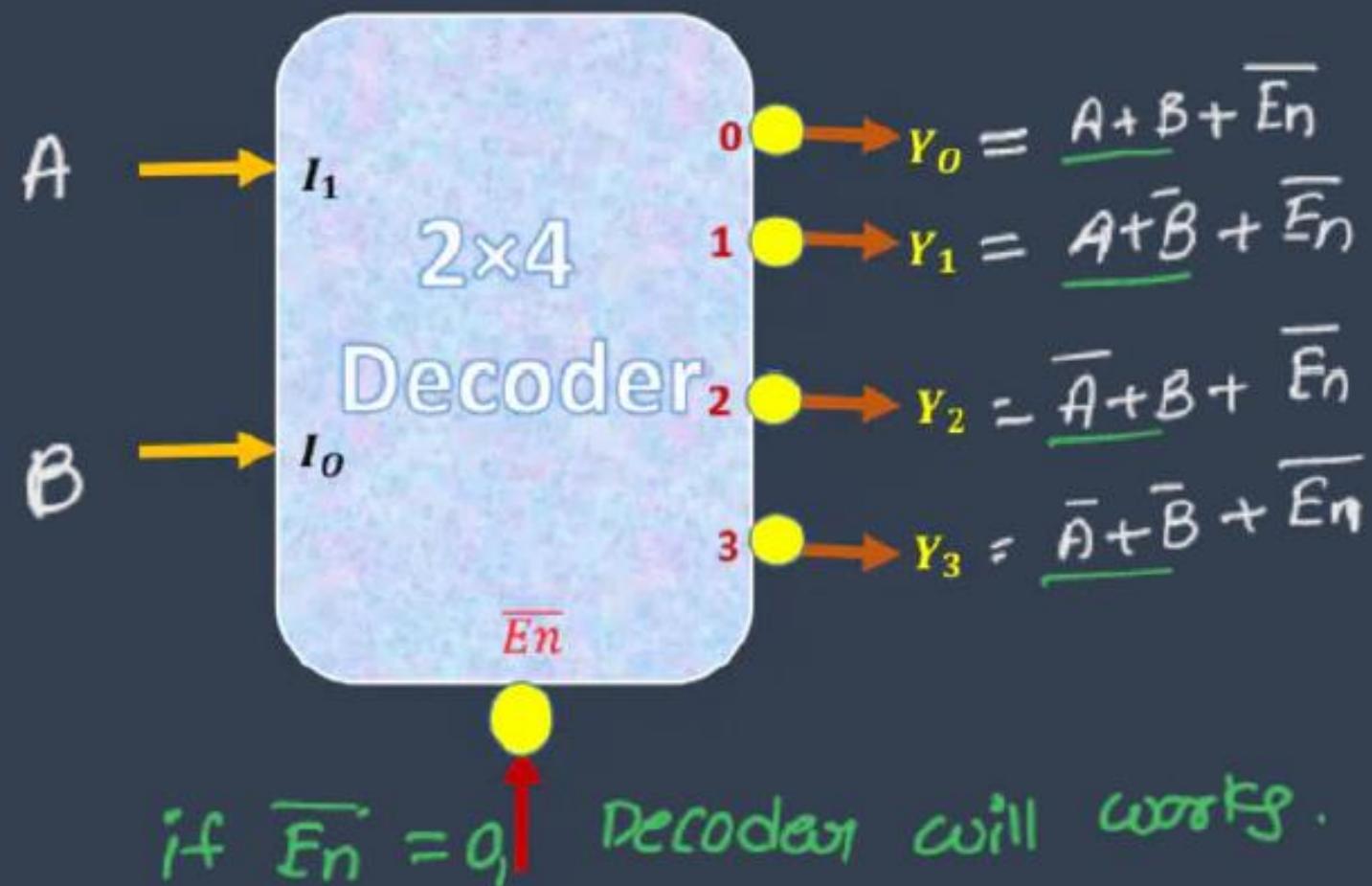
En	A	B	$Y_3$	$Y_2$	$Y_1$	$Y_0$
0	X	X	0	0	0	0
1	0	0	1	1	1	0
1	0	1	1	1	0	1
1	1	0	1	0	1	1
1	1	1	0	1	1	1

# Active Low Decoder



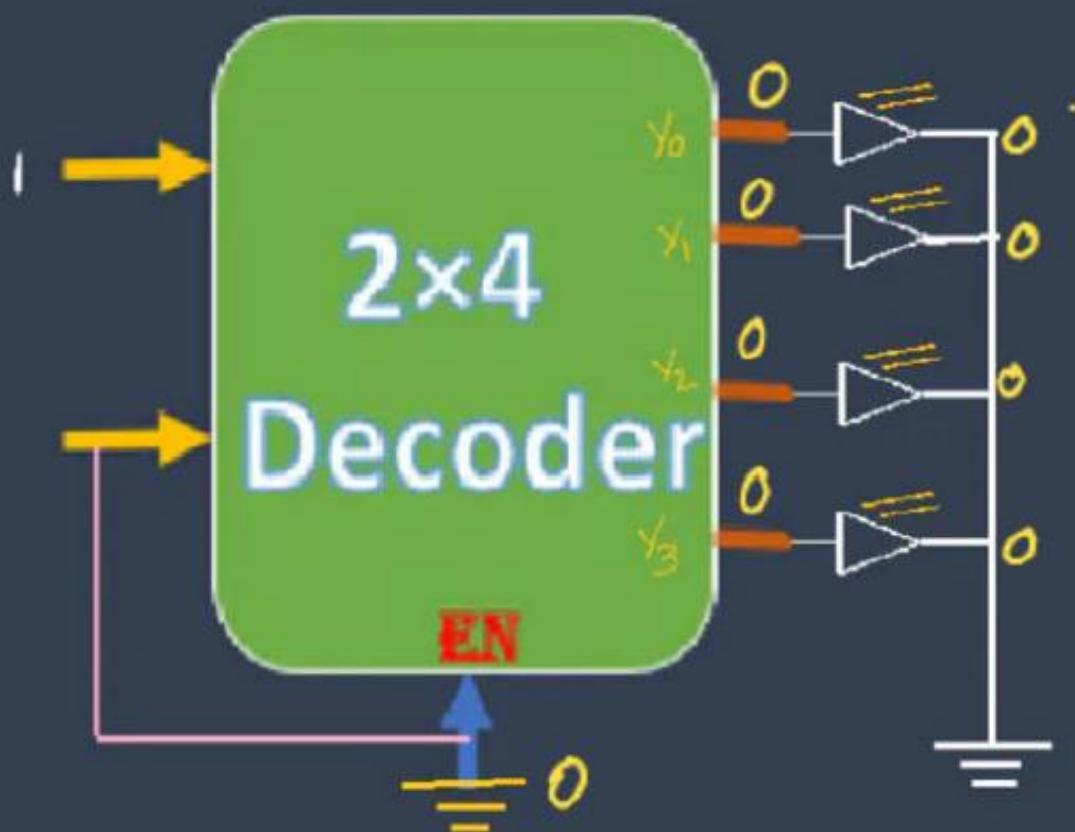
$\overline{En}$	A	B	$Y_3$	$Y_2$	$Y_1$	$Y_0$
1	X	X	1	1	1	1
0	0	0	0	0	0	1
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	0	0	0

# Active Low Decoder

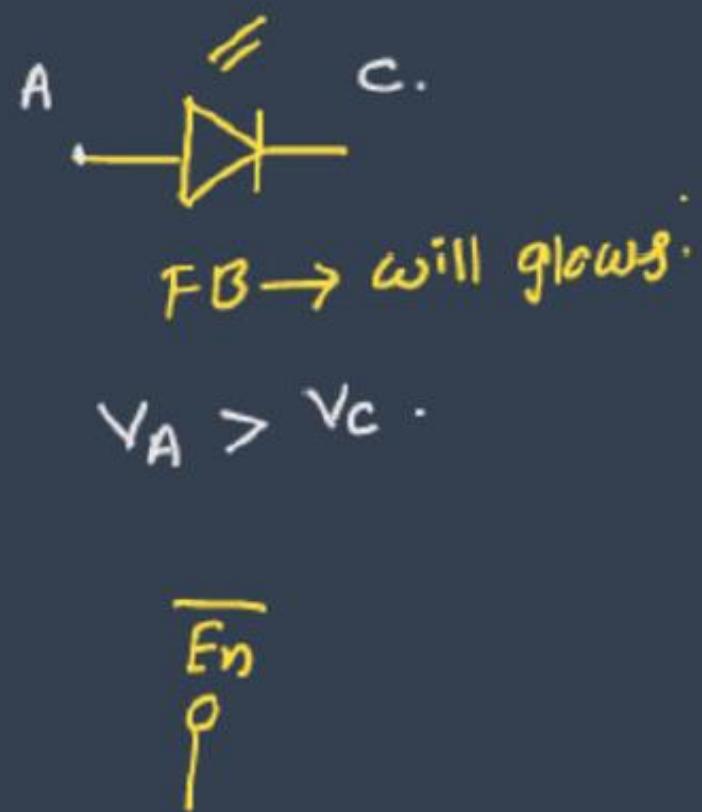


$\overline{E_n}$	A	B	$Y_3$	$Y_2$	$Y_1$	$Y_0$
1	X	X	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

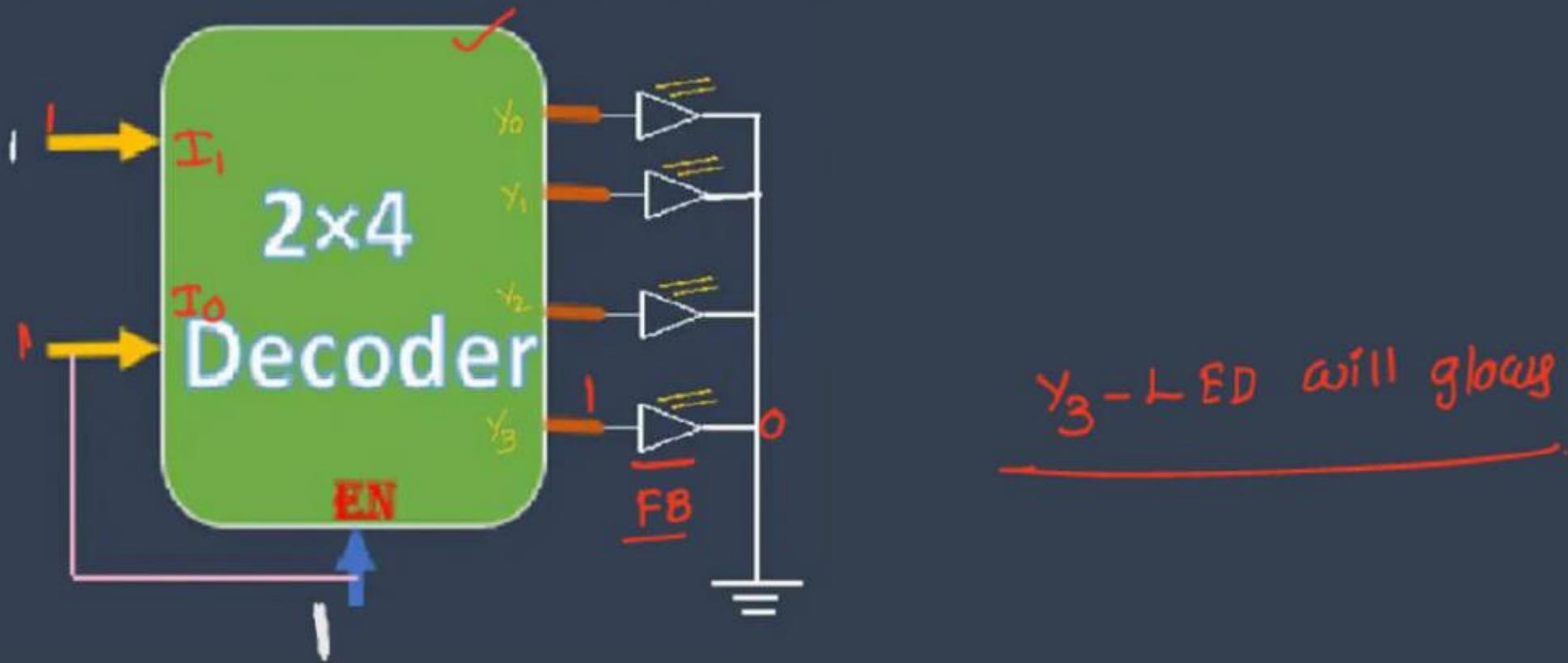
Q) Which of the following LED will glows



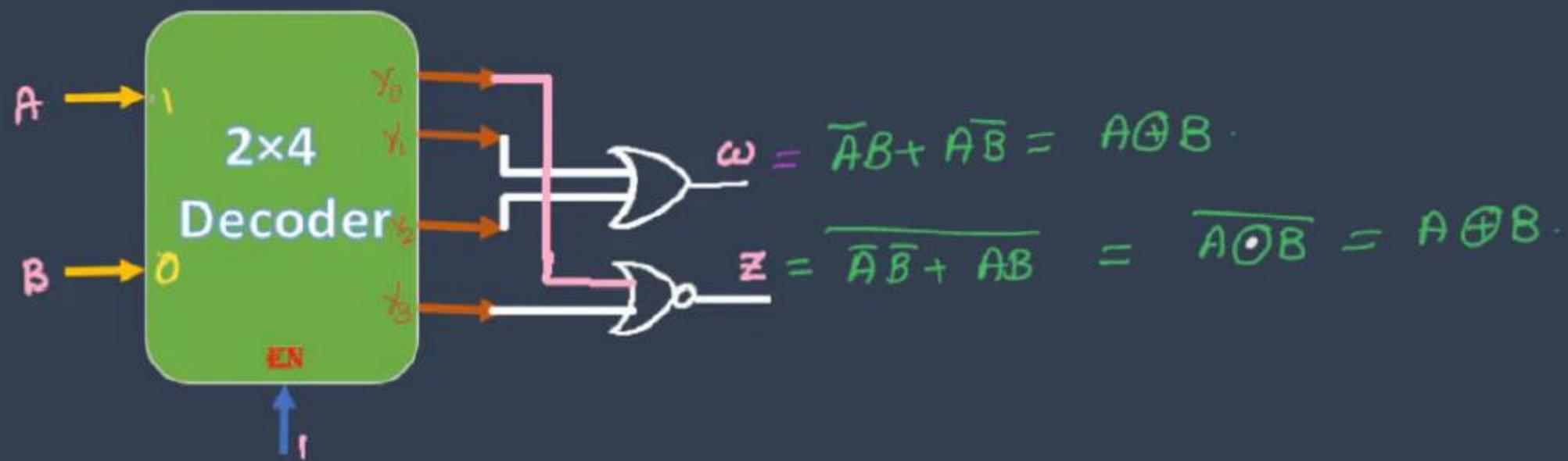
No LED will glow  $\bar{E}_n$



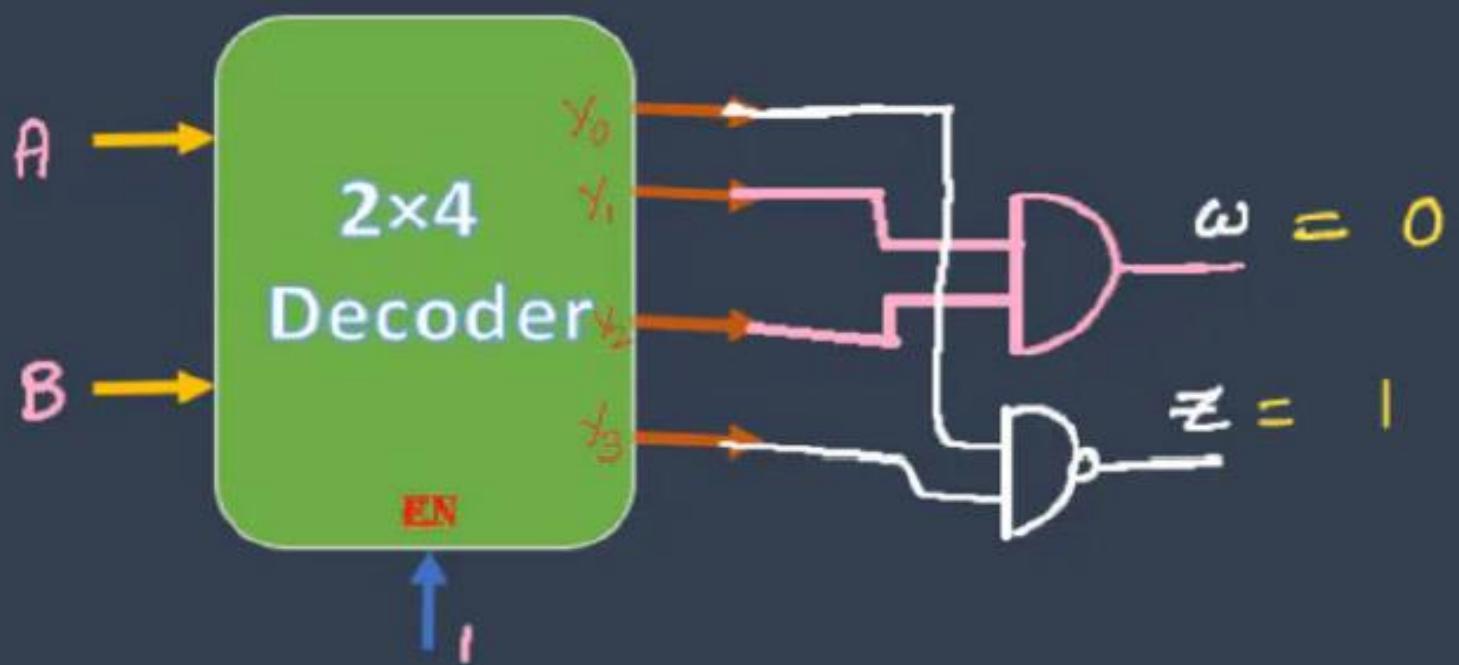
Q) Which of the following LED will glows



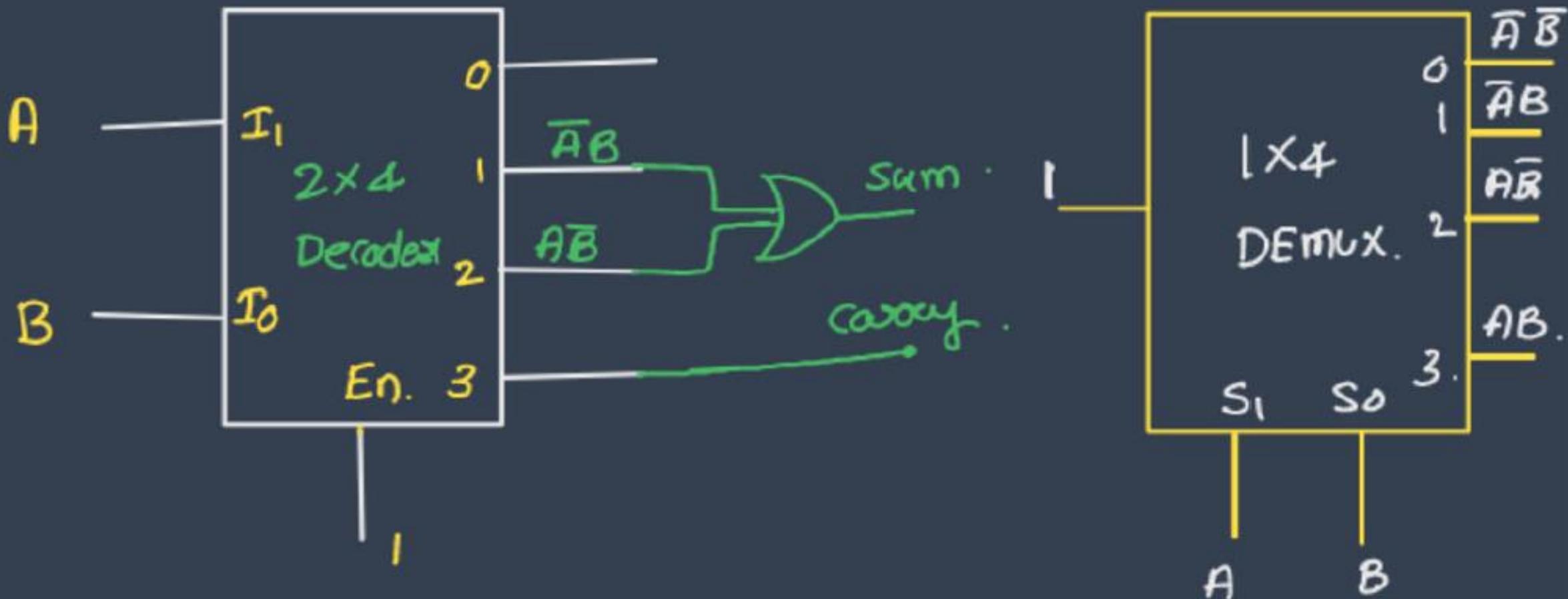
Q) Find the logic expression of W and Z



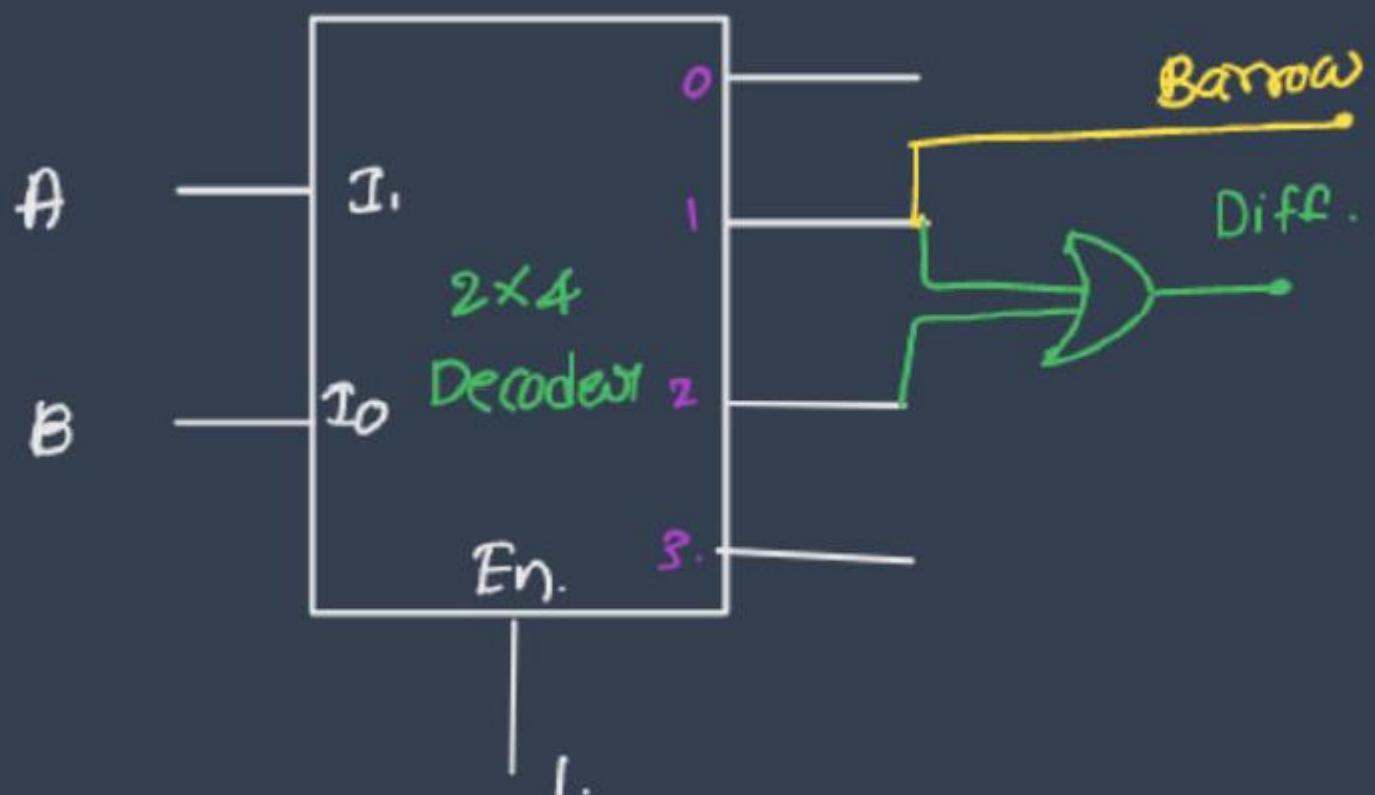
Q) Find the logic expression of W and Z



Q) Implement HA using  $2 \times 4$  decoder

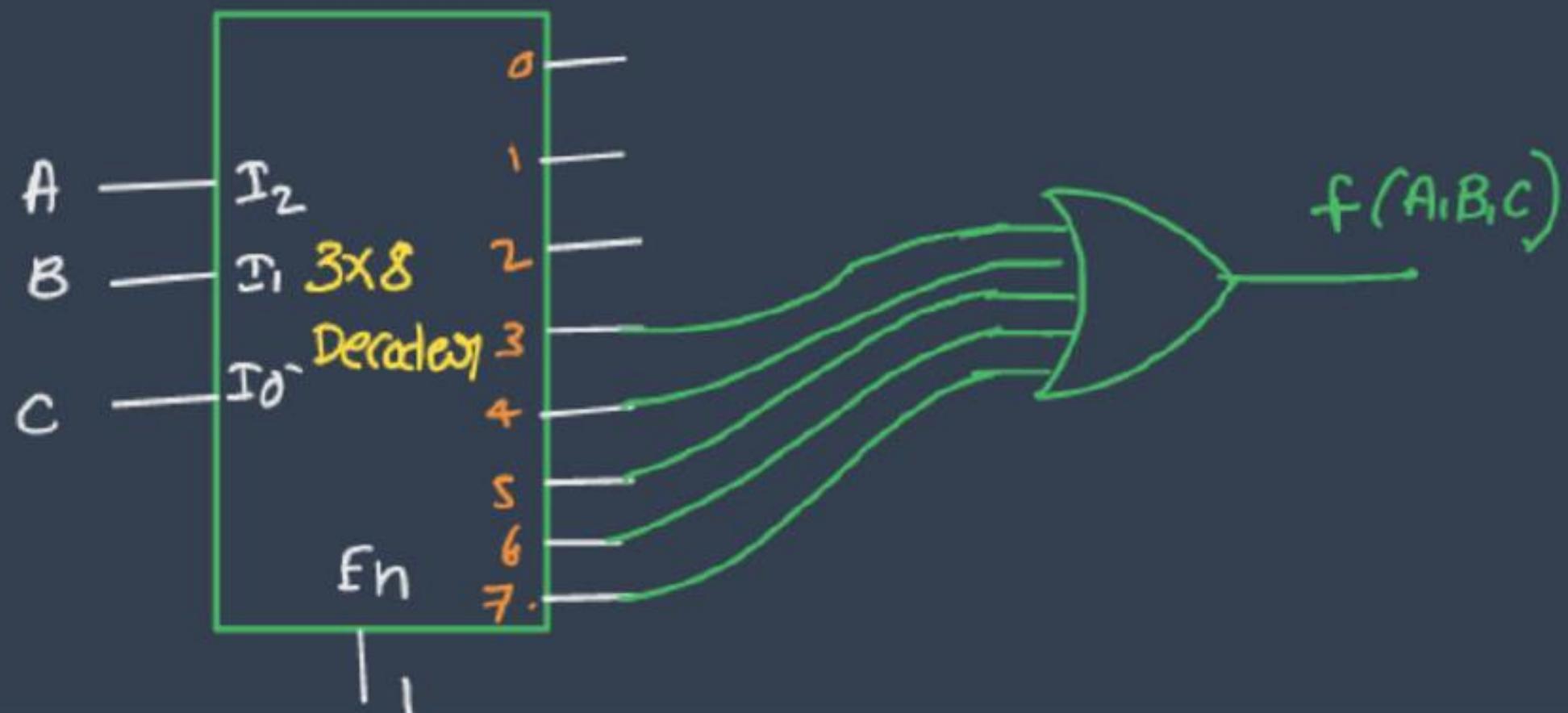


Q) Implement HS using  $2 \times 4$  decoder

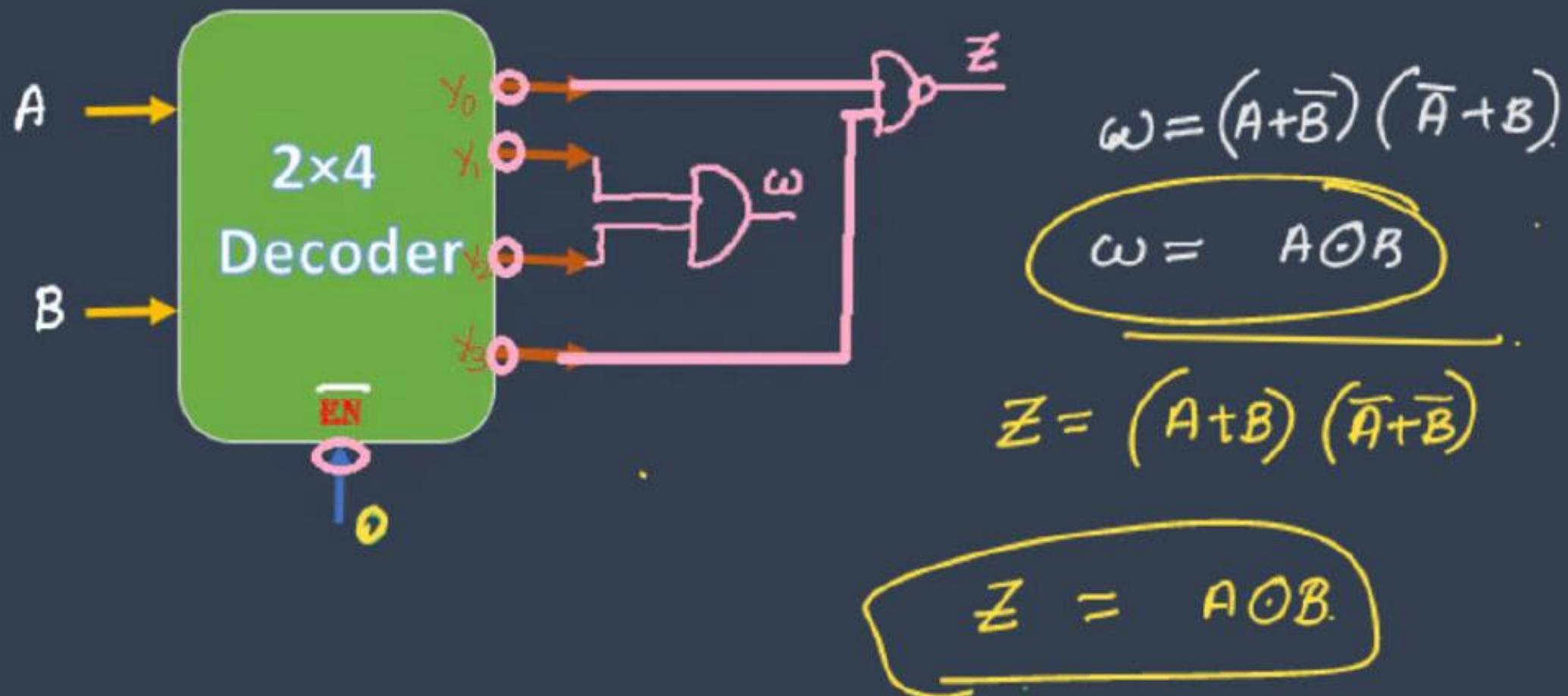


Q) implement  $F(A, B, C) = A + BC$ , using decoder

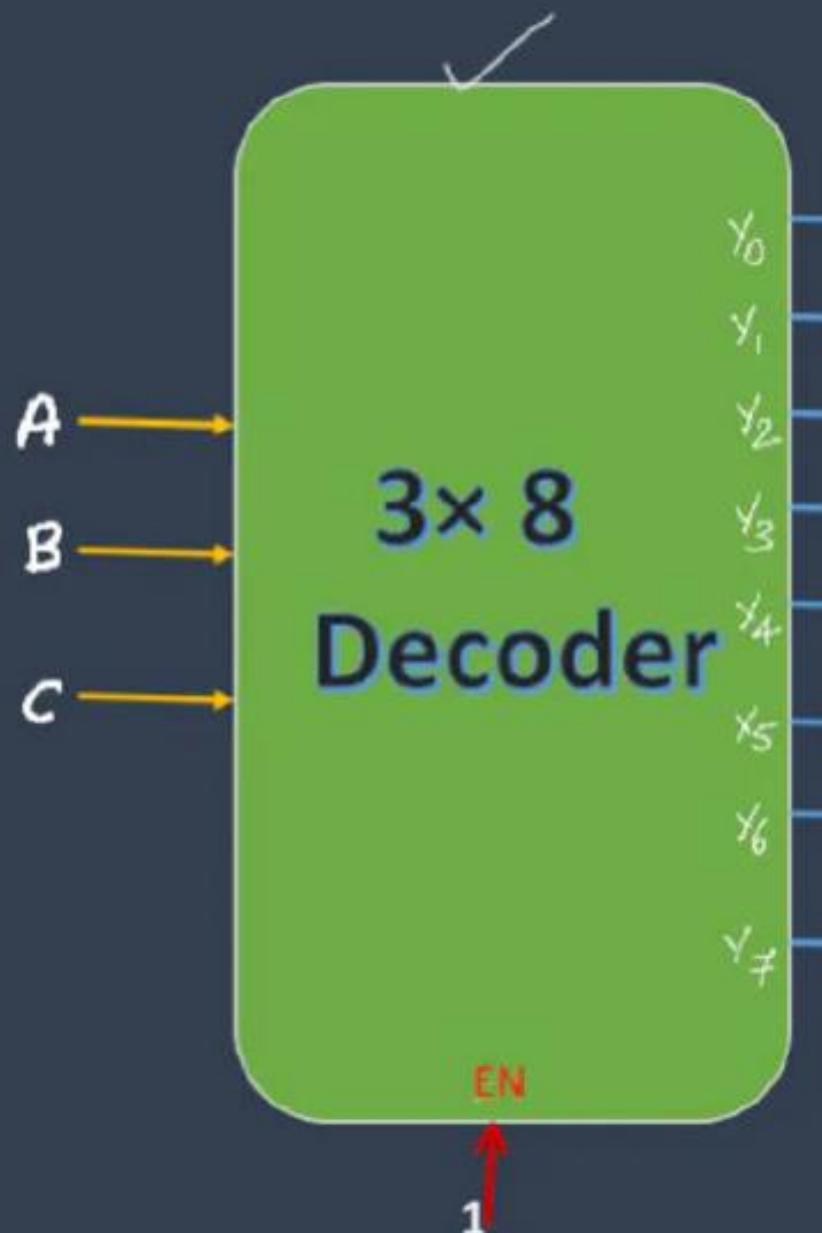
$$F(A, B, C) = A + BC = \sum m(3, 4, 5, 6, 7)$$



Q) Find the logic expression of W and Z



Q) The logic expression of F1 and F2



$$(0, 1, 2) \rightarrow (1, 2, 3, 4)$$
$$(0, 3, 4)$$

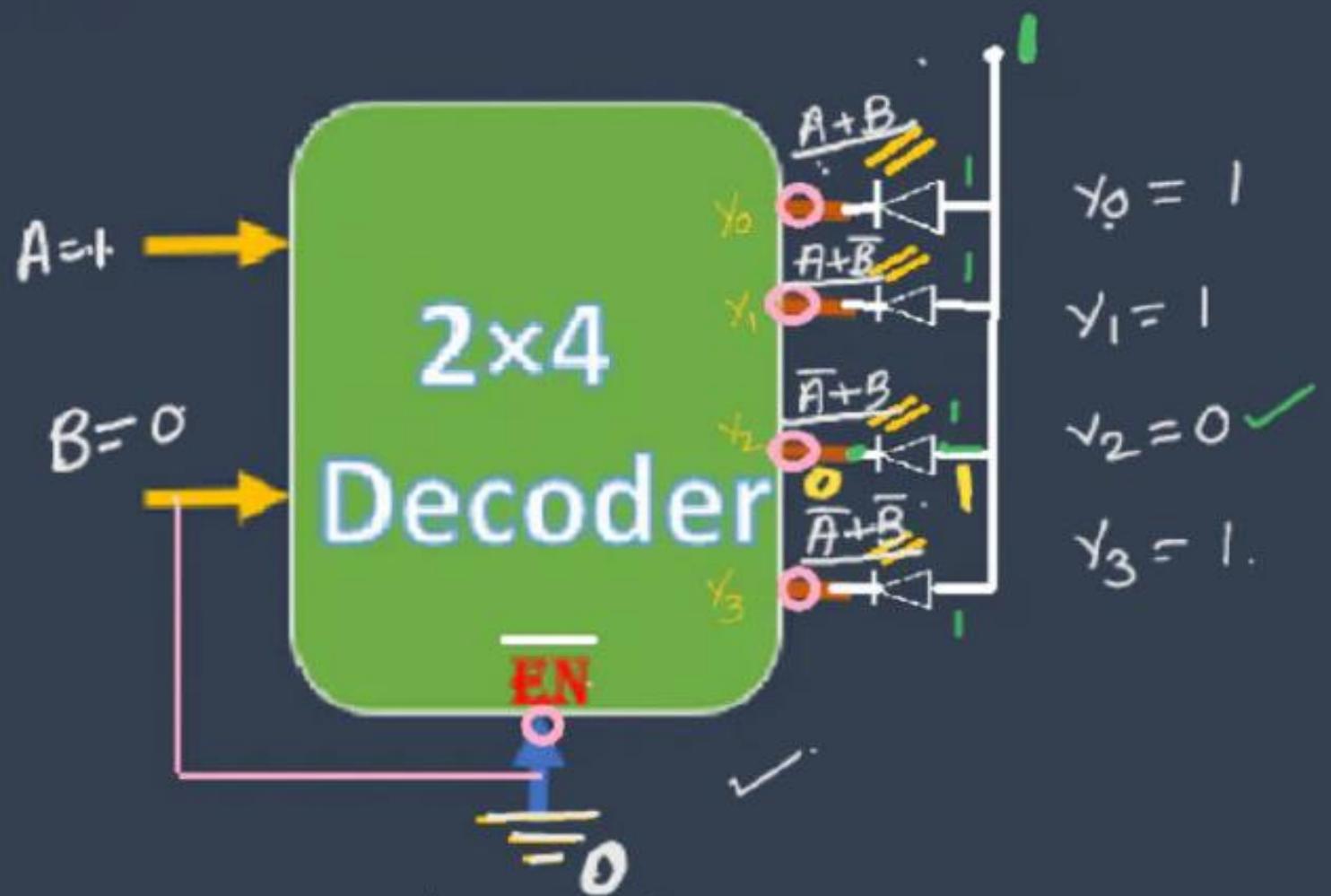
$$\overline{(0, 1, 2)} = (3, 4, 5, 6, 7)$$
$$f_1 = \overline{(3, 4, 5, 6, 7)}$$

$$f_1 = \sum m(0, 1, 2).$$

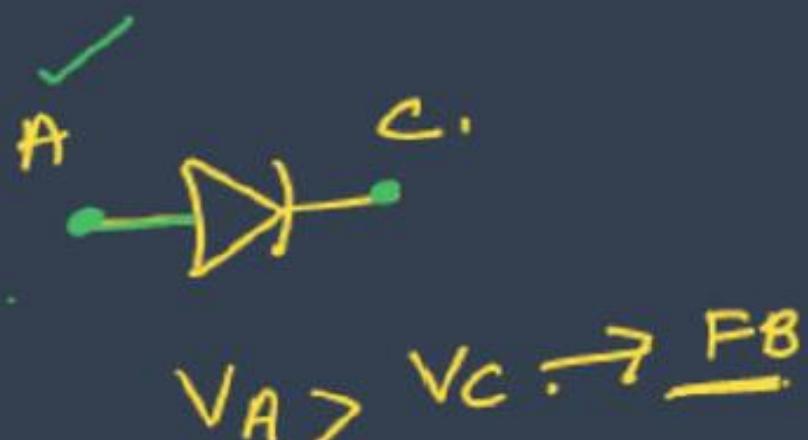
$$f_2 = \overline{(0, 1, 2, 3)}$$

$$f_2 = (4, 5, 6, 7)$$

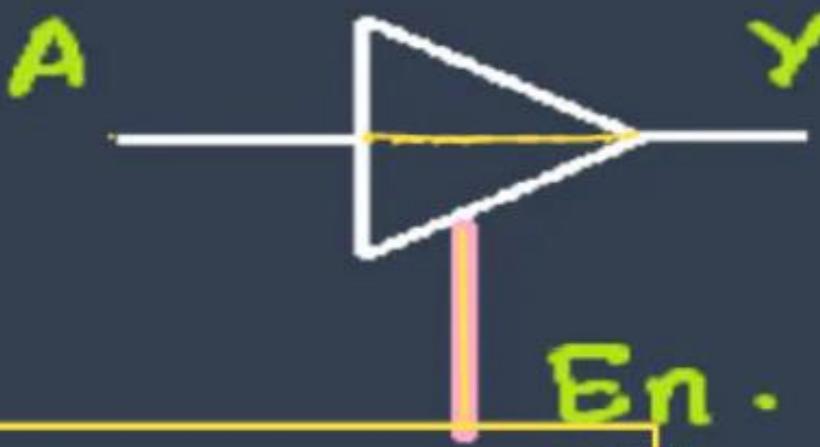
Q) Which of the following LED will glow



$$y_0 = 1$$
$$y_1 = 1$$
$$y_2 = 0 \checkmark$$
$$y_3 = 1.$$

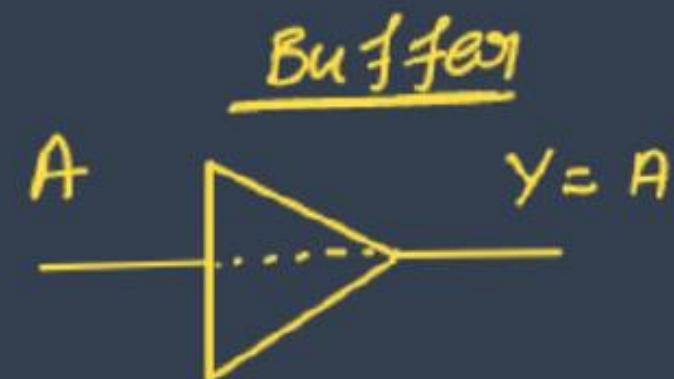


# Tri-state Buffer



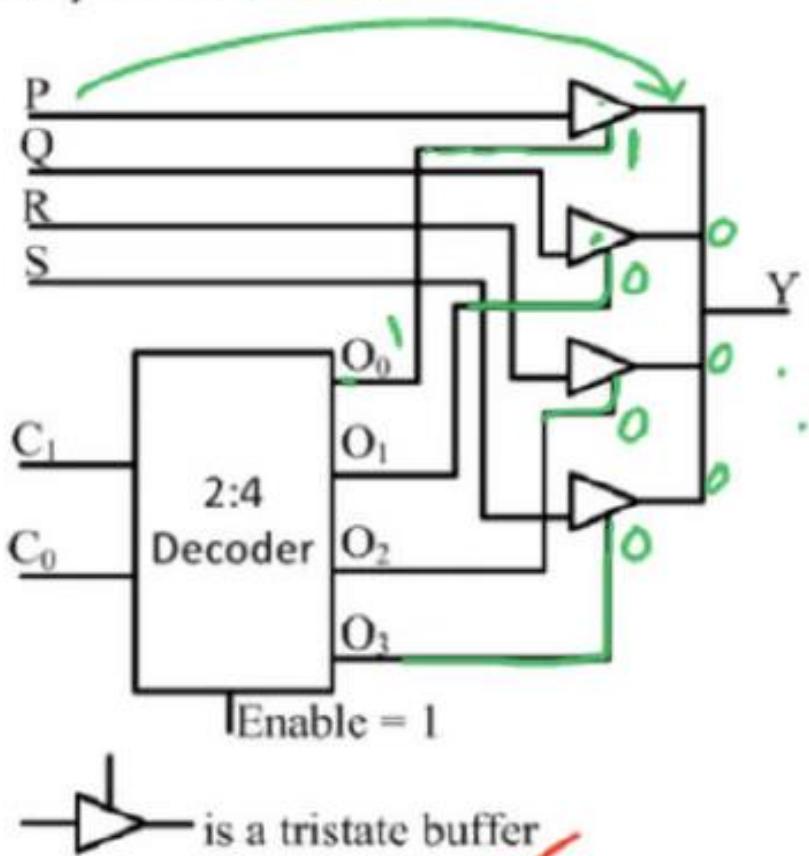
if  $E_{n\cdot} = 0$ ,  $Y = 0$

$E_{n\cdot} = 1$ ,  $Y = A$



The functionality implemented by the circuit below is

$$\begin{aligned}O_0 &= \overline{C_1} \overline{C_0} \\O_1 &= \overline{C_1} C_0 \\O_2 &= C_1 \overline{C_0} \\O_3 &= C_1 C_0\end{aligned}$$

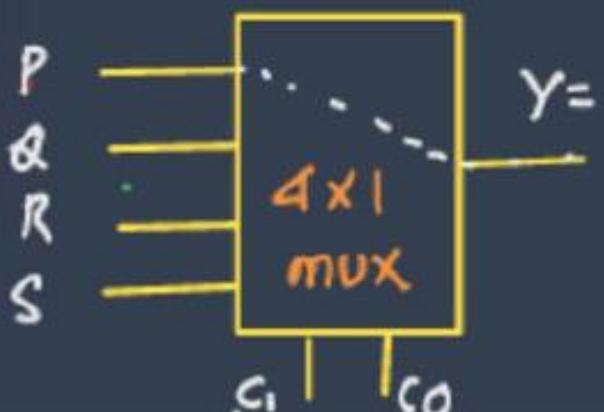


is a tristate buffer

(B) 4-to-1 multiplexer

(D) 6-to-1 multiplexer  $\times$

$C_1$	$C_0$	$O_0$	$O_1$	$O_2$	$O_3$	$Y$
0	0	1	0	0	0	P
0	1	0	1	0	0	Q
1	0	0	0	1	0	R
1	1	0	0	0	1	S

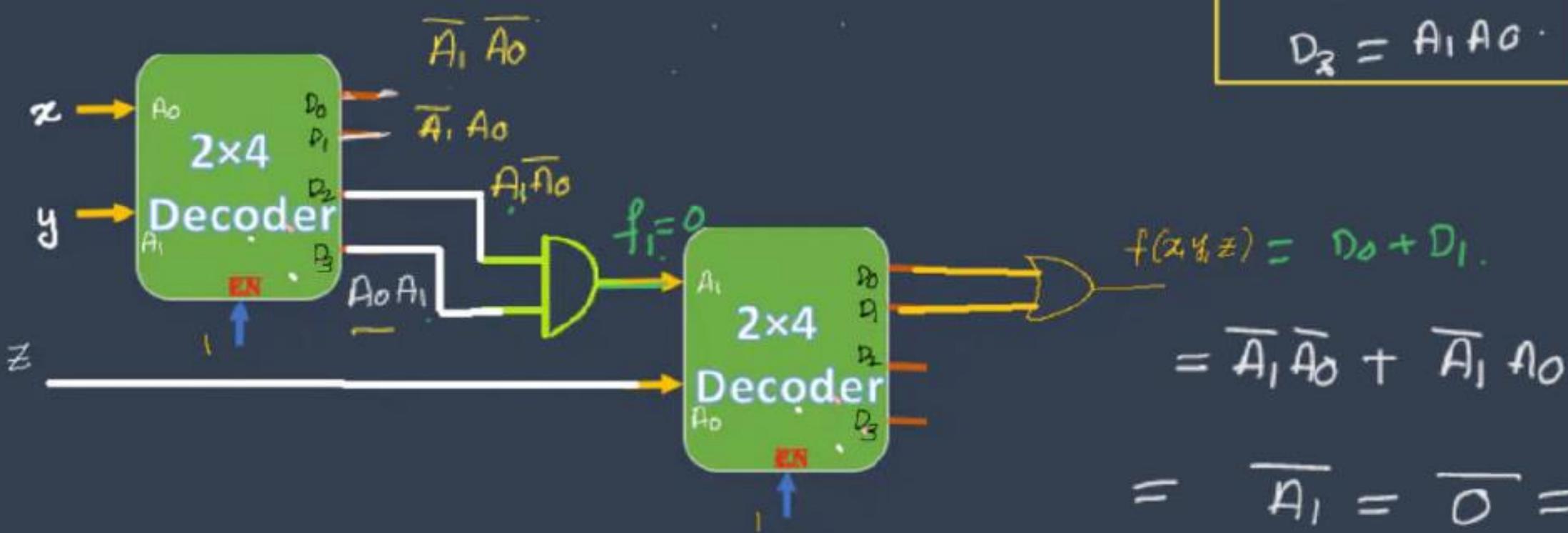


Q) A logic circuit consists of two  $2 \times 4$  decoders as shown in the fig , the output of the decoder are as follows

- $D_0 = 1$  when  $A_0 = 0$  and  $A_1 = 0$
- $D_1 = 1$  when  $A_0 = 1$  and  $A_1 = 0$
- $D_2 = 1$  when  $A_0 = 0$  and  $A_1 = 1$
- $D_3 = 1$  when  $A_0 = 1$  and  $A_1 = 1$

then the  $f( x, y, z ) =$

$$\begin{aligned} D_0 &= \overline{A}_1 \overline{A}_0 \\ D_1 &= \overline{A}_1 A_0 \\ \dots \\ D_2 &= A_1 \overline{A}_0 \\ D_3 &= A_1 A_0 \end{aligned}$$



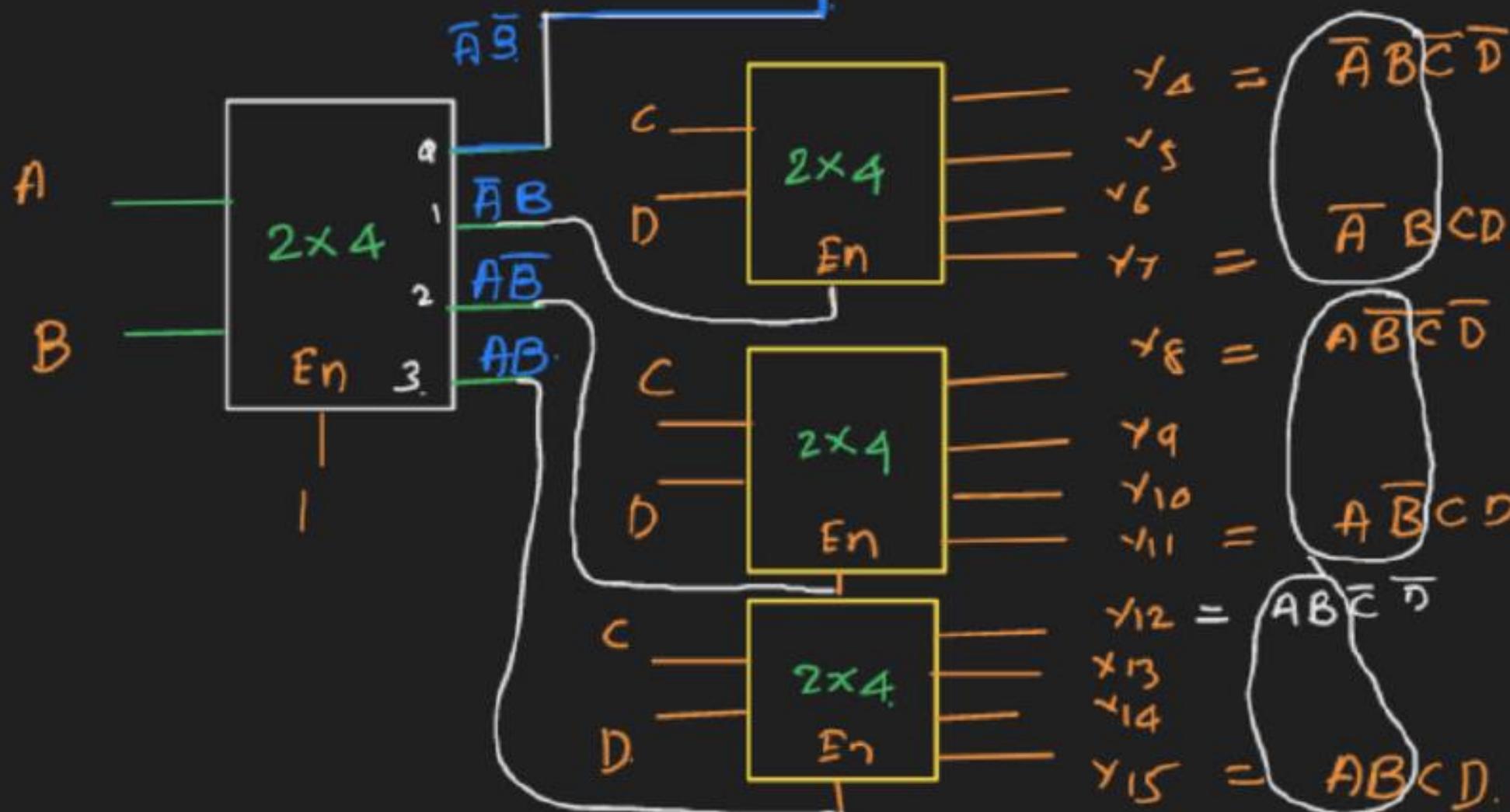
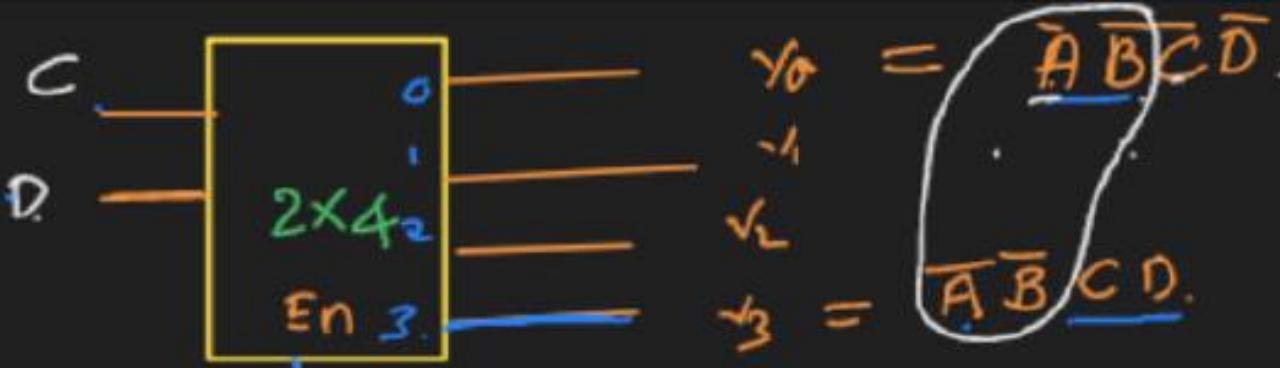
# Implementation of higher order Decoders using lower order Decoders

Q) Implement  $4 \times 16$  decoder using  $2 \times 4$  decoder

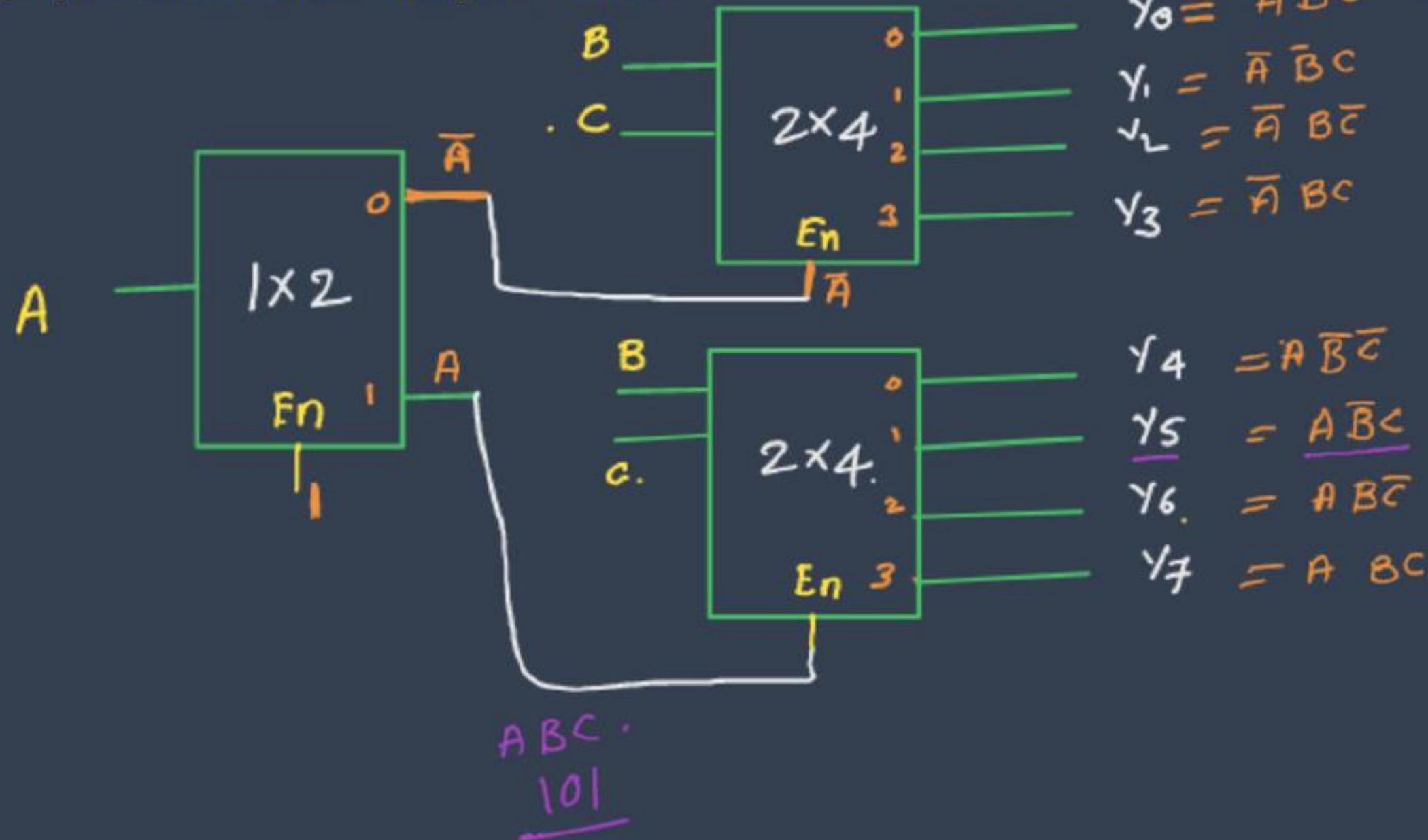
$$\frac{16}{4} = 4 \quad \textcircled{L_2} \quad \text{LSB}$$

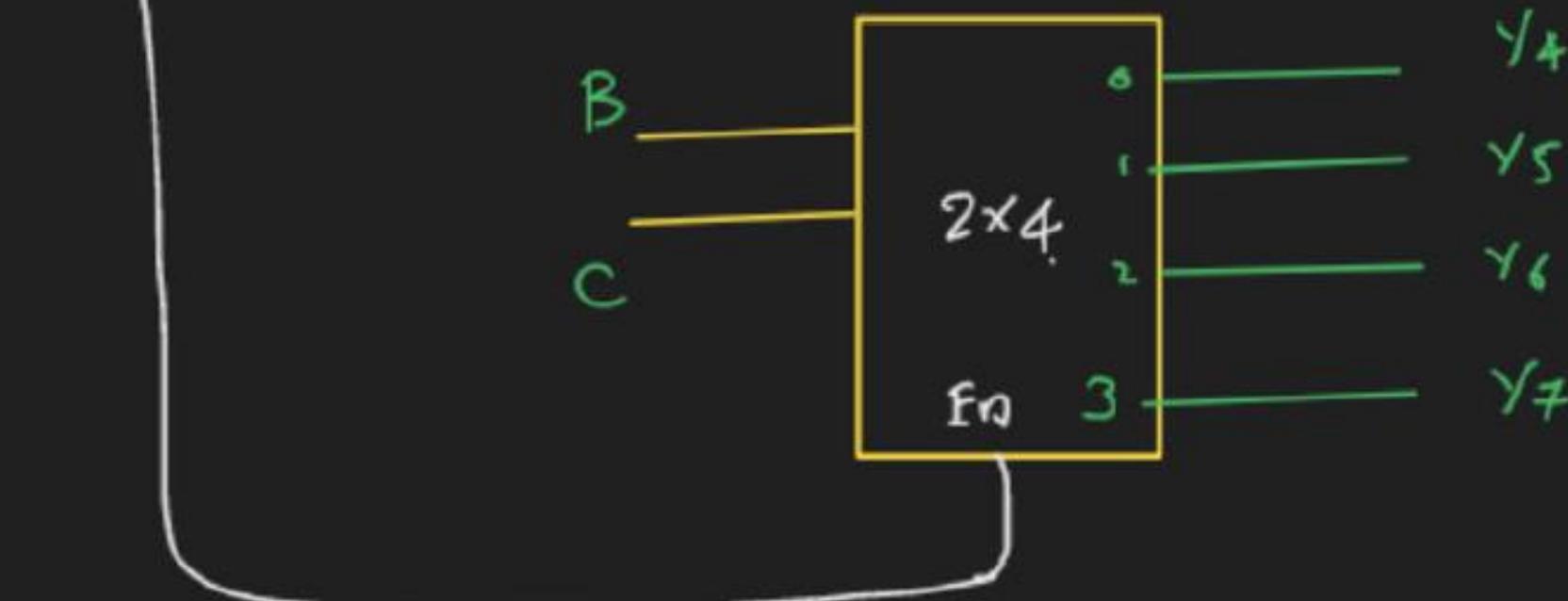
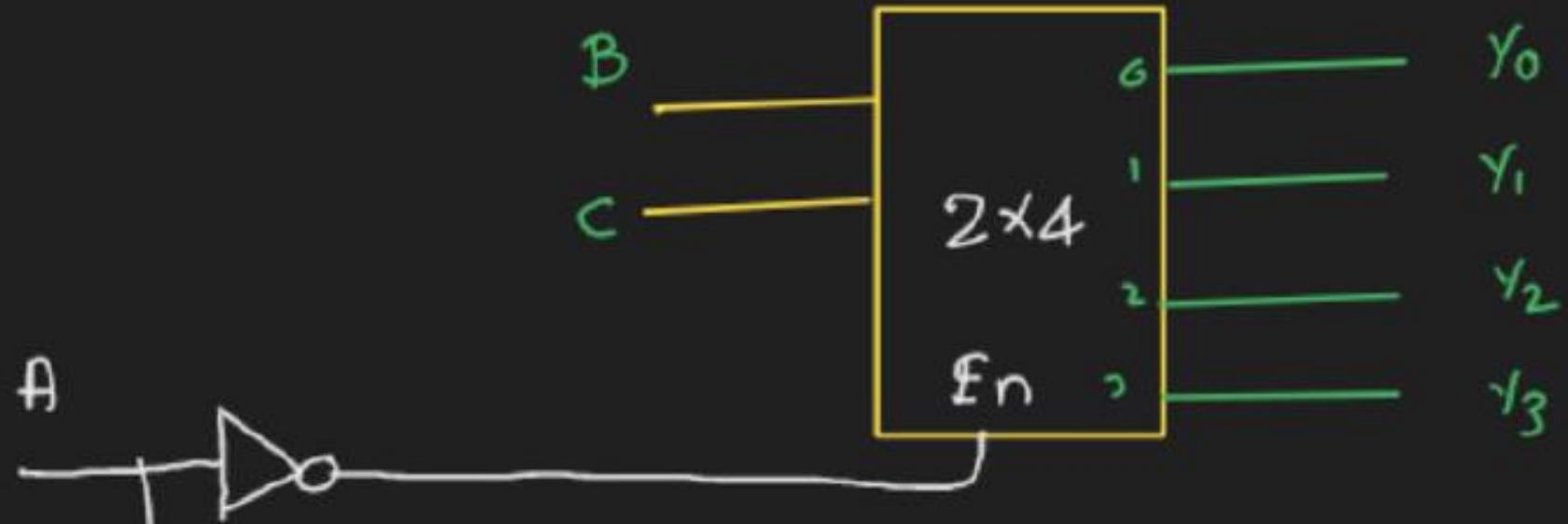
$$\frac{4}{4} = 1 \quad \textcircled{L_1} \quad \text{msb}$$

        
 $\textcircled{5}$

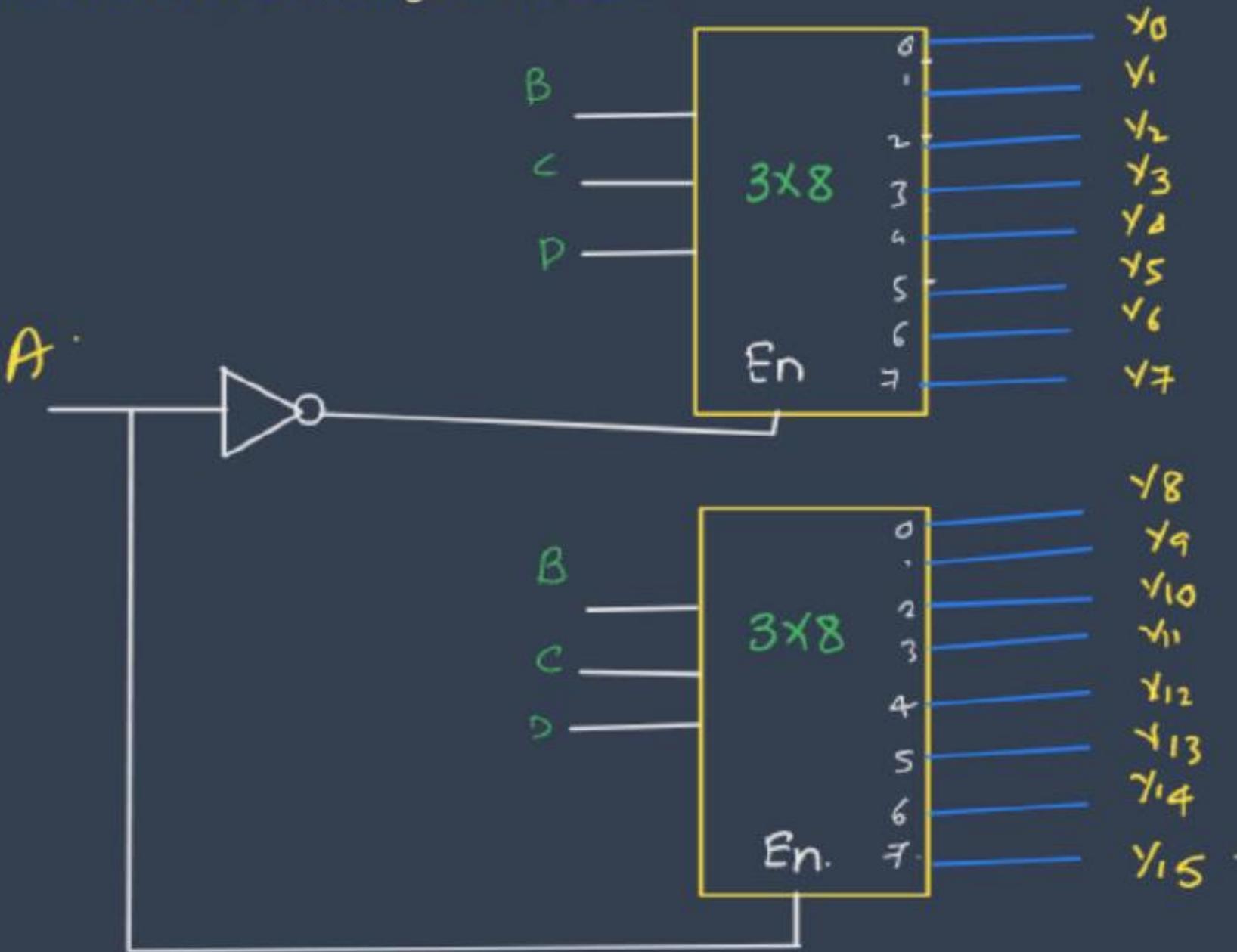


Q) Implement  $3 \times 8$  decoder using  $2 \times 4$  decoder





Q) Implement  $4 \times 16$  decoder using  $3 \times 8$  decoder



# Encoder

Encoder is a combinational circuit , which is used to convert

1. Octal to binary (  $8 \times 3$  encoder )
2. Decimal to Binary (  $10 \times 4$  encoder )
3. Hexadecimal to Binary (  $16 \times 4$  encoder )

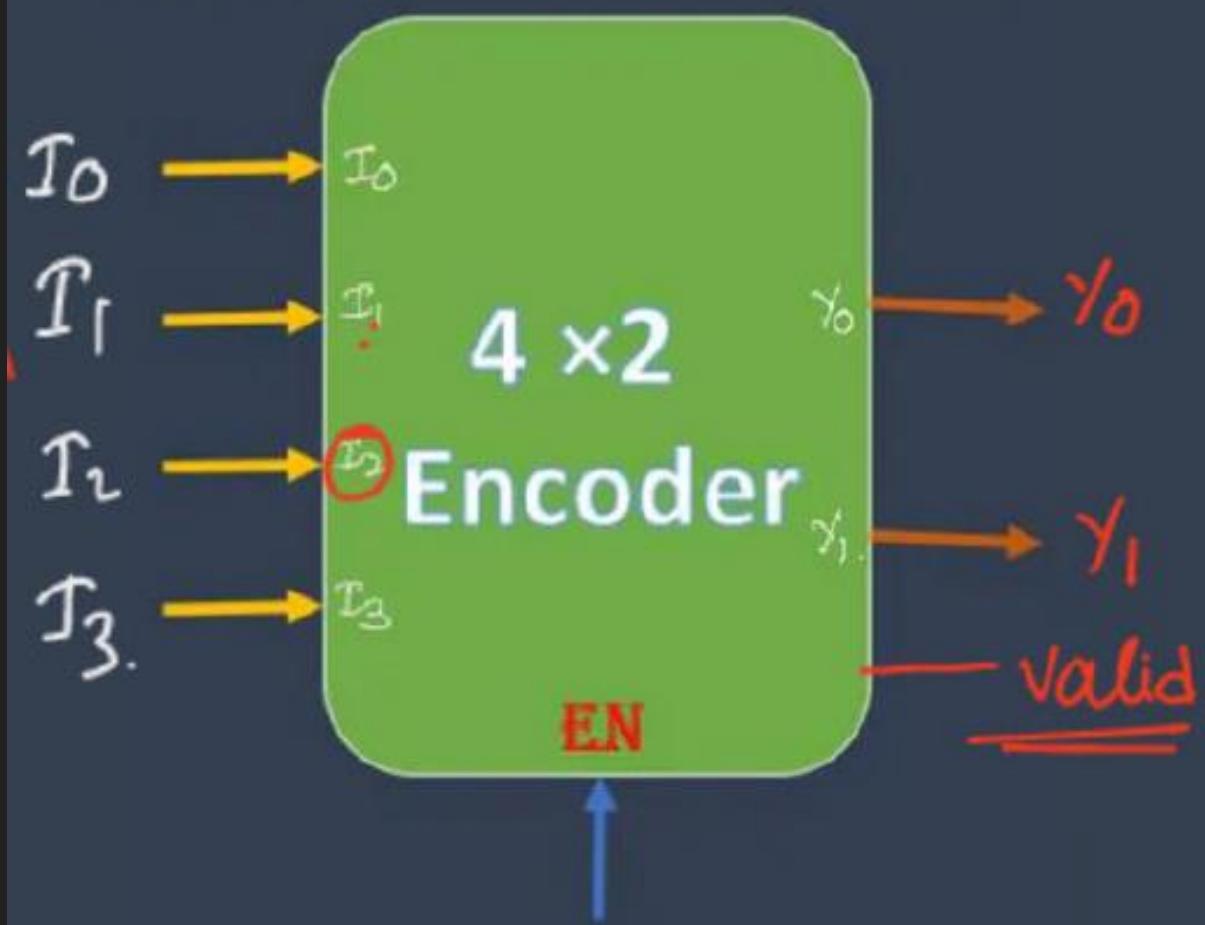
# General structure

$2^n \times n$

$n$  -----> number of outputs

$2^n$  -----> number of inputs

# 4 X 2 Encoder

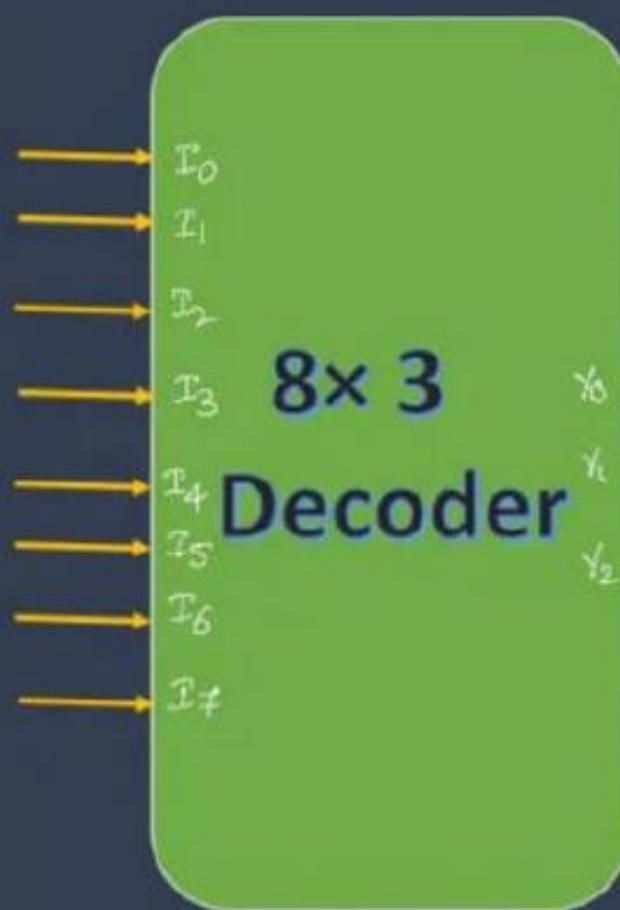


I3	I2	I1	I0	-	-	Y1	Y0	Valid
0	0	0	1	0	0	1	1	
0	0	1	0	0	1	1	1	
0	1	0	0	1	0	1	1	
1	0	0	0	1	1	1	1	

# Drawbacks of Encoder

- For an Encoder at a time only one among the all inputs is high , remaining all inputs should be zero
- If multiple inputs are simultaneously high, then the output is not valid, to avoid this restriction we will go for priority encoder.

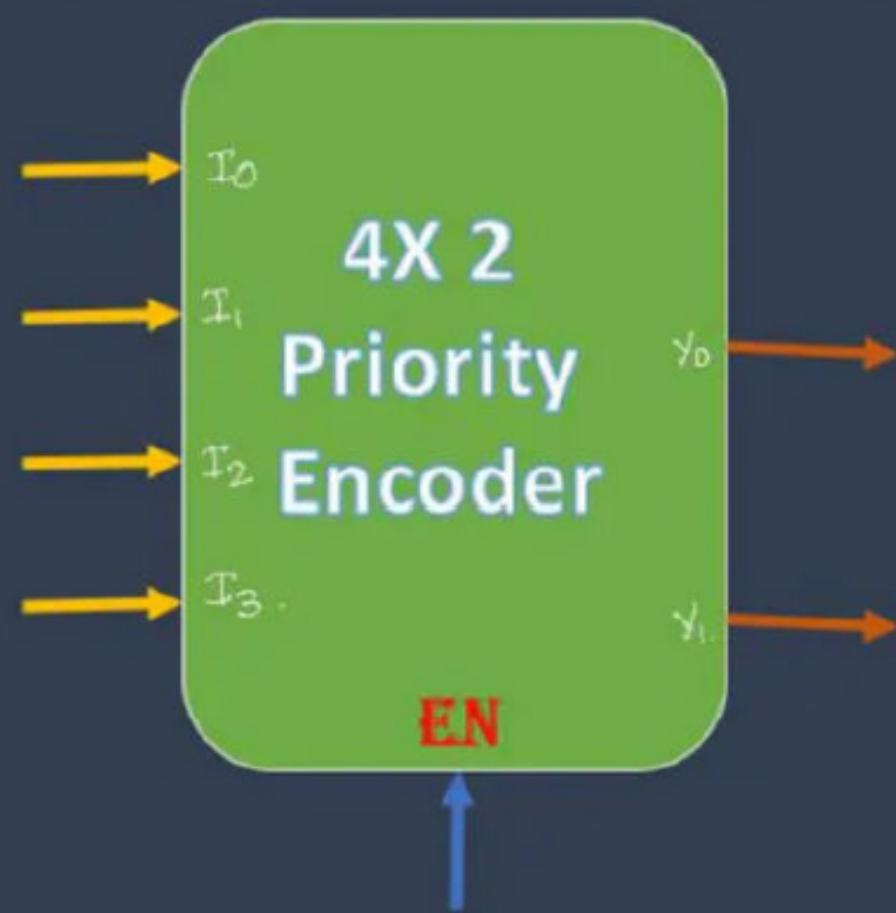
# 8 X 3 Encoder



I <sub>7</sub>	I <sub>6</sub>	I <sub>5</sub>	I <sub>4</sub>	I <sub>3</sub>	I <sub>2</sub>	I <sub>1</sub>	I <sub>0</sub>	Y <sub>2</sub>	Y <sub>1</sub>	Y <sub>0</sub>	Valid
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	0	0	0	1	1
0	0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	1	0	0	0	1	1	1
0	0	0	0	1	0	0	0	1	0	0	1
0	0	1	0	0	0	0	0	1	0	1	1
0	1	0	0	0	0	0	0	1	0	0	1
1	0	0	0	0	0	0	0	1	1	1	1

# Priority Encoder

Priority encoder assign priority to every input and whenever higher priority input is one , then other inputs are not consider

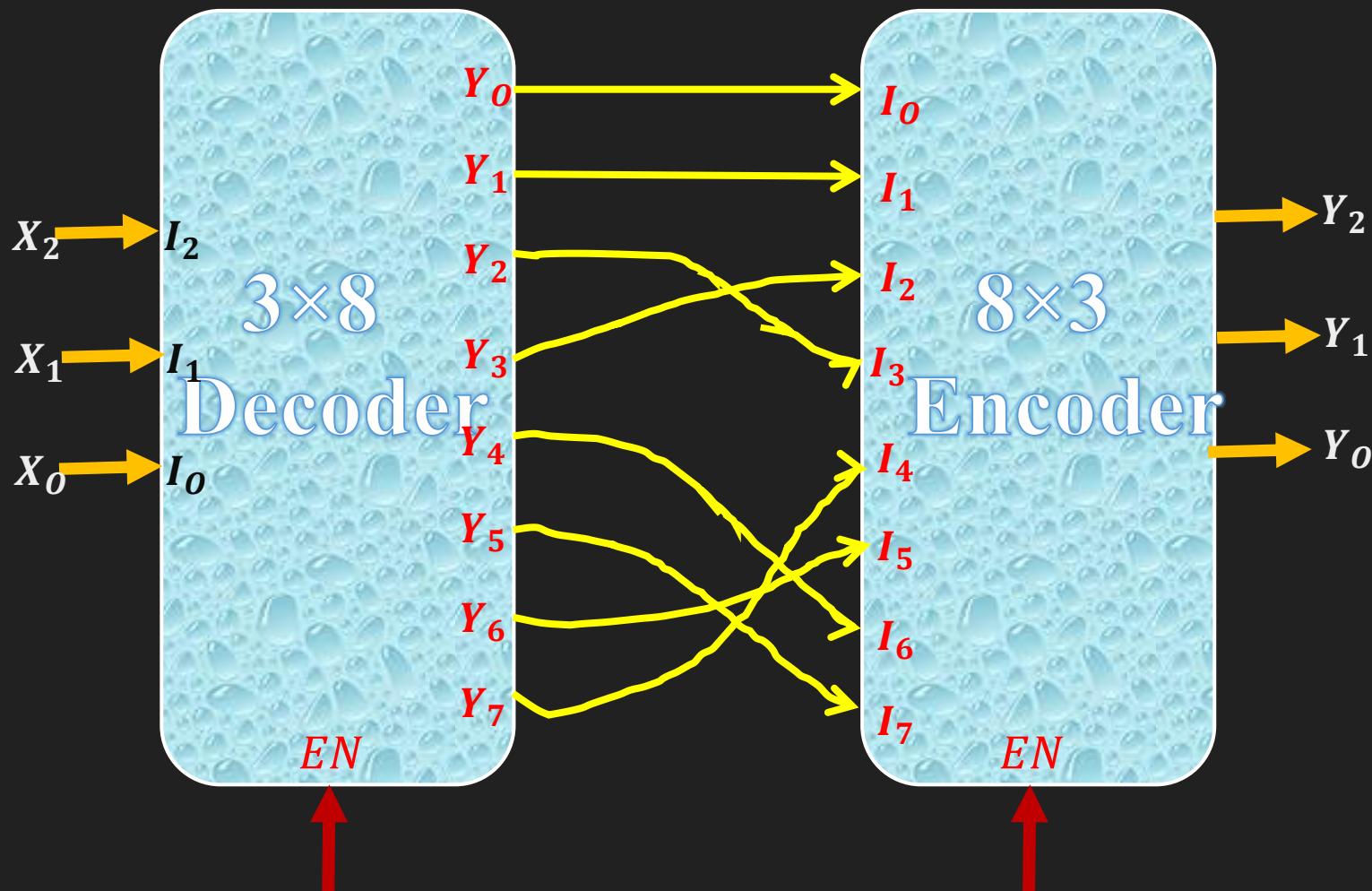


$$I_3 > I_2 > I_1 > I_0$$

$I_3$	$I_2$	$I_1$	$I_0$	$Y_1$	$Y_0$	Valid
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	X	X	X	1	1	1

# Code Converter

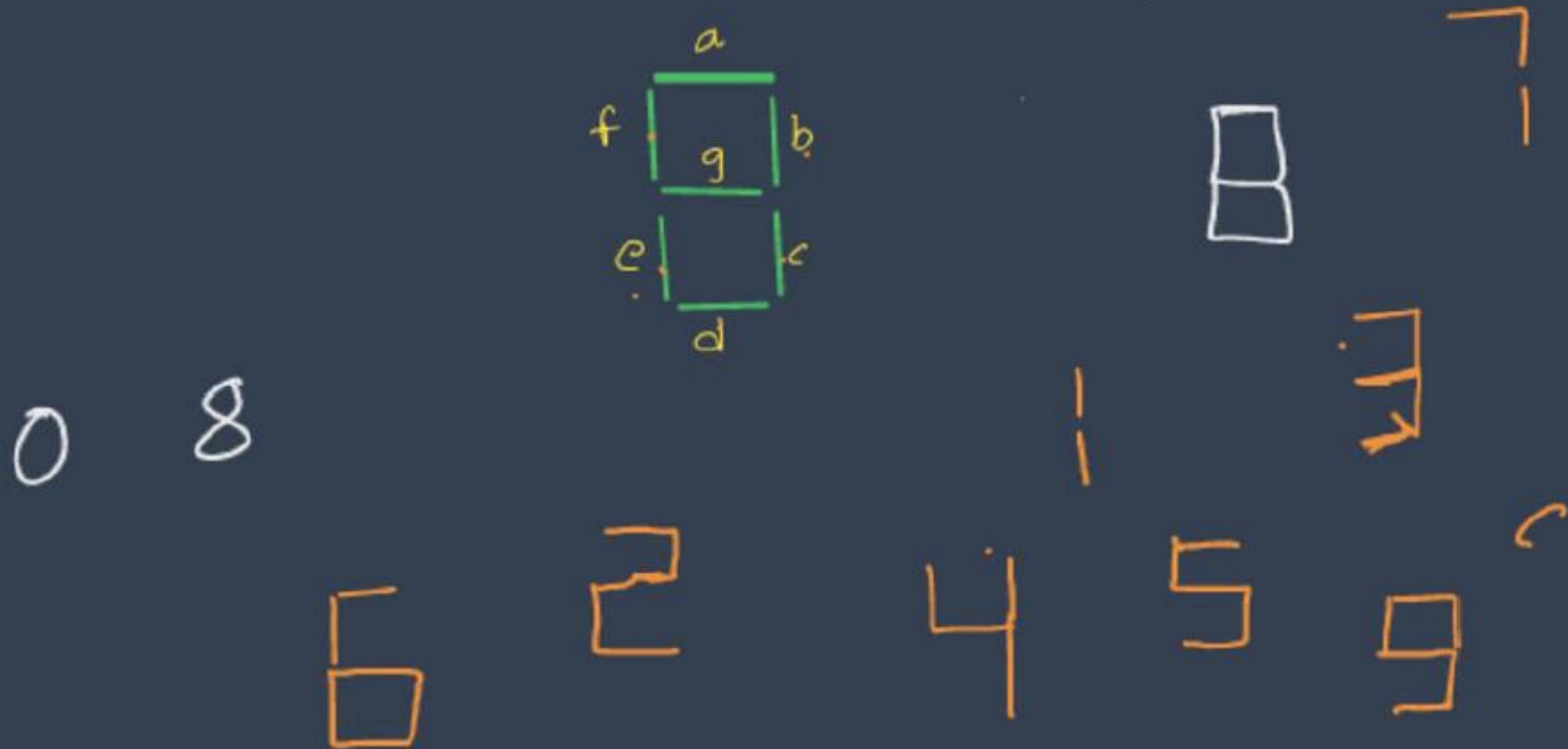
Q) Identify the circuit below



- a) ~~Binary to Gray code converter~~
- b) Binary to XS -3 converter
- c) Gray to Binary converter
- d) XS -3 to Binary converter

$X_2$	$X_1$	$X_0$	$Y_2$	$Y_1$	$Y_0$
0	0	0	0	0	0
0	1	0	1	0	0
1	1	0	1	1	0
1	0	1	1	1	1
1	1	1	1	0	1

Q) Design a circuit for BCD to 7- segment display decoder



BCD

7-segment

Display.

0 0 0 0

a b c d e f g

0 0 0 1

0 1 1 0 0 0 0

0 0 1 0

0 1 0 1 0 0 1

0 0 1 1

1 1 1 1 0 0 1

0 1 0 0

0 1 1 1 0 1 1

0 1 0 1

0 1 1 0 1 1 1

0 1 1 0

0 1 1 1 1 1 1

0 1 1 1

0 0 0 0 0 0 0

1 0 0 0

1 0 0 1 1 1 1

1 0 0 1

1 0 0 1 1 1 1

$$a = \sum m(0, 2, 3, 5, 6, 7, 8, 9)$$

$$b = \sum m(0, 1, 2, 3, 4, 7, 8, 9)$$

$$c = \sum m(0, 1, 3, 4, 5, 6, 7, 8, 9)$$

$$d = \sum m(0, 2, 3, 5, 6, 8, 9)$$

$$e = \sum m(0, 3, 6, 8) \quad g = \sum m(2, 3, 4, 5, 6, 8, 9)$$

$$f = \sum m(0, 4, 5, 6, 8, 9)$$

Q) Design a circuit for Binary to BCD

Binary	BCD.
$x_3 \ x_2 \ x_1 \ x_0$	$y_7 \ y_6 \ y_5 \ y_4 \ y_3 \ y_2 \ y_1 \ y_0$
0 0 0 0	0 0 0 0 0 0 0 0
0 0 0 1	0 0 0 0 1 0 0 1
0 0 1 0	0 0 0 1 0 0 0 0
0 0 1 1	0 0 0 1 0 0 0 1
0 1 0 0	0 0 0 1 0 0 1 0
0 1 0 1	0 0 0 1 0 0 1 1
0 1 1 0	0 0 0 1 0 1 0 0
1 1 1 1	0 0 0 1 0 1 0 1

Q) Design a circuit for BCD to ES-3 code

$BCD$	$ES-3$
$x_3 \ x_2 \ x_1 \ x_0$	$y_3 \ y_2 \ y_1 \ y_0$
0 0 0 0	0 0 1 1
: : : :	: : : :
0   1 1	0 1 0
<hr/>	
1 0 0 1	1 1 0 0

An  $n$ -bit carry look ahead adder is designed using only Ex-OR, AND, OR gates. The propagation delay of each Ex-OR gate is  $\underline{20 \text{ ns}}$  and that of each AND, OR gates is  $t_0$  ns. If the total propagation delay of the adder circuit is 60 ns, then the value of  $t_0$  will be

(given that  $t_0 \leq 20 \text{ ns}$ )

$$\text{Sum} = \max[\text{XOR}, \text{AND}] + \text{AND} + \text{OR} + \text{XOR}.$$

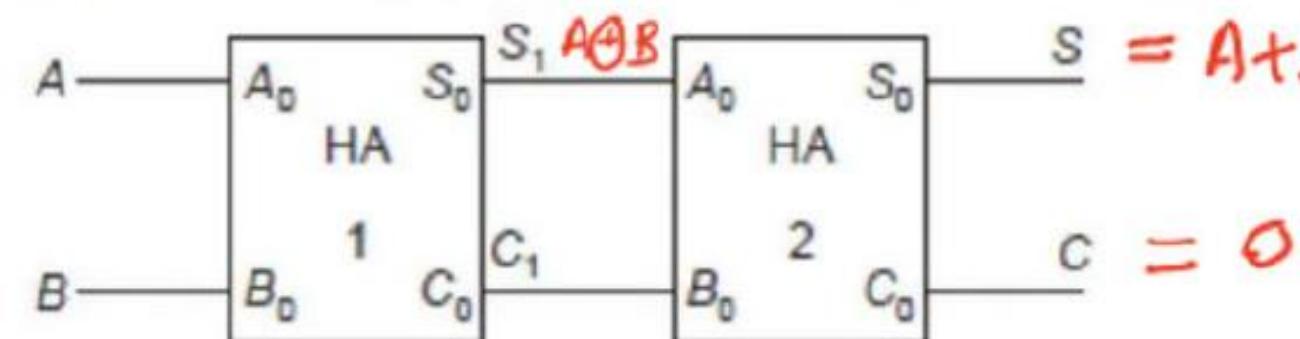
- a. 10
- b. 15
- c. 20
- d. depends on ' $n$ ' value

$$60 = 20 + 2x + 20$$

$$2x = 20$$

$$x = 10$$

Two half adders are connected in cascade as shown below.



The output 'S' and 'C' is

- a.  $S = A \oplus B, C = AB$
- b.  $S = A \odot B, C = 0$
- c.  $S = A + B, C = 0$  ✓

$$S = (A \oplus B) \oplus AB$$

$$A \oplus B \oplus AB$$

$$A \oplus B [I \oplus A]$$

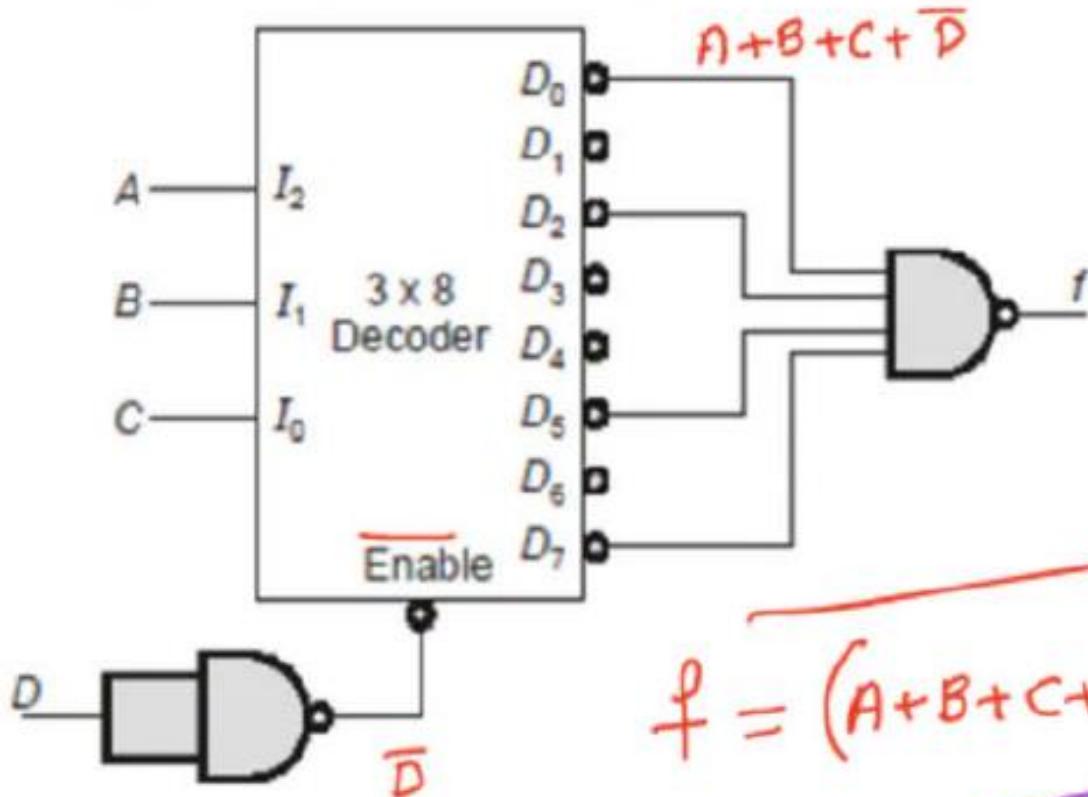
$$A \oplus B [\overline{A}] = A + \overline{A}B = \underline{A + B}$$

$$C = (A \oplus B) AB$$

$$C = (\overline{A}B + A\overline{B}) AB$$

$$C = 0$$

The logic function  $f(A, B, C, D)$  implemented by the circuit shown below is



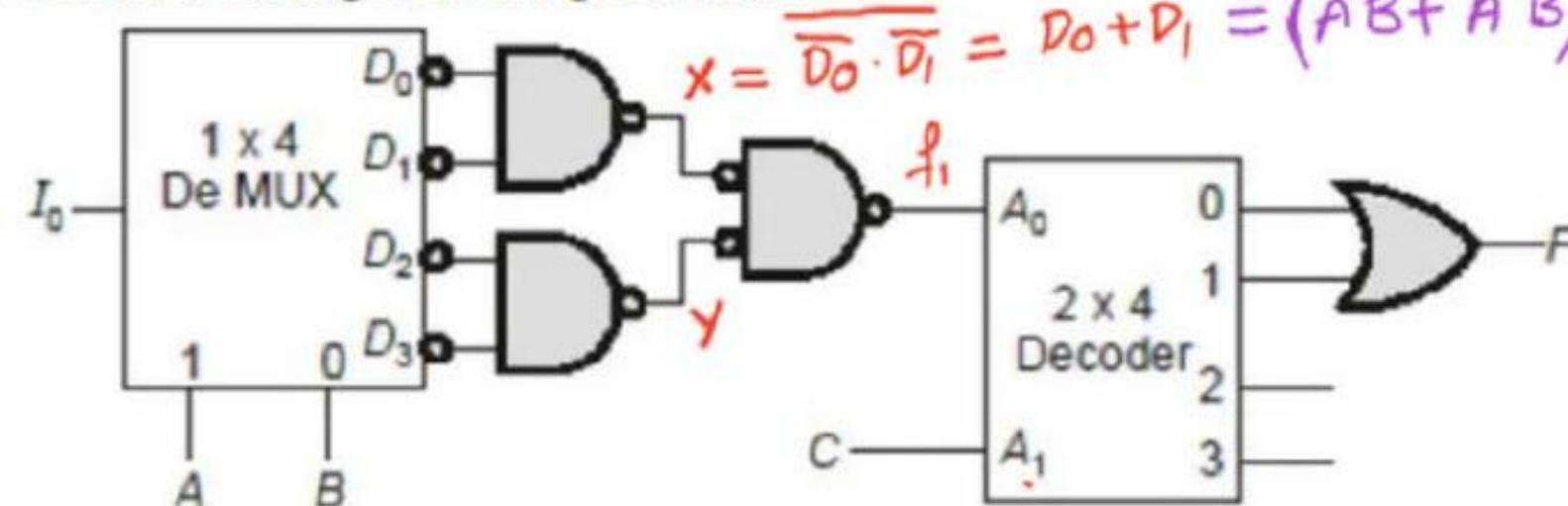
- a.  $\bar{D}(A \oplus C)$
- b.  $\bar{D}(A \odot C)$
- c.  $\bar{D}(A \oplus B)$
- d.  $D(A \odot C)$

$$f = (A + B + C + \bar{D})(A + \bar{B} + C + \bar{D})(\bar{A} + B + \bar{C} + \bar{D})(\bar{A} + \bar{B} + \bar{C} + \bar{D})$$

$$f = \overbrace{\bar{A}\bar{B}\bar{C}D} + \overbrace{\bar{A}B\bar{C}D} + ABC\bar{D} + ABCD$$

$$f = D[\bar{A}\bar{C} + AC] = D[\underline{\underline{A}\odot C}]$$

Consider the logic circuit given below



The minimized expression for  $F$  is

- a.  $\overline{C}$
- b.  $I_0$
- c.  $C$
- d.  $\overline{I_0}$

$$\left| \begin{array}{l} D_0 = \overline{A}\overline{B} \\ D_1 = \overline{A}B \\ D_2 = A\overline{B} \\ D_3 = AB \end{array} \right. \quad \left| \begin{array}{l} Y = (D_2 + D_3) I_0 \\ Y = (A) I_0 \end{array} \right.$$
$$X = \overline{D_0} \cdot \overline{D_1} = D_0 + D_1 = (\overline{A}B + A\overline{B}) = \overline{A} I_0$$

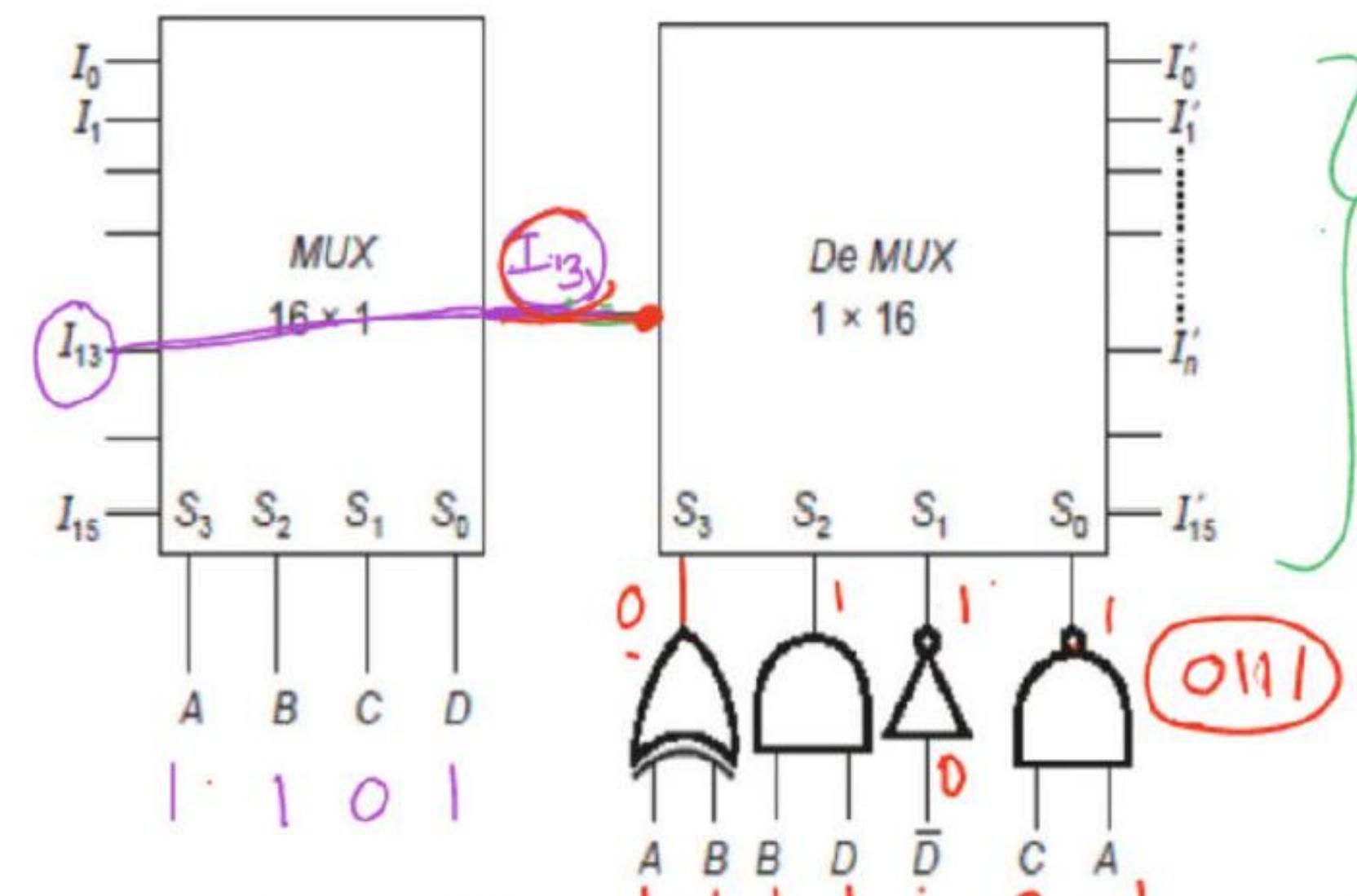
$$f_1 = \overline{X \cdot Y} = X + Y$$

$$f_1 = I_0$$

$$f = \overline{A_1} \overline{A_0} + \overline{f_1} A_0$$

$$f = \overline{A_1} = \overline{C}$$

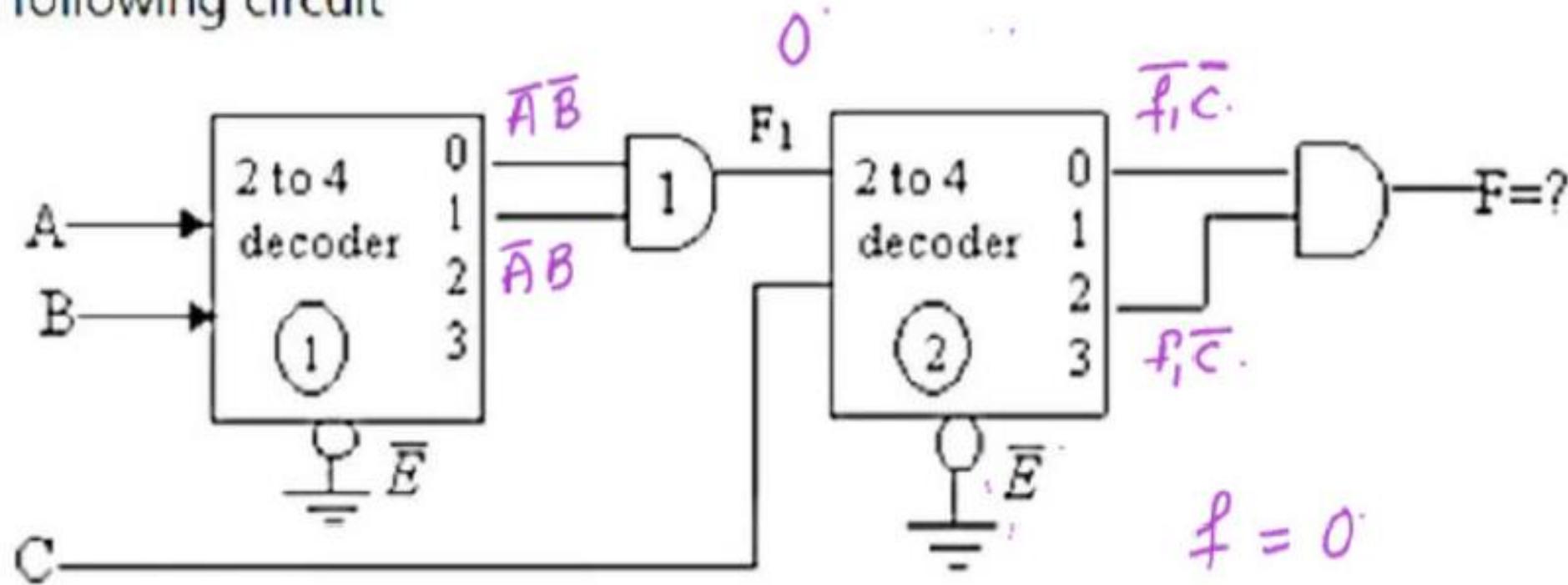
Consider the logic circuit given below:

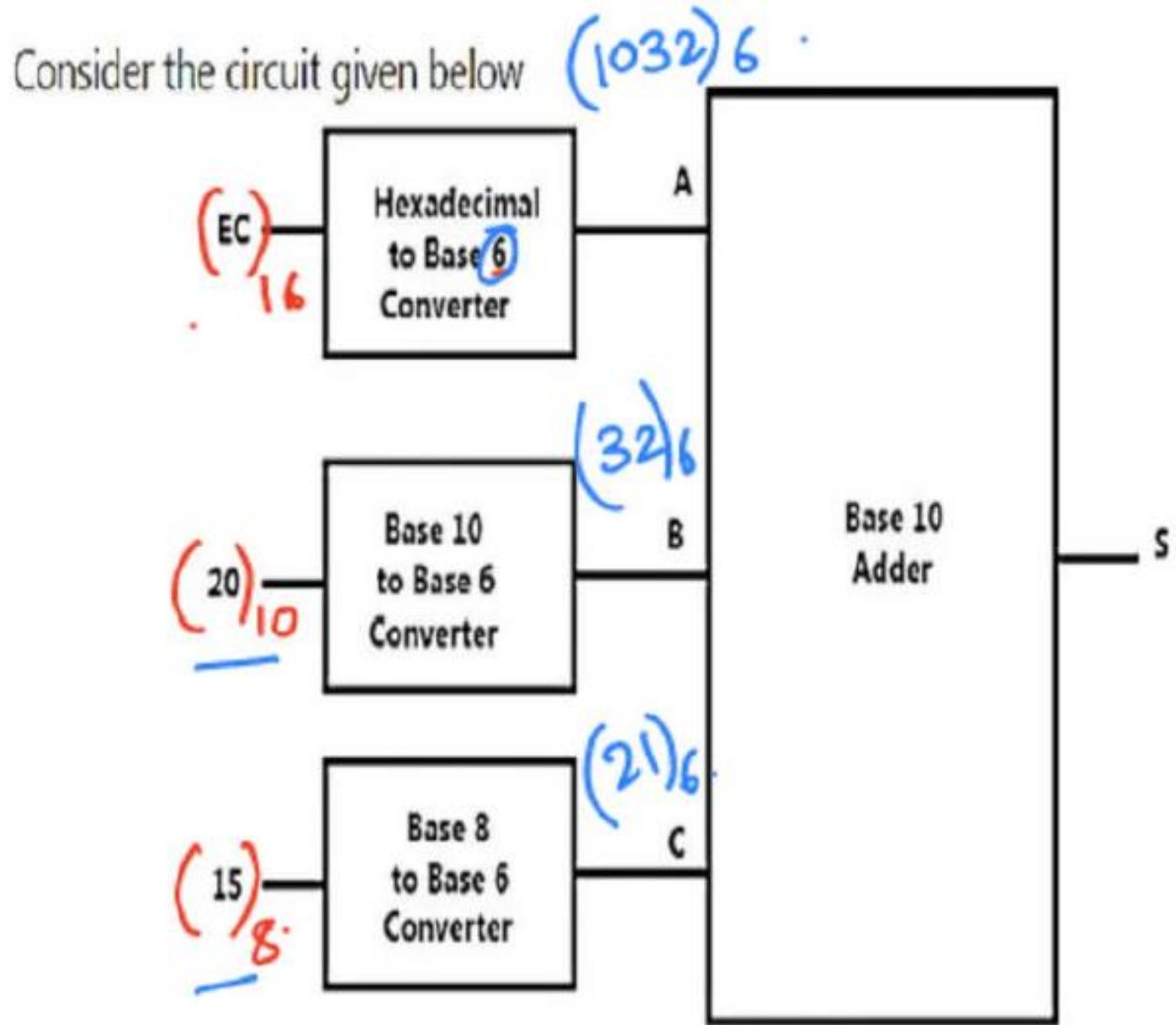


Input at line  $I_{13}$  in  $16 \times 1$  Mux corresponds to output at line  $I_{15}'$  of  $1 \times 16$  De Mux. The value of  $n$  is \_\_\_\_\_.

Find the output of the following circuit

- (a) 1
  - (b) C
  - (c)  $\overline{C}$
  - (d) 0



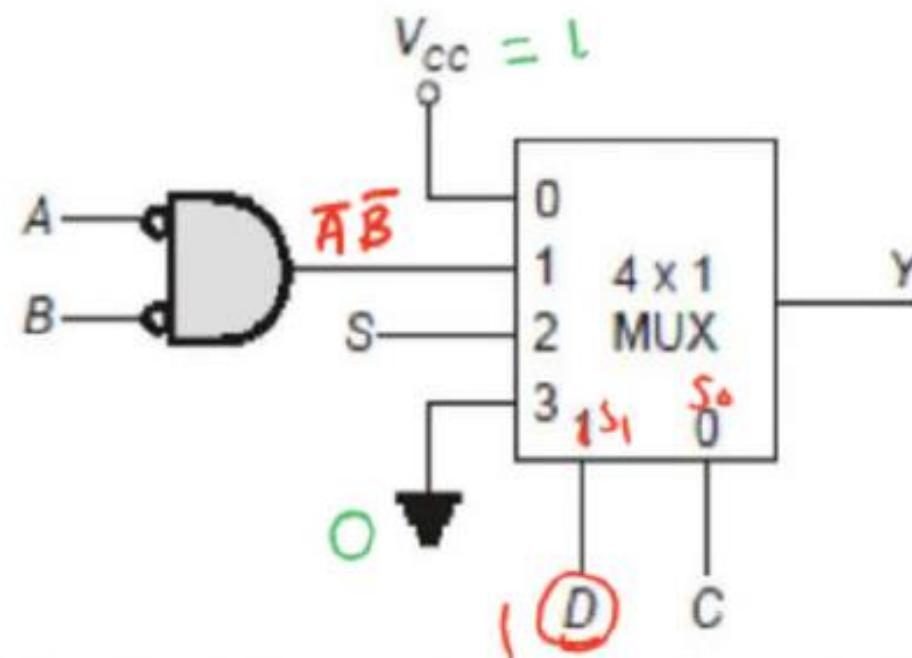


$$\begin{aligned}
 (EC)_{16} &= 14(16) + 12 \\
 &= (236)_{10}
 \end{aligned}$$

$$\begin{array}{r}
 1032 \\
 32 \\
 21 \\
 \hline
 085
 \end{array}$$

The output of each converter is given to adder which adds them considering decimal number. The output of adder is S. The value of S is \_\_\_\_.

Consider the circuit given below

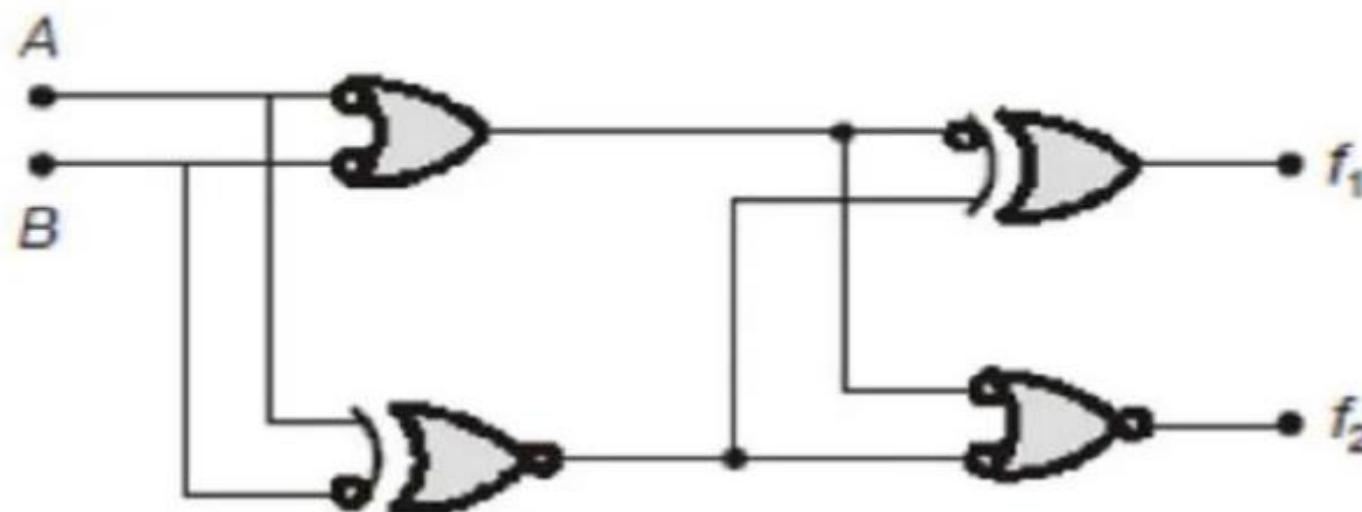


Which of the following statements is true for  $Y$ .

- a.  $Y = \bar{C}\bar{D} + \bar{D}C(\bar{A} + \bar{B}) + \bar{C}DS$
- b.  $Y = CD + D\bar{C}(\bar{A} + \bar{B}) + CDS$
- c.  $Y = \bar{C}\bar{D} + (\bar{D} + \bar{C})(\bar{A} + \bar{B}) + \overline{C + \bar{D} + \bar{S}}$
- d.  $Y = \bar{C}\bar{D} + (\bar{D} + \bar{C})(\bar{A} + \bar{B}) + \overline{C + \bar{D} + \bar{S}}$

$$= \bar{D}\bar{C} + \bar{A}\bar{B}(\bar{D}C) + D\bar{C}(S) +$$
$$Y = \bar{C}\bar{D} + \overline{(A+B)} \overline{(\bar{C}+D)} + \overline{C+\bar{D}+\bar{S}}$$

Consider the digital circuit shown below

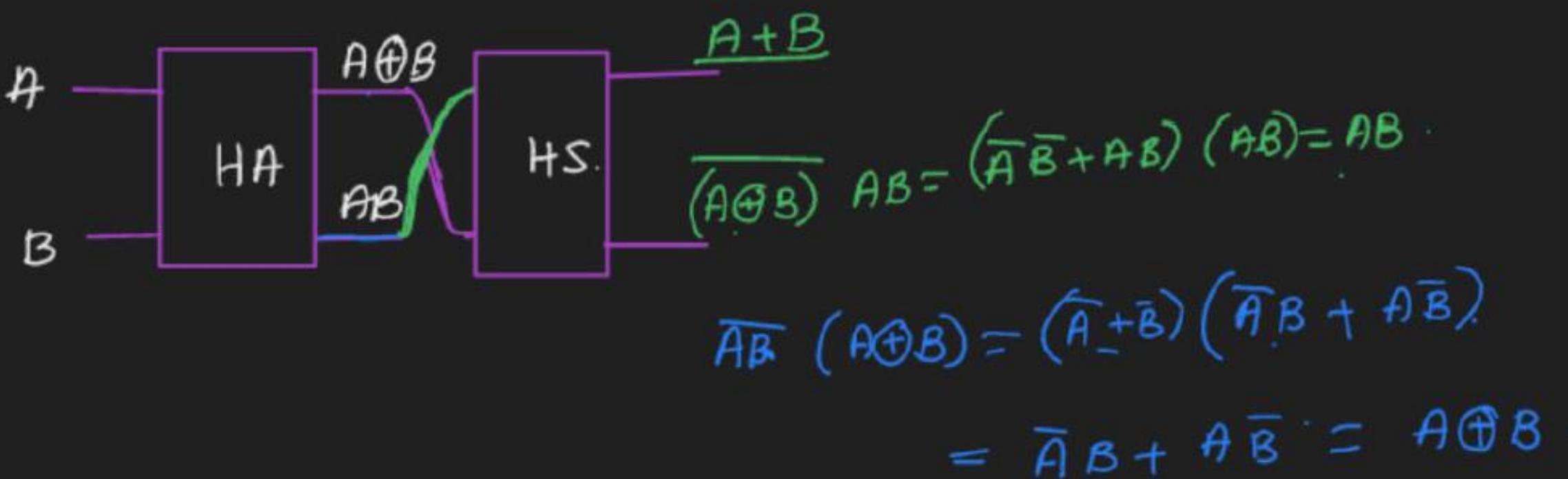
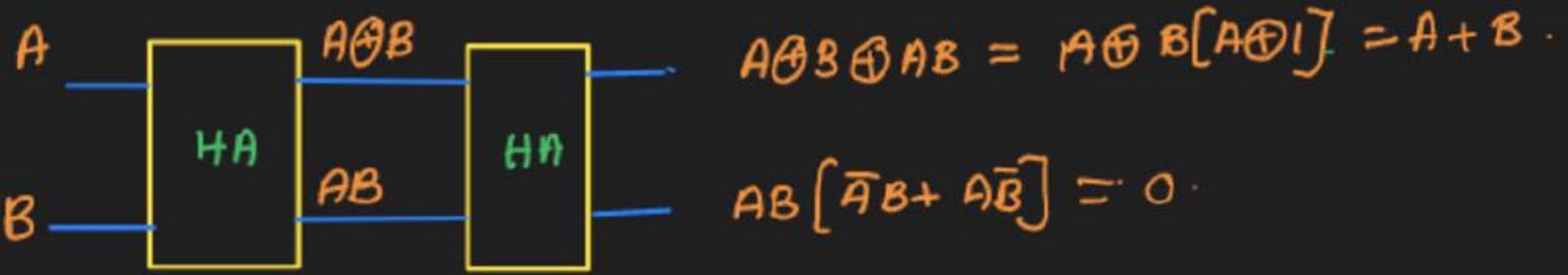


$$= A + B$$

$$= A \oplus B$$

It represents

- a. Half adder followed by half subtractor
- b. Half subtractor followed by half adder
- c. Half adder followed by a half adder
- d. A full adder



The minimum number of NOR gates required to realize the half adder circuit is \_\_\_\_\_.

⑤

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The output  $Y$  of a  $\textcircled{2}$  bit comparator is logic 1 whenever the 2 bit input  $A$  is greater than the 2-bit input  $B$ . The number of combinations for which the output is logic 1 is \_\_\_\_\_.

$$\frac{2^{2n} - 2^n}{2} = \textcircled{6}$$

$$\begin{array}{c} A \\ \hline 00 \\ 01 \\ 10 \\ 10 \end{array}$$

01

10

11

$$\begin{array}{c} B \\ \hline 00 \\ 01 \\ 10 \\ 10 \end{array}$$

1

2

3

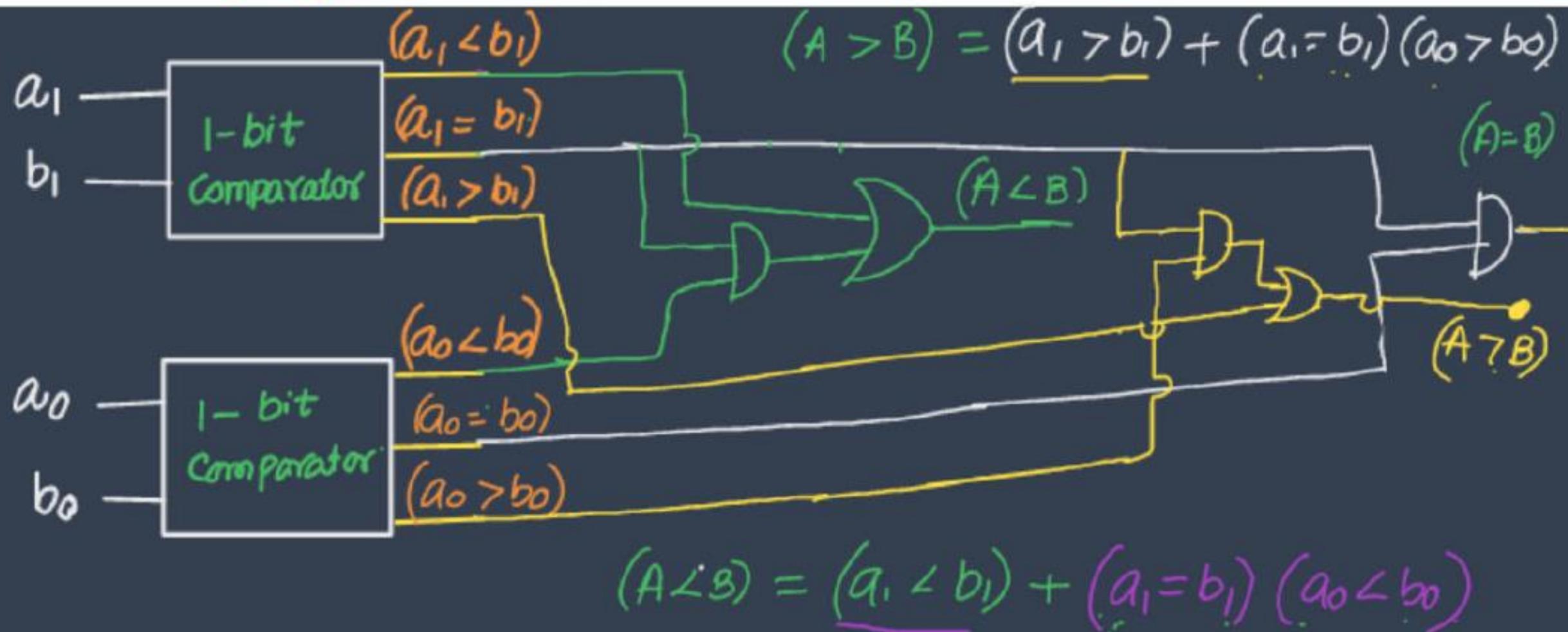
How many 1-bit comparators, 2-input AND gates, 2-input OR gates required to design a 2-bit comparator.

- (a) 2, 3, 2 ✓  
(c) 2, 3, 3

$$\begin{array}{c} \underline{\text{A}} \\ a_1 \ a_0 \end{array} \quad \begin{array}{c} \underline{\text{B}} \\ b_1 \ b_0 \end{array}$$

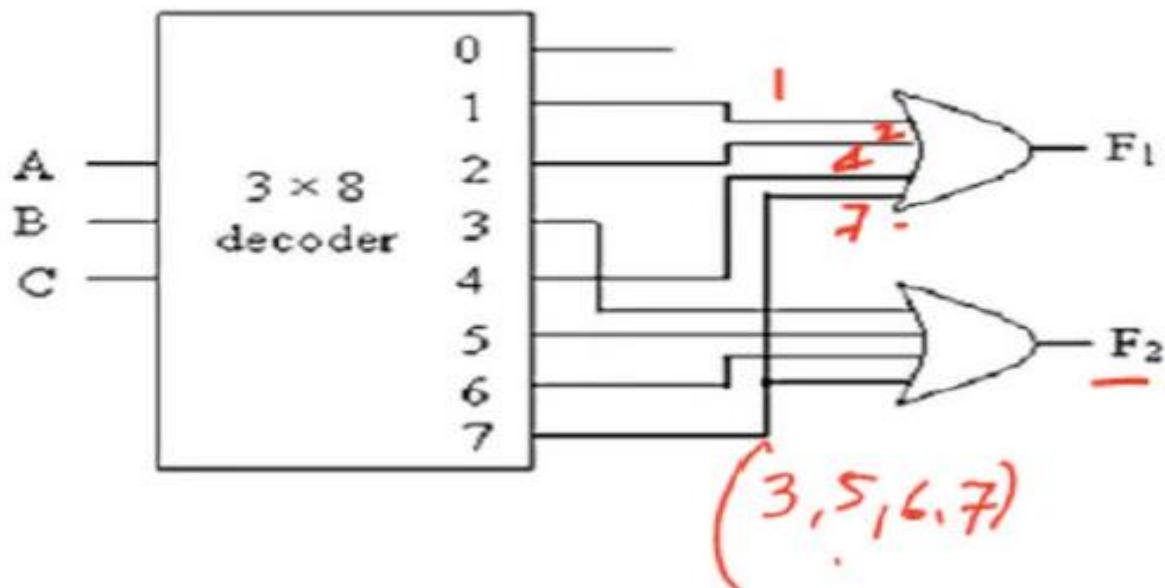
$$A = 10 \quad (b) \ 2, 2, 3$$
$$B = 11 \quad (d) \ 2, 2, 2$$

$$A = 11 \quad (b) \ 2, 2, 3$$
$$B = 10 \quad (d) \ 2, 2, 2$$



What is the name of given circuit?

- (a) Full Subtractor
- (b) Full Adder
- (c) 3-bit even parity generator
- (d) 3-bit odd parity generator



In a 2-bit magnitude comparator circuit ( $A = A_1A_0$ ,  $B = B_1B_0$ ), the expression for  $A > B$  &  $A < B$  is

(a)  $A > B = \bar{A}_1 \bar{B}_1 + (A_1 \oplus B_1) A_0 \bar{B}_0$  ✗  
 $A < B = \bar{A}_1 \bar{B}_1 + (A_1 \oplus B_1) \bar{A}_0 B_0$

(c)  $A > B = A_1 B_1 + (A_1 \oplus B_1) A_0 \bar{B}_0$   
 $A < B = A_1 B_1 + (A_1 \oplus B_1) \bar{A}_0 B_0$

(b)  $A > B = A_1 \bar{B}_1 + (A_1 \oplus B_1) A_0 \bar{B}_0$  ✓  
 $A < B = \bar{A}_1 B_1 + (A_1 \oplus B_1) \bar{A}_0 B_0$  ✓

(d)  $A > B = A_1 B_1 + (A_1 \oplus B_1) A_0 \bar{B}_0$   
 $A < B = A_1 B_1 + (A_1 \oplus B_1) \bar{A}_0 \bar{B}_0$

An  $8 \times 1$  multiplexer has inputs A, B and C connected to the selection input  $S_2$ ,  $S_1$ , and  $S_0$ , respectively. The data inputs  $I_0$  through  $I_7$  are as follows:  
 $I_1 = I_2 = I_7 = 0$ ;  $I_3 = I_5 = 1$ ;  $I_0 = I_4 = D$ ; and  $I_6 = \bar{D}$ ;  
The Boolean function that the multiplexer implements is

- (a)  $Y = \sum m(1, 6, 7, 9, 10, 11, 13)$   
(c)  $Y = \sum m(4, 5, 7, 8, 9, 11, 15)$

- ~~(b)  $Y = \sum m(1, 6, 7, 9, 10, 11, 12)$~~   
(d)  $Y = \sum m(0, 1, 3, 4, 5, 7, 9, 11)$



$$Y = \overline{A}\overline{B}\overline{C}D + \overline{A}\overline{B}C + A\overline{B}\overline{C}D + A\overline{B}C$$

$$(1, 6, 7, 9, 10, 11, 12) + A\overline{B}\overline{C}D$$

1011

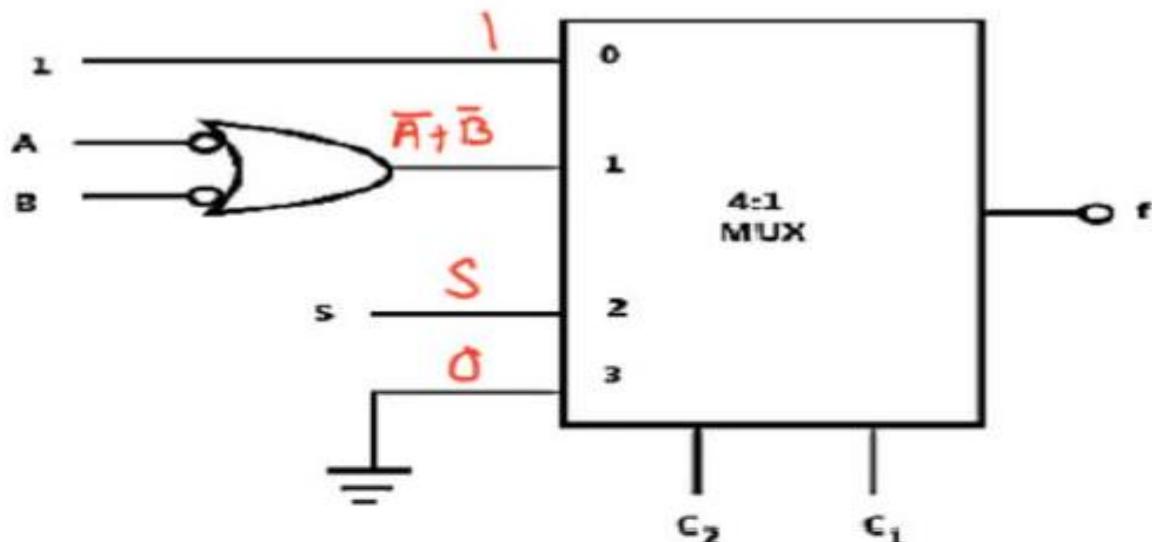
In the following MUX, find the output f.

(a)  $C_2 \cdot \overline{C_1}S + \overline{C_2}C_1(\overline{A} + \overline{B})$

(b)  $\overline{C_2}\overline{C_1} + C_2C_1 + \overline{C_2}\overline{C_1}S + \overline{C_2}C_1\overline{AB}$

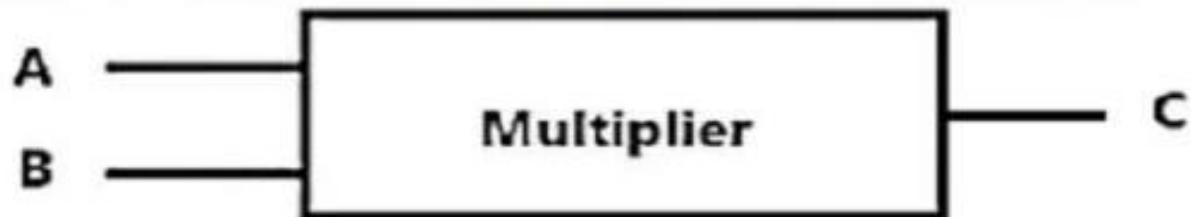
(c)  $\overline{AB} + S$

(d)  ~~$\overline{C_2}C_1 + C_2\overline{C_1}S + \overline{C_2}C_1(\overline{AB})$~~



$$f = \overline{C_2}\overline{C_1} + \overline{C_2}C_1(\overline{A}+\overline{B}) + C_2\overline{C_1}S.$$

Consider a 3-bit number A and 2 bit number B are given to a multiplier. The output of multiplier is realized using AND gate and one bit full adders. If minimum number of AND gates required are X and one bit full adders required are Y, then  $X + Y = \underline{\hspace{2cm}}$ .



$$AND = 6$$

$$A = \begin{matrix} a_2 & a_1 & a_0 \end{matrix}$$

$$x = 6$$

$$HA = 1+1$$

$$B = \begin{matrix} b_1 & b_0 \end{matrix}$$

$$y = 3$$

$$FA = \underline{ }$$

$$\begin{matrix} c_3 & a_2 b_0 & a_1 b_0 & a_0 b_0 \end{matrix}$$

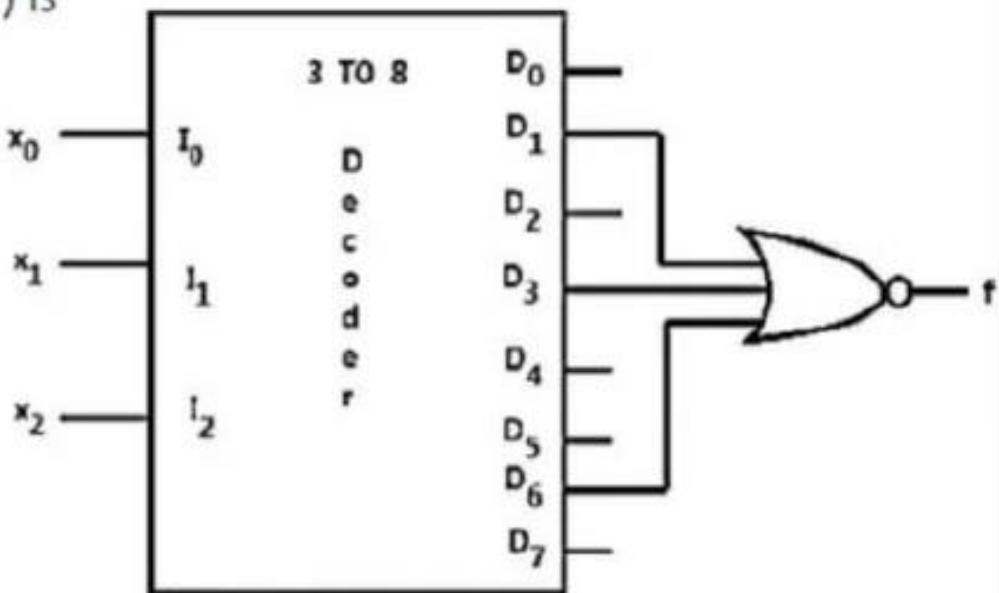
⑨

$$\begin{matrix} a_2 b_1 & a_1 b_1 & b_1 a_0 \\ c_2 & . & . \end{matrix}$$

$$\begin{matrix} c_4 & s_3 & s_2 & s_1 & s_0 \end{matrix}$$

In the following circuit the function  $f(x_2, x_1, x_0)$  is

- (a)  $\prod M(0, 2, 4, 5)$
- (b)  $\sum m(0, 2, 4, 5, 7)$  ✓
- (c)  $\sum m(1, 3, 6)$
- (d)  $\sum M(1, 3, 6)$



$$F = \overline{m_1 + m_3 + m_6}$$

$$= \underline{M_1 \cdot M_3 M_6}$$

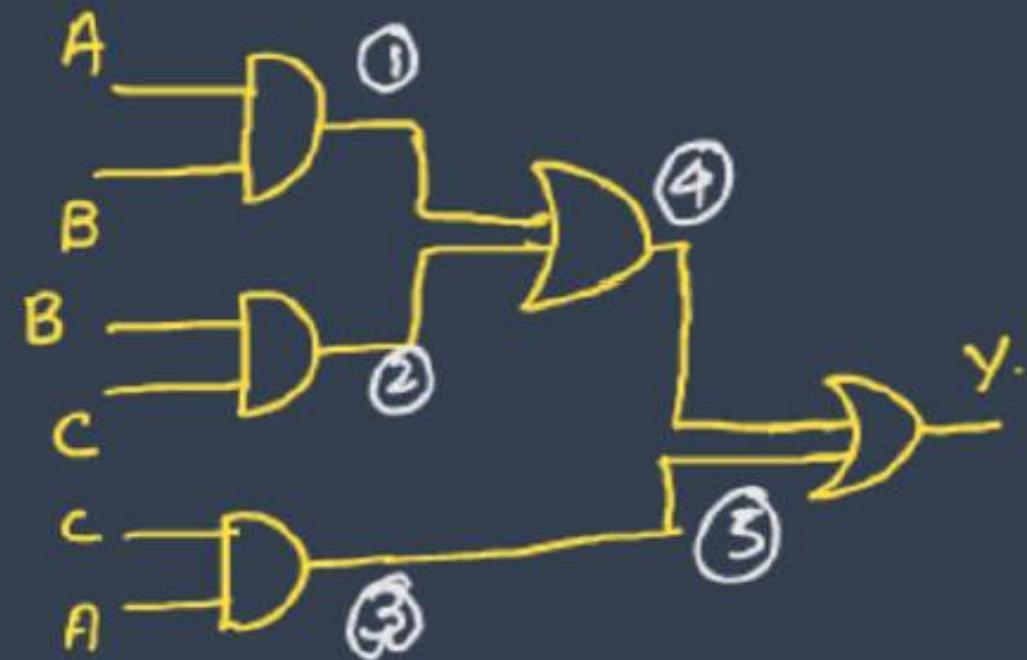
$$f = \underline{\pi M (1, 3, 6)} = \sum m (0, 2, 4, 5, 7)$$

A combinational logic circuit has three inputs A, B and C and one output Y. The output Y = 1 when at least two inputs are 1. Otherwise, Y = 0. In its minimized SOP realization, the maximum number of two input terms is \_\_\_\_.

Majority logic gate

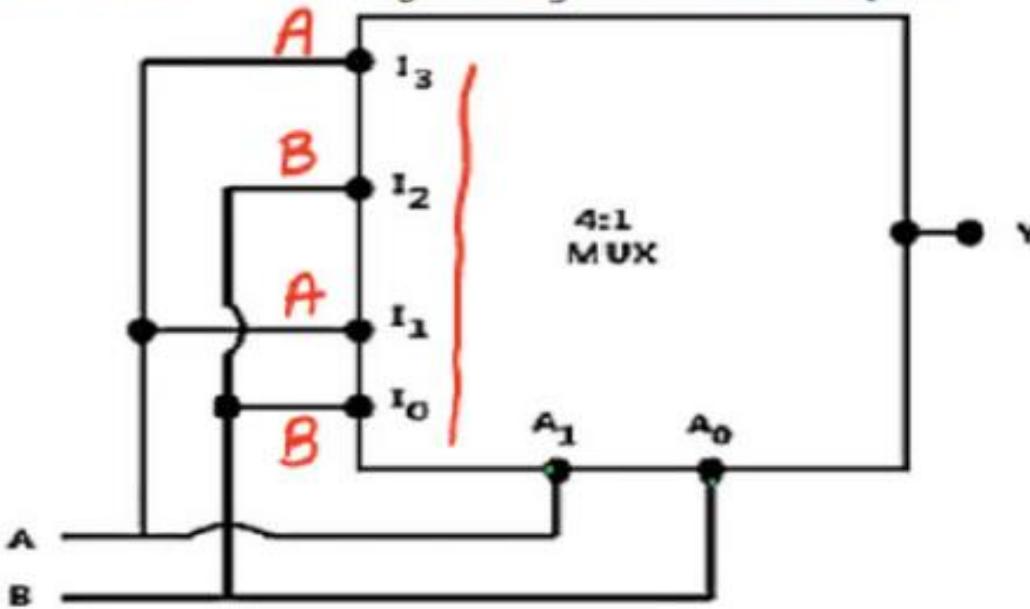
$$Y = \sum m(3, 5, 6, 7)$$

$$Y = AB + BC + CA$$



A gate having two inputs (A, B) and one output (Y) is implemented using 4 :1 MUX as shown in figure below.  $A_1$  (MSB) and  $A_0$  are the control bits and  $I_0$  to  $I_3$  are the inputs to the MUX. The gate is

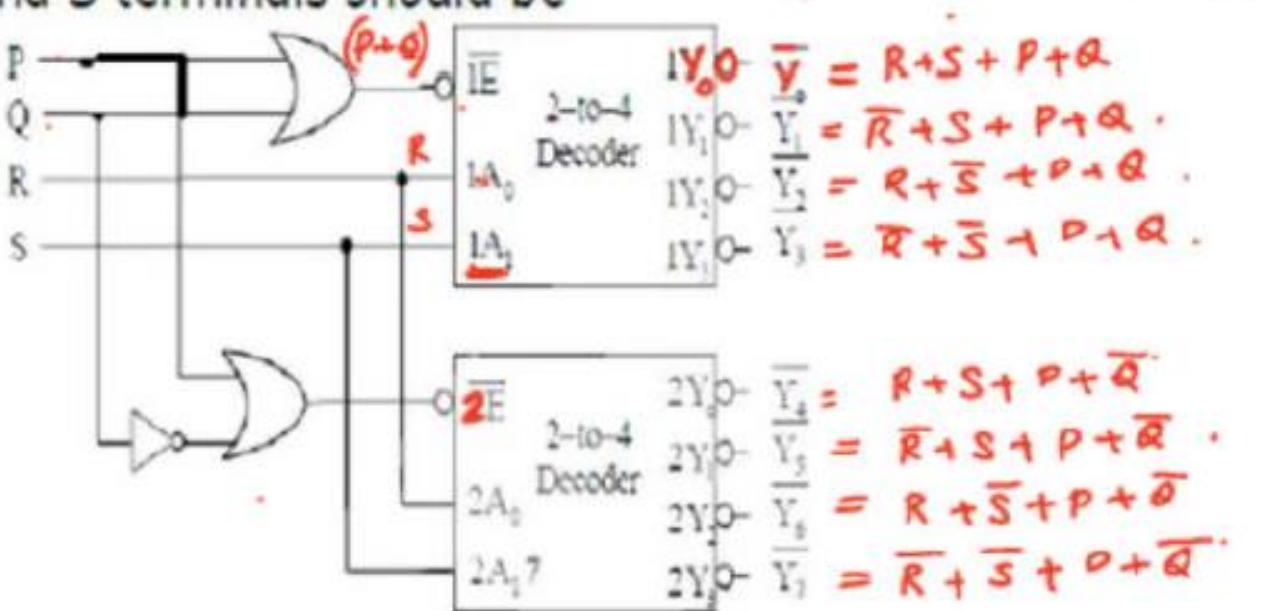
- (a) AND ✓
- (b) NOR
- (c) OR
- (d) EX-OR



$$Y = \bar{A} \bar{B} (I_3) + \bar{A} B (I_2) + A \bar{B} (I_1) + A B (I_0)$$

$$Y = AB$$

A 1-to-8 demultiplexer with data input  $D_{in}$ , address inputs  $S_0, S_1, S_2$  (with  $S_0$  as the LSB) and  $\bar{Y}_0$  to  $\bar{Y}_7$  as the eight demultiplexed output, is to be designed using two 2-to-4 decoders (with enable input  $\bar{E}$  and address input  $A_0$  and  $A_1$ ) as shown in the figure.  $D_{in}, S_0, S_1$  and  $S_2$  are to be connected to P, Q, R and S, but not necessarily in this order. The respective input connections to P, Q, R and S terminals should be



- A.  $S_2, D_{in}, S_0, S_1$  B.  $S_1, D_{in}, S_0, S_2$   
 C.  $D_{in}, S_0, S_1, S_2$  D.  $D_{in}, S_2, S_0, S_1$

$$\begin{aligned} P &= D_{in} \\ Q &= S_2 \\ R &= S_0 \\ S &= S_1 \end{aligned}$$

$D_{in}$

$1 \times 8$

DEMUX.

$S_2 \quad S_1 \quad S_0$

$$\overline{y}_0 = S_2 + S_1 + S_0 + D_{in}$$

$$\overline{y}_1 = S_2 + S_1 + \overline{S_0} + D_{in}$$

$$\overline{y}_2 = S_2 + \overline{S_1} + S_0 + D_{in}$$

$$\overline{y}_3 = S_2 + \overline{S_1} + \overline{S_0} + D_{in}$$

$$\overline{y}_4 = \overline{S_2} + S_1 + S_0 + D_{in}$$

$$\overline{y}_5 = \overline{S_2} + S_1 + \overline{S_0} + D_{in}$$

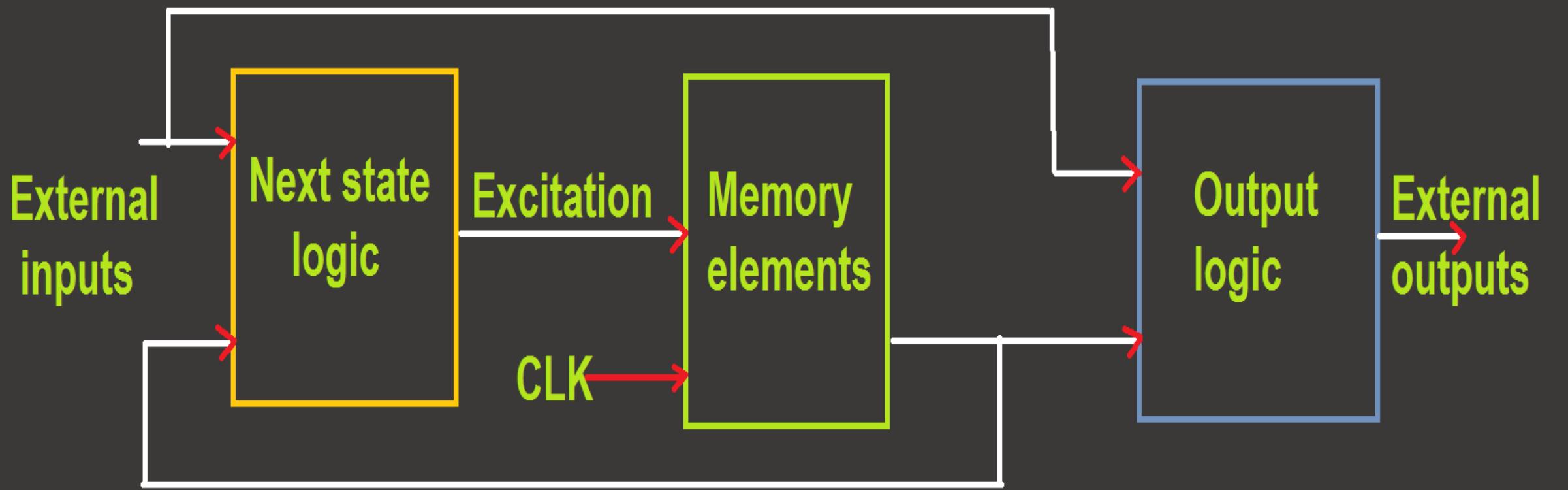
$$\overline{y}_6 = \overline{S_2} + \overline{S_1} + S_0 + D_{in}$$

$$\overline{y}_7 = \overline{S_2} + \overline{S_1} + \overline{S_0} + D_{in}$$

# Sequential Circuits

# Sequential Circuits

## Block Diagram of Sequential Circuits



# Comparison between combinational and sequential circuits

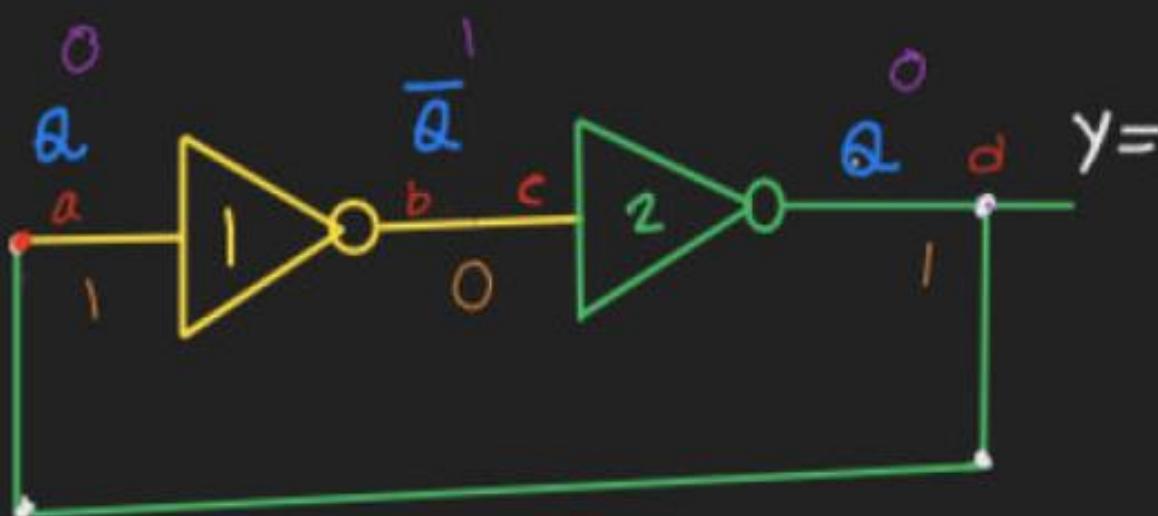
Combinational circuits	Sequential circuits
1. In combinational circuits , the output at any instant of time dependent only on the present input variables	1. In sequential circuits , the output at any instant of time dependent not only on the present input , but also on the present state . i.e on the past history of the system
2. Memory unit is not required	2. Memory unit is required to store the past history of the input
3. Combinational circuits are faster	3. Sequential circuits are slower than combinational circuits
4. Combinational circuits are easy to design	4. Sequential circuits are comparatively harder to design

The logic circuit whose outputs at any instant of time depends on the present inputs as well as on the past outputs are called sequential circuits, in sequential circuits , the output signals are fed back to the input side .

# Sequential Circuits

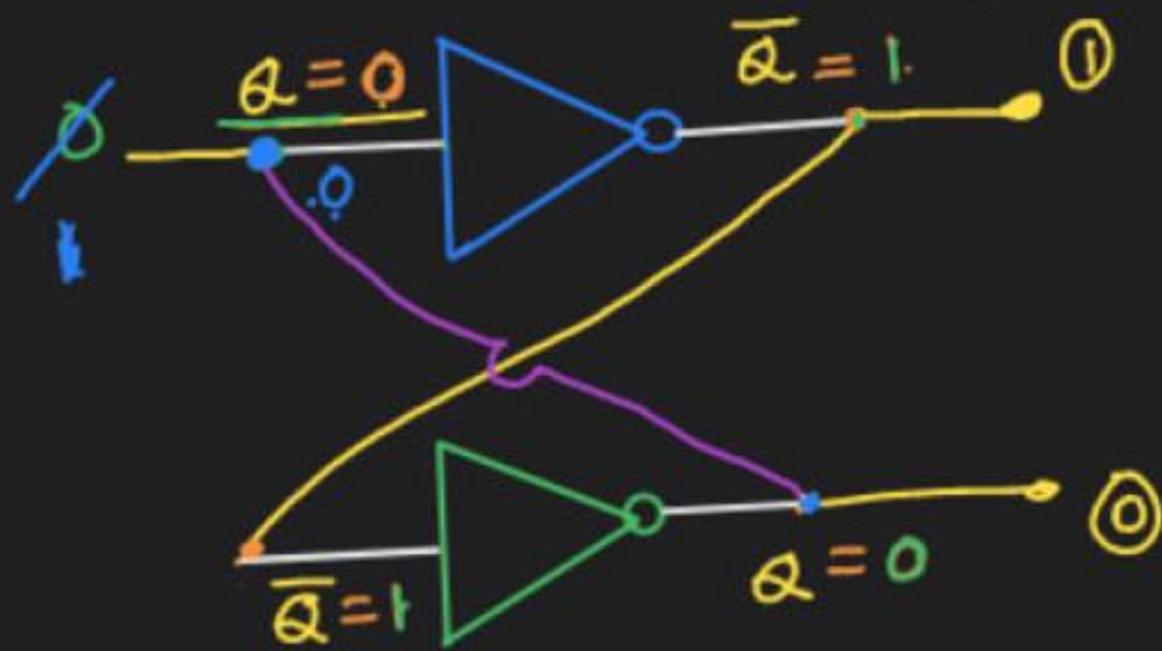
- Latch
- Flip flops
- Shift Register
- counters

**Latch** → Bistable multivibrator.



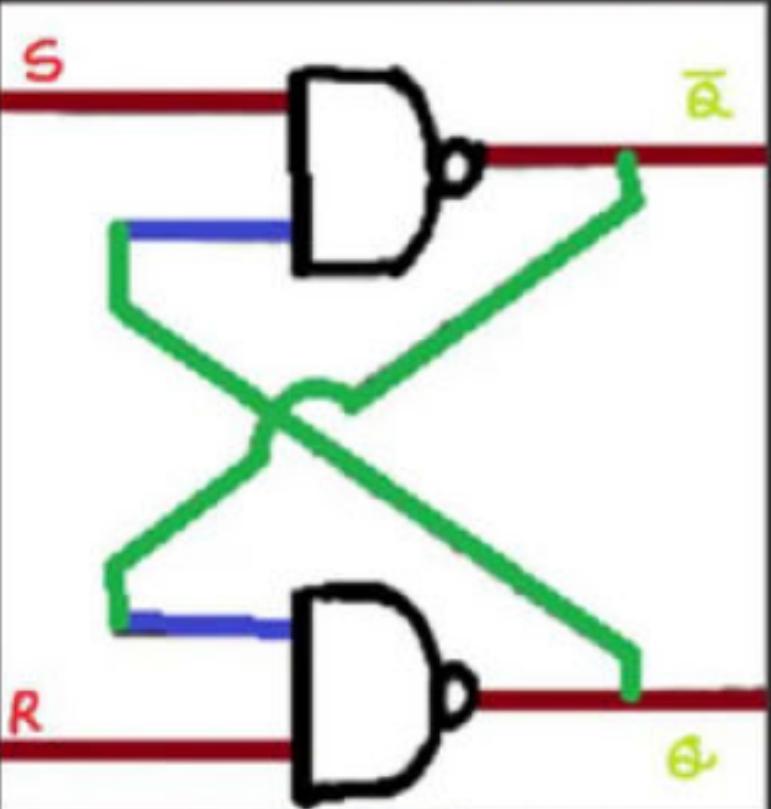
→ Basic memory unit.

→ Store 1-bit of information.



✓  
 dat ch

# NAND Latch



$Q \rightarrow \text{Previous O/P} = Q_n$

$Q^+ \rightarrow \text{Present O/P} = Q_{n+1}$

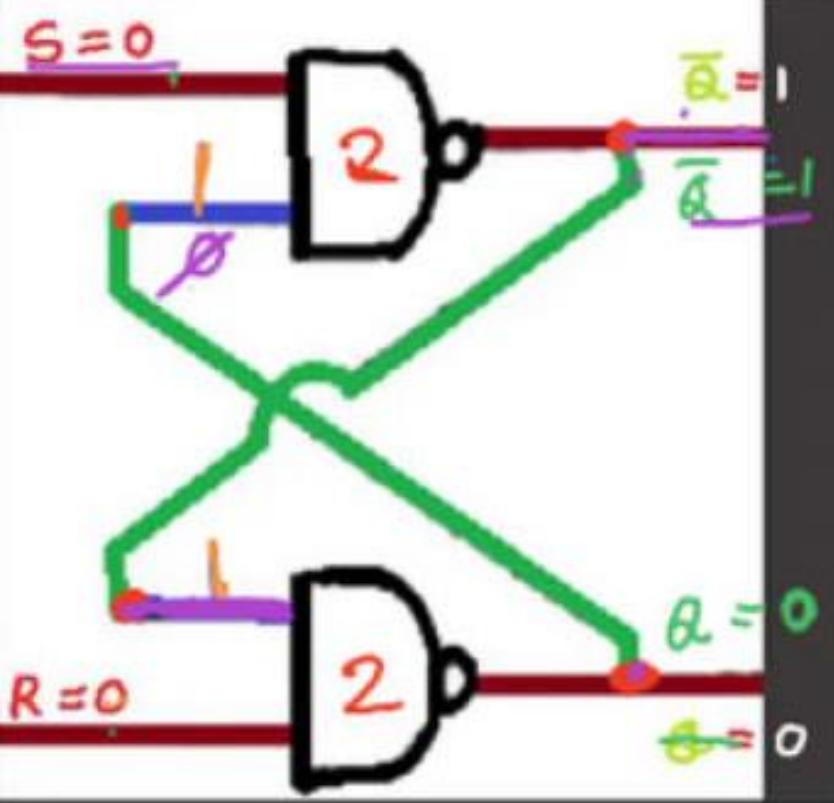
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

S	R	Q	$Q^+$	$\bar{Q}^+$
0	0	0	1	1
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	0	1

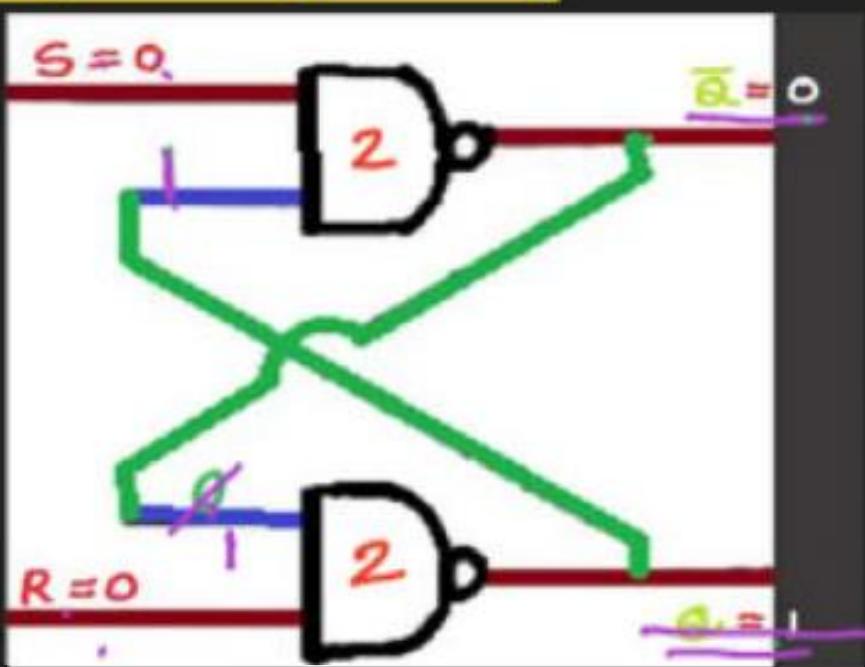
Set      Reset

S	R	$Q^+$	State
0	0	X	Invalid $(Q^+ = \bar{Q}^+ = 1)$
0	1	0	Reset
1	0	1	Set
1	1	Q	No change

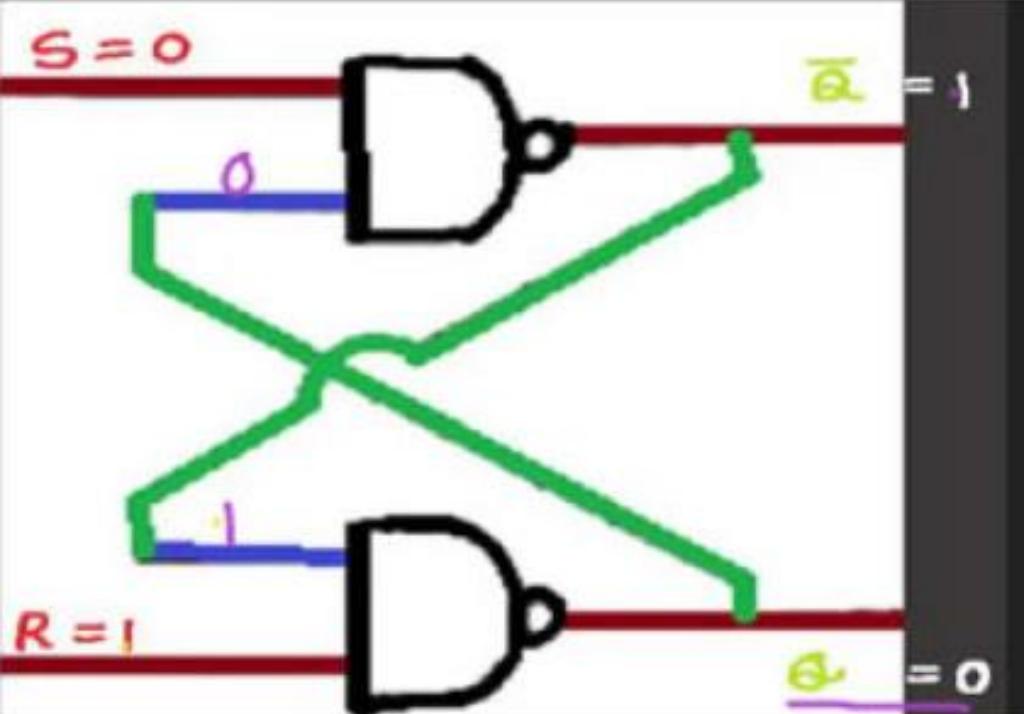
(memory)  
(hold)



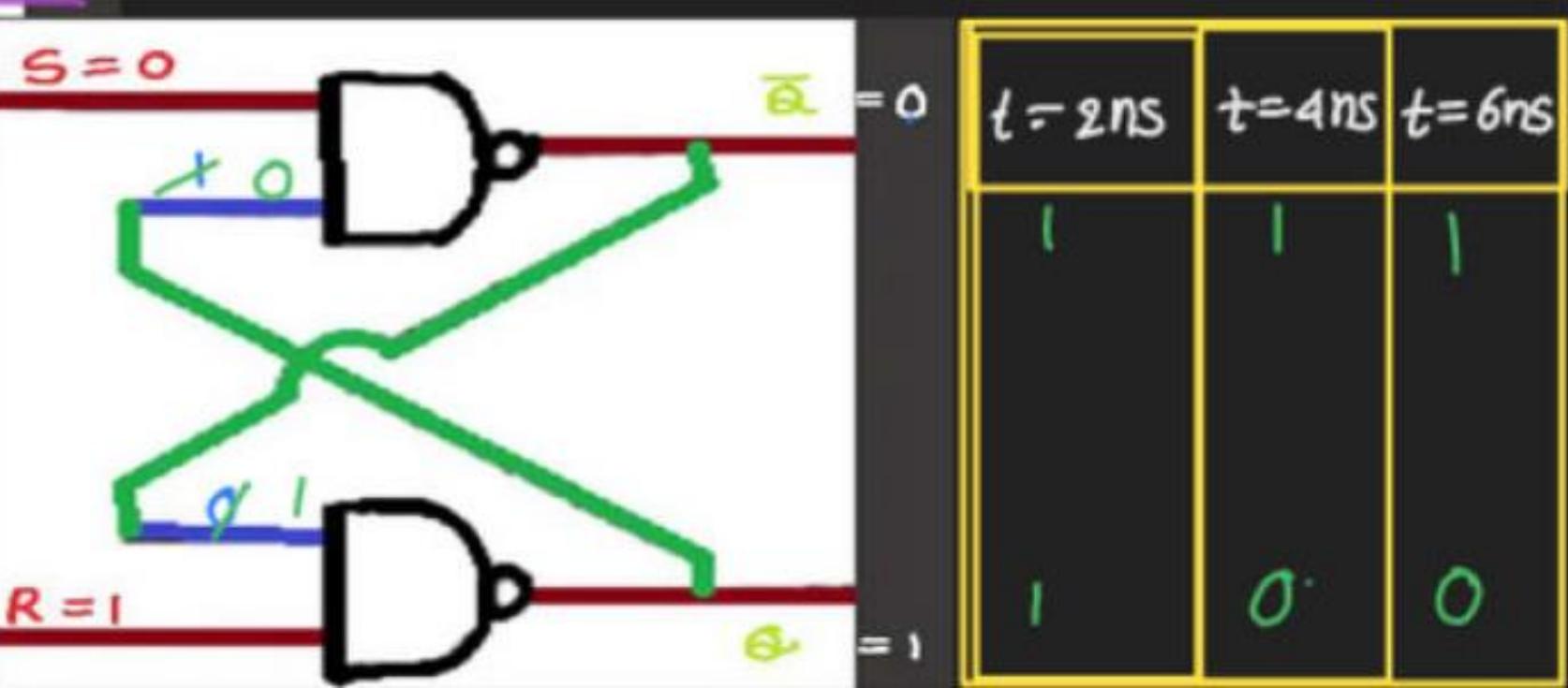
$t = 2\text{ns}$	$t = 4\text{ns}$
1	1
1	1

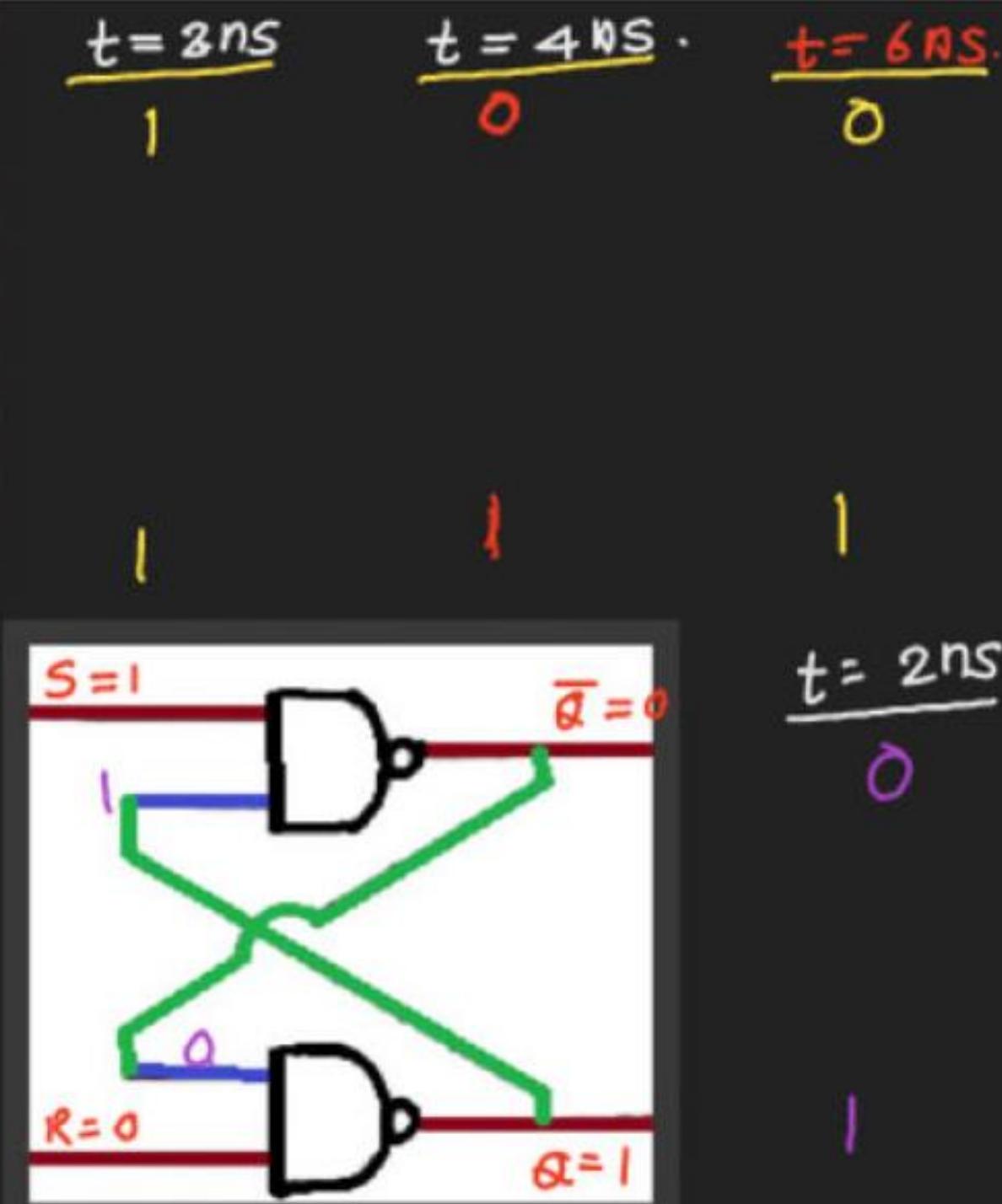
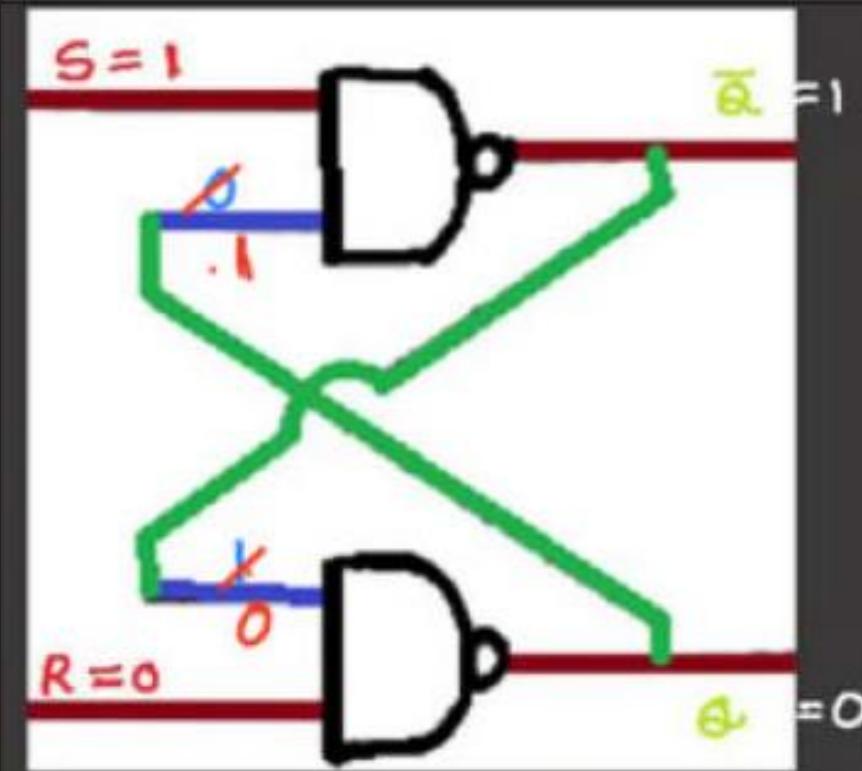


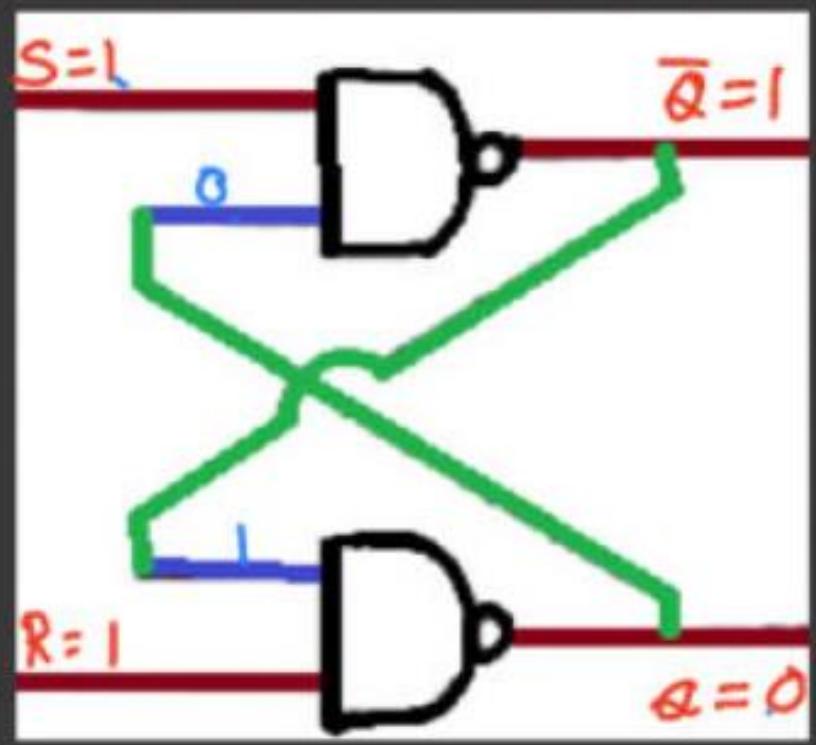
$t = 2\text{ns}$	$t = 4\text{ns}$
1	1
1	1



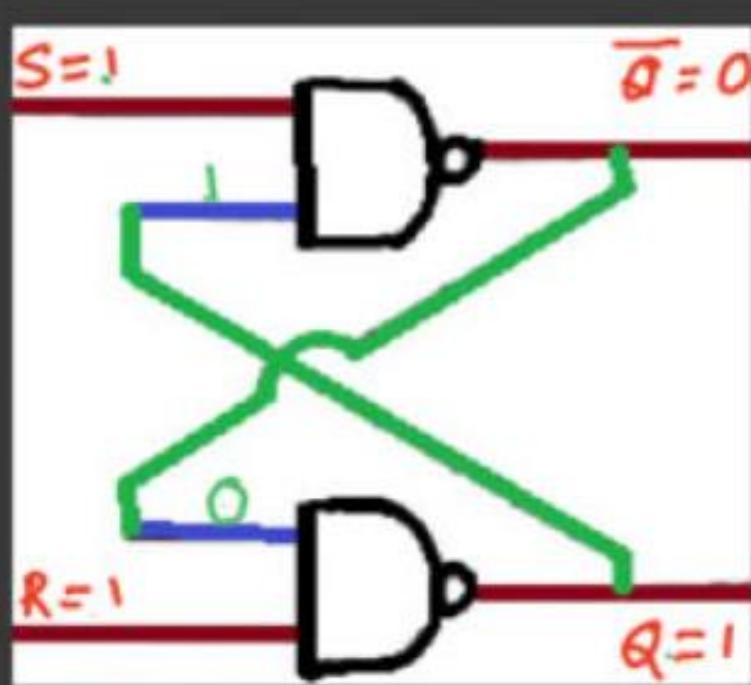
$$\frac{t = 2\text{ns}}{1}$$





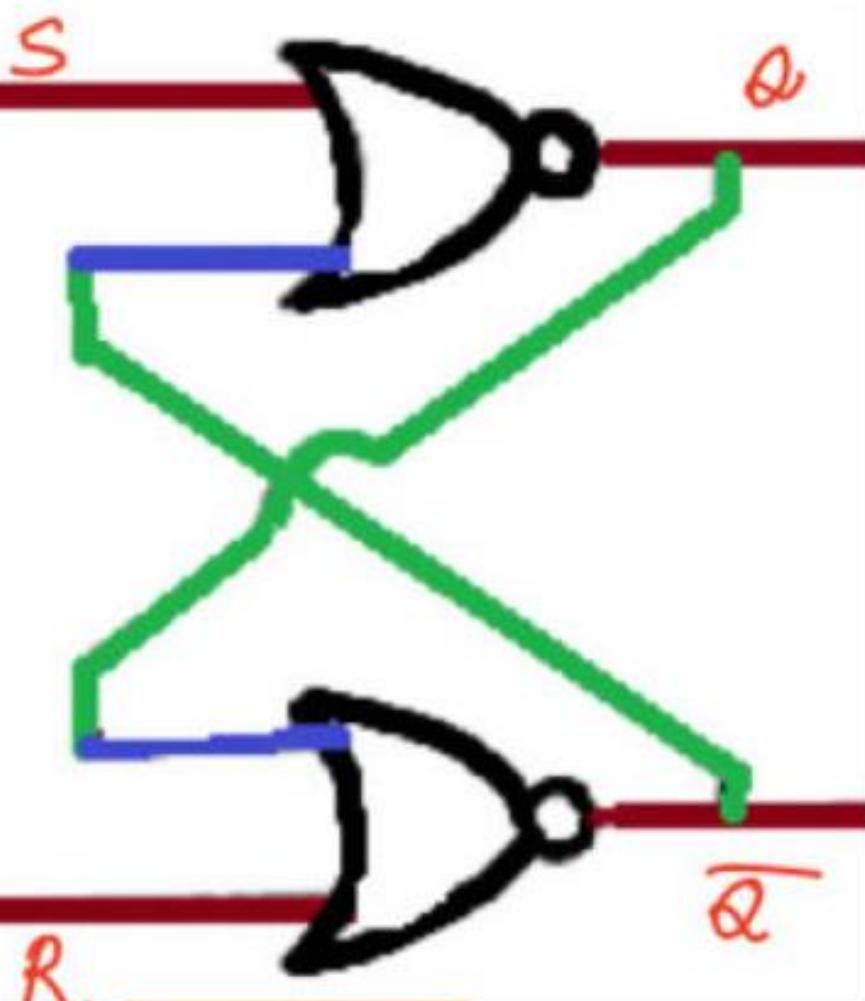


$t = 2 \text{ ns}$



$t = 2 \text{ ns}$

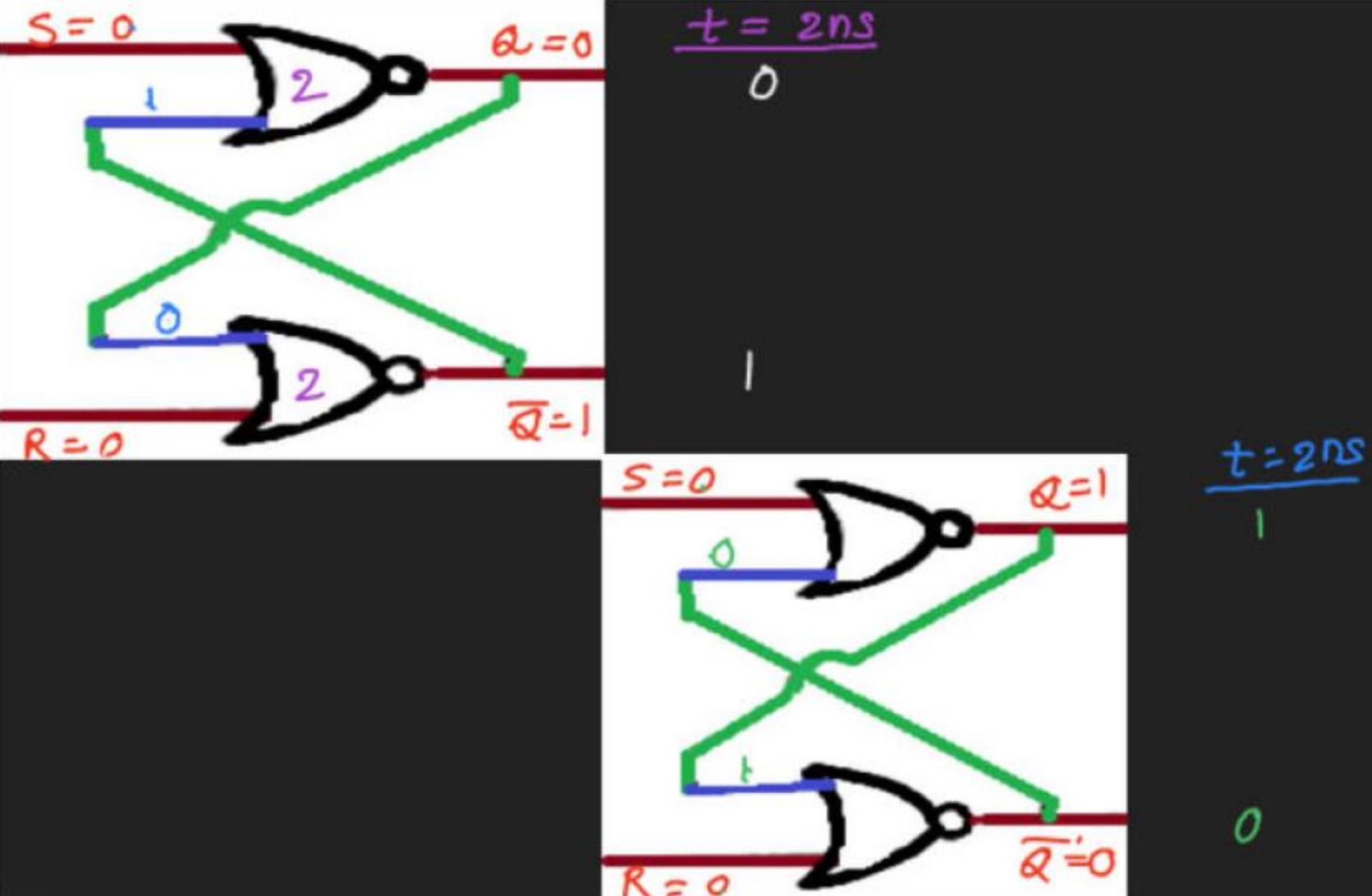
# NOR Latch

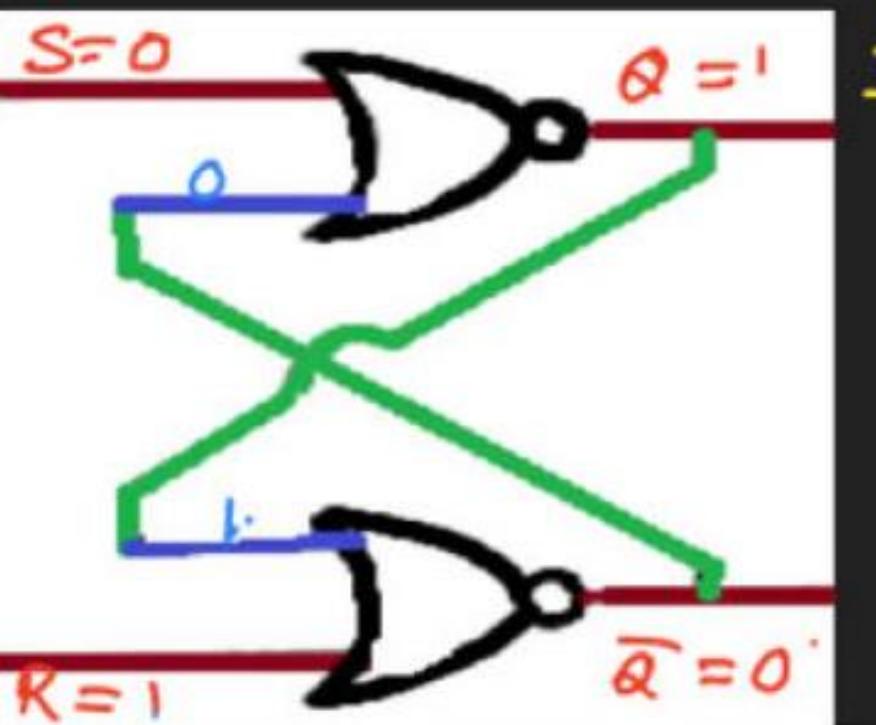
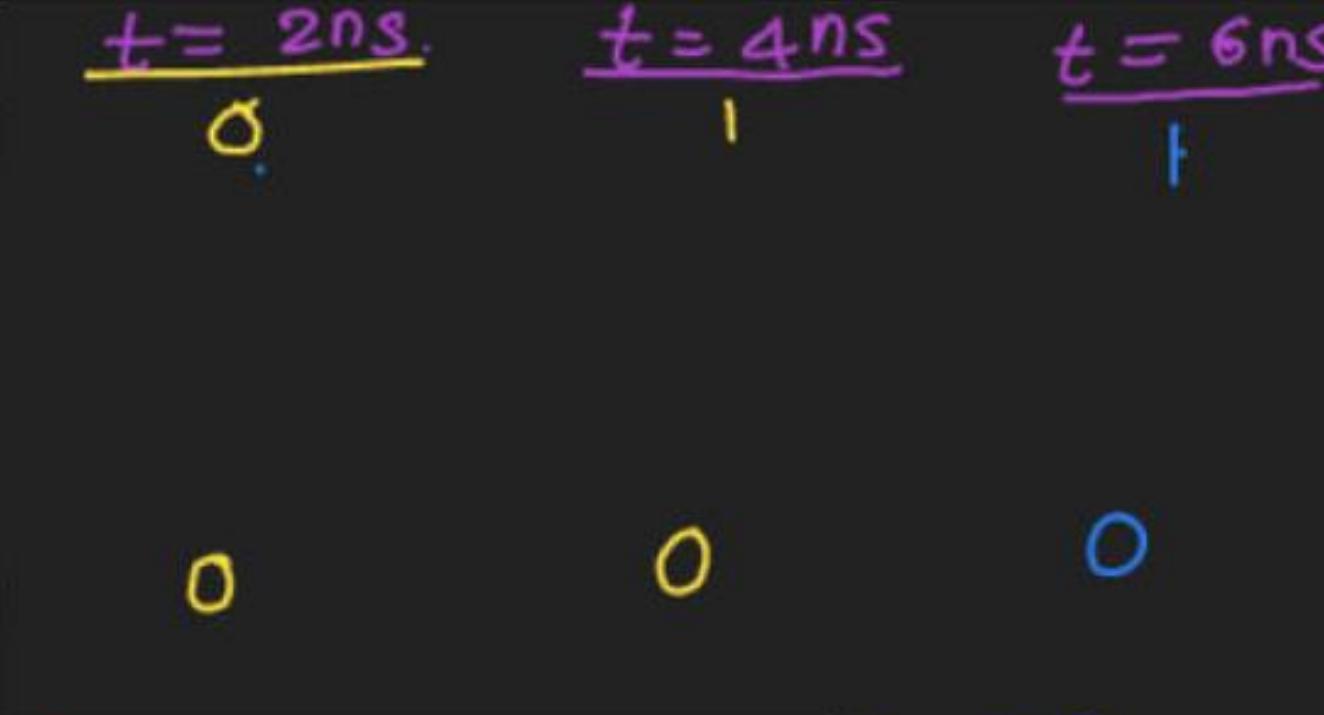
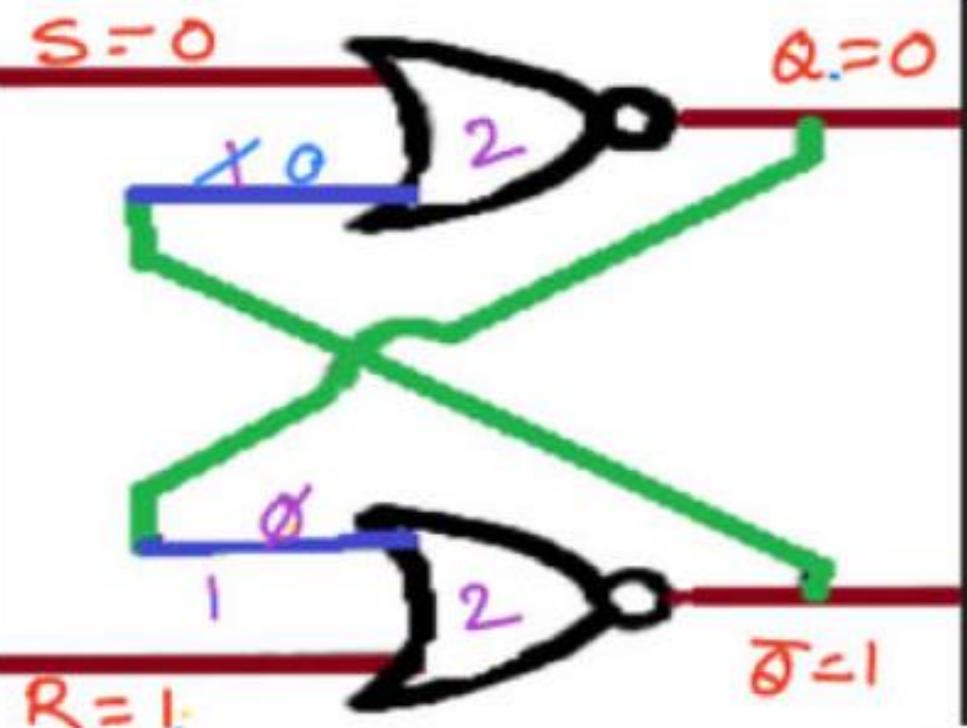


A	B	Y
0	0	1
0	1	0
1	0	0

S	R	Q	Q <sup>+</sup>	Q̄ <sup>+</sup>
0	0	0	0	1
		0	1	0
0	1	1	1	0
		1	0	0
1	0	0	0	1
		0	1	0
1	1	1	1	0
		1	0	0

S	R	$Q^+$	State
0	0	Q	memory (hold/no change)
0	1	I	set
1	0	O	Reset
1	1	X	invalid ( $Q^+ = \bar{Q}^+ = 0$ )

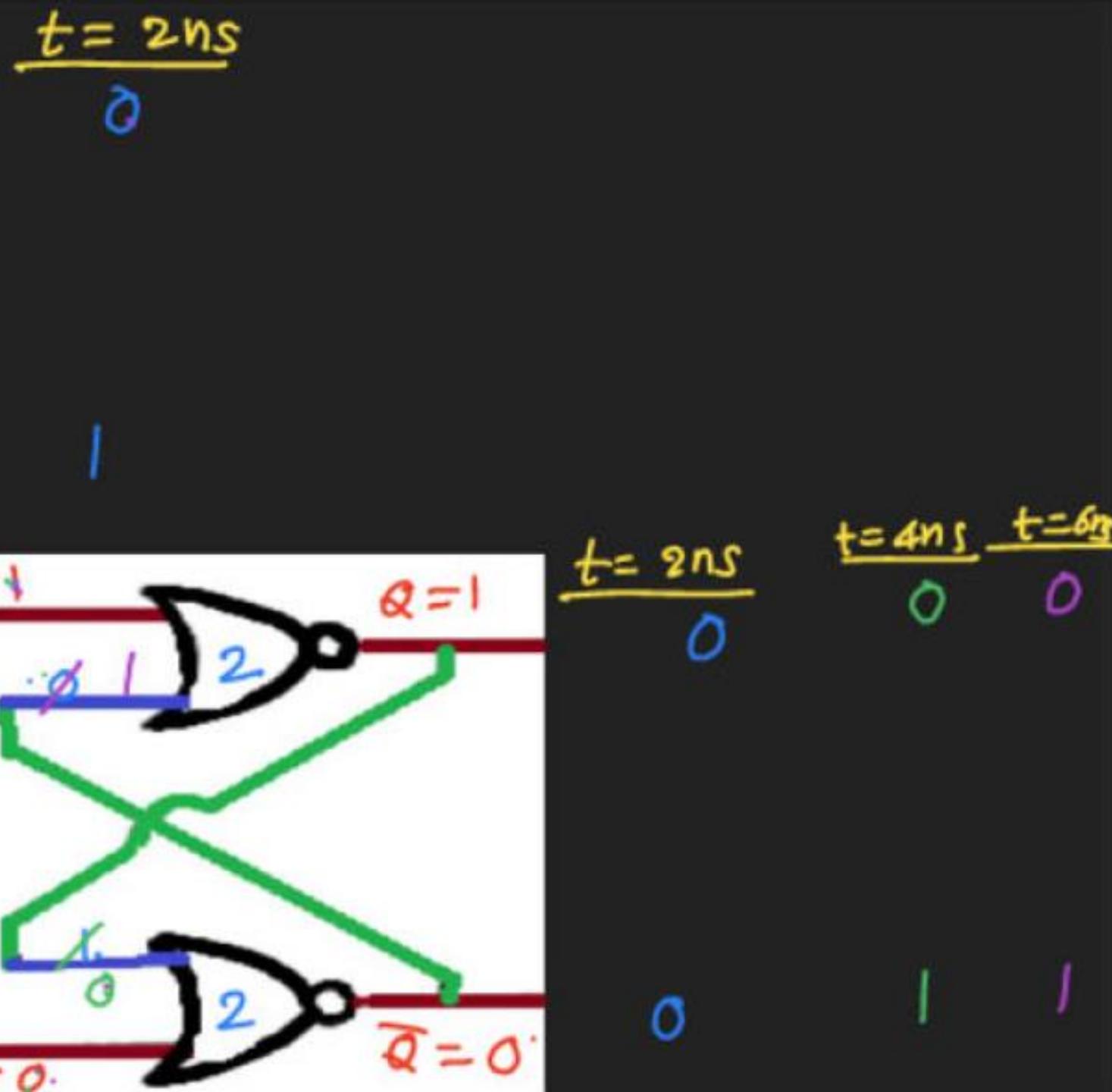
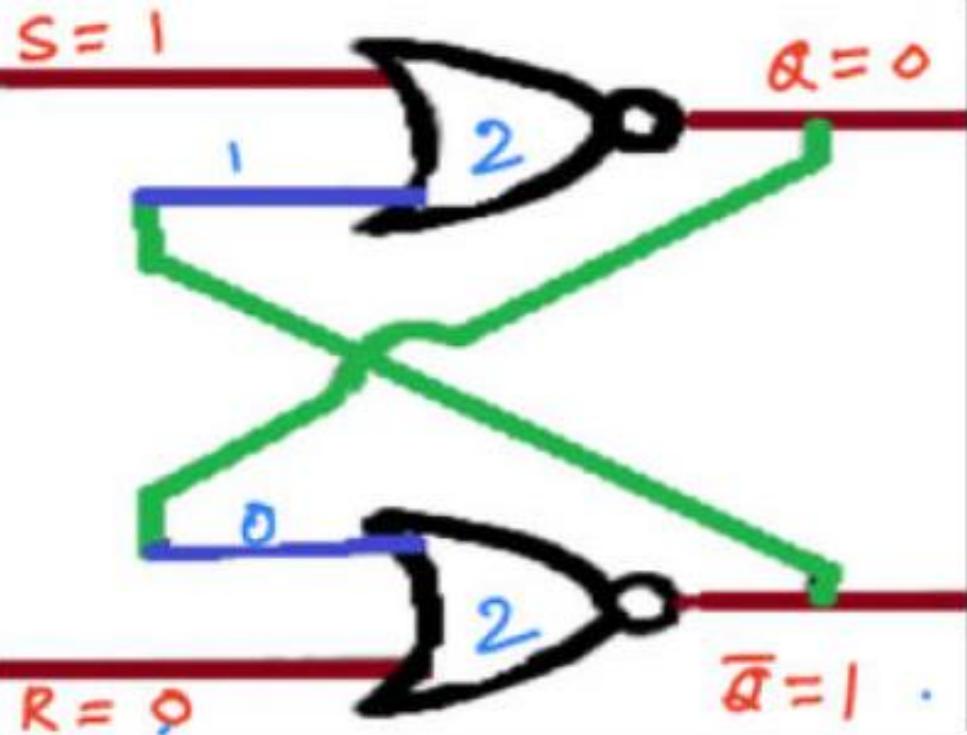


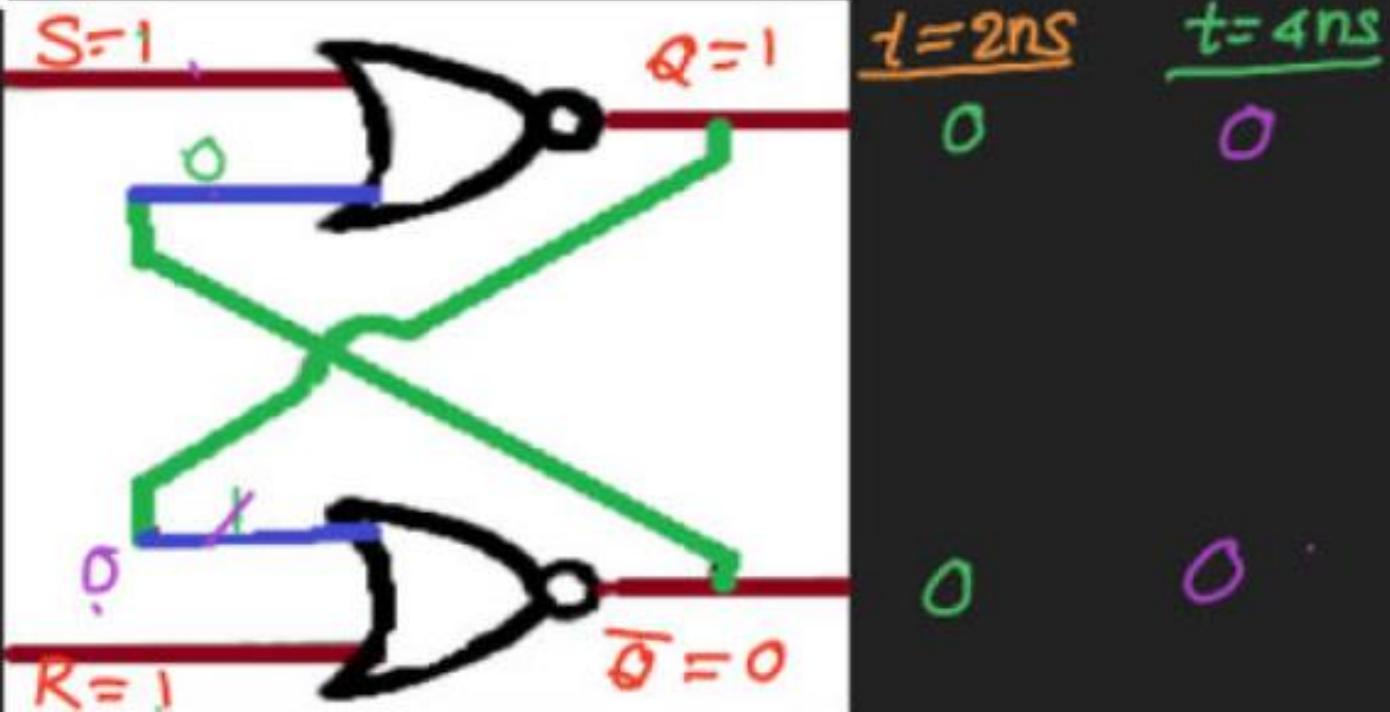
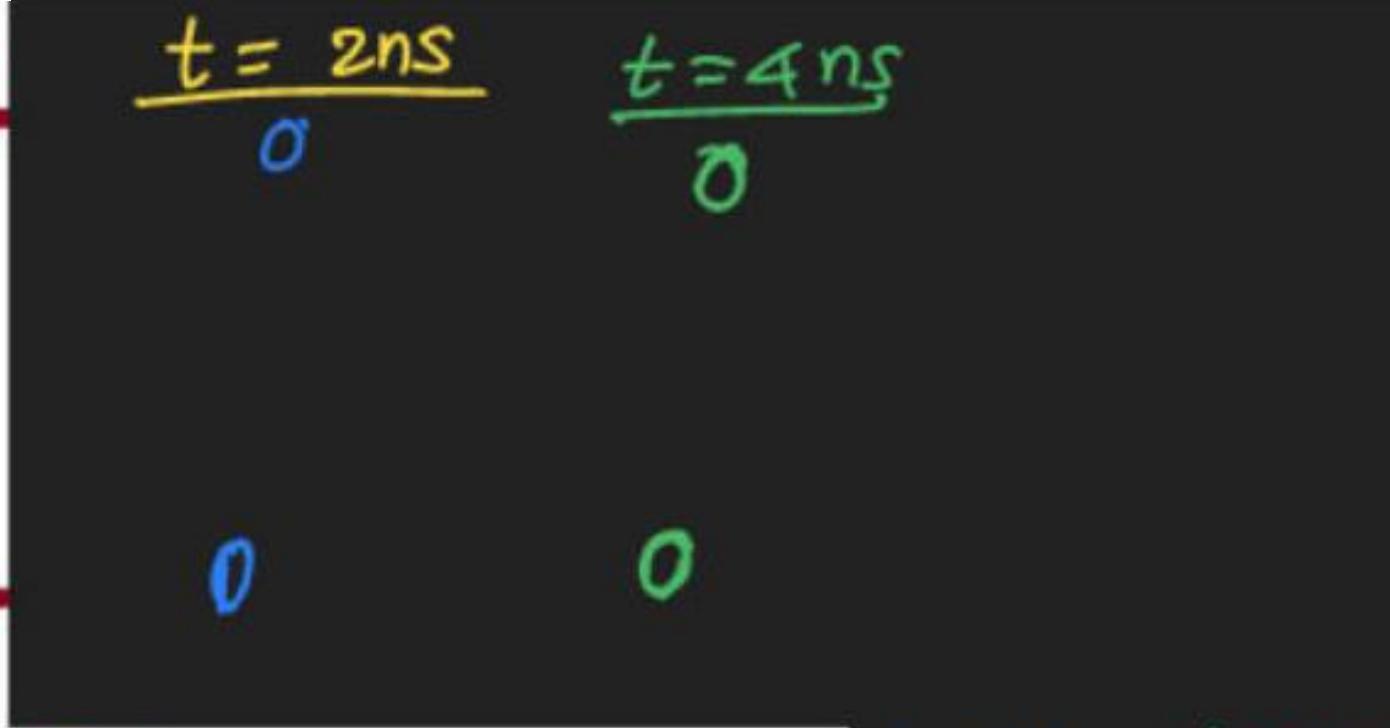
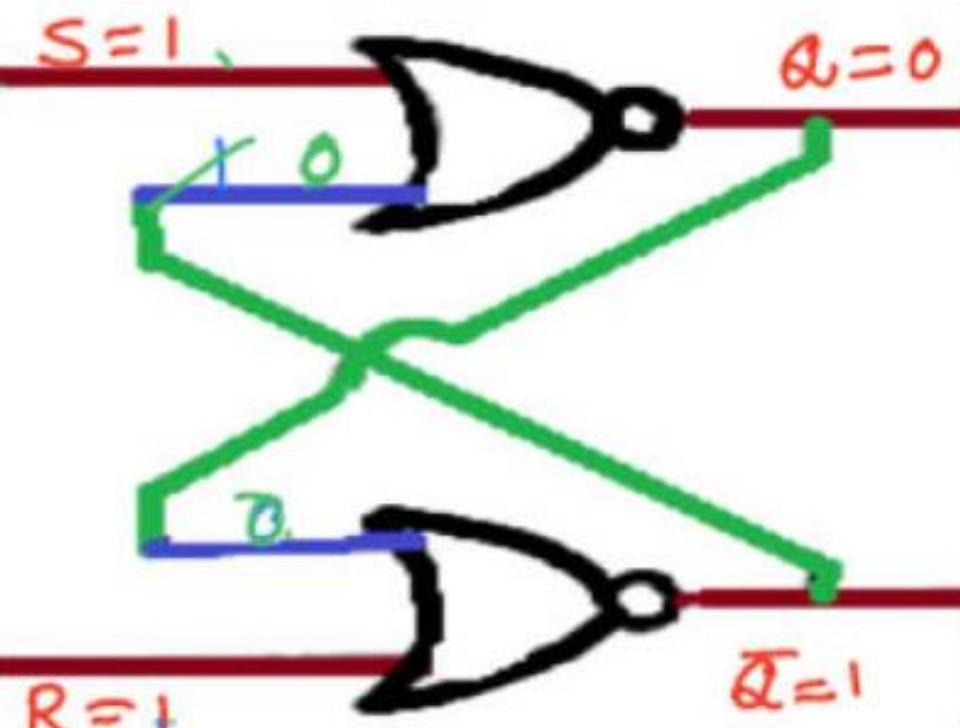


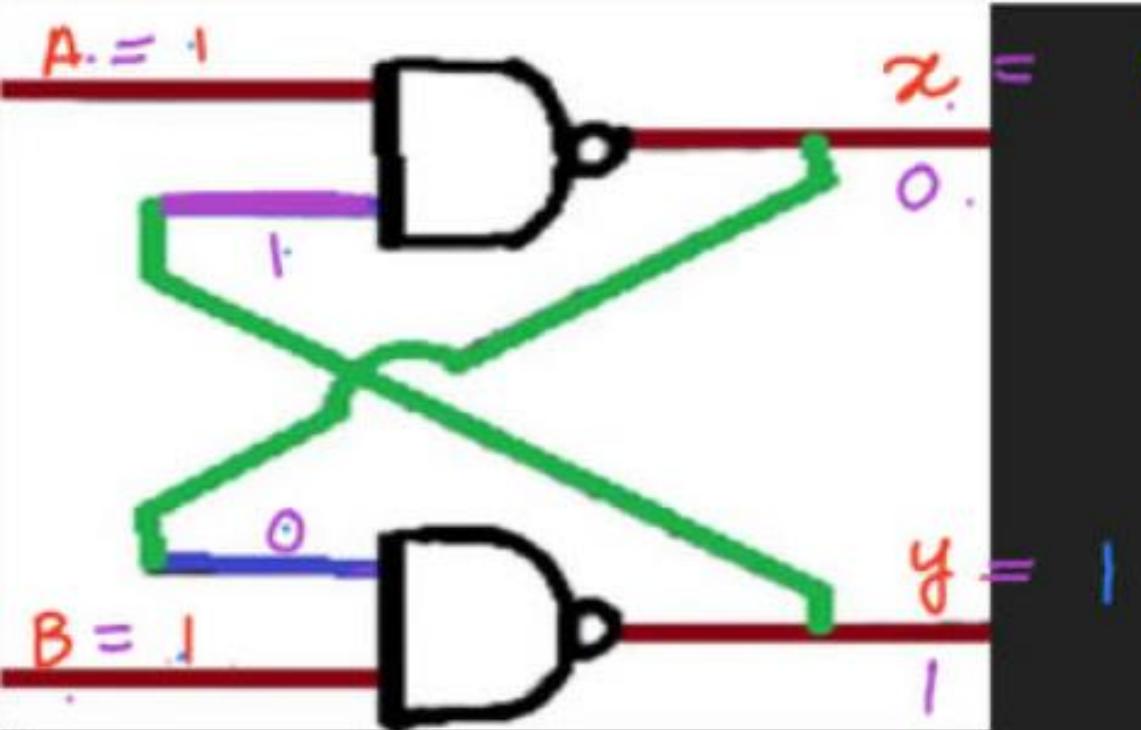
$t = 4 \text{ ns}$

$1$

$0$

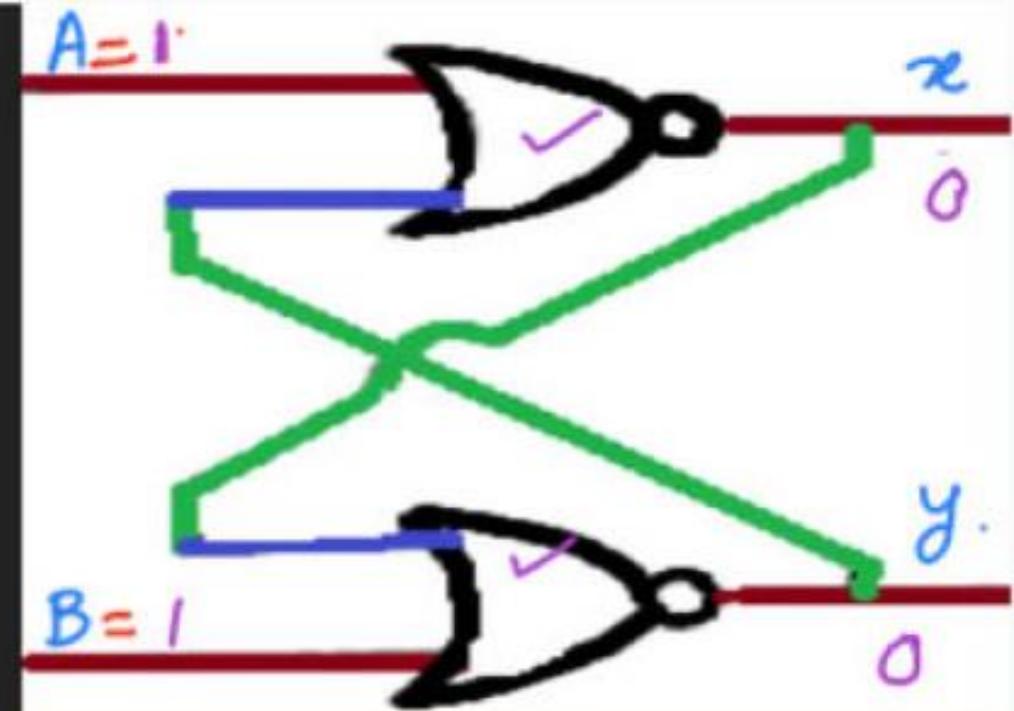






$A$	$B$	$x$	$y$
0	0	1	1
0	1	1	0
1	0	0	1
1	1	memory	

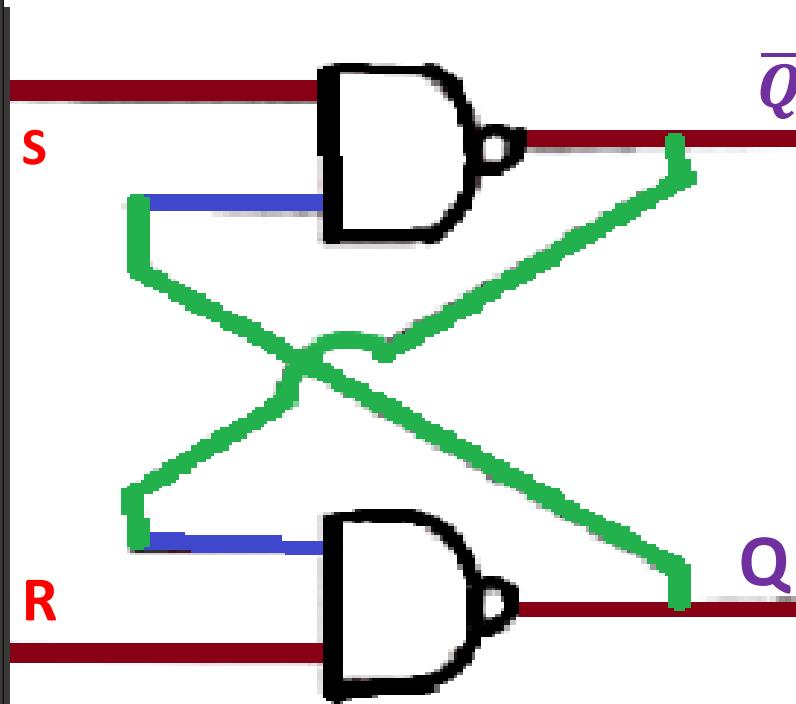
$$\overline{1+x} = 0$$



$A$	$B$	$x$	$y$
0	0	0	memory
0	1	1	0
1	0	0	1
1	1	1	0

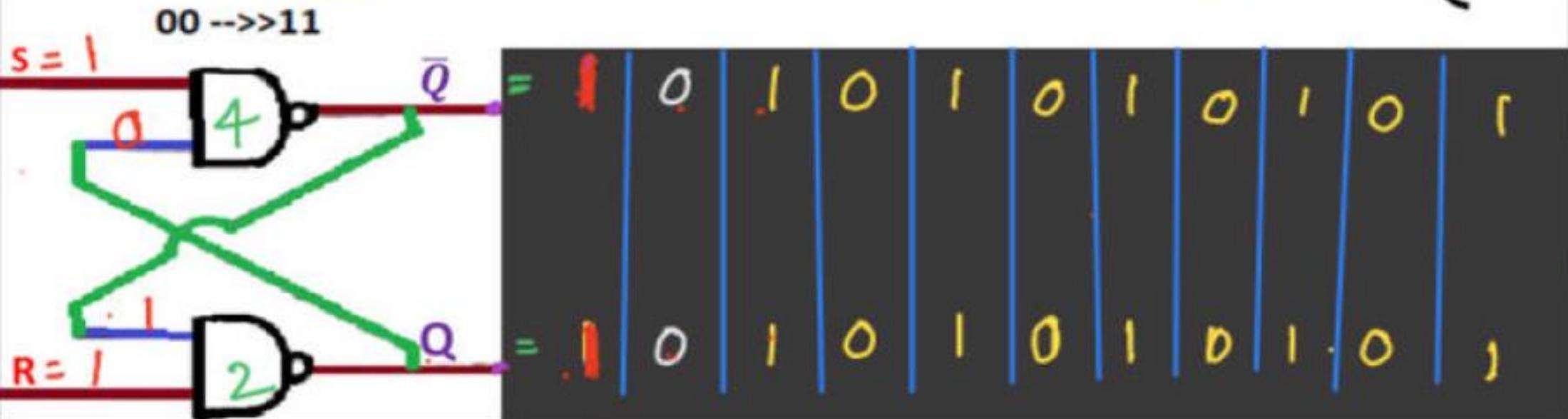
Assume initially  $Q = 0$  for given ckt then find the o/p for the following sequence (SR)

01 -->10 -->11 -->00 -->01--> 11 -->10



- Out put of combinational circuit depends on input combinations .
- Output of sequential circuits depends on input sequence.
- For unequal delay of gates also the operation is valid.

Assume initially  $Q = 0$  for given ckt then find the o/p for the following sequence (SR)



Critical  
Race  
↓  
For Equal  
Delays.

# For unequal delays

$$\overline{Q} = 1 \quad 0$$

$$\overline{Q} = 1$$

Q = 1

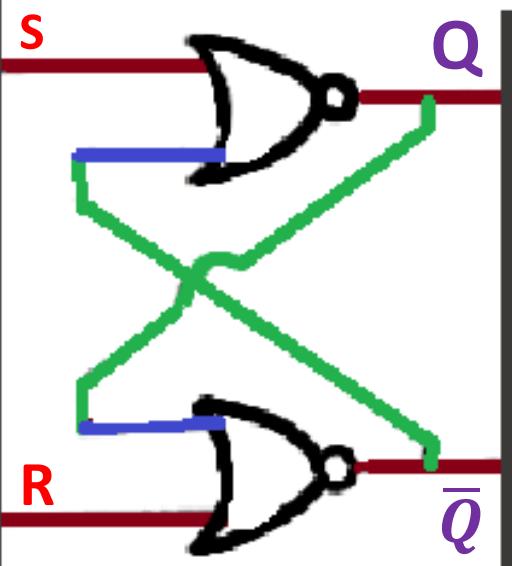
$$Q = \begin{pmatrix} 1 & 0 \\ 0 & 0 \end{pmatrix}$$

For **SR NAND** latch , if the input sequence is **00 -----> 11** , then the following cases arises

- If the delay of both gates are same then we don't have any stable output , the output is oscillatory , this condition is known as critical race
- However if the delay of both gates are not equal then there exist a stable output , but it depends on the individual delay of the gates

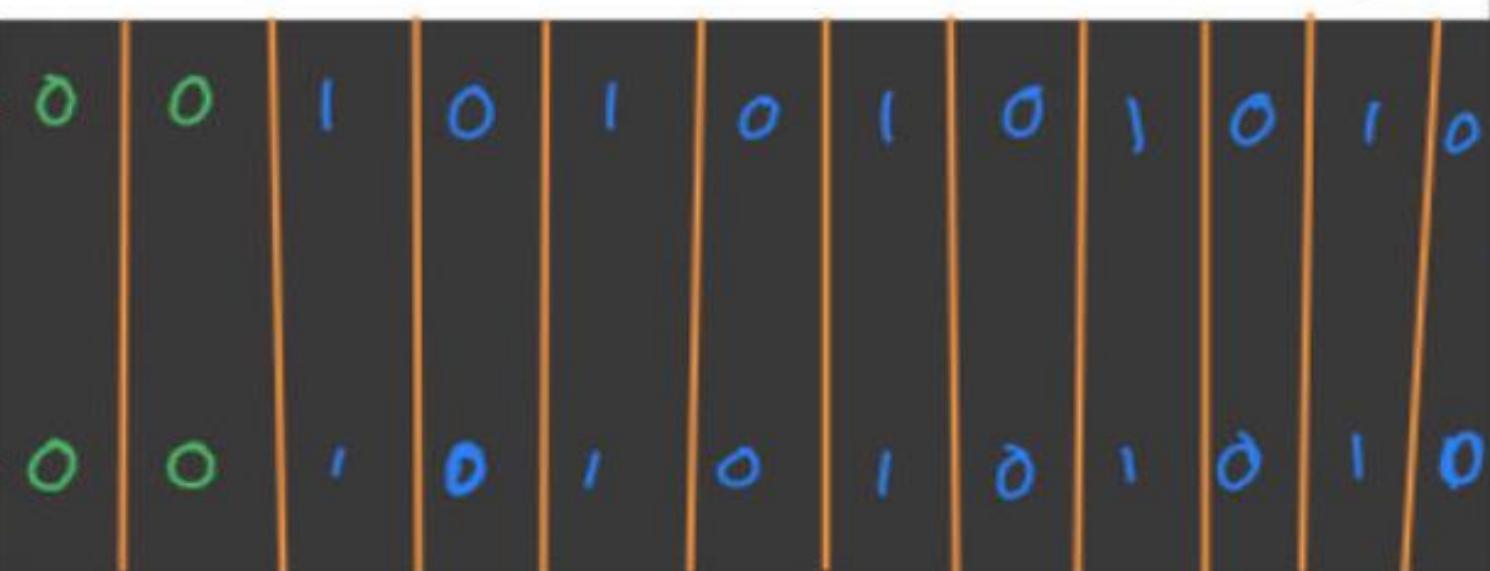
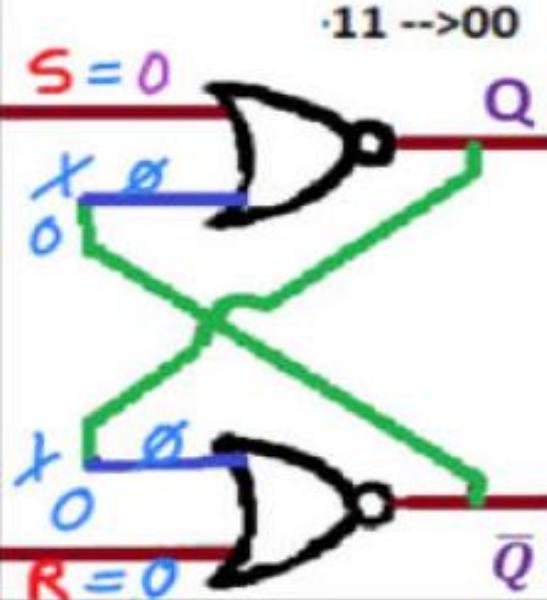
Assume initially  $Q = 0$  for given ckt then find the o/p for the following sequence (SR)

01-->10-->00-->11-->01-->11--10



S	R.	$Q^t$	$\bar{Q}^t$
0	1	1	0
1	0	0	1
0	0	0	1
1	1	0	0
0	1	1	0
1	1	0	0
1	0	0	1

Assume initially  $Q = 0$  for given ckt then find the o/p for the following sequence (SR)



Equal delay  
Critical Race

For unequal delays

$$\bar{Q} = 1 \quad 0$$

$$\bar{Q} = 1 \quad 1$$

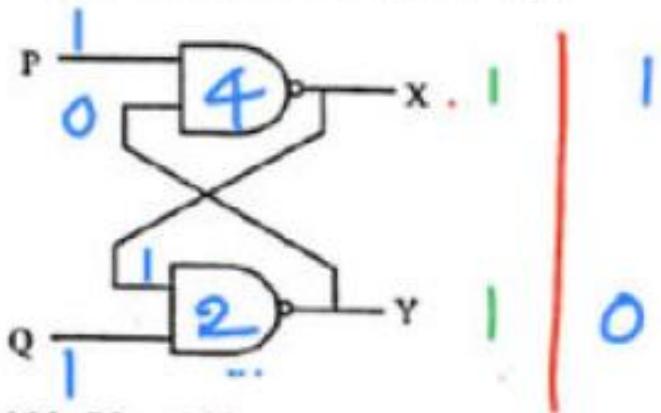
$$Q = 1 \quad 1$$

$$Q = .1. \quad 0$$

For **SR NOR** latch , if the input sequence is **11 -----> 00** , then the following cases arises

- If the delay of both gates are same then we don't have any stable output , the output is oscillatory , this condition is known as critical race .
- However if the delay of both gates are not equal then there exist a stable output , but it depends on the individual delay of the gates .

In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is:  $P = Q = '0'$ . If the input condition is changed simultaneously to  $P = Q = '1'$ , the outputs X and Y are



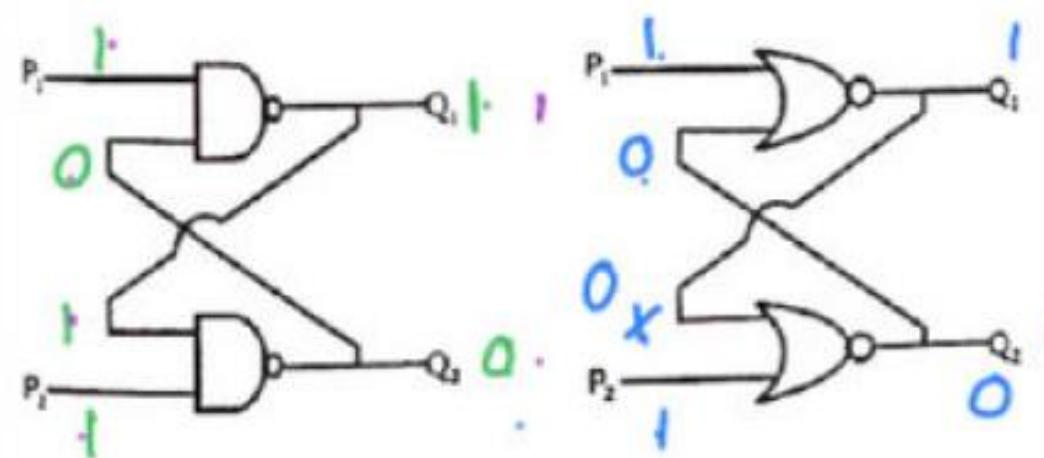
- (A)  $X = '1'$ ,  $Y = '1'$
- (B) Either  $X = '1'$ ,  $Y = '0'$  or  $X = '0'$ ,  $Y = '1'$  ✓
- (C) Either  $X = '1'$ ,  $Y = '1'$  or  $X = '0'$ ,  $Y = '0'$
- (D)  $X = '0'$ ,  $Y = '0'$

$$\begin{array}{l} X = 0 \\ Y = 1 \end{array}$$

or

$$\begin{array}{l} X = 1 \\ Y = 0 \end{array}$$

Refer to the NAND and NOR latches shown in the figure. The inputs ( $P_1, P_2$ ) for both the latches are first made (0, 1) and then, after a few seconds, made (1, 1). The corresponding stable outputs ( $Q_1, Q_2$ ) are



- (A) NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)
- (B) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (1, 0)
- ~~(C) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (0, 0)~~
- (D) NAND: first (1, 0) then (1, 1) NOR: first (0, 1) then (0, 1)

NAND

$$Q_1, Q_2 = 1 \text{ } 0 \rightarrow 1 \text{ } 0$$

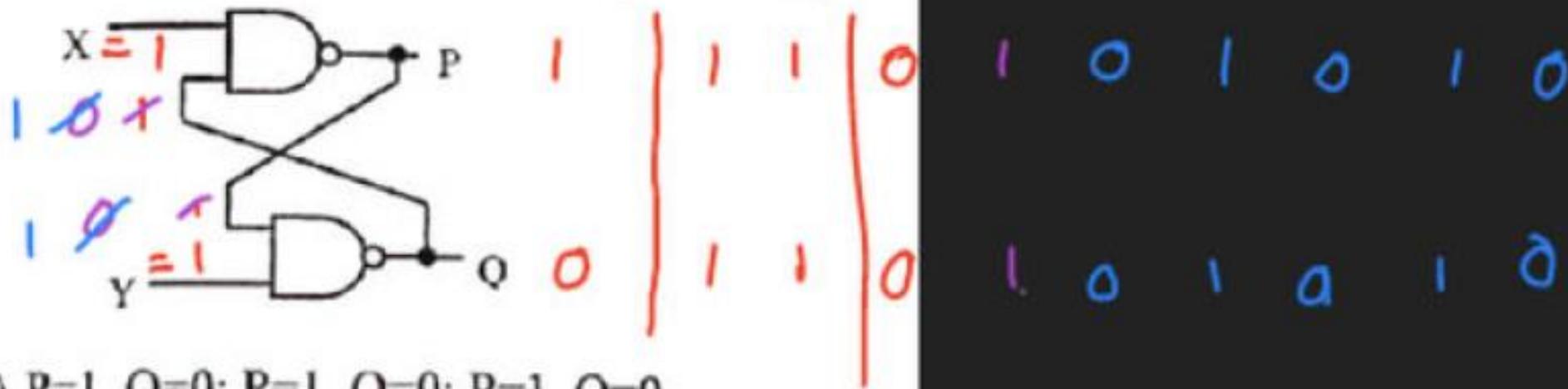
NOR

$$Q_1, Q_2 = 1 \text{ } 0 \rightarrow 0 \text{ } 0 \rightarrow 0 \text{ } 0$$

The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:

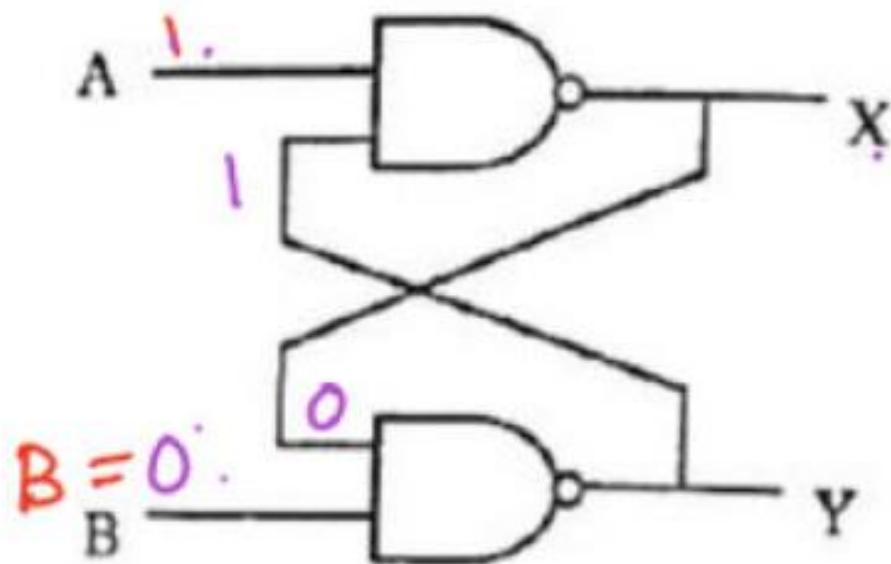
$$X = 0, Y = 1; \quad X = 0, Y = 0; \quad X = 1, Y = 1.$$

The corresponding stable P, Q outputs will be:



- (A) P=1, Q=0; P=1, Q=0; P=1, Q=0  
or P=0, Q=1
- (B) P=1, Q=0; P=0, Q=1; or P=0, Q=1;  
P=0, Q=1
- (C) P=1, Q=0; P=1, Q=1; P=1, Q=0  
or P=0, Q=1
- (D) P=1, Q=0; P=1, Q=1; P=1, Q=1 or P=0, Q=0

The given figure,  $A = 1$  and  $B = 1$ , the input  $B$  is now replaced by a sequence  $101010\dots$ .



The outputs  $x$  and  $y$  will be

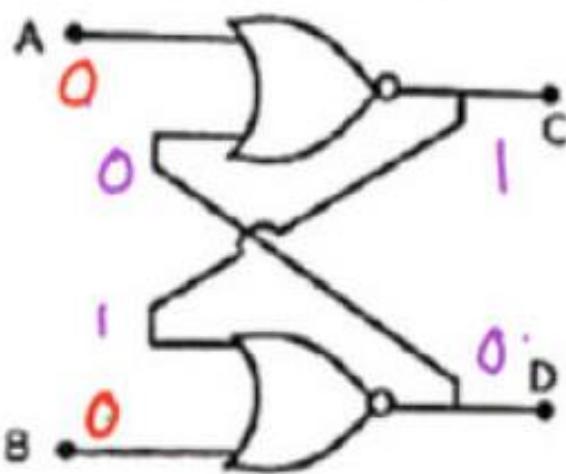
- (A) Fixed at  $0$  and  $1$ , respectively ✓
- (B)  $x = 1010 \dots$  while  $y = 0101 \dots$
- (C)  $x = 1010 \dots$  and  $y = 0101 \dots$
- (D) Fixed at  $1$  and  $0$ , respectively

<u>initial</u>				
$x = 0$	○	○	○	○
$y = 1$	1	1	1	1

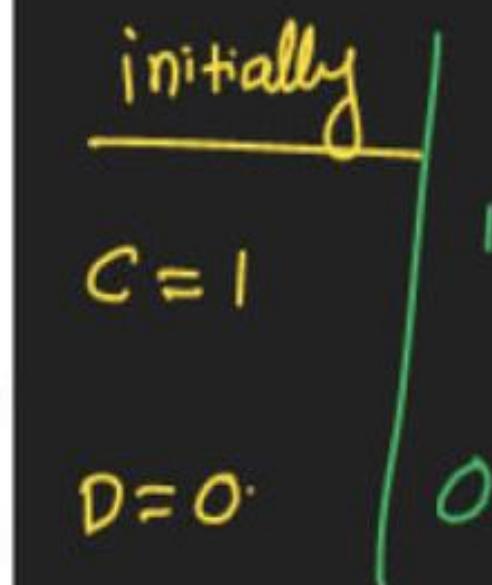
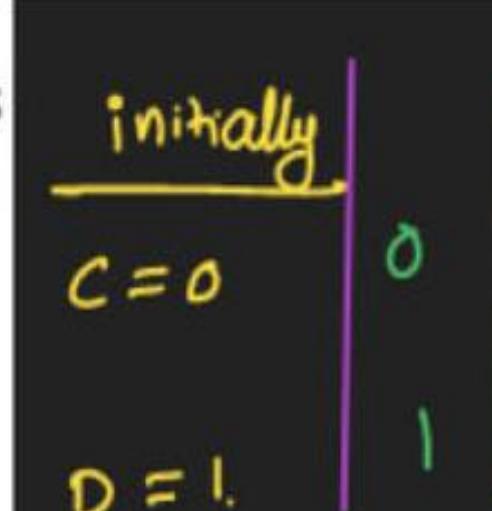
  

<u>initial</u>				
$x = 1$	1	1	0	00
$y = 0$	0	1	1	1

In the circuit shown in figure, when inputs  $A=B=0$ , the possible logic states of C and D are



- (A) ~~C = 0, D = 1 or C = 1, D = 0~~
- (B) C = 1, D = 1 or C = 0, D = 0
- (C) C = 1, D = 0
- (D) C = 0, D = 1



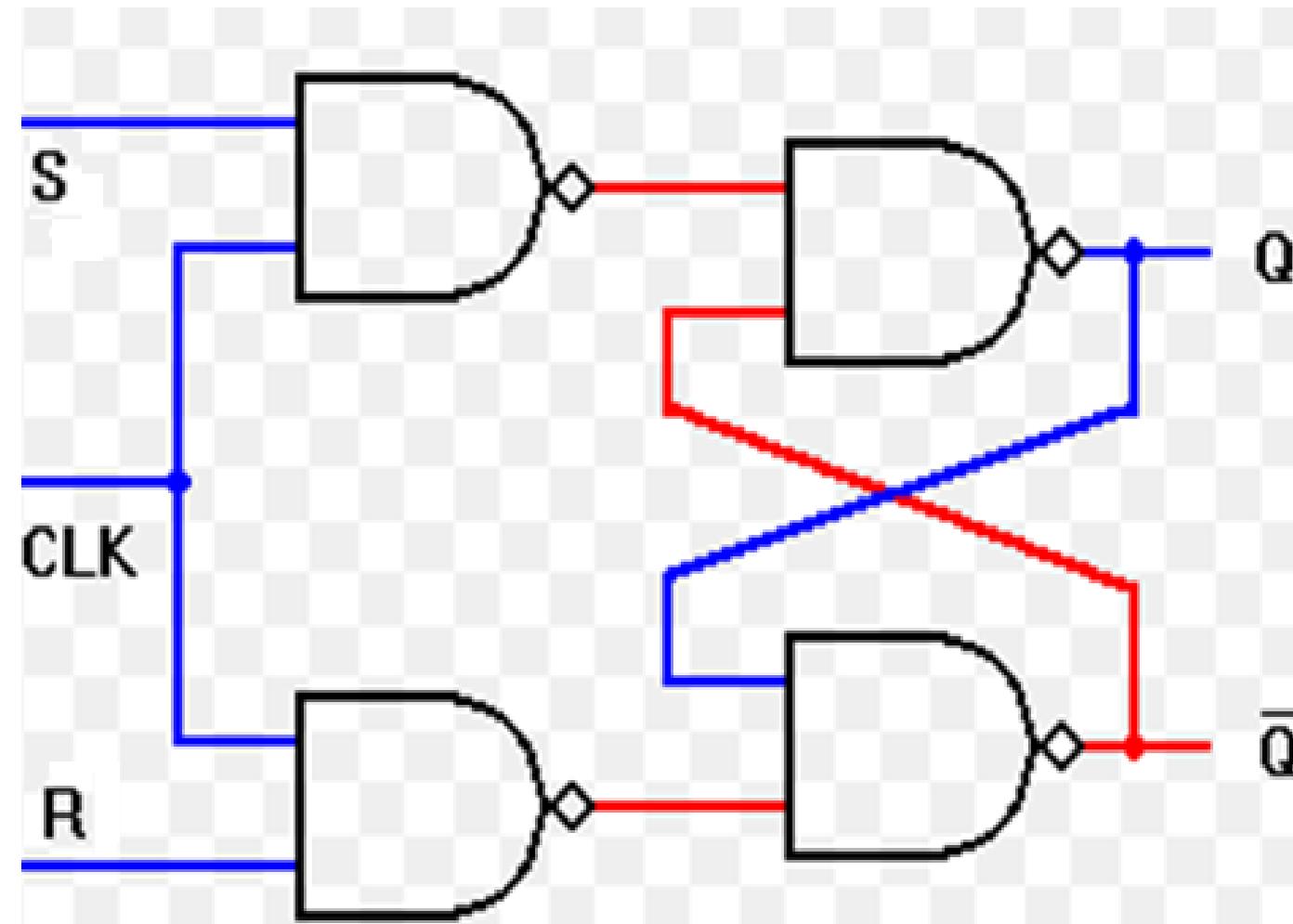
# FLIP FLOP

In a latch the output changes immediately in response to external input , so to have an additional control , we are introducing a signal called “ **CLOCK** “, whose purpose is same as Enable pin of Decoder.

**Latch + Clock = Flip Flop**

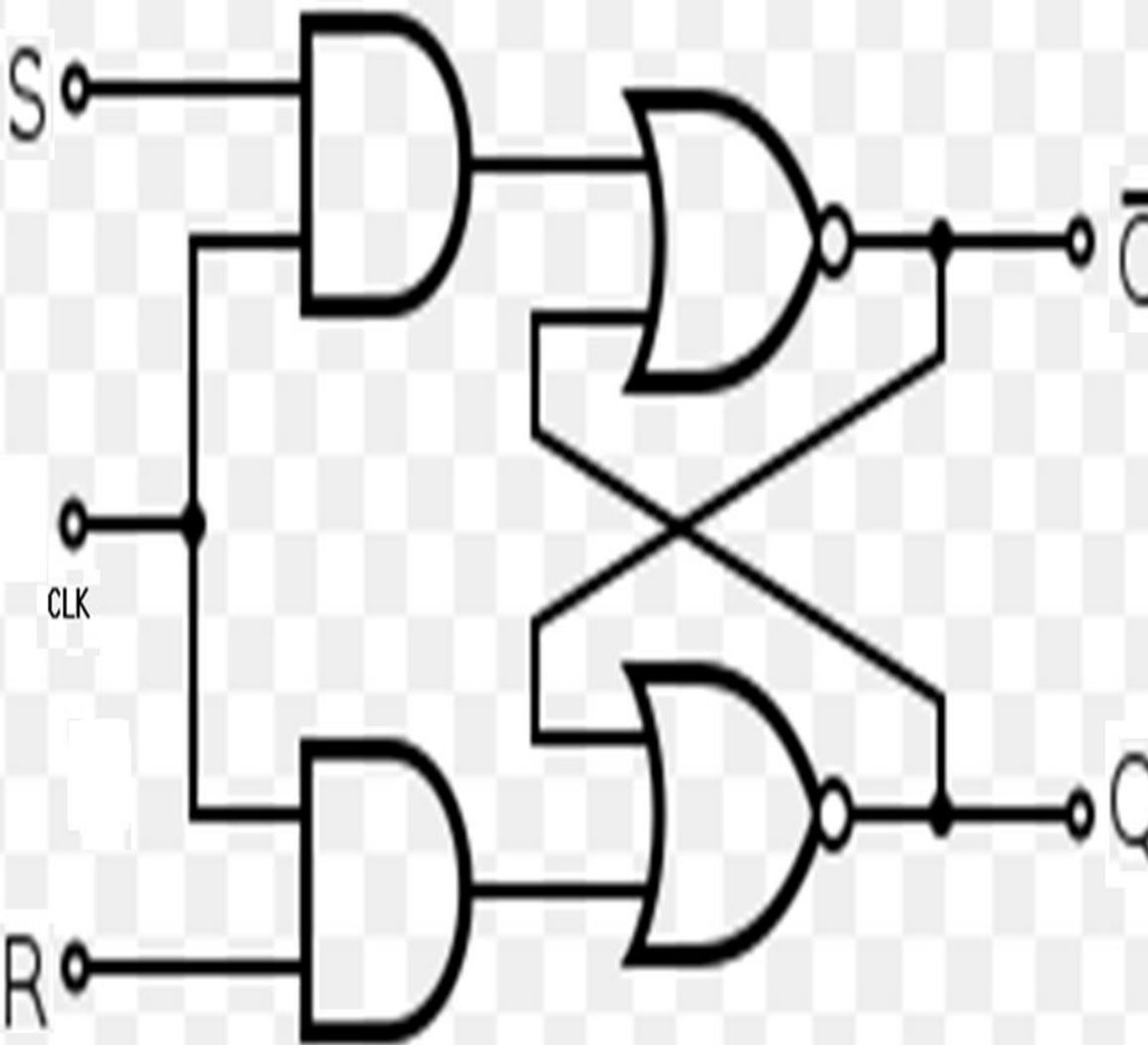
# SR Flip Flop

## 1. SR Flip Flop using NAND Latch



CLK	S	R	Q	Q+
0	*	*	*	Q
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	*
1	1	1	1	*

## 2. SR Flip Flop using NOR Latch

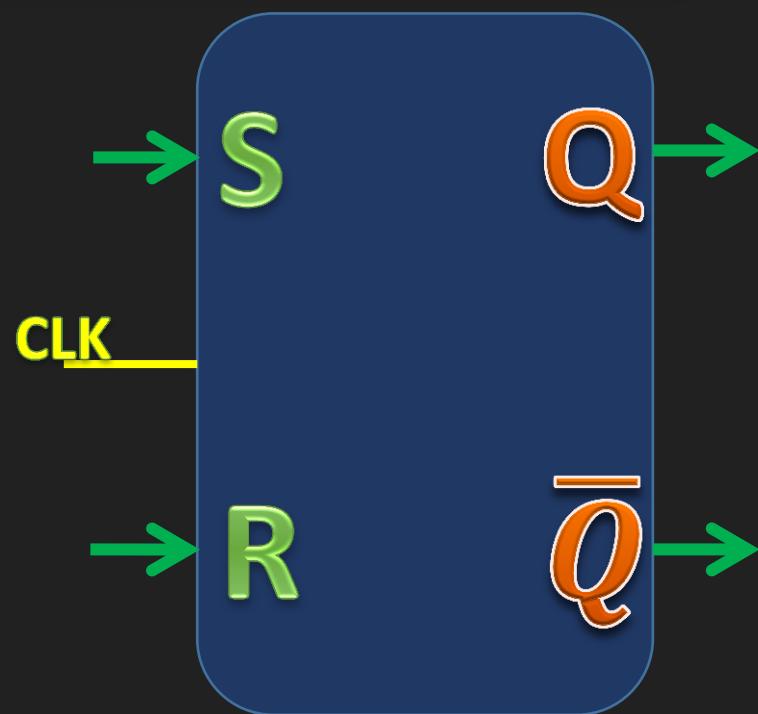


CLK	S	R	Q	Q+
0	x	x	x	Q
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	x
1	1	1	1	x

Latches are universally not unique and hence their truth tables are not unique .

Flip Flops are universally unique , and their truth tables are unique .

# S R Flip Flop



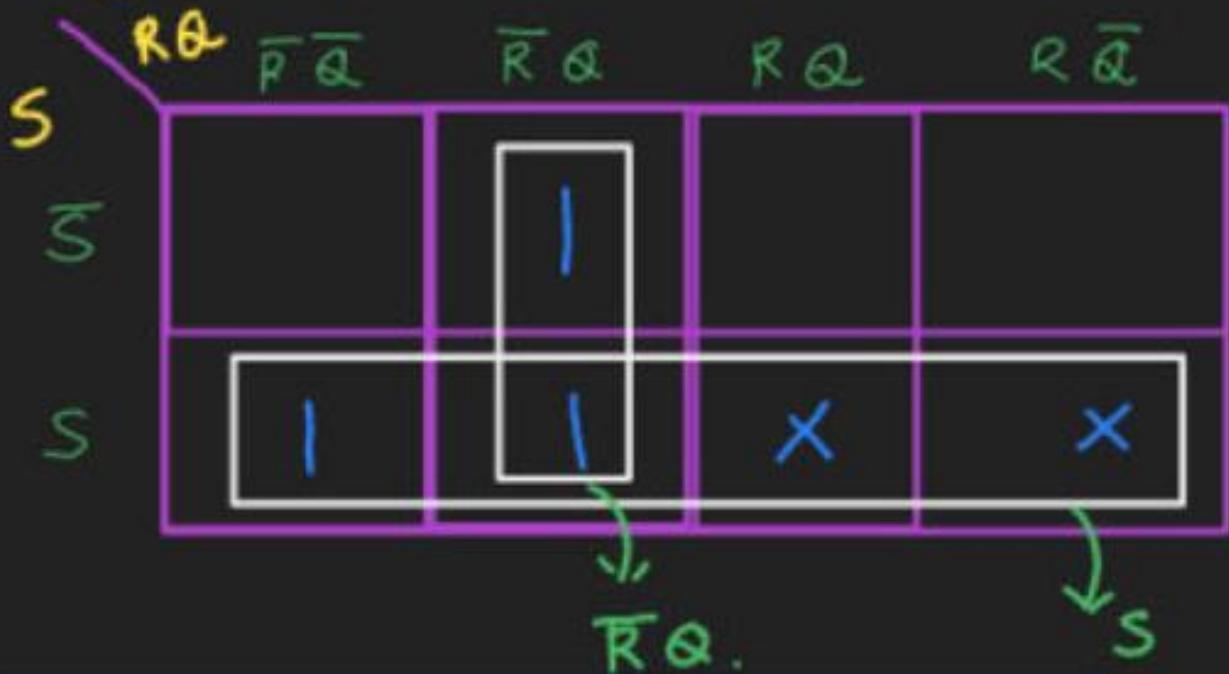
CLK	S	R	Q+	State
0	*	*	Q	Memory
1	0	0	Q	Memory
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	*	Invalid

## Characteristic table

CLK	S	R	Q	Q+
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	x
1	1	1	1	x

## Characteristic Equation ✓

$$\alpha^+(S, R, Q) = \sum m(1, 4, 5) + d(6, 7)$$



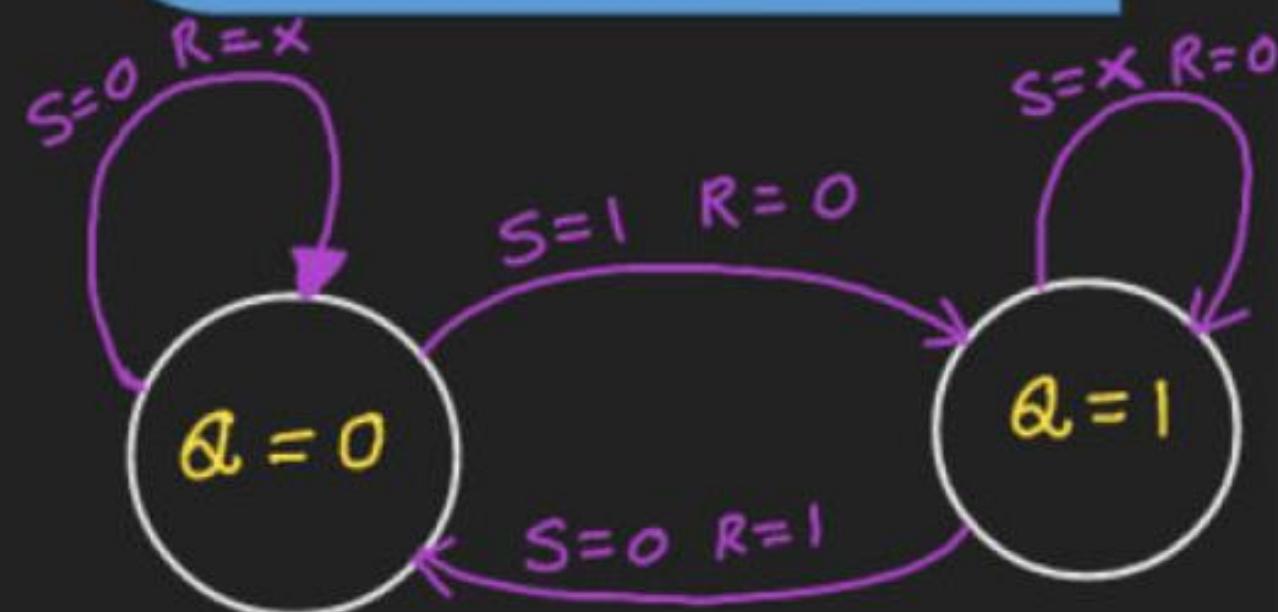
$$\alpha^+(S, R, Q) = S + \bar{R} \alpha$$

not valid, if  $S = R = 1$ .

## Excitation table

$Q$	$Q^+$	$S$	$R$
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

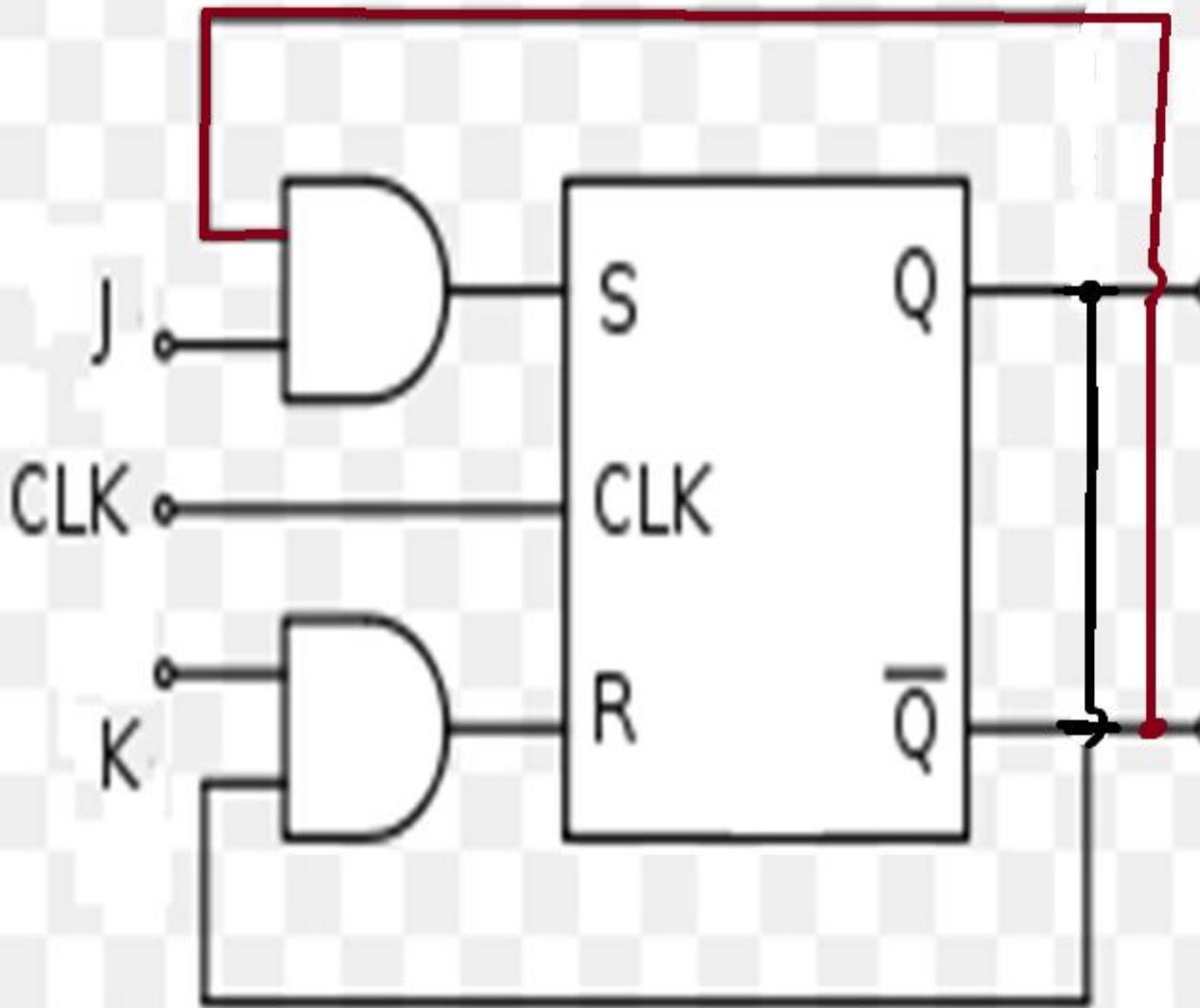
## State Diagram



# Drawbacks

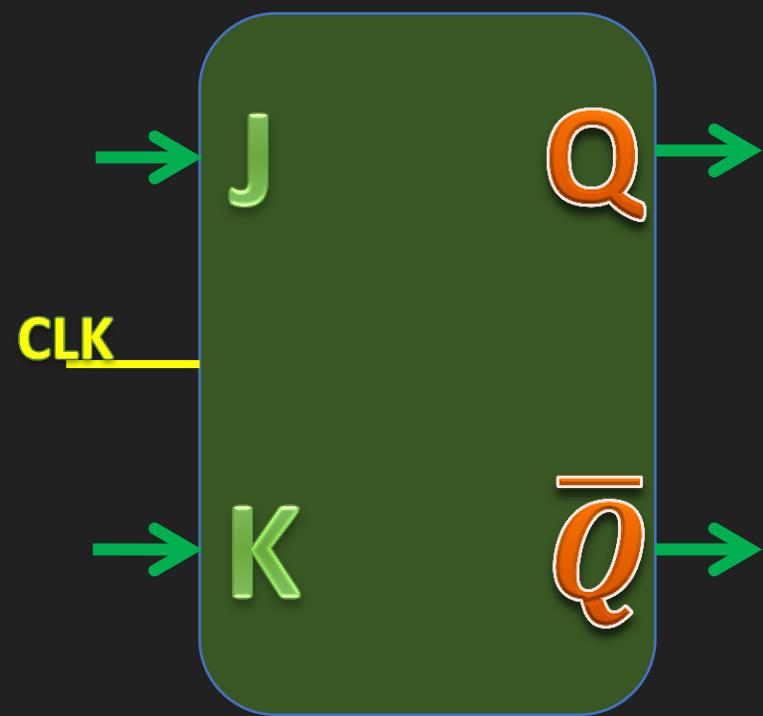
Because of presence of invalid state there is a restriction on the sequence of the applied input ,since it leads to **CRITICAL RACE**, which is undesirable

# J K Flip Flop



CLK	J	K	Q+
0	*	*	Q
1	0	0	Q
1	0	1	0
1	1	0	1
1	1	1	Q̄

# J K Flip Flop



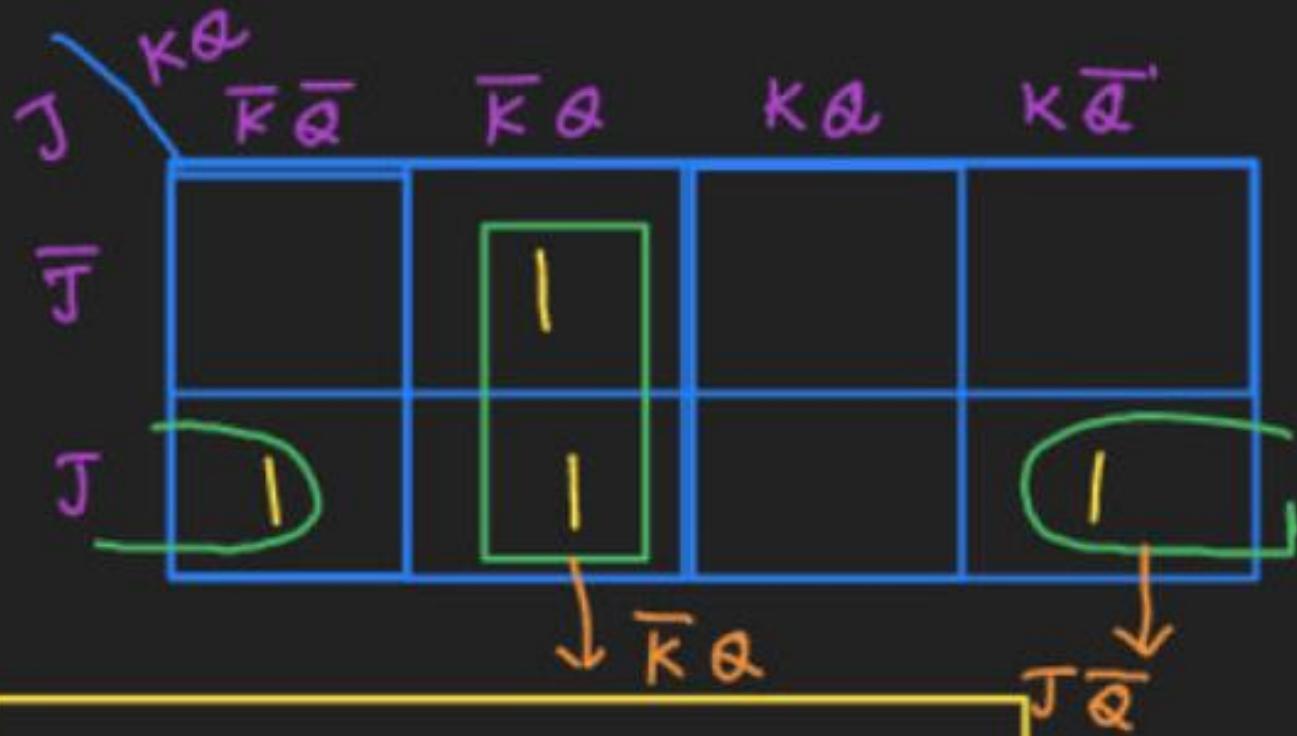
CLK	J	K	Q+	State
0	*	*	Q	Memory
1	0	0	Q	Memory
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	*	Invalid

## Characteristic table

CLK	J	K	Q	Q+
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

## Characteristic Equation

$$Q^+(J, K, Q) = \sum m(1, 4, 5, 6)$$

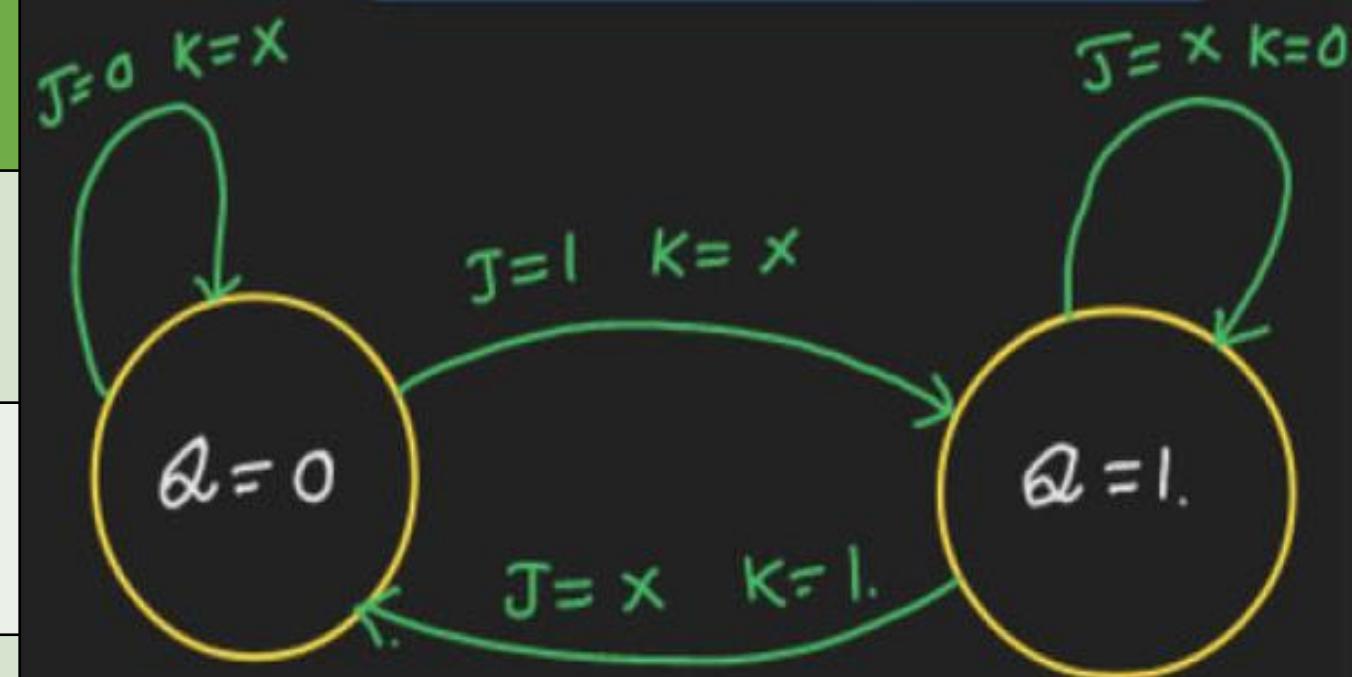


$$Q^+(J, K, Q) = J\bar{Q} + \bar{K}Q$$

# Excitation table

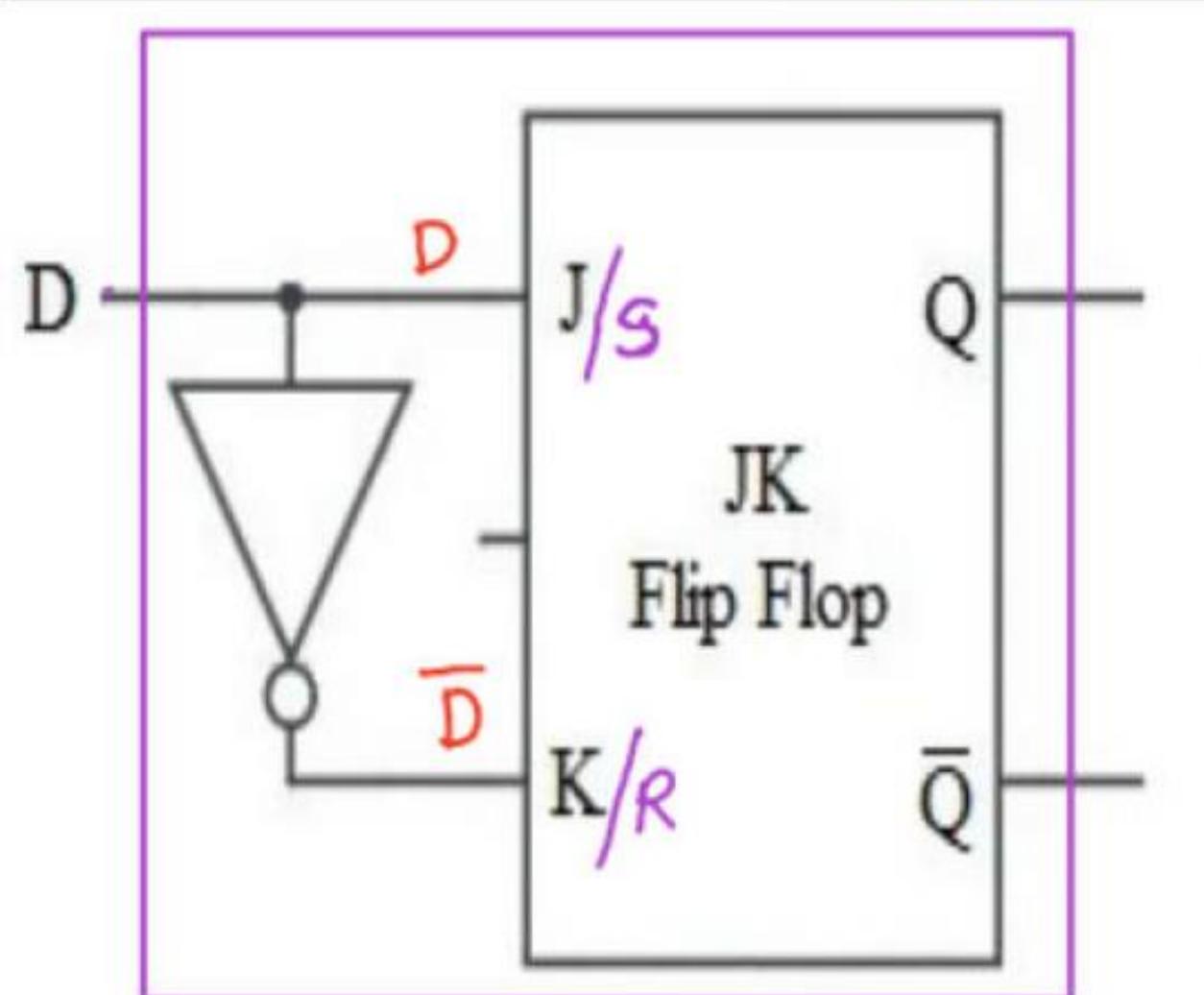
Q	Q+	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

# State Diagram



# D Flip Flop ✓

Data FF  
Delay FF.  
Transparent FF.



CLK      D      Q+

O	X	Q.
I	O	O
I	I	I

$$\begin{aligned}Q^+ &= J\bar{Q} + \bar{K}Q \\&= D\bar{Q} + \bar{D}Q = D\end{aligned}$$

Characteristic table

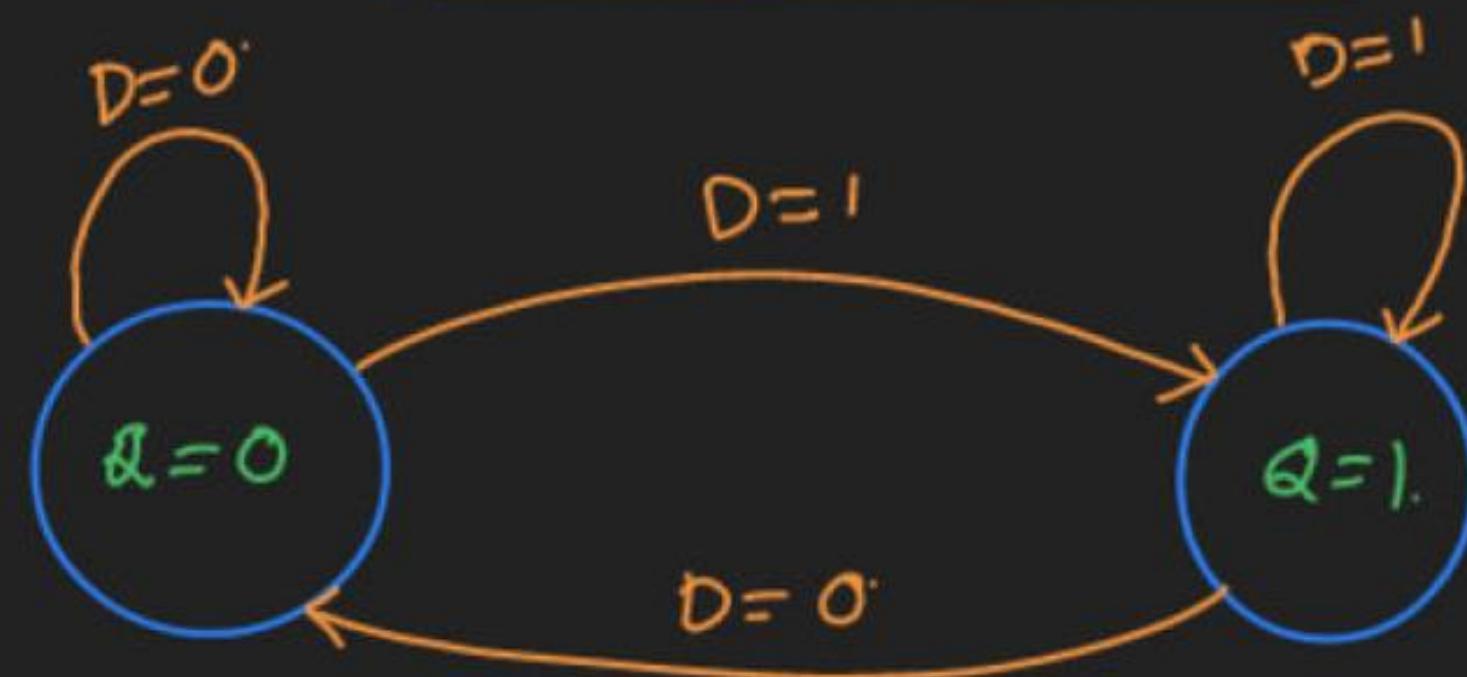
Characteristic Equation

CLK	D	Q	Q+	
0	x	x	Q	$Q^+ = D$
1	0	0	0	
1	0	1	0	
1	1	Q	1	
1	1	1	1	

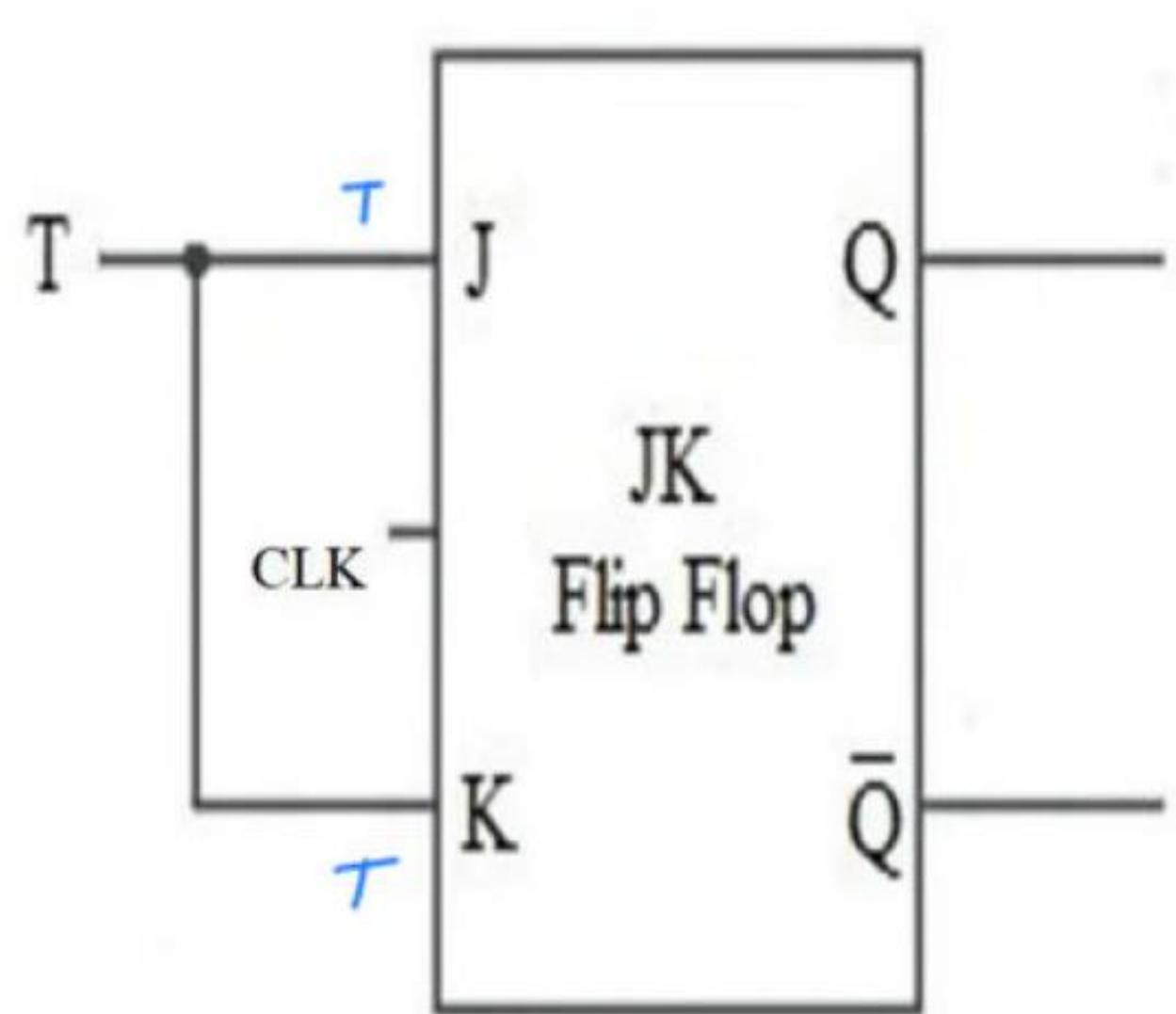
## Excitation table

Q	Q+	D
0	0	0
0	!	1
1	0	0
1	1	1

## State Diagram



# T Flip Flop



CLK      T      Q+

0	X	Q
1	0	Q
1	1	$\bar{Q}$

$$\begin{aligned}Q^+ &= J\bar{Q} + \bar{K}Q \\&= T\bar{Q} + \bar{T}Q = T \oplus Q\end{aligned}$$

## Characteristic table

## Characteristic Equation

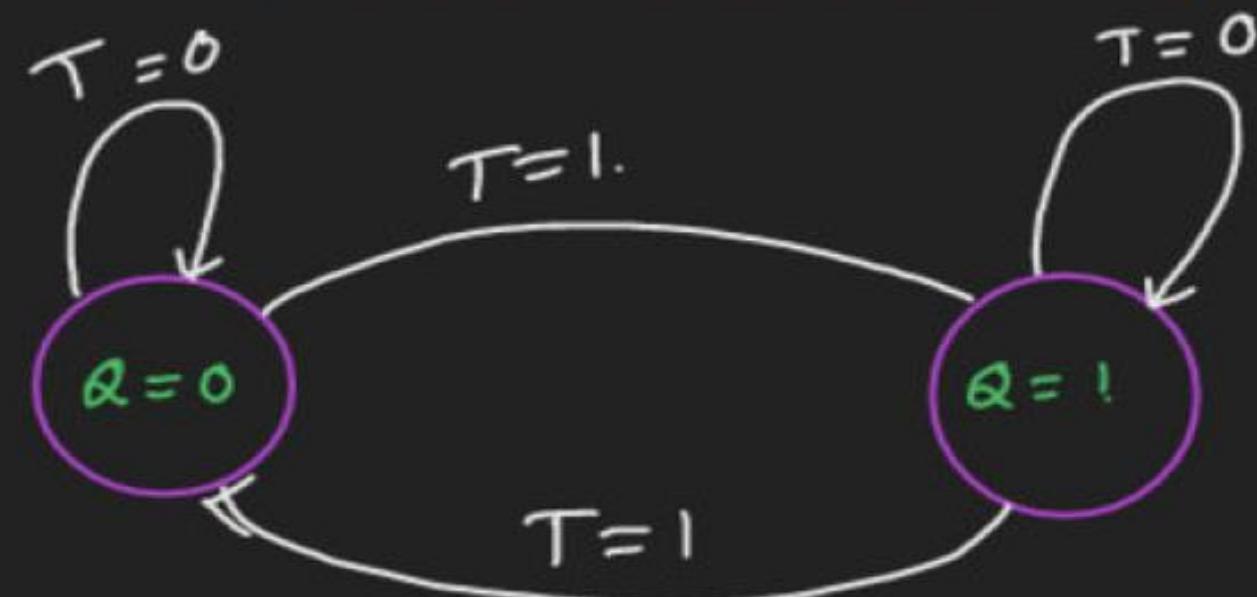
CLK	T	Q	Q+
0	x	x	Q
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

$$Q^+ = T \oplus Q$$

## Excitation table

$Q$	$Q+$	$T$
0	0	0
0	1	1
1	0	1
1	1	0

## State Diagram



### SR FF

$$Q^+ = S + \bar{R} Q$$

S	R	$Q^+$
0	0	Q
0	1	0
1	0	1
1	1	X

Q	$Q^+$	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

### JK FF

$$Q^+ = J\bar{Q} + \bar{K}Q$$

J	K	$Q^+$
0	0	Q
0	1	0
1	0	1
1	1	X

Q	$Q^+$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

### D- FF

$$Q^+ = D$$

D	$Q^+$
0	0
0	1
1	0
1	1

Q	$Q^+$	D
0	0	0
0	1	1
1	0	0
1	1	1

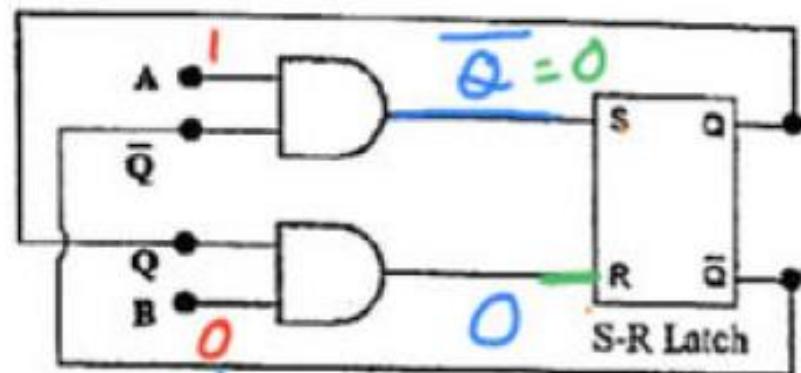
### T- FF

$$Q^+ = T \oplus Q$$

T	$Q^+$
0	Q
1	X

Q	$Q^+$	T
0	0	0
0	1	1
1	0	1
1	1	0

The two inputs A and B are connected to an R-S latch via two AND gates as shown in the figure.



If  $A = 1$  and  $B = 0$ , the output  $Q\bar{Q}$  is

- (A) 00      ~~(B) 10~~      (C) 01      (D) 11

$Q$	$\bar{Q}$	
0	1	<u>initial</u>
1	0	

$Q$	$\bar{Q}$	
1	0	<u>initial</u>
1	0	

A sequential circuit using D FlipFlop and logic gates is shown in the figure, where X and Y are the inputs and Z is the output. The circuit is

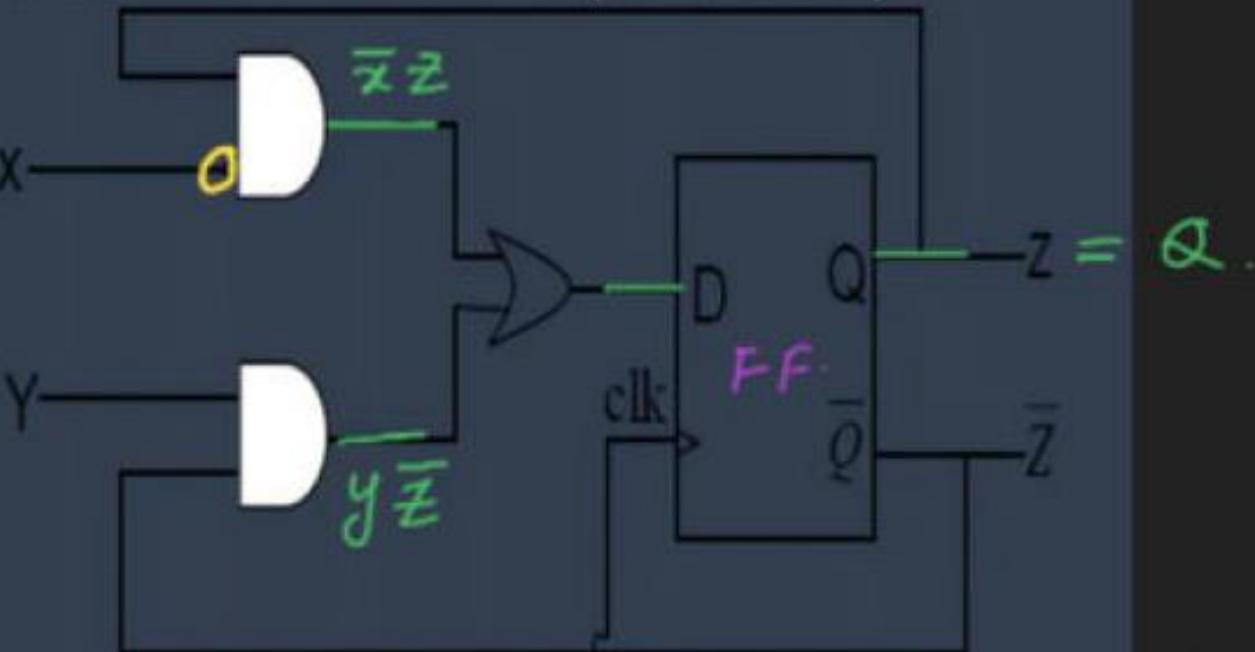
(GATE-2000)

(a) S-R FlipFlop with inputs X= R and Y=S

(b) S-R FlipFlop with inputs X= S and Y=R

(c) J-K FlipFlop with inputs X= J and Y=K

(d) J-K FlipFlop with inputs X= K and Y=J



$$D = \bar{x}z + y\bar{z}$$

$$Q^+ = D$$

$$Q^+ = \bar{x}z + y\bar{z}$$

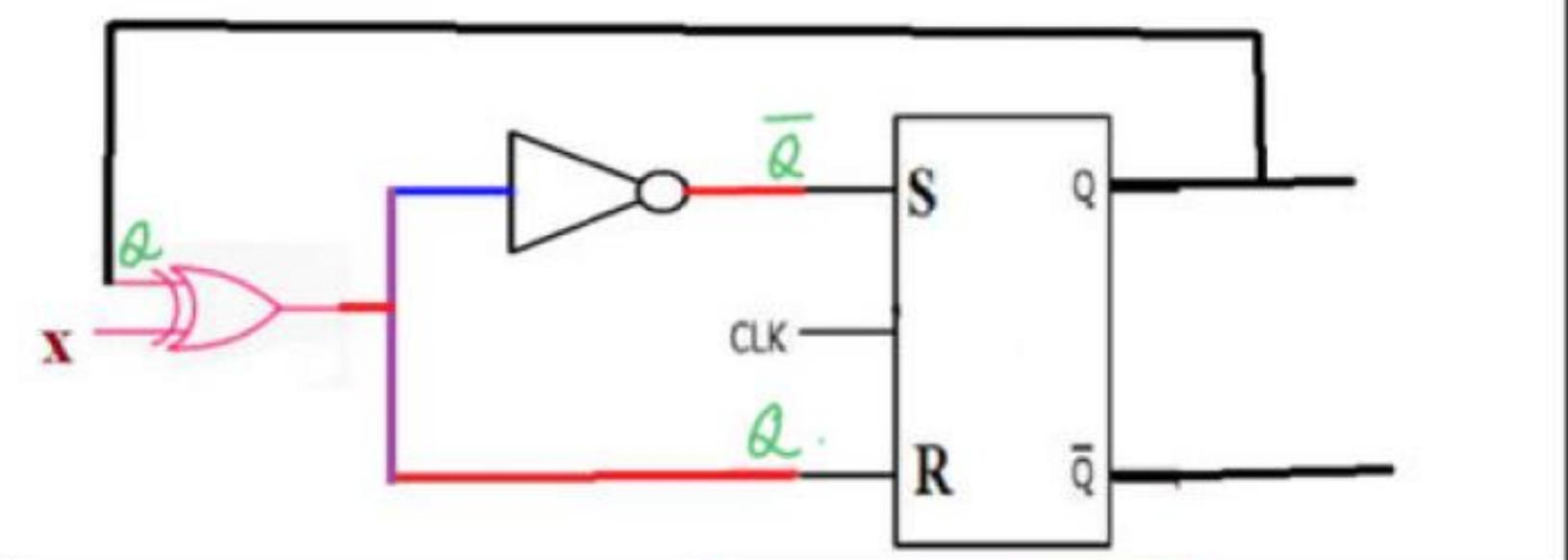
$$Q^+ = \bar{x}Q + y\bar{Q} \quad (1)$$

$$Q^+ = S + \bar{R}Q \quad (2)$$

$$Q^+ = \underline{J}\bar{Q} + \bar{K}Q \quad (2)$$

$$J = y \quad K = x$$

write the truth table , state table and excitation table



$x$	$Q^+$
0	$\bar{Q}$
1	$Q$

$x$	$Q$	$Q^+$
0	0	1
0	1	0
1	0	0
1	1	1

$Q$	$Q^+$	$x$
0	0	1
0	1	0
1	0	0
1	1	1

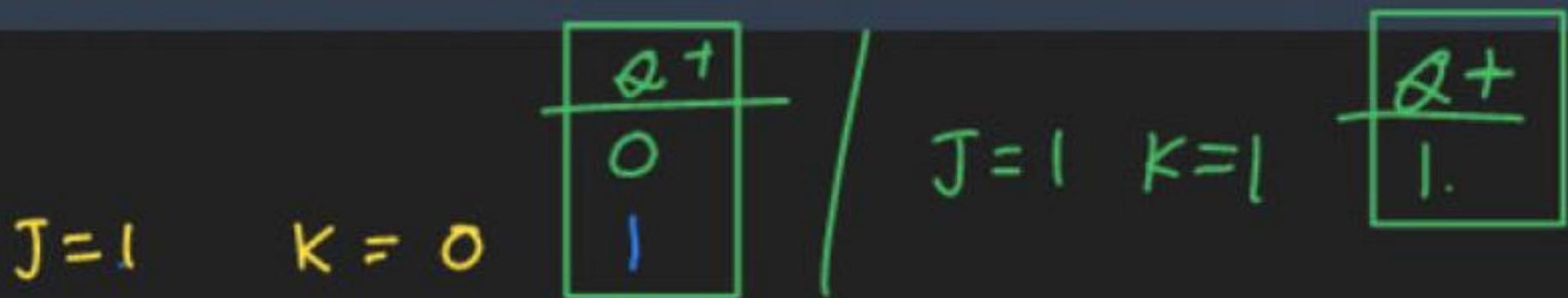
$$\begin{aligned}
 Q^+ &= S + \bar{R} Q \\
 &= (\bar{x} \odot Q) + (\bar{x} \oplus Q) Q \\
 &= (\bar{x} \odot Q) + (\bar{x} \odot Q) Q \\
 &= (\bar{x} \odot Q) [1 + Q]
 \end{aligned}$$

$$Q^+ = x \odot Q$$

The present output  $Q_n$  of an edge triggered JK flipflop is logic 0. If  $J=1$ , then  $Q_{n+1}$  (GATE-2005)

- (a) cannot be determined  
(c) will be logic 1 ✓

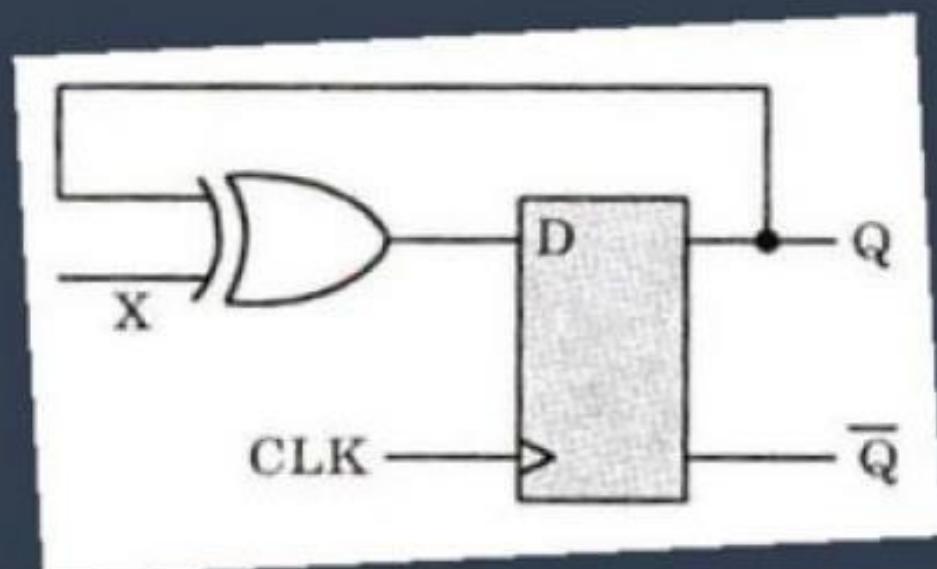
- (b) will be logic 0  
(d) will race around



The digital circuit shown in the figure works as a

(GATE - EE - 2005)

- (a) JK flip-flop
- (b) Clocked RS flip-flop
- (c) T flip-flop ✓
- (d) Ring counter



$$D = Q \oplus \bar{Q}$$

$$Q^+ = \bar{Q} \oplus Q$$

$$\underline{Q^+ = \bar{Q} \oplus Q}$$

In a JK flip-flop, the output  $Q_n$  is 1 and it does not change when a clock pulse applied.  
The possible combination of  $J_n$  and  $K_n$  could be (x denotes don't care).

(IES-1992)

- (a) x and 0 ✓      (b) x and 1  
(c) 0 and x      (d) 1 and x

①

$Q = 1$  ✓      ①  $\downarrow$   $J=1 \quad K=0$        $Q^+ = 1$   
②  $J=0 \quad K=0$        $Q^+ = 1.$

<u><math>J</math></u>	<u><math>K</math></u> :	
	0	1
0	0	1
		0

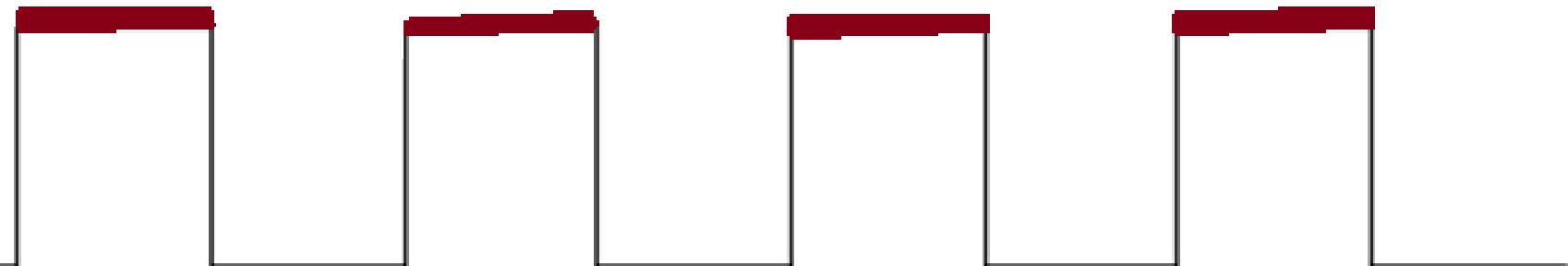
$J = X \quad K = 0$

# Triggering

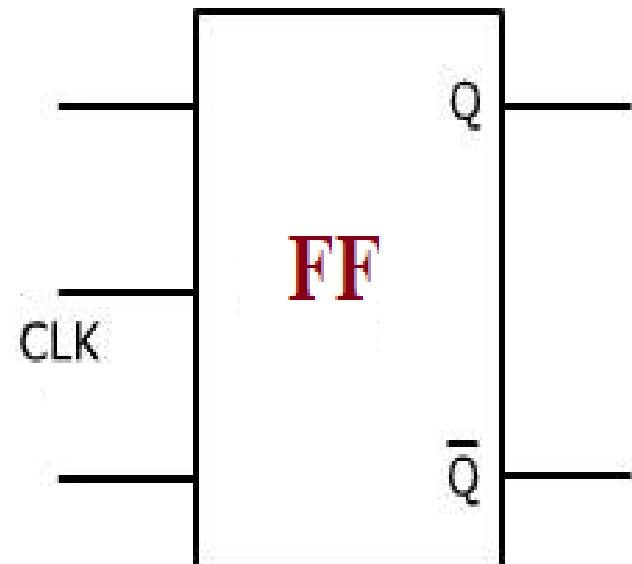
- Sequential circuits are dependant on clock pulses applies to their inputs.
- The result of flip-flop responding to a clock input is called **clock pulse triggering**, of which there are four types. Each type responds to a clock pulse in one of four ways :-
  1. High level triggering
  2. Low level triggering
  3. Positive edge triggering
  4. Negative edge triggering

# Types of Triggering

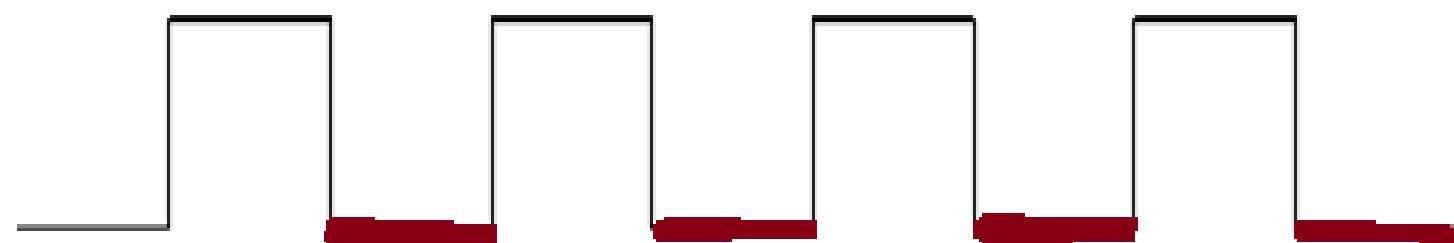
## 1. High (Positive) Level Triggering



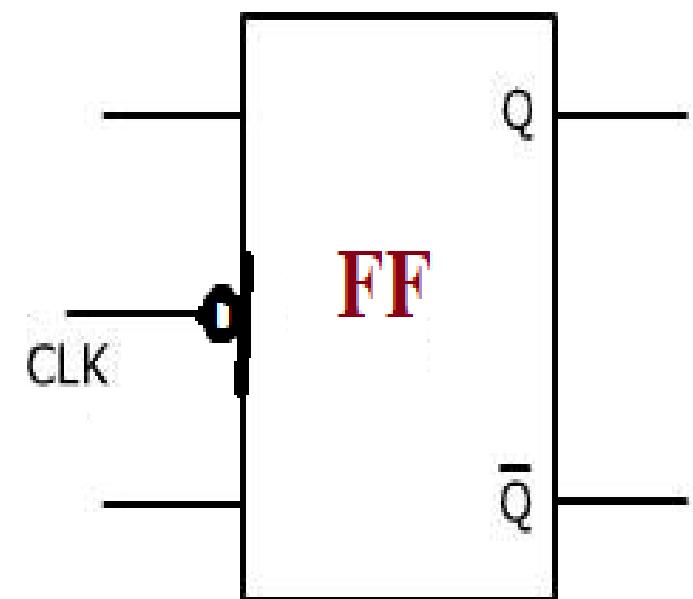
Positive level triggering



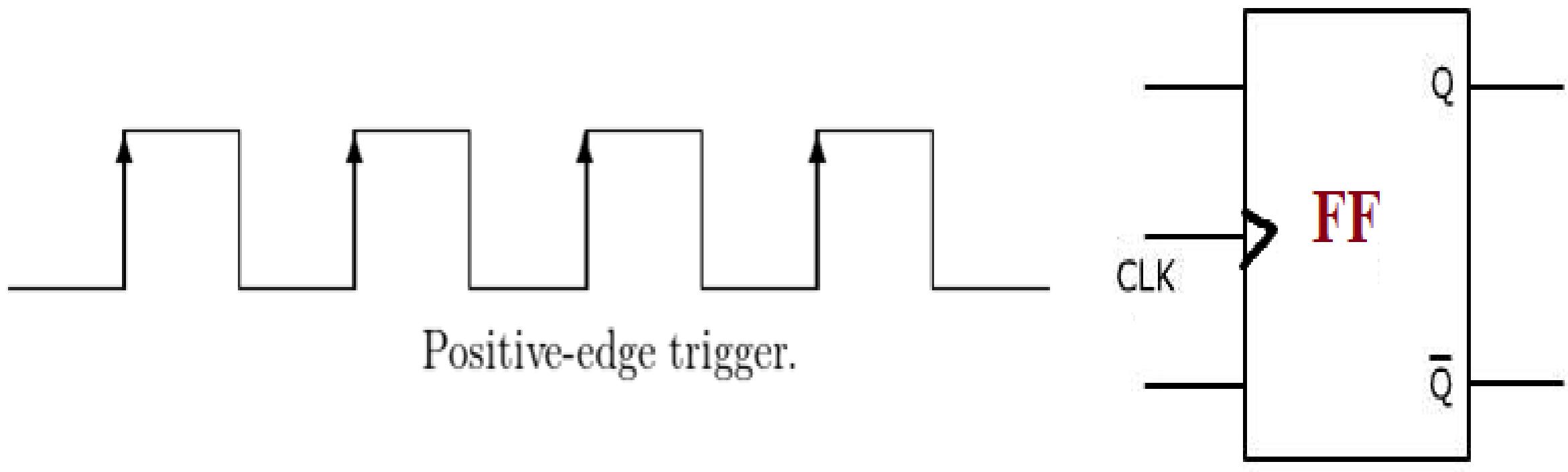
## 2. Low (Negative) Level Triggering



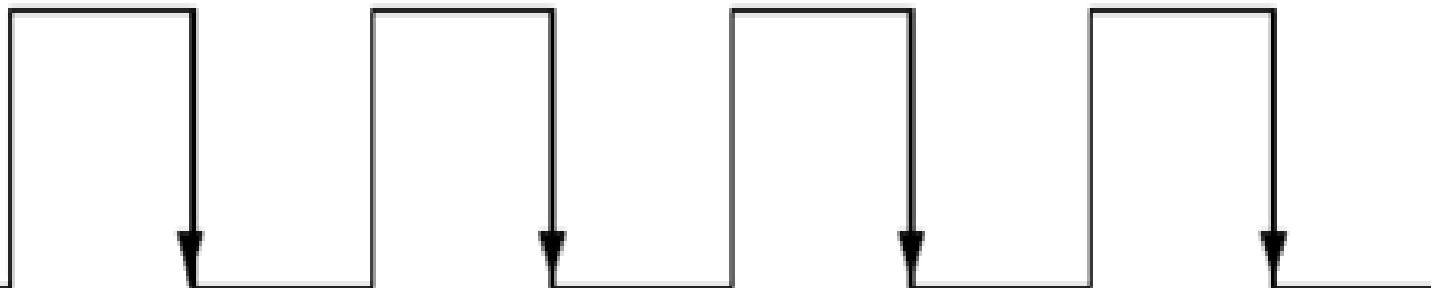
Negative level triggering



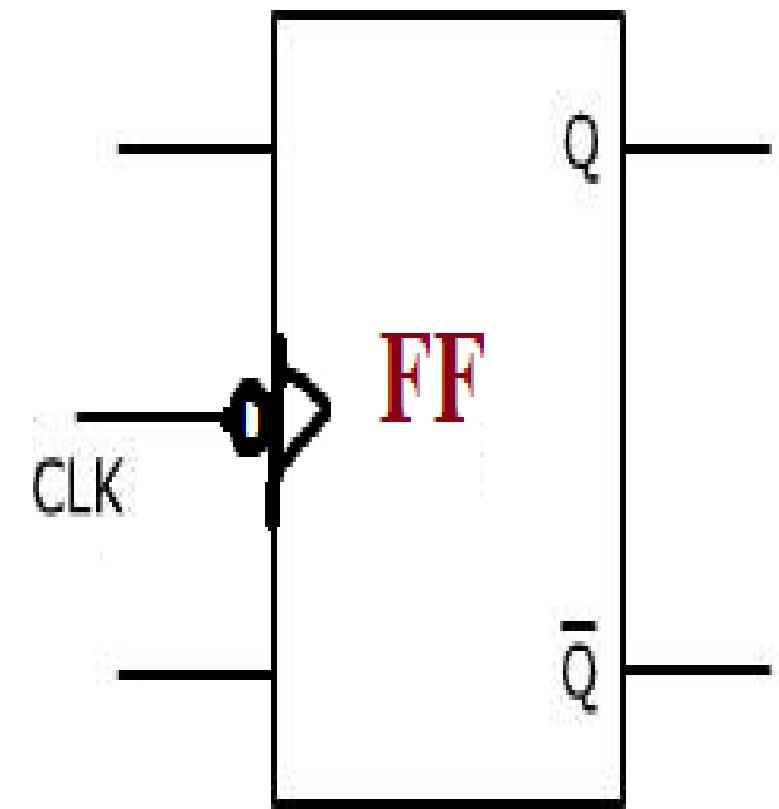
# 3. Positive Edge trigger



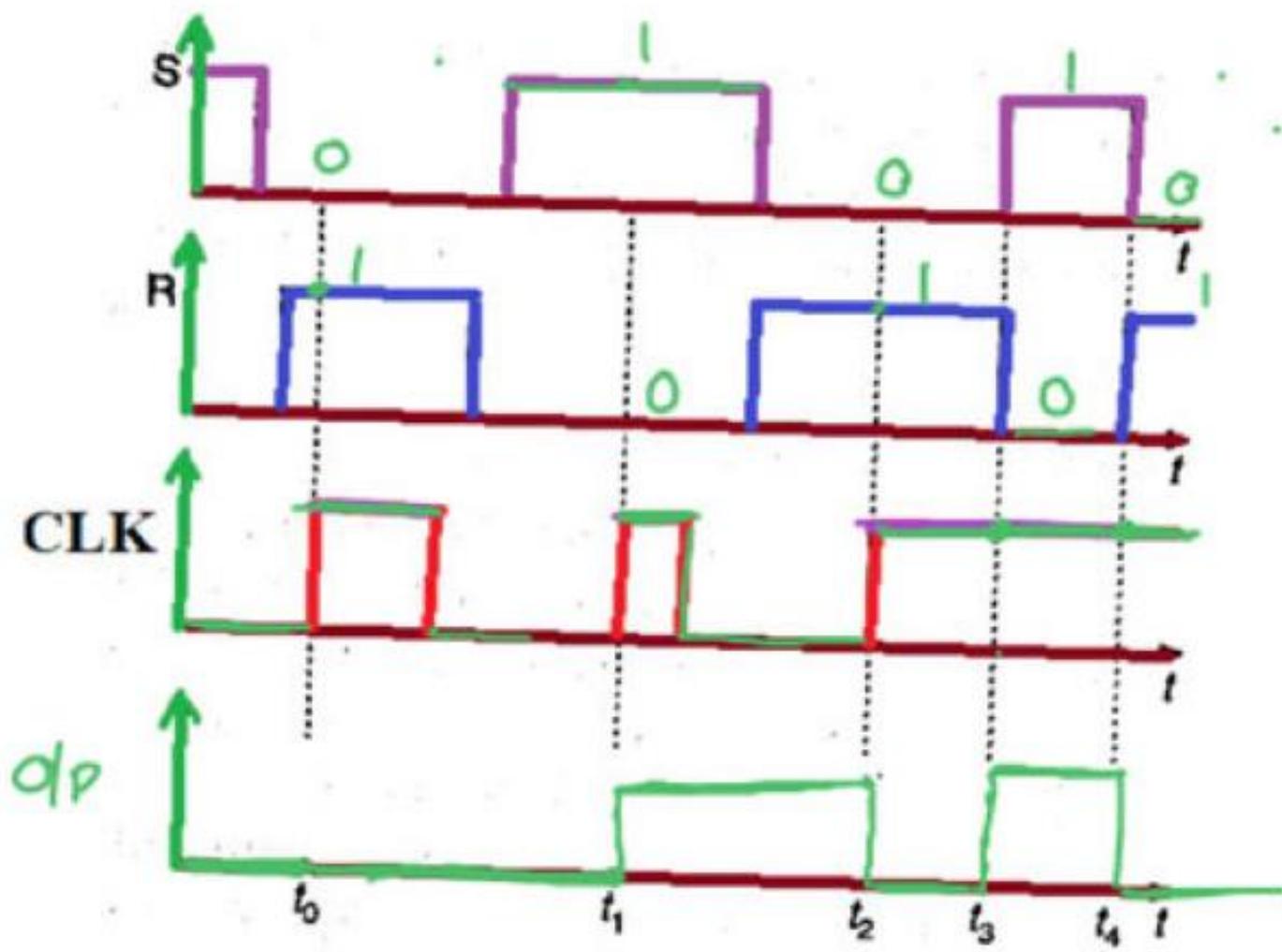
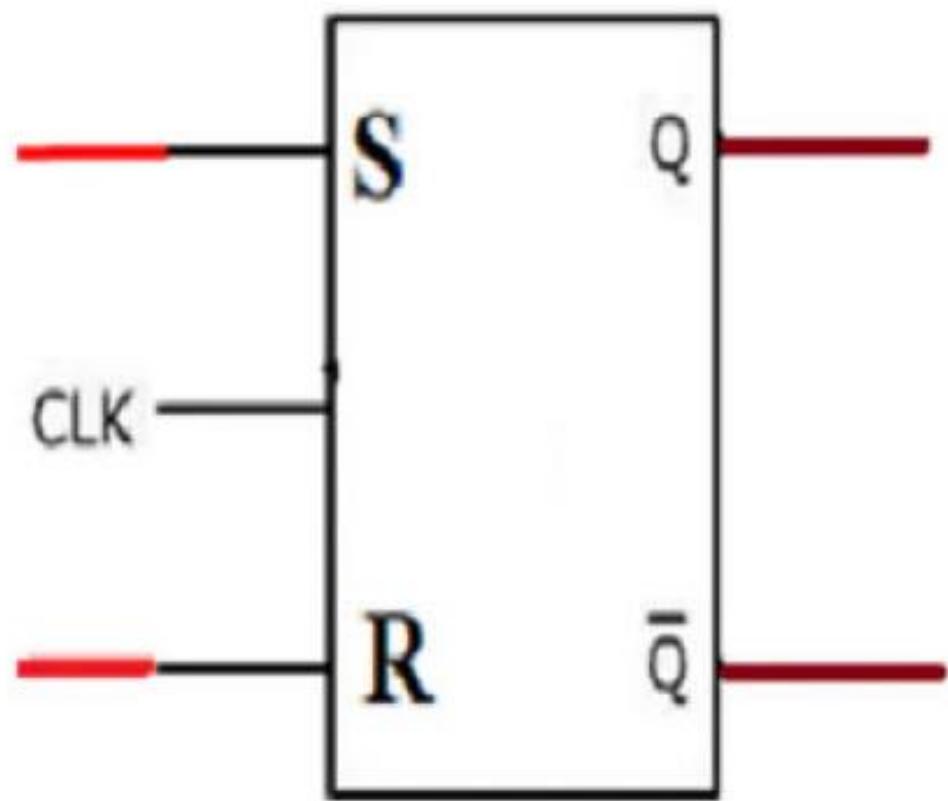
# 4. Negative Edge trigger



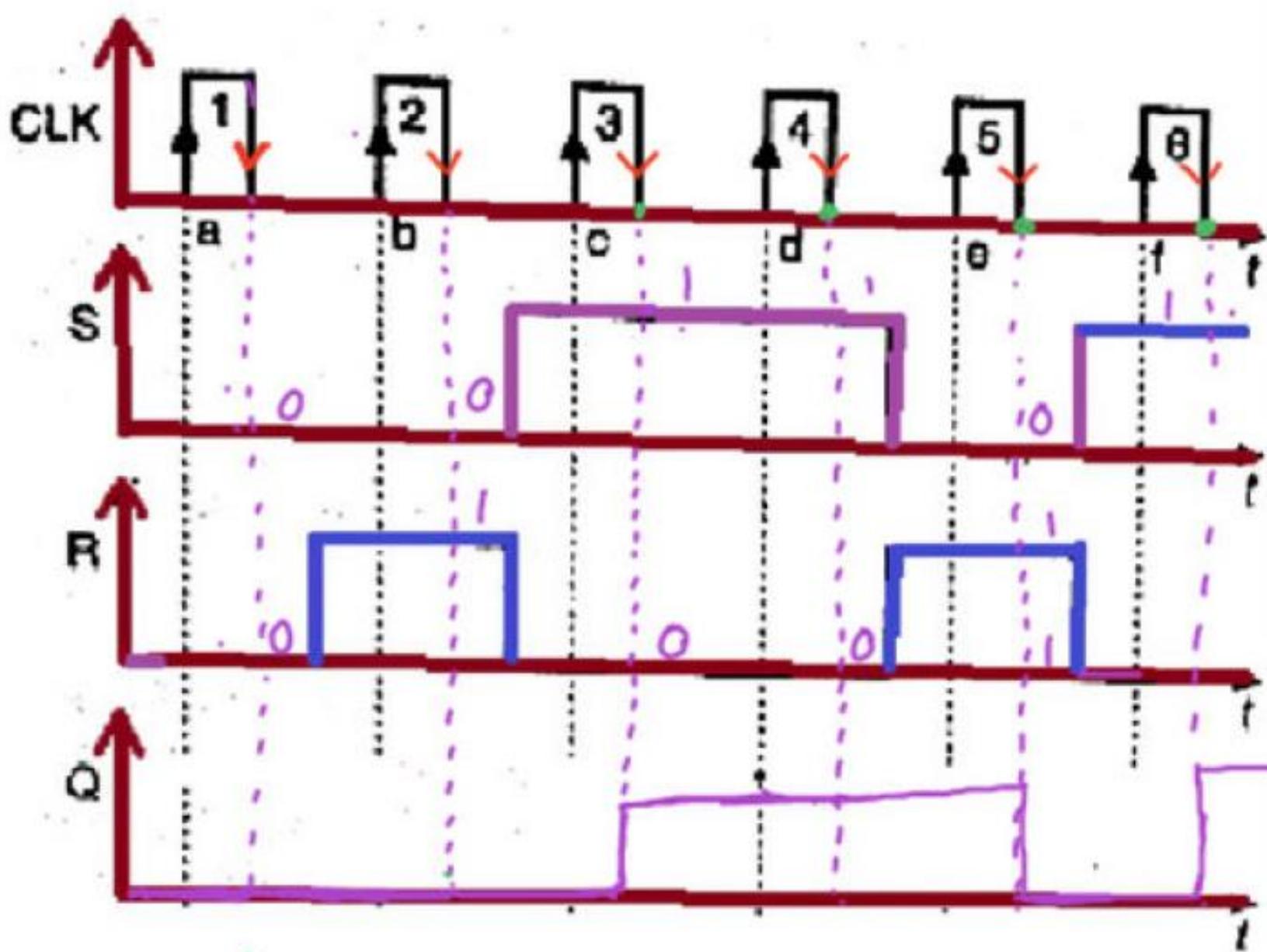
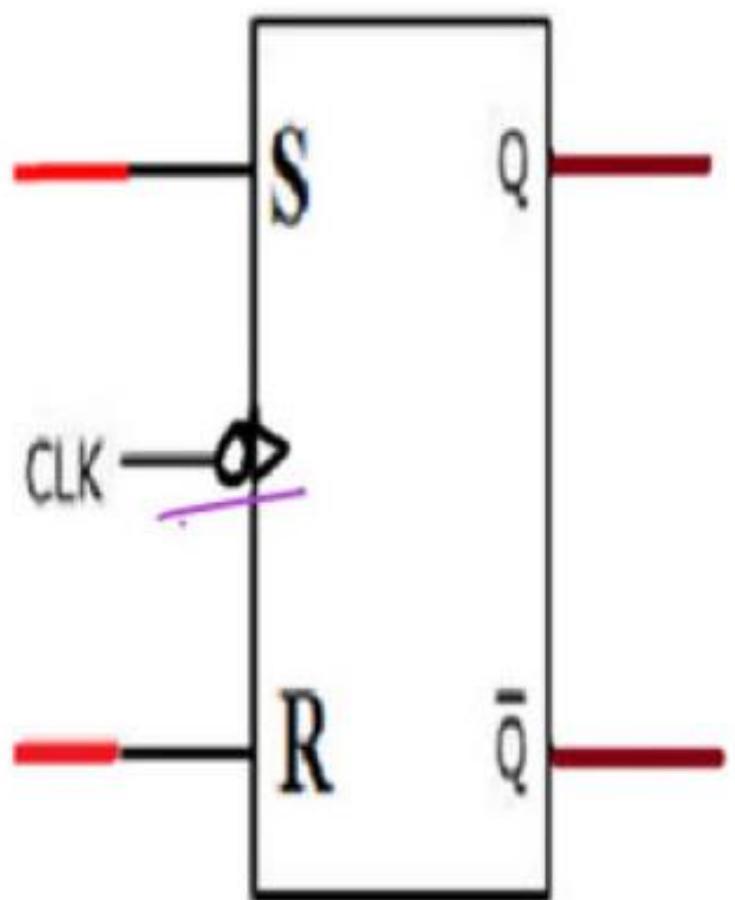
Negative-edge trigger.



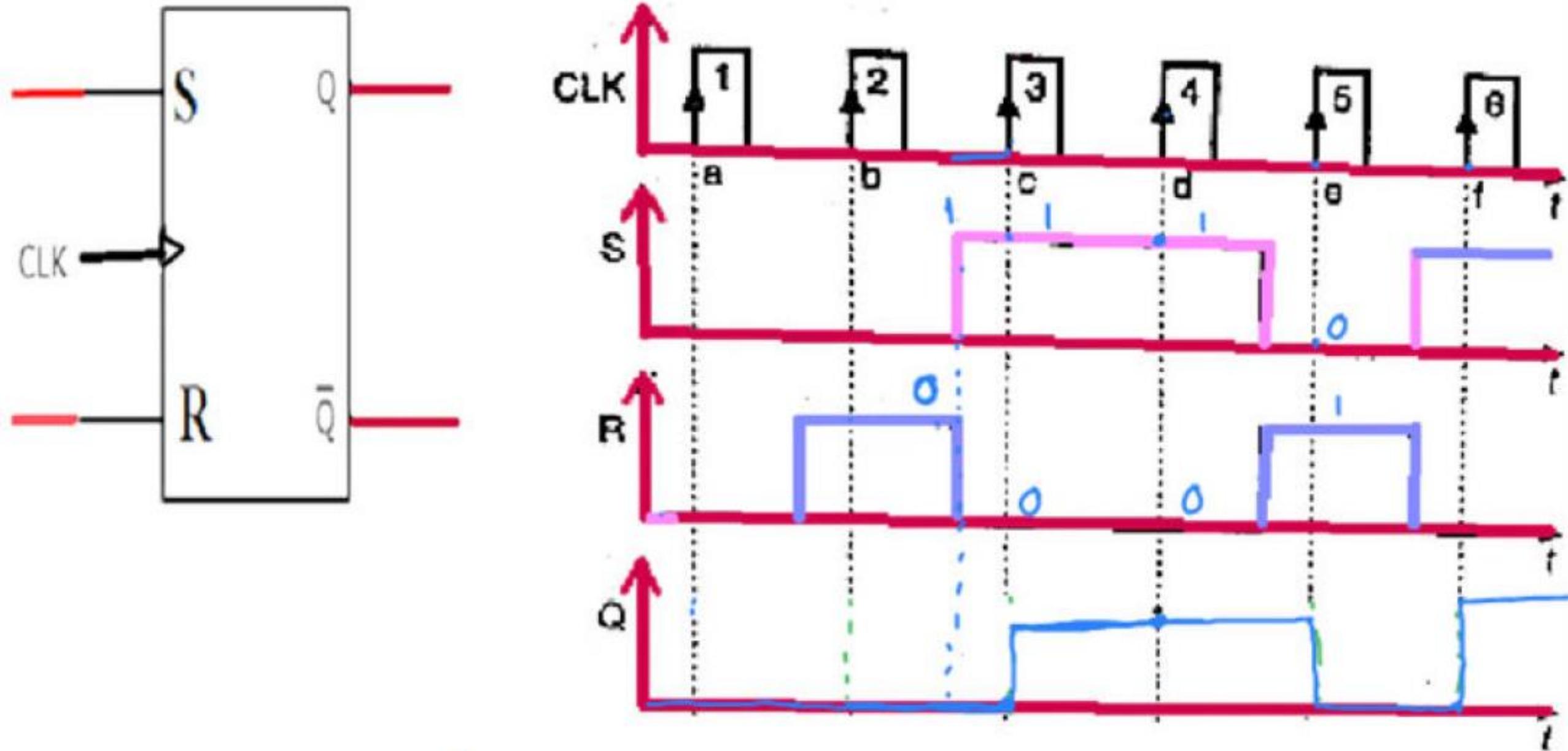
Draw the output waveform



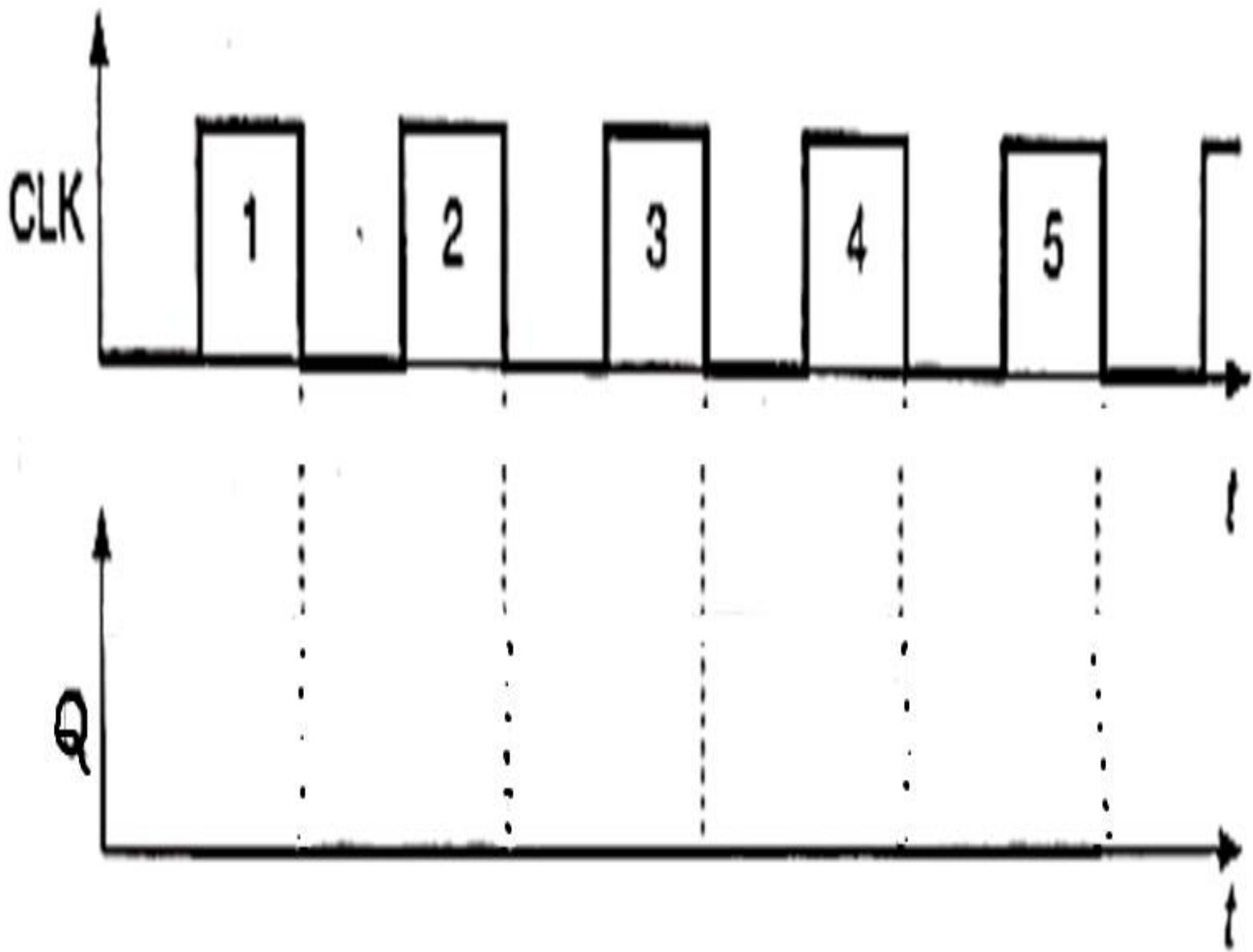
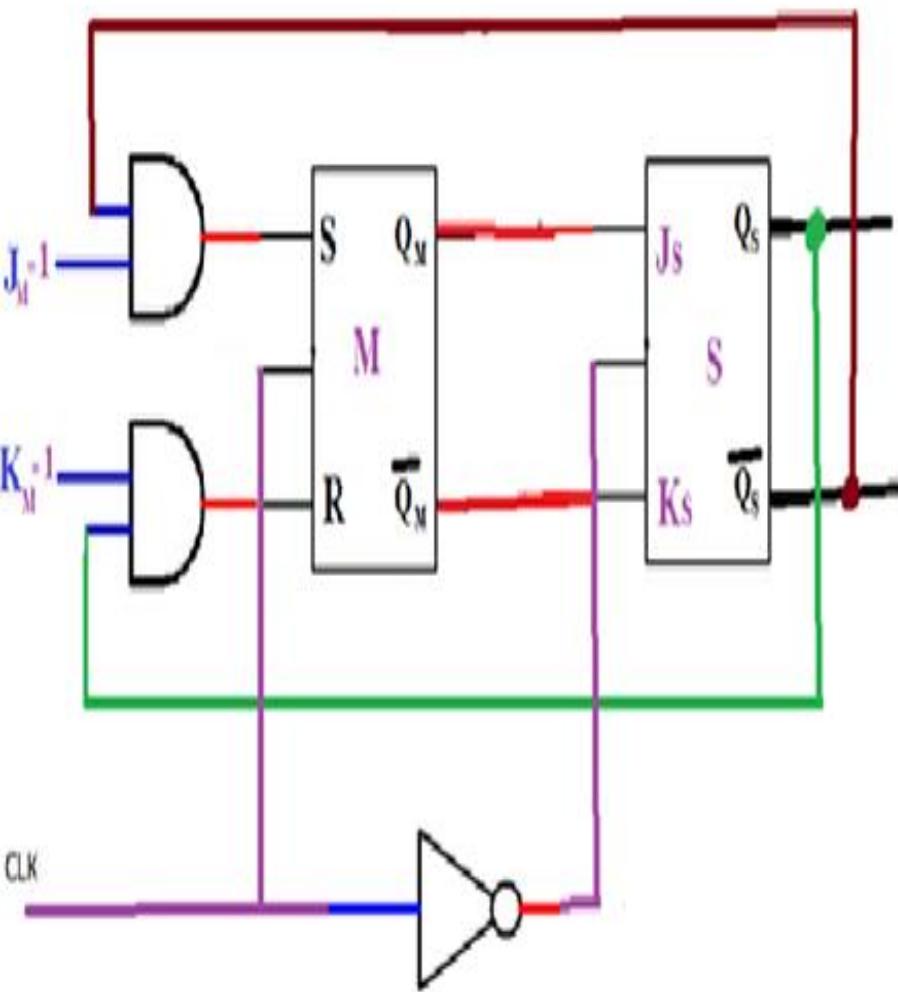
Draw the output wave form



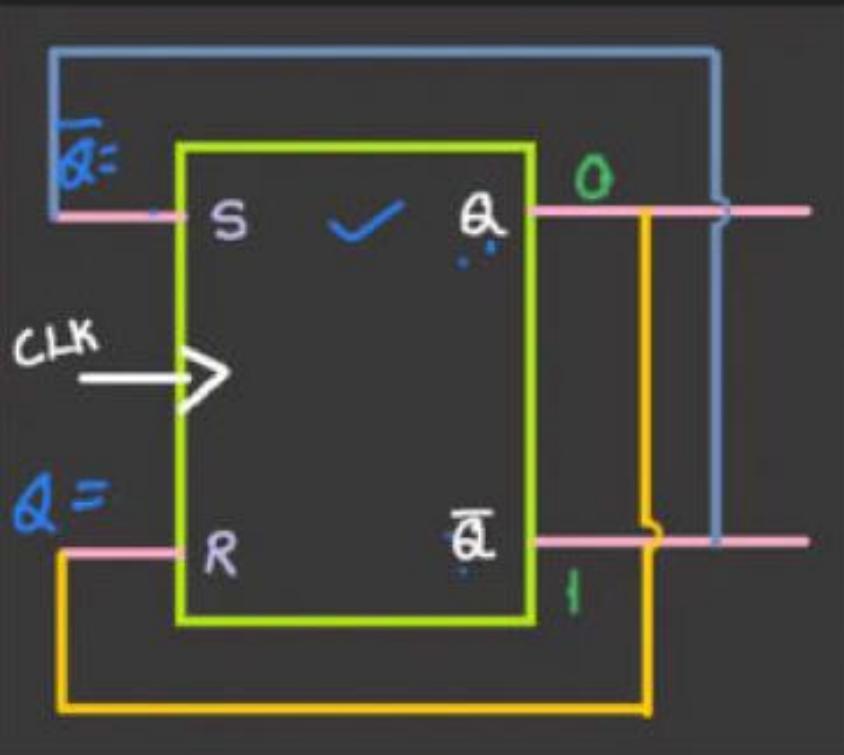
Draw the output wave form



Draw the output waveform



Q) Find the output frequency of the FF



$Q = 0 \quad 1 \quad 0 \quad 1$

$\bar{Q} = 1 \quad 0 \quad 1 \quad 0$

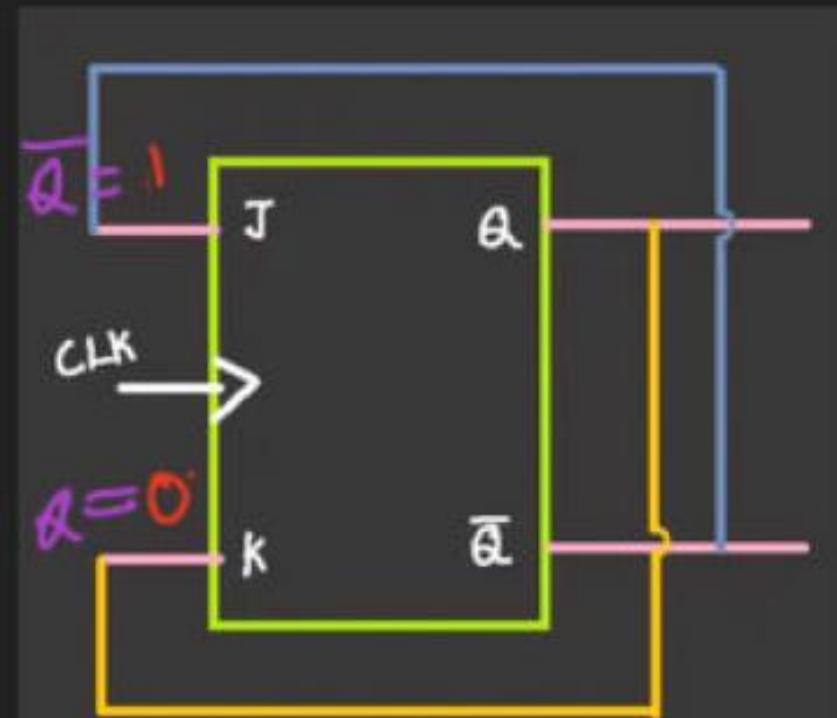
$$T_{O/P} = 2 T_{CLK}$$

$$\frac{1}{f_{O/P}} = \frac{2}{f_{CLK}}$$

$$f_{O/P} = \frac{f_{CLK}}{2}$$



Q) Find the output frequency of the FF



$$Q = 0 \quad 1 \quad 0 \quad 1$$

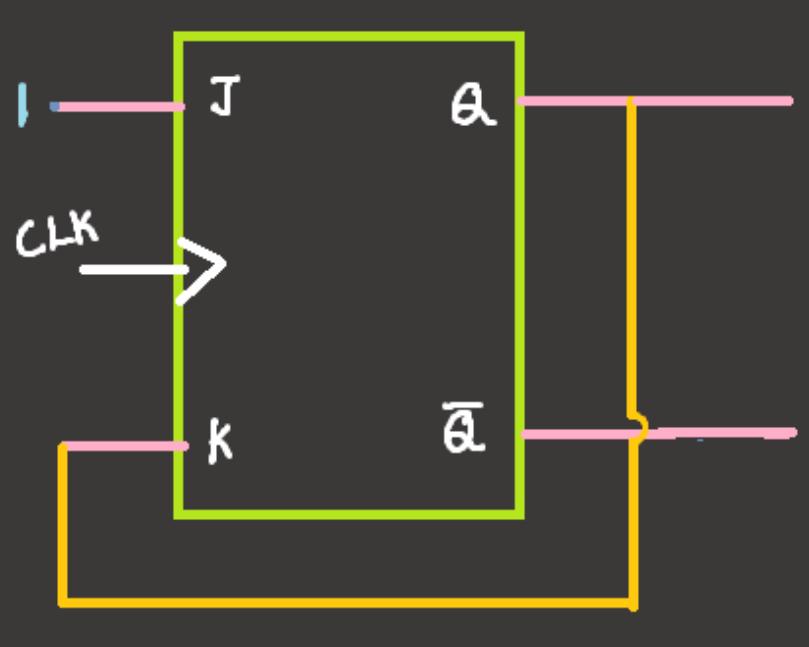
$$\bar{Q} = 1 \quad 0 \quad 1 \quad 0$$

$$T_{OLP} = 2 T_{qK}$$

$$f_{OLP} = \frac{f_{CLK}}{2}$$



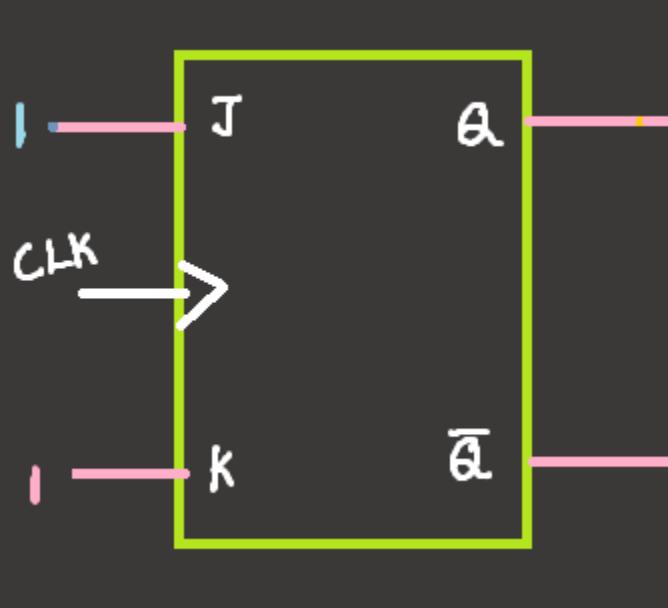
Q) Find the output frequency of the FF



$$f_{OP} = \frac{f_{CLK}}{2}$$

$$T_{OP} = 2 T_{CLK}$$

Q) Find the output frequency of the FF

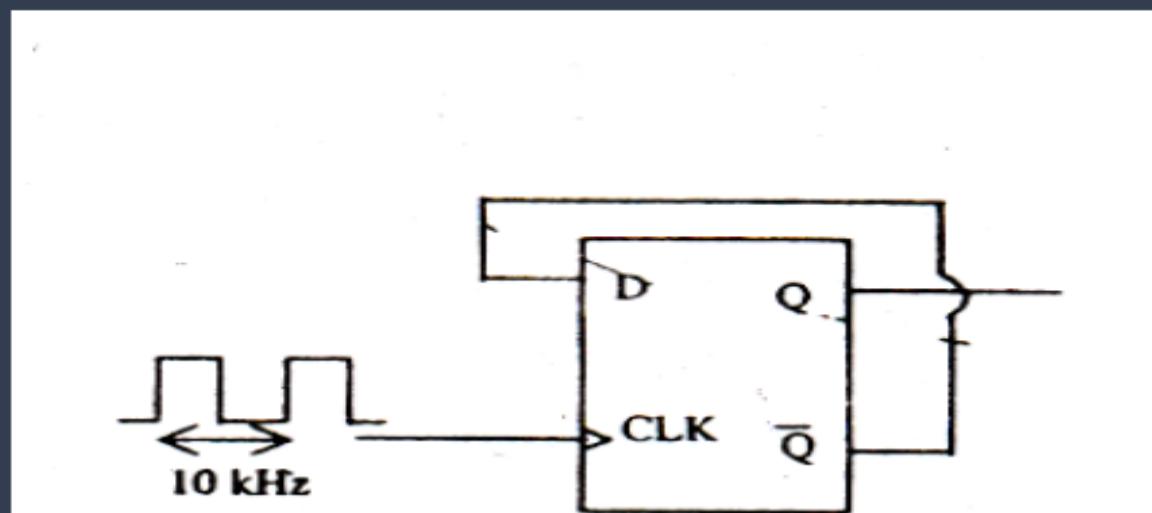


$$T_{DIP} = 2 \text{ TCK.}$$

$$f_{DIP} = \frac{f_{CK}}{2}.$$

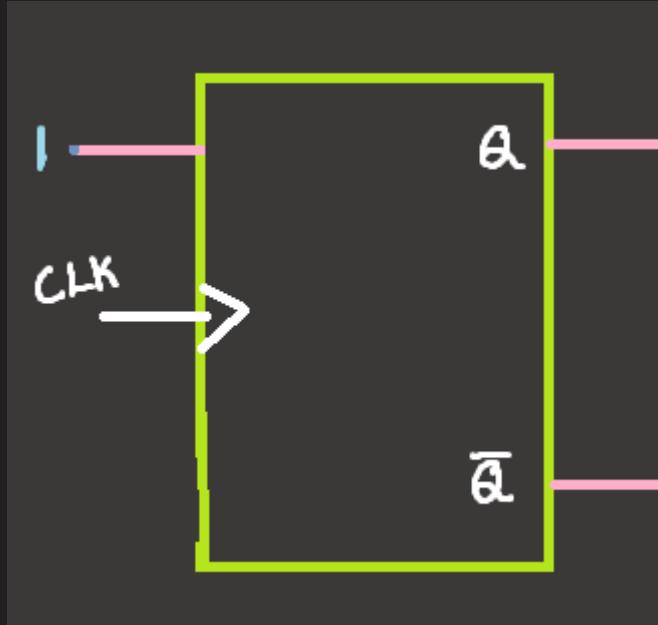
The frequency of the clock signal applied to the rising edge triggered D flip-flop shown in Fig. is 10 kHz. The frequency of the signal available at Q is (GATE – EE – 2002)

- (a) 10 kHz
  - (b) 2.5 kHz
  - (c) 20 kHz
  - (d) 5 kHz



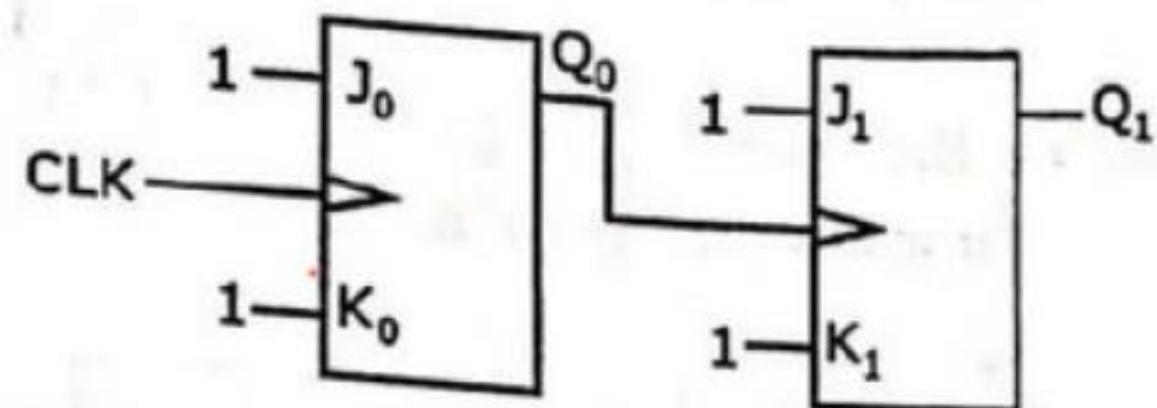
$$f_{0/D} = \frac{f_{CK}}{2}.$$

Q) Find the output frequency of the FF



$$f_{OP} = \frac{f_{CLK}}{2}$$

Find the frequency of Q<sub>0</sub> and Q<sub>1</sub>, if the clock frequency is 10khz



$$T_{Q_0} = 2 T_{CK}$$

$$f_{Q_0} = \frac{f_{CK}}{2}$$

$$f_{Q_0} = 5 \text{ kHz}$$

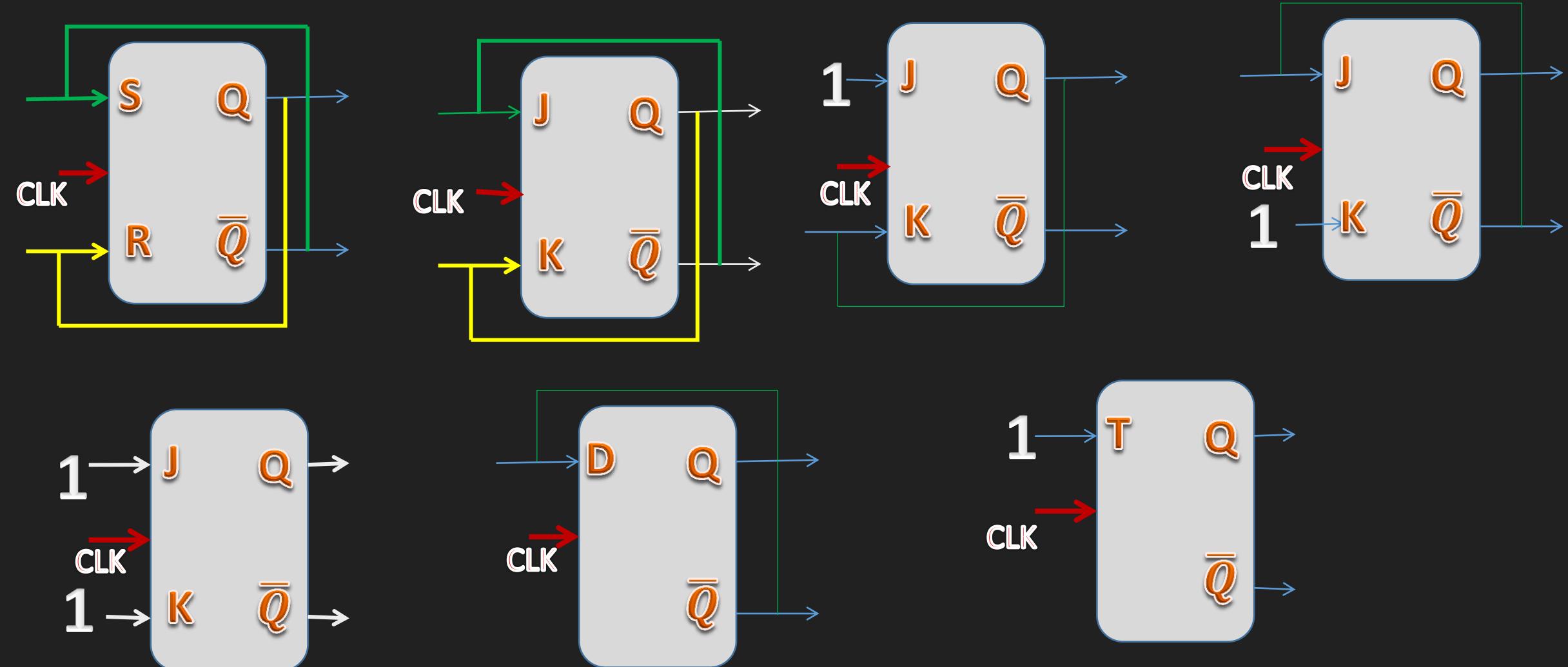
$$T_{Q_1} = 4 T_{CK}$$

$$f_{Q_1} = \frac{f_{CK}}{4}$$

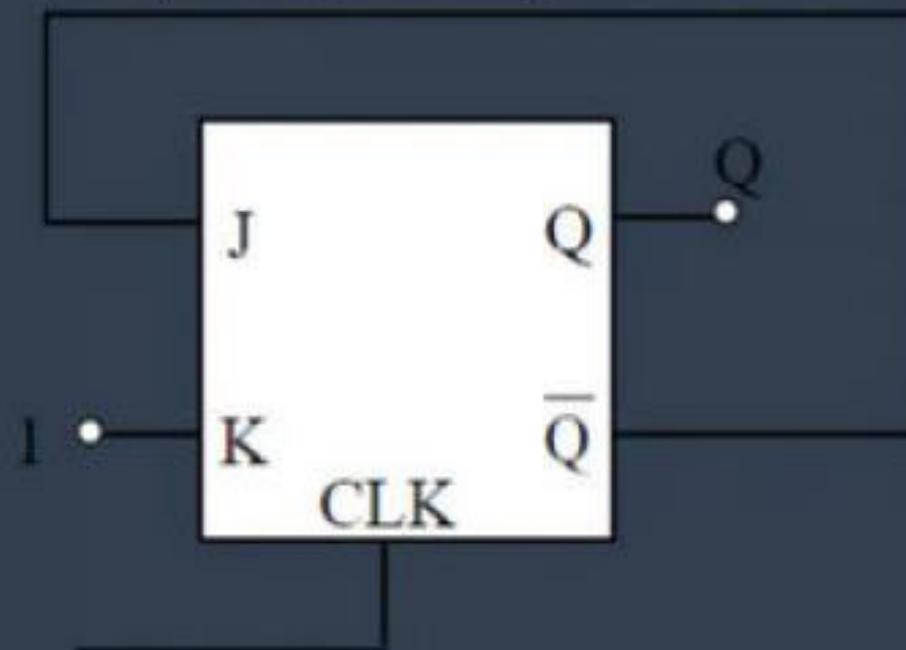
$$f_{Q_1} = 2.5 \text{ kHz}$$



# Toggle Modes



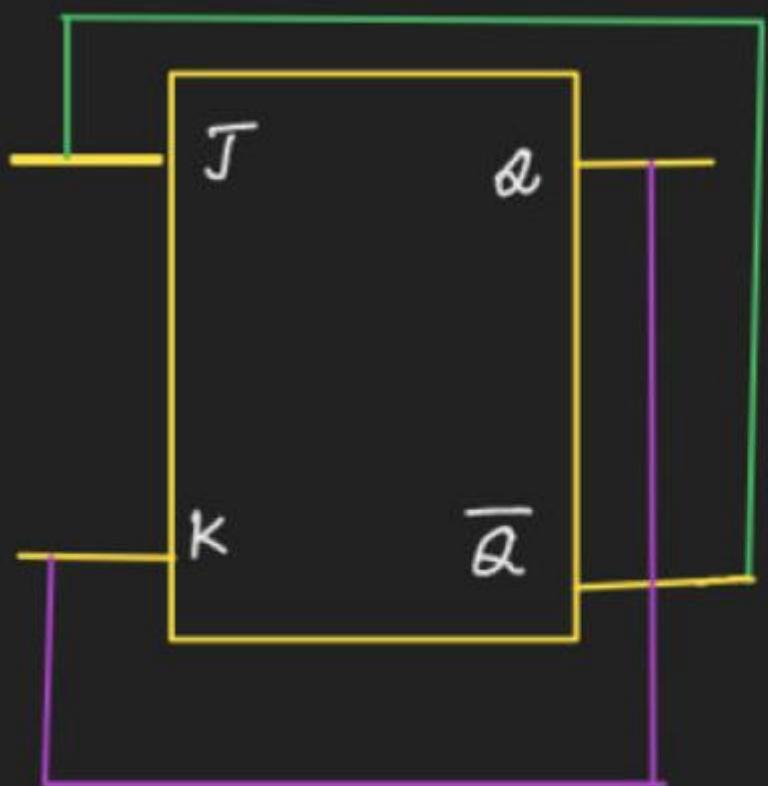
In a J-K flip-flop we have  $J=Q$  and  $K=1$  (see figure) Assuming the flip-flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be (GATE-1997)



*Toggle mode*

- (a) 010000      (b) 011001      (c) 010010      (d) 010101

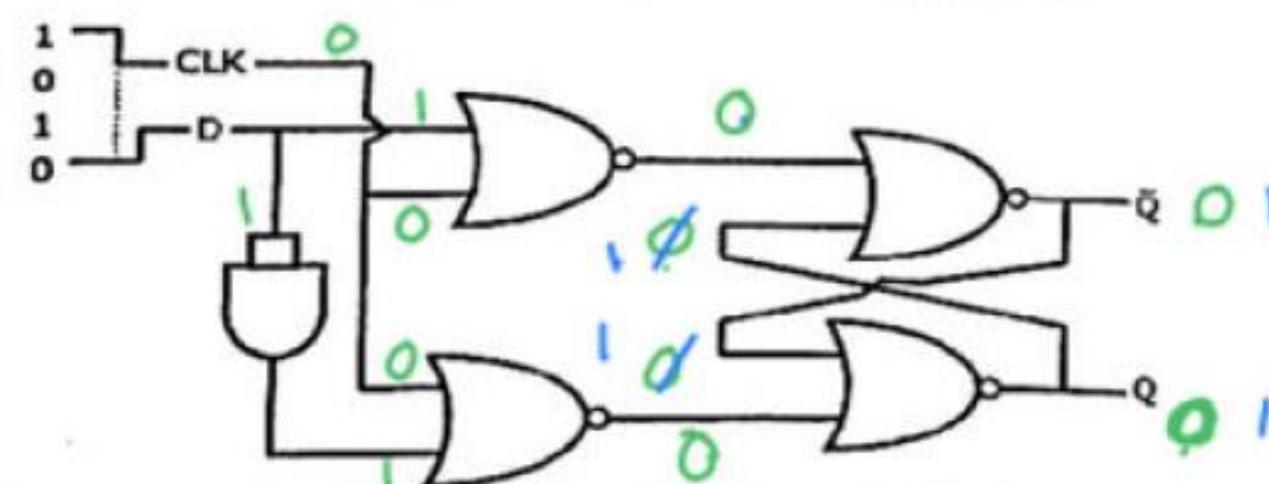
For a J-K flip-flop its J input is tied to its own Q output and its K input is connected to its own Q output. If the flip-flop is fed with a clock of frequency 1 MHz, its Q output frequency will be \_\_\_\_\_. (GATE – EE – 1995)



Toggle mode

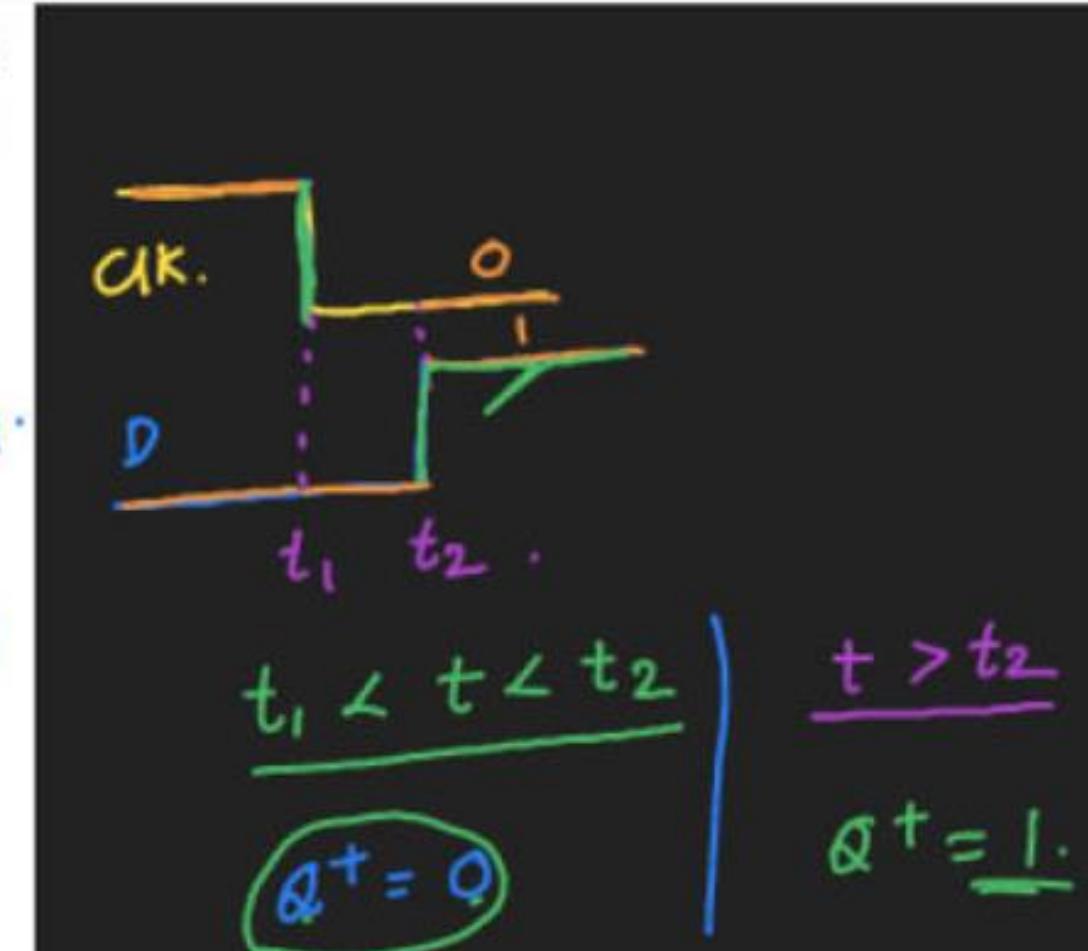
$$f_{O/P} = \frac{f_{CLK}}{2} = 0.5 \text{ MHz}$$

For the circuit shown in the figure, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible



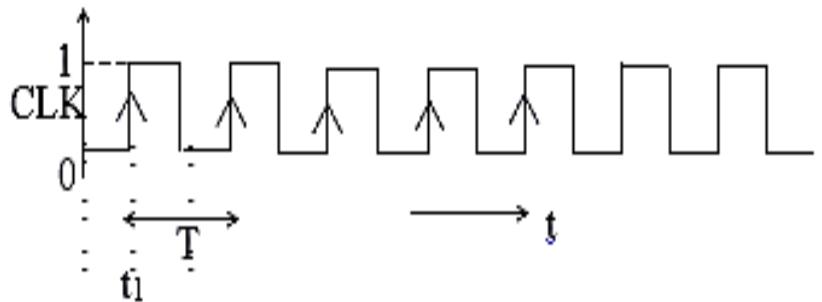
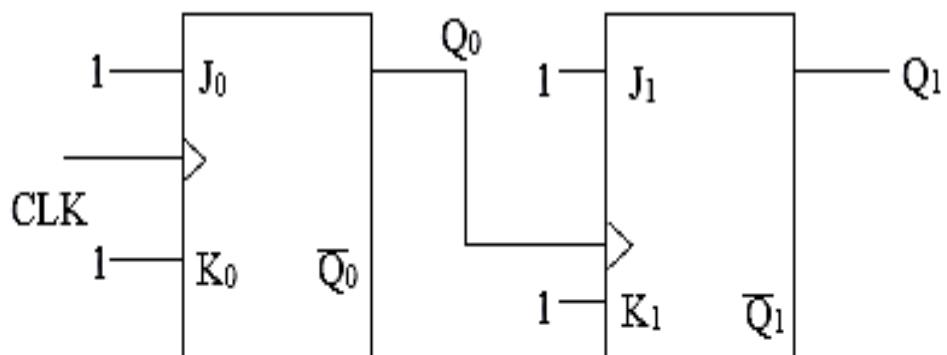
Which of the following statements is true?

- (A) Q goes to 1 at the CLK transition and stays at 1
- (B) Q goes to 0 at the CLK transition and stays at 0
- (C) Q goes to 1 at the CLK transition and goes to 0 when D goes to 1
- (D) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1

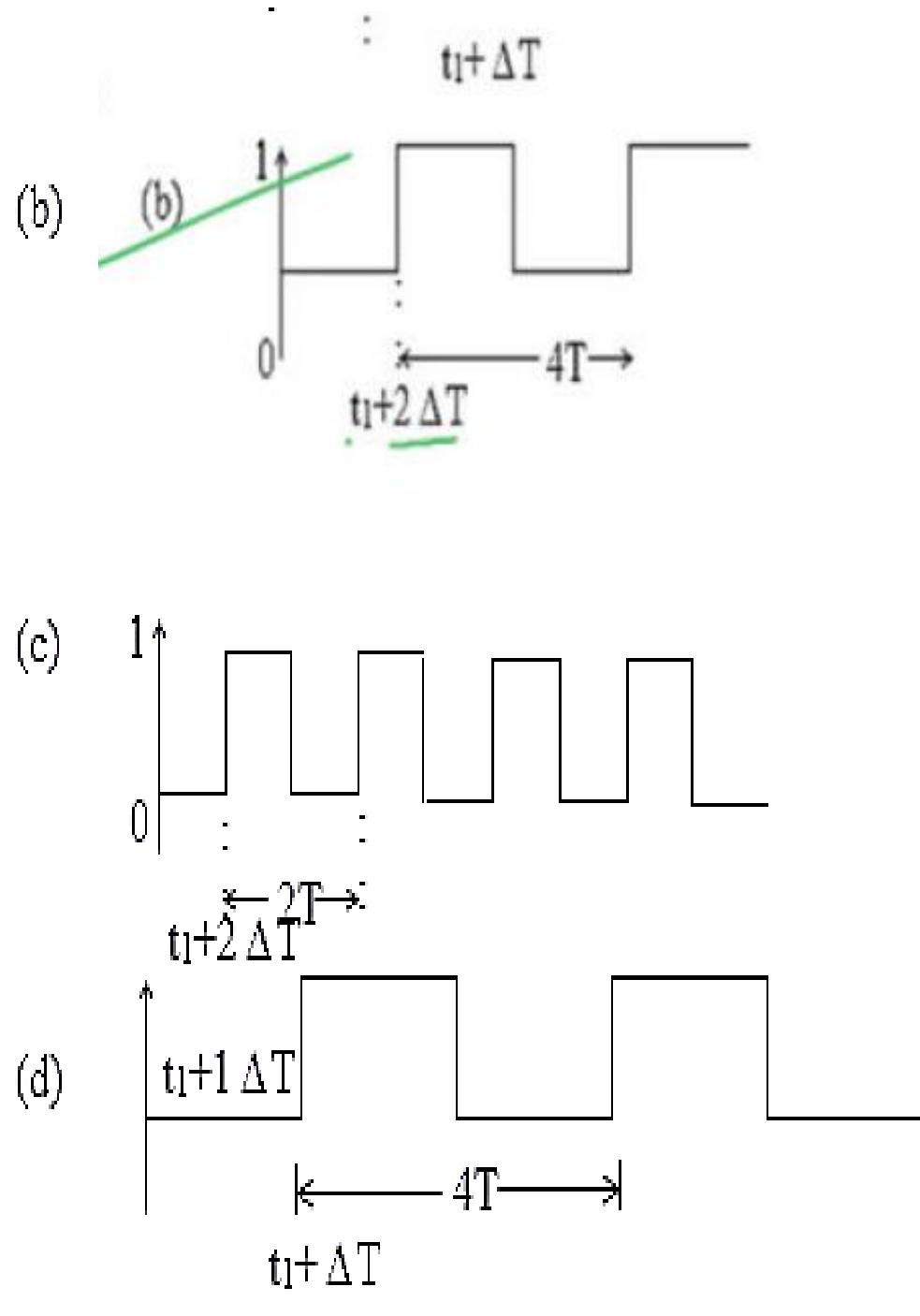
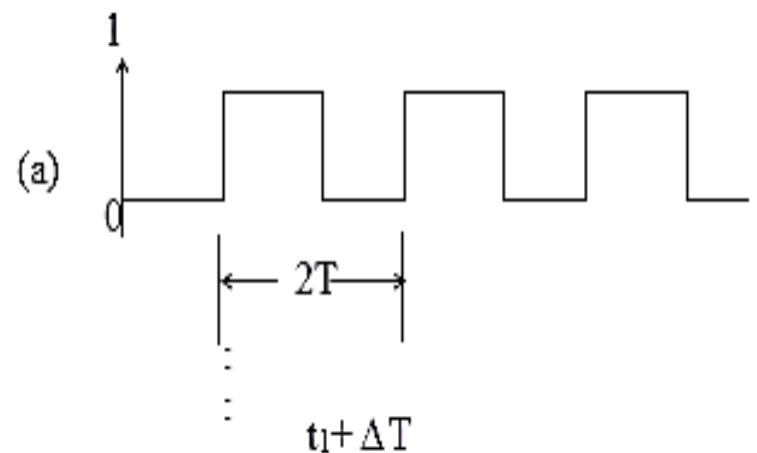


For each of the positive edge-triggered J-K flipflop used in the following figure, the propagation delay is  $\Delta T$

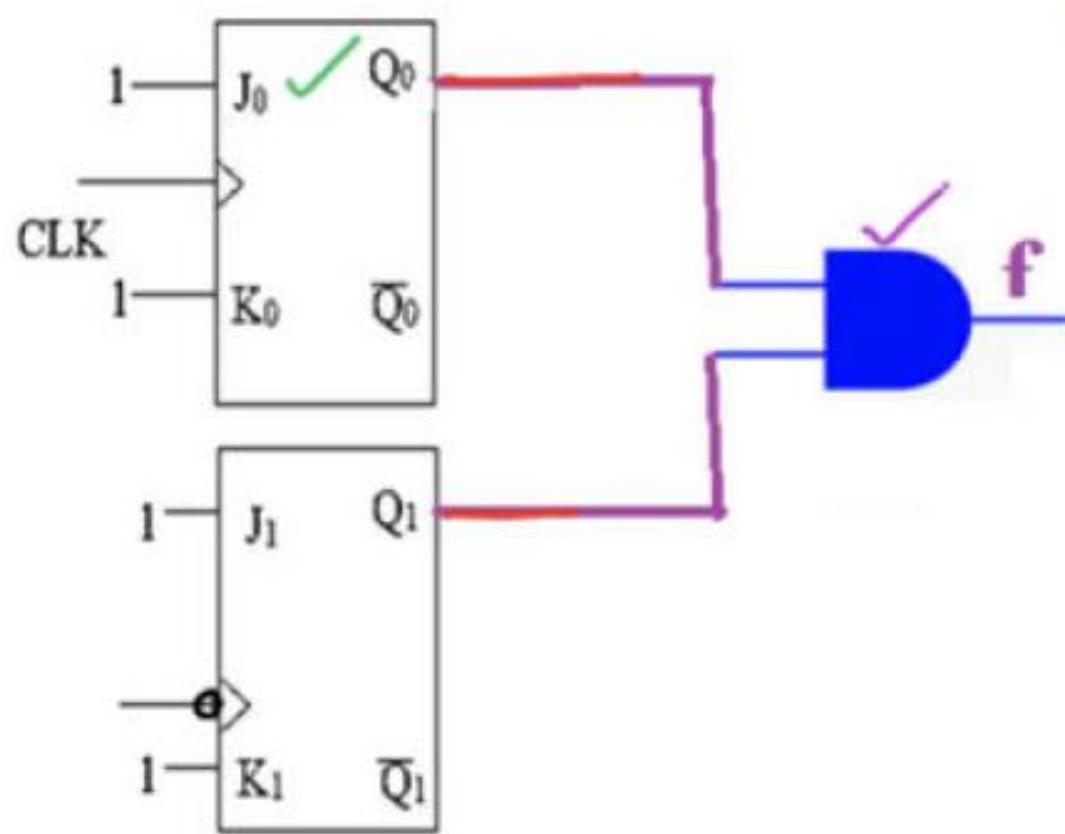
(GATE-2008)



Which of the following waveforms correctly represents the output at  $Q_1$ ?

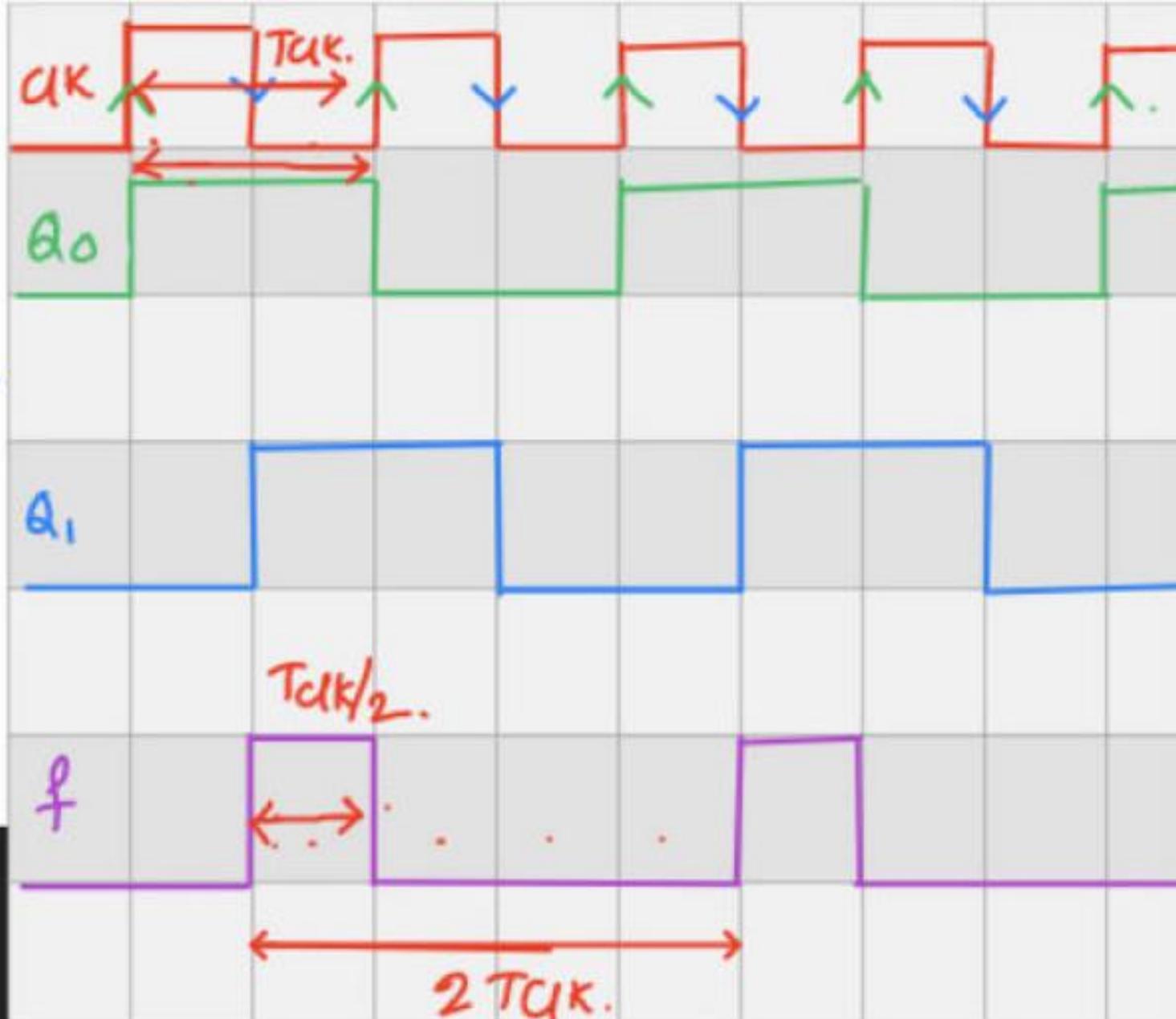


Find the frequency of f and duty cycle



$$T_{d/p} = 2 T_{CK}$$

$$f_{o/p} = \frac{f_{CK}}{2}$$



Duty cycle

$$D = \frac{T_{on}}{Total} = \frac{T_{clk}/2}{2\ T_{clk}}$$

$$D = \frac{1}{4} \times 100 \%$$

$$D = 25 \%$$

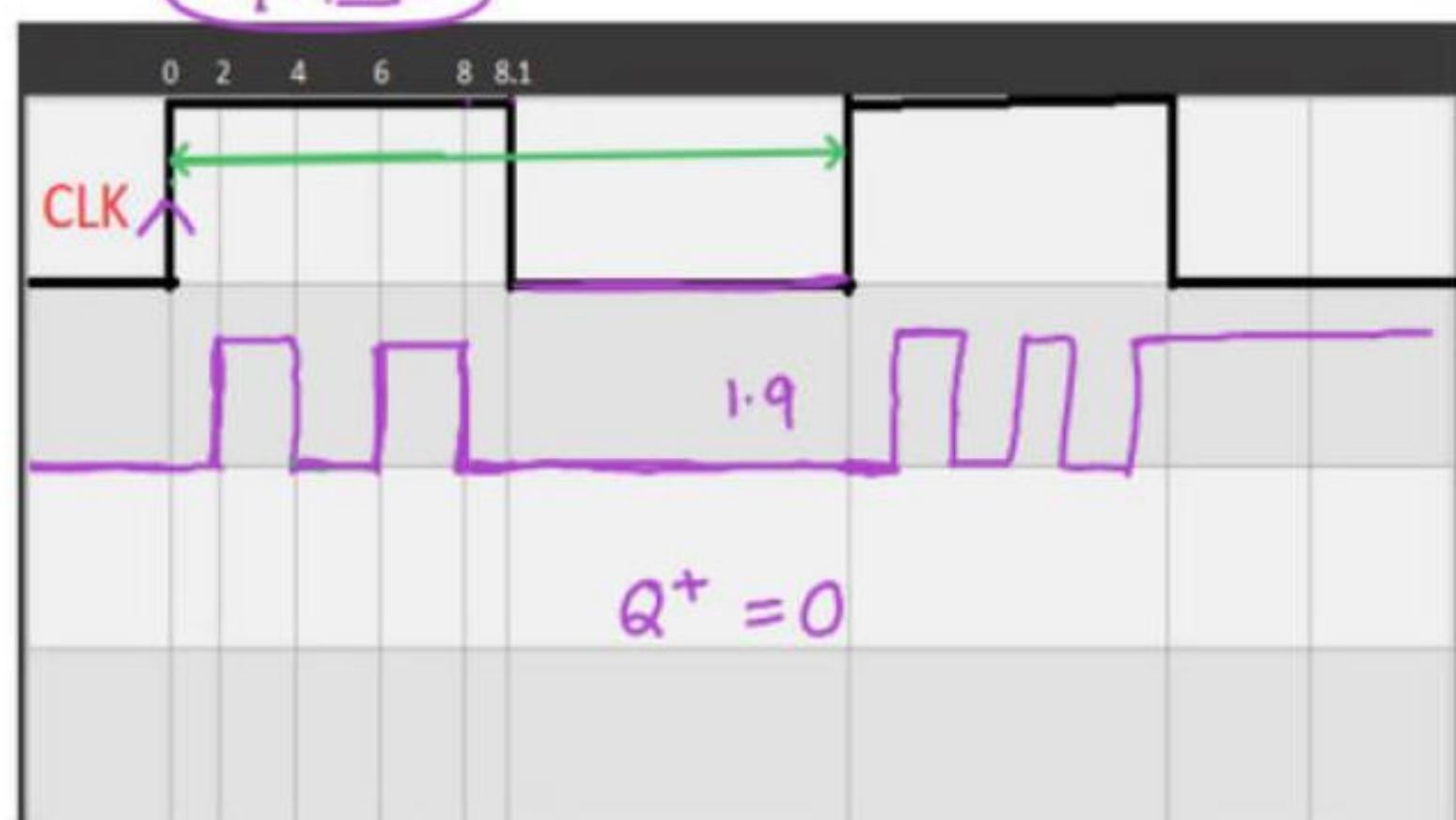
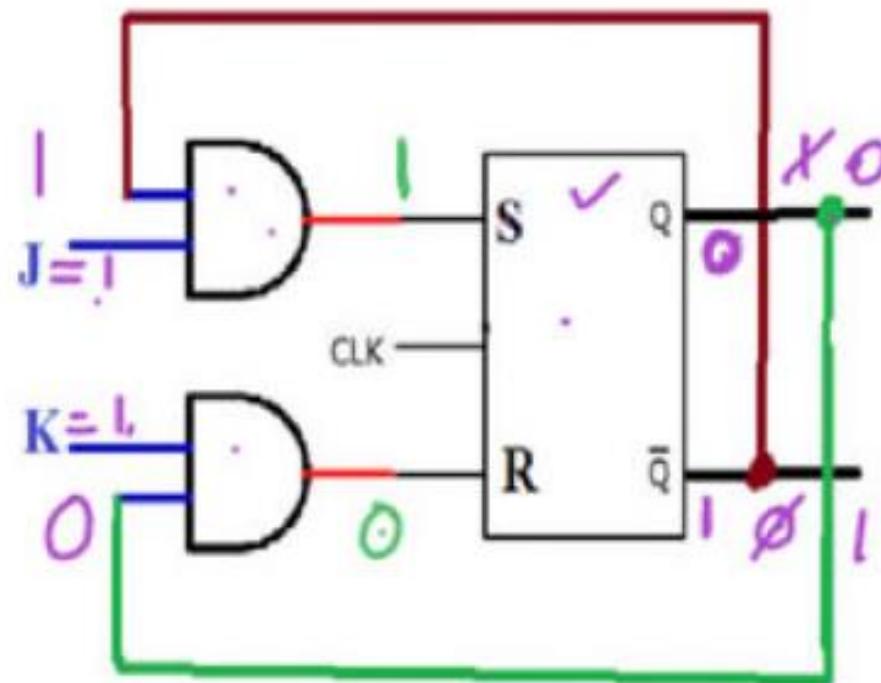
# Race Around Condition

# Race Around Condition

Case : 1

$$T_{clk} = 16.2 \text{ ns}$$

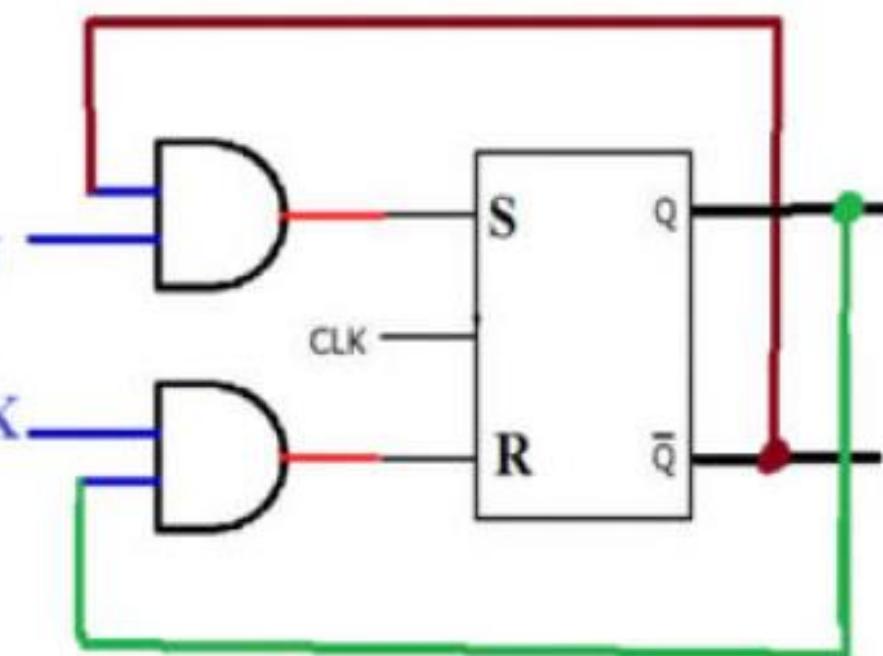
$$t_{pd} = 2 \text{ ns}$$



Case : 2

$$T_{clk} = \underline{20.2 \text{ ns}}$$

$$t_{pd} = 2 \text{ ns}$$



$$Q^+ = 1$$

The output of the FF changes to  $0 \rightarrow 1 \rightarrow 0 \dots$  Continuously at the starting of the next clock the output is uncertain , which is called as Race Around Condition (RAC )

RAC occurs in any FF if the following conditions satisfies

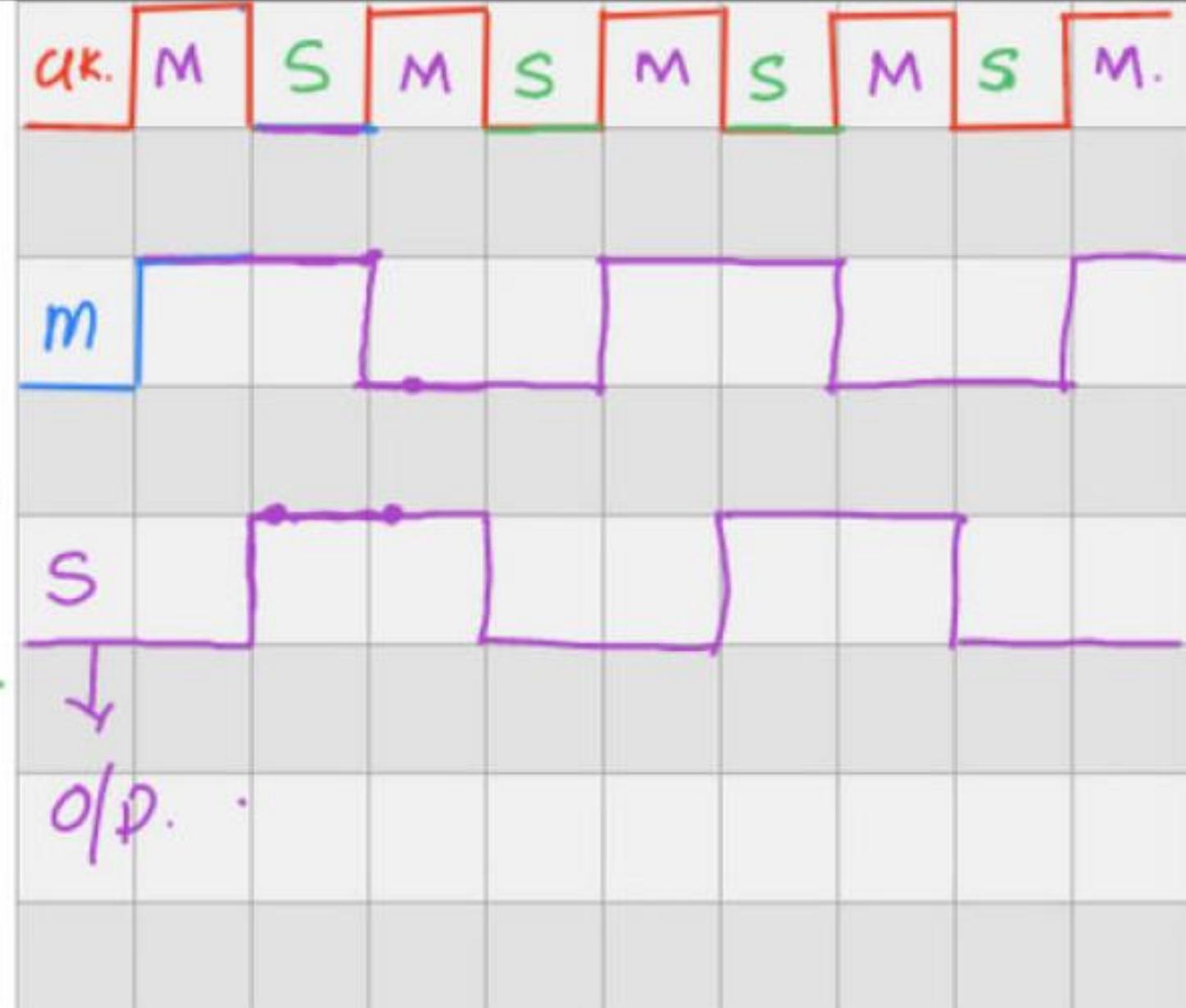
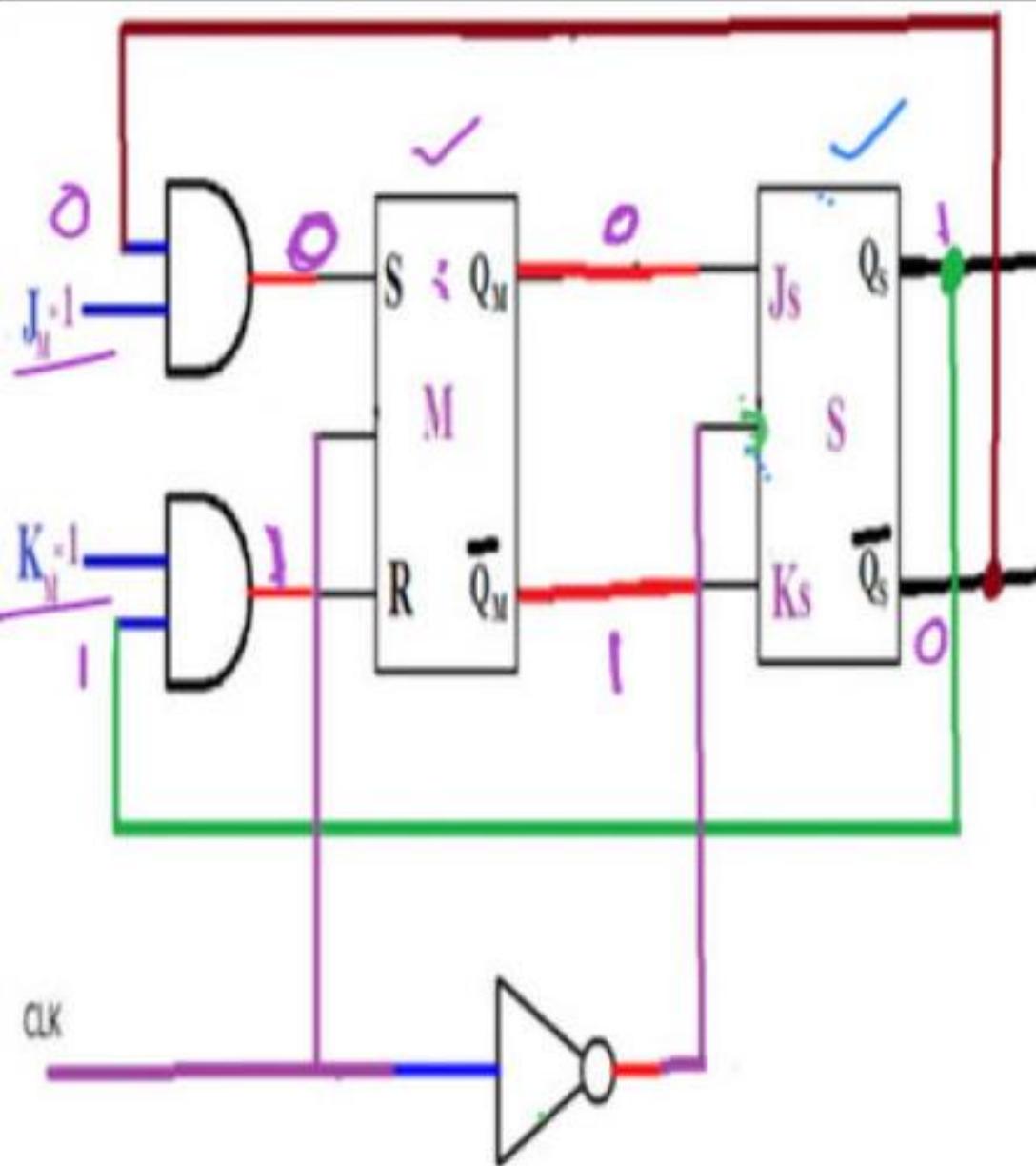
- 1.If the FFs are operated in level triggering
2. if  $(tpd) < (Tclk)_{on}$  ,
- 3.If the FFs are operated in Toggle mode

If the above conditions satisfies simultaneously then there is a continuous race in the output of the FF between 0 and 1 to reach the next state , who will be the winner of the race is not certain , that depends on tpd and (  $T_{clk}$  ) on .

## Remedy

1. (  $T_{clk}$  ) <sub>on</sub> < (tpd) < T
2. By using Edge triggered FF
3. By Master – Slave Configuration

# Master – Slave Configuration



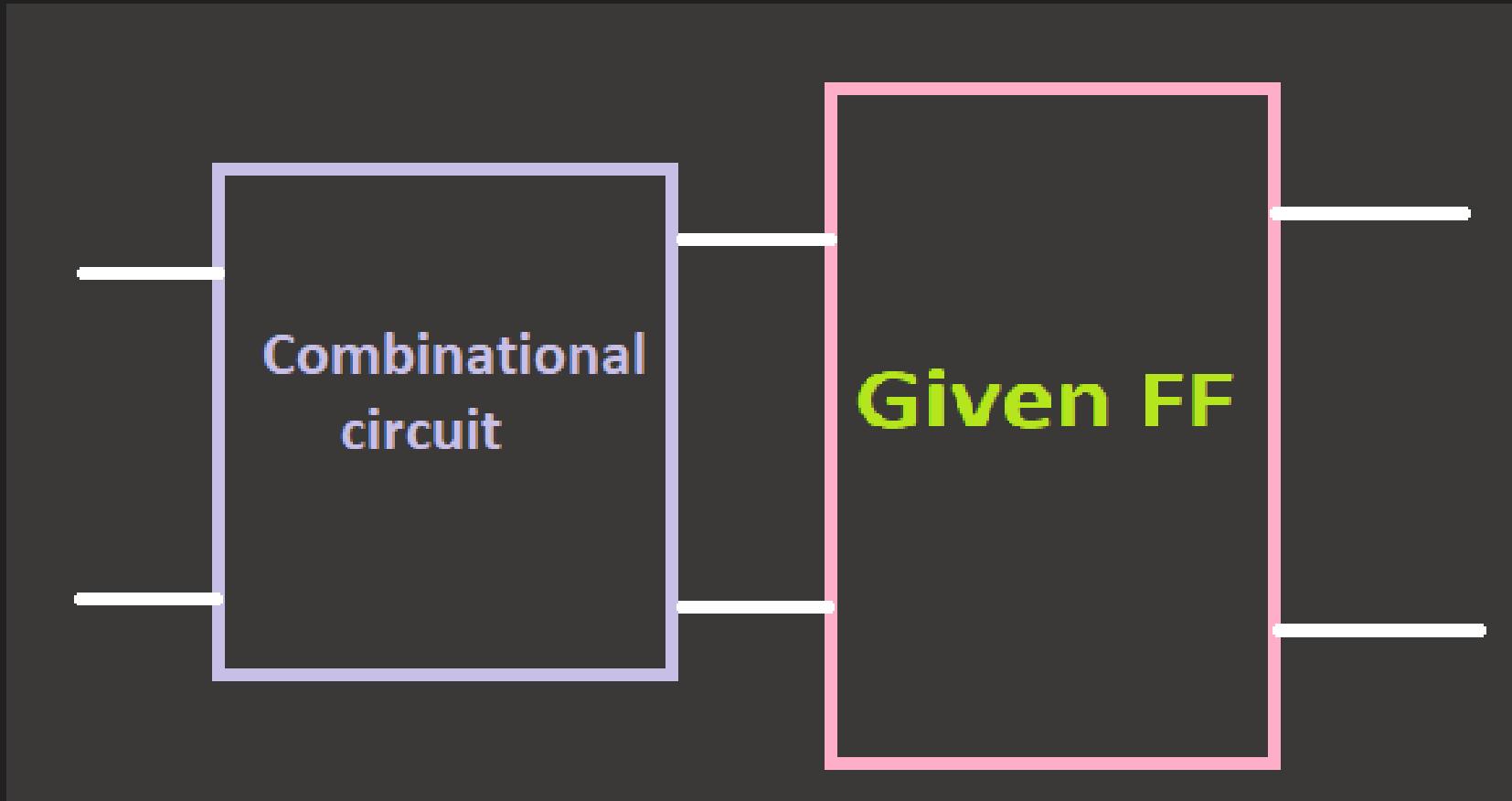
1. In case of **Master Slave configuration** , Master is applied with input clock and Slave is applied with inverted clock , so out of two FFs, at a time only one of the FF respond and other will not respond . As a result , Many times toggling in a single clock cycle has been converted to one time toggle , **hence RAC is avoided** .
2. In Master Slave configuration , command signal is generated by master FF and the response of the command signal is given by slave FF .
3. Master slave FF can store 1 – bit of data .

A master slave flip-flop has the characteristic that

(GATE-2004)

- (a) change in the input immediately reflected in the output
- (b) change in the output occurs when the state of the master is affected
- (c) change in the output occurs when the state of the slave is affected
- (d) both the master and the slave states are affected at the same time.

# Conversion of FFs



# Steps

1. Write the state table of the required FF
2. Match the excitation table of the given FF to required FF
3. Write excitation expression
4. Minimize logical expression
5. Implement logic circuit

Q) Convert the SR FF to JK FF

$J$	$K$	$Q$	$Q^+$	$S$	$R$
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

$Q$	$Q^+$	$S$	$R$
0	0	0X	
0	1	10	
1	0	01	
1	1	X0	

$$S(J, K, Q) = \sum m(4, 6) + d(1, 5)$$

$$R(J, K, Q) = \sum m(3, 7) + d(0, 2)$$

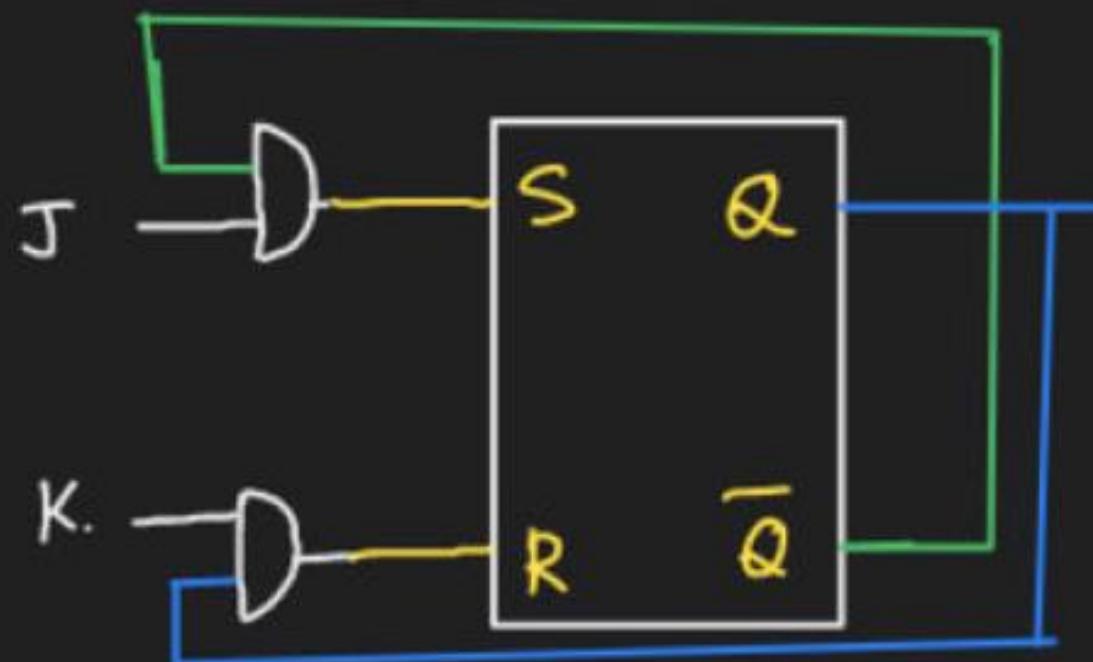
S

$J$	$KQ$	$\bar{K}\bar{Q}$	$\bar{K}Q$	$K\bar{Q}$	$K\bar{Q}$
$\bar{J}$			$X$		
$J$		$X.$		$C$	

R

$J$	$KQ$	$\bar{K}\bar{Q}$	$\bar{F}Q$	$K\bar{Q}$	$K\bar{Q}$
$\bar{J}$		$X$			
$J$			$I$	$I$	$X.$

$$S = \underline{\bar{J}\bar{Q}}$$



$$R = \underline{KQ}$$

Convert the SR FF to the XY FF whose truth table is given below

X	Y	Q+
0	0	1
0	1	<u><u><math>\overline{Q}</math></u></u>
1	0	<u><u>Q</u></u>
1	1	0

T T

Q	Q <sup>+</sup>	SR
00	0x	
01	10	
10	01	
11	x0	

X	Y	Q	Q <sup>+</sup>	S	R
0	0	0	1	1	0
0	0	1	1	x	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	0	0	x
1	0	1	1	x	0
1	1	0	0	0	x
1	1	1	1	0	1

$$S(x, y, Q) = \sum m(0, 2) + d(1, 5)$$

$$R(x, y, Q) = \sum m(3, 7) + d(4, 6)$$

R

S

x	$yQ$	$\bar{y}\bar{Q}$	$\bar{y}Q$	$y\bar{Q}$	$yQ$
$\bar{x}$	1	x		1	
x		x			

x	$yQ$	$\bar{y}\bar{Q}$	$\bar{y}Q$	$y\bar{Q}$	$yQ$
$\bar{x}$					
x	x			1	x

$$R = yQ$$

$$S = \bar{x}\bar{Q} = \bar{x+yQ}$$



# Conversion of FFs

JK to SR

$$\begin{aligned} J &= S \\ K &= R \end{aligned}$$

JK to D

$$\begin{aligned} J &= D \\ J &= \bar{D} \end{aligned}$$

JK to T

$$\begin{aligned} J &= T \\ K &= T \end{aligned}$$

SR to JK

$$\begin{aligned} S &= J\bar{Q} \\ R &= KQ \end{aligned}$$

SR to D

$$\begin{aligned} S &= D \\ R &= \bar{D} \end{aligned}$$

SR to T

$$\begin{aligned} S &= T\bar{Q} \\ R &= TQ \end{aligned}$$

D to SR

$$D = S + \bar{R}Q$$

D to JK

$$D = J\bar{Q} + \bar{K}Q$$

D to T

$$D = T \oplus Q$$

T to SR

$$T = S\bar{Q} + RQ$$

T to JK

$$T = J\bar{Q} + KQ$$

T to D

$$T = D \oplus Q$$

# Shift Registers

- A FF is a single bit memory element , which cant store multiple bits at a time , so we combine number of FFs the resultant ckt can serve this purpose , is known as shift registers .
- Since no data manipulation is required , so we prefer D- FFs for this purpose

As we know for D –FF

$$Q+ = D$$

To store n –bits , n – FFs are required

The data is available in two forms

1. Serial data ( Temporal code )

2. Parallel data ( spatial code )

➤ Depending on i/p and o/p , registers are classified into 4 types

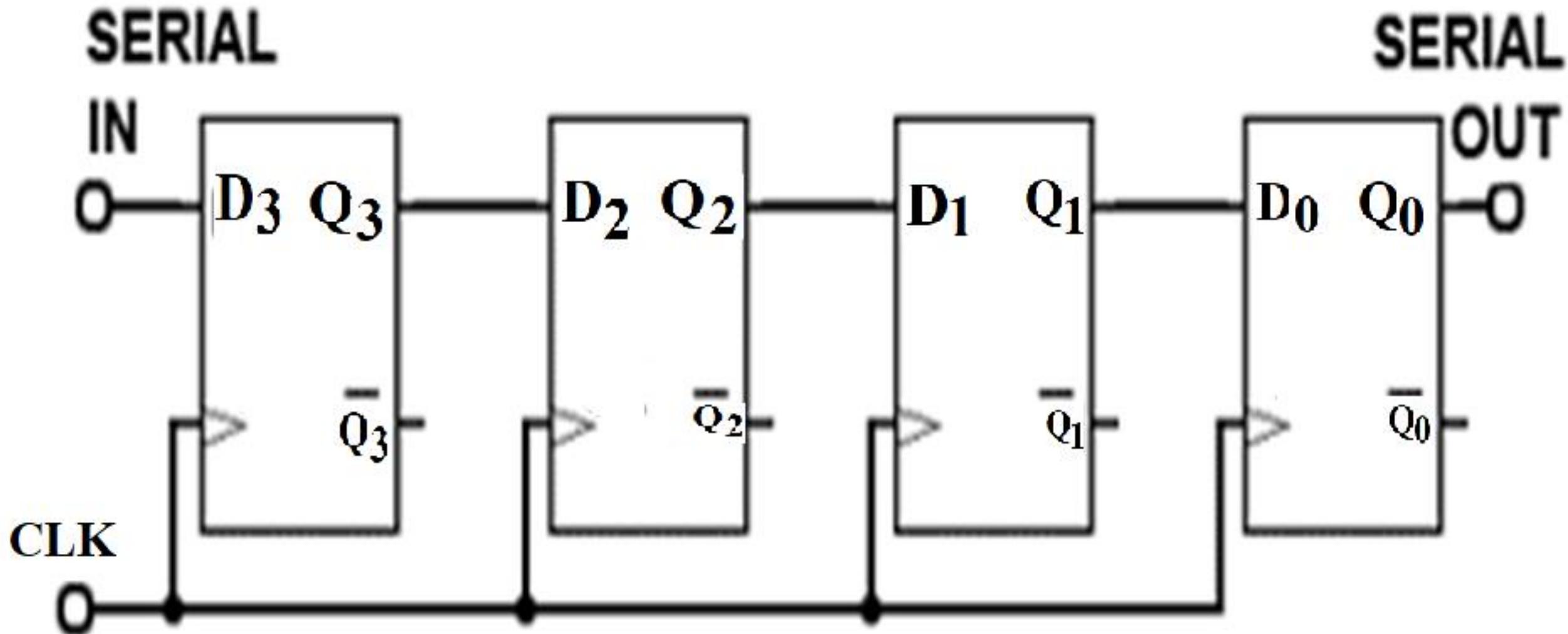
1.Serial In Serial Out (SISO )

2.Serial In Parallel Out (SIPO)

3.Parallel In Parallel Out (PIPO )

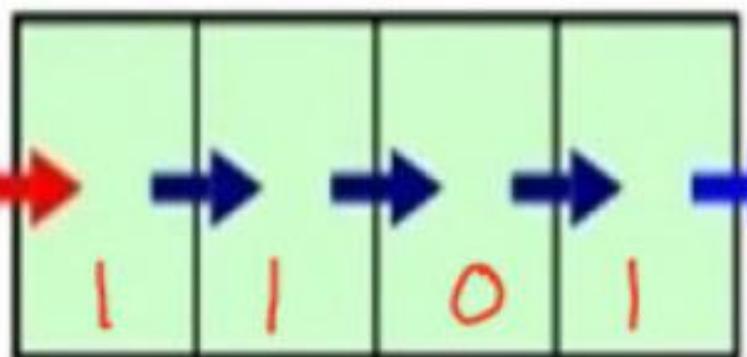
4.Parallel In Serial Out ( PISO )

# Serial In Serial Out



# Block Diagram representation

Data in → Data out



➤ SISO Configuration has only

1- input  
1- output

1101

➤ For SISO configuration

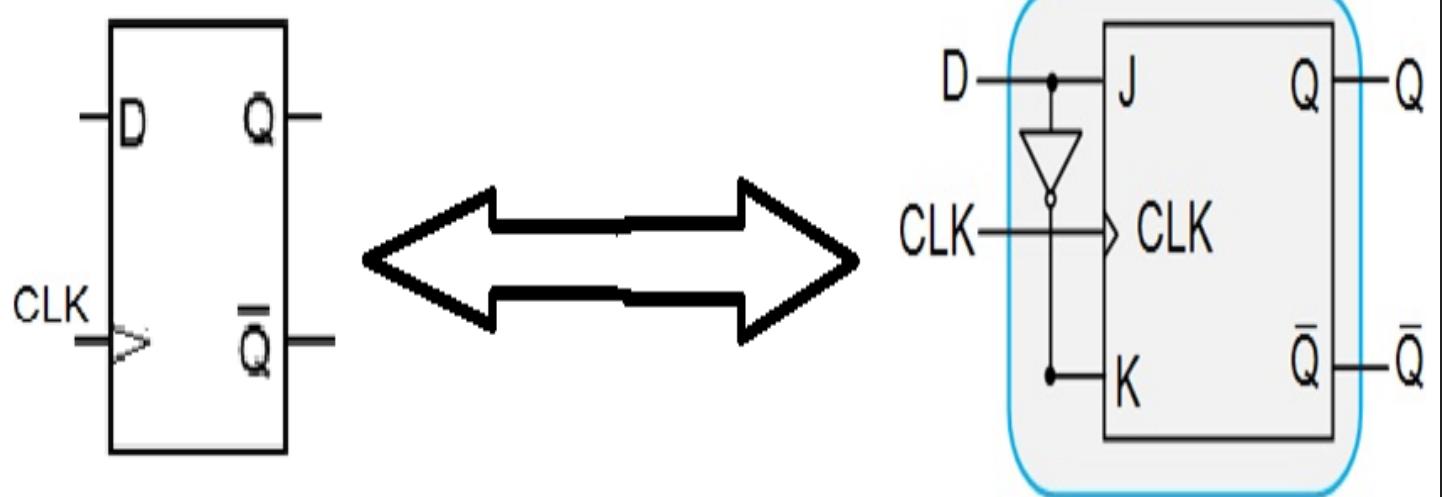
for storing =  $n$  - Clock pulses

for retrieving =  $(n-1)$  clock pulses

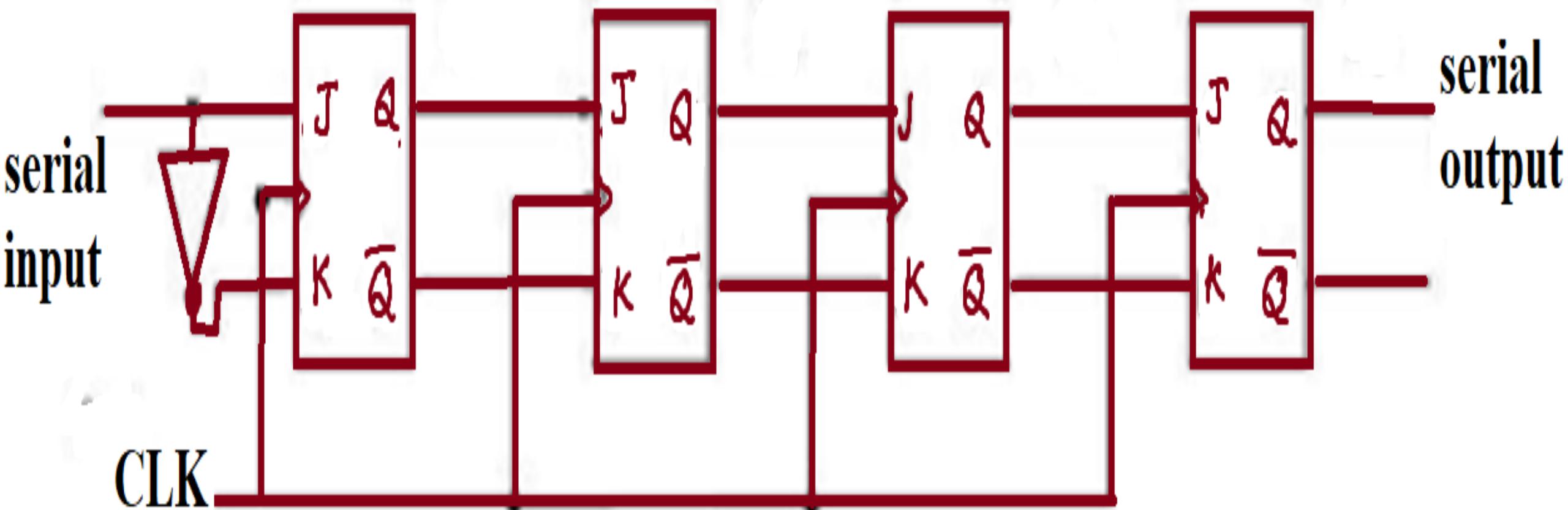
Total number clock pulses =  $(2n-1)$

CLK	INPUT	Q3	Q2	Q1	Q0
0	x	0	0	0	0
1	1	1	0	0	0
2	0	0	1	0	0
3	1	1	0	1	0
4	1	1	1	0	1
5	x	x	1	1	0
6	x	x	x	1	1
7	x	x	x	x	1

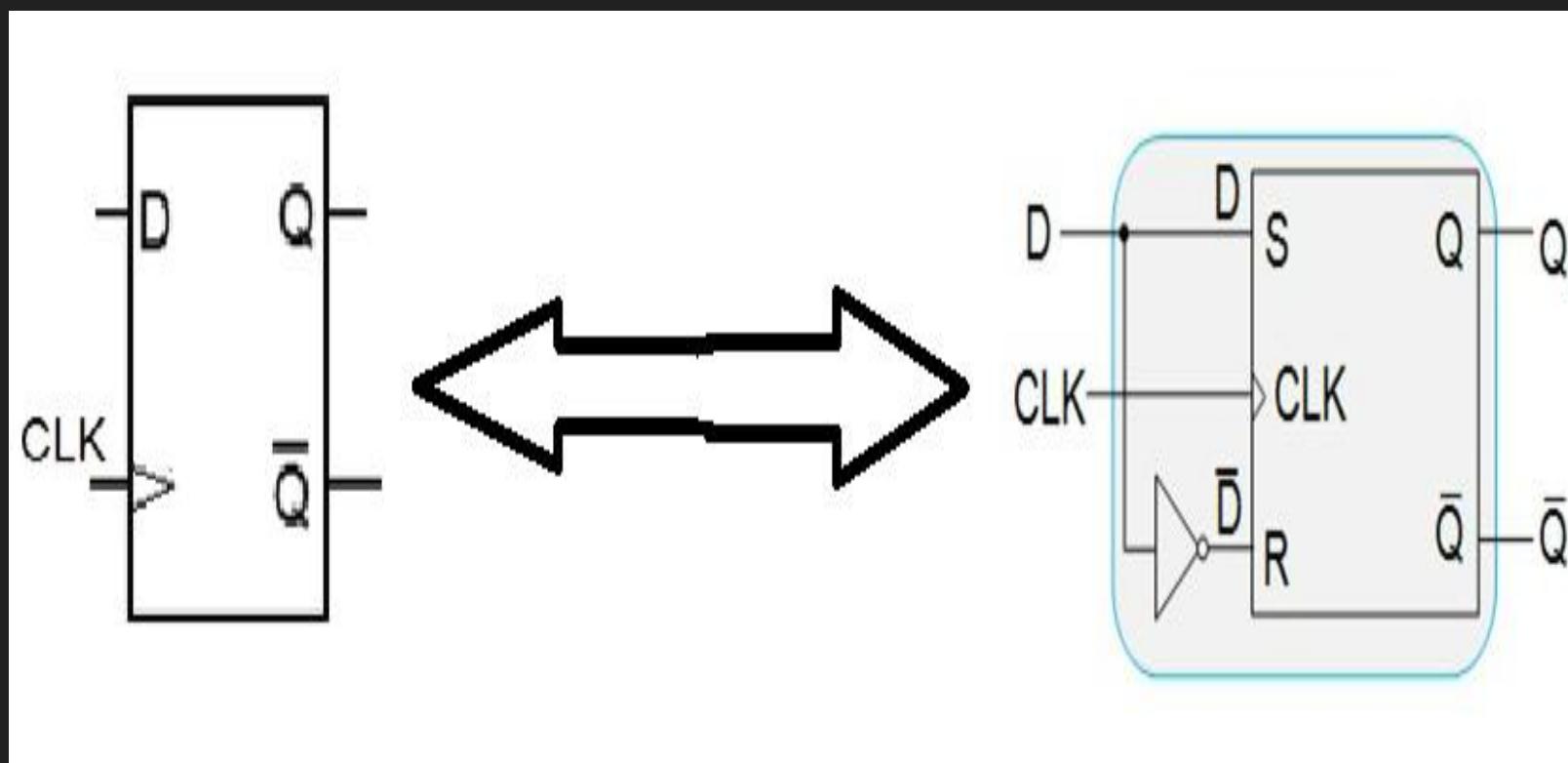
**JK FF**  **D FF**



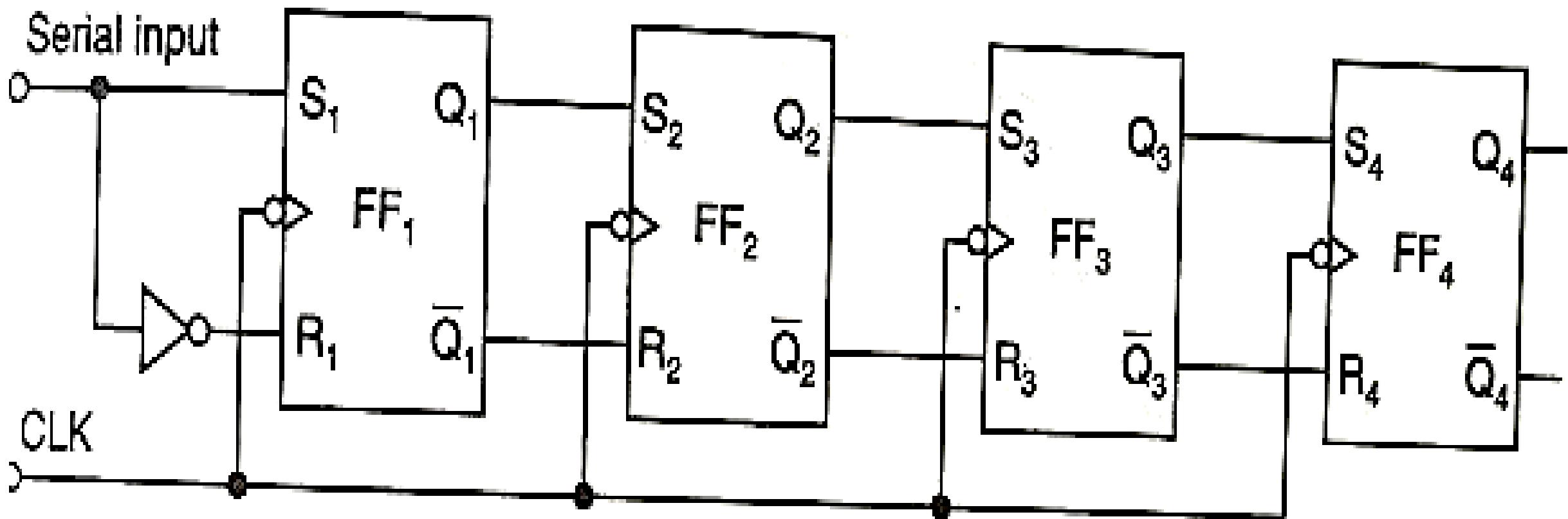
# SISO Shift Register using JK FF



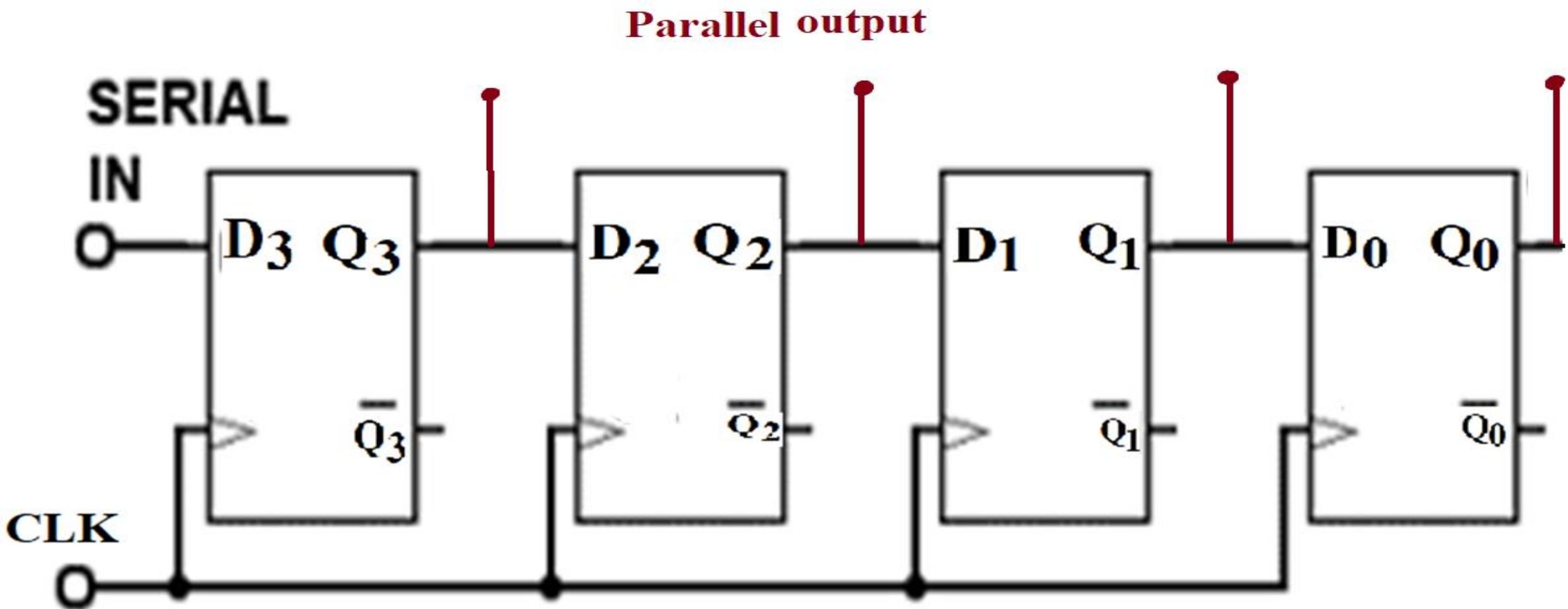
# SR FF to D FF



# SISO using SR FF



# Serial In Parallel Out



➤ SIPO Configuration has only

1- input

4- output

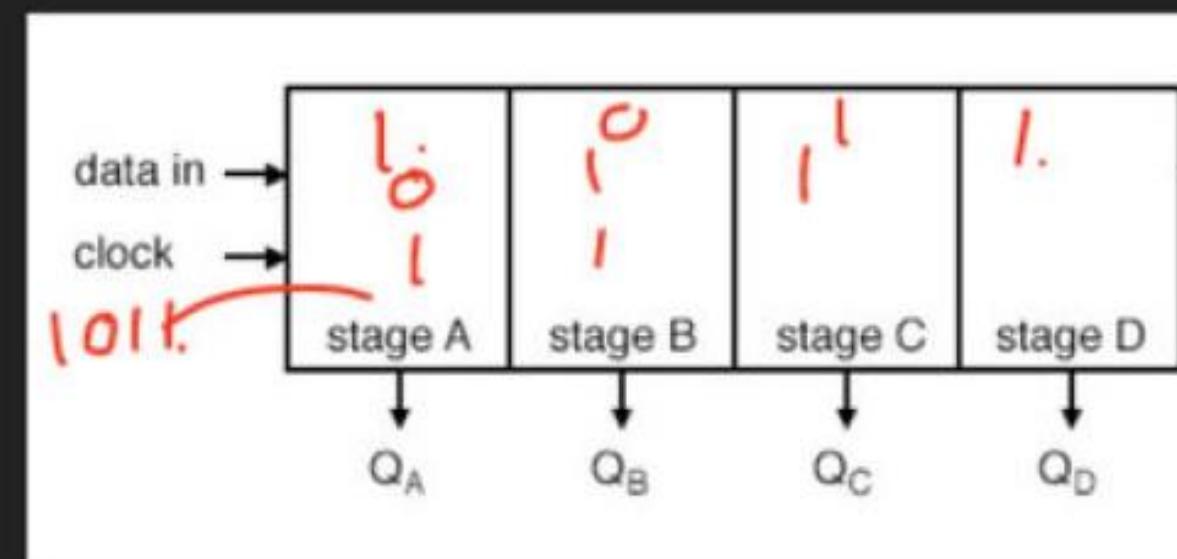
➤ For SIPO configuration

for storing =  $N$ - Clock pulses

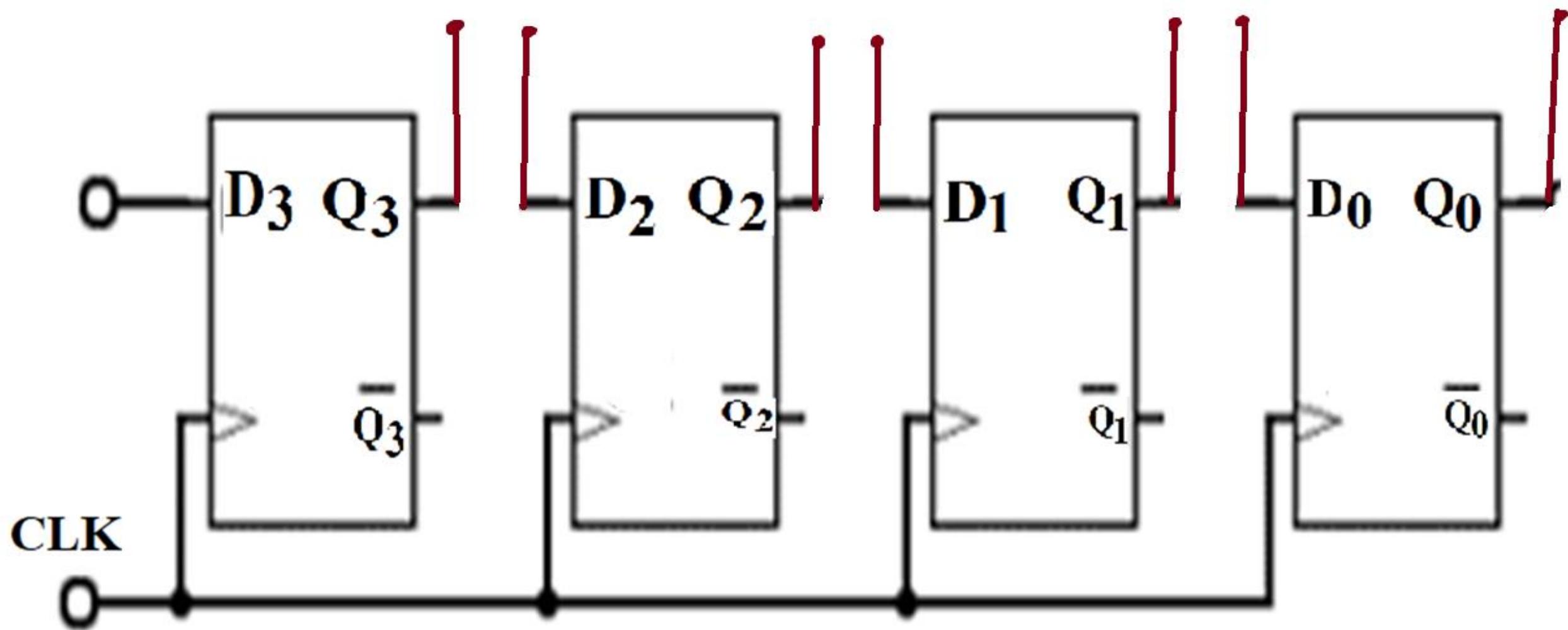
for retrieving =  $O$ - clock pulses

Total number clock pulses =  $N$

1011



# Parallel In Parallel Out



► PIPO Configuration has only

4- input

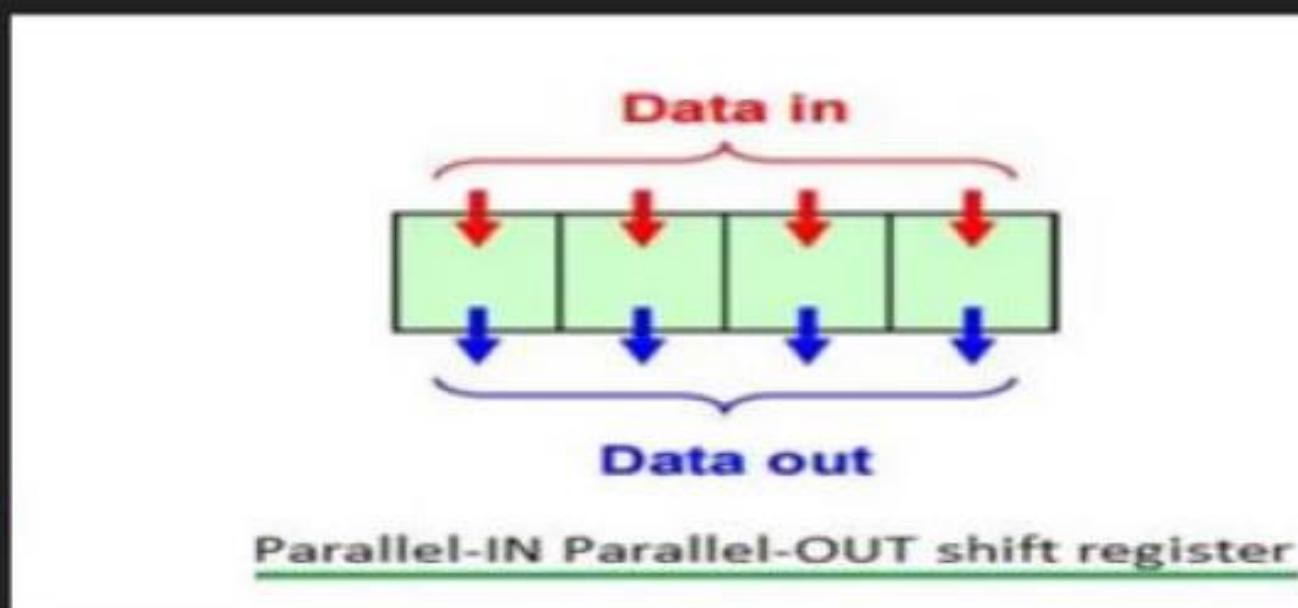
4- output

► For PIPO configuration

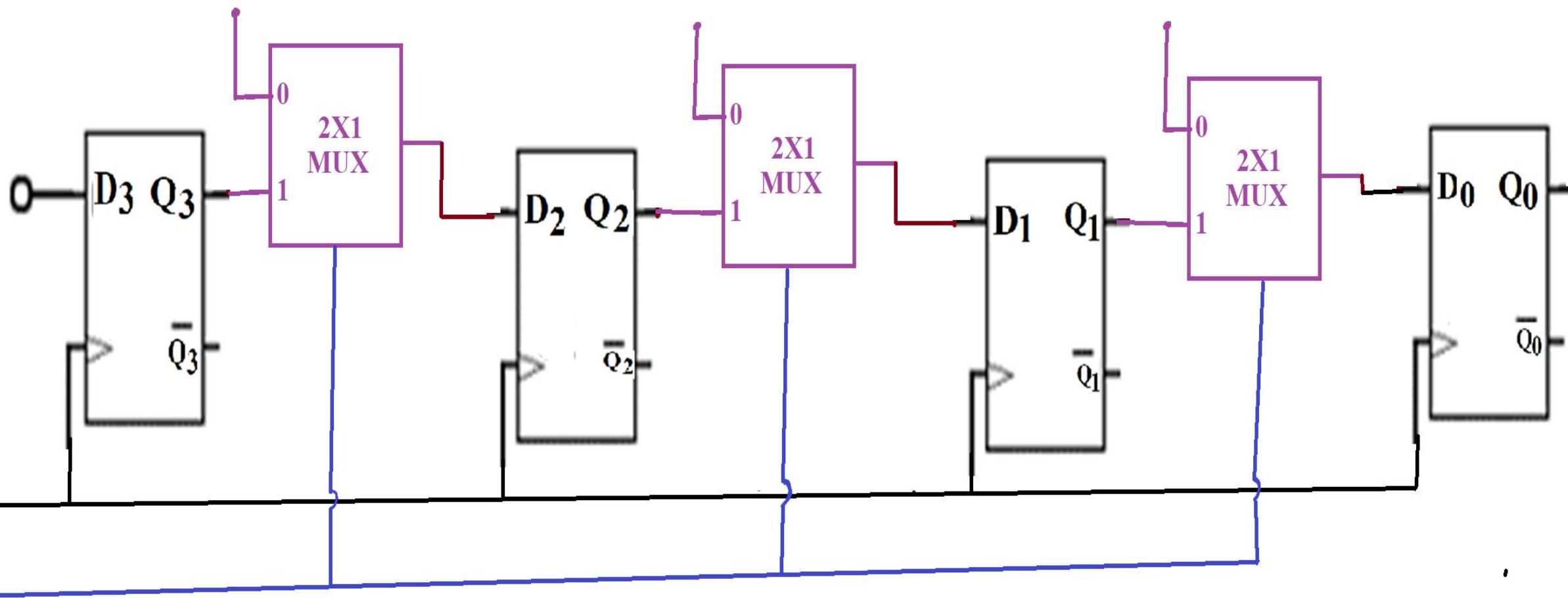
for storing = 1- Clock pulses

for retrieving = 0- Clock pulses

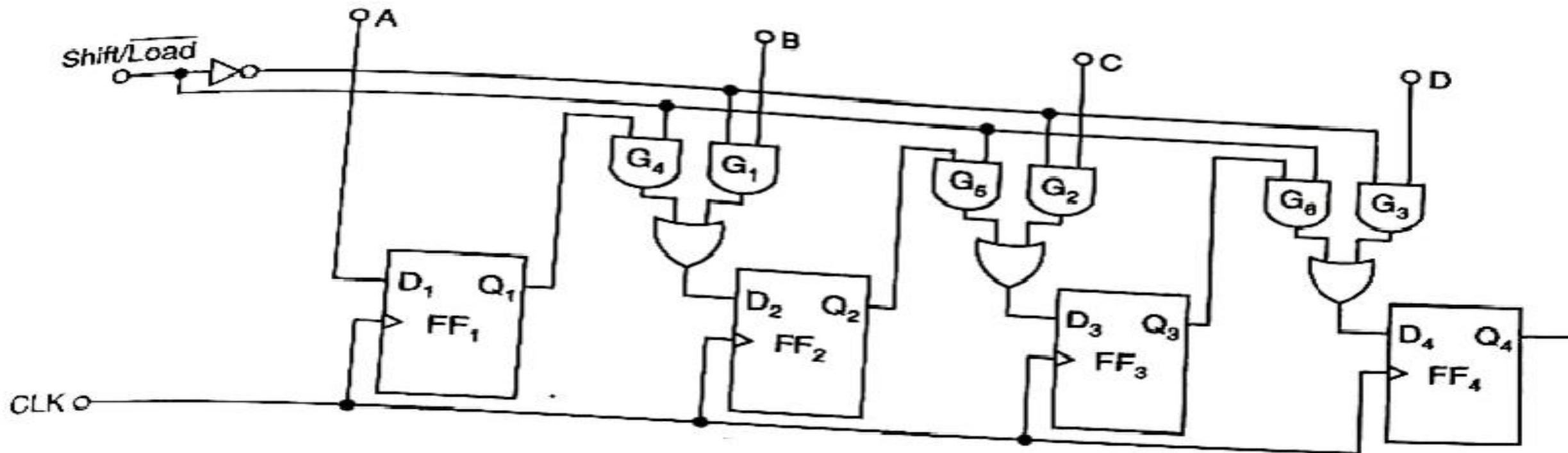
Total number clock pulses = 1



# Parallel In Serial Out



# Parallel In Serial Out

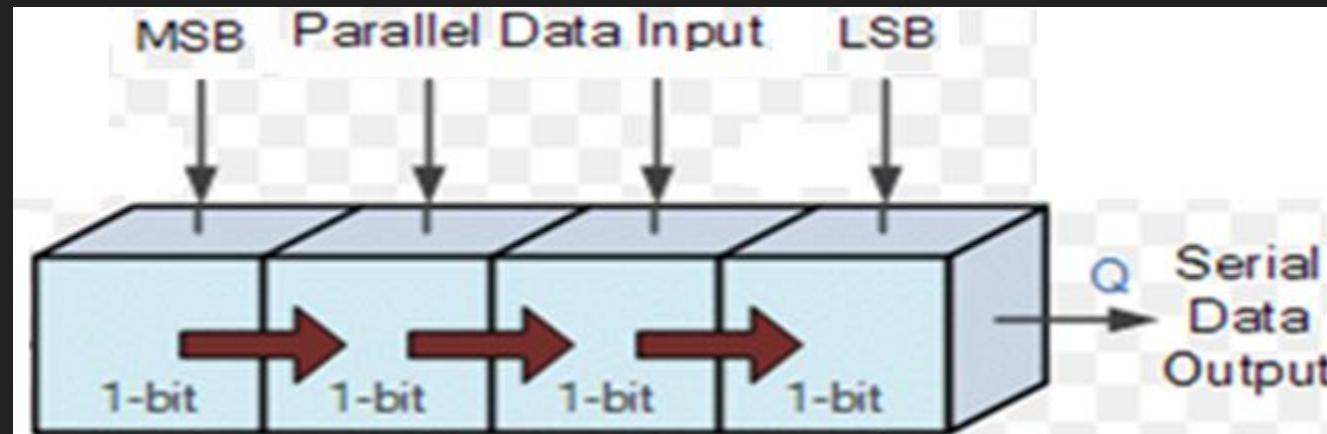


- PISO Configuration has only
  - 4- input
  - 1- output

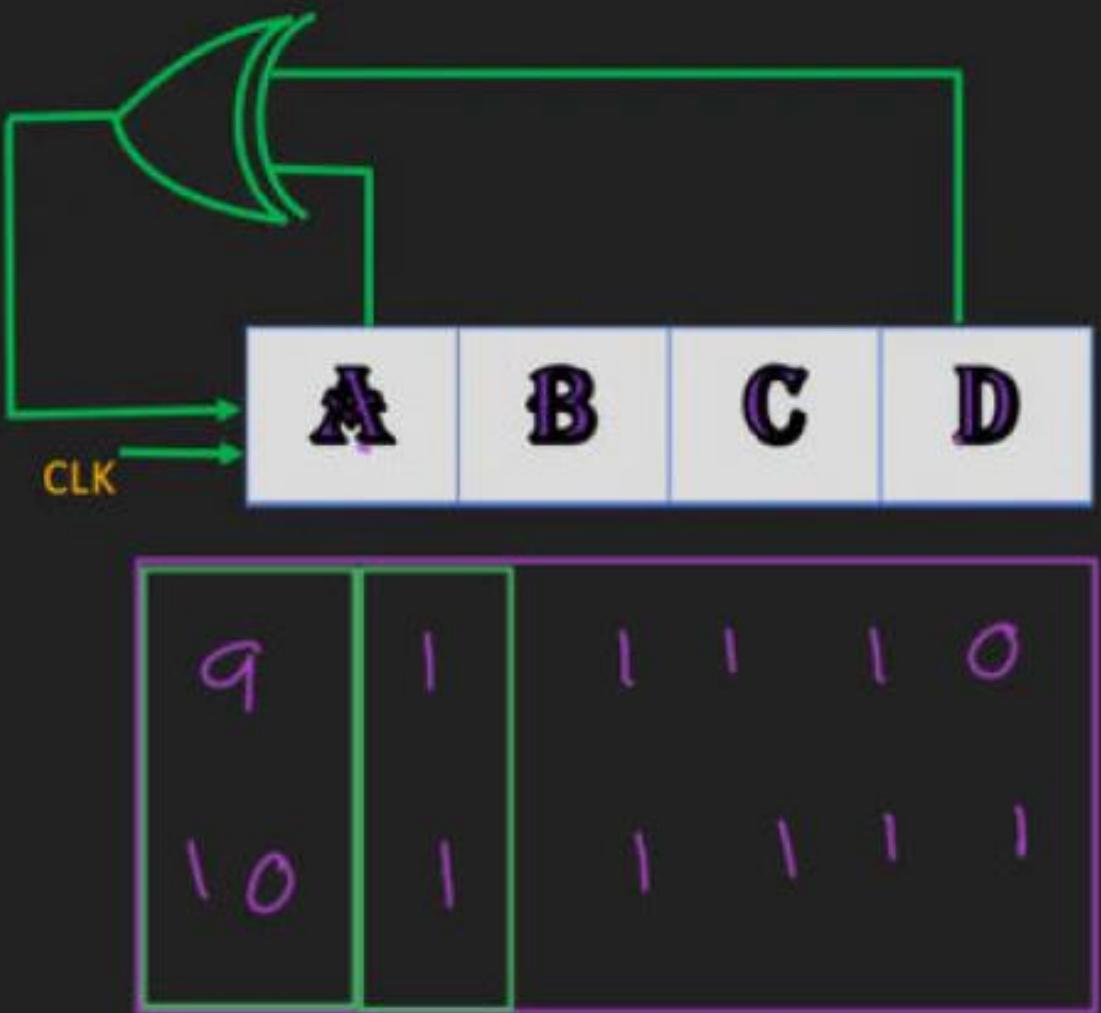
➤ For PISO configuration

for storing =  $i$  Clock pulses  
 for retrieving =  $(N-i)$  Clock pulses

Total number clock pulses =  $N$

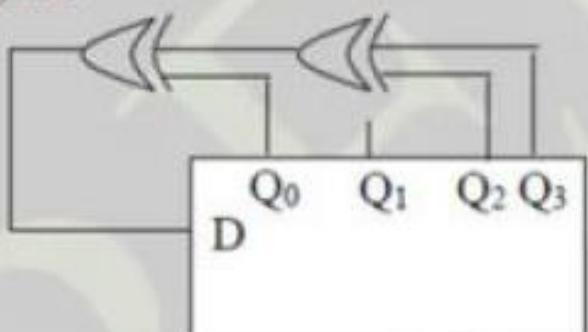


Q) A 4-bit shift register circuit configured for right shift operation  $Din \rightarrow A$ , is shown, if the present state of the shift register is  $ABCD = 1101$ , the number of clock cycles required to reach the state  $ABCD = 1111$  is ....



<u>clk</u>	<u>i/p</u>	<u>A</u>	<u>B</u>	<u>C</u>	<u>D</u>
0	x	1	1	0	1
1	0	0	1	1	0
2	0	0	0	1	1
3	1	1	0	0	1
4	0	0	1	0	0
5	0	0	0	1	0
6	0	0	0	0	1
7	1	1	0	0	0
8	1	1	1	0	0

A 4-bit shift register, which shifts 1 bit to the right at every clock pulse, is initialized to values (1000) for  $(Q_0 Q_1 Q_2 Q_3)$ . The D input is derived from  $Q_0$ ,  $Q_2$  and  $Q_3$  through two XOR gates as shown in figure. (GATE-1996)



- (a) Write the 4-bit values  $(Q_0 Q_1 Q_2 Q_3)$  after each clock pulse till the pattern (1000) reappears on  $(Q_0 Q_1 Q_2 Q_3)$ .
- (b) To what values should the shift register be initialized so that the pattern (1001) occurs after the first clock pulse?

$$i/p = \overline{Q_0} \oplus \overline{Q_2} \oplus \overline{Q_3}$$

$clk$	$i/p$
0	0 0 1 0

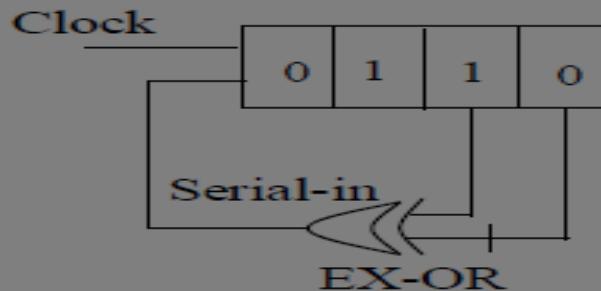
④  $\rightarrow 1001$

$clk$	$i/p$	$Q_0$	$Q_1$	$Q_2$	$Q_3$
0	x	1	0	0	0
1	1	1	1	0	0
2	1	1	1	1	0
3	0	0	1	1	1
4	0	0	0	1	1
5	0	0	0	0	1
6✓	1	1	0	0	0

The initial contents of the 4-bit series-in-parallel-out, right shift, shift register as shown in figure below are 0110. After 3 clock pulses the contents of the shift register will be

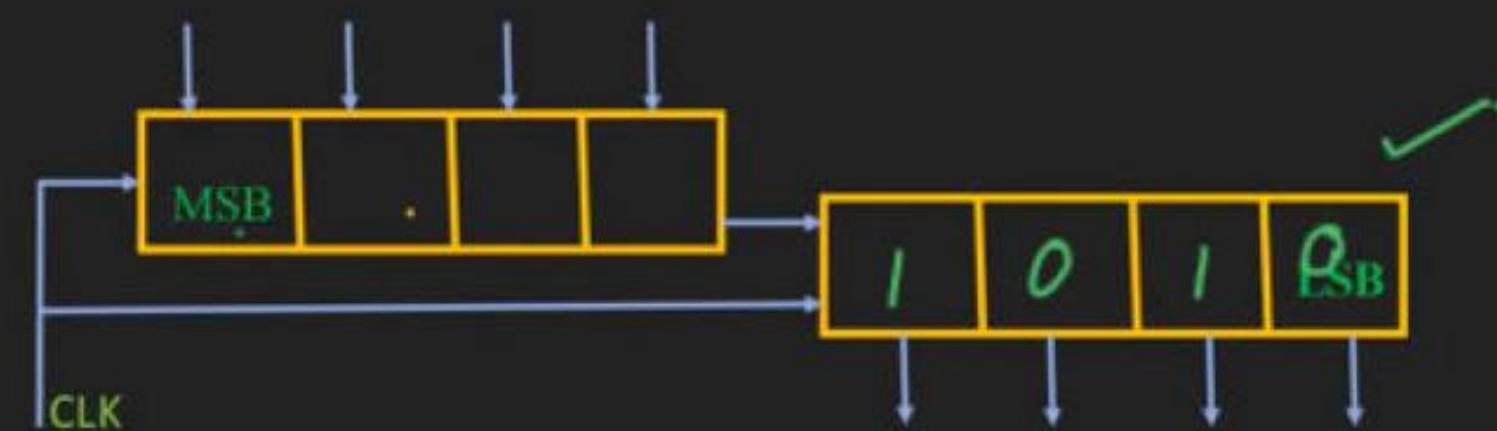
- (a) 0000
- (b) 0101
- (c) 1010
- (d) 1110

(IES-2001)  
(IES-2003)  
(IES-2004)



<u>uk</u>	✓	✓
0	0 1 1 0	
1	1 0 1 1	
2	0 1 0 1	
3	1 0 1 0	

Q) An 8-bit register is made of one 4-bit PISO register (synchronous loading) cascaded with a 4-bit SIPO register as shown in the figure below, then total number of clock pulses required to perform write and read operations for one byte is -----



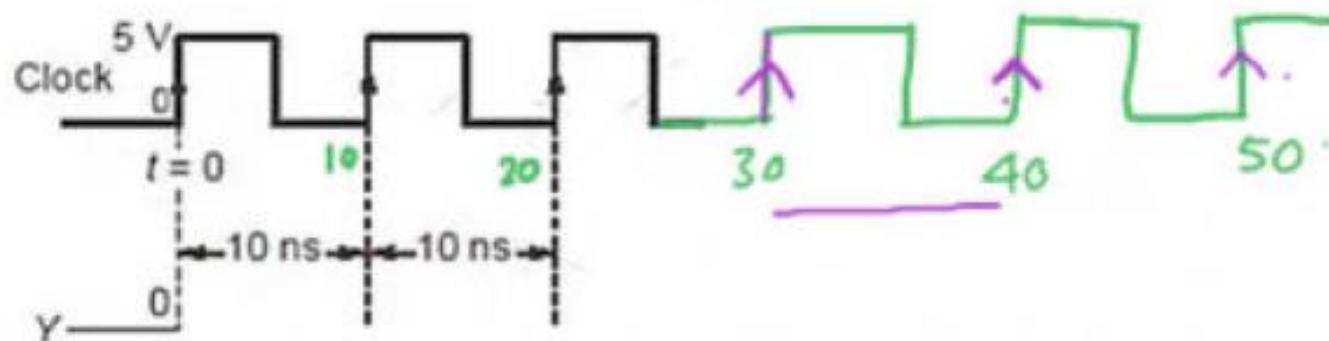
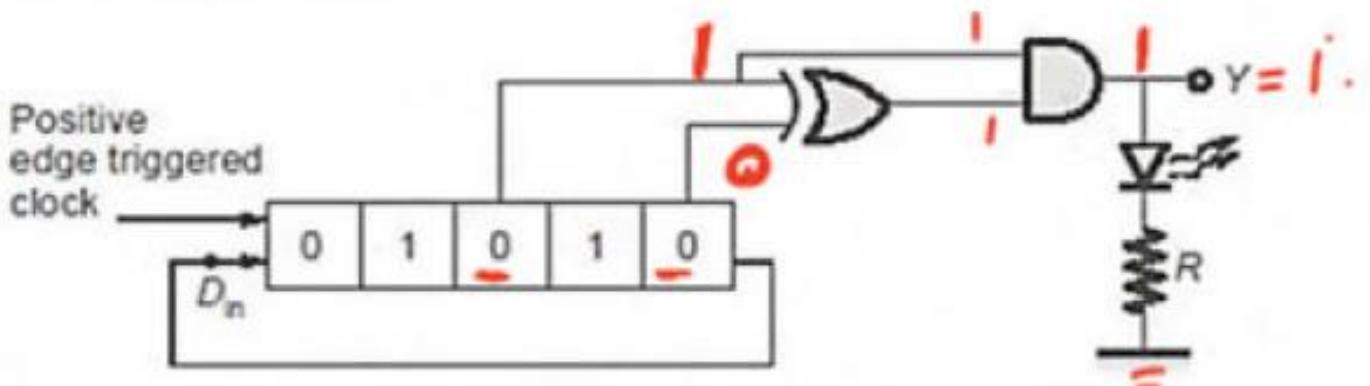
To load the data into PISO = !

To 10 10 SIPO = 4 .

To load the again into PISO = 1.

To Read the data from SIPO = 0 .

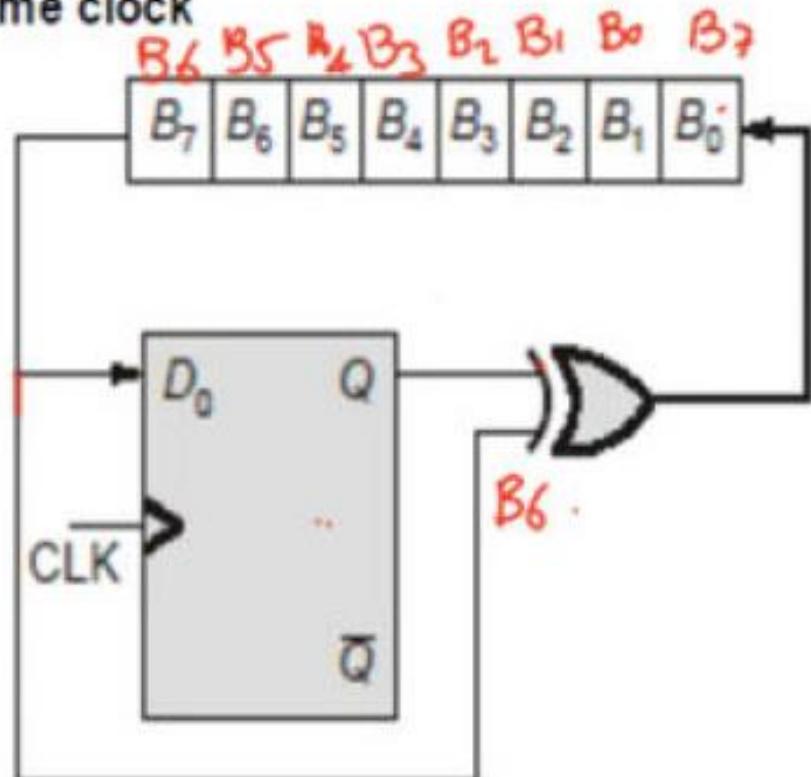
Consider a serial-in-parallel-out, right shift register circuit with initial contents as "01010" as shown in the figure. This circuit is operated with a positive edge triggered clock signal as given in figure. If +5 V and 0 V are used to represent logic-1 and logic-0 respectively, then at which of the following instances, the LED will be in ON state?



- a. 15 ns
- b. 25 ns
- c. 35 ns
- d. 45 ns

$Clk$	$Q_4$	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	1	0	1	0
(0-10)	1	0	0	0	1
(10-20)	2	1	0	0	1
(20-30)	3	0	1	0	1
(30-40)	4	1	0	0	0

An 8-bit register and D flip flop shown in figure below are synchronized with same clock



$$\begin{aligned} & B_7, (B_2 \oplus B_6) \quad (B_6 \oplus B_5) \quad (B_5 \oplus B_4) \quad (B_4 \oplus B_3) \\ & (B_3 \oplus B_2) \quad (B_2 \oplus B_1) \quad (B_1 \oplus B_0) \end{aligned}$$

Assuming the flip flop is initially cleared. The circuit act as a

- a. Binary to 2's compliment converter
- b. Binary to Gray code converter ✓
- c. Binary to 1's compliment converter
- d. Binary to Excess-3 converter

# Counters

Counters are the combination of various FFs , that generates a desired counting patterns when the clocks are applied

# Counters

Asynchronous

Binary

UP

Down

Non Binary

UP

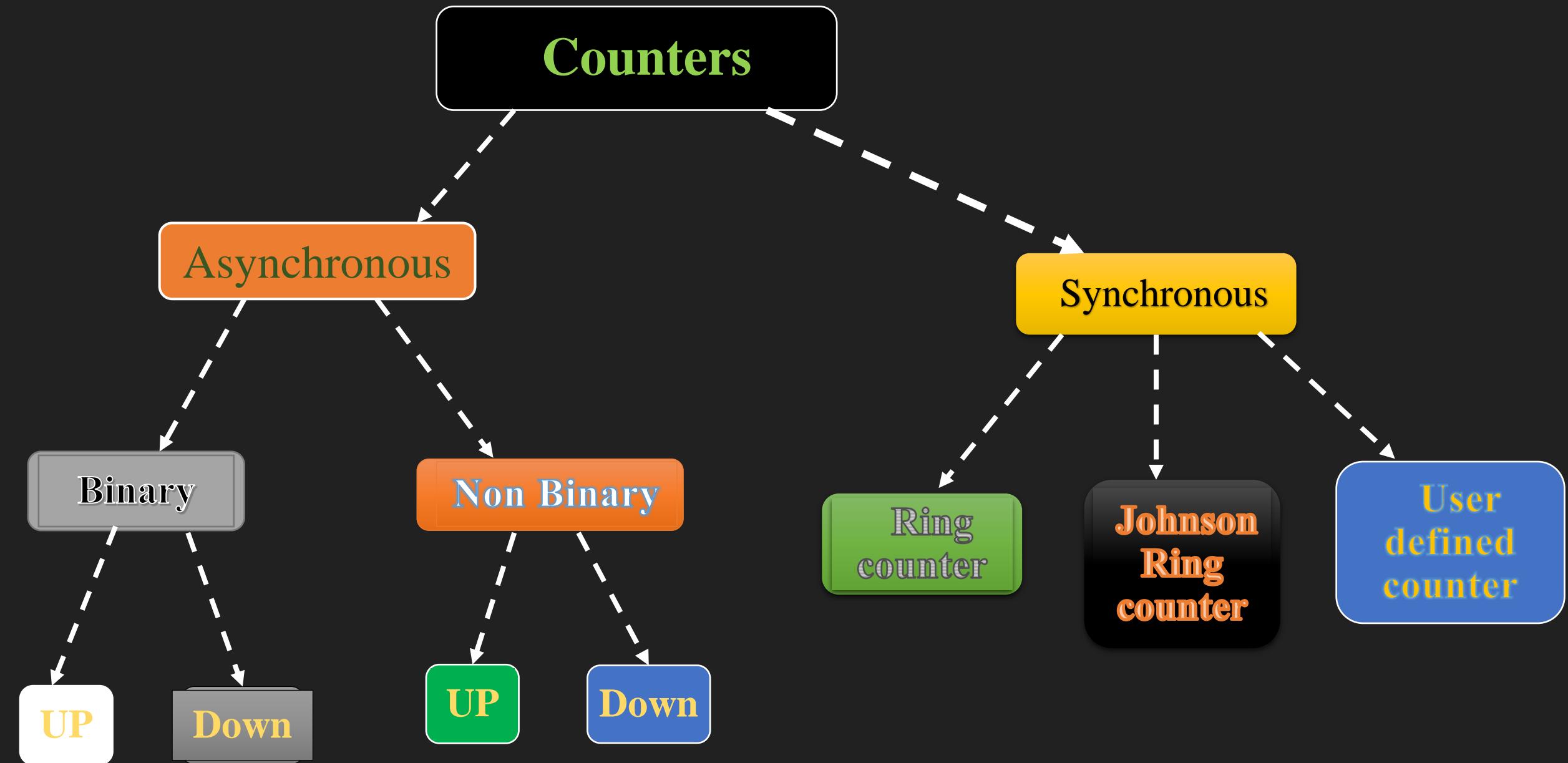
Down

Synchronous

Ring  
counter

Johnson  
Ring  
counter

User  
defined  
counter

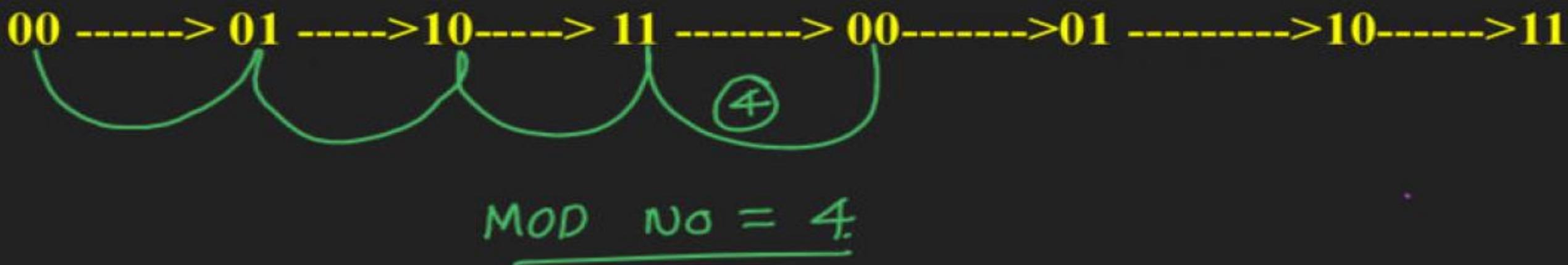


# State of a counter

Any possible output of a counter is known as its state , for a n – bit counter the maximum possible states are  $2^n$

## Modulus of a counter (Mod number )

The minimum number of clocks needed to get the counting pattern repeats is called as Modulus of a counter



AB

00

01

10

11

0 to 3

ABC

000

001

010

011

100

101

110

111

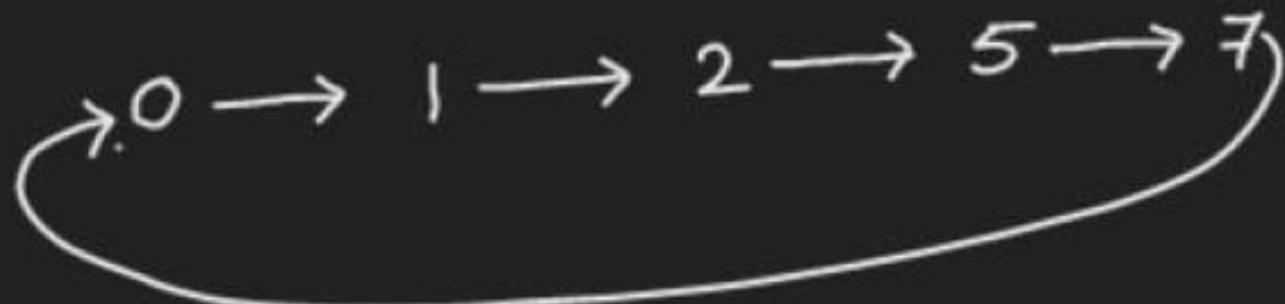
ABCD

0 to 15

0 to 7

1. The states which are counted by the counter are called as valid states .
2. The states which are not counted( skipped ) by the counter are called as invalid states .

3-bit



Valid States: 0, 1, 2, 5, 7.

Invalid States: 3, 4, 6.

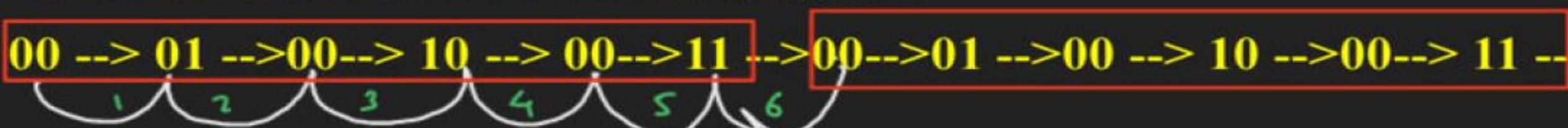
Q) What is the MOD number of the counting sequence .



MOD NO: 8

---

Q) What is the MOD number of the counting sequence .



MOD NO = 6.



# Design equation of counter

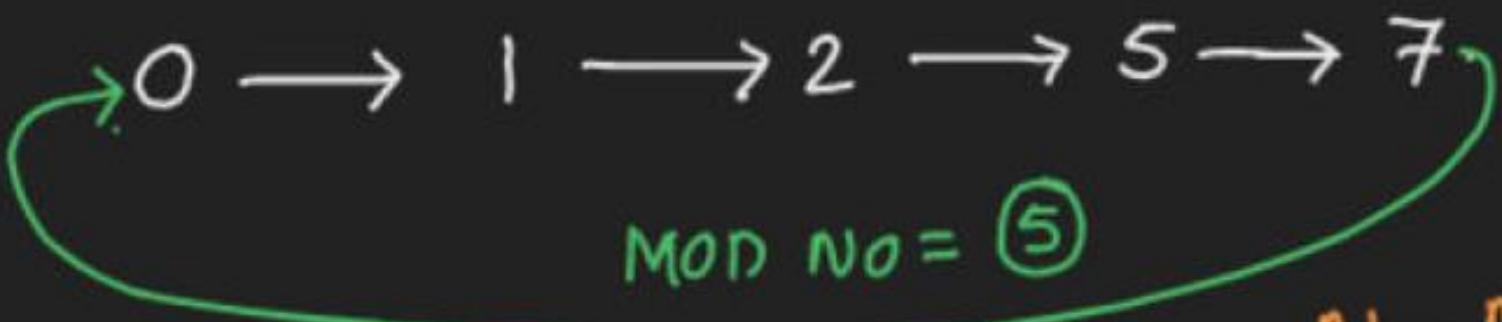
1FF -----> 2 States

2FF -----> 4 States

3FF -----> 8 States.

0 1

By using  $n$  - FFs , the maximum possible states =  $2^n$

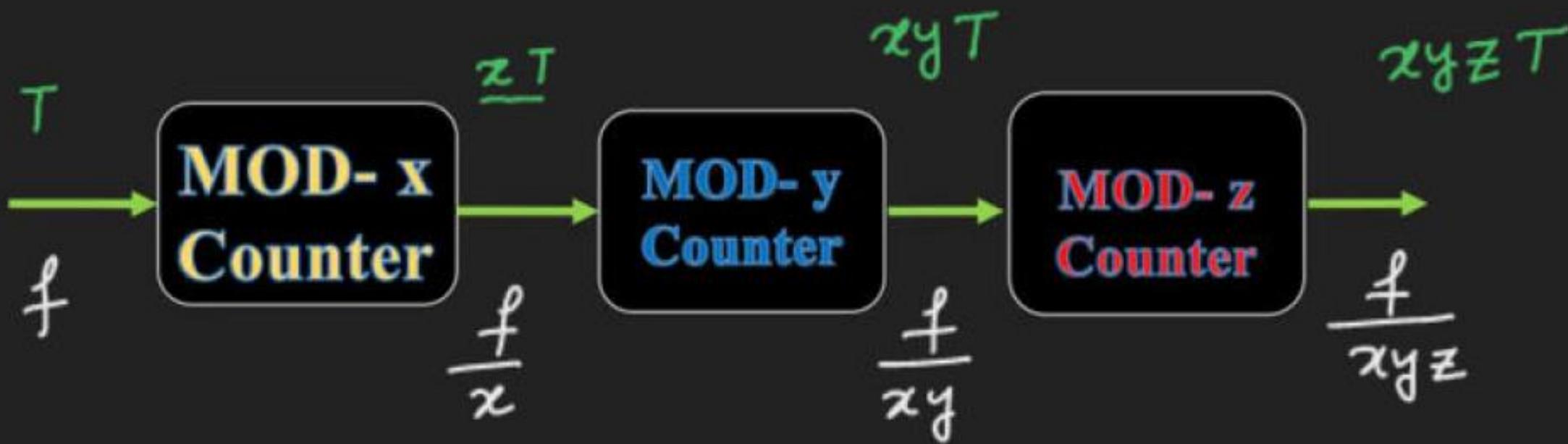
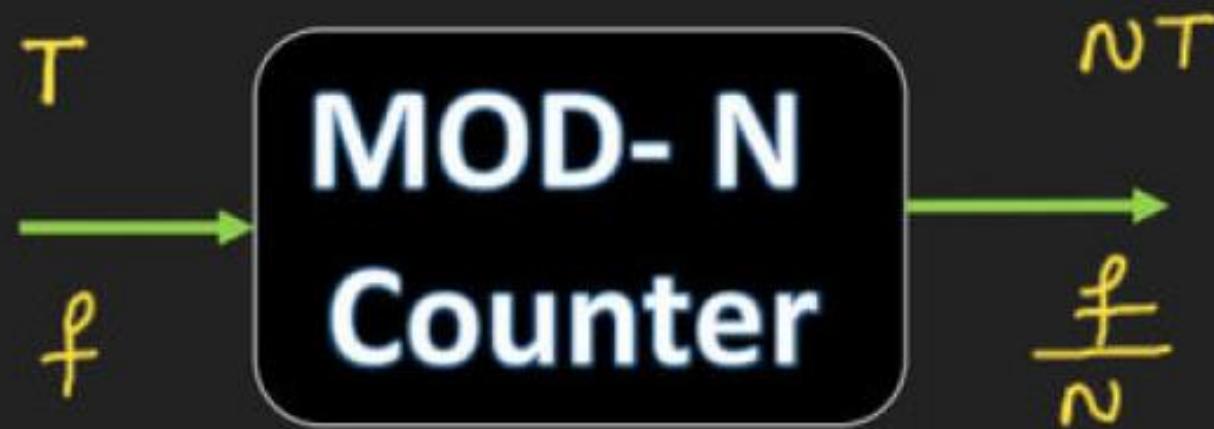


MOD No = 5

$N$  - No. of used States  
(MOD No).

$n$  - NO. of flip flop.

$$N \leq 2^n$$



## **Comparison of Asynchronous and Synchronous counters**

### **ASYNCHRONOUS COUNTERS**

1. Different flip flops are applied with different clocks

2. Design and implementation is very simple even for more number of states

3. Slower

4. Transition states are present

5. Only fixed counting sequence is possible to implement

---->up counting

---->down counting

### **SYNCHRONOUS COUNTERS**

1. All flip flops are applied with same clocks

2. Design and implementation becomes tedious and complex as the number of states increases

3. Faster compared to Asynchronous counters

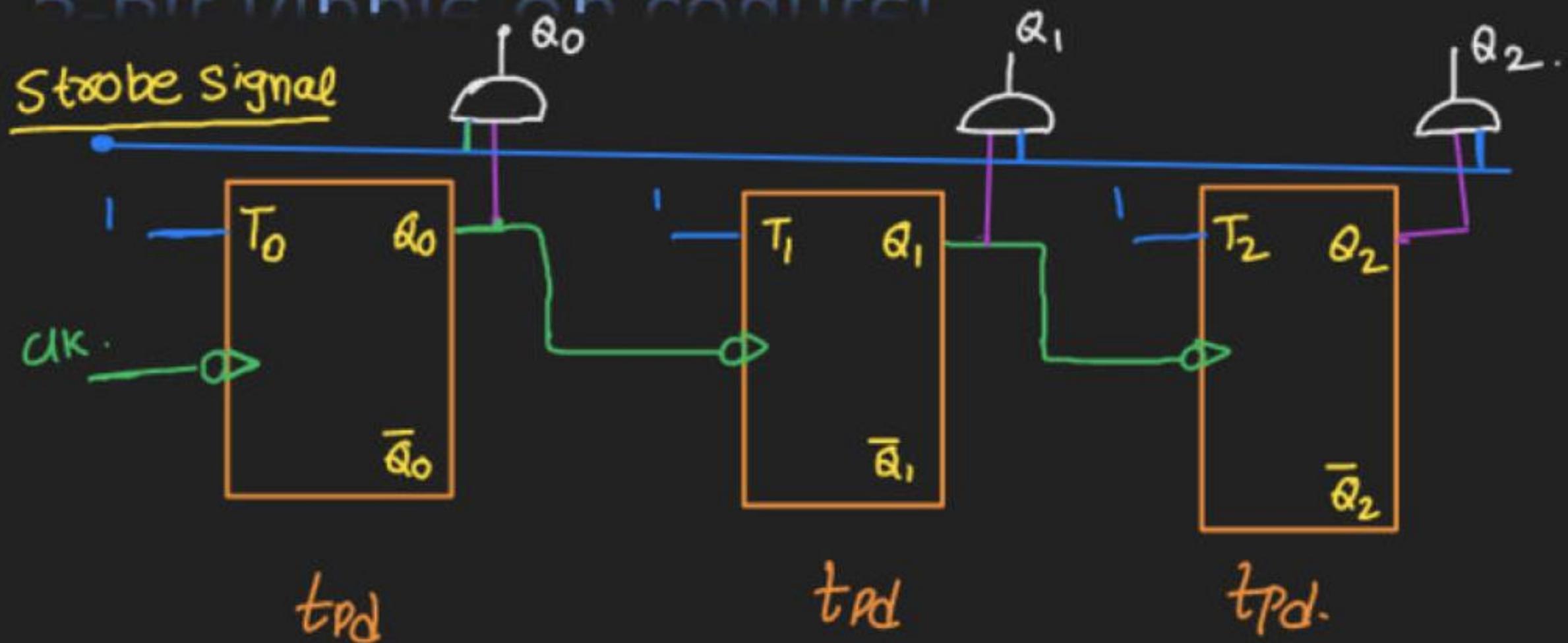
4. Transition states are not present

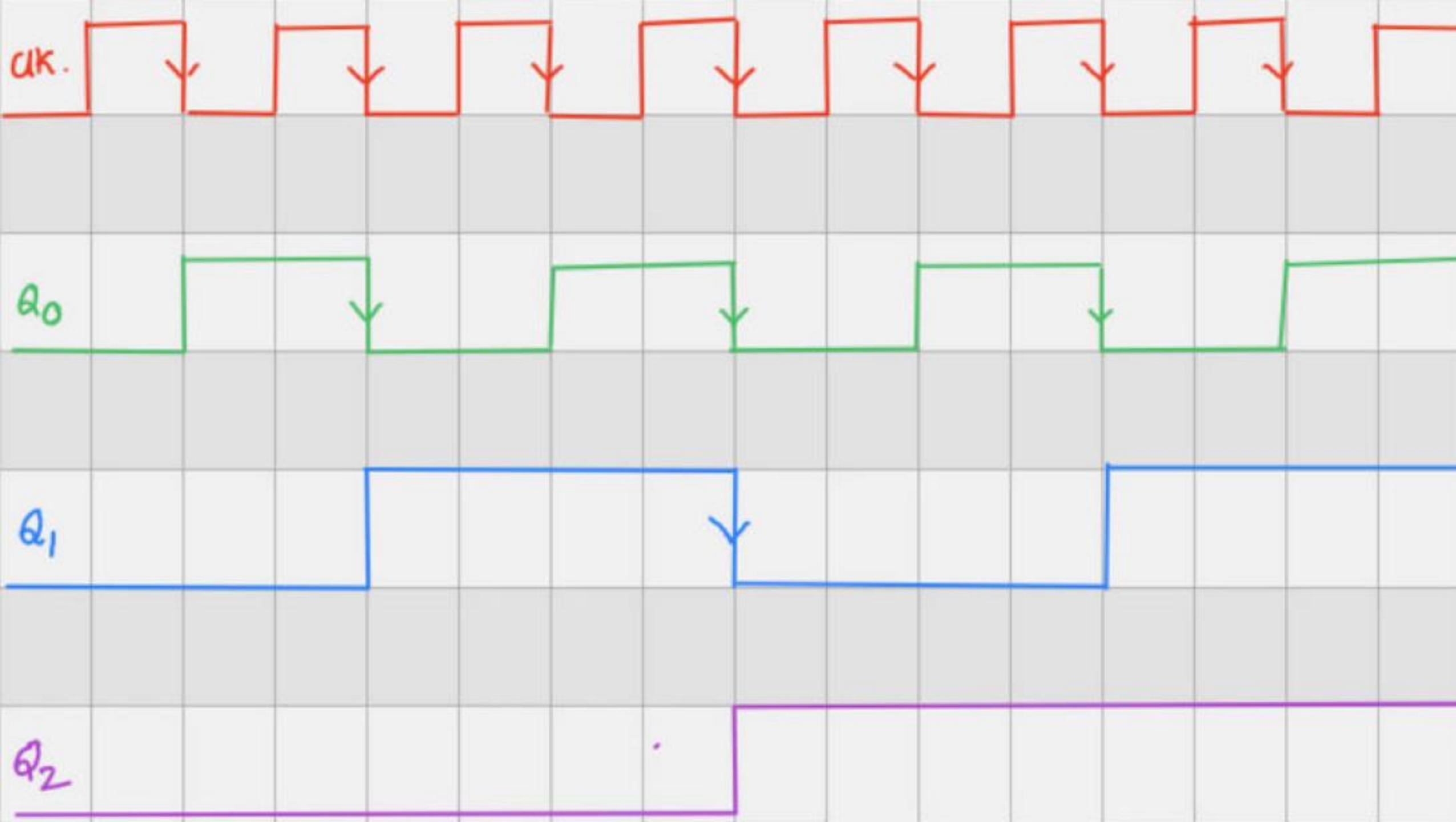
5. Any counting sequence is possible

# Asynchronous Counter

- Different FFs are applied with different clocks
- For only one FF external clock is applied ,which is LSB and output of one FF will acts as clock to next FFs
- FFs are operated in toggle mode
- Fixed counting sequence
  - 1. up counter
  - 2. down counter

# 3-Bit Ripple Up counter





*$Q_0$  – Toggles for every  $\ominus$  ve edge of clock*

*$Q_1$  – Toggles for every  $\ominus$  ve edge of  $Q_0$*

*$Q_2$  – Toggles for every  $\ominus$  ve edge of  $Q_1$*

$C/K$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0
9	0	0	1

$t_{pd}$

$2t_{pd}$

$t_{pd}$

$3t_{pd}$

$t_{pd}$

$2t_{pd}$

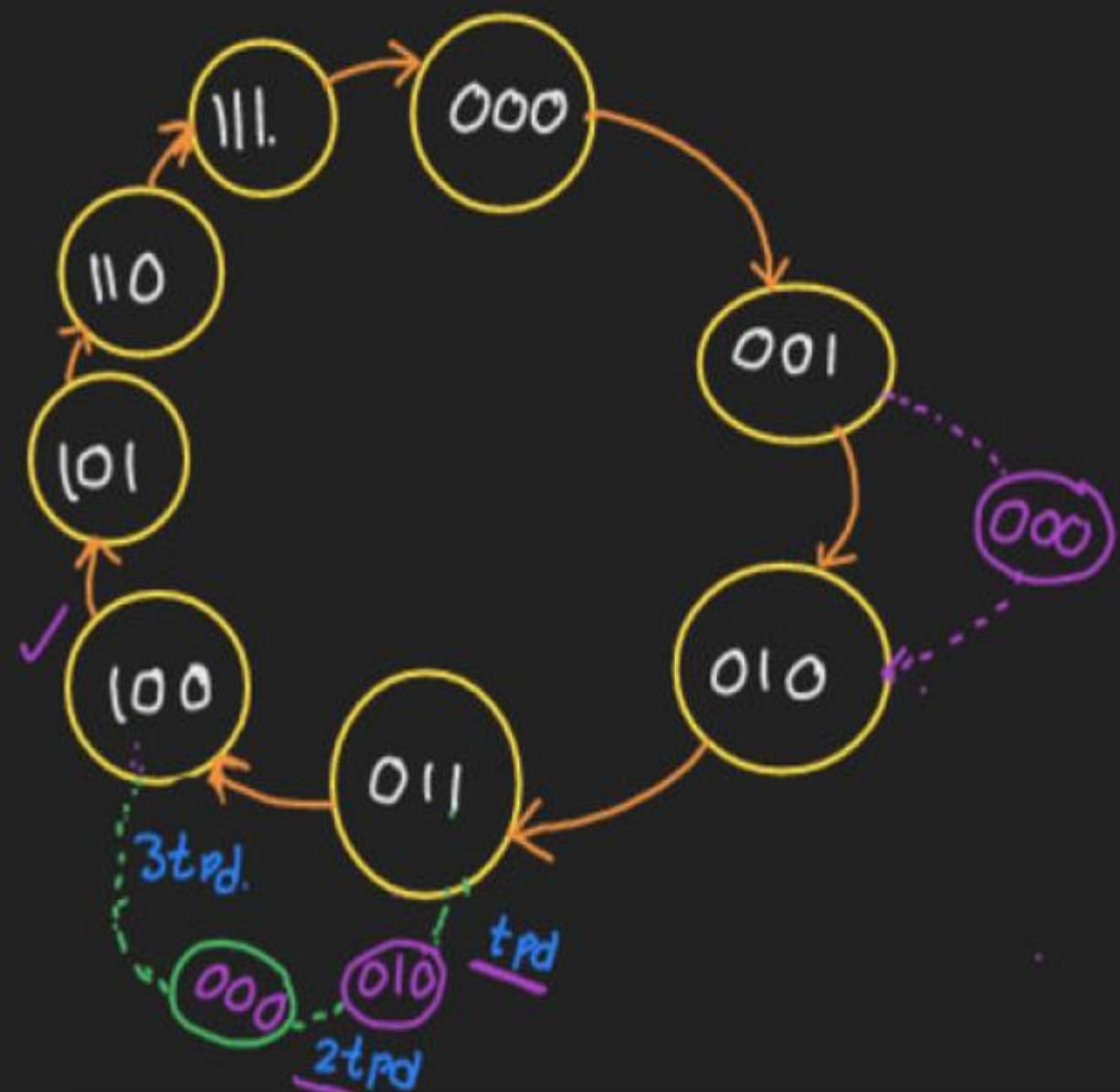
$t_{pd}$

$3t_{pd}$



UP Counter

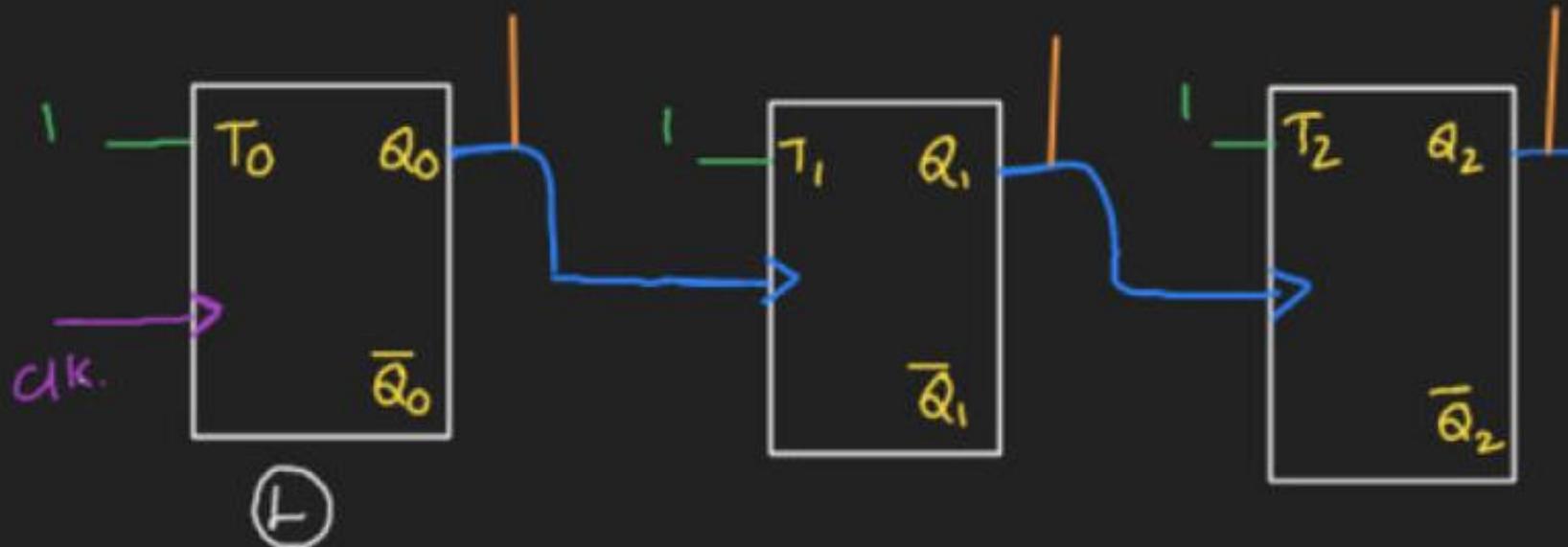
# State Diagram



- The disadvantages of the ripple counter is that transition states are present due to delay of the FF ( Decoding errors) .
- If only one FF changes its state ,then no transition states will be present , if more than one FF changes its states than transition states present.
- To avoid decoding errors strobe signal is used .
- Strobe signal is kept low for  $3t_{pd}$  , for 3- bit counter , so that transition states are not reflected, and after  $3t_{pd}$  strobe signal is made high .



# 3-Bit Ripple Down counter

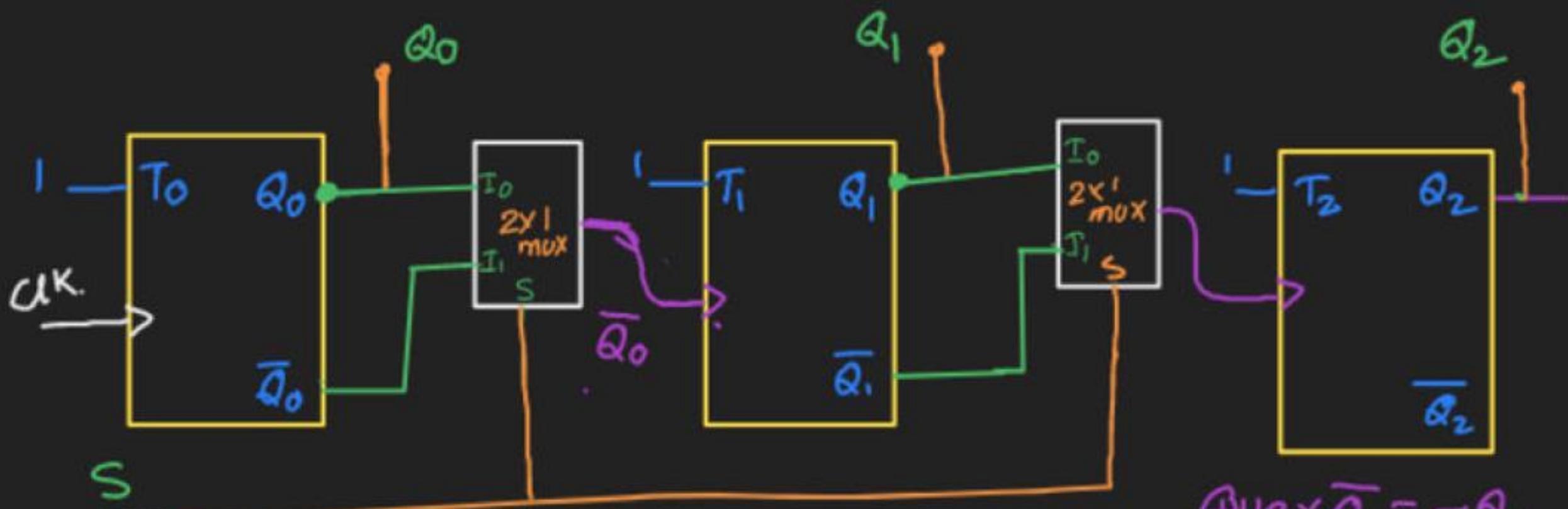


- $Q_0$  – Toggles for every  $\oplus ve$  edge of clock
- $Q_1$  – Toggles for every  $\oplus ve$  edge of  $Q_0$
- $Q_2$  – Toggles for every  $\oplus ve$  edge of  $Q_1$

MOD-8

clk	$Q_2$	$Q_1$	$Q_0$
→ 0	0	0	0
→ 1	1	1	1
2	1	1	0
3	1	0	1
→ 4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
→ 8	0	0	0
→ 9	1	1	1

# 3-Bit Ripple Up/Down counter



if S = 0, Down Counter,  
S = 1, Up Counter ✓

$$\oplus \text{ve} \times \bar{Q}_0 = -Q$$

$$\oplus \text{ve} \times Q = +Q$$

D.



$$\oplus \text{ve} \times Q = +Q$$

$\downarrow$

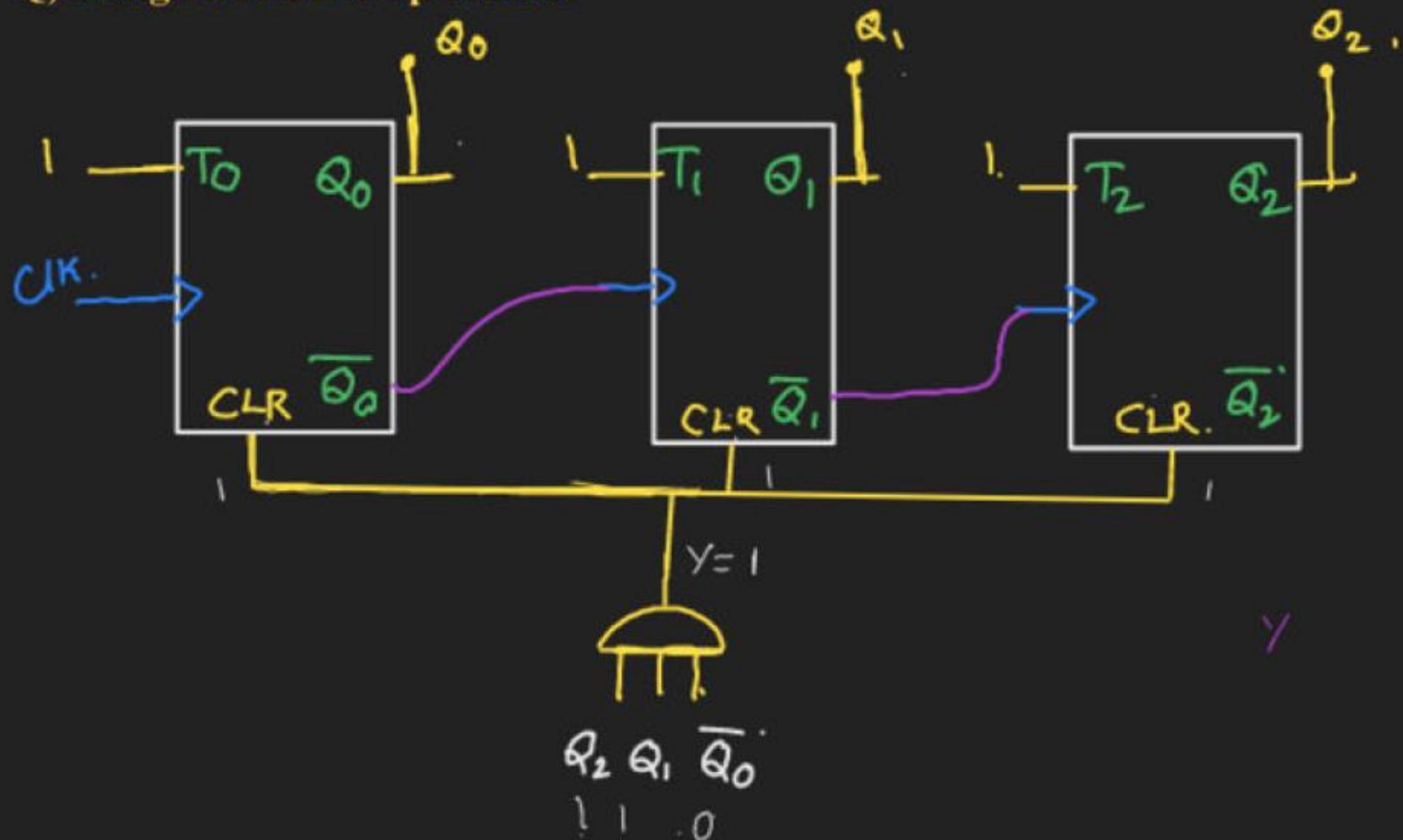
if  $S=0$ ,  $y = Q$ ,  $\rightarrow$  down Counter.

if  $S=1$ ,  $y = \bar{Q}$   $\rightarrow$  UP Counter

- In order to reduce the number of states, feedback signal is applied to counter through **CLEAR** or **PRESET** signal
- **CLEAR** control is used to Reset the Flip Flop
- **PRESET** control is used to set the Flip Flop



Q) Design a MOD-6 up counter



CK	$Q_2$	$Q_1$	$Q_0$
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
	0	0	0

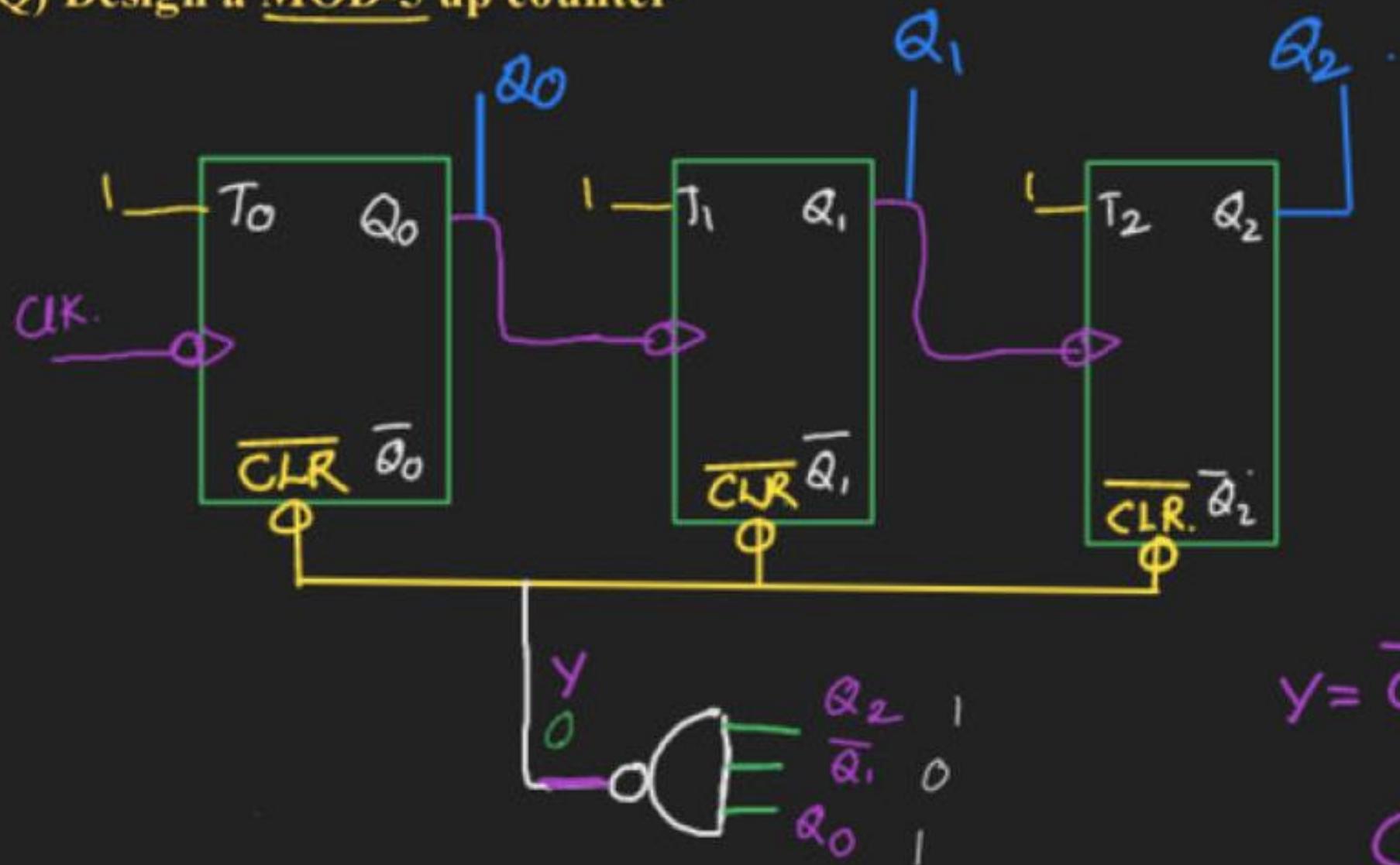
$$R = 110$$

$$R = Q_2 Q_1 \bar{Q}_0$$

$$CLR = Q_2 Q_1 \bar{Q}_0 \rightarrow \underline{\text{AND}}$$

$$\overline{CLR} = \overline{Q_2 Q_1 \bar{Q}_0} \rightarrow \underline{\text{NAND}}$$

Q) Design a MOD-5 up counter

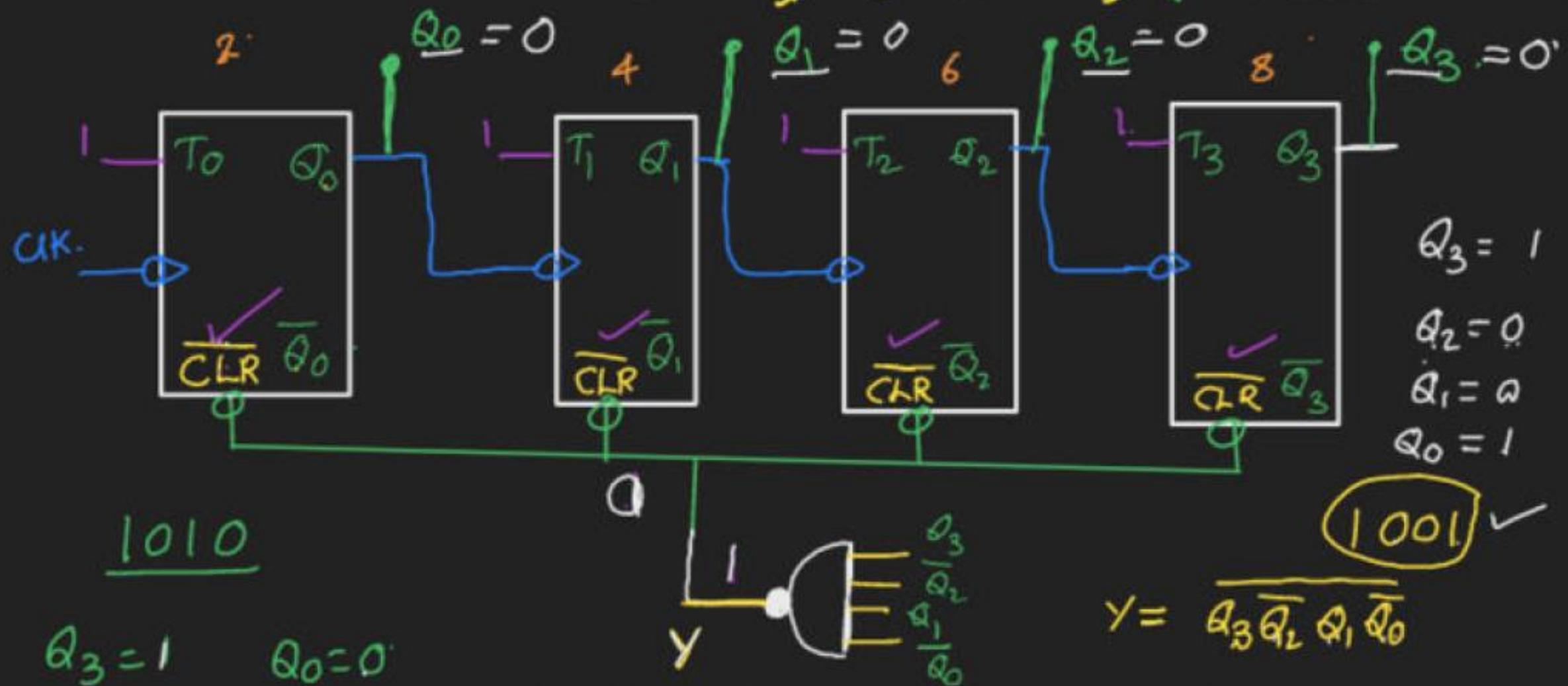


$$Y = \overline{CLR} = \overline{Q_2 \overline{Q_1} Q_0}$$

$$CLR = Q_2 \overline{Q_1} Q_0$$

1 0 1

Q) Design a BCD up counter ( $0 - 9$ ) (mod-10) (Decade counter)



$$Q_3 = 1 \quad Q_0 = 0$$

$$Q_2 = 0 \\ Q_1 = 1$$

$$Y = \overline{Q_3 \bar{Q}_2 Q_1 \bar{Q}_0} \\ Y = \overline{1(1)01} = 0$$

$$Y = \overline{1100} = \overline{0} = 1$$

$$Y = \overline{Q_3 \bar{Q}_2 Q_1 \bar{Q}_0}$$

# Delay analysis

If the delay of each FF is  $t_{pd}$ , then the overall delay for n-bit Ripple Counter.

$$\text{Delay} = n t_{pd}$$

$$T_{clk} \geqslant \text{Delay}.$$

$$T_{clk} \geqslant n t_{pd}$$

$$f_{clk} < \frac{1}{n t_{pd}}$$

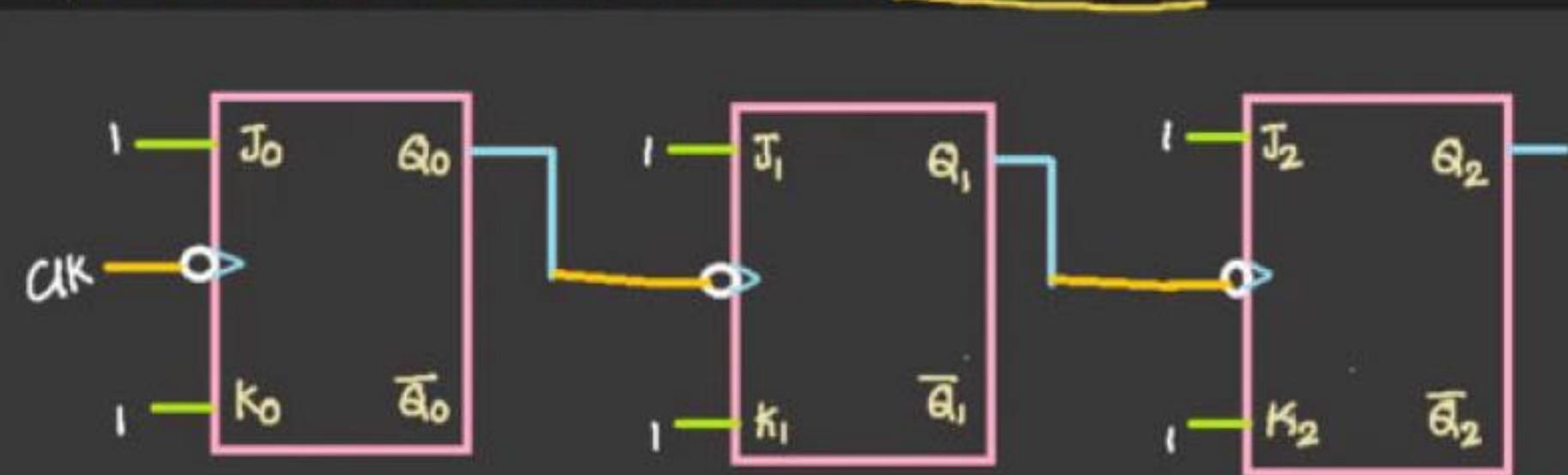
$$(f_{clk})_{\max} = \frac{1}{n t_{pd}}.$$

Q) Find

- a) MOD number
- b) Output frequency of the counter , if the input frequency is 10Mhz
- c) if the delay of each FF is 50 ns , then the maximum frequency of the clock
- d) state of the counter after 500 clocks if the initial state is 100

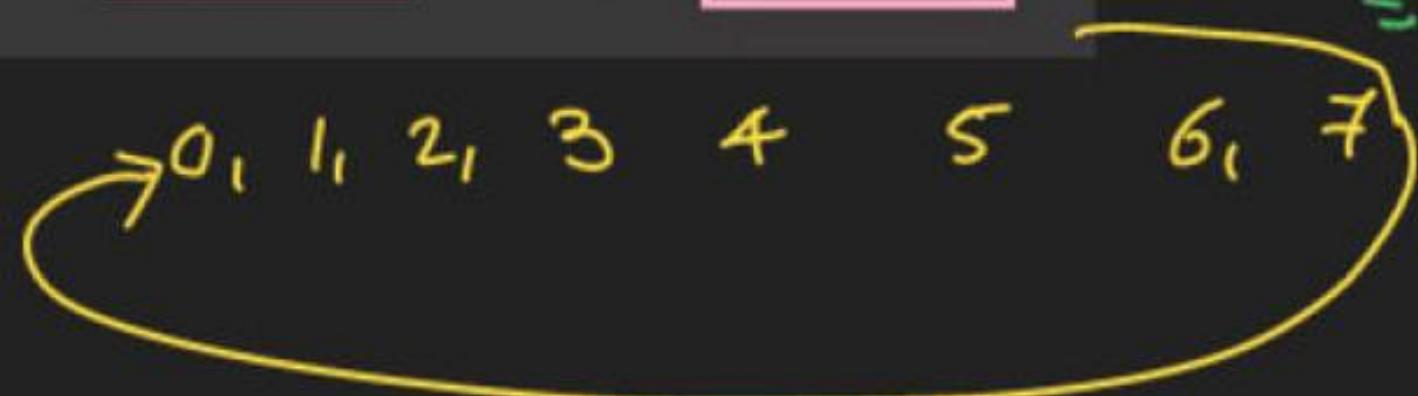
MOD - 8

UP Counter



$$f_{out} = \frac{f_{clk}}{Mod.}$$
$$= \frac{5 \times 10^6}{84}$$

1.25 MHz



$$\text{Delay} = n \cdot t_{pd} = 3(50 \times 10^{-9})$$

$$T_{dK} > 150 \text{ ns.}$$

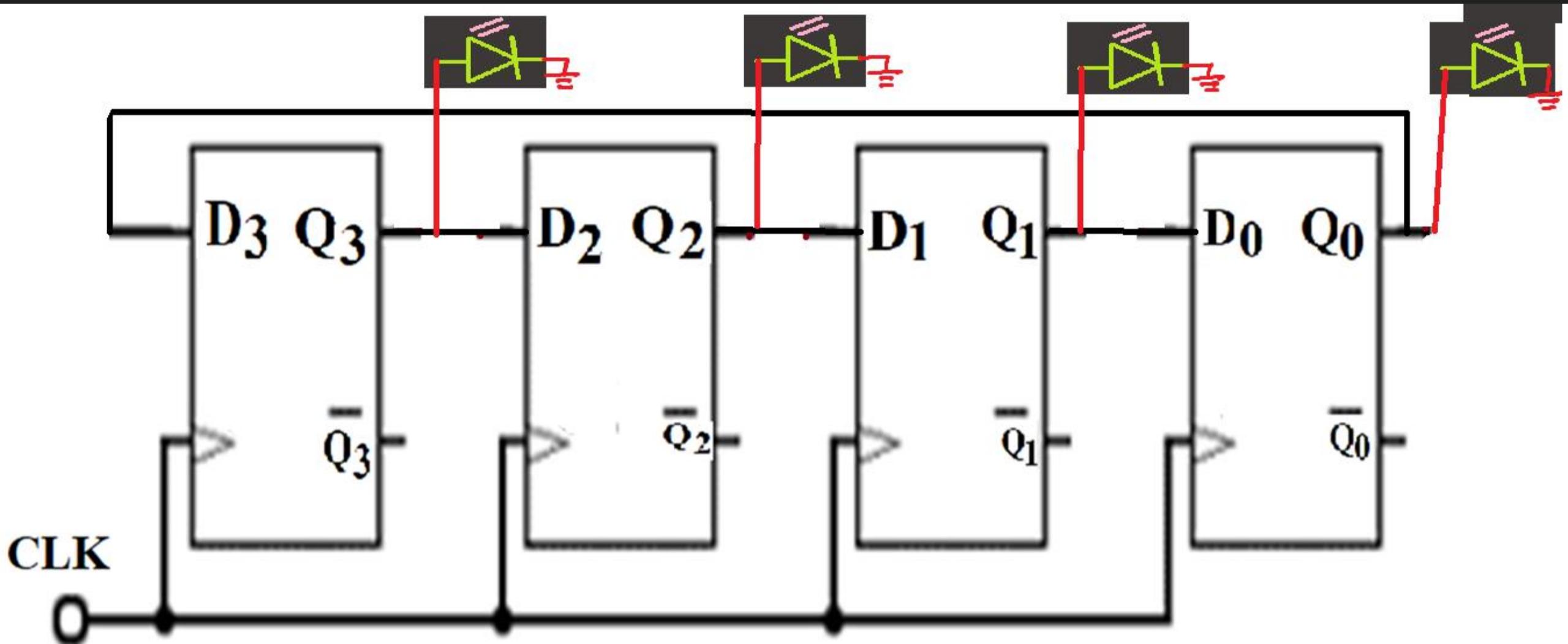
$$(f_{dK}) < \frac{1}{150 \times 10^{-9}}$$

$$(f_{dK})_{\max} = \frac{1 \times 10^9}{150} = 6.6 \times 10^6 \text{ Hz.}$$

$Q_K$	$Q_2 \ Q_1 \ Q_0$	
<u>0</u>	<u>1 0 0</u>	
$8^{th}$ .	1 0 0	
$8 \times 2$ .	1 0 0	
$8(3)$	1 0 0	
$\underline{8(62) = 496.}$	1. 0 0	
		$\begin{array}{r} 8 ) 500 ( 62 \\ \underline{48} \\ 20 \\ \underline{16} \\ ④ \checkmark \end{array}$
		$497 \rightarrow 101$
		$498 \rightarrow 110$
		$499 \rightarrow 111$
		$500 \rightarrow \underline{0 \ 00} \rightarrow \underline{\text{Any}}$

# Synchronous Counter

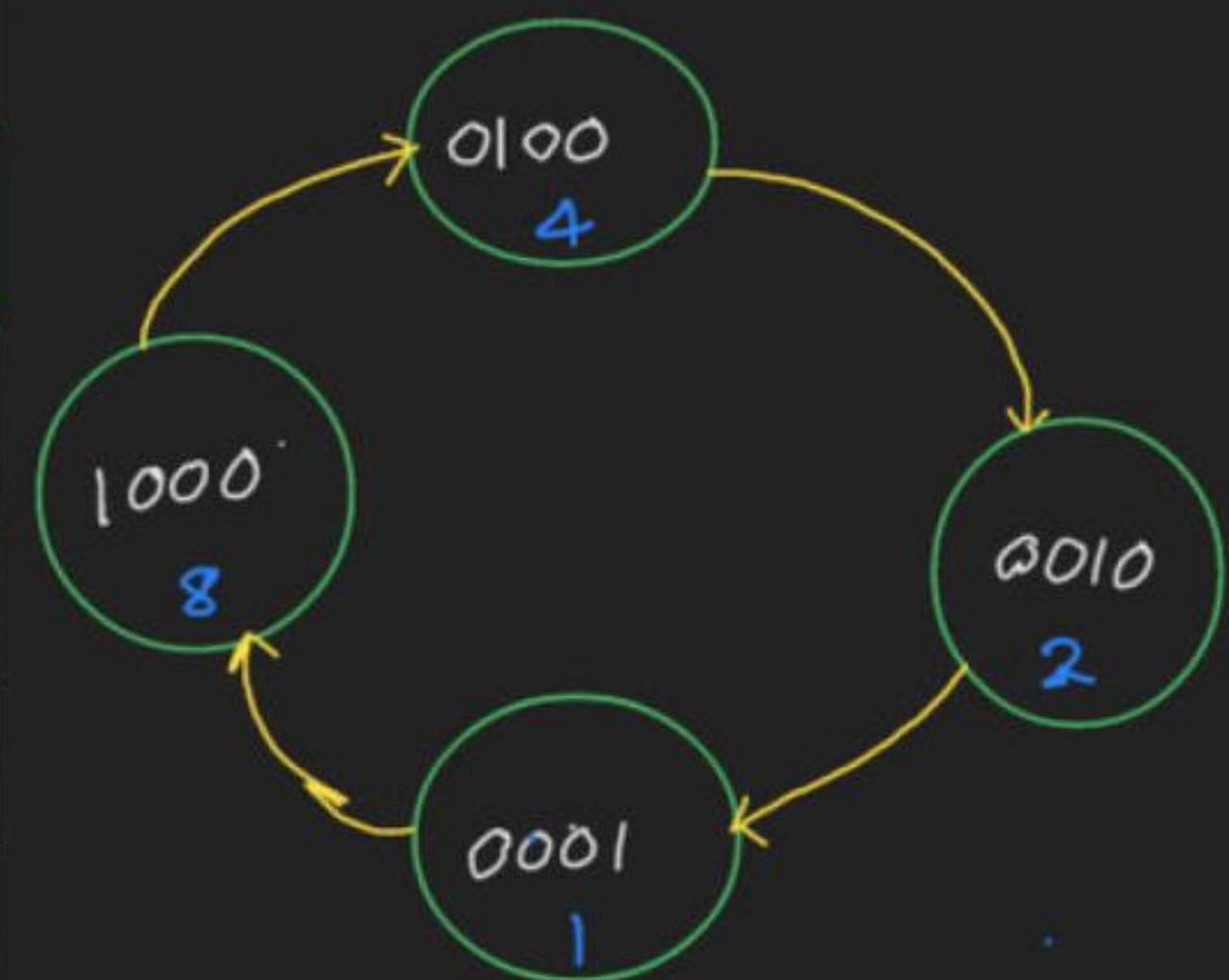
# 4-Bit Ring Counter



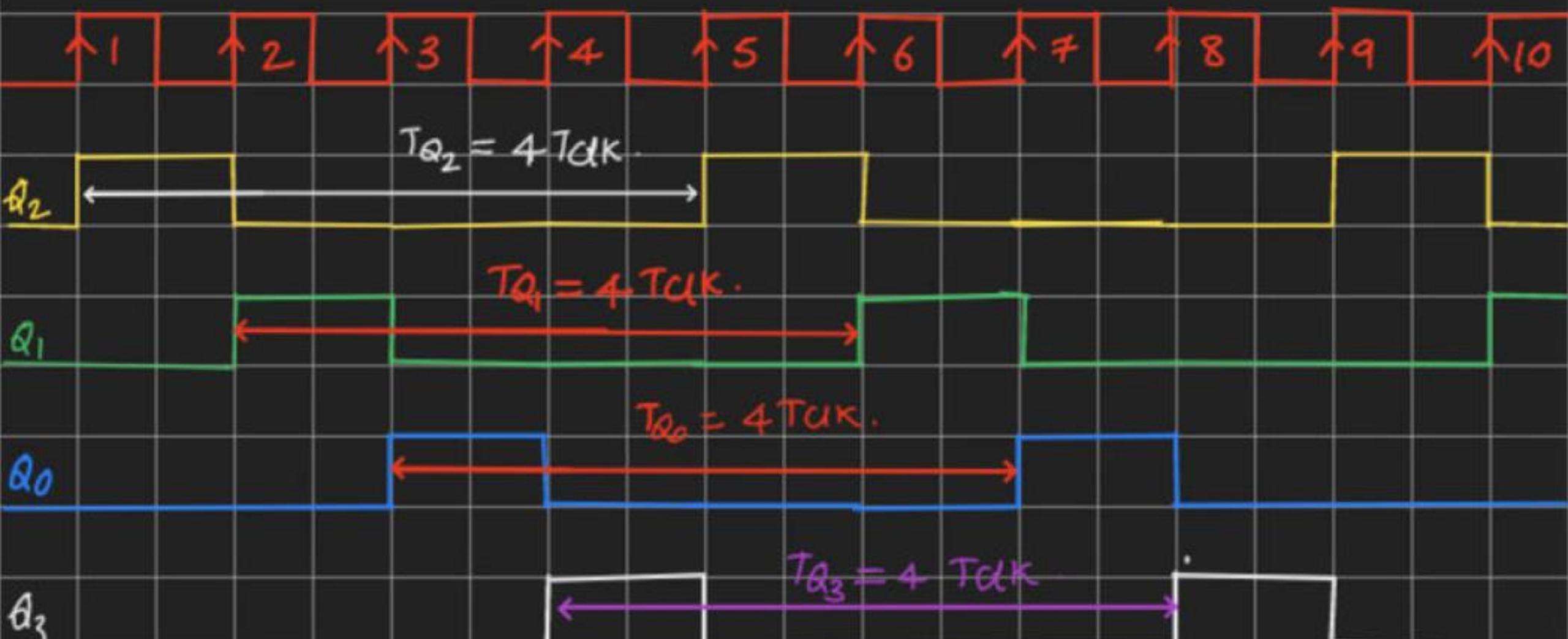
- Ring counter is a synchronous counter , it is a shift register in which last FF output is connected to the first FF output
- In ring counter only one FF output is logic ‘1 ‘ and it will rotate with clock
- Ring counter performs right shift operation



## State Diagram



# Timing Diagram



# Repeating pattern

$$\text{Duty cycle} = \frac{T_{on}}{\tau} = \frac{1}{4}.$$

$Clk$	$Q_0$
1	0
2	0
3	1
4	0

$Clk$	$Q_1$
1	0
2	1
3	0
4	1

$Clk$	$Q_2$
1	1
2	0
3	0
4	0

$Clk$	$Q_3$
1	0
2	0
3	0
4	1

$$T_{Q_0} = 4 T_{Clk}$$

$$f_{Q_0} = \frac{f_{Clk}}{4}$$

$$D = \frac{1}{4} = 25\%$$

$$T_{Q_1} = 4 T_{Clk}$$

$$f_{Q_1} = \frac{f_{Clk}}{4}$$

$$D = 25\%$$

$$T_{Q_2} = 4 T_{Clk}$$

$$f_{Q_2} = \frac{f_{Clk}}{4}$$

$$D = 25\%$$

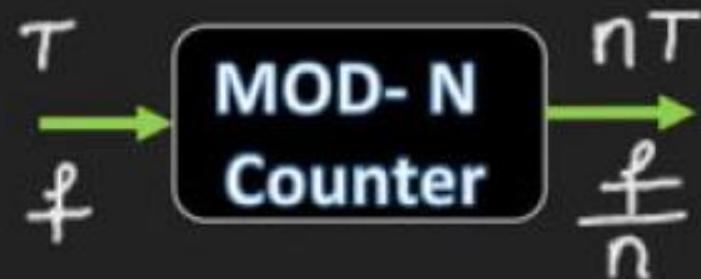
$$T_{Q_3} = 4 T_{Clk}$$

$$f_{Q_3} = \frac{f_{Clk}}{4}$$

$$D = 25\%$$

# For n-bit Ring counter

- Number of used states =  $n$
- Number of unused states =  $2^n - n$



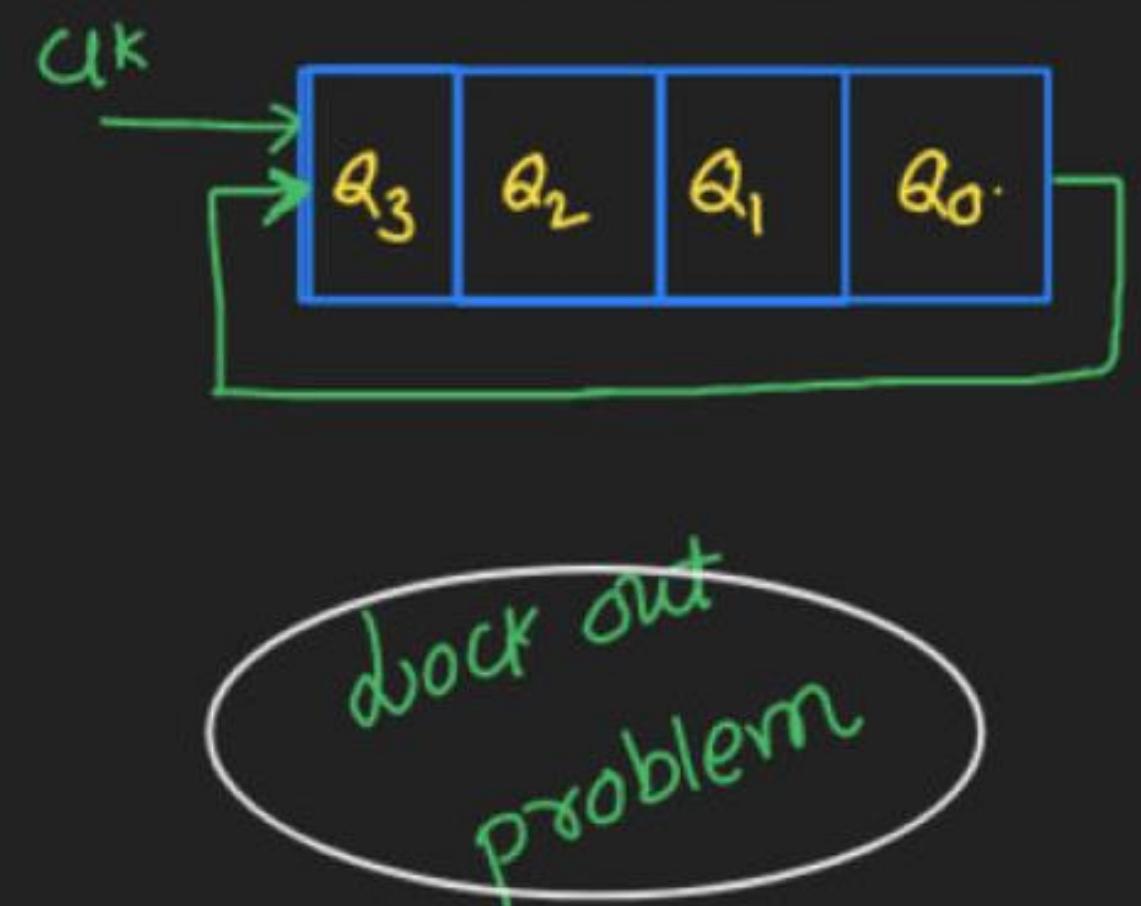
- The phase shift between successive wave form =  $\frac{360}{n}$
- If the delay of each Flip Flop is  $t_{pd}$ , then  $T_{clk} \geq t_{pd}$ .
- If the Flip Flops are having different delay then,  $T_{clk} \geq (t_{pd})_{max}$

# For Ring counter

Used states : 1 , 2, 4, 8

Unused states : 0, 3,5,6,7,9,10,11,12,13,14,15

Q) What happens if the Ring counter will enter into any of its unused states



$CLK.$	$Q_3$	$Q_2$	$Q_1$	$Q_0$	
0	1	1	0	0	$\rightarrow 12$
1	0	1	1	0	$\rightarrow 6$
2	0	0	1	1	$\rightarrow 3$
3	1	0	0	1	$\rightarrow 9$
4	1	1	0	0	$\rightarrow 12$

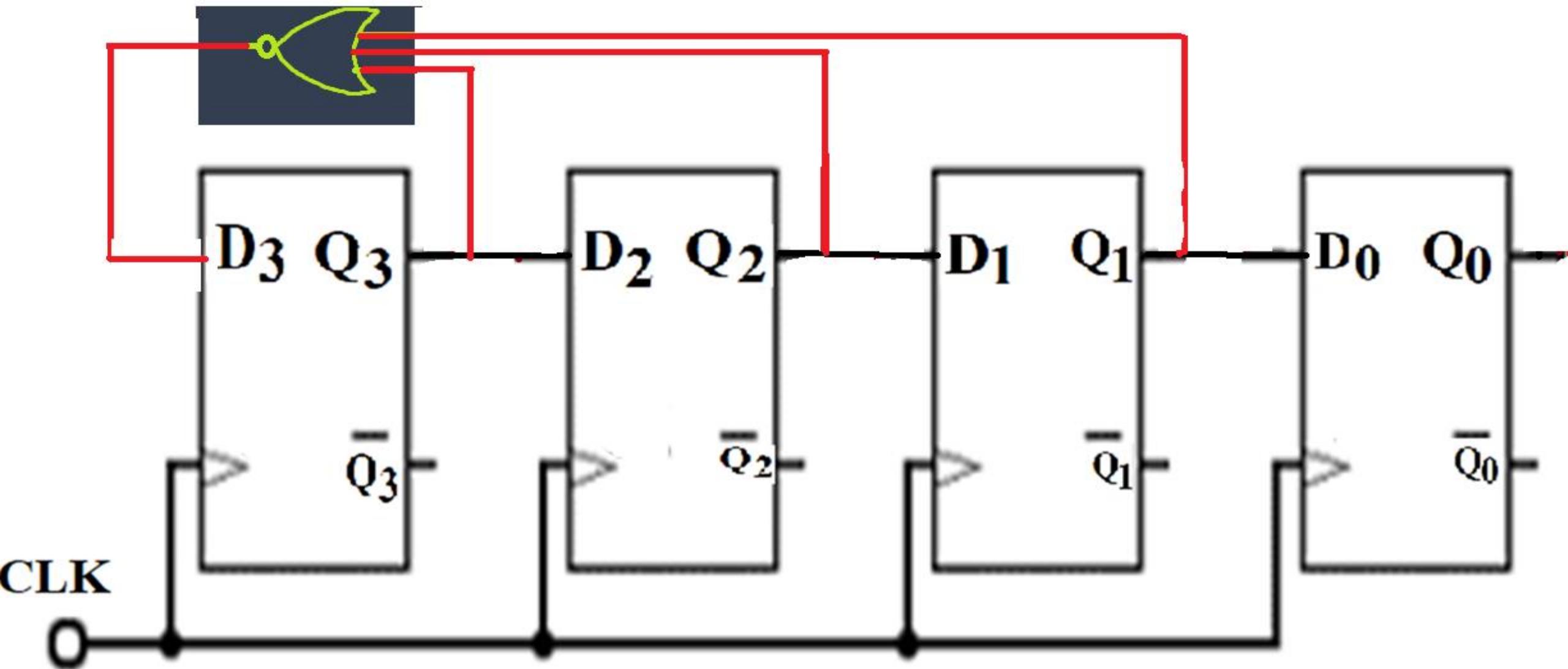
# Advantage

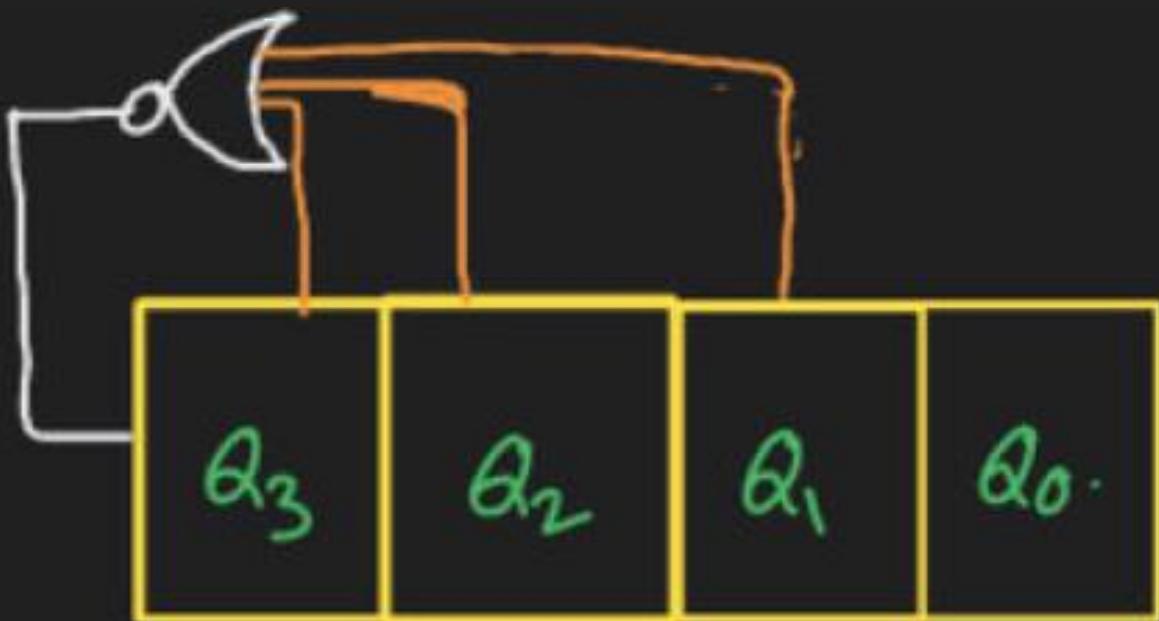
Decoding logic of ring counter is simple and does not require any external logic circuit .

## Draw back of Ring counter

- If all the outputs of FFs initially zero , then the Ring counter does not start .
- If more than one FF outputs' are high initially , then the ring counter enters into unused state and never come out of the unused state , this is called as **Lock out problem** .

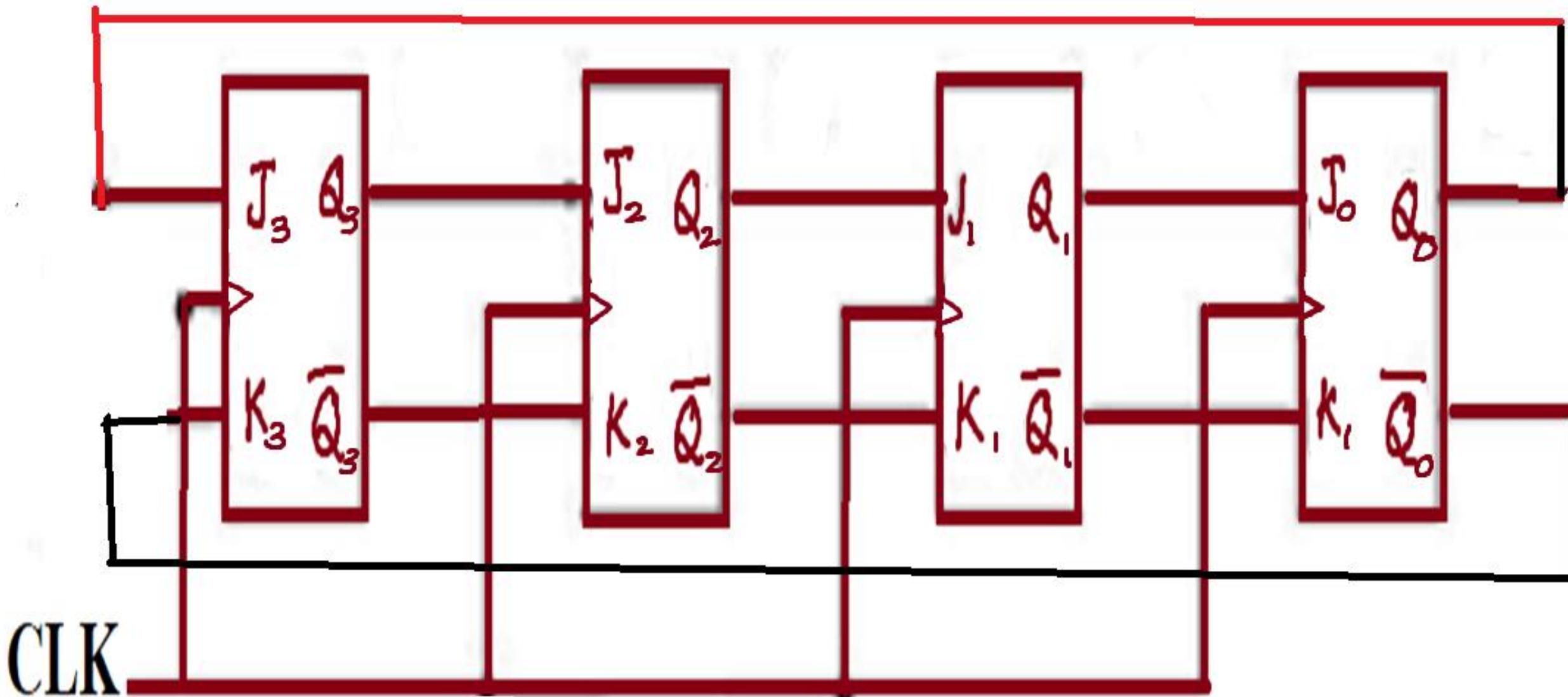
# Self starting Ring counter



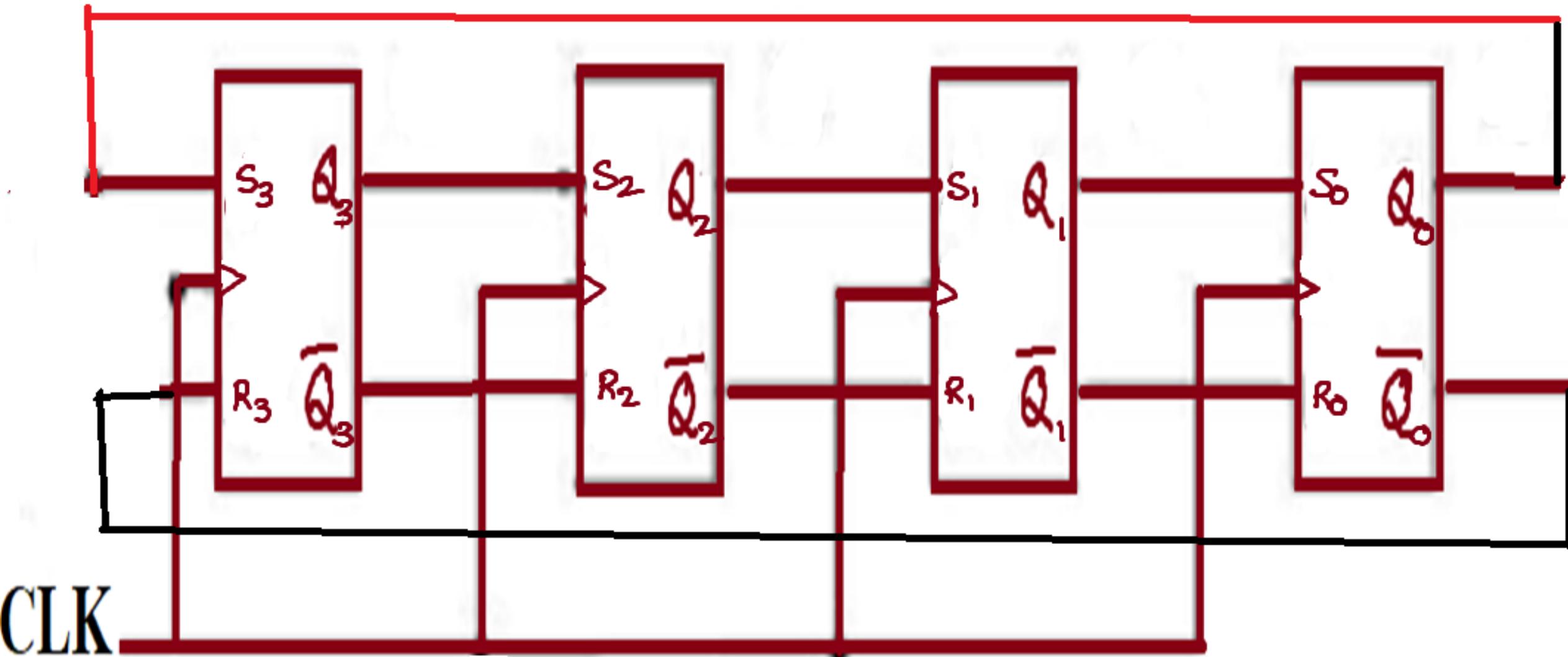


clk	$\checkmark$ $Q_3$	$\checkmark$ $Q_2$	$\checkmark$ $Q_1$	$Q_0$
0	1	1	0	0
1	0	1	1	0
2	0	0	1	1
→3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1
8	1	0	0	0
9	0	1	0	0
10	0	0	1	0
11	0	0	0	1

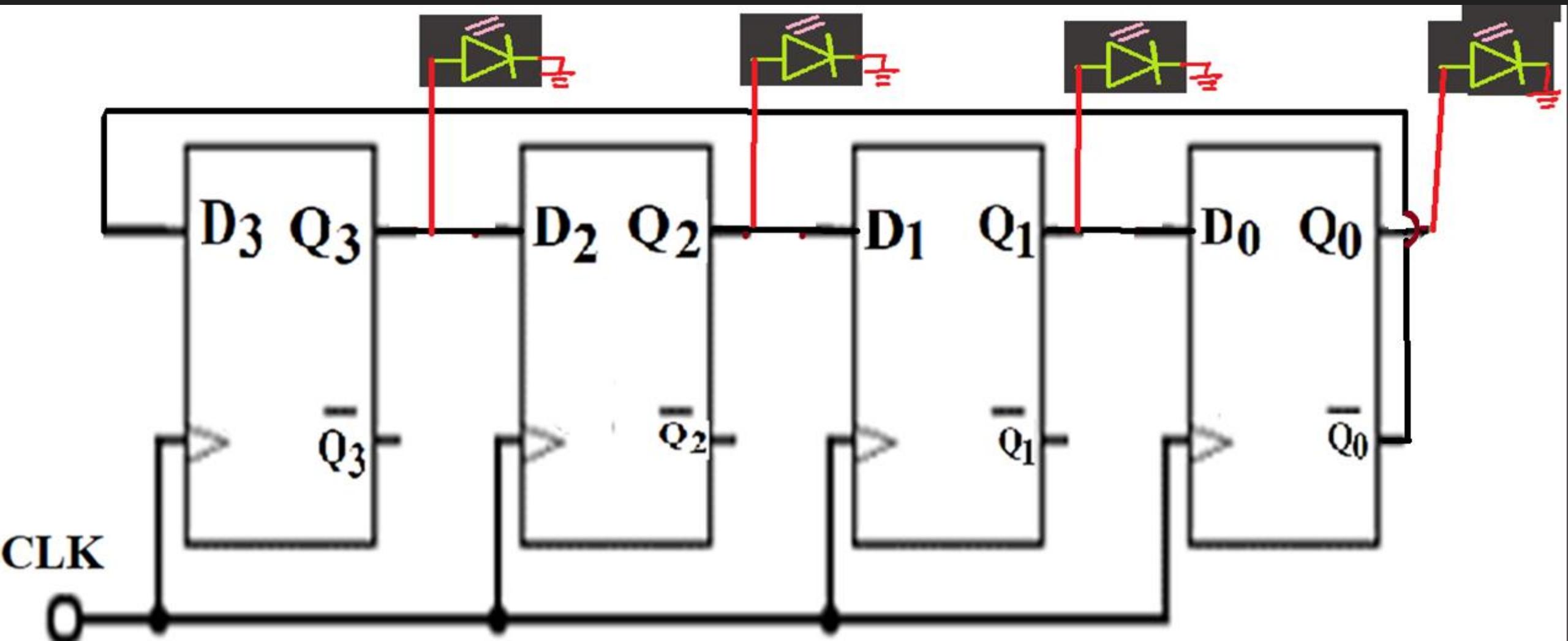
# Ring Counter using JK FF

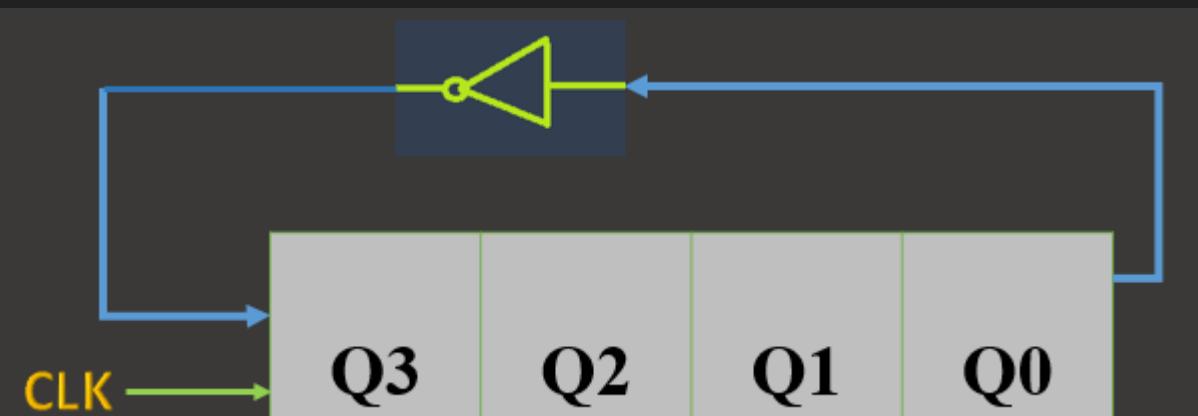


# Ring Counter using JK FF



# Johnson Ring Counter





CLK	$Q_3$	$Q_2$	$Q_1$	$Q_0$	Decoding logic
0	0	0	0	0	$\overline{Q}_3 \overline{Q}_0$
1	1	0	0	0	$Q_3 \overline{Q}_2$
2	1	1	0	0	$Q_2 \overline{Q}_1$
3	1	1	1	0	$Q_1 \overline{Q}_0$
4	1	1	1	1	$Q_3 Q_0$
5	0	1	1	1	$\overline{Q}_3 Q_2$
6	0	0	1	1	$\overline{Q}_2 Q_1$
7	0	0	0	1	$\overline{Q}_1 Q_0$
8	0	0	0	0	$\overline{Q}_3 \overline{Q}_0$
9	1	0	0	0	

# Repeating Pattern

AK	$Q_0$
1	0
2	0
3	0
4	0
5	1
6	1
7	1
8	1

AK	$Q_1$
1	0
2	0
3	0
4	1
5	1
6	1
7	1
8	0

AK	$Q_2$
1	0
2	0
3	1
4	1
5	1
6	1
7	0
8	0

AK	$Q_3$
1	0
2	1
3	1
4	1
5	1
6	0
7	0
8	0

$$T_{Q_0} = 8 \text{ Tak.}$$

$$f_{Q_0} = \frac{1}{8} \text{ Tak.}$$

$$D = \frac{1}{2} = 50\%.$$

$$T_{Q_1} = 8 \text{ Tak.}$$

$$f_{Q_1} = \frac{1}{8} \text{ Tak.}$$

$$D = 50\%.$$

$$T_{Q_2} = 8 \text{ Tak.}$$

$$f_{Q_2} = \frac{1}{8} \text{ Tak.}$$

$$D = 50\%.$$

$$T_{Q_3} = 8 \text{ Tak.}$$

$$f_{Q_3} = \frac{1}{8} \text{ Tak.}$$

$$D = 50\%.$$

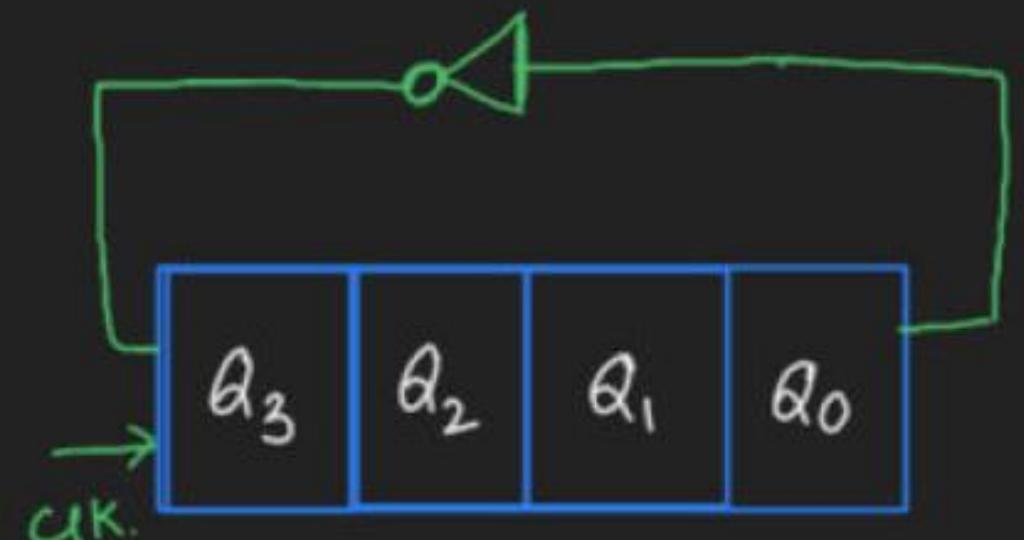
# For 4- bit Johnson Counter

- Number of used states = 8
  - Number of unused states = 8
  - Mod No = 8
  - Frequency of each FF =  $\frac{f_{clk}}{8}$
- Used states : 0,1,3,7,8,12,14,15
  - Unused states : 2,4,5,6,9,10,11,13

# For n- bit Johnson Counter

- Number of used states =
- Number of unused states =
- Mod No =
- Frequency of each FF =

Q) What happens when Johnson counter enters into any one of its unused states .

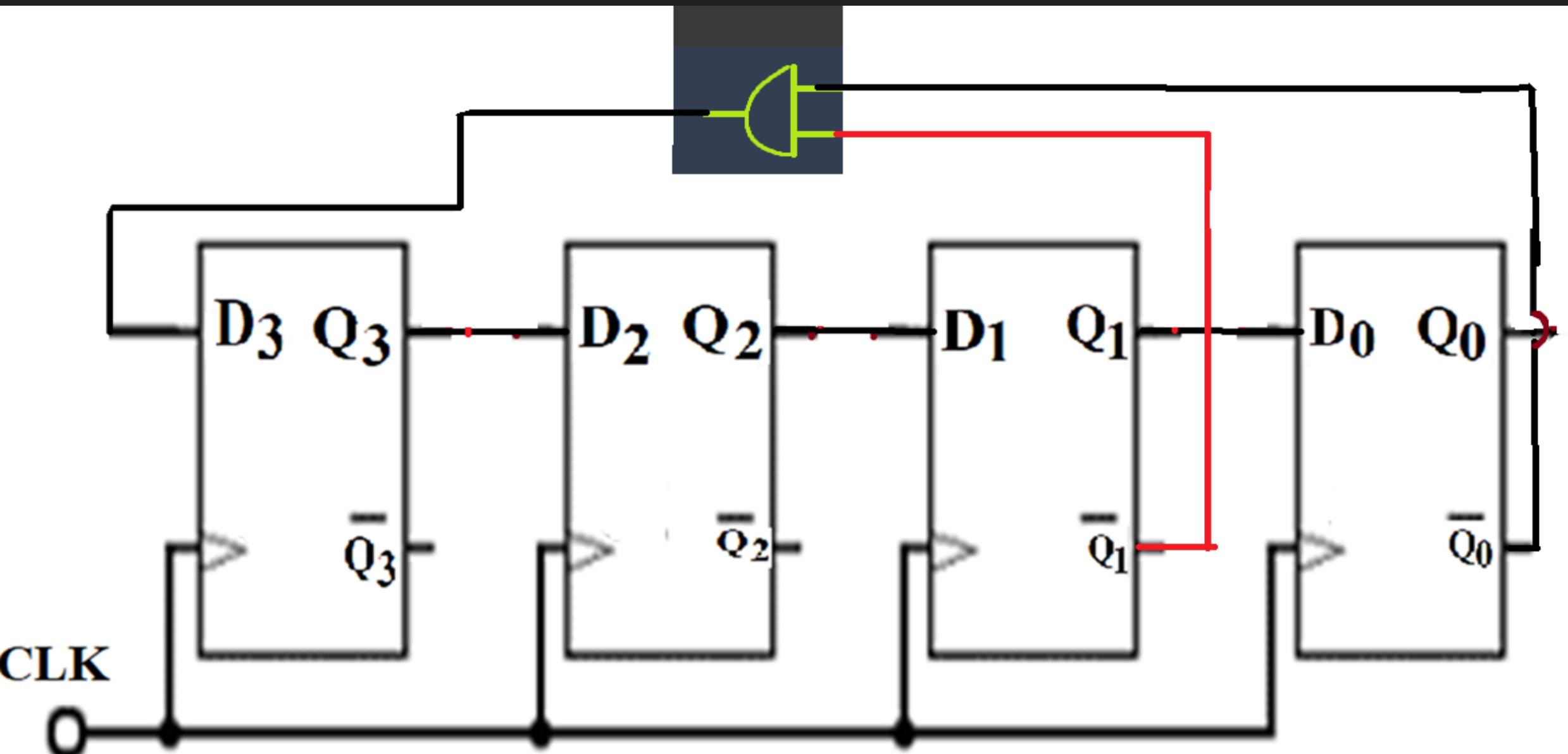


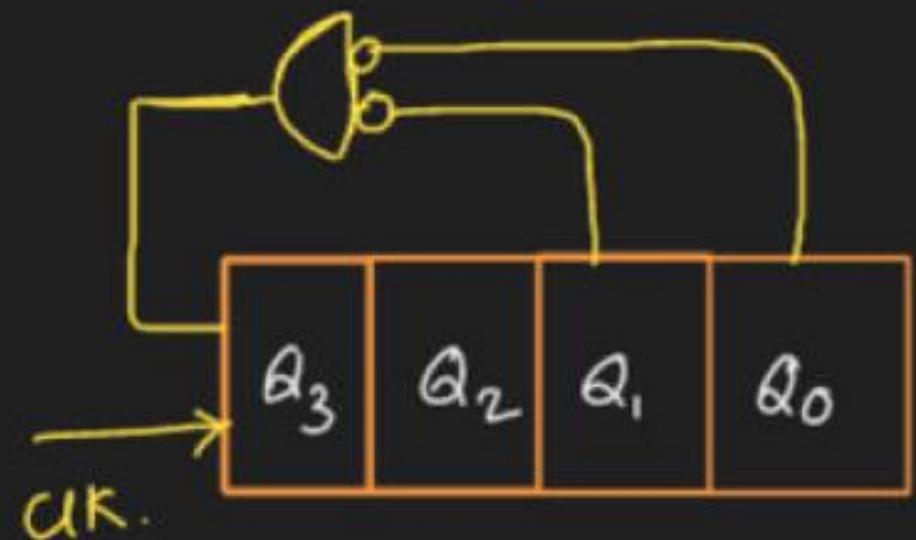
$Q_K$	$Q_3$	$Q_2$	$Q_1$	$Q_0$	
0	0	0	1	0	$\rightarrow 2$
1	1	0	0	1	$\rightarrow 9$
2	0	1	0	0	$\rightarrow 4$
3	1	0	1	0	$\rightarrow 10$
4	1	1	0	1	$\rightarrow 13$
5	0	1	1	0	$\rightarrow 6$
6	1	0	1	1	$\rightarrow 11$
7	0	1	0	1	$\rightarrow 5$

# Draw back of Johnson Ring counter

If the Johnson counter enters into any of its unused state , it completely stay in the unused state only

# Johnson Ring counter to prevent lock out problem





clk	$Q_3$	$Q_2$	$\check{Q}_1$	$\check{Q}_0$
0	0	0	1	0
1	0	0	0	1
2	0	0	0	0
3	1	0	0	0
4	1	1	0	0
5	1	1	1	0
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1
9	0	0	0	0

Johnson Ring counter

Twisted Ring counter

Switch tail counter

Walking Counter

Creeping counter

Mobjes counter

### Ring counter

### Johnson ring counter

1. Mod No =  $n$

2. Number of used states =  $\frac{n}{n}$ .  
Number of unused states =  $2^n - n$

3. Time period of each FF =  $n T_{d\kappa}$

4. Frequency of each FF =  $\frac{f_{d\kappa}}{n}$

5. Suffer from lock out problem

6. Decoding logic is simple

1. Mod No =  $2n$

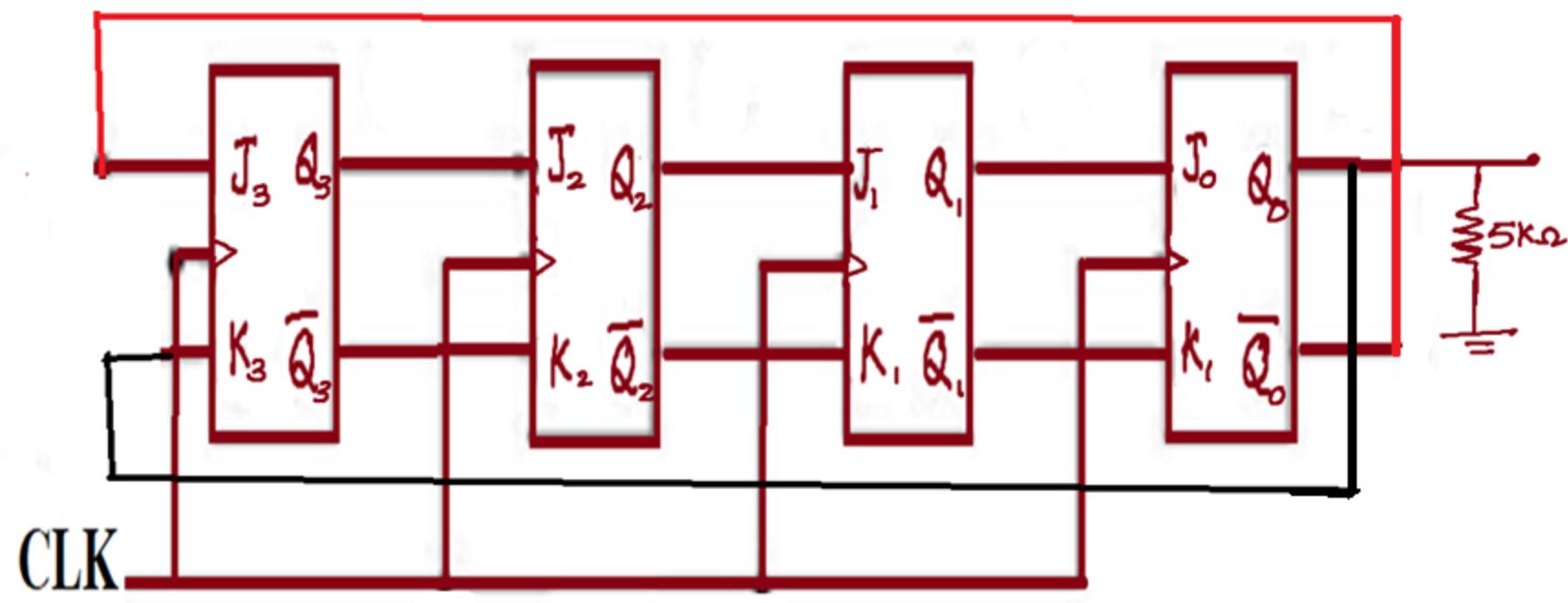
2. Number of used states =  $2^n$ .  
Number of unused states =  $2^n - 2n$

3. Time period of each FF =  $(2n) T_{d\kappa}$ .

4. Frequency of each FF =  $\frac{f_{d\kappa}}{2n}$

5. Suffer from lock out problem

6. Decoding logic requires AND and NOR gates



Q) Find

- power dissipation  $5\text{ k}\Omega$
- frequency of each FF
- If the transition probability of data bit at each is 0.7 , find the average value of  $Q_1$

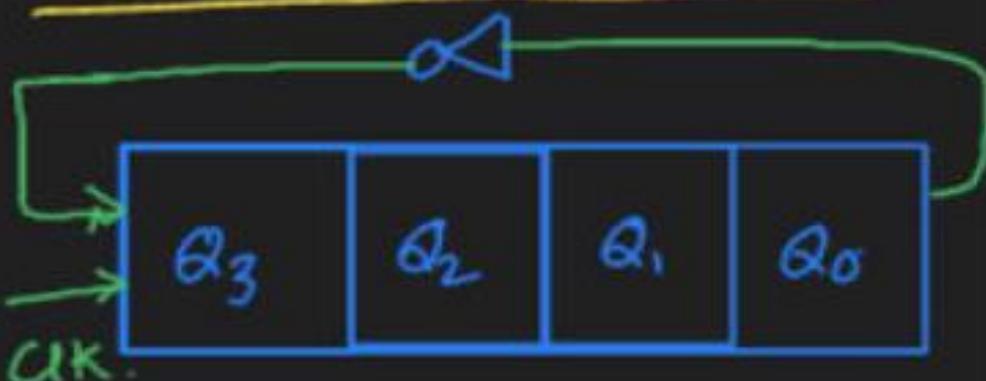
$$V_{on} = 5\text{ V}$$

$$V_{off} = 0\text{ V}$$

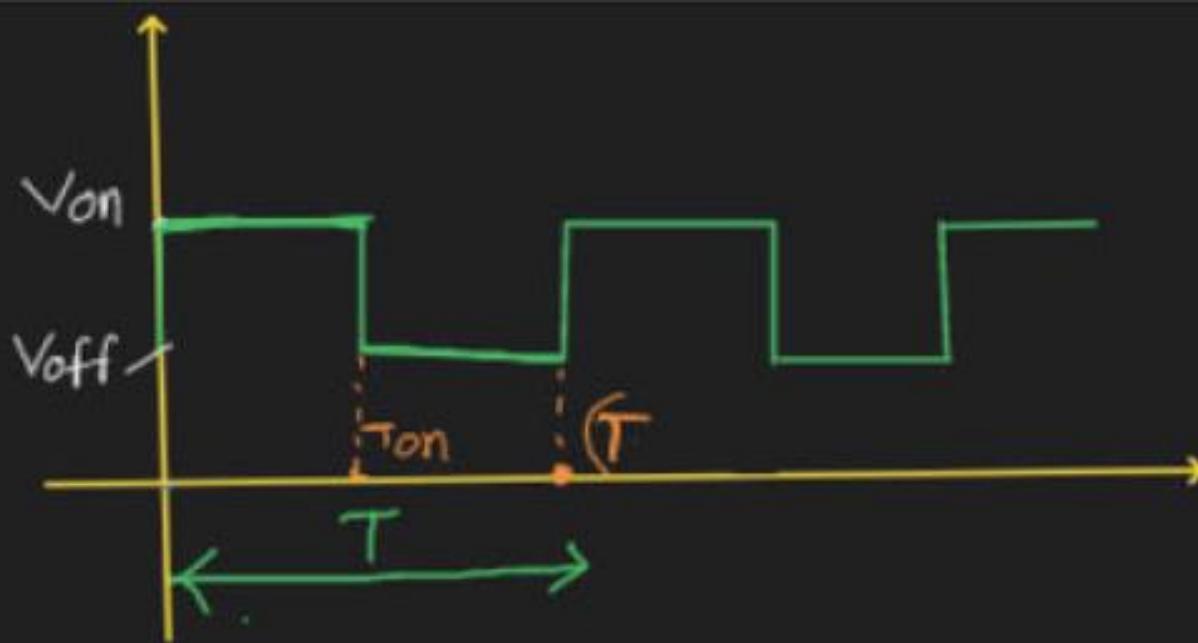
$$P_{diss} = \frac{V_{rms}^2}{R}$$

$Q_K$	$Q_3$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

Thomson Ring counter



MOD NO = 8



$$\begin{aligned}
 \text{avg} &= \frac{1}{T} \int_0^T v(t) dt \\
 &= \frac{1}{T} \left[ \int_0^{T_{on}} V_{on} dt + \int_{T_{on}}^T V_{off} dt \right]
 \end{aligned}$$

$$\begin{aligned}
 &= \frac{1}{T} \left( V_{on}(T_{on}) + V_{off}(T - T_{on}) \right) \\
 &= V_{on} \left( \frac{T_{on}}{T} \right) + V_{off} \left( 1 - \frac{T_{on}}{T} \right) \\
 &= V_{on}(D) + V_{off}(1 - D)
 \end{aligned}$$

✓

$\text{Avg} = V_{on}(D) + V_{off}(1 - D)$

$$RMS = \sqrt{\frac{1}{T} \int_0^T v(t)^2 dt}$$

$$Rms^2 = \frac{1}{T} \left[ \int_0^{T_{on}} v_{on}^2 dt + \int_{T_{on}}^T v_{off}^2 dt \right]$$

$$= \frac{1}{T} \left[ v_{on}^2 (T_{on}) + v_{off}^2 (T - T_{on}) \right]$$

$$Rms^2 = v_{on}^2 (D) + v_{off}^2 (1-D)$$
✓

$$\text{V}_{\text{rms}}^2 = \text{V}_{\text{on}}^2(D) + \text{V}_{\text{off}}^2(1-D)$$

$$= 5^2 \left(\frac{1}{2}\right) + 0 \left(1 - \frac{1}{2}\right)$$

$$\text{V}_{\text{rms}}^2 = \frac{25}{2}$$

$$P_{\text{diss}} = \frac{\text{V}_{\text{rms}}^2}{R} = \frac{25}{2 \times 5 \times 10^3} = 2.5 \underline{\underline{m\omega}}$$

$$\text{V}_{\text{rms}}^2 = \text{V}_{\text{on}}^2(D) + \text{V}_{\text{off}}^2(1-D)$$

$$= 5^2 \left(\frac{1}{2}\right) + 0 \left(1 - \frac{1}{2}\right)$$

$$\text{V}_{\text{rms}}^2 = \frac{25}{2}$$

$$P_{\text{diss}} = \frac{\text{V}_{\text{rms}}^2}{R} = \frac{25}{2 \times 5 \times 10^3} = 2.5 \underline{\underline{m\omega}}$$

$$f_{Q_0} = \frac{f_{ck}}{2n} = \frac{f_{ck}}{8}$$

$$f_{Q_1} = \frac{f_{ck}}{8}$$

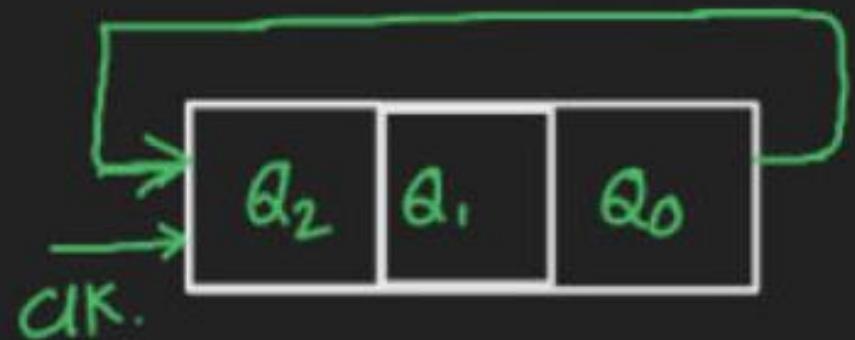
$$f_{Q_2} = \frac{f_{ck}}{8}$$

$$f_{Q_3} = \frac{f_{ck}}{8}$$

$$\begin{aligned}\text{avg } \delta Q_1 &= [v_{on}(D) + v_{off}(1-D)]P \\ &= [5(\frac{1}{2}) + 0(1-\frac{1}{2})] \underline{\underline{0.7}} \\ &= \left(\frac{5}{2}\right) 0.7 \\ &= \end{aligned}$$

Q) If the initial state of  $Q_2 Q_1 Q_0 = \underline{110}$ , then

- find
- a) MoD No
  - b) MSV of wave form of  $Q_1$
  - c) Pdiss in  $5k\Omega$  ✓
  - d) Average value of wave form of  $\underline{Q_0}$
  - e) Frequency of  $Q_2 Q_1 Q_0$  ✓



MoD No = 3

$\rightarrow$   $clk$

0

1

2

3

4

$Q_2$      $Q_1$      $Q_0$

1    1    0

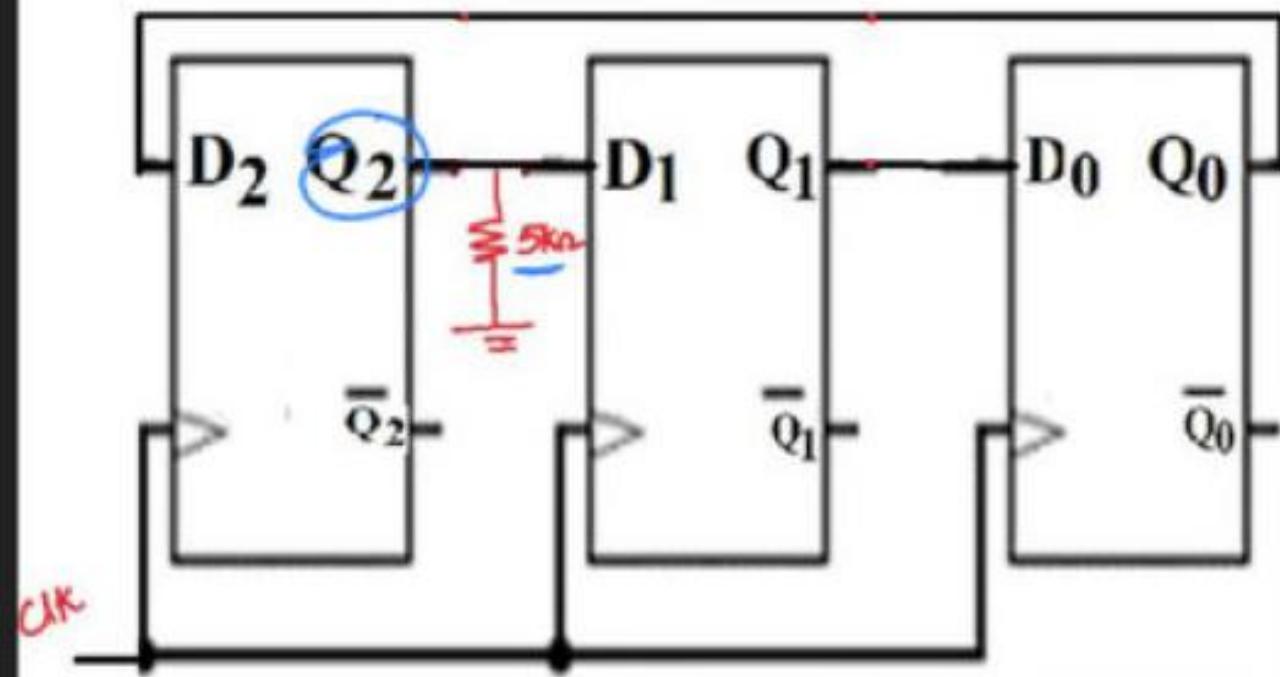
0    1    1

1    0    1

1    1    0

0    1    1

$$D = \frac{2}{3}.$$



$$MSV = (RMS)^2 = V_{on}^2(D) + V_{off}^2(1-D) \quad \left| \begin{array}{l} V_{on} = SV \\ V_{off} = \sigma V \end{array} \right.$$

$$= 5^2 \left(\frac{2}{3}\right) + 0 \left(1 - \frac{2}{3}\right)$$

$$MSV \text{ at } Q_1 = \frac{50}{3}.$$

$$MSV \text{ at } Q_2 = V_{on}^2(D) + V_{off}^2(1-D)$$

$$= \frac{50}{3}$$

$$\rho_{diss} = \frac{V_{rms}^2}{\kappa} = \frac{MSV}{5 \kappa} = \frac{10}{3} m \omega$$

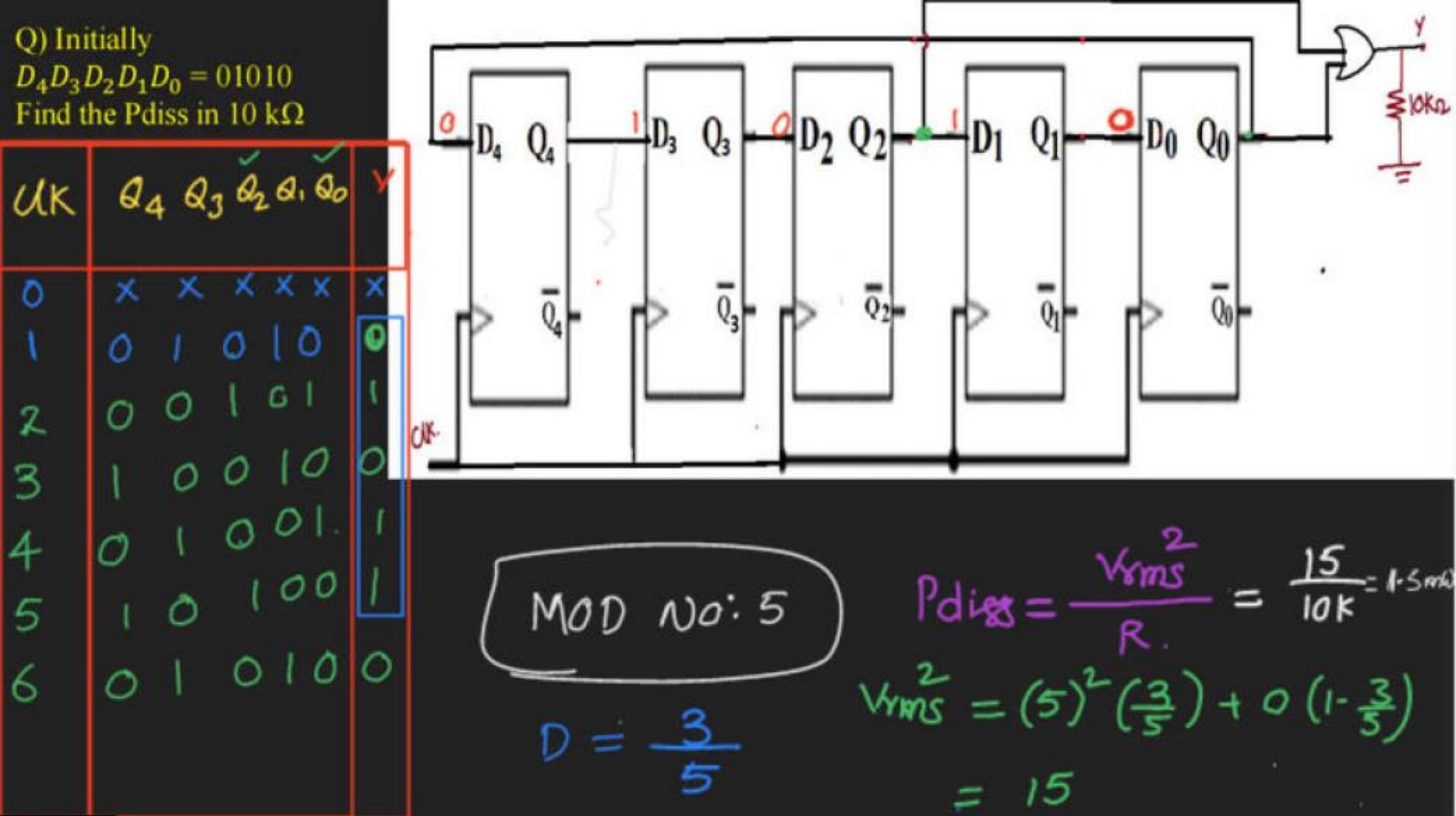
$$\text{avg value of } Q_0 = \gamma_{on}(D) + \gamma_{off}(1-D)$$
$$= 5 \left(\frac{2}{3}\right)$$

$$= \frac{10}{3} \text{ "}$$

$$f_{Q_0} = \frac{f_{ck}}{\text{MOD No.}} = \frac{f_{ck}}{3}$$

$$f_{Q_1} = \frac{f_{ck}}{3}$$

$$f_{Q_2} = \frac{f_{ck}}{3} \text{ "}$$



# User defined counter design

Q) Design synchronous counter , whose counting sequence is

$Q_1 Q_0 = 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00 \rightarrow \dots$  By using T- FF

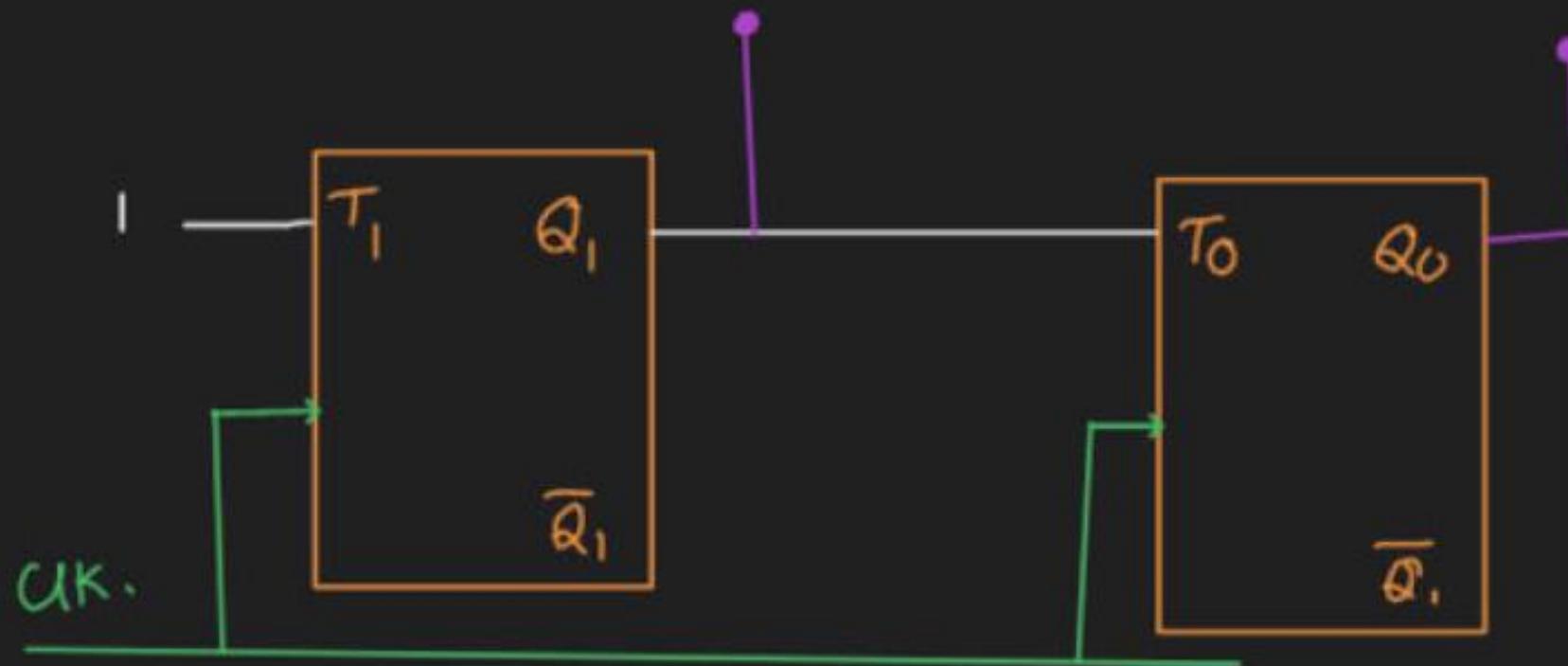
Present State $Q_1$ $Q_0$	Next State $Q_1^+$ $Q_0^+$	FF Inputs $T_1$	FF Inputs $T_0$
0    0	1    0	1	0
1    0	0    1	1	1
0    1	1    1	1	0
1    1	0    0	1	1

$Q_1$	$Q_0$	$T$
0	0	0
0	1	1
1	0	1
1	1	0

$$T_1 = 1.$$

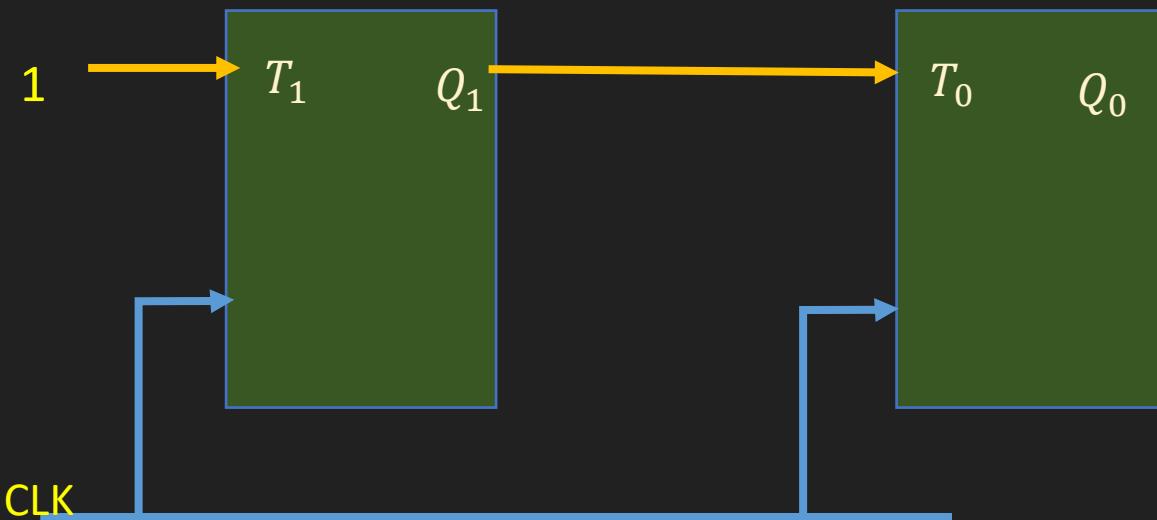
$$T_0 = Q_1 \bar{Q}_0 + Q_1 Q_0$$

$$T_0 = Q_1.$$



Q) Design synchronous counter , whose counting sequence is  $Q_1Q_0 = 00 \rightarrow 10 \rightarrow 01 \dots \rightarrow 11 \rightarrow 00 \dots \rightarrow 10 \dots$

By using D- FF



$00 \rightarrow 10 \rightarrow 01 \rightarrow 11$   
 $MOD = 4$

Q) Find the counting sequence of the following  
If the initial state of the counter  $Q_1Q_0 = 00$   
then the state of counter after  
a) 236 clocks b) 251 clocks c) 333 clocks

FF ips.	Next state	
$T_1 = 1$	$Q_1$	$Q_0$
—	0	0 $\rightarrow$
1	0	1
1	1	0
0	1	1
0	0	0 $\rightarrow$

$$4) \quad 236 \quad (59$$

$$\frac{20}{\underline{36}}$$

$$\frac{36}{\underline{36}}$$

$$\textcircled{0}$$

$4^{\text{th}} \rightarrow 00$

$236^{\text{th}} \rightarrow 00$

$$4) \quad 251 \quad (62$$

$$\frac{24}{\underline{11}}$$

$$\frac{8}{\textcircled{3}}$$

$4^{\text{th}} \rightarrow 00$

$4 \times 62 \rightarrow 00$

$4(62)+1 \rightarrow 10$

$4(62)+2 \rightarrow 01$

$4(62)+3 \rightarrow 11$

$$4) \quad 333 \quad (83$$

$$\frac{32}{\underline{13}}$$

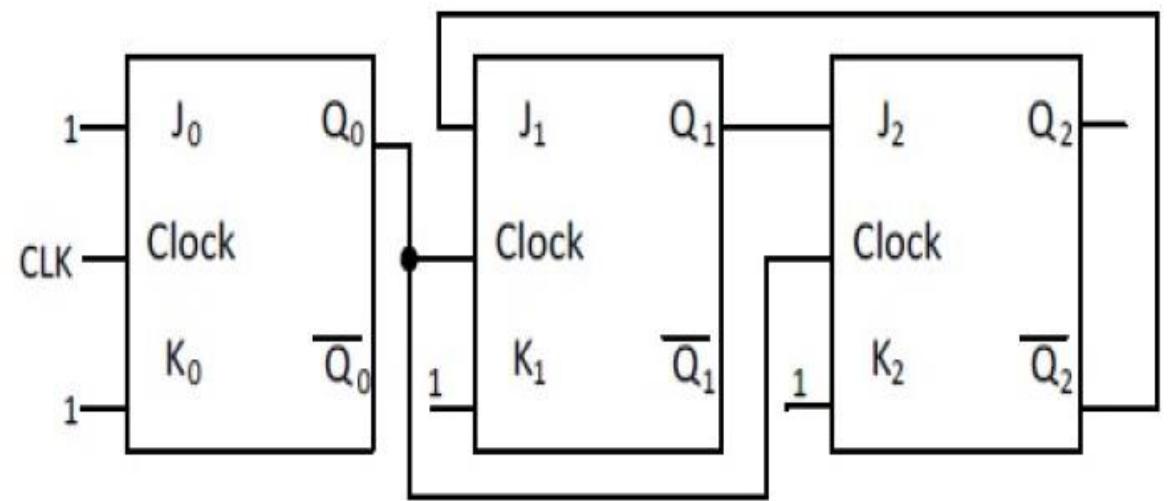
$$\frac{12}{\textcircled{0}}$$

$4^{\text{th}} \rightarrow 00$

$4 \times 83 \rightarrow 00$

$4(83)+1 \rightarrow 10$

The figure shows a digital circuit constructed using negative edge triggered J-K flip flops. Assume a starting state of  $Q_2Q_1Q_0=000$ . This state  $Q_2Q_1Q_0=000$  will repeat after \_\_\_\_\_ number of cycles of the clock CLK.



$000 \rightarrow 011 \rightarrow 100 \rightarrow 001$

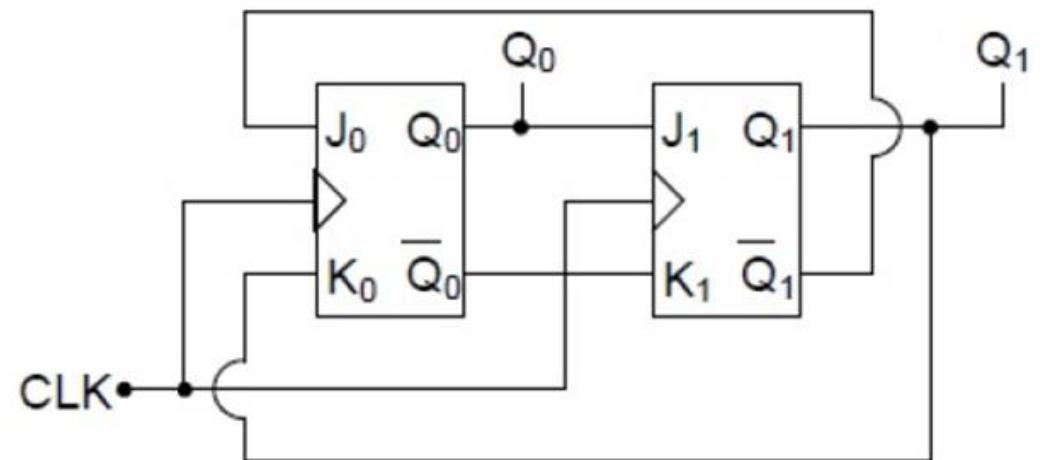
$\downarrow$

$101 \leftarrow 010$

$MOD = 6$

FF 1/PS						
$J_2 = Q_1$ , $K_2 = 1$	$J_1 = \bar{Q}_2$ , $K_1 = 1$	$J_0 = 1$ , $K_0 = 1$	$Q_2 \quad Q_1 \quad Q_0$			
—	—	—	0 0 0	0 0 0	0 0 0	
0	1	1	0 1 1	0 1 1	0 1 1	
1	1	1	1 1 1	1 1 1	1 1 1	
1	1	1	1 0 0	1 0 0	1 0 0	
0	1	0	0 0 1	0 0 1	0 0 1	
0	1	0	0 1 0	0 1 0	0 1 0	
1	1	1	1 0 1	1 0 1	1 0 1	
0	1	0	0 0 0	0 0 0	0 0 0	

In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is  $Q_1 Q_0 = 00$ . The state ( $Q_1 Q_0$ ), immediately after the 333<sup>rd</sup> clock pulse is



- (A) 00
- (B) 01
- (C) 10
- (D) 11

**Mod = 4**

4) 333. (83

32

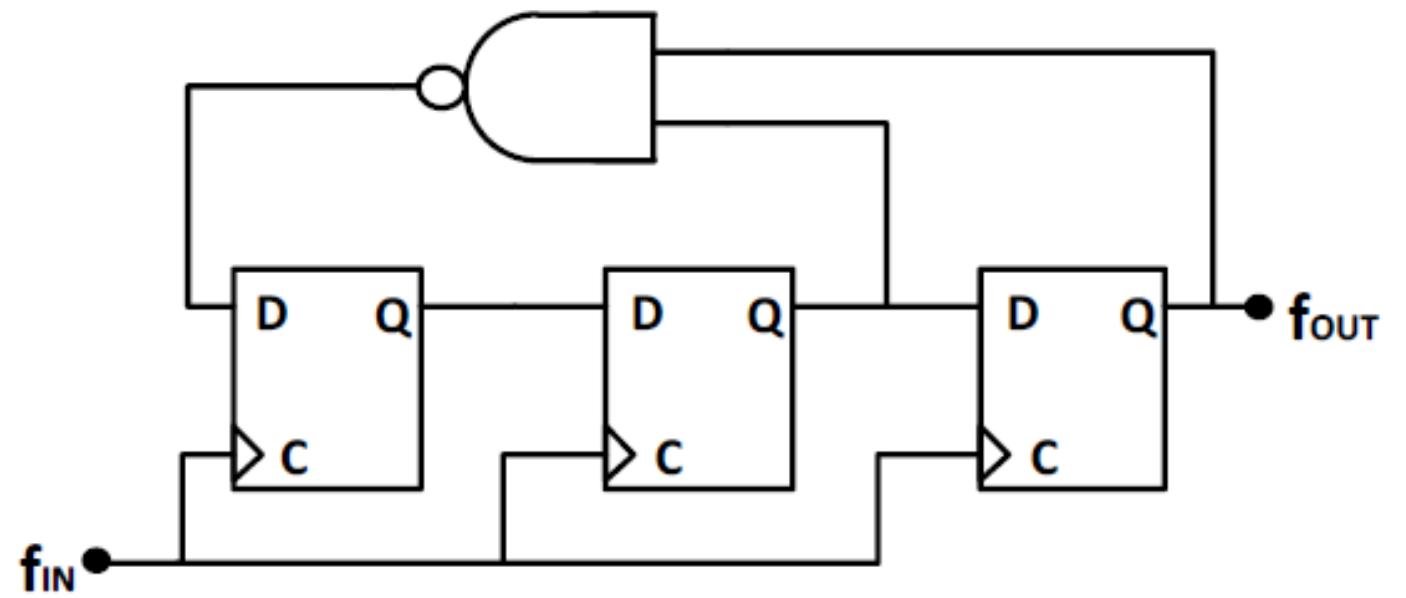
13  
12  
—  
1

$J_1 = Q_0 \quad K_1 = \bar{Q}_0$		$J_0 = \bar{Q}_1 \quad K_0 = Q_1$		$Q_1$	$Q_0$
0	1	1	0	0	0
1	0	1	0	1	1
1	0	0	1	1	0
0	1	0	1	0	0

$$4 \times 83 \rightarrow 00$$

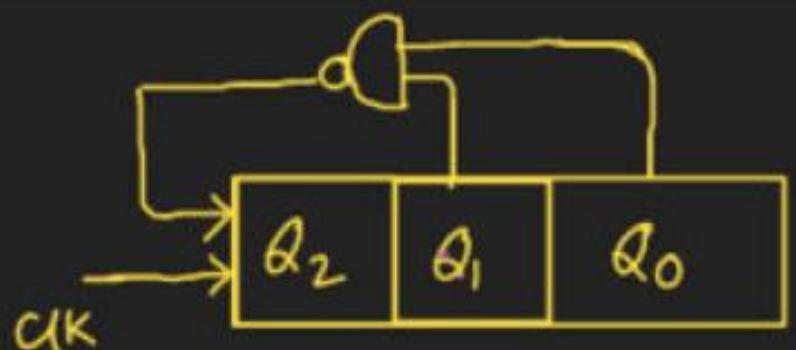
$$4(83) + 1 \rightarrow \underline{\underline{01}}$$

Which one of the following statements is true about the digital circuit shown in the figure



- (A) It can be used for dividing the input frequency by 3.
- (B) It can be used for dividing the input frequency by 5.
- (C) It can be used for dividing the input frequency by 7.
- (D) It cannot be reliably used as a frequency divider due to disjoint internal cycles.

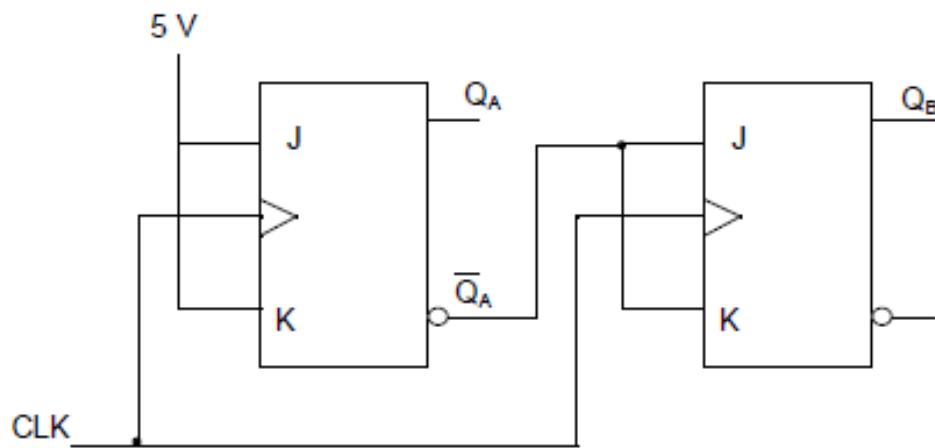
clk	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0	0	0
1	0	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	1	0	0
7	1	1	0



MOD - 5

$$f_{out} = \frac{f_{clk}}{5}$$

The current state  $Q_A$   $Q_B$  of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of the system is



(A) 00

(B) 01

(C) 11

(D) 10

$J_B = \bar{Q}_A$	$K_B = \bar{Q}_A$	$J_A = 1$	$K_A = 1$	$Q_B$	$Q_A$
1	1	1	1	1	1
0	0	1	1	1	0
1	1	1	1	0	1
0	0	1	1	0	0

# Set up time

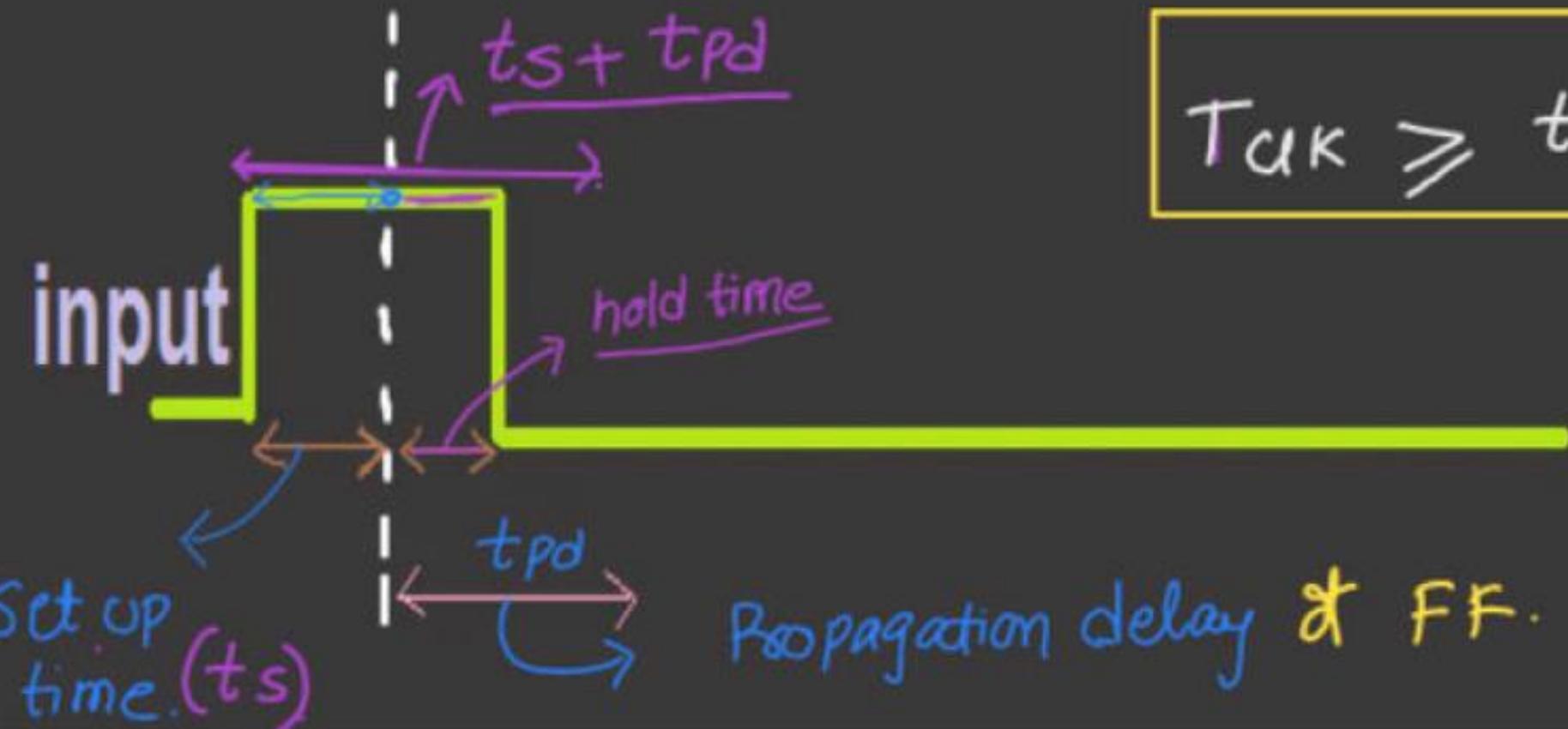
It is the minimum amount of time before the active edge of the clock, the input signal should remain constant

# Hold time

It is the minimum amount of time after the active edge of the clock, the input signal should remain constant



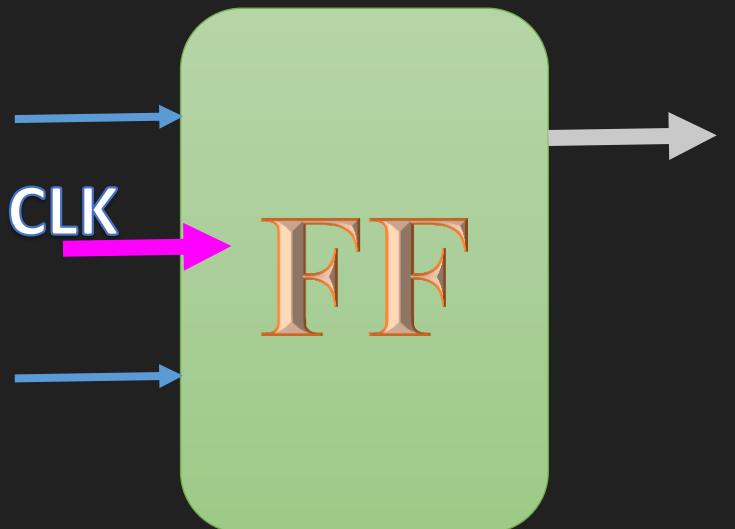
$T_{clk} \cdot$



$$T_{clk} \geq t_{SU} + t_{pd}$$

Propagation delay & FF.

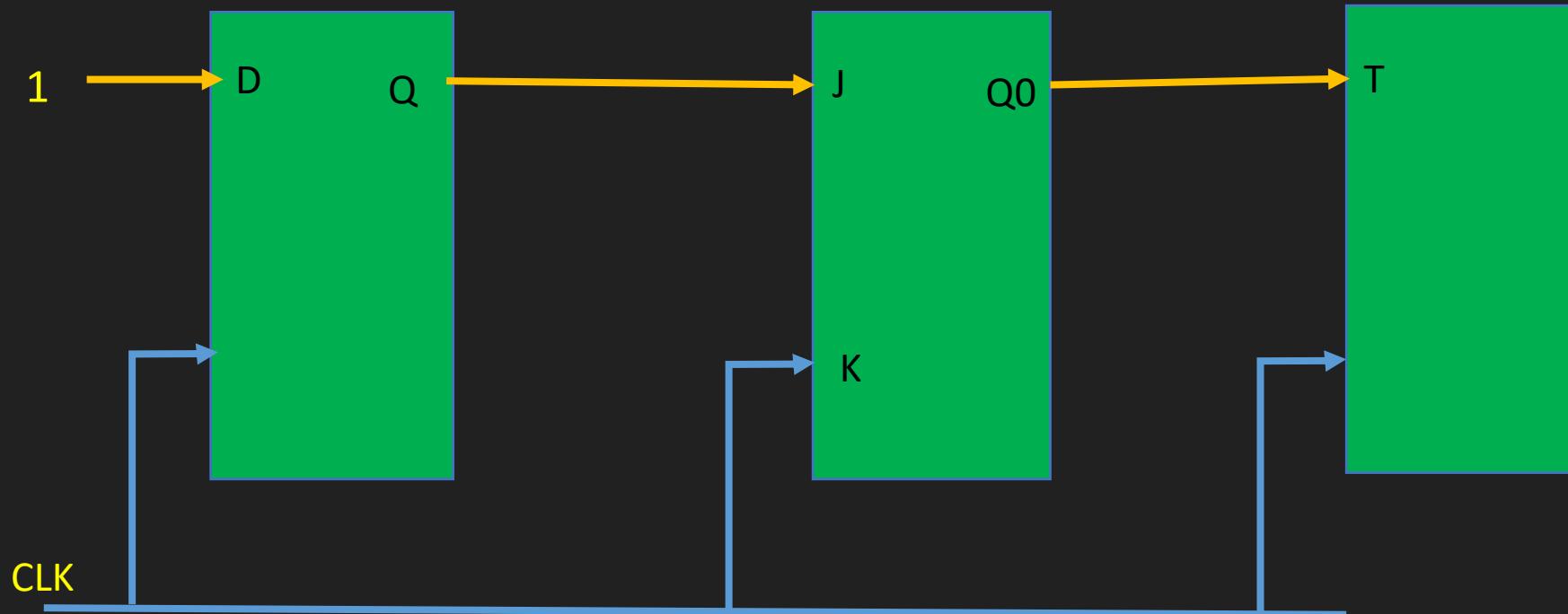
# Delay in single FF



$$\text{Delay} = (t_{pd})_{FF} + t_s .$$

$$T_{clk} \geq (t_{pd})_{FF} + t_s$$

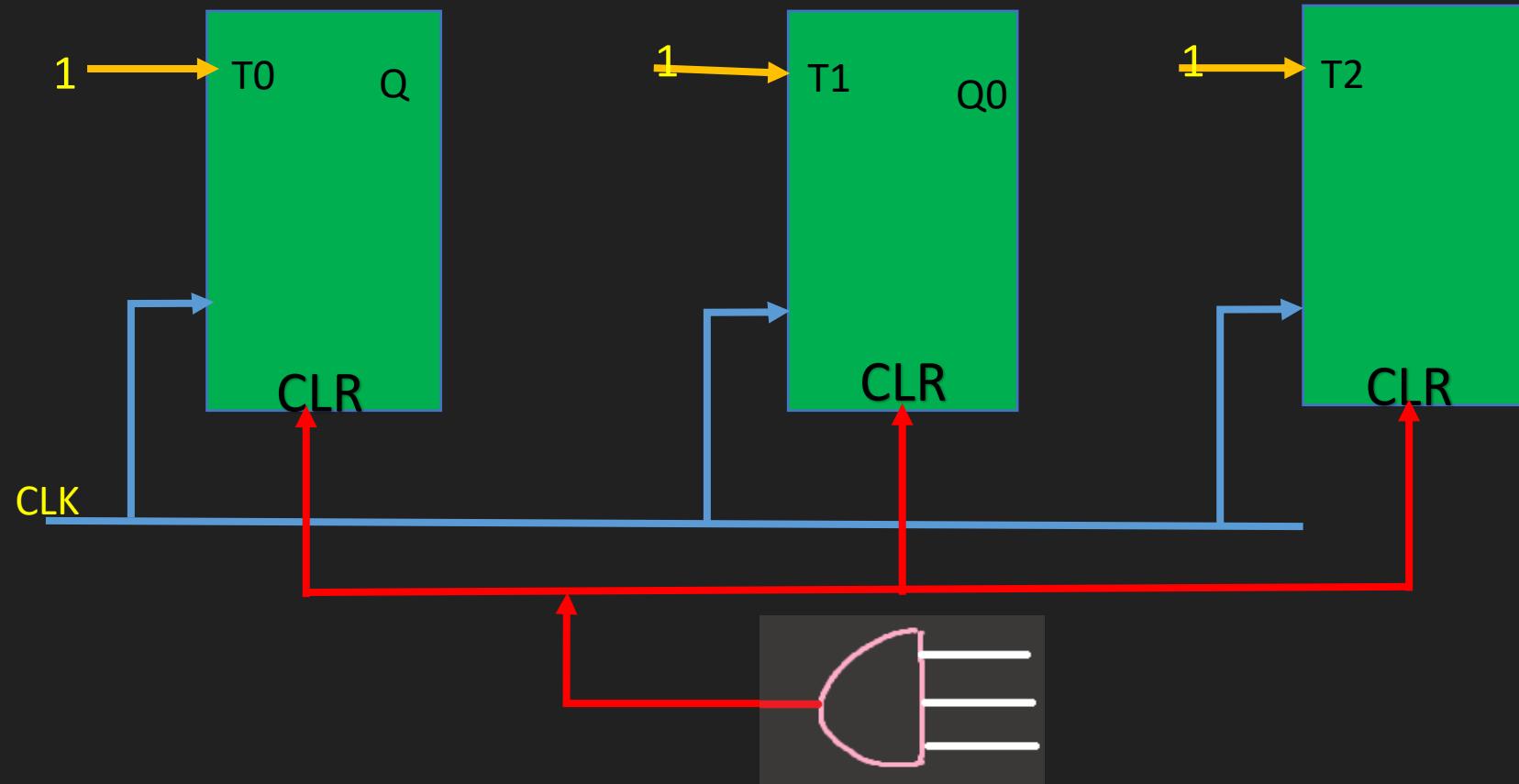
# Delay in Synchronous counter without feedback



$$\text{Delay} = \left. (t_{pd})_{FF} \right|_{\max} + t_s .$$

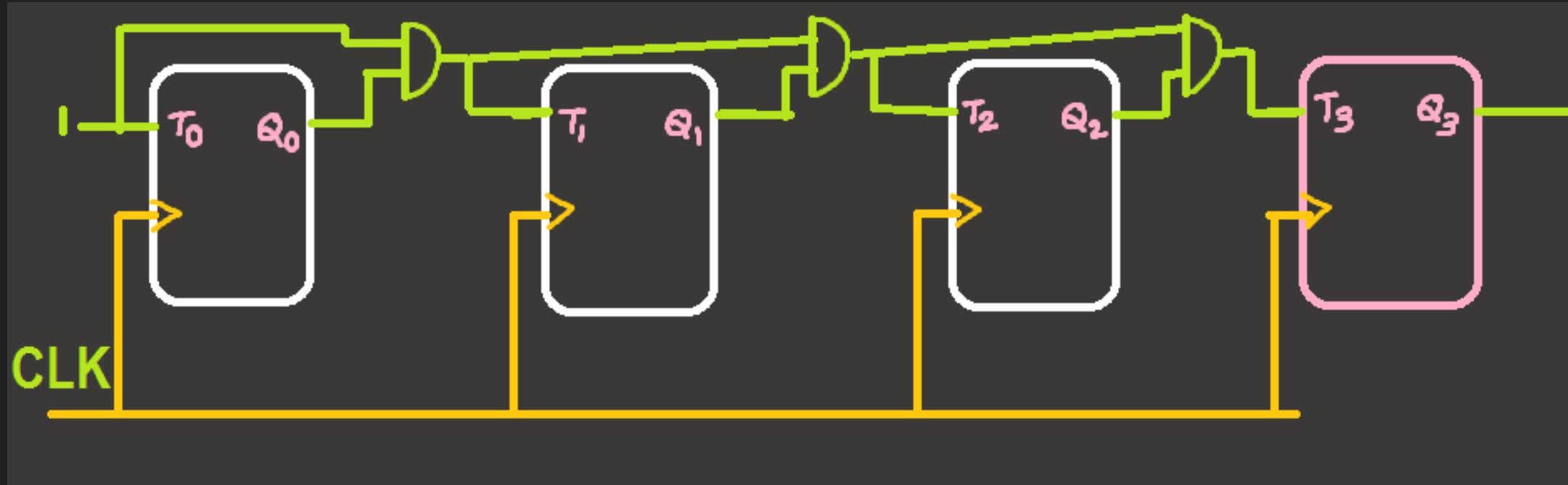
$$\tau_{clk} \geq \left. (t_{pd})_{FF} \right|_{\max} + t_s .$$

# Delay in Synchronous counter with feedback



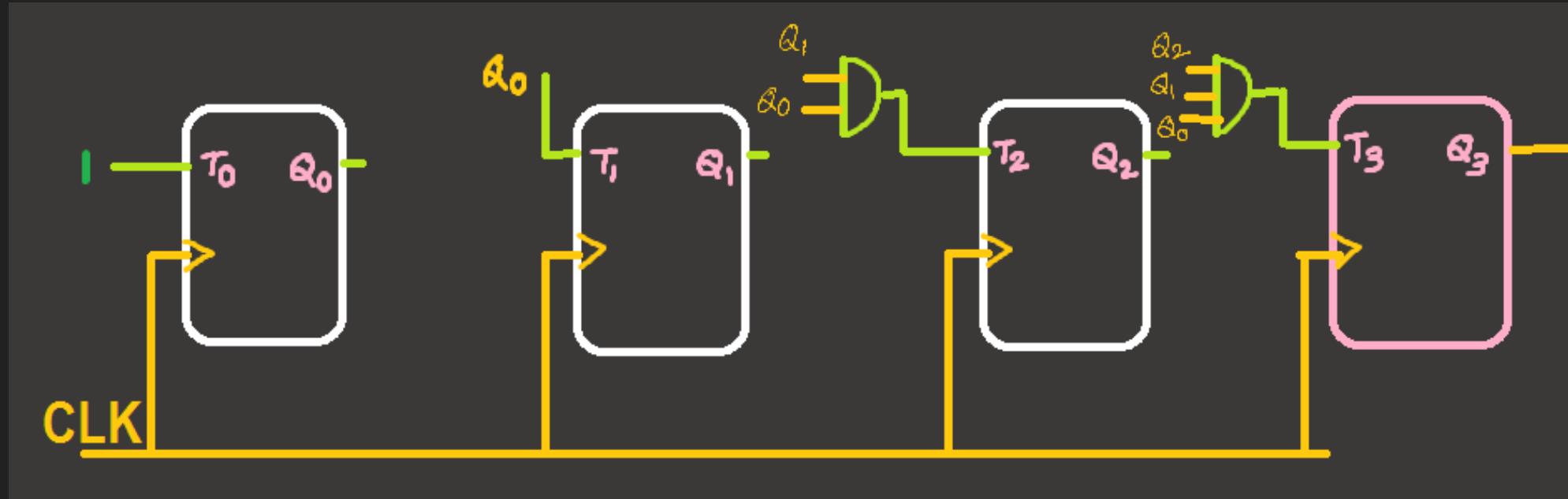
$$T_{clk} \geq (t_{pd})_{FF} + t_s + (t_{pd})_{AND}$$

# Synchronous series carry counter



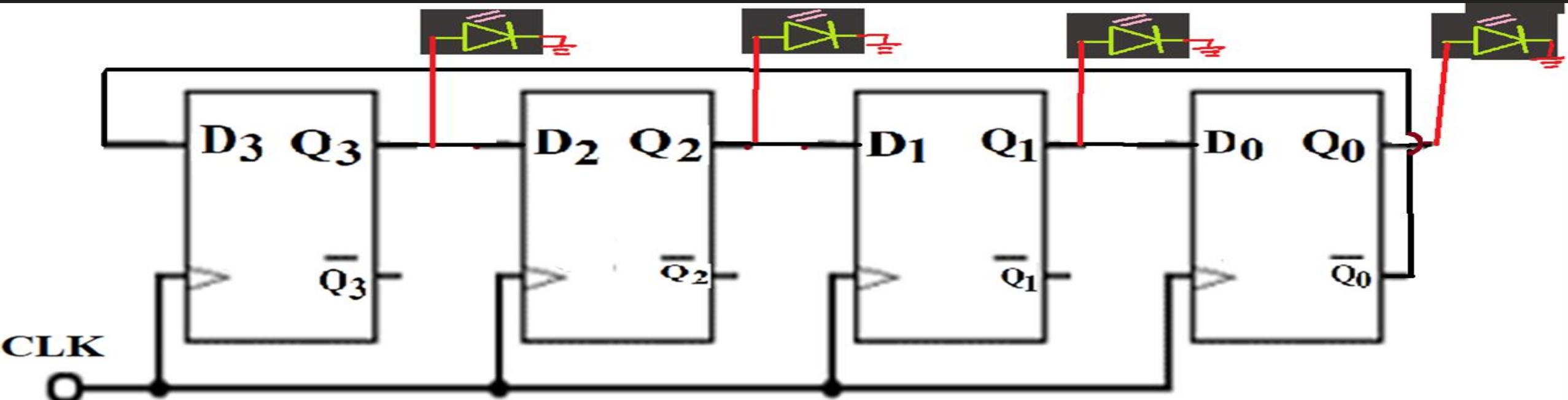
$$T_{dK} \geq (t_{pd})_{FF} + t_s + \underline{3}(t_{pd})_{AND}.$$

# Synchronous parallel carry counter



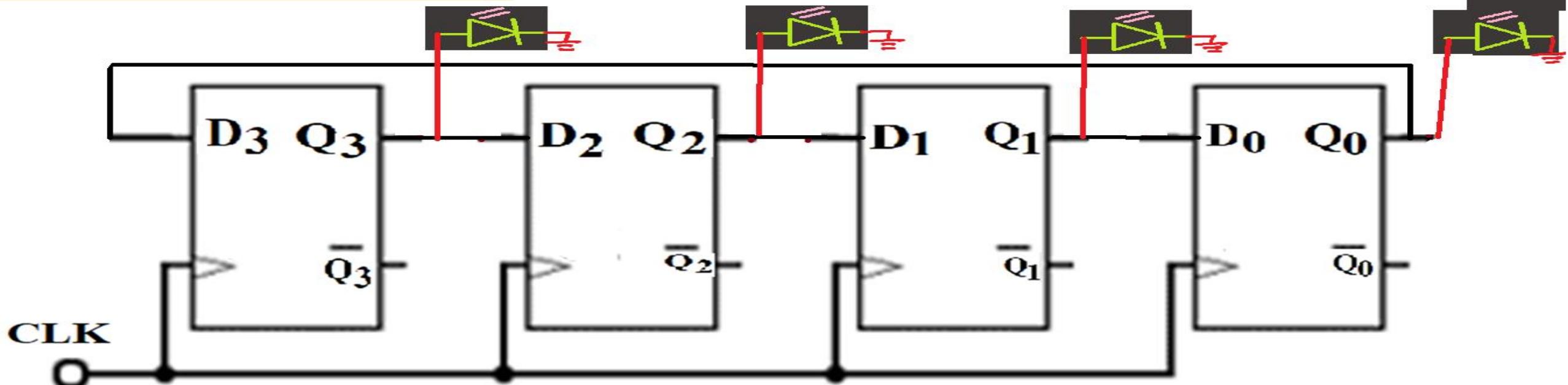
$$T_{dK} \geq (t_{pd})_{FF} + t_s + (t_{pd})_{AND} .$$

# Johnson Ring Counter



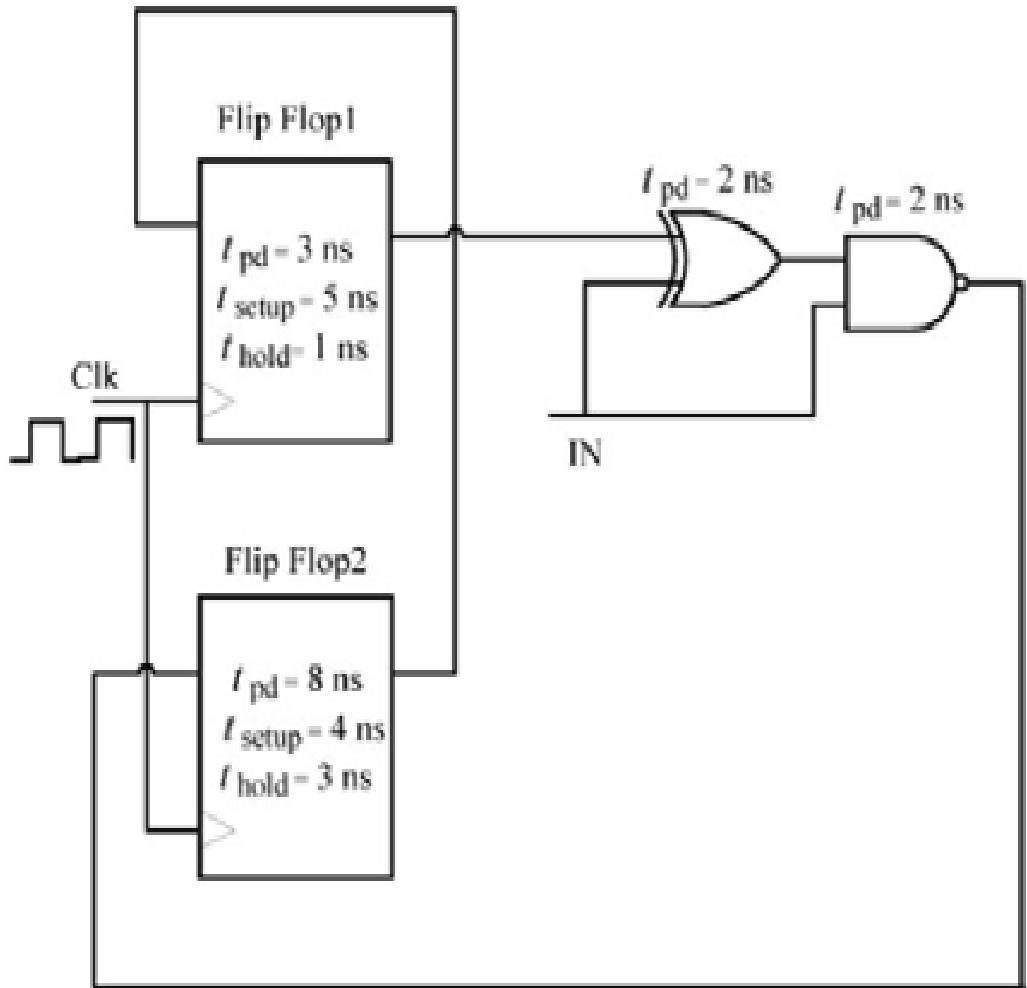
$$T_{CLK} \geq (t_{PD})_{FF} + t_s.$$

# Ring Counter



$$T_{clk} \geq (t_{pd})_{FF} + t_s$$

For the components in the sequential circuit shown below,  $t_{pd}$  is the propagation delay,  $t_{setup}$  is the setup time, and  $t_{hold}$  is the hold time. The maximum clock frequency (rounded off to the nearest integer), at which the given circuit can operate reliably, is \_\_\_\_\_ MHz.



①

$$T_{clk} \geq (t_{pd})_{FF2} + t_{s1}$$

$$T_{clk} \geq 8 + 5$$

**T<sub>clk</sub> > 13 ns** ①

FF2

$$T_{clk} \geq (t_{pd})_{FF1} + (t_{pd})_{XOR} + (t_{pd})_{AND} + t_{s2}$$

$$T_{clk} \geq 3 + 2 + 2 + 4$$

**T<sub>clk</sub> > 11 ns** ②

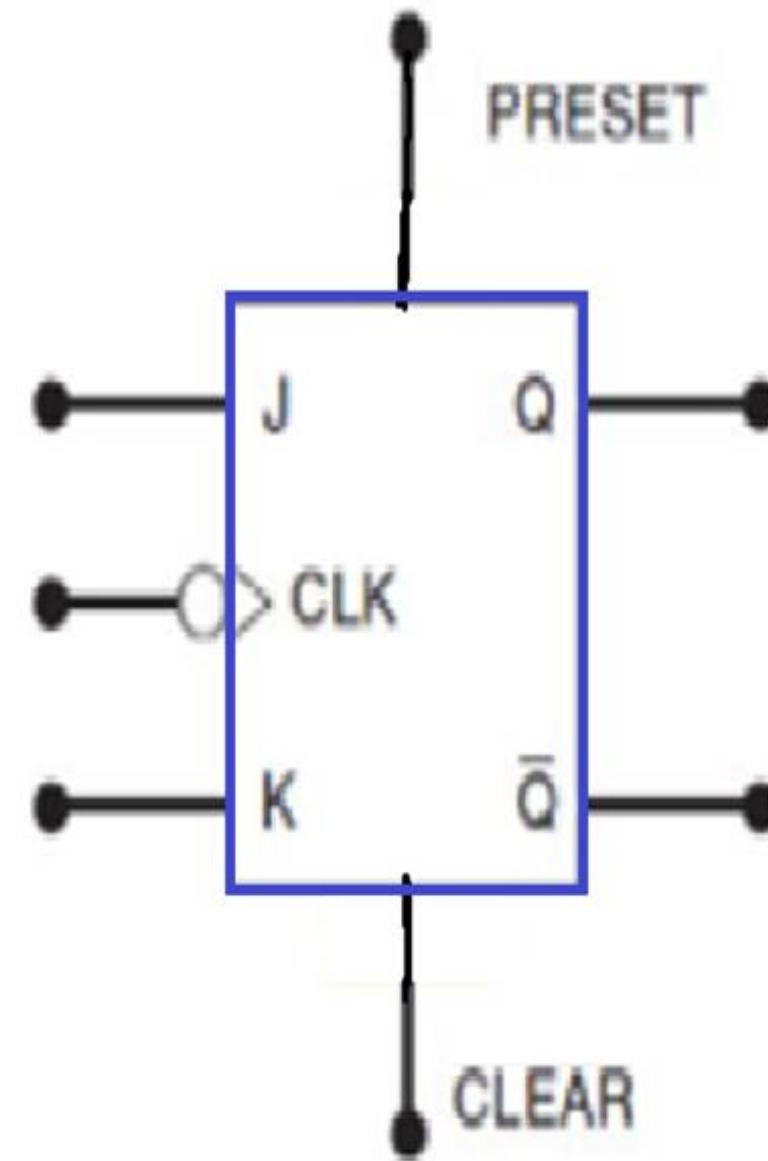
$$T_{ck} \geq 13 \text{ ns.}$$

$$(T_{ck})_{\min} = 13 \text{ ns.}$$

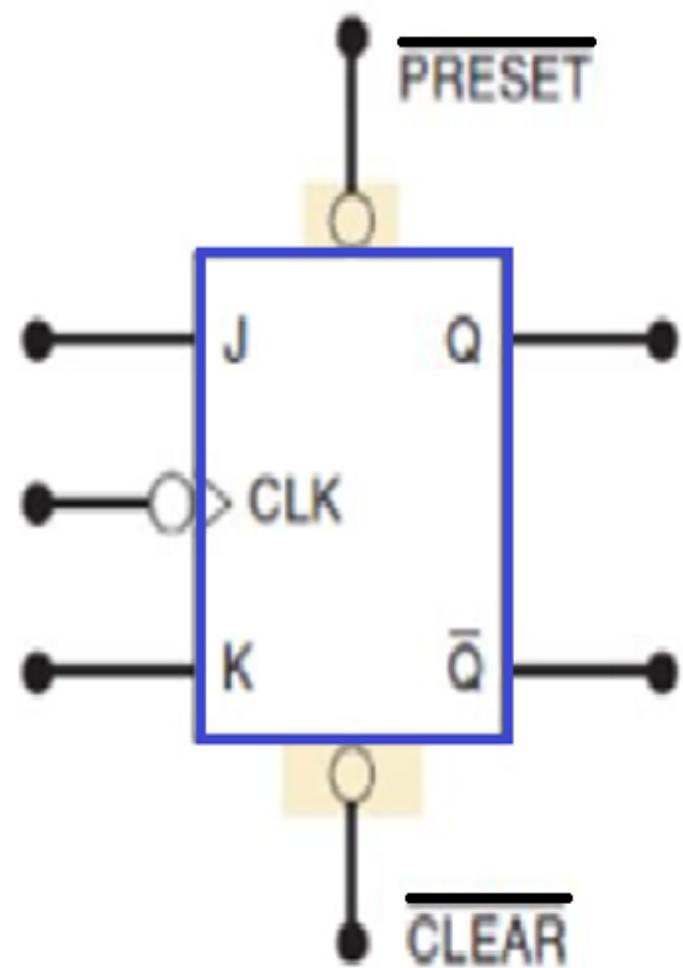
$$(f_{ck})_{\max} = \frac{1}{(T_{ck})_{\min}}$$

$$(f_{ck})_{\max} = \frac{1}{13 \times 10^9} = 76.9 \text{ MHz}$$

# Asynchronous Clear and Asynchronous Preset

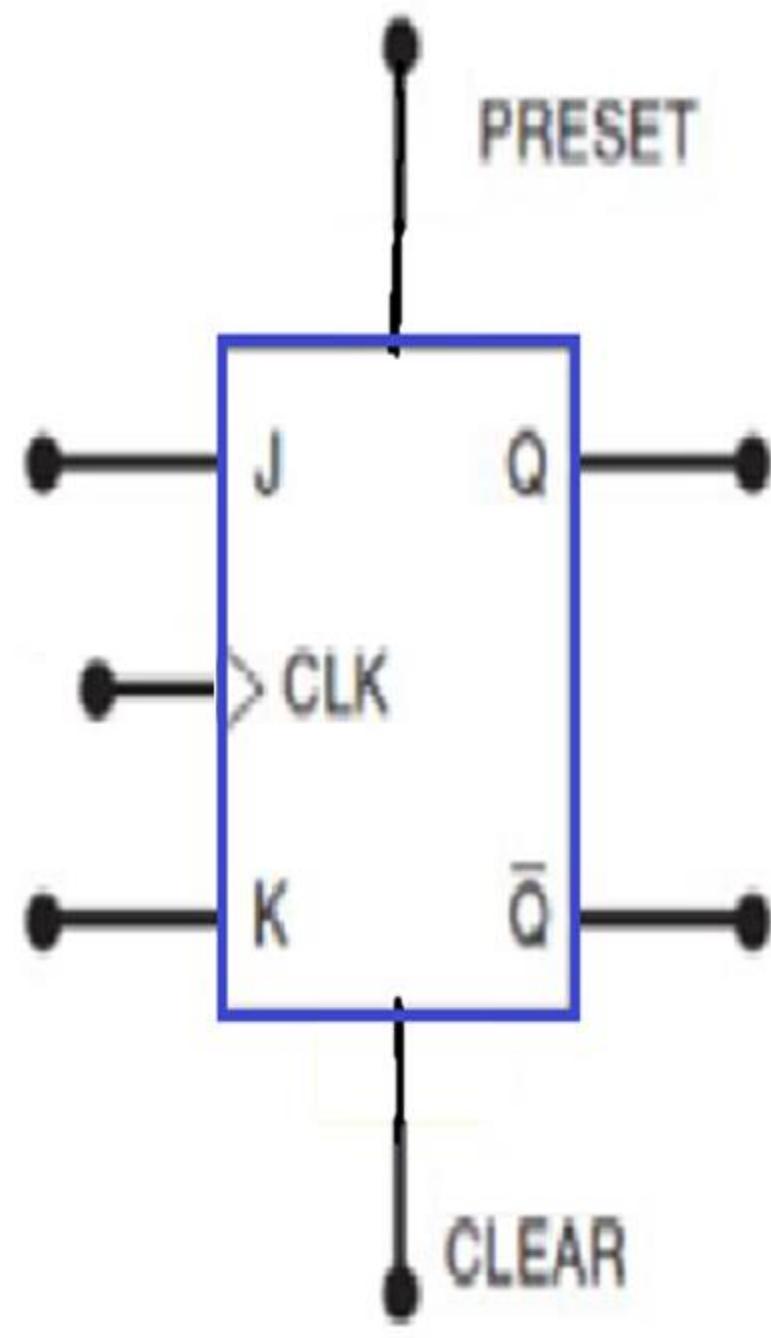


PRESET	CLEAR	FF Response
0	0	clocked operation
0	1	Reset (0)
1	0	Set (1)
1	1	invalid (x).

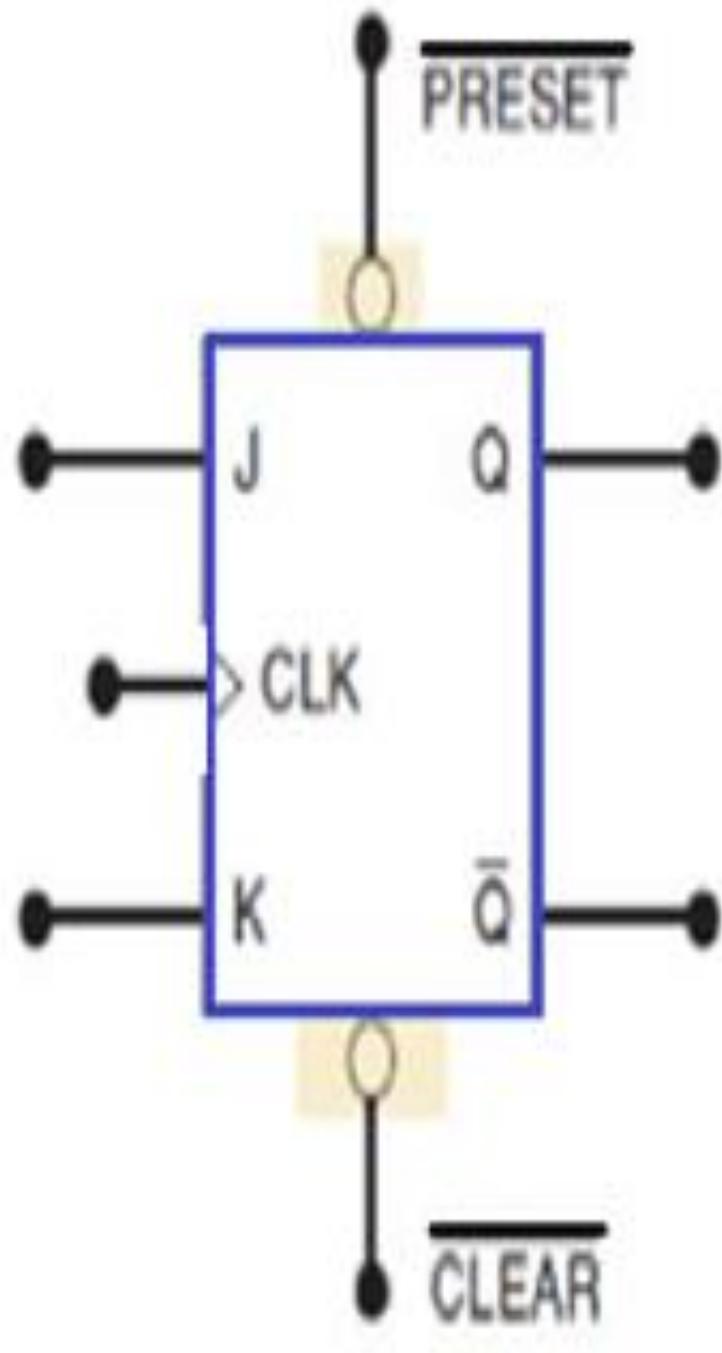


<u>PRESET</u>	<u>CLEAR</u>	FF Response .
0	0	Invalid (x)
0	1	Set (1)
1	0	Reset (0)
1	1	Clocked operation .

# **Synchronous Clear and Synchronous Preset**



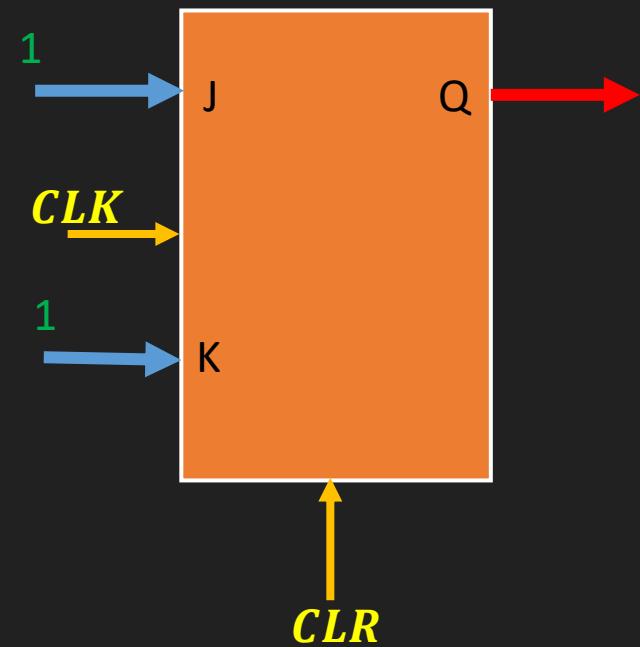
CLR	PRE	CLK	$Q^+$
0	0	0	Q
0	0	1	docked operation
0	1	0	Q
0	1	1	1 (set)
1	0	0	Q
1	0	1	0 (Reset)
1	1	0	Q
1	1	1	Invalid.

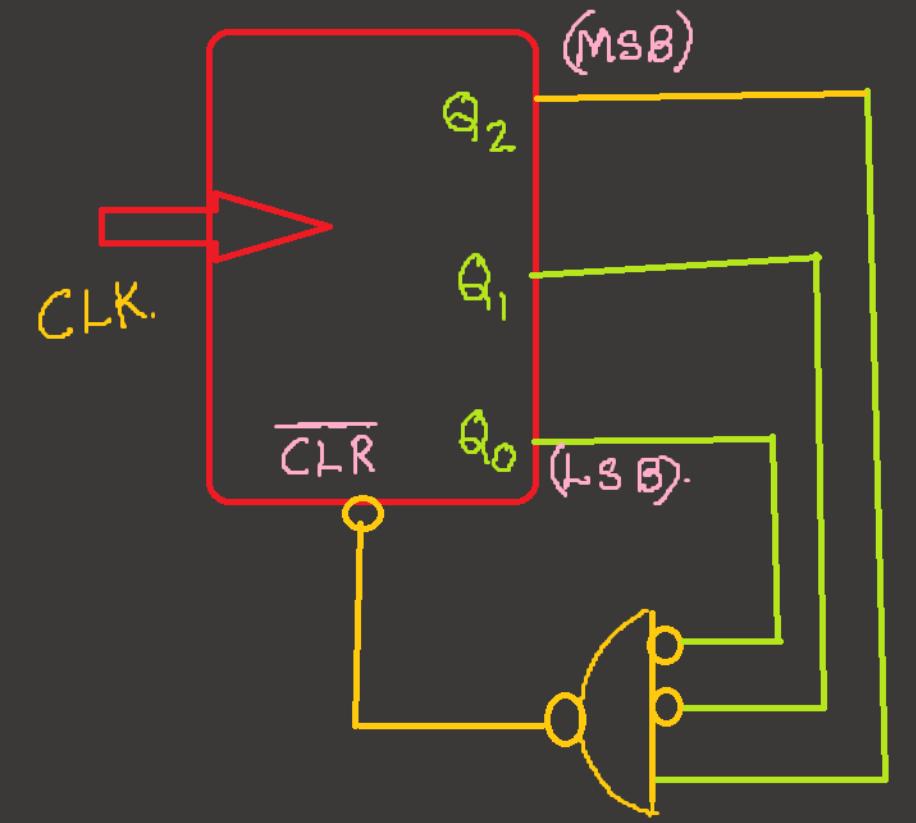


$\overline{CLR}$	$\overline{PRE}$	CLK	$Q +$
0	0	0	Q
0	0	1	invalid
0	1	0	Q
0	1	1	Reset(0)
1	0	0	Q
1	0	1	Set(1)
1	1	0	Q
1	1	1	clocked operation

Q) Draw the output wave form of the JK FF ,

- a) Asynchronous CLR
- b) Synchronous CLR





Q) Find the Mod number of the counter

- a) If ( tpd ) comb = 0 , Asynchronous Clear
  - b) If ( tpd ) comb = 0 , synchronous Clear
  - c) If ( tpd ) comb = Tclk , Asynchronous Clear
  - d) If ( tpd ) comb = Tclk , synchronous Clear
  - e) If ( tpd ) comb < Tclk , Asynchronous Clear

Q)

Clk	$Q_2\ Q_1\ Q_0$	R.
0	0 0 0	0
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
4	<del>1 0 0</del>	1
	0 0 0	

$$(t \oplus d)_{\text{Comb}} = 0$$

$$R = Q_2 \bar{Q}_1 \bar{Q}_0$$

$$R = 1 \cdot 0 \cdot 1 = 1$$

MOD NO = 4

⑬ . Synchronous CLR &  $(t_{pd})_{comb} = 0$ .

Clk	$Q_2\ Q_1\ Q_0$	R.
0	0 0 0	0
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
<u>4</u>	<u>1 0 0</u>	1
<u>—</u>	<u>0 0 0</u>	

$$R = Q_2 \bar{Q}_1 \bar{Q}_0$$

$$R = 100$$

MOD = 4

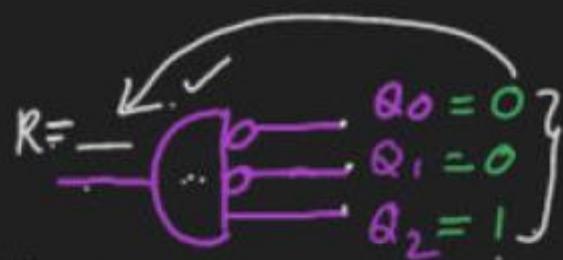
$$c) \quad (t_{pd})_{\text{comb}} = T_{\text{clk}}$$

Asynchronous CLR

G1K	$Q_2 \ Q_1 \ Q_0$	R
0	0 0 0	0
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
4	1 0 0	0
5	1 0 1	1
	0 0 0	

$$R = Q_2 \bar{Q}_1 \bar{Q}_0$$

1 0 0



5<sup>th</sup> clock

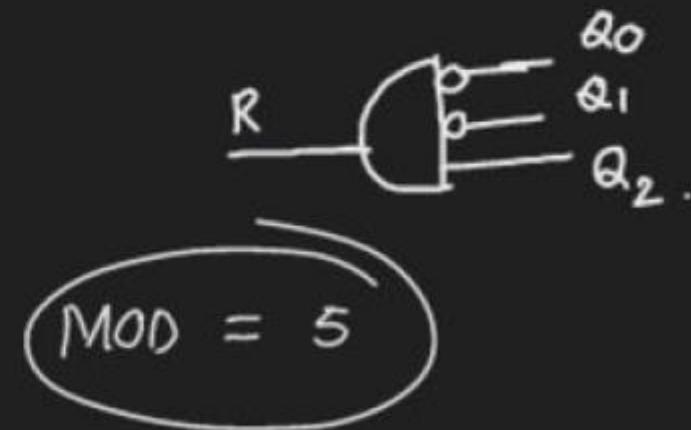
4<sup>th</sup> clock

MOD = 5

d)  $\underline{(t_{PD})_{Comb} = T_{clk}}$ . Synchronous CLR

CLK	$Q_2$	$Q_1$	$Q_0$	R.
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	1
	0	0	0	

$$R = Q_2 \overline{Q}_1 \overline{Q}_0$$

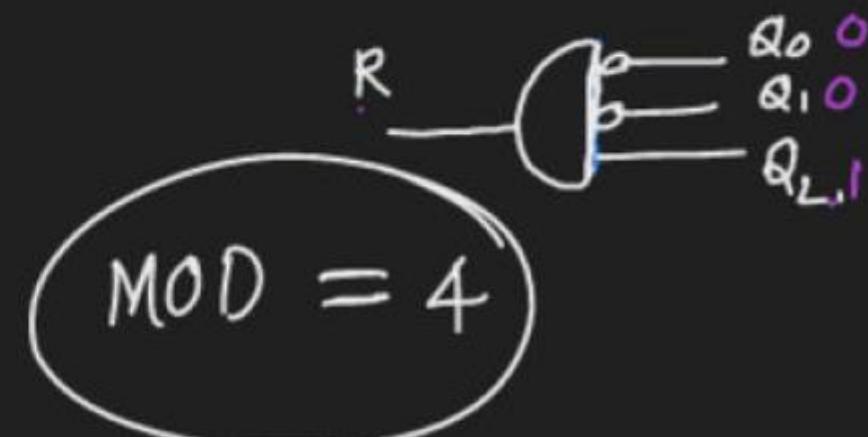


$$e) \quad (\underline{t_{pd}})_{\text{comb.}} < \tau_{\text{clk.}}$$

Asynchronous CLR

CLK	$Q_2$	$Q_1$	$Q_0$	R.
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
<u><math>4+x</math></u>	<u>1</u>	<u>0</u>	<u>0</u>	<u>1</u>
	0	0	0	

$$R = Q_1 \bar{Q}_0 \bar{Q}_2$$



If ( tpd ) comb < Tclk , Asynchronous Clear



$$f) (t_{pd})_{\text{comb}} < T_{\text{clk}}$$

Synchronous CLR.

CLK	$Q_2$ $Q_1$ $Q_0$	R
0	0 0 0	0
1	0 0 1	0
2	0 1 0	0
3	0 1 1	0
4	1 0 0	0
$4+x$	1 0 0	1
5	<del>1 0 1</del>	<del>1</del>
	0 0 0	

$$R = Q_2 \bar{Q}_1 \bar{Q}_0$$

MOD. = 5

## Note :

1. If  $(tpd_{comb}) = nTclk$

MoD No of Synchronous counter = MoD No of Asynchronous counter

2. If  $(tpd_{comb}) \neq nTclk$

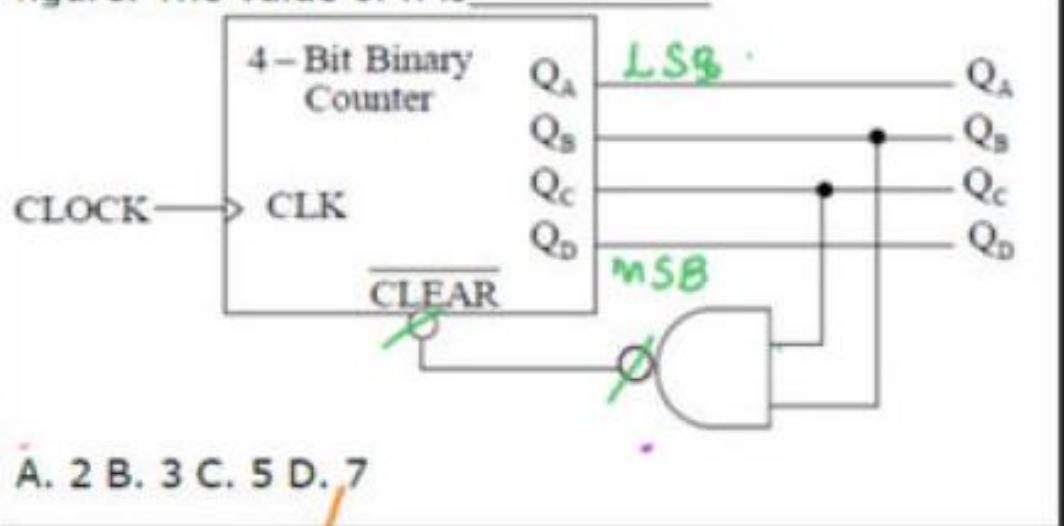
MoD No of Synchronous counter = MoD No of Asynchronous counter + 1

# Assumptions

1. Consider Up counter , if not mentioned
2. Q(subscript high ) = MSB , if not mentioned
3. Assume Asynchronous CLR , if not mentioned
4. Assume  $(tpd)_{comb} < Tclk$  , if not mentioned

$Q_2 \rightarrow \text{MSB}$  .  
 $Q_1$   
 $Q_0$ .

A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure. The value of n is \_\_\_\_\_



A. 2 B. 3 C. 5 D. 7

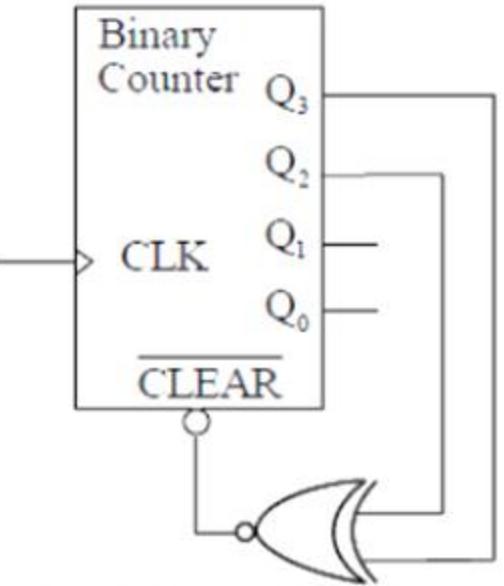
$$R = Q_C Q_B$$

$$(t_{pd})_{comb} < T_{clk}$$

$$mod = 7$$

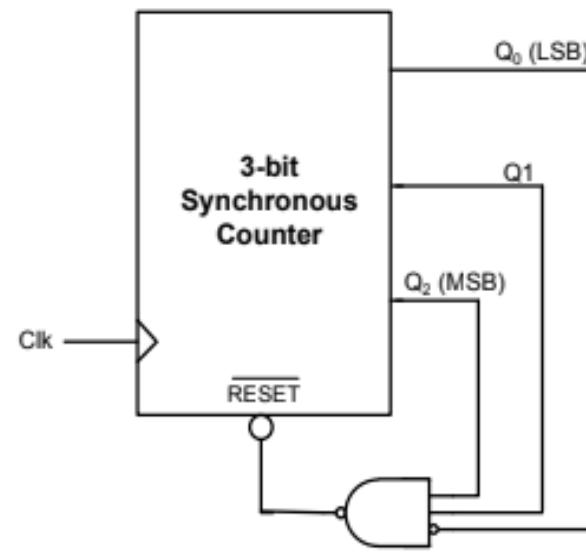
CLK	$Q_D$	$Q_C$	$Q_B$	$Q_A$	R.
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
6+x	0	1	1	0	1
7	0	1	1	1	1
	0	0	0	0	

The figure shows a binary counter with synchronous clear input. With the decoding log shown, the counter works as a



- A. mod-2 counter B. mod-4 counter C. mod-5 counter D. mod-6 counter

For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero.



If the clock (Clk) frequency is 1 GHz, then the counter behaves as a

- (A) mod-5 counter
- (B) mod-6 counter
- (C) mod-7 counter
- (D) mod-8 counter

$$(t_{pd})_{NAND} = 2 \text{ ns}$$

$$f_{CLK} = 1 \text{ GHz}$$

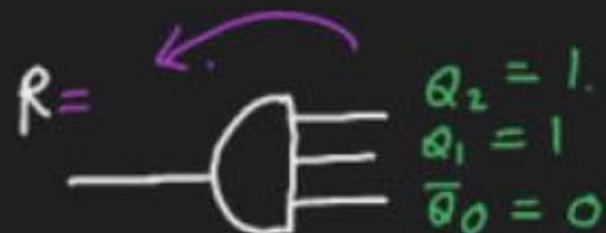
$$T_{CLK} = 1 \text{ ns}$$

$$R = Q_2 Q_1 \overline{Q_0}$$

CK	$Q_2$	$Q_1$	$Q_0$	R
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
→ 6	1	1	0	0
→ 7	1	1	1	0
8	0	0	0	1

$$R = Q_2 Q_1 \overline{Q_0}$$

$$(t_{pd})_{NAND} = 2 \text{ ns.}$$



8ns 6th.

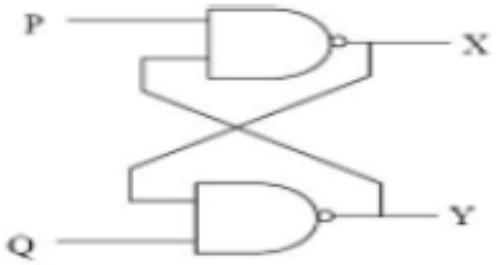
6ns

MOD = 8

# DPP - 7

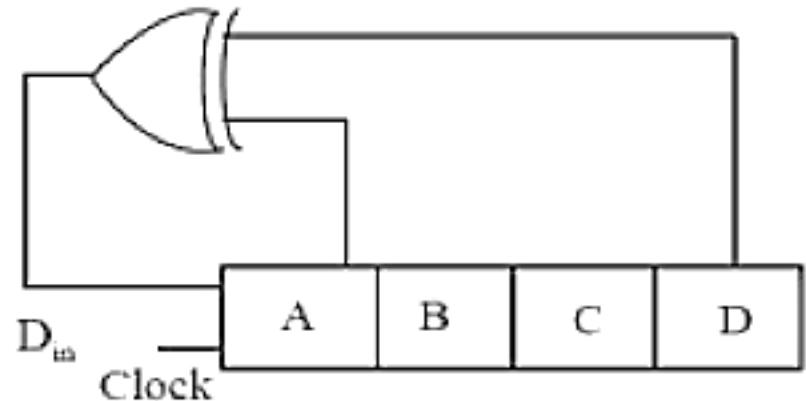
# SEQUENTIAL CKTS

In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is:  $P = Q = '0'$ . If the input condition is changed simultaneously to  $P = Q = '1'$ , the outputs X and Y are



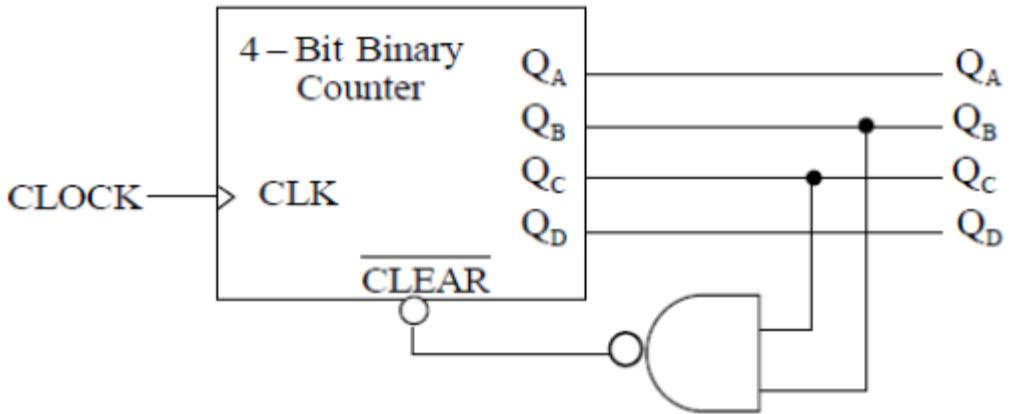
- A.  $X = '1'$ ,  $Y = '1'$
- B. either  $X = '1'$ ,  $Y = '0'$  or  $X = '0'$ ,  $Y = '1'$
- C. either  $X = '1'$ ,  $Y = '1'$  or  $X = '0'$ ,  $Y = '0'$
- D.  $X = '0'$ ,  $Y = '0'$

A 4-bit shift register circuit configured for right-shift operation,  $D_{in} \rightarrow A, A \rightarrow B, B \rightarrow C, C \rightarrow D$ , is shown. If the present state of the shift register is  $ABCD = 1101$ , the number of clock cycles required to reach the state  $ABCD = 1111$  is \_\_\_\_\_.



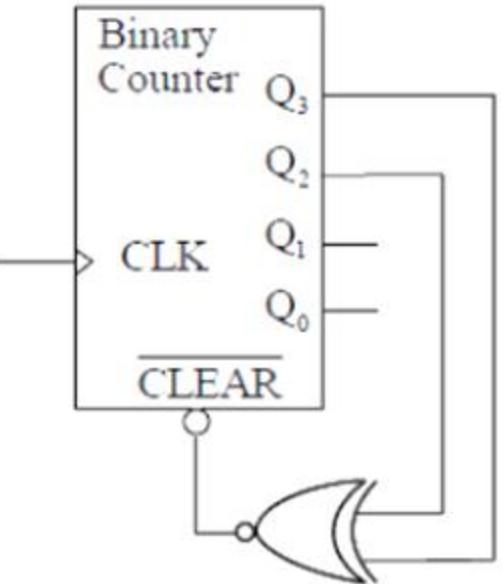
- A. 10
- B. 11
- C. 12
- D. 8

A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure. The value of n is \_\_\_\_\_



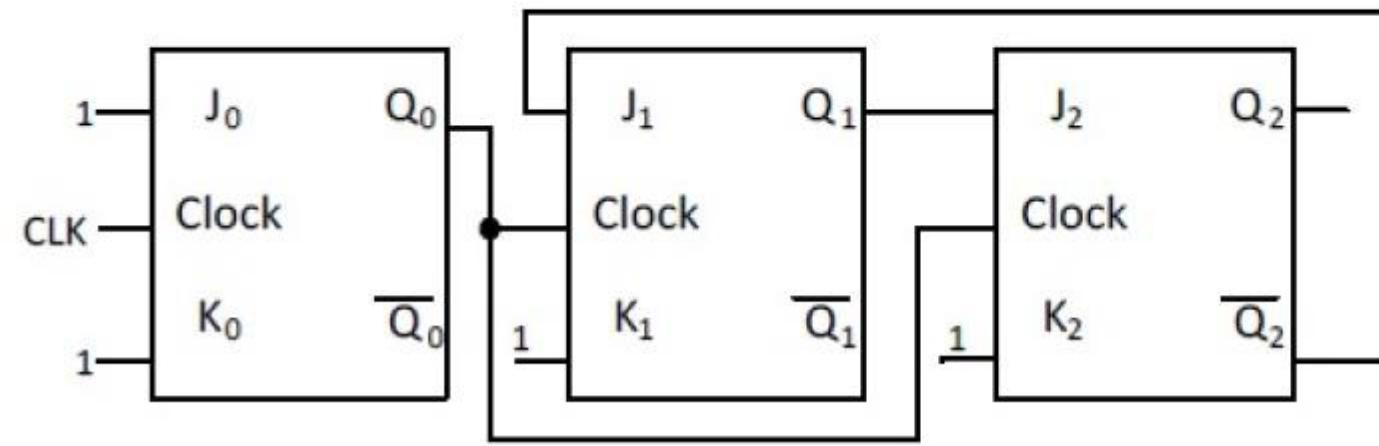
- A. 2 B. 3 C. 5 D. 7

The figure shows a binary counter with synchronous clear input. With the decoding log shown, the counter works as a

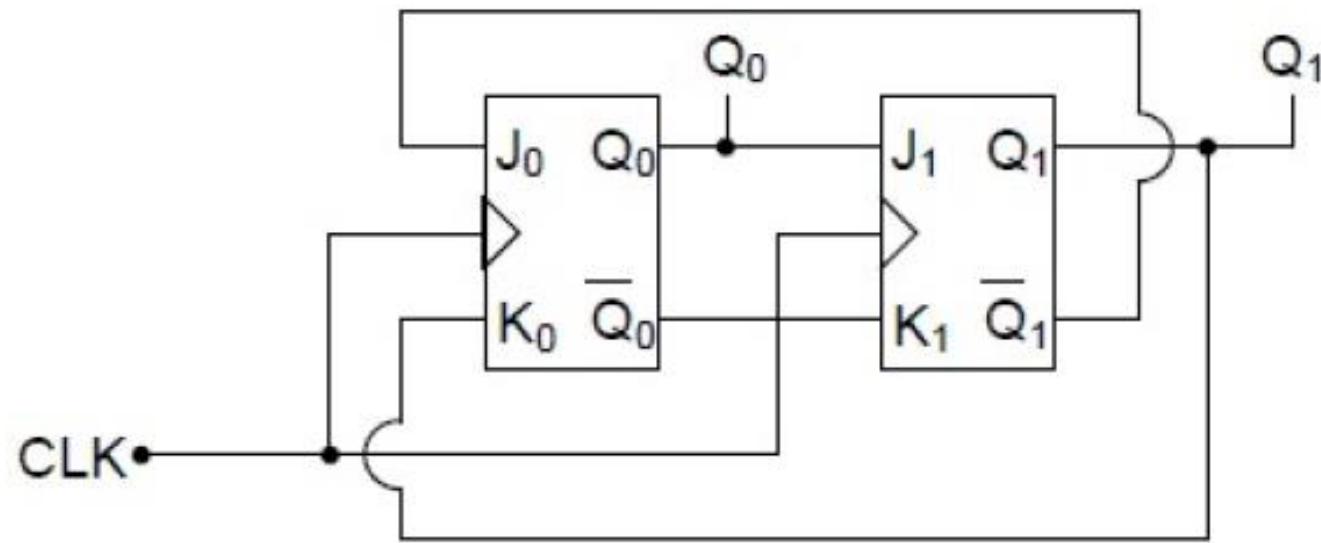


- A. mod-2 counter B. mod-4 counter C. mod-5 counter D. mod-6 counter

The figure shows a digital circuit constructed using negative edge triggered J-K flip flops. Assume a starting state of  $Q_2Q_1Q_0=000$ . This state  $Q_2Q_1Q_0=000$  will repeat after \_\_\_\_\_ number of cycles of the clock CLK.

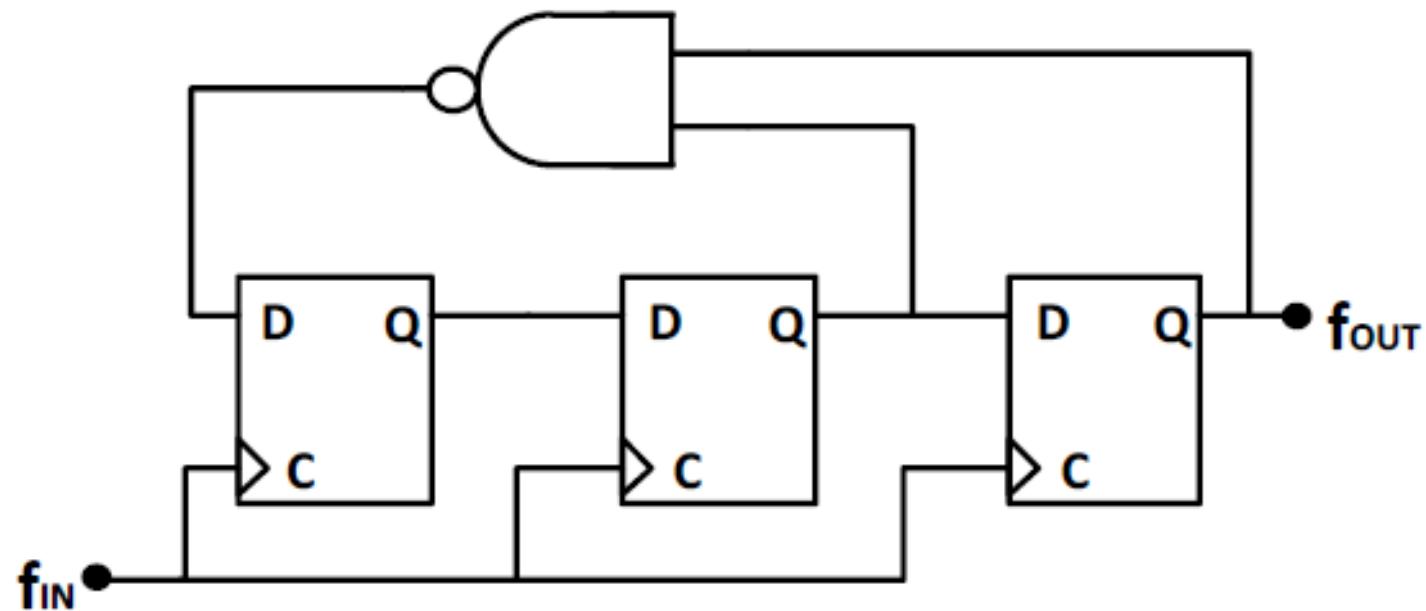


In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is  $Q_1 Q_o = 00$ . The state ( $Q_1 Q_o$ ), immediately after the 333<sup>rd</sup> clock pulse is



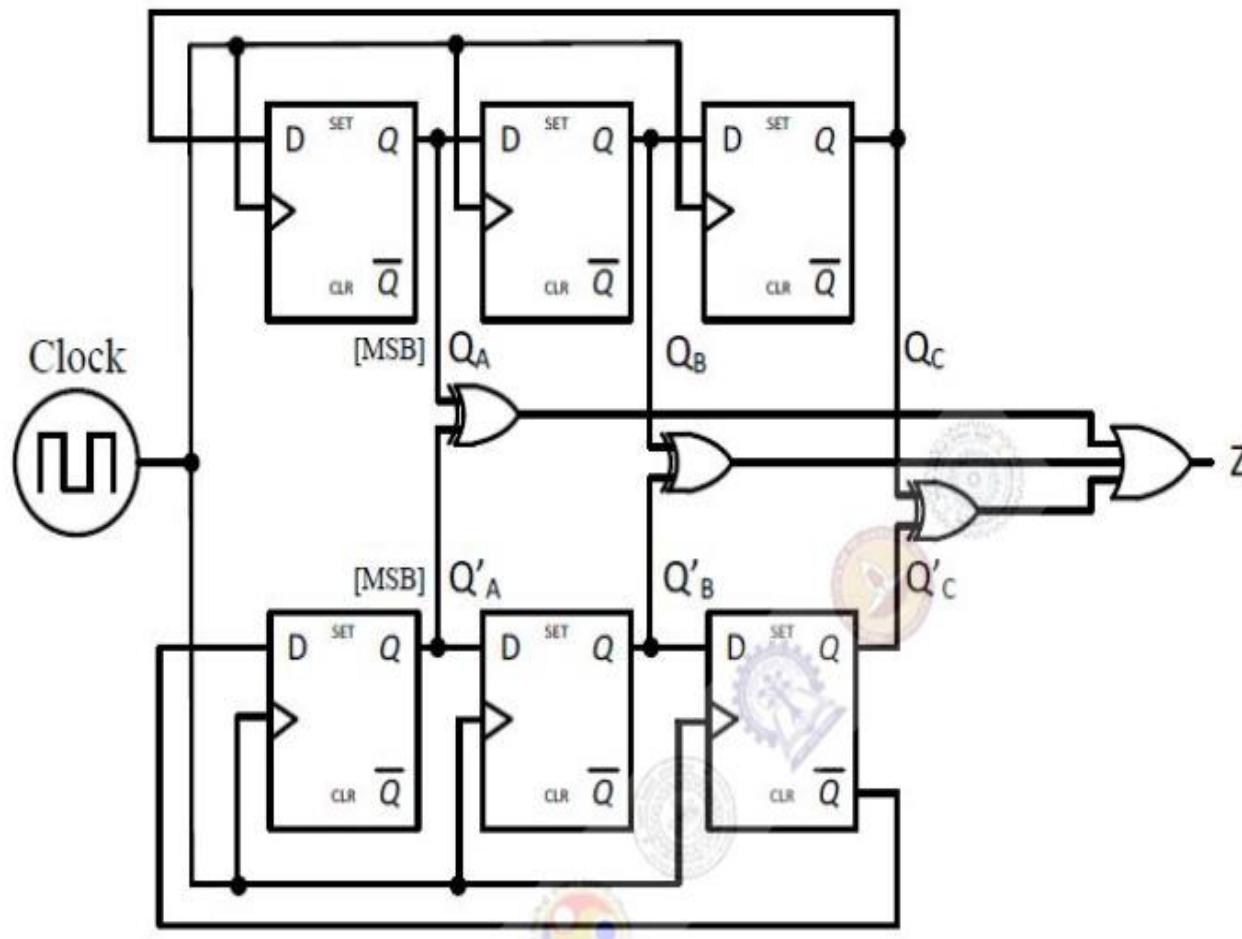
- (A) 00      (B) 01      (C) 10      (D) 11

Which one of the following statements is true about the digital circuit shown in the figure



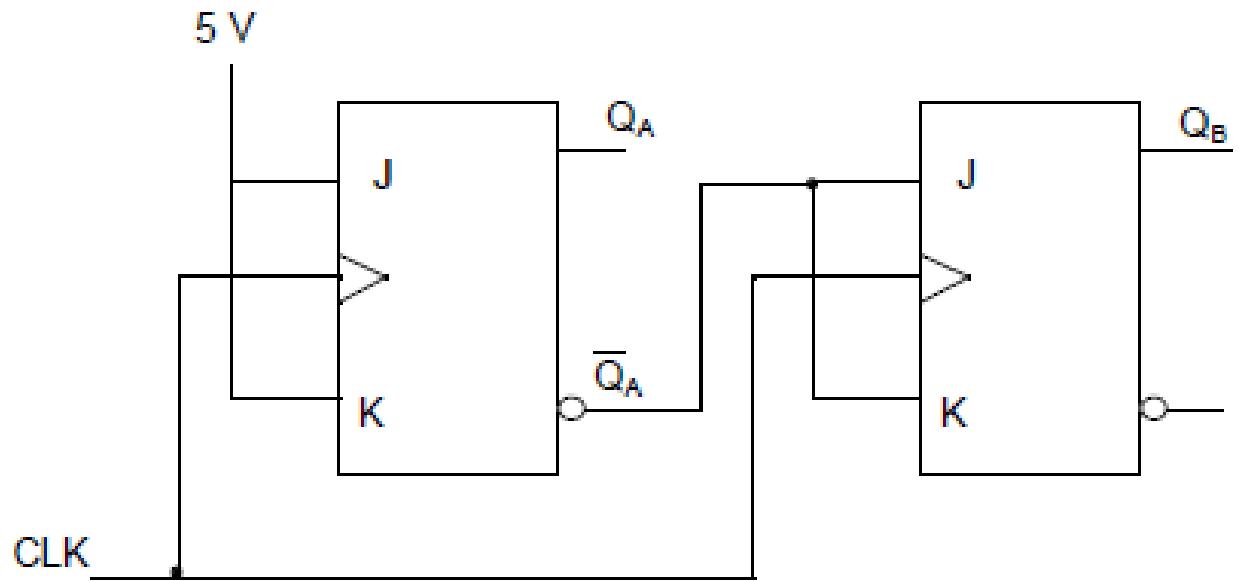
- (A) It can be used for dividing the input frequency by 3.
- (B) It can be used for dividing the input frequency by 5.
- (C) It can be used for dividing the input frequency by 7.
- (D) It cannot be reliably used as a frequency divider due to disjoint internal cycles.

For the synchronous sequential circuit shown below, the output Z is zero for the initial conditions  $Q_A Q_B Q_C = Q'_A Q'_B Q'_C = 100$ .



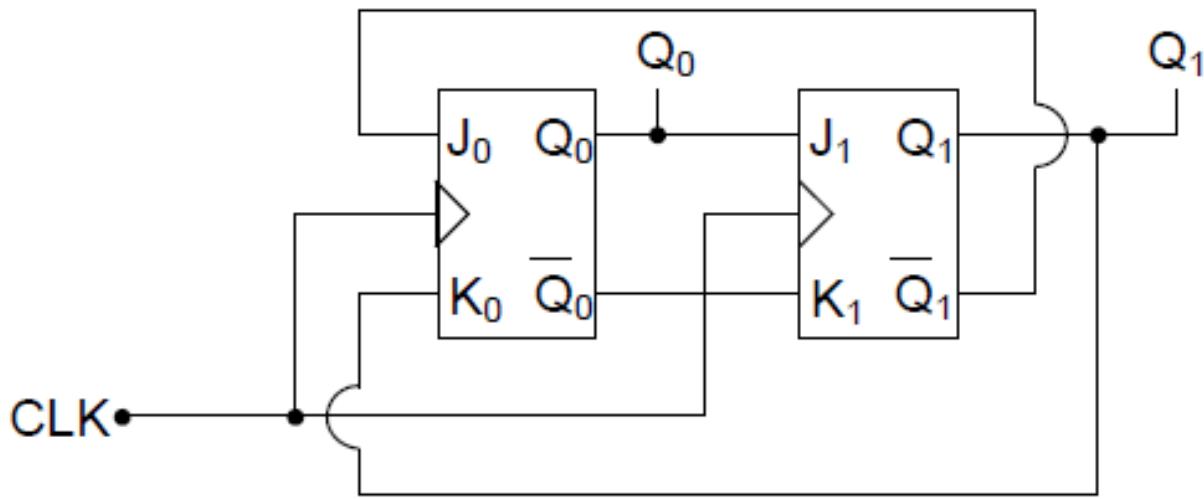
The minimum number of clock cycles after which the output Z would again become zero is

The current state  $Q_A$   $Q_B$  of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of the system is



- (A) 00      (B) 01      (C) 11      (D) 10

In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is  $Q_1 Q_o = 00$ . The state ( $Q_1 Q_o$ ), immediately after the 333<sup>rd</sup> clock pulse is



- (A) 00                    (B) 01                    (C) 10                    (D) 11

Which one of the following statements best describes the operation of a negative-edge-triggered D flip-flop ?

- (a) The logic level at the D input is transferred to Q on NGT of CLK.
- (b) The Q output is always identical to the CLK input if the D input is high.
- (c) The Q output is always identical to the D input when  $\text{CLK} = \text{PGT}$ .
- (d) The Q output is always identical to the D input.

A 3-bit ripple counter is constructed using three T flip-flops to do the binary counting. The three flip-flops have T-inputs fixed at

- (a) 0, 0 and 1
- (b) 1, 0 and 1
- (c) 0, 1 and 1
- (d) 1, 1 and 1

The initial content of a four-bit shift register is 1000. What is the register content after it is shifted four times to the right, with the serial input being 111100 ?

- (a) 1111
- (b) 1100
- (c) 1000
- (d) 0011

A flip-flop is a

- (a) Combinational logic circuit and edge sensitive
- (b) Sequential logic circuit and edge sensitive
- (c) Combinational logic circuit and level sensitive
- (d) Sequential logic circuit and level sensitive

*Statement (I) :*

A basic memory unit of a flip-flop is a bistable multivibrator.

*Statement (II) :*

A flip-flop has two stable states. It remains in one state until it is directed by an input signal to switch over.

If the input to a  $T$  flip-flop is a 100 MHz signal, the final output of three  $T$  flip-flops in a cascade is

- (a) 1000 MHz
- (b) 520 MHz
- (c) 333 MHz
- (d) 12.5 MHz

In a master-slave JK flip-flop

- (a) both master and slave are positive-edge-triggered
- (b) both master and slave are negative-edge-triggered
- (c) master is positive-edge-triggered and slave is negative-edge-triggered
- (d) master is negative-edge-triggered and slave is positive-edge-triggered

In a 4-stage ripple counter, the propagation delay of a flip-flop is 30 ns. If the pulse width of the strobe is 30 ns, the maximum frequency at which the counter operates reliably is nearly

- (a) 9.7 MHz
- (b) 8.4 MHz
- (c) 6.7 MHz
- (d) 4.4 MHz

For what minimum value of propagation delay in each flip-flop will a 10-bit ripple counter skip a count, when it is clocked at 10 MHz?

- (a) 5 ns
- (b) 10 ns
- (c) 20 ns
- (d) 40 ns

A cascaded arrangement of flip-flops, where the output of one flip-flop drives the clock input of the following flip-flop, is known as

- (a) synchronous counter
- (b) ripple counter
- (c) ring counter
- (d) up counter

The number of flip-flops required to construct an 8-bit shift register will be

- (a) 32
- (b) 16
- (c) 8
- (d) 4

Master-Slave flip-flop is also called

- (a) Pulse triggered flip-flop
- (b) Latch
- (c) Level triggered flip-flop
- (d) Buffer

Consider the following statements :

1. Race-around condition occurs in a JK flip-flop when the inputs are 1, 1
2. A flip-flop is used to store one bit of information
3. A transparent latch consists of D-type flip-flops
4. Master-slave configuration is used in a flip-flop to store two bits of information

Which of the above statements are correct ?

- (a) 1, 2 and 3 only
- (b) 1, 2 and 4 only
- (c) 3 and 4 only
- (d) 1, 2, 3 and 4

Consider the following circuits :

1. Full adder
2. Half adder
3. JK flip-flop
4. Counter

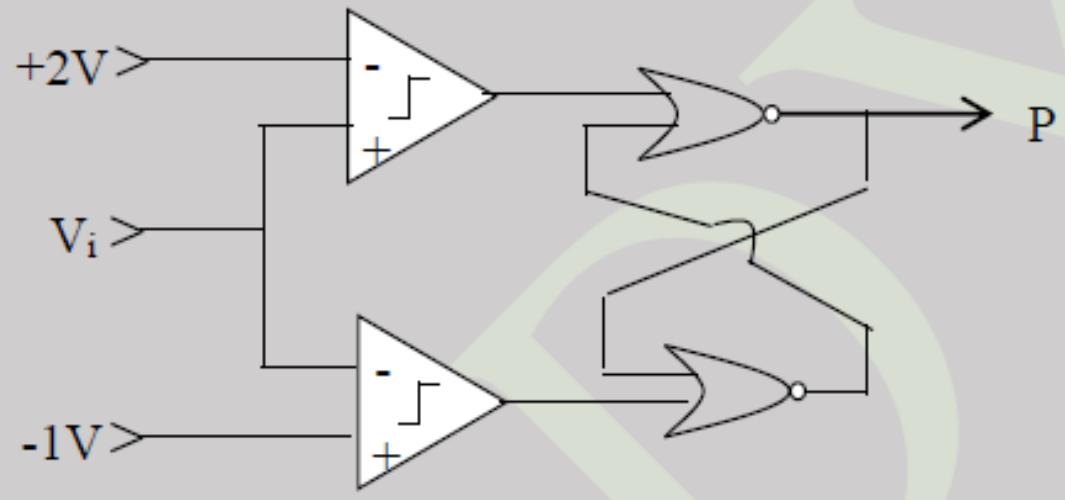
Which of the above circuits are classified as sequential logic circuits ?

- (a) 1 and 2
- (b) 3 and 4
- (c) 2 and 3
- (d) 1 and 4

Choose the correct statements relating to the circuit of figure

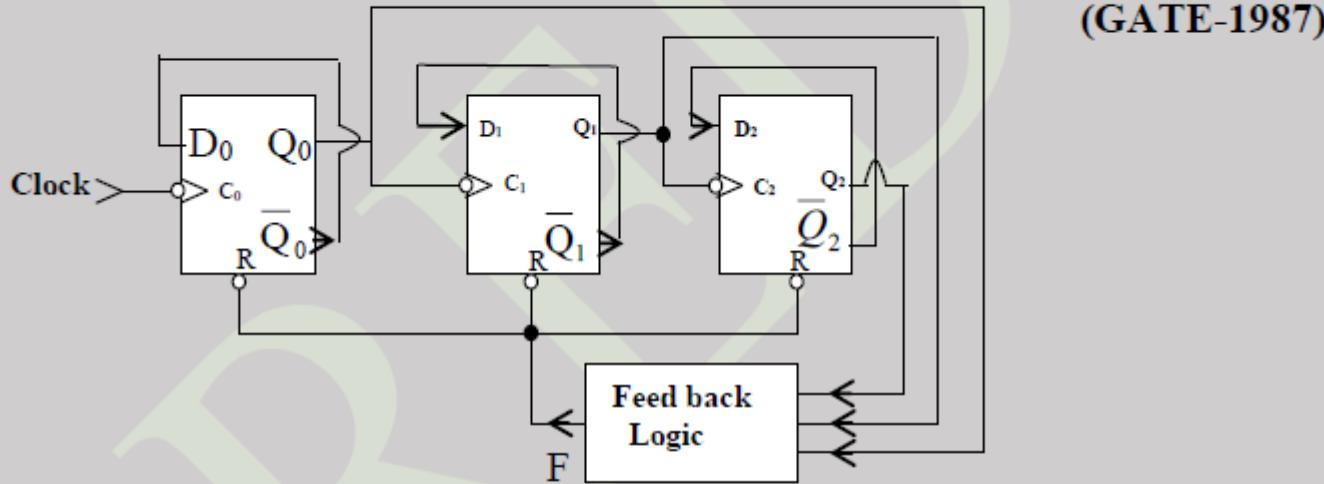
(GATE-1987)

- (a) For  $V_i = -2V$ ,  $P=0$
- (b) For  $V_i = +3V$ ,  $P=0$
- (c) For  $V_i = 0V$ ,  $P = 0$  always
- (d) For  $V_i=0V$ ,  $P$  can be either 0 or 1.

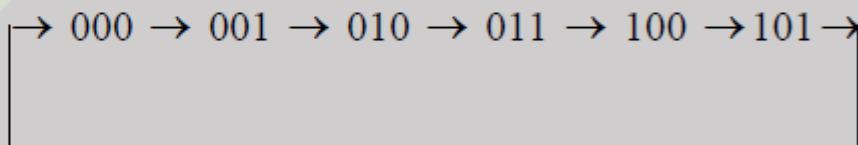


A ripple counter using negative edge-triggered D-flip flops is shown in Fig:A-28. The flipflops are cleared to '0' by a '0' at the R input. The feedback logic is to be designed to obtain the count sequence shown in the same figure. The correct feedback logic is:

(GATE-1987)



**Count sequence in the order of  $Q_2 Q_1 Q_0$ :**



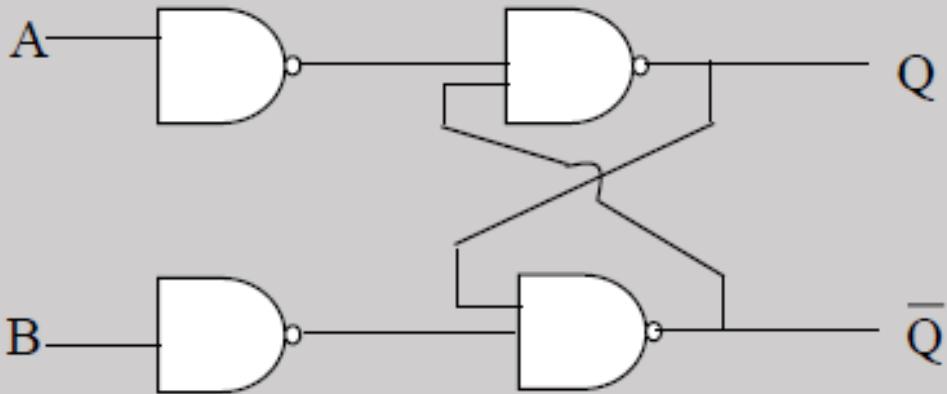
- (a)  $F = \overline{Q_2 Q_1 Q_0}$
- (b)  $F = Q_2 \overline{Q_1} \overline{Q_0}$
- (c)  $F = \overline{Q}_2 \overline{Q}_1 Q_0$
- (d)  $F = \overline{Q}_2 \overline{Q}_1 \overline{Q}_0$

Fig:A-28

The circuit given below is a

(GATE-1988)

- (a) J-K Flip-flop
- (b) Johnson's counter.
- (c) R-S latch
- (d) None of above.



A 4 bit modulo-16 ripple counter uses JK flip-flops. If the propagation delay of each FF is 50ns, the maximum clock frequency that can be used is equal to: (GATE-1990)

- (a) 20 MHz
- (b) 10 MHz
- (c) 5 MHz
- (d) 4 MHz

An S-R FLIP-FLOP can be converted into a T FLIP-FLOP by connecting \_\_\_\_\_ to Q and \_\_\_\_\_ to  $\bar{Q}$ . (GATE-1991)

A pulse train with a frequency of 1MHz is counted using a modulo-1024 ripple-counter built with J-K flip flops. For proper operation of the counter, The maximum permissible propagation delay per flip flop stage is \_\_\_\_\_ nSec. (GATE-1993)

Synchronous counters are \_\_\_\_\_ than the ripple counters.

(GATE-1994)

A switch-tail ring counter is made by using a single D flip-flop. The resulting circuit is a  
**(GATE-1995)**

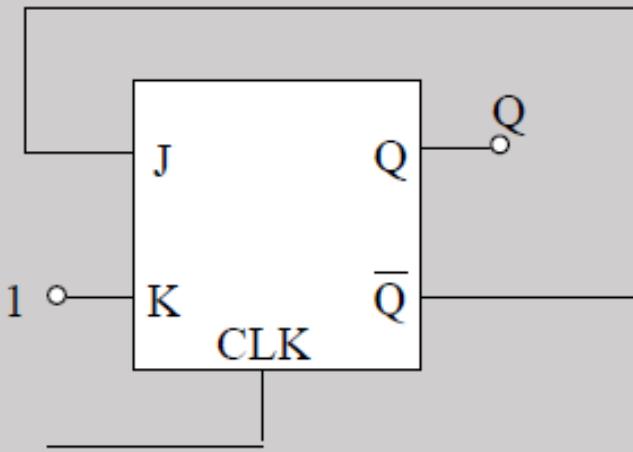
- (a) SR flip-flop
- (b) JK flip-flop
- (c) D flip-flop
- (d) T flip-flop

An R-S latch is

(GATE-1995)

- (a) combinatorial circuit
- (b) synchronous sequential circuit.
- (c) one bit memory element
- (d) one clock delay element.

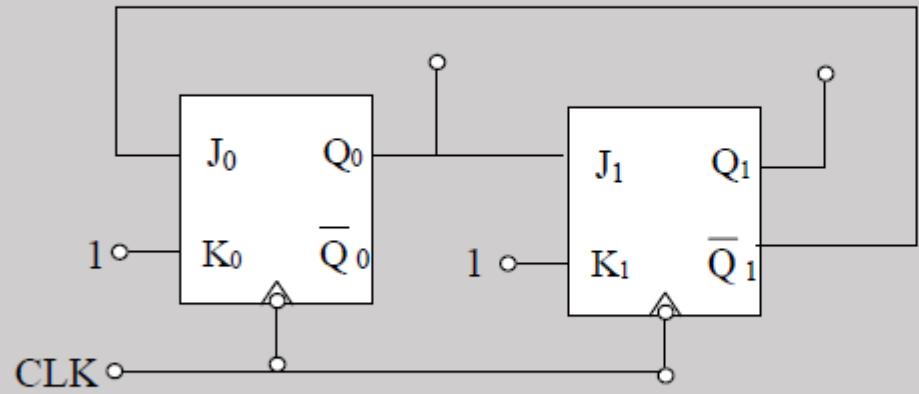
In a J-K flip-flop we have  $J = \bar{Q}$  and  $K=1$  (see figure) Assuming the flip-flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be (GATE-1997)



- (a) 010000
- (b) 011001
- (c) 010010
- (d) 010101

. Figure shows a mod-K counter, Here K is equal to

(GATE-1998)



(a) 1

(b) 2

(c) 3

(d) 4

A 0 to 6 counter consists of 3 flipflops and a combination circuit of 2 input gate(s).

The combination circuit consists of

(GATE-2003)

- (a) one AND gate
- (b) one OR gate
- (c) one AND gate and one OR gate
- (d) two AND gates

A master slave flip-flop has the characteristic that

(GATE-2004)

- (a) change in the input immediately reflected in the output
- (b) change in the output occurs when the state of the master is affected
- (c) change in the output occurs when the state of the slave is affected
- (d) both the master and the slave states are affected at the same time.

Choose the correct one from among the alternatives A, B, C, D after matching an item from Group1 with the most appropriate item in Group2. **(GATE-2004)**

**Group1**

- P. shift register
- Q. Counter
- R. Decoder

**Group2**

- 1. Frequency division
- 2. Addressing in memory chips
- 3. Serial to parallel data conversion

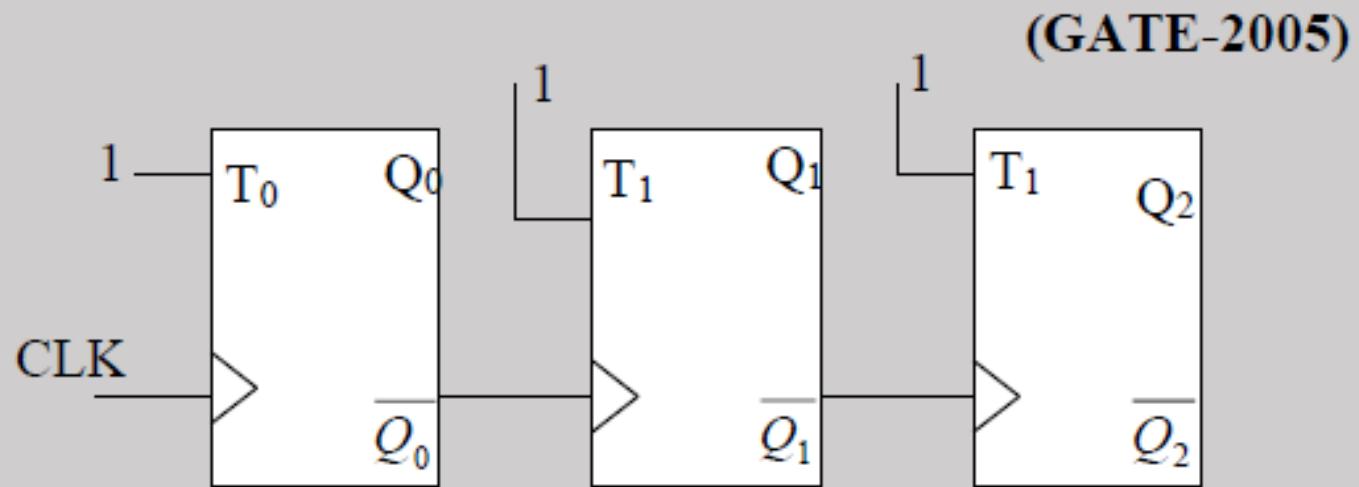
- (a) P-3, Q-2, R-1      (b) P-3, Q-1, R-2      (c) P-2, Q-1, R-3      (d) P-1, Q-3, R-2

The present output  $Q_n$  of an edge triggered JK flipflop is logic 0. If J=1, then  $Q_{n+1}$   
**(GATE-2005)**

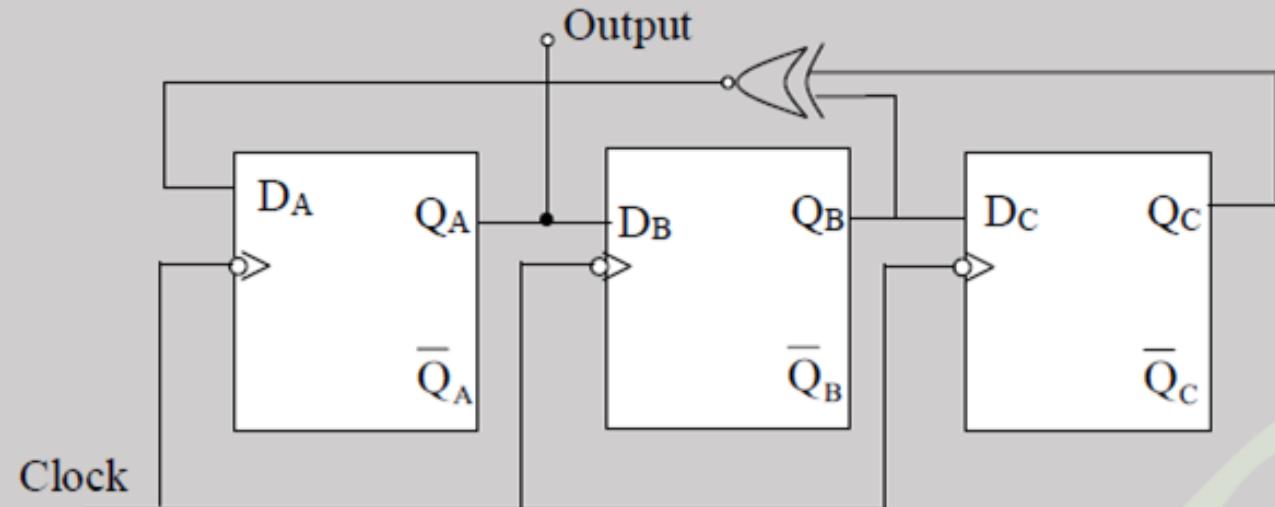
- (a) cannot be determined
- (b) will be logic 0
- (c) will be logic 1
- (d) will race around

The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is  $Q_2Q_1Q_0=011$ , then its next state ( $Q_2Q_1Q_0$ ) Will be

- (a) 010
- (b) 100
- (c) 111
- (d) 101



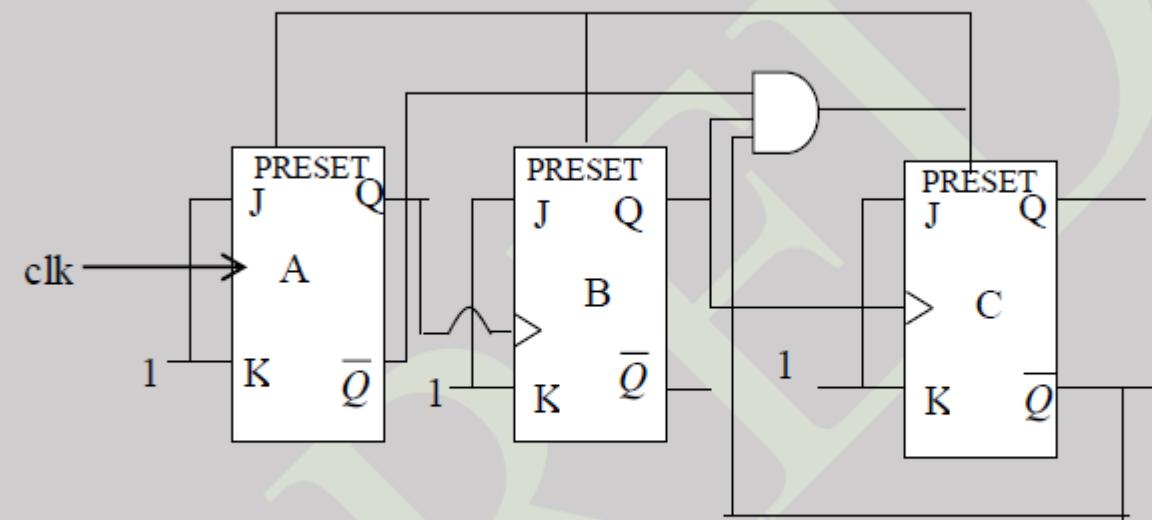
Assuming that all flip-flops are in reset condition initially, the count sequence observed at Q<sub>A</sub> in the circuit shown is (GATE-2010)



- (a) 0010111...    (b) 0001011....    (c) 0101111...    (d) 0110100...

The ripple counter shown in the figure works as a

(GATE-1999)



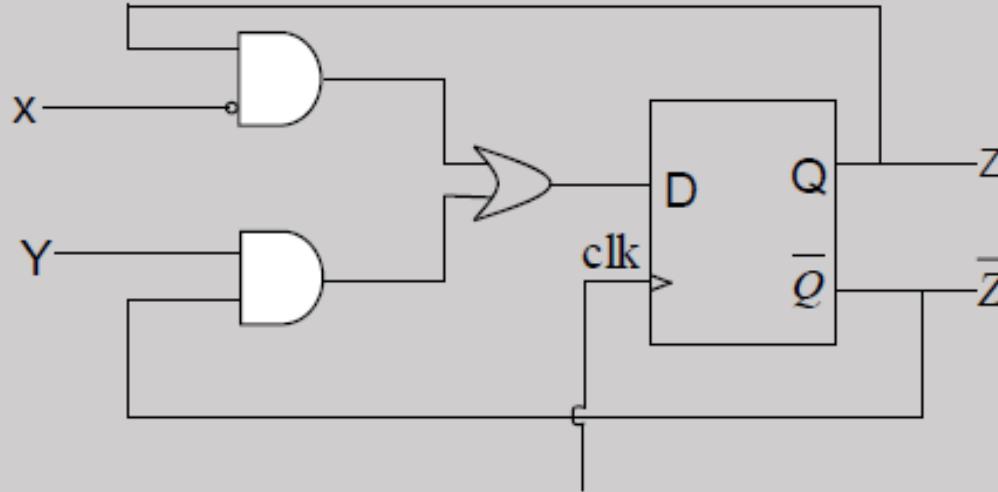
- (a) Mod-3 up counter  
(c) Mod-3 down counter

- (b) Mod-5 up counter  
(d) Mod-5 down counter

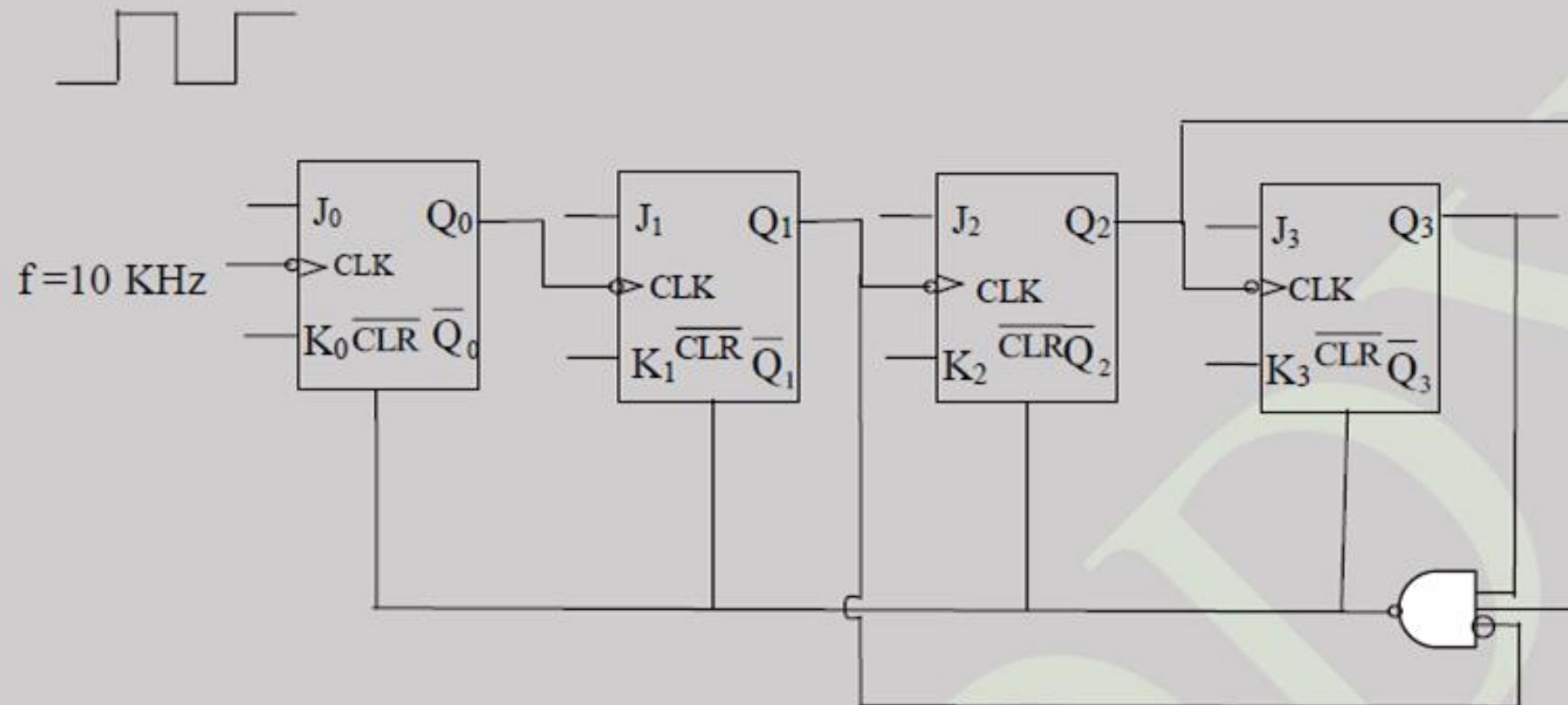
A sequential circuit using D FlipFlop and logic gates is shown in the figure, where X and Y are the inputs and Z is the output. The circuit is

(GATE-2000)

- (a) S-R FlipFlop with inputs X= R and Y=S
- (b) S-R FlipFlop with inputs X= S and Y=R
- (c) J-K FlipFlop with inputs X= J and Y=K
- (d) J-K FlipFlop with inputs X= K and Y=J

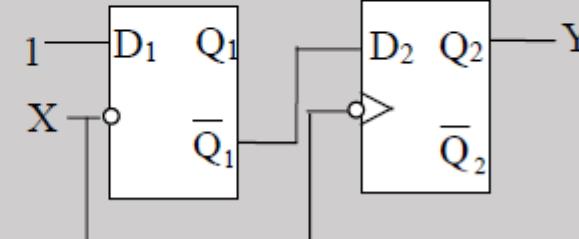
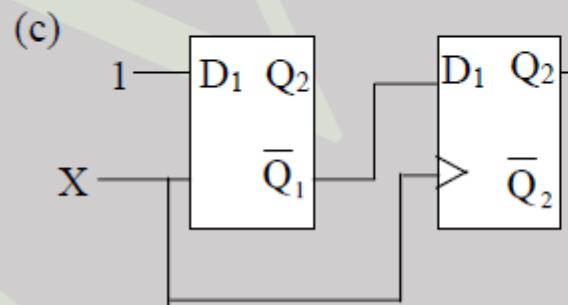
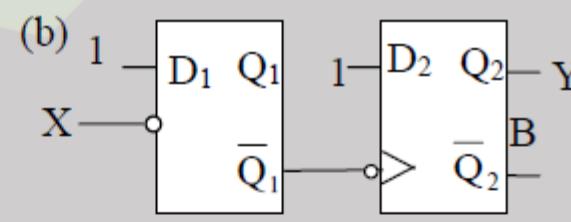
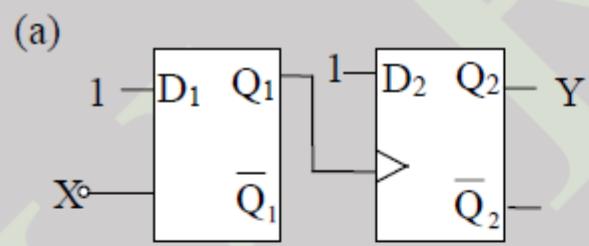
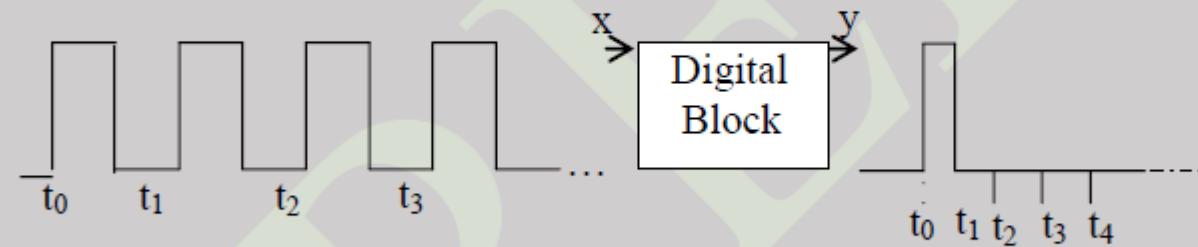


In the figure, the J and K inputs of all the four flipflops are made high. The frequency of the signal at output Y is **(GATE-2000)**



- (a) 0.833KHz      (b) 1.0KHz      (c) 0.91KHz      (d) 0.77KHz

The digital block in the figure is realized using two positive edge triggered D flip-flops. Assume that for  $t < t_0$ ,  $Q_1 = Q_2 = 0$ . The circuit in the digital block is given by  
**(GATE-2001)**

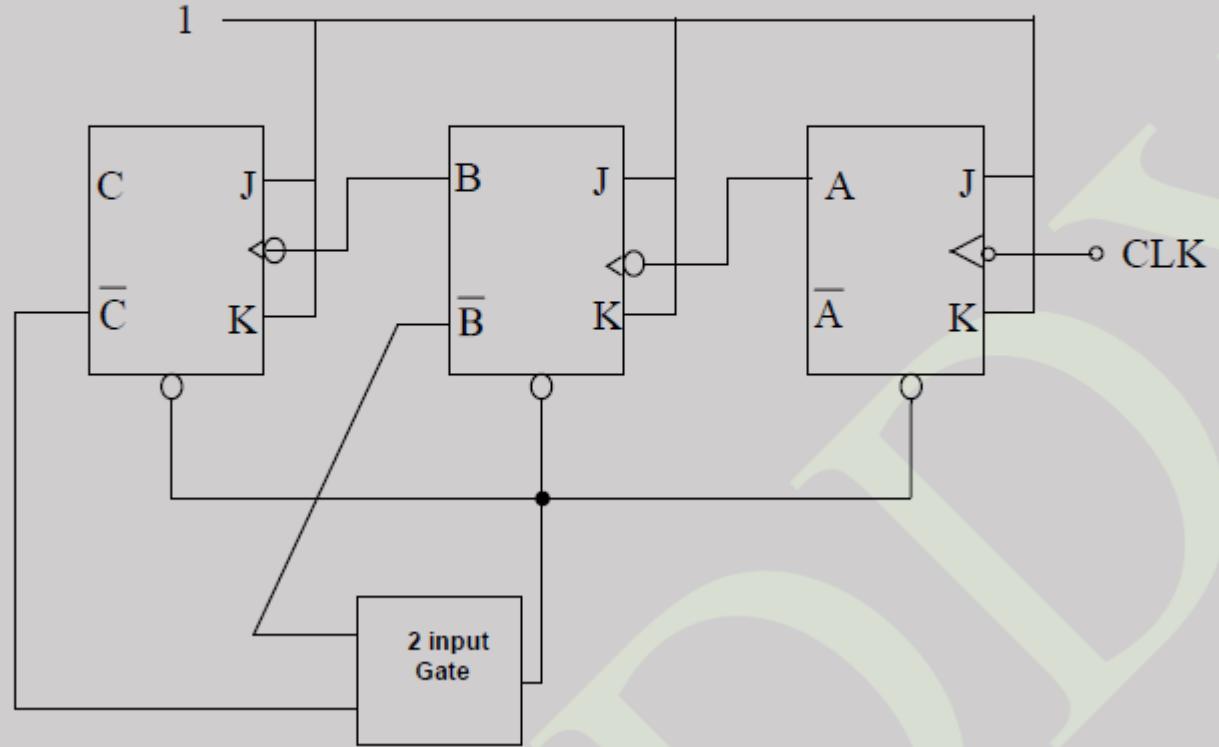


A 4 bit ripple counter and a 4 bit synchronous counter are made using flipflops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, Then **(GATE-2003)**

- (a)  $R = 10\text{ns}$ ,  $S = 40\text{ns}$
- (b)  $R = 40\text{ns}$ ,  $S = 10\text{ns}$
- (c)  $R = 10\text{ns}$ ,  $S = 30\text{ns}$
- (d)  $R = 30\text{ns}$ ,  $S = 10\text{ns}$

In the modulo-6 ripple counter shown in the figure, the output of the 2-input gate is used to clear J-K flipflops. The 2-input gate is (GATE-2004)

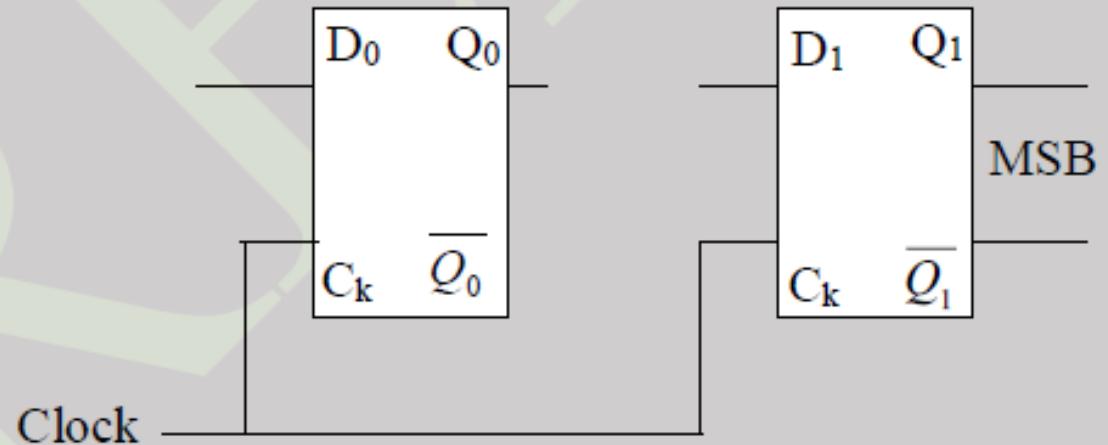
(a) a NAND gate    (b) a NOR gate    (c) an OR gate    (d) an AND gate



Two D-flipflops, as shown below, are to be connected as a synchronous counter that goes through the following  $Q_1Q_0$  sequence  $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow \dots$

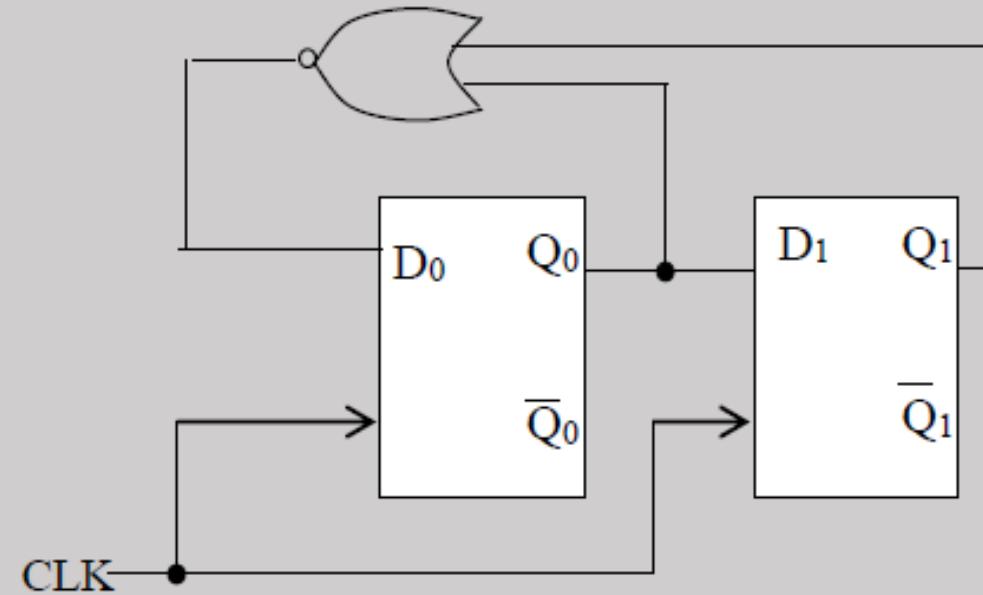
The inputs  $D_0$  and  $D_1$  respectively should be connected as **(GATE-2006)**

- (a)  $\overline{Q_1}$  and  $Q_0$
- (b)  $\overline{Q_0}$  and  $Q_1$
- (c)  $\overline{Q_1}Q_0$  and  $\overline{Q_1}Q_0$
- (d)  $\overline{Q_1}\overline{Q_0}$  and  $Q_1Q_0$



For the circuit shown, the counter state ( $Q_1Q_0$ ) follows the sequence

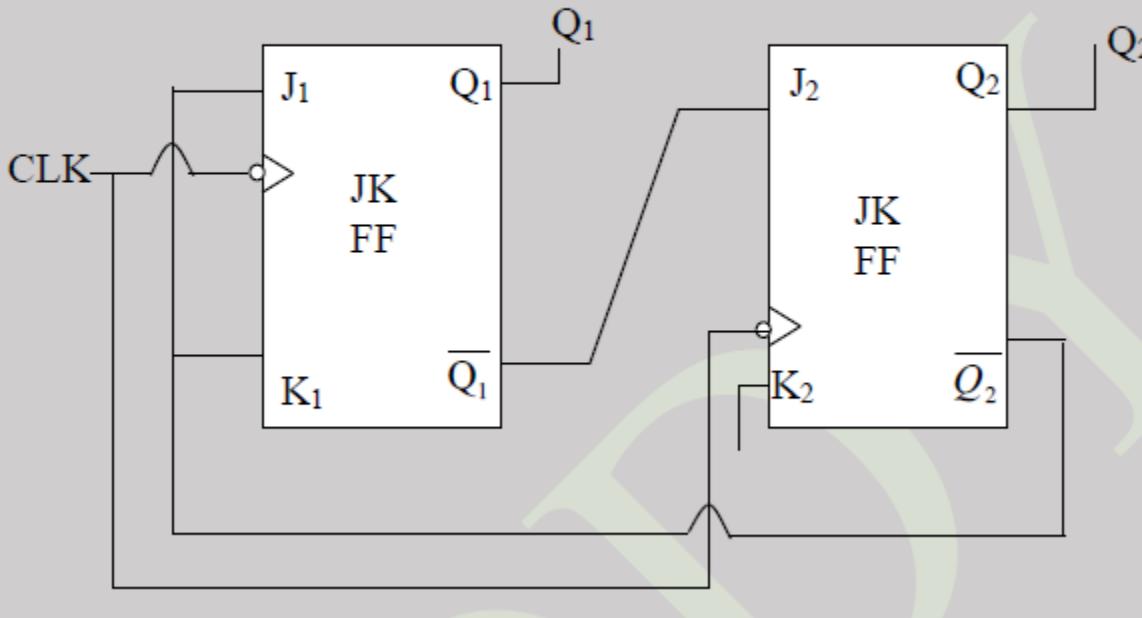
- (a) 00,01,10,11,00.....
- (b) 00,01,10,00,01.....
- (c) 00,01,11,00,01.....
- (d) 00,10,11,00,10.....



What are the counting states  $(Q_1, Q_2)$  for the counter shown in the figure below?

(GATE-2009)

- (a) 11, 10, 00, 11, 10,.....
- (b) 01,1011,00,01.....
- (c) 00,11,01,10,00.....
- (d) 01,10,00,01,10.....



A 2-input up/down synchronous counter using two toggle flip-flops is shown in Fig:B-11. The counter's sequence is to be controlled by the input M as follows:

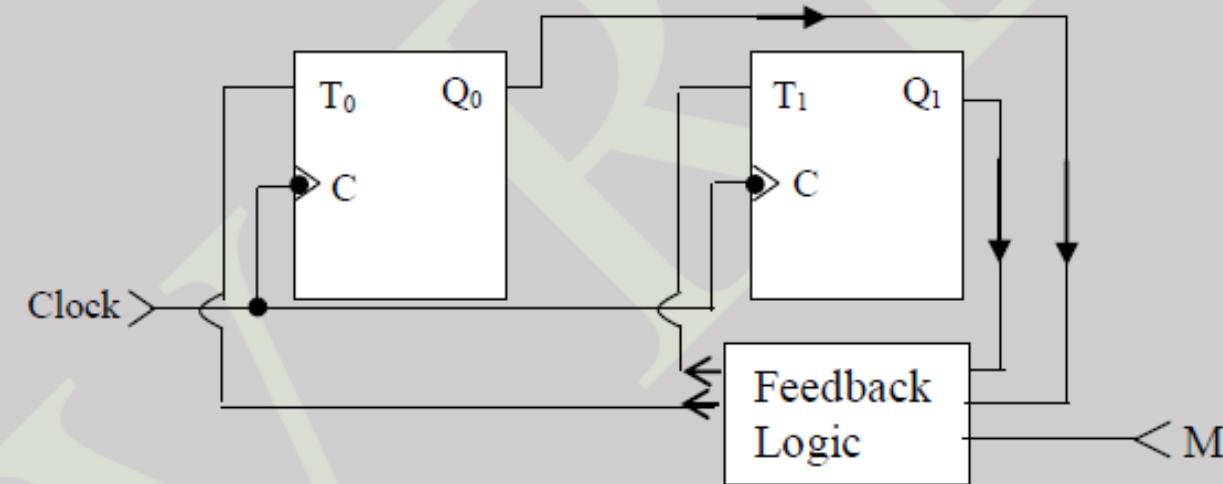
For  $M=1$ , sequence of  $Q_1, Q_0$  is ..00, 01, 10, 11, 00, 01.....

For  $M=0$ , sequence of  $Q_1, Q_0$  is ..00, 11, 10, 01, 00, 11.....

a) Design the necessary feedback logic for  $T_1$  and  $T_0$ .

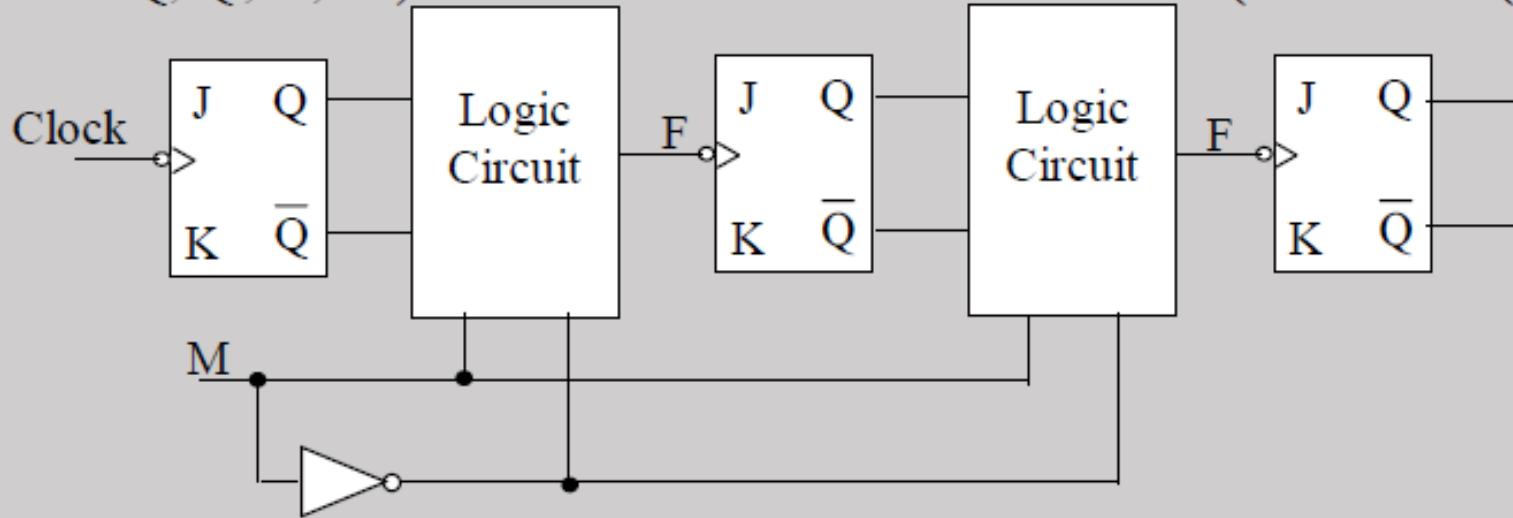
b) Realize the feedback logic using inverters and 4-input multiplexers only. Use  $Q_1$  and  $Q_0$  as the control inputs of the multiplexer with  $Q_1$  as the MSB.

(GATE-1987(8 M))



The circuit shown below uses TTL flip - flops. The flip-flops are triggered at the negative transistors of the clock. It is desired that when  $M = 1$  the circuit should function as an up-counter (in 8421 BCD) and when  $M=0$ , as a down-counter. Design the combinational circuit interposed between the flip-flops so that the circuit works as desired. (i.e. find  $F$  as a function of  $Q$ ,  $\bar{Q}$ ,  $M$ ,  $\bar{M}$ ).

(GATE-1988(8M))



A new clocked “X-Y” flip-flop is defined with two inputs, X and Y in addition to the clock input. The flip-flop functions as follows:

If XY = 00, the flip-flop changes state with each clock pulse.

If XY = 01, the flip-flop state Q becomes 1 with the next clock pulse

If XY = 10, the flip-flop state Q becomes 0 with the next clock pulse.

If XY = 11, no change of state occurs with the clock pulse.

- (a) Write the Truth table for the X-Y flip-flop
- (b) Write the Excitation table for the X-Y flip-flop
- (c) It is desired to convert a J-K flip-flop into the X-Y flip-flop by adding some external gates, if necessary. Draw a circuit to show how you will implement the X-Y flip-flop using a J-K flip-flop.

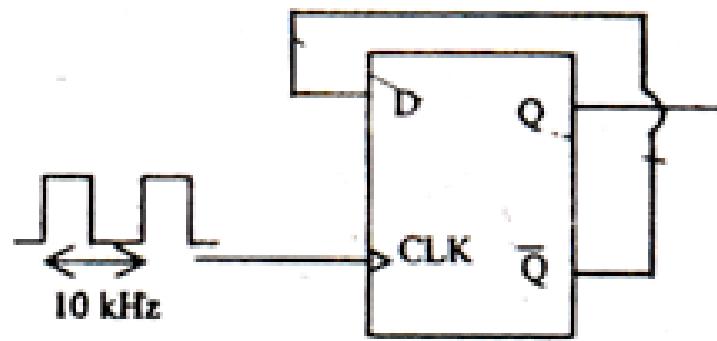
**(GATE-1992(8 M))**

For a J-K flip-flop its J input is tied to its own Q output and its K input is connected to its own Q output. If the flip-flop is fed with a clock of frequency 1 MHz, its Q output frequency will be \_\_\_\_\_.

(GATE – EE – 1995)

The frequency of the clock signal applied to the rising edge triggered D flip-flop shown in Fig. is 10 kHz. The frequency of the signal available at Q is (GATE – EE – 2002)

- (a) 10 kHz
- (b) 2.5 kHz
- (c) 20 kHz
- (d) 5 kHz



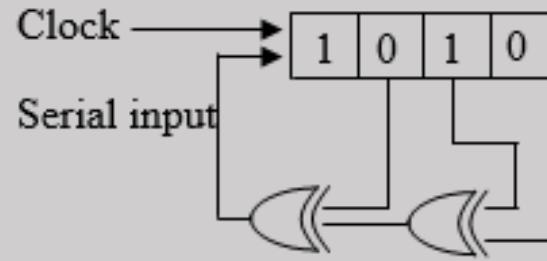
The shift register shown in fig. is initially loaded with the bit pattern 1010. Sequential ckts. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). After how many clock pulses will the content of the shift register become 1010 again?

(a) 3

(b) 7

(c) 11

(d) 15

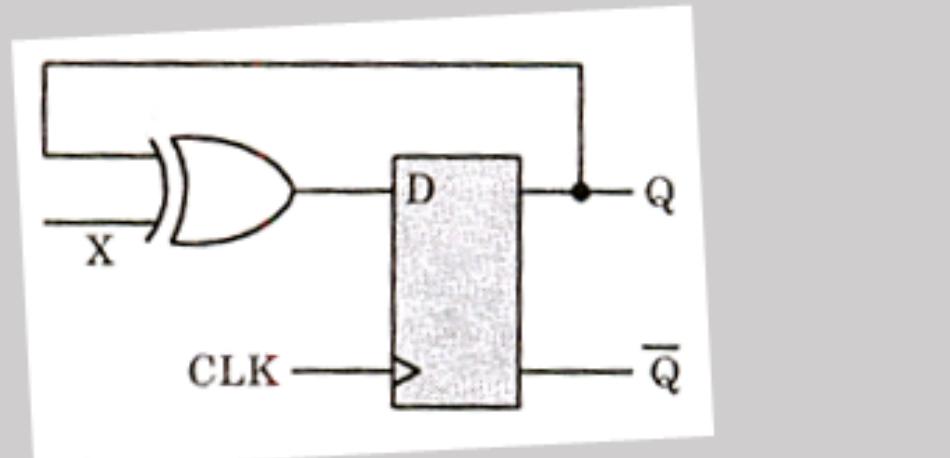


**(GATE – EE – 2003)**

The digital circuit shown in the figure works as a

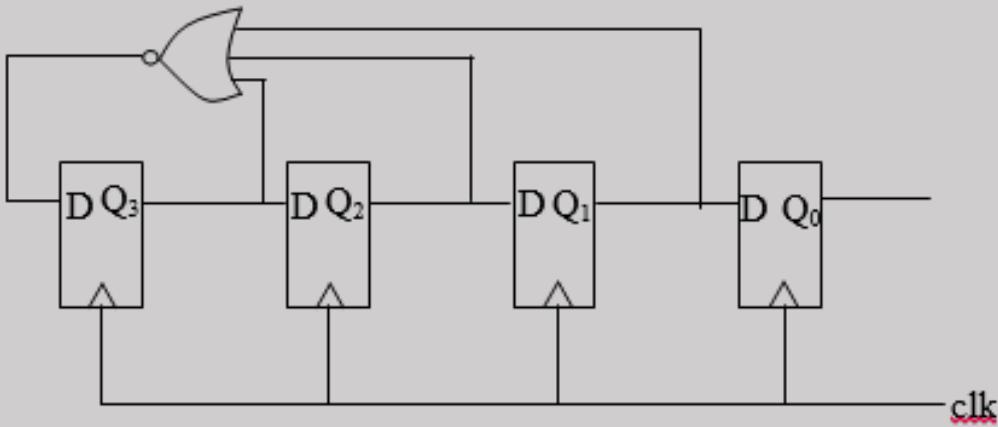
(GATE – EE – 2005)

- (a) JK flip-flop
- (b) Clocked RS flip-flop
- (c) T flip-flop
- (d) Ring counter



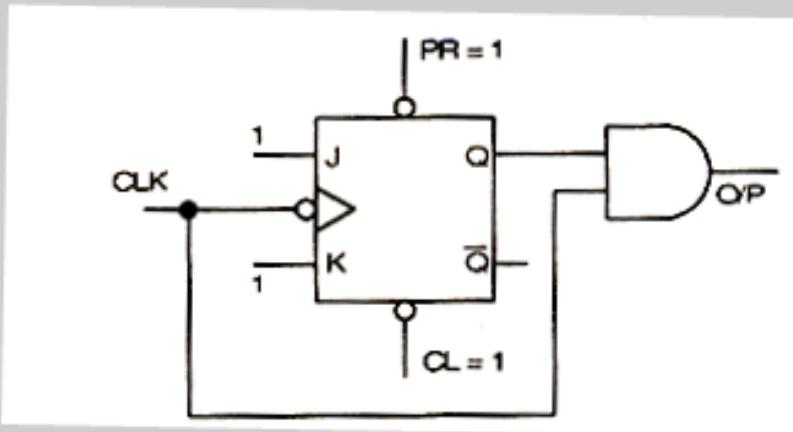
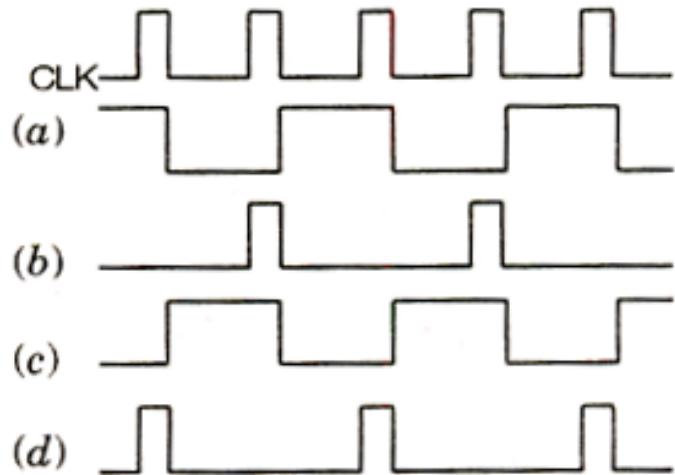
For the ring counter shown in Fig., find the steady state sequence if the initial state of the counter is 1110(i.e.,  $Q_3Q_2Q_1Q_0=1110$ ). Determine the MOD number of the counter.

| (GATE – EE – 2001)

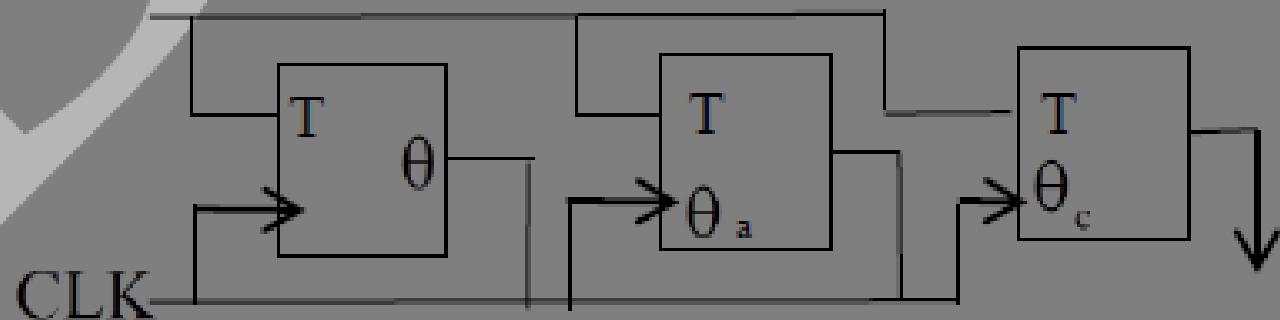


The digital circuit shown in Fig. Q. 68 generates a modified clock pulse at the output. Choose the correct output waveform from the options given below.

(GATE – EE – 2004)



01. Find radix of the system shown in the figure below: (IES-1991)



- (a) 2
- (b) 4
- (c) 6
- (d) 8

The race around condition exists in J – K flip flop if

(IES-1992)

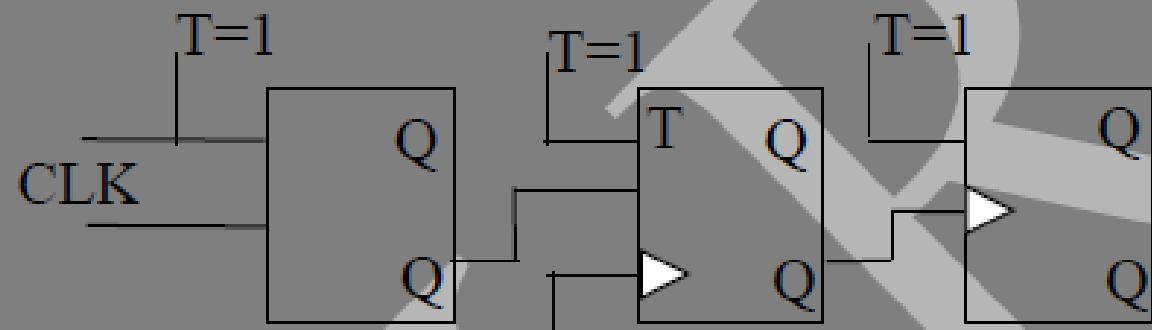
- (a)  $J = 0; K = 1$
- (b)  $J = 0; K = 1$
- (c)  $J = 0; J = 0$
- (d)  $J = 1; K = 1$

In a JK flip – flop, the output  $Q_n$  is 1 and it does not change when a clock pulse applied.  
The possible combination of  $J_n$  and  $K_n$  could be (x denotes don't care).

(IES-1992)

- (a) x and 0
- (b) x and 1
- (c) 0 and x
- (d) 1 and x

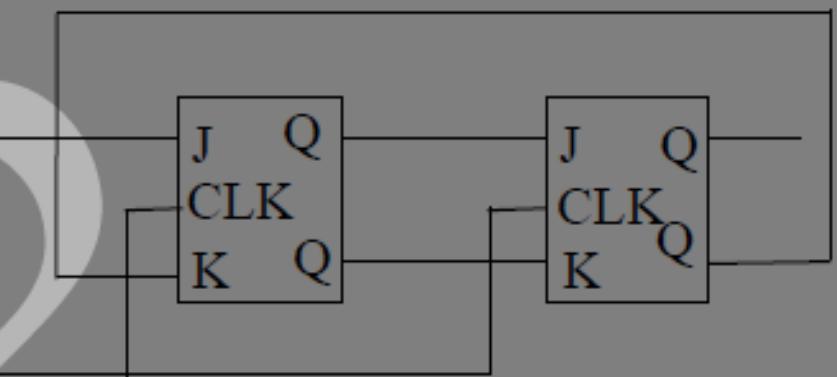
05. Which type of counter is shown in the figure  
(IES-1992)



- (a) Synchronous
- (b) Johnson
- (c) Ring
- (d) None

06. The circuit shown below is:

(IES-1992)



- (a) 2:1 scalar
- (b) 4:1 scalar
- (c) Up – down counter
- (d) None

The difference between sequential and combinational circuit is that  
**(IES-1992)**

- (a) Combinational circuits store bits
- (b) Combinational circuits have memory
- (c) Sequential circuits store bits
- (d) Sequential circuits have memory

Which of the following flip-flop cannot be converted to D-type (delay) flip-flop  
**(IES-1992)**

- (a) S – R flip flop
- (b) J – K flip flop
- (c) Master slave flip – flop
- (d) None of the above

Which of the following is not a characteristic of a flip – flop?

(IES-1992)

- (a) The flip – flop is a bistable device with only two stable states
- (b) The flip – flop has two input signals
- (c) The flip – flop has two output signals
- (d) The outputs are complement of each other.

Which of the following statements are correct?

(IES-1993)

1. A flip – flop is used to store 1 – bit of information.
2. Race – around condition occurs in a J – K flip – flop to store 2 – bits of information.
3. Master – slave configuration is used in flip – flops to store 2 – bits of information.
4. A transparent latch consists of a D – type flip – flop.

Select the correct answer using the codes given below:

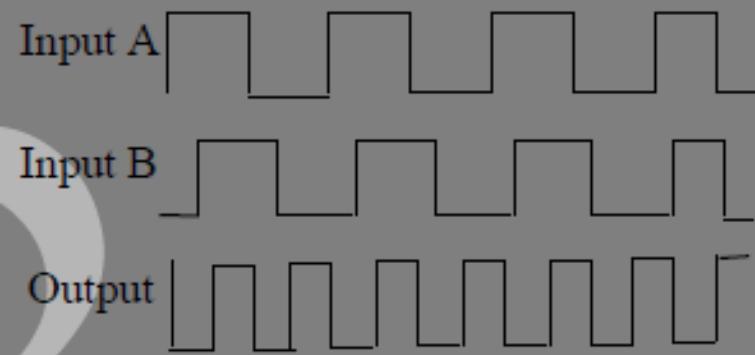
- (a) 1,2 and 3      (b) 1,3 and 4  
(c) 1,2 and 4      (d) 2,3 and 4

Which one of the following can be used to change data from spatial code to temporal code?(IES-1993)

- (a) Shift registers
- (b) Counters
- (c) A/D converters
- (d) Combinational circuits

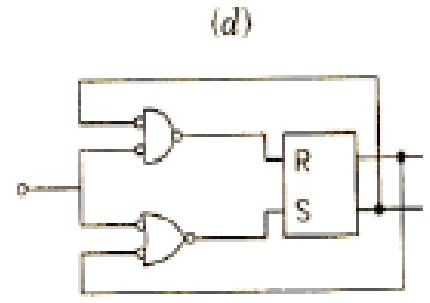
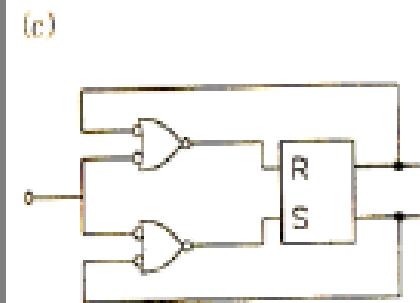
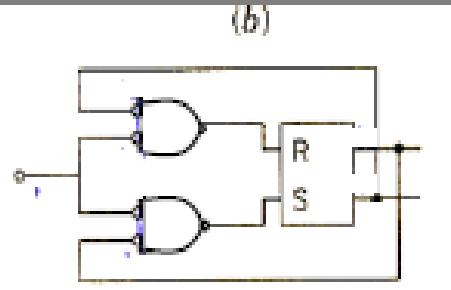
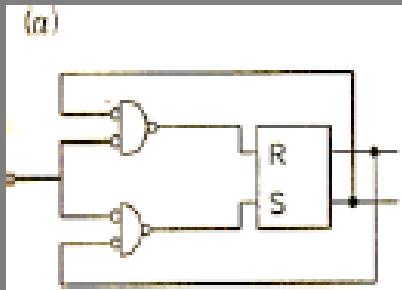
If the input and signals of a black box are as given in the following figure then the black box is a/an

(IES-1994)



- (a) Coincidence circuit
- (b) EX OR circuit
- (c) JK Flip Flop
- (d) R-S Flip Flop

Which one of the following circuits converts an RS Flip Flop to T Flip Flop?  
**(IES-1994)**



The Q output of a J-K FLIP\_FLOP is ‘1’. The pulse is applied. The inputs J and K will be state)(IES-1994)

- (a) 0 and x
- (b) x and 0
- (c) 1 and 0
- (d) 0 and 1

output does not change when a clock-pulse respectively (where ‘x’-don’t care

(IES-1994)

Q. A divide-by-78 counter can be realized by using

- (a) 6 nos of mod-13 counters
- (b) 13 nos of mod-6 counters
- (c) one mod-13 counter followed by one mod- 6 counters
- (d) 13 nos of mod-13 counters

In a sequential circuits, the output at any instant of time depend(IES-1994)

- (a) only on the inputs present at that instant of time
- (b) on past output as well as present inputs
- (c) only on the past inputs
- (d) only on the past outputs

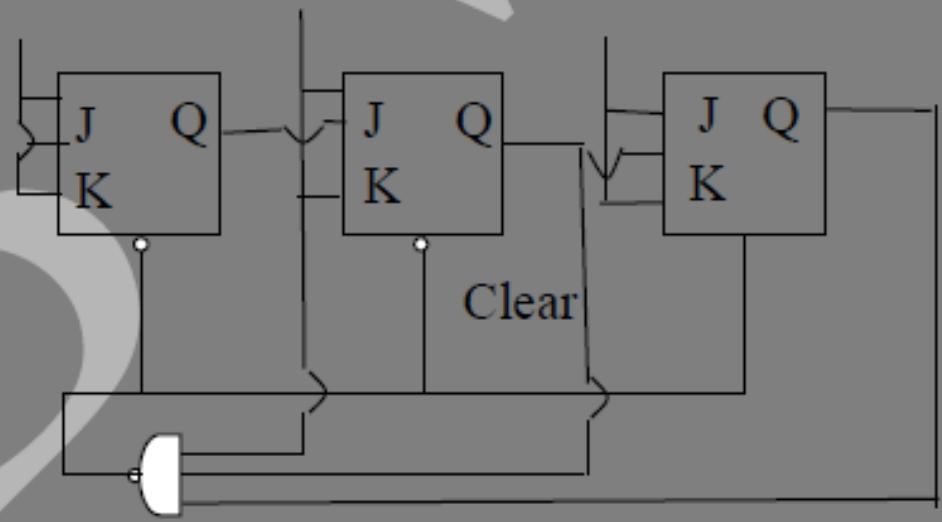
A bit synchronous counter uses flip-flops with propagation delay time of 15ns each. The maximum possible time required for change of state will be

(IES-1994)

- (a) 15 ns
- (b) 30 ns
- (c) 45 ns
- (d) 60 ns

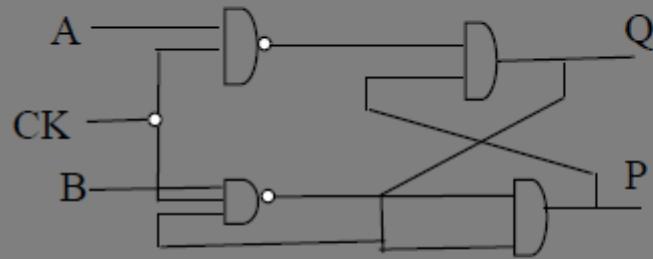
18. The block diagram shown in the given figure represents

(IES-1994)



- (a) modulo-3 ripple counter
  - (b) modulo-5 ripple counter
  - (c) modulo-7 ripple counter
  - (d) modulo-7 synchronous counter

19. Given  $A = 1$ ,  $B = 1$ ,  $Q_n = 0$  and  $P_n = 1$ , what will be output  $Q_{n+1}$  and  $P_{n+1}$  when the clock input (CK) is applied? (IES-1995)



- (a)  $Q_{n+1}=0$ ,  $P_{n+1}=0$
- (b)  $Q_{n+1}=0$ ,  $P_{n+1}=1$
- (c)  $Q_{n+1}=1$ ,  $P_{n+1}=0$
- (d)  $Q_{n+1}=1$ ,  $P_{n+1}=1$

20. Which of the following characteristics are necessary for a sequential circuit?

(IES-1995)

1. It must have at least six gates.
2. It must have some feedback.
3. Its output should depend on some past value.

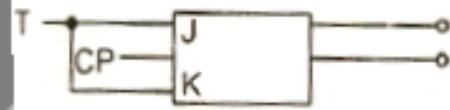
**Codes:**

- (a) 1,2 and 3      (b) 1 and 2  
(c) 2 and 3      (d) 1 and 3

21. Which one of the circuits given below converts a JK F/F to a T F/F?

(IES-1995)

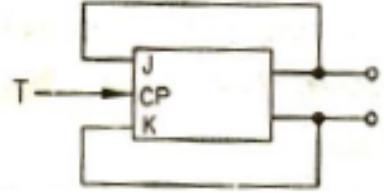
(a)



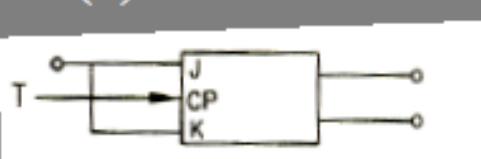
(b)



(c)



(d)

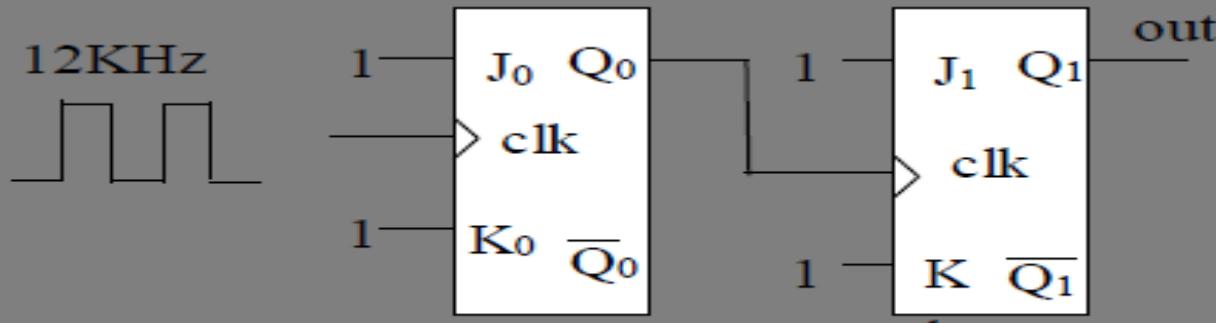


22. A 1 m sec pulse can be converted into a 10 m sec pulse by using(IES-1995)

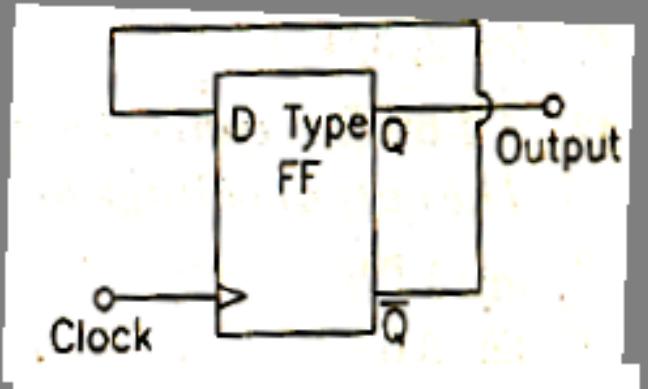
- (a) An astable multivibrator
- (b) A monostable multivibrator
- (c) A bistable multivibrator
- (d) A J – K flip – flop

An input frequency of 12 KHz is applied to the J – K flip – flops arrangement shown in the given figure. The resulting output frequency will be (IES-1995)

- (a) 24 KHz
- (b) 12 KHz
- (c) 6 KHz
- (d) 3 KHz

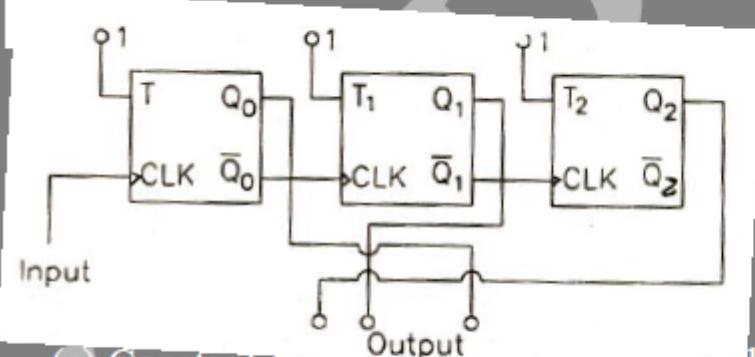


For the circuit shown in the given figure, the frequency of the output Q will be  
**(IES-1996)**



- (a) Twice the input clock frequency
- (b) Half the input clock frequency
- (c) Same as the input clock frequency
- (d) Inverse of the propagation delay of the EF

25. The input pulses to the different stages of the counter shown in the following figure must be of (IES-1996)



- (a) Constant frequency and constant width
- (b) Constant frequency but variable width
- (c) Variable frequency but constant width
- (d) Variable frequency as well as variable width

26. State transition table and state transition diagrams from part of the design steps is the case of (IES-1996)

- (a) Combinational circuits
- (b) Amplifier circuits
- (c) Delay circuits
- (d) Sequential circuits

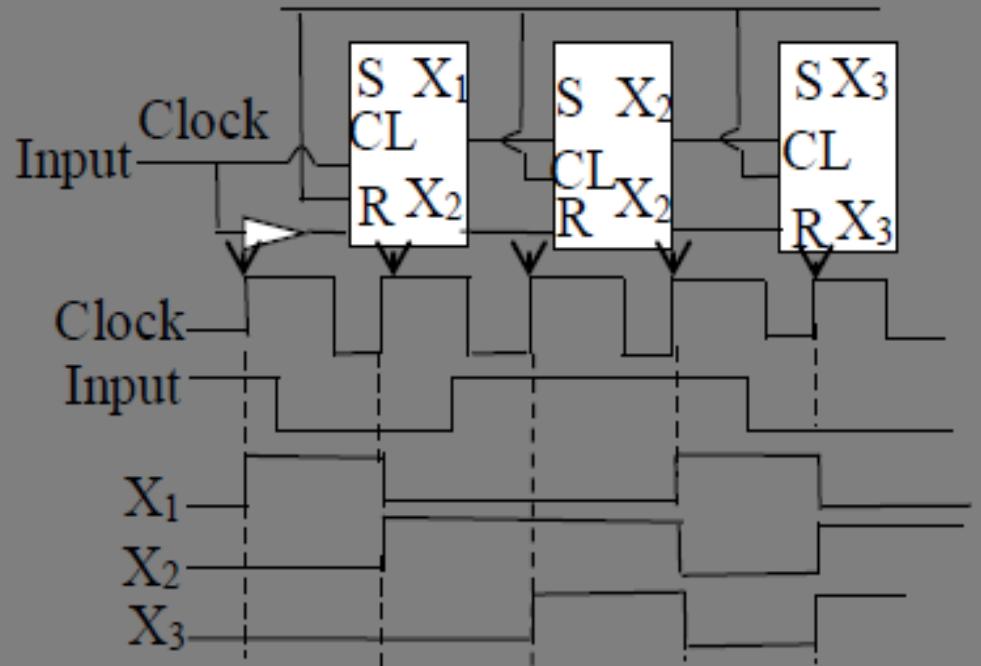
A 4 – bit binary ripple counter uses flip – flops with a propagation delay time of 25 ns each. The maximum possible time required for change of state will be

(IES-1997)

- (a) 25ns
- (b) 50 ns
- (c) 75 ns
- (d) 100ns

28 Shift register with associated waveform is shown in the following figure: Which of these is/are correct?

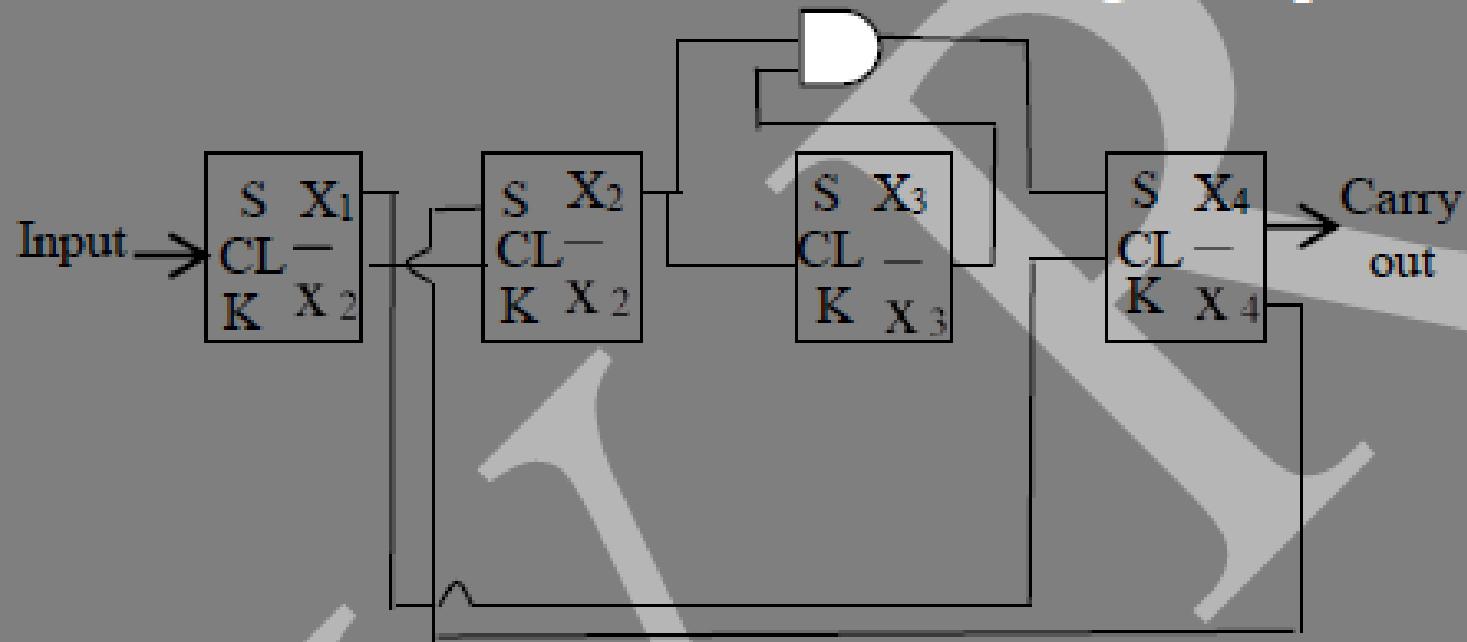
(IES-1997)



- (a)  $X_1$  alone
- (b)  $X_2$  alone
- (c)  $X_3$  alone
- (d)  $X_1$ ,  $X_2$  and  $X_3$

29. The schematic shown in the figure represents a

(IES-1997)



- (a) Divide by seven counter
- (b) Divide by five counter
- (c) Binary coded decimal counter
- (d) Divide by twelve counter

In a negative edge triggered J-K flip-flop, in order to have the output Q state 0, 0 and 1 in the next three successive clock pulses, the J-K input states required would be respectively. (IES-1999)

- (a) 00, 00 and 10
- (b) 00, 01 and 11
- (c) 00, 10 and 11
- (d) 01, 10 and 11

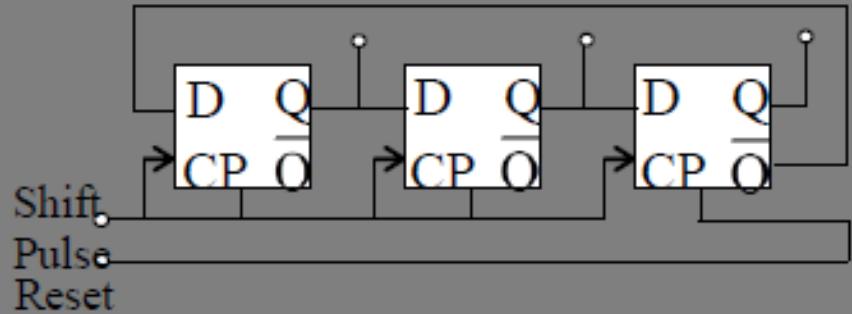
The initial state of MOD-16 down counter is  
the counter will be

- (a) 1011                   (b) 0110
- (c) 0101.                 (d) 0001.

0110. After 37 clock pulses, the state of  
**(IES-1999)**

32. A three-bit shift register is shown in the given figure.

(IES-1999)



To have the content '000' again, the number of clock pulses required would be

- (a) 3
- (b) 6
- (c) 8
- (d) 16

Symmetrical square wave of time period  $100\text{ }\mu\text{s}$  can be obtained from square wave of time period  $10\text{ }\mu\text{s}$  by using a

(IES-1999)

- (a) divide by-5 circuit
- (b) divide by-2 circuit
- (c) divide by-5 circuit followed by a divide by-2 circuit.
- (d) BCD counter.

A  $1 \mu\text{s}$  pulse can be converted into a  $1\text{ms}$  pulse by using.

(IES-1999)

- (a) a monostable multivibrator
- (b) an astable multivibrator
- (c) a bistable multivibrator.
- (d) a J-K flip-flop

**Assertion (A):** A ring counter is preferred over a binary sequential counter.

**Reason (R):** The decoding logic is simple for a ring counter. (IES-2000)

- (a) Both A and R are true and R is the correct explanation of A.
- (b) Both A and R are true but R is NOT the correct explanation of A.
- (c) A is true but R is false.
- (d) A is false but R is true.

A T-flip-flop function is obtained from a JK flip-flop. If the flip-flop belongs to a TTL family, the connection needed at the input must be

(IES-2000)

- (a)  $J = K = 1$
- (b)  $J = K = 0$ .
- (c)  $J = 1$  and  $K = 0$
- (d)  $J = 0$  and  $K = 1$ .

Consider the following statements:

1. Race around condition occurs in a JK flip- flop when both the inputs are one
2. A flip-flop is used to store one bit of information.
3. A transparent latch consists of a D-type flip- flop
4. Master-slave configuration is used in flip- flops to store two bits of information

Which of these statements are correct?

(IES-2000)

- (a) 1, 2 and 3 (b) 1, 3 and 4  
(c) 1, 2 and 4 (d) 2, 3 and 4

A ring counter consisting of five flip-flop will have

(IES-2000)

- (a) 5 states              (b) 10 states
- (c) 32 states              (d) infinite states.

.. A crystal oscillator is frequently used in digital circuits for timing purposes because of its (IES-2000)

- (a) low cost
- (b) high frequency stability
- (c) simple circuitry
- (d) ability to set the frequency at the desired value.

The 54/74164 chip is an 8-bit serial-input- parallel-output shift register. The clock is 1MHz. The time needed to shift an 8-bit binary number into the chip is

**(IES-2001)**

- (a) 1  $\mu$ s
- (b) 2  $\mu$ s
- (c) 8  $\mu$ s
- (d) 16  $\mu$ s

**Assertion (A):** A lock-ahead carry adder is a

**Reason (R):** A parallel carry adder generates  
(IES-2001)

fast adder.

sum digits directly from the input digits.

- (a) Both A and R are true and R is the correct explanation of A.
- (b) Both A and R are true but R is NOT the correct explanation of A.
- (c) A is true but R is false.
- (d) A is false but R is true.

**Assertion (A):** Master-slave JK flip-flop is free from race-around condition.

**Reason (R):** Master-slave uses two JK flip- flop. (IES-2001)

- (a) Both A and R are true and R is the correct explanation of A.
- (b) Both A and R are true but R is NOT the correct explanation of A.
- (c) A is true but R is false.
- (d) A is false but R is true.

The characteristic equation of the T-flip-flop is given by

(IES-2001)

- (a)  $Q^+ = TQ + \bar{T}\bar{Q}$
- (b)  $Q^+ = T\bar{Q} + Q\bar{T}$
- (c)  $Q^+ = T + Q$
- (d)  $Q^+ = T\bar{Q}$

Four memory chips of  $16 \times 4$  size have their address buses connected together. This system will be of size(IES-2001)

- (a)  $64 \times 4$
- (b)  $16 \times 16$
- (c)  $32 \times 8$
- (d)  $256 \times 1$

**Assertion (A):** Master-slave JK flip-flop is preferred to an edge-triggered JK flip-flop in high speed circuits.

**Reason (R):** Master-slave JK flip-flop is free from race-around problem. (IES-2002)

- (a) Both A and R are true and R is the correct explanation of A.
- (b) Both A and R are true but R is NOT the correct explanation of A.
- (c) A is true but R is false.
- (d) A is false but R is true.

A sequence detector is required to give a logical output of 1 whenever the sequence 1011 is detected in the incoming pulse stream. Minimum number of flip-flops needed to build the sequence detector is (IES-2002)

- (a) 4
- (b) 3
- (c) 2
- (d) 1

**Assertion(A):** Asynchronous sequential circuits are difficult to design.

**Reason (R):** External clock is used for synchronization of asynchronous sequential circuits.

**(IES-2003)\**

- (a) Both A and R are true and R is the correct explanation of A.
- (b) Both A and R are true but R is NOT the correct explanation of A.
- (c) A is true but R is false.
- (d) A is false but R is true.

- The output of a Moore sequential machine is a function of
- (a) All present states of the machine
  - (b) All the inputs
  - (c) A few combination of inputs and the present state
  - (d) All the combinationas of inputs and the present state

Minimum number of J-K flip-flops needed to construct a BCD counter is  
**(IES-2003)**

- (a) 2
- (b) 3
- (c) 4
- (d) 5

The characteristic equation for the next state ( $Q_{n+1}$ ) of a J-K flip-flop is  
**(IES-2003)**

- (a)  $Q_{n+1} = JQ_n + K \bar{Q}_n$
- (b)  $Q_{n+1} = \bar{J} \bar{Q}_n + \bar{K} \bar{Q}_n$
- (c)  $Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$
- (d)  $Q_{n+1} = JQ_n + K Q_n$

The number of unused states in a 4-bit Johnson counter is

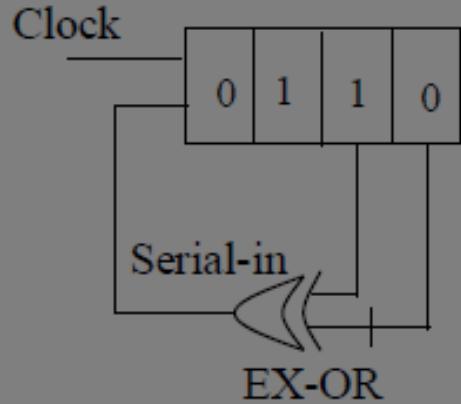
(IES-2003)

- (a) 2
- (b) 4
- (c) 8
- (d) 12

The initial contents of the 4-bit series-in-parallel-out, right shift, shift register as shown in figure below are 0110. After 3 clock pulses the contents of the shift register will be

(IES-2001)  
(IES-2003)  
(IES-2004)

- (a) 0000
- (b) 0101
- (c) 1010
- (d) 1110



Consider the following statements: For a master-slave J-K flip-flop, 1. the toggle frequency is the maximum clock frequency at which the flip-flop will toggle reliably 2. the data input must precede the clock triggering edge transition time by some minimum time 3. the data input must remain fixed or a given time after the clock triggering edge transition time for reliable operation. 4. propagation delay time is equal to the rise time and fall time of the data. Which of the statements given above are correct? (IES-2004)

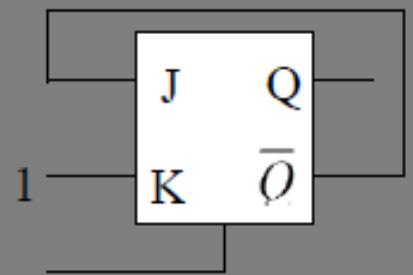
- (a) 1, 2 and 3
- (b) 1, 2 and 4
- (c) 1, 3 and 4
- (d) 2, 3 and 4

The total number of 1's in a 15-bit shift register is to be counted by clocking into a counter which is preset to 0. The counter must have which one of the following?

(IES-2004)

- (a) 4-bits
- (b) 5-bits
- (c) 16-bits
- (d) 6-bits

Consider the following J-K flip-flop.



In the above J-K flip-flop,  $J = \bar{Q}$  and  $K = 1$ . Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

(IES-2004)

- (a) 01000
- (b) 011001
- (c) 010010
- (d) 010101

Consider the following statements regarding registers and latches:

1. Registers are made of edge-triggered FFS, whereas latches are made from level-triggered FFS.
2. Registers are temporary storage devices whereas latches are not.
3. A latch employs cross-coupled feedback connections.
4. A register stores a binary word whereas a latch does not.

Which of the statements given above are correct? (IES-2004)

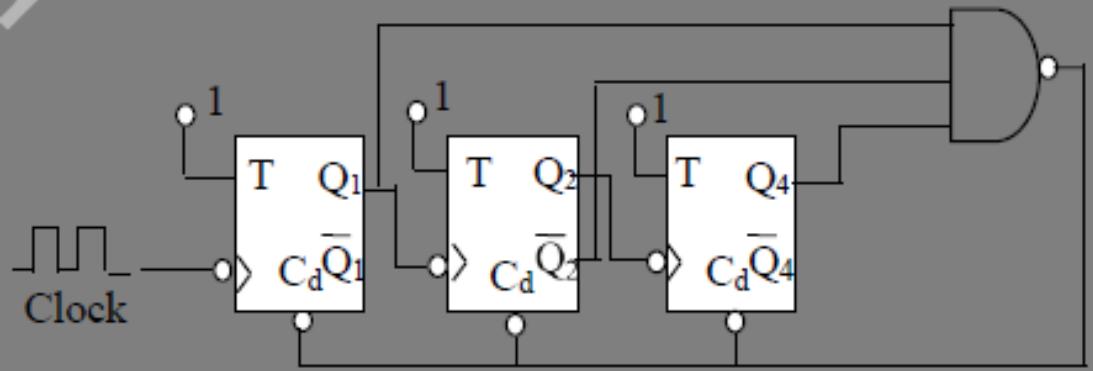
- |             |             |
|-------------|-------------|
| (a) 1 and 2 | (b) 1 and 3 |
| (c) 2 and 3 | (d) 3 and 4 |

12 MHz clock frequency is applied to a cascaded counter of modulus-3 counter, modulus-4 counter and modulus-5 counter. What are the lowest output frequency and the overall modulus, respectively?

(IES-2005)

- (a) 200kHz, 60
- (b) 1MHz, 60
- (c) 3MHz, 12
- (d) 4MHz, 12

58. The circuit given below is that of a  
(IES-2005)



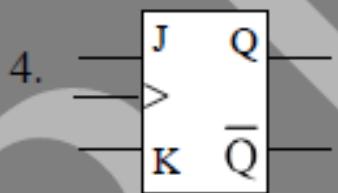
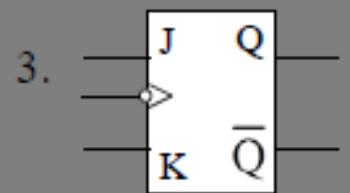
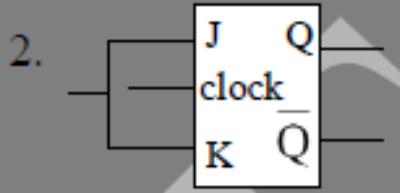
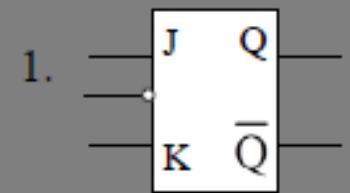
- (a) Mod-5 counter
- (b) Mod-6 counter
- (c) Mod-7 counter
- (d) Mod-8 counter

Match List-I(Type of flip-flop) with List-II (Symbol) and select the correct answer using the code given below the lists: (IES-2005)

**List-I**

- A. T flip-flop
- B. Level-triggered JK flip-flop
- C. Leading edge-triggered JK flip-flop
- D. Trailing edge-triggered JK flip-flop

**List-II**



**Codes:**

	A	B	C	D
(a)	1	2	3	4
(b)	2	1	3	4
(c)	1	2	4	3
(d)	2	1	4	3

Which one of the following equations satisfies the JK flip-flop truth table?

(IES-2006)

- (a)  $Q_{n+1} = J_n \bar{Q}_n + \bar{K}_n Q_n$
- (b)  $Q_{n+1} = \bar{J}_n \bar{Q}_n + \bar{K}_n Q_n$
- (c)  $Q_{n+1} = J_n Q_n + K_n Q_n$
- (d)  $Q_{n+1} = \bar{J}_n \bar{Q}_n + \bar{K}_n \bar{Q}_n$

A master slave configuration consists of two identical flip-flop connected in such a way that the output of the master is input to the slave. Which one of the following is correct?

(IES-2006)

- (a) Master is level triggered and slave is edge triggered.
- (b) Master is edge triggered and slave is level triggered
- (c) Master is positive edge triggered and slave is negative edge triggered.
- (d) Master is negative edge triggered and slave is positive edge triggered.

Match List-I(Circuit) with List-II(Application) and select the correct answer using the code given below the lists:  
**(IES-2006)**

**List-I**

- A. Ripple up counter
- B. Synchronous down counter
- C. Shift left register
- D. Shift right register.

**List-II**

- 1. Division
- 2. Multiplication
- 3. To create delay
- 4. Transient states.

**Codes:**

	A	B	C	D
(a)	2	3	4	1
(b)	4	1	2	3
(c)	2	1	4	3
(d)	4	3	2	1

The characteristic equation of a flip-flop gives the next state  $Q_{N+1}$  in terms of the present state  $Q_N$  and the inputs. Which one of the following is the characteristic equation of J-K flip flop? (IES-2007)

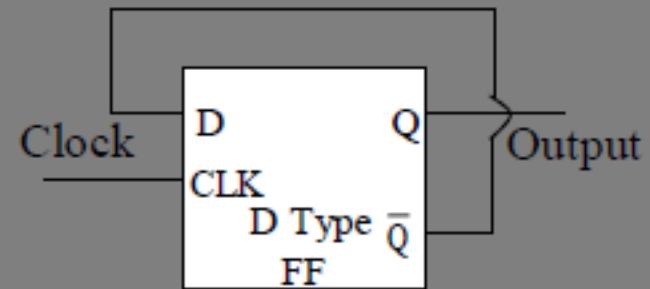
- (a)  $Q_{N+1}=J\bar{Q}_N + \bar{K}Q_N$
- (b)  $Q_{N+1}=J+ \bar{K}Q_N$
- (c)  $Q_{N+1}=K\bar{Q}_N + \bar{J}Q_N$
- (d)  $Q_{N+1}=K+ \bar{J}Q_N$

A 1ms pulse can be converted into a 10ms pulse by using which one of the following?

(IES-2007)

- (a) An astable multivibrator
- (b) A monostable multivibrator
- (c) A bistable multivibrator
- (d) A J-K flip-flop

For the circuit shown in the below figure, what is Pthe frequency of the output Q? (IES-2007)



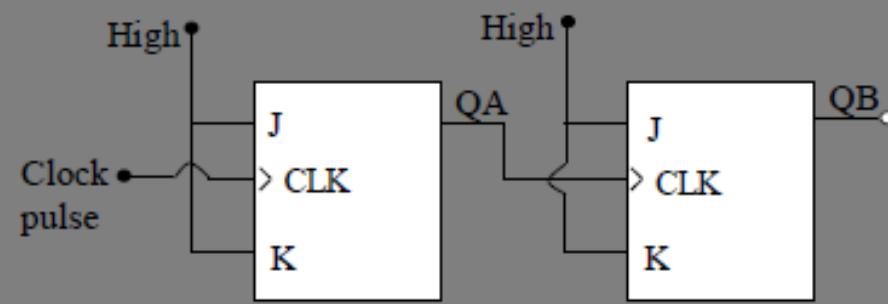
- (a) Twice the input clock frequency
- (b) Half the input clock frequency
- (c) Same as the input clock frequency
- (d) Inverse of the propagation delay of the FF.

**Assertion (A):** D-flip-flops are used as buffer register.

**Reason (R):** D-flip-flops are free from “race-around” condition.

- (a) Both A and R are true and R is the correct explanation of A.
- (b) Both A and R are true but R is NOT the correct explanation of A.
- (c) A is true but R is false.
- (d) A is false but R is true.

68. The below circuit illustrates a typical application of the JK flip-flops. What does this represent? (IES-2008)



- (a) A shift register
- (b) A data storage device.
- (c) A frequency divider circuit
- (d) A decoder circuit

69. Match List I with List II and select the correct answer using the code given below the Lists: (IES-2009)

**List I**

(Application of circuit)

- A. Divider
- B. Clips input voltage at Two predetermined levels
- C. Square wave generator
- D. Narrow current pulse generator

**List II**

(Circuit Name)

- 1. Astable multivibrator
- 2. Schmitt trigger
- 3. Bistable multivibrator
- 4. Blocking oscillator

**Codes:**

	A	B	C	D
(a)	4	2	1	3
(b)	3	2	1	4
(c)	4	1	2	3
(d)	3	1	2	4

Consider the following statements: For a master-slave J-K flip-flop,

1. the toggle frequency is the maximum clock frequency at which the flip-flop will toggle reliably.
2. the data input must precede the clock triggering edge transition time by some minimum time.
3. the data input must remain fixed for a given time after, the clock triggering edge transition time for reliable operation.
4. propagation delay time is equal to the rise time and fall time of the data.

Which of the above statements is/are correct? (IES-2009)

- (a) 1, 2 and 3
- (b) 1 and 2 only
- (c) 2 and 3 only
- (d) 3 and 4 only

Consider the following statements:

1. A flip-flop is used to store 1-bit of information
2. Race-around condition occurs in a J-K flip-flop when both the inputs are 1.
3. Master-slave configuration is used in flip-flops to store 2-bits of information
4. A transparent latch consists of a D-type flip-flop.

Which of the above statements is/are correct?

- (a) 1 only    (b) 1, 3 and 4  
(c) 1, 2 and 4    (d) 2 and 3 only

(IES-2009)

Which of the following flip-flop is used as a latch? (IES-2009)

- (a) J K flip-flop
- (b) R S flip-flop
- (c) T flip-flop
- (d) D flip-flop

Which of the following conditions should be satisfied to call an astable multivibrator circuit using discrete components as a digital circuit? (IES-2009)

1. A flip-flop is always a digital circuit.
2. Only when we assign 1 and 0 to the high and low levels of the output, a flip-flop is called a digital circuit
3. Only if the power supply voltage is maintained at +5 V or -5 V, it is called a digital circuit.
4. Only if it is in IC form, following the technology of IC manufacture, it is called a digital circuit.

Select the correct answer from the codes given below:

- (a) 1 only      (b) 2 and 3 only  
(c) 2 only      (d) 3 and 4

Which of the following circuits come under the class of sequential logic circuits?  
**(IES-2009)**

1. Full adder
2. Full subtractor
3. Half adder
4. J-K flip-flop
5. Counter

Select the correct answer from the codes given below:

- (a) 1 and 2      (b) 2 and 3  
(c) 3 and 4      (d) 4 and 5

Consider the following statements regarding registers and latches:  
**(IES-2009)**

1. Registers are made of edge-triggered FFs, whereas latches are made from level-triggered FFs.
2. Registers are temporary storage devices whereas latches are not.
3. A latch employs cross-coupled feedback connections.
4. A register stores a binary word whereas a latch does not.

Which of the above statements is/are correct?

- (a) 1 only      (b) 1 and 3  
(c) 2 and 3      (d) 3 and 4

Which of the following capabilities are available in a Universal Shift register?  
**(IES-2009)**

- 1. Shift left
- 2. Shift right
- 3. Parallel load
- 4. Serial add

Select the correct answer from the codes given below:

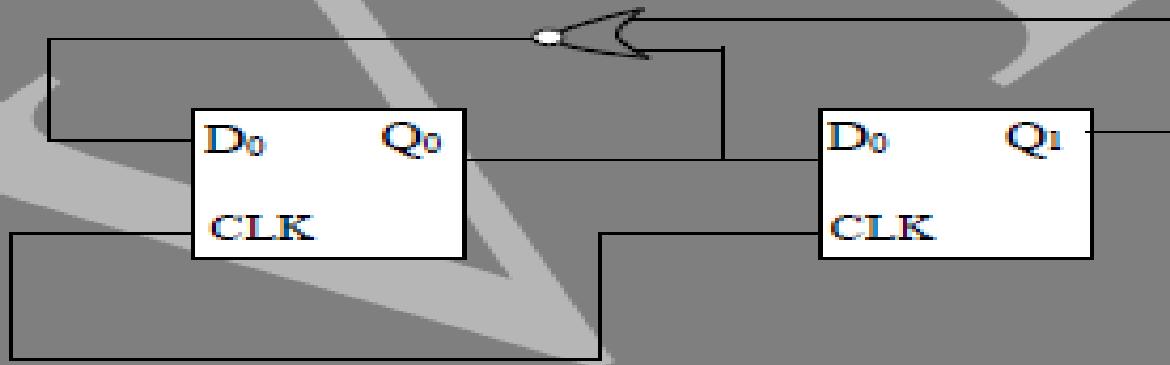
- (a) 2 and 4 only
- (b) 1, 2 and 3
- (c) 1, 2 and 4
- (d) 1, 3 and 4

Which of the following measurements can be done using a counter?  
**(IES-2009)**

1. Pulse duration
2. Interval between two pulses
3. Amplitude of the pulse
4. Rise time of a pulse

Select the correct answer from the codes given below:

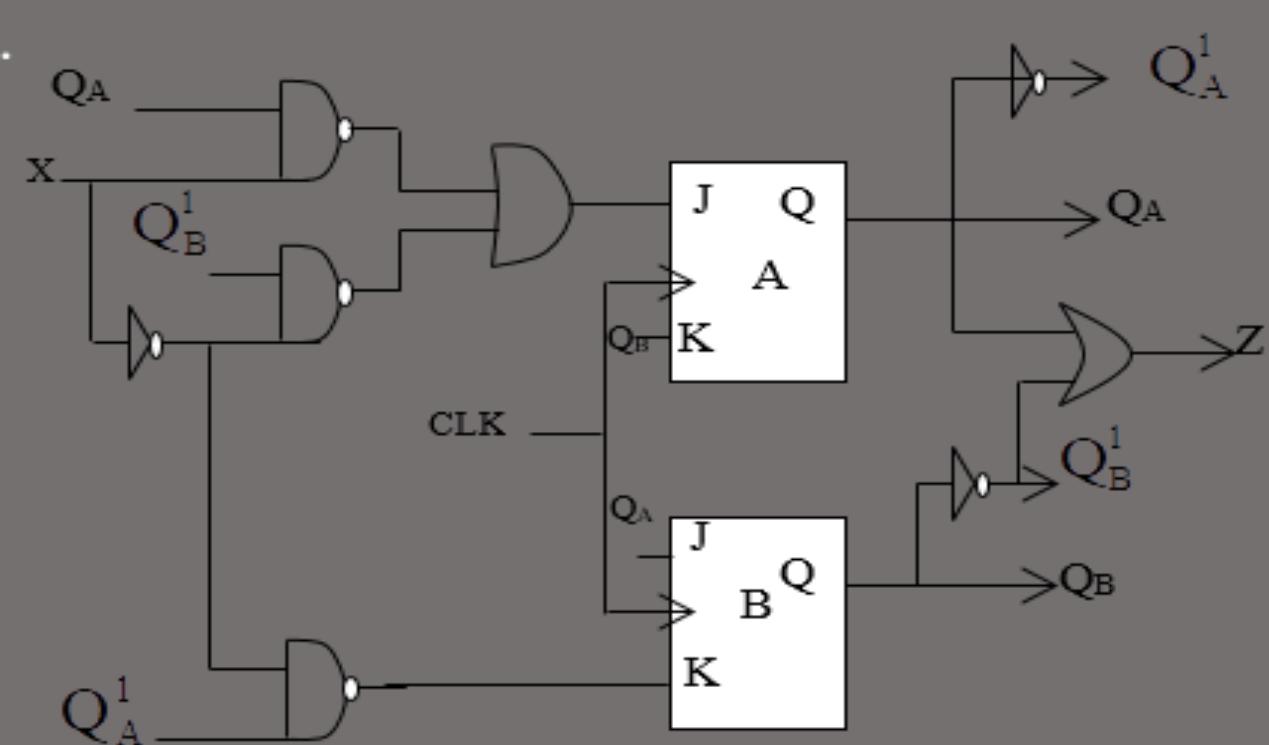
- (a) 1 and 2      (b) 2 and 3  
(c) 1 and 4      (d) 2 and 4



For the circuit shown, the counter state ( $Q_1Q_0$ )  
**(IES-2009)**

- (a) 00, 01, 10, 11, 00 -----
- (b) 00, 01, 10, 00, 01 -----
- (c) 00, 01, 11, 00, 01 -----
- (d) 00, 10, 11, 00, 10 -----

follows the sequence.

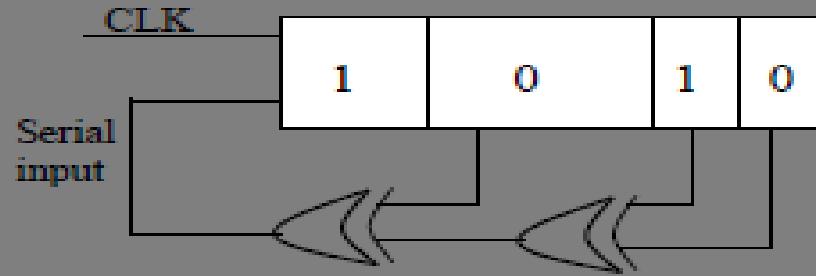


Analyze the sequential circuit shown above in figure. Assuming that initial sequence would lead to state 11?

(IES-2010)

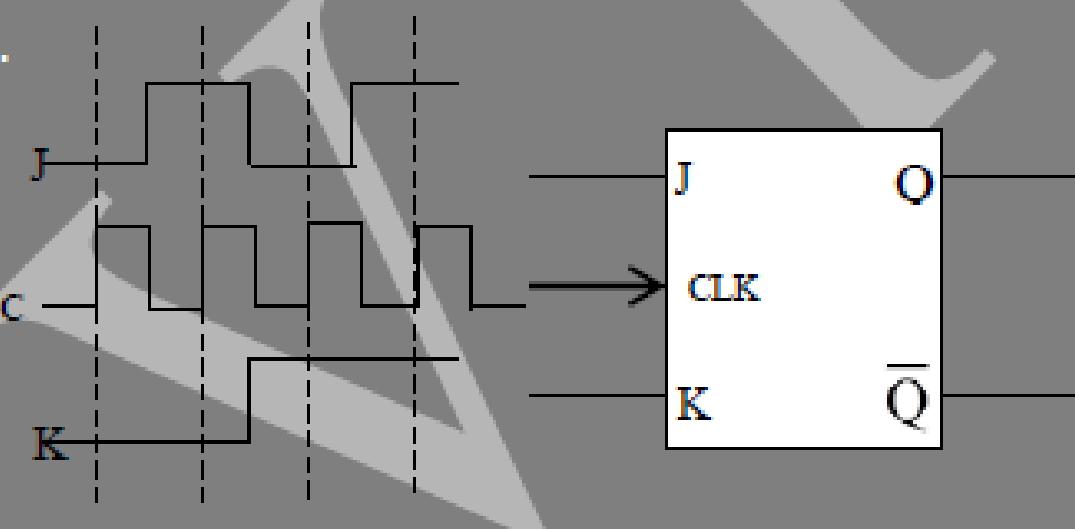
- (a) 1 – 1
- (b) 1 – 0
- (c) 0 – 0
- (d) state 11 is

unreachable.



The shift register shown in the given figure is initially loaded with the bit pattern 1010 subsequently the shift register is clocked, and with each pulse the pattern gets shifted by one bit position to the right with each shift, the bit at the serial input is pushed to the msb position. After how many clock pulse will content of the shift register become 1010 again?

- (IES-2010 & 2011)
- (a) 3
  - (b) 7
  - (c) 11
  - (d) 15



The J\_K flipflop shown above is initially reset so that  $Q = 0$ . If a sequence of four clock pulses is then applied, with the J and K inputs as given in the figure, the resulting sequence of values that appear at the output Q starting with its initial state, is given by:

(IES-2010)

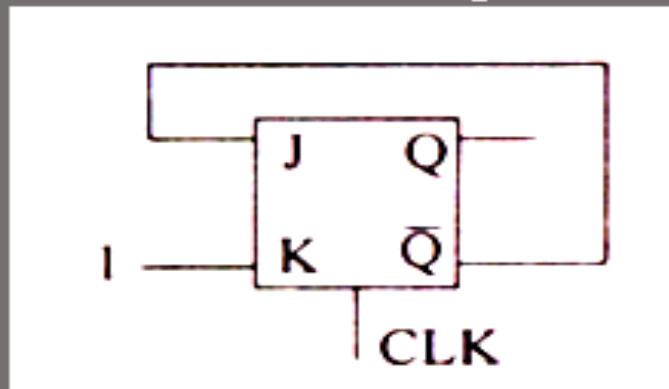
- (a) 01011
- (b) 01010
- (c) 00110
- (d) 00101

X	Y	$Q_{n+1}$
0	0	1
0	1	<u><math>Q_n</math></u>
1	0	$\overline{Q_n}$
1	1	0

An X-Y flip flop, whose characteristic table is given above is to be implemented using JK flip flop. This can be done by making:-

- (a)  $J = X, K = \overline{Y}$
- (b)  $J = \overline{X}, K = Y$
- (c)  $J = Y, K = \overline{X}$
- (d)  $J = \overline{Y}, K = X$

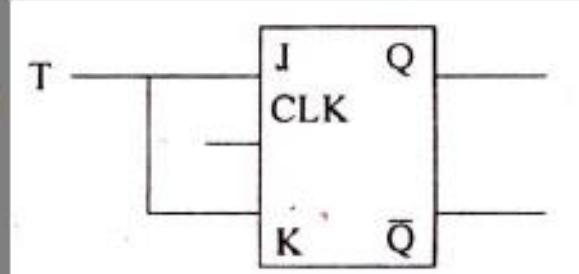
In a JK flip-flop we have  $J = \bar{Q}$  and  $K = 1$ . Assuming the flip-flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be: (IES-2011)



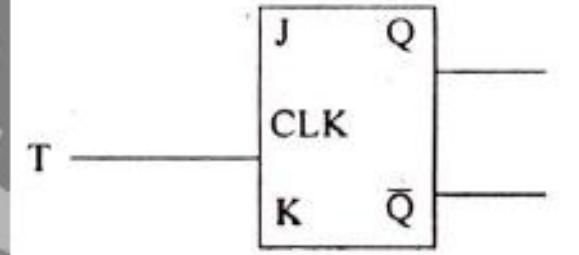
- (a) 010000
- (b) 011001
- (c) 010010
- (d) 010101

Which one of the following circuits converts a JK F/F to a T F/F?  
(IES-2011)

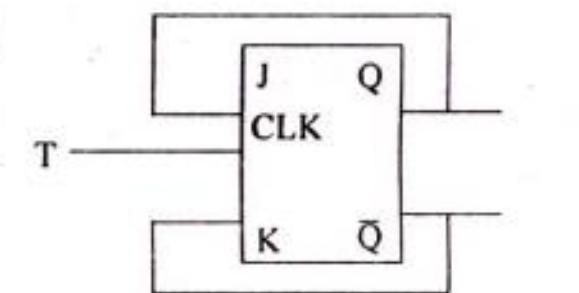
(a)



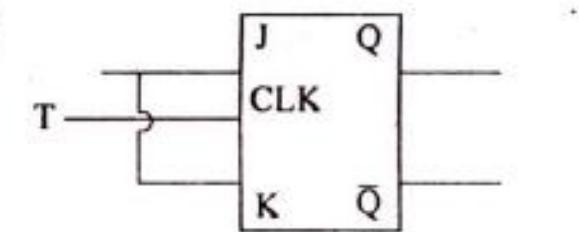
(b)



(c)



(d)



A 4-bit ripple counter consisting of flip-flops that each have a propagation delay of 12ns from clock to Q output. For the counter to recycle from 1111 to 0000, it takes a total of :

(IES-2011)

- (a) 12ns
- (b) 24ns
- (c) 48ns
- (d) 26ns

An eight-bit binary ripple UP counter with a modulus of 256 is holding the count 01111111. What will be the count after 135 clock pulses?

(IES-2011)

- (a) 0000 0101
- (b) 1111 1001
- (c) 0000 0110
- (d) 0000 0111

By placing an inverter between both input of an S – R flip-flop, the resulting flip-flop becomes

- (a) J-K flip-flop
- (b) D-flip-flop
- (c) T-flip-flop
- (d) Master slave JK flip-flop

(IES-EE - 92)

A synchronous sequential circuit is to be designed which will produce an output '1' when previous two and present input represent an even number, with present input being least significant bit. The minimum number of states of the machine will be?

(a) 2

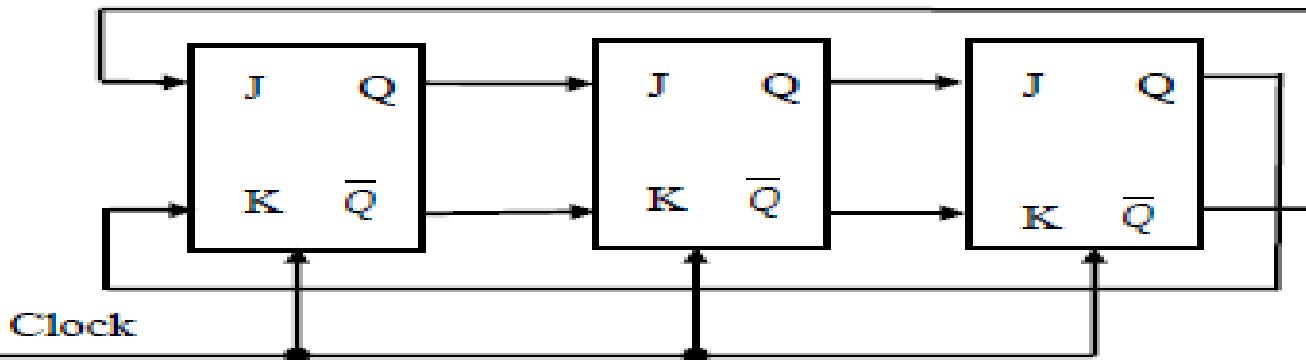
(b) 3

(c) 4

(d) 5

(IES—EE – 94)

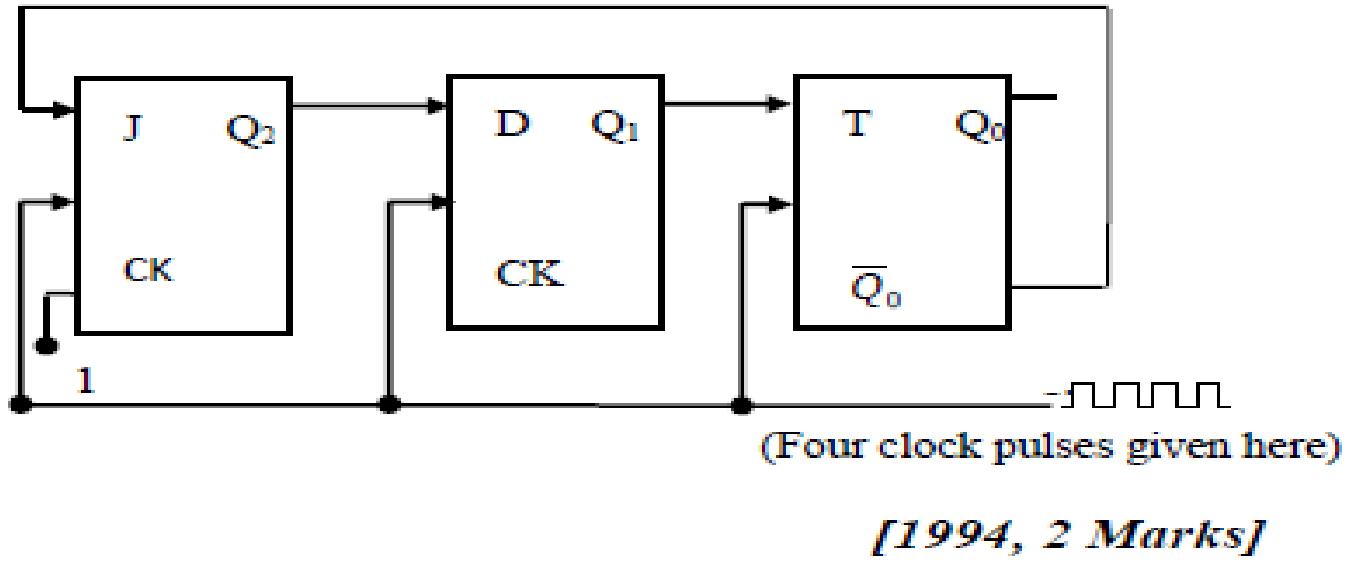
For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in figure is:



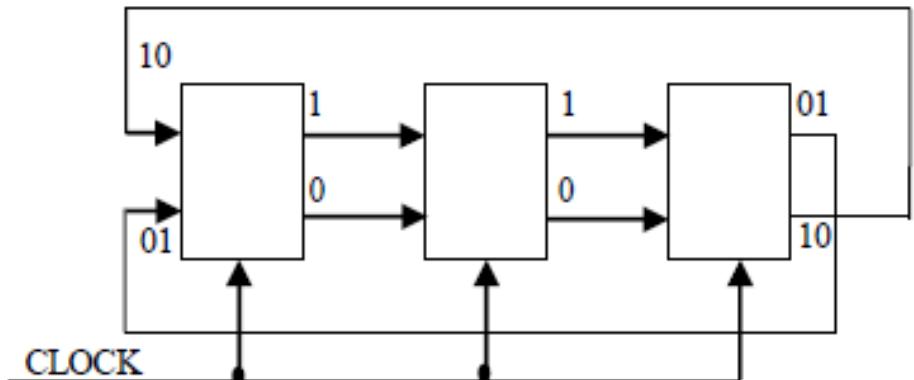
- (A) Shift Register
- (B) Mod-3 Counter
- (C) Mod-6 Counter
- (D) Mod-2 Counter
- (E) None of the above

[1993, 2 Marks]

Find the contents of the flip-flop  $Q_2$ ,  $Q_1$  and  $Q_0$  in the circuit of figure, after giving four clock pulses to the clock terminal. Assume  $Q_2Q_1Q_0 = 000$  initially.



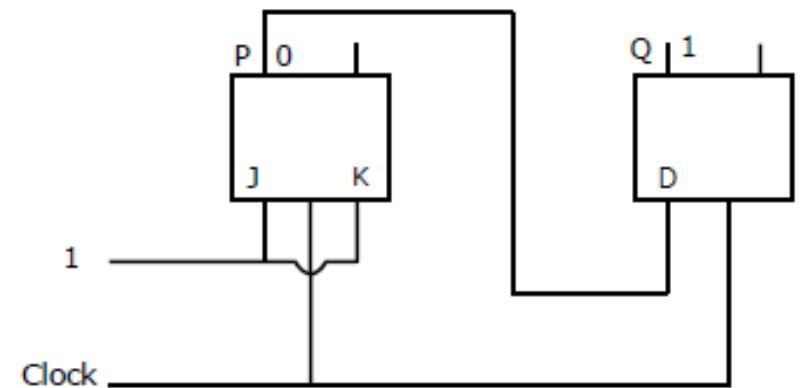
For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in the figure.



- (A) Shift Register
- (B) Mod-3 Counter
- (C) Mod-6 Counter
- (D) Mod-2 Counter
- (E) None of the above

[1993, 2 Marks]

The following arrangement of master-slave flip flops has the initial state of P, Q as 0, 1 (respectively).



After the clock cycles the output state P, Q is (respectively),

- (A) 1, 0
- (B) 1, 1
- (C) 0, 0
- (D) 0, 1

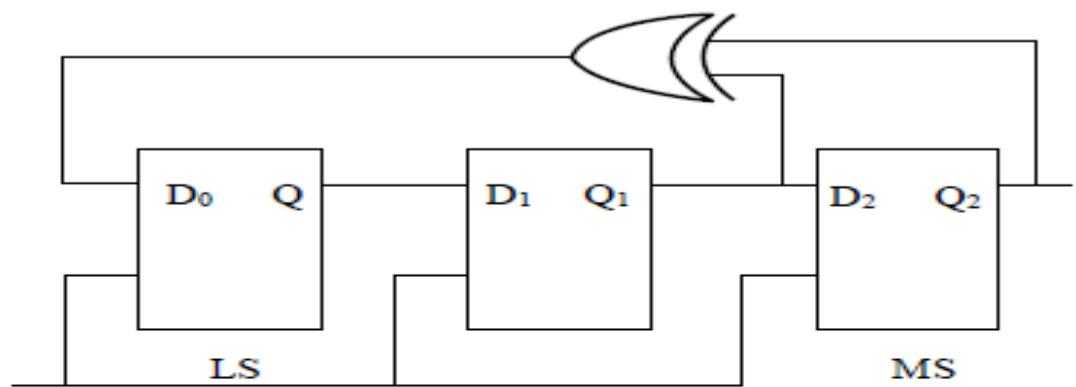
*[2000, 2 Marks]*

The number of flip-flops required to construct a  
binary modulo N counter is \_\_\_\_\_

*[1994, 2 Marks]*

Consider the circuit given above with initial state  $Q_0 = 1$ ,  $Q_1 = Q_2 = 0$ . The state of the circuit is given by the value  $4Q_2 + 2Q_1 + Q_0$ .

Which one of the following is the correct state sequence of the circuit?

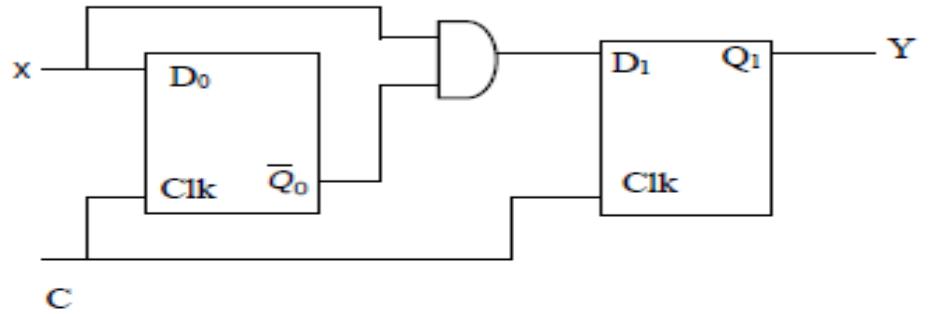


Clock

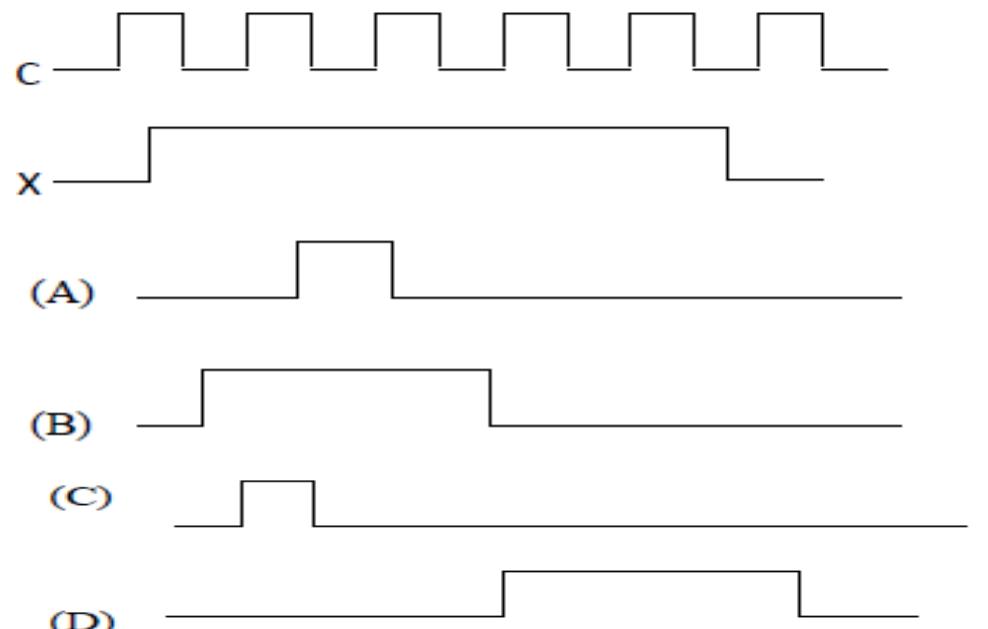
- (A) 1,3,4,6,7,5,2
- (B) 1,2,5,3,7,6,4
- (C) 1,2,7,3,5,6,4
- (D) 1,6,5,7,2,3,4

[2001, 2 Marks]

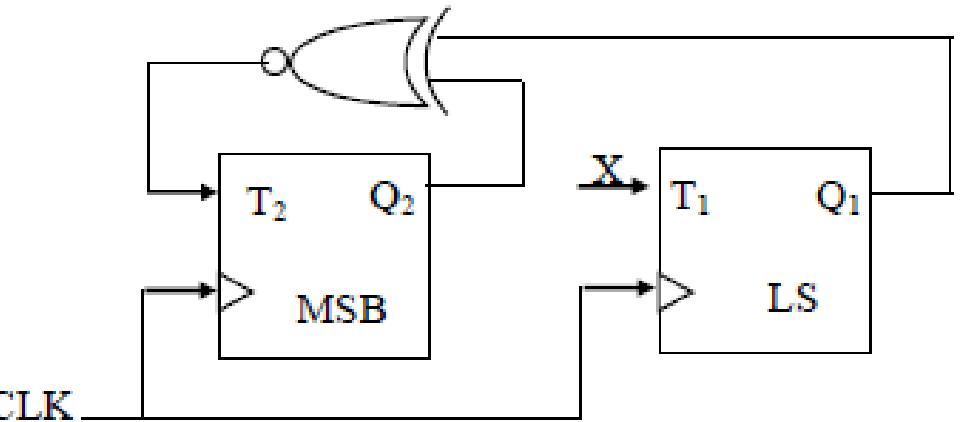
Consider the following circuit with initial state  $Q_0 = Q_1 = 0$ . The D Flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



Consider the following timing diagrams of X and C; the clock period of  $C \geq 40$  nanosecond. Which one is the correct plot of Y?



Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0, as shown below.



To complete the circuit, the input X should be

- (A)  $Q_2'$
- (B)  $Q_2 + Q_1$
- (C)  $(Q_1 \oplus Q_2)'$
- (D)  $Q_1 \oplus Q_2$

[2004, 2 Marks]

In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

- (A)  $Q = 0, Q' = 1$
- (B)  $Q = 1, Q' = 0$
- (C)  $Q = 1, Q' = 1$
- (D) Indeterminate states

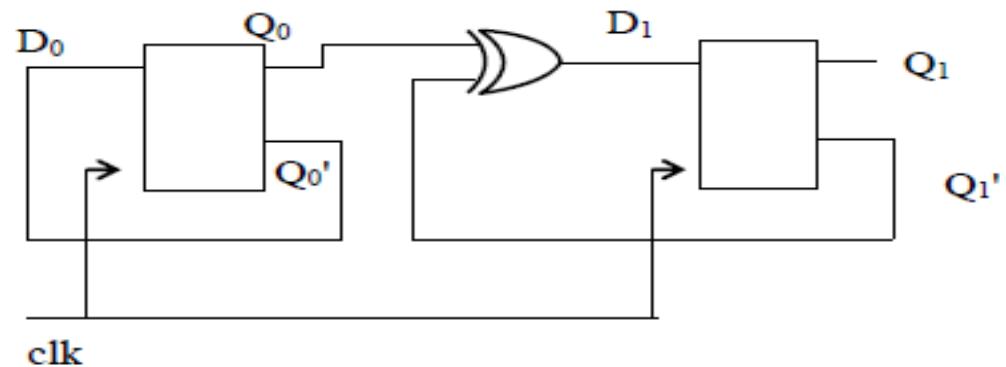
*[2004, 1 Mark]*

Consider the following circuit.

The flip-flops are positive edge triggered D FFs.

Each state is designated as a two-bit string

$Q_0Q_1$ . Let the initial state be 00. The state transition sequence is



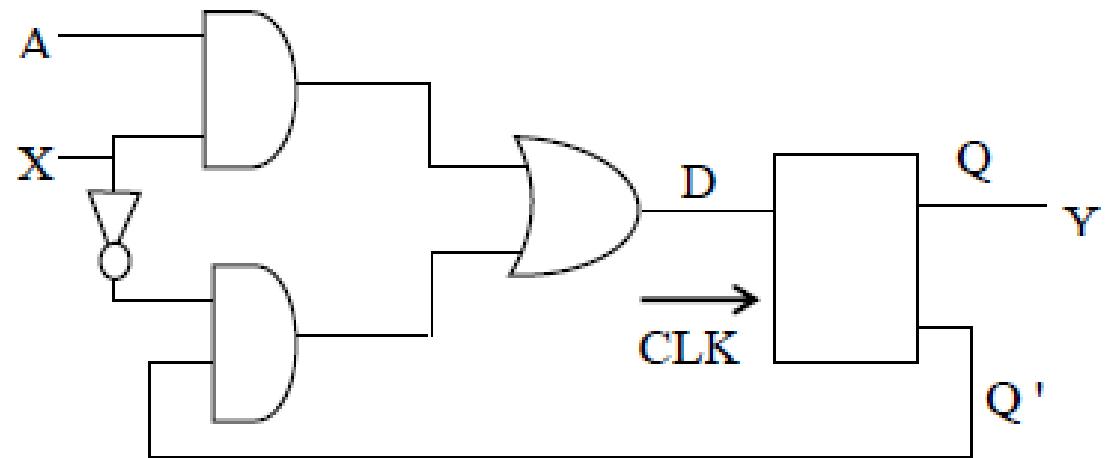
(A)  $00 \rightarrow 11 \rightarrow 01$

(B)  $00 \rightarrow 11$

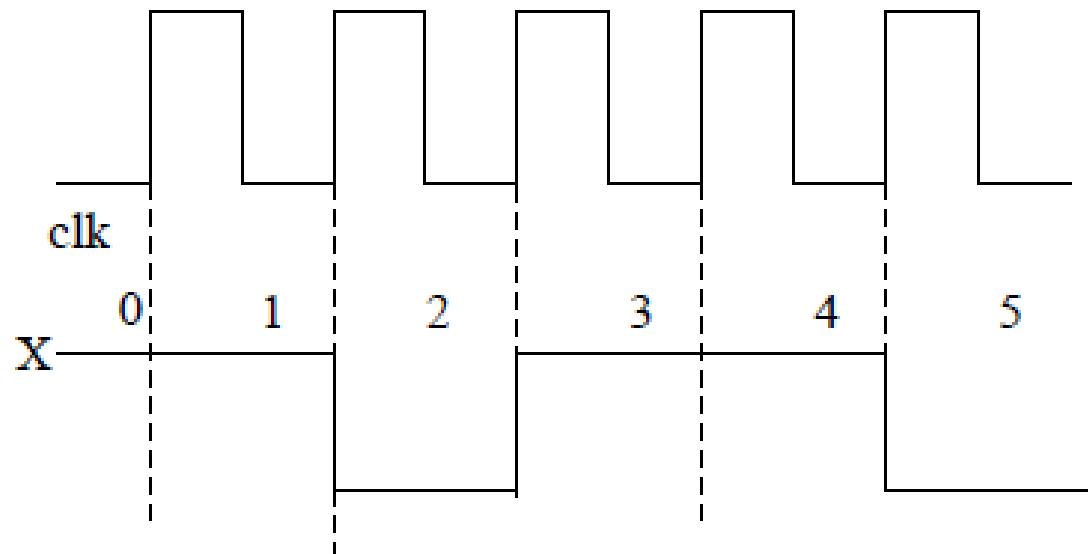
(C)  $00 \rightarrow 10 \rightarrow 01 \rightarrow 11$

(D)  $00 \rightarrow 11 \rightarrow 01 \rightarrow 10$

Consider the following circuit involving a positive edge triggered D FF.



Consider the following timing diagram.



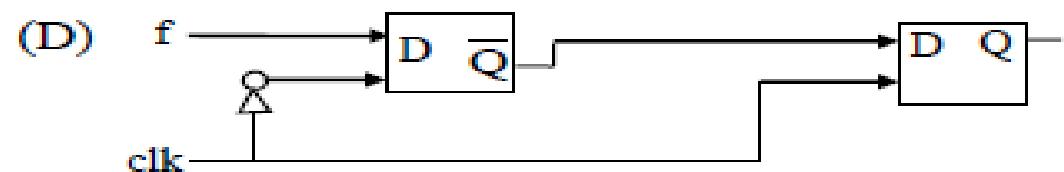
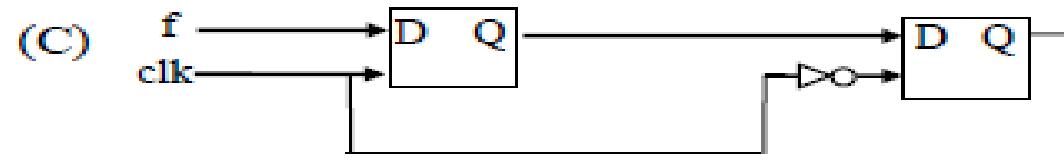
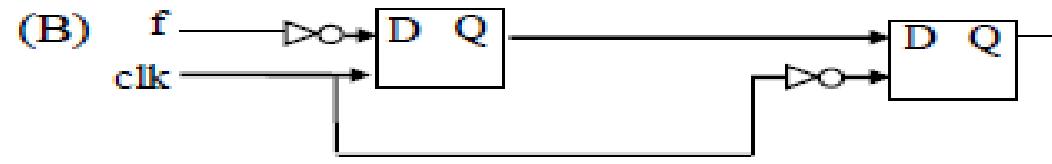
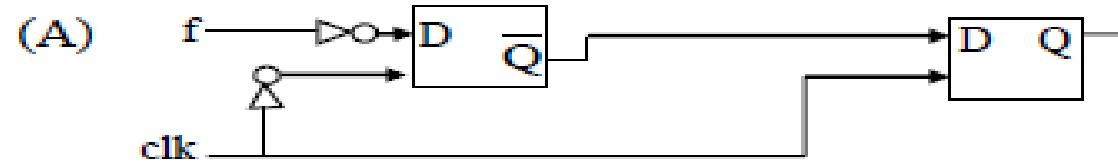
Let  $A_i$  represent the logic level on the line A in the  $i$ -th clock period.

Let  $A'$  represent the complement of A. The correct output sequence on Y over the clock periods 1 through 5 is:

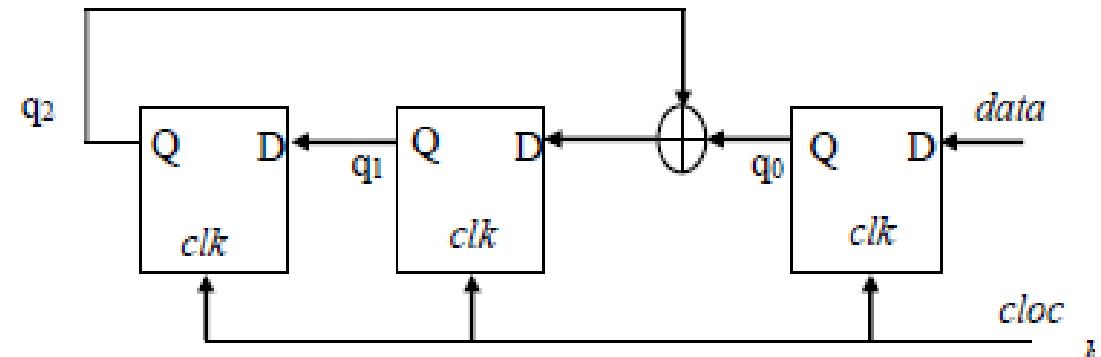
- (A)  $A_0 \ A_1 \ A_1' \ A_3 \ A_4$
- (B)  $A_0 \ A_1 \ A_2' \ A_3 \ A_4$
- (C)  $A_1 \ A_2 \ A_2' \ A_3 \ A_4$
- (D)  $A_1 \ A_2' \ A_3 \ A_4 \ A_5'$

[2005, 2 Marks]

You are given a free running clock with a duty cycle of 50% and a digital waveform  $f$  which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of  $f$  by  $180^\circ$ ?



13. Consider the circuit in the diagram. The  $\oplus$  operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).



The following data: 100110000 is supplied to the 'data' terminal in nine clock cycles. After that the values of  $q_2q_1q_0$  are:

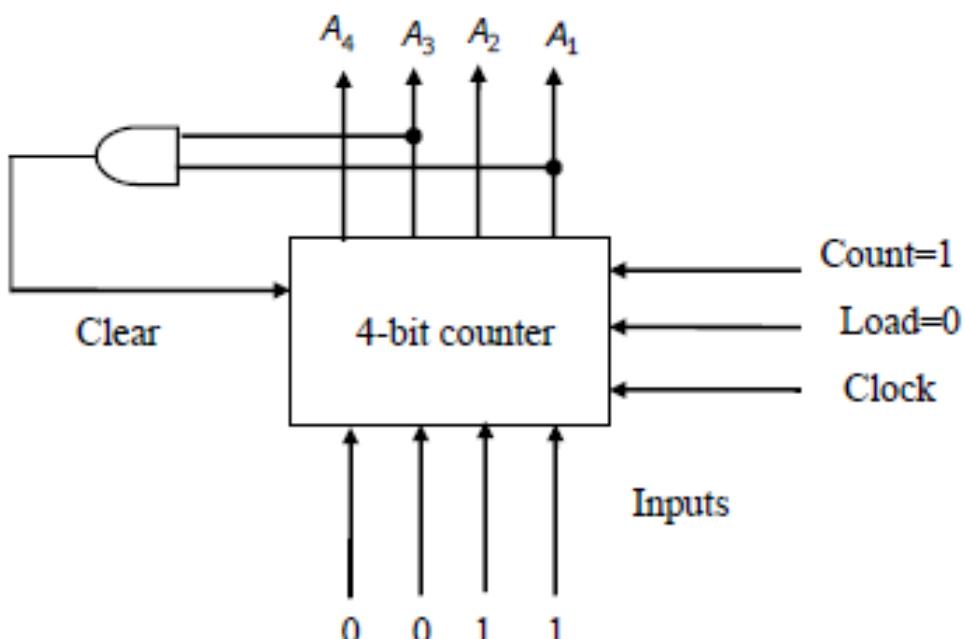
- (A) 000    (B) 001    (C) 010    (D) 101

[2006, 2 Marks]

The control signal functions of a 4-bit binary counter are given below (where X is “don’t care”):

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No change
0	↑	1	X	Load input
0	↑	0	1	Count next

The counter is connected as follows:

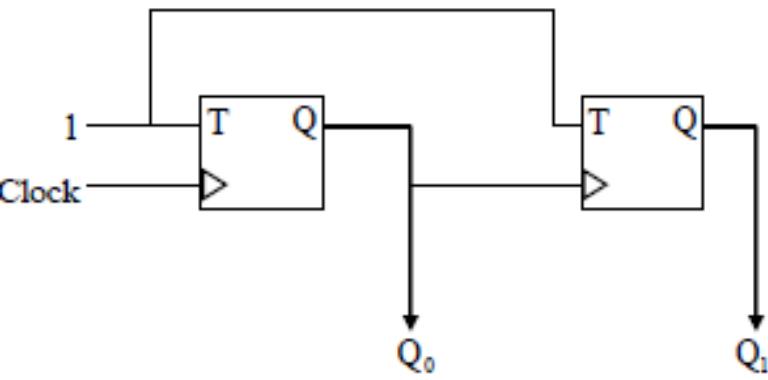


Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence:

- (A) 0, 3, 4                          (B) 0, 3, 4, 5  
(C) 0, 1, 2, 3, 4                    (D) 0, 1, 2, 3, 4, 5

[2007, 2 Marks]

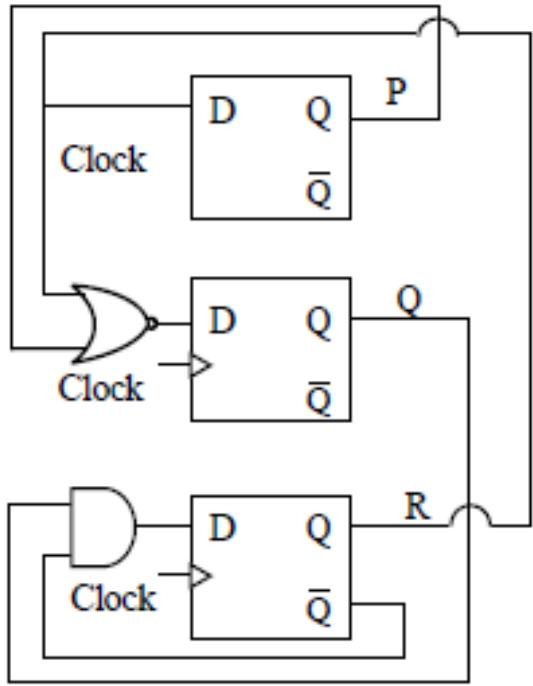
In the sequential circuit shown below, if the initial value of the output  $Q_1Q_0$  is 00, what are the next four values of  $Q_1Q_0$ ?



- (A) 11,10,01,00
- (B) 10,11,01,00
- (C) 10,00,01,11
- (D) 11,10,00,01

[2010, 2 Marks]

Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

- (A) 000    (B) 001    (C) 010    (D) 011

[2011, 2 Marks]

If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?

- (A) 3    (B) 4    (C) 5    (D) 6

[2011, 2 Marks]

The minimum number of D flip-flops needed to design a mod-258 counter is

- (A) 9      (B) 8      (C) 512      (D) 258

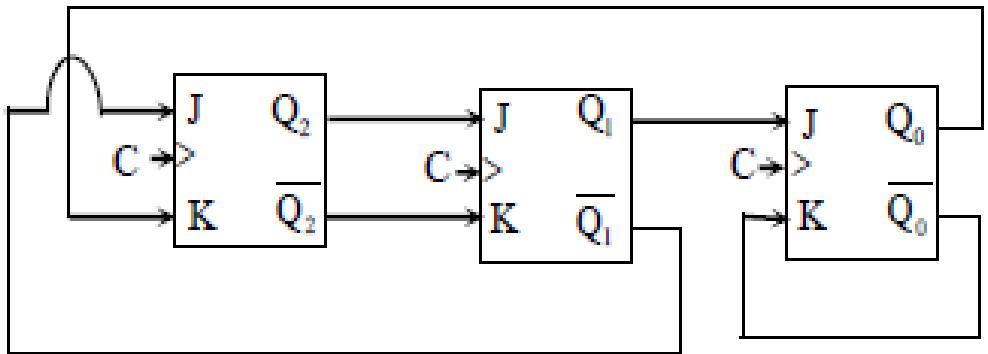
*[2011, 2 Marks]*

We want to design a synchronous counter that counts the sequence 0-1-0-2-0-3 and then repeats. The minimum number of J-K flip-flops required to implement thi

**2016-Set-I, 1M**

*[2014, 2 Marks]*

The above synchronous sequential circuit built using JK flip-flops is initialized with  $Q_2Q_1Q_0 = 000$ . The state sequence for this circuit for the next 3 clock cycles is



- (A) 001, 010, 011      (B) 111, 110, 101  
(C) 100, 110, 111      (D) 100, 011, 001

[2014, 2 Marks]

Let  $k = 2^n$ . A circuit is built by giving the output of an  $n$ -bit binary counter as input to an  $n$ -to- $2^n$  bit decoder. This circuit is equivalent to a

- (A)  $k$ -bit binary up counter
- (B)  $k$ -bit binary down counter
- (C)  $k$ -bit ring counter
- (D)  $k$ -bit Johnson counter

*[2014, 1 Mark]*