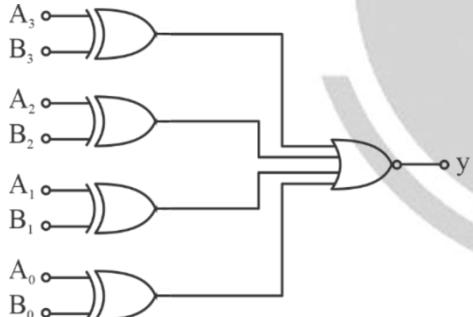
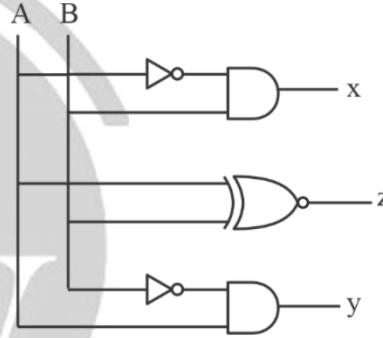


Subject : Digital Logic Combinational Circuit

DPP - 1

1. Let $x = x_1x_0$ and $y = y_1y_0$ be unsigned 2-bit numbers. The function $F = 1$ if $x > y$ and $F = 0$ otherwise. The minimal sum of product expression for F , is
- $y_1y_0 + x_0y_0 + \overline{x_1}x_0\overline{y_1}$
 - $x_0\overline{y_1} + y_1\overline{y_0} + x_1\overline{x_0}$
 - $y_1\overline{x_1} + y_0\overline{x_1}\overline{x_0} + y_1y_0\overline{x_0}$
 - $x_1\overline{y_1} + x_0\overline{y_0}\overline{y_1} + x_0x_1\overline{y_0}$
2. The two 4 - bit numbers $A_3 A_2 A_1 A_0$ and $B_3 B_2 B_1 B_0$ are applied to a comparator circuit shown below. A pair of correct input numbers forcing the output $y = 0$, will be
- 
- (a) 1100, 1100
(b) 0111, 0111
(c) 1011, 1011
(d) 1100, 1101
3. The output y of a 2-bit comparator is logic-1 whenever the 2-bit A is greater than 2-bit B the number of combination for which the output is logic - 1 is ____?
- 6
 - 2
 - 1
 - 7
- Common Statement for Question 4 and 5**
- A logic Circuit is given,
- 
4. A pair of correct input number (AB) forcing the output $x = 1$, will be
- 10
 - 01
 - 11
 - 00
5. A pair of correct input number (AB) forcing the output $y_2 = 1$, will be
- 00,11
 - 01,10
 - 00,10
 - 11,01

Answer Key

- 1. (d)
- 2. (d)
- 3. (a)

- 4. (b)
- 5. (a)



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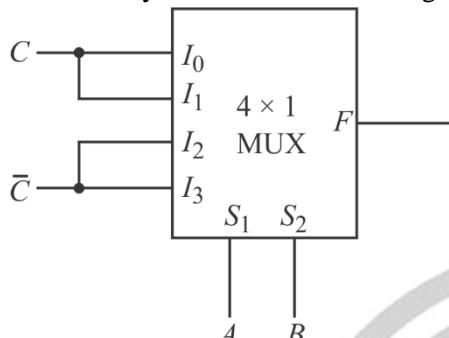
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Digital Logic

DPP - 02

COMBINATIONAL CIRCUIT

1. The logic realized by the circuit shown in figure is

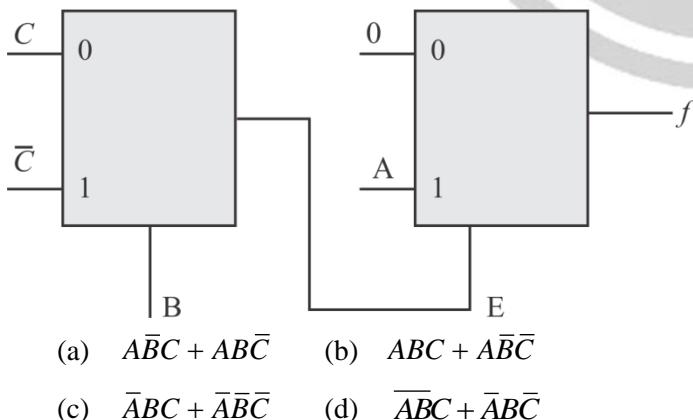


- (a) $F = A \odot C$ (b) $F = A \oplus C$
 (c) $F = B \odot C$ (d) $F = B \oplus C$

2. The minimum number of 2-to-1 multiplexers required to realize a 4-to-1 multiplexer is

- (a) 1 (b) 2
 (c) 3 (d) 4

3. The Boolean function f implemented in the figure using two input multiplexers is

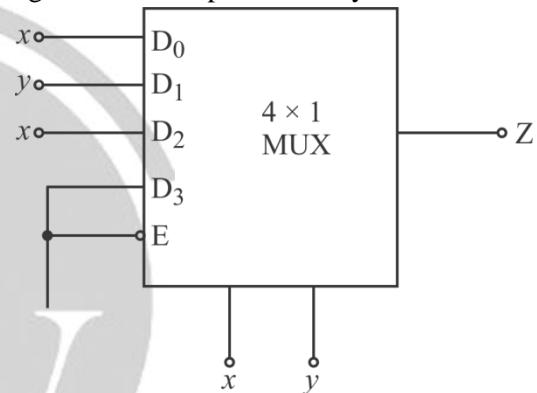


- (a) $A\bar{B}C + AB\bar{C}$ (b) $ABC + A\bar{B}\bar{C}$
 (c) $\bar{A}BC + \bar{A}\bar{B}\bar{C}$ (d) $\overline{ABC} + \bar{A}\bar{B}\bar{C}$

4. A designer has multiplexer units of size 2×1 and multiplexer of size 16×1 is to be realized. The number of units of 2×1 MUXs required, will be

- (a) 30 (b) 7
 (c) 15 (d) 11

5. The logic function implemented by 4×1 MUX, is



- (a) $Z = xy$ (b) $Z = x + y$
 (c) $Z = \overline{x + y}$ (d) $x \oplus y$

6. The minimum number of multiplexers of size 2×1 required to implement a 2-input XNOR gate and 2-input AND gate, are

- (a) 1 and 1 (b) 2 and 1
 (c) 2 and 2 (d) 3 and 1

Answer Key

- 1. (b)
- 2. (c)
- 3. (a)

- 4. (c)
- 5. (d)
- 6. (b)



Hints and solutions

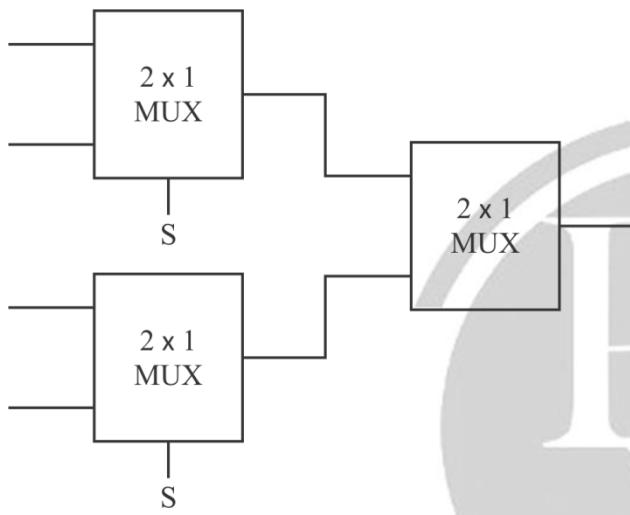
1. $F = \bar{A}\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$

$$F = \bar{A}C(B + \bar{B}) + A\bar{C}(B + \bar{B})$$

$$F = \bar{A}C + A\bar{C}$$

$$F = A \oplus C$$

2.



3. $E = \bar{B}C + B\bar{C}$

$$f = AE$$

$$f = A(\bar{B}C + B\bar{C})$$

$$f = A\bar{B}C + AB\bar{C}$$

4. $\frac{16}{2} = 8$

$$\frac{8}{2} = 4$$

$$\frac{4}{2} = 2$$

$$\frac{2}{2} = 1$$

15

Total 15 2×1 MUX required to implemented 16×1 MUX.

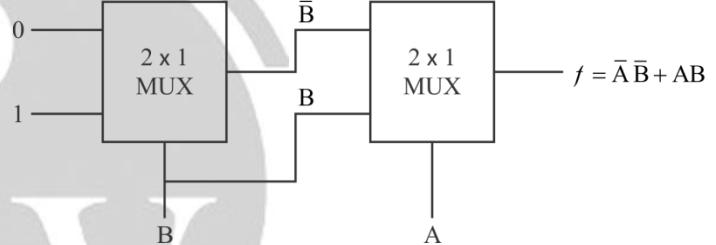
5. $z = \bar{x}y x + \bar{x}y y + x\bar{y}x + xy \cdot 0$

$$z = \bar{x}y + x\bar{y}x$$

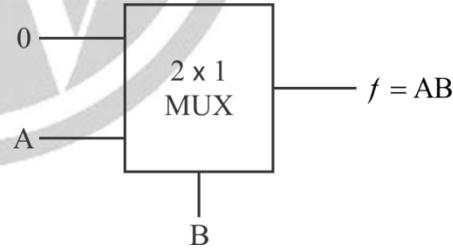
$$z = \bar{x}y + x\bar{y}$$

$$z = x \oplus y$$

6. X-NOR gate implementation



Two 2×1 MUX required to implementation X-NOR gate.



One 2×1 MUX required to implementation AND gate.



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Digital Logic

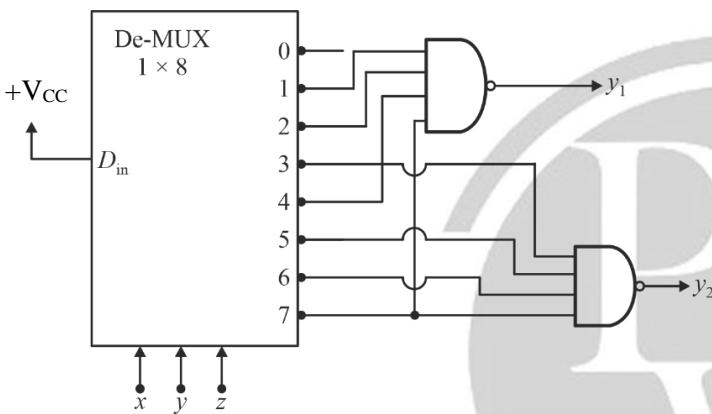
Combinational Circuits

DPP-03

[MCQ]

★★★

1. A demultiplexer of size 1×8 with active low outputs, is programmed as shown below. The circuit has three inputs x, y, z and generates two outputs y_1, y_2 .



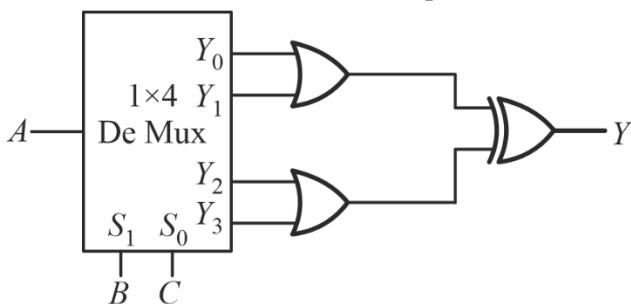
If de-multiplexer has active high output instead of active low outputs, then in order that outputs do not change

- (a) NAND gates should be replaced by NOR gates
- (b) NAND gates should be replaced by OR gates
- (c) NAND gates should be replaced by AND gates
- (d) the inputs x, y, z should be inverted

[MCQ]

★★★

2. For what values of A, B, C the output (Y) will be 0

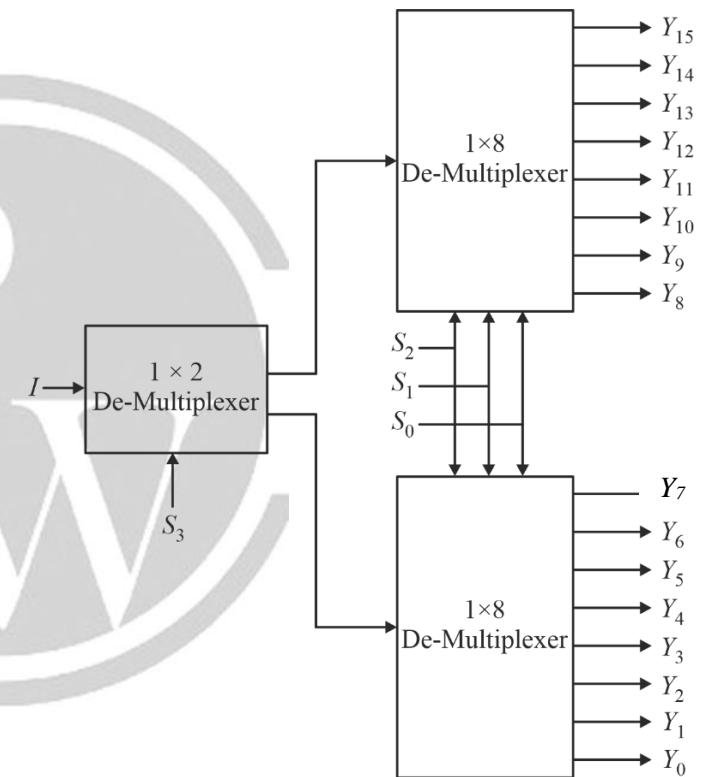


- (a) $A = 1, B = 0, C = 0$
- (b) $A = 0, B = 1, C = 1$
- (c) $A = 1, B = 1, C = 0$
- (d) $A = 1, B = 1, C = 1$

[MCQ]

★★★☆

3. The figure shown below is a block diagram of _____ demultiplexer?



(a) 1 to 4

(b) 1 to 8

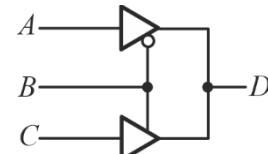
(c) 1 to 16

(d) None of the above

[MCQ]

★★★☆

4. Identify the circuit shown below?



- (a) Bidirectional buffer
- (b) De-multiplexer
- (c) Multiplexer
- (d) Encoder

[NAT]

★☆☆

5. How many inputs will a decimal to BCD encoder have? _____

[MCQ]

★☆☆

6. Which one of the following de multiplexer requires only five select lines?
- 1×2 de Mux
 - 1×4 De Mux
 - 1×8 De Mux
 - 1×32 De Mux

[NAT]

★☆☆

7. What is the minimum number of 1×4 De Mux required to implement 1×2^{10} De Mux. _____

[MCQ]

★☆☆

8. To implement a $1 : 128$ De-Mux we require M number of $1 : 8$ De-mux and N numbers of $1 : 2$ De-mux.

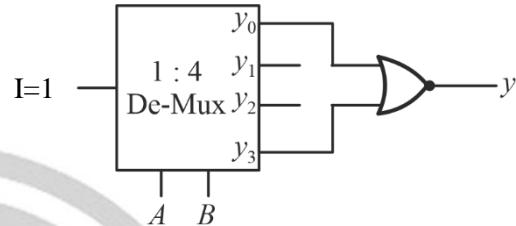
Then which of the following is correct

- $(M - N)/2 = 9$
- $M + N = M$
- $M/N = M$
- $(M + N)/2 = 9$

[MCQ]

★☆☆

9. Consider a circuit as shown below:



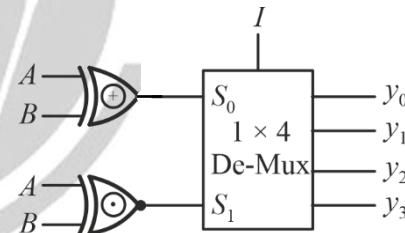
Output y is

- $A + B$
- $\overline{A \cdot B}$
- $A \oplus B$
- $A \odot B$

[MCQ]

★☆☆

10. Consider a combinational circuit as shown below.



For any sequence A, B which of the output pins (y_0 to y_3) can be active

- y_0 and y_3 only
- y_1 and y_2 only
- y_1 only
- all pins can be active

Answer Key

1. (b)
2. (b)
3. (c)
4. (c)
5. (10)
6. (d)
7. (341)
8. (c)
9. (c)
10. (b)



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Digital Logic Combinational Circuit

DPP-04

[MCQ]

★☆☆

1. What are basic gates required to implement a full adder
- 1 EX-OR gate, 1 AND gate
 - 2 EX-OR gate, 1 OR gate
 - 2 EX-OR gate, 2 AND gate, 1 OR gate
 - 1 EX-OR gate, 2 AND gate, 2 OR gate

[NAT]

2. How many half adders are required to implement the following expressions.

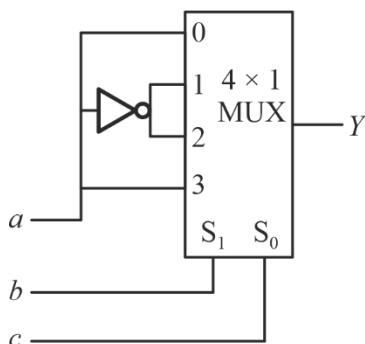
$$D = \bar{A}BC + A\bar{B}C, E = A \oplus B \oplus C$$

$$F = \bar{A}\bar{C} + AB\bar{C} + \bar{B}C$$

[MCQ]

★☆☆

3. The following multiplexer circuit is equivalent to _____.

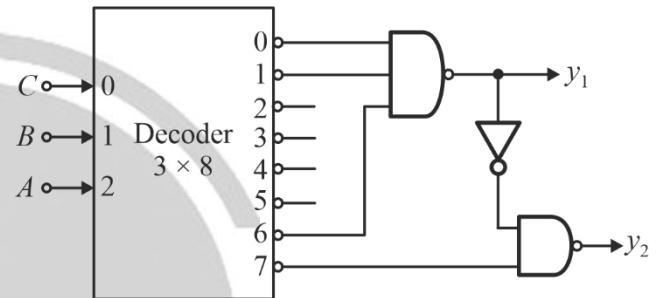


- Implementation of sum equation of full adder
- Implementation of carry equation of full adder
- Implementation of borrow equation of full subtractor
- All the above

[MCQ]

★☆☆

4. A 3 line to 8 line decoder with three inputs A, B, C and two outputs y_1 and y_2 , is configured as shown below. The minimized expression of outputs will be

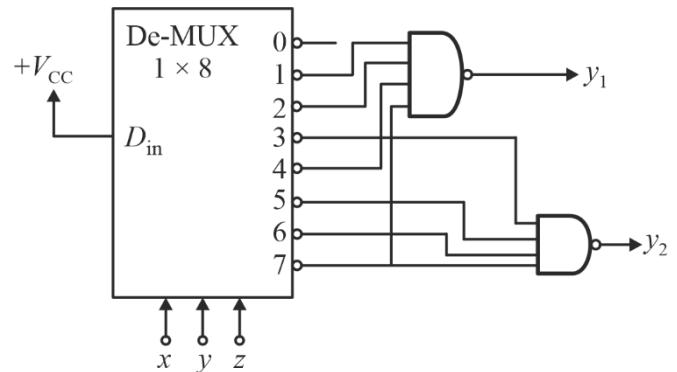


- $y_1 = \bar{A}\bar{B} + AB\bar{C}; y_2 = \bar{A} \oplus B$
- $y_1 = AB + \bar{A}\bar{B}C; y_2 = A \oplus B$
- $y_1 = \bar{A}\bar{B} + A\bar{C}; y_2 = AB + AC$
- $y_1 = A\bar{B} + \bar{A}C; y_2 = \bar{A}B + \bar{B}C$

[MCQ]

★☆☆

5. A demultiplexer of size 1×8 with active low outputs, is programmed as shown below. The circuit has three inputs x, y, z and generates two outputs y_1, y_2 .



★★★☆

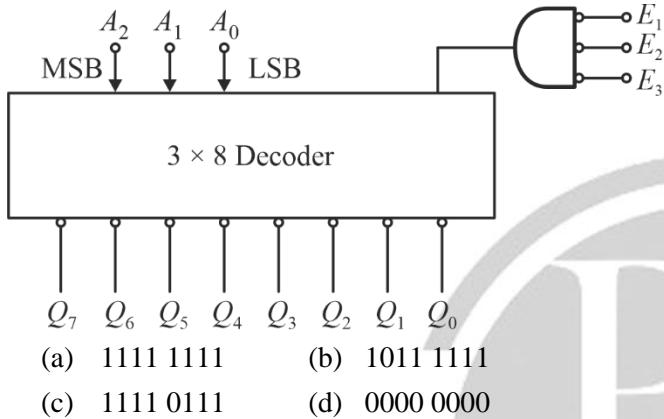
What is this circuit?

- (a) Half subtracter
- (b) Full subtractor
- (c) Half adder
- (d) Full adder

[MCQ]

★★★☆

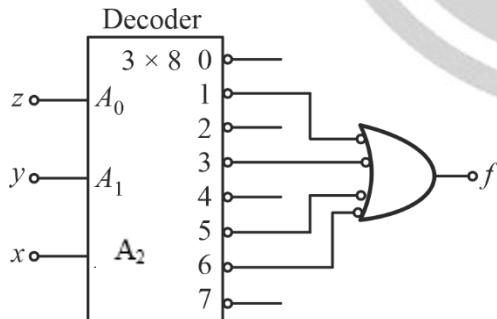
6. The logic diagram of a 3×8 decoder with active low outputs is shown below. What is state of outputs Q_7, \dots, Q_0 for the set of inputs $E_3 = E_1 = 1, E_2 = 0, A_2 = A_1 = 1$ and $A_0 = 0$?



[MCQ]

★★★☆

7. A 3 line to 8 line decoder with active low outputs, is used to realize Boolean function involving three variables x, y and z (x is MSB and z is LSB) as shown below.



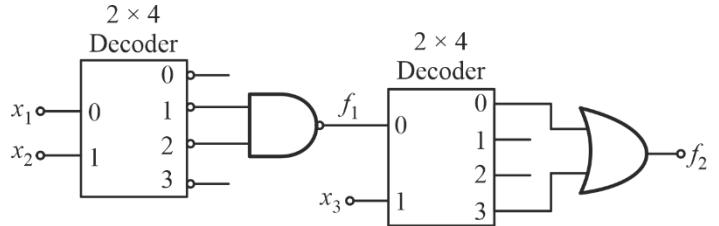
The minimized Boolean function $f(x, y, z)$ in POS format, will be

- (a) $(\bar{x} + \bar{y} + \bar{z})(x + y + z)(x + \bar{y} + \bar{z})(\bar{x} + y + \bar{z})$
- (b) $(\bar{x} + \bar{y} + z)(\bar{x} + y + z)(x + \bar{y} + z)(x + y + \bar{z})$
- (c) $(x + z)(y + z)(\bar{x} + \bar{y} + \bar{z})$
- (d) $(\bar{x} + \bar{z})(\bar{y} + \bar{z})(x + y + z)$

[MCQ]

★★★☆

8. Two 2×4 decoders one with active low outputs and another with active high output are interconnected as shown below. The output function $f_2(x_3, x_2, x_1)$ will be

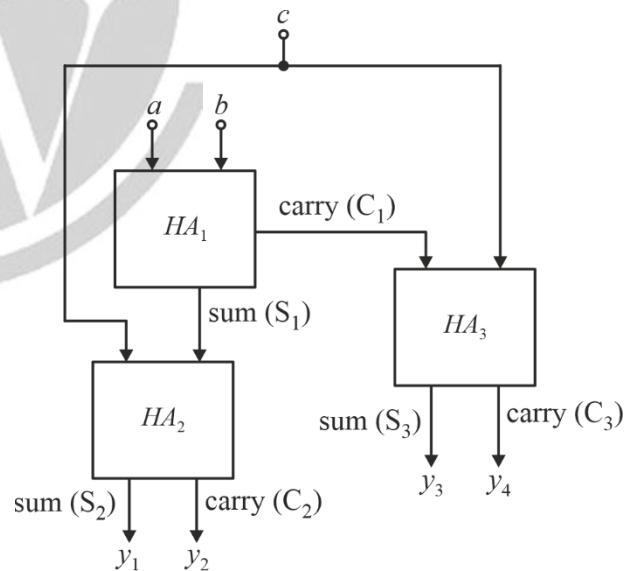


- (a) $f_2 = (x_1 \oplus x_2) \odot x_3$
- (b) $f_2 = (x_1 \odot x_2) \odot x_3$
- (c) $f_2 = (x_1 \oplus x_2) \oplus x_3$
- (d) $f_2 = (x_1 \oplus x_2) \oplus x_3$

[MCQ]

★★★☆

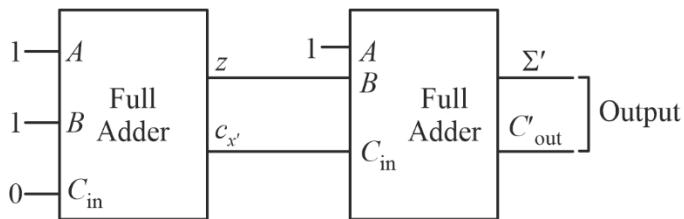
9. Three half adders HA_1, HA_2 and HA_3 are intercoupled as shown below. The four output functions y_1, y_2, y_3 and y_4 are expressed in terms of inputs a, b and c . Which one of the following output expressions, is correct?



- (a) $y_1 = (a \oplus b)c$
- (b) $y_2 = (a \oplus b) \oplus c$
- (c) $y_3 = ab \oplus c$
- (d) $y_4 = a(b \oplus c)$

[MCQ]

10. Determine the outputs for the circuit shown below.



- (a) $\Sigma' = 1, C'_\text{out} = 1$
- (b) $\Sigma' = 0, C'_\text{out} = 0$
- (c) $\Sigma' = 0, C'_\text{out} = 1$
- (d) $\Sigma' = 1, C'_\text{out} = 0$

★☆☆**[MCQ]**

11. How many half adders, will be required to add two k bit numbers?

- | | |
|--------------|----------------|
| (a) $2k + 1$ | (b) $2k - 1$ |
| (c) $2k$ | (d) $2(k + 1)$ |

★★☆**[NAT]**

12. Eight 1-bit full adders are cascaded. Each 1-bit full adder generates carry out bit in 10 ns and sum bit in 30 ns. The number of addition performed per second, will be _____ $\times 10^7$.



Answer Key

1. c
2. 3
3. a
4. a
5. d
6. a
7. c
8. a
9. c
10. c
11. b
12. 1



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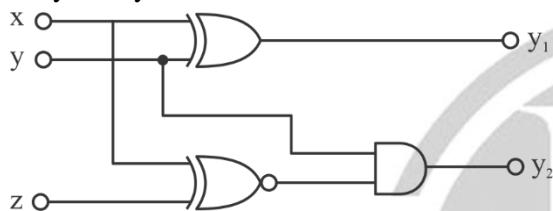
Digital Logic Combinational Circuit

DPP-05

[MCQ]

★☆☆

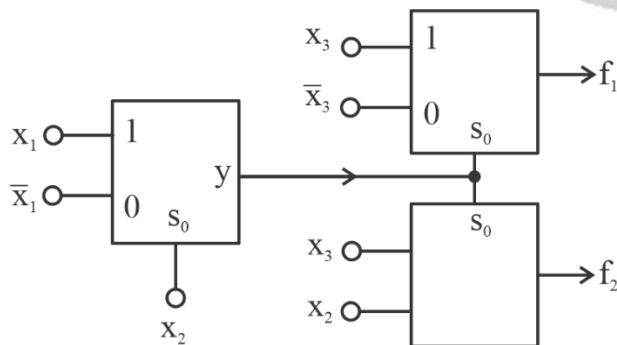
1. The circuit shown below, is a controlled half adder/ half subtractor. The inputs to half adder/ half subtractor are x and y while z is a control. The outputs are y_1 and y_2 .



- (a) Half adder for $z = 0$
- (b) Half subtractor for $z = 1$
- (c) Half adder for $z = 1$ and half subtractor for $z = 0$
- (d) Half adder regardless of whether $z = 0$ or $z = 1$ due to design defect.

Statement for question 2 & 3.

Three multiplexer of size 2×1 , are interconnected as shown below:

**[MCQ]**

★☆☆

2. The function f_1 and f_2 are

- (a) $f_1 = (x_1 \oplus x_2)x_3$ and $f_2 = x_1\bar{x}_2 + x_1\bar{x}_3 + x_2x_3$
- (b) $f_1 = x_1 \oplus x_2 \oplus x_3$ and $f_2 = \bar{x}_1x_2 + \bar{x}_1x_3 + x_2x_3$
- (c) $f_1 = \overline{(x_1 \oplus x_2 \oplus x_3)}$ and $f_2 = x_1x_2 + x_1x_3 + x_2x_3$
- (d) $f_1 = x_1(x_2 \oplus x_3)$ and $f_2 = x_1x_2 + x_1x_3 + \overline{x_2x_3}$

[MCQ]

★☆☆

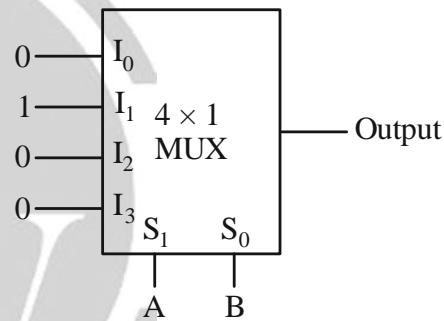
3. What is this circuit?

- (a) Full adder
- (b) Full subtractor
- (c) Magnitude comparator
- (d) Priority encoder

[MCQ]

★☆☆

4. The output of the following circuit diagram represents



- (a) Borrow of half subtractor
- (b) Carry of Half Adder
- (c) Sum of half adder
- (d) None of them

[MCQ]

★☆★

5. The design of a combinational logic circuit with three inputs x , y , z and three outputs A , B , C is attempted. The constraint is that designer has only HA, HS, FA and FS units only in his inventory.

When the binary input is 0, 1, 2 or 3 the binary output is same as input and when binary input is 4, 5, 6 or 7 the binary output is 2 less than binary input. What completes the design?

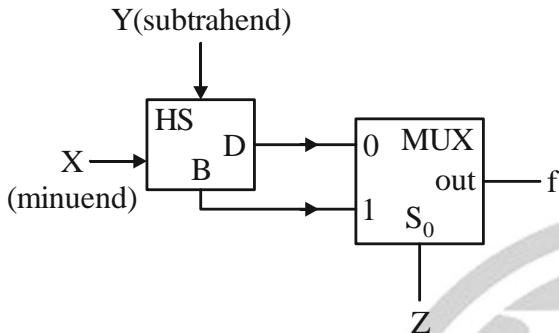
- (a) One FA and one HS
- (b) One HA and one HS
- (c) One HA only
- (d) One FA only

[NAT]**★☆☆**

6. A serial adder is operating with a clock frequency of 10 MHz. The time required to sum 1011011 and 10110 is _____ (in μ sec)

[MCQ]**★☆☆**

7. A half subtractor (HS) and 2×1 MUX are interconnected as demonstrated below. What is NOT correct about this circuit?



- (a) For $Z = 0$, $f = 1$ indicates that the minuend and the subtrahend bits are different.
- (b) For $Z = 0$, $f = 0$ indicates that minuend and subtrahend bits are same, that is, $X = Y = 0$ or $X = Y = 1$.
- (c) For $Z = 1$, $f = 1$ indicates that $X < Y$.
- (d) For $Z = 1$, $f = 0$ indicates that subtrahend bit is definitely 0.

[MCQ]**★☆☆**

8. What does minuend and subtrahend denotes in a subtractor?

- (a) Their corresponding bits of input
- (b) Its output
- (c) Its input
- (d) Borrow bits

[MCQ]**★☆☆**

9. What is the expression for difference, borrow of full subtractor circuit

- (a) Diff = $A \oplus B \oplus C$,
Borrow = $\bar{A}C + (A \odot B)C$
- (b) Diff = $A \oplus B \oplus C$,
Borrow = $\bar{A}B + (\bar{A} \oplus B) \cdot C$
- (c) Diff = $A \odot B \odot C$,
Borrow = $\bar{A}B + (\bar{A} \odot B)C$
- (d) Diff = $A \odot B \odot C$,
Borrow = $\bar{A}C + (A \odot B)C$

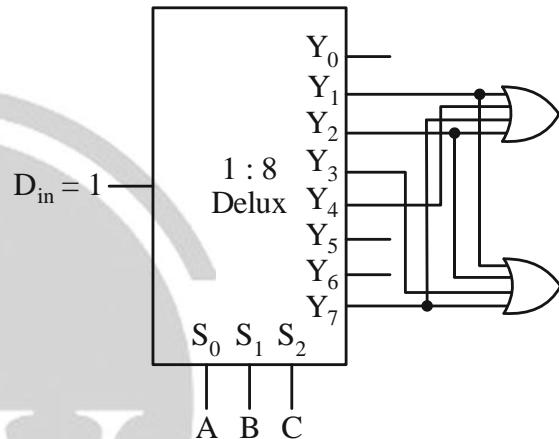
[MCQ]**★☆☆**

10. A D flip-flop is used in a 4-bit serial adder, why?

- (a) It is used to invert the input of the full adder
- (b) It is used to store the output of the full adder
- (c) It is used to store the carry output of the full adder
- (d) It is used to store the sum output of the full adder

[MCQ]**★☆☆**

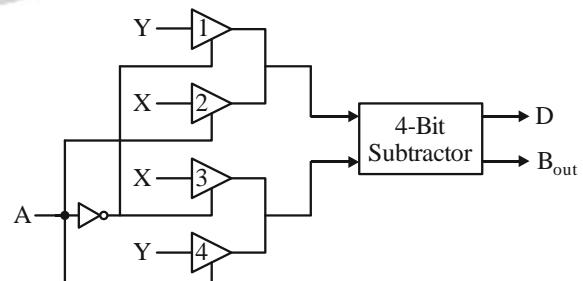
11. The circuit shown in the given figure represents a/an:



- (a) decoder
- (b) equality detector
- (c) full adder
- (d) full subtractor

[MCQ]

12. Consider the following circuit diagram



A 4-bit subtractor, four 4-bit three-state buffers (with bus input and output), and one inverter is used to subtract two numbers ($Y - X$), $X = 0101$ and $Y = 0010$. If $A = 0$, then D and B_{out} are respectively

- (a) 0011 and 0
- (b) 1101 and 0
- (c) 0011 and 1
- (d) 1101 and 1

Answer Key

- | | |
|--|---|
| 1. (c)
2. (b)
3. (b)
4. (a)
5. (c)
6. (0.7) | 7. (d)
8. (c)
9. (b)
10. (c)
11. (d)
12. (d) |
|--|---|



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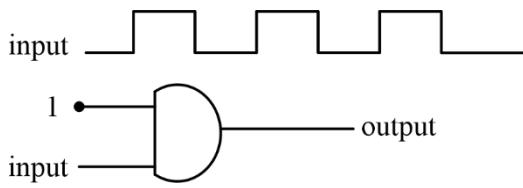
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Digital Logic

Logic Gate

DPP-01

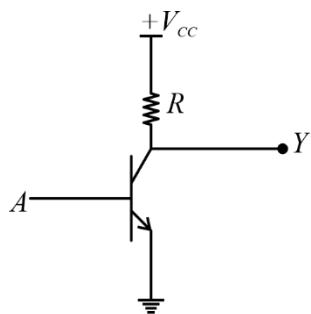
1. The input wave form is given



Draw output wave form

- (a)
- (b)
- (c)
- (d)

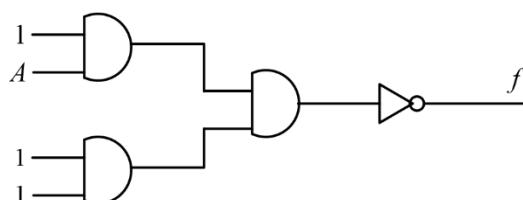
- 2.



When $A = 1$ then the value of Y equal

- (a) 0
- (b) 1
- (c) V_{CC}
- (d) none of the above

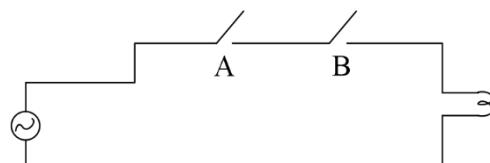
- 3.



Find value of f ?

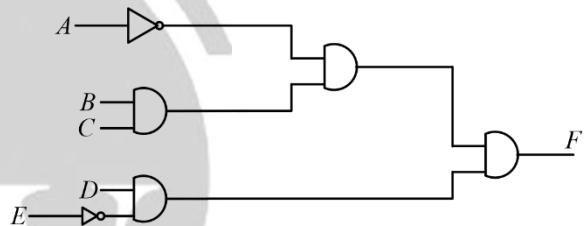
- (a) 1
- (b) 0
- (c) A
- (d) \bar{A}

4. Bulb will glow when A and B are respectively.



- (a) 00
- (b) 01
- (c) 10
- (d) 11

5. Find expression of F

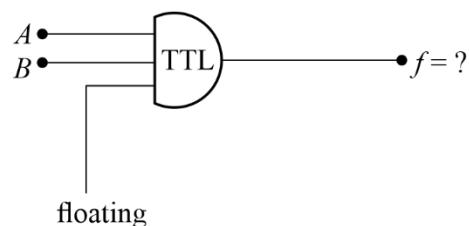


- (a) $\bar{A}BC + D\bar{E}$
- (b) $\bar{A}BCD\bar{E}$
- (c) $(\bar{A} + BC)D\bar{E}$
- (d) $\bar{A}BC(D + \bar{E})$

6. The inverter is _____ gate

- (a) AND
- (b) OR
- (c) NOT
- (d) none of the above

- 7.

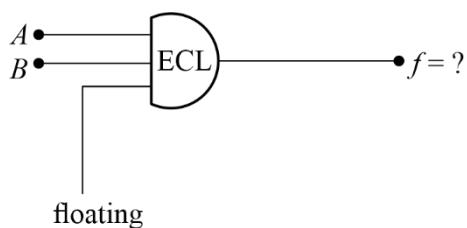


Find expression of f ?

- (a) AB
- (b) 1
- (c) $A + B$
- (d) \overline{AB}

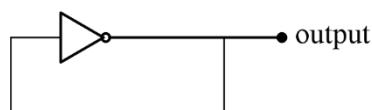
\overline{AB}

8.

Find expression of f ?

- (a) 0
- (b) 1
- (c) AB
- (d) \overline{AB}

09.

Find output frequency, if the propagation delay of NOT gate is $2 n$ sec.

- (a) 125 MHz
- (b) 500MHz
- (c) 250 MHz
- (d) none of the above



Answer Key

1. (d)
2. (a)
3. (d)
4. (d)
5. (b)
6. (c)
7. (a)
8. (a)
9. (c)



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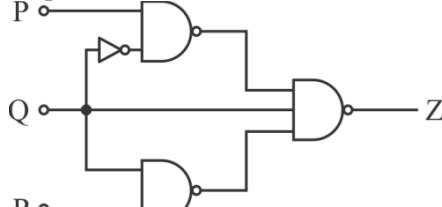
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Subject : Digital Logic

Chapter : Logic Gate

DPP-02

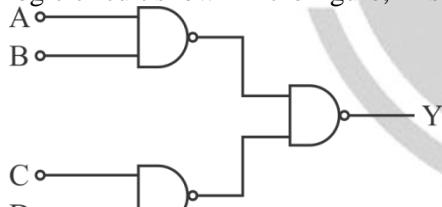
1. For a 3-input logic circuit shown below, the output Z can be expressed as



- (a) $Q + \bar{R}$ (b) $P\bar{Q} + R$
 (c) $\bar{Q} + R$ (d) $P + \bar{Q} + R$

2. The complete set of only those Logic Gates designated as Universal Gates is
 (a) NOT, OR and AND Gates
 (b) XNOR, NOR and NAND Gates
 (c) NOR and NAND Gates
 (d) XOR, NOR and NAND Gates

3. In the logic circuit shown in the figure, Y is given by



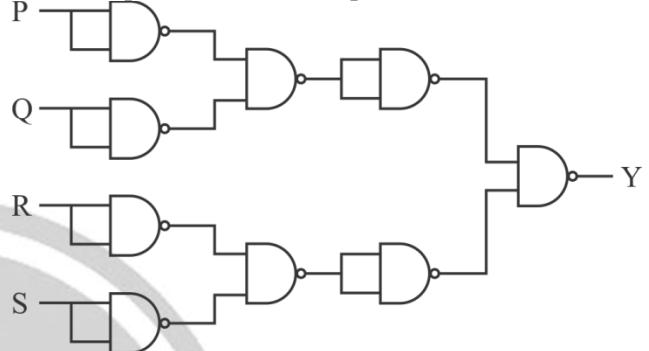
- (a) $Y = ABCD$
 (b) $Y = (A+B)(C+D)$
 (c) $Y = A + B + C + D$
 (d) $Y = AB + CD$

4. $F = AB + CD + E$ will be implemented with how many minimum number NAND gates?
 (a) Three (b) Four
 (c) Five (d) Six

5. The minimum number of NAND gates required to reduce the expression $((A + B) C) D$ is
 (a) 6 (b) 5
 (c) 8 (d) 4

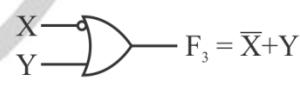
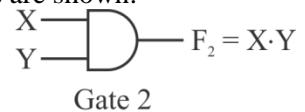
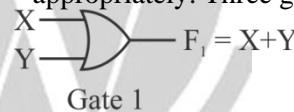
6. In a two-input NAND gate, if both inputs are shorted, it will behave like a _____ gate.
 (a) Buffer (b) AND
 (c) NOT (d) EX-OR

7. For the circuit shown in figure the Boolean expression for the output Y in terms of inputs P, Q, R and S is



- (a) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$ (b) $P + Q + R + S$
 (c) $(\bar{P} + \bar{Q}) + (\bar{R} + \bar{S})$ (d) $(P + Q)(R + S)$

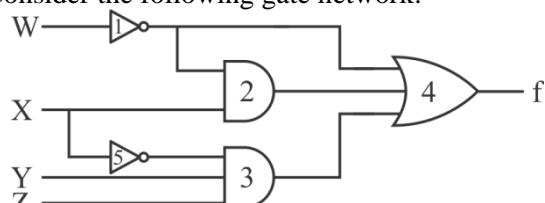
8. A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown:



Which one of the following statements is TRUE ?

- (a) Gate 1 is a universal gate.
 (b) Gate 2 is a universal gate.
 (c) Gate 3 is a universal gate
 (d) None of the shown is a universal gate.

9. Consider the following gate network:



Which one of the following gates is redundant?

- (a) Gate No. 1 (b) Gate No. 2
 (c) Gate No. 3 (d) Gate No. 4

10. The minimum of NAND gates required to implement $A + A B C$ is equal to
 (a) 0 (b) 1
 (c) 4 (d) 7

Answer Key

- 1. (c)
- 2. (c)
- 3. (d)
- 4. (d)
- 5. (b)

- 6. (c)
- 7. (b)
- 8. (c)
- 9. (b)
- 10. (a)



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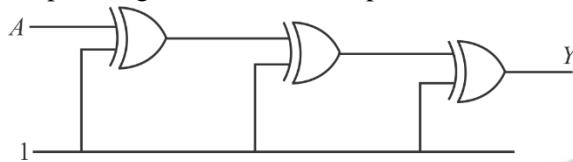
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Subject : Digital Logic

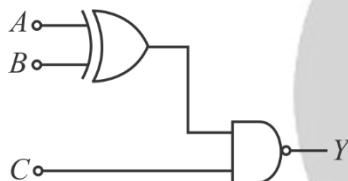
Chapter : Logic Gate

DPP-03

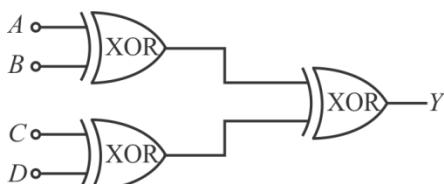
1. The initial output of the following circuit is 1. If we apply 010101 at input A (first bit is zero), then what is the bit pattern generated at the output Y.



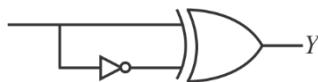
- (a) 010101 (b) 101010
 (c) remains at 0 (d) remains at '1'
2. The Boolean expression of the output of the logic circuit shown in figure is



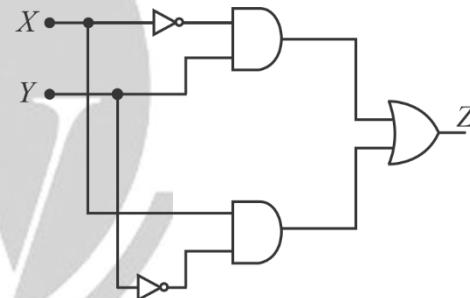
- (a) $Y = \bar{A}\bar{B} + AB + \bar{C}$
 (b) $Y = \bar{A}\bar{B} + AB + C$
 (c) $Y = \bar{A}\bar{B} + \bar{A}\bar{B} + C$
 (d) $Y = \bar{A}\bar{B} + \bar{A}\bar{B} + C$
3. A, B, C and D are input, and Y is the output bit in the XOR gate circuit of the figure below. Which of the following statements about the sum S of A, B, C, D and Y is correct?



- (a) S is always either zero or odd.
 (b) S is always either zero or even.
 (c) S = 1 only if the sum of A, B, C and D is even.
 (d) S = 1 only if the sum of A, B, C and D is odd.
4. The output Y of the logic circuit given below is



- (a) 1 (b) 0
 (c) x (d) \bar{x}
5. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles
- (a) an AND gate (b) an OR gate
 (c) an XOR gate (d) a NAND gate
6. In the circuit shown below, X and Y are digital inputs, and Z is a digital output. The equivalent circuit is



- (a) XNOR gate (b) NOR gate
 (c) NAND gate (d) XOR gate
7. Which one of the following gate is also known as equivalence gate?
- (a) EX-OR (b) AND
 (c) EX-NOR (d) NOR
8. The logic function $f = \overline{xy + \bar{x}\bar{y}}$ is equal to
- (a) EX-NOR (b) NAND
 (c) EX-OR (d) NOR
9. The minimum number of 2 input NOR gates required to implement a 2 input XOR gate is _____
10. The minimum number of 2 input NAND gates required to implement a 2 input EX-NOR gates is
- (a) 4 (b) 5
 (c) 3 (d) 6

Answer Key

- | | |
|--|---|
| 1. (b)
2. (a)
3. (b)
4. (a)
5. (c) | 6. (d)
7. (c)
8. (c)
9. (5)
10. (b) |
|--|---|



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Subject : Digital Logic

Chapter : Minimization

DPP-01

- 1.** Find out minimize expression for following function.

$$f = ABC\bar{C} + ABC + \bar{A}BC$$

- (a) $AB + BC$ (b) $A\bar{C} + \bar{A}B$
 (c) $BC + \bar{A}B$ (d) $\bar{A}B + BC$

- 2.** Find out minimize expression for following function.

$$f = AB + A\bar{B} + \bar{A}\bar{B}$$

- (a) $\bar{A} + B$ (b) $A + \bar{B}$
 (c) $\bar{A} + \bar{B}$ (d) $A + B$

- 3.** Find out minimize expression for following function.

$$f = (A + B)(A + \bar{B})(\bar{A} + B)(\bar{A} + \bar{B})$$

- (a) 1 (b) $\bar{A}\bar{B}$
 (c) 0 (d) $A\bar{B}$

- 4.** Find out minimize expression for following function.

$$f = (A + B + C)(A + B + \bar{C})$$

- (a) $(A + C)B$ (b) $A + B$
 (c) $AB\bar{C}$ (d) $A(B + C)$

- 5.** The Boolean expression

$$f = (X + Y)(X + \bar{Y}) + \bar{X}\bar{Y} + \bar{X}$$

- (a) Y (b) X
 (c) $\bar{X}\bar{Y}$ (d) $X + \bar{Y}$

- 6.** The logic expression

$$f = X + \bar{X}Y$$

Is equivalent to

- (a) $X + Y$ (b) XY
 (c) $\bar{X} + Y$ (d) $X + \bar{Y}$

- 7.** The logic expression

$$f = (A + B)(A + C)$$

Is equivalent to

- (a) $A + BC$ (b) $B + AC$
 (c) $C + AC$ (d) $\bar{A} + BC$

- 8.** The Boolean expression

$$f = (1 + \bar{A})(B + AC)$$

is equivalent to

- (a) $AC + B$ (b) $\bar{A}C + B$
 (c) $\bar{A} + BC$ (d) 1

- 9.** Find minimization expression

$$f = (A + \bar{A}) + (BC + AC)(A + D)$$

- (a) 1 (b) 0
 (c) $AB + CD$ (d) $ABC + BCD + ACD$

- 10.** Find out minimization

$$f = (A + B)(A + B + C)$$

- (a) $B + C$ (b) $A + B$
 (c) $A + B + C$ (d) $AB + BC + AC$

Answer Key

- 1. (a)
- 2. (b)
- 3. (c)
- 4. (b)
- 5. (b)

- 6. (a)
- 7. (a)
- 8. (a)
- 9. (a)
- 10. (b)



Hints and solutions

1. $f = ABC\bar{C} + ABC + \bar{A}BC$

$$= AB + \bar{A}BC$$

$$= B(A + \bar{A}C)$$

$$= B(A + C)(A + \bar{A})$$

$$= AB + BC$$

2. $f = AB + A\bar{B} + \bar{A}\bar{B}$

$$= AB + (A + \bar{A})\bar{B}$$

$$= AB + \bar{B}$$

$$= (A + \bar{B})(B + \bar{B})$$

$$= A + \bar{B}$$

3. $f = (A + AB + A\bar{B})(\bar{A} + \bar{A}B + \bar{A}\bar{B})$

$$f = 0$$

4. $f = (A + B + C)(A + B + \bar{C})$

$$f = (A + AB + AC)(AB + B + BC)(A\bar{C} + B\bar{C} + 0)$$

$$f = (A)(B)(A\bar{C} + B\bar{C})$$

$$f = ABC\bar{C} + AB\bar{C}$$

$$f = ABC\bar{C}$$

5. Let $f = (X + Y)(X + \bar{Y}) + (\bar{X}\bar{Y}) + \bar{X}$

$$f = (X + Y)(X + \bar{Y}) + \bar{X}\bar{Y} \cdot \bar{X}$$

$$f = (X + Y)(X + \bar{Y}) + (X + Y)X$$

$$f = (X + Y)(X + \bar{Y}) + X + XY$$

$$f = X + XY + X\bar{Y} + Y\bar{Y} + X + XY$$

$$f = X[1 + Y + \bar{Y} + 1 + Y]$$

$$f = X$$

6. $f = X + \bar{X}Y$

$$f = (X + \bar{X})(X + Y)$$

$$f = X + Y$$

7. $f = (A + B)(A + C)$

$$f = A + AB + AC + BC$$

$$f = A + BC$$

8. $f = (1 + \bar{A})(B + AC)$

$$f = 1 \cdot (AC + B)$$

$$f = AC + B$$

9. $f = (A + \bar{A}) + (BC + AC)(A + D)$

$$f = 1 + (BC + AC)(A + D)$$

$$f = 1$$

10. $f = (A + B)(A + B + C)$

$$f = A + AB + AB + B + AC + BC$$

$$f = A + B$$



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Subject : Digital Logic Minimization

DPP-02

1. For the given Boolean function $f(A, B, C) = \sum_m(0,1,5,6)$

$$\sum_m(0,1,5,6)$$

Simplified output will be

- (a) $A\bar{B} + B\bar{C} + AB\bar{C}$
 - (b) $\bar{A}\bar{B} + \bar{B}\bar{C} + AB\bar{C}$
 - (c) $A\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{B}\bar{C}$
 - (d) $\bar{A}\bar{B} + \bar{B}\bar{C} + AB\bar{C}$
2. For the given Boolean function $f(A, B, C) = \sum_m(1,3,6,7) + \sum_d(0,2)$ simplified output will be

- (a) $A + B$
- (b) $B + C$
- (c) $\bar{A} + B$
- (d) $\bar{A}C + AB$

3. What is the other canonical form of the given function $f(A, B, C) = \sum_m(0,1,2,3,4,5,6,7)$

- (a) $f(A, B, C) = \Pi_M(0,1,2,3,4,5,6,7)$
- (b) $f(A, B, C) = \Pi_M(0, 2, 4, 7)$
- (c) $f(A, B, C) = \Pi_M(1,2,4,7)$
- (d) Does not exist

4. The product of all the maxterms of a given Boolean function is always equal to _____?

- (a) 0
- (b) 1
- (c) 2
- (d) Complement of the function

5. The simplified SOP form of the k-map is

		yz	00	01	11	10	
		wx	00	1	1	x	1
		wx	01	0	0	0	0
		wx	11	0	0	0	0
		wx	10	1	x	x	1

- (a) $\bar{x}\bar{z} + \bar{w}\bar{x}\bar{y}$
- (b) \bar{x}
- (c) $\bar{w}\bar{x} + w\bar{x}$
- (d) $\bar{x}\bar{z}$

6. The Boolean function $f(A, B, C, D) = \sum_m(5,7,9,11,13,15)$ is independent of variables
- (a) A
 - (b) C
 - (c) B
 - (d) B and C

7. The simplified Boolean function is

		BC	00	01	11	10	
		A	0	1	0	1	0
		A	1	0	1	0	1
		A					

- (a) $A \oplus B \oplus C$
- (b) $A \oplus B \odot C$
- (c) $A \odot B \odot C$
- (d) $A \odot B \oplus C$

8. The simplified Boolean expression $f(w, x, y, z) = \sum_m(0, 2, 5, 9, 15) + \sum_d(6, 7, 8, 10, 12, 13)$

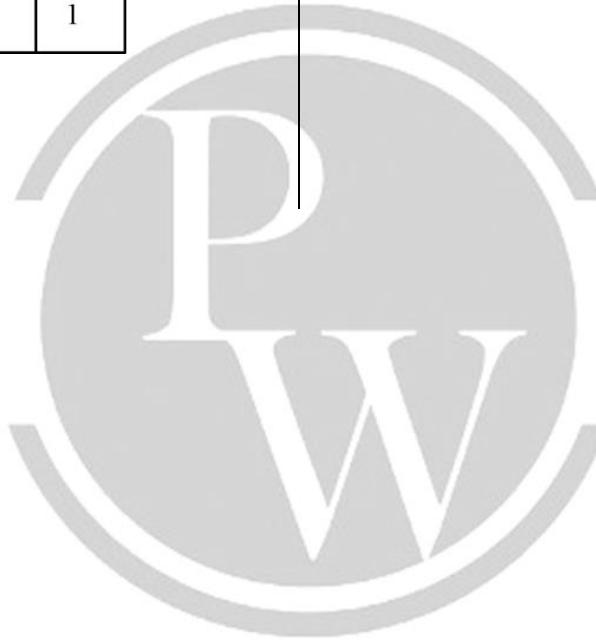
- (a) $\bar{x}\bar{z} + w\bar{y} + xz$ (b) $\bar{x}\bar{z} + w\bar{y} + x\bar{z}$
 (c) $x\bar{z} + w\bar{y} + \bar{x}z$ (d) $\bar{x}\bar{z} + \bar{w}\bar{y} + xz$

9. The minimum number of NAND gate required to simplify k-map

		BC	00	01	11	10
		A	0	1	1	1
		A	1	0	1	1
(a)	4					
(b)	3					
(c)	5					
(d)	9					

10. The simplified expression of k-map is independent of variables

		BC	00	01	11	10
		A	0	1	1	1
		A	1	1	1	1
(a)	A					
(b)	B					
(c)	C					
(d)	A, B and C					



Answer Key

- 1. (b)
- 2. (c)
- 3. (d)
- 4. (a)
- 5. (b)
- 6. (b)

- 7. (b, d)
- 8. (a)
- 9. (b)
- 10. (d)

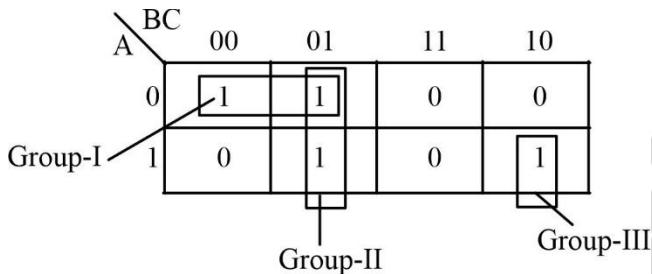


Hints and Solutions

1. (b)

$$\text{Given: } f(A, B, C) = \sum_m(0, 1, 5, 6)$$

3 variable k-map

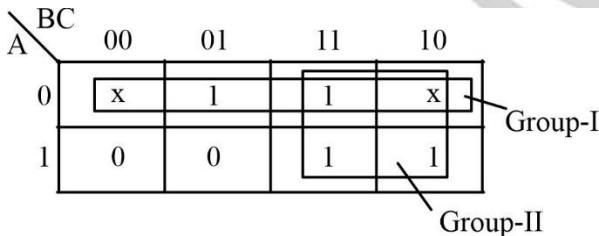


$$\text{The simplified output expression } f(A, B, C) = \bar{A}\bar{B} + \bar{B}C + AB\bar{C}$$

2. (c)

$$\text{Given: } f(A, B, C) = \sum_m(1, 3, 6, 7) + \sum_d(0, 2)$$

3-variable k-map



$$\therefore (A, B, C) = \bar{A} + B$$

3. (d)

$$\text{Given: } f(A, B, C) = \sum_m(0, 1, 2, 3, 4, 5, 6, 7)$$

In these functions are min terms are covering.

The relation between min terms and max terms is

$$x_j = \bar{x}_j$$

\therefore Hence max term does not exist

4. (a)

The product of all the max terms is always zero.

5. (b)

Given: k-map

wx	yz	00	01	11	10
00	1	1	x	1	
01	0	0	0	0	
11	0	0	0	0	
10	1	x	x	1	

$$f(w, x, y, z) = \bar{x}$$

6. (b)

k-map of 4-variables

	CD	00	01	11	10
AB	00	0	0	0	0
01	0	1	1	0	
11	0	1	1	0	
10	0	1	1	0	

$$f(A, B, C, D) = BD + AD$$

\therefore function is independent of C.

7. (b, d)

	BC	00	01	11	10
A	0	(1)	0	(1)	0
	1	0	(1)	0	(1)

$$f(A, B, C) = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}C + AB\bar{C}$$

$$f(A, B, C) = \bar{A}(B \odot C) + A(B \oplus C)$$

$$f(A, B, C) = \bar{A}(\overline{B \odot C}) + A(B \oplus C)$$

$$f(A, B, C) = \bar{A}(B \odot C) + A(\overline{B \oplus C})$$

$$f(A, B, C) = A \oplus B \odot C \text{ or } A \odot B \oplus C$$

8. (a)

	yz	00	01	11	10
wx	00	1	0	0	1
	01	0	1	x	x
	11	x	x	1	0
	10	x	1	0	x

$$f(w, x, y, z) = \bar{x}\bar{z} + w\bar{y} + xz$$

9. (b)

	BC	00	01	11	10
A	0	1	1	0	0
	1	0	0	1	1

$$f(A, B, C) = \bar{A}\bar{B} + AB$$

$$f(A, B, C) = A \odot B$$

Hence 5 NAND gate required

10. (d)

	BC	00	01	11	10
A	0	1	1	1	1
	1	1	1	1	1

$$f(A, B, C) = 1$$

Hence independent of A, B and C.



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Subject : Digital Logic

Topic : Number System

DPP - 01

- 1.** The two addition operations $24 + 14 = 41$ and $23 + 12 = 101$ are performed on number bases b_1 and b_2 respectively. The values of b_1 and b_2 are respectively
 (a) 7 and 4 (b) 4 and 7
 (c) 8 and 4 (d) 4 and 8
- 2.** If x and y are successive numbers in a number system of base b such that $(xy)_b = (25)_{10}$ and $(yx)_b = (31)_{10}$, then
 (a) $x = 4, y = 5$ and $b = 7$
 (b) $x = 3, y = 4$ and $b = 6$
 (c) $x = 4, y = 5$ and $b = 6$
 (d) $x = 3, y = 4$ and $b = 7$
- 3.** If $a = (4.4)_5$ and $b = (3.3)_5$, then $a + b = (x)_5$. The subscript 5 denotes the base on which the corresponding number is expressed. The value of x is
 (a) 31.2 (b) 7.2
 (c) 8.7 (d) 13.2
- 4.** If $(X 1CY)_{16} = (120702)_8$, then X and Y are
 (a) A and 2 (b) B and 1
 (c) 1 and B (d) 2 and A
- 5.** Given $(135)_b + (144)_b = (323)_b$ where subscript b denotes the base on which numbers are expressed. What is value of b ?
 (a) 4 (b) 5
 (c) 6 (d) 7
- 6.** In a digital computer, binary subtraction is performed
 (a) In the same way as we perform subtraction in decimal number system
 (b) Using two's complement method
 (c) Using 9's complement method.
 (d) Using 10's complement
- 7.** The greatest negative number, which can be stored in a computer that has 8-bit word length and uses 2's complement arithmetic, is
 (a) -256 (b) -255
 (c) -128 (d) -127
- 8.** F's complement of $(2BFD)_{hex}$ is
 (a) E304 (b) D403
 (c) D402 (d) C403
- 9.** The result of addition operation $34 + 43$ performed on minimum base is stored in an 8-bit register. The content of register will be
 (a) 01000011 (b) 00101010
 (c) 01010101 (d) 01010100
- 10.** Which of the following is equal to $(AB)_{16}$?
 (a) $(B7)_{16} - (A)_{16}$ (b) $(B5)_{16} - (A)_{16}$
 (c) $(A0)_{16} + (D)_{16}$ (d) $(BA)_{16} + (01)_{16}$
- 11.** An equivalent 2's complement representation of the 2's complement number 1101 is
 (a) 110100 (b) 001101
 (c) 110111 (d) 111101
- 12.** The 2's complement representation of -17 is
 (a) 101110 (b) 101111
 (c) 111110 (d) 110001
- 13.** 11001, 1001 and 111001 correspond to the 2's complement representation of which one of the following sets of number?
 (a) 25.9 and 57 respectively
 (b) -6, -6 and -6 respectively
 (c) -7, -7 and -7 respectively
 (d) -25, -9 and -57 respectively

14. $X = 01110$ and $Y = 11001$ are two 5-bit binary numbers represented in two's complement format. The sum of X and Y represented in two's complement format using 6 bits is

- (a) 100111 (b) 001000
(c) 000111 (d) 101001



Answer Key

- | | |
|--|--|
| 1. (a)
2. (d)
3. (d)
4. (a)
5. (c)
6. (b)
7. (c) | 8. (c)
9. (b)
10. (b)
11. (d)
12. (b)
13. (c)
14. (c) |
|--|--|



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Subject : Digital Logic

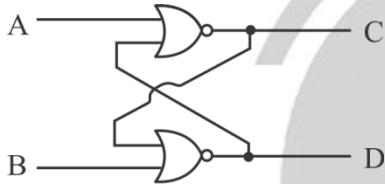
Chapter : Sequential Circuit

DPP - 1

1. In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

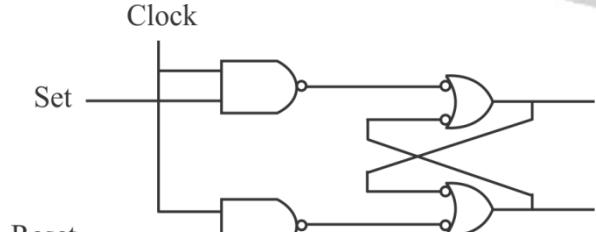
- (a) $Q = 0, Q' = 1$
- (b) $Q = 1, Q' = 0$
- (c) $Q = 1, Q' = 1$
- (d) Indeterminate states

2. In the circuit shown below, when inputs $A = B = 0$, the possible logic states of C and D are



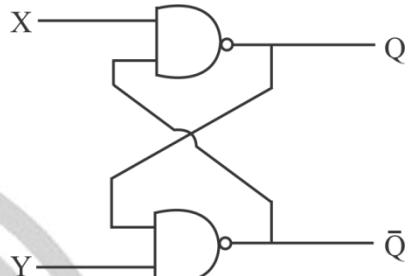
- (a) $C = 0, D = 1$ or $C = 1, D = 0$
- (b) $C = 1, D = 0$
- (c) $C = 1, D = 1$ or $C = 0, D = 0$
- (d) $C = 0, D = 1$

3. The two NAND gates before the latch circuit shown below, are used to



- (a) act as buffers
- (b) operate the latch faster
- (c) avoid racing
- (d) invert the latching action

4. In the circuit shown below, outputs $Q\bar{Q} = 01$, the possible values of X and Y are



- (a) $X = 1, Y = 0$
- (b) $X = 1, Y = 1$
- (c) $X = 0, Y = 1$
- (d) $X = 0, Y = 0$

5. Latch is a device with

- (a) One stable state
- (b) Two stable state
- (c) Three stable state
- (d) Infinite stable states

Answer Key

- 1. (c)
- 2. (a)
- 3. (d)

- 4. (d)
- 5. (b)



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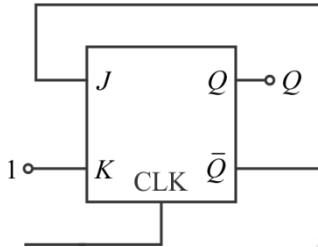


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Subject : Digital Logic

Chapter: Sequential Circuit

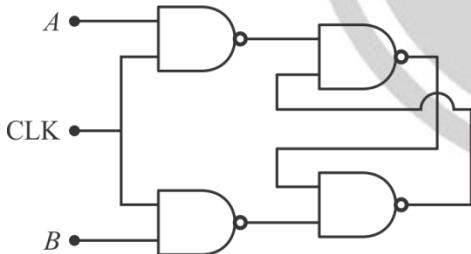
1. Consider the following J-K flip-flop



In the above J-K flip-flop, $J = \bar{Q}$ and $K = 1$. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

- (a) 010000 (b) 011001
 (c) 010010 (d) 010101

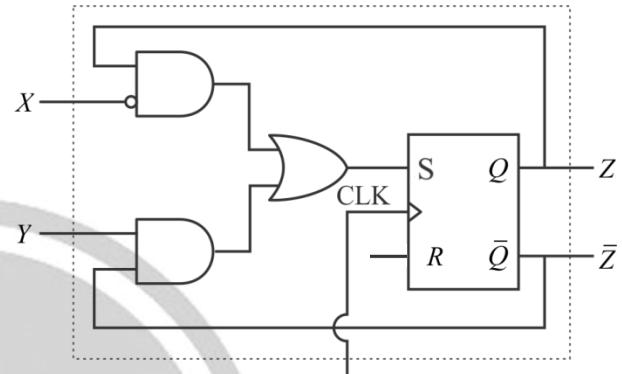
2. Consider the given circuit.



In this circuit, the race around

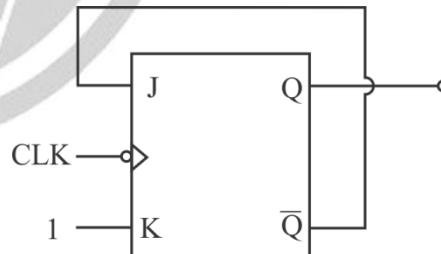
- (a) does not occur.
 (b) occurs when $CLK = 0$.
 (c) occurs when $CLK = 1$ and $A = B = 1$.
 (d) occurs when $CLK = 1$ and $A = B = 0$.

3. A sequential circuit using D Flip-Flop and logic gates is shown in figure, where X and Y are the inputs and Z is the output. The circuit is



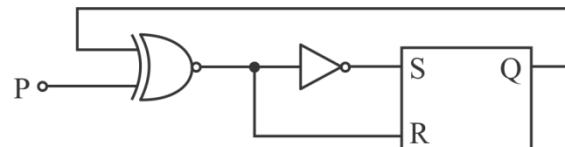
- (a) S-R Flip-Flop with inputs $X = R$ and $Y = S$.
 (b) S-R Flip-Flop with inputs $X = S$ and $Y = R$.
 (c) J-K Flip-Flop with inputs $X = J$ and $Y = K$.
 (d) J-K Flip-Flop with inputs $X = K$ and $Y = J$.

4. The frequency of the clock signal applied to the negative going edge triggered JK flip flop shown below is 5 kHz. What is frequency of signal available at Q ?



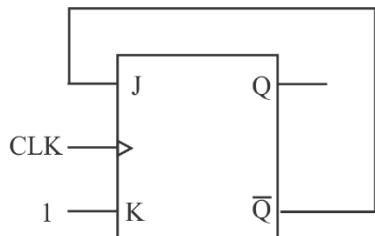
- (a) 2.5 kHz (b) 5 kHz
 (c) 10 kHz (d) 1.25 kHz

5. The RS flip flop is modified so as to realize a flip flop with single input P. The characteristic equation of a new flip-flop will be



- (a) $Q(t+1) = P \oplus Q$
 (b) $Q(t+1) = \overline{P \oplus Q}$
 (c) $Q(t+1) = P + Q$
 (d) $Q(t+1) = P$

6. The J-K FF shown below is initially cleared and then clocked for 5 pulses, the sequence at the Q output will be



- (a) 0 1 0 0 0 0 (b) 0 1 1 0 0 1

- (c) 0 1 0 0 1 0 (d) 0 1 0 1 0 1
7. For a J-K flip-flop, J input is tied to its own \bar{Q} output and its K input is connected to its own Q output. If the flip-flop is fed with a clock of frequency 1 MHz, its Q output frequency (in MHz) will be_____.



Answer Key

1. (d)
2. (a)
3. (d)
4. (a)
5. (a)
6. (d)
7. (0.5)

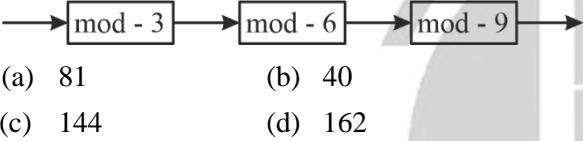
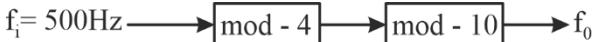


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1. If Mod-60 counter is cascaded with Mod – 40 counter, then it will becomes,
- Mod – 100 counter
 - Mod – 2400 counter
 - Mod – 20 counter
 - Mod – 140 counter
2. The maximum decimal count of 7-bit asynchronous counter is ____.
3. The modulus of given block is,
- 
- 81
 - 40
 - 144
 - 162
4. If input frequency of clock is 10 KHz then output frequency of counter will be ____ KHz [Assume mod of counter is 5]
5. For given block, the value of f_0 is ____ Hz.
- 
6. Symmetric square wave of time period 100 μ sec can be obtained from square wave of time period 10 μ sec by using a
- divide by – 5 circuit
 - divide by – 2 circuit
 - divide by – 5 followed by a divide by 2 – circuit
 - None of these
7. How many flip – flops are required to construct Mod– 31 counter?
- 4
 - 3
 - 2
 - 5

Answer Key

- | | |
|--|-------------------------------|
| 1. (b)
2. (127)
3. (d)
4. (2) | 5. (12.5)
6. (c)
7. (d) |
|--|-------------------------------|



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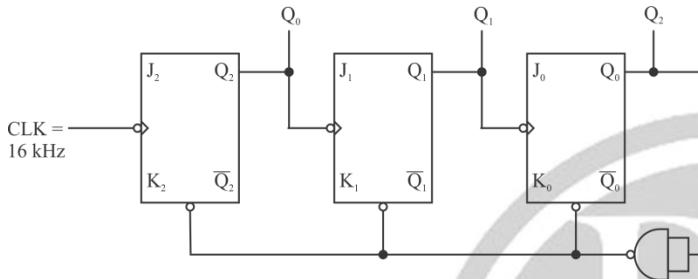


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Subject : Digital Logic
Chapter : Sequential Circuits

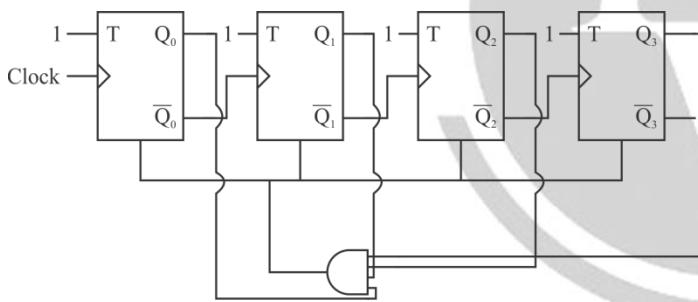
DPP - 04

1. What is the output signal frequency of the following counter if the clock signal frequency is 16 kHz? All 'J' and 'K' inputs are connected to 1.



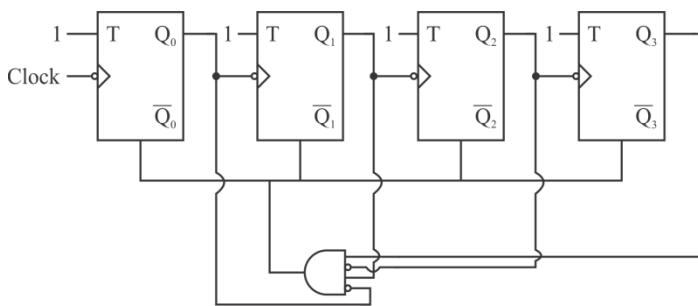
- (a) 4 kHz (b) 8 kHz
 (c) 10 kHz (d) 16 kHz

2. The circuit is counter of mod

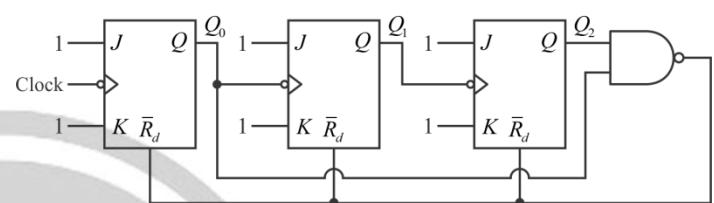


- (a) Mod-0 (b) Mod-16
 (c) Mod-15 (d) Mod-14

3. The circuit is a counter of mod

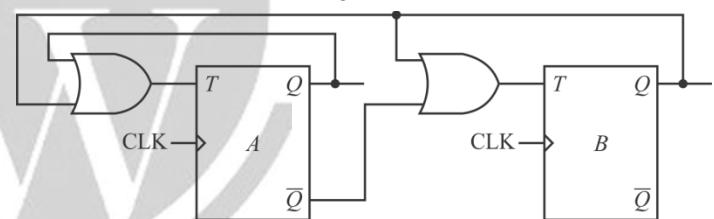


4. The circuit shown consists of J-K flip-flops, each with an active low asynchronous reset (\bar{R}_d input). The counter corresponding to this circuit is



- (a) a modulo-5 binary up counter.
 (b) a modulo-6 binary down counter.
 (c) a modulo-5 binary down counter.
 (d) a modulo-6 binary up counter.

5. The circuit shown in figure is



- (a) a MOD-2 counter
 (b) a MOD-3 counter
 (c) generate sequence 00, 10, 01, 00.....
 (d) generate sequence 00, 10, 00, 10, 00

Answer Key

- 1. (a)
- 2. (c)
- 3. (10)
- 4. (a)

- 5. (b)



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