OVERALL ANALYSIS | Solution Report

All | Correct Answers | Wrong Answers | Not Attempted Questions

Q.1) Max Marks: 1

Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate-Speed up ratio

Correct Answer

Solution: (2.8)
Answer: 2.8
Cycle time
= Maximum delay due to any stage + Delay due to its register
= Max { 60, 50, 90, 80 } + 10 ns
= 90 ns + 10 ns
= 100 ns
Part-02: Non-Pipeline Execution Time-
Non-pipeline execution time for one instruction
= 60 ns + 50 ns + 90 ns + 80 ns
= 280 ns
Part-03: Speed Up Ratio-
Speed up
= Non-pipeline execution time / Pipeline execution time
= 280 ns / Cycle time
= 280 ns / 100 ns
= 2.8

Q.2) Max Marks: 1

In the MIPS32 pipeline, which of the following scenarios of data dependency will always result in a pipeline stall due to data hazard without any instruction scheduling?

A. **An ADD instruction followed by a SUB instruction**

B. **A STORE instruction followed by a LOAD instruction**

C. **A LOAD instruction followed by an ADD instruction** — Correct Option

Solution: (C)
Answer: C
Explanation:
Only a LOAD followed by an immediate use will result in a mandatory stall in the pipeline

D. **None of the above**

Q.3) Max Marks: 1

A pipeline P operating at 400 MHz has a speedup factor of 6 and operating at 70% efficiency. How many stages are there in the pipeline?

A. 5

B. 6

C. 8

D. 9 — Correct Option

Solution: (D)

Answer: D
Explanation:
Efficiency of K stage Pipeline = SpeedUp Factor (Sk) / Number of Stages (K)
0.70 = 6/K
K = 6/0.70 = 8.57 ≅ 9

Number of Stages = 9

Q.4) Max Marks: 1

Consider the following instructions.
I1 : R1 = 100
I2 : R1 = R2 + R4
I3 : R2 = R4 + 25
I4 : R4 = R1 + R3

I5 : R1 = R1 + 30

Calculate sum of (WAR, RAW and WAW) dependencies the above instructions.

A 9

B 8 — Correct Option

Solution: (B)
RAW Hazards:
2⟶4
2⟶5
WAR Hazards:
2⟶3
2⟶4
3⟶4
4⟶5
WAW Hazards:
1⟶2
2⟶5

C 6

D 14

Q.5) Max Marks: 1

Consider the following assembly language program:
I1: Move R3, R7 /R3 <-- (R7)/
I2: Load R8, (R3) /R8 <-- Memory (R3)/
I3: Add R3, R3, 4 /R3 <-- (R3) + 4/
I4: Load R9, (R3) /R9 <-- Memory (R3)/
I5: BLE R8, R9, L3 /Branch if (R9) > (R8)/
Total number of hazards including WAW, RAW, and WAR dependencies are_____

A 2

B 3

C 4

D None of these — Correct Option

Solution: (D)
True data dependency (RAW): I1 - I2, I1 - I3, I3 - I4, I4 - I5 , I2-I5
Output dependency (WAW): I1 - I3
Antidependency (WAR): I2 - I3

Q.6) Max Marks: 1

Consider the below instructions executed on a 5 stage(IF,ID,EX,MA,WB) RISC pipeline with operand forwarding.
I1: ADD R0,R1,R2 (R0=R1+R2)
I2: SUB R3,R0,R2
I3:MUL R4,R3,R0
I4:DIV R5,R4,R0
How many RAW dependencies?

Correct Answer

Solution: (5)
Answer:5
Explanation:
Ro from 1->2,3,4
R3 from 2->3
R4 from 3 -> 4

Q.7) Max Marks: 1

For an n-stage pipeline implementation of some computation, the maximum speedup that can be obtained is upper bounded by:

A 2n

B n — Correct Option

Solution: (B)
Answer: B
Explanation:
The maximum speedup that can be obtained in a pipeline is upper bounded by the number of stages

C 2^n

D None of the above

Q.8) Max Marks: 1

Pipelining improves performance by:

A decreasing instruction latency

B eliminating data hazards

C exploiting instruction level parallelism — Correct Option

Solution: (C)
Answer: C
Explanation:
Pipelining improves performance by exploiting instruction level parallelism.

D decreasing the cache miss rate

Q.9) Max Marks: 1

A non pipelined system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a dock cycle of 10 ns. Determine the speedup ratio of the pipeline for 100 tasks.

Correct Answer

Solution: (4.76)
Answer:4.76
Explanation:
tn = 50 ns
k = 6
tp = 10 ns
n = 100
Speed up = $nt_n/(k+n-1)t_p$ = 100*50 / (6+100-1)*10 = 5000/1050 = 4.76

Q.10) Max Marks: 1

You are given a non-pipelined processor design which has a cycle time of 10ns and average CPI of 1.4. The speedup you can get by pipelining it into 5 stages.

A No Speedup

B 2

C 5 — Correct Option

Solution: (C)
Answer: C
Explanation:
Since IC and CPI don't change, and, in the best case, pipelining will reduce CT to 2ns
Speedup = CT_{old} /CT_{new} = 10ns/ 2ns = 5x Speedup

D 4

Q.11) Max Marks: 2

Consider an instruction pipeline with five stages without any branch prediction: Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX) and Operand Write(OW). The stage delays for IF, ID, OF, EX and OW are 5 nsec, 7 nsec, 10 nsec, 8 nsec and 6 nsec, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 nsec. A program consisting of 12 instructions I1, I2, ..., I12 is executed in the pipelined processor. Instruction I4 is the only branch instruction and its branch target is I9. If the branch is taken during the execution of this program, the time needed to complete the program is:

A 132 nsec

B 165 nsec — Correct Option

Solution: (B)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
I1	IF	ID	OF	EX	OW										
2		IF	ID	OF	EX	OW									
3			IF	ID	OF	EX	OW								

4				IF	ID	OF	EX	OW							
5				-	-	-	-	-							
6				-	-	-	-	-							
7				-	-	-	-	-							
8				-	-	-	-	-							
9								IF	ID	OF	EX	OW			
10									IF	ID	OF	EX	OW		
11										IF	ID	OF	EX	OW	
12											IF	ID	OF	EX	OW

Total 15 clock cycles are needed.
So, here maximum delay is 10 ns. Buffer delay given is 1ns. So, each stage takes 11 ns in total.
Time required to complete the program is 15*11 = 165 nsec

C 176 nsec

D 328 nsec

Q.12) Max Marks: 2

How long would the following sequence of instructions take to execute on a superscalar processor with two execution units, each of which can execute any instruction? Load operations have a latency of two cycles, and all other operations have a latency of one cycle. Assume that the pipeline depth is 5 stages
LD r1, (r2)
ADD r3, r1, r4
SUB r5, r6, r7
MUL r8, r9, r10

Correct Answer

Solution: (9)

In-order execution
There are five pipeline stages and load has latency of 2 clock cycles
Fetch, Decode, Execution, Memory access and Write back are the pipeline stages
Total number of cycles is 9

	1	2	3	4	5	6	7	8	9
LD	F	D	E	E	M	WB			
ADD	F	D	-	-	-	E	M	WB	
SUB		F	D	-	-	-	E	M	WB
MUL		F	D	-	-	-	E	M	WB

Q.13) Max Marks: 2

Consider the following sequence of instructions, where the syntax consists of an opcode followed by the destination register followed by one or two source registers:
0 ADD R3, R1, R2
1 LOAD R6, [R3]
2 AND R7, R5, 3
3 ADD R1, R6, R7
4 SRL R7, R0, 8
5 OR R2, R4, R7
6 SUB R5, R3, R4
7 ADD R0, R1, 10
8 LOAD R6, [R5]
9 SUB R2, R1, R6
10 AND R3, R7, 15
Assume the use of a four-stage pipeline: fetch, decode/issue, execute, write back. Assume that all pipeline stages take one clock cycle except for the execute stage. For simple integer arithmetic and logical instructions, the execute stage takes one cycle, but for a LOAD from memory, five cycles are consumed in the execute stage.
If we have a simple scalar pipeline, but allow out-of-order execution, we can construct the following table for the execution of the first seven instructions:

Instruction	Fetch	Decode	Execute	Write Back
0	0	1	2	3
1	1	2	4	9
2	2	3	5	6
3	3	4	10	11
4	4	5	6	7
5	5	6	8	10

6	6	7	9	12

then the last instruction I10 completes at the ____ th clock cycle.

Correct Answer

Solution: (15)

Answer:15

Explanation:

The entries under the four pipeline stages indicate the clock cycle at which each instruction begins each phase. In this program, the second ADD instruction (instruction 3) depends on the LOAD instruction (instruction 1) for one of its operands, r6. Because the LOAD instruction takes five clock cycles, and the issue logic encounters the dependent ADD instruction after two clocks, the issue logic must delay the ADD instruction for three clock cycles. With an out-of-order capability, the processor can stall instruction 3 at clock cycle 4, and then move on to issue the following three independent instructions, which enter execution at clocks 6, 8, and 9. The LOAD finishes execution at clock 9, and so the dependent ADD can be launched into execution on clock 10.

Instruction	Fetch	Decode	Execute	Writeback
0 ADD r3, r1, r2	0	1	2	3
1 LOAD r6, [r3]	1	2	4	9
2 AND r7, r5, 3	2	3	5	6
3 ADD r1, r6, r0	3	4	10	11
4 SRL r7, r0, 8	4	5	6	7
5 OR r2, r4, r7	5	6	8	10
6 SUB r5, r3, r4	6	7	9	12
7 ADD r0, r1, 10	7	8	12	13
8 LOAD r6, [r5]	8	9	13	18
9 SUB r2, r1, r6	9	10	19	20
10 AND r3, r7, 15	10	11	14	15

Q.14) Max Marks: 2

A 5 stage pipelined processor has the following stages:
IF : instruction fetch
ID : instruction decode
EX : execute
MA : memory access
WB : write back
IF→ID→EX→MA→WB
Each stage needs one cycle for all instructions.
I1. Load R1,[1000] :R1←M[1000]
I2. Load R3,5(R2) :R3←M[R2+5]
I3. MUL R4,R1,R3 :R4←R1*R3
I4. DIV R5,R1,R4 :R5←R1÷R4
I5. SUB R6,R4,R5 :R6←R4−R5
No. of cycles needed to execute these instructions using operand forwarding is
_____

Correct Answer

Solution: (10)

	1	2	3	4	5	6	7	8	9	10	11
I1	IF	ID	EX	MA	WB						
I2		IF	ID	EX	MA	WB					
I3			IF	ID		EX	MA	WB			
I4				IF		ID	EX	MA	WB		
I5					IF		ID	EX	MA	WB	

Q.15) Max Marks: 2

The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage is replaced with a functionally equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput of the pipeline increases by ..... percent.

A **33.3%** Correct Option

Solution: (A)
Answer A:
Explanation: 33.3%.
Pipeline 1: To process n data, time = 3 + 800n
Throughput = 1/800 (approx.)
Pipeline 2: To process n data, time = 4 + 600n
Throughput = 1/600 (approx..)
% improvement = (1/600 – 1/800) / (1/800) * 100 = 33.3

B **30%**

C **10%**

D None of these

close