



Kunal Jha  
 Course: GATE  
 Computer Science Engineering(CS)

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## MULTIPLE SUBJECT : COMPUTER ORGANIZATION AND ARCHITECTURE + OPERATING SYSTEM (GATE - 2020) - REPORTS

OVERALL ANALYSIS    COMPARISON REPORT    **SOLUTION REPORT**

ALL(33)    CORRECT(0)    INCORRECT(0)    SKIPPED(33)

Q. 1

Solution Video

Have any Doubt ?



Consider the following  $\mu$ -program:

$$I_1 : MAR \leftarrow IR[Addr]$$

$$I_2 : MBR \leftarrow M[MAR]$$

$$I_3 : ALU \leftarrow MBR$$

Which of the following operation is performed by above  $\mu$ -program?

A Instruction fetch

B Direct operand fetch

Correct Option

Solution :

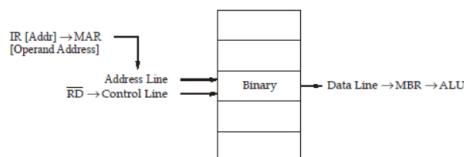
(b)

In  $T_1$  cycle content register goes to MAR i.e. address which contain actual data.

In  $T_2$  cycle content of MAR i.e. actual data transferred to MBR.

In  $T_3$  cycle content of MBR transferred ALU after the execution start.

So this  $\mu$ -program represent direct operand fetch which is shown by below diagram.



C Interrupt sub program initiation

D Indirect operand fetch

QUESTION ANALYTICS



Q. 2

Solution Video

Have any Doubt ?



Consider the following statements:

$S_1$  : Two user level threads implemented in the user space in the same process can not be synchronized using a semaphore.

$S_2$  : When a context switch occurs between two threads of the same process then only program counter will be changed and no other attribute changed.

Which of the above statements is/are correct?

A  $S_1$  only

Correct Option

Solution :

(a)

$S_1$  : User level threads, when one thread blocks on a semaphore, the Kernel thinks the entire process is blocked and does not run it again.

$S_2$  : When a context switch occurs then program counter and stack pointer also will be changed.

B  $S_2$  only

C Both  $S_1$  and  $S_2$

D Neither  $S_1$  nor  $S_2$

QUESTION ANALYTICS



Q. 3

Solution Video

Have any Doubt ?



Consider the following instruction used implement addition operation i.e.  $C \leftarrow [A] + [B]$ :

(i) Add A, B  $[A] + [B] \rightarrow B \equiv \text{MOV } B, C$   $[B] \rightarrow C$ , Add A, C  $[A] + [C] \rightarrow C$

(ii) Add A, B, C  $[A] + [B] \rightarrow C \equiv \text{MOV } A, C$   $[A] \rightarrow C$ , Add B, C  $[B] + [C] \rightarrow C$

In which of the following option, result of RHS execution is same as execution of LHS?

A Only (i)

B Only (ii)

Correct Option

Solution :

(b)

(i) Add A, B  
 $[A] + [B] \rightarrow B$

$\text{MOV } B, C$   
 $[B] \rightarrow C$ ,  $[A] + [C] \rightarrow C$

$\equiv$

Here old content of location B is lost.

- (ii) Add A, B, C  
[A] + [B] → C  
Old content of A, B, is not lost.

Here old content of B and A are preserved.

MOV B, C Add B, C  
[A] → C, [B] + [C] → C  
Here also old content of A, B are preserved.

C Both (i) and (ii)

D Neither (i) nor (ii)

QUESTION ANALYTICS

Q. 4

Solution Video

Have any Doubt?

Which of the following is correct about Multilevel Queue (MLQ) scheduling and Multilevel Feedback Queue (MLFBQ) scheduling?

A MLQ only suffer from starvation.

B MLQ and MLFBQ both suffer from starvation.

Correct Option

Solution :

(b)  
Option (b) is correct.

C MLFBQ only suffer from starvation.

D None of these

QUESTION ANALYTICS

Q. 5

Solution Video

Have any Doubt?

Consider a machine with a byte addressable main memory of 256 MB, block size of 128 bytes and 8-way set associative cache of size 64 kB. If the address of one of the memory location AB01C23H accessed by the CPU. What are the tag field of the corresponding cache line is

A 10101011000000

Correct Option

Solution :

(a)

$$\text{Cache size} = 64 \text{ kB} = 2^{16}$$

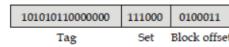
$$\text{Block size} = \text{Cache line size} = 128 \text{ bytes} = 2^7$$

$$\text{Number of cache lines} = \frac{2^{16}}{2^7} = 2^9$$

$$\text{Number of sets} = \frac{2^9}{2^3} = 2^6 = 64$$



Memory location : A B 0 1 C 2 3



B 101110100000

C 101010110000

D 101101010100000

QUESTION ANALYTICS

Q. 6

Solution Video

Have any Doubt?

Which of the following is true?

A While context switching from process A to process B, operating system does not change the address translation table.

B An ISR is invoked on completion of I/O in asynchronous I/O but not in synchronous I/O.

C There is no problem to use single level page table even if it is large size.

D None of these

Correct Option

Solution :

(d)

Address translation table need to be changed when switching context from process A to process B.  
In both synchronous and asynchronous I/O an ISR is involved after completion of the I/O.  
There is overhead to maintain a large page table so not suitable.

### QUESTION ANALYTICS

Q. 7

Solution Video

Have any Doubt ?



Consider the following code:

```
Program concurrency;
var a : integer (: = 0);           /*int a initialized to 0*/
    b : integer (: = 0);           /*int b initialized to 0*/
procedure thread P();
begin
    a = 1;                      /*statement 1*/
    b = b + a;                  /*statement 2*/
end;
procedure thread Q();
begin
    b = 4;                      /*statement 3*/
    a = a + 5;                  /*statement 4*/
end;
begin (*main program*)
    par begin
        thread P();
        thread Q();
    par end
end.
```

Suppose a process has 2 concurrent threads; one thread executes statement 1 and 2 and other thread executes statement 3 and 4. What are the possible values of variable 'a' and 'b' when the code finishes execution ?

**A**  $a = \{6, 1\}$   
 $b = \{10, 4, 5\}$

Correct Option

Solution :

(a) For variable 'a':

- I.  $a = 1$   
 $a = 1 + 5 = 6$
- II.  $a = 0 + 5 = 5$   
 $a = 1$

Hence possible value are {1, 6}.

For variable 'b':

- I.  $b = 0 + 1 = 1$   
 $b = 4$
- II.  $b = 4$   
 $b = 4 + 1 = 5$
- III.  $b = 4$   
 $b = 4 + 6 = 10$

Hence possible value are {4, 5, 10}.

**B**  $a = \{1, 5, 6\}$   
 $b = \{1, 4, 5, 10\}$

**C**  $a = \{5, 6\}$   
 $b = \{10, 4, 5\}$

**D**  $a = \{6, 1\}$   
 $b = \{1, 4, 5, 10\}$

### QUESTION ANALYTICS

Q. 8

Solution Video

Have any Doubt ?



Consider the two processors  $P_1$  and  $P_2$  with intermediate register gateway is 0.

$P_1$ : Has four stage pipeline with stage latency 1.5 nsec, 2 nsec, 1 nsec and 0.5 nsec.

$P_2$ : Has five stage pipeline with stage latency 1 nsec, 2.5 nsec, 1.5 nsec, 2 nsec and 1 nsec.

If each processor has infinite number of instruction to execute, then which of the following is true?

**A** Processor 2 slower than processor 1

Correct Option

Solution :

(a) For  $P_1$ :

$$\text{Pipeline time} = \max(1.5, 2, 1 \text{ and } 0.5) \text{ nsec} = 2 \text{ nsec}$$

$$\text{Clock rate} = \frac{1}{2 \text{ nsec}} = 500 \text{ MHz}$$

For  $P_2$ :

$$\text{Pipeline time} = \max(1, 2.5, 1.5, 2 \text{ and } 1) \text{ nsec} = 2.5 \text{ nsec}$$

$$\text{Clock rate} = \frac{1}{2.5 \text{ nsec}} = 400 \text{ MHz}$$

So, processor-1 faster than processor-2.

**B** Both processor have same clock rate

C Processor 1 slower than processor 2

D None of the above

QUESTION ANALYTICS



Q. 9

Solution Video

Have any Doubt?



Assume that there are 4 page frames which are initially empty, if the page reference string 1, 2, 3, 2, 1, 4, 5, 2, 3, 1, 2 then the number of page fault using the least recently used policy \_\_\_\_\_.

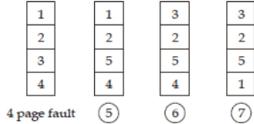
7

Correct Option

Solution :

7

String 1, 2, 3, 2, 1, 4, 5, 2, 3, 1, 2



Total 7 page faults.

QUESTION ANALYTICS



Q. 10

Solution Video

Have any Doubt?



Consider the following process table with Arrival time and Burst time (All time in ms).

Process	Arrival Time	Burst Time
P <sub>1</sub>	1	2
P <sub>2</sub>	6	4
P <sub>3</sub>	4	10
P <sub>4</sub>	5	6

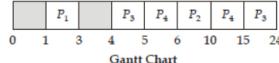
Average waiting time of these processes by using SRTF scheduling is \_\_\_\_\_ (ms). (Upto 1 decimal place)

3.50 [3.49 - 3.52]

Correct Option

Solution :

3.50 [3.49 - 3.52]



Process	Waiting Time
P <sub>1</sub>	0
P <sub>2</sub>	0
P <sub>3</sub>	10
P <sub>4</sub>	4

$$\text{Average Waiting Time} = \frac{0+0+10+4}{4} = \frac{14}{4} = 3.5$$

QUESTION ANALYTICS



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Q. 11

Solution Video

Have any Doubt ?



The access time of cache memory is 45 nsec and that of main memory is 750 nsec. It is found that 75% of memory requests are for read and remaining for write. If the hit access for read and write is 0.9 and 1 respectively and write through protocol is used, then the average memory access time is \_\_\_\_\_. (in nsec) (Upto 3 decimal places)

274.125 [274.122 - 274.127]

Correct Option

**Solution :**

$$\begin{aligned} 274.125 [274.122 - 274.127] \\ T_{\text{avg. read}} &= 0.90 \times 45 + 0.10 \times 750 \\ &= 40.5 + 75 = 115.5 \text{ nsec} \end{aligned}$$

In write-through technique, CPU performs simultaneous WRITE operation in both cache memory and main memory. So,

$$\begin{aligned} T_{\text{avg. write}} &= \text{Max}[T_{\text{updation}}(\text{cache}), T_{\text{updation}}(\text{main memory})] \\ &= \text{Max}[45, 750] = 750 \text{ nsec} \\ \text{So} \quad T_{\text{avg.}} &= 0.75 (115.5) + 0.25 (750) \\ &= 86.625 + 187.5 = 274.125 \text{ nsec} \end{aligned}$$

QUESTION ANALYTICS



Q. 12

Solution Video

Have any Doubt ?



Consider the computer system with 32 bits virtual addressing and page size 16 KB, if the computer has one level page table and each page table entry requires 24 bits, size of the page table is \_\_\_\_\_. (KB).

768

Correct Option

**Solution :**

768

Number of entries in page table

$$= \frac{2^{32}}{2^{14}} = 2^{18}$$

$$\text{Page table size} = 2^{18} \times 3B \\ = 768 \text{ KB}$$

QUESTION ANALYTICS



Q. 13

Solution Video

Have any Doubt ?



Consider a Direct cache with 64 blocks and block size of 16 bits. The block number where the byte address  $(1440)_{10}$  mapped in the cache is \_\_\_\_\_.  
 \_\_\_\_\_.

16

Correct Option

**Solution :**

16

$$\text{Block number with respect to } (1440)_{10} \text{ cell is } \frac{1440}{2} = 720$$

$$\text{Location in cache memory} = 720 \bmod 64 = 16$$

QUESTION ANALYTICS



Q. 14

Solution Video

Have any Doubt ?



A system has 9 identical resources and n process competing for them. Each process can request atmost 4 resources. Minimum possible value of N which lead to deadlock

3

Correct Option

**Solution :**

3

Resources = 9

Process = N

Requirement = Max = 4

$$[N - 1] \times 3 + 4 = 9$$

$$3N - 3 + 4 = 9$$

$$3N = 8$$

$$N = 2$$

If value of N = 2 then there is no deadlock.

So minimum value of N is 3 which lead to deadlock.

## QUESTION ANALYTICS



Q. 15

▶ Solution Video

Have any Doubt ?



A DMA is transferring characters to processor from a device transmitting at 8000 bits per sec. Assume DMA using cycle stealing mode. If processor needs access to main memory once every micro second. The percentage processor be slow down due to DMA activity is \_\_\_\_\_ (in %). (Upto 1 decimal places)

0.1 [0.0 - 0.2]

Correct Option

**Solution :**

0.1 [0.0 - 0.2]

8000 bits transmitting = 1 seconds

$$\begin{aligned} \text{1 character takes} &= \frac{8}{8000} \text{ second} = 1 \text{ msec} \\ &= 1000 \mu\text{sec} \end{aligned}$$

Processor access main memory in every  $\mu\text{sec}$ .

$$\begin{aligned} \text{Slow \%} &= \frac{y}{x+y} \times 100 \\ x &= 1000 \mu\text{sec} \text{ and } y = 1 \mu\text{sec} \end{aligned}$$

$$\text{So, slow \%} = \frac{1 \mu\text{sec}}{(1000+1) \mu\text{sec}} \times 100 = 0.1$$

## QUESTION ANALYTICS



Q. 16

▶ Solution Video

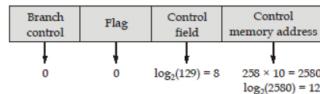
Have any Doubt ?



Consider a CPU where all the instruction require 10 clock cycles to complete execution. There are 258 instructions in instruction set. It is found that 129 control signals are needed to be generated by control unit. While designing the vertical  $\mu$ -programmed control unit, single address field format is used for branch control logic. The size of control memory in byte is \_\_\_\_\_.

6450

Correct Option

**Solution :**  
6450

So, control memory size = 2580 Control words

$$= 2580 = 20 \text{ bits}$$

$$\text{Size in bytes} = \frac{2580 \times 20 \text{ bits}}{8} = 6450$$

## QUESTION ANALYTICS



Q. 17

▶ Solution Video

Have any Doubt ?



Consider a queue between two process below. N is the length of queue and  $q, f, r$  are semaphore.  $q = N, f = 0, r = 1$

**Process 1:**

While (1)

 $p(q)$  $p(r)$ 

enqueue

 $V(r)$  $V(f)$ **Process 2:**

While (1)

 $p(f)$  $p(r)$ 

dequeue

 $V(r)$  $V(q)$ 

Which of the following is true about the above scenario?

- The purpose of semaphore  $r$  is to provide mutual exclusion for queue operation.
- The purpose of semaphore  $q$  is to ensure that deadlock does not occur.
- The purpose of semaphore  $f$  is to ensure that dequeue is not executed on an empty queue.

 A I and II only B I and III only

Correct Option

**Solution :**

(b)

The purpose of semaphore  $f$  is to ensure that dequeue is not executed on an empty queue. Process 2 will block on first statement  $p(f)$ .

The purpose of semaphore  $r$  is to ensure mutual exclusion for queue operations.The purpose of semaphore ' $q$ ' is to keep track of number of enqueue operations possible. C I only D III only

Q. 18

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider the following statements:

- I. Waiting time can be large if short requests are waiting behind the long requests in FCFS.
  - II. It is not necessary to have loader every time in main memory.
  - III. Deadlock avoidance has less restrictions than deadlock prevention.
- Which of the above statements is/are true?

 A I and II only B I only C I and III only

Correct Option

**Solution :**

- (c)
- I. Waiting time will be large if short requests are behind the long requests.
  - II. Loader must be in main memory every time.
  - III. Under deadlock avoidance, the safe state need to be checked and hence less restrictions.

 D III only

Q. 19

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider the floating point Arithmetic for single precision, match the following pairs if E' = Biased exponent and M = Mantissa:

**List-1**

- |                         |                         |
|-------------------------|-------------------------|
| P. E' = 0, M = 0        | (i) $\pm \infty$        |
| Q. E' = 0, M $\neq$ 0   | (ii) $\pm 0$            |
| R. E' = 255, M = 0      | (iii) Denormal numbers  |
| S. E' = 255, M $\neq$ 0 | (iv) Not a number (NaN) |

Which of the following is the correct match between the List-1 and List-2?

P    Q    R    S

- (a) (ii) (iii) (iv) (i)
- (b) (ii) (iv) (i) (iii)
- (c) (ii) (iii) (i) (iv)
- (d) (ii) (iv) (iii) (i)

 A a B b C c

Correct Option

**Solution :**

- (c)

 D d

Q. 20

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider a micro program control unit and list of corresponding properties in control unit design:

**Micro program control unit**

- P. Horizontal  $\mu$  Control unit  
Q. Vertical  $\mu$  Control unit

**Properties**

- (i) Control signals are in decoded binary format
- (ii) Control signals are in encoded binary format
- (iii) Shorter Control Word
- (iv) Longer Control Word
- (v) Low degree of parallelism
- (vi) High degree of parallelism

Which of the following is the correct match between the Micro program control unit and their properties?

 A (P-1, 4, 6) and (Q-2, 3, 5)

Correct Option

**Solution :**

- (a)

- In Horizontal  $\mu$  Control unit design Control signals are in decoded binary format, Longer Control Word and High degree of parallelism.
- In Vertical  $\mu$  Control unit design Control signals are in encoded binary format, Shorter Control Word and Low degree of parallelism.

 B (P-1, 4, 5) and (Q-2, 3, 6) C (P-2, 4, 6) and (Q-1, 3, 5) D (P-2, 3, 6) and (Q-1, 4, 5)





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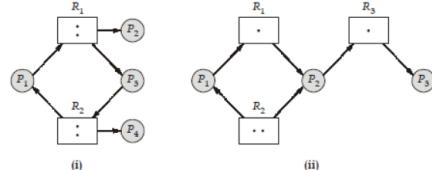
Q. 21

Solution Video

Have any Doubt ?



Consider the following resource allocation graph.



Which of the following is true about given resource allocation graph?

- A** Deadlock occur in both (i) and (ii).
- B** Deadlock occurs in (i) but not in (ii).
- C** Deadlock occurs in (i) but not in (ii).
- D** None of the above

Correct Option

Solution :

(d)

There is no deadlock in (i), processes will be executed in  $P_2, P_4, P_3, P_1$  or some other order also.  
 There is no deadlock in (ii) processes will be executed in order  $P_3, P_2$  and  $P_1$ .

QUESTION ANALYTICS



Q. 22

Solution Video

Have any Doubt ?



Suppose a CPU contains 1000 memory references there are 40 misses in  $L_1$  cache (First Level Cache) and 20 misses in the  $L_2$  cache (Second Level Cache). Assume miss penalty from the  $L_2$  cache to memory is 100 clock cycles the hit time of  $L_2$  cache is 10 clock cycles, the hit time of  $L_1$  cache is 1 clock cycle. What is the average memory access time?

- A** 3.4 clock cycles

Correct Option

Solution :

(a)

Average Memory Access time

$$\begin{aligned}
 &= \text{Hit Time } L_1 + \text{Miss rate } L_1 \times (\text{Hit time } L_2 + \text{Miss rate } L_2 \times \text{Miss} \\
 &\text{Penalty } L_2) \\
 &= 1 + 4\% (10 + 50\% \times 100) \left[ \text{Miss rate } L_1 = \frac{40}{1000} \times 100 = 4\% \right] \\
 &= 1 + 4\% \times 60 \left[ \text{Miss rate } L_2 = \frac{20}{40} \times 100 = 50\% \right] \\
 &= 3.4 \text{ clock cycles}
 \end{aligned}$$

Alternate

$$\begin{aligned}
 T_{avg} &= \text{Hit time}_{L_1} + (\text{Miss rate}_{L_1} * \text{Miss penalty}_{L_1}) \\
 \text{Miss penalty}_{L_1} &= \text{Hit time}_{L_2} + (\text{Miss rate}_{L_2} * \text{Miss penalty}_{L_2}) \\
 &= 10 \text{ cycles} + 50 \text{ cycles} = 60 \text{ cycles} \\
 T_{avg} &= \left( 1 + \left( \frac{40}{1000} \times 60 \right) \right) = 3.4 \text{ cycles}
 \end{aligned}$$

- B** 3.5 clock cycles

- C** 5.3 clock cycles

- D** 1.8 clock cycles

QUESTION ANALYTICS



Q. 23

Solution Video

Have any Doubt ?



Consider the following producer and consumer code:

```

#define N = 100
int mutex = 1;           // Binary semaphore variable
int empty = N;           // Counting semaphore variable
int full = 0;             // counting semaphore variable
Void producer ()          Void consumer ()
    
```

```

    int item;
    while (1)
    {
        item = producer-item ();
        down (empty);
        down (mutex);
        insert-item (item);
        up (mutex);
        up (full);
    }
}

```

In the above code mutex, empty and full are semaphore shared variables and item is local to the both producer and consumer. Insert\_item (item) function will place "item" into buffer and consume\_item function removes an item from the buffer. Consider the following statements:

- S<sub>1</sub>: Above solution satisfied mutual exclusion.
- S<sub>2</sub>: Above solution satisfied progress.
- S<sub>3</sub>: Above solution can have deadlock.

Which of the following statements is true?

A S<sub>1</sub> and S<sub>3</sub> only

Correct Option

Solution :

(a)

Given code correctly implements solve the mutual exclusion but producer and consumer may enter the deadlock. Deadlock may occur if consumer executes first down (mutex) and then down (full), consumer goes to block mode. Now producer executes down (empty) and then down (mutex), producer goes to block mode. Deadlock may occur due to the above executions when buffer is initially empty. Since deadlock is present so progress is not satisfied.

B S<sub>2</sub> and S<sub>3</sub> only

C S<sub>1</sub> only

D All the statement

 QUESTION ANALYTICS



Q. 24

 Solution Video

 Have any Doubt ?



Consider 4 stage instruction pipeline executed on a system:

	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>
I <sub>1</sub>	1	3	1	1
I <sub>2</sub>	2	1	2	1
I <sub>3</sub>	1	2	1	2
I <sub>4</sub>	2	1	2	1

If all instructions are executed only once, what is the throughput of system?

A 4/9 cycles

B 4/10 cycles

C 4/12 cycles

D 4/11 cycles

Correct Option

Solution :

(d)

	c <sub>1</sub>	c <sub>2</sub>	c <sub>3</sub>	c <sub>4</sub>	c <sub>5</sub>	c <sub>6</sub>	c <sub>7</sub>	c <sub>8</sub>	c <sub>9</sub>	c <sub>10</sub>	c <sub>11</sub>
S <sub>4</sub>					I <sub>1</sub>		I <sub>2</sub>	I <sub>3</sub>	I <sub>3</sub>	I <sub>4</sub>	
S <sub>3</sub>					I <sub>1</sub>	I <sub>2</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>4</sub>		I <sub>4</sub>
S <sub>2</sub>		I <sub>1</sub>	I <sub>1</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>3</sub>	I <sub>3</sub>	I <sub>4</sub>			
S <sub>1</sub>	I <sub>1</sub>	I <sub>2</sub>	I <sub>2</sub>		I <sub>3</sub>	I <sub>4</sub>	I <sub>4</sub>				

$$\text{Throughput} = \frac{\text{Number of task completed}}{\text{Total time taken to process the tasks}}$$

$$= 4/11 \text{ cycles}$$

 QUESTION ANALYTICS



Q. 25

 Solution Video

 Have any Doubt ?



Suppose that a 4-way set associative cache has 2048 cache lines and main memory of size  $2^{25}$  bytes. Both cache and main memory are partitioned into 64 words block, where word size is 1 byte. Which of the following represents the size of tag memory (bytes) \_\_\_\_\_.

2560

Correct Option

Solution :

2560

Number of cache lines = 2048 =  $2^{11}$

$$\text{Number of sets} = \frac{2^{11}}{2^2} = 2^9 \text{ (9 bits required)}$$

Block size = Cache line size =  $2^6$  (6 bits required)

So,

10	Set (9)	Block offset (6)
----	---------	------------------

25 bits

$$\begin{aligned}
 \text{Tag bits} &= 10 \\
 \text{Tag memory size} &= \text{Number of tag bits} \times \text{Number of set} \times \text{Number of cache line in each set} \\
 &= 10 \times 2^9 \times 2^2 \\
 &= 10 \times 2^{11} \text{ bits} \\
 &= \frac{20480}{8} \text{ bytes} = 2560 \text{ bytes}
 \end{aligned}$$

### QUESTION ANALYTICS

Q. 26

Solution Video

Have any Doubt ?



In a paged memory, the page hit ratio is 0.45. The time required to access a page in secondary memory is 160 ns and to access main memory is 15 ns, the average time required to access a page is \_\_\_\_\_ (ns). (Upto 2 decimal places)

94.75 [94.74 - 94.76]

Correct Option

**Solution :**  
94.75 [94.74 - 94.76]

Hit ratio,  $h = 0.45$

Main Memory Access Time ( $t_m$ ) = 15 ns

Secondary Memory Success Time ( $t_s$ ) = 160 ns

$$\begin{aligned}
 \text{Average Access Time} &= h \times t_m + (1 - h) t_s \\
 &= 0.45 \times 15 + 0.55 \times 160 \\
 &= 6.75 + 88 = 94.75 \text{ ns}
 \end{aligned}$$

### QUESTION ANALYTICS

Q. 27

Solution Video

Have any Doubt ?



A CPU has 24 bit instructions and we have to calculate the sum of n number by using below code:

MOV N, R <sub>1</sub>
Clear R <sub>0</sub> , R <sub>2</sub>
Loop: R <sub>0</sub> ← [R <sub>0</sub> ] + R <sub>2</sub> [PC]
Dec R <sub>1</sub>
R <sub>2</sub> = [R <sub>2</sub> ] + 1;
Branch > 0, X [PC]
MOV R <sub>0</sub> SUM

The value of X, if target address of branch is loop, when instruction is uses PC relative addressing mode is \_\_\_\_\_. (Assume memory is byte addressable)

-12

Correct Option

**Solution :**  
-12

Each instruction of 24 bits =  $\frac{24}{8} = 3 \text{ B}$

So, loop:  $\leftarrow [R_0] + R_2[\text{PC}] \quad i$

Dec R<sub>1</sub>  $i + 3\text{B}$

R<sub>2</sub>  $\leftarrow [R_2] + 1 \quad i + 6\text{B}$

Branch > 0, offset  $i + 9\text{B}$

At this time, PC =  $[i + 12\text{B}]$

Offset = X, such that PC + X = i

$$\begin{aligned}
 \Rightarrow [i + 12] + X &= i \\
 X &= [-12]
 \end{aligned}$$

### QUESTION ANALYTICS

Q. 28

Solution Video

Have any Doubt ?



Consider the following table:

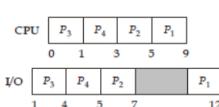
Process ID	CPU Burst Time	I/O Service Time
P <sub>1</sub>	4	3
P <sub>2</sub>	2	2
P <sub>3</sub>	1	3
P <sub>4</sub>	2	1

Assume all process arrived at same time. Every process completes its CPU request then get I/O service. If any two process need same amount of CPU time then prefer the process which has less amount of I/O service request. Process are scheduled using SJF for CPU service and I/O scheduling is done using FCFS scheduling, the time at which process P<sub>1</sub> completes both CPU and I/O requests is \_\_\_\_\_.

12

Correct Option

**Solution :**  
12



At time unit 12 process P<sub>1</sub> complete its CPU and I/O service time.

Q. 29

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider a 2-way set associative cache with 8 cache blocks. If the memory block requests are accessed 2 time in the following order 0, 4, 8, 4, 0, 4, 8, 4, 3, 15, 19, 15, 3, 15, 19, 15. If LRU replacement policy is used, then the total number of misses are \_\_\_\_\_.

18

Correct Option

Solution :

18

$$\text{Number of sets} = \frac{\text{Number of blocks}}{2} = \frac{8}{2} = 4$$

0	∅	∅	∅	8	4
1					
2					
3	∅	∅	∅	19	15

0	∅	∅	∅	8	4
1					
2					
3	∅	∅	∅	19	15

1st access  
[Initially all sets are empty]  
Number of miss = 10

2nd access  
[Initially set 1 contains 8, 4 and  
set 3 contains 19, 15]  
Number of miss = 8

So, total number of misses are = 10 + 8 = 18

Q. 30

[▶ Solution Video](#)[Have any Doubt ?](#)

Consider a pipeline processor with 5 stages, Instruction Fetch (IF), Instruction Decode and Operand Fetch (ID), Operation performed (OP), Data memory access (MA) and Write back (WB). The IF, ID, MA and WB stages takes 1 clock cycle each for any instruction. The OP stage takes 1 clock cycle for ADD and SUB instructions and takes 3 clock cycles for MUL instruction. The minimum number of clock cycles are needed to complete following sequence of instruction if operand forwarding is used \_\_\_\_\_.

Instruction                      Meaning of Instruction

- |                             |                                 |
|-----------------------------|---------------------------------|
| $I_0$ : ADD $R_2, R_0, R_1$ | $R_2 \leftarrow R_0 + R_1$      |
| $I_1$ : SUB $R_1, R_2, R_1$ | $R_1 \leftarrow R_2 - R_1$      |
| $I_2$ : MUL $R_2, R_1, R_0$ | $R_2 \leftarrow R_1 \times R_0$ |
| $I_3$ : SUB $R_0, R_2, R_0$ | $R_0 \leftarrow R_2 - R_0$      |
| $I_4$ : ADD $R_3, R_1, R_0$ | $R_3 \leftarrow R_1 + R_0$      |

11

Correct Option

Solution :

11

Clock cycles	Instruction (operation)										
	1		SUB								
	1		ADD								
$I_0$	IF	ID	OP	MA	WB						
$I_1$		IF	ID	OP	MA	WB					
$I_2$			IF	ID	OP	OP	OP	MA	WB		
$I_3$				IF	ID		OP	MA	WB		
$I_4$					IF		ID	OP	MA	WB	

Total number of clock cycles needed for given program is 11.



Kunal Jha

Course: GATE  
Computer Science Engineering(CS)

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## MULTIPLE SUBJECT : COMPUTER ORGANIZATION AND ARCHITECTURE + OPERATING SYSTEM (GATE - 2020) - REPORTS

OVERALL ANALYSIS

COMPARISON REPORT

SOLUTION REPORT

ALL(33)

CORRECT(0)

INCORRECT(0)

SKIPPED(33)

Q. 31

Solution Video

Have any Doubt ?



Consider a disk system where 1 GB disk rotates at 5000 rpm, the data is transferred at a rate of  $10^7$  bps, the average seek time is 10 ms where the block size is 64 Kb, the average service time required to retrieve a single disk block from a random location on the disk is \_\_\_\_\_ (ms). (Upto 2 decimal places)

22.55 [22.53 - 22.57]

Correct Option

**Solution :**

22.55 [22.53 - 22.57]

Seek time ( $T_{\text{seek}}$ ) = 10 ms

$$T_{\text{rotational}} = \frac{1}{2} \text{ rotational latency}$$

$$= \frac{1}{2} \times \frac{60}{5000} = 6 \text{ ms}$$

$$T_{\text{transfer}} = \frac{64 \times 1024}{10^7} = 6.55 \text{ ms}$$

$$T_{\text{service}} = 10 + 6 + 6.55 = 22.55 \text{ ms}$$

QUESTION ANALYTICS



Q. 32

Solution Video

Have any Doubt ?



A computer has a cache, main memory, and a disk used for virtual memory. If a referenced word is in the cache, 30 ns are required to access it. If it is in main memory but not in cache, 80 ns are needed to load it into the cache, and then the reference is started again. If the word is not in main memory, 22 ms are required to fetch the word from disk, followed by 80 ns to copy it to the cache and the start again. The cache hit ratio is 0.8 and main memory hit ratio is 0.9. The approximate average time ( $\mu\text{s}$ ) required to access a referenced word on this system \_\_\_\_\_ (Upto 2 decimal places)

440.04 [440.00 - 440.10]

Correct Option

**Solution :**

440.04 [440.00 - 440.10]

Location of Reference word	Probability	Total Time
In cache	0.8	30 ns
Not in cache but in main memory	(0.2) (0.9) = 0.18	30 + 80 = 110 ns
Not in cache and not in main memory	(0.2) (0.1) = 0.02	30 + 80 + 22 × 10 <sup>6</sup> ns

$$\therefore \text{Average access time} = 0.8 \times 30 \text{ ns} + 0.18 \times 110 \text{ ns} + (0.02) \times (30 + 80 + 22000000) \text{ ns}$$

$$= 440.046 \mu\text{s} = 440 \mu\text{s}$$

QUESTION ANALYTICS



Q. 33

Solution Video

Have any Doubt ?



Consider a computer system having 30 physical page frames numbered from 1 to 30 which are initially empty, now a program accesses the page 1, 2 ... 150 twice, in same order, the difference in the number of page faults between LIFO and optimal page replacement policy is \_\_\_\_\_.

1

Correct Option

**Solution :**

1

LIFO initially there is compulsory miss from 1 to 30.

At 31 there is page fault which will be replaced by 30 and so on.

Total miss on first access = 1 to 150 ⇒ 150

On second access = 30 to 150

Total = 150 + 121 = 271

Optimal page replacement policy

Total miss on first access = 1 to 150 = 150

On second access = 30 to 149 = 120

Total = 270

Difference = 271 - 270 = 1

QUESTION ANALYTICS

