



Kunal Jha

 Course: GATE
 Computer Science Engineering(CS)

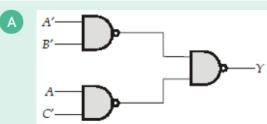
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DIGITAL LOGIC-1: (GATE - 2021) - REPORTS

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Q. 1

Consider the min-term expression $Y(A, B, C, D) = \Sigma_m(0, 1, 2, 3, 8, 9, 12, 13)$. Which among the following options represent the circuit of the simplified versions of Y?

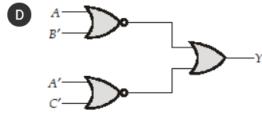
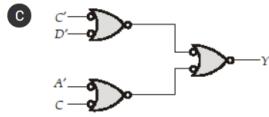
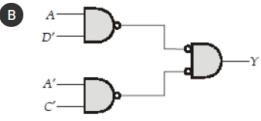

[Correct Option](#)
Solution :
(a)

$$Y(A, B, C, D) = \Sigma_m(0, 1, 2, 3, 8, 9, 12, 13)$$

		CD	00	01	11	10
AB	00	1	1	1	1	$\bar{A}\bar{B}$
		1	1	1	1	$\bar{A}\bar{B}$
01	11	1	1	1	1	$A\bar{C}$
		1	1	1	1	$A\bar{C}$
11	10	1	1	1	1	$A\bar{C}$
		1	1	1	1	$A\bar{C}$

$$Y = \bar{A}\bar{B} + A\bar{C}$$

So, option (a) is correct.


[QUESTION ANALYTICS](#)

Q. 2
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Which of the following statement(s) is/are correct?

- I. Taking OR of min-terms, canonical Sum of Product (SOP) form of Boolean equation can be obtained.
- II. Taking AND of max-terms canonical Product of Sum (POS) form of Boolean equation can be obtained.
- III. 2-level SOP realization considers AND-OR or NAND-NAND while 2-level POS realization considers OR-AND or NOR-NOR realization.
- IV. 2-level SOP realization considers OR-AND or NOR-NOR while 2-level POS realization considers AND-OR or NAND-NAND realization.

A III only

B IV only

C I, II and III

[Correct Option](#)
Solution :

(c)
Statement I, II and III are correct.

D I, II and IV

[QUESTION ANALYTICS](#)

Q. 3
[FAQ](#)
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How many min-terms and Boolean functions can be formed using n -Boolean variables?



A 2^{2n} and 2^n respectively

B 2^n and 2^{2n} respectively

C 2^n and 2^{2n} respectively

Correct Option

Solution :

(c)
Total min-terms with n -variables = 2^n
Total Boolean function n -variables = 2^{2n}

D 2^{2n} and 2^{2n} respectively

QUESTION ANALYTICS

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Q. 4

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⌚ Have any Doubt ?

🔗

Determine the hazard free SOP expression for $f(A, B, C, D) = BD + A'B'C + ACD + B'CD$

A $f(A, B, C, D) = BD + A'B'C + ACD + B'CD$

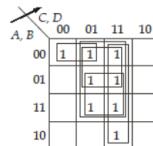
B $f(A, B, C, D) = BD + A'B'C + ACD + B'CD' + A'C'D + AB'C$

C $f(A, B, C, D) = BD + CD + A'D + A'B'C$

Correct Option

Solution :
(c)

$$f(A, B, C, D) = BD + A'B'C + ACD + B'CD \\ (5, 7, 13, 15) \quad (0, 1) \quad (11, 15) \quad (3, 11)$$



$$f(A, B, C, D) = \sum m(0, 1, 3, 5, 7, 11, 13, 15) \\ = BD + CD + A'D + A'B'C$$

D $f(A, B, C, D) = BD + A'B'C + ACD + B'CD' + AB'C$

QUESTION ANALYTICS

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Q. 5

? FAQ

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⌚ Have any Doubt ?

🔗

For an n -variable Boolean logic expression, the minimum and maximum possible number essential prime implicants are

A n and 2^n respectively

B 0 and 2^{n-1} respectively

Correct Option

Solution :
(b)
Minimum number of EPI = 0
Maximum number of EPI = 2^{n-1}

C 1 and $n - 1$ respectively

D $2n$ and 2^n respectively

QUESTION ANALYTICS

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Q. 6

? FAQ

⌚ Have any Doubt ?

🔗

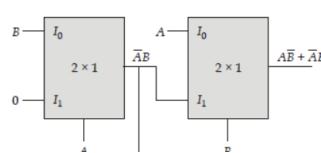
The minimum number of 2×1 MUX required to implement a half-subtraction circuit when only basic inputs 0, 1, A and B are available is _____.

2

Correct Option

Solution :

2



Borrow = $\bar{A}B$

Hence only 2 MUX required.

QUESTION ANALYTICS

Q. 7

FAQ Solution Video Have any Doubt ?

If $(11X1Y)_8 = (12C9)_{16}$, then the value of $X + Y$ is _____.

4

Correct Option

Solution :

4

$$(11X1Y)_8 = (12C9)_{16}$$
$$001001 X \ 001 Y = 0001 \ 0010 \ 1100 \ 1001$$

The binary representation of $(11X1Y)_8$ is $001001 X \ 001 Y$. The digits X and Y are underlined to indicate they are variables.

These are missing in left side. Hence $X = 3$ and $Y = 1$.
So, $X + Y = 3 + 1 = 4$

QUESTION ANALYTICS

Q. 8

FAQ Solution Video Have any Doubt ?

The function $f = (A\bar{B}\bar{C} + \bar{A}B\bar{C} + ABC + \bar{A}\bar{B}C) \oplus A$ can be written as:

A B' XOR C

Correct Option

B B XOR C

Correct Option

C B' XOR C'

Correct Option

D (B XNOR C)'

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - b,c,d

STATUS - SKIPPED

Solution :

(b, c, d)

Option (a)

$$\begin{aligned}f &= (AB' C' + A'BC' + ABC + A'B'C) \text{ XOR } A \\f &= (C' (AB' + A'B) + C (AB + A'B') \text{ XOR } A \\f &= [C' (A \text{ XOR } B) + C (A \odot B)] \text{ XOR } A \\f &= [C' (A \text{ XOR } B) + C (A \text{ XOR } B)'] \text{ XOR } A \\f &= [C \text{ XOR } (A \text{ XOR } B)] \text{ XOR } A \\f &= C \text{ XOR } A \text{ XOR } B \text{ XOR } A \\f &= B \text{ XOR } C \text{ or } B' \text{ XOR } C' \text{ or } (B \text{ XNOR } C)'\end{aligned}$$

QUESTION ANALYTICS

Q. 9

FAQ Solution Video Have any Doubt ?

Consider the following statements about logic gates and select which one is correct

A The AND gate is an electronic circuit that gives a high output (1) only if all of its inputs are high.

Correct Option

B The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high.

Correct Option

C The NOT gate is an electronic circuit that produces an inverted version of the input at its output

Correct Option

D The outputs of all NAND gates are high if any of the inputs are low.

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c,d

STATUS - SKIPPED

Solution :

(a, b, c, d)

All the statements are correct.

QUESTION ANALYTICS

Consider the following statements:

S₁ : 16X1 MUX can be implemented using three 4X1 MUX.

S₂ : Number of prime implicants is same as the number of terms obtained in minimized function of K-map.

Which of the below is correct?

A Only S₁

B Only S₂

C Both S₁ and S₂

D None of the above

Correct Option

Solution :

(d)

- S₁ is incorrect, as mentioned in question would require five 4X1 MUX instead of three.
- S₂ is incorrect, as it is not always the case. For example, the function $f(x, y, z) = \sum_m(2, 4, 5, 6)$ can have different PI when grouped differently in K-map.

 QUESTION ANALYTICS

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Q. 11
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A function $f(x, y, z) = x \odot y \odot z = 1$. Then which one of the following always true?

 A $x + yz = 1$
 B $x = y \oplus z$
 C $x.y.z = 1$
 D $x = y \odot z$

Correct Option

Solution :

(d)

 Let $x = y \odot z$

 So, $x \odot y \odot z$

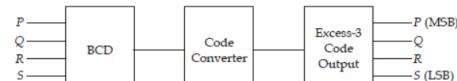
$$\frac{y \odot z}{P} \odot \frac{y \odot z}{P}$$

 and $P \odot P = 1$. So option (d) is correct.

[QUESTION ANALYTICS](#)

Q. 12
[FAQ](#)
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Consider a code converter as shown below that converts BCD to excess-3 code for the decimal digits.



The simplified Boolean function output excess-3 code for P will be

 A $P + QS + QR$

Correct Option

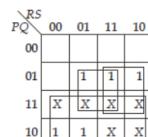
Solution :

(a)

Truth table for BCD to excess-3 code output:

Decimal Value	Input				Output				Decimal Value
	P	Q	R	S	P	Q	R	S	
0	0	0	0	0	0	0	1	1	3
1	0	0	0	1	0	1	0	0	4
2	0	0	1	0	0	1	0	1	5
3	0	0	1	1	0	1	1	0	6
4	0	1	0	0	0	1	1	1	7
5	0	1	0	1	1	0	0	0	8
6	0	1	1	0	1	0	0	1	9
7	0	1	1	1	1	0	1	0	10
8	1	0	0	0	1	0	1	1	11
9	1	0	0	1	1	1	0	0	12

K-map for P: $f(P, Q, R, S) = \sum m(5, 6, 7, 8, 9) + d(10, 11, 12, 13, 14, 15)$



$$= P + QS + QR$$

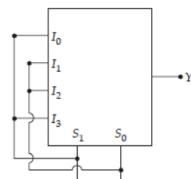
$$= P + Q(S + R)$$

 B $P \oplus Q$
 C $PQ + (R \odot S)$
 D $PQ + (\overline{Q} + \overline{S})$
[QUESTION ANALYTICS](#)


Q. 13

[FAQ](#)
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Consider the below combinational circuit which has 2 inputs A and B and output Y .



If the function $Y = B$, then the select line will be

A $S_0 = \bar{A}, S_1 = \bar{B}$

B $S_0 = B, S_1 = A$

Correct Option

Solution :
(b)

$$\begin{aligned}
 Y &= \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3 \\
 I_0 &= I_3 = S_1 \text{ and } I_1 = I_2 = S_0 \\
 \text{So,} \quad Y &= \bar{S}_1 \bar{S}_0 S_1 + \bar{S}_1 S_0 S_0 + S_1 \bar{S}_0 S_0 + S_1 S_0 S_1 \\
 &= \bar{S}_1 S_0 + S_1 S_0 = S_0
 \end{aligned}$$

So, whenever $S_0 = B$, output (Y) = B
So, option (b) is correct.

C $S_0 = \bar{B}, S_1 = \bar{A}$

D $S_0 = A, S_1 = \bar{B}$

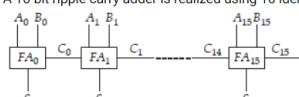
QUESTION ANALYTICS

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Q. 14

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A 16-bit ripple carry adder is realized using 16 identical full adders as shown below:



The carry propagation delay of each FA is 12 ns and sum propagation delay of each FA is 15 ns. The worst case delay (in ns) of this 16-bit adder will be _____.

195

Correct Option

Solution :

$$\begin{aligned}
 &195 \\
 &\text{We consider the last full adder for worst case delay.} \\
 &\text{Time after which output carry bit becomes available from the last full adder.} \\
 &= \text{total number of full address} \times \text{carry propagation delay of full adder.} \\
 &= 16 \times 12 \text{ ns} = 192 \text{ ns} \\
 &\text{Time after which output sum bit becomes available from the last full adder.} \\
 &= \text{time taken for its carry in to become available} + \text{sum propagation delay of full adder.} \\
 &= \{\text{total number of full address before last full adder} \times \text{carry propagation delay of full adder}\} + \\
 &\text{sum propagation delay of full adder.} \\
 &= [15 \times 12 \text{ ns}] + 15 \text{ ns} = 195 \text{ ns}
 \end{aligned}$$

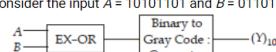
QUESTION ANALYTICS

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Q. 15

[FAQ](#)
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Consider the input $A = 10101101$ and $B = 01101100$ is feeded as input as shown below:



The value of Y is _____.

161

Correct Option

Solution :
161

$$\begin{aligned}
 A \oplus B &= 10101101 \oplus 01101100 = 11000001 \\
 \text{Now convert above binary code to gray code.} \\
 \text{Gray of } (11000001)_2 &\text{ is } (10100001)_2 \\
 (10100001)_2 &= (161)_{10}
 \end{aligned}$$

QUESTION ANALYTICS

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Q. 16

FAQ Solution Video Have any Doubt ?

Which of the following statements is/are correct with respect to K-maps?

A K-map simplification does not demand for the knowledge of boolean algebraic theorems.

Correct Option

B Usually it requires less number of steps when compared to algebraic minimization technique.

Correct Option

C Complexity of k-map simplification process increases with the increase in the number of variables.

Correct Option

D The minimum expression obtained might not be unique.

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c,d

STATUS - SKIPPED

Solution :

(a, b, c, d)
All the statements are correct.

QUESTION ANALYTICS

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Q. 17

FAQ Solution Video Have any Doubt ?

Which of the following is/are termed as minimum error code (Choose all the correct options)

A Binary code

B Gray code

Correct Option

C Excess 3 code

D Octal code

YOUR ANSWER - NA

CORRECT ANSWER - b

STATUS - SKIPPED

Solution :

(b)
Gray codes are less error-prone for mechanical devices that involve making and breaking electrical circuits because they only change in one bit position at a time.
So, they are considered as the minimum error code.

QUESTION ANALYTICS

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OVERALL ANALYSIS COMPARISON REPORT **SOLUTION REPORT**

ALL(17) CORRECT(0) INCORRECT(0) SKIPPED(17)

Q. 1

Solution Video

Have any Doubt?



Which of the following are the characteristic equation of J-K and S-R flip flop?

A $Q_{n+1} = J_n Q'_n + K'_n Q_n$ and $Q_{n+1} = S_n + R'_n Q_2$

Correct Option

Solution:

(a) Characteristic equation for J-K flip flop:

$$Q_{n+1} = J_n Q'_n + K'_n Q_n$$

Characteristic equation for S-R flip flop:

$$Q_{n+1} = S_n + R'_n Q_n$$

B $Q_{n+1} = J_n Q_n + K'_n Q_n$ and $Q_{n+1} = S_n + R'_n Q_2$

C $Q_{n+1} = J_n Q_n + K'_n Q'_n$ and $Q_{n+1} = S_n + R'_n Q_2$

D $Q_{n+1} = J'_n Q'_n + K_n Q_n$ and $Q_{n+1} = S'_n + R'_n Q_2$

QUESTION ANALYTICS



Q. 2

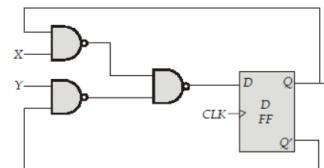
? FAQ

Solution Video

Have any Doubt?



The following circuit functions like:



A S-R flip-flop, $X = S$, $Y = R$

B S-R flip-flop, $X = R$, $Y = S$

C J-K flip-flop, $X = K$, $Y = J$

Correct Option

Solution:

(c)

Normally, characteristic equation for J-K flip flop

$$Q_{n+1} = J_n Q'_n + K'_n Q_n$$

Now here, $D = \overline{XQ_n} \cdot \overline{YQ'_n} = XQ_n + YQ'_n$

where $X = K$ and $Y = J$

So, option (c) is correct.

D J-K flip-flop, $X = J$, $Y = K$

QUESTION ANALYTICS



Q. 3

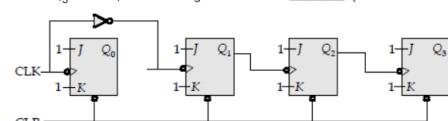
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Solution Video

Have any Doubt?



Given that Q_3 as MSB, the following circuit is a/an _____. (Assume that J-K inputs are 1 for all flip-flop)



A Synchronous binary up counter

B Asynchronous binary up counter

C None of the option is true

Correct Option

Solution :

(c) All the flip-flops are negative edged triggered.

(i) External clock is applied directly to FF0.

(ii) NOT gate output is the clock of FF1.

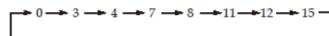
NOT ate input is external clock

Note: For every clock pulse FF0 and FF1 will change. FF0 will change when external clock is changing from 1 to 0 and FF1 will change when external clock is changing from 0 to 1.

(iii) FF1 output Q_1 is clock of FF2.(iv) FF2 output Q_2 is clock of FF3.

Clock	Q_3	Q_2	Q_1	Q_0
1	0	0	1	1
2	0	1	0	0
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	1	1
8	0	0	0	0

The switching sequence of the counter is



So it is not a binary up or down counter.

D Asynchronous binary down counter

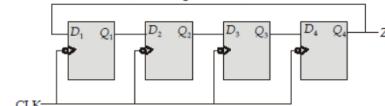
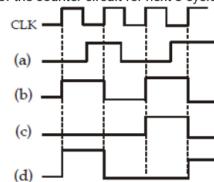
QUESTION ANALYTICS

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Q. 4[FAQ](#)[Solution Video](#)[Have any Doubt ?](#)

□

Consider the counter shown in figure below:

Let the initial state of counter before the clock is applied is $(Q_1 Q_2 Q_3 Q_4) = 1010$. What will be the output waveform of counter circuit at Z. What will be the output waveform of Z of the counter circuit for next 3 cycles?**A** a

Correct Option

Solution :

(a)

Note: Clock is negative edge triggered, so when clock goes from 1 → 0 then output is changes.

CLK	Q_1 $D_1 = Z$	Q_2 $D_2 = Q_1$	Q_3 $D_3 = Q_2$	Q_4 $D_4 = Q_3$	Z
1	0	1	0	1	0
2	1	0	1	0	0
3	0	1	0	1	1

Output Z for next 3 clock cycles = 101.

Hence option (a) is correct wave form for 101.

B b**C** c**D** d

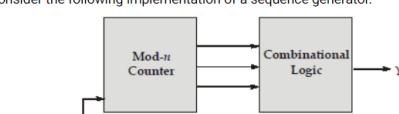
QUESTION ANALYTICS

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Q. 5[FAQ](#)[Solution Video](#)[Have any Doubt ?](#)

□

Consider the following implementation of a sequence generator.



The minimum number of flip-flops needed to generate a sequence of length S is:

A S

B 2^S

C $\log_2 S + 1$

D $\log_2 S$

Correct Option

Solution :

(d)

To generate length S we need $\log_2 S$ flip-flop.

QUESTION ANALYTICS



Q. 6

FAQ

Solution Video

Have any Doubt ?



The clock frequency of 12 MHz is applied to a cascaded counter of modulus-3 counter, modulus-4 counters and modulus-5 counters. The lowest output frequency will be _____ (in KHz).

A 200

Correct Option

Solution :

200

$$\text{Lowest frequency} = \frac{12 \text{ MHz}}{3 \times 4 \times 5} = \frac{12 \times 10^3}{60} \text{ KHz} = 200 \text{ KHz}$$

QUESTION ANALYTICS



Q. 7

FAQ

Solution Video

Have any Doubt ?



Consider the following statements:

- I. Addition of positive and negative number cannot give overflow.
 - II. In BCD addition, if the result is less than or equal to 1001 then further addition of 0110 is correct representation.
 - III. 10's complement subtraction in decimal is similar to 2's complement subtraction in binary.
- The number of correct statements is/are _____.

A 2

Correct Option

Solution :

2

- Statement I and III are correct.
- In BCD addition, when result is greater than 1001 then 0110 is added.

QUESTION ANALYTICS



Q. 8

FAQ

Solution Video

Have any Doubt ?



Which of the following statements is/are correct

A A flip-flop is used to store 1 bit of information only.

Correct Option

B Race around condition occur in JK flip-flop when both of its input are 1.

Correct Option

C Master Slave configuration is used in flip-flop to store two bit of information.

D A transparent latch consist of D-type flip-flop.

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,d

STATUS - SKIPPED

Solution :

(a, b, d)

Flip-flop can store only one bit information.

When both inputs are high in JK flip-flop then output toggles.

No flip-flop can store two bits. Flip-flop can always store one bit.

QUESTION ANALYTICS



Q. 9

Solution Video

Have any Doubt ?



What are the least and largest integers representable in the 10-bit signed 2's complement format (choose both least and largest integers irrespective of the order)?

A -2^9

Correct Option

B $-2^9 - 1$

—

C $-2^9 + 1$

D $2^9 - 1$

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,d

STATUS - SKIPPED

Solution :

(a, d)
Option (a) resembles least integer while option (d) resembles the largest integer.

QUESTION ANALYTICS



Q. 10

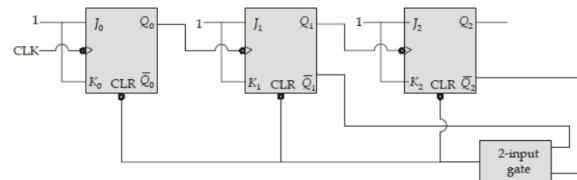
FAQ

Solution Video

Have any Doubt ?



A mod-6 ripple counter is given below. The output of the 2-input gate is used to clear the J-K flipflops.



The 2-input gate is _____.

A AND gate

B OR gate

Correct Option

Solution :
(b)

CLK	Q_0	Q_1	Q_2	$J_0\ K_0$	$J_1\ K_1$	$J_2\ K_2$	$\bar{Q}_1\ \bar{Q}_2$ (2 input gate)
0	0	0	0	1 1	1 1	1 1	1 1
1	1	0	0	1 1	1 1	1 1	1 1
2	0	1	0	1 1	1 1	1 1	0 1
3	1	1	0	1 1	1 1	1 1	0 1
4	0	0	1	1 1	1 1	1 1	1 0
5	1	0	1	1 1	1 1	1 1	1 0
6	0	1	1	1 1	1 1	1 1	0 0

Now if we will use OR gate then the flip flop will be CLR and we will get mod-6 counter from (0 to 5).

C NOR gate

D NAND gate

QUESTION ANALYTICS



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Q. 11
[FAQ](#)
[Solution Video](#)
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Which of the following statements are TRUE?

- I. In fixed point representation, width and position of binary point are defined.
- II. Floating point representation has variable precision.
- III. The floating point representation comprises three parts: Mantissa, Exponent and sign.
- IV. Fixed point arithmetic is similar to integer arithmetic.
- V. In floating point representation gap between numbers is higher for large numbers.

A I and III only

B I, II and III only

C III, IV and V only

D All the above

Correct Option

Solution :

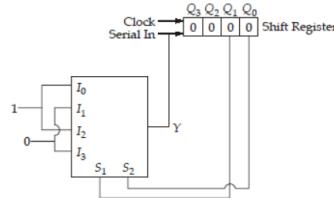
(d)

All the above statements are correct.

QUESTION ANALYTICS


Q. 12
[FAQ](#)
[Solution Video](#)
[Have any Doubt?](#)


Serial IN parallel OUTRIGHT shift register is shown below with the initial content. The number of clock pulses required to get the content of register 0111 is _____.



A 4

Correct Option

Solution :

(a)

4 clock cycles are required.

Note : here s_2 is MSB and s_1 is LSB.

B 5

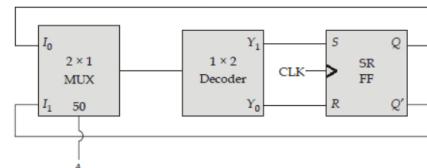
C 6

D 7

QUESTION ANALYTICS


Q. 13
[FAQ](#)
[Solution Video](#)
[Have any Doubt?](#)


Consider the circuit shown in the figure below:



The circuit can work as:

A 4-bit counter

B D flip-flop

C T flip-flop

Correct Option

Solution :

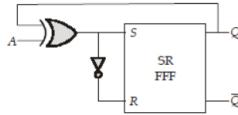
(c)

$$\text{Output of MUX} = \bar{A}Q + A\bar{Q}$$

$$\text{Output of decoder, } S = \bar{A}Q + A\bar{Q}$$

$$R = \bar{A}Q + A\bar{Q}$$

So,



In SRFF

$$\begin{aligned} Q_{n+1} &= S + \bar{R}Q_n \\ &= (A \oplus Q_n) + (\overline{A \oplus Q_n})Q_n \\ &= A \oplus Q_n \end{aligned}$$

So, Q_{n+1} is excitation equation of T-flip flop. Thus, the circuit will function as T-flip flop.**D** SR flip-flop

QUESTION ANALYTICS



Q. 14

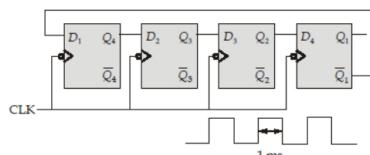
FAQ

Solution Video

Have any Doubt ?



Consider the Johnson counter shown in the figure below. The clock applied to the counter is also shown:



Let the initial state of Johnson counter be 0000. Consider the delay from input to output of each flip-flop is 0.1 ms. After how much time (in ms) the output of the counter will be all zero again _____. (Upto 1 decimal places)

16.1

Correct Option

Solution :

16.1

Johnson counter with n -flip flops has 2^n state.Here, $n = 4$

So total state is = 8

$$\begin{aligned} &= n \times 2 + 0.1 \text{ ms} \\ &= 8 \times 2 + 0.1 = 16.1 \text{ ms} \end{aligned}$$

QUESTION ANALYTICS



Q. 15

FAQ

Solution Video

Have any Doubt ?



Consider the following bit pattern represents the floating point number in IEEE-754 single precision format.

11000101011100000000000000000000

The above represents the decimal value _____. (Upto 2 decimal places)

-3840

Correct Option

Solution :

-3840

Single Precision Format

1-bit	8-bit	23-bit
Sign	Exponent	Mantissa

Sign = 1, so number is negative.

Exponent = 10001010 = 138

Actual exponent = 138 - 127 = 11

[∴ 127 is biased value]

Normalized Mantissa = 111000.....
20 timesActual value = 1.11100.....
20 times

$$\begin{aligned} \text{Decimal value} &= -1.11100 \dots \times 2^{11} = -(111100000000) \\ &= -(2048 + 1024 + 512 + 256) = (-3840)_{10} \end{aligned}$$

QUESTION ANALYTICS



Q. 16

FAQ

Solution Video

Have any Doubt ?



Which of the following statements are correct?

A In 2's complement representation binary zero is having unique representation.

Correct Option

B The range of the numbers in 2's complement representation is more comparing with 1's complement representation. Correct Option

C The range of n-bit number in 1's complement is -2^{n-1} to $(2^{n-1} - 1)$.

D The range of the n-bit number in 2's complement is -2^{n-1} to $(2^{n-1} - 1)$. Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,d

STATUS - SKIPPED

Solution :

(a, b, d)

 QUESTION ANALYTICS



Q. 17

? FAQ Have any Doubt ?



Zero has two representations in:

A Sign magnitude Correct Option

B 1's complement Correct Option

C 2's complement

D Floating point representation. Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,d

STATUS - SKIPPED

Solution :

(a, b, d)

Zero has two representation in sign's magnitude:

1 – MSB is 0

2 – MSB is 1

Both of these representation have equal value that is 0.

Also zero have two representation in 1's compliments:

1 – All bits are Zero.

2 – All bits are 1

IEEE 754 floating point also have 2 representation for zero.

 QUESTION ANALYTICS



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Q. 1
[Solution Video](#)
[Have any Doubt?](#)


The 9's and the 10's complement of 00,000,000 (decimal number) would respectively be:

A 99999999 and 100000000

[Correct Option](#)
Solution :

 (a)
 9's comp: 99999999
 10's comp: 100000000

B 9999999 and 1000000

C 999999999 and 100000000

D 88888888 and 10000000

[QUESTION ANALYTICS](#)

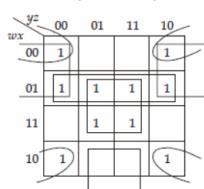
Q. 2
[FAQ](#) [Solution Video](#) [Have any Doubt?](#)

 Which of the following products represent the non essential prime implicants in the given boolean function: $F(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$
A $xz, x'z'$
B $xz, x'z$
C $w'x, w'z'$
[Correct Option](#)
Solution :

 (c)
 Essential: $xz, x'z'$
 Non-essential: $w'x, w'z'$

So,

$$F = xz + x'z' + (w'x \text{ or } w'z')$$


D $w'x, w'z$
[QUESTION ANALYTICS](#)

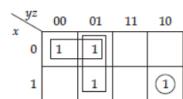
Q. 3
[Solution Video](#) [Have any Doubt?](#)


Consider a circuit with three inputs, x, y, z and three outputs, A, B and C. When the binary input is 0, 1, 2 or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is three less than the input. Then the expression for B is

A $x'y' + y'z + xyz'$
[Correct Option](#)
Solution :

(a)

xyz	A B C
000	010
001	011
010	100
011	101
100	001
101	010
110	011
111	100



$$B = x'y' + y'z + xyz'$$

B $x'z + xz'$

C $x'y + yz$

D z

QUESTION ANALYTICS +

Q. 4

FAQ

Solution Video

Have any Doubt?



A flip-flops has a 3 ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum frequency at which the MOD-1024 ripple counter can operate reliably?

A 33 MHz

B 40 MHz

C 33.3 MHz

Correct Option

Solution :

(c)

The worst case is when all 10 flip-flops are complemented.

The maximum frequency is $\frac{10^9}{30} = 33.3 \text{ MHz}$

D 10 MHz

QUESTION ANALYTICS +

Q. 5

FAQ

Solution Video

Have any Doubt?



Consider a counter with T flip-flops that goes through the following binary repeated sequence: 0, 1, 3, 7, 6, 4. Then which of the following input should we apply to get the consistent MSB:

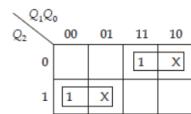
A $Q_2 \oplus Q_1$

Correct Option

Solution :

(a)

Present State			Next State			T_2
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	
0	0	0	0	0	1	0
0	0	1	0	1	1	0
0	1	0	X	X	X	X
0	1	1	1	1	1	1
1	0	0	0	0	0	1
1	0	1	X	X	X	X
1	1	0	1	0	0	0
1	1	1	1	1	0	0



$T_2 = Q_2 \oplus Q_1$

B $Q_2Q_0 + Q'_2 Q'_1 Q'_0$

C $\overline{Q_2 + Q_0}$

D $Q_2 \odot Q_0$

QUESTION ANALYTICS +

Q. 6

FAQ

Solution Video

Have any Doubt?



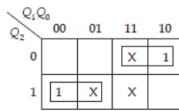
Design a counter with the following repeated binary sequence: 0, 1, 2, 4, 6 using DF's. Then which of the following input should we apply to get the consistent MSB:

A $Q_2 \oplus Q_1$

Correct Option

Solution :
(a)

Present State $Q_2\ Q_1\ Q_0$			Next State $Q_2\ Q_1\ Q_0$			D_2
0	0	0	0	0	1	0
0	0	1	0	1	0	0
0	1	0	1	0	0	1
0	1	1	X	X	X	X
1	0	0	1	1	0	1
1	0	1	X	X	X	X
1	1	0	0	0	0	0
1	1	1	X	X	X	X



$$D_2 = Q_1 \oplus Q_0$$

B $Q_2 Q_0 + Q'_2 Q'_1 Q'_0$

C $\overline{Q_2 + Q_0}$

D $Q_2 \odot Q_0$

QUESTION ANALYTICS



Q. 7

? FAQ

▶ Solution Video

⌚ Have any Doubt ?



Without any additional circuitry, an 8 : 1 MUX can be used to obtain.

A All boolean functions with 3 variables.

B Some functions of 4-variables and all of 3-variables

Correct Option

Solution :

(b)

All functions of 3 variables and some functions of 4 variables can be implemented without any additional circuit and only using 8×1 MUX.

C All functions of 4 variables.

D All functions of 3 variables but none of 4 variables.

QUESTION ANALYTICS



Q. 8

▶ Solution Video

⌚ Have any Doubt ?



The number of comparisons for which $A > B$ is true in 5-bit comparator is _____.

A 250

B 124

C 256

D 496

Correct Option

Solution :

(d)

The simple formula for this is $\frac{(2^{(2n)} - 2^n)}{2}$ and here n is the number of bits comparator and in this case it is 5.

QUESTION ANALYTICS



Q. 9

? FAQ

▶ Solution Video

⌚ Have any Doubt ?



The solutions to the quadratic equation $x^2 - 11x + 22 = 0$ are $x = 3$ and $x = 6$. Then the value of the base could be _____.

8

Correct Option

Solution :

8

$$(x - 3)(x - 6) = x^2 - (6 + 3)x + 6 \times 3 = x^2 - 11x + 22$$

$$\begin{aligned}
 (6+3)_{10} &= (11)_b \\
 9 &= b+1 \\
 b &= 8 \\
 \text{Also, } 6 \times 3 &= (18) \text{ in base 10} = (22) \text{ in base 8.}
 \end{aligned}$$

 QUESTION ANALYTICS

+

Q. 10

? FAQ

▶ Solution Video

⌚ Have any Doubt ?

🔍

Number of literals present in the minimized boolean expression given below:
 $ABC + B'C'D' + BCD + ACD' + A'B'C + ABCD$

9

Correct Option

Solution :

9

	CD	00	01	11	10
AB	00	1		1	1
	01		1	1	
	11			1	1
	10	1		1	1

Minimized expression = $CD + B'D' + AC + A'BD$
 Number of literals is counting number of variables in the expression.
 Thus, $2 + 2 + 2 + 3 = 9$

 QUESTION ANALYTICS

+

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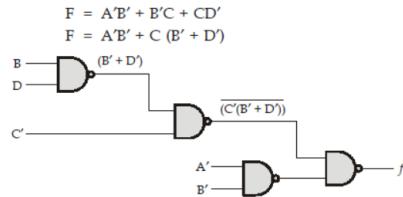
Q. 11

Minimum number of 2-input NAND gates required to implement the complement of the following function: $F(A, B, C, D) = \Sigma(0, 1, 2, 3, 6, 10, 11, 14)$. (Assume complemented forms are available).

4
[Correct Option](#)
Solution :

4

				CD
				1
				1
				1
				1
				1
				1
				1
				1



Therefore we need 4 NAND gates.

[QUESTION ANALYTICS](#)

Q. 12
[FAQ](#)
[Solution Video](#)
[Have any Doubt ?](#)

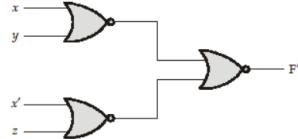

Minimum number of NOR gates required to implement the complement of the following function:
 $F(x, y, z) = [(x + y)(x' + z)]'$. (Assume complemented forms are available).

3
[Correct Option](#)
Solution :

3

$$F = [(x + y)(x' + z)]' = (x + y)' + (x' + z)'$$

$$F' = [(x + y)' + (x' + z)']'$$


[QUESTION ANALYTICS](#)

Q. 13
[Solution Video](#)
[Have any Doubt ?](#)


Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions is _____.

3
[Correct Option](#)
Solution :

3

 Changing (123) base 5 into base 10 = $1 \times 25 + 2 \times 5 + 3 \times 1 = 38$

 Changing x8 base y in decimal = $x \times y + 8$

 Equating both we get $xy + 8 = 38$

 • $xy = 30$

• Possible combinations = (1,30), (2, 15), (3, 10)

• Value of y never less than 8 show (5, 6) is also invalid but we have '8' present in x8 so base y > 8

∴ Total number of solutions 3.

[QUESTION ANALYTICS](#)


Q. 14

[▶ Solution Video](#)[Have any Doubt ?](#)

The state of a 12-bit register is 100010010111. Which of the following is/are true?

A The content of the register is 897 if it represents Three decimal digits in BCD.

Correct Option

B The content of the register is 564 if it represents Three decimal digits in the excess-3 code.

Correct Option

C The content of the register is 871 if it represents Three decimal digits in the 8-4-2-1 code.

D The content of the register is 2,199 if it represents A binary number.

Correct Option

YOUR ANSWER - NA

CORRECT ANSWER - a,b,d

STATUS - SKIPPED

Solution :

(a, b, d)

- Given 1000 1001 0111
For BCD take 4 bits so, content = 897.
- Now, if given bits are excess 3 code.
Then for decimal subtract 3 from each
 $8 - 3 = 5$, $9 - 3 = 6$, $7 - 3 = 4$
So, content of register is 564.
- Option (c) is wrong. Standard BCD code is commonly known as weighted 8421 BCD code.
- If A is binary number $(1000\ 1001\ 0111)_2 = (2199)_{10}$.

QUESTION ANALYTICS



Q. 15

[▶ Solution Video](#)[Have any Doubt ?](#)

Which of the following Boolean expression(s) results in a literal:

A $xy + xy'$

Correct Option

B $(x + y)(x + y')$

Correct Option

C $xyz + x'y + xyz'$

Correct Option

D $(A + B)'(A' + B')'$

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)

- (a) $xy + xy' = x(y + y') = x$
- (b) $(x + y)(x + y') = x + yy' = x(x + y') + y(x + y') = xx + xy' + xy + yy' = x$
- (c) $xyz + x'y + xyz' = xy(z + z') + x'y = xy + x'y = y$
- (d) $(A + B)'(A' + B')' = (A'B')(A'B) = (A'B')(BA) = A'(B'B)A = 0$

QUESTION ANALYTICS



Q. 16

[▶ Solution Video](#)[Have any Doubt ?](#)

Which of the following statement(s) is/are true?

A $(a + b + c')(a'b' + c) = ac + bc + a'b'c'$

Correct Option

B $a'bc + abc' + abc + a'bc' = b$

Correct Option

C ABC'D + A'BD + ABCD reduces to two literals

Correct Option

D $a'bc + a'bc' = b$

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)

- (a) $(a + b + c')(a'b' + c)$

$$= aa'b' + ac + ba'b' + bc + c'a'b' + c'c$$

$$= ac + bc + a'b'c'$$
- (b) $a'bc + abc' + abc + a'bc'$

$$= a'b(c + c') + ab(c + c')$$

$$= a'b + ab = (a' + a)b = b$$
- (c) ABC'D + A'BD + ABCD reduces to two literals.
ABC'D + A'BD + ABCD
$$= AB(C + C')D + A'BD$$

$$= ABD + A'BD = BD$$

Option (d) is false.

Q. 17

[Solution Video](#)[Have any Doubt?](#)

Addition of all gray code when (0-9) decimal digit are converted to Gray code?

 A 129 B 108 C 69 D 53

Correct Option

Solution :

(d)

First we can write the binary digit of 0 to 9 and then convert it into Grey code.

Binary	Gray code
0000	0000 → 0
0001	0001 → 1
0010	0011 → 3
0011	0010 → 2
0100	0110 → 6
0101	0111 → 7
0110	0101 → 5
0111	0100 → 4
1000	1100 → 12
1001	1101 → 13

So, $0 + 1 + 3 + 2 + 6 + 7 + 5 + 4 + 12 + 13 = 53$.

Q. 18

[FAQ](#)[Solution Video](#)[Have any Doubt?](#)

Which of the following logic expression is incorrect?

 A $1 \oplus 0 = 1$ B $1 \oplus 1 \oplus 0 = 1$

Correct Option

Solution :

(b)

Option (b) is the incorrect as EX-OR gate gives output 1 on getting odd number of 1's else output will be 0.

- (a) Contains odd number of 1's so output is 1.
- (b) Contains even number of 1's so output should be 0 ... but it is given 1.
- (c) Contains odd number of 1's so output should be 1 yes it is 1.
- (d) Even number of 1's so output should be 0 ... yes it is zero.

 C $1 \oplus 1 \oplus 1 = 1$ D $1 \oplus 1 = 0$

Q. 19

[FAQ](#)[Solution Video](#)[Have any Doubt?](#)

In a ripple counter using edge-triggered J-K flip-flops, the pulse output of one flip-flop is applied to

 A Clock input of all flip-flops. B J and K input of one flip-flop. C J and K input of next flip-flops. D Clock input of next flip-flop.

Correct Option

Solution :

(d)

In ripple counter using J-K flip-flop with positive edge triggered, the output of one FF is fed as clock input to the next FF. All FF are fed with inputs. Hence the option (c) is correct.

Which one of the following is the function of a multiplexer?

A To decode information.

B To select 1 out of N input data sources and to transmit it to single channel

Correct Option

Solution :

(b)

In electronics, a multiplexer (or mux; spelled sometimes as multiplexor), also known as a data selector, is a device that selects between several analog or digital input signals and forwards it to a single output line.

C To transmit data on N lines.

D To perform serial to parallel conversion.

 QUESTION ANALYTICS

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Q. 21
[Solution Video](#)
[Have any Doubt ?](#)

 How many 2-input multiplexers are required to construct a 2^{10} input multiplexer?

A 1023

[Correct Option](#)
Solution :

 (a)
 For 1024 input MUX:

$$\begin{array}{ll} \text{1st level} = \frac{1024}{2} = 512 & \text{2nd level} = \frac{512}{2} = 256 \\ \text{3rd level} = \frac{256}{2} = 128 & \text{4th level} = \frac{128}{2} = 64 \\ \text{5th level} = \frac{64}{2} = 32 & \text{6th level} = \frac{32}{2} = 16 \\ \text{7th level} = \frac{16}{2} = 8 & \text{8th level} = \frac{8}{2} = 4 \\ \text{9th level} = \frac{4}{2} = 2 & \text{10th level} = \frac{2}{2} = 1 \end{array}$$

Total sum all MUX = 1023.

B 31

C 10

D 127

QUESTION ANALYTICS


Q. 22
[FAQ](#) [Solution Video](#)
[Have any Doubt ?](#)

 In RS flip-flop, the output of the flip-flop at time $(t + 1)$ is same as the output at time t , after the occurrence of a clock pulse if

A $S = R = 1$
B $S = 0, R = 1$
C $S = 1, R = 0$
D $S = R = 0$
[Correct Option](#)
Solution :

(d)

QUESTION ANALYTICS


Q. 23
[Solution Video](#)
[Have any Doubt ?](#)


The hexadecimal equivalent of the binary integer number 110101101 is

A D24

B 18D

C 1AE

D 1AD

[Correct Option](#)
Solution :

(d)

Group the given number in subgroup of 4 from right and assign alphabet when it exceeds 1001:

1010 – A

1011 – B

1100 – C

1101 – D

1110 – E

1111 – F

Given number is 110101101:

1101 – D

1010 – A

1 – 1

Hexadecimal equivalent is 1AD

So, option (d) is correct.

QUESTION ANALYTICS

Q. 24

Solution Video

Have any Doubt?



Simplify the following using K-map:
 $F(A, B, C, D) = \Sigma(0, 1, 2, 8, 9, 12, 13)$
 $d(A, B, C, D) = \Sigma(10, 11, 14, 15)$
d stands for don't care condition.

A $A + B' D' + BC$

B $A + B' D' + B' C'$ Correct Option

C $A + B' C'$

D $A' + B'' C' + B' D'$

QUESTION ANALYTICS

Q. 25

FAQ Solution Video

Have any Doubt?



The smallest negative number which can be stored in computer that has 8-bit word length and uses 2's complement arithmetic is _____.

-128 Correct Option

Solution :

-128

The largest negative number is 1000 0000 = -128.

QUESTION ANALYTICS

Q. 26

FAQ Solution Video

Have any Doubt?



What is the value of $A \times B + C$ for a MOD-24 counter where A is the number of flip-flop for ripple counter, B is the number of flip-flop of ring counter, C is the number of the flip-flop of Johnson counter (used for the above given MOD value)?

132 Correct Option

Solution :

132

For MOD-24 counter \rightarrow

A = Number of flip-flop for ripple counter = $\lceil \log_2 24 \rceil = 5$

B = Number of flip-flop for ring counter = N = 24

C = Number of flip-flop for Johnson counter = $\frac{N}{2} = \frac{24}{2} = 12$

Therefore, $A \times B + C = 5 \times 24 + 12 = 132$

QUESTION ANALYTICS

Q. 27

FAQ Solution Video

Have any Doubt?



Let X = 1011 be a binary number. Y be a gray code equivalent of X. Then find decimal equivalent of Y.

14 Correct Option

Solution :

14

X = (1 0 1 1) in base 2

Y = 1 1 1 0 is gray code of X

Y = (14) in base 10

QUESTION ANALYTICS

Q. 28

FAQ Solution Video

Have any Doubt?



A 1-bit full adder takes 20 ns to generate carry out bit and 40 ns for the sum bit. What is the maximum rate of addition per microsecond when four 1-bit full adders are cascaded?

Solution :

10

Given,

$$\begin{aligned} T_c &= 20 \text{ ns and } T_s = 40 \text{ ns} \\ T_{s0} &= 40 \text{ ns} \\ T_{s1} &= (40 + 20)\text{ns} = 60 \text{ ns} \\ T_{s2} &= (60 + 20)\text{ns} = 80 \text{ ns} \\ T_{s3} &= (80 + 20)\text{ns} = 100 \text{ ns} \end{aligned}$$

Since final sum result takes 100 ns, therefore rate of addition per second = $\frac{1}{100 \text{ ns}} = (10)^7$.

QUESTION ANALYTICS



Q. 29

▶ Solution Video

Have any Doubt ?



The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0, ...) is _____.

3

Correct Option

Solution :

3

From the design a counter for 0, 1, 2, 3. It is a MOD-4 counter. Hence, number of flip-flops required will be two. Count sequence will be:

00, 01, 10, 11

Count sequence you mentioned is:

00, 00, 01, 01, 10, 10, 11, 11

Now, two flip-flops won't suffice, since we are confronted with repeated sequence, we may add another bit to the above sequence:

000, 100, 001, 101, 010, 110, 011, 111

Now each and every count is unique, occurring only once. Meanwhile, our machine has been extended to a MOD-8 counter. So the 3 flip-flops would do.

Just neglect the MSB flip-flop output and take the o/p of only other two.

So, we have: 0, 0, 1, 1, 2, 2, 3, 3 repeat.

QUESTION ANALYTICS



Q. 30

FAQ

▶ Solution Video

Have any Doubt ?



Consider a combinational circuit that converts BCD number to its 9's complement in BCD format only. Let the number of don't care conditions in this circuit be x and the number of outputs that are negative be y. Then find the value of $x - y$ is _____.

6

Correct Option

Solution :

6

The following is the truth table for conversion of a BCD input into its 9's complement form. Or 10 combinations are existing , rest 6 are don't care.

BCD number (d)	Binary equivalent of BCD number				9's complement (9 - d)	Binary equivalent of 9's complement number			
	w	x	y	z		C ₃	C ₂	C ₁	C ₀
0	0	0	0	0	9	1	0	0	1
1	0	0	0	1	8	1	0	0	0
2	0	0	1	0	7	0	1	1	1
3	0	0	1	1	6	0	1	1	0
4	0	1	0	0	5	0	1	0	1
5	0	1	0	1	4	0	1	0	0
6	0	1	1	0	3	0	0	1	1
7	0	1	1	1	2	0	0	1	0
8	1	0	0	0	1	0	0	0	1
9	1	0	0	1	0	0	0	0	0

Hence $x = 6$, $y = 0$ (As all are positive)Hence $x - y = 6$

QUESTION ANALYTICS



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OVERALL ANALYSIS COMPARISON REPORT **SOLUTION REPORT**

ALL(33) CORRECT(0) INCORRECT(0) SKIPPED(33)

Q. 31

[FAQ](#) [Solution Video](#) [Have any Doubt ?](#)

Which of the following Boolean expression(s) is/are true?

- A** $A'C' + ABC + AC'$ reduces to three literals.
- B** $(x'y' + z)' + z + xy + wz$ reduces to three literals.
- C** $A'B(D' + C'D) + B(A + A'CD)$ reduces to one literal.
- D** $(A' + C)(A' + C')(A + B + C'D)$ reduces to four literals.

[Correct Option](#)

[Correct Option](#)

[Correct Option](#)

YOUR ANSWER - NA

CORRECT ANSWER - a,b,c

STATUS - SKIPPED

Solution :

(a, b, c)

$$\begin{aligned}
 (a) \quad & A'C' + ABC + AC' \\
 &= C' + ABC \\
 &= (C + C')(C' + AB) \\
 &= AB + C' \\
 (b) \quad & (x'y' + z)' + z + xy + wz \\
 &= (x'y')' z' + z + xy + wz \\
 &= [(x + y)z' + z] + xy + wz \\
 &= (z + z')(z + x + y) + xy + wz \\
 &= z + wz + x + xy + y \\
 &= z(1 + w) + x(1 + y) + y \\
 &= x + y + z \\
 (c) \quad & A'B(D' + C'D) + B(A + A'CD) \\
 &= B(A'D' + A'C'D + A + A'CD) \\
 &= B(A'D' + A + A'D(C + C')) \\
 &= B(A + A'(D' + D)) \\
 &= B(A + A') = B \\
 (d) \quad & (A' + C)(A' + C')(A + B + C'D) \\
 &= (A' + CC')(A + B + C'D) \\
 &= A'(A + B + C'D) \\
 &= AA' + A'B + A'C'D \\
 &= A'(B + C'D)
 \end{aligned}$$

QUESTION ANALYTICS



Q. 32

[FAQ](#) [Solution Video](#) [Have any Doubt ?](#)

In 2's complement addition, Choose all the correct statement(s) with respect to the overflow

- A** It can only occur when positive value gets added to negative value.
- B** It will definitely occur when we add the values of same sign.
- C** It may/may not occur when we add values of same sign
- D** It can never occur when we add values of different sign.

[Correct Option](#)

[Correct Option](#)

YOUR ANSWER - NA

CORRECT ANSWER - c,d

STATUS - SKIPPED

Solution :

(c, d)

Adding two's-complement numbers requires no special processing if the operands have opposite signs: the sign of the result is determined automatically. The last two bits of the carry row (reading right-to-left) contain vital information: whether the calculation resulted in an arithmetic overflow, a number too large for the binary system to represent (in this case greater than 8 bits). An overflow condition exists when these last two bits are different from one another. As mentioned above, the sign of the number is encoded in the MSB of the result. In other terms, if the left two carry bits (the ones on the far left of the top row in these examples) are both 1's or both 0's, the result is valid; if the left two carry bits are "1 0" or "0 1", a sign overflow has occurred. Conveniently, an XOR operation on these two bits can quickly determine if an overflow condition exists.

QUESTION ANALYTICS



Q. 33

[FAQ](#) [Solution Video](#) [Have any Doubt ?](#)

Which of the following correctly define(s) the race around condition. (Choose all the correct options)

- A** Complementing the final result once in enable situation.

B

Complementing the final result more than once in enable situation.

Correct Option

C

Not Complementing the final result at all in enable situation.

D

Complementing the final result only twice in enable situation

YOUR ANSWER - NA

CORRECT ANSWER - b

STATUS - SKIPPED

Solution :

(b)

Race around condition in digital circuits occur when the final state of the output depends on how the inputs arrive. Digital circuits have inherent delays. So, it is possible that one of the inputs arrive a little earlier or later than others i.e. the inputs which were meant to be present at the same time actually arrive at different times due to different delays along their path. As a result of this, the output changes unpredictably. In other words, there is a race among the inputs as to which one will affect the output. Generally, this takes the form of spikes, which can be both high or low.



QUESTION ANALYTICS



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