



GATE CRASH COURSE

EC/EE/CS & IT/IN



Digital Electronics

PYQ SESSION



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20 Jan , - 28 Jan

Maha Revision

29th → Apti / Maths

30 | 31 → 30-40 hours



अभी तो असली मंजिल पाना बाकी है
अभी तो इरादों का इम्तिहान बाकी है
अभी तो तोली है मुट्ठी भर जमीन
अभी तोलना आसमान बाकी है

DIGITAL ELECTRONICS



NUMBER SYSTEMS

MCQ

If $(1235)_x = (3033)_y$, where x and y indicate the bases of the corresponding numbers, then

$$1x^3 + 2x^2 + 3x + 5 = 3y^3 + 3y + 3$$

$$8^3 + 2 \times 8^2 + 3 \times 8 + 5 = 3 \times 6^3 + 3 \times 6 + 3$$

- A** $x = 8$ and $y = 6$ **B** $x = 7$ and $y = 5$
- C** $x = 6$ and $y = 4$ **D** $x = 9$ and $y = 7$

✓ [GATE-2022-EC]

MCQ



Two numbers are chosen independently and uniformly at random from the set {1, 2, ..., 13}. The probability (rounded off to 3 decimal places) that their 4-bit (unsigned) binary representations have the same most significant bit is ____.

[GATE-2019 CSE]

- A 0.502
- B 0.461
- C 0.402
- D 0.561

$\frac{7}{13} \times \frac{7}{13}$	<table border="0"> <tr> <td>1 → 0001</td><td>X</td></tr> <tr> <td>2 → 0010</td><td>X</td></tr> <tr> <td>3 → 0011</td><td></td></tr> <tr> <td>4 → 0100</td><td></td></tr> <tr> <td>5 → 0101</td><td></td></tr> <tr> <td>6 → 0110</td><td></td></tr> <tr> <td>7 → 0111</td><td></td></tr> <tr> <td>8 → 1000</td><td></td></tr> <tr> <td>9 → 1001</td><td></td></tr> <tr> <td>10 → 1010</td><td></td></tr> <tr> <td>11 → 1011</td><td></td></tr> </table>	1 → 0001	X	2 → 0010	X	3 → 0011		4 → 0100		5 → 0101		6 → 0110		7 → 0111		8 → 1000		9 → 1001		10 → 1010		11 → 1011	
1 → 0001	X																						
2 → 0010	X																						
3 → 0011																							
4 → 0100																							
5 → 0101																							
6 → 0110																							
7 → 0111																							
8 → 1000																							
9 → 1001																							
10 → 1010																							
11 → 1011																							

$$\begin{aligned}
 & 12 \rightarrow 1100 \\
 & 13 \rightarrow 1101 \\
 \text{MSB = 0} & \rightarrow 3 \\
 \text{MSB = 1} & \rightarrow 6
 \end{aligned}$$

$$\frac{6}{13} \times \frac{6}{13}$$

$$\{0, 1, \dots, 13\}$$

$$P = \left(\frac{7}{13} \times \frac{7}{13}\right) + \left(\frac{6}{13} \times \frac{6}{13}\right)$$

$$P = 0.502$$

$$MSB=0 \rightarrow \checkmark$$

$$MSB=1 \rightarrow 6$$

The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) form is _____

[GATE-2014-EC]

MCQ

When two 8-bit numbers $A_7 \dots A_0$ and $B_7 \dots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a ripple-carry adder, the sum bits obtained are $S_7 \dots S_0$ and the carry bits are $C_7 \dots C_0$. An overflow is said to have occurred if

[GATE-2017-set-01] CS

- A The carry bit C_7 is 1
- B All the carry bits (C_7, \dots, C_0) are 1
- C $(A_7 \cdot B_7 \cdot \bar{S}_7 + \bar{A}_7 \cdot B_7 \cdot S_7)$ is 1
- D $(A_0 \cdot B_0 \cdot \bar{S}_0 + \bar{A}_0 \cdot B_0 \cdot S_0)$ is 1

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	+	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0							
																$=$							
																S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

 The carry bits are labeled $C_7, C_6, C_5, C_4, C_3, C_2, C_1, C_0$ from left to right. A green circle highlights the 7th column of bits (the most significant column). A green arrow points from the 7th column of the sum S to the label 'Overflow'."/>
$$\overline{A}_7 \overline{B}_7 S_7 + A_7 B_7 \overline{S}_7$$

Overflow



MINIMIZATION

$$(x+y)(x+z)$$

Select the Boolean function(s) equivalent to $x + yz$, where x,y, and z are Boolean variables, and + denotes logical OR operation.

[GATE-2022-EC]

$$x(1+y) + z = x + z$$

A

$$x + z + xy$$

B

$$(x+y)(x+z)$$

b,c

C

$$x + xy + yz$$

D

$$x + xz + xy$$

$$x(1+y) + yz$$

$$x(1+z+y) = x$$

$$x + yz = (x+y)(x+z)$$

MCQ

P
W

Following is the K-map of a Boolean function of five variables P, Q, R, S and X. The minimum sum-of-product (SOP) expression for the function is

$\overline{X}P\overline{Q}RS$

$\overline{Q}\overline{S}\overline{X}$

		PQ	00	01	11	10
		RS	00	01	11	10
00	00	0	0	0	0	0
		1	0	0	1	
11	01	1	0	0	1	
		0	0	0	0	0
10	10	0	0	0	0	0

$X = 0$

		PQ	00	01	11	10
		RS	00	01	11	10
00	00	0	1	1	0	0
		0	0	0	0	0
11	01	0	0	0	0	0
		0	1	1	0	0
10	10	0	1	1	0	0

$X = 1$

[GATE-2016-EC]

$Q\bar{S}X$

$\overline{Q}S\bar{X} + Q\bar{S}X$

A

$$\overline{P}\overline{Q}S\bar{X} + P\overline{Q}S\bar{X} + Q\overline{R}\bar{S}X + QR\bar{S}X$$

B

$$\overline{Q}S\bar{X} + Q\bar{S}X$$

C

$$\overline{Q}SX + Q\overline{S}\bar{X}$$

D

$$\overline{Q}S + Q\bar{S}$$

A function of Boolean variables, X, Y and Z is expressed in terms of the min-terms as

$$F(X, Y, Z) = \sum m(1, 2, 5, 6, 7) = \pi M(0, 3, 4)$$

Which one of the product of sums given below is equal to the function F (X, Y, Z)?

POS.

[GATE-2015-EC]

- A $(\bar{X} + \bar{Y} + \bar{Z}) \cdot (\bar{X} + Y + Z) \cdot (X + \bar{Y} + \bar{Z})$
- B ~~$(X + Y + Z) \cdot (X + \bar{Y} + \bar{Z}) \cdot (\bar{X} + Y + Z)$~~
- C $(\bar{X} + \bar{Y} + Z) \cdot (\bar{X} + Y + \bar{Z}) \cdot (X + \bar{Y} + Z) \cdot (X + Y + \bar{Z}) \cdot (X + Y + Z)$
- D $(X + Y + \bar{Z}) \cdot (\bar{X} + Y + Z) \cdot (\bar{X} + Y + \bar{Z}) \cdot (\bar{X} + \bar{Y} + Z) \cdot (\bar{X} + \bar{Y} + \bar{Z})$

		$y+z$	$\bar{y}+z$
x	\bar{x}	0	1
\bar{x}	x	1	0
$y+z$	00	01	11
$\bar{y}+z$	01	11	10

$$(x+y+z)(\bar{x}+y+z)(x+\bar{y}+z)$$

MCQ

Consider the minterm list form of a Boolean function F given below.

$$F(P, Q, R, S) = \sum m(0, 2, 5, 7, 9, 11) + d(3, 8, 10, 12, 14)$$

Here, m denotes a minterm and d denotes a don't care term. The number of essential prime implicants of the function F is ____.

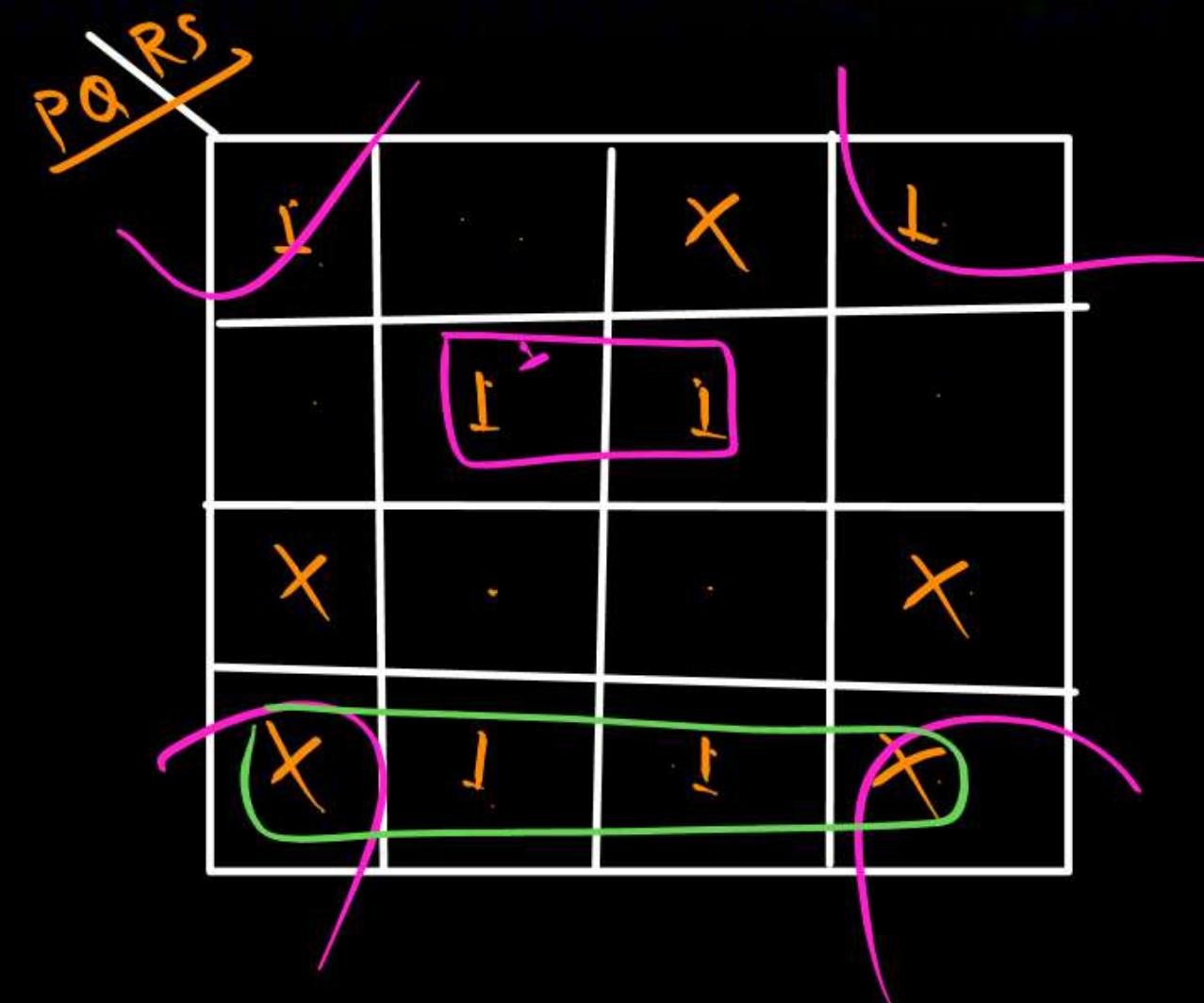
[GATE-2018 CSE]

A 3

B 4

C 5

D 6



MCQ

The Boolean expression

$$\underbrace{(X + Y)(X + \bar{Y})}_{X+Y\cdot\bar{Y}} + \overline{\overline{XY} + \bar{X}}$$

$$+ \overline{\bar{X}(\bar{Y}+1)}$$

X

$$X + \bar{X} = X + X = X \checkmark$$

A X

B Y

C XY

D X + Y

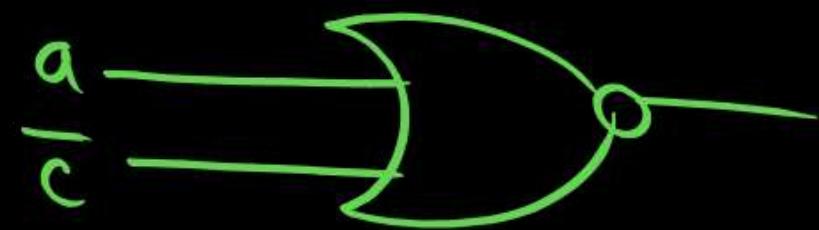
[GATE-2014-EC]

#CHAMKA .

Consider the Karnaugh map given below, where X represents “don’t care” and blank represents 0.

$$\bar{a} \cdot c = \overline{(a + \bar{c})}$$

	ba	00	01	11	10
dc	00	x	x		
00	01	1			x
01	11	1			1
11	10		x	x	
10					



Assume for all inputs (a, b, c, d) , the respective complements (a', b', c', d') are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is _____.

A 1

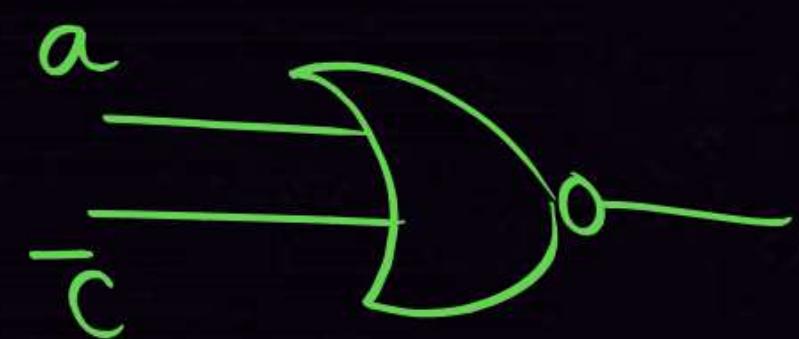
C 3

B 2

D 4

[GATE-2017 set-01 CSE]

$$\overline{(a + \bar{c})} = \bar{a} \cdot \bar{\bar{c}}$$
$$= \bar{a} \cdot c$$



$$f = a \cdot b \cdot \bar{c} \cdot d \cdot \dots \dots$$

n = no. of Variables

$k \rightarrow$ no. of Variables in complement

$$\text{Number of NAND GATE} = (2n-2) + k$$

$$\text{Number of NOR GATE} = (3n-3) - k$$

MCQ

P
W

The output expression for the Karnaugh map shown below is

[GATE-2019-EE]

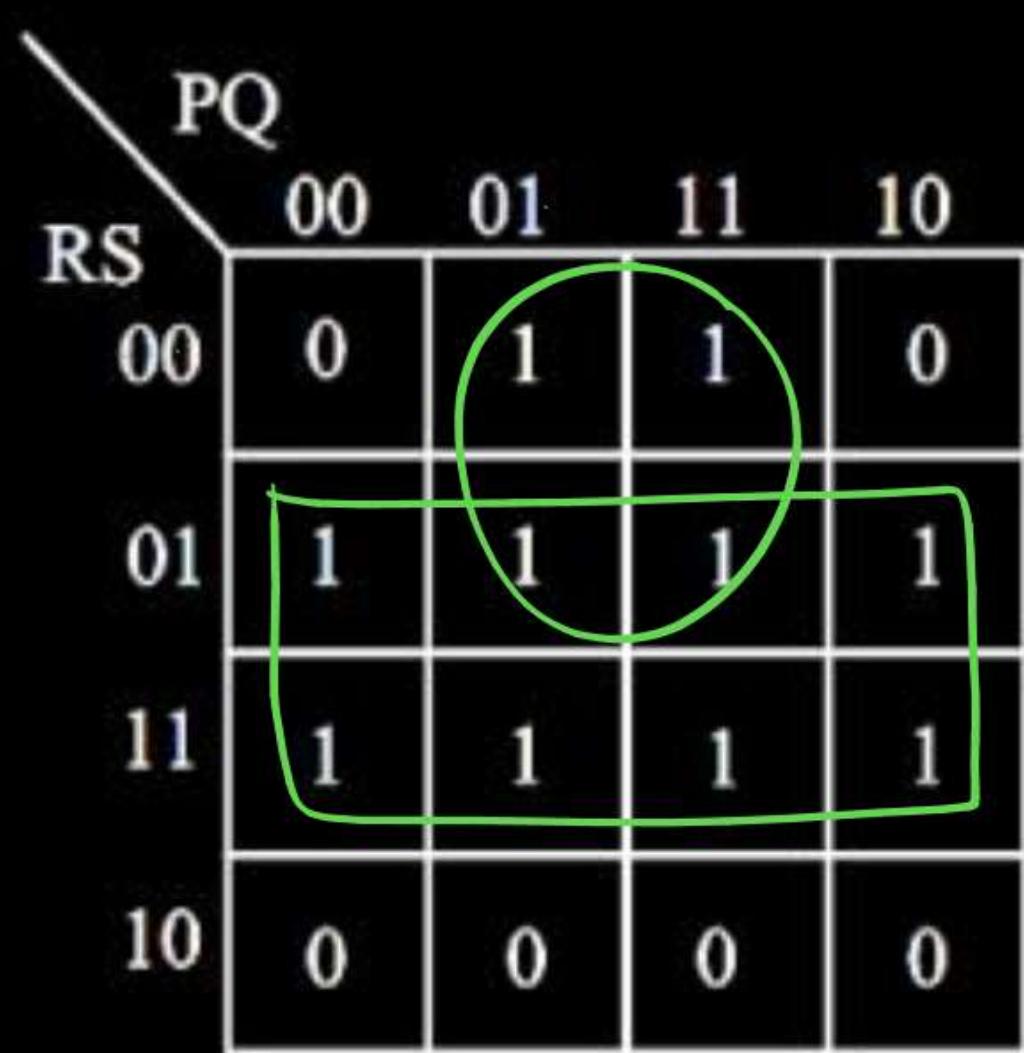
A $Q\bar{R} + S$

B $Q\bar{R} + \bar{S}$

C $QR + S$

D $QR + \bar{S}$

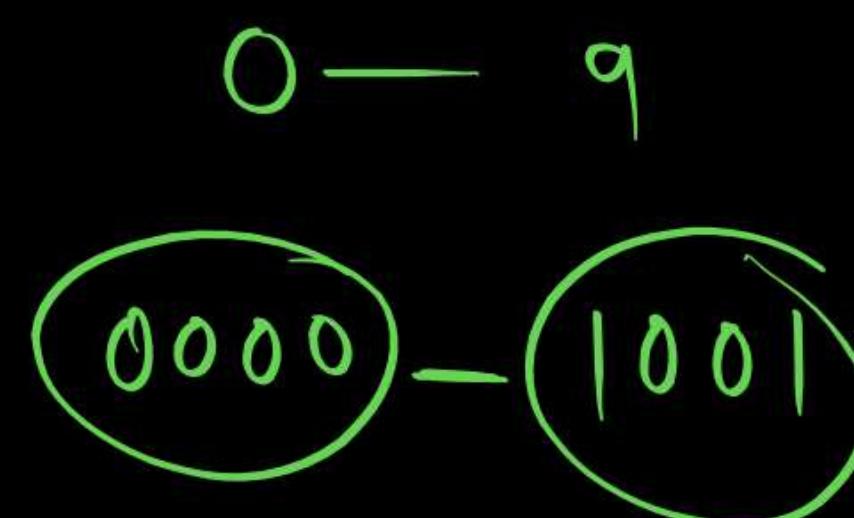
$S + \bar{R}Q$



Which of the following is an invalid state in 8-4-2-1 Binary Coded Decimal counter?

[GATE-2014-EE]

- A 1000
- B 1001
- C 0011
- D 1100





LOGIC GATES

MCQ

Consider three 4-variable functions f_1 , f_2 and f_3 , which are expressed in sum-of-minterms as

$$f_1 = \Sigma(0, 2, 5, 8, 14), f_2 = \Sigma(2, 3, 6, 8, 14, 15), f_3 = \Sigma(2, 7, 11, 14)$$

For the following circuit with one AND gate and one XOR gate, the output function f can be expressed as:

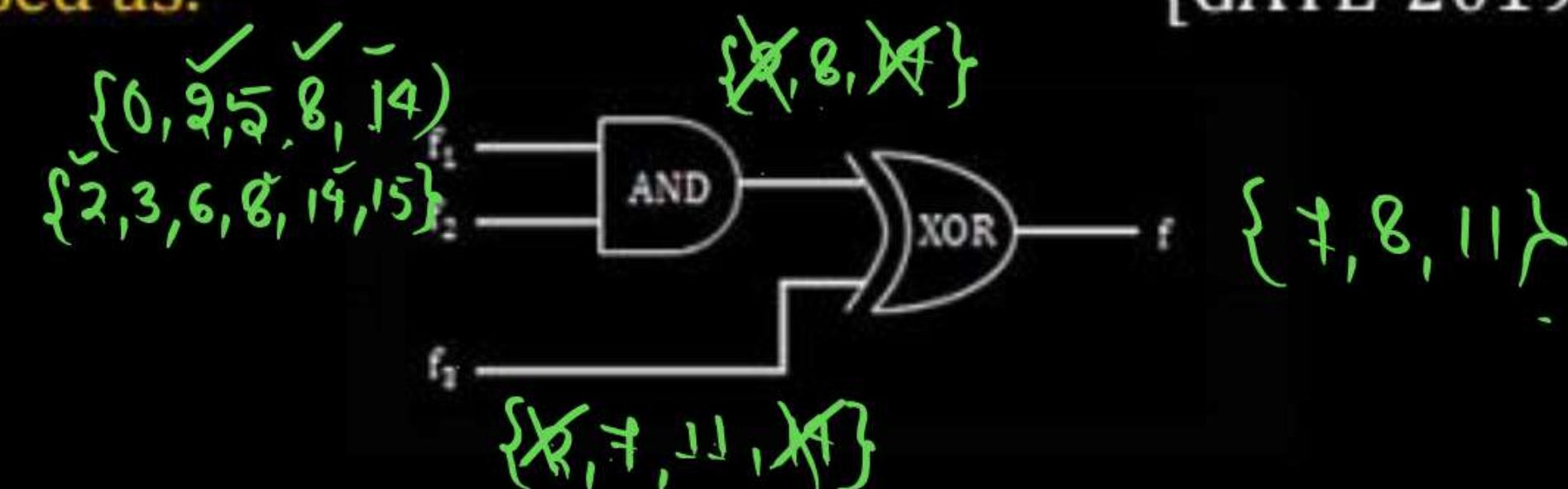
[GATE-2019 CSE]

A $\Sigma(2, 14)$

B $\cancel{\Sigma}(7, 8, 11)$

C $\Sigma(2, 7, 8, 11, 14)$

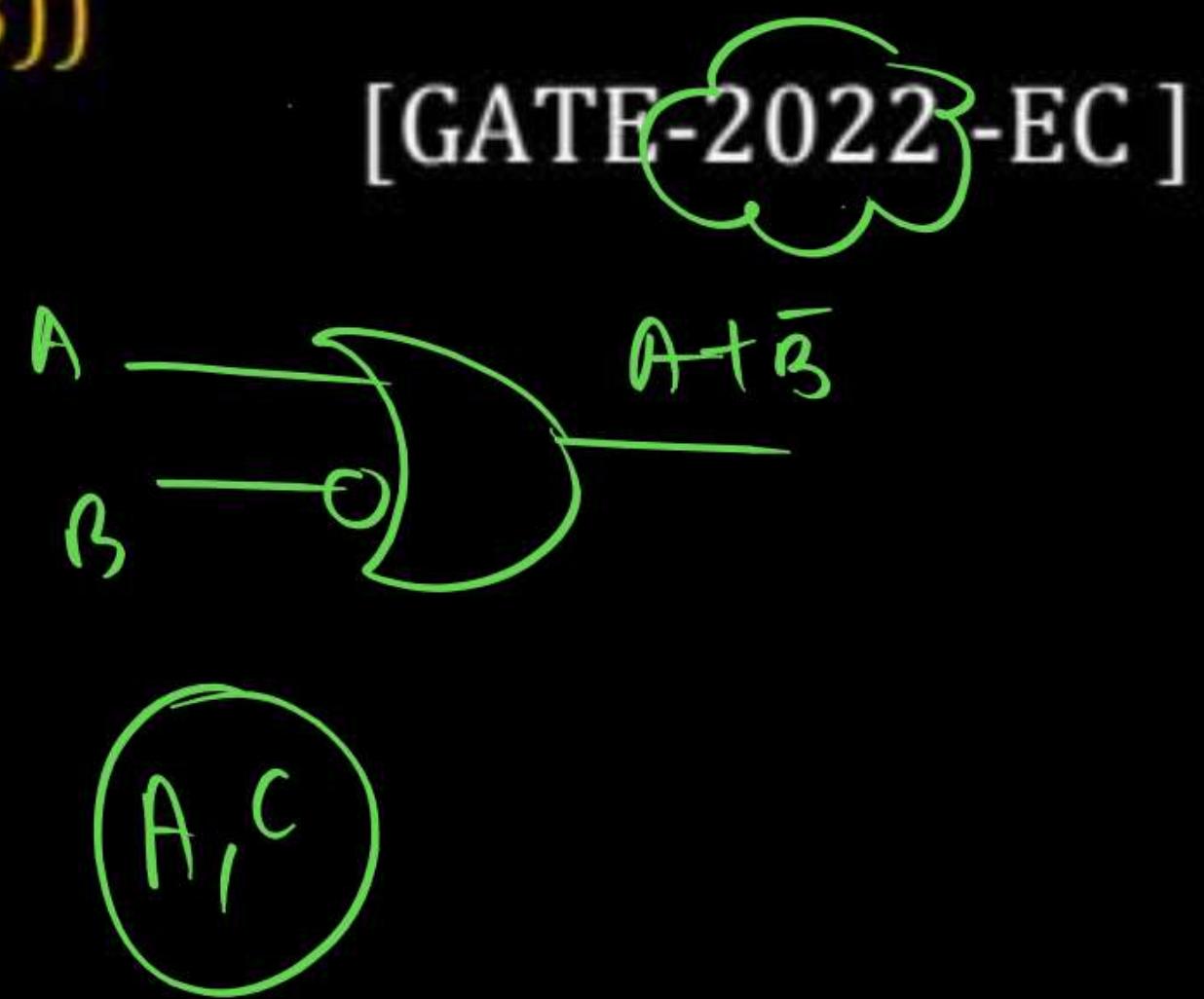
D $\Sigma(0, 2, 3, 5, 6, 7, 8, 11, 14, 15)$



Consider a Boolean gate (D) where the output Y is related to the inputs A and B as, $Y = A + \bar{B}$, where + denotes logical OR operation. The Boolean inputs '0' and '1' are also available separately. Using instances of only D gates and inputs '0' and '1', _____ (Select the correct option(s)). (49(3))

[GATE-2022-EC]

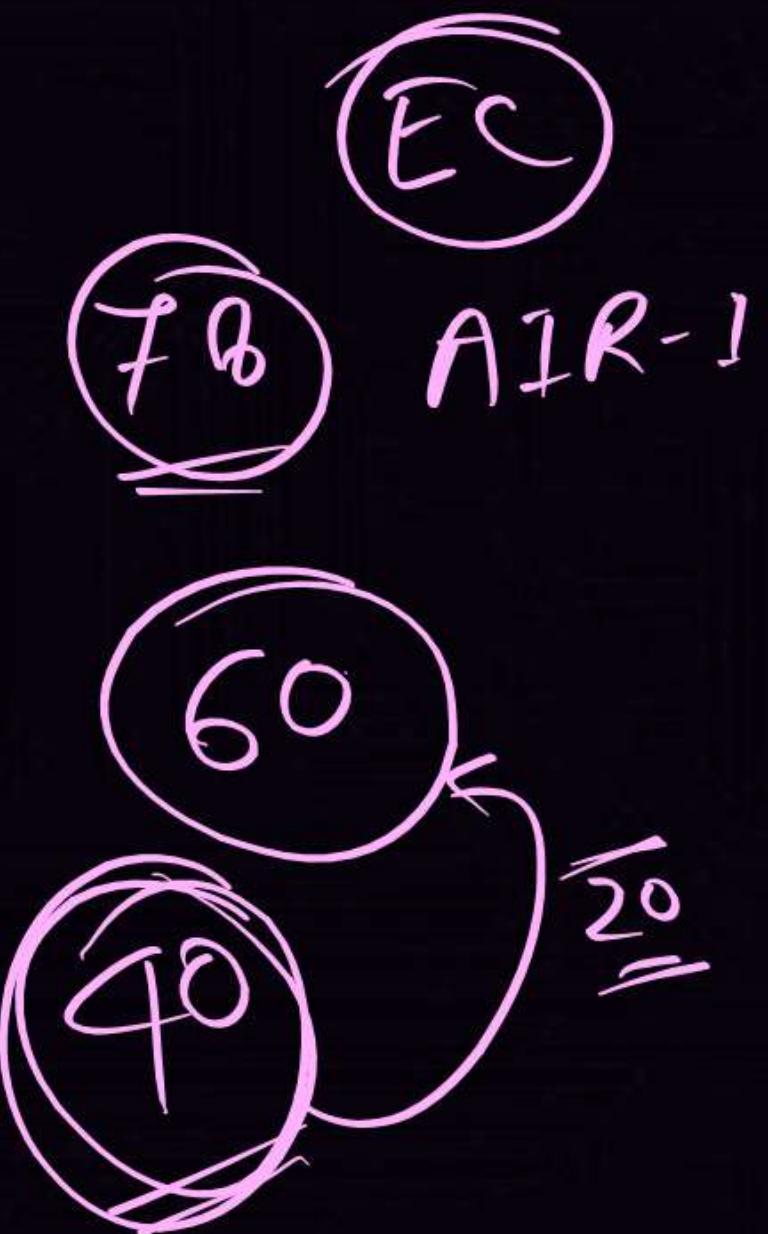
- A NAND logic can be implemented
- B OR logic cannot be implemented
- C NOR logic can be implemented
- D AND logic cannot be implemented



TEST SERIES.

Improvement

- ① Question ✓ → Concepts
- ② Question → X
- ③ silly mistake.
- ④ Formula apply



universal

$\overline{A \cdot B} = \overline{A} + \overline{B}$

$\overline{A+B} = \overline{A} \cdot \overline{B}$

$\overline{A} \cdot B$

$A \cdot \overline{B}$

$\overline{A} + B$

$A + \overline{B}$

MUX

Decoder+OR

universal
Invert.
NAND
OR
NOR
XOR
X-NOR

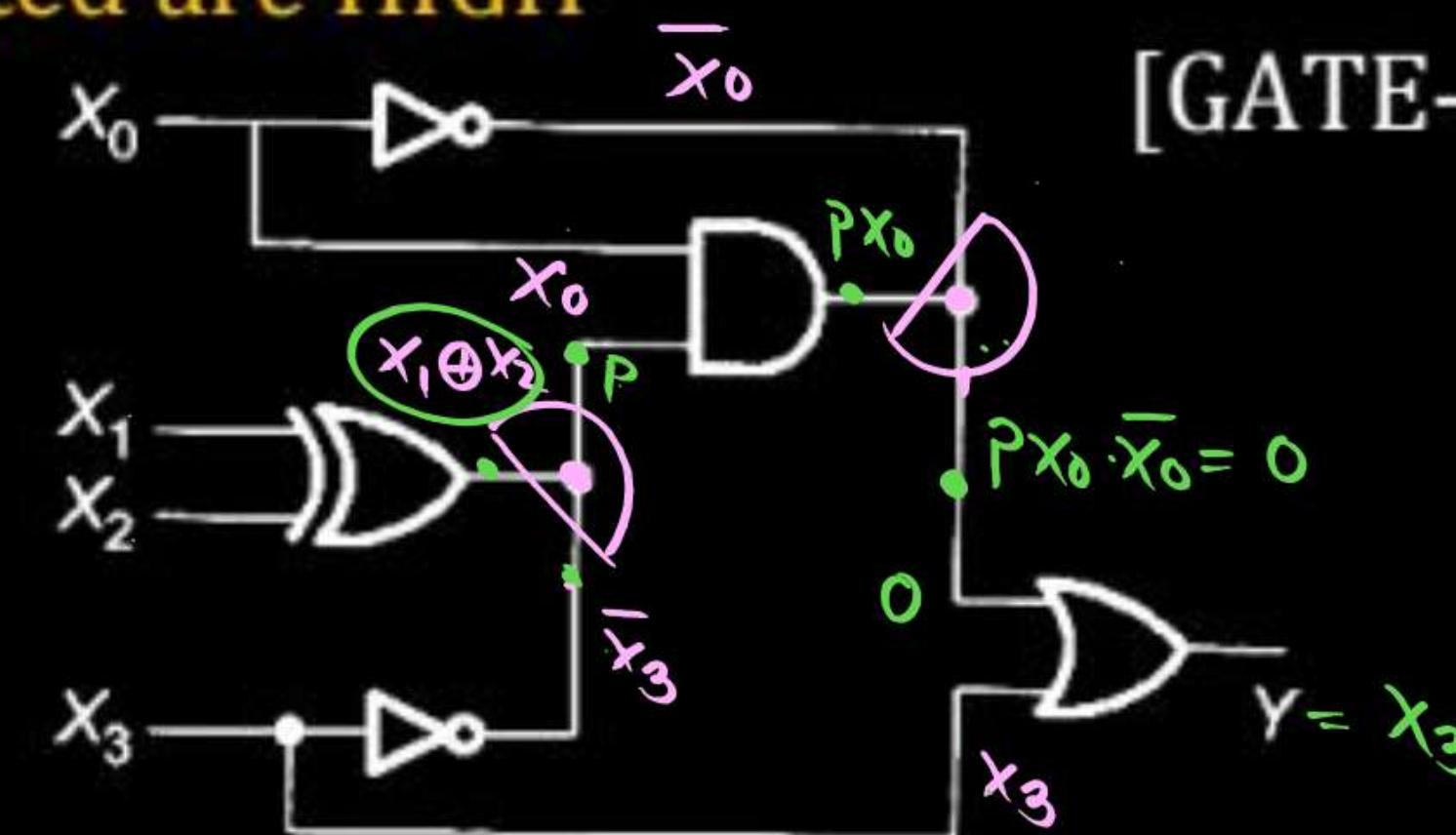
MCQ

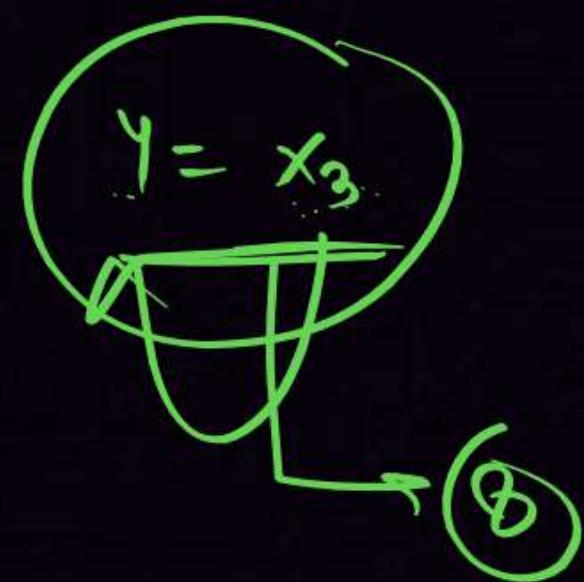
The logic gates shown in the digital circuit below use strong pull-down nMOS transistors for LOW logic level at the outputs. When the pull-downs are off, high-value resistors set the output logic levels to HIGH (i.e. the pull-ups are weak). Note that some nodes are intentionally shorted to implement "wired logic". Such shorted nodes will be HIGH only if the outputs of all the gates whose outputs are shorted are HIGH

$$P = (x_1 \oplus x_2) \bar{x}_3$$

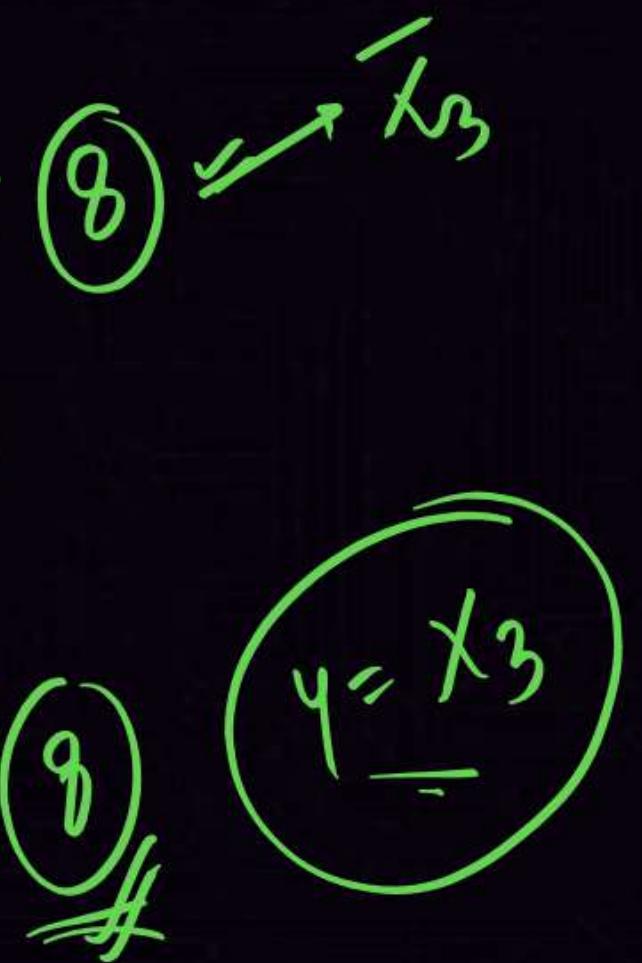
The number of distinct values of x_3 , x_2 , x_1 , x_0 (out of the 16 possible values) that give $Y = 1$ is

8



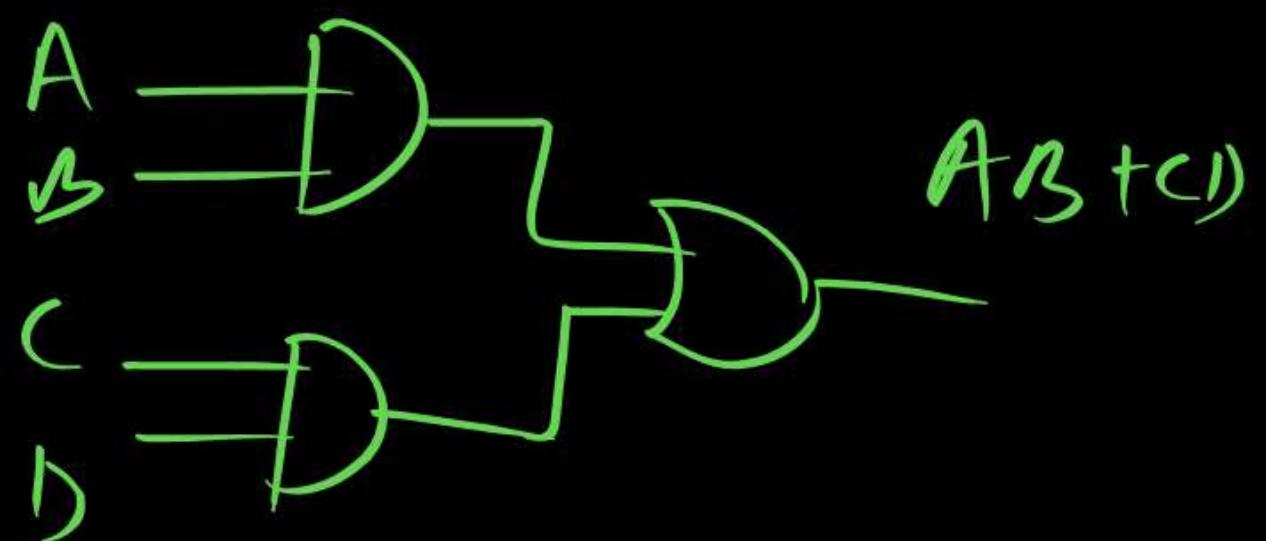
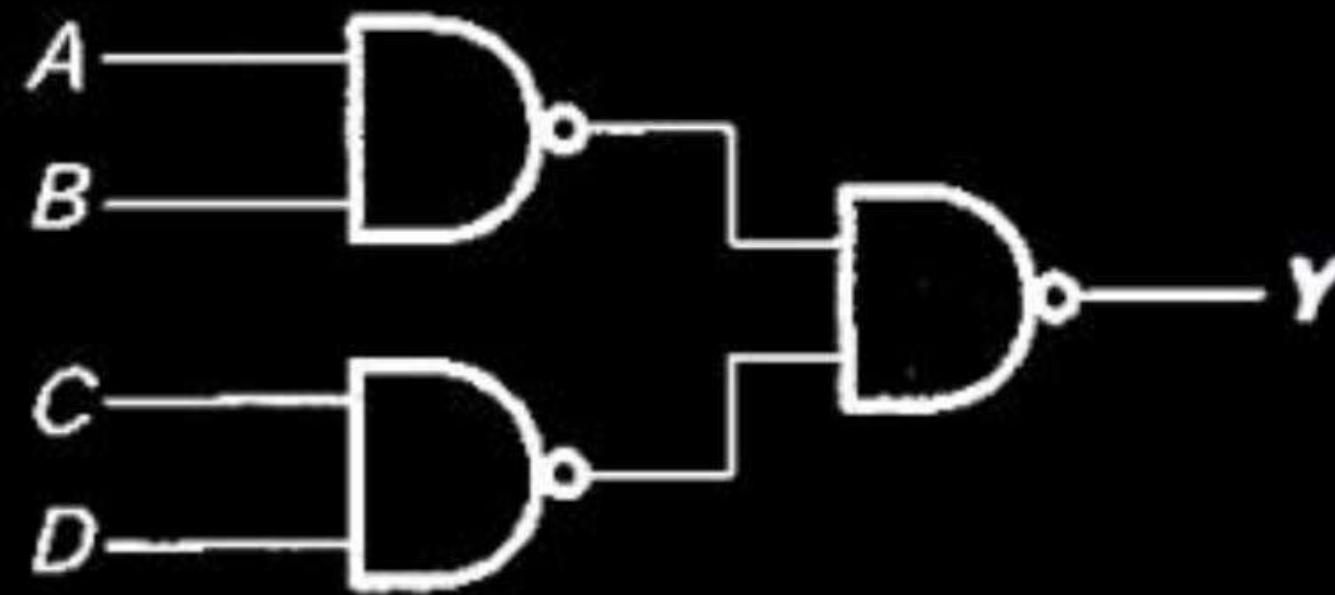


x_3	x_2	x_1	x_0
0	0	0	0
0	0	0	1
0	0	1	0
⋮	⋮	⋮	⋮
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
⋮	⋮	⋮	⋮
1	1	1	1



In the logic circuit shown in the figure, Y is given by

[GATE-2018-EE]



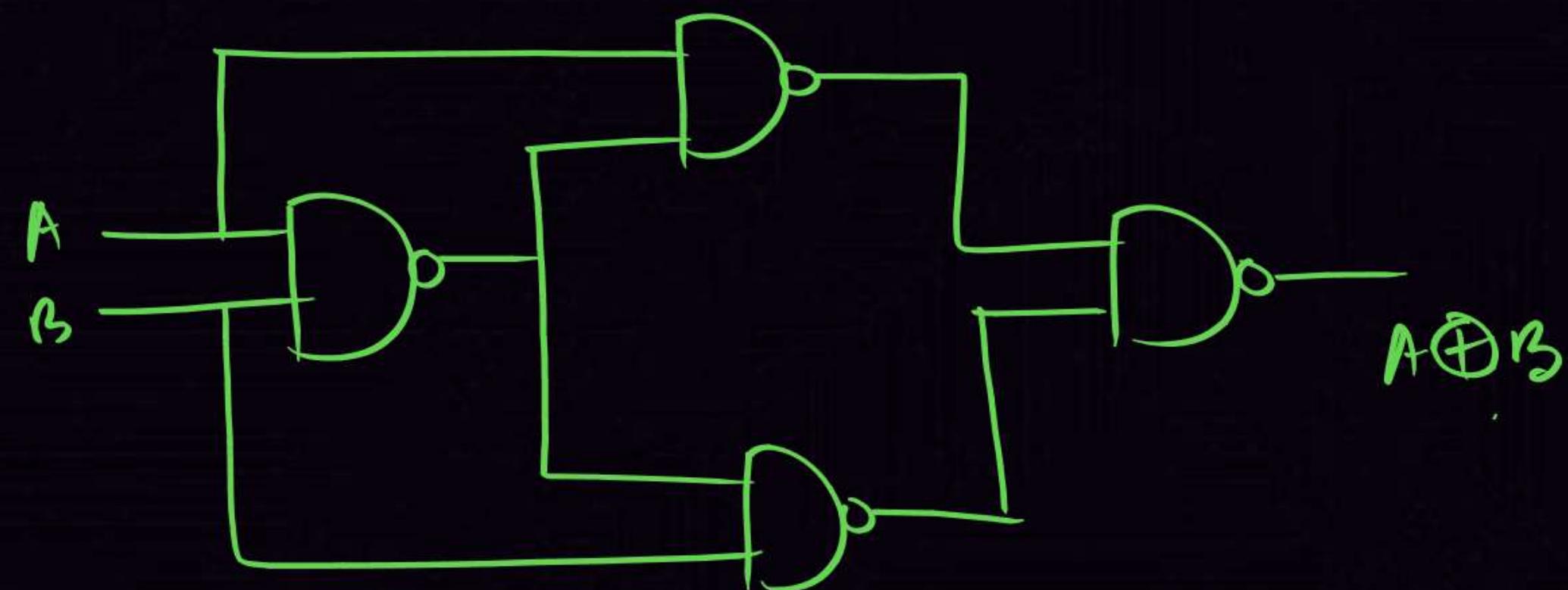
- A $Y = ABCD$
- B $Y = (A + B)(C + D)$
- C $Y = A + B + C + D$
- D $Y = AB + CD$

MCQ

The minimum number of 2-input NAND gates required to implement a 2-input XOR gate is

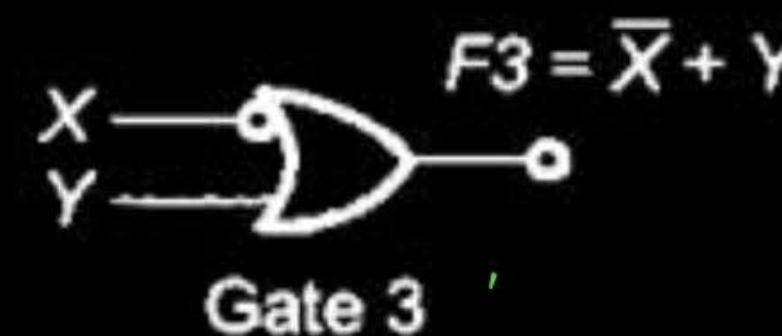
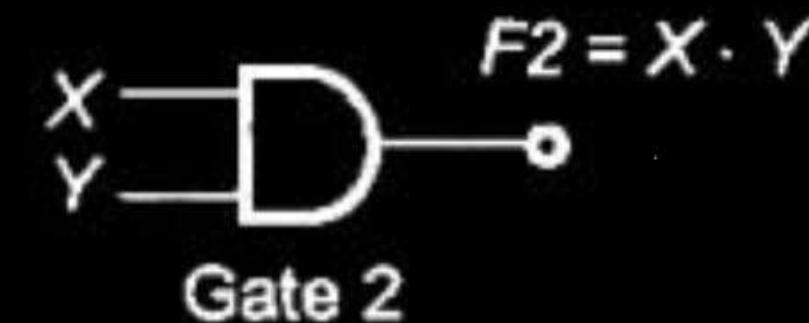
[GATE-2016-EC]

- A 4
- B 5
- C 6
- D 7



MCQ

A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown.



[GATE-2015-EC]

Which one of the following statements is TRUE?

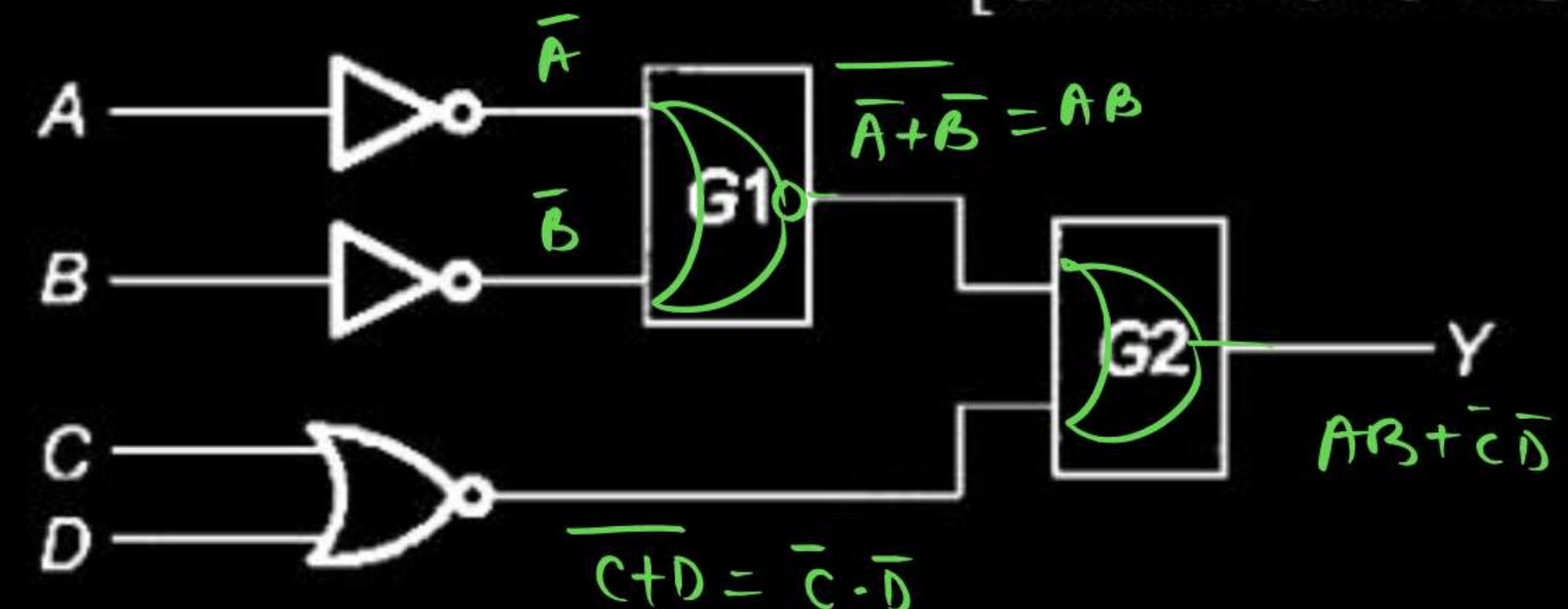
- A Gate 1 is a universal gate.
- B Gate 2 is a universal gate.
- C Gate 3 is a universal gate.
- D None of the gates shown is a universal gate.

MCQ

In the figure shown, the output Y is required to be $Y = AB + \overline{CD}$.
The gates G1 and G2 must be,

- A NOR, OR
- B OR, NAND
- C NAND, OR
- D AND, NAND

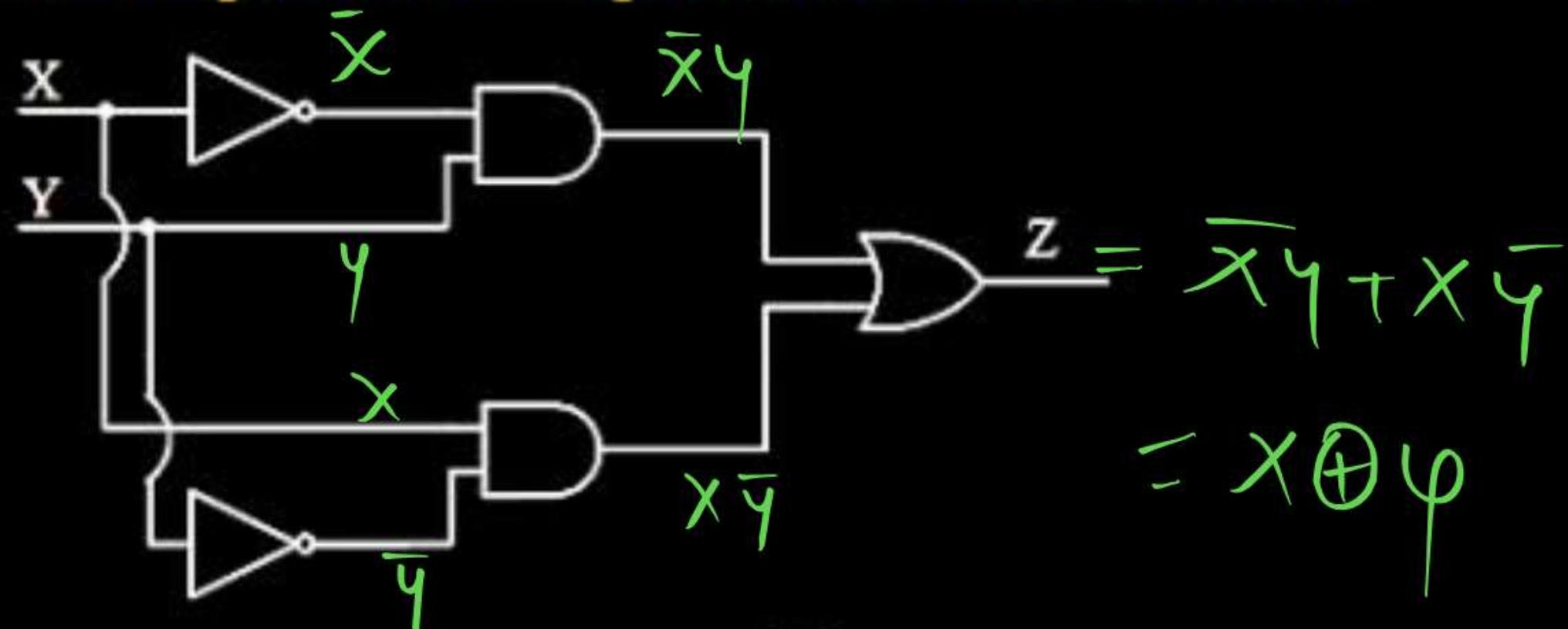
[GATE-2015-EC]



P
W



In the circuit shown below, X and Y are digital inputs, and Z is a digital output. The equivalent circuit is a

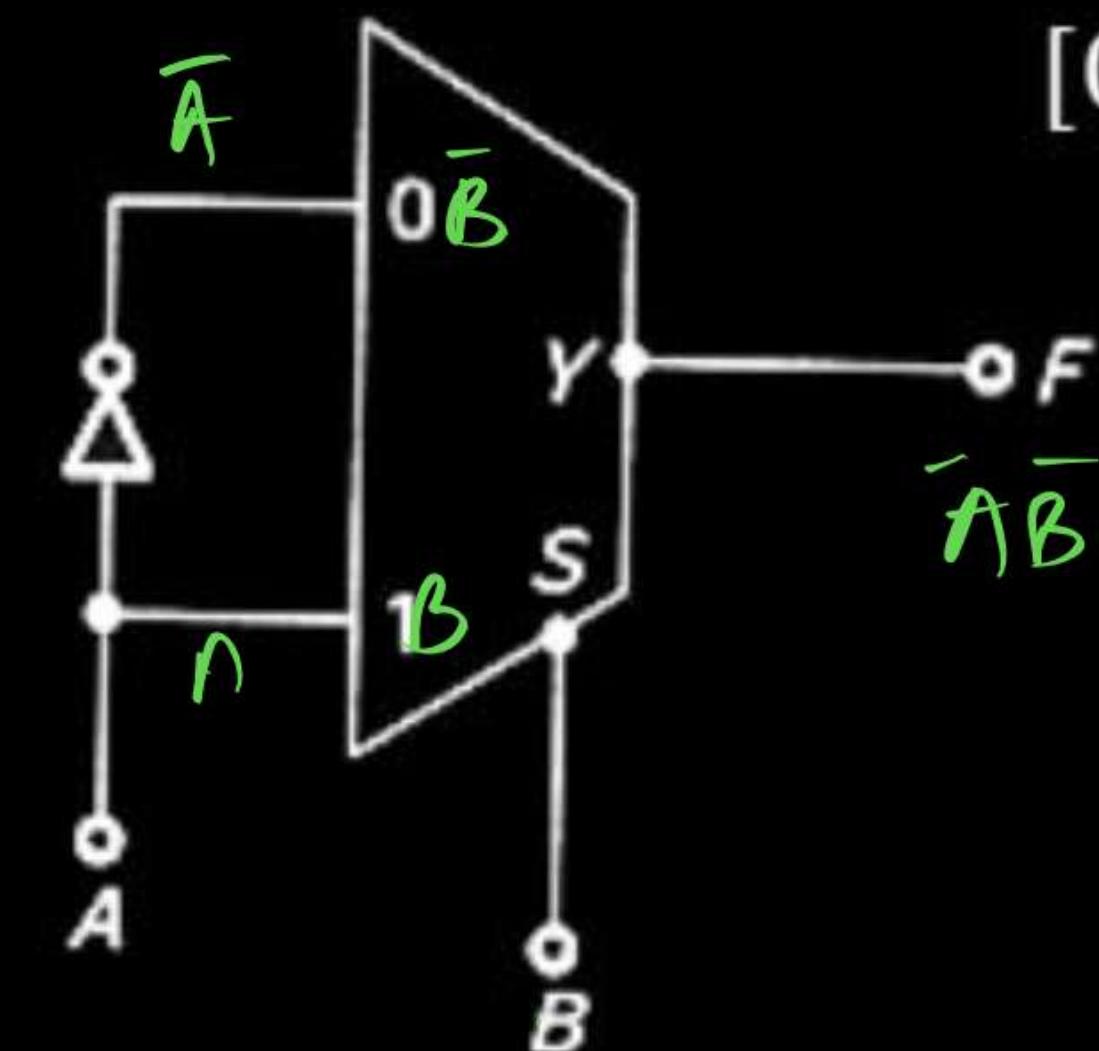


[GATE-2019-EE]

- A NAND gate
- B NOR gate
- C XOR gate
- D XNOR gate

Consider the following circuit which uses a 2-to-1 multiplexer as shown in the figure below. The Boolean expression for output F in terms of A and B is?

- A $A \oplus B$
- B $\overline{A + B}$
- C $A + B$
- D $\overline{A \oplus B}$



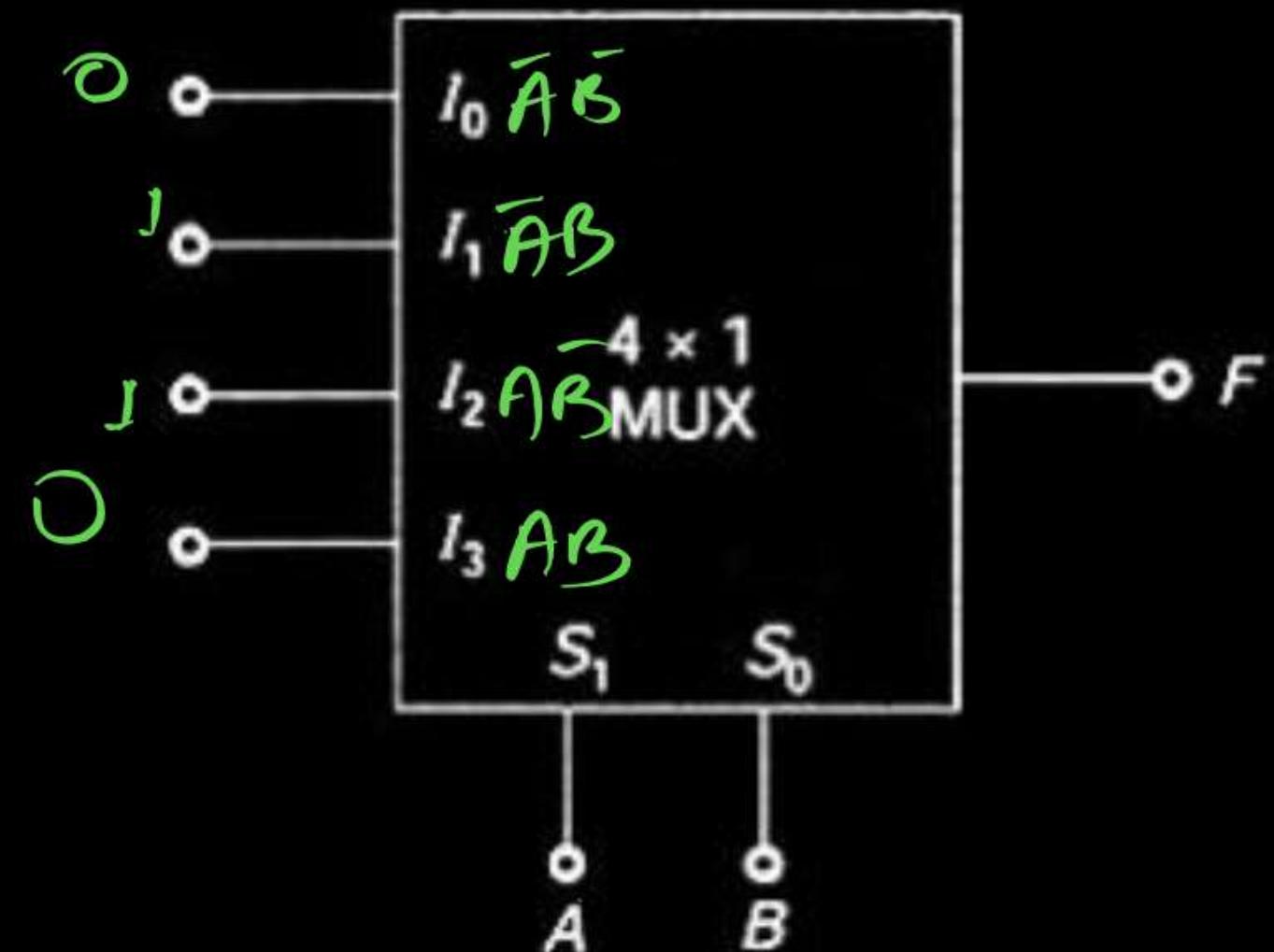
[GATE-2019-EE]

$$\begin{aligned}\bar{A}\bar{B} + A\bar{B} &= A \oplus B \\ &= \overline{A \oplus B}\end{aligned}$$

In the 4×1 multiplexer, the output F is given by $F = A \otimes B$. Find the required input ' $I_3 I_2 I_1 I_0$ '.

[GATE-2015-EE]

- A 1010
- B 0110
- C 1000
- D 1110





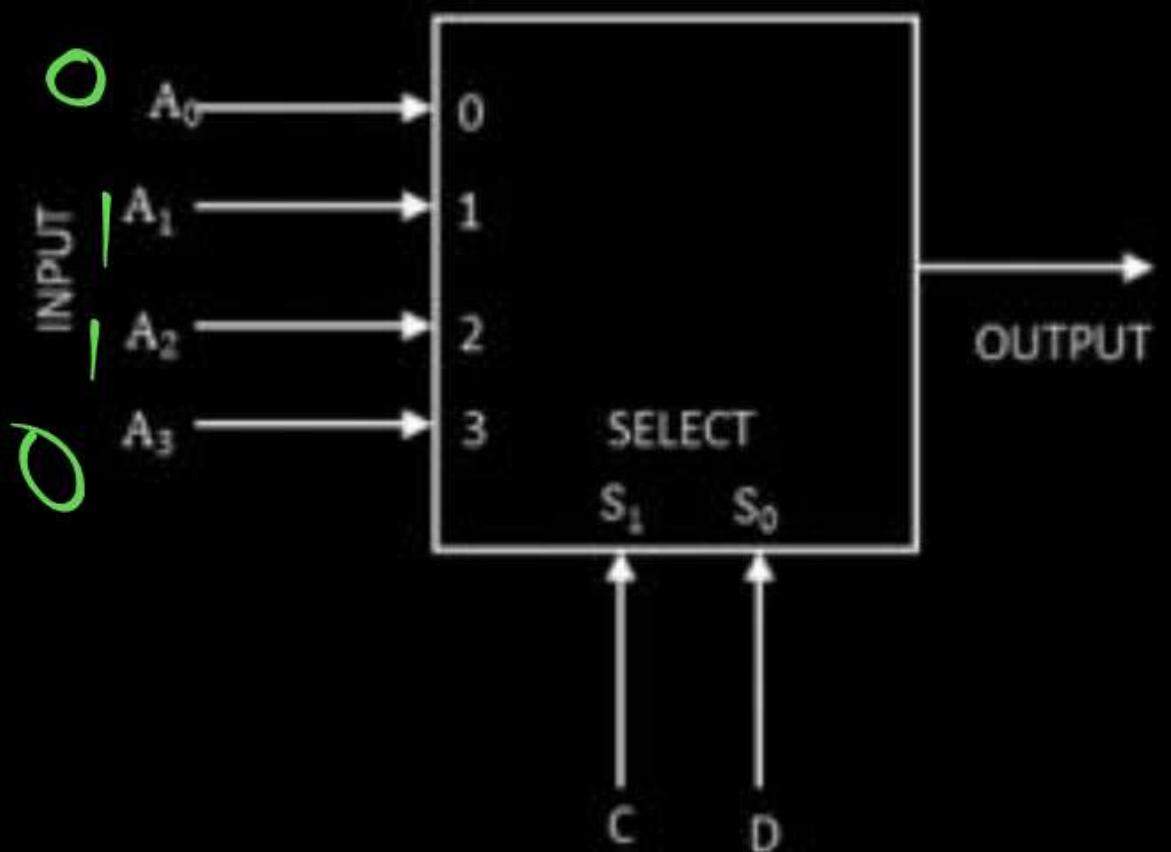
COMBINATIONAL CIRCUITS

MCQ

Consider the 2-bit multiplexer (MUX) shown in the figure. For OUTPUT to be the **XOR** of C and D, the values for A_0, A_1, A_2 , and A_3 are _____.

[GATE-2022-EC]

- A $A_0 = 0, A_1 = 0, A_2 = 1, A_3 = 1$
- B $A_0 = 1, A_1 = 0, A_2 = 1, A_3 = 0$
- C $A_0 = 0, A_1 = 1, A_2 = 1, A_3 = 0$
- D $A_0 = 1, A_1 = 1, A_2 = 0, A_3 = 0$

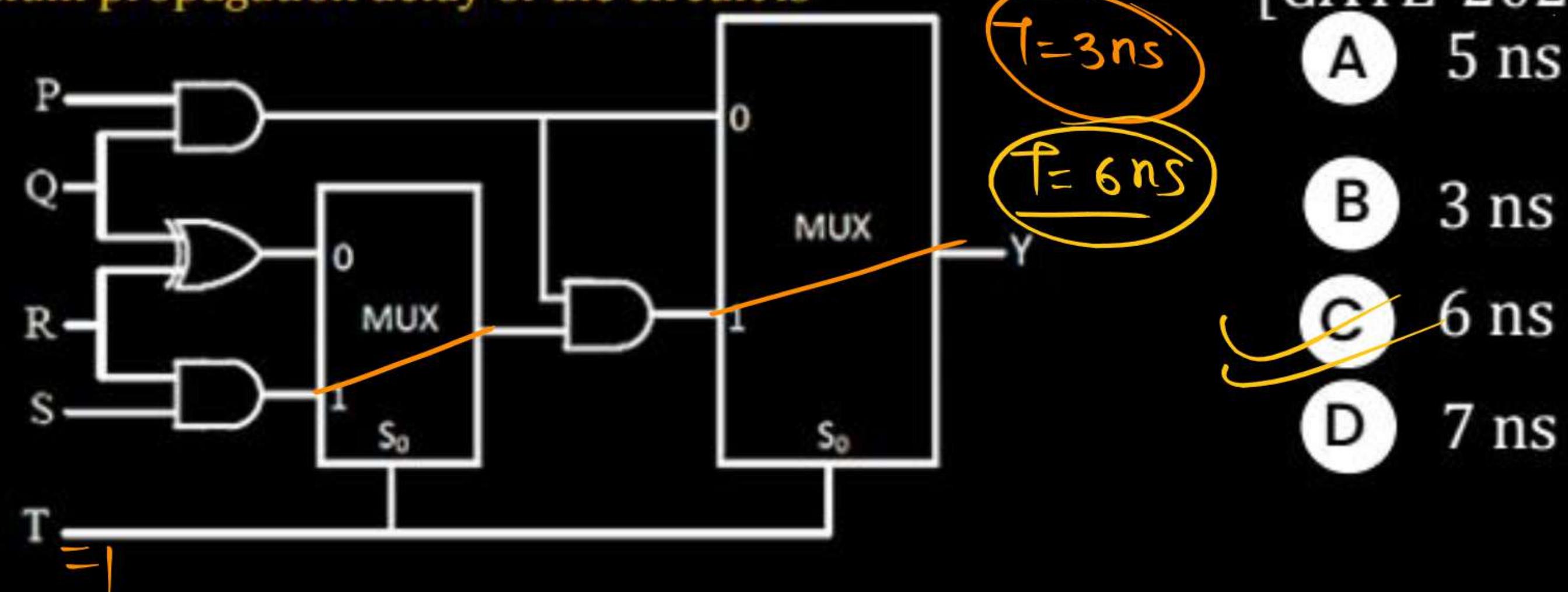


MCQ

The propagation delays of the XOR gate, AND gate and multiplexer (MUX) in the circuit shown in the figure are 4 ns, 2 ns and 1 ns, respectively.

If all the inputs P, Q, R, S and T are applied simultaneously and held constant, the maximum propagation delay of the circuit is

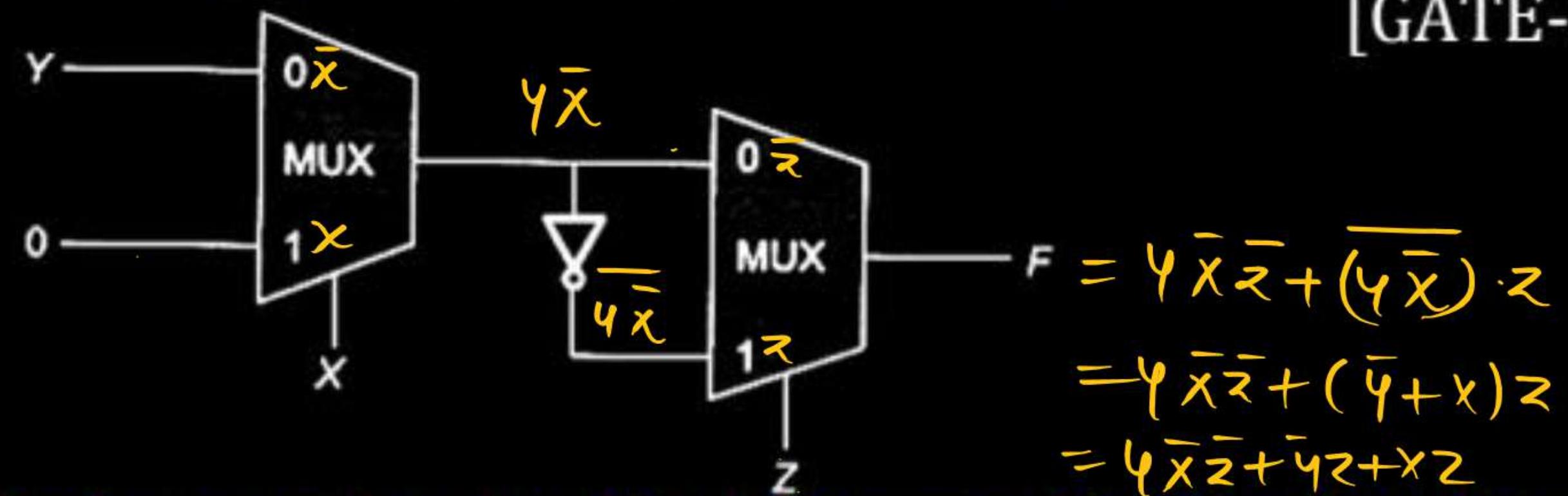
[GATE-2021-EC]



MCQ

Consider the circuit shown in the figure.

[GATE-2017-EC]



The Boolean expression F implemented by the circuit is

A $\bar{XYZ} + XY + \bar{YZ}$

B $\bar{XYZ} + XZ + \bar{YZ}$

C $\bar{XYZ} + XY + \bar{YZ}$

D $\bar{XYZ} + XZ + \bar{YZ}$

MCQ

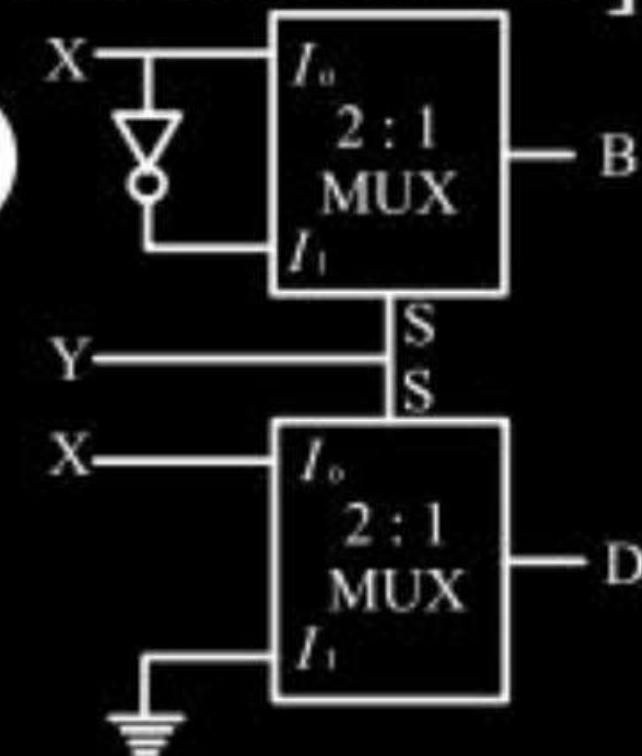
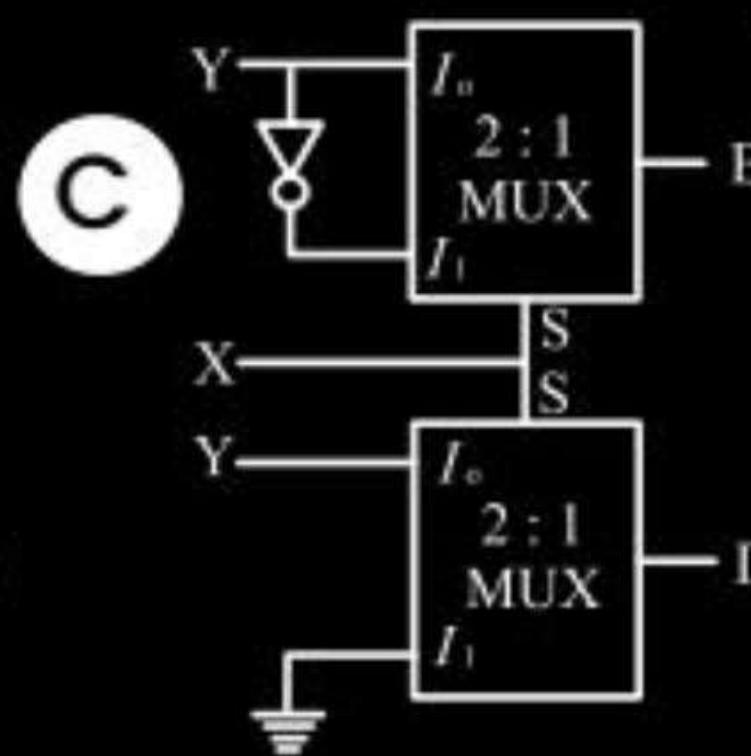
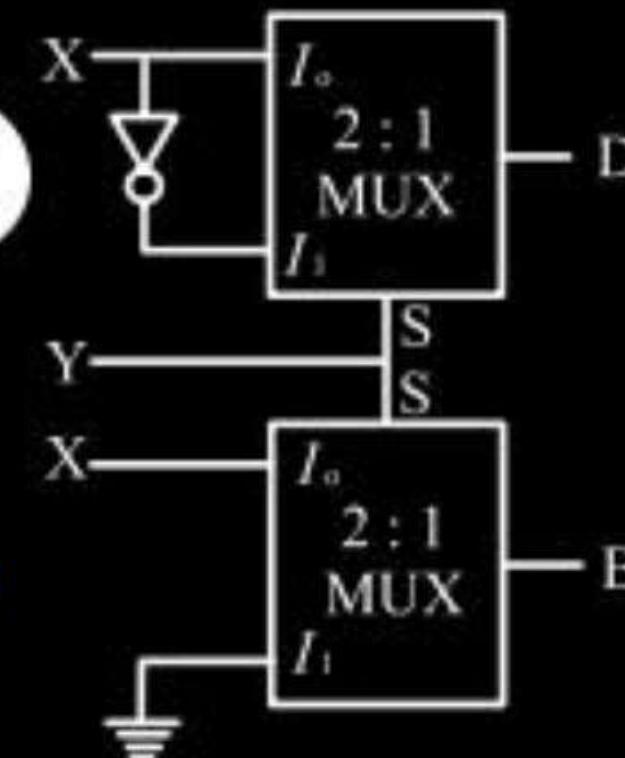
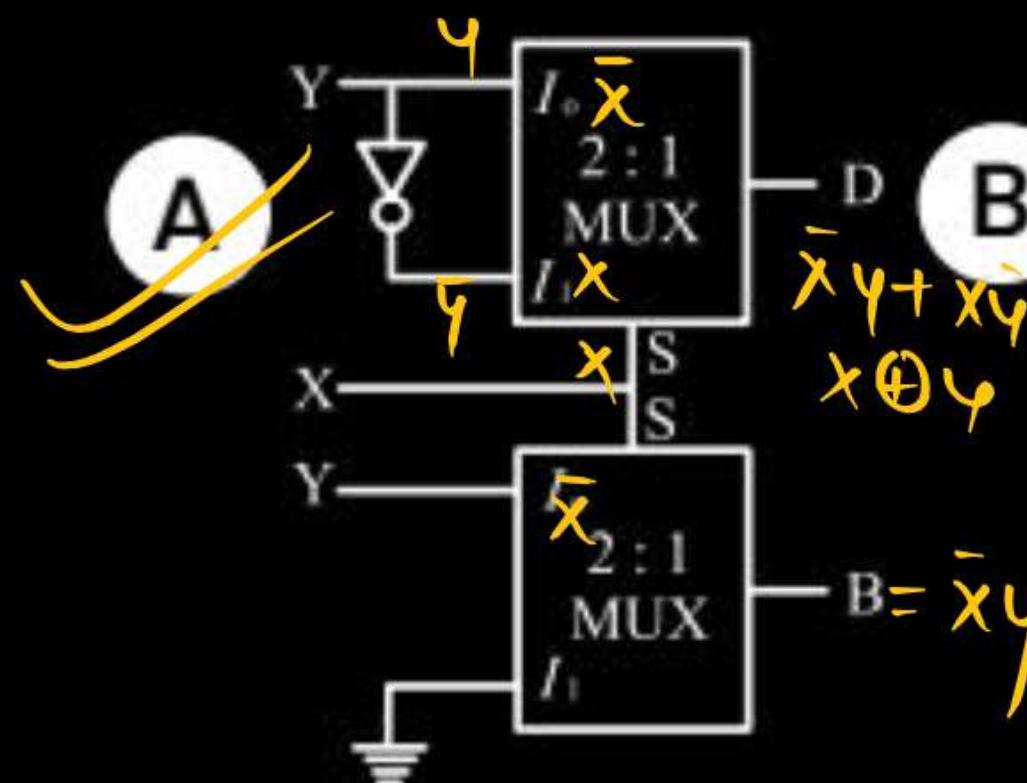
$$D = \bar{X}Y + X\bar{Y} = X \oplus Y$$

$$B = \bar{X}Y$$



If X and Y are inputs and the Difference(D=X-Y) and the Borrow(B) are the outputs, which one of the following diagrams implements a half-subtractor?

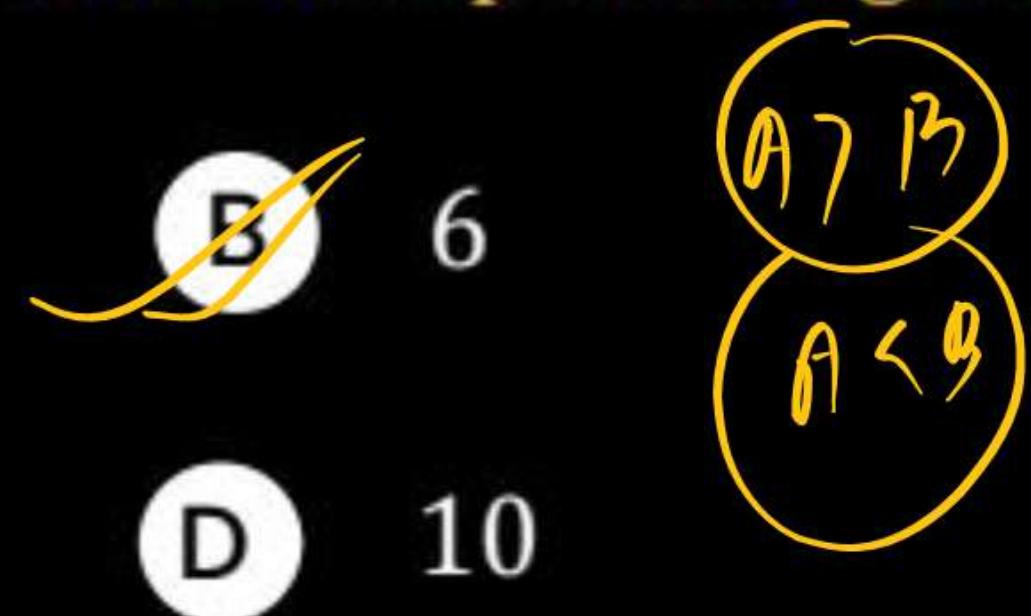
[GATE-2014-EC]



MCQ

The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is

- A 2
- C 8



[GATE-2014-EC]

$$\frac{2^{2n} - 2^n}{2}$$

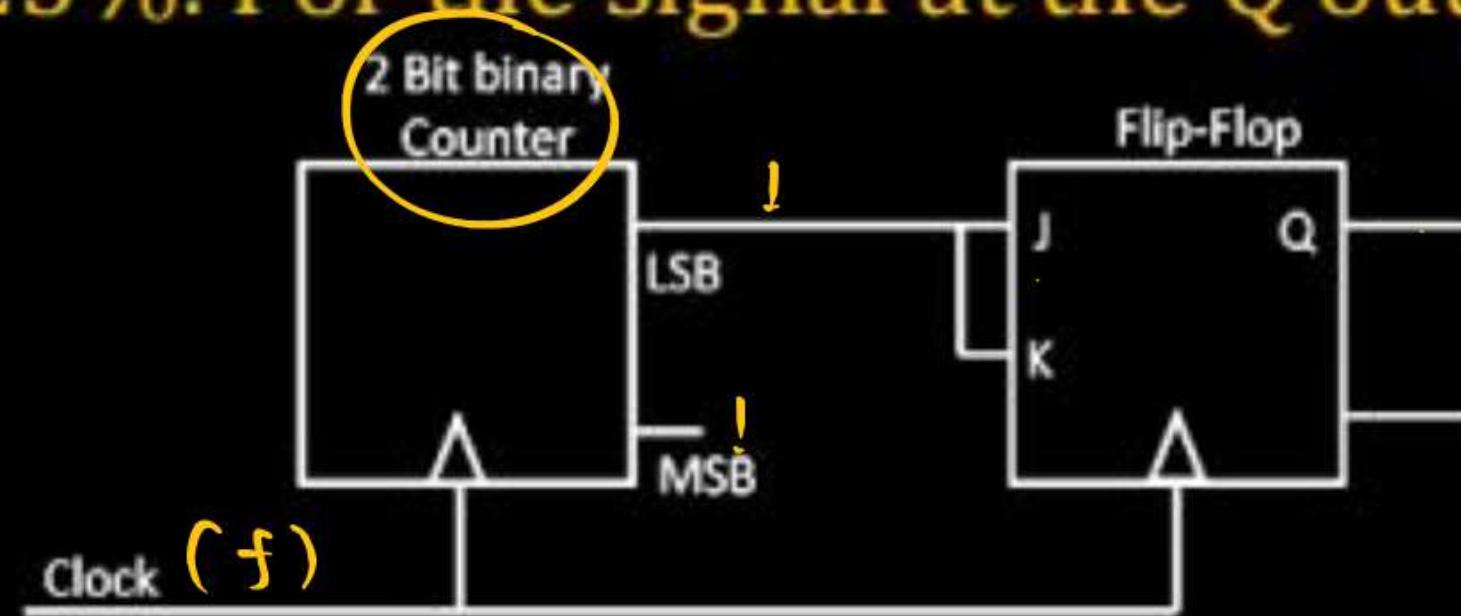


SEQUENTIAL CIRCUITS

MCQ

For the circuit shown, the clock frequency is f and the duty cycle is 25%. For the signal at the Q output of the Flip-Flop, _____.

[GATE-2022-EC]



$$T_{ON} = T_{OFF}$$

$$\mu = 50\%$$

$$\frac{T_{ON}}{T_{ON} + T_{OFF}}$$

A

frequency is $f_0/4$ and duty cycle is 50% ✓

B

frequency is $f_0/4$ and duty cycle is 25%

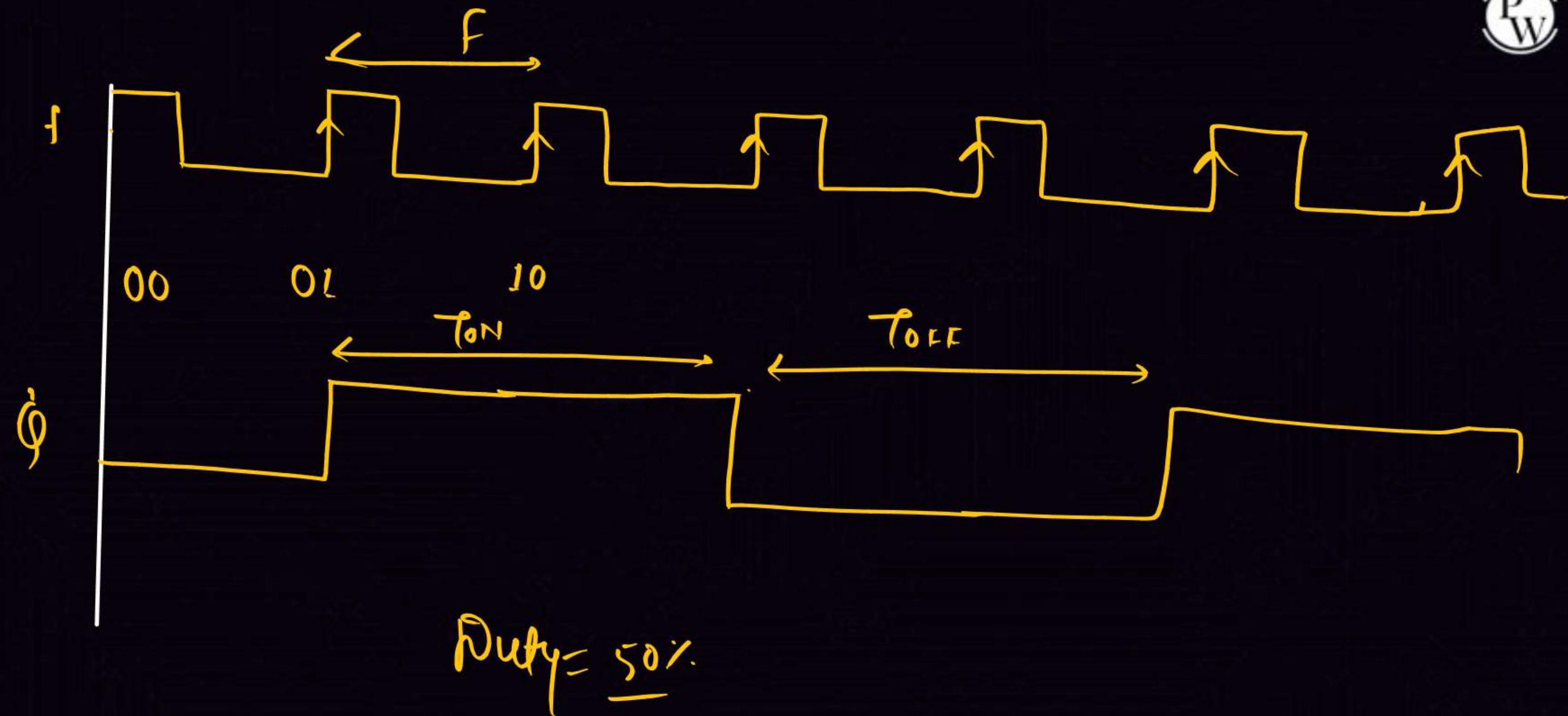
C

frequency is $f_0/2$ and duty cycle is 50% ✓

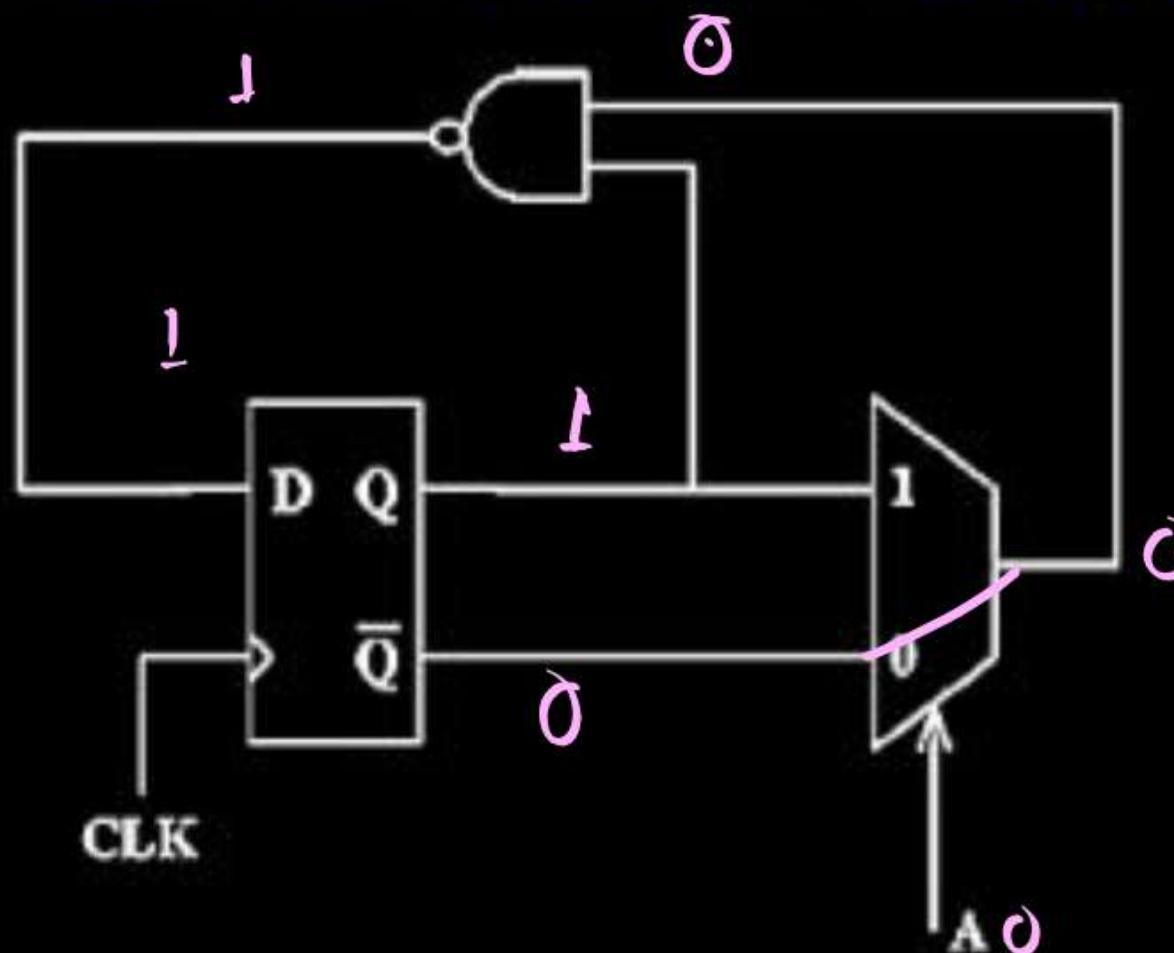
D

frequency is f_0 and duty cycle is 25%

P
W

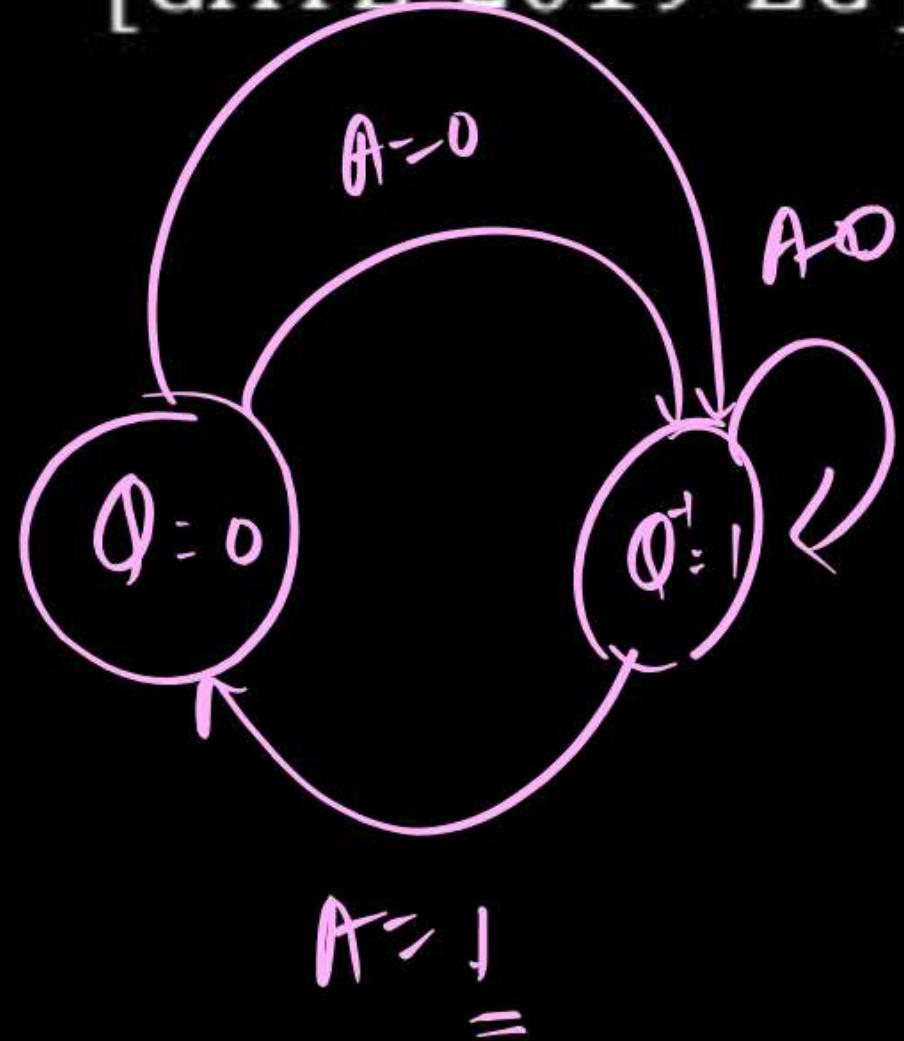


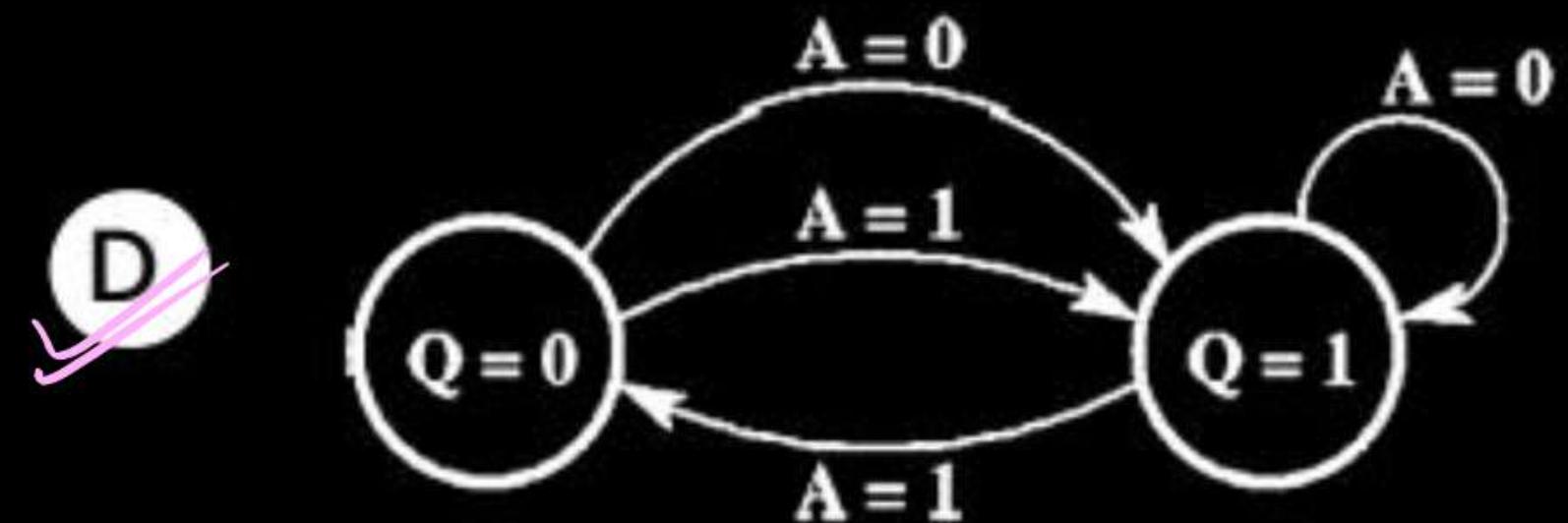
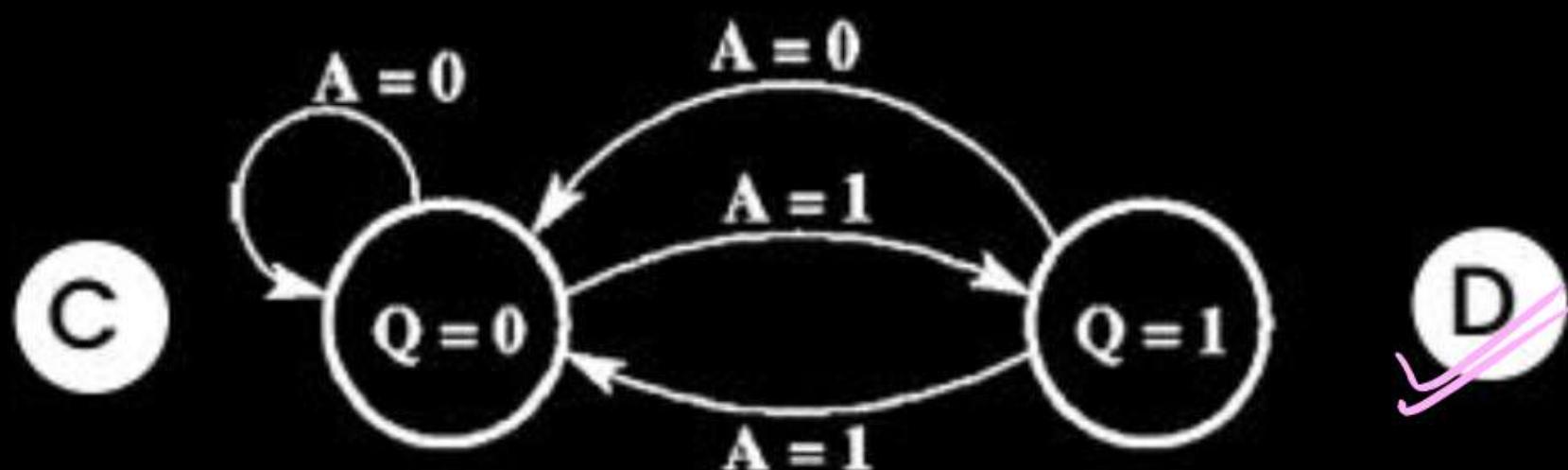
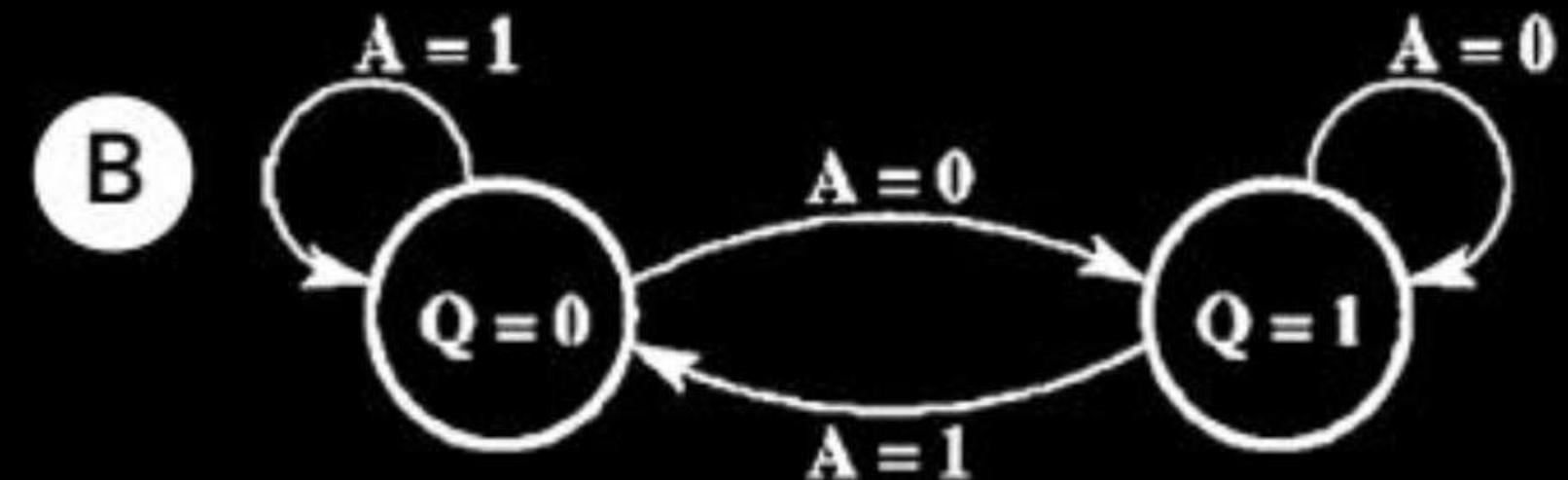
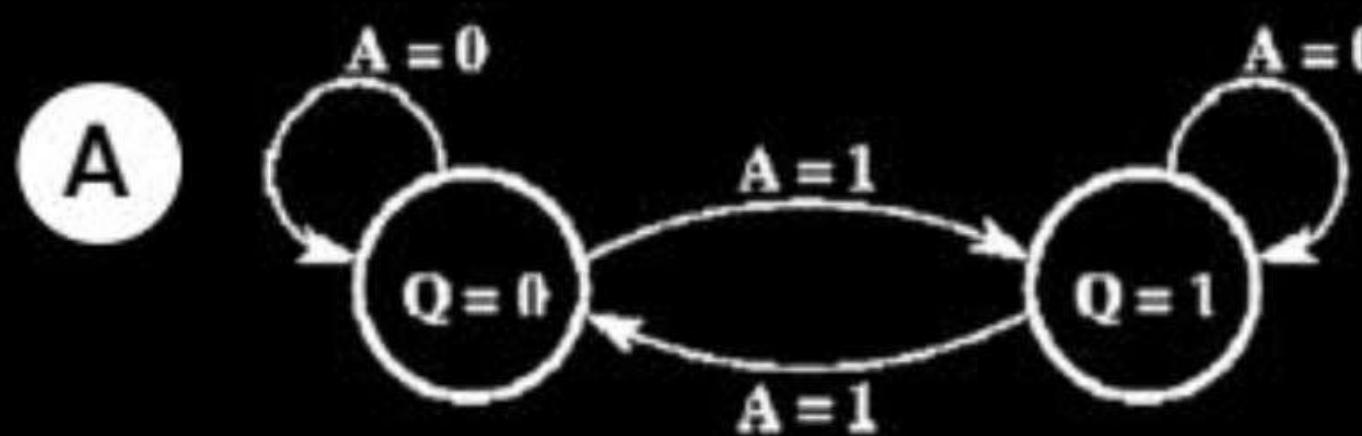
The state transition diagram for the circuit shown is



[GATE-~~2019~~-EC]

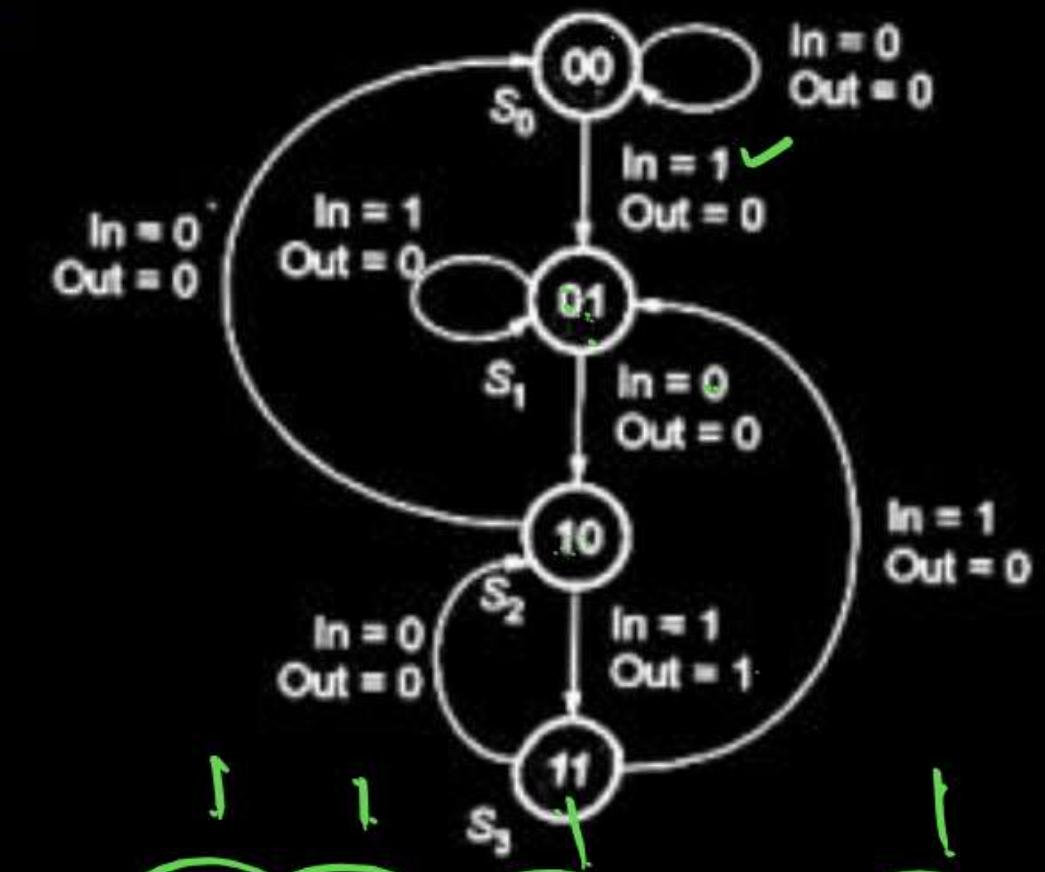
Q	A	Q^+
0	0	1
0	1	1
1	0	1
1	1	0





The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the figure. The FSM has an input 'In' and an output 'Out'. The initial state of the FSM is S_0 .

101 Detector
with overlapping

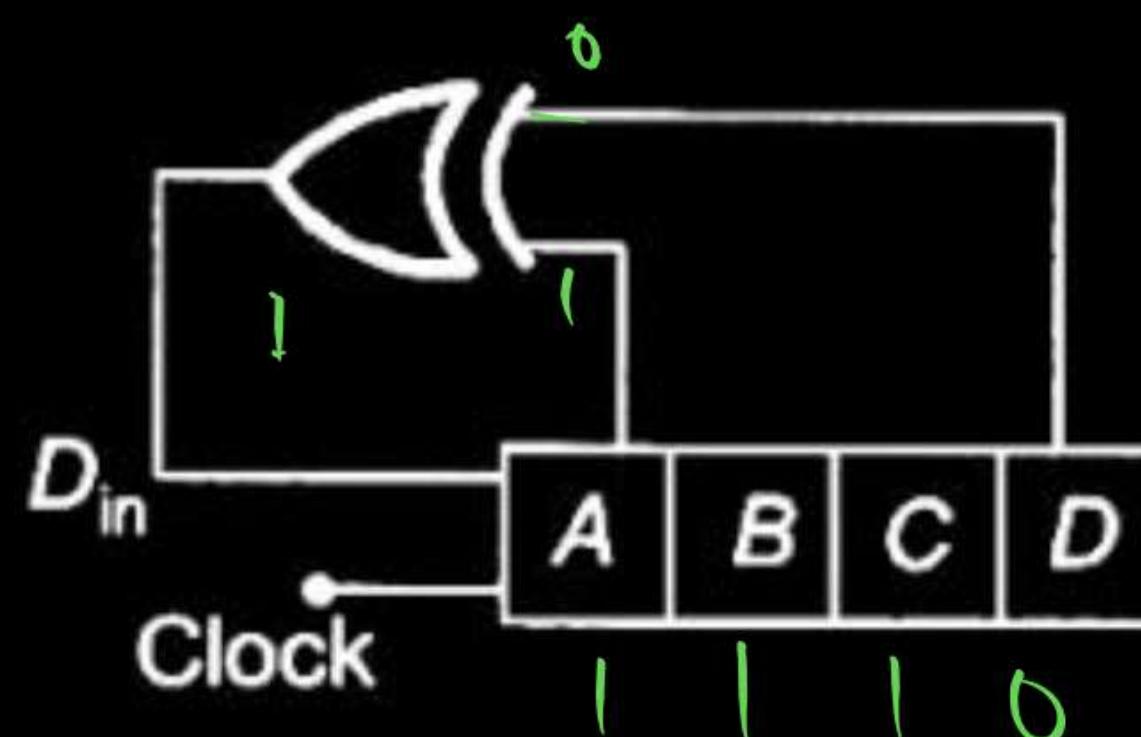


[GATE-2017-EC]

If the input sequence is 10101101001101 starting with the left-most bit, then the number of times 'Out' will be 1 is _____

4 Times o/p
will be high

A 4-bit shift register circuit configured for right-shift operation, i.e. $D_{in} \rightarrow A, A \rightarrow B, B \rightarrow C, C \rightarrow D$, is shown. If the present state of the shift register is $ABCD = 1101$, the number of clock cycles required to reach the state $ABCD = 1111$ is _____.



[GATE-2017-EC]

CLK	A	B	C	D
0	1	1	0	1
1	0	1	1	0
2	0	0	1	0
3	1	0	0	1
4	0	1	0	0
5	0	0	1	0
6	0	0	0	1

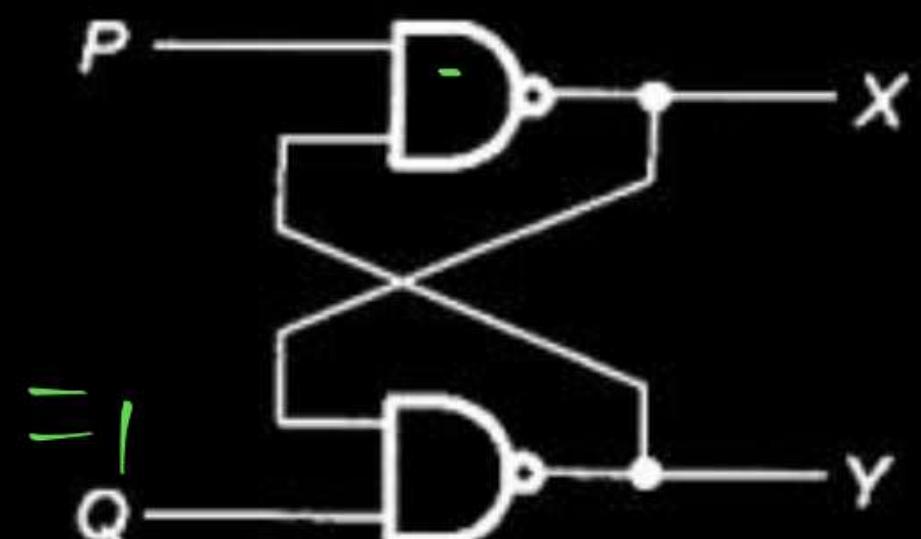
$7 \rightarrow 1100$
 $8 \rightarrow 1100$
 $9 \rightarrow 1110$
 $10 \rightarrow 1111$

MCQ

12. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is: $P = Q = '0'$. If the input condition is changed simultaneously to $P = Q = '1'$, the outputs X and Y are

[GATE-2017-EC]

- A $X = '1', Y = '1'$
- B \checkmark Either $X = '1', Y = '0'$ or $X = '0', Y = '1'$
- C either $X = '1', Y = '1'$ or $X = '0', Y = '0'$
- D $X = '0', Y = '0'$

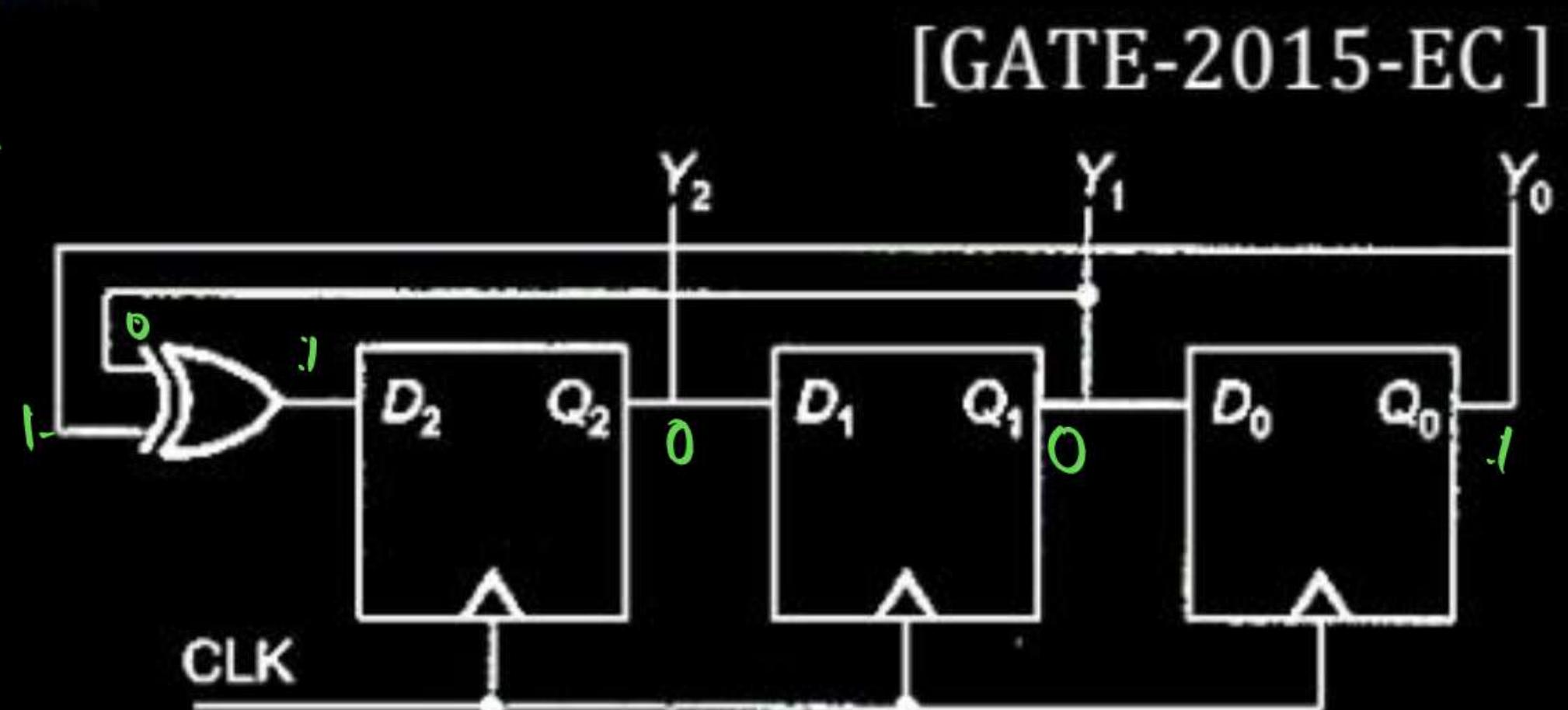


MCQ

A three-bit pseudo random number generator is shown. Initially the value of output $Y = Y_2 Y_1 Y_0$ is set to 111. The value of output Y after three clock cycles is

- A 000
- B 001
- C 010
- D 100

clk	Q ₂	Q ₁	Q ₀
0	1	1	1
1	0	1	1
2	0	0	1
3	0	0	0



MCQ

The figure shows a binary counter with synchronous clear input. With the decoding logic shown, the counter works as a

[GATE-2015-EC]

- A mod - 2 counter
- B mod - 4 counter
- C mod - $\overline{5}$ counter
- D mod - 6 counter

$$\begin{array}{c} Q_3 \quad Q_2 \quad Q_1 \quad Q_0 \\ \hline \end{array}$$

0 0 0 0

0 0 0 1

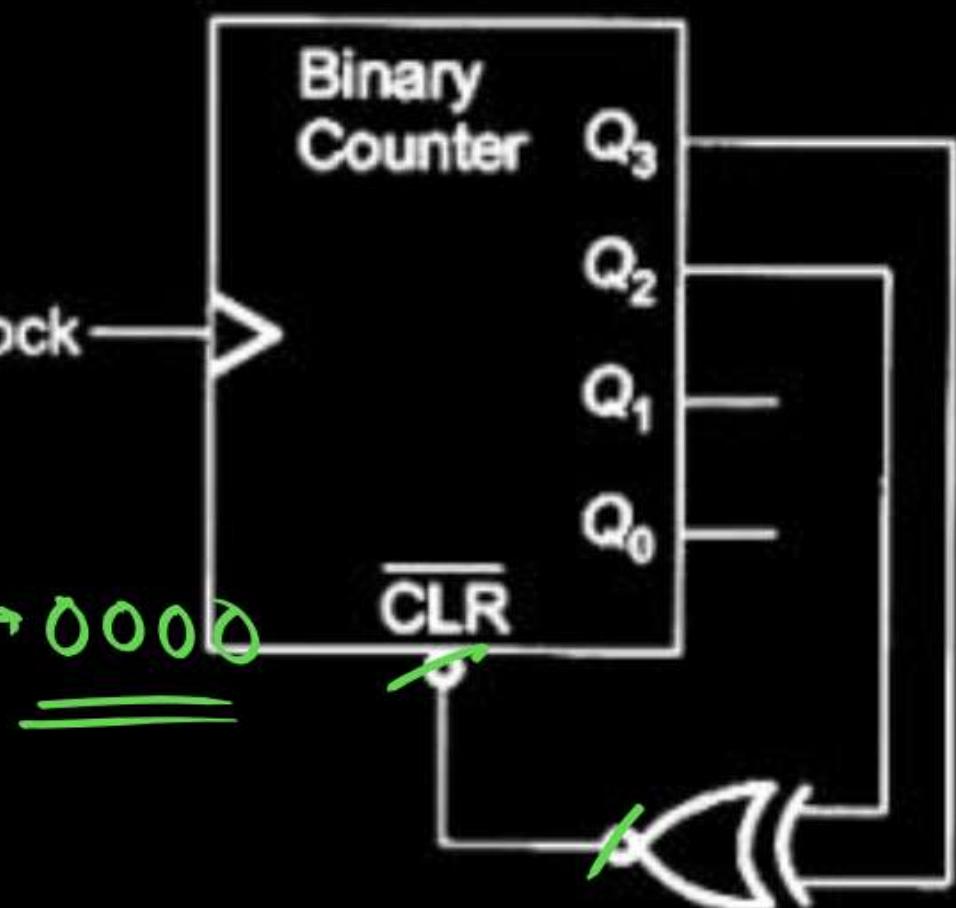
0 0 1 0

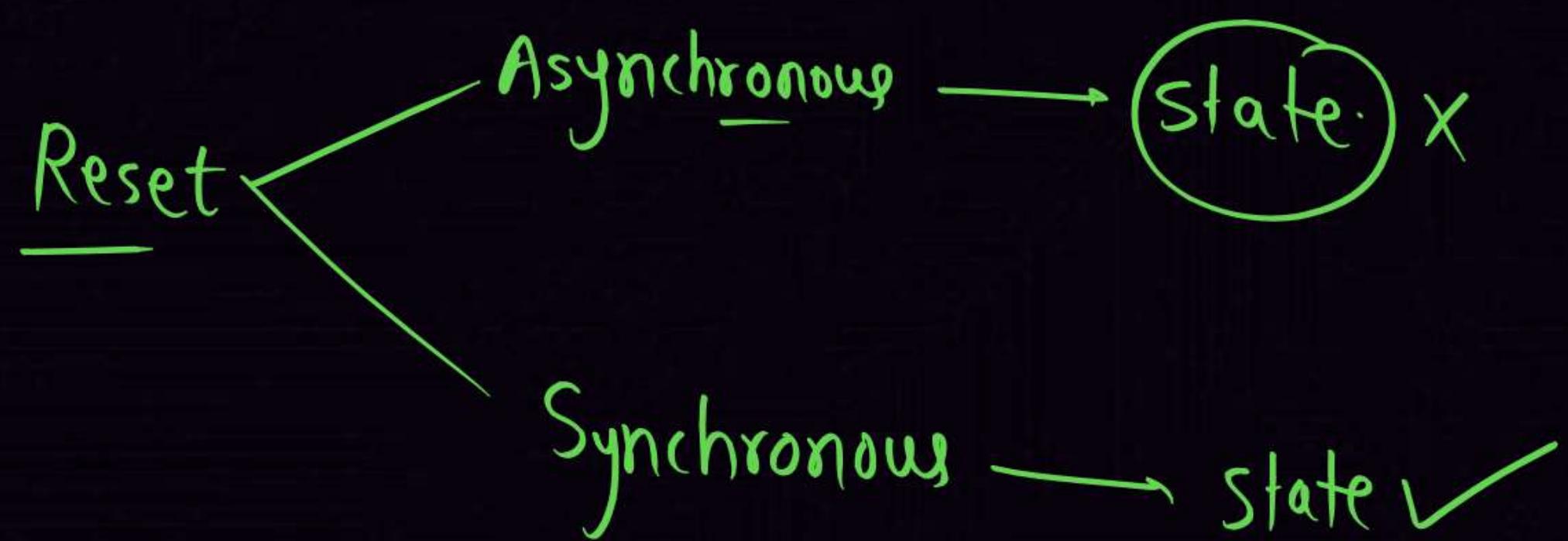
0 0 1 1

0 1 0 0

→ 0000

Clock





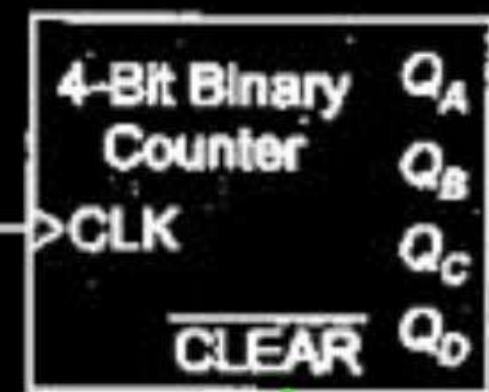
A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure. The value of n is

	Q_0	Q_1	Q_2	Q_3	Q_4
1	0	0	0	0	1
2	0	0	0	1	1
3	0	0	1	0	1
4	0	0	1	1	1
5	0	1	0	0	1
6	0	1	0	1	1
7	0	1	1	0	1
8	0	0	0	0	0

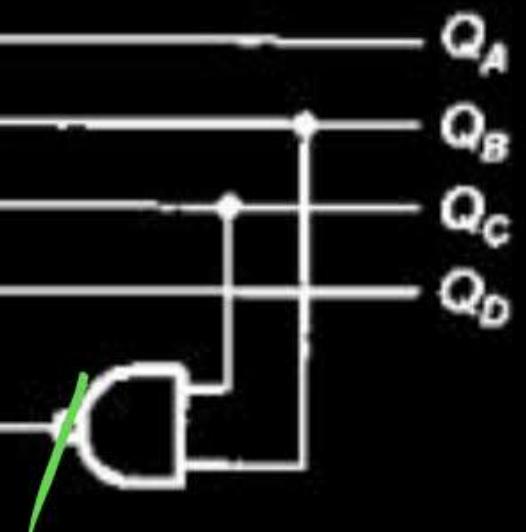
MOD-7

MOD-7

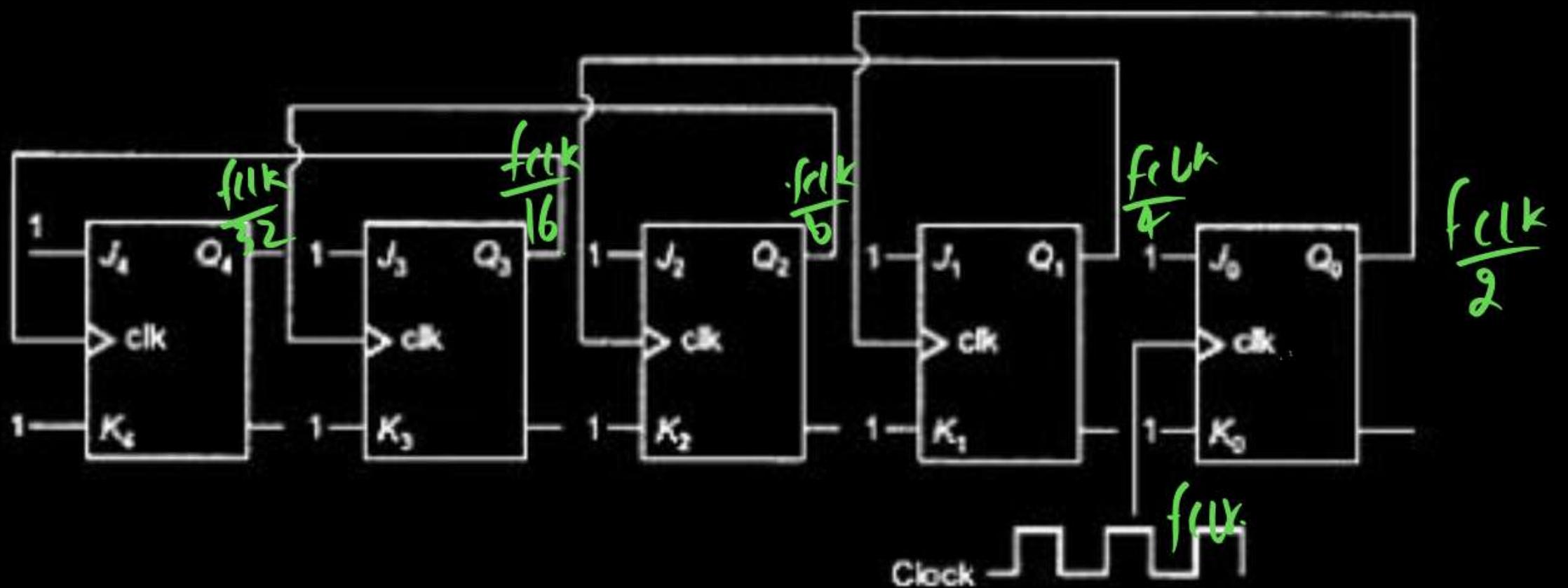
CLOCK



[GATE-2015-EC]



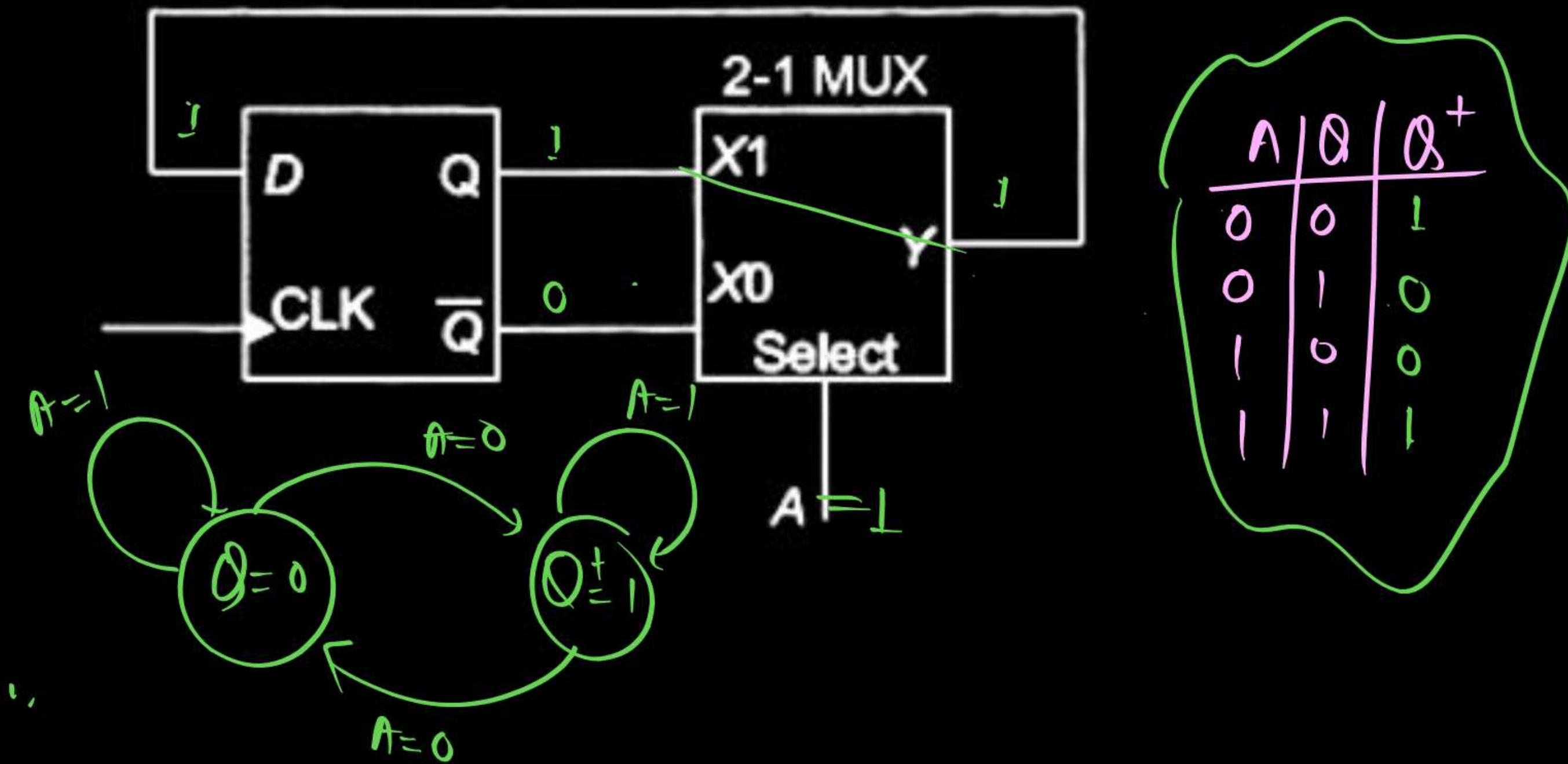
Five JK flip-flops are cascaded to form the circuit shown in Figure. Clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in kHz) of the waveform at Q_3 is

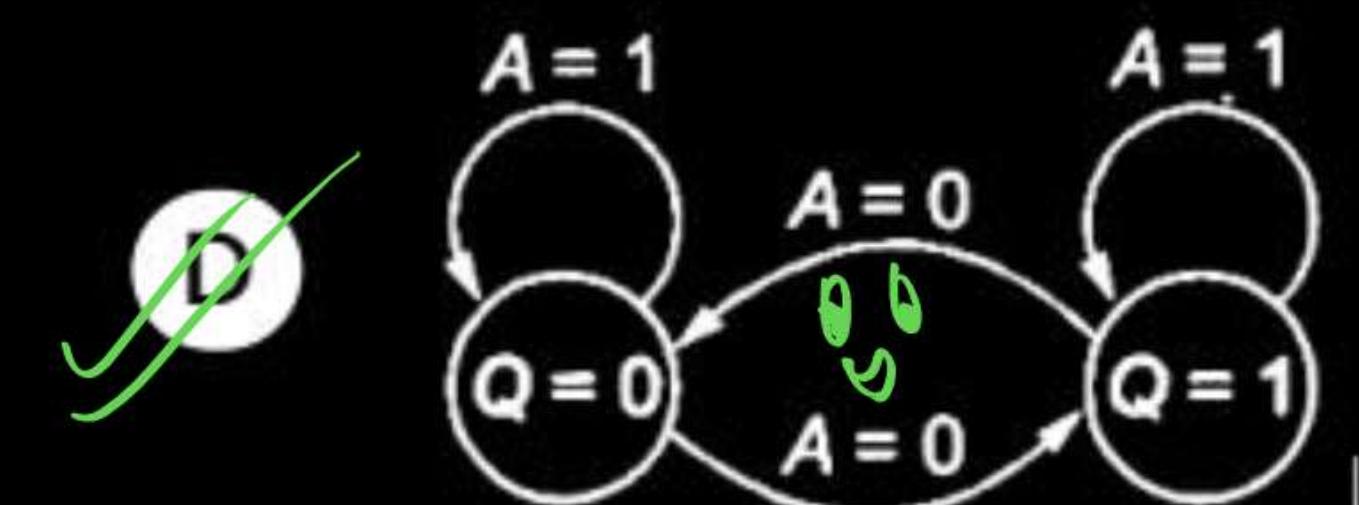
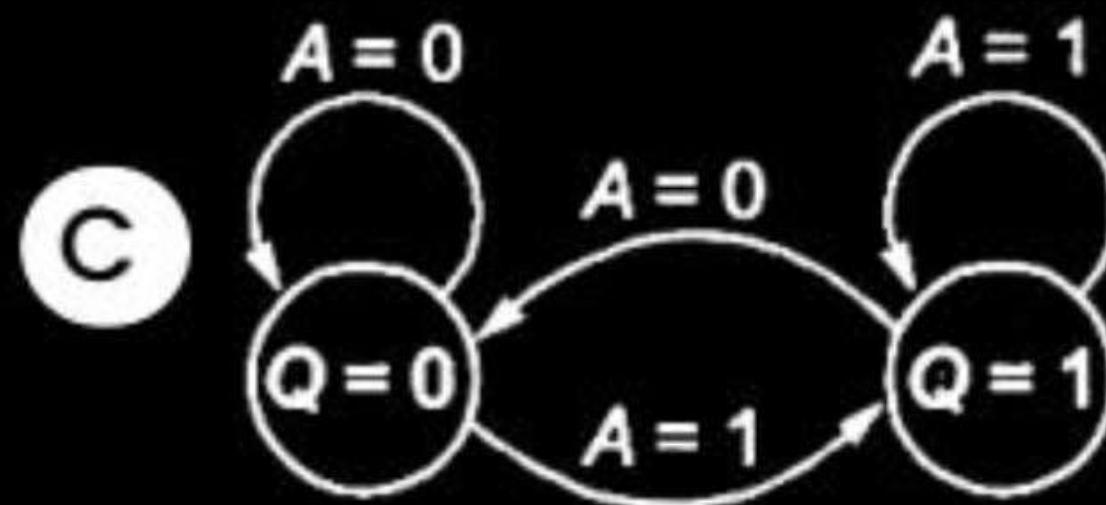
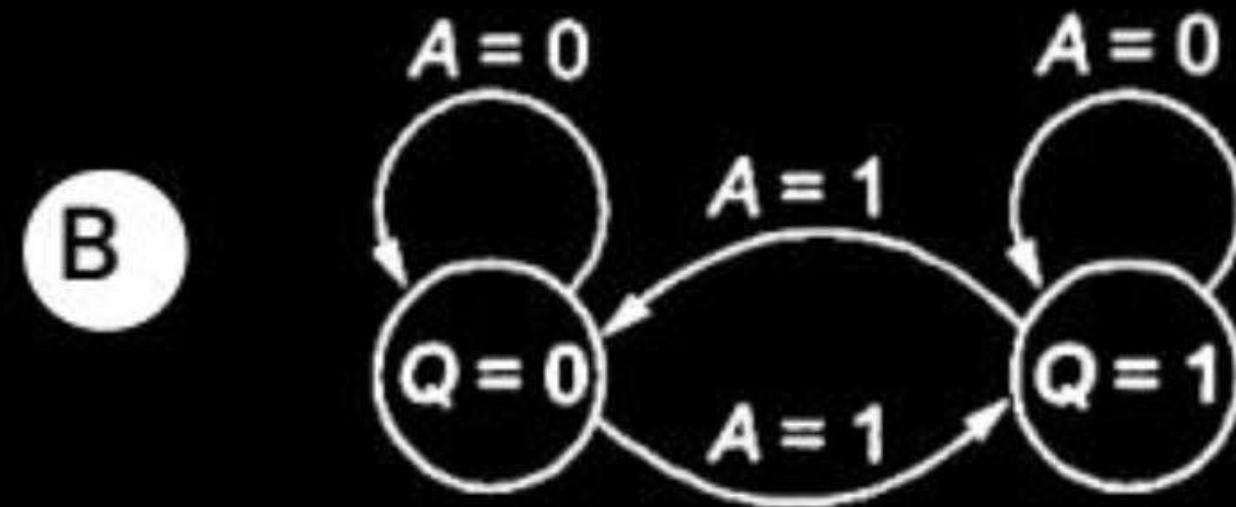
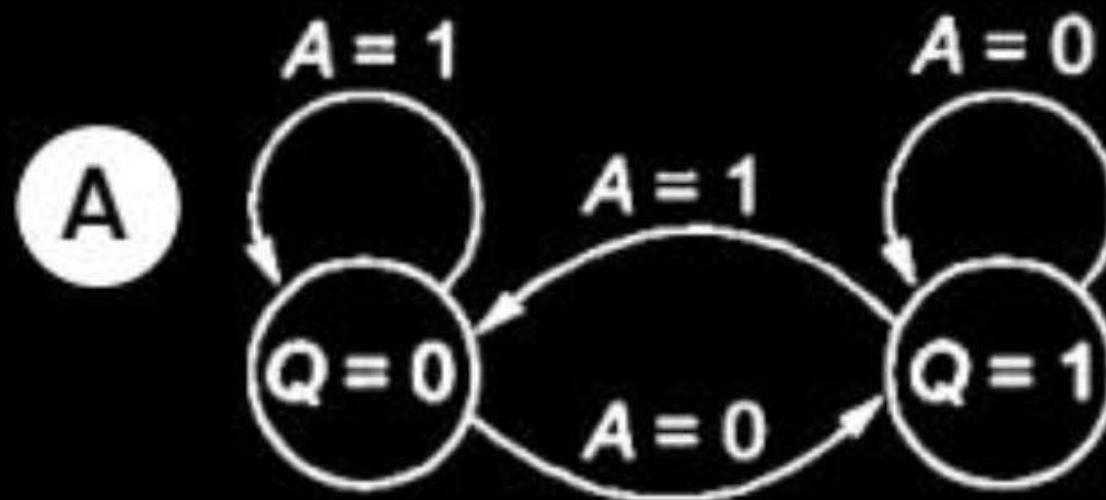


$$f_{Q_3} = \frac{f_{clk}}{16^5} = \frac{1000}{16^5} \text{ kHz}$$

The state transition diagram for the logic circuit shown in

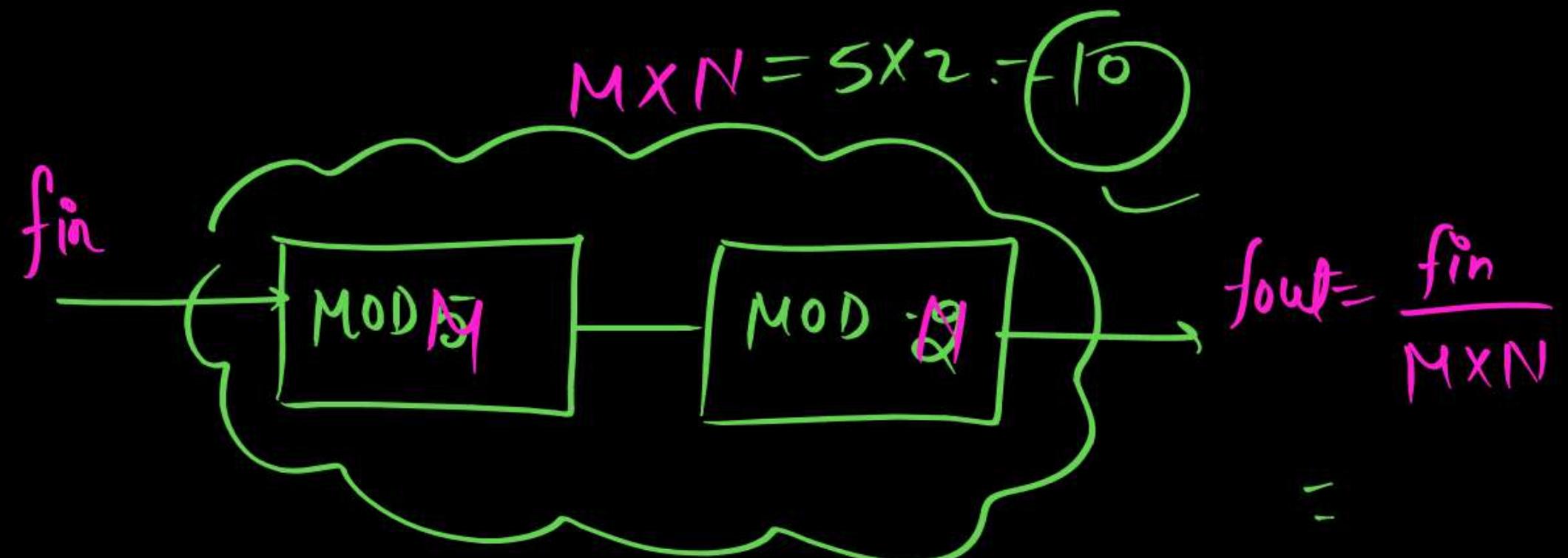
[GATE-2012-EC]





A MOD 2 and MOD 5 up-counter when cascaded together results in a MOD ____ counter. (in integer)

[GATE-2022-EE]



The maximum clock frequency in MHz of a **4-stage** ripple counter, utilizing flip-flops, with each flip-flop having a propagation delay of 20 ns, is __ (round off to one decimal place)

[GATE-**2022**-EE]

$$(f_{clk})_{max} = \frac{1}{n \cdot \tau_{pd,ff}}$$

n=4

$$\tau_{pd,ff} = 20 \times 10^{-9} \text{ s}$$

$$= \frac{1}{4 \times 20 \times 10^{-9}}$$

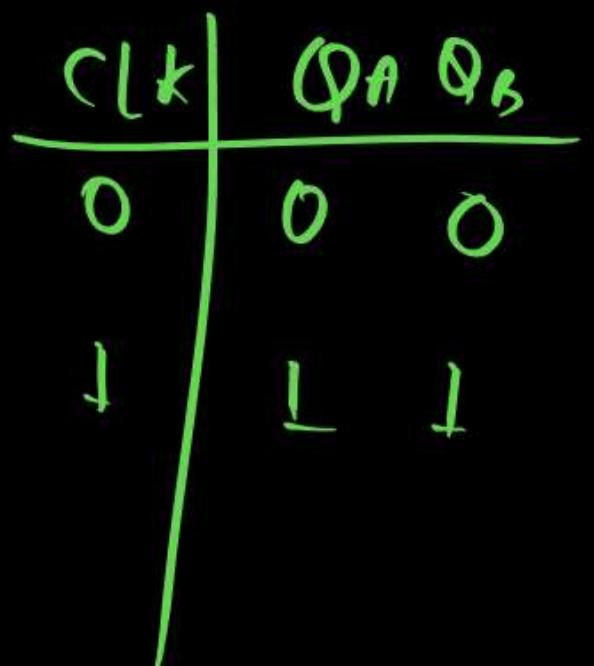
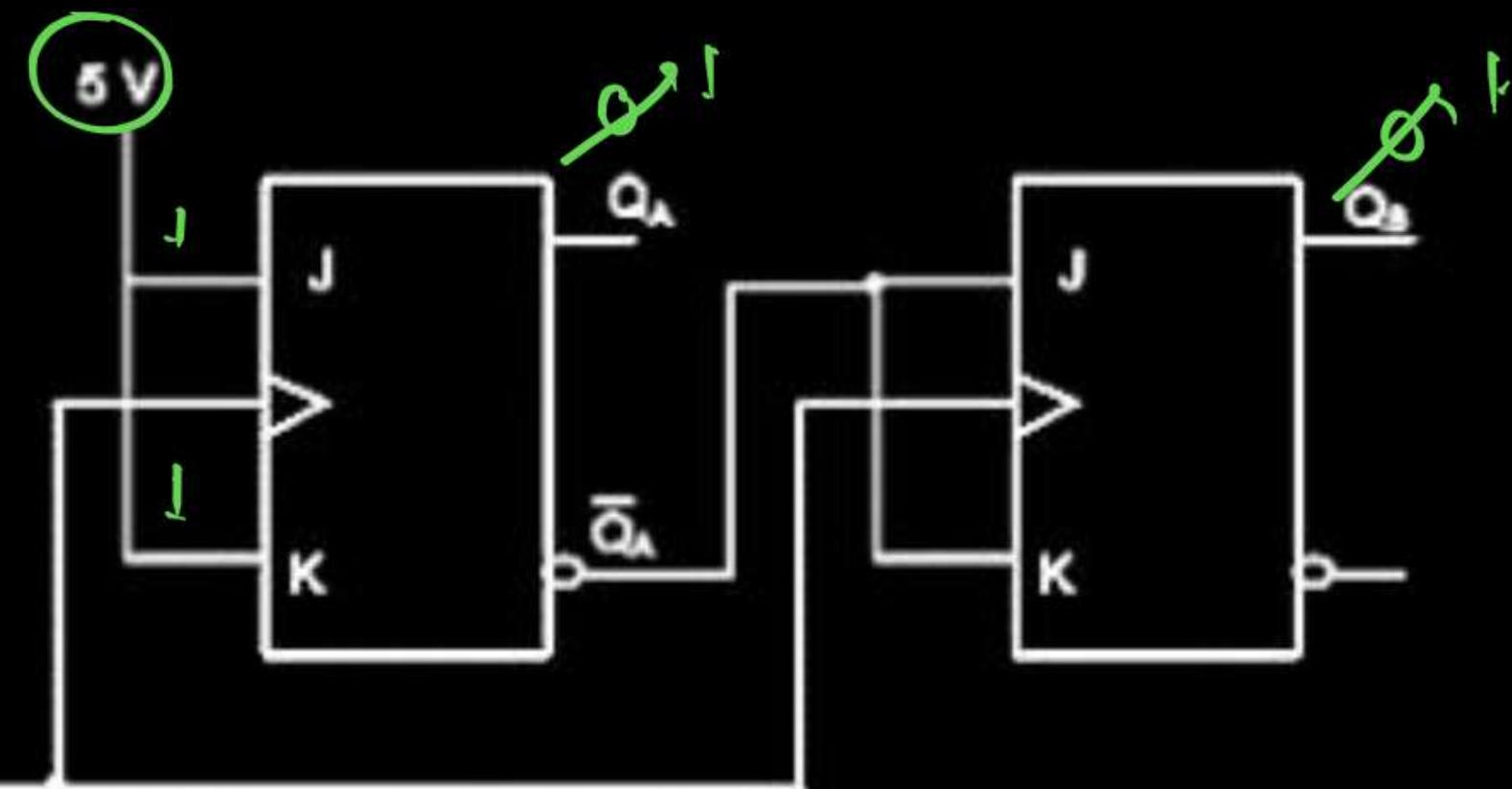
$$= \frac{25000 \times 10^6 \text{ Hz}}{4 \times 20}$$

$$(f_{clk})_{max} = 12.5 \text{ MHz}$$

The current state $Q_A Q_B$ of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of the system is

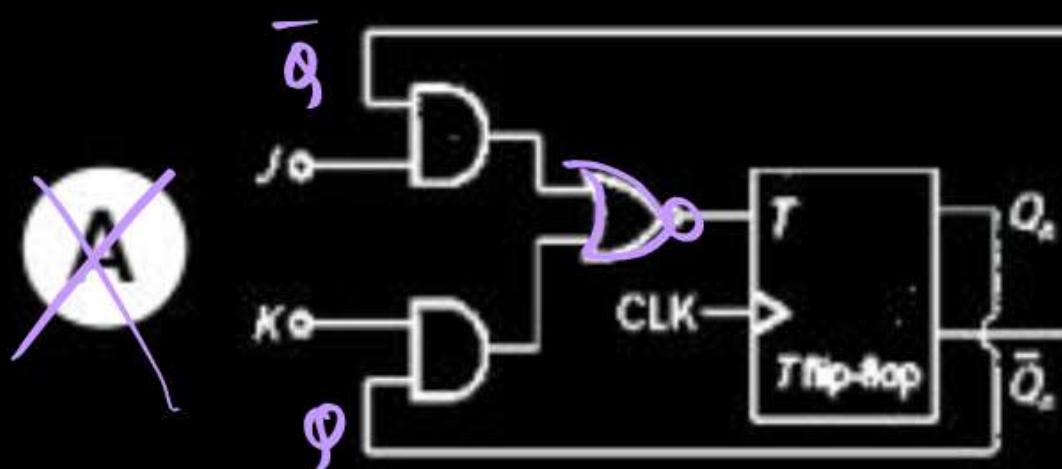
[GATE-2016-EE]

- A 00
- B 01
- C 11
- D 10



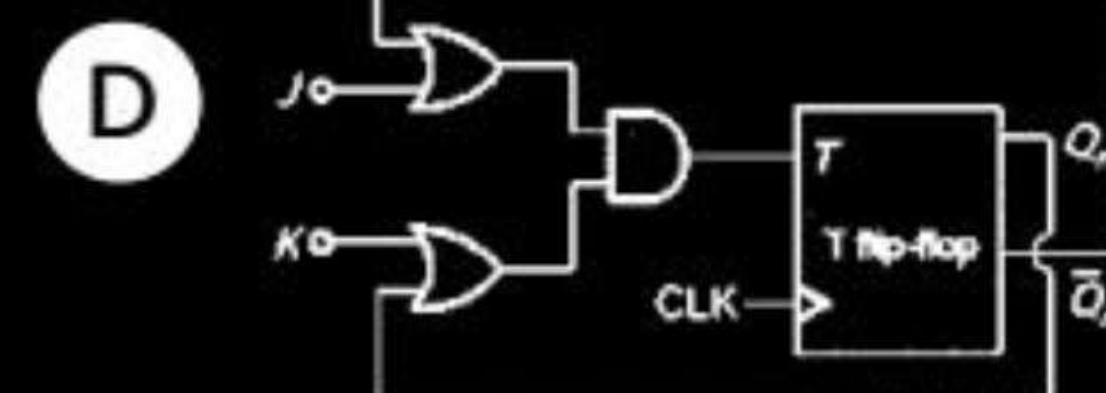
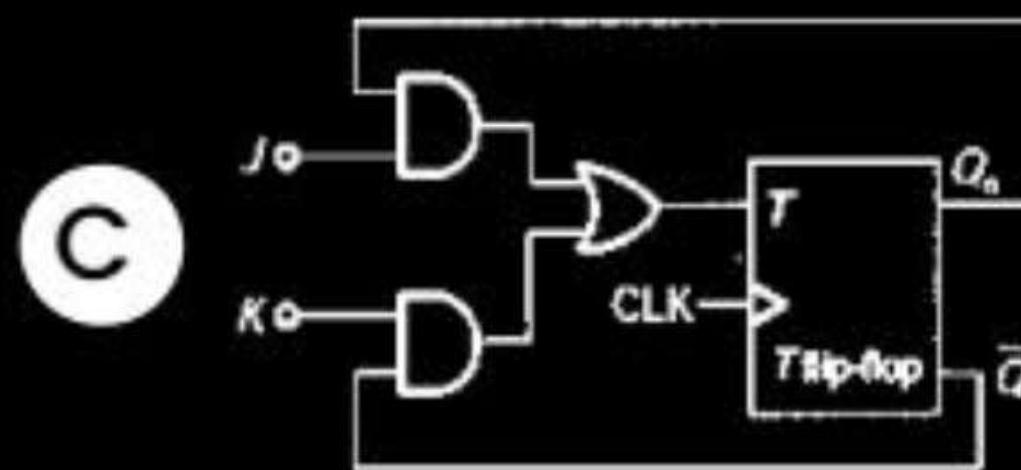
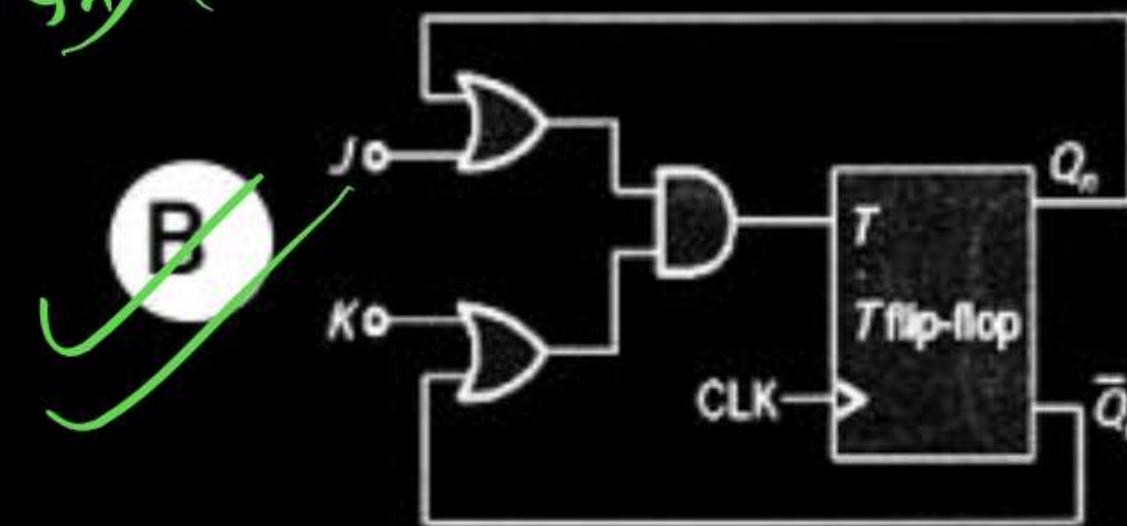
A JK flip-flop can be implemented by T flip-flops. Identify the correct implementation.

$$T = \overline{J} \bar{Q} + \overline{K} Q$$



$$T = (\overline{J} + Q_n) \cdot (\overline{K} + \bar{Q}_n)$$

[GATE-2014-EE]



JF-F
avalues

JK
Required

J	K	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

~~J \bar{Q}_n K \bar{Q}_n~~

\bar{J}	0	0	1	1	0
J	1	1	0	0	1
00	0	0	1	1	0
01	0	1	0	1	1
11	1	1	0	1	1
10	0	1	1	0	0

SOP

$$\bar{J} \bar{Q}_n + \bar{K} \bar{Q}_n = P$$

POS

$$T = (\bar{J} + Q_n) \cdot (\bar{K} + \bar{Q}_n)$$

A cascade of three identical modulo-5 counters has an overall modulus of.

[GATE-2014-EE]

- A 5
- C 125

$$\begin{array}{c} 5 \times 5 \times 5 \\ 25 \times 5 \\ \textcircled{125} \end{array}$$

- B 25
- D 625



ADC AND DAC

Consider a four-bit D to A converter. The analog value corresponding to a digital signal of values 0000 and 0001 are 0 V and 0.0625 V respectively. The analog value (in Volts) corresponding to the digital signal 1111 is _____.

[GATE-2015-EC]



THANK
You! ☺

