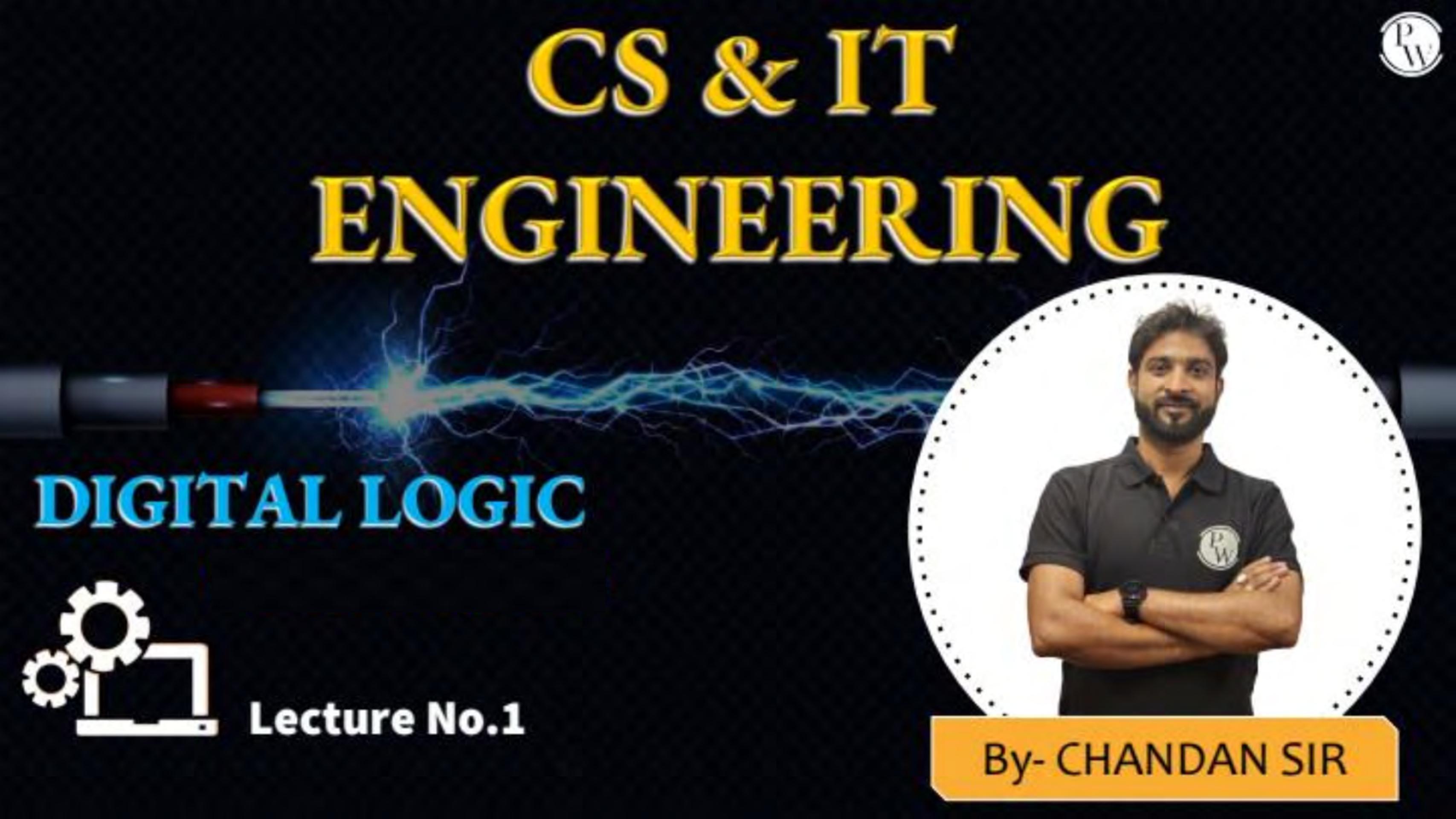


CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No.1



By- CHANDAN SIR

TOPICS TO BE COVERED

01 Question Practice

02 Discussion

#Q. The minimum value of y for which the given equation $2^{(21)y} = (11202)_y$ satisfy?



(MCQ)

- A 4
- B 3
- C 5
- D None of the above

Method ①

$$y > 2$$

$$2^{(2y+1)} = y^4 + y^3 + 2y^2 + 2$$

$$y=3 \checkmark$$

$$2^7 = 3^4 + 3^3 + 2 \cdot 3^2 + 2$$

Method 2.

$$2^{(21)}_y = (11202)_y$$

$$y > 2$$

$$(21)_y = \log_2 \{11202\}_y$$

$$2y+1 = \log_2 \{y^4 + y^3 + 2y^2 + 2\}$$

$$y=3$$

$$7 = \log_2 128$$

#Q. The given equation $(110)_6 = (x6)_y$ satisfy for unknown values of x and y, then the total possible solutions of given equation is ④ (NAT)

$$(110)_6 = (x6)_y$$

$y > 6$

$y > x$

$$1 \times 6^2 + 1 \times 6^1 + 0 \times 6^0 = xy + 6 \times y^0$$

$$36 + 6 = xy + 6$$

$$\boxed{xy = 36}$$

x	y
1	36 ✓ ✓
36	1 ✓ ✓
2	18 ✓ ✓
18	2 ✓ ✓
4	9 ✓ ✓
9	4 ✓ ✓
3	12 ✓ ✓
12	3 ✓ ✓
6	6

#Q. The minimum value of x and y for which the given equation

$$(4425)_x + (1750)_y = \frac{\log_2((40x+25y))^2}{\log_2 a} \text{ satisfy?}$$

- A X=6, y=8 ✓
- B X=6, y=9 ✓
- C X=7, y=9
- D X=7, y=8

$$\log_a b = \frac{\log b}{\log a}$$

$$(4425)_x + (1750)_y = \log_2 ((40_x + 25_y)^2)$$

$$(4425)_x + (1750)_y = \log_2^2 = 1$$

$$(40_x + 25_y)^2 = 1$$

$$(4425)_x + (1750)_y = [(40)_x + (25)_y]^2$$

$$x > 5$$

$$y > 7$$

$$4x^3 + 4x^2 + 2x + 5 + y^3 + 7y^2 + 5y = [4x + 2y + 5]^2$$

$$x = 6$$

$$y = 8$$

#Q. The solutions to the quadratic equation $x^2 - 11x + 22 = 0$ are $x = 3$ and $x = 6$. The base value of the numbers is _____. **(NAT)**

$$(x-3)(x-6) = x^2 - 9x + 18$$

$$(x^2 - 11x + 22)_b = (x^2 - 9x + 18)_{10}$$

$$(11)_b = (9)_{10}$$

$$b+1 = 9$$

$$b = 8$$

#Q. P, Q are the integers corresponding to the 4-bit binary number 1110 considered in 1's complement and 2's complement representations, respectively. The 5-bit 1's complement representation of (Q - P) is? **(MCQ)**

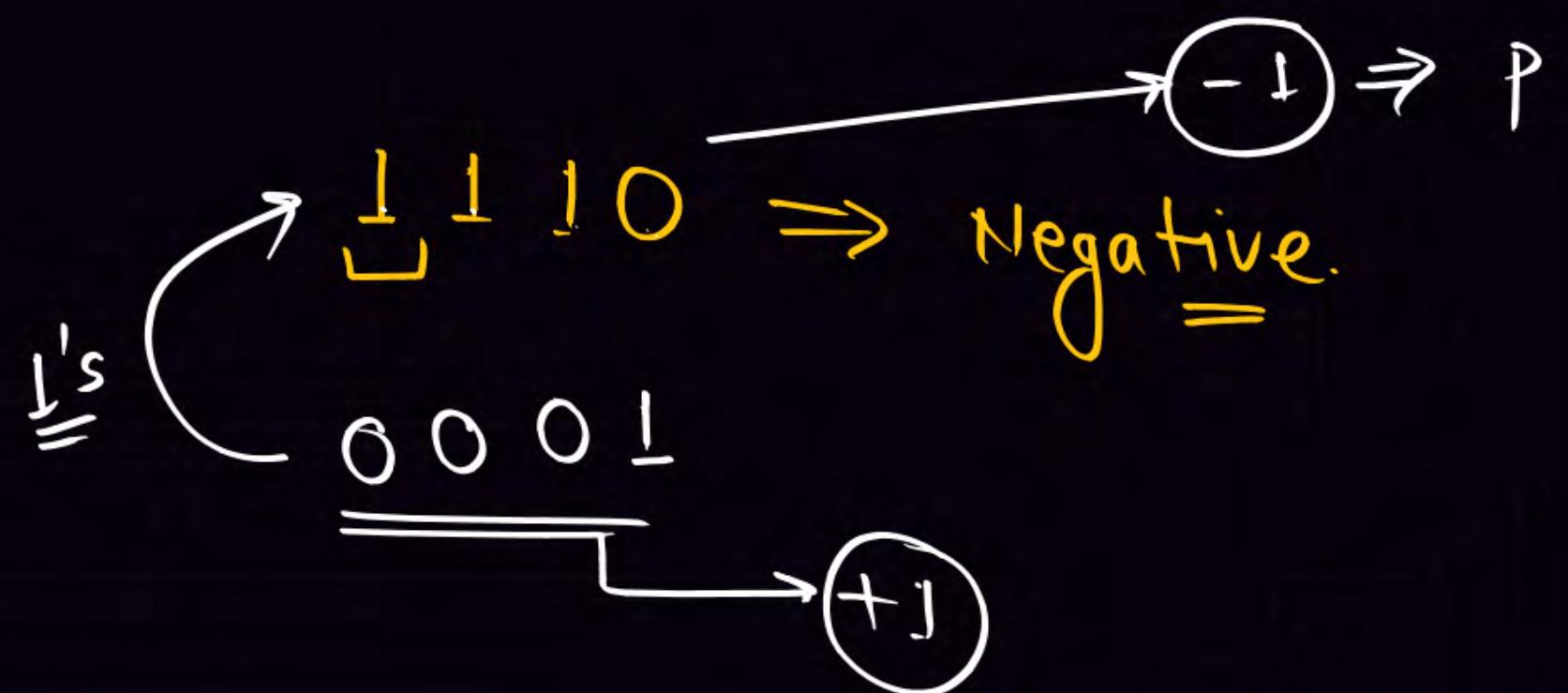
- A 11111
- B 11011
- C 11110
- D 11100

$$\begin{array}{r} \text{1110} \\ \underline{-\text{0001}} \\ \text{1110} \end{array} \Rightarrow \begin{array}{l} P = -1 \\ Q = -2 \end{array}$$

$$Q - P = -2 - (-1) = -1$$

00001

$$\underline{\text{11110}} \Rightarrow \text{-1}$$



$$P = -1 \quad Q = -2$$

$$Q - P = -2 - (-1) = -1$$

#Q. Consider the signed binary number $A = 01010110$ and $B = 11101100$ where B is the 1's complement and MSB is the sign bit, then the value of $-A - B$ in 2's complement format is $\underline{64+16+4+2}$

Method ①

$$\begin{array}{r} A = + \underline{86} \\ -A \text{ (1's complement)} \Rightarrow 10101001 \\ -B \\ \hline \end{array}$$
$$\begin{array}{r} \Rightarrow 00010011 \\ \hline 10111100 \\ +1 \end{array}$$

- [A] 10111100
- ~~[B] 10111101~~
- [C] 01000010
- [D] None of the above

No carry generated, hence number is negative & already written in 1's complement.

10111101

Method ②

$$A = +86$$

$$\begin{array}{r} B = \underline{1\ 1\ 1\ 0\ 1\ 1\ 0\ 0} \Rightarrow -19 \\ = \\ 0\ 0\ 0\ 1\ 0\ 0\ 1\ 1 \end{array}$$

$$B = -19$$

$$-A - B = -86 - (-19)$$

$$= -86 + 19$$

$$\begin{array}{r} -67 \\ \hline \end{array}$$

$$\begin{array}{r} 64\ 32\ 16\ 8\ 4\ 2\ 1 \\ 1\ 0\ 0\ 0\ 0\ 1\ 1 \\ \hline \end{array}$$

$$\begin{array}{r} + 67 = 01000011 \\ - 67 \Rightarrow \underline{10111101} \end{array}$$

#Q. Let P be the number of distinct 10-bit integers in 1's complement representation. Let Q be the number of distinct 10-bit integers in 2's complement representation. Then $P-Q$ in 5-bit 2's complement representation is,

A 00001

B 00011

C 11111

D None of the above

$$P = \underbrace{1's}_{\emptyset} - [2^{n-1}-1] + [2^{n-1}-1]$$

$$Q = \underbrace{2's}_{\emptyset} - [2^{n-1}] + [2^{n-1}-1]$$

$$P-Q = (-1) \quad \begin{matrix} \leftarrow \\ +1 \rightarrow 0000 \\ -1 \rightarrow 1111 \end{matrix}$$

#Q. Which of the following notations have same representation of +0 and -0?

- A ~~1's complement with radix of number being 2~~
- B ~~7's complement with radix of number being 8~~
- C ~~9's complement with radix of number being 10~~
- D ~~10's complement with radix of number being 10~~

$$2 \longrightarrow \frac{2^5}{-}$$

γ 's complement with Radix number being $\underline{\underline{\gamma}}$

#Q. The r's complement of an n-digit decimal number N in base r is defined for all values of N except for N=0. If the given number is $(143)_5$, then its 5's complement is $(X)_5$, then the value of X is $(302)_5$ **(NAT)**

Base r

r=2

r=4

r=5

$r-1$'s

1's

3's

4's

8's

2's

4's

5's

4's comp

5's comp

4 4 4

1 4 3

3 0 1

+1

(302)

5
RQ

$$\begin{array}{r} 444 \\ 143 \\ \hline 301 \\ + 1 \\ \hline 302 \end{array}$$

$y = 5$

$(5-1)$

$4's$

$5's$

#Q. From the 7 symbols (0-6), we can construct $P!$ different codes. The value of P is .



(NAT)

$$n \geq \log_2 M$$

$$M = 7$$

$$n \geq \log_2 7$$

$n \geq 2 \cdot \text{something}$

$$\boxed{n=3}$$

8 distinct symbol

x_1
x_2
x_3
x_4
x_5
x_6
x_7

$$8P_7 = 8! = P!$$

$$\boxed{P=8}$$

#Q. The number of digit '1' present in the binary representation of the number $(1199)_{12}$ is **(MCQ)**

A 7

B 8

C 10

D 12

$$(1199)_{12} = (1 \times 12^3 + 1 \times 12^2 + 9 \times 12 + 9)_{10} \\ = (1989)_{10}$$

$$(1989)_{10} = 1024 + 512 + 256 + 128 + 64 + 4 + 1 \\ = 2^{10} + 2^9 + 2^8 + 2^7 + 2^6 + 2^2 + 2^0$$

⊕ → L.

$$2^0 = 1$$

$$2^1 = 10$$

$$2^2 = 100$$

$$2^3 = 1000$$

$$2^4 = 10000$$

$$(17)_{10} = 10001$$

16+1

$$2^4 + 2^0 \rightarrow 2 \text{ times } \underline{1 \text{ present}}$$

Q
=

$$512 + 8 + 6 + 3 + 1$$

$$512 + 8 + 4 + 2 + 2 + 1 + 1$$

$$512 + 8 + 4 + 6$$

$$512 + 8 + 4 + 4 + 2$$

$$512 + 16 + 2$$

$$2^9 + 2^4 + 2^1$$

 $\xrightarrow{3 \rightarrow 1 \text{ present}}$

#Q. The two numbers represented in signed 2's complement form are
★ P=10010011 and Q=11100110. If Q is subtracted from P, the value
RW. obtained in signed magnitude form is

(MCQ)

- [A] 11010011
- [B] 10101101
- [C] 10101100
- [D] None of the above

#Q. Which of the following is/are correct?

★

W.W

- | A In a 5-digit representation of a number A, $(A)_{16} + F$'s complement of $A=16^5 - 1$ in decimal representation.
- | B The result of subtraction operation $(BA)_{16} - (AB)_{16}$ is $(F)_{16}$
- | C To avoid overflow condition in signed number n-bit addition, the result would require minimum $(n+1)$ bits.
- | D If a number 1000 on base y is equivalent to cube of binary number 11, then the value of y is 3.

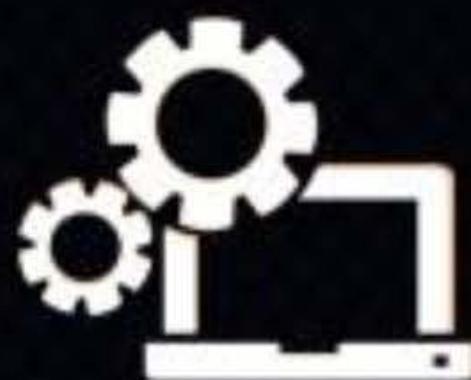


**Thank you
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CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No.2



By - CHANDAN SIR

TOPICS TO BE COVERED

- ... ► **01 Question Practice**
- ... ► **02 Discussion**
- ... ►

#Q. The two numbers represented in signed 2's complement form are P=10010011 and Q=11100110. If Q is subtracted from P, the value obtained in signed magnitude form is

(MCQ)

- A 11010011
- B 10101101
- C 10101100
- D None of the above

$$P - Q$$

$$P + (-Q)$$

$$Q = 11100110$$

$$-Q = 00011010$$

$$P = 10010011$$

$$-Q = 00011010$$

$$\begin{array}{r} 10010011 \\ - 00011010 \\ \hline 10101101 \end{array}$$

→ -ve

10101101

01010011
↓ signed bit

$$P = \underline{\underline{1}}0010011 = -109 \quad Q = \underline{\underline{1}}1100110 = -26$$

$$P - Q = -109 - (-26)$$

$$= -109 + 26$$

$$= -83$$

$$64 + 16 + 3$$

$$+ 83 \Rightarrow 01010011$$

$$- 83 \Rightarrow 11010011$$

#Q. Which of the following is/are correct?

(MSQ)

P
W

- A In a 5-digit representation of a number A, $(A)_{16} + F$'s complement of $A = 16^5 - 1$ in decimal representation.
- B The result of subtraction operation $(BA)_{16} - (AB)_{16}$ is $(F)_{16}$ ✓
- C To avoid overflow condition in signed number n-bit addition, the result would require minimum $(n+1)$ bits.
- D If a number 1000 on base y is equivalent to cube of binary number 11 , then the value of y is 3.

$$(1000)_2 = 3^3$$

$$\text{1's complement of } \underset{\uparrow}{A} = (2^n - 1)_2 - A$$

Three bit $A_2 A_1 A_0$

$$= (2^3 - 1)_2 - A_2 A_1 A_0$$

$$= (\underline{\underline{7}})_2 - A_2 A_1 A_0$$

$$= \begin{array}{c} 111 \\ \hline A_2 A_1 A_0 \end{array}$$

$$\text{F's complement} = (16^n - 1)_{16} - A$$

$$n=5 \quad = (16^5 - 1)_{16} - A_5 A_4 A_3 A_2 A_1$$

(NAT)P
W

#Q. Consider the following represented series,

$(2)_3, (3)_6, (12)_3, (12)_5, (14)_7, (111)_3 \dots\dots$, then the average value of first 10 number in decimal number system is ____.

$$(2)_3 = (2)_{10}$$

$$(3)_6 = (3)_{10}$$

$$(13)_3 = (5)_{10}$$

$$(12)_5 = (7)_{10}$$

$$(14)_7 = (11)_{10}$$

$$(111)_3 = (13)_{10}$$

$$\begin{aligned} & 2, 3, 5, 7, 11, 13, 17, 19, 23, 29 \\ & = \frac{2+3+5+7+11+13+17+19+23+29}{10} \\ & = 12.9 \quad \text{Ans} \end{aligned}$$

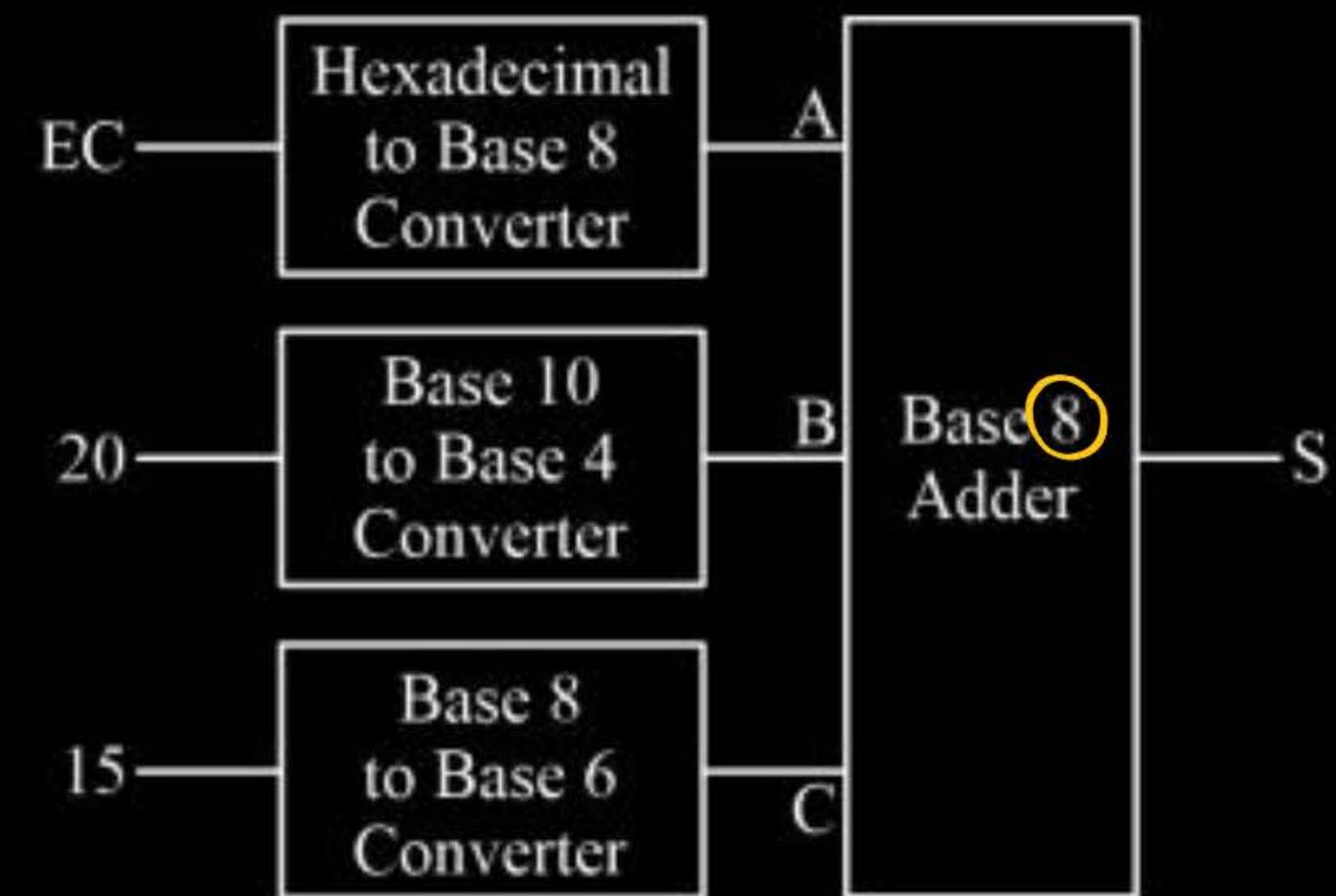
(MCQ)

#Q. Consider the circuit given below:

The output of each converter is given to adder which adds them considering octal number. The output of adder is S. The value of S is

_____.

- A** $(480)_8$ X
- B** $(548)_8$ X
- C** $(485)_8$ X
- D** $(505)_8$ ✓



$$(Ec)_{10} = \underbrace{0 \underline{1} \underline{1} 0}_{3 \ 5 \ 4} \quad \underbrace{1 \ \underline{0} \ 0} = (354)_8 = A$$

$$(20)_{10} = (110)_4 = B$$

$$(15)_8 = (13)_{10} = (21)_6 = C$$

1

3 5 4

1 1 0

$$\overline{(5 \ 0 \ 5)}_0$$

8 = 10

9 = 11

10 = 12

(MCQ)

#Q. Which one of the following is the correct summation of numbers (in base 2) represented in the series $(3)_4$, $(5)_6$, $(14)_5$, $(15)_6$?

- A** 11100
- B** 11001
- C** 11011
- D** 10101

$$(3)_4 = (3)_{10}$$

$$(5)_6 = (5)_{10}$$

$$(14)_5 = (9)_{10}$$

$$(15)_6 = (11)_{10}$$

$$(28)_{10} \Rightarrow \begin{array}{l} 1 \\ 1 \\ 1 \\ 0 \\ 0 \end{array}$$

(MCQ)

#Q. If p and q are successive numbers in a number system of base x such that $(pq)_x = (27)_9$ and $(qp)_x = (133)_4$, then

- A** $p=4, q=5$ and $x=7$
- B** $p=4, q=5$ and $x=6$ \times
- C** ~~$p=3, q=4$ and $x=7$~~
- D** $p=3, q=4$ and $x=6$ \times

$$P \qquad q = P+1$$
$$(P q)_x = (27)_9$$

$$Px + q = 25$$

$$Px + P+1 = 25$$

$$Px + P = 24$$

$$3P = 24 \qquad \textcircled{P=3}$$

$$P(x+1) = 24$$

$$qx + P = 31$$

$$(P+1)x + P = 31$$

$$Px + x + P = 31$$

$$(Px + P) + x = 31$$

$$24 + x = 31$$

$$x = 31 - 24 = 7$$

(NAT)

#Q. If $x = (4.4)_5$ and $y = (3.3)_5$, then $x + y = (a)_5$. The subscript 5 denotes the base on which the corresponding number is expressed. Then the value of a is ____.

$$\begin{array}{r} 1 \\ 4 \cdot 4 \\ \underline{-} 3 \cdot 3 \\ \hline 13 \cdot 2 \\ \hline \end{array}$$

$$\begin{array}{r} 5 = 10 \\ 6 = 11 \\ 7 = 12 \\ 8 = 13 \\ 9 = 14 \end{array}$$

$$\begin{array}{r} 1 \\ 4 \cdot 4 \\ \underline{-} 4 \cdot 1 \\ \hline 14 \cdot 0 \\ \hline \end{array}$$

9 →

$$\begin{array}{r} 1 \ 1 \ 1 \\ (3 + 2 \cdot 3)_8 \\ (1 + 6 \cdot 5)_8 \\ \hline (5 + 1 \cdot 0) \\ 8 \text{ Ans} \end{array}$$

)

7 → 7
8 = 10
9 = 11
10 = 12
11 = 13
12 = 14

(MSQ) ✓

#Q. Consider the following equation,

$$\left(\frac{422}{21.1}\right)_x = 20$$

The base value which can satisfy the above equation is ____.

A Base=4**B** Base =6 ✓**C** Base =7 ✓**D** Any base value ≥ 4

$$\frac{(422)_x}{(21.1)_x} = (20)_x \quad x > 4$$

$$\frac{4x^2 + 2x + 2}{2x+1+x^{-1}} = 2x \Rightarrow 4x^2 + 2x + 2 = 2x^2 + 2x + 2$$
$$\Rightarrow 4x^2 + 2x + 2 = 4x^2 + 2x + 2$$

Satisfy for all value of x

(MCQ)

#Q. Find the result in 2's complement form of the following
 $(1211)_4 + (1121)_3$

- A 010010000
- B 111100000
- C 011110000
- D 001110000

$$(1211)_4 = 4^3 + 2 \times 16 + 4 + 1 = 101$$

$$(1121)_3 = 3^3 + 9 + 6 + 1 = 43$$

$$(144)_{10} = 10010000$$

$$= 01001000$$

#Q. Consider the following multiplication operation of unsigned binary numbers. $(110X) \times (1Y01) = (Z110101)_2$. The appropriate values of X, Y and Z are

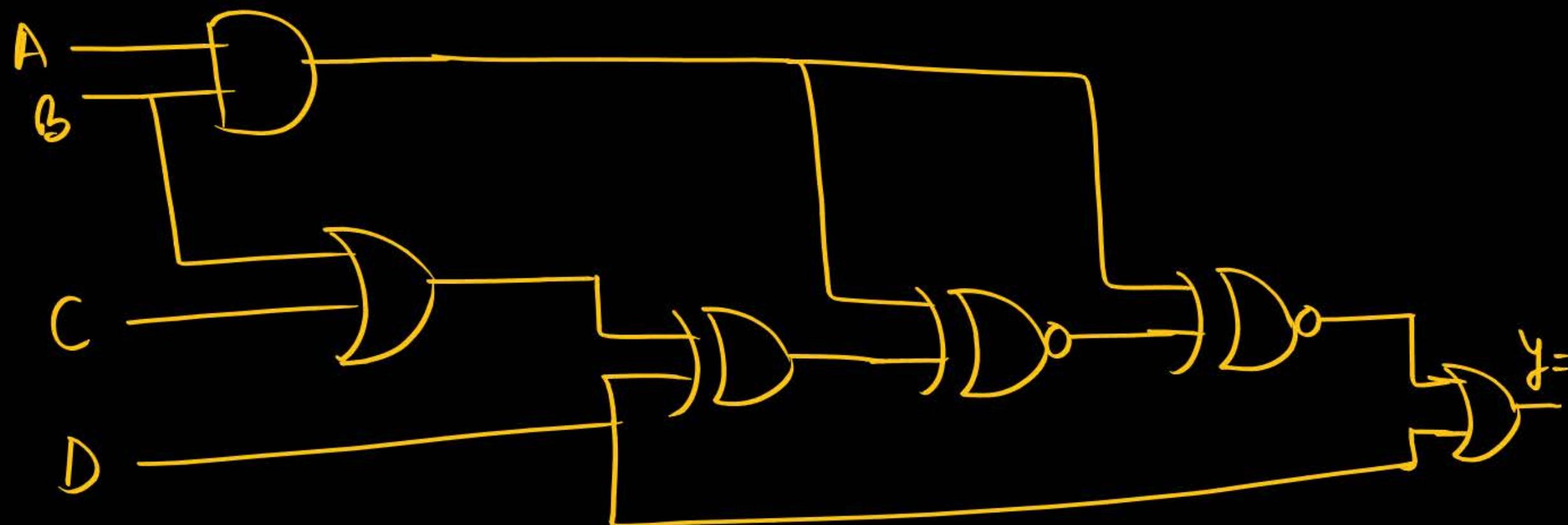
HW

- A** X = 0, Y = 1 and Z = 1
- B** X = 1, Y = 0 and Z = 1
- C** X = 1, Y = 0 and Z = 0
- D** X = 0, Y = 0 and Z = 1

Summary

↳ What is the value of y ?

#Q :



$$2) T_{AND}/T_{OR} = 5 \mu s$$

$$T_{X-OR}/T_{X-NOR} = 10 \mu s$$

Find Maximum & minimum delay to get output
if all input is applied at $t=0$

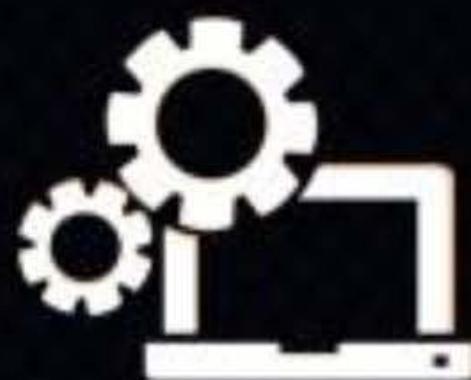


Thank you
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CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No.3



By - CHANDAN SIR

Recap of Previous Lecture



Number system

- ↳ Base conversion
- ↳ Magnitude Representation

Topics to be Covered



Logic Gates

Questions Practice

#Q. Consider the following function f,

$$f = A \oplus B \oplus \overline{AB}$$

The number of 2 input NAND gate to implement the minimized function f is ____.

$$f = (A \oplus B) \oplus \overline{AB}$$

$$f = (\overline{A \oplus B}) \cdot \overline{AB} + (A \oplus B) \overline{\overline{AB}}$$

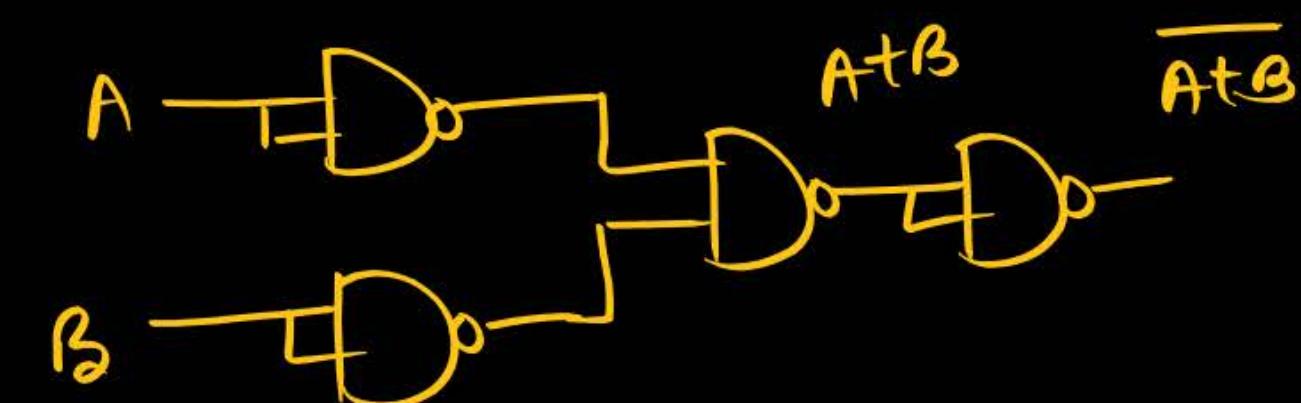
$$= (A \oplus B)(\overline{A} + \overline{B}) + (A \oplus B)AB$$

$$= (\overline{A}\overline{B} + AB)(\overline{A} + \overline{B}) + (\overline{A}B + A\overline{B})AB$$

$$= \overline{A}\overline{B} + \overline{A}\overline{B} + 0 + 0$$

$$= \overline{A}\overline{B} = \overline{A+B}$$

$\overline{A+B} \rightarrow \text{NOR GATE}$



$\bar{A}\bar{B}$

$$n=2 \quad k=2$$

Short trick

$$\text{NAND} = (2n-2) + k$$

$$= (2 \times 2 - 2) + 2$$

$$= 4$$

NOTE ①

$$A \oplus B \oplus AB = A + B$$

$$A \oplus B \oplus C \oplus ABC = A + B + C$$

$$A \oplus B \oplus \overline{AB} = \overline{A+B}$$

$$A \oplus B \oplus C \oplus \overline{ABC} = \overline{A+B+C}$$

NOTE

② $f = \bar{A} \cdot \bar{B} \cdot C \cdot \bar{D} \cdot \bar{E} \cdot F \cdot \bar{G} \dots$

$n \rightarrow$ Total number of Variables

$k \rightarrow$ Total number of complement Variable

Minimum number of NAND

$$= (2n-2) + k$$

Minimum number of NOR

$$= (3n-3) - k$$

NOTE

③ $f = \bar{A} + \bar{B} + C + \bar{D} + \bar{E} + F + \bar{G} + : + - + .$

$n \rightarrow$ Total number of Variables

$k \rightarrow$ Total number of complement Variable

Minimum number of NAND

$$= (3n-3) - k$$

Minimum number of NOR

$$= (2n-2) + k$$

(MCQ)

#Q. Consider the following function f_1, f_2

$$f_1 = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D \longrightarrow (3n-3)-k \Rightarrow (3 \times 4 - 3) - 3 = 6$$

$$f_2 = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D + \overline{B}$$

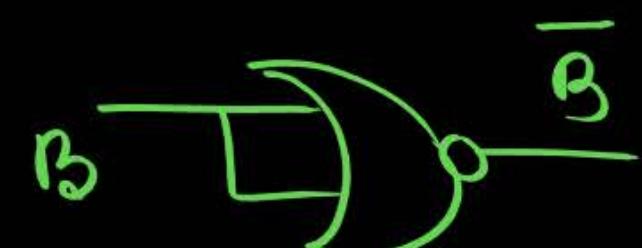
The number of NOR gate to implement f_1, f_2 will be n and m respectively. The value of $n-m$ will be ?

$$f_1 \rightarrow n = 6$$

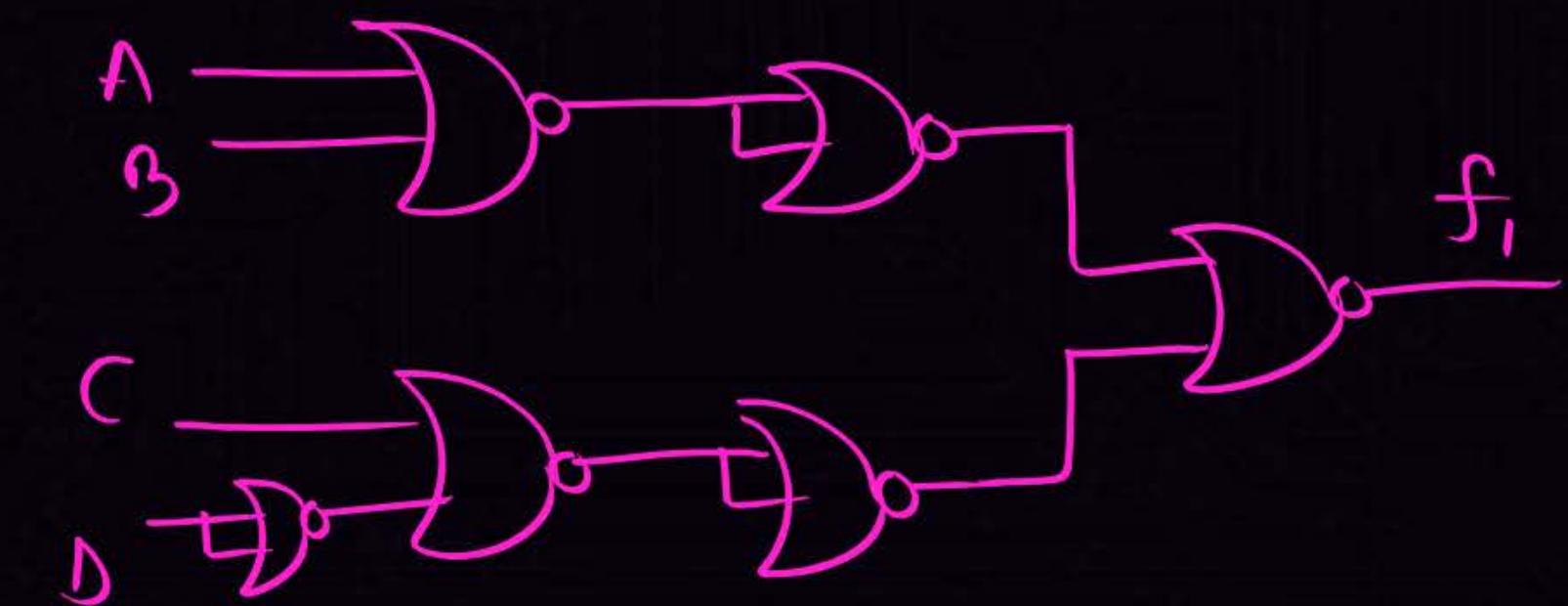
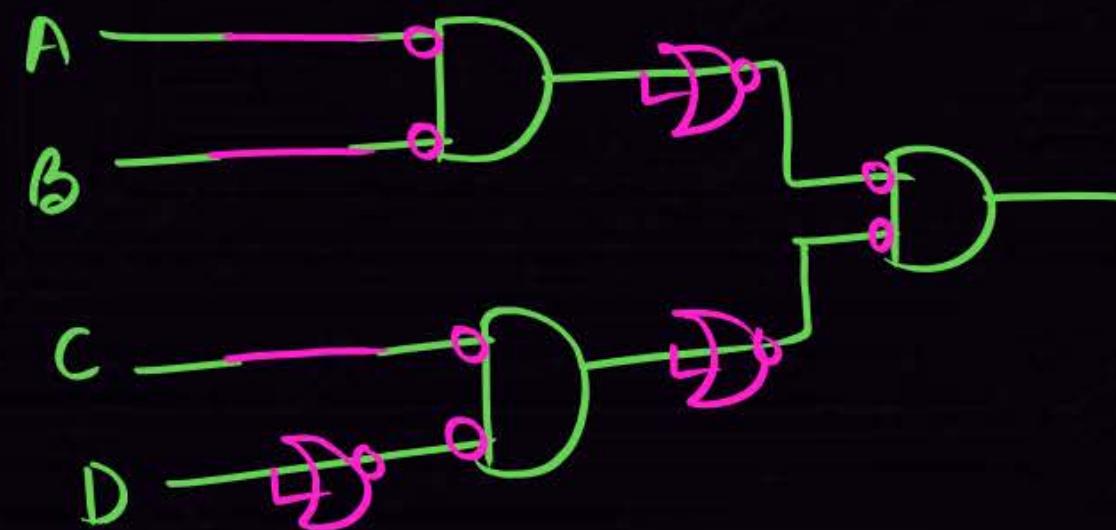
- [A] 4
- [B] 5
- [C] 6
- [D] 7

$$f_2 = \overline{B} [\overline{A} \cdot \overline{C} \cdot D + 1] = \overline{B} \quad m = 1$$

$$n-m = 6-1 = 5$$



$$f = \bar{A} \bar{B} \bar{C} D$$



#Q. Which of the following is/are self dual function?

[A] $f_1(A, B, C) = m_1 + m_2 + m_3 + m_6 \quad \times$

$$\begin{matrix} m_6 \\ m_1 \\ | \\ 110, \\ | \\ 001 \end{matrix}$$

[B] $f_2(A, B, C) = m_1 + m_2 + m_3 + m_7 \quad \checkmark$

$$\begin{matrix} 0 \\ 0 \\ 0 \\ | \\ 111 \end{matrix}$$

[C] $f_3(A, B, C, D) = \prod M(0, 1, 2, 3, 4, 5, 6, 8) \quad \checkmark$

$$\begin{matrix} 0 \\ 1 \\ 1 \\ 1 \end{matrix}$$

[D] $f_4(A, B, C) = \overline{m_1 + m_2 + m_3 + m_7} \quad \checkmark$

$$\begin{matrix} 1 \\ 0 \\ 0 \\ 0 \end{matrix}$$

Dual

Ex.1 $f = A \cdot B$ AND \longleftrightarrow Dual
 $f^D = A + B$ OR \longleftrightarrow Dual

Ex.2 $f = \overline{A \cdot B}$ NAND \longleftrightarrow Dual
 $f^D = \overline{A+B}$ NOR \longleftrightarrow Dual

- ① AND \longleftrightarrow OR
- ② $\cdot \longleftrightarrow \bar{\cdot}$
- ③ NAND \longleftrightarrow NOR
- ④ X-OR \longleftrightarrow X-NOR
- ⑤ $A \longleftrightarrow \bar{A}$
- ⑥ $\bar{A} \longleftrightarrow \bar{\bar{A}}$
- ⑦ 0 \longleftrightarrow 1

Ex $f = ABC + A\bar{B}C + A\bar{B}\bar{C}$

$$f^D = (A+B+C) \cdot (A+\bar{B}+C) \cdot (A+\bar{B}+\bar{C})$$

Self Dual

$$A \xleftrightarrow{\text{Dual}} A$$

$$\bar{A} \xleftrightarrow{\text{Dual}} \bar{A}$$

$$f = A$$

$$f^D = A$$

$$f = f^D$$

Self Dual

Self Dual.

- ① Number of Minterms = Number of Maxterm
- ② Does not present Mutual exclusive function

Mutual Exclusive

$$m_0 \rightarrow 000 \rightarrow \bar{A}\bar{B}\bar{C}$$

$$m_1 \rightarrow 001 \rightarrow \bar{A}\bar{B}C$$

$$m_2 \rightarrow 010 \rightarrow \bar{A}B\bar{C}$$

$$m_3 \rightarrow 011 \rightarrow \bar{A}BC$$

$$m_4 \rightarrow 100 \rightarrow A\bar{B}\bar{C}$$

$$m_5 \rightarrow 101 \rightarrow A\bar{B}C$$

$$m_6 \rightarrow 110 \rightarrow AB\bar{C}$$

$$m_7 \rightarrow 111 \rightarrow ABC$$

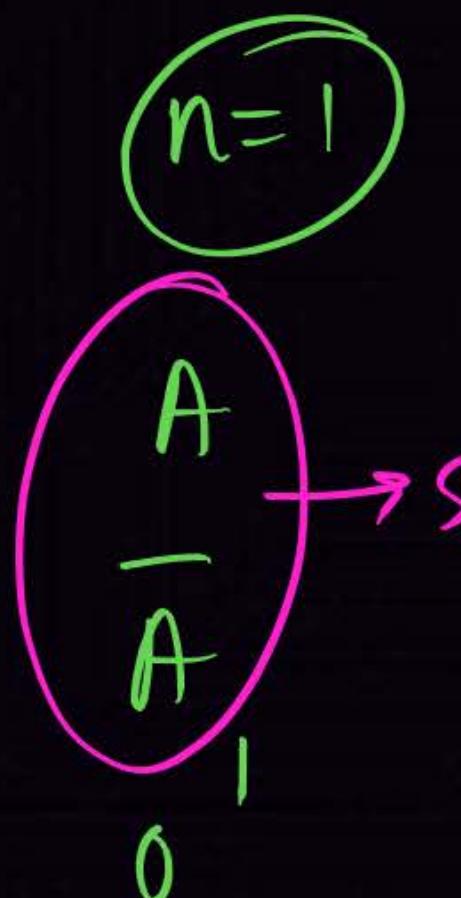
$$\{\bar{A}\bar{B}\bar{C}, ABC\} \Rightarrow \{m_0, m_7\}$$

$$\{010, 101\}$$

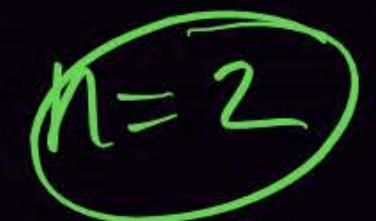
$$\{m_1, m_6\}$$

$$\{m_2, m_5\}$$

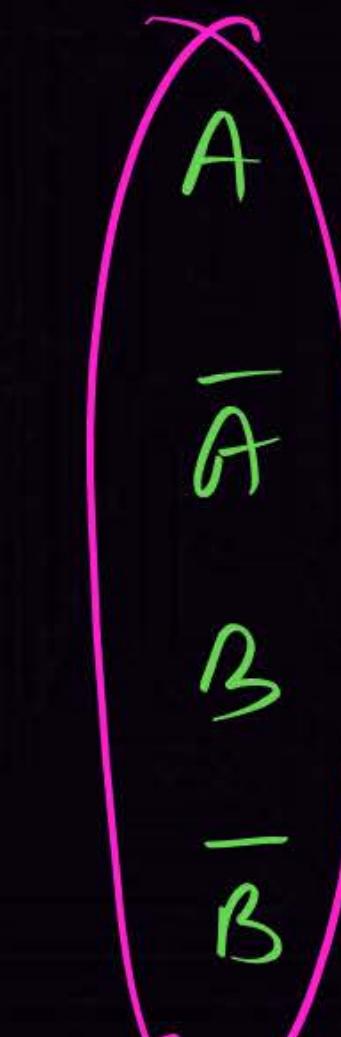
$$\{m_3, m_4\}$$



self dual

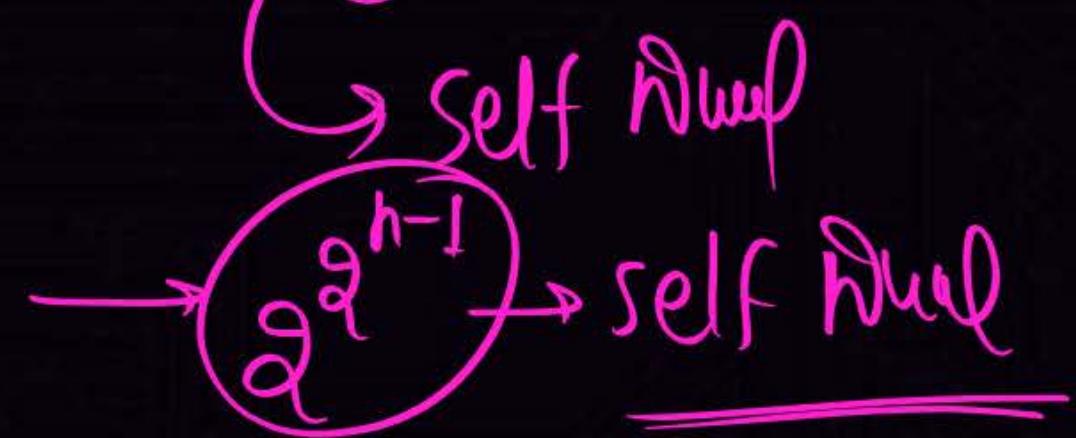


$$\begin{array}{ll} \bar{A}\bar{B} & \bar{A}+\bar{B} \\ \bar{A}B & \bar{A}+B \\ A\bar{B} & A+\bar{B} \\ AB & A+B \end{array}$$



$$\begin{array}{ll} 0 & \bar{A}B+\bar{A}\bar{B} \\ L & \bar{A}\bar{B}+AB \end{array}$$

"n" Variable $\rightarrow q^n$ distinct expression



Q = Find the dual.

$$f = AB + BC + AC \quad \leftarrow \text{self dual}$$

$$f^D = (A+B) \cdot (B+C) \cdot (A+C)$$

$$= (AB + AC + BC + BC) (A+C)$$

$$= [B(A+1+C) + AC] \{ A+C \}$$

$$= \{B+AC\} (A+C)$$

$$= AB + AC + BC + AC$$

$$= AB + BC + AC$$

$$f = AB + BC + AC$$

$$f = AB(\bar{C}+C) + (\bar{A}+A)BC + A(\bar{B}+B)$$

$$f = AB\bar{C} + ABC + \bar{A}BC + ABC$$

$$f = \bar{A}BC + \bar{A}\bar{B}C + A\bar{B}\bar{C} + ABC$$

$$f = m_3 + m_5 + m_6 + m_7$$

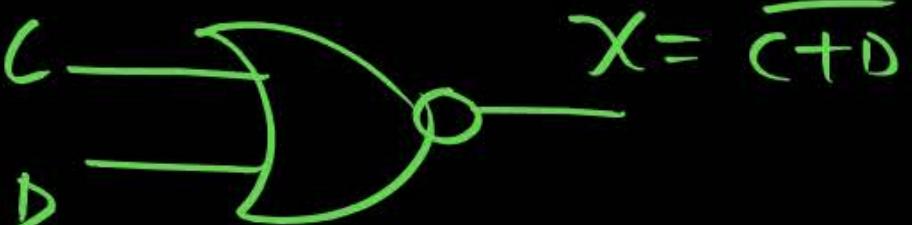
Self Dual

(MCQ)

#Q. Find the number of 2-input NOR gate to implement to the following function,

$$f = A \bar{C} \bar{D} + B$$

$$\overline{C+D} = X$$



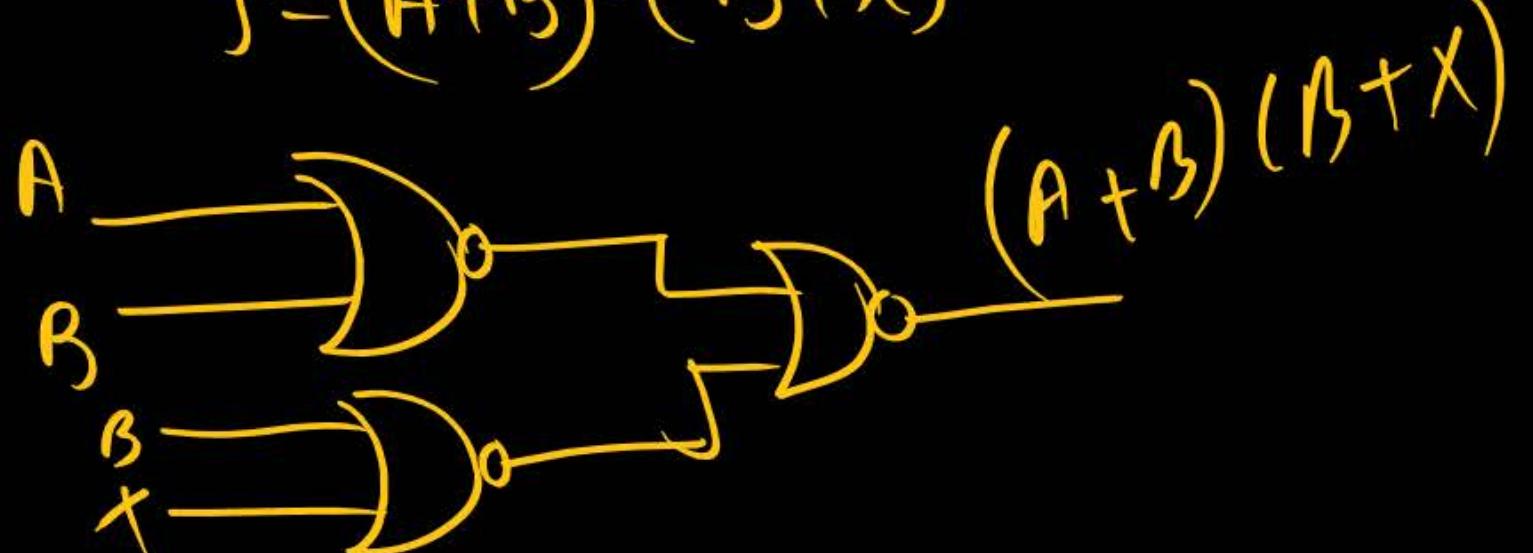
- A 4
- B 5
- C 10
- D 12

$$f = A \bar{C} \bar{D} + B$$

$$f = A(\overline{C+D}) + B$$

$$f = AX + B$$

$$f = (A+B) \cdot (B+X)$$

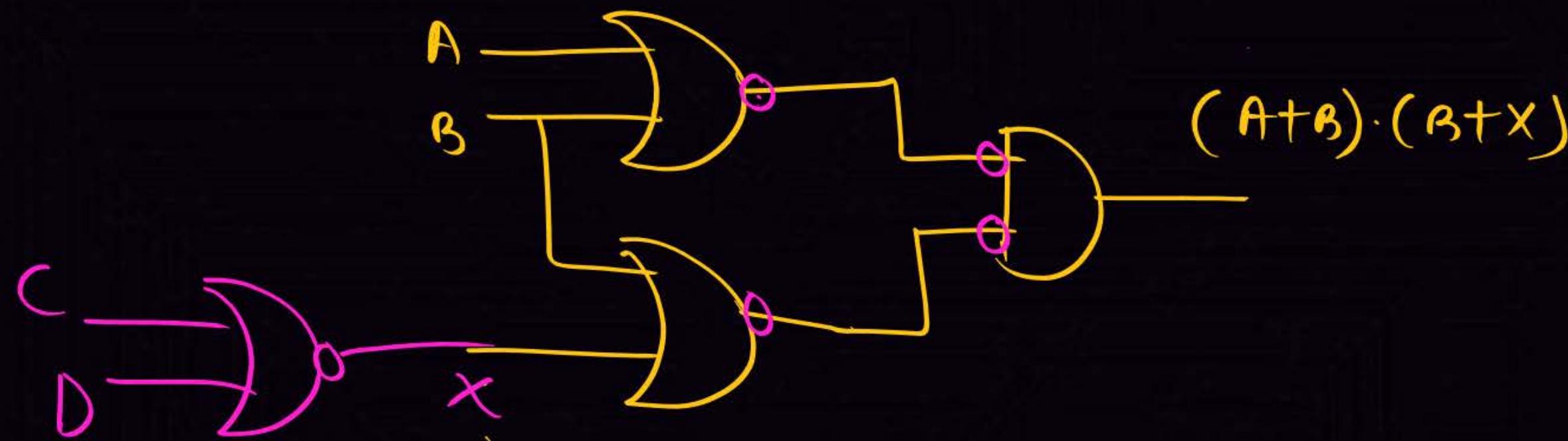


$$f = A \bar{C} \bar{D} + B$$

$$\begin{aligned} & A \cdot [\bar{C} + \bar{D}] + B \\ &= A\bar{x} + B = (A+B)(B+x) \end{aligned}$$

$$\bar{C} + \bar{D} = x$$

$$\neg \neg D = \neg \neg \neg d$$



AND - OR \Rightarrow N AND - N AND

OR - AND \Rightarrow NOR - NOR

#Q. Consider the logical functions given below:

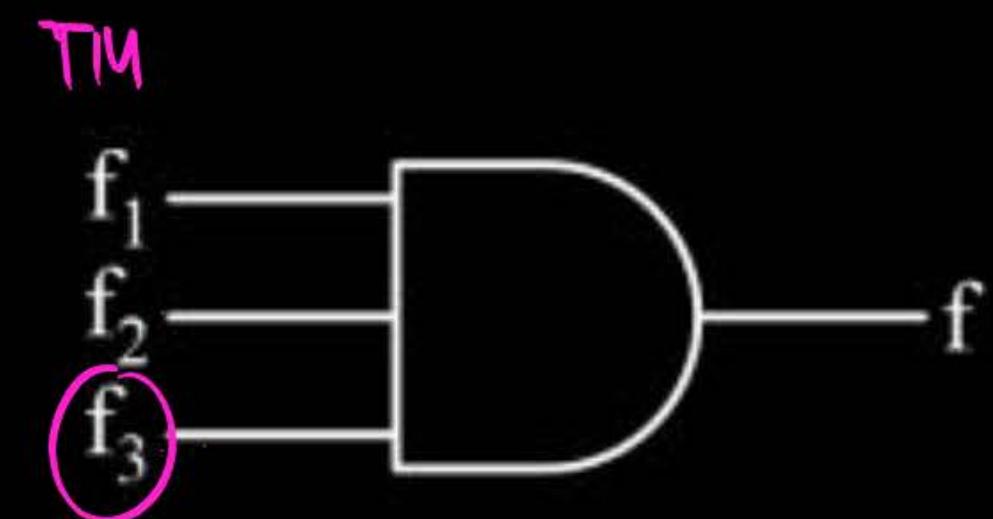
$$f_1 = (A, B, C) = \sum (2, 6, 7) = \text{TIM}(0, 1, 3, 4, 5)$$

$$f_2 = (A, B, C) = \prod (4, 5, 6, 7)$$

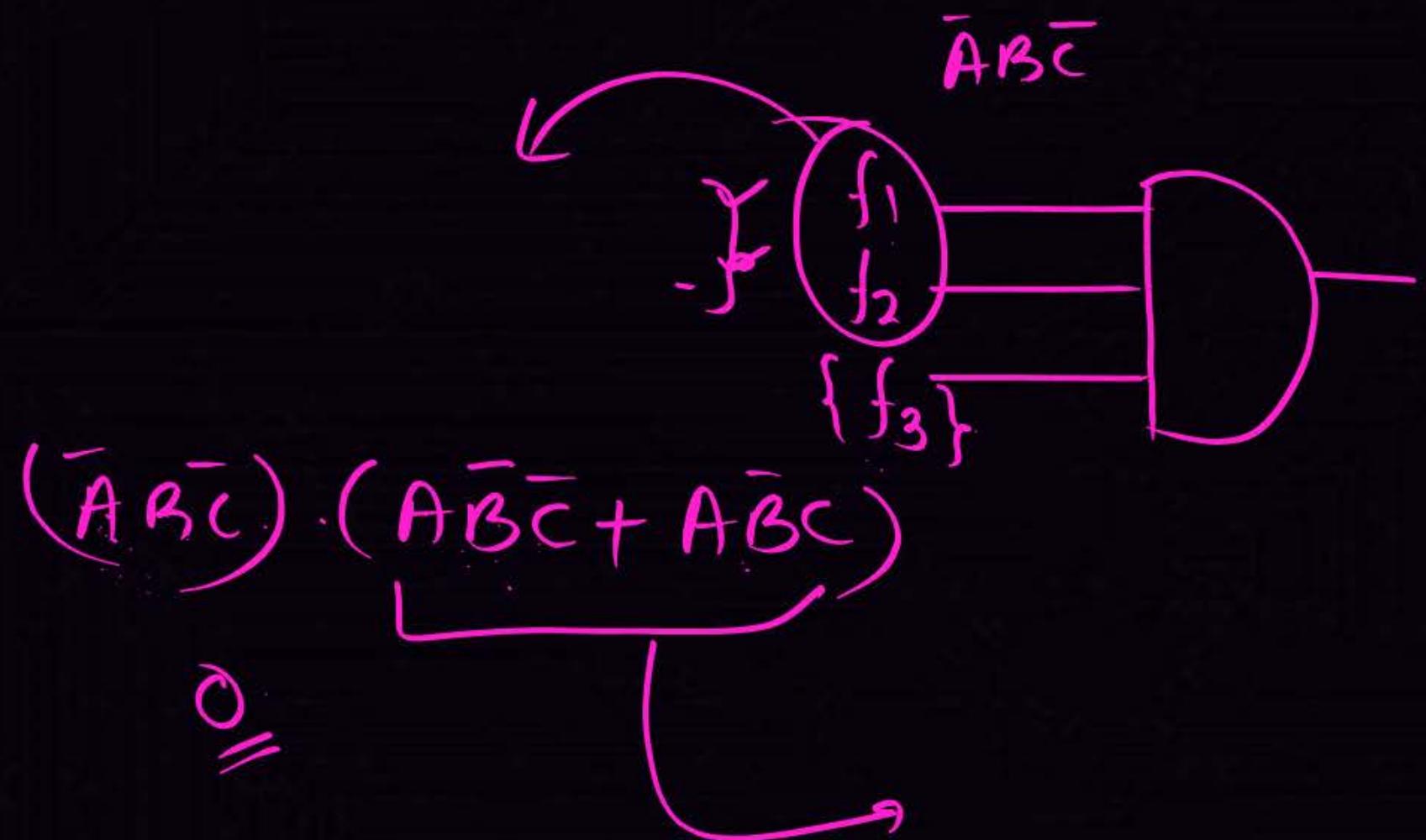
$$= \prod (\overline{f_1} \wedge f_2)$$

$$= \prod \{ \overline{4, 5} \}$$

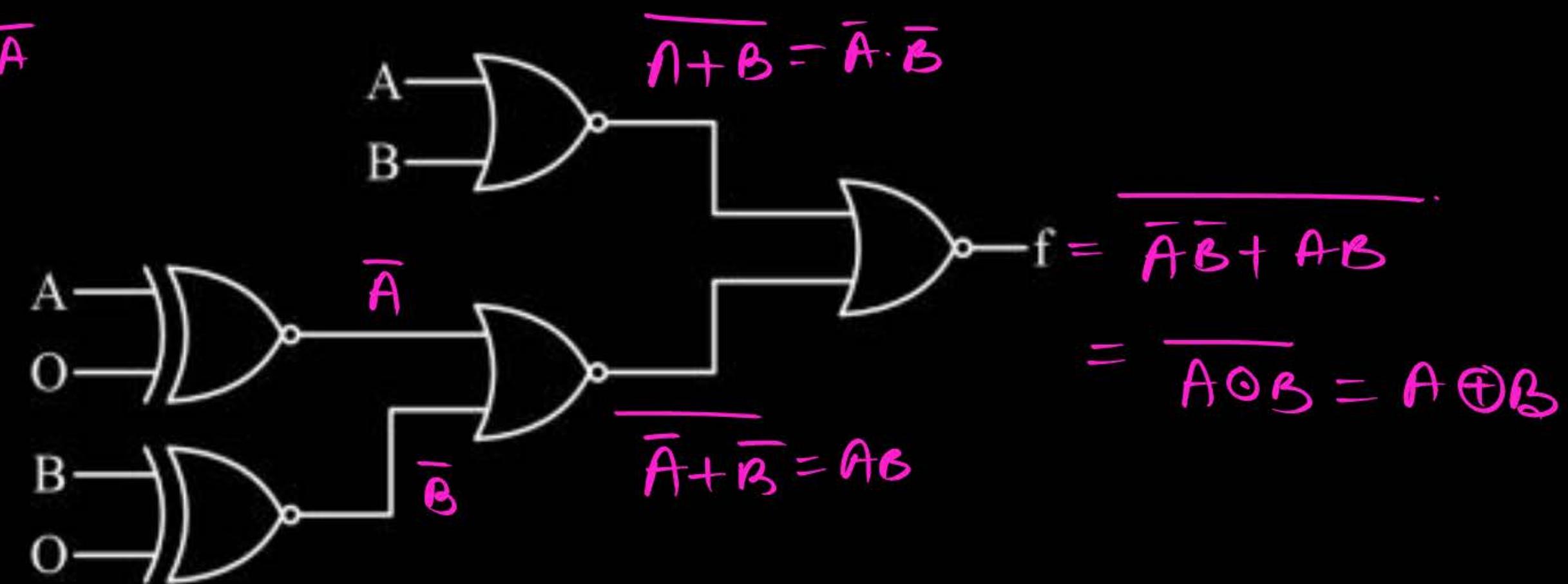
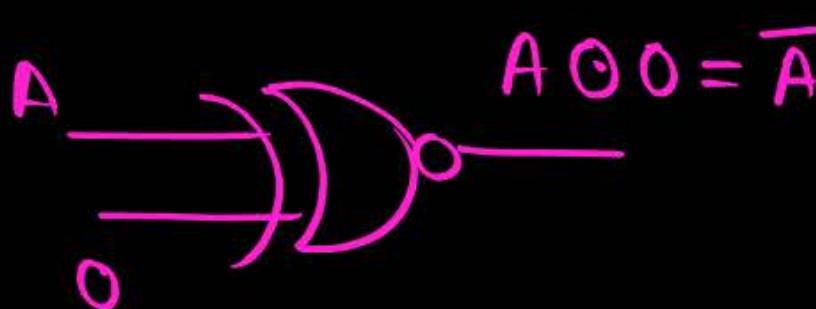
$$= \prod (0, 1, 2, 3, 6, 7)$$



If f is logic 1, then maximum number of possible maxterms in function f_3 are ____.

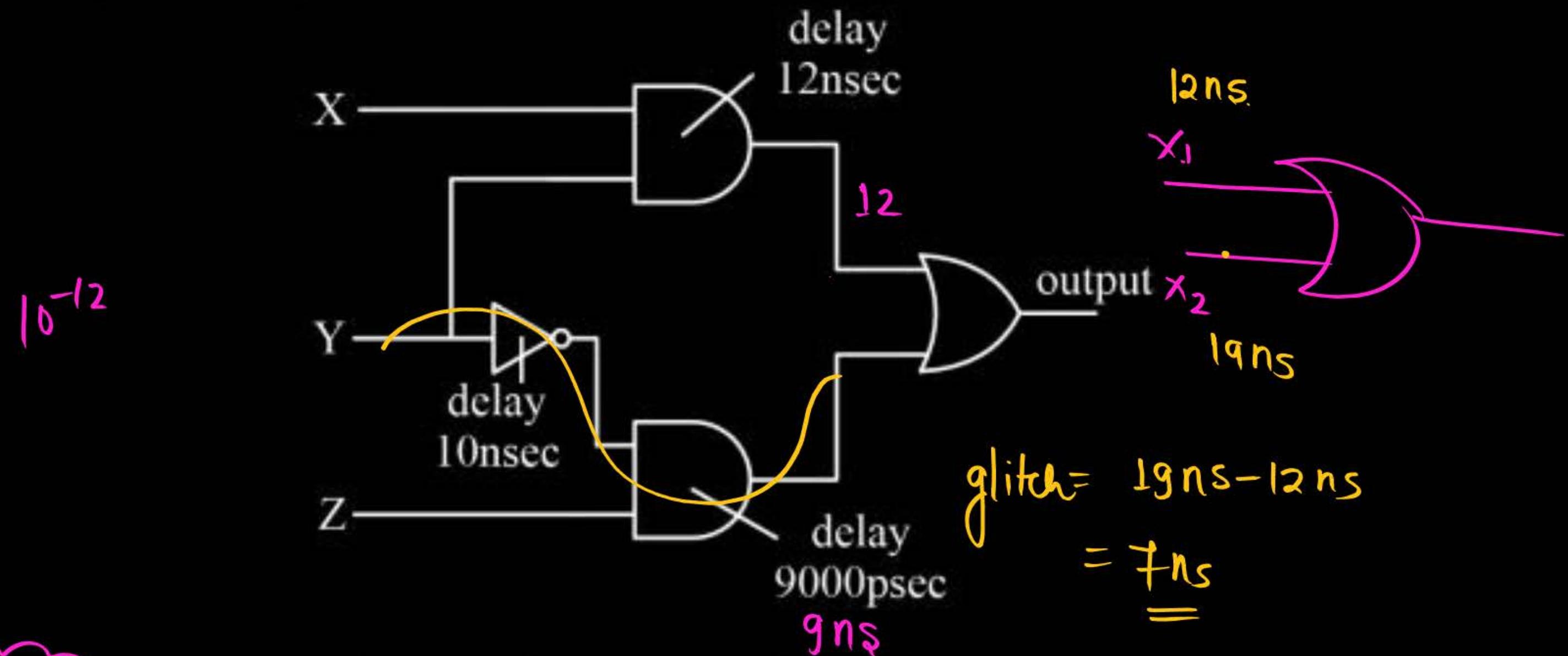


#Q. Consider the Boolean circuit:



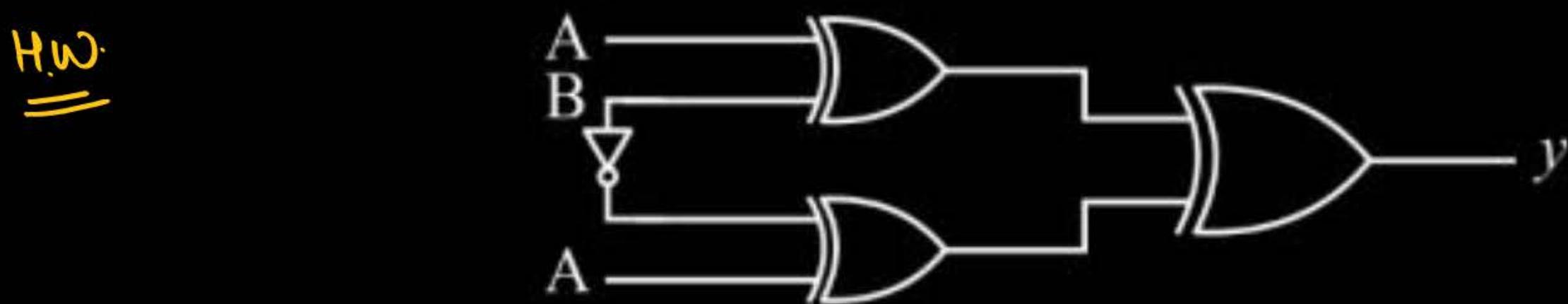
The number of NAND gate to implement f is ____.

#Q. For the given diagram



A **glitch** is generated for a short time, then the output attains its correct value, the duration of glitch is 7 (in nsec).

#Q. A digital circuit is implemented as shown



Output y is '1' for input $A = 1$ and $B = 0$. If input is changed to $A = 0$ and $B = 1$ then output y will

- A** Change from '1' to '0'
- B** Remains at '1'
- C** Oscillate between '1' and '0'
- D** None of the above

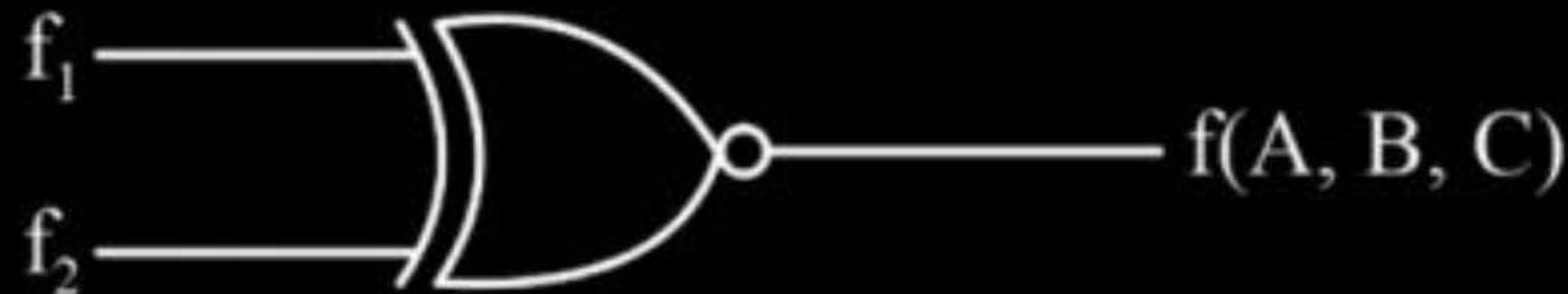
(MCQ)

#Q. Two logical functions f_1 , & f_2 are given as:

HW $f_1(A, B, C) = A\bar{B} + BC$

$$f_2(A, B, C) = (\bar{A} + \bar{B})(A + C)$$

A logical function $f(A, B, C)$ is implemented as:



Then, $f(A, B, C)$ will be:

- A** $(A \oplus B) + \bar{C}$
- B** $A \square B + AC$
- C** $AB + BC + CA$
- D** $A\bar{B} + \bar{B}C + AC$



Thank You
GW
soldiers!



CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No. - 4



By - CHANDAN SIR

Recap of Previous Lecture



Logic Gate

Topics to be Covered

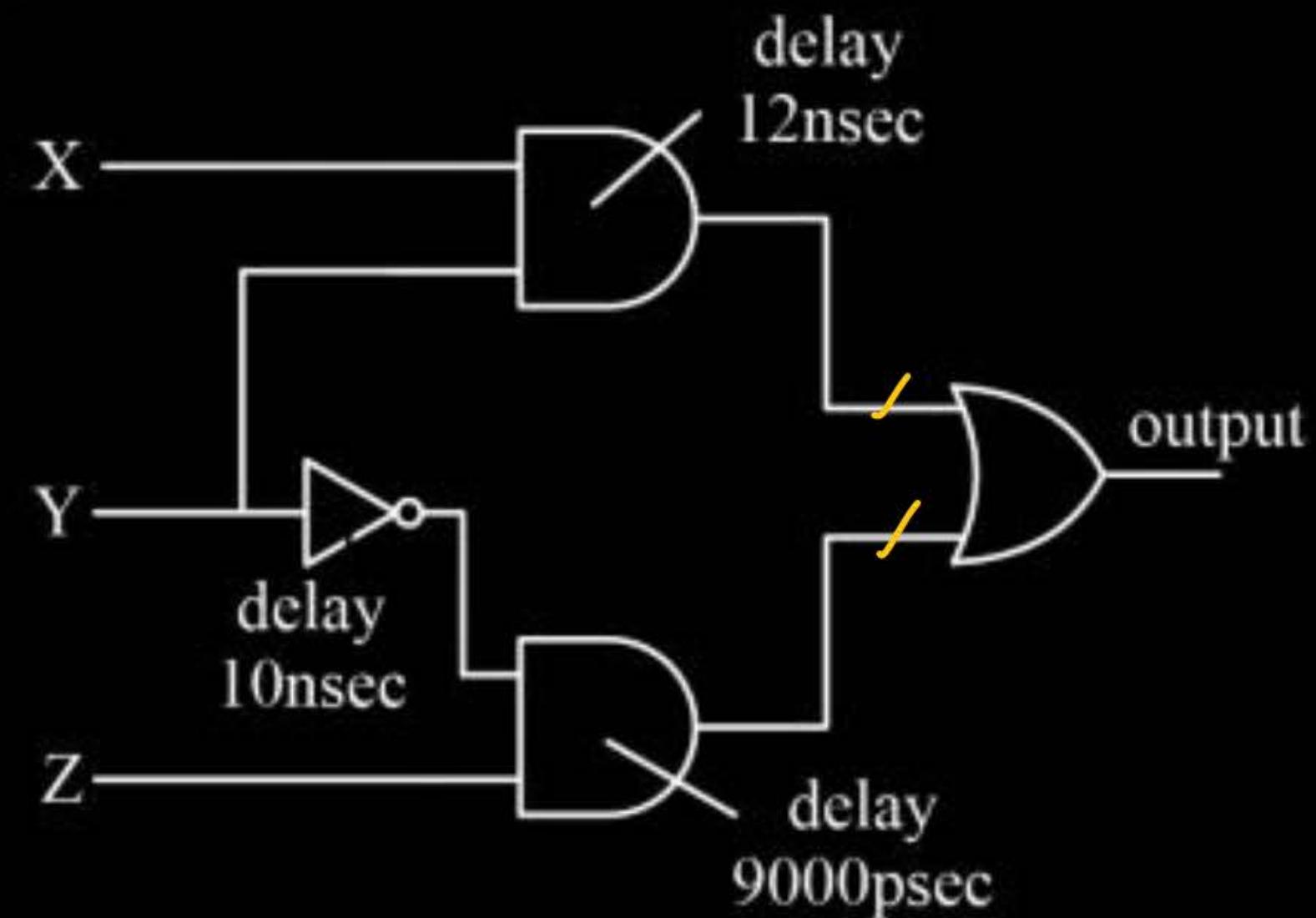


K-Map

Questions Practice

(NAT)

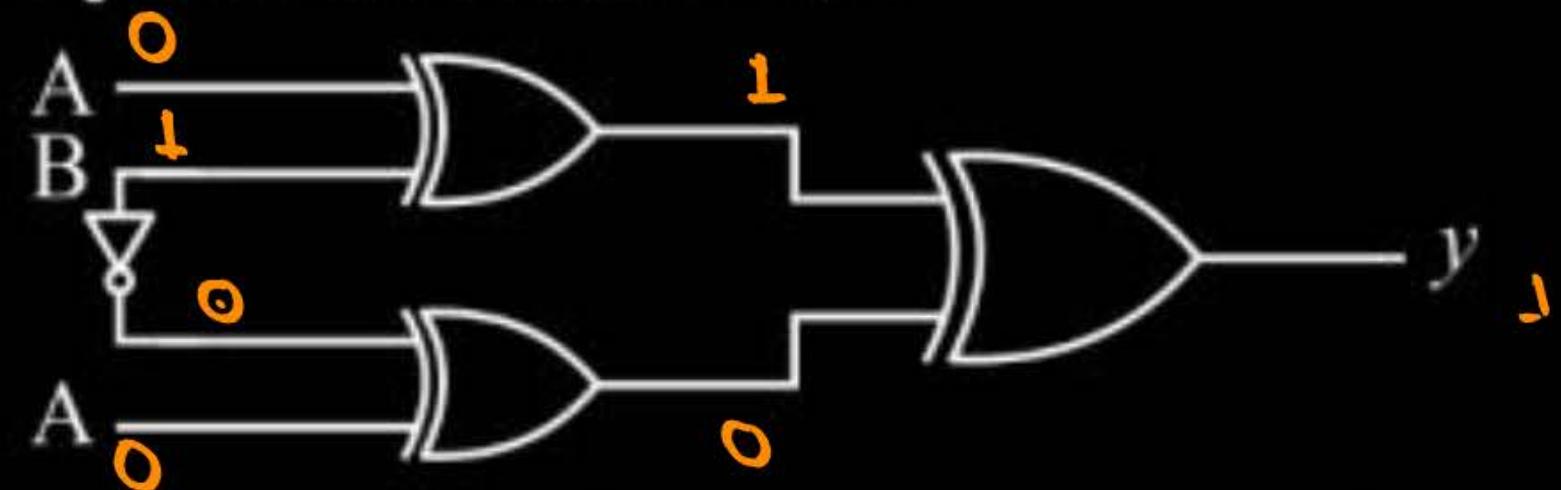
#Q. For the given diagram



A glitch is generated for a short time, then the output attains its correct value, the duration of glitch is ____ (in nsec).

(MCQ)

#Q. A digital circuit is implemented as shown



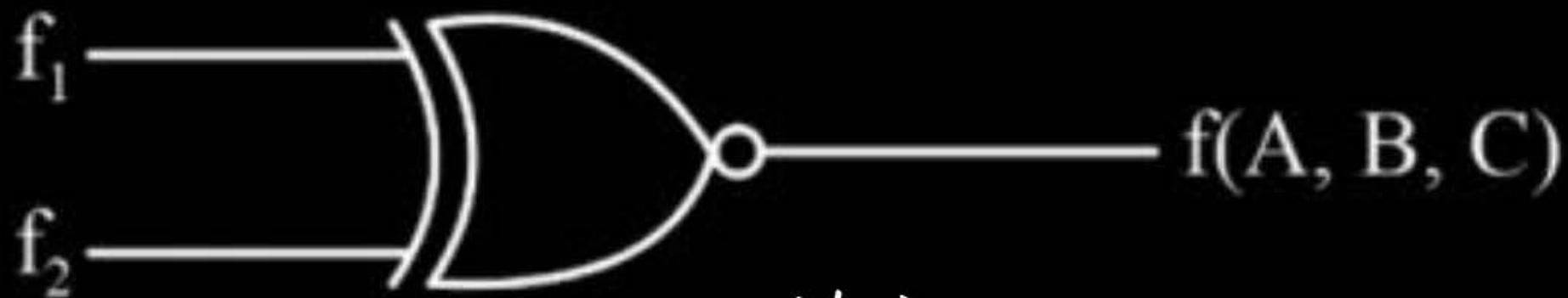
Output y is '1' for input $A = 1$ and $B = 0$. If input is changed to $A = 0$ and $B = 1$ then output y will

- A Change from '1' to '0'
- B Remains at '1'
- C Oscillate between '1' and '0'
- D None of the above

(MCQ)

$$f_1(A, B, C) = A\bar{B} + BC = \sum m(4, 5, 3, 7)$$

$$\begin{aligned} f_2(A, B, C) &= (\bar{A} + \bar{B})(A + C) = \sum m(1, 3, 4, 5, 1) \\ &= \bar{A}C + A\bar{B} + \bar{B}C \end{aligned}$$



$$= \sum m(1, 4, 5, 7)$$

A $(A \oplus B) + \bar{C}$

B $A \oplus B + AC$

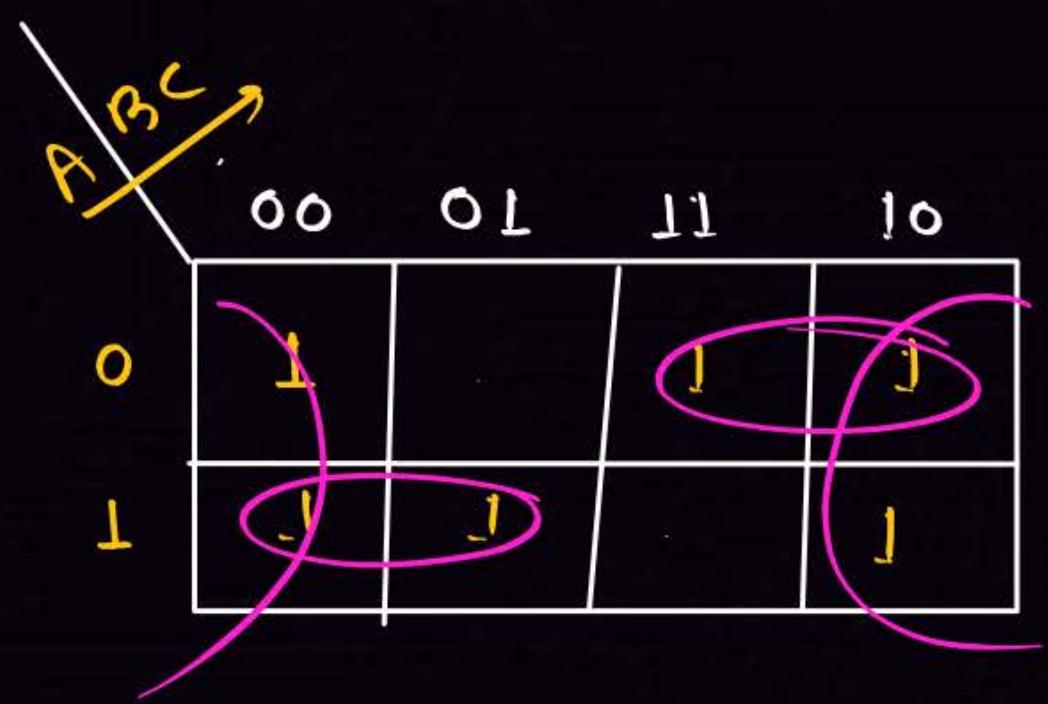
C $AB + BC + CA$

D $A\bar{B} + \bar{B}C + AC$



$$\sum m(0, 2, 3, 4, 5, 6)$$

$$= \sum m(1, 3, 4, 5, 7)$$



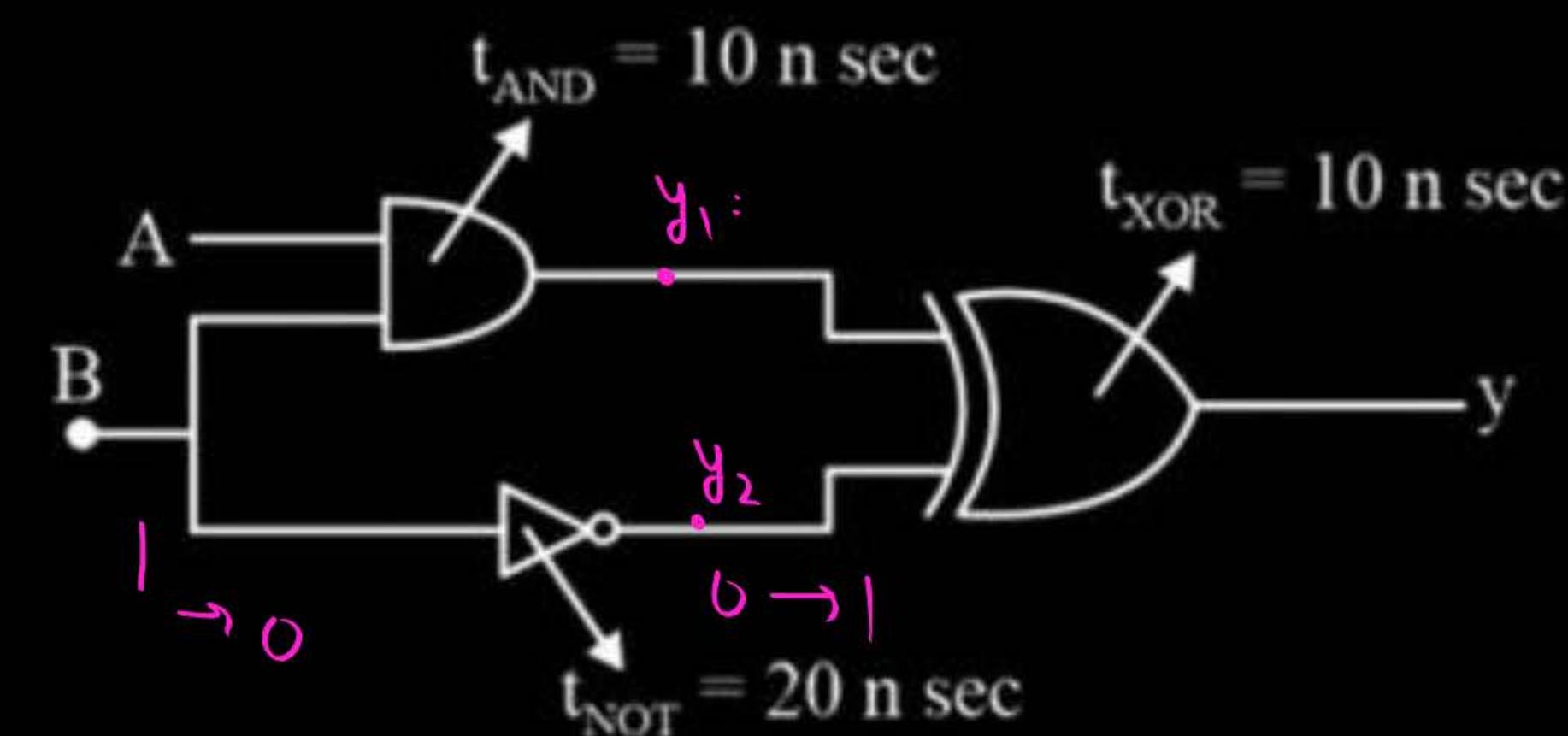
$$= \bar{A}\bar{B} + \bar{A}B + \bar{C}$$

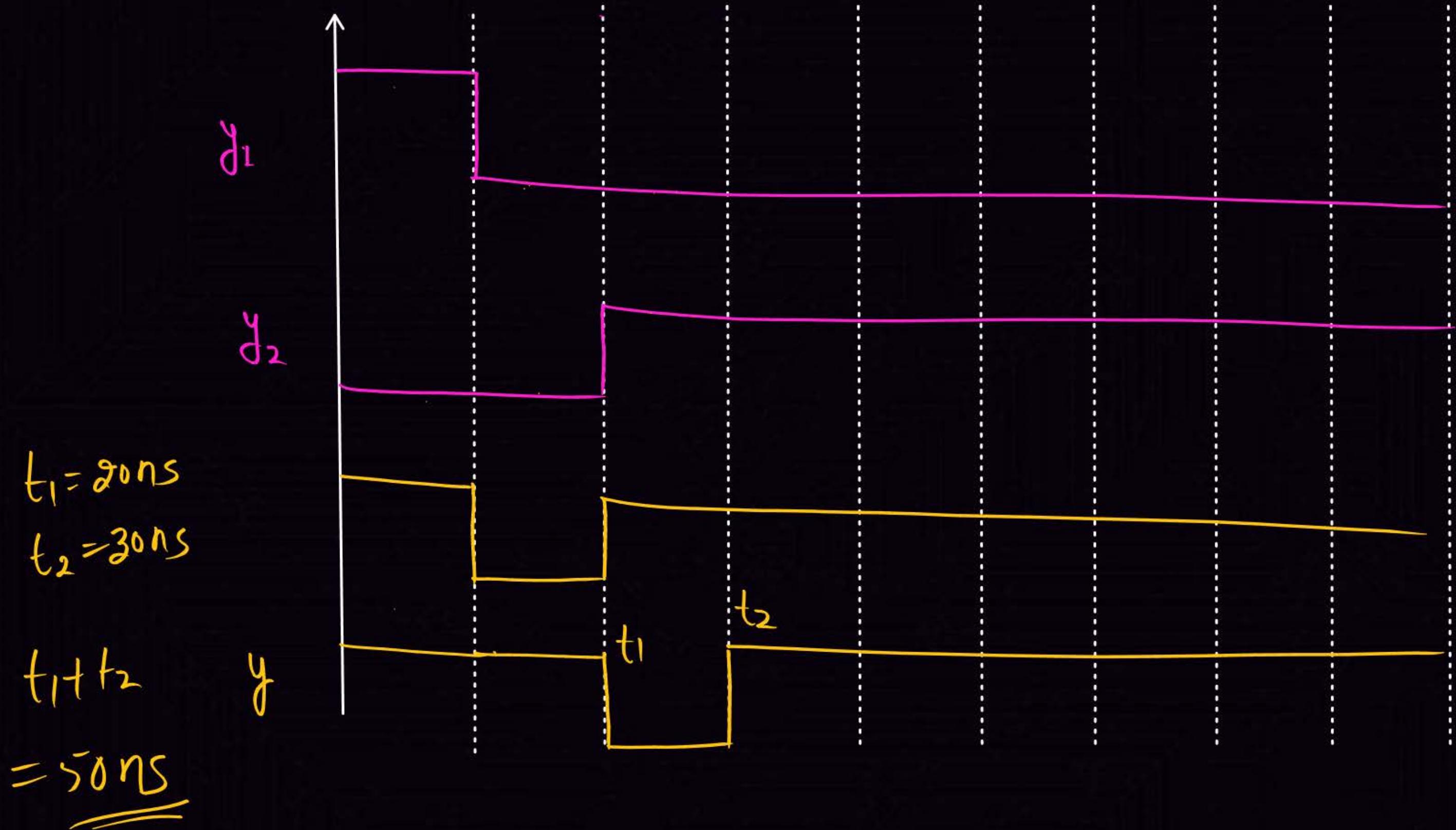
$$= (\bar{A} \oplus B) + \bar{C}$$

(NAT)

#Q. A logical circuit is implemented as shown:

Initially $A = B = 1$ & output is at '1'. Delay of each gate is mentioned in the circuit. If A & B are changed to '0' at $t = 0$ then output goes to '0' from time t_1 to t_2 . Then the value of $(t_1 + t_2)$ _____ (n sec).

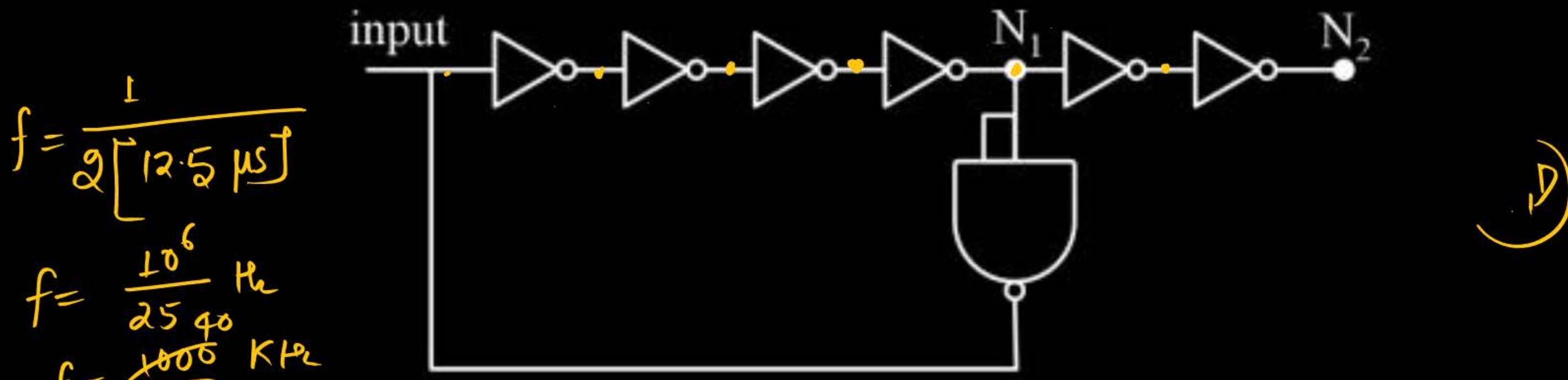




(MSQ)

#Q. Consider the below circuit:

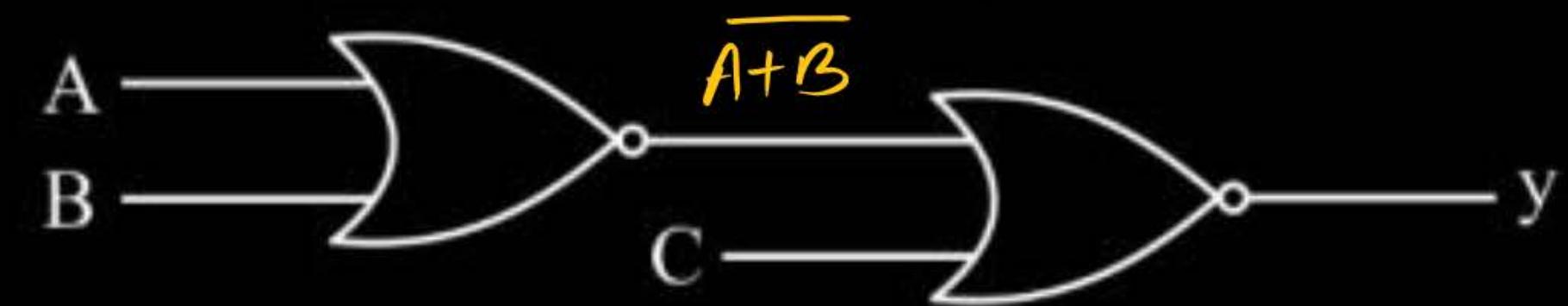
Delay of each NOT gate is $2 \mu\text{s}$ and delay of NAND gate is $4.5 \mu\text{s}$ then which of the following statement is/are correct?



- A Frequency of the rectangular waveform will be 50 kHz ✗
- B Frequency of the rectangular waveform will be 40 kHz
- C Frequency of the waveform at node N_1 will be less than node N_2 ✗
- D Frequency of the waveform at every node will be same ✓

(NAT)

#Q. A logical function implementation is as given below.



The minimum number of 2-input NAND gates required to implement y is ____.

$$\begin{aligned} \overline{\overline{A+B}+C} &= (\overline{A+B}) \bar{C} \\ &= \overline{A\bar{C} + B\bar{C}} \quad 1 \\ &\quad 3 \end{aligned}$$

$3+1=4$ ~~3~~

(NAT)

#Q. Consider a 4-variable Boolean function

$$f(w, x, y, z) = w + \bar{w}x + \bar{w}\bar{x}y + \bar{w}\bar{x}\bar{y}z$$

The number of NOR gate to implement the minimized expression will be ____.

$$(w + \bar{w})(w + x)$$

$$(w + x) + (\bar{w} + \bar{x}) \cdot y$$

$$P + (\bar{P} \cdot y)$$

$$w + x = P$$

$$\begin{aligned}(P + \bar{P})(P + y) &= P + y \\ &= w + x + y\end{aligned}$$

$$f = w + x + y + z$$

$$n=4 \quad k=0$$

$$NOR = (2^{n-2}) + k$$

$$= 6 \text{ AS } //$$

#Q. Two function f_1 and f_2 are given as follows:

$$f_1(A, B, C, D) = \sum m(1, 2, 4, 7, 9, 15)$$

$$f_2(A, B, C, D) = \prod M(1, 2, 5, 6, 8, 9, 13, 14) = \sum m(0, 3, 6, 10, 11, 12, 15)$$

Then the number of essential prime implicants of the function

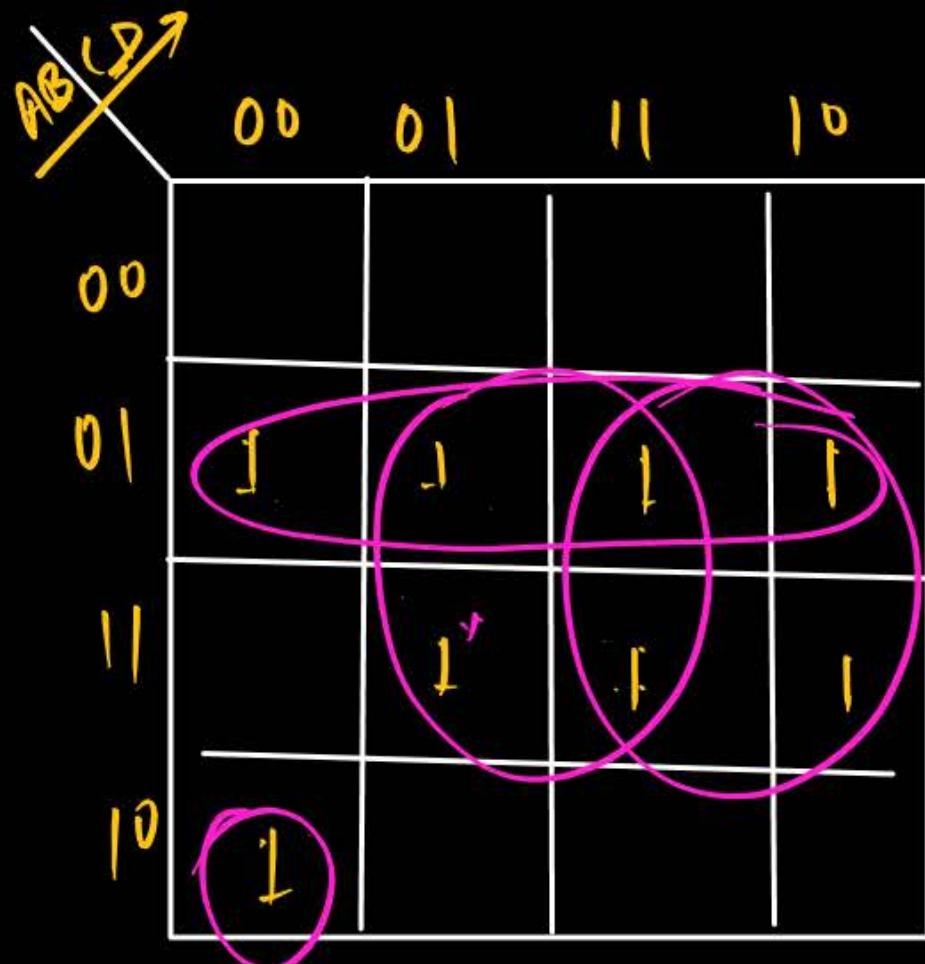
$$f_3 = \overline{f_1 \oplus f_2}$$

$$f_1 \oplus f_2 = \sum m(0, 1, 2, 3, 9, 10, 11, 12)$$

$$f_3 = \overline{f_1 \oplus f_2} = \sum m(4, 5, 6, 7, 8, 13, 14, 15)$$

④

$\bar{A}B, BD, BC, A\bar{B}\bar{C}\bar{D}$

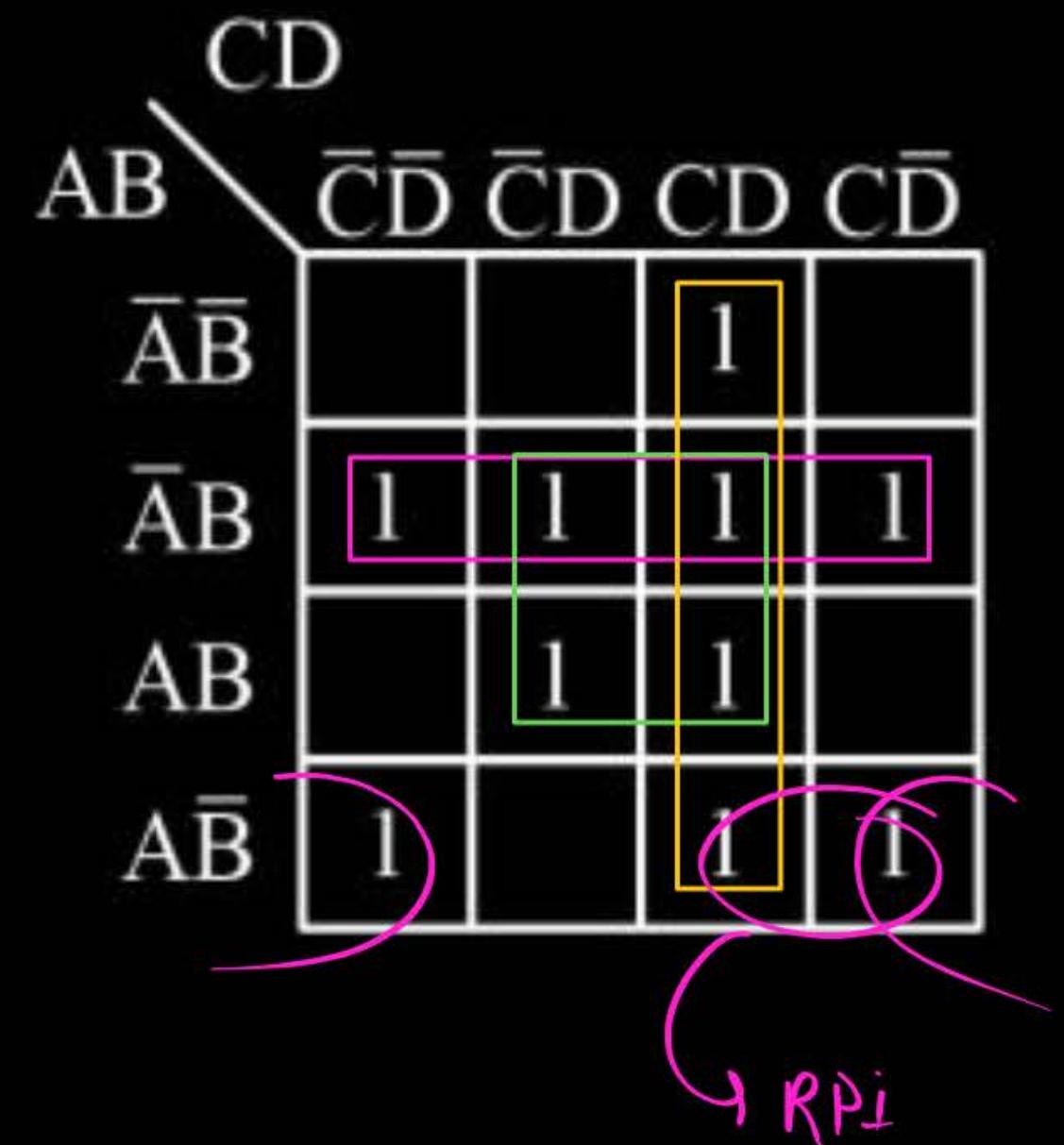


(MCQ)

#Q. Consider the K-map

The redundant prime implicant term is

- A** $CD, \bar{A}B$ ✗
- B** $A\bar{B}C$ ✓
- C** $BD, \bar{A}B$ ✗
- D** None of these ✗



(MCQ)

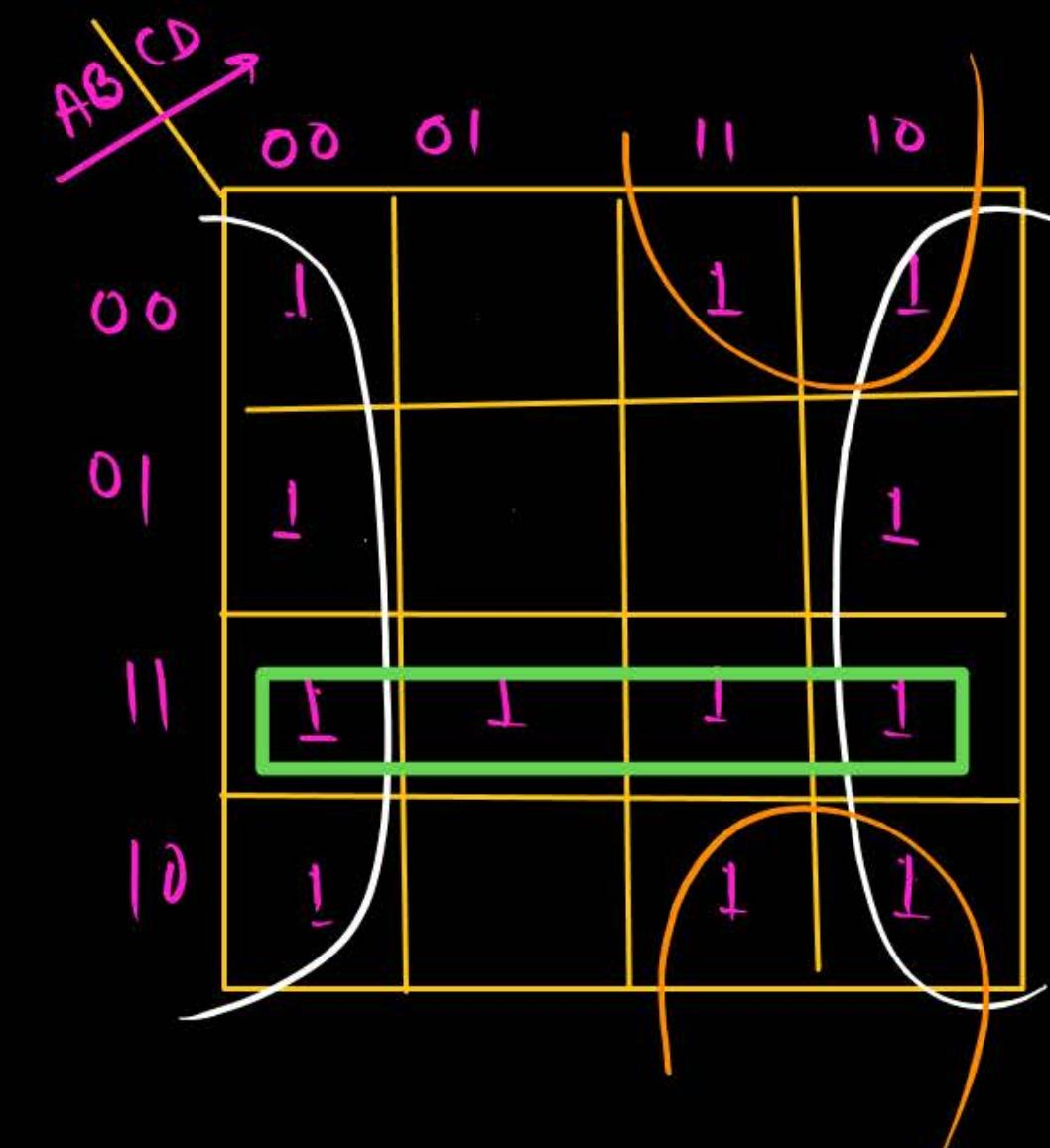
#Q. Consider the following Boolean function,

$$f = BD + \bar{B}CD + ABC + AB\bar{C}D + \bar{B}\bar{D}$$

The minimum number of two input NAND gates required to implement this function is ____.

0 0 0 . 0
0 0 1 0
1 0 0 0
1 0 1 0

- A** 4
- B** 5
- C** 6
- D** 10



4

$AB + \bar{B}C + \bar{D}$

$4+2=6$

(MSQ) ✓



#Q. A three variable Boolean function is defined as,

$$f(A, B, C) = \prod M(1, 2, 4, 7) = \sum m(0, 3, 5, 6)$$

If $\overline{f(A, B, C)}$ denotes the complement of the function $f(A, B, C)$, then the simplified expression of $\overline{f(A, B, C)}$ can be given as

$$\overline{f} = \sum m(1, 2, 4, 7) = A \oplus B \oplus C$$

- A $(A \oplus B) \odot C$
- B $A \oplus B$
- C $A \oplus B \oplus C$
- D $B \square C$

$$A, C$$

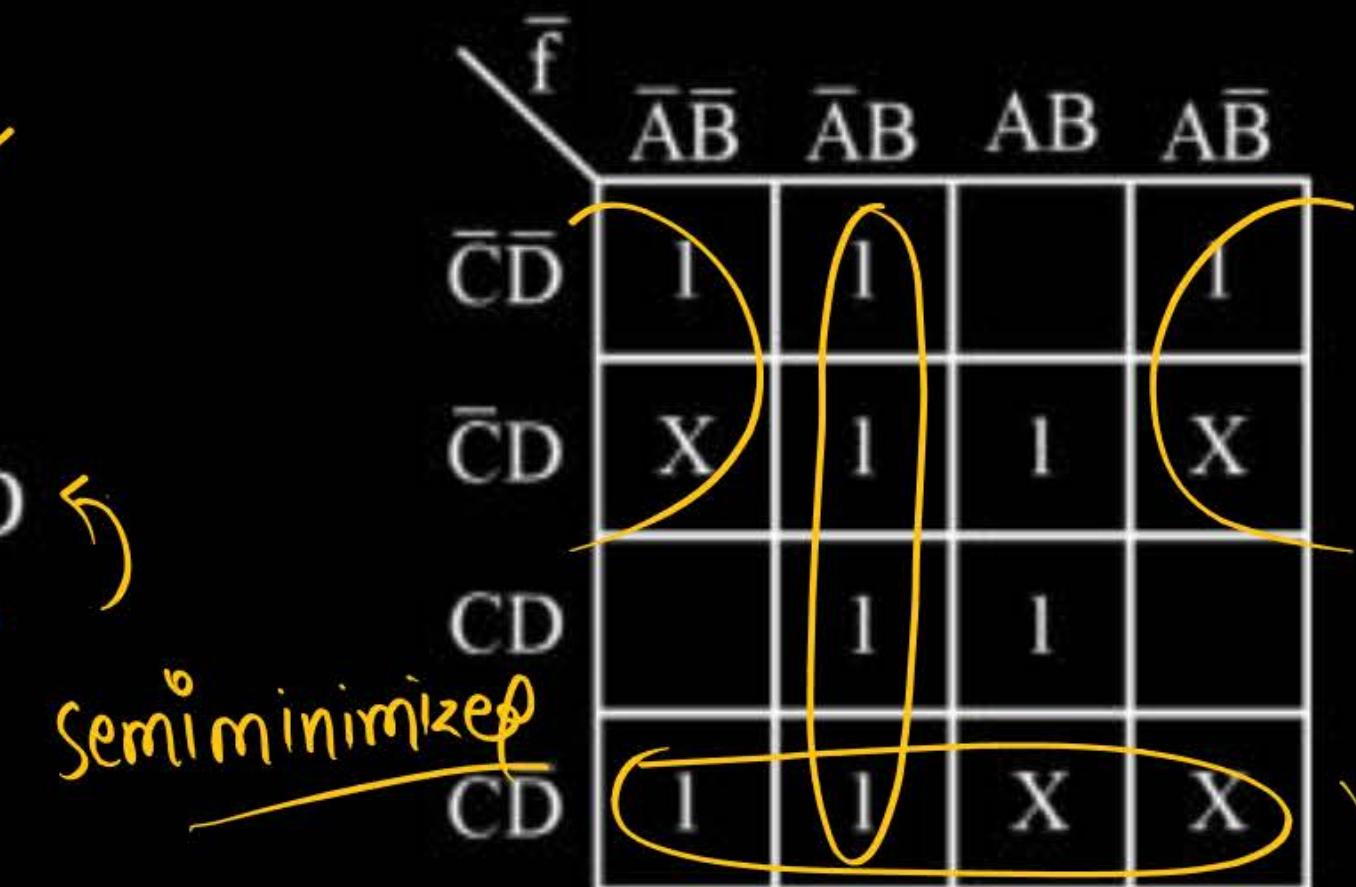
$$\neg(A \oplus B) \odot C$$

#Q. Consider the K-map given below:

Which of the following is/are minimized form of above K-map?

- A** $\overline{AD} + BD + \overline{BC}$ ✓
- B** $\overline{BC} + \overline{AB} + \overline{CD}$ ✗
- C** $\overline{AB} + \overline{CD} + \overline{BD} + BD$ ↗
- D** $BD + \overline{AD} + \overline{BD}$ ✓

A/D



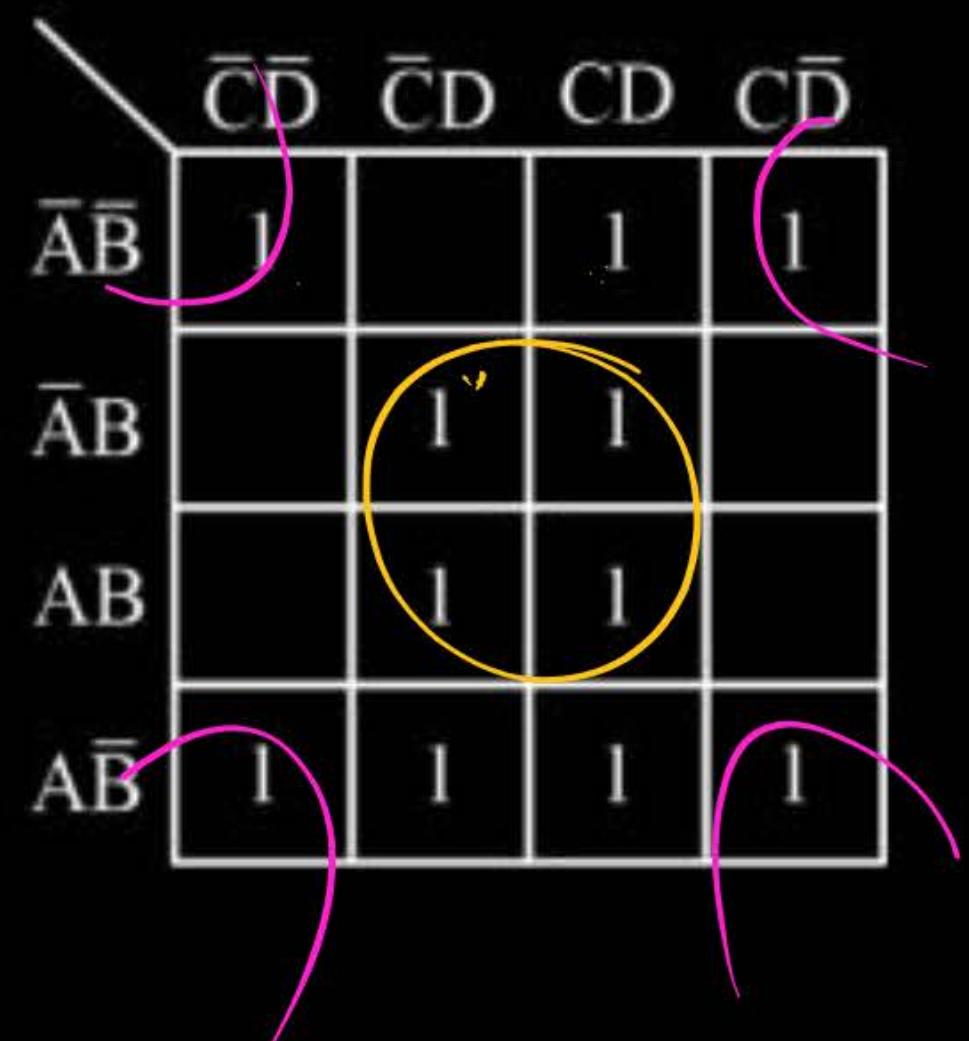
$$\begin{aligned} &BD + \overline{A}\overline{D} + \overline{B}\overline{C} \\ &BD + \overline{A}\overline{D} + \overline{B}\overline{D} \end{aligned}$$

(MCQ)

#Q. Consider the K-map given below:

The EPI term will be:

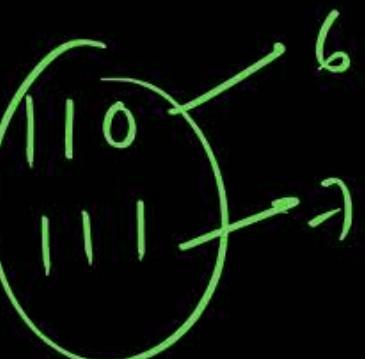
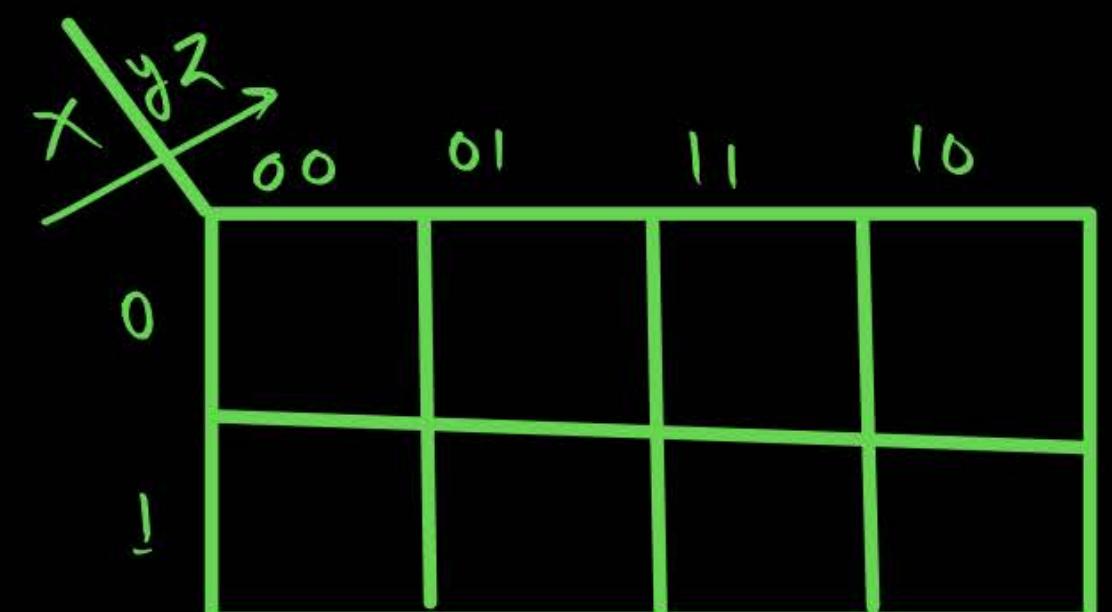
- A** BD, A \bar{B}
- B** A \bar{B} , CD
- C** BD, $\bar{B}\bar{D}$
- D** BD, $\bar{B}C$



(MCQ)

#Q. A logic circuit implements the Boolean function $f = \bar{x}y + x\bar{y}z$. It is found ~~hw~~ that the input combination $x = y = 1$ can never occur. Taking this into accounts a simplified expression for f is given by

- A** $\bar{x} + \bar{y} \cdot \bar{z}$
- B** $x + z$
- C** $x + y$
- D** $y + xz$



(MCQ)

#Q. In a function f , the difference between PI and EPI is 2. Then the number of minimal expressions are
HW (Given RPI = 0)

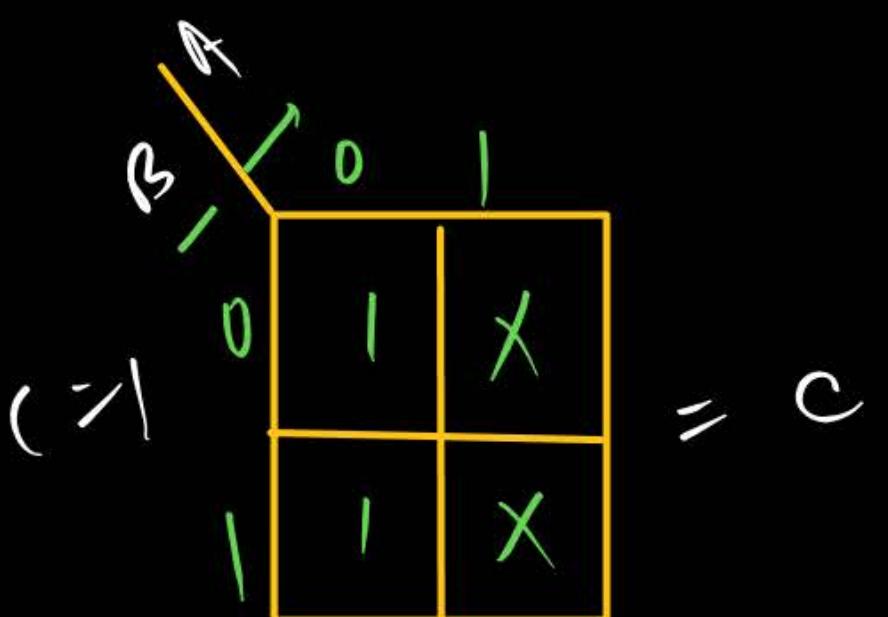
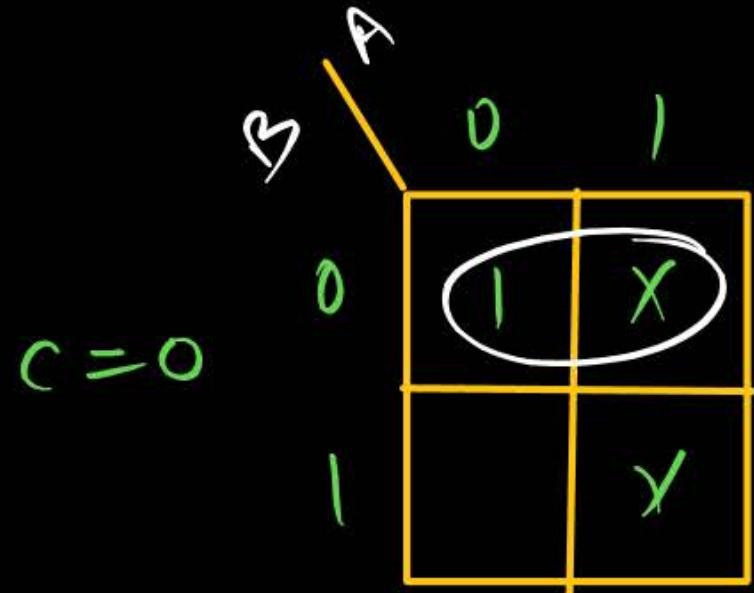
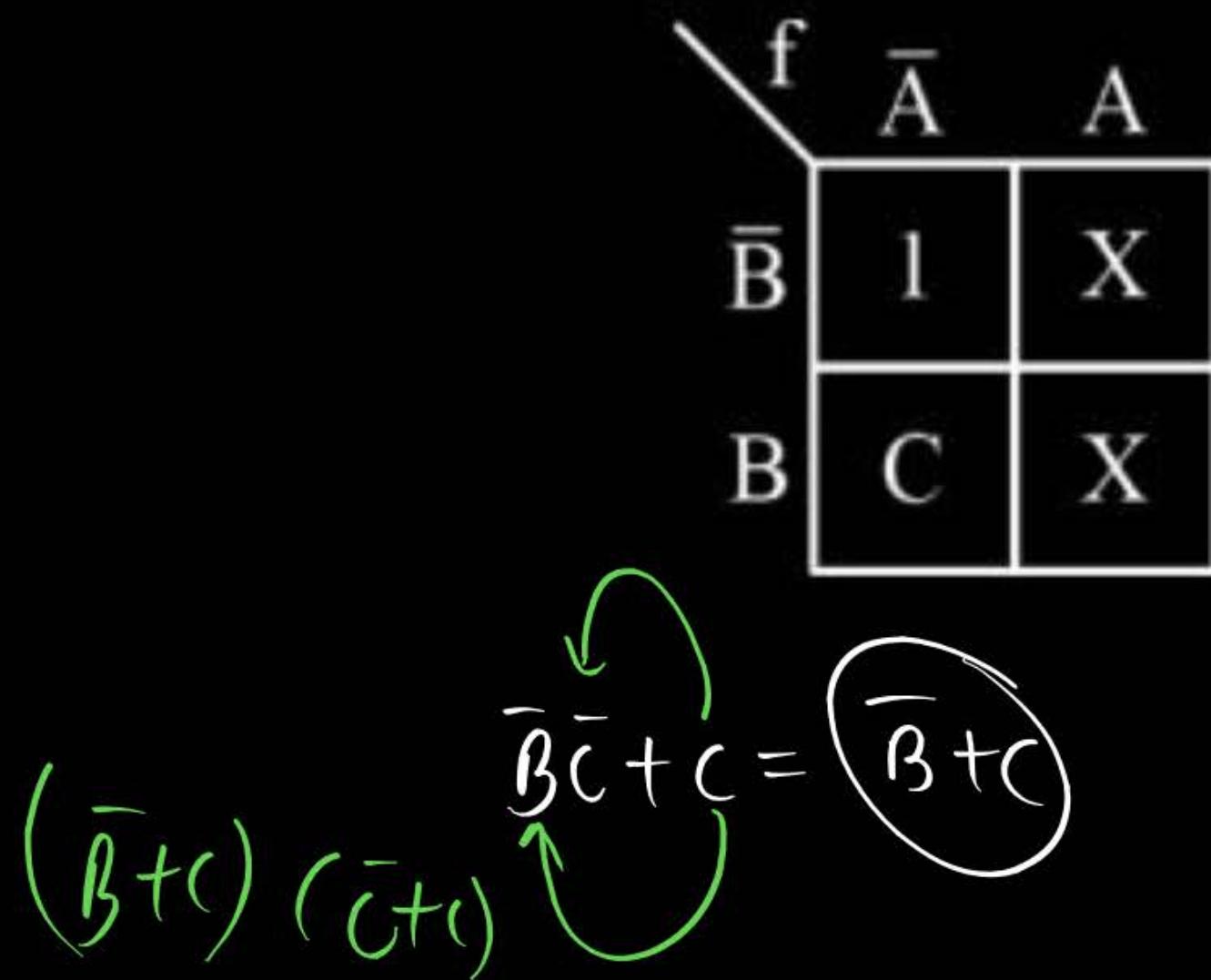
- A** 4
- B** 2
- C** 1
- D** cannot determine

(MCQ)

#Q. Consider the given K-map:

The solution of the K-map is:

- A** $B + C$
- B** $A + \bar{B}$
- C** $A + \bar{B} + C$
- D** $\bar{B} + C$



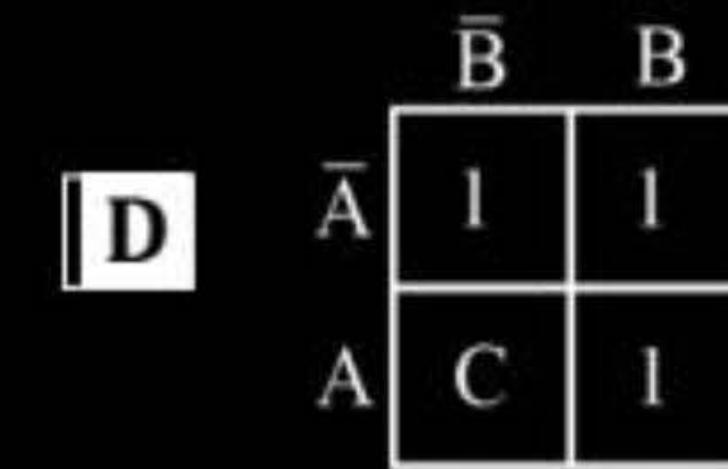
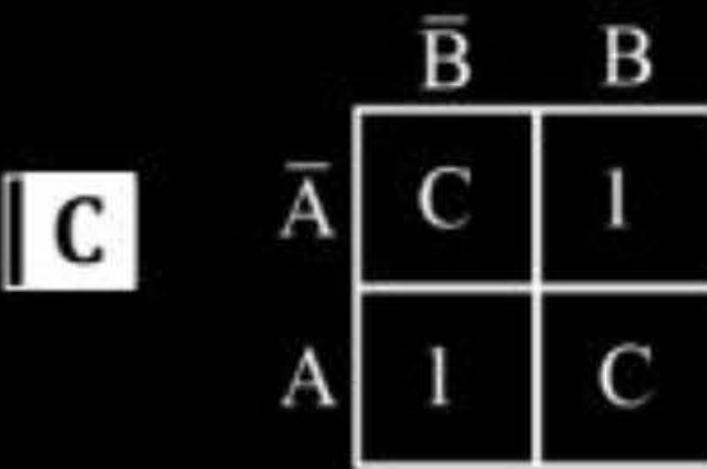
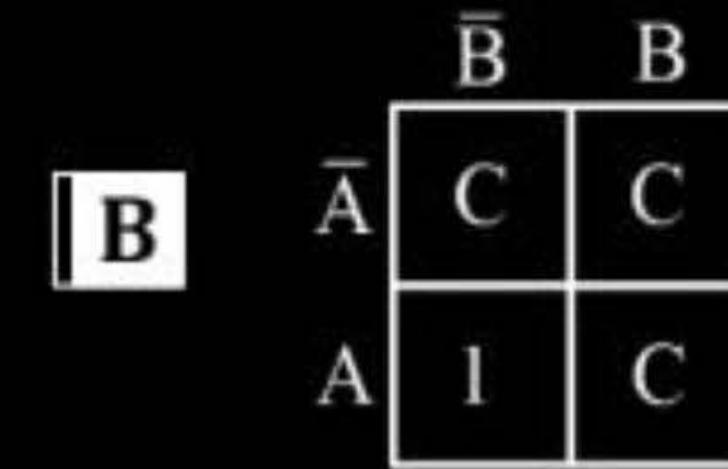
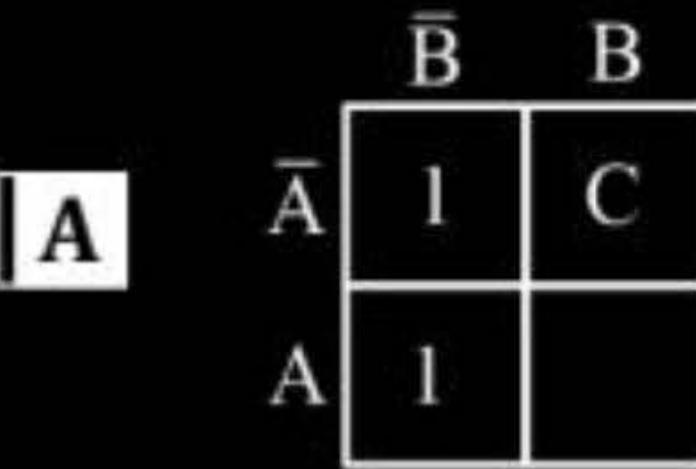
(MCQ)

#Q. Consider the function f,

$$f = A\bar{B} + C$$

Which of the following is the correct K-map of the f.

HW



(MCQ)

#Q. A switching function of four variables, $f(w, x, y, z)$ is equal to the product of two other functions f_1 and f_2 of the same variable, i.e. $f = f_1 f_2$. The function f and f_1 are as follows:

$$f = \sum m(4, 7, 15)$$

$$f_1 = \prod M(5, 6, 12, 13, 14)$$

The number of full specified function f_2 , that will satisfy the given condition is

- A** 32
- B** 16
- C** 4
- D** 1

(MCQ)

#Q. How many maxterms, does the minimal switching function,
 $f(v, w, x, y, z) = \bar{w} + y\bar{z}$
originally have?

- A** 20
- B** 2
- C** 12
- D** 3

#Q. Which of the following statements is/are correct?

- A** The number count of maxterms and min-terms in the expression $f_3(x_1, x_2, x_3, x_4) = 0$ are 16 and 0 respectively.
- B** $(\text{min-term})^c = (\text{maxterm})$
- C** If function $f(A, B, C)$ is expressed by 3 min-terms, then maxterm expression also needs 3 terms to express $f(A, B, C)$
- D** Only essential prime implicant terms are used to write minimized expression

(MCQ)

#Q. Consider 11-variable of inputs are connected to an Ex-NOR gate, the number of min-terms in the Boolean expression of the output of Ex-NOR gate will be

- A** 256
- B** 1024
- C** 512
- D** 2048

(MCQ)

#Q. A 3-Input majority gate is defined by the logic function $f(x, y, z) = (x+y)(y+z)(z+x)$. Which one of the following gates is represented by the function $M(\overline{M(x, y, z)}, M(x, y, \bar{z}), z)$?

- A** 3-Input NAND gate
- B** 3-Input XOR gate
- C** 3-Input NOR gate
- D** 3-Input XNOR gate



Thank You
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CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No. - 5



By - CHANDAN SIR

Recap of Previous Lecture



K-Map

Topics to be Covered



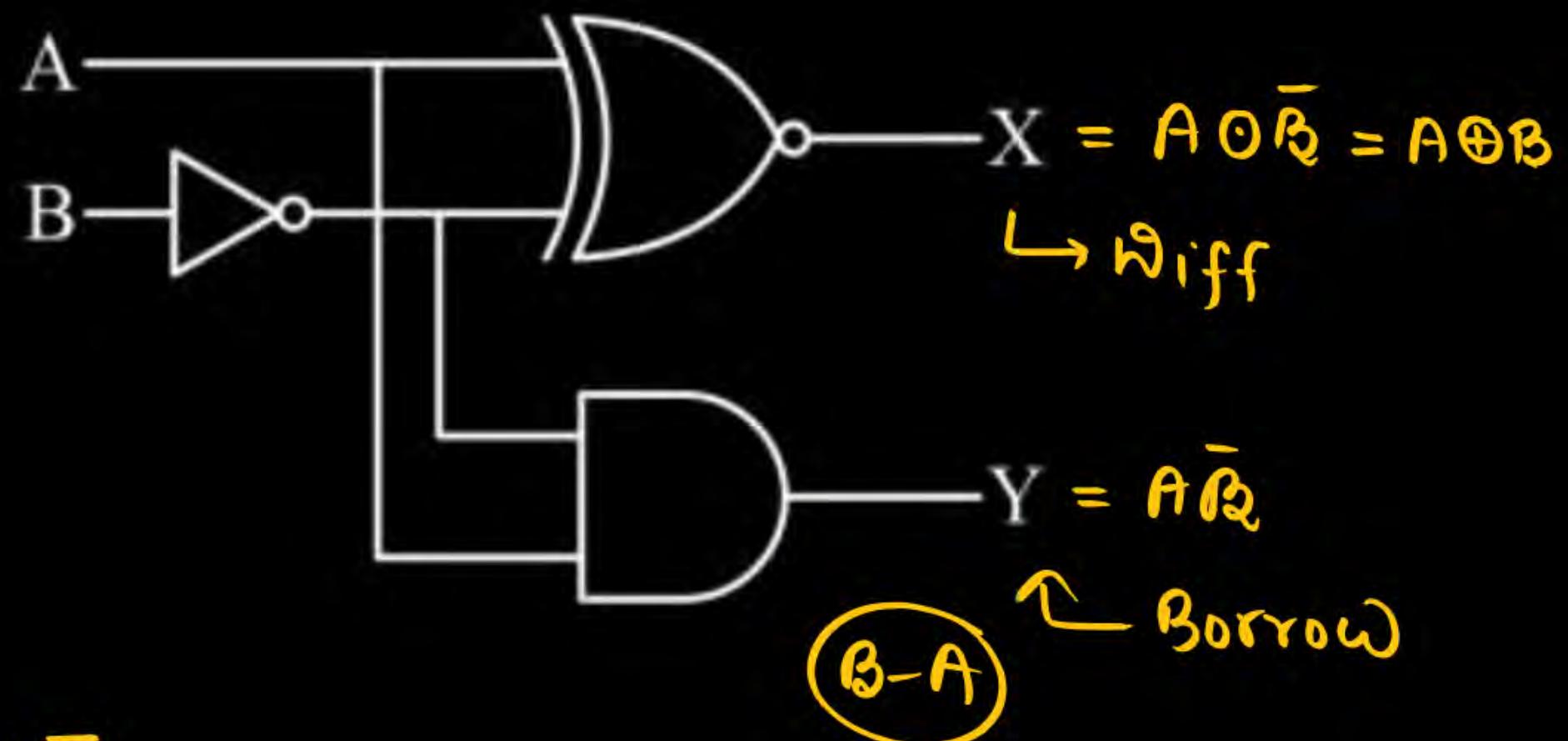
Combination Circuit

Questions Practice

(MCQ)P
W

#Q. The digital circuit shown below is a,

- A Half adder
- B Code converter
- C Half subtractor ($A - B$)
- D Half subtractor ($B - A$)



$$\begin{aligned}A \Theta \bar{B} &= \bar{A} \bar{B} + A \bar{B} \\&= \bar{A} B + A \bar{B} = A \oplus B\end{aligned}$$



#Q. Manufacturer A implements 5-bit parallel adder by using FA only.
Manufacturer B implements 5-bit parallel adder by using HA and OR gate.

Cost of,

$$1 \text{ FA} = 2 \text{ unit}$$

$$1 \text{ HA} = 1 \text{ unit}$$

$$1 \text{ OR gate} = 0.25 \text{ unit}$$

The cost difference between manufacturer A and B is 0

$$A : 5 \text{ FA} = 5 \times 2 \text{ unit} = 10 \text{ unit}$$

$$B : (n-1) \text{ HA} + (n-1) \text{ OR}$$

$$9 \text{ HA} + 4 \text{ OR} = 9 \times 1 \text{ unit} + 4 \times 0.25 \text{ unit} \\ = 10 \text{ unit}$$

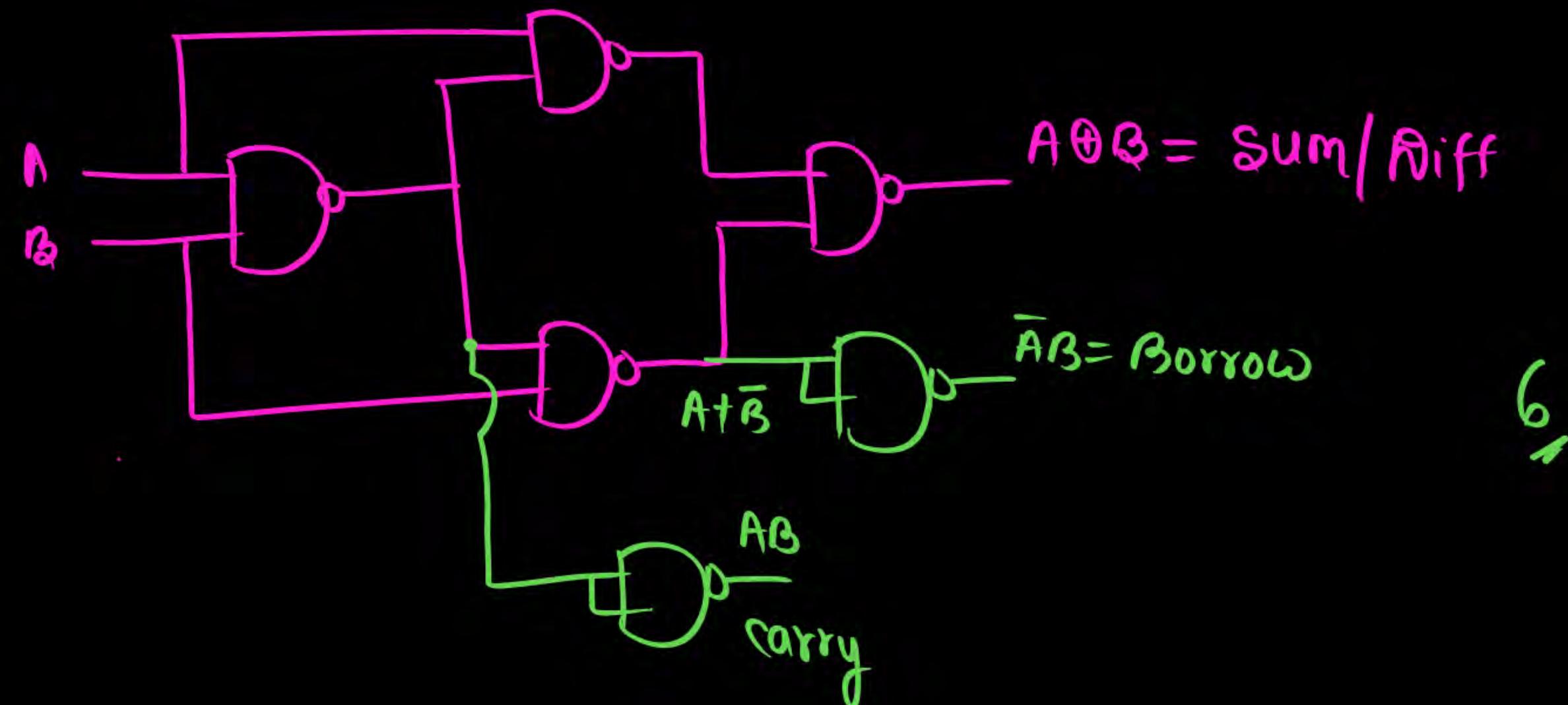
n bit Parallel adder

- ① $(n-1)$ FA + 1 HA
 - ② $n \cdot$ FA
 - ③ $(2n-1)$ HA + $(n-1)$ OR GATE
- A →
- B →


$$\begin{aligned}\bar{A} \oplus B &= \bar{A} \cdot B + \bar{A} \cdot \bar{B} \\ &= AB + \bar{A}\bar{B} \\ &= A \oplus B\end{aligned}$$



#Q. A manufacturer wants to make single IC to realize HA and HS. The used number of NAND gate will be ____.



H.A.

$$S = A \oplus B$$

$$\text{Carry} = AB$$

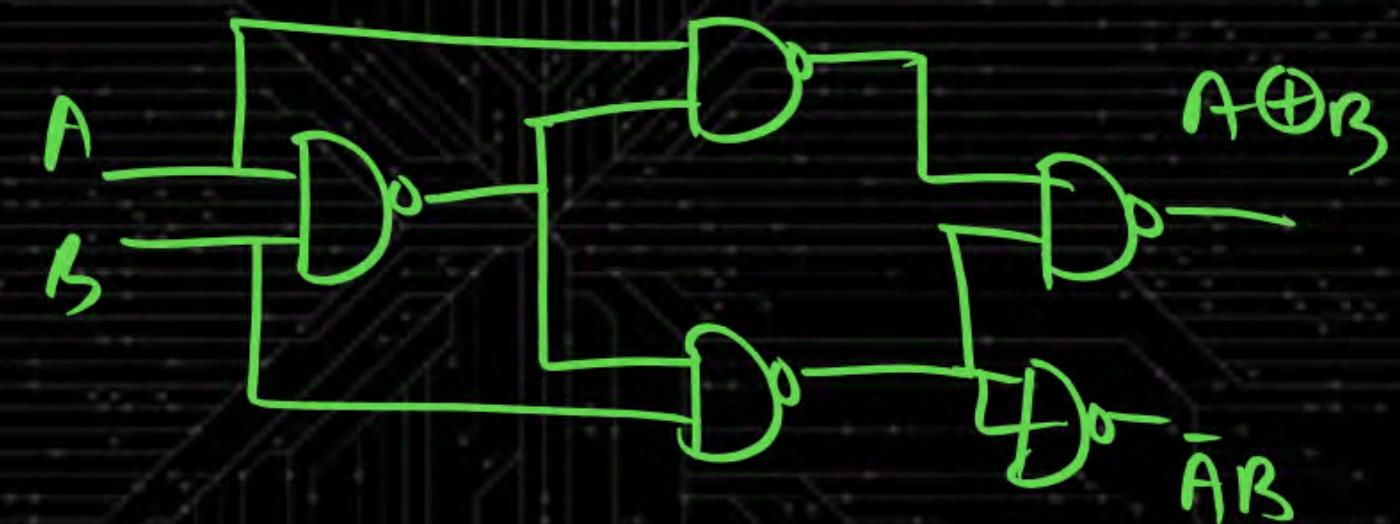
$$\text{NAND/NOR} = 5$$

H.S.

$$\text{Diff} = A \oplus B$$

$$\text{Borrow} = \bar{A}B$$

$$\text{NAND/NOR} = 5$$



F.A

$$\text{Sum} = A \oplus B \oplus C = \sum m(1, 2, 4, 7)$$

$$\begin{aligned}\text{Carry} &= \sum m(3, 5, 6, 7) \\ &= (\underline{A \oplus B})C + AB \\ &= AB + BC + AC\end{aligned}$$

→ Majority input high logic

$$\text{NAND} | \text{NOR} = 9$$

F.S.

$$\text{Riff} = A \oplus B \oplus C = \sum m(1, 2, 4, 7)$$

$$\begin{aligned}\text{Borrow} &= \sum m(1, 2, 3, 7) \\ &= (\overline{A \oplus B})C + \bar{A}B \\ &= \bar{A}B + BC + \bar{A}C\end{aligned}$$

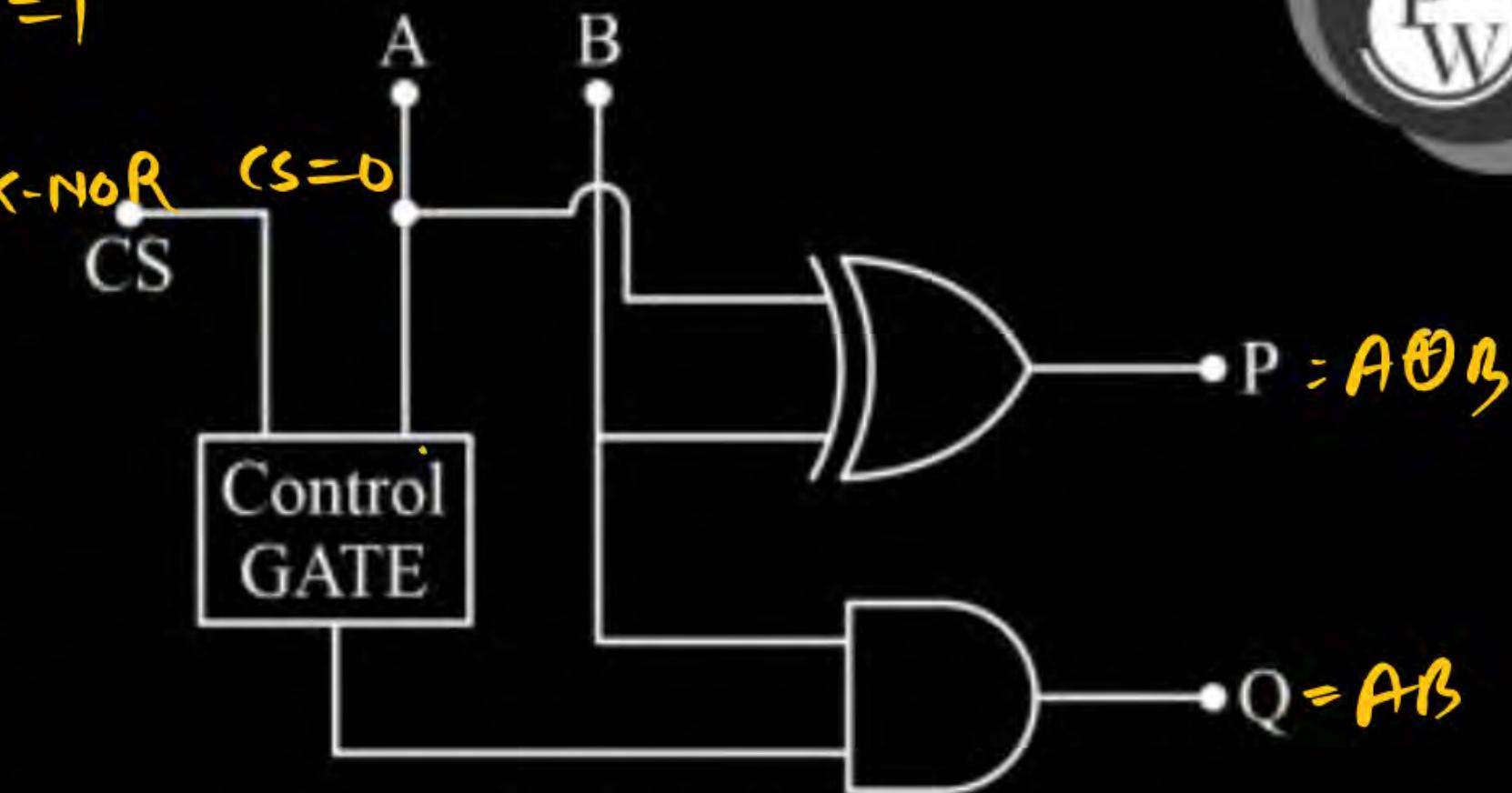
$$\text{NAND} | \text{NOR} = 9$$

(MSQ) $\text{HA} \Rightarrow \text{X-OR } CS=0 \quad \text{X-NOR} \Rightarrow CS=1$

#Q. Consider the digital circuit as

shown below: H.S. $\text{X-OR } CS=1$ $\text{X-NOR } CS=0$

Which of the following condition(s) are required so that this above digital circuit works both as HALF ADDER as well as HALF SUBTRACTOR?



- A** If control gate is Ex-OR and $CS = 0$ then HALF SUBTRACTOR and $CS = 1$ then HALF ADDER.
- B** If control gate is Ex-NOR and $CS = 0$ then HALF SUBTRACTOR and $CS = 1$ then HALF ADDER.
- C** If control gate is Ex-NOR and $CS = 1$ then HALF SUBTRACTOR and $CS = 0$ then HALF ADDER
- D** If control gate is Ex-OR and $CS = 1$ then HALF SUBTRACTOR and $CS = 0$ then HALF ADDER.

$$A \oplus A = 0$$

$$A \oplus \bar{A} = 1$$



(MCQ)

#Q. If A and B are the MSB's of two numbers and carry in for MSB bit is (C_{in}). After adding this if we get carry out (C_{out}). Then if we realize the overflow concept by an Ex-OR gate as shown below:
For “overflow” will occur during addition, the value of Y will be

- A 1
- B 0
- C $C_{in} \oplus C_{out}$
- D $\overline{C_{in} \oplus C_{out}}$



Overflow

$$\begin{array}{r} 0 \\ 0 \\ \hline 1 \end{array}$$

$c_{out} = 0$

$$c_{in} = 1$$

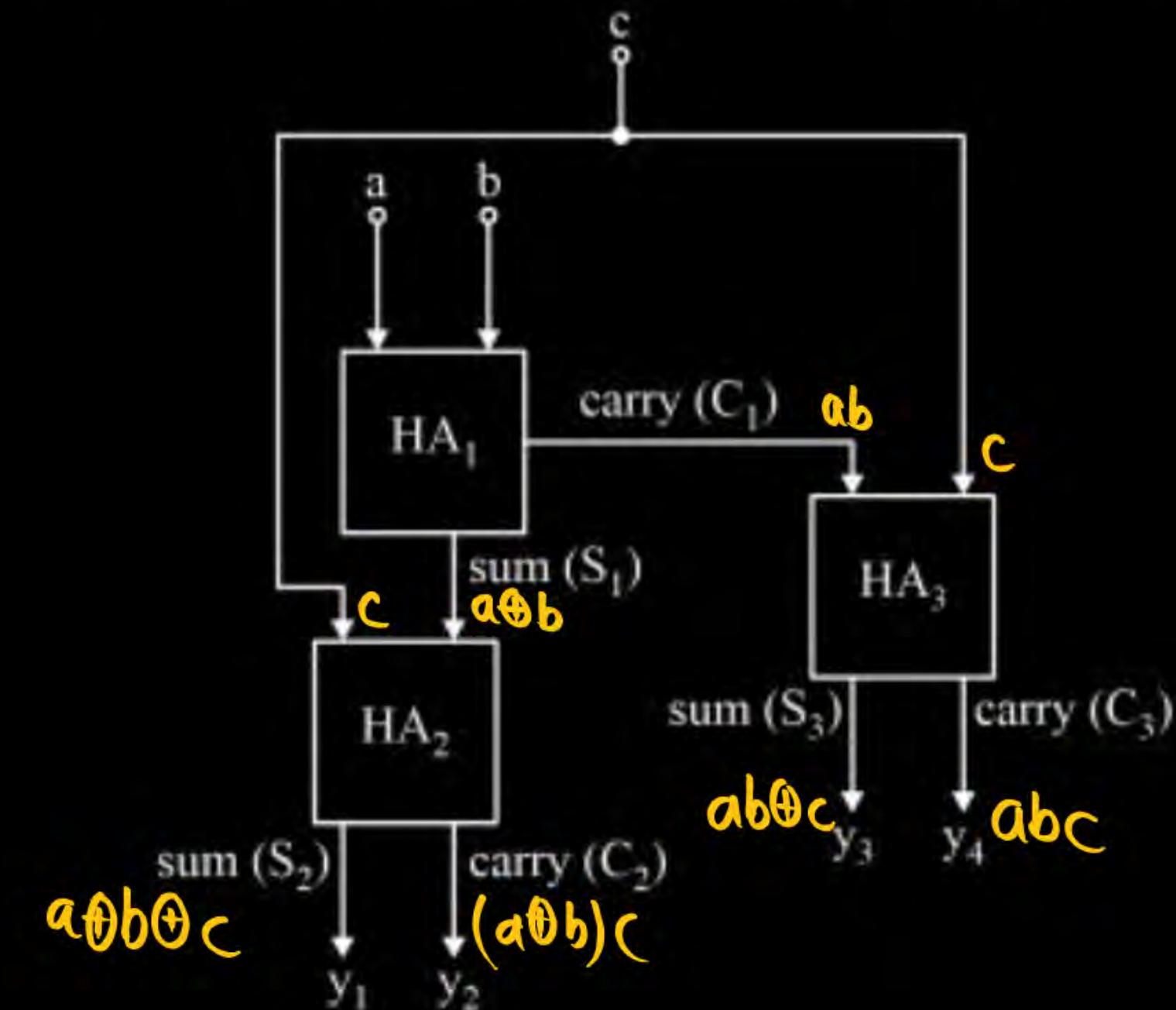
$$\begin{array}{r} 1 \\ 1 \\ \hline 0 \end{array}$$

$c_{out} = 1$

$$c_{in} = 0$$

#Q. Three half adders HA_1 , HA_2 and HA_3 are inter-coupled as shown below. The four output functions y_1 , y_2 , y_3 and y_4 are expressed in terms of inputs a , b and c . Which one of the following output expressions is correct?

- A** $y_1 = (a \oplus b) c$ ✗
- B** $y_2 = (a \oplus b) \oplus c$ ✘
- C** $y_3 = ab \oplus c$ ✓
- D** $y_4 = abc$ ✓



(MCQ)

#Q. A 1-bit Full Adder circuit takes 5 ns to generate carry-out bit and 2ns for the sum-bit. When 4, 1-bit Full Adders are cascaded then the maximum rate of addition/second will be

A 10^7

B 5×10^7

C 3×10^7

D 4×10^7

$$T = (n-1)T_{\text{carry}} + \text{Max}\{T_{\text{sum}}, T_{\text{carry}}\}$$

$$= 3 \times 5 \text{ ns} + 5 \text{ ns} = 20 \text{ ns}$$

$$\frac{1}{T} = \frac{10^9}{20} \text{ 1/sec.}$$

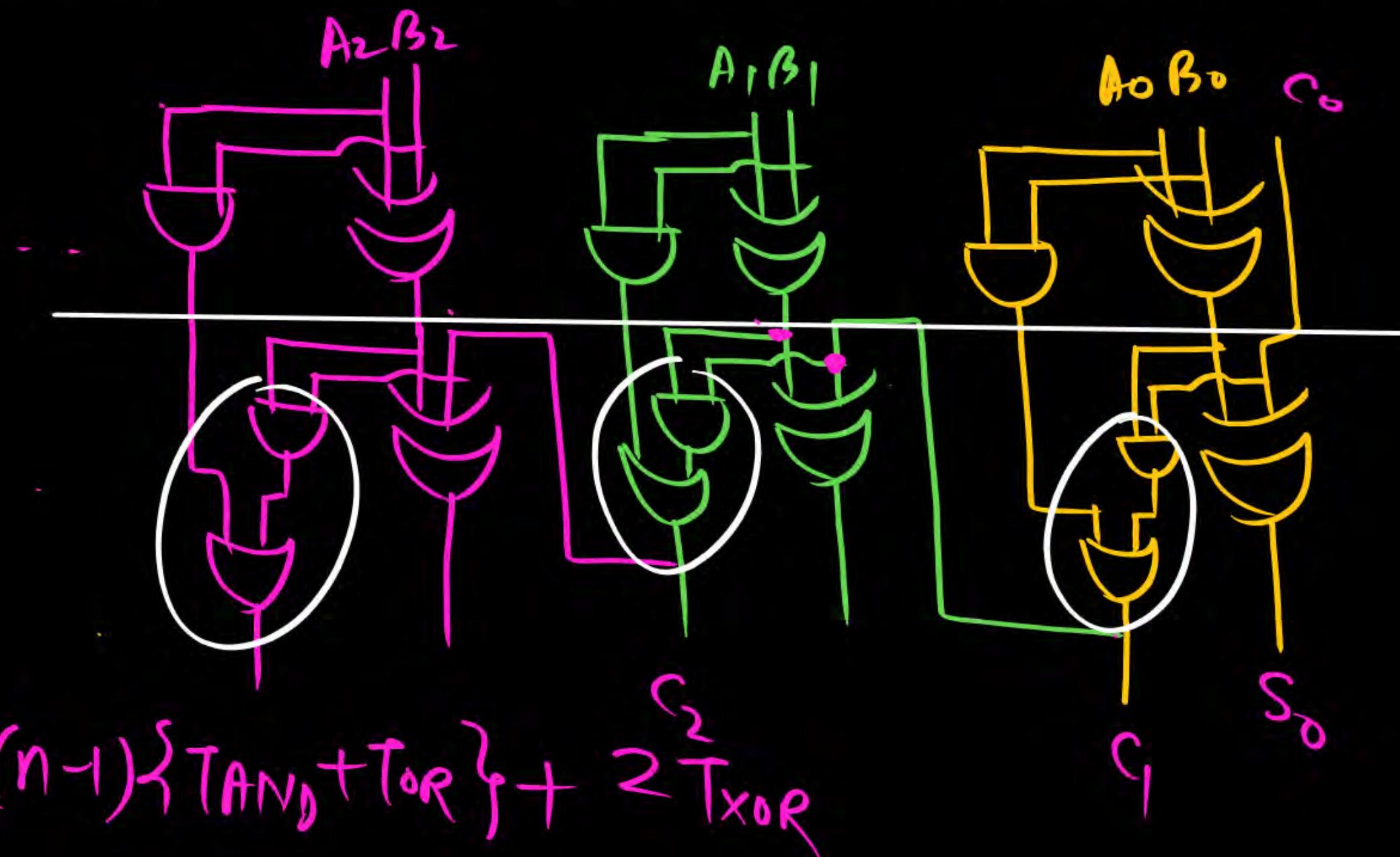
$$= \frac{100 \times 10^7 \text{ add}}{20} / \text{s}$$

$$= 5 \times 10^7 \text{ add/s.}$$

(MCQ)

#Q. For a 10-bit parallel Adder, how many number of gate levels are required for the carry to propagate from input to output?

- A 5
- B 10
- C 25
- D 20



$$T = (n-1) \left\{ T_{AND} + T_{OR} \right\} + 2 T_{XOR}$$

For carry 2 Level GATES required (AND+OR)

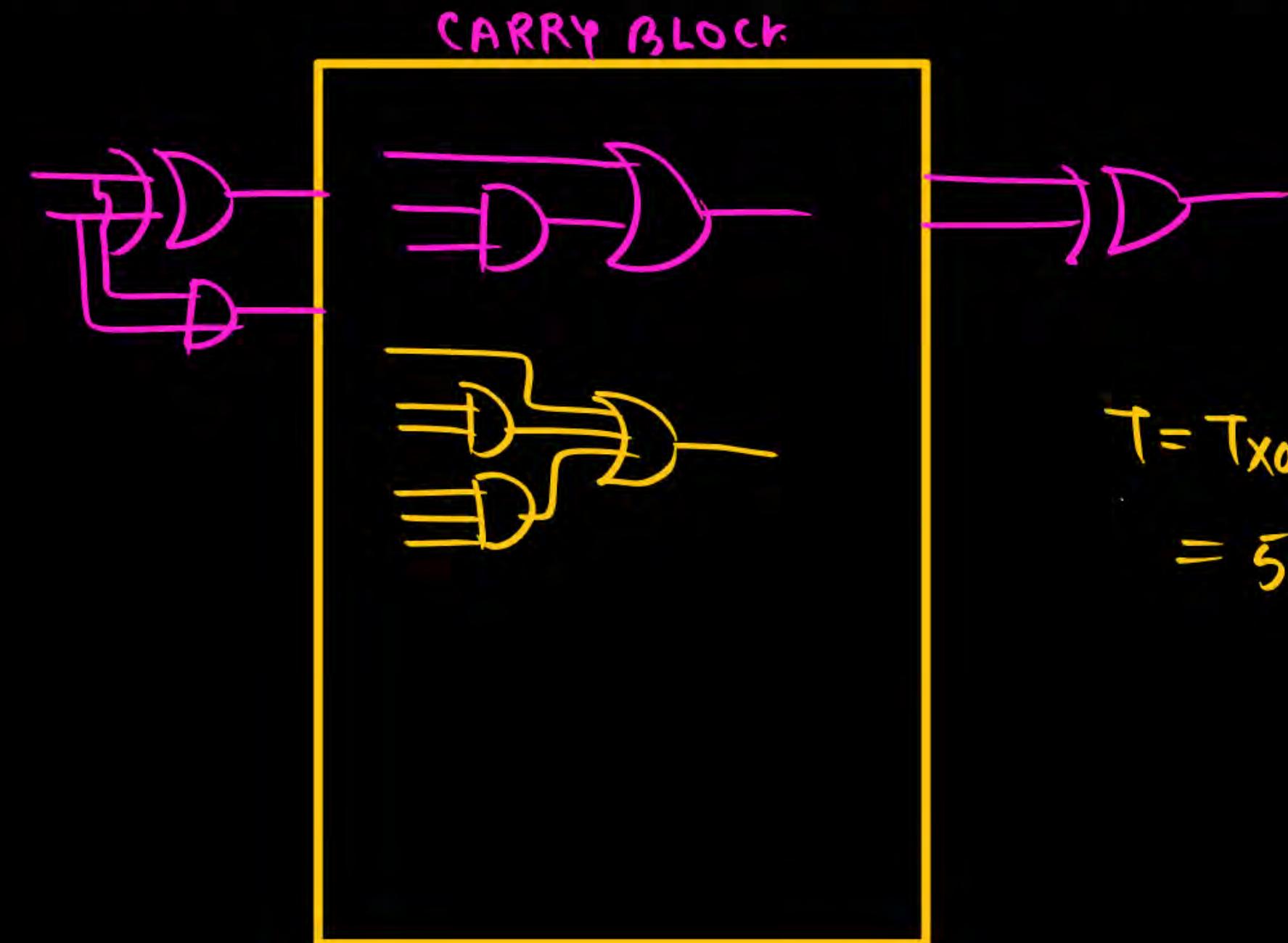
10X2 Level GATE

= 20 Level GATES

(MCQ)

#Q. In a 100-bit carry look ahead adder, the X-OR gate has delay of 5 ns and AND/OR gate has delay of 2 ns each. The sum will appear after delay of

- A 100 ns
- B 500 ns
- C 14 ns
- D 5 ns



$$\begin{aligned} T &= T_{XOR} + T_{AND} + T_{OR} \\ &= 5 + 2 + 2 + 5 = \underline{14 \text{ ns}} \end{aligned}$$

(MCQ)

#Q. A 5-bit parallel adder is designed using 5, 1-bit full adders. Each 1-bit full adder is designed using X-OR, AND and OR gates. The delay contributed by X-OR gate is 10 ns while that contributed by AND/OR gate is 2 ns. The number of additions per second that a 5-bit parallel adder can perform reliably, will be

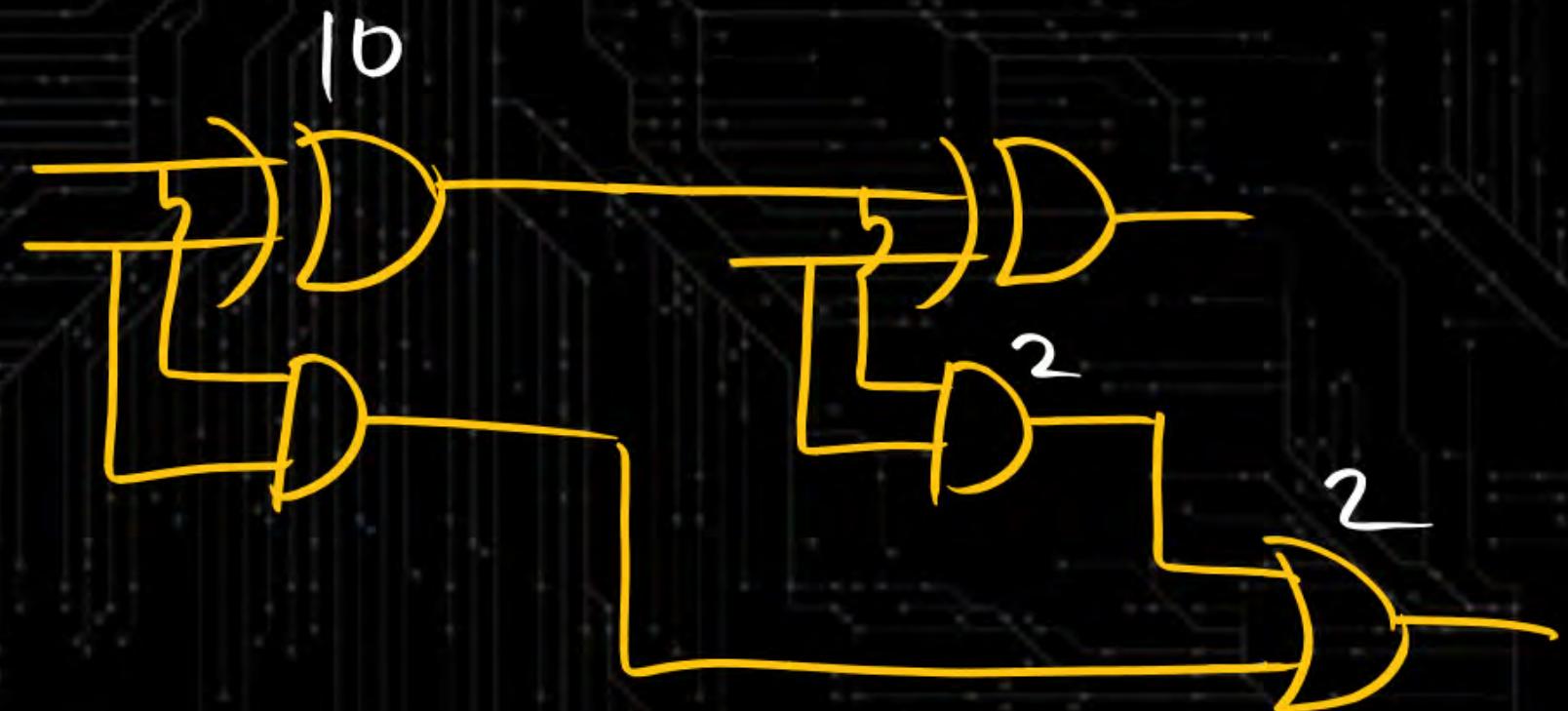
- A** 13.16×10^6
- B** 3.125×10^6 ✓
- C** 3.33×10^6
- D** 4×10^6

$$T = (n-1) \{ T_{AND} + T_{OR} \} + 2 T_{XOR}$$

$$4 \times \{ 4 \} + 20$$

$$T = 36 \text{ ns}$$

$$\frac{1}{T} = \frac{1}{36 \text{ ns}}$$

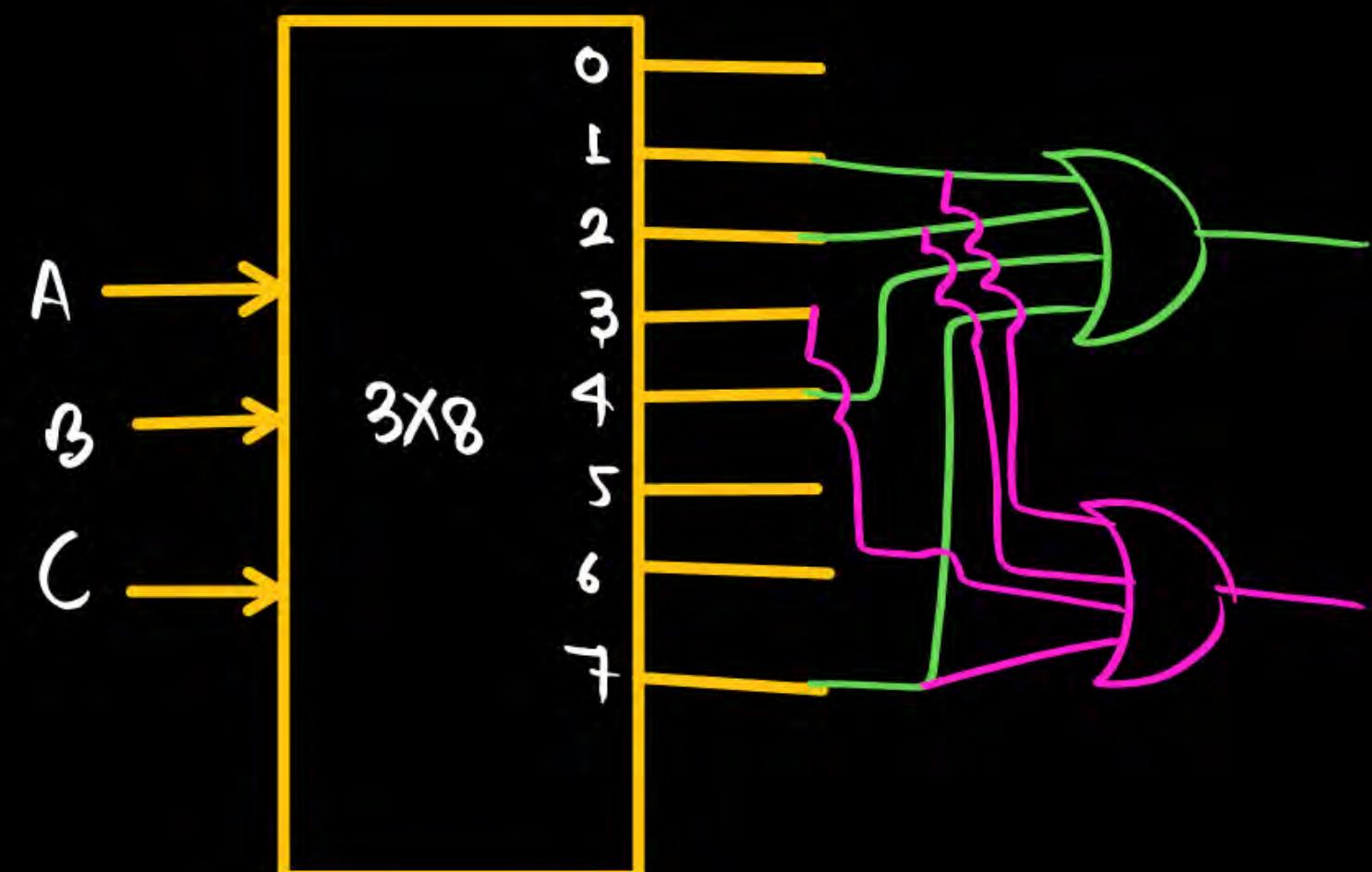


$T_{\text{carry}} = 14 \text{ ns}$

X

#Q. To design a full subtractor, having 3-inputs and two outputs. Then, it may be implemented by

- A** two 3×8 decoder and 2 OR gates
- B** two 3×8 decoder and 3 AND gates
- C** one 3×8 decoder and 2 OR gates
- D** one 4×16 decoder and 2 OR gates



(MCQ)

#Q. Consider a 2 : 1 MUX having propagation delay $t_{pd} = 10 \mu\text{sec}$, then device is referred as,

Ans

- A** Monostable multivibrator
- B** Bistable multivibrator
- C** Astable multivibrator of frequency 50 kHz
- D** pulse train generator of frequency 0.2 MHz

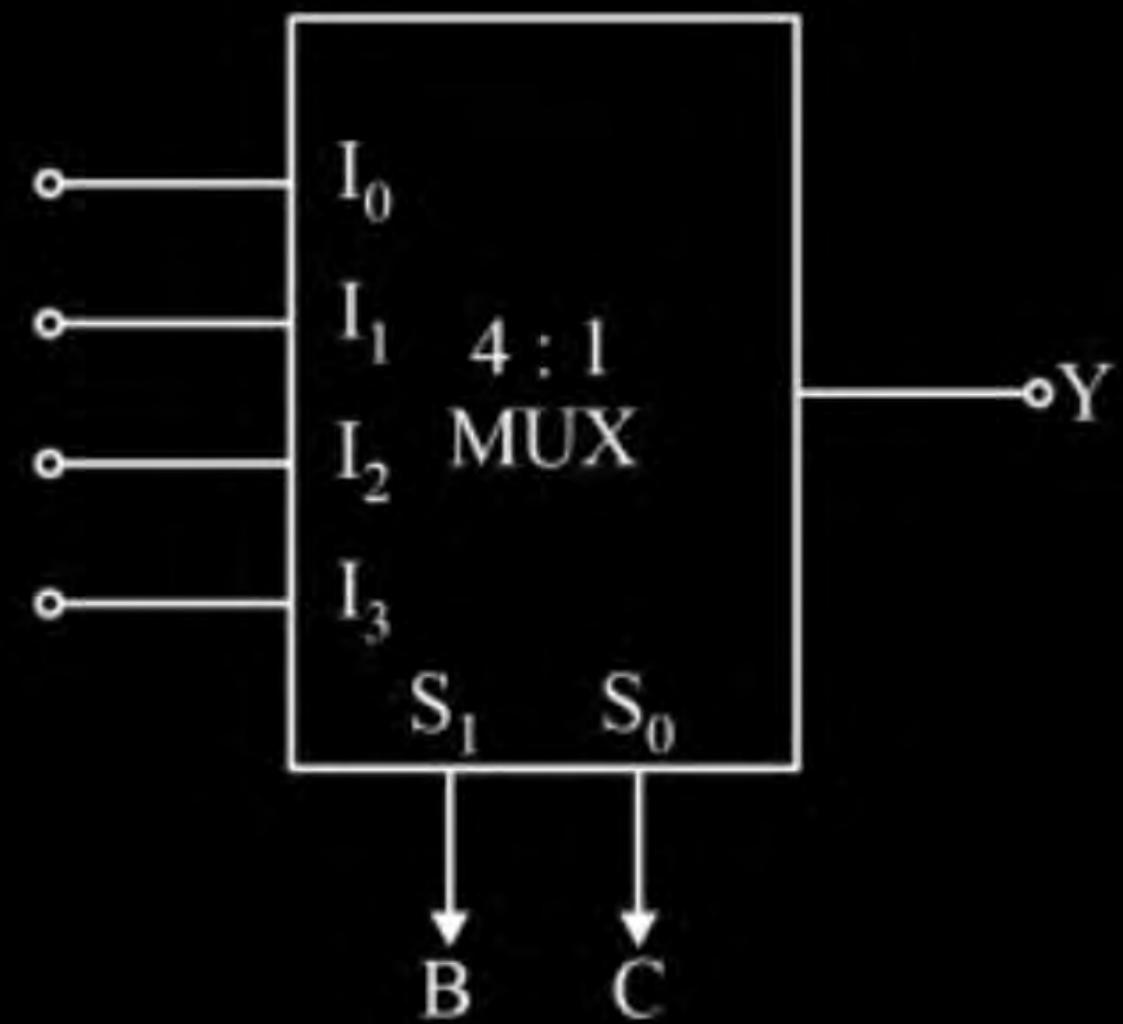


(MCQ)

#Q. The Boolean function $f(A, B, C) = \pi(1, 3, 5, 6)$ is to be implemented by using 4 : 1 MUX having select lines $S_1 = B$ and $S_0 = C$ is shown in figure below.

HW: The required inputs I_0, I_1, I_2, I_3 respectively are,

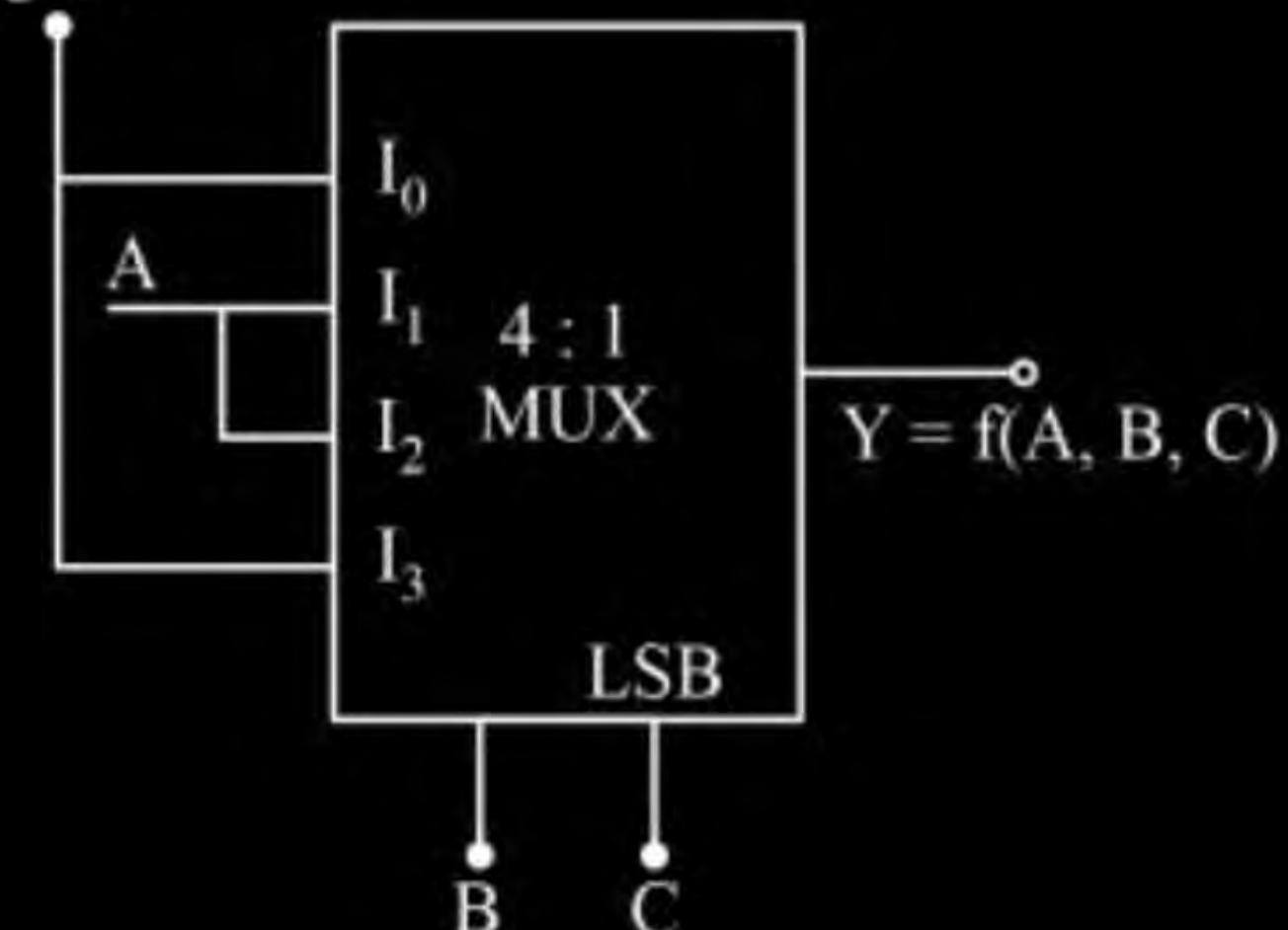
- A** 0, 1, A, \bar{A}
- B** 1, 0, A, \bar{A}
- C** 0, 1, \bar{A} , A
- D** 1, 0, \bar{A} , A



#Q. A 4 : 1 MUX is used to implemented the 3-input (A, B, C) Boolean function as shown in the figure below:
The $f(A, B, C)$ equals to

R.W.

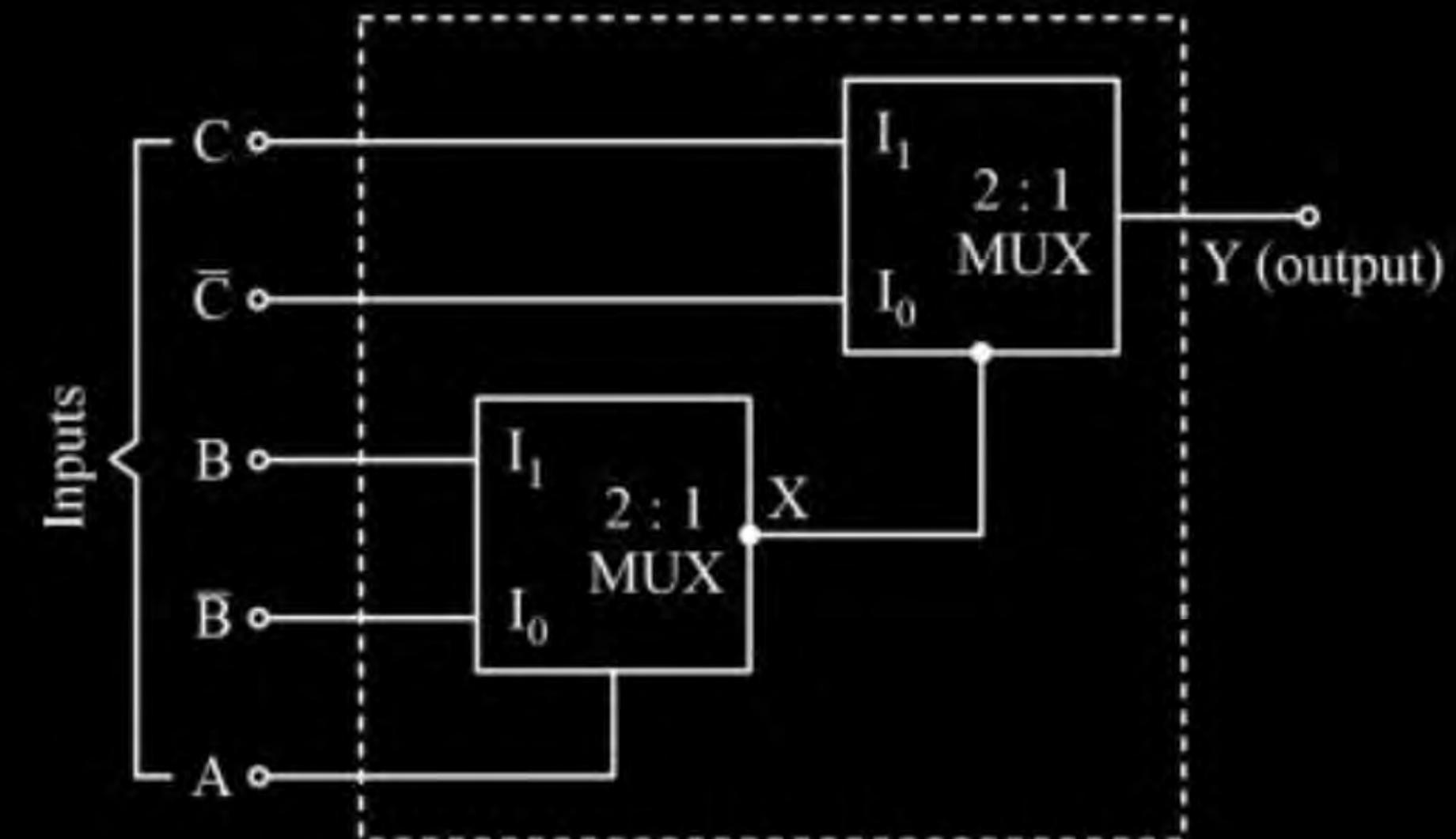
Logic '1'



- [A] $\pi(0, 4, 5, 6, 7)$
- [B] $\Sigma(0, 3, 4, 5, 6, 7)$
- [C] $\Sigma(0, 2, 3, 4, 5, 6, 7)$
- [D] $\pi(1, 2)$

#Q. A cascaded 2 : 1 MUX circuit is shown in the figure below. The no. of NAND gate to implement Boolean function Y is ____.

HW

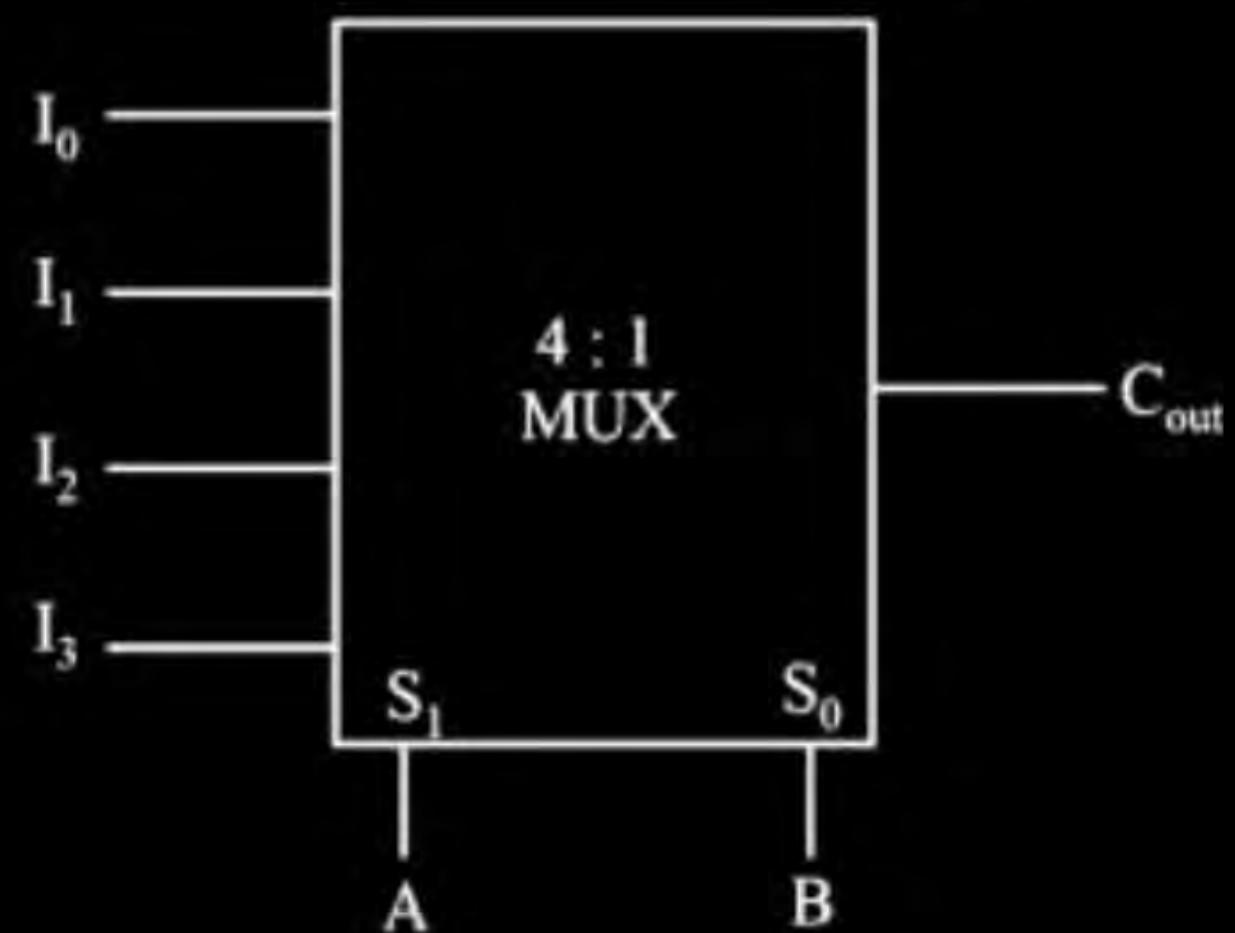


(MCQ)

#Q. A 4 :1 multiplexer is to be used for generating the output carry of a full adder. A and B are the bits to be added while C_{in} is the input carry C_{out} is the output carry. A and B are to be used as the select bits with A being the more significant select bit.

Which one of the following statements correctly describes the choice of signals to be connected to the inputs I_0 , I_1 , I_2 and I_3 so that the output is C_{out} ?

- A** $I_0 = 0$, $I_1 = C_{in}$, $I_2 = C_{in}$ and $I_3 = 1$
- B** $I_0 = 1$, $I_1 = C_{in}$, $I_2 = C_{in}$ and $I_3 = 1$
- C** $I_0 = C_{in}$, $I_1 = 0$, $I_2 = 1$ and $I_3 = C_{in}$
- D** $I_0 = 0$, $I_1 = C_{in}$, $I_2 = 1$ and $I_3 = C_{in}$





2 Minute Summary



Topic

at.me/cJSIR

Base = 8
7's
8's

Base 10
9
10

$$\begin{array}{r} 777 \\ 236 \\ \hline 541 \text{ R } 8 \end{array}$$

$$\begin{array}{r} 999 \\ 236 \\ \hline 763 \end{array}$$



Thank You
GW
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CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No. - 6



By - CHANDAN SIR

Recap of Previous Lecture



Combinational Circuit

Topics to be Covered



Combinational Circuit

Questions Practice



Topic : Combinational Circuit



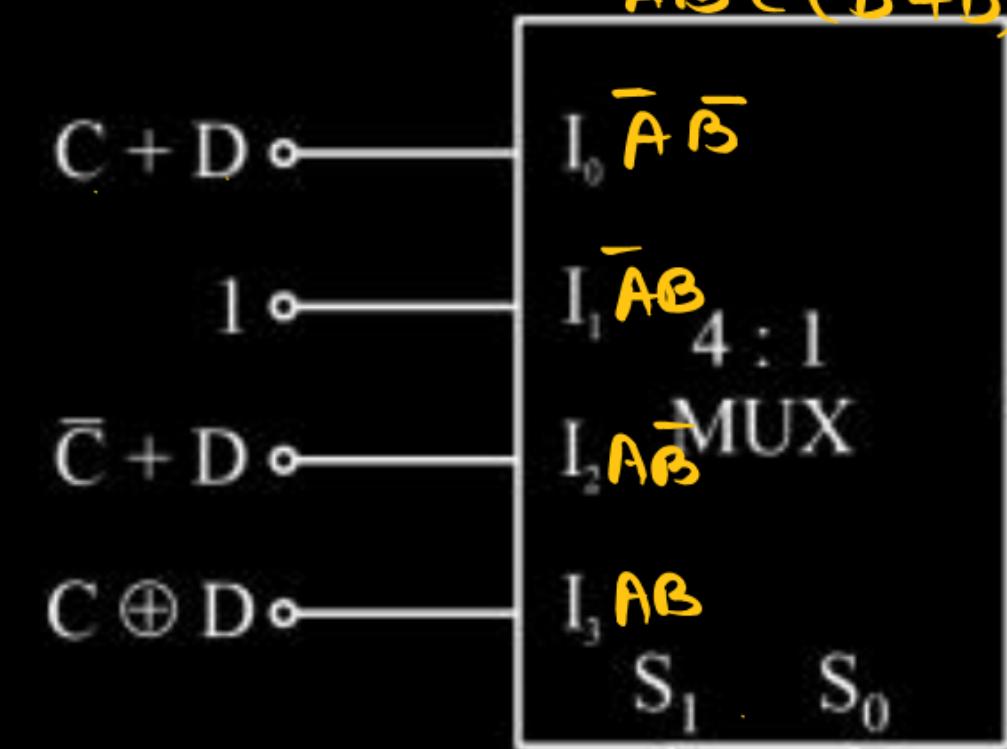
(MCQ)

#Q. Find maxterm expression of f.

- A $\prod M(0, 10, 12, 15)$
- B $\sum m(3, 5, 10, 14)$
- C $\sum m(8, 10, 12, 14, 15)$
- D $\prod M(2, 3, 8, 7, 10, 12, 15)$

$$\bar{A}\bar{B}((+D) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{D}$$

$$\bar{A}\bar{B}C(\bar{D}+D) + \bar{A}\bar{B}C(\bar{C}+D)D$$



$$\prod M(0, 10, 12, 15)$$

$$f(A, B, C, D)$$

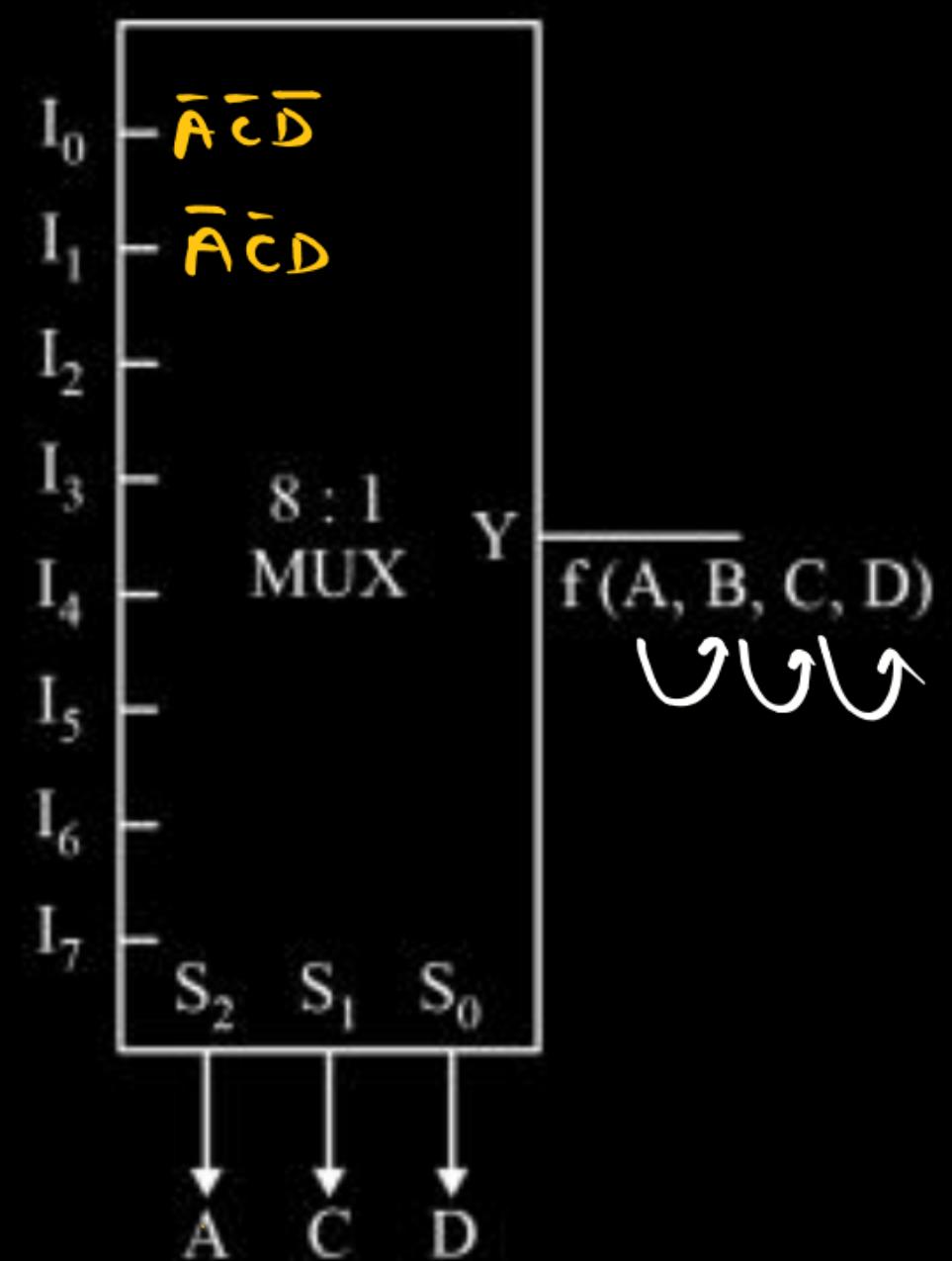
$$= \sum m(1, 2, 3, 4, 5, 6, 7, 8, 9, 11, 13, 14)$$

$\bar{A}\bar{B}\bar{D}$	$\bar{A}\bar{B}D$	$\bar{A}B\bar{D}$	$A\bar{B}\bar{C}$	$A\bar{B}D$	A	B	$AB\bar{C}D$	$AB\bar{C}\bar{D}$
0010	0001	0100	1000	1001	1101	1110		
0011		0101	1001	1011				
		0110						
		0111						

(MCQ)

#Q. Find the value of Pin I_2 , I_4 , I_7 . $f(A, B, C, D) = \sum m(1, 2, 3, 4, 5, 7, 8, 10, 12, 14, 15)$

- A** $I_2 = 1, I_4 = B, I_7 = 1$
- B** $I_2 = 1, I_4 = \bar{B}, I_7 = 0$
- C** $\cancel{I_2 = \bar{B}, I_4 = 1, I_7 = B}$
- D** $I_2 = 0, I_4 = 0, I_7 = \bar{B}$

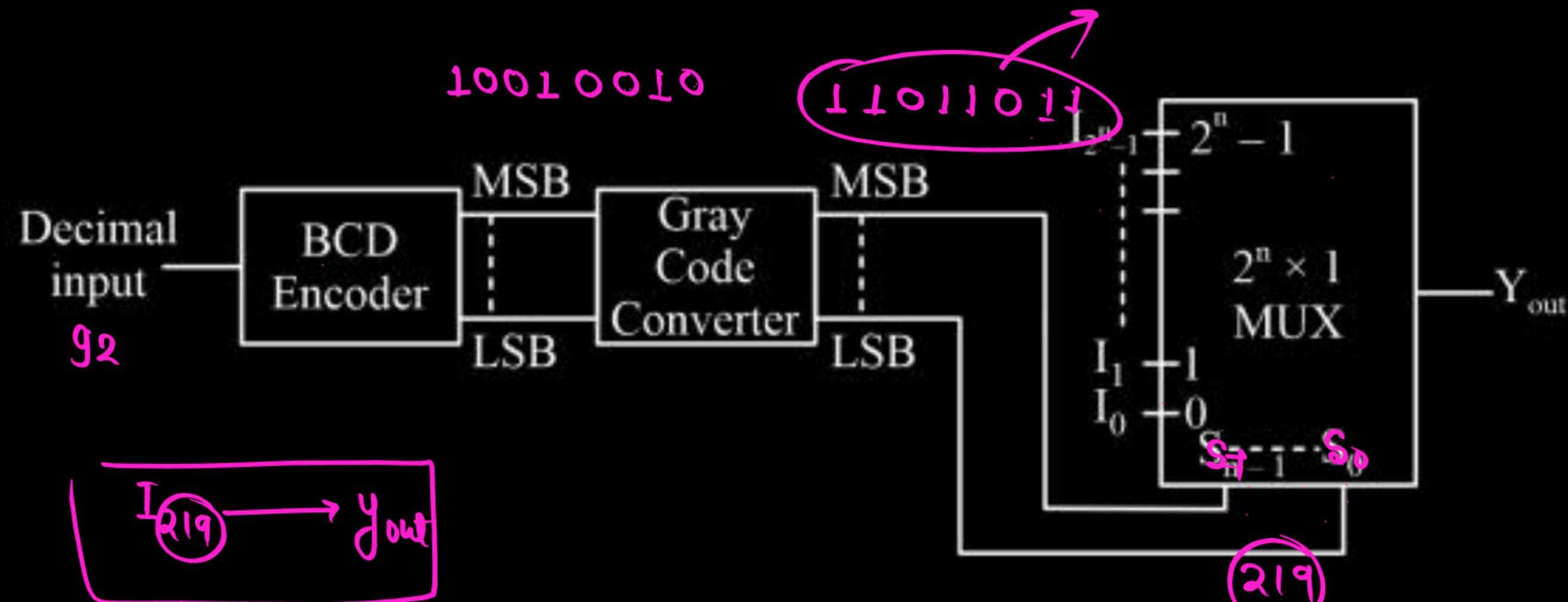


0010.

	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7
	$\bar{A}\bar{C}\bar{D}$	$\bar{A}\bar{C}D$	$\bar{A}C\bar{D}$	$\bar{A}CD$	$A\bar{C}\bar{D}$	$A\bar{C}D$	$AC\bar{D}$	ACD
\bar{B}	0	1	2	3	8	9	10	11
B	4	5	6	7	12	13	14	15
B	1	\bar{B}	1	1	0	1	B	.

(NAT)

#Q. Consider the circuit given below.



If the decimal input is **92** then Y_{out} corresponds to I_m , then value of m is ____.

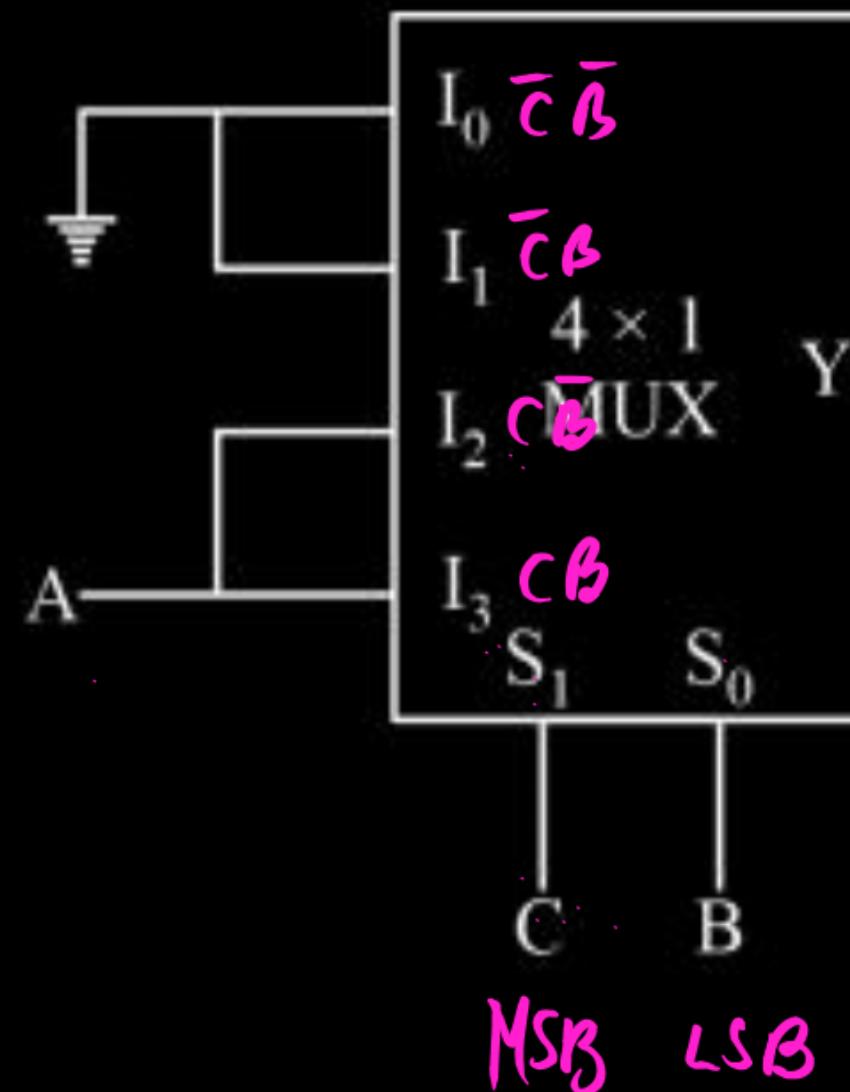
$$m = 219$$

(MCQ)

#Q. Consider the MUX circuit shown in the figure below:

The output function $f(A, B, C)$ can be represented as

- A** $\sum m(6, 7)$
- B** $\sum m(3, 7)$
- C** ~~$\prod m(0, 1, 2, 3, 4, 6)$~~
- D** $\prod m(0, 1, 7)$

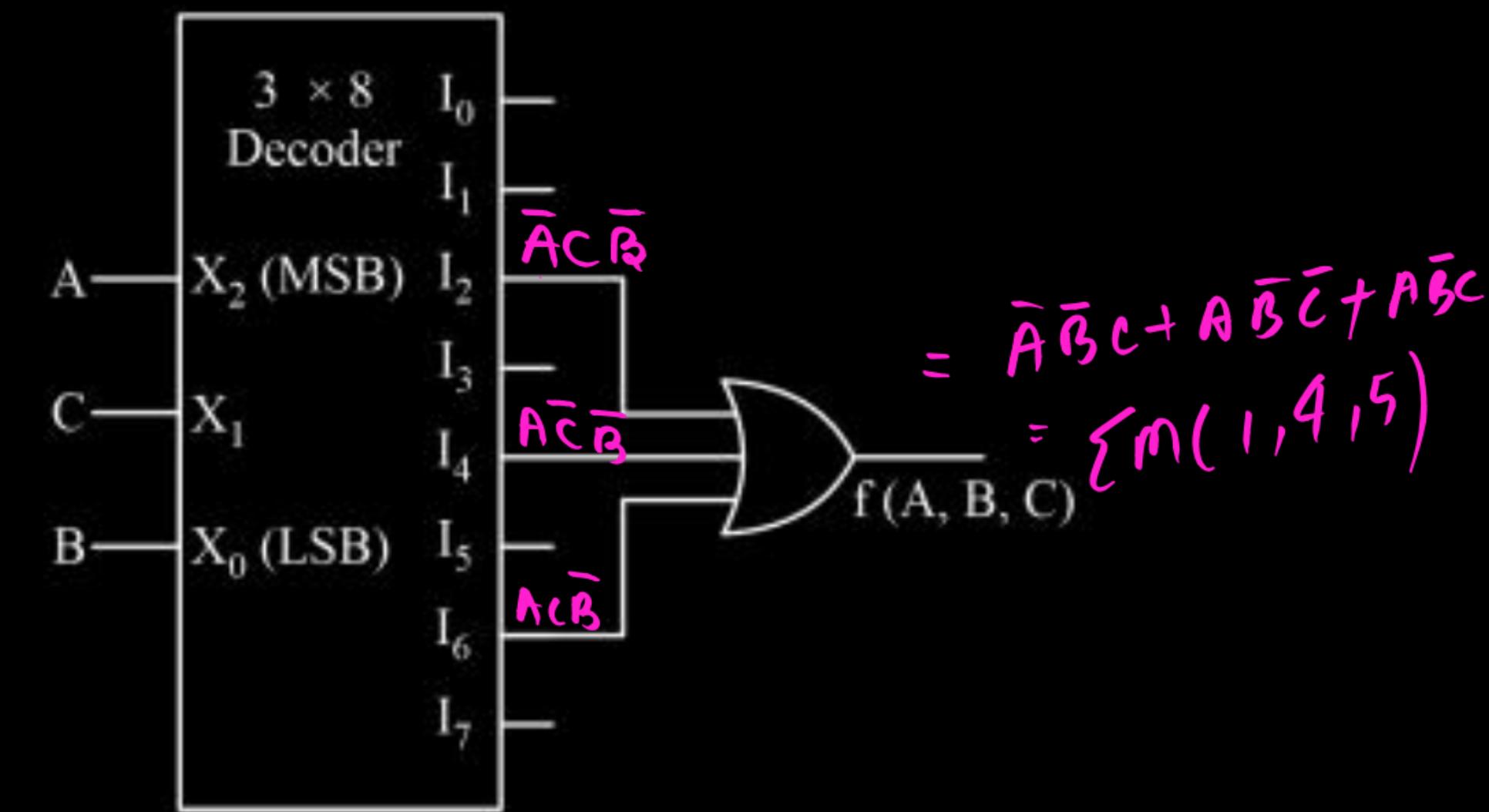


$$\begin{aligned}
 & \cancel{\bar{S}_1 S_0 I_0} + \cancel{\bar{S}_1 S_0 I_1} + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3 \\
 & \bar{C} \bar{B} A + C \bar{B} A \\
 & f = C \bar{B} A + C B A \\
 & f = A \bar{B} C + A B C \\
 & = \sum m(5, 7) \\
 & f = \prod m(0, 1, 2, 3, 4, 6)
 \end{aligned}$$

(MCQ)

#Q. A function $f(A, B, C)$ is to be implemented using an 3×8 decoder, where A is the MSB of the function and C is the LSB of the function at the output. If the connections of the input to the decoder are as shown in the figure below, then the function $f(A, B, C)$ can be expressed as

- A** $f(A, B, C) = \sum m(2, 4, 6)$
- B** $f(A, B, C) = \prod M(0, 1, 7)$
- C** $f(A, B, C) = \prod M(2, 4, 6)$
- D** $f(A, B, C) = \sum m(1, 4, 5)$



#Q. Consider two binary numbers y_2 and y_1 . Here y_2 is 5-bit number and y_1 is 3-bit number. The number of maxterm in $f(y_2 > y_1)$ will be ____.

$$\begin{array}{ccc} y_2 & > & y_1 \\ \left. \begin{array}{c} a_4, a_3 \\ 0, 1 \\ 1, 0 \\ 1, 1 \end{array} \right\} & & \left. \begin{array}{c} a_2, a_1, a_0 \\ 0, 0, 0 \\ 0, 0, 0 \end{array} \right\} \\ 2^6 = 64 & & 2^3 = 8 \\ & & 64 \\ & & 64 \\ \hline & & 192 \end{array}$$

$y_2 > y_1$

Total combination = 256

$$\begin{matrix} X \\ a_4 \ a_3 \quad (a_2 \ a_1 \ a_0 > b_2 \ b_1 \ b_0) \\ 0 \ \ 0 \end{matrix}$$

For 3 bit
 $(y_2 > y_1) : \frac{2^{2n} - 2^n}{2} = \frac{64 - 8}{2} = 28$

$$y_2 > y_1 = 192 + 28$$

$$\begin{matrix} 220 \\ \equiv \\ \text{minterm} \end{matrix} \quad 256 - 220 = 36 \quad \text{Maxterm}$$

$$8 \text{ bit} \rightarrow \text{Total combination} \\ = 256$$

$$\begin{array}{c} y_2 \\ y_1 \end{array} \quad \begin{array}{c} a_4 \ a_3 \ \textcolor{red}{a_2 \ a_1 \ a_0} \\ b_2 \ b_1 \ b_0 \end{array}$$

$$\left\{ \begin{array}{l} 0 \\ 0 \\ 0 \end{array} \right\} \left\{ \begin{array}{l} 0 \\ 1 \\ 1 \end{array} \right\} \left\{ \begin{array}{l} 0 \\ 0 \\ 1 \end{array} \right\} > \left\{ \begin{array}{l} 0 \\ 1 \\ 1 \end{array} \right\} \left\{ \begin{array}{l} 0 \\ 1 \\ 0 \end{array} \right\} \left\{ \begin{array}{l} 0 \\ 0 \\ 1 \end{array} \right\} \} \text{ 64 combination}$$

$$64 + 64 + 64 + 2^8 = \underline{\underline{220}}$$

$$\text{Maxterm} = 256 - 2^{20}$$

$$= \underline{\underline{36}}$$

#Q. Consider two binary numbers A and B. Here A is 3-bit number and B is 2-bit number. The number of minterm in $f(B > A)$ will be 6.

A	B	$B > A$
$a_2 \ a_1 \ a_0$	$b_1 \ b_0$	
0 0 0	0 0	
0 0 0	0 1	
0 0 0	1 0	
⋮ ⋮ ⋮	⋮ ⋮ ⋮	
0 1 1	1 1	
1 0 0	0 0	
1 0 0	0 1	
1 0 0	1 0	
⋮ ⋮ ⋮	⋮ ⋮ ⋮	
1 1 1	1 1	

$\left\{ \right. \quad \left. \right\} 16$

$16 \rightarrow A > B \times$

2 bit comparator

$$B > A \Rightarrow \frac{2^{2n} - 2^n}{2} = \frac{16 - 4}{2} = 6$$

#Q. To implement 1:128 De MUX, we require,

410

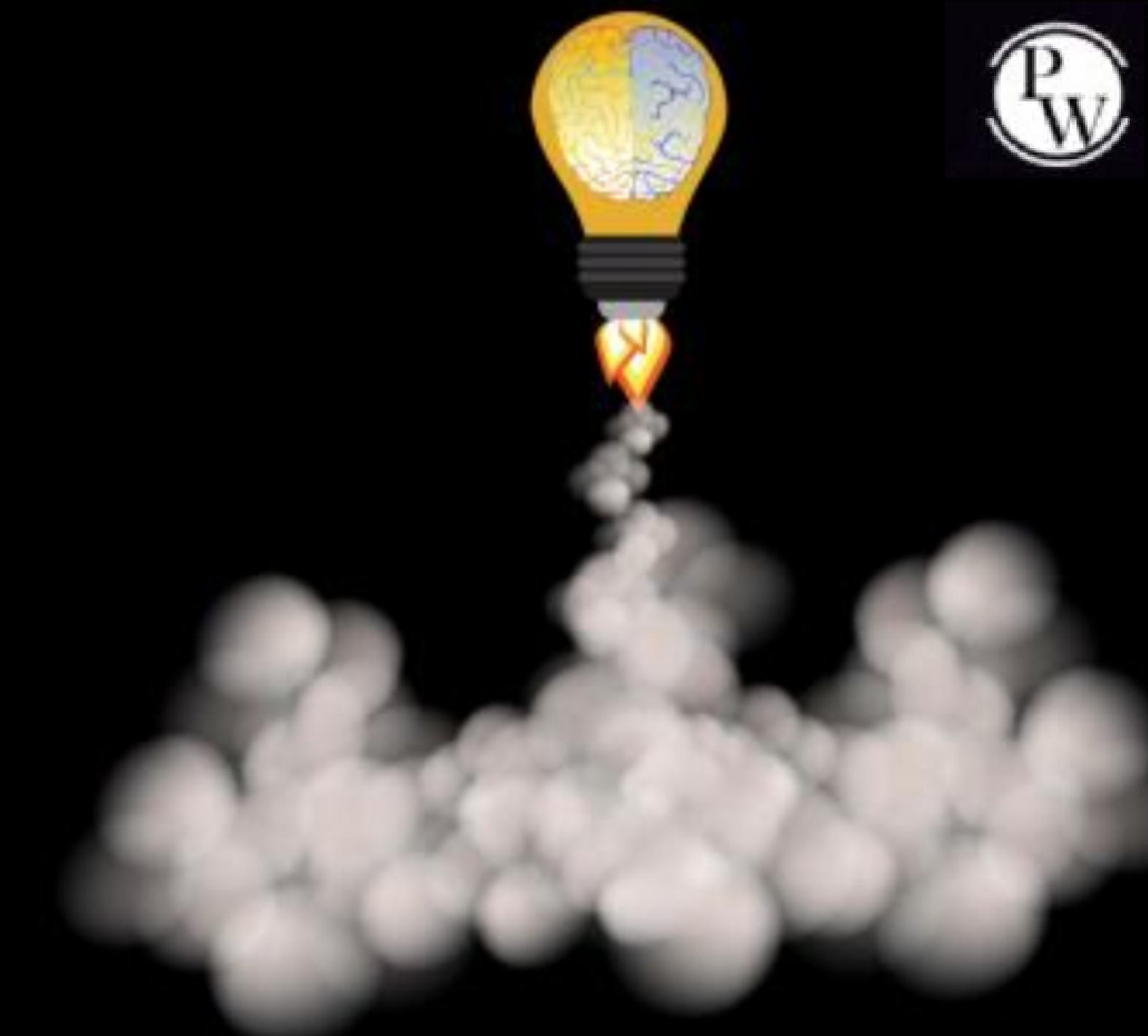
- A** 128 - 1:2 De MUX
- B** 42 - 1:4 De MUX
- C** 18- 1:8 De MUX and 1- 1:2 De MUX
- D** 42- 1:4 De MUX and 1- 1:2 De MUX

#Q. Which of the following is/are incorrect?

HW

- A** De Mux is a universal circuit.
- B** Some 4-variable Boolean function can be implemented by 8:1 MUX.
- C** All 4-variable Boolean function can be implemented by 8:1 MUX.
- D** De MUX is serial to parallel convertor.

**Thank You
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CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No. - 7



By - CHANDAN SIR

Recap of Previous Lecture



combinational Circuit

Topics to be Covered



Sequential Circuit

Questions Practice

(MCQ)

#Q. The output of the present state ' Q_n ' of a JK-FF is 1. Its output changes after applying a clock pulse, then the inputs ' J_n ' and ' K_n ' are respectively ['X' represents the do not care conditions].

- A** X and 0
- B** ✓ X and 1
- C** 1 and X
- D** 0 and X

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table

Q_n	Q_{n+1}	S	R	J	K	N	T
0	0	0	x	0	x	0	0
0	1	1	0	1	x	1	1
1	0	0	1	x	1	0	1
1	1	x	0	x	0	1	0

$$Q_{n+1} = S + \bar{R} Q_n$$

$$Q_{n+1} = J \bar{Q}_n + \bar{K} Q_n$$

$$Q_{n+1} = H$$

$$Q_{n+1} = T \Theta Q_n$$

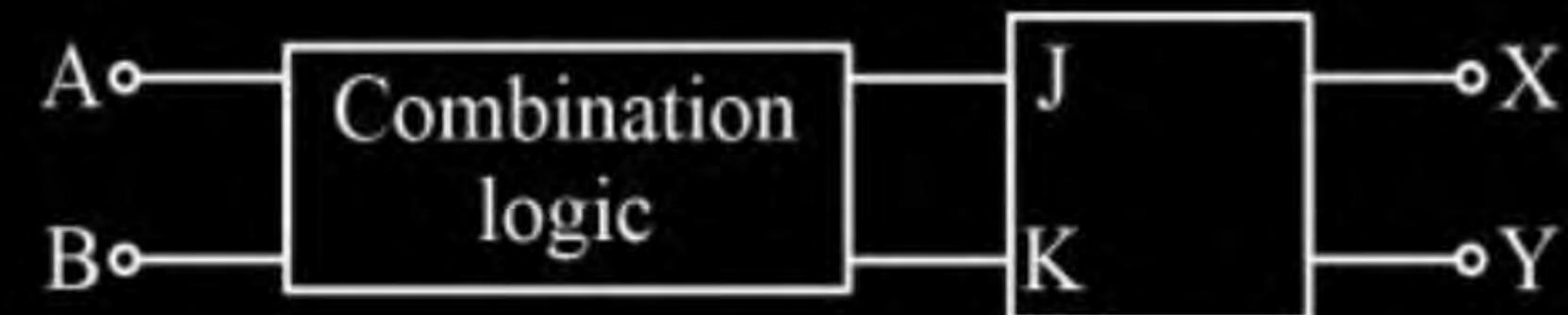
(MCQ)

#Q. Consider a circuit realization of a combinational logic block as shown in figure to obtain the following truth table:

The combinational logic involves

A	B	Q_{n+1}
0	0	\bar{Q}_n
0	1	1
1	0	Q_n
1	1	0

- A** Only Ex-OR gates
- B** AND and NOT gates
- C** NOT and Ex-NOR gates
- D** OR and NAND gates



A	B	Q_n	Q_{n+1}	J	K
{0 0}		0 ↗ 1		1	X
{0 0}		1 ↗ 0		X	1
{0 1}		0	↑ ✓	1	X
{0 1}		1	1 ✓	X	0
{1 0}	0	0	0	0	X
{1 0}	1	1	X	0	
1 1	0	0	0	0	X
1 1	1	0	X	1	

J

$P \nearrow B_{in}$

00	01	11	10
1	X	X	1
	X	X	

$J = \bar{A}$

$P \nearrow B_{in}$

00	01	11	10
X 1			X
X		1 X	

$k = \bar{A}\bar{B} + AB = A \oplus B$

#Q. A master-slave FF is basically constructed from 2 FFs has the characteristic that:

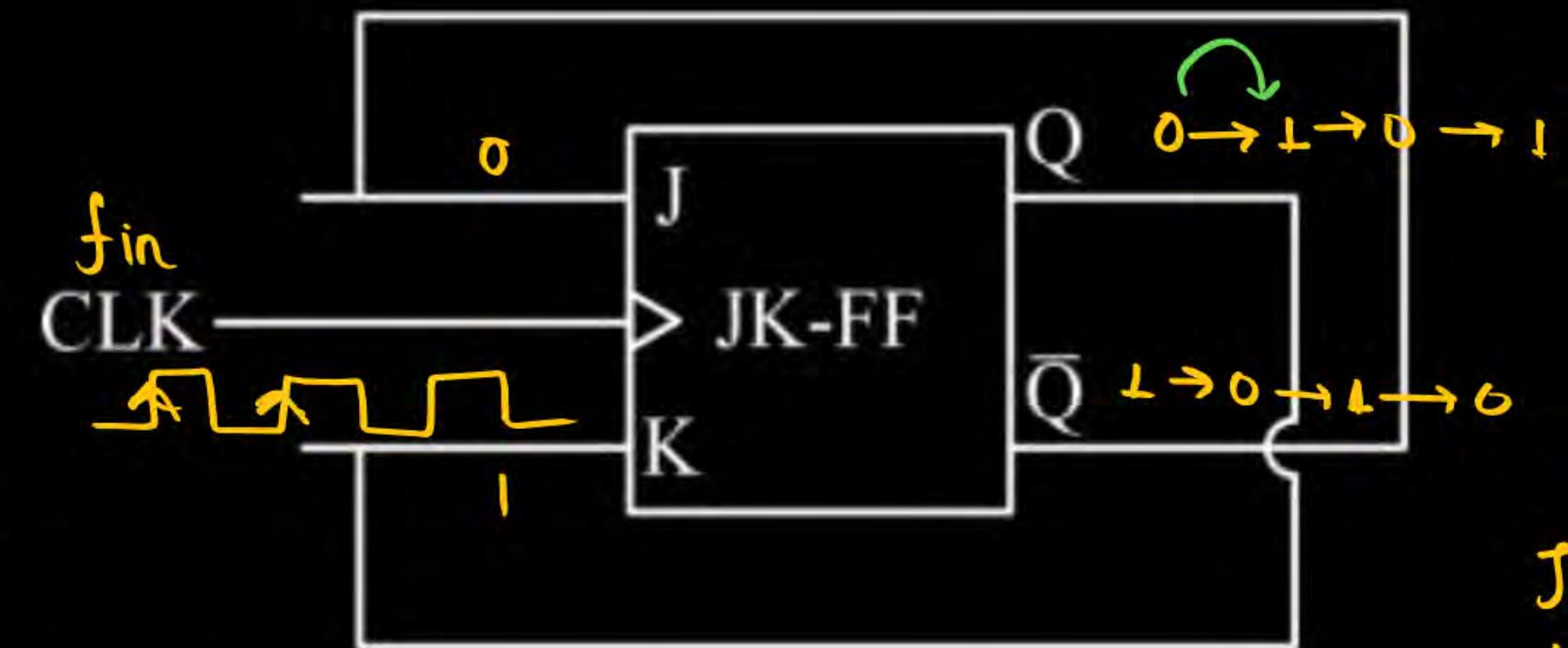
- A** both the master and the slave states are affected at the same time. ✗
- B** change in the input signal immediately reflected at the output. ✗
- C** change in the output occurs when the states of the slave is affected. ✓
- D** change in the output occurs when the states of the master is affected. ✗

(MCQ)

#Q. For the circuit given below, if clock frequency is 15 kHz then output frequency is

$$Q_{n+1} = \bar{Q}_n$$

→ Toggle Mode



$$J = \bar{Q}_n$$

$$K = Q_n$$

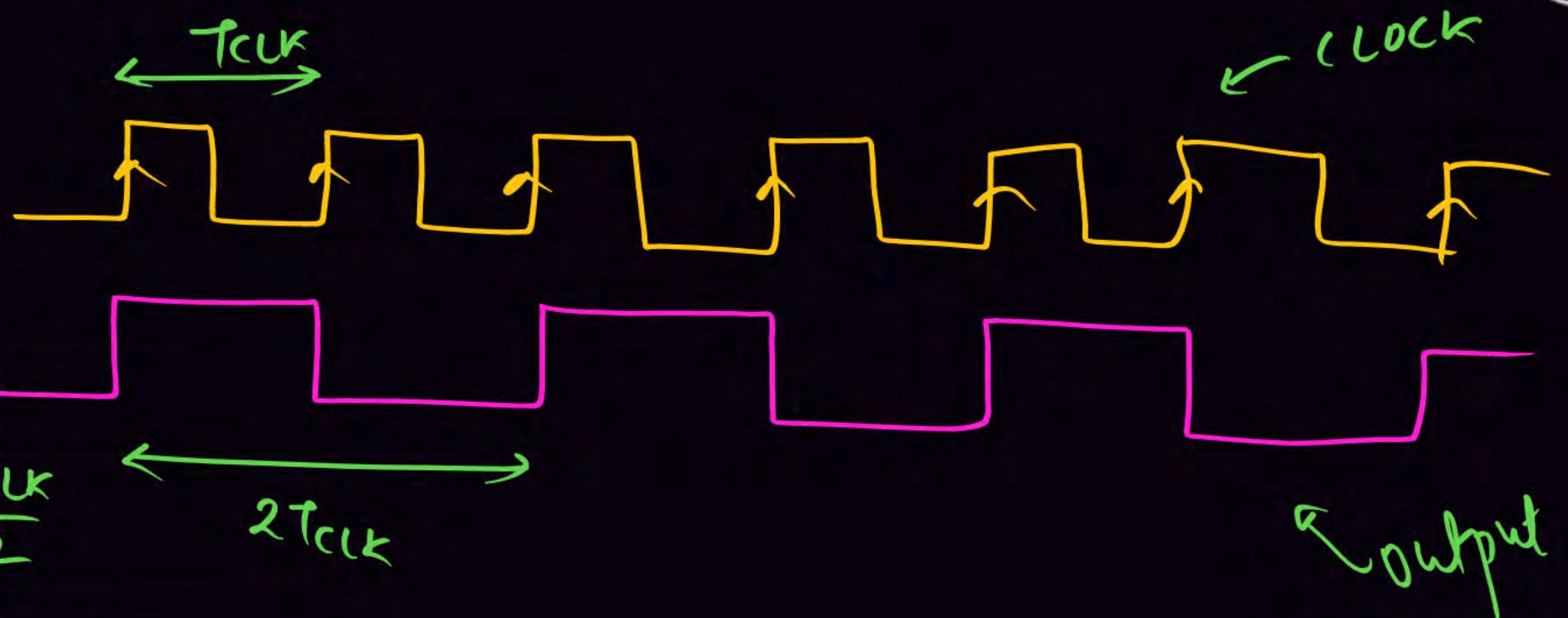
$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

$$= \bar{Q}_n\bar{Q}_n + \bar{Q}_nQ_n$$

$$Q_{n+1} = \bar{Q}_n$$

- A** Twice the input clock frequency.
- B** Same as the input clock frequency.
- C** Inverse of the propagation delay of the FF.
- D** Half the input clock frequency.

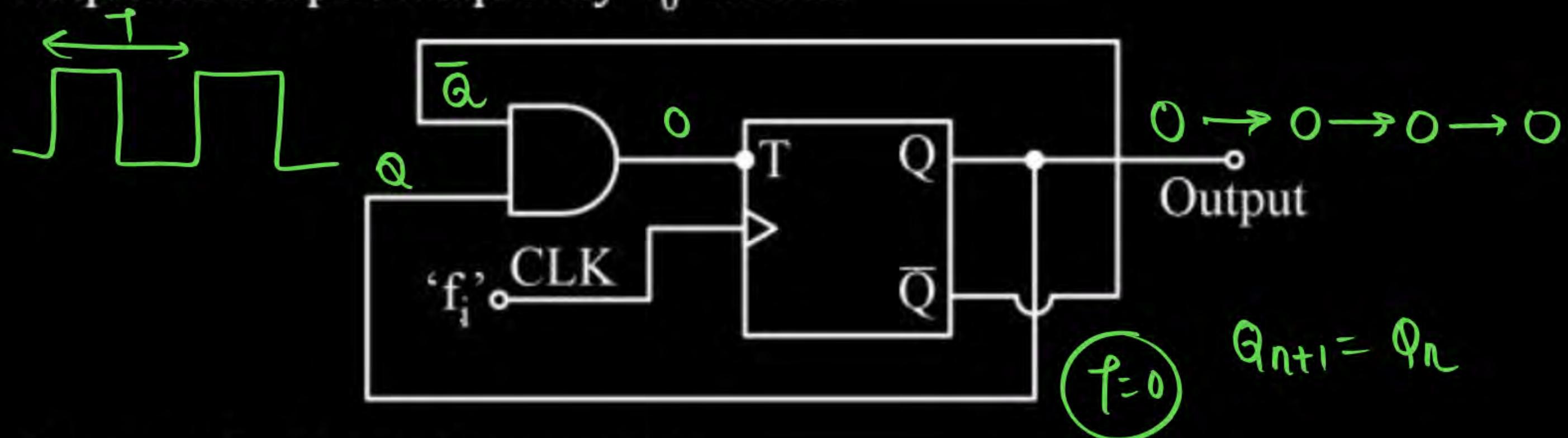
$$f_{\text{CLK}} = \frac{1}{T_{\text{CLK}}}$$



$$f_{Q_{n+1}} = \frac{1}{2T_{\text{CLK}}} = \frac{f_{\text{CLK}}}{2}$$

(MCQ)

#Q. In the following sequential circuit, initially FF is set to **LOW** level having input clock frequency ' f_i '. Required output frequency ' f_o ' will be



- A Same as the input frequency
- B Twice the input frequency
- C Half of the input frequency
- D DC value i.e. zero frequency

(NAT)P
W

#Q. A certain JK-FF has propagation delay (t_{pd}) = 12 ns. The largest Mod counter that can be designed from these FFs which still operate up to 10 MHZ will be 256

$$f_{CLK} \leq \frac{1}{n \cdot t_{pd,ff}}$$

$$n \leq \frac{1}{f_{CLK} \cdot t_{pd,ff}}$$

$$\leq \frac{1}{10 \times 10^6 \times 12 \times 10^{-9}}$$

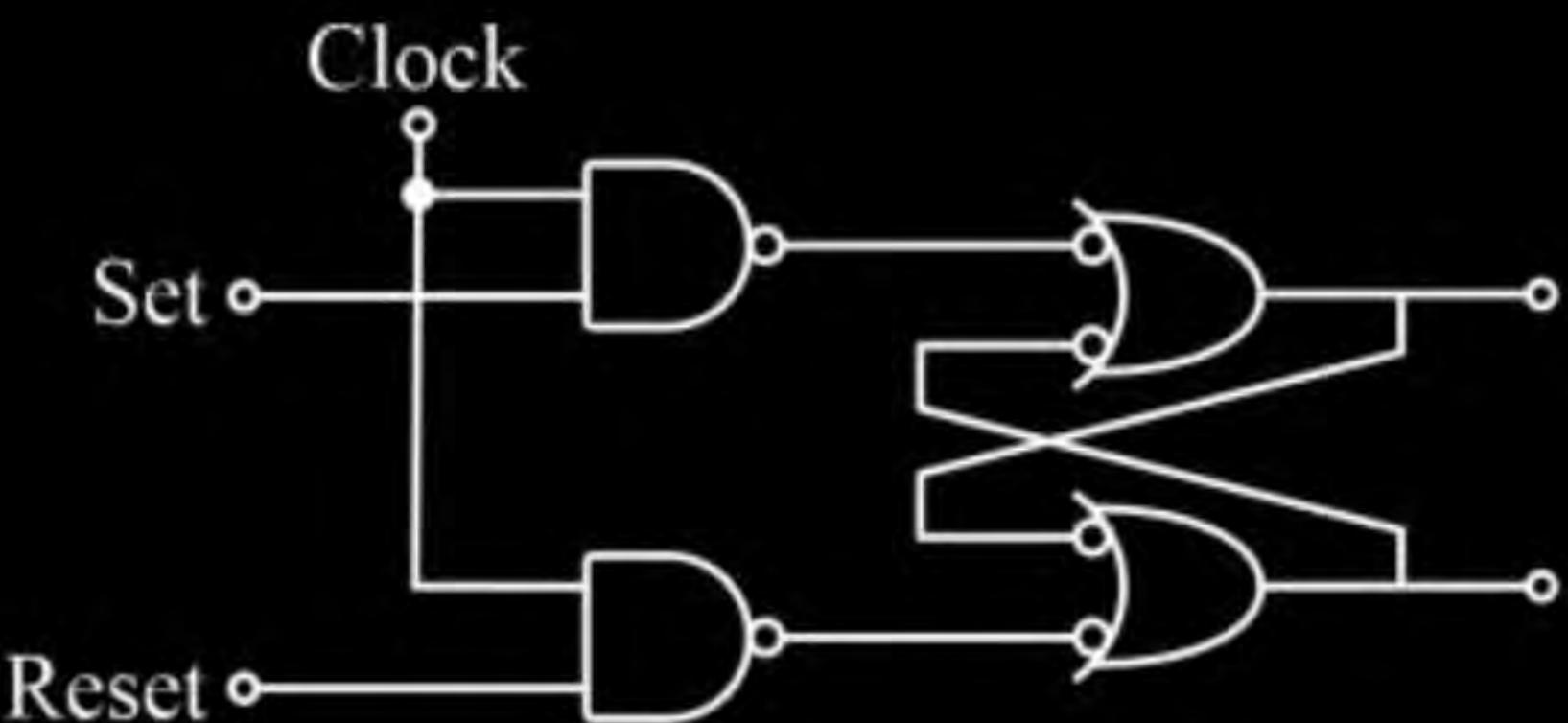
$$n \leq \frac{100 \times 10^9}{10 \times 12}$$

$$n \leq 8.33 \text{ m}$$

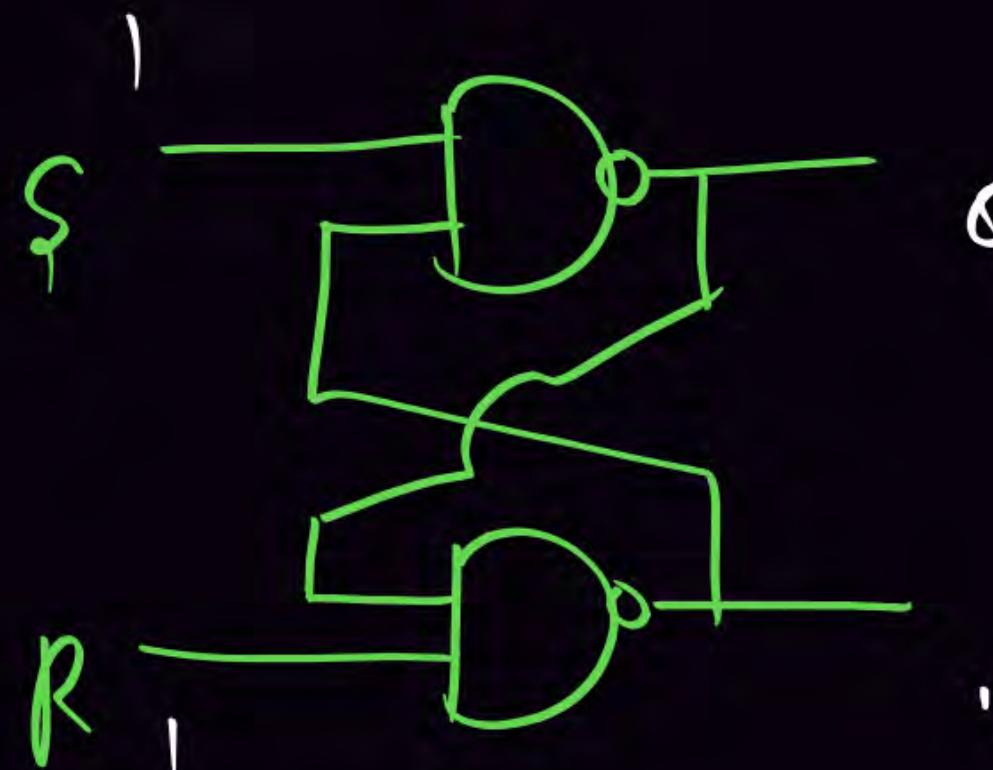
$$(n=8)$$

$$\text{Mod} = 2^n = 2^8 = 256$$

#Q. The two NAND gates before the latch circuit shown below, are used to

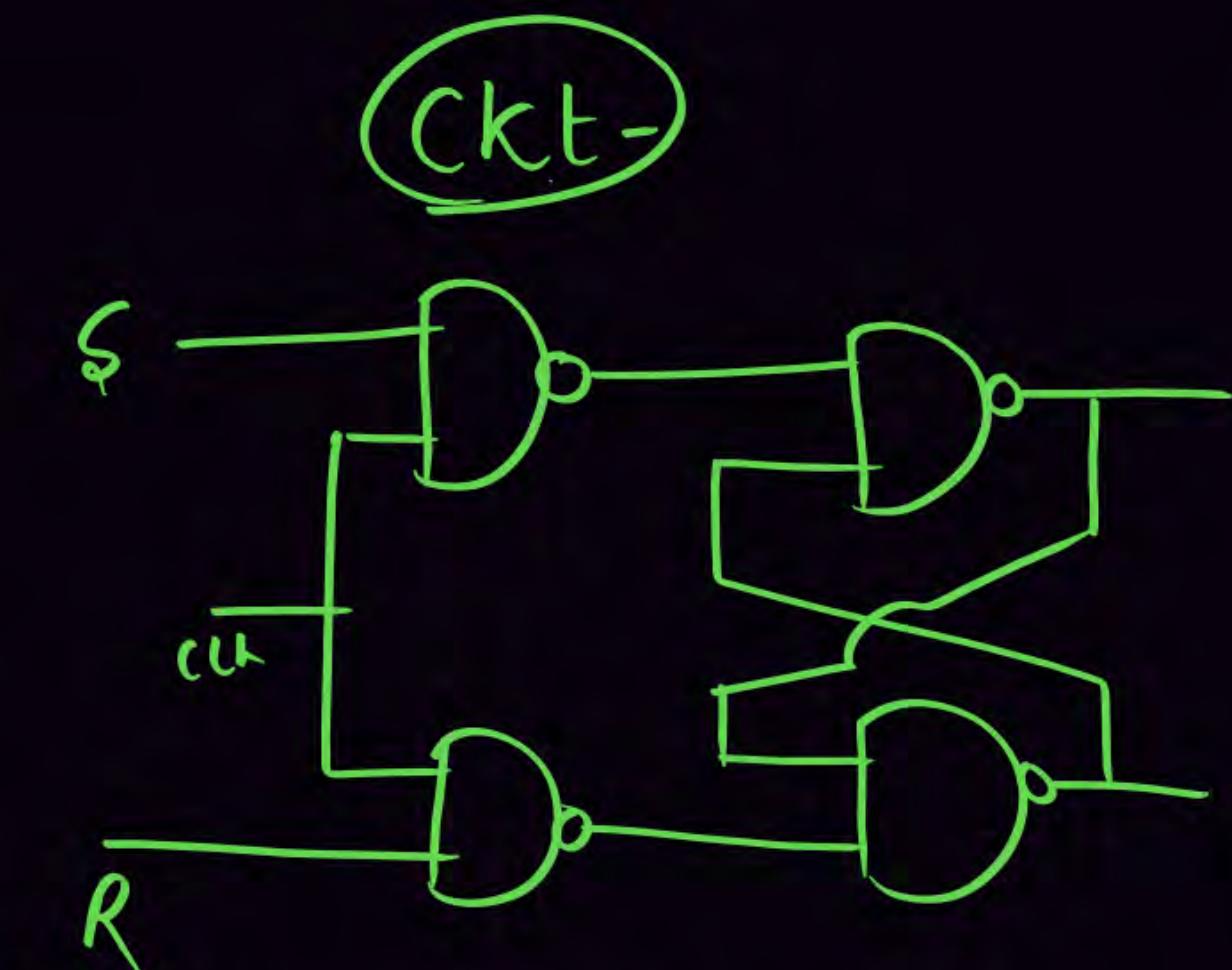


- A** acts as buffers.
- B** operate the latch faster.
- C** avoid racing.
- D** invert the latching action. ✓



S	R	Q_{n+1}
0	0	InValid
0	1	1
1	0	0
1	1	Q_n

Reverse

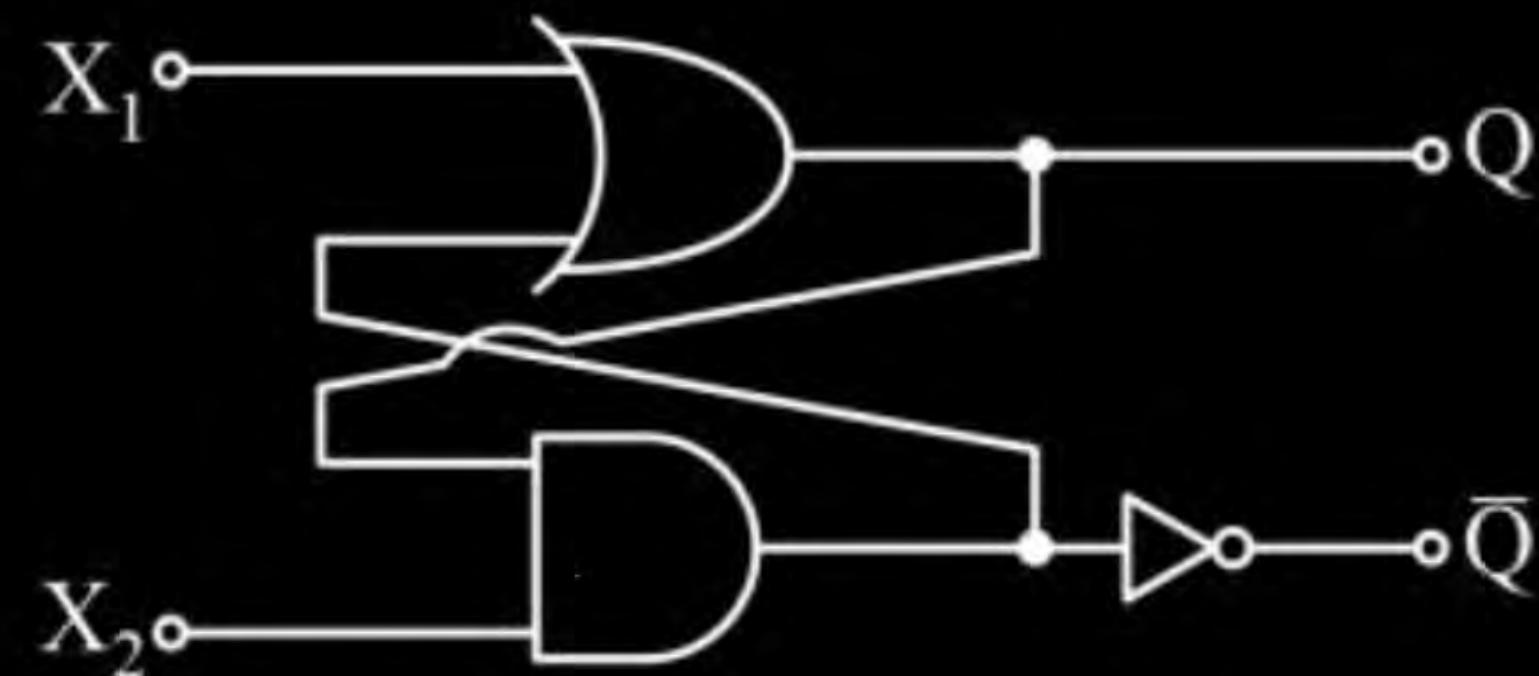


S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

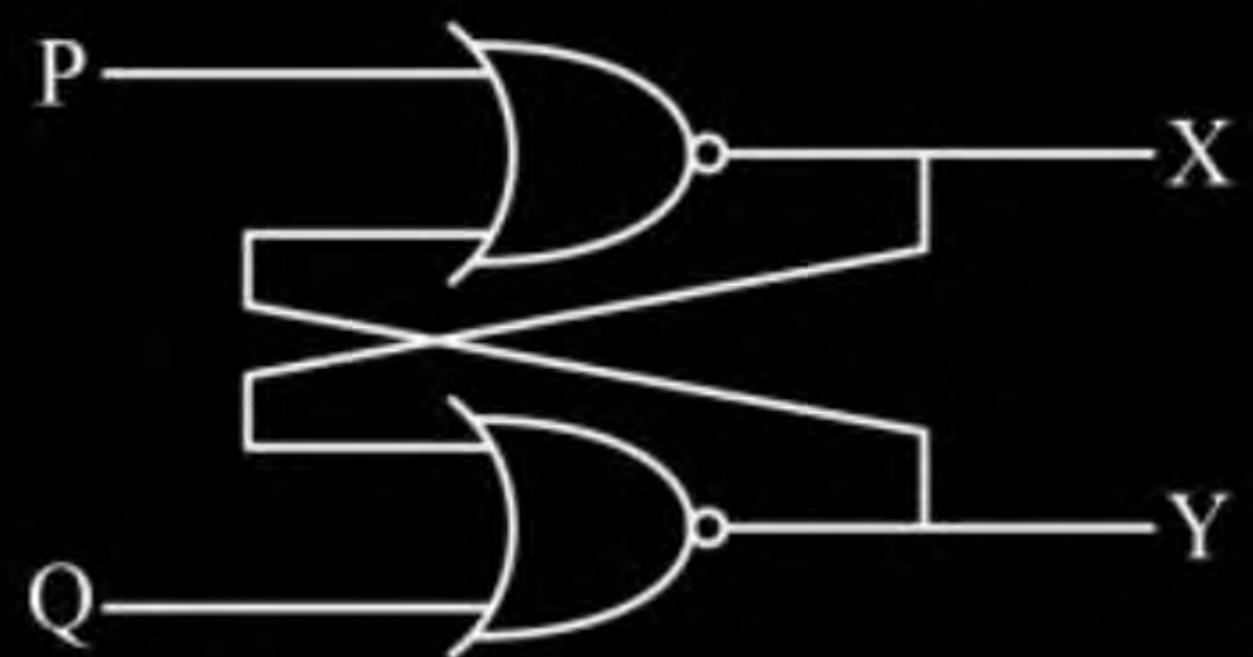
(MCQ)

#Q. The latching action of a latch shown below, is controlled by two inputs X_1 , X_2 . The invalid input combination X_1, X_2 will be

- A $X_1 = 1, X_2 = 0$ ✓
- B $X_1 = 0, X_2 = 1$ ✗ → HOLD
- C $X_1 = X_2 = 0$ ✗
- D $X_1 = X_2 = 1$



#Q. In the latch circuit shown, the NOR gates have non-zero but unequal propagation delays. The present input condition is $P = Q = 1$. If the input condition is changed simultaneously to $P = Q = 0$, the outputs X and Y are



case(2) $| < 2$

$X=1 \quad Y=0$

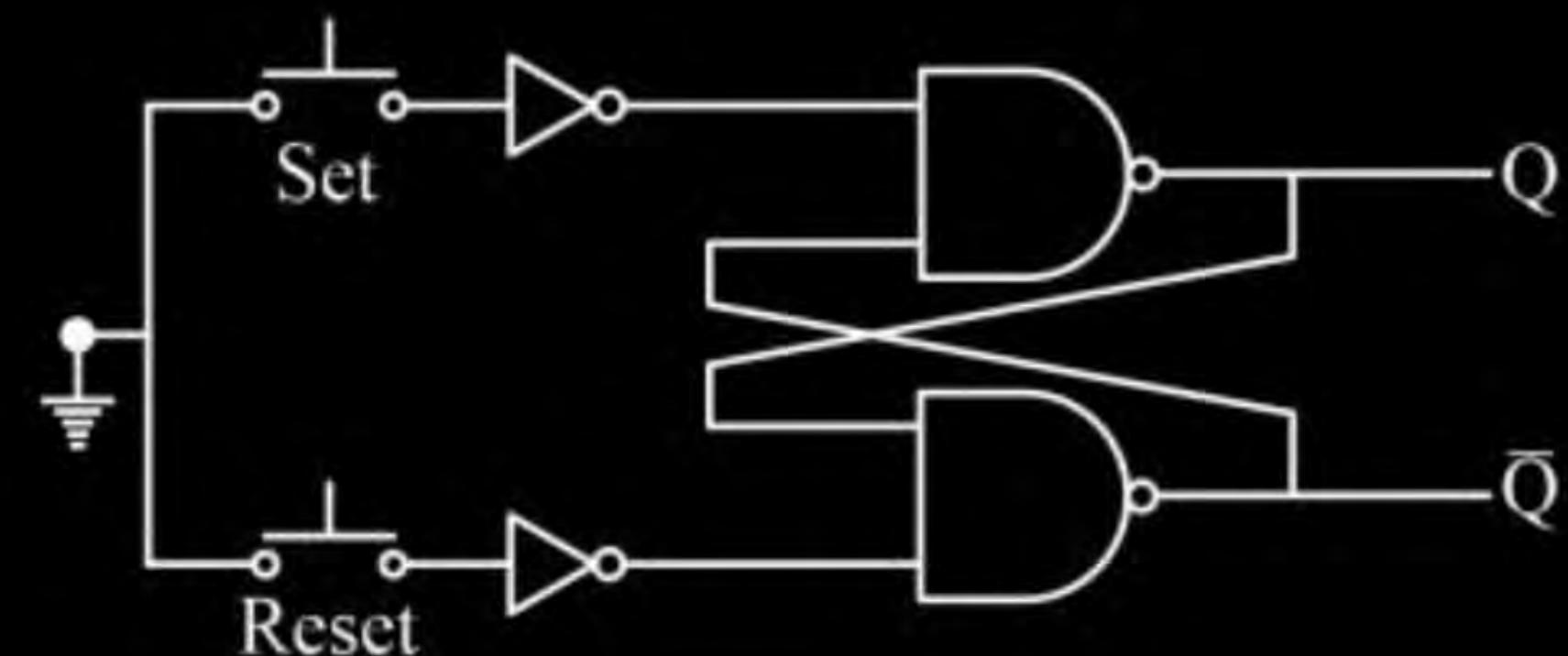
case(1) 172

$X=0 \quad Y=1$

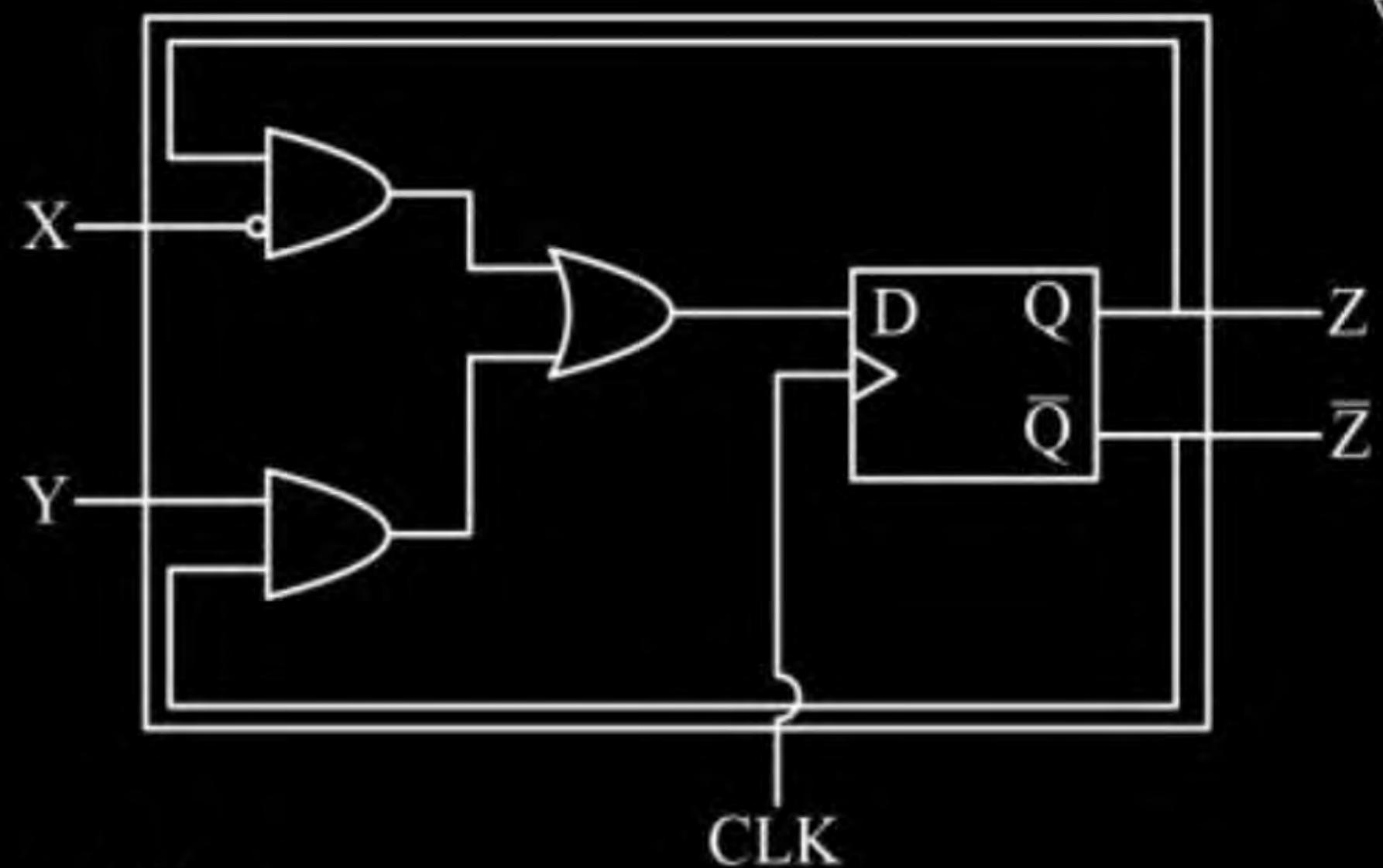
- A Hold the previous state
- B Enter into a new valid state (1, 0)
- C Enter into a new valid state (0, 1)
- D Enter into an invalid state

#Q. An SR latch is implemented using ECL gates as shown in the figure. The set and reset pulse inputs are provided using the push-button switches. It is observed that the circuit fails to work as desired. The SR latch can be made function by changing

- A NAND gate to NOR gate
- B Ground to V_{CC} (5 V)
- C Inverters to buffers
- D ECL logic to TTL logic



#Q. A sequential circuit using D flip-flop and logic gates is shown in the following figure, where X and Y are the inputs and Z is the output. The circuit is



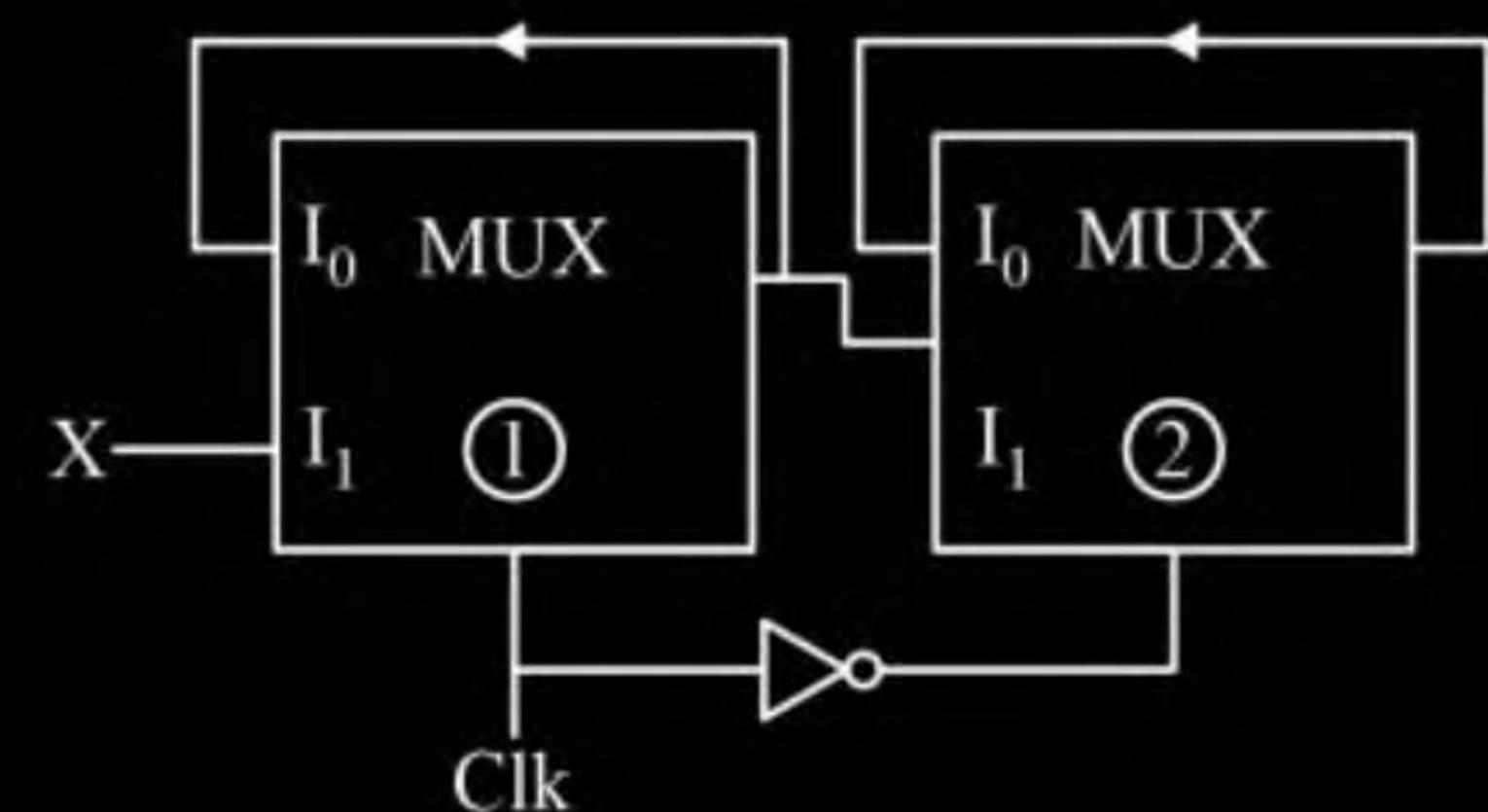
- A** S-R flip-flop with inputs $X = R$ and $Y = S$
- B** S-R flip-flop with inputs $X = S$ and $Y = R$
- C** J-K flip-flop with inputs $X = J$ and $Y = K$
- D** J-K flip-flop with inputs $X = K$ and $Y = J$

(MCQ)

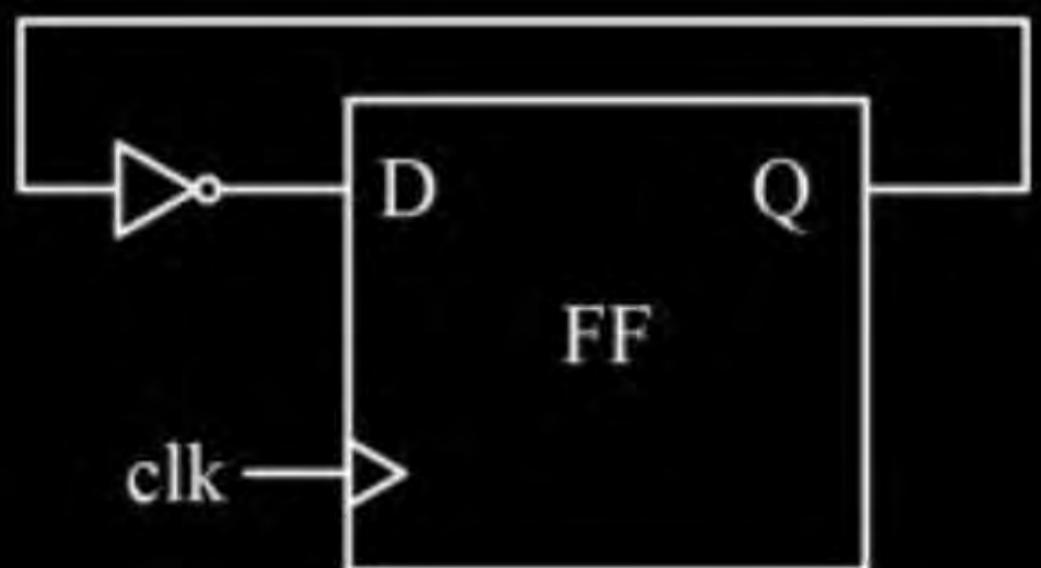
#Q. Identify the following circuit, constructed using multiplexers

Hw

- A** 2-Bit counter
- B** Master Slave D-FF
- C** D-Latch
- D** 2-Bit Johnson counter



#Q. The maximum frequency of operation of the following circuit, if propagation delay of Flip-Flop and inverter are 20ns, 5ns respectively is _____MHz.



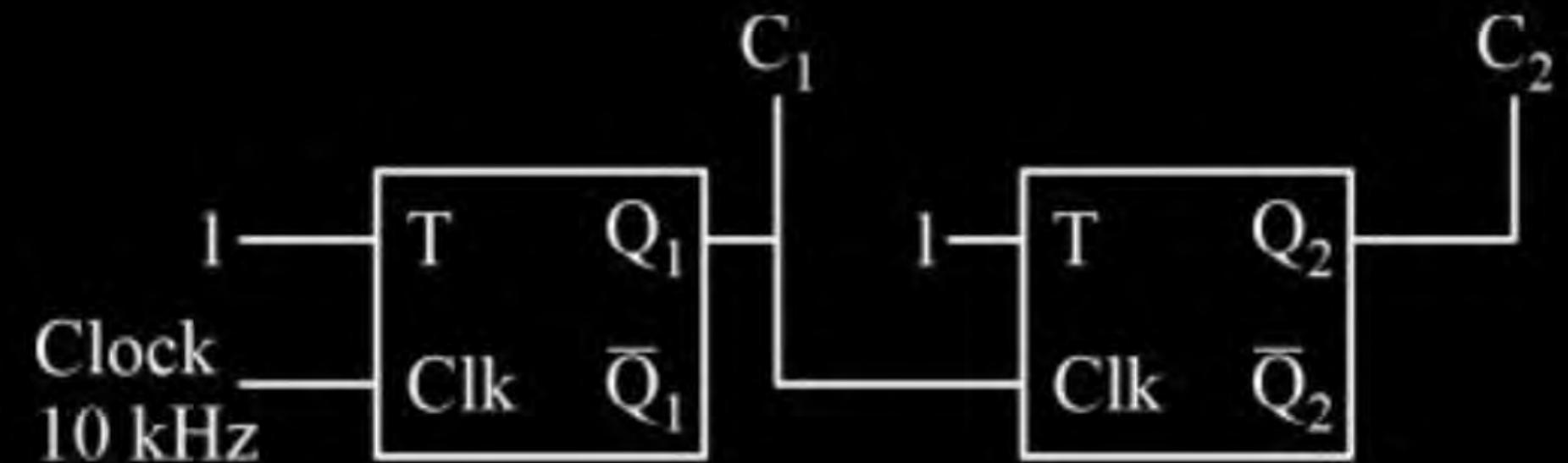
(MCQ)

#Q. A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively. The characteristics equation for the PN FF is

- A** $\overline{P}Q(t) + NQ(t)$
- B** $P\overline{Q}(t) + NQ(t)$
- C** $P\overline{Q}(t) + \overline{N}\overline{Q}(t)$
- D** $PQ(t) + \overline{N}Q(t + 1)$

(MCQ)

#Q. In the circuit shown below, find the frequencies of C_1 and C_2



- A** 5 kHz and 2.5 kHz
- B** 5 kHz and 5 kHz
- C** 2.5 kHz and 5 kHz
- D** 2.5 kHz and 2.5 kHz

(MCQ)

#Q. A flip-flop has a delay of 10 nsec from the time the clock edge applied to the time the output is obtained. There is a mod-10 ripple counter that uses this type of flipflops. The maximum delay in output is

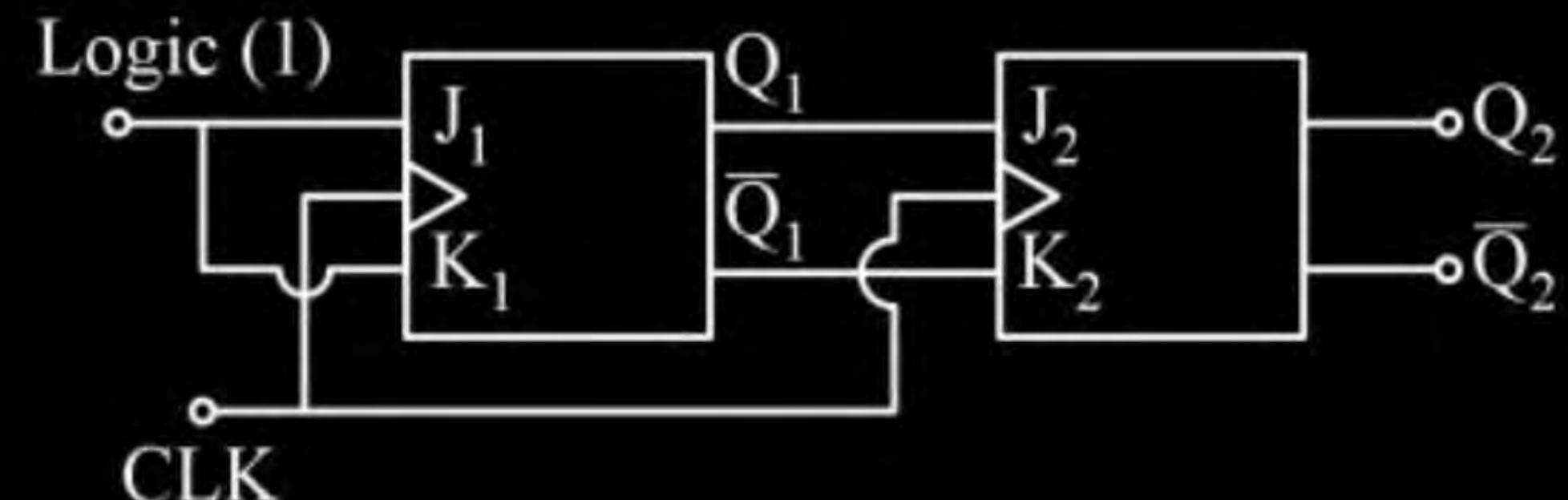
- A** 100 nsec
- B** 10.24 μ sec
- C** 40 nsec
- D** 33.21 μ sec

(MCQ)

#Q. In the circuit shown, JK-TTL FFs are synchronized. Assuming an input set-up time (t_s) = 40 ns, hold time (t_h) = 20 ns and a propagation delay of 140 ns for each FFs.

The maximum clock frequency for the reliable operation of the TTL circuit is

- A** 5.5 MHz
- B** 5.0 MHz
- C** 16.6 MHz
- D** 6.25 MHz



Thank You
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CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No. - 8



By - CHANDAN SIR

Recap of Previous Lecture



Sequential Circuit

Topics to be Covered

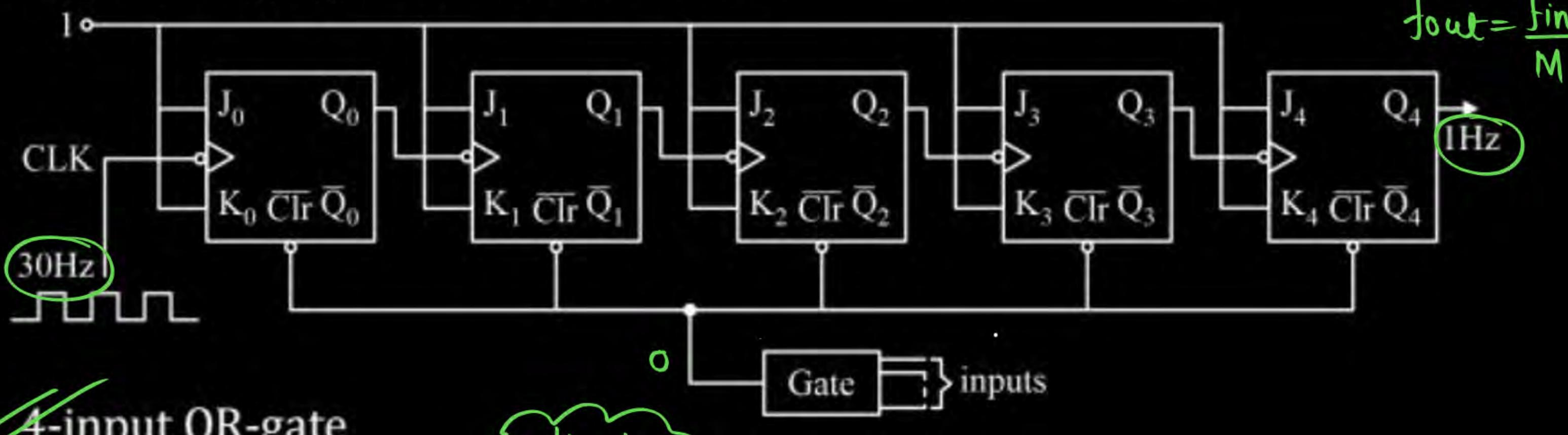


Sequential Circuit

- Questions Practice

(MCQ)

#Q. Consider the following counter as shown below is needed to divide the 30 Hz line frequency down to 1 Hz. \bar{Q} output is used in input of gate. Required logic gate for this counter is,



A 4-input OR-gate

B 3-input NAND-gate ×

C 4-input NAND-gate ×

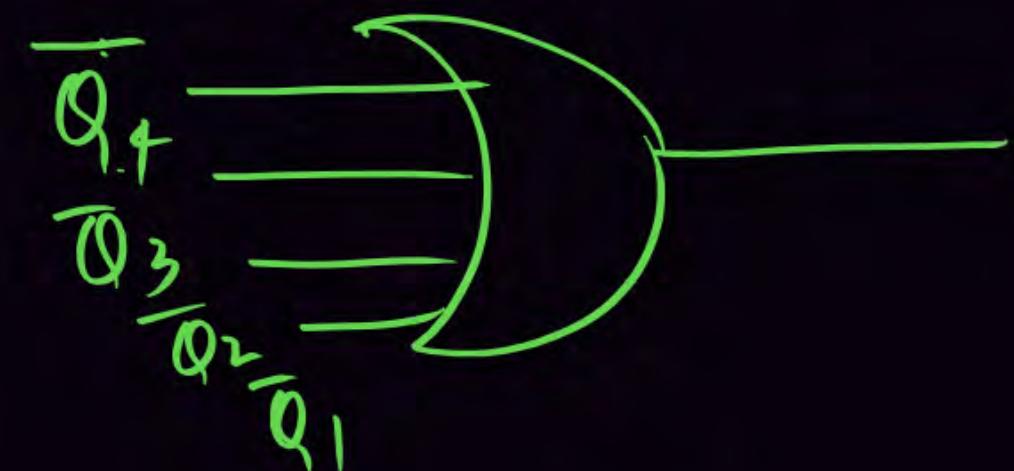
D 4-input NOR-gate ×

Active Low

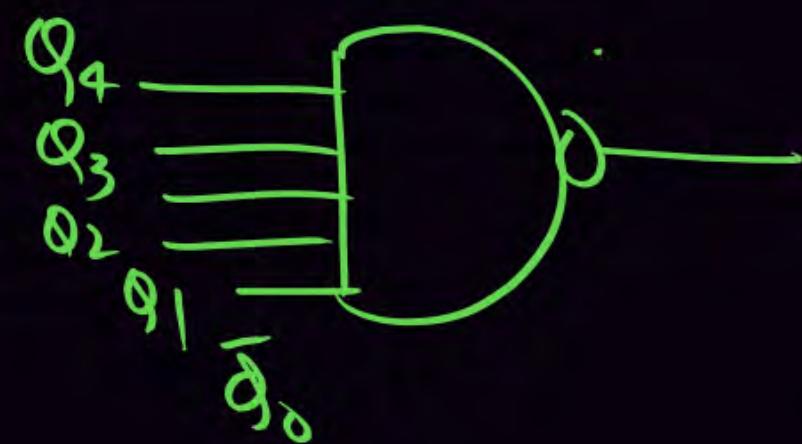
$$\text{MOD} = \underline{30}$$

(1)

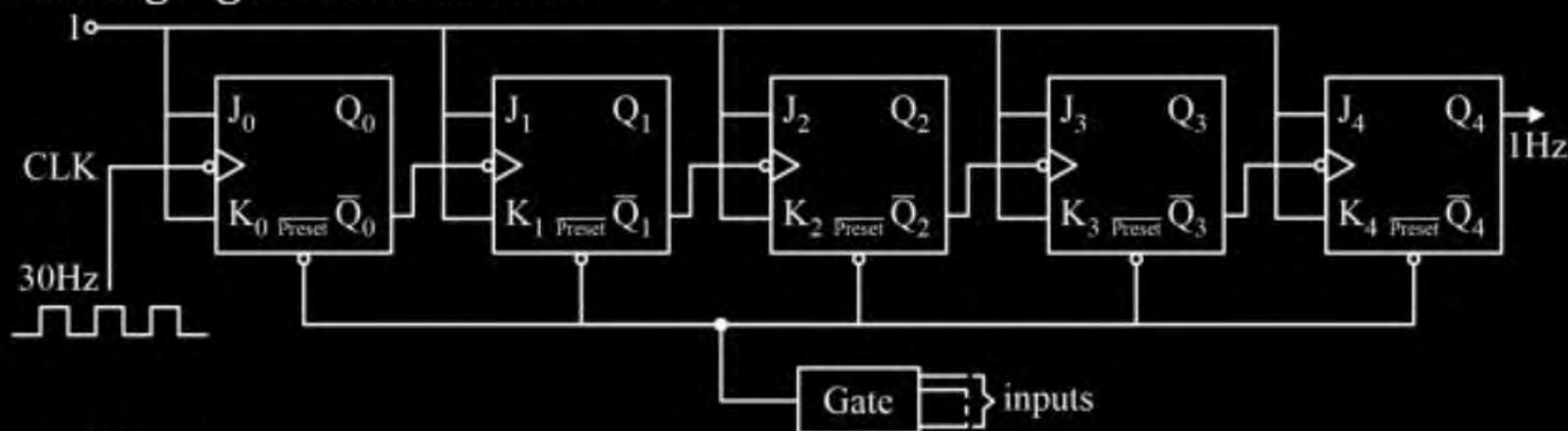
$$\begin{matrix} Q_4 & Q_3 & Q_2 & Q_1 & Q_0 \\ 1 & 1 & 1 & 1 & 0 \end{matrix}$$



$$\begin{matrix} \bar{Q}_4 & \bar{Q}_3 & \bar{Q}_2 & \bar{Q}_1 & \bar{Q}_0 \\ 0 & 0 & 0 & 0 & 1 \end{matrix}$$



#Q. Consider the following counter as shown below is needed to divide the 30 Hz line frequency down to 1 Hz. Q output is used in input of gate.
Required logic gate for this counter is

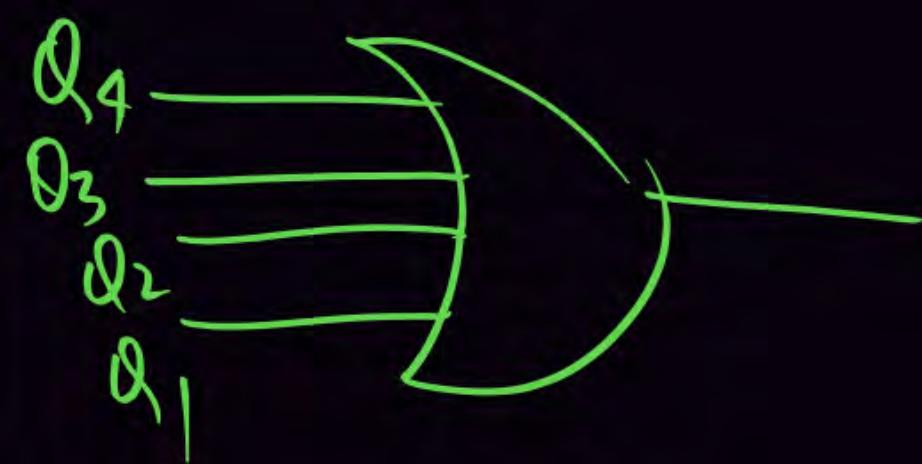
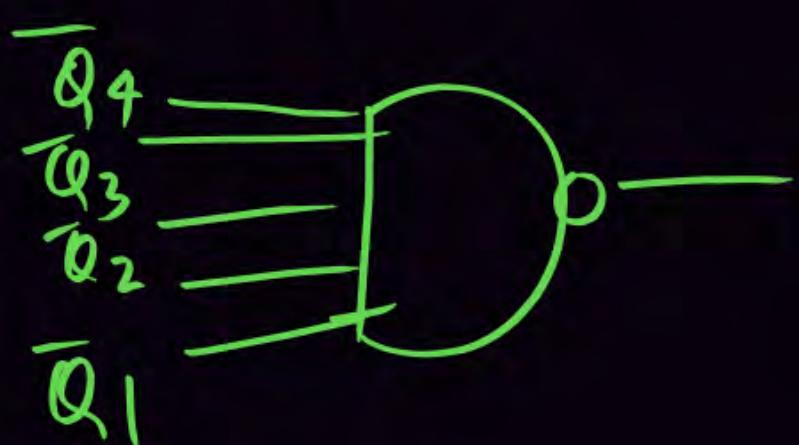


- A 3-input OR-gate
- B 3-input NOR-gate
- C 4input NAND-gate
- D 4-input OR gate

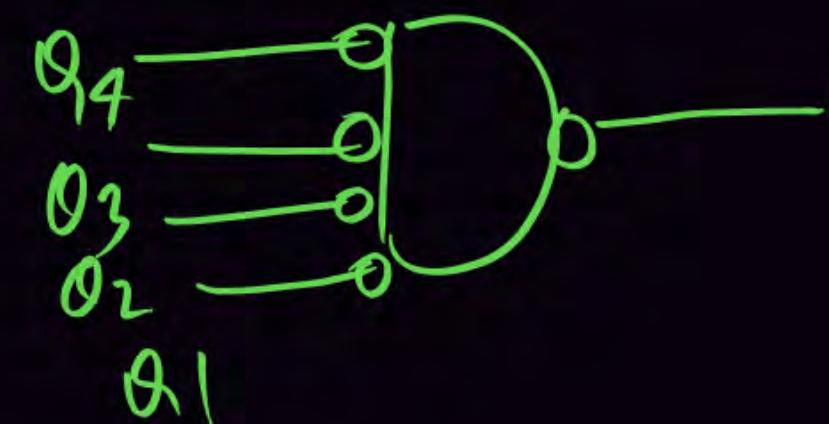
Mod 30



$\bar{Q}_4 \bar{Q}_3 \bar{Q}_2 \bar{Q}_1 Q_0$
0 0 0 0 1

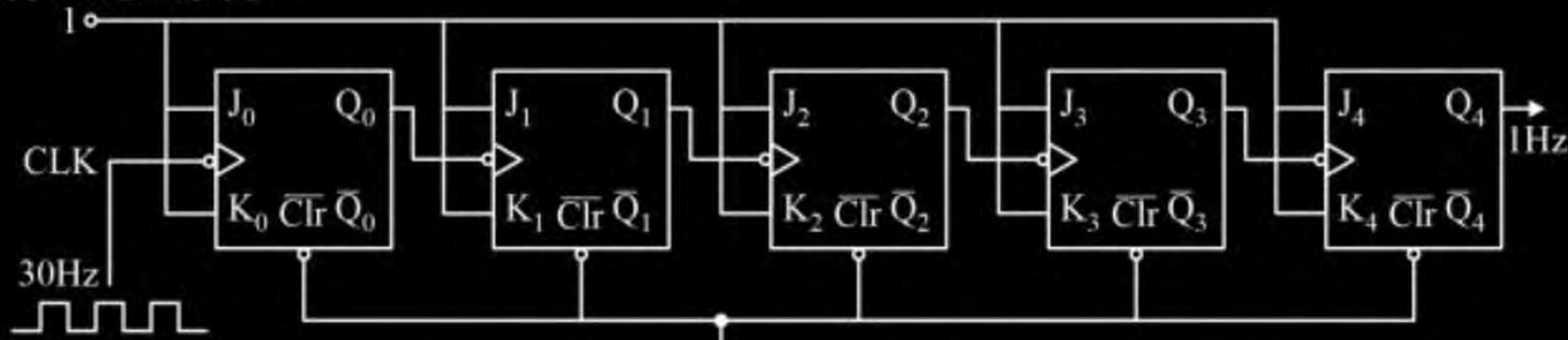


≡



(MCQ)

#Q. Counter circuit as shown in figure given below, if all the FFs outputs(Q) are connected as the inputs of the NAND-gate with Q_3 , Q_1 and Q_0 HIGH and rest are LOW. $\overline{\text{Clr}}$ pin is synchronous with clock, then the ripple counter works as

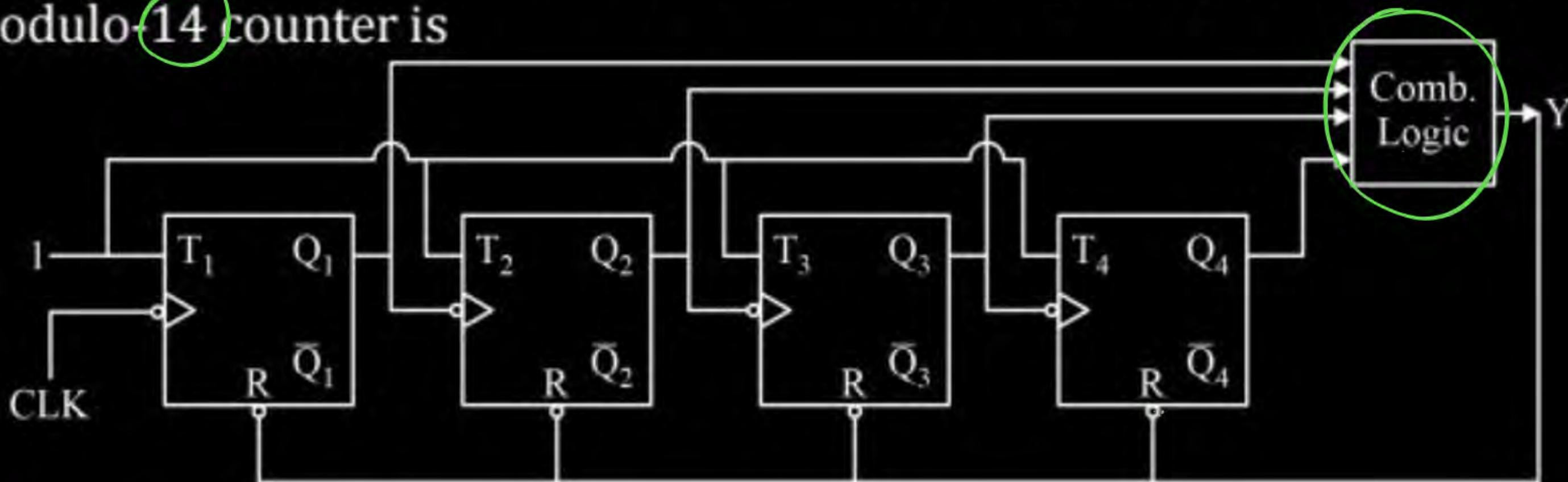


- A mod-20 Up counter
- B mod-11 Up counter
- C mod-11 Down counter
- D mod-12 Up counter

$\overline{Q_4} \ \overline{Q_3} \ \overline{Q_2} \ \overline{Q_1} \ \overline{Q_0}$
 0 1 0 1 1 → (11)₁₀
 Gate } inputs
 Mod-12 VP

(MCQ)

#Q. The counter shown in figure is built with 4-toggled FFs. The FFs can be set asynchronous clear when $R = 0$. The logic required to realize a modulo-14 counter is

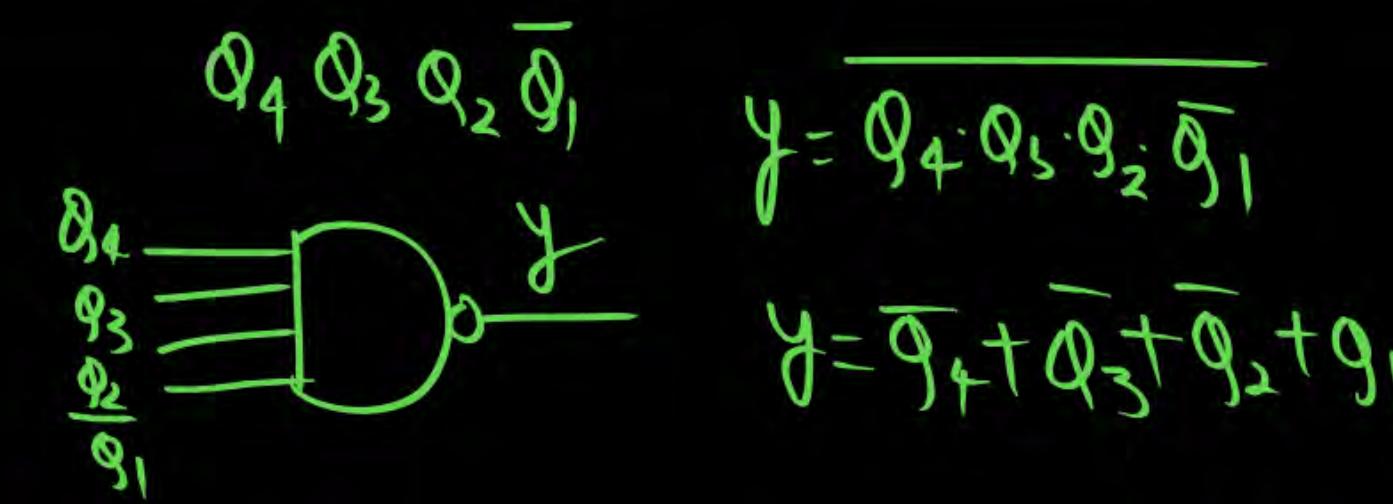


A $Y = \bar{Q}_4 + \bar{Q}_3 + \bar{Q}_2 + Q_1$

B $Y = Q_4 Q_3 Q_2 \bar{Q}_1$

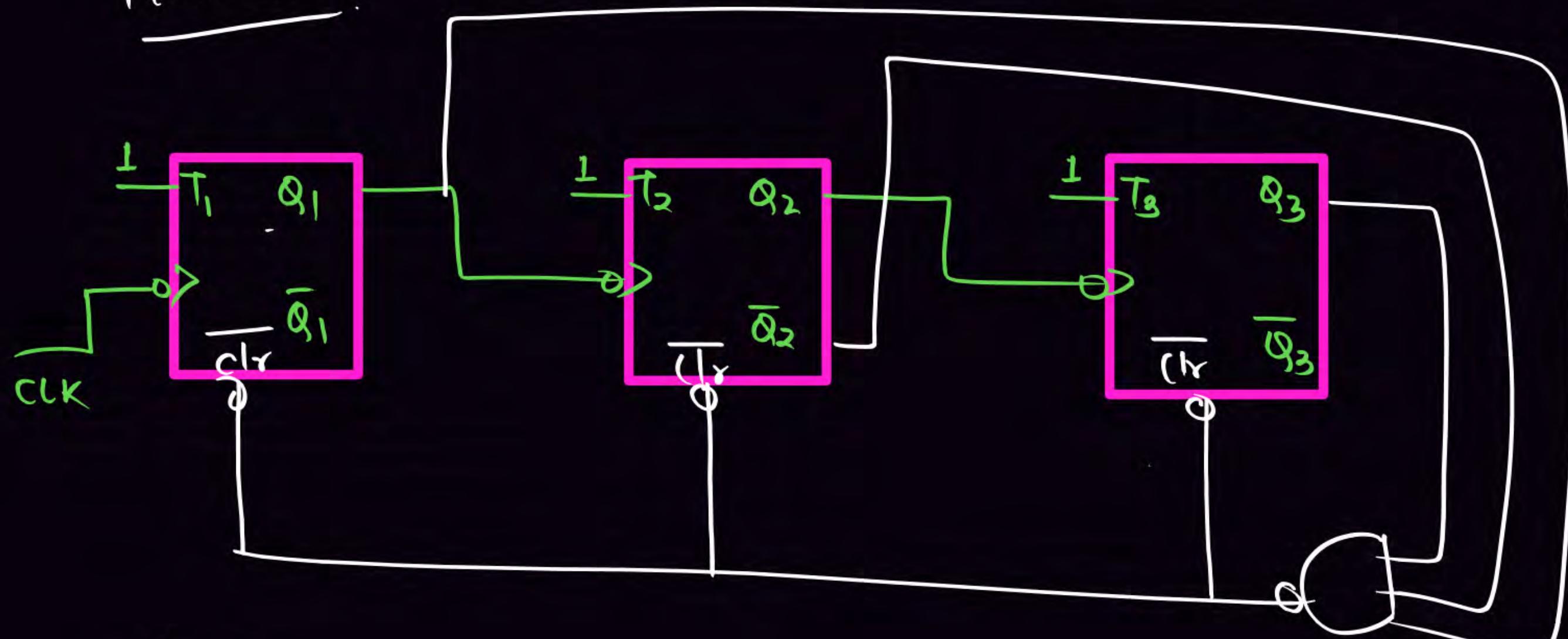
C $Y = Q_4 + Q_3 + Q_2 + \bar{Q}_1$

D $Y = \bar{Q}_4 \bar{Q}_3 \bar{Q}_2 Q_1$



$$Y = \overline{Q_4 \cdot Q_3 \cdot Q_2 \cdot \bar{Q}_1}$$

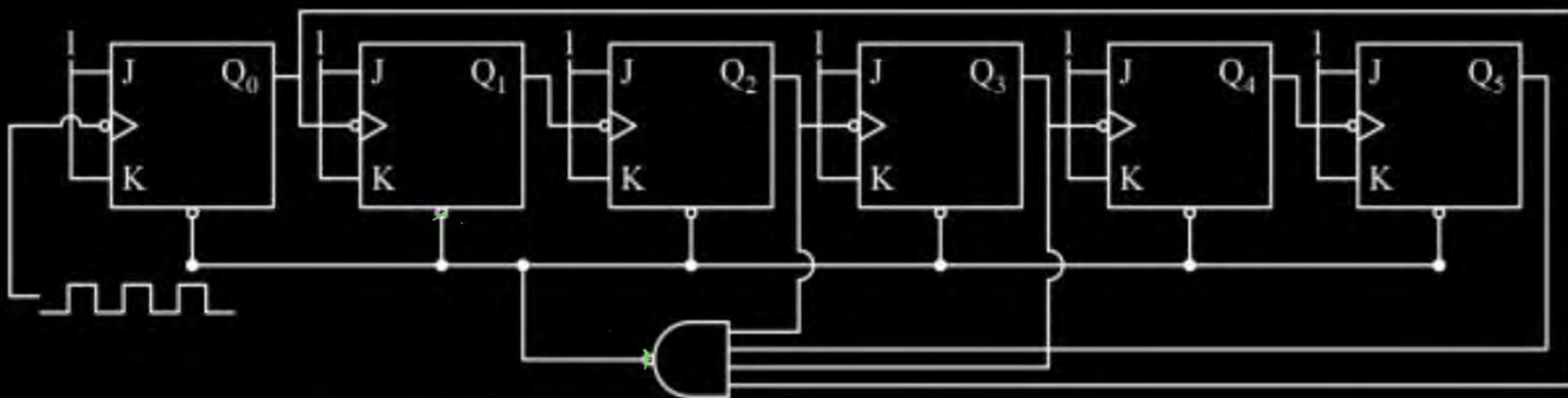
$$Y = \bar{Q}_4 + \bar{Q}_3 + \bar{Q}_2 + Q_1$$

MOD-5

| 0 |

#Q. Consider an asynchronous counter design as shown below.

Assume Q_0 is the output of LSB FFs and Q_5 is the output of MSB FF and all J, K inputs are logically at '1'. $\overline{\text{Clr}}$ pin is synchronous, the mod number 'N' for this given counter is 46.



$$\text{Clr} = \overline{Q_5} \cdot \overline{Q_4} \cdot \overline{Q_3} \cdot \overline{Q_2} \cdot \overline{Q_1} \cdot Q_0$$

1	0	1	1	0	1
---	---	---	---	---	---

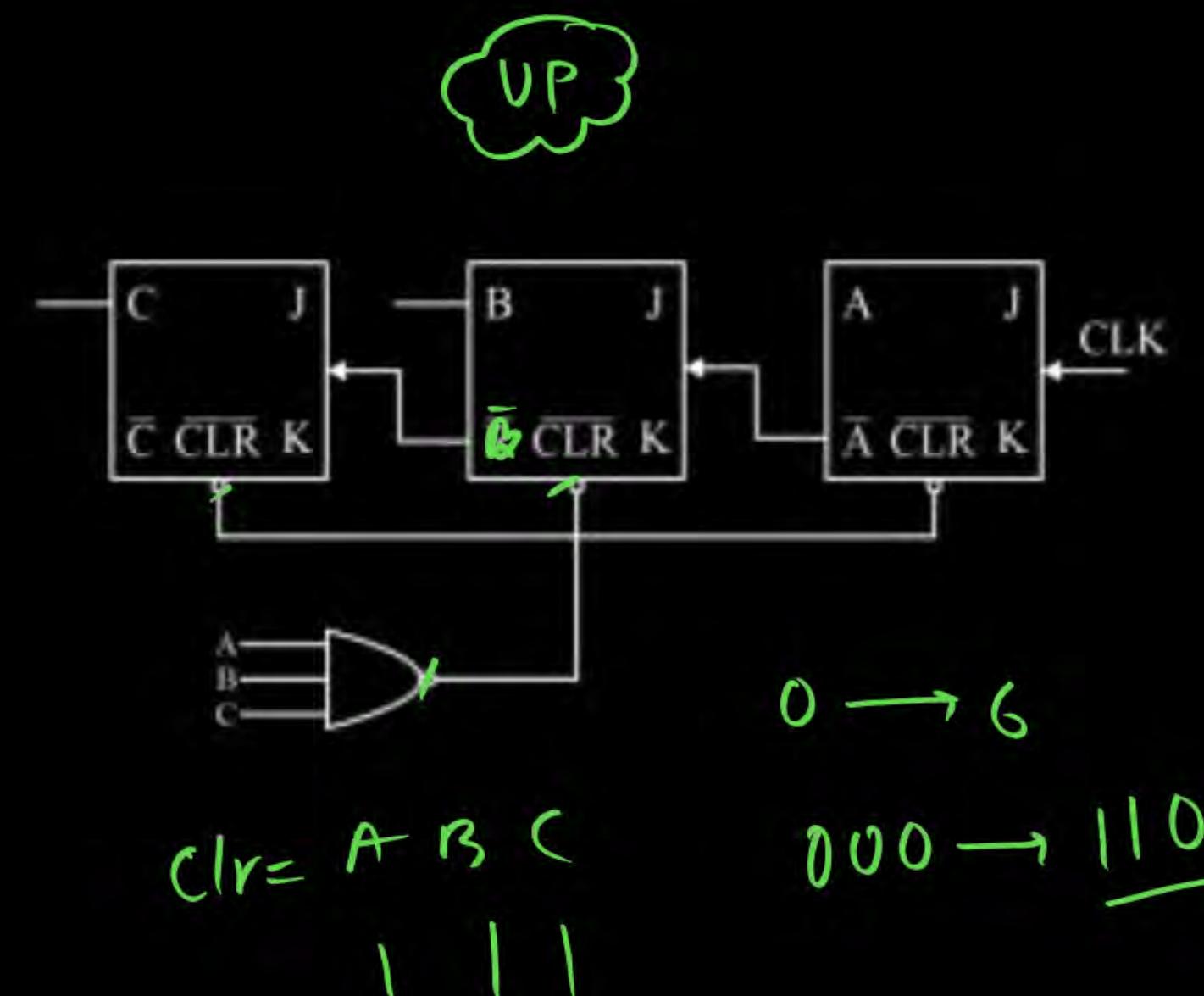
0 → 45

MOD = 46

(MCQ)

#Q. Assuming all $J = K = 1$ in the counter shown below, find the counting sequence

- A** 000 to 111
- B** 111 to 000
- C** 100 to 000
- D** 000 to 110



NOTE

P
W

1. For Synchronous Reset/Preset

→ State at which Reset/Preset happened need to consider that state in MOD.

Ex. $\text{Clr} = Q_3 \bar{Q}_2 Q_1$ $0 \rightarrow 5$ MOD=6

1 0 1 → 5

2. For Asynchronous Reset/Preset.

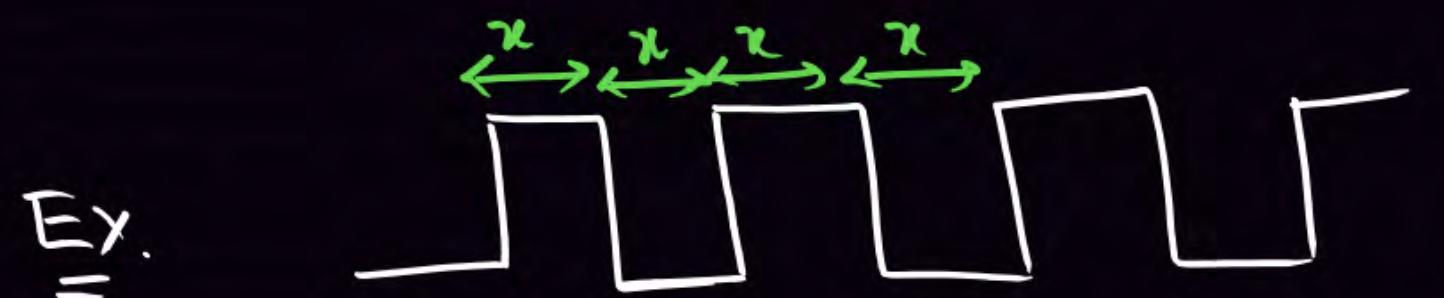
→ state at which Reset/Preset happened need not to be counted into MOD

$0 \rightarrow 4$ MOD=5

Ex $\text{Clr} = Q_3 \bar{Q}_2 Q_1 = 101$

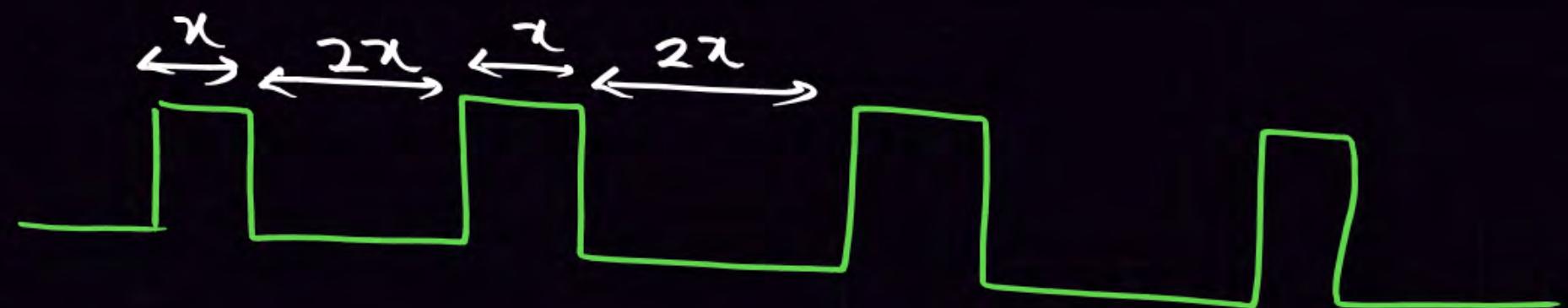
Duty cycle

$$\% D = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100$$



$$\% D = \frac{x}{x+x} \times 100$$

$$= \frac{x}{2x} \times 100 = 50\%$$



$$\eta = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times 100$$

$$= \frac{x}{3x} \times 100$$

$$= 33.33\%$$

#Q. The count of a mod 10(4 bit) counter is represented as $b_3 b_2 b_1 b_0$, where b_3 is the MSB and b_0 is the LSB. If the counter counts from '0' onwards, then the duty cycle of the bit b_2 is ____%.

b_3	b_2	b_1	b_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

$$b_2 \Rightarrow T_{ON} = 4\pi \quad T_{OFF} = 6\pi$$

$$D = \frac{4\pi}{10\pi} \times 100 = 40\% =$$

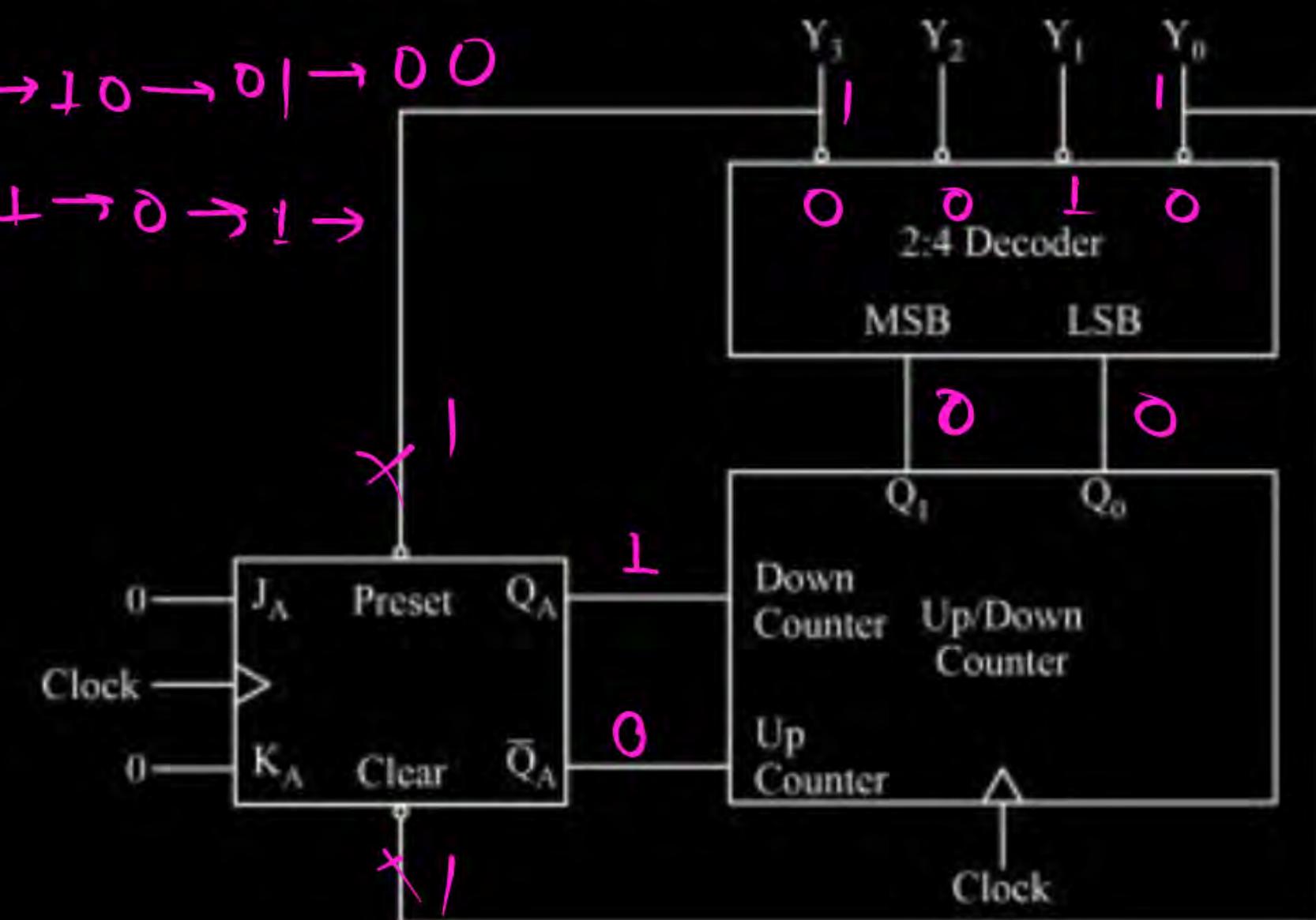
(MCQ)

#Q. Consider the circuit given below

Assuming the initial value of counter output (Q_1, Q_0) as zero, the counter output for 10 clock pulses in decimal form is

$00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 10 \rightarrow 01 \rightarrow 00$
 $0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 0 \rightarrow 1 \rightarrow$

- A** 0, 3, 2, 1, 0, 1, 2, 3, 1, 0
- B** 0, 1, 2, 3, 2, 1, 0, 1, 2, 3
- C** 0, 1, 2, 3, 3, 2, 1, 0, 2, 1
- D** 0, 3, 2, 1, 0, 0, 1, 2, 1, 1

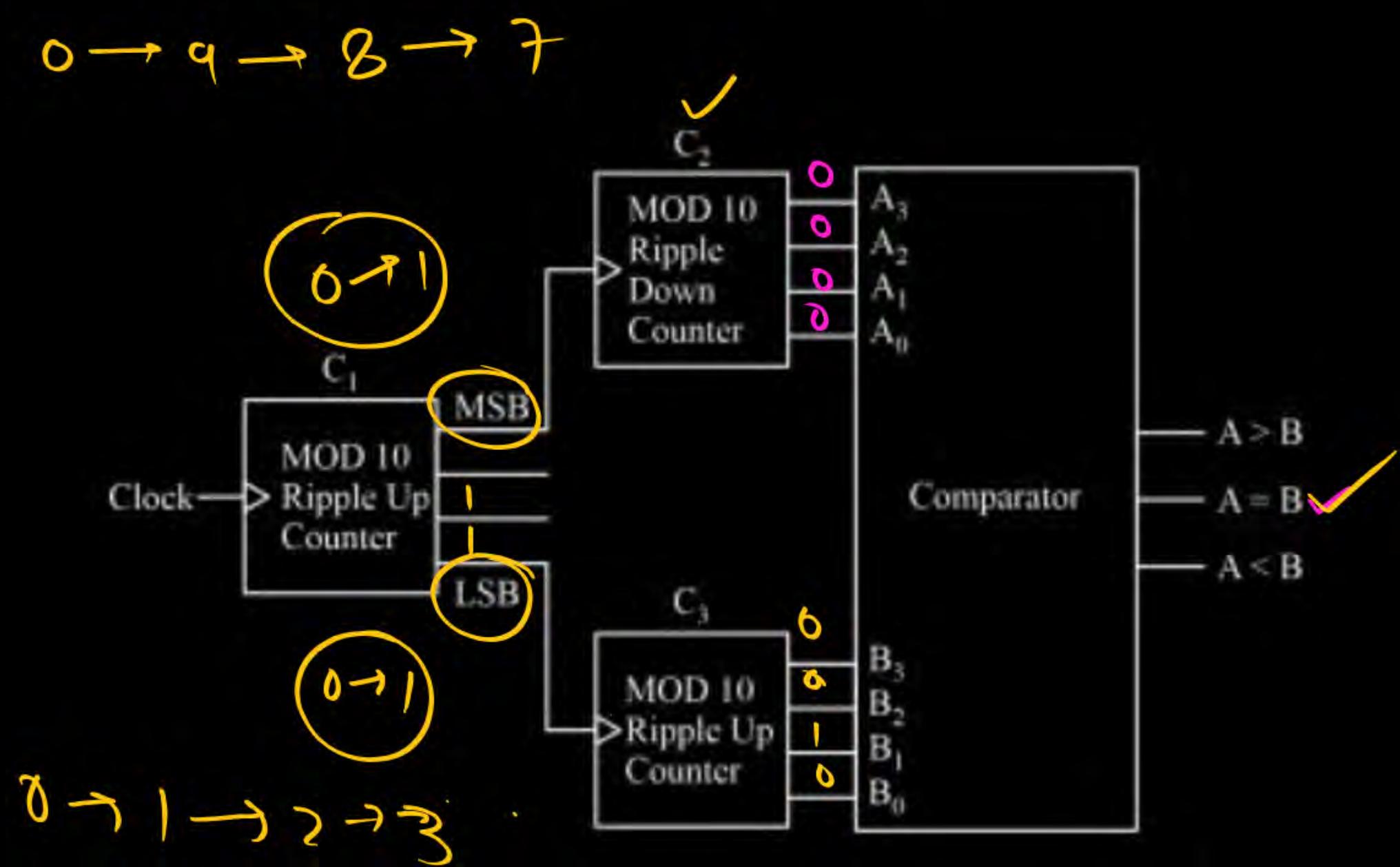


(MCQ)

#Q. Consider the circuit given below

Initially all the counter were reset, and output of comparator was $A = B$.
The minimum number of clock pulses required to make $A = B$ again

- [A] 15
- [B] 16
- [C] 17
- [D] 20



$c_2 \quad c_3$
 0 0 0 0 \rightarrow 1 c_3
 0 0 0 1 \leftarrow
 0 0 1 0 \rightarrow 2 c_3
 0 0 1 1 \leftarrow
 0 1 0 0 \rightarrow 3 c_3
 0 1 0 1 \leftarrow

 c_1

$c_2 \quad \underline{c_3}$
 0 1 1 0 \rightarrow 4 c_3
 0 1 1 1 \leftarrow
 1 0 0 0 \rightarrow 5 c_3
1 0 0 1

0 0 0 0 \rightarrow 6 c_3

0 0 0 1 \leftarrow

0 0 1 0 \rightarrow 7 c_3

0 0 1 1 \leftarrow

0 1 0 0 \rightarrow 8 c_3

0 1 0 1 \leftarrow

0 1 1 0 \rightarrow 9 = c_3

0 1 1 1 \leftarrow

~~1 0 0 6~~

~~c_2 = 8~~
~~1 0 0 1~~

c_2
 c_3

c_2
 c_3

17 clock

#Q. A 4-bit ripple counter and a 5-bit synchronous counter are made by FFs having a propagation delay of 4 ns each. The difference (magnitude) between worst case delay between these counters is ___(ns).

$$T_{\text{Asy}} = 4 \cdot T_{\text{Pd}_{\text{ff}}} = 4 \times 4 \text{ ns} \\ = 16 \text{ ns}$$

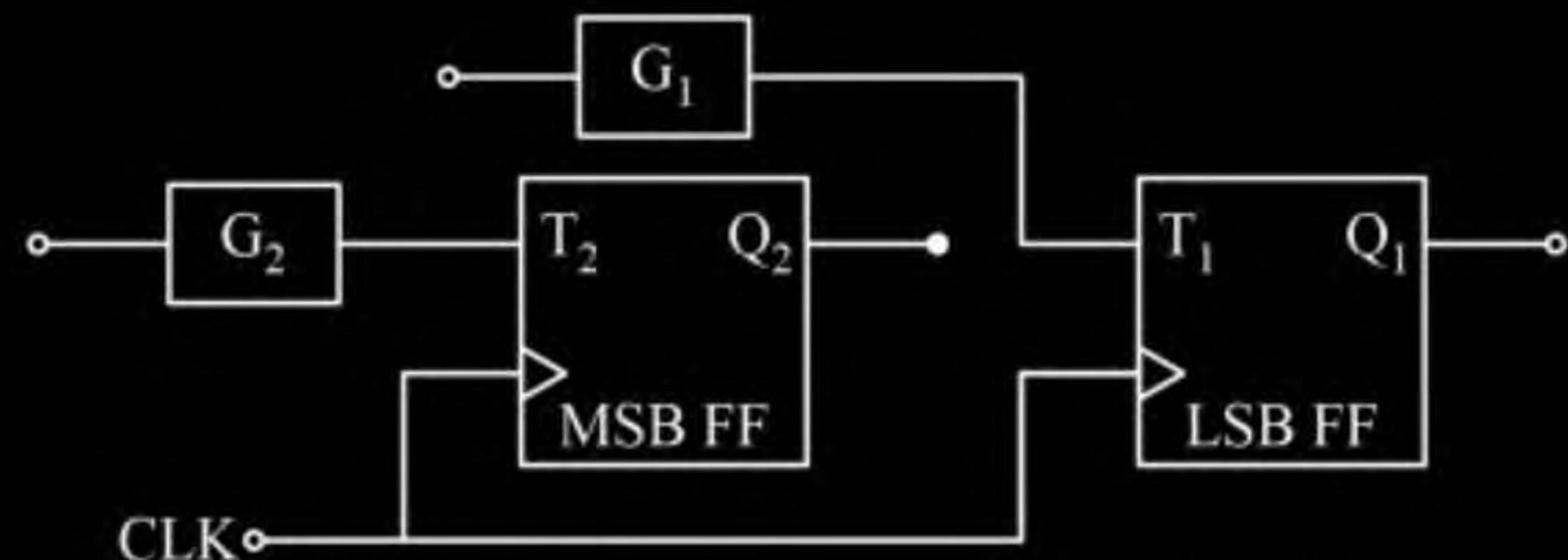
$$\Rightarrow T_{\text{Asy}} - T_{\text{syn}}$$

$$T_{\text{syn}} = T_{\text{Pd}_{\text{ff}}} = 4 \text{ ns} \\ = 16 - 4 = \underline{\underline{12 \text{ ns}}} \checkmark$$

(MCQ)

#Q. By using two T-flip-flops we wish to design a synchronous counter having two-bit random sequence are $00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00$.
For this design of counter, the involved logic gates G1 and G2 respectively are

HW

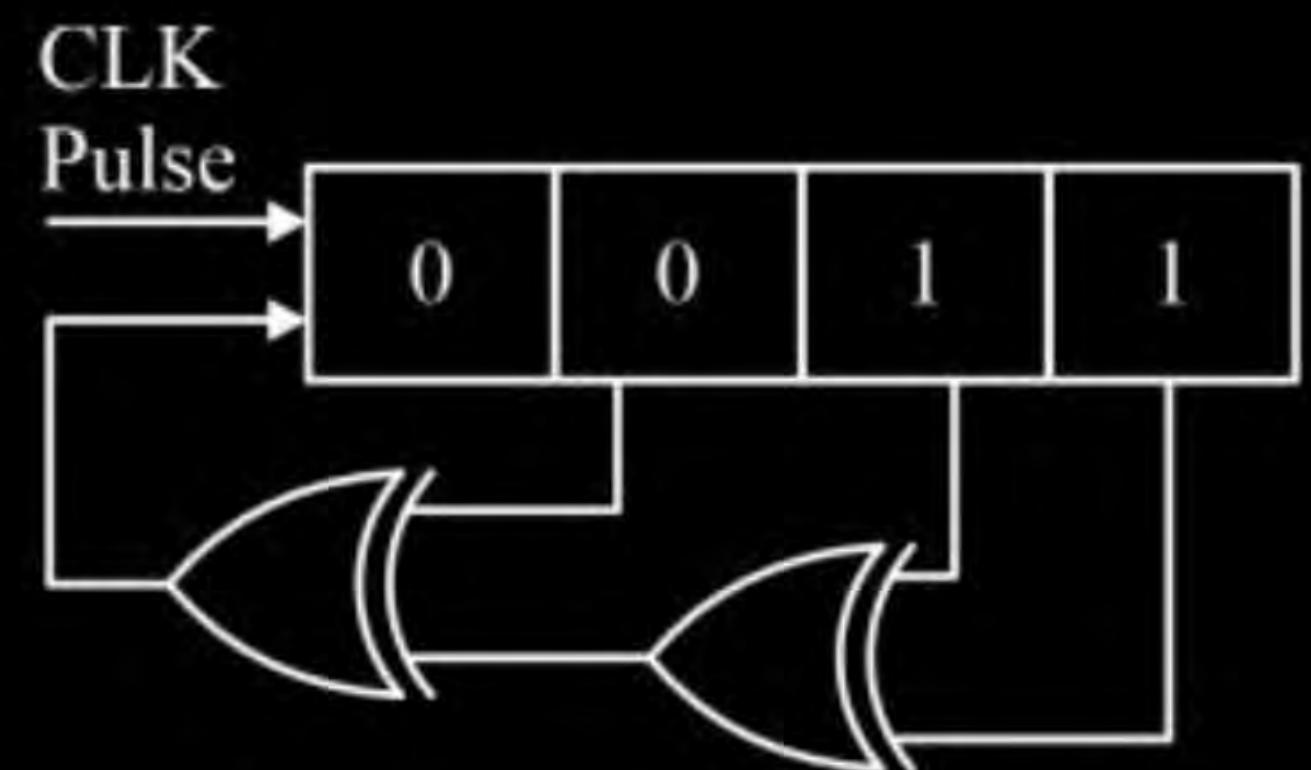


- [A] Ex-OR and NOT
- [C] NOT and Ex-NOR

- [B] Ex-OR and Ex-NOR
- [D] NOT and AND

#Q. The shift register shown below is initially loaded with binary bit stream 0011. If clock pulse are applied continuously and after some clock pulse the loaded data is repeats in shift register. During this the highest decimal data to be stored in the shift register is got for the pulse no._____.

H.W.
=



Thank You
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CS & IT ENGINEERING



DIGITAL LOGIC



Lecture No. - 9



By - CHANDAN SIR

Recap of Previous Lecture



Sequential Circuit

Topics to be Covered



- Questions Practice





Topic : Sequential Circuit

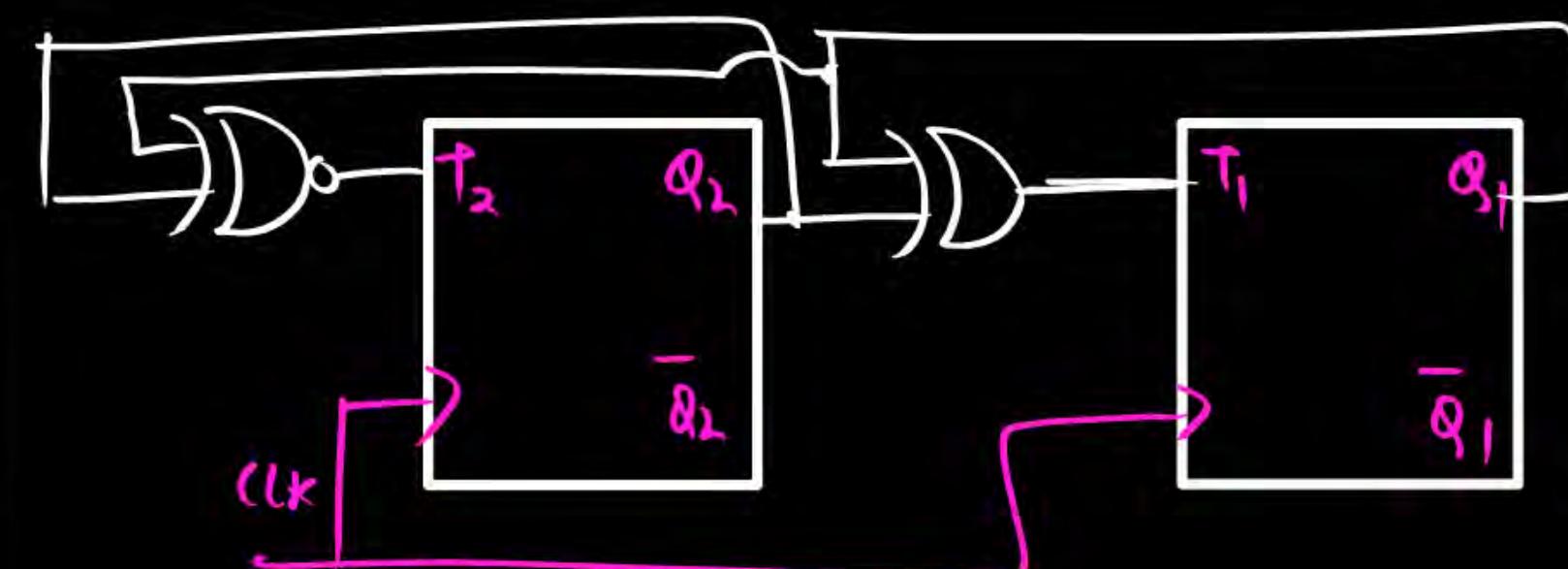
$00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00$

(b)

Q_2	Q_1	Q_2^+	Q_1^+	T_2	T_1
0	0	1	0	1	0
0	1	0	0	0	1
1	0	1	1	0	1
1	1	0	1	1	0

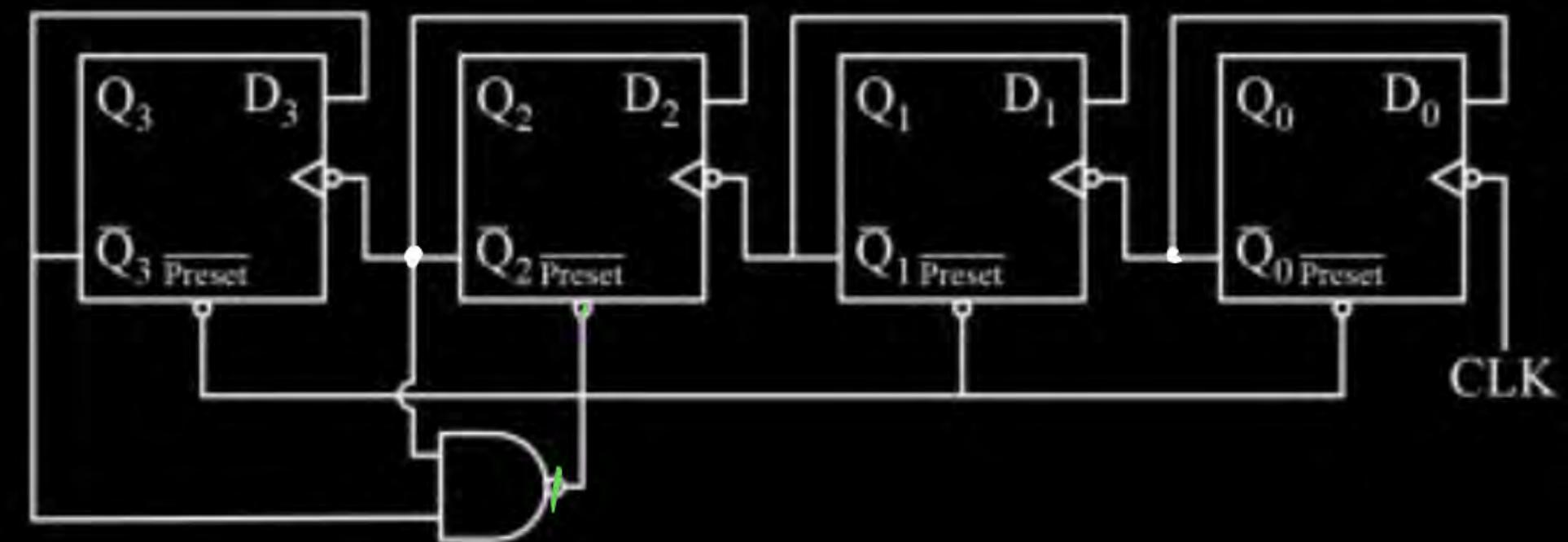
$$T_2 = Q_2 \oplus Q_1$$

$$T_1 = Q_2 \oplus Q_1$$



#Q. Find the Mod number of the counter.

- A** 3
- B** 12
- C** 13
- D** 14

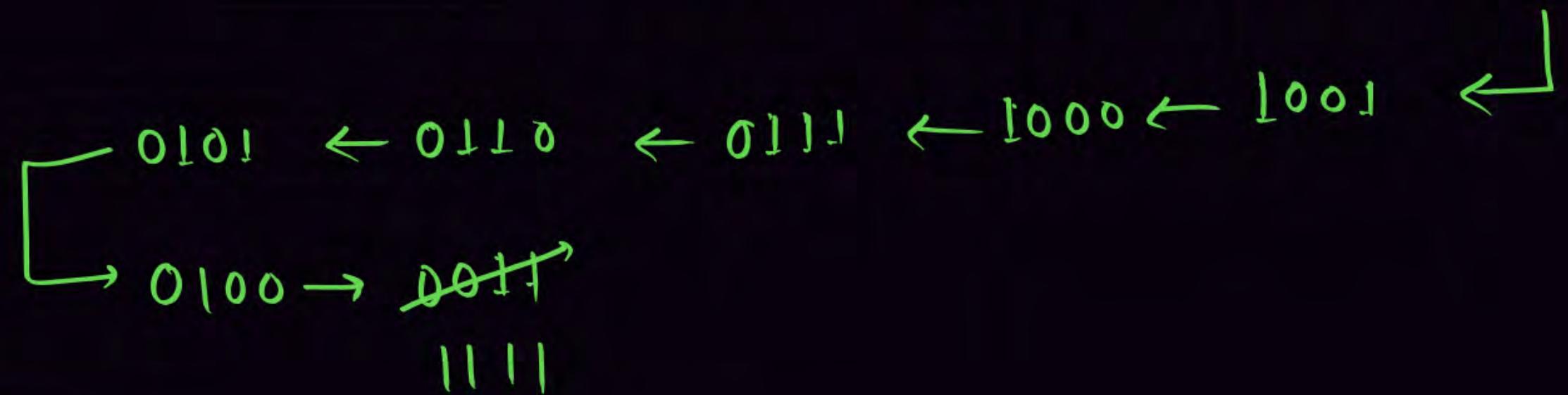


Down counter

$$P_Y = \overline{Q_3} \overline{Q_2} Q_1 Q_0$$

0 0 1 1 → Preset occurs

1 1 1 1 → 1 1 1 0 → 1 1 0 1 → 1 1 0 0 → 1 0 1 1 → 1 0 1 0



MOD 12

(MCQ)

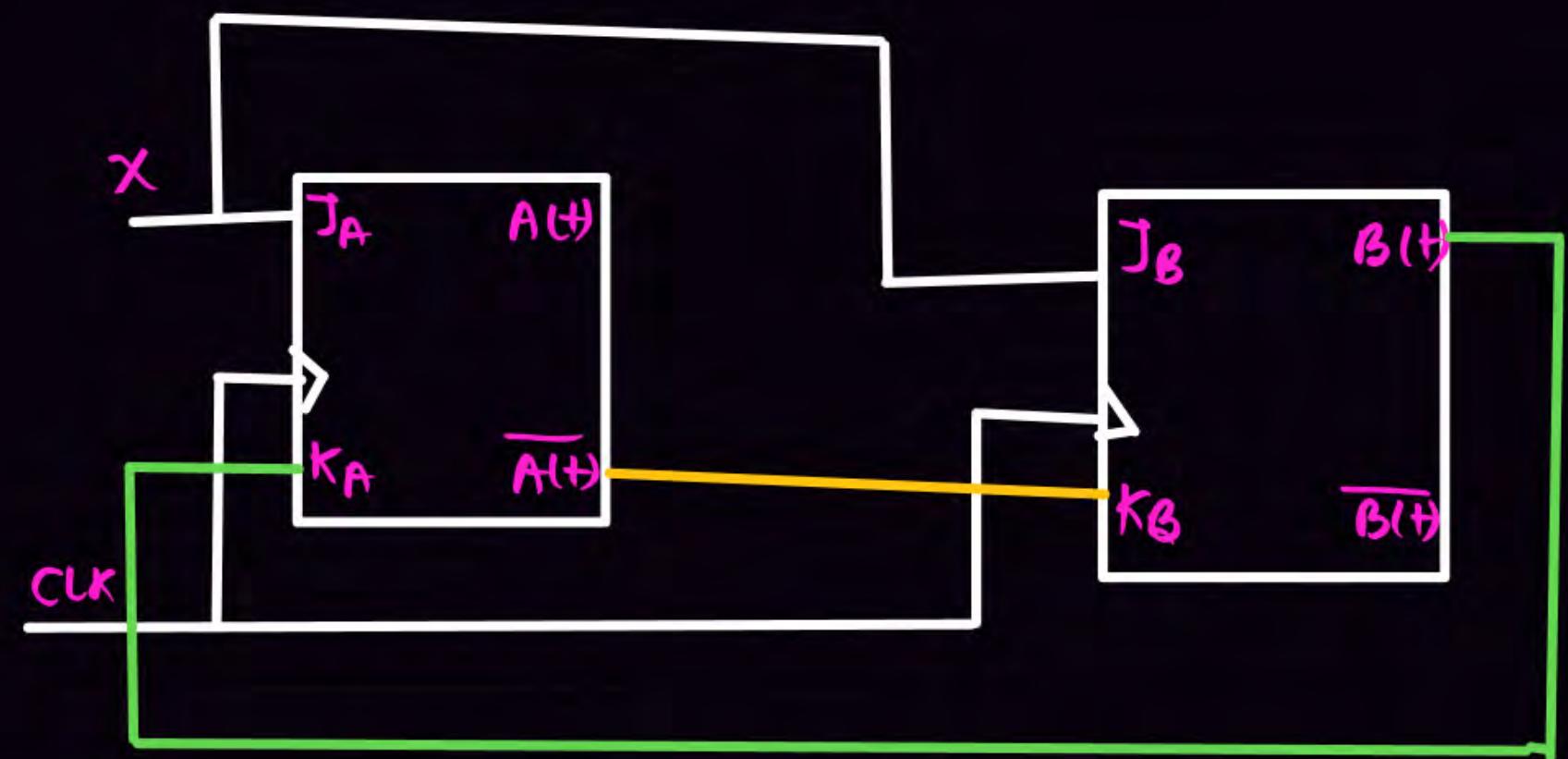
#Q. A sequential circuit has two JK flip-flop A and B and one input x. The circuit is described by the following flipflop input equations:

$$J_A = x, K_A = B$$

$$J_B = x, K_B = \bar{A}$$

The state equations $A(t + 1)$ and $B(t + 1)$ for the given sequential circuit are

- A** ✓ $A(t + 1) = x\overline{A(t)} + A(t)\bar{B}, B(t + 1) = A(t)B(t) + x\overline{B(t)}$
- B** $A(t + 1) = \bar{x}A(t) + \bar{A}(t)B(t), B(t + 1) = A(t)B(t) + x\overline{B(t)}$
- C** $A(t + 1) = A(t)B(t) + x\overline{B(t)}, B(t + 1) = x\overline{A(t)} + A(t)\bar{B}$
- D** $A(t + 1) = \bar{x}\overline{A(t)} + A(t)\bar{B}, B(t + 1) = \bar{A}(t)\bar{B}(t) + x\overline{B(t)}$

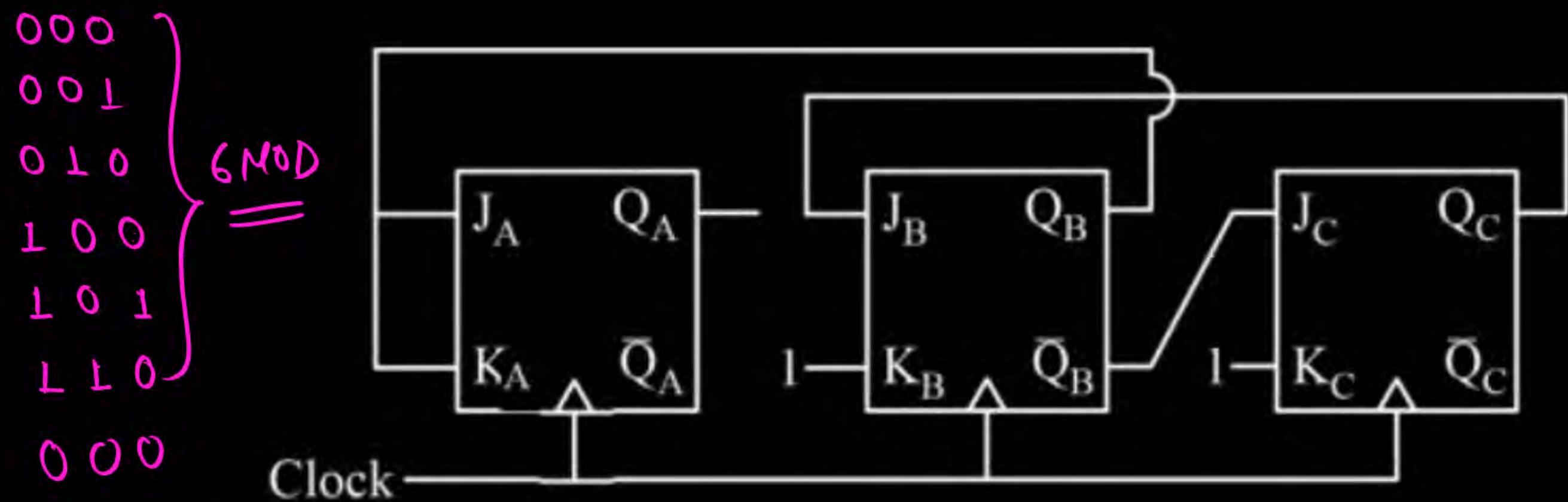


$$Q(t+1) = J \bar{Q}(t) + \bar{K} Q(t)$$

$$B(t+1) = X \bar{B}(t) + A(t) \cdot B(t)$$

$$A(t+1) = X \bar{A}(t) + \bar{B}(t) A(t)$$

#Q. Consider the sequential circuit given below. The number of unused states are 2.



Used state = 6

Unused state = 2

#Q. The initial state of the Johnson counter is 0100010. The number of clock pulses required to return to the initial state are ____.

0100010

1 → 1010001

2 → 0101000

,

,

,

,

19th → 0100010

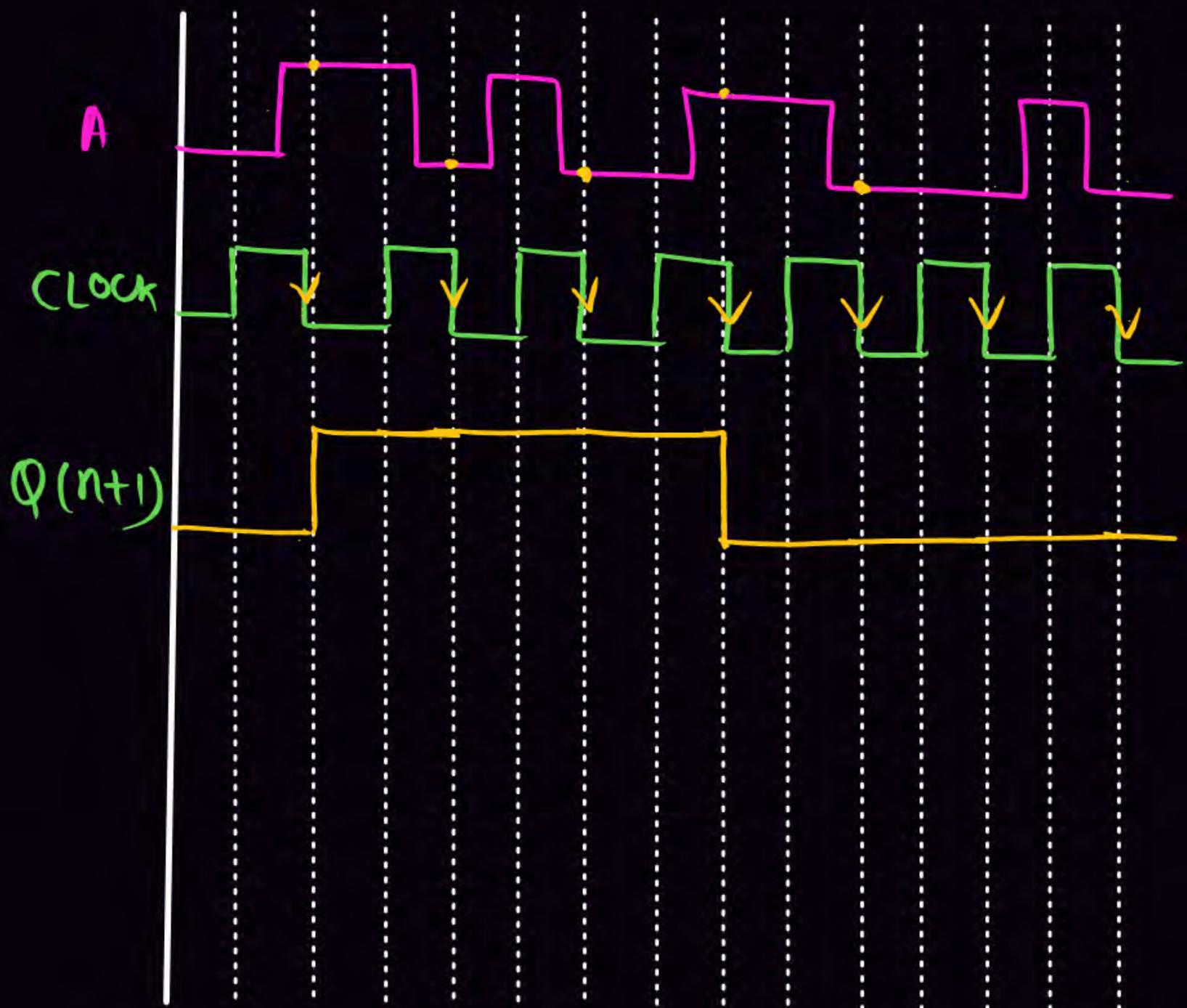
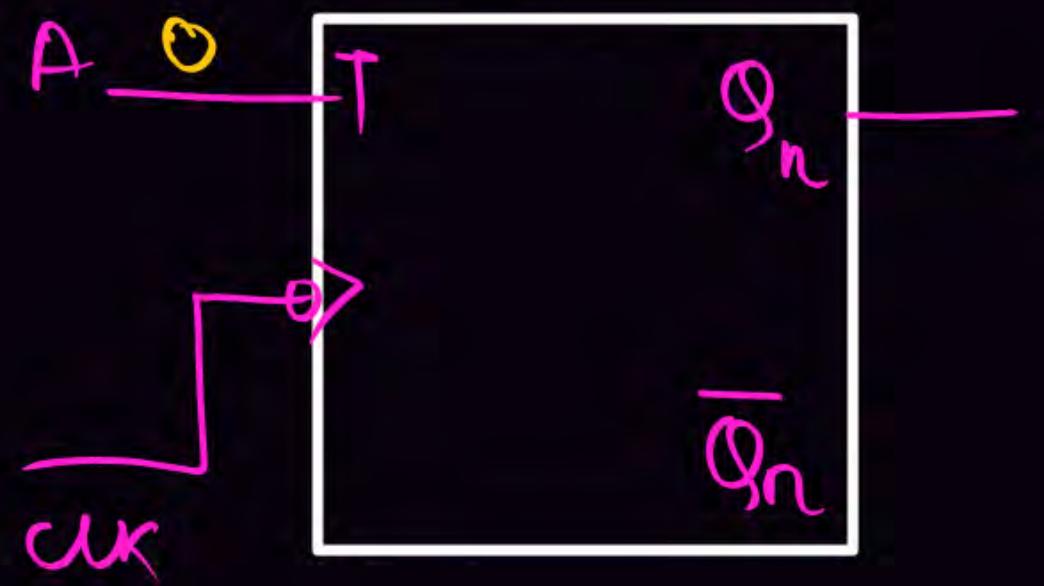
#Q. A switch-tail ring counter consisting of 4-FFs. If this counter has N states and it counts the maximum decimal number M, the value of M-N is ____.

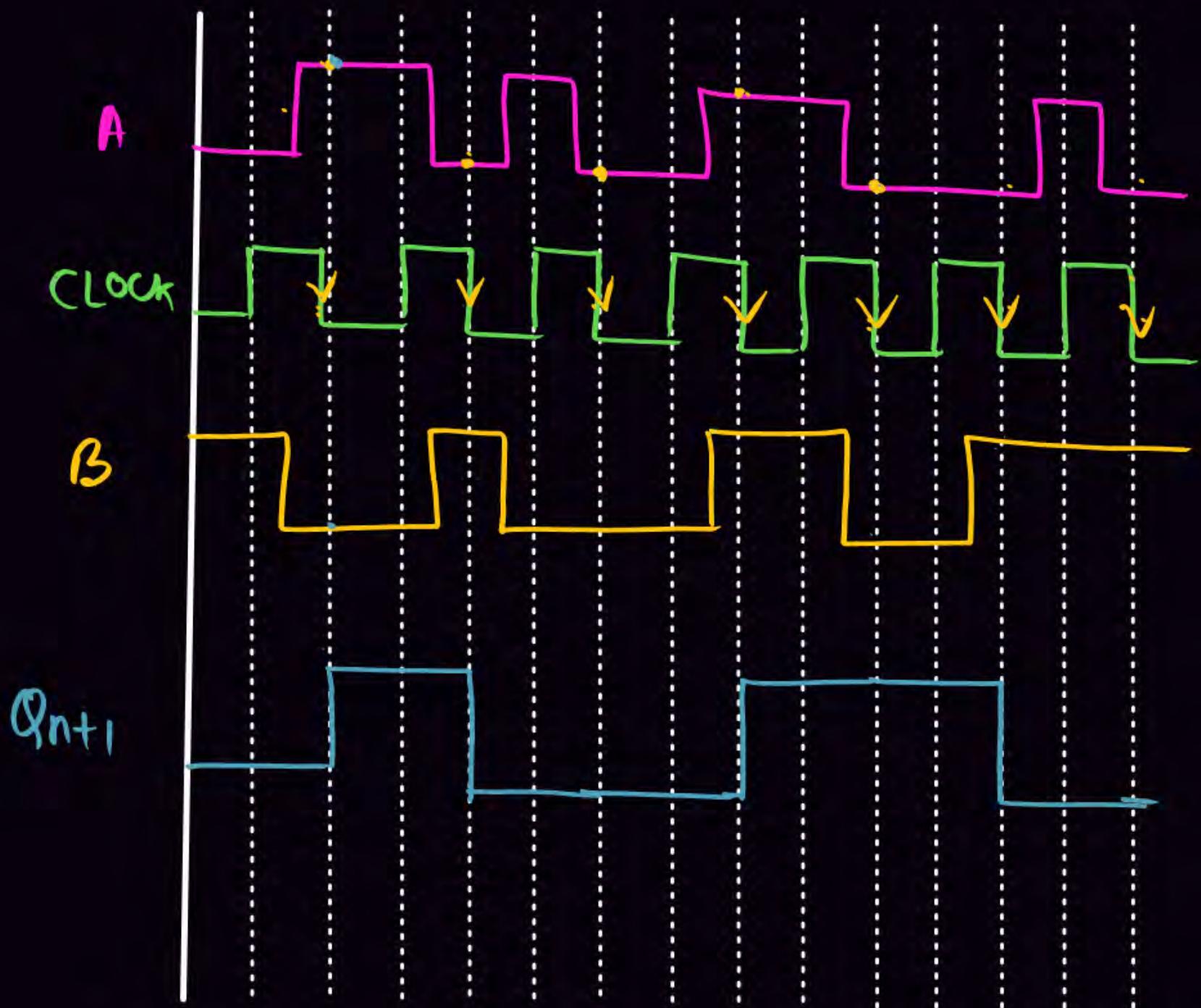
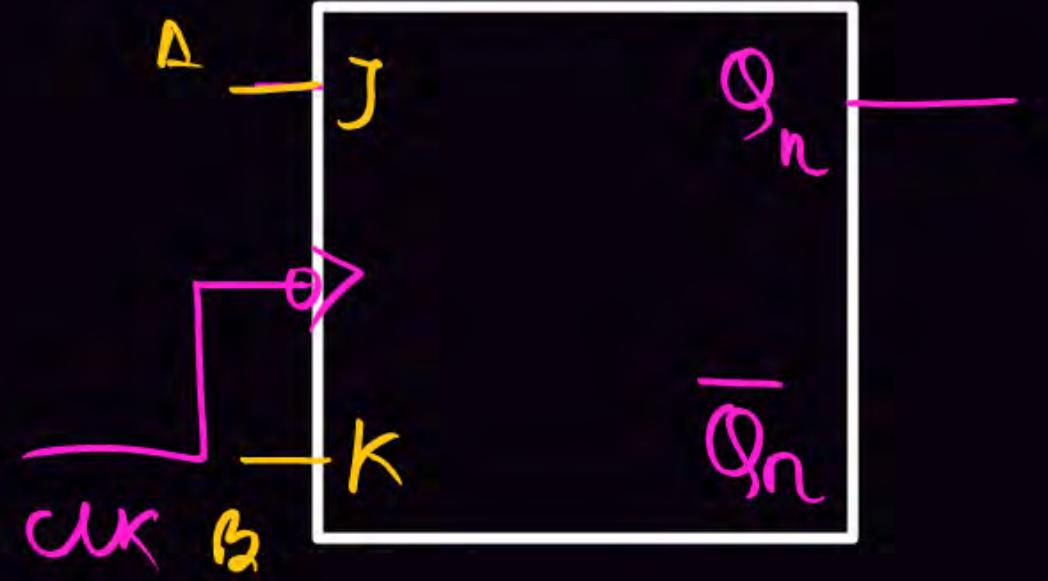
$$M = 2^n - 1 = 15$$

$$N = 2n = 8$$

$$M - N = 15 - 8 = 7$$

Avg

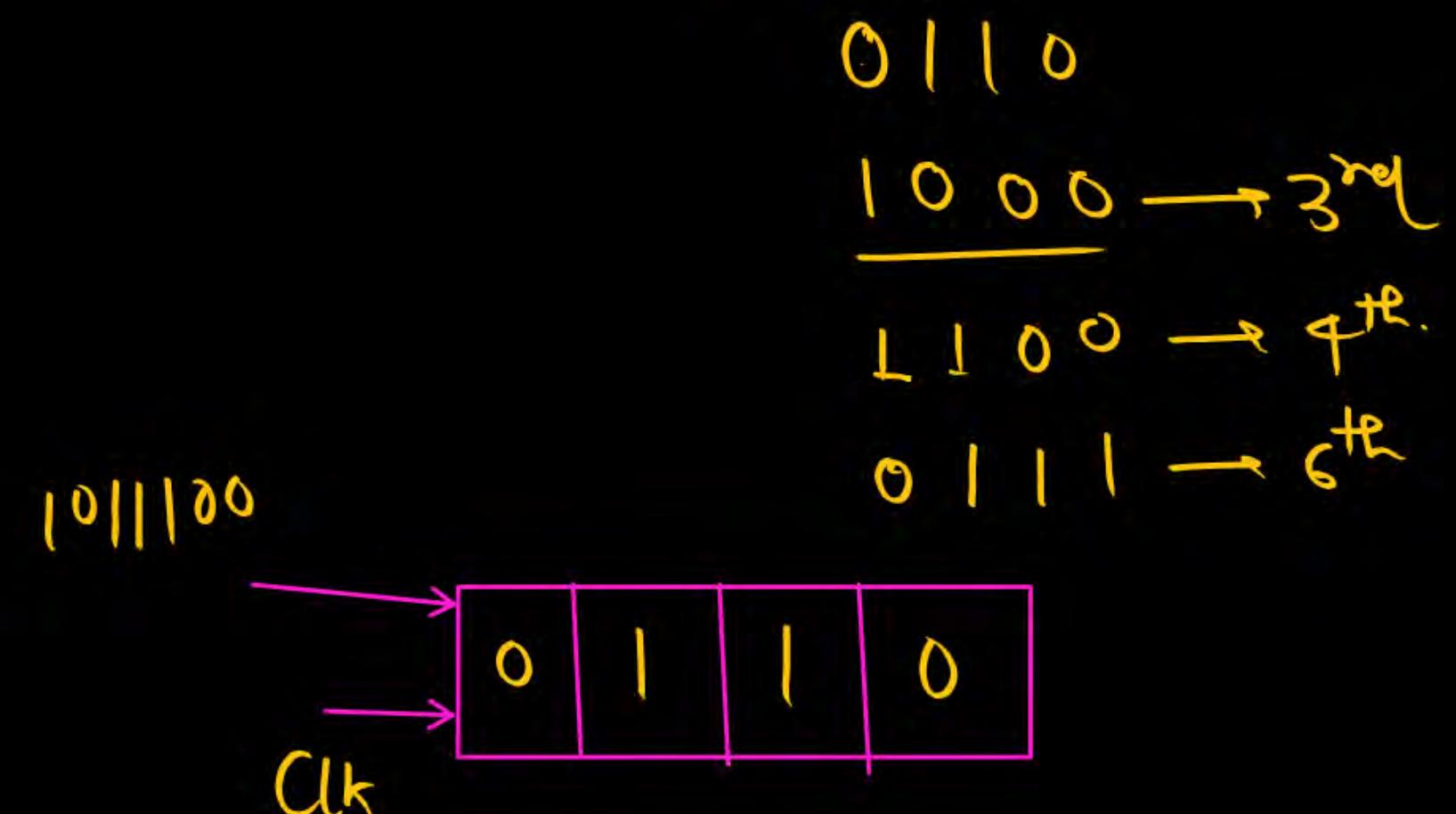




(MCQ)

#Q. The contents of a register initially is 0110. The register is shifted six times to the right with serial input being 1011100. The contents of the register after 3rd, 4th & 6th shifts respectively are.

- A** 1010,1101,1110
- B** 0001, 0011, 0111
- C** 1000, 1100, 1011
- D** 1000, 1100, 0111



(MCQ)

#Q. The initial word content of a 4-bit register is 1111. This is first shifted three counts to the right and then two counts to the left. The new content word of the register will be (both shift right and shift left are performed through 0_s)

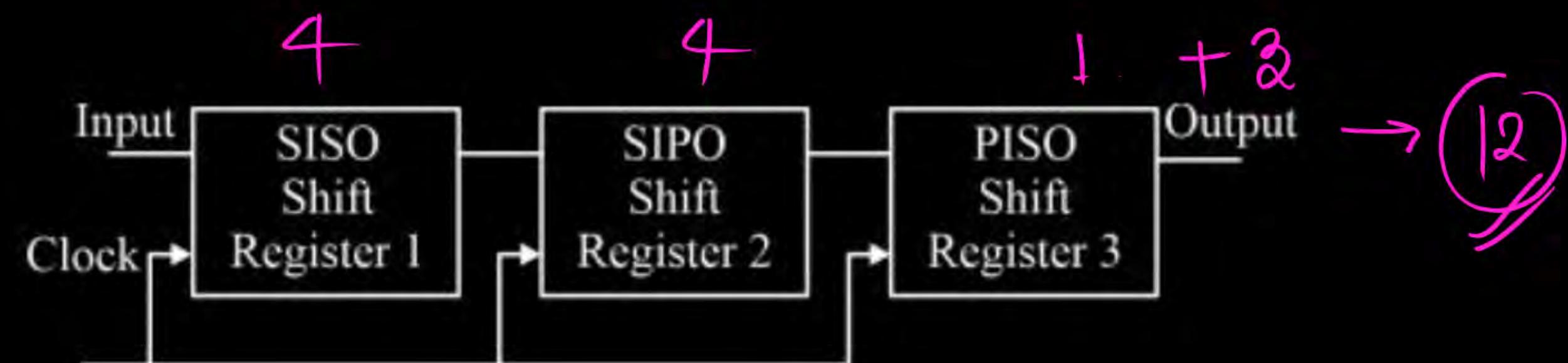
- A** ✓ 0100
- B** 0010
- C** 0011
- D** 1100

1111
1 → 0111
2 → 0011
3 → 0001
4 → 0010
5 → 0100

(MCQ)

#Q. Three 4-bit shift registers are connected in cascade as shown in figure below. Each register is applied with same clock. A 4-bit data 1011 is applied to the shift register 1. The minimum number of clock pulses required to get same input data at output are

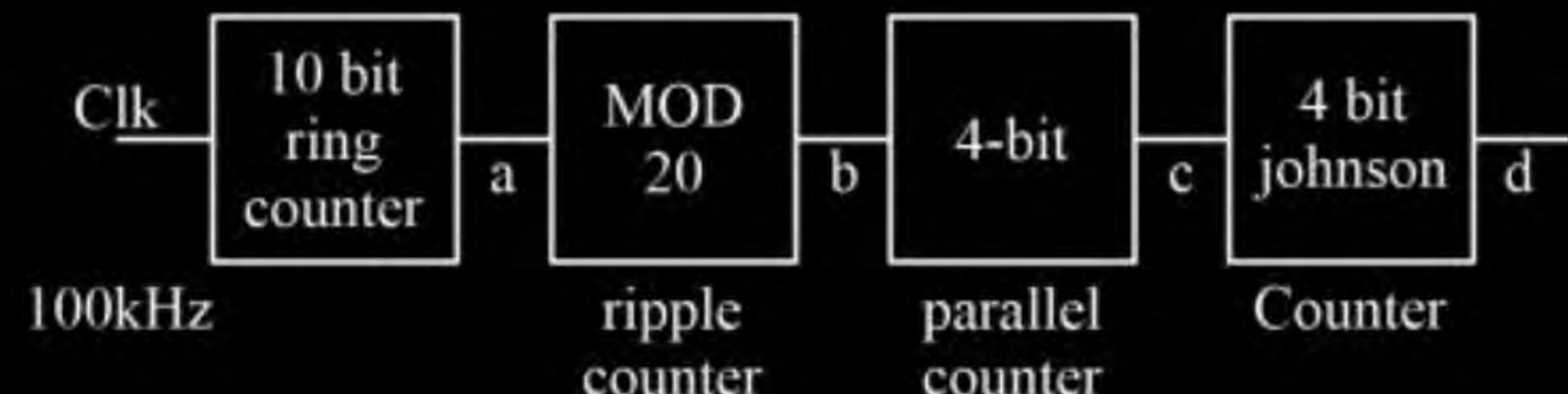
- A** 11
- B** 12
- C** 9
- D** 7



#Q. A SISO shift register may be used to introduce time delay $\Delta T = 200$ ns in digital signals. Assume this shift registers is manufactured by 'N' number of D flip-flops having clock frequency 50MHz. The required value of 'N' is ____.

#Q. The frequency of the pulses at the point d in the following circuit is _____ Hz.

HW



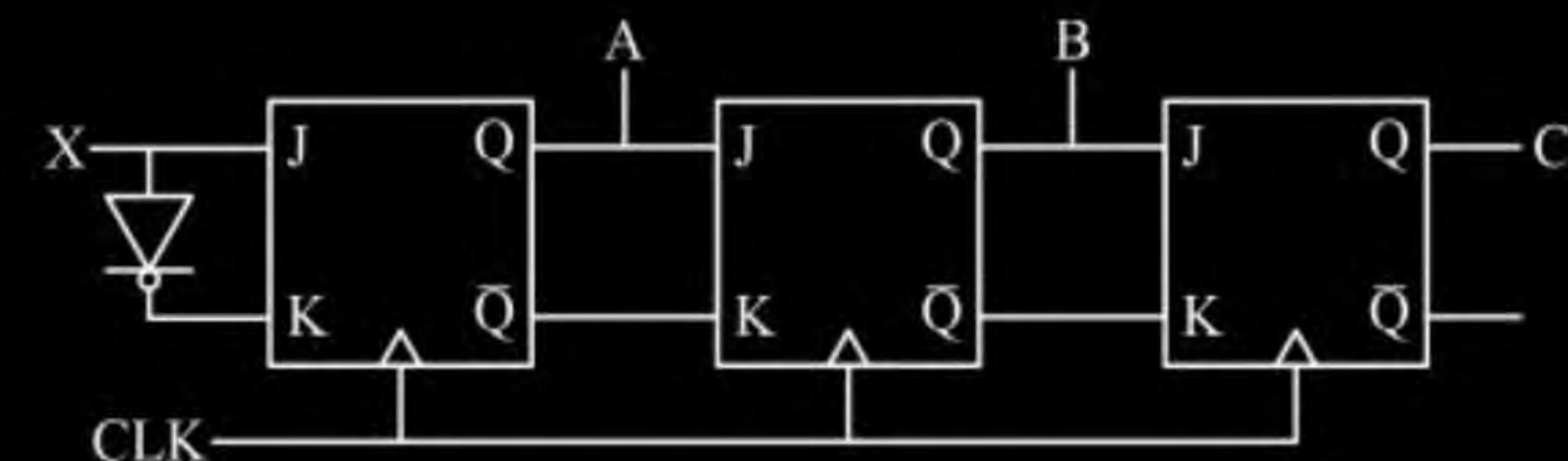
(MCQ)

#Q. For the circuit given below,

If input $X = 1, 0, 1$, with register initially cleared, then after three clock pulses the value of A, B and C is

H W

- A** 1, 0, 1
- B** 0, 1, 1
- C** 1, 1, 1
- D** 0, 1, 0



(MCQ)

A number N is stored in a 4 bit 2's complement format as

HW

d_3	d_2	d_1	d_0
-------	-------	-------	-------

It is copied into a 6-bit register and after few operations, the final bit pattern is

d_3	d_3	d_2	d_1	d_0	1
-------	-------	-------	-------	-------	---

The value of this bit pattern in 2's complement format is expressible in terms of original number N as

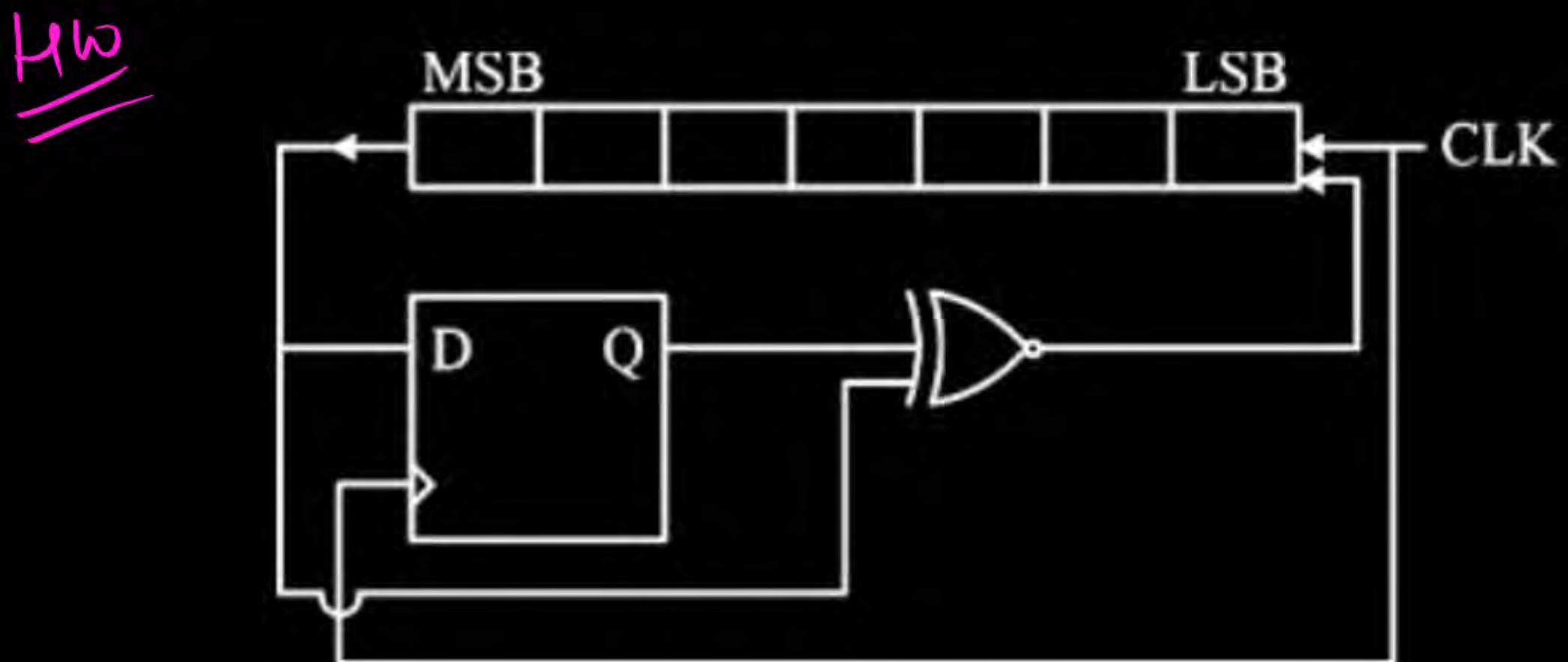
| A $32 d_3 + 2N + 1$

| B $32 d_3 + 2N - 1$

| C $2N - 1$

| D $2N + 1$

A 7-bit register with shift left is configured with D FF as shown below. The FFs used in register are set and other FF is in reset state.



The content of register after 3 clock pulse is $(__)_{10}$.

Thank You
GW
soldiers!

