

2

# Digital Logic

## Practice Questions

## Number System



- Q.2** Decimal 43 in Hexadecimal and BCD number system is respectively

(A)B2, 01000011  
(B) 2B, 01000011  
(C) 2B, 0011 0100  
(D)B2, 01000100

- Q.3**  $X = 01110$  and  $Y = 11001$  are two 5-bit binary numbers represented in two's complement format. The sum of  $X$  and  $Y$  represented in 2's complement format using 6 bits is

(A) 100111      (B) 001000  
 (C) 000111      (D) 101001

- Q.4** The two numbers represented in signed 2's complement form are

$$P = 11101101 \text{ and } Q = 11100110$$

If  $Q$  is subtracted from  $P$ , the value obtained in signed 2's complement form is

- Q5** What is the gray code word for the binary number 101011?  
(A) 110101      (B) 111110  
(C) 101011      (D) 011111

- Q.6** Consider the equation  $(123)_5 = (x8)_y$ , with  $x$  and  $y$  as unknown. The number of possible solutions are \_\_\_\_\_.



- Q.8** The number  $(A72E)_{16}$  is equivalent to  
(A)  $(1010001100101110)_2$  and  
 $(123456)_8$   
(B)  $(1010011100111111)_2$  and  
 $(123456)_8$   
(C)  $(1010011100101110)_2$  and  
 $(123456)_8$   
(D) None of these

## Boolean Algebra

- Q.9** The K-map for a Boolean function is shown below. The number of essential prime implicants for this function is

$\overline{AB}$	00	01	11	10	
$CD$	00	1	1	0	1
	01	0	0	0	1
	11	1	0	0	0
	10	1	0	0	1



- (A) 4 (B) 5  
 (C) 6 (D) 8

**Q.10** The logical expression  $y = A + \bar{A}B$  is equivalent to  
 (A)  $y = AB$  (B)  $y = \bar{A}B$   
 (C)  $y = \bar{A} + B$  (D)  $y = A + B$

**Q.11** The minimized form of the logical expression  $(\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C})$  is  
 (A)  $\bar{A}\bar{C} + B\bar{C} + \bar{A}B$   
 (B)  $A\bar{C} + \bar{B}C + \bar{A}B$   
 (C)  $\bar{A}C + \bar{B}C + \bar{A}B$   
 (D)  $A\bar{C} + \bar{B}C + A\bar{B}$

**Q.12** The number of distinct Boolean expression of 4 variables is  
 (A) 16 (B) 256  
 (C) 1024 (D) 65536

**Q.13** The Boolean expression  $Y = \bar{A}\bar{B}\bar{C}D + \bar{A}BC\bar{D} + A\bar{B}\bar{C}D + AB\bar{C}\bar{D}$  can be minimized to  
 (A)  $Y = \bar{A}\bar{B}\bar{C}D + \bar{A}B\bar{C} + A\bar{C}D$   
 (B)  $Y = \bar{A}\bar{B}\bar{C}D + BC\bar{D} + A\bar{B}\bar{C}D$   
 (C)  $Y = \bar{A}BC\bar{D} + \bar{B}\bar{C}D + A\bar{B}\bar{C}D$   
 (D)  $Y = \bar{A}BC\bar{D} + \bar{B}\bar{C}D + AB\bar{C}\bar{D}$

**Q.14** The number of essential prime implicants in the function  
 $f(a, b, c, d) = \Sigma(1, 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, 15)$  is \_\_\_\_\_.

**Q.15** The Boolean expression  $(X + Y)(X + \bar{Y}) + \overline{(X\bar{Y})} + \bar{X}$  simplifies to  
 (A)  $X$  (B)  $Y$   
 (C)  $XY$  (D)  $X+Y$

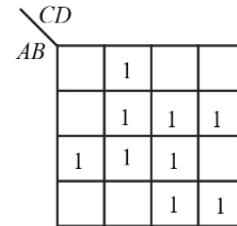
**Q.16** Consider the Boolean function,

$$F(w,x,y,z) = wy + xy + \bar{w}x yz \\ + \bar{w}\bar{x}yz + xz + \bar{x}\bar{y}\bar{z}$$

Which one of the following is the complete set of essential prime implicants?

- (A)  $w, y, xz, \bar{x}\bar{z}$       (B)  $w, y, xz$   
 (C)  $y, \bar{x}\bar{y}\bar{z}$       (D)  $y, xz, \bar{x}\bar{z}$

**Q.17** Find how many number of literals are there in given K-map by using all possible type K-map?






**Q.18** A function of Boolean variables  $X$ ,  $Y$  and  $Z$  is expressed in terms of the minterms as  $F(X, Y, Z) = \sum m(1, 2, 5, 6, 7)$

Which one of the product of sums given below is equal to the function  $F(X,Y,Z)$ ?

- (A)  $(\bar{X} + \bar{Y} + \bar{Z})(\bar{X} + Y + Z)(X + \bar{Y} + \bar{Z})$   
 (B)  $(X + Y + Z)(X + \bar{Y} + \bar{Z})(\bar{X} + Y + Z)$

$$(C) (\overline{X} + \overline{Y} + Z)(\overline{X} + Y + \overline{Z})$$

$$(X + \overline{Y} + Z)(X + Y + \overline{Z})(X + Y + Z)$$

$$(D) (X+Y+Z)(X+Y+Z) \\ (\bar{X}+Y+\bar{Z})(\bar{X}+\bar{Y}+Z)(\bar{X}+\bar{Y}+\bar{Z})$$

Consider the following expression:

$$f(A, B, C, D) = AD + ABCD + ACD$$

$$+AB+ACD+AB+A(B+A)$$

The minimized expression of  $f(A, B, C, D)$  is equal to



- (A)  $AD$       (B)  $\bar{A} + D$   
 (C)  $A + B\bar{C}$       (D)  $A\bar{D} + B\bar{C}$

**Q.20** Consider the function

$$f(A,B,C,D) = \Sigma m(1,5,7,12,13,14) + d(0,3,11,15)$$

After implementing the given function in minimal SOP form, what is the output for the inputs  $ABCD = 0011$ ,  $1011$  and  $1111$  respectively?

- (A) 0, 0 and 1      (B) 0, 1 and 0  
 (C) 1, 0 and 1      (D) 1, 1 and 1

## Logic Gates

**Q.21** Consider the Karnaugh map given below, where X represents “don’t care” and blank represents 0.

$dc$	$ba$	00	01	11	10
00		$x$	$x$		
01	1				$x$
11	1				1
10		$x$	$x$		

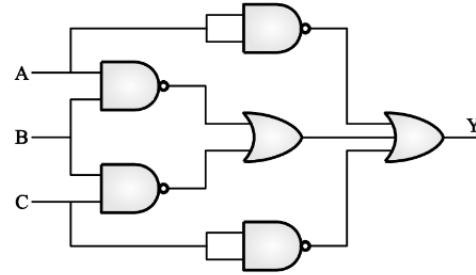
Assume for all input  $(a, b, c, d)$ , the respective complements  $(\bar{a}, \bar{b}, \bar{c}, \bar{d})$  are also available. The above logic is implemented using 2-input NOR gates only.

The minimum number of gates required is .

**Q.22** Minimum number of 2-input NAND gates required to implement the function,  $F = (\bar{X} + \bar{Y})(Z + W)$  is



**Q.23** For the logic circuit shown in figure, the output is equal to [MSQ]



- (A)  $\overline{ABC}$   
 (B)  $\bar{A} + \bar{B} + \bar{C}$   
 (C)  $\overline{AB} + \overline{BC} + \overline{A} + \overline{C}$   
 (D)  $\overline{AB} + \overline{BC}$

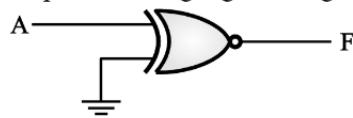
**Q.24** The output of a logic gate is ‘1’ when all its inputs are at logic ‘0’. The gate is either

- (A) a NAND or an EX-OR gate.
  - (B) a NOR or an EX-NOR gate.
  - (C) an OR or an EX-NOR gate.
  - (D) an AND or an EX-OR gate.

**Q.25** The minimum number of NAND gates required to implement the Boolean function  $A + A\bar{B} + A\bar{B}C$  is equal to



**Q.26** The output of the logic gate in figure is

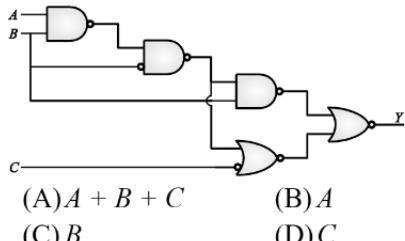





**Q.27** The minimum number of 2-input NAND gates required to implement the Boolean function  $Z = A\bar{B}C$ , assuming that  $A$ ,  $B$  and  $C$  are available is

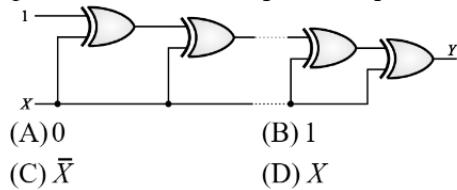


**Q.28** For the logic circuit shown in figure, the simplified Boolean expression for the output  $Y$  is



- (A)  $A + B + C$       (B)  $A$   
 (C)  $B$       (D)  $C$

**Q.29** If the input to the digital circuit consisting of a cascade of 20 X-OR gates is  $X$ , then the output  $Y$  is equal to

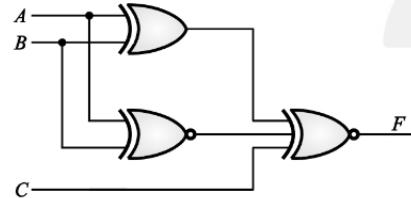


- (A) 0      (B) 1  
 (C)  $\bar{X}$       (D)  $X$

**Q.30** The Boolean function  $Y = AB + CD$  is to be realized using only 2-input NAND gates. The minimum number of gates required is

- (A) 2      (B) 3  
 (C) 4      (D) 5

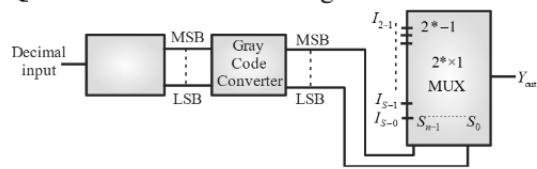
**Q.31** For the output  $F$  to be 1 in the logic circuit shown, the input combination should be



- (A)  $A = 1, B = 1, C = 0$   
 (B)  $A = 1, B = 0, C = 0$   
 (C)  $A = 0, B = 1, C = 0$   
 (D)  $A = 0, B = 0, C = 1$

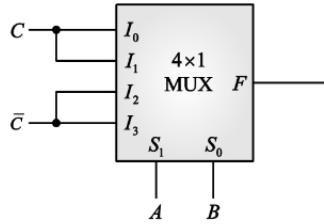
### Combinational Circuits

**Q.32** Consider the circuit given below :



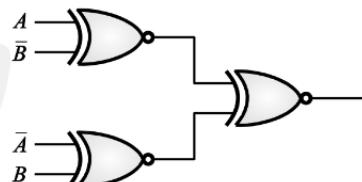
If the decimal input is 92 then  $Y_{\text{out}}$  corresponds to  $I_{\text{gv}}$  then value of m is \_\_\_\_.

**Q.33** The logic realized by the circuit shown in figure is



- (A)  $F = A \odot C$       (B)  $F = A \oplus C$   
 (C)  $F = B \odot C$       (D)  $F = B \oplus C$

**Q.34** The output of the circuit shown in figure is equal to



- (A) 0      (B) 1  
 (C)  $\bar{A}B + A\bar{B}$   
 (D)  $(\overline{A \oplus B}) \oplus (\overline{A \oplus B})$

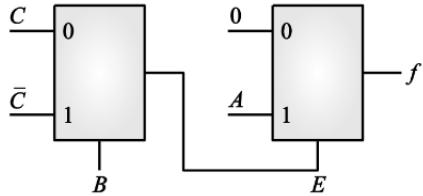
**Q.35** A 2-bit binary multiplier can be implemented using

- (A) 2 input AND gates only.  
 (B) Six 2-input AND gates and two XOR gates.  
 (C) Two 2-input NORs and one XNOR gate.  
 (D) XOR gates and shift registers.

**Q.36** The minimum number of 2 to 1 multiplexers required to realize a 4 to 1 multiplexer is

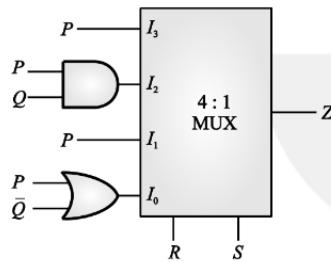
- (A) 1      (B) 2  
 (C) 3      (D) 4

**Q.37** The Boolean function ' $f$ ' implemented in the figure using two input multiplexers is



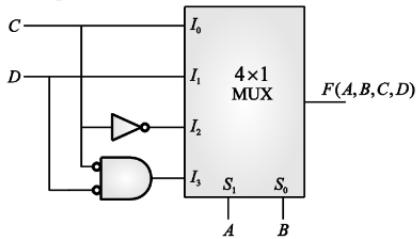
- (A)  $A\bar{B}C + A\bar{B}\bar{C}$   
 (B)  $ABC + A\bar{B}\bar{C}$   
 (C)  $\bar{A}BC + \bar{A}\bar{B}\bar{C}$   
 (D)  $\bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$

**Q.38** For the circuit shown in the following figure,  $I_0 - I_3$  are inputs to the 4 : 1 multiplexer.  $R$  (MSB) and  $S$  are control bits.



- The output  $Z$  can be represented by,  
 (A)  $PQ + PS + \bar{Q}\bar{R}\bar{S}$   
 (B)  $P\bar{Q} + PQ\bar{R} + \bar{P}\bar{Q}\bar{S}$   
 (C)  $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}\bar{R}\bar{S}$   
 (D)  $PQ\bar{R} + PQR\bar{S} + P\bar{Q}\bar{R}S + \bar{Q}\bar{R}\bar{S}$

**Q.39** The Boolean function realized by the logic circuit shown is

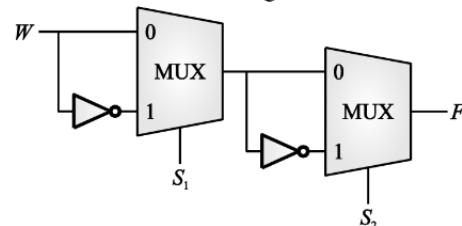


- (A)  $F = \sum m(0, 1, 3, 5, 9, 10, 14)$   
 (B)  $F = \sum m(2, 3, 5, 7, 8, 12, 13)$   
 (C)  $F = \sum m(1, 2, 4, 5, 11, 14, 15)$   
 (D)  $F = \sum m(2, 3, 5, 7, 8, 9, 12)$

**Q.40** The output  $Y$  of a 2-bit comparator is logic 1 whenever the 2-bit input  $A$  is greater than the 2-bit input  $B$ . The number of combinations for which the output is logic 1, is

- (A) 4 (B) 6  
 (C) 8 (D) 10

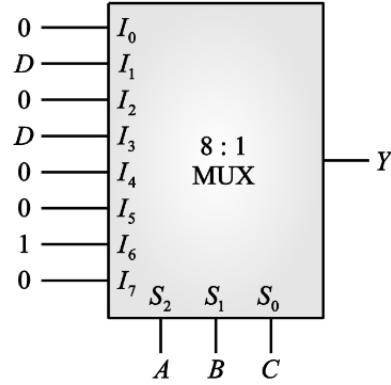
**Q.41** Consider the multiplexer based logic circuit shown in the figure.



Which one of the following Boolean functions is realized by the circuit?

- (A)  $F = W\bar{S}_1\bar{S}_2$   
 (B)  $F = WS_1 + WS_2 + S_1S_2$   
 (C)  $F = \bar{W} + S_1 + S_2$   
 (D)  $F = W \oplus S_1 \oplus S_2$

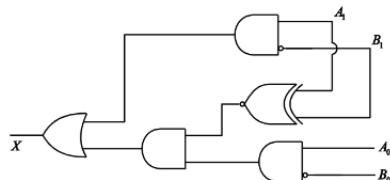
**Q.42** An 8 to 1 multiplexer is used to implement a logical function  $Y$  as shown in the figure. The output  $Y$  is given by



- (A)  $Y = A\bar{B}C + A\bar{C}D$   
 (B)  $Y = \bar{A}BC + A\bar{B}D$   
 (C)  $Y = AB\bar{C} + \bar{A}CD$   
 (D)  $Y = \bar{A}\bar{B}C + A\bar{B}C$



**Q.43** Consider the given circuit

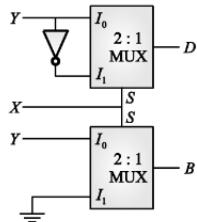


The logic circuit above is used to compare two unsigned 2-bit number. Where  $A = A_1A_0$  and  $B = B_1B_0$ , where  $A_1$  and  $B_1$  represent MSB and  $A_0$  and  $B_0$  represent LSB. Which of the following will make output  $X=1$  always.

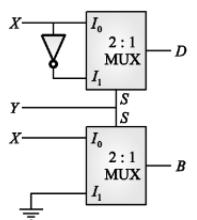
- (A)  $A > B$       (B)  $A < B$   
 (C)  $A \pm B$       (D)  $A \geq B$

**Q.44** If  $X$  and  $Y$  are inputs and the Difference ( $D = X - Y$ ) and the Borrow ( $B$ ) are the outputs, which one of the following diagrams implements a half-subtractor?

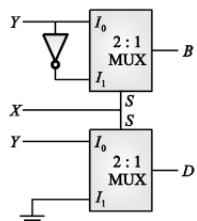
(A)



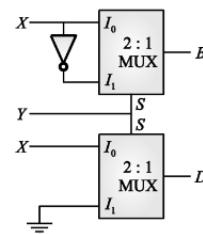
(B)



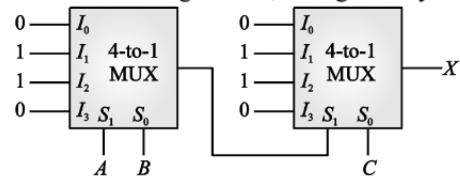
(C)



**(D)**

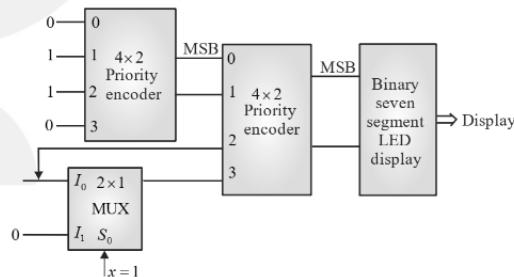


**Q.45** In the following circuit,  $X$  is given by



- (A)  $X = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$   
 (B)  $X = \bar{A}BC + A\bar{B}C + ABC\bar{C} + \bar{A}\bar{B}\bar{C}$   
 (C)  $X = AB + BC + AC$   
 (D)  $X = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$

**Q.46** Consider the combinational circuit below :



What is the output of the combinational circuit?

- (A) 1      (B) 2  
 (C) 3      (D) 4

### Sequential Circuit

**Q.47** A-S-R flip flop with a clock input can be converted to a 'D' flip flop using :

- (A) Two inverters  
 (B) The flip flop outputs ( $Q$  &  $\bar{Q}$ ) connected to its inputs ( $S$  &  $R$ )  
 (C) One inverter  
 (D) Not possible

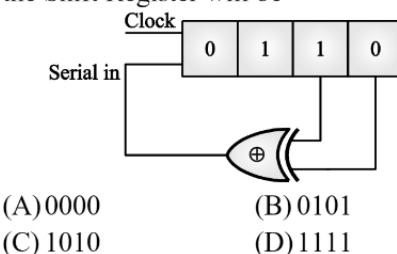


- Q.48** For one of the following conditions, clocked JK flip-flop can be used as divided by 2 circuit where the pulse train to be divided is applied at clock input :
- J = 1, K = 1 and the flip-flop should have active HIGH inputs.
  - J = 1, K = 1 and the flip-flop should have active LOW inputs.
  - J = 0, K = 0 and the flip-flop should have active HIGH inputs.
  - J = 1, K = 1 and the flip-flop should be a negative edge triggered one.

- Q.49** The mod number of a Johnson counter will be always equal to the number of flip flops used :
- Same
  - Twice
  - 2N where N is the number of flip flops.
  - None of the these

- Q.50** A 4-bit presentable UP counter has preset input 0101. The preset operation takes place as soon as the counter reaches 1111. The modulus of the counter is
- 5
  - 10
  - 11
  - 15

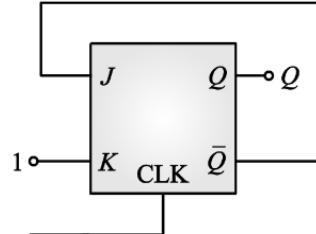
- Q.51** The initial contents of the 4-bit serial-in-parallel-out, right-shift, Shift Register shown in the figure is 0110. After three clock pulses are applied, the contents of the Shift Register will be



- Q.52** A pulse train with a frequency of 1 MHz is counted using a modulo-1024 ripple-

counter built with J-K flip flops. For proper operation of the counter, the maximum permissible propagation delay per flip flop stage is \_\_\_\_\_ nsec.

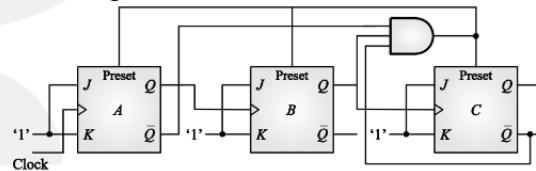
- Q.53** Consider the following J-K flip-flop



In the above J-K flip-flop,  $J = \bar{Q}$  and  $K = 1$ . Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the  $Q$  output?

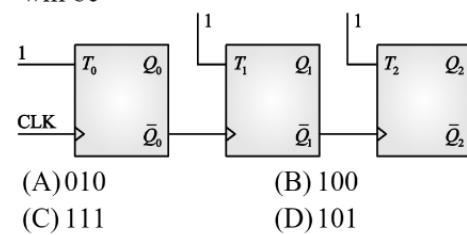
- 010000
- 011001
- 010010
- 010101

- Q.54** The ripple counter shown in the given figure is works as a



- MOD-3 up counter.
- MOD-5 up counter.
- MOD-3 down counter.
- MOD-5 down counter.

- Q.55** The given figure shows a ripple counter using positive edge triggered Flip-Flops. If the present state of the counter is  $Q_2Q_1Q_0 = 011$  then its next state  $Q_2Q_1Q_0$  will be

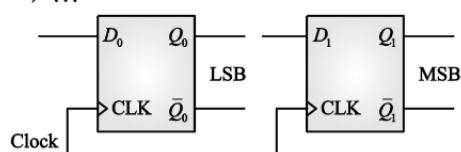


- 010
- 100
- 111
- 101





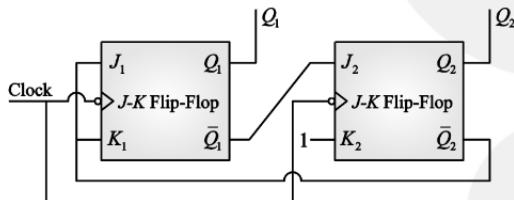
- Q.56** Two  $D$  flip-flops, as shown below, are to be connected as a synchronous counter that goes through the following  $Q_1 Q_0$  sequence  $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \rightarrow \dots$



The inputs  $D_0$  and  $D_1$  respectively should be connected as

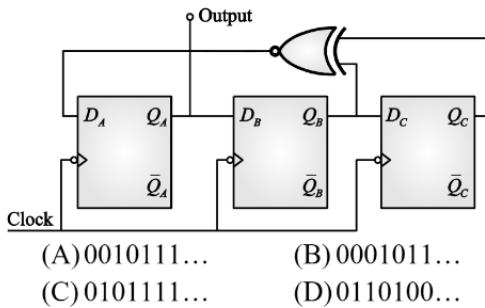
- (A)  $\bar{Q}_1$  and  $Q_0$
- (B)  $\bar{Q}_0$  and  $Q_1$
- (C)  $\bar{Q}_1 Q_0$  and  $\bar{Q}_1 Q_0$
- (D)  $\bar{Q}_1 \bar{Q}_0$  and  $Q_1 Q_0$

- Q.57** What are the counting state  $(Q_1, Q_2)$  for the counter shown in the figure below?



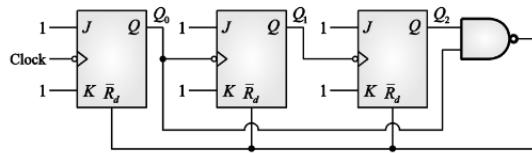
- (A) 11, 10, 00, 11, 10,...
- (B) 01, 10, 11, 00, 01,...
- (C) 00, 11, 01, 10, 00,...
- (D) 01, 10, 00, 01, 10,...

- Q.58** Assuming that all flip-flops are in reset condition initially, the count sequence observed at  $Q_A$  in the circuit shown is



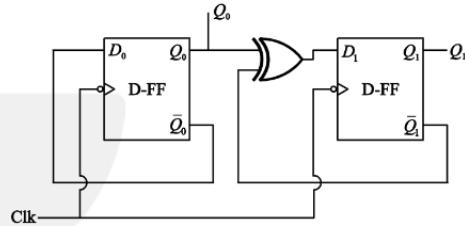
- (A) 00010111...
- (B) 0001011...
- (C) 0101111...
- (D) 0110100...

- Q.59** The circuit shown consists of  $J-K$  flip-flops, each with an active low asynchronous reset ( $\bar{R}_d$  input). The counter corresponding to this circuit is



- (A) a modulo-5 binary up counter.
- (B) a modulo-6 binary down counter.
- (C) a modulo-5 binary down counter.
- (D) a modulo-6 binary up counter.

- Q.60** Consider the following circuit :



Each state of output is designated as a two bit strings  $Q_0 Q_1$ . If the initial state of flip-flops is 00, then the state transition sequence is

- (A) 00  $\rightarrow$  10  $\rightarrow$  01  $\rightarrow$  11
- (B) 00  $\rightarrow$  11  $\rightarrow$  10  $\rightarrow$  01
- (C) 00  $\rightarrow$  11  $\rightarrow$  01  $\rightarrow$  10
- (D) 00  $\rightarrow$  11

- Q.61** Which of the following functions are self dual? [MSQ]

- (A)  $F(A, B, C) = \Sigma\{0, 2, 3\}$
- (B)  $F(A, B, C) = \Sigma\{0, 1, 6, 7\}$
- (C)  $F(A, B, C) = \Sigma\{0, 1, 2, 4\}$
- (D)  $F(A, B, C) = \Sigma\{3, 5, 6, 7\}$

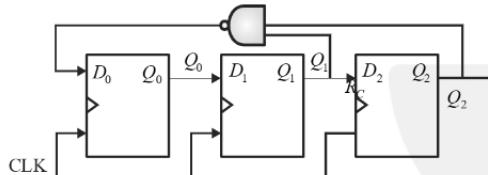


**Q.62** A is a 9 bit signed integer the 2's complement representation of A is  $(765)_8$  the 2's complement representation of  $6 \times A$  is?

- (A)  $(202)_8$       (B)  $(676)_8$   
 (C)  $(457)_8$       (D)  $(675)_8$

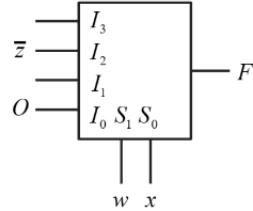
**Q.63** Consider the equation  $(57)_X = (Y7)_{10}$  where  $X \& Y$  are unknown then find the number of possible solution.

**Q.64** For the circuit shown in figure below what is the output  $Q_2 Q_1 Q_0$  as per four clock pulse. Initially all flip flop are reset.



- (A) 100      (B) 110  
 (C) 101      (D) 010

**Q.65** The 4 to 1 multiplexer shown below implements the Boolean expression



$$\text{If } F(w, x, y, z) = \sum m(4, 5, 7, 8, 10, 12, 15)$$

The input to  $I_1$  &  $I_3$  will be

- (A)  $yz, y' + z'$       (B)  $y + z', y \oplus z$   
 (C)  $y' + z, y \odot z$       (D)  $y' + z, y \oplus z$

### Answers      Digital Logic

1.	D	2.	B	3.	C	4.	B	5.	B
6.	3	7.	D	8.	C	9.	A	10.	D
11.	A	12.	D	13.	D	14.	2	15.	A
16.	D	17.	B	18.	B	19.	B	20.	C
21.	1	22.	B	23.	B, C	24.	B	25.	A
26.	C	27.	C	28.	C	29.	B	30	B
31.	D	32.	219	33.	B	34.	B	35.	B
36.	C	37.	A	38.	A	39.	D	40	B
41.	D	42.	C	43.	A	44.	A	45.	A
46.	B	47.	C	48.	D	49.	C	50.	B
51.	C	52.	100	53.	D	54.	D	55.	B
56.	A	57.	A	58.	D	59.	A	60.	C
61.	C,D	62.	B	63.	6	64.	B	65.	C

