OVERALL ANALYSIS | Solution Report

All | Correct Answers | Wrong Answers | Not Attempted Questions

Q.1) Max Marks: 1

Which of the following statements are false for horizontal microinstruction Encoding?

A. If there are k control signals, every control word stored in control memory (CM) consists of k bits, one bit for every control signal.

B. Parallel activation of several micro-operations in a single time step can be performed.

C. Parallel activation of several micro-operations in a single time step cannot be performed. — Correct Option

Solution: (C)
Answer: C
Explanation:
In horizontal microinstruction encoding, there is one separate bit for every control signal. Hence any number of control signals can be activated simultaneously.

D. None of the above

Q.2) Max Marks: 1

In the following pairs of addressing modes the first element refers to one having minimum operand fetching time and second one refers to the addressing mode with maximum operand fetching time. Pick Up the correct pair

A. Register direct and memory indirect

B. Immediate and indexed indirect — Correct Option

Solution: (B)
Answer: B
Explanation:
Immediate operand obviously needs minimum time while the indexed indirect mode results in maximum time because it involves the generation of indirect address by addition of operand field with the contents of index register.

C. Register direct and indexed

D. Immediate and Base-displacement

Q.3) Max Marks: 1

Consider a 16 bit processor in which the following one address instruction is loaded into main memory :

100	Opcode
101	300
102	Next instruction
	M
200	800

The effective address using PC-relative addressing mode when processor is executing an instruction at location 100 is _____ (Assume memory is of Byte addressable).

Correct Answer

Solution: (402)
Answer: 402
Explanation:
Effective address = PC+ Relative value
Program counter contains the address of the next instruction.
= 102+300 = 402

Q.4) Max Marks: 1

Assume that a 1G x 1 DRAM memory cell array is organized as 1M rows and 1K columns. The number of address bits required to select a row and a column will be:

A. 20 and 10 — Correct Option

Solution: (A)
Answer: A
Explanation:
Since there are 1M rows, the number of row address lines will be 20, as 2^{20} = 1M. Also, for selecting one of the 1K columns, the number of column address lines will be 10, as 2^{10} = 1K.

B 30 and 1

C 2^{20} and 2^{10}

D None of the above

Q.5) Max Marks: 1

In indirect index addressing mode using the index register having value X and address A, the effective operand address is

A (X+A)

B Content of the memory location addressed by (X+A) Correct Option

Solution: (B)
Answer: B
Explanation:
(X+A) provides the indirect address, with which the memory is accessed to get the address from where the operand data is accessed.

C X+content of memory location addressed by A

D A+ content of memory location addressed by X

Q.6) Max Marks: 1

Suppose an instruction set architecture of a general-purpose machine has a total of 126 control signals. The number of bits required in control word for horizontal and vertical microinstruction encoding are:

A 126, 7 Correct Option

Solution: (A)
Answer: A
Explanation:
For horizontal encoding, one bit is used for each control signal; therefore, we shall require 126 control signals.
For vertical encoding, the 126 control signals can be encoded in ceiling($\log_2$ 126) = 7 bits.

B 128, 7

C 7, 126

D 126, 8

Q.7) Max Marks: 1

A computer system supports one address and two address instructions and the word size is 16 bits. Main memory is 64 words. If there are 8 two address instructions than how many one address instructions are used?

A 64

B 128

C 256

D 512 Correct Option

Solution: (D)
Answer: D
Explanation:
Instruction length= 16 bits
Address size = 64 words = 6 bits
Number of two address instructions are possible

16 bits		
Opcode	Address 1	Address 2
4	6	6

2^4 = 16 two address instructions are possible.
But we have 8 two address instructions are there.
16-8 = 8*2^6 one address instructions are possible =2^9 = 512

Q.8) Max Marks: 1

Consider the instruction set architecture of a general-purpose machine. Suppose that a total of 20 control signals are present, out of which 7 are mutually exclusive while the rest are not. The number of bits required in the control word (for microprogramming) will be at least .....

Correct Answer

Solution: (16)

Answer: 16
Explanation:
The 7 mutually exclusive signals can be encoded in ceiling($\log_2$ 7) = 3 bits, while the remaining 13 signals will remain un-encoded. So the number of bits in a control word will be 3 + 13 = 16.

Q.9) Max Marks: 1

The ____ addressing mode is similar to register indirect addressing mode, except that an offset is added to the contents of the register. The offset and register are specified in the instruction.

A **Base indexed**

B **Base indexed plus displacement** Correct Option

Solution: (B)
Answer:B
Explanation:
Indirect addressing mode is similar to Base indexed plus displacement.

C **Indexed**

D **Displacement**

Q.10) Max Marks: 1

In _____ addressing mode, the operands are stored in the memory. The address of the corresponding memory location is given in a register which is specified in the instruction.

A **Register direct**

B **Register indirect** Correct Option

Solution: (B)
Answer: (B)
Explanation:
In register indirect addressing mode, the operands are stored in the memory. The address of the corresponding memory location is given in a register which is specified in the instruction.

C **Base indexed**

D **Displacement**

Q.11) Max Marks: 2

Consider a hypothetical CPU which supports 2 address, 1 address and 0 address instructions. A 16 bit instruction is placed in 128 word memory. If there exists 2 two address instructions and 100 one address instructions, then how many 0 address instructions can be designed?

Correct Answer

Solution: (19968)

Answer: 19968
Explanation:
Instruction size = 16 bits
Address size = 128 word =7 bits
Total Two address instruction = 16 - (7 + 7) bits = 2 bits = 4
But we use only 2 two address instructions.
Remaining 2 can be used for 1 address instruction and also 7 bits by reducing an address field.
Total 1 address instruction = 2 * 2^7 = 256
But we use 100 one address instructions.
Remaining 156 along with 7 bits by reducing an address field can be used for zero address instruction.
So Total zero address instruction = 156 * 2^7 = 19968

Q.12) Max Marks: 2

A m/c has 32 bit instruction and 10 bit address. There are two types of instructions exists in m/c. One address instruction and two address instruction . Suppose the max number of two address instructions are x and max number of one address instructions are y . Then x+y = ?

Correct Answer

Solution: (4198400)

Answer:
Explanation:

16 bits		
Opcode	Address 1	Address 2
12	10	10

Possible two address instructions are 2^{12} =4096
X=4096

16 bits	
Opcode	Address 1
22	10

Possible one address instructions are 2^{22} = 4194304
Y=4194304
X+Y = 4198400

Q.13) Max Marks: 2

The memory locations 2000, 2001 and 2020 have data values 18, 1 and 16 respectively before the following program is executed.

```
MOVI    Rs, 1           ; Move immediate
LOAD    Rd, 2000(Rs)    ; Load from memory
ADDI    Rd, 2000        ; Add immediate
STOREI  0(Rd), 20       ; Store immediate
```

Which of the statements below is TRUE after the program is executed ?

A **Memory location 2000 has value 20**

B **Memory location 2020 has value 20**

C **Memory location 2021 has value 20**

D **Memory location 2001 has value 20** Correct Option

Solution: (D)

Answer: (D)
Explanation:
Rs<-1
Rd<-1
Rd<-2001
store in address 2001 <- 20

Q.14) Max Marks: 2

A RAM chip has a capacity of 1024 words of 8 bits each. The number of 2-to-4 decoders with enable lines needed to construct a 16K x 16 RAM system will be .....

Correct Answer

Solution: (5)
Answer:5
Explanation:
To construct a memory system with 16K words using 1024x8 RAM chips, we have to connect 16 such chips in parallel. The decoder will have to select one of the 16 chips. To construct a 4x16 decoder, we require 5 2x4 Decoders.

Q.15) Max Marks: 2

Consider a hypothetical control unit that supports 5 groups of mutually exclusive control signals. Also assume that group 1 & group 2 are using horizontal micro-programming whereas group-3, 4 and 5 are using vertical micro-programming. The total number of bits used for control words are _____.

Groups	G_1	G_2	G_3	G_4	G_5
Control signals	43	29	76	130	100

Correct Answer

Solution: (94)

Answer: 94

Explanation:

Groups	G_1	G_2	G_3	G_4	G_5
Control signals	43	29	76	130	100

Group1 and Group 2 are using the horizontal micro-programming.
Number of bits are 43+29 =72
Remaining are supporting/using Vertical micro-programming
76 signals are in Group 3. Number of bits are used to represent signals are 7
130 signals are in Group 4. Number of bits are used to represent 130 signals are 8
100 signals are in Group 5. Number of bits are used to represent 100 signals are 7
Total number of bits for vertical microprogramming is 22bits.
Number of bits in a control word is = 72+22 =94

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