Provide a brief description of your proposed practicum project:

The practicum research will extend the performance portability backend Legion - developed by LANL, Nvidia, SLAC, and Stanford. There are multiple front-ends for Legion: CuNumeric, FleSCI, Legion C++, Regent, and others. In addition, numerous applications from the high performance computing (HPC) domain have been ported to Legion. The project is open source and freely available. Currently, Legion does not make any automatic decisions regarding the mapping of applications onto target hardware*. Many applications of interest to LANL and other laboratories are memory bound. This memory bottleneck is caused by unstructured data accesses and small number of instructions per data fetch. One could say that this simply argues for mapping all their kernels on a distributed GPU cluster due to the GPU's high bandwidth and throughput available. However, the emergence of a new architectural paradigm, Processing In Memory, competes directly with the GPU. This presents an interesting new target architecture for LANL and other labs, and also produces a novel mapping problem for Legion.

Processing in Memory (PIM) involves integrating computational elements into DRAM memory modules significantly reducing data movement overhead. One goal of my practicum is to determine if this paradigm shift in computer architecture can substantially enhance the performance of HPC workloads. I believe I can address this question through supporting PIM architectures through the Legion backend. A machine model contains required information to make an informative mapping decision for an application. I will explore the machine model within Realm, the backend runtime for Legion, to see if PIMs can be adequately represented.

Once a PIM target is generated with the Legion backend, my evaluation of the new paradigm can begin. The end goal is to assess the performance, energy efficiency, and scalability benefits of leveraging PIM technology for a wide range of small scale applications. We will profile a representative set of applications to identify the specific computational and memory access patterns. The results of this analysis will feed into the mapping problem. The ability to characterize HPC kernels that are performant on PIM is a next step in the automatic mapping problem.

In short, I anticipate three main contributions:
1) Adding a PIM hardware target to the Legion backend. 2) Characterizing types of HPC workloads that are performant on PIM by using existing ported Legion applications. 3) Taking the first step towards the automatic mapping problem with PIM targets included.

* This is referred to as the mapping problem.

How will your practicum research broaden your perspective beyond your thesis research?

The practicum broadens my perspective beyond my thesis. My current research focuses within the database domain, and considers finding the optimal mapping of high level language programs, e.g. SQL queries, to various architectures. I have extensively focused on UPMEM PIM; this is the first publicly available state of the art general purpose PIM architecture. I am currently examining different transactional and analytical database workloads on UPMEM PIM. However, architecture organization can influence the data structure(s) and algorithms used within the operators. This results in unique memory layouts and communication patterns that generate additional complexity in creating a communication schedule across devices.

The approach of using a performance portability layer, Legion, as a backend to codegen PIM instructions and provide data structure management based on a machine model is novel. This will allow for applications that utilize Legion to support a new architecture paradigm. The workloads will be evaluated to characterize performant PIM kernels. My thesis work focuses on the optimal layout for specific data structures and communication patterns for common database workloads on a given architecture. The practicum work will explore Legion's backend to generate automatic data structure layout and communication pattern schedule with a system containing PIM. Also, this will be a next step towards an automatic schedule mapper for Legion, namely allowing for an application to be mapped and scheduled on various heterogeneous components of hardware concurrently.

Since Legion has been an ongoing project at multiple institutions, it has accumulated many HPC use cases. This allows for exposure to real HPC workloads by showcasing how domain scientists use Legion for their applications.

List computational resources required for practicum project, if any:

In order to make the project feasible, access to state-of-the-art PIM technology will be needed. UPMEM, SAMSUNG and SK-HYNIX are the solutions that we are considering. Currently, we have access to UPMEM. We are working to gain access to SAMSUNG and SK-HYNIX. The best solution changes depending on the type of computation within the program. The evaluation across multiple PIM solutions will allow for a greater understanding of the role PIM within HPC.

Are you planning on utilizing any of the HPC resources at the lab?

This project mainly plans on using single/small node testbed systems on the Darwin cluster. After gaining access to the computational resources (as described in the previous statement), we can add small-scale testbed nodes to Darwin with PIM. This node(s) would consist of a CPU, GPU, and PIM.

In addition to the classic CPU and GPU node setup, other memory layouts should be considered. LANL is obtaining a cluster with the Nvidia Grace Hopper architecture named Venado. This architecture has a unique unified memory layout between the CPU and GPU. It would be interesting to see how the addition of PIM would influence the application mapping on this unified architecture.