February 1, 2001

AGB Programming Manual

Version 1.01

Game Boy Advanced (AGB) stresses portability and focuses on 2D rather than 3D image processing functions, resulting in a cutting-edge portable game device with revolutionary capabilities.

It provides window-like functions, rotation, scaling, α blending, and fade-in/fade-out features that can be combined to produce exactly the image representations desired.

Additionally, the bitmap image-rendering function, with its two modes (double buffering mode for rewriting full-screen images in real time and single buffering mode for stills), can be used to handle realistic images that are indistinguishable from actual photographs.

The 2.9-inch-wide reflective TFT color LCD screen provides a clear display with little afterimage.

In addition to Game Boy Color compatible sound, AGB has a PCM stereo sound generator. Multiple tracks can be played simultaneously by overlapping them using the CPU. L and R buttons have been added to the Controller. The broader range of control provided also expands the breadth of game designs possible.

Although AGB uses a 32-bit RISC CPU whose computing performance and data processing capabilities far surpass those of Game Boy Color, it consumes little power, allowing approximately 15 hours of continuous play. This is made possible by the inclusion of the various types of RAM on a single custom chip.

Furthermore, software for AGB can be developed using the C language, minimizing the cost of development equipment. This favorable development environment and the high level of freedom of the system configuration allow one to build a profound world of play in which anyone can become absorbed.

With its extremely high-performance computational and data processing capabilities as a foundation, AGB provides greater image and sound representation capabilities, making the pursuit of fun its essential aim.

The purpose of this high level of performance is to bring unique game ideas fully to life.

AGB is an innovation born from experience. While providing backwards compatibility with the enormous software resources available for the 100 million Game Boy units in use worldwide, it also breaks new ground for portable game devices.

Revision History

Version	Date	Description
0.3.6.2	12/21/1999	-Minor modification. (Numbering for items: P81,P82,P149), (Reference to chapter removed) -Deleted 14.3
0.3.6.3	01/05/2000	-Minor modification. -Corrected BG Offset Registers diagrams -Corrected the diagrams of Registers for Setting the Direction Parameters of BG data. -Corrected diagram of the Sound 1 Duty Cycle. -Corrected the name of d05 bit for the DISPCNT Register. -Added the description of Bit map BG mode. -Corrected the SIO Timing Chart of Normal Serial Communication. -Changed the diagrams and descriptions of the Sound Control Registers. -Added the formula for calculating the number of OBJs that can be displayed on 1 line.
0.4.0	01/25/2000	-Changed specifications. *Changed CPU internal working RAM memory capacity, and created CPU external working RAM. *Changed the bit structures of DMA control registers. *Deleted Infrared Communication functions. *Created the interrupt IME register, and changed the bit structures of IE and IF registers. *Changed the number of colors that can be displayed to 32,768. *Changed the specifications of Normal Serial Communication (Bit width, communication speed) *Changed the specifications of Multi SIO Communication (UART system). *Changed the center coordinate of OBJ Rotation to dot boundary. *Added UART system communication function.
	02/09/2000	-Added the Complete Block Diagram.
0.4.1	02/22/2000	-Modified the description of Direct Sounds, and corrected register R bit structure.
	02/24/2000	-Added the PWM sampling cycle control function.
	02/25/2000	-Changed the method to specify OBJ size. -Corrected misprints in the communication control register.
0.4.1.1	03/08/2000	-Added the description of ROM registration data.
	03/10/2000	-Improved the description of interrupt and multiple interrupt process.
	03/10/2000	-Improved the description of system call and multiple system call process.
0.4.1.2	04/06/2000	-Added the description of UART system communication.

Version	Date	Description
0.4.1.3	05/08/2000	-Corrected [Sound 1 Usage Notes]. -In 1) Normal Communication of Communication Functions, mentioned not to use a cable.
	05/16/2000	-Added the diagram of Multi Player Communication Cable connection.
	05/25/2000	-Changed the diagram in System-Allocated Area in Working RAM, and deleted "(Tentative)". -Revised ROM registration data. -Corrected the description of internal shift clock of normal SIO control register. -Newly added the description of "Communication Cable" in the chapter of Communication Functions. -Corrected Overview of Screen Sizes for Text BG Screens in "Rendering Functions".
0.4.1.4	05/29/2000	-Added the description for the device type of ROM Registration Data. -Corrected "Fault Function" to "Halt Function." -Corrected the diagram of "Communication Cable."
0.4.1.5	06/01/2000	-Corrected the attributes of timer setting values register from W to R/W. -Added one sentence to 1) of 15.2.1. Normal Interrupt and 15.2.2. Multiple Interrupts respectively. -Emphasized the prohibition of use of cable for normal SIO communication.
0.4.1.6	06/26/2000	-Modified the connection diagram of the multi-play cable. -Added the transition diagram of the multi-play communication data. -Modified the description of "16-Bit Multi-play Communication".
0.4.1.7	08/10/2000	-Modified the description of an error flag for the multi=play control register. -Modified the description of a valid flag for all the DMA control registers. -Added the number of transfer when 0 is set for the DMA word count register.
0.4.1.8	10/16/2000	-Added cautions to the priority setting of OBJ. -Added a description and cautions to Sound 1,2,3, and 4. -Added the description to "Mapping of character data". -Revised the description in SCCNT_L[d14] and [06] of UART communication register. -Revised the connection diagram of 16 bit multi-play communication. -Added a description to all sound operation modes of the sound control register. -Revised the itemized description of Chapter 10 "Sound".

Version	Date	Description
1.0	12/01/2000	-Deleted the checksum of ROM registration data and revised the diagram. -Revised the diagram for "Communication Cable" in the "Communication Function". -Revised the number of DMG sold from tens of millions to a hundred million in the introduction of AGB. -Revised the hours you can play continuously from "about 20 hours" to "about 15 hours". -Revised the illustrations of the AGB hardware and the Multi Player Communication Cable in the multi play communication diagram. -Added the description of the timing chart for normal SIO communication. -Added a caution in the DMA valid flag of all the DMA control registers. -Added a caution in the master start bit of the multi-play control register. -Revised the multi-play timing chart. -Revised the memory map for system reserve area in the work RAM. -Added a caution to "Communication Function". -Revised the first sentence in "UART Communication". Added "Relation between Data register, FIFO and Shift register". -Revised the expression of [Cautions] to a more specific expression [Cautions for ~~]. -Added a description of X coordinate and Y coordinate for OAM. Added the diagram to Y coordinate. -Revised the description of the pre-fetch buffer flag in the Game Pak memory wait control register. -Added cautions to the description of the input/output select flag in the R register of general communication.
1.01	2/01/2001	-Modified the description of pin 31 in the Game Pak bus. -Revised the cancel conditions for the Stop function in the power-down mode. -Added additional descriptions and cautions for the initial flag of Sound 1.

Table of Contents

Using This Manual

Important terms and symbols used in this manual are defined below.

1. Terms

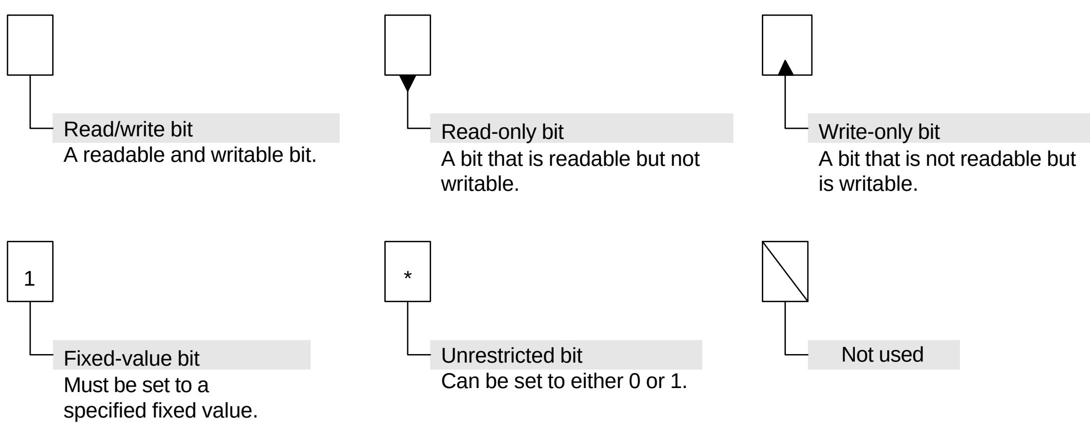
The term “user” in this manual refers to the software developer, not to the general consumer.

Bit lengths in this manual are expressed as follows.

Bit Length	Term Used
8 bits	byte
16 bits	half-word
32 bits	word

2. Symbols

The attributes of bits used in bit operations are represented as follows.



3. Abbreviations

The following abbreviations are used to denote Nintendo handheld systems.

- DMG (Game Boy)
- CGB (Game Boy Color)
- AGB (Game Boy Advance)

1 AGB System

1.1 System Overview

AGB is a portable game device that maintains downward compatibility with Game Boy Color (CGB) and provides higher performance.

AGB's 2.9-inch-wide reflective TFT color LCD and 32-bit RISC CPU enable production of games that match or surpass the Super Nintendo Entertainment System (Super NES) in performance.

AGB CPU

32-bit RISC CPU (ARM7TDMI)/16.78 MHz

Downward Compatibility with CGB

Integral 8-bit CISC CPU for compatibility
(However, it cannot operate at the same time as the AGB CPU.)

Memory

System ROM	16 Kbytes (and 2 Kbytes for CGB System ROM)
Working RAM	32 Kbytes + CPU External 256 Kbytes (2 wait)
VRAM	96 Kbytes
OAM	64 bits x 128
Palette RAM	16 bits x 512 (256 colors for OBJ ; 256 colors for BG)
Game Pak memory	Up to 32 MB: mask ROM or flash memory + Up to 512 Kbits: SRAM or flash memory

Display

240 x 160 x RGB dots
32,768 colors simultaneously displayable
Special effects features (rotation/scaling, α blending, fade-in/fade-out, and mosaic)
4 image system modes

Operation

Operating keys (A, B, L, R, START, SELECT, and Control Pad)

Sound

4 sounds (corresponding to CGB sounds) + 2 CPU direct sounds (PCM format)

Communication

Serial communication (8 bit/32 bit, UART, Multi-player, General-purpose, JOY Bus)

Game Pak

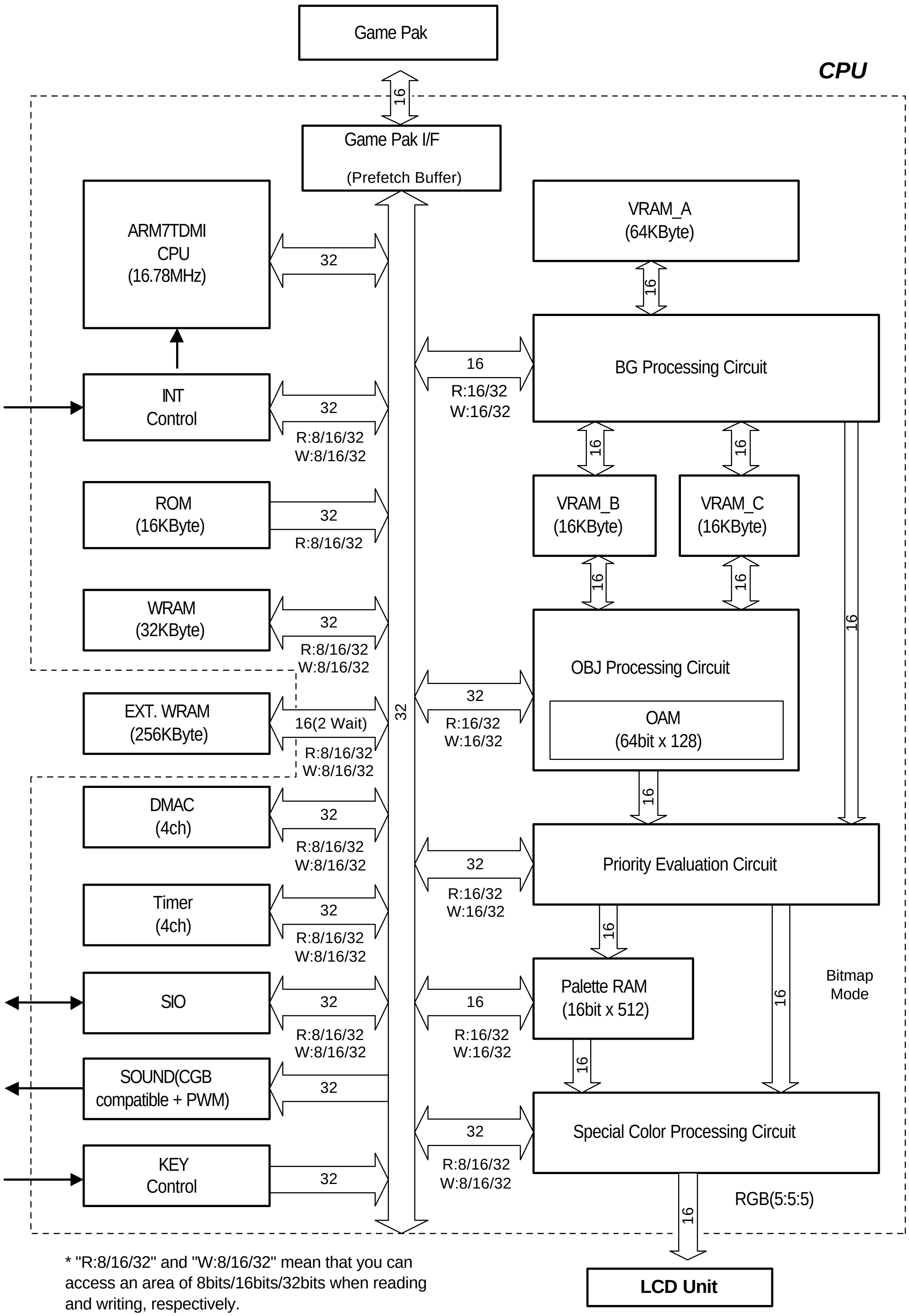
Like DMG and CGB, AGB is equipped with a 32-pin connector for Game Pak connection. When a Game Pak is inserted, AGB automatically detects its type and switches to either CGB or AGB mode.

The following Game Paks operate on the AGB system.

1. DMG Game Paks, DMG/CGB dual mode Game Paks, and CGB dedicated Game Paks
2. AGB dedicated Game Paks(Game Paks that only function with AGB)

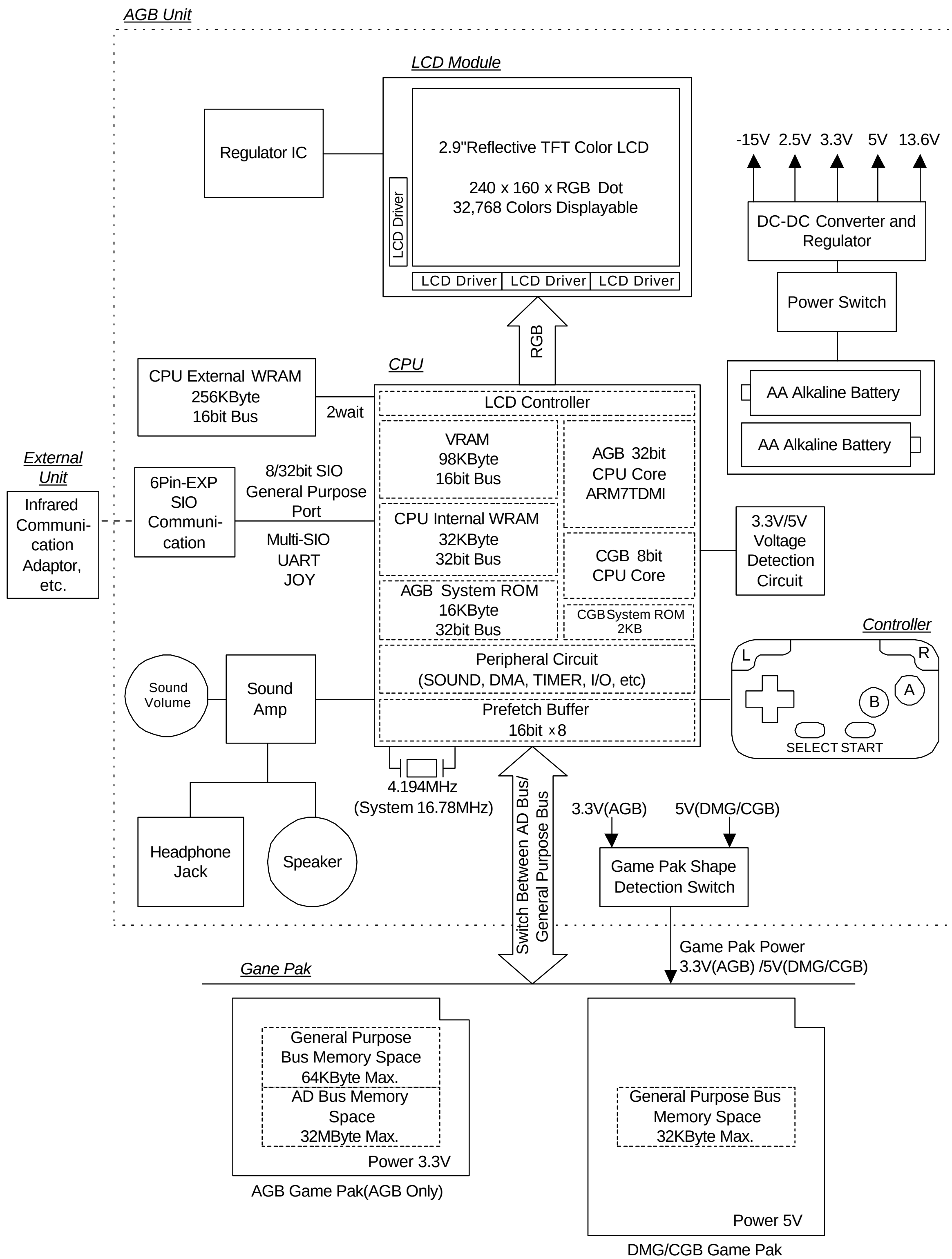
2 System Configuration

2.1 CPU Block Diagram



* "R:8/16/32" and "W:8/16/32" mean that you can access an area of 8bits/16bits/32bits when reading and writing, respectively.

2.2 Complete Block Diagram



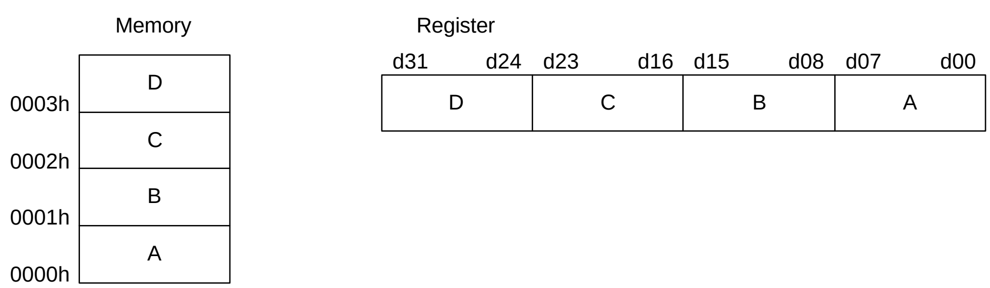
2.3 Memory Configuration and Access Width

Memory Type	Bus Width	DMA		CPU	
		Read Width	Write Width	Read Width	Write Width
OAM	32	16/32	16/32	16/32	16/32
Palette RAM	16	16/32	16/32	16/32	16/32
VRAM	16	16/32	16/32	16/32	16/32
CPU Internal Working RAM	32	16/32	16/32	8/16/32	8/16/32
CPU External Working RAM	16	16/32	16/32	8/16/32	8/16/32
Internal registers	32	16/32	16/32	8/16/32	8/16/32
Game Pak ROM (Mask ROM, Flash Memory)	16	16/32	16/32	8/16/32	16/32
Game Pak RAM (SRAM, Flash Memory)	8	--	--	8	8

Good execution efficiency is obtained when programs that operate from the Game Pak use 16-bit instructions (16-bit compiler), and those that operate from CPU Internal Working RAM use 32-bit instructions (32-bit compiler).

2.4 Little-Endian

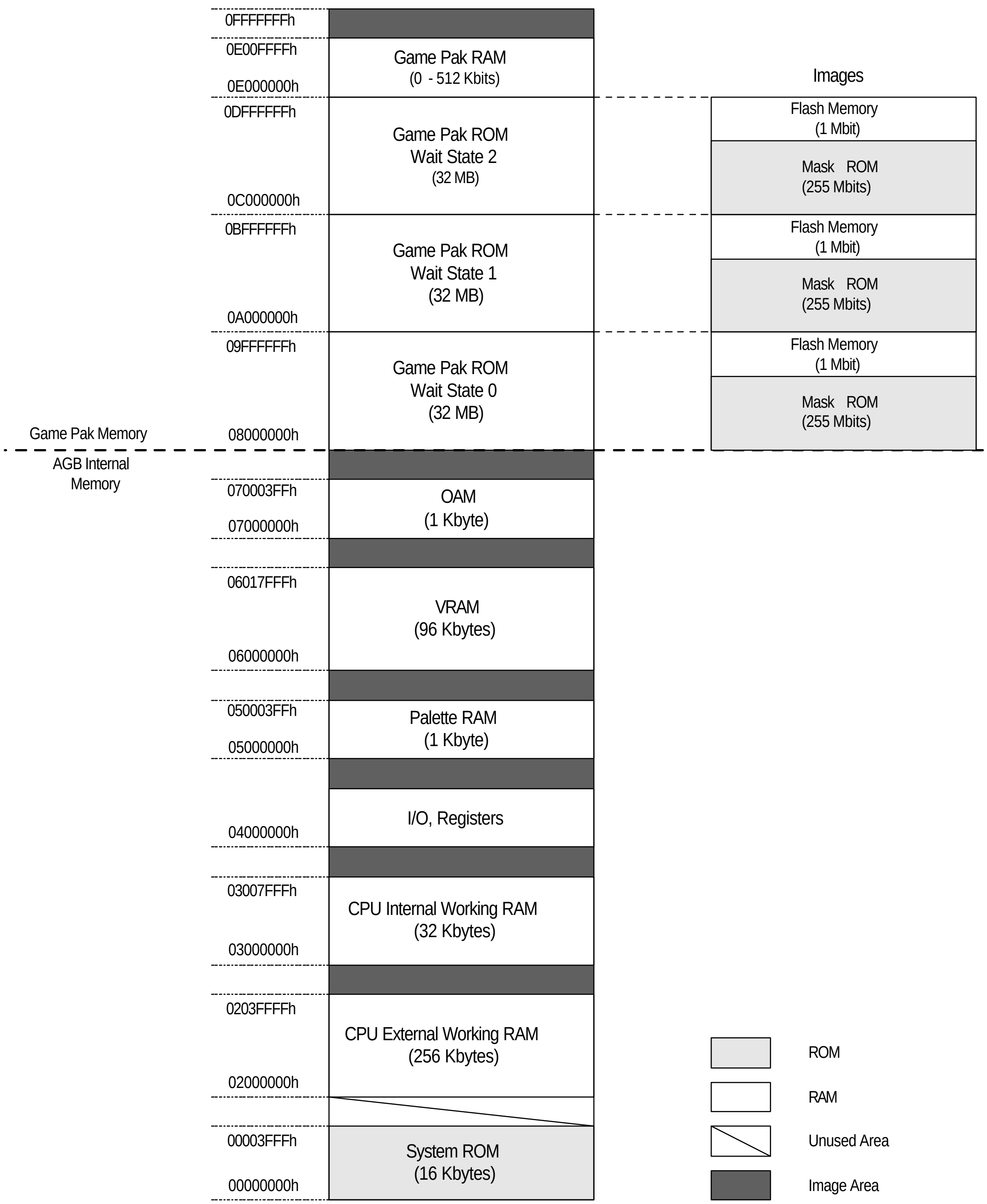
In the AGB CPU, memory addresses are allocated in 8-bit increments, and little-endian format is used in implementing the 8-, 16-, and 32-bit access widths.



3 AGB Memory

3.1 Overall Memory Map

The following is the overall memory map of the AGB system.



3.2 Memory Configuration

In broad terms, the area 00000000h-07FFFFFFh is allocated as AGB internal memory, and 08000000-0EFFFFFFh is allocated as Game Pak memory.

3.2.1 AGB Internal Memory

1) System ROM

The 16 KBytes from 000000000h is the system ROM.

Various types of System Calls can be used.

2) CPU External Working RAM

The 256 Kbytes from 02000000h is CPU External Working RAM. Its specifications are 2 Wait 16 bit Bus.

3) CPU Internal Working RAM

The 32 Kbytes from 03000000h is CPU Internal Working RAM. It is used to store programs and data.

4) I/O and Registers

This area is used for various registers.

5) Palette RAM

The 1 Kbyte from 05000000h is palette RAM. It is used to assign palette colors.

6) VRAM

The 96 Kbytes from 06000000h is the VRAM area. This area is for BG and OBJ data.

7) OAM

The 1 Kbyte from 07000000h is Object Attribute Memory (OAM). It holds the objects to be displayed and their attributes.

3.2.2 Game Pak Memory

1) Game Pak ROM

Three 32 MB Game Pak ROM spaces are allocated to the area beginning from 08000000h.

The access speed of each of these spaces can be set individually. Thus, they are named Wait State 0, Wait State 1, and Wait State 2.

This specification enables memory of varying access speeds in Game Pak ROM to be accessed optimally.

The base addresses of the 3 spaces are 08000000h for Wait State 0, 0A000000h for Wait State 1, and 0C000000h for Wait State 2.

In addition, the upper 1 Mbit of each space is allocated as flash memory.

This area is used primarily for saving data.

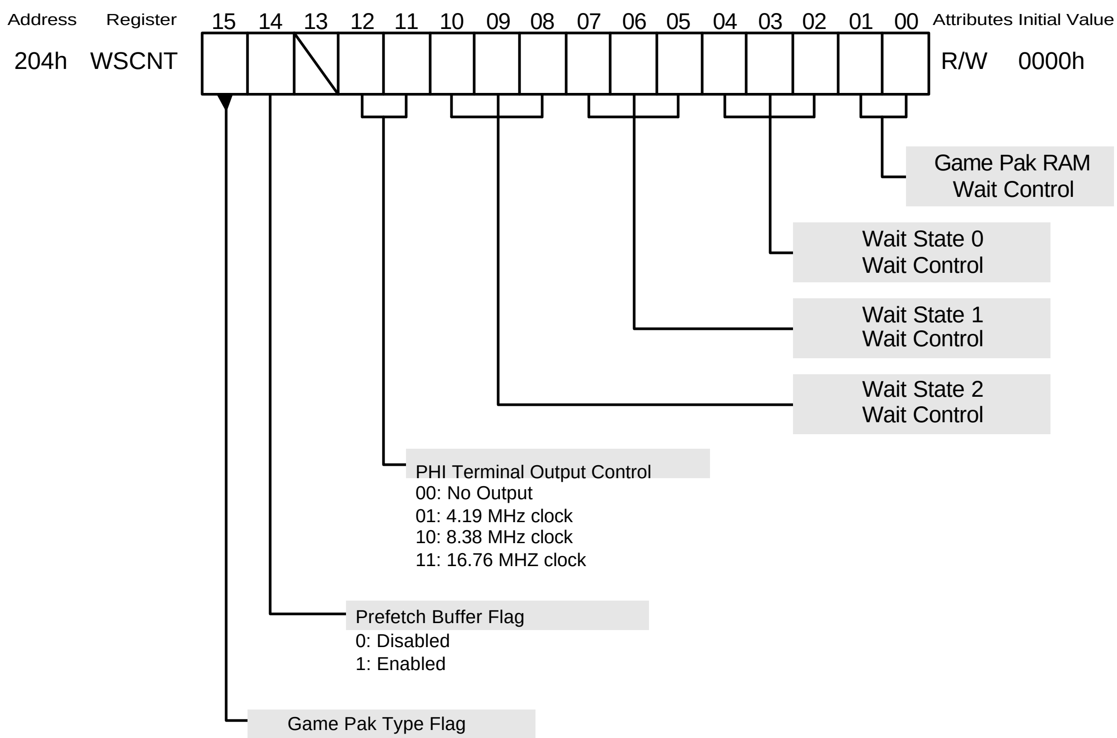
2) Game Pak RAM

The area beginning from 0E000000h is the Game Pak RAM area. Up to 512 Kbits of SRAM or Flash Memory can be stored here. However, it is an 8 bit data bus. Due to the specifications, any Game Pak device other than ROM must be accessed using Nintendo's library.

3.3 Game Pak Memory Wait Control

Although the 32 MB Game Pak memory space is mapped to the area from 08000000h onward, the 32 MB spaces beginning from 0A000000h and 0C000000h are images of the 32 MB space that starts at 08000000h.

These images enable memory to be used according to the access speed of the Game Pak memory (1-4 wait cycles).



WSCNT [d15] Game Pak Type Flag

The System ROM uses this.

WSCNT [d14] Prefetch Buffer Flag

When the Prefetch Buffer Flag is enabled and there is some free space, the Prefetch Buffer takes control of the Game Pak Bus during the time when the CPU is not using it, and reads Game Pak ROM data repeatedly. When the CPU tries to read instructions from the Game Pak and if it hits the Prefetch Buffer, the fetch is completed with no wait in respect to the CPU. If there is no hit, the fetch is done from the Game Pak ROM and there is a wait based on the set wait state.

If the Prefetch Buffer Flag is disabled, the fetch is done from the Game Pak ROM. There is a wait based on the wait state associated with the fetch instruction to the Game Pak ROM in respect to the CPU.

WSCNT [d12-11] PHI Terminal Output Control

Controls the output from the PHI terminal. This should always be set to 00(No Output).

WSCNT [d10-08],[d07-05],[d04-02] Wait State Wait Control

Individual wait cycles for each of the three areas(Wait States 0-2) that occur in Game Pak ROM can be set. The relation between the wait control settings and wait cycles is as follows. Use the appropriate settings for the device you are using.

Wait Control Value	Wait Cycles			
	1st Access	2nd Access		
		Wait State 0	Wait State 1	Wait State 2
000	4	2	4	8
001	3	2	4	8
010	2	2	4	8
011	8	2	4	8
100	4	1	1	1
101	3	1	1	1
110	2	1	1	1
111	8	1	1	1

After executing the System ROM (when the User Program is started) the Wait Control Value is 000. In the Game Pak Mask ROM used with the actual manufactured product, the specifications are 1st Access/3 Wait, 2nd Access/1 Wait. In this case, set the Wait Control Value to 101.

WSCNT [d01-00] Game Pak RAM Wait Control

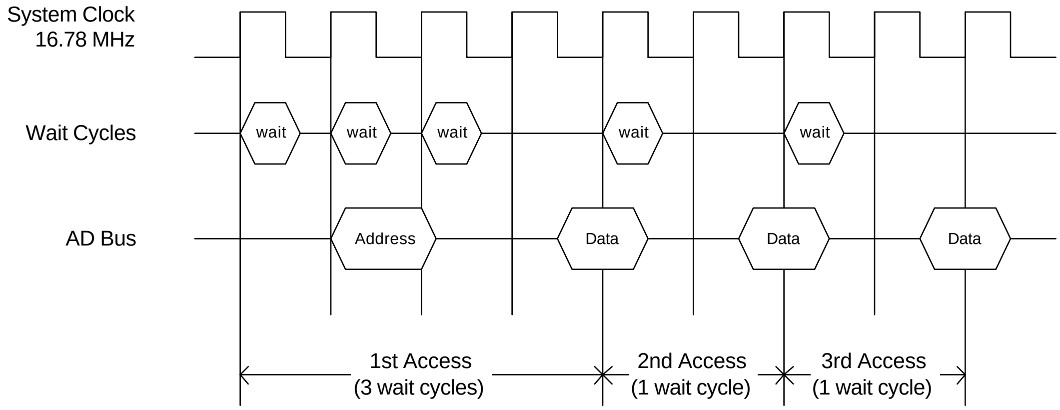
Wait cycles for the Game Pak RAM can be set. The relation between the wait control settings and wait cycles is as follows. Use the appropriate settings for the device you are using.

Wait Control Value	Wait Cycles
00	4
01	3
10	2
11	8

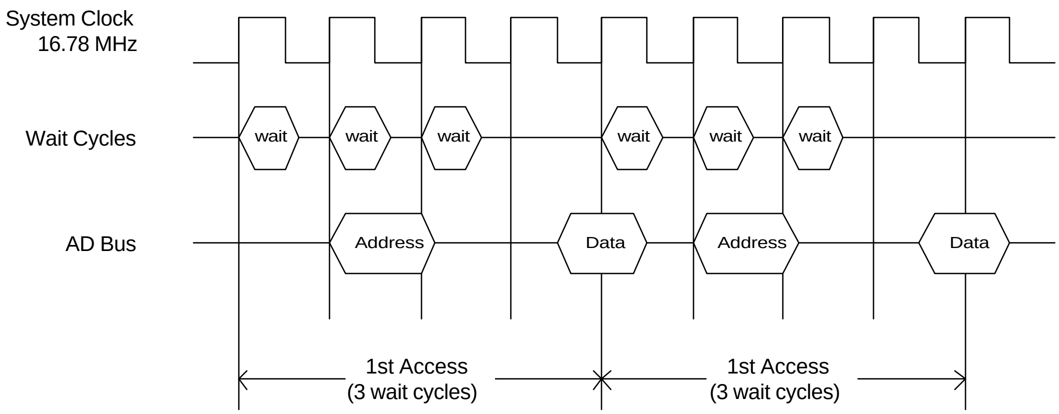
3.3.1 Access Timing

The following timing charts illustrate Game Pak ROM access with 3 wait cycles on the first access and 1 wait cycle on the second.

1) Sequential Access



2) Random Access



3.3.2 Game Pak Bus

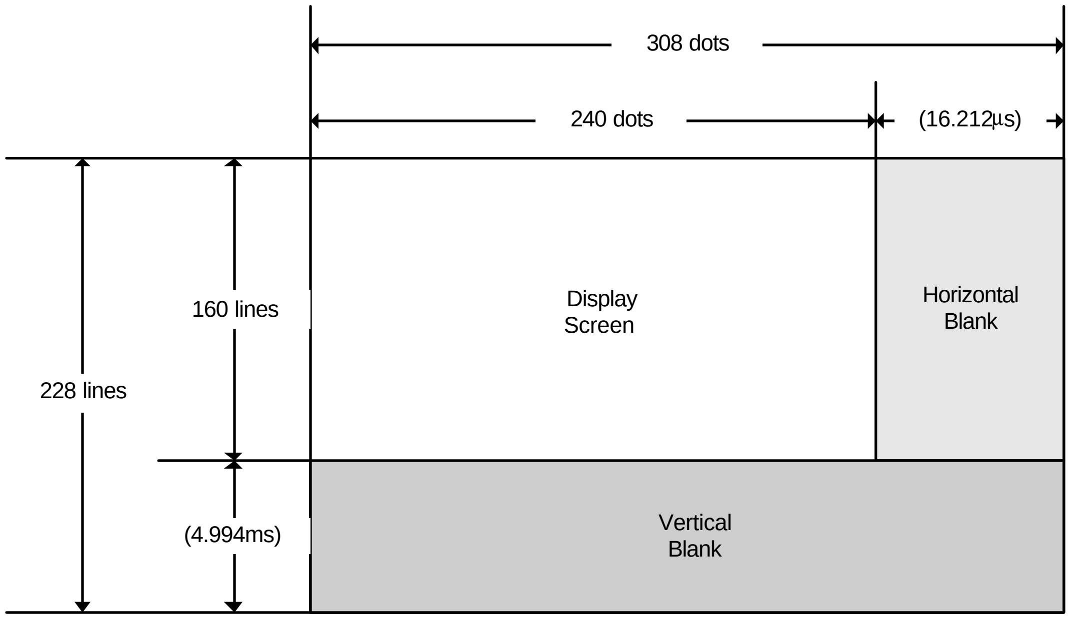
The Game Pak bus has a total of 32 terminals, which are described in the following table.

No.	Game Pak ROM Access		Game Pak RAM Access	
	Terminal	Use	Terminal	Use
1	VDD(3.3V)		VDD(3.3V)	
2	PHI		PHI	
3	/WR	Write Flag	/WR	Write Flag
4	/RD	Read Flag	/RD	Read Flag
5	/CS	ROM Chip Selection	/CS	
6	AD0	Terminals used for both address(lower) and data	A0	Address
7	AD1		A1	
8	AD2		A2	
9	AD3		A3	
10	AD4		A4	
11	AD5		A5	
12	AD6		A6	
13	AD7		A7	
14	AD8		A8	
15	AD9		A9	
16	AD10		A10	
17	AD11		A11	
18	AD12		A12	
19	AD13		A13	
20	AD14		A14	
21	AD15		A15	
22	A16	Address(upper)	D0	Data
23	A17		D1	
24	A18		D2	
25	A19		D3	
26	A20		D4	
27	A21		D5	
28	A22		D6	
29	A23		D7	
30	/CS2		/CS2	RAM Chip Selection
31	IREQ and DREQ	Terminal used for IREQ and DREQ	IREQ and DREQ	Terminal used for IREQ and DREQ
32	GND		GND	

4 LCD

AGB uses a 2.9-inch-wide reflective TFT color LCD screen.

The vertical blanking interval of AGB is longer than that of DMG and CGB, and its horizontal blanking interval is fixed.

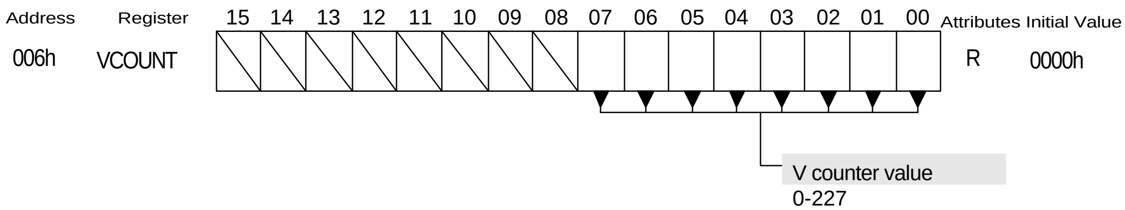


Item		Value	Interval
Display screen size	Number of dots per horizontal line	240 dots	57.221 µs
	Number of horizontal lines	160 lines	11.749 ms
Total number of dots	Number of dots per horizontal line	308 dots	73.433 µs
	Number of horizontal lines	228 lines	16.743 ms
Blanking	Number of dots per horizontal blank	68 dots	16.212 µs
	Number of horizontal lines per vertical blank	68 lines	4.994 ms
Scanning cycle	H interval frequency	13.618 KHz	73.433 µs
	V interval frequency	59.727 Hz	16.743 ms

4.1 LCD Status

4.1.1 V Counter

The VCOUNT register can be used to read which of the total of 228 LCD lines (see previous figure) is currently being rendered.



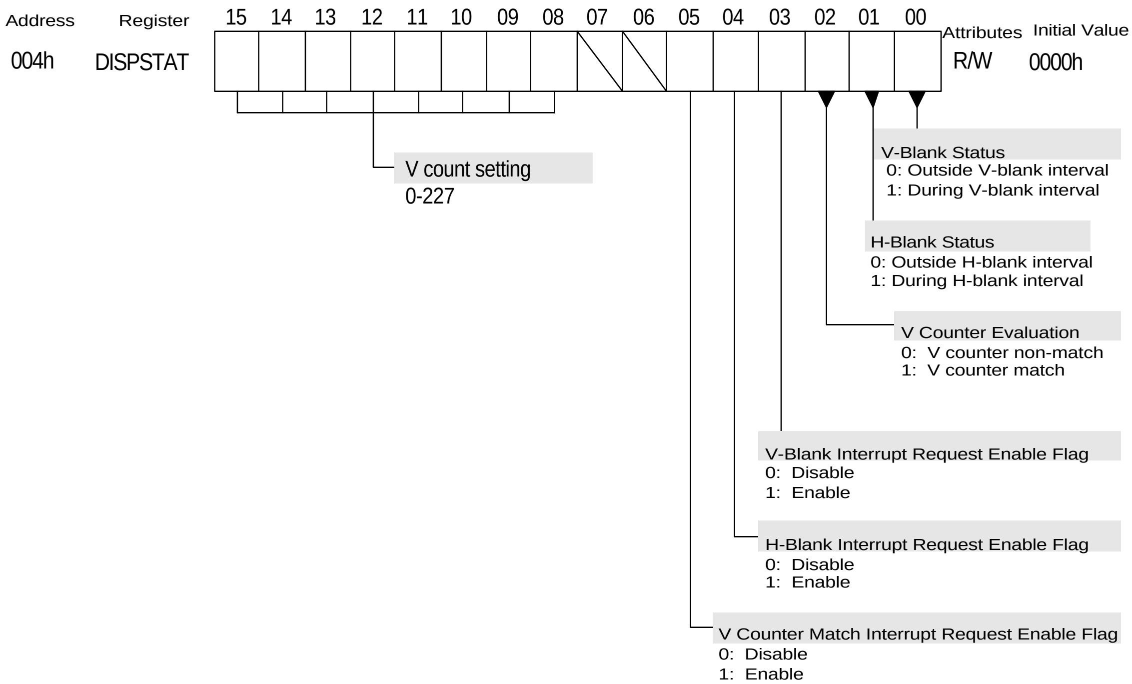
A value of 0-227 is read.

A value of 0-159 indicates that rendering is in progress; a value of 160-227 indicates a vertical blanking interval.

4.1.2 General LCD Status

General LCD status information can be read from bits 0-5 of the DISPSTAT register.

In addition, 3 types of interrupt requests can be generated by the LCD controller.



DISPSTAT [d15-08] V Count Setting

Can be used to set the value used for V counter evaluation and V counter match interrupts. The range for this setting is 0-227.

DISPSTAT [d05] V Counter Match Interrupt Request Enable Flag

Allows an interrupt request to be generated when the value of the V counter setting and the value of the line actually rendered (VCOUNT register value) agree.

DISPSTAT [d04] H-Blank Interrupt Request Enable Flag

Allows an interrupt request to be generated during horizontal blanking.

DISPSTAT [d03] V-Blank Interrupt Request Enable Flag

Allows an interrupt request to be generated during vertical blanking.

DISPSTAT [d02] V Counter Evaluation

Flag indicating whether the V count setting and the V count register value match. It is set while they match and automatically reset when they no longer match.

DISPSTAT [d01] H-Blank Status

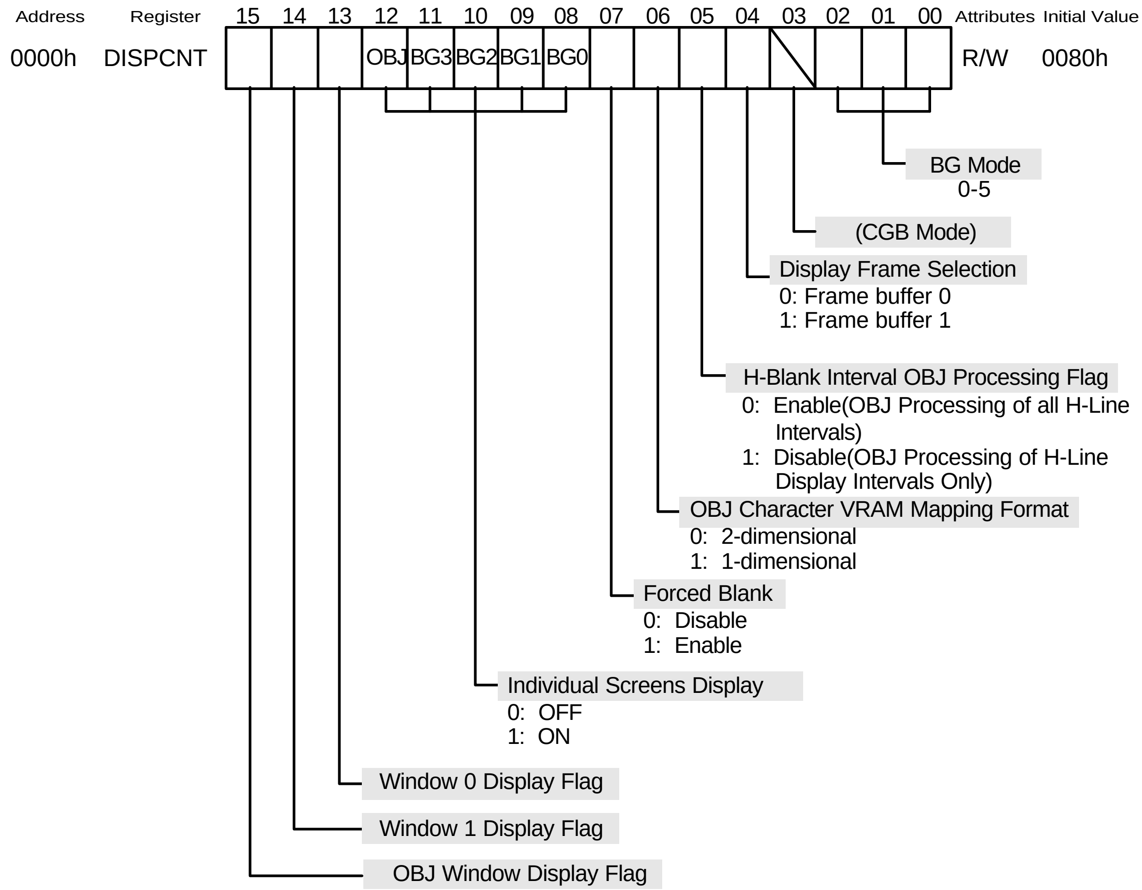
Can check whether a horizontal blanking interval is currently in effect.

DISPSTAT [d00] V-Blank Status

Can check whether a vertical blanking interval is currently in effect.

5 Image System

AGB can use different image systems depending on the purpose of the software.
These display-related items are changed mainly using the DISPCNT register.



DISPCNT [d15] OBJ Window Display Flag

Master flag that controls whether the OBJ window is displayed.

For information on the OBJ window, see section “6.3, OBJ (Object)”.

DISPCNT [d14][d13] Display Flags for Windows 0 and 1

Master flag that controls whether windows 0 and 1 are displayed.

For information on windows, see “Chapter 8, Window Feature”.

DISPCNT [d12-08] Individual Screens Display Flag

Allows individual control of whether BG0, BG1, BG2, BG3, and OBJ, respectively, are displayed.

DISPCNT [d07] Forced Blank

Setting this bit causes the CPU to forcibly halt operation of the image processing circuit, allowing access to VRAM, color palette RAM, OAM, and the internal registers. The LCD screen displays white during a forced blank. However, the internal HV synchronous counter continues to operate even during a forced blank. When the internal HV synchronous counter cancels a forced blank during a display period, the display begins from the beginning, following the display of three vertical lines.

DISPCNT [d06] OBJ Character VRAM Mapping Format

Specifies the VRAM mapping format for an OBJ character.

A setting of 0 causes the OBJ character to be handled in memory mapped 2-dimensional. A setting of 1 causes the OBJ character to be handled in memory mapped 1-dimensional.

For information on OBJ character VRAM mapping formats, see section 6.3.2, Character Data Mapping.

DISPCNT [d05] H-Blank Interval OBJ Processing Flag

A setting of 0 executes OBJ Render Processing with all H-Line intervals(including H-Blank intervals).

A setting of 1 executes OBJ Render Processing with the display intervals only and not for H-Blank intervals. Thus, when the user accesses OAM or OBJ VRAM during an H-Blank interval, this bit needs to be set. However, also in this situation, maximum OBJ display performance cannot be obtained.

DISPCNT [d04] Display Frame Selection

When rendering in bitmap format in a mode in which there are 2 frame buffers (BG modes 4 and 5), this bit allows selection of one of the frame buffers for rendering. A setting of 0 selects the contents of frame buffer 0 for rendering; a setting of 1 selects the contents of frame buffer 1 for rendering.

DISPCNT [d03] (CGB Mode)

AGB is equipped with 2 CPUs. In AGB mode, a 32-bit RISC CPU starts, and in CGB mode, an 8-bit CISC CPU starts.

Because this bit is controlled by the system, it cannot be accessed by the user.

DISPCNT [d02-00] BG Mode

Selects the BG mode from a range of 0-5.

For more information on BG modes, see the following section.

5.1 BG Modes

5.1.1 Details of BG Modes

In AGB, changing the BG mode allows character format and bitmap format to be used selectively, as appropriate.

In modes 0, 1, and 2, rendering to the LCD screen is performed in a character format suitable for the game.

In modes 3, 4, and 5, rendering to the LCD screen is performed in bitmap format.

BG Mode	Character Format BG Screen			Number of Characters Specifiable	Number of Colors/ Palettes	Features					
	Rotation/ Scaling	No. of Screens	Size			*1	*2	*3	*4	*5	*6
0	No	4	256 x 256 to 512 x 512	1024	16 / 16 256 / 1	O	O	O	O	O	O
1	No	2	256 x 256 to 512 x 512	1024	16 / 16 256 / 1	O	O	O	O	O	O
	Yes	1	128 x 128 to 1024 x 1024	256	256 / 1	O	X	O	O	O	O
2	Yes	2	128 x 128 to 1024 x 1024	256	256 / 1	O	X	O	O	O	O

BG Mode	Bitmap Format BG Screen			Frame Memory	No. of Colors	Features					
	Rotation/ Scaling	No. of Screens	Size			*1	*2	*3	*4	*5	*6
3	Yes	1	240 x 160	1	32,768	O	X	O	O	O	O
4	Yes	1	240 x160	2	256	O	X	O	O	O	O
5	Yes	1	160 x 128	2	32,768	O	X	O	O	O	O

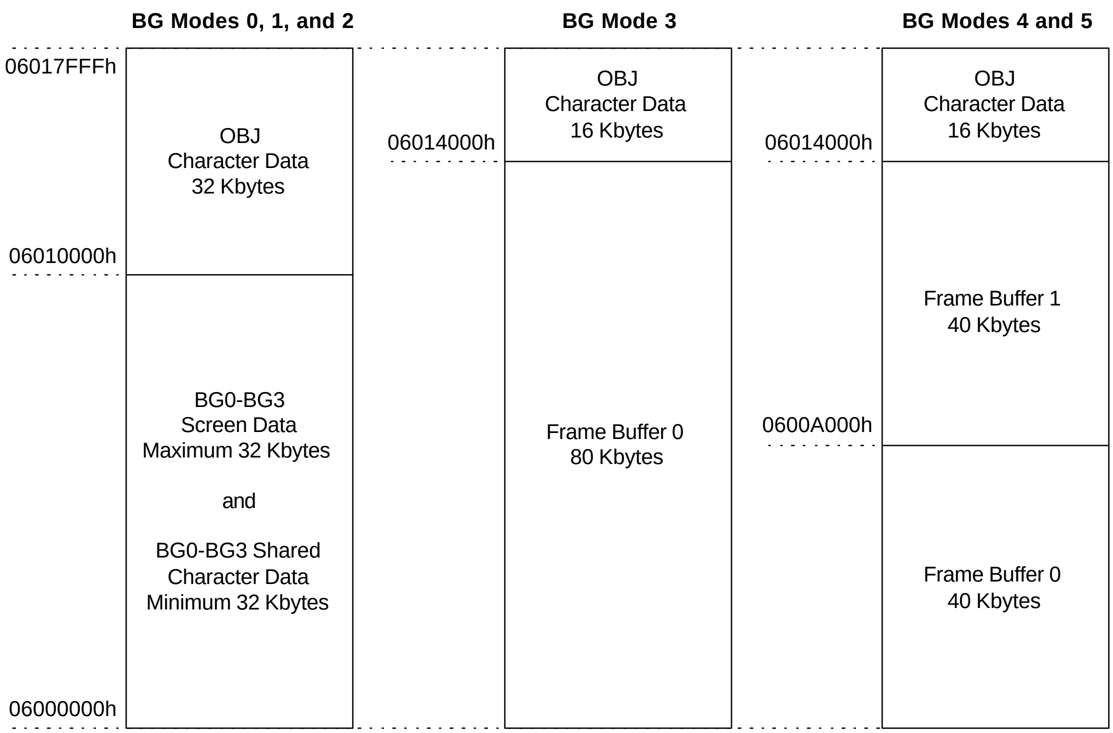
Features
*1 HV Scroll (individual screens)
*2 HV Flip (individual characters)
*3 Mosaic (16 levels)
*4 Semitransparent(16 levels)
*5 Fade-in/Fade-out
*6 Screen priority specification (2 bits)

[Note]
In mode 3, one frame memory is available that can display 32,768 colors, which is suitable for rendering still images. Modes 4 and 5 allow double buffering using two frame memories, and are thus suitable for rendering animated video.

The method of controlling text BG scrolling is different from that of BG rotation/scaling and bitmap BG scrolling. (See “6.1.8 BG Scrolling” and “6.1.7 BG Rotation and Scaling Features”.)

5.1.2 VRAM Memory Map

The VRAM (96 Kbyte) memory maps in the BG modes are as shown in the following figure.



Users can map the screen and character data areas in the 64 Kbyte BG area in BG modes 0, 1, and 2. For more information, see section 6.1.3, VRAM Address Mapping of BG Data.

In addition, see the descriptions below for more information on the memory areas and the data formats for each area.

6 Rendering Functions

The AGB CPU has 96 Kbytes of built-in VRAM.

Its rendering functions include BG and OBJ display capability. The method used for BG rendering varies with the BG mode, as described below.

6.1 Character Mode BG (BG Modes 0-2)

In character mode, the components of the BG screen are basic characters of 8 x 8 dots.

6.1.1 BG Control

There are 4 BG control registers, corresponding to the maximum number of BG screens (registers BG0CNT, BG1CNT, BG2CNT, and BG3CNT).

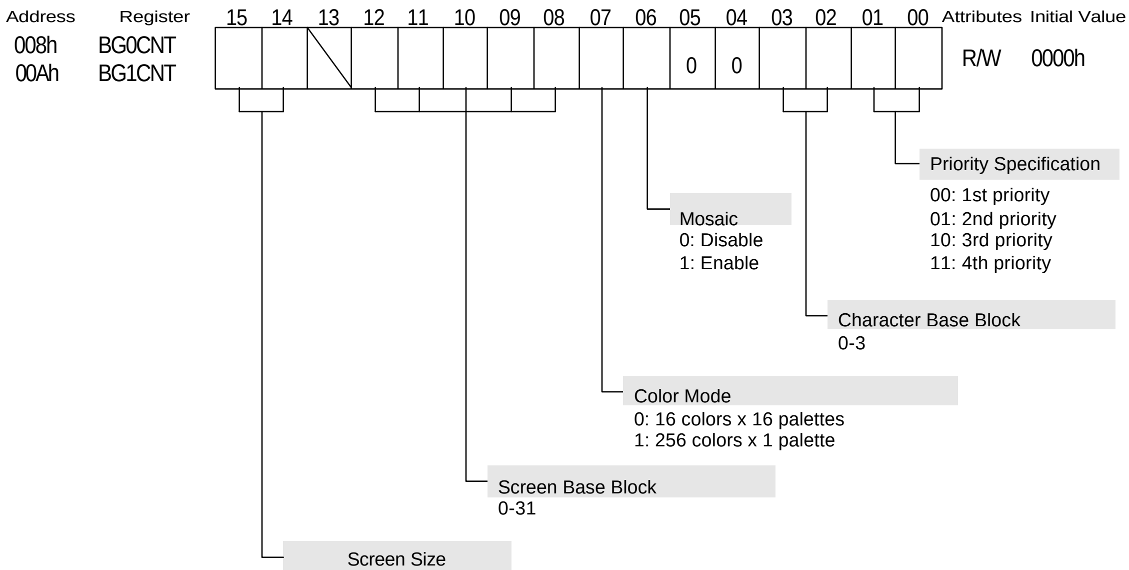
Registers BG0CNT and BG1CNT are exclusively for text BG control, while BG2CNT and BG3CNT also support BG rotation and scaling control.

The registers used by the BG modes are as follows.

BG Mode	BG Control Register			
	BG0CNT	BG1CNT	BG2CNT	BG3CNT
0	BG0 (text)	BG1 (text)	BG2 (text)	BG3 (text)
1	BG0 (text)	BG1 (text)	BG2 (rotation/scaling)	
2			BG2 (rotation/scaling)	BG3 (rotation/scaling)

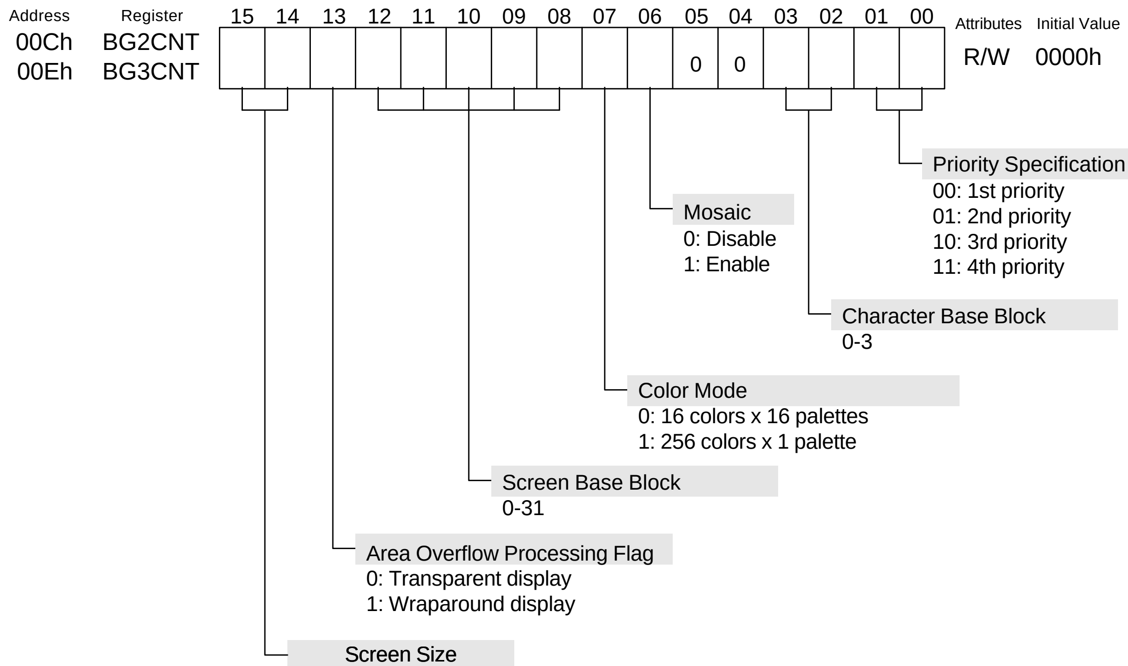
The contents of the BG control registers are shown below.

1) Text BG Screen Control (BG0, BG1)



2) Text BG and Rotation/Scaling BG Screen Control (BG2 and BG3)

Whether the screen is a text screen or a scaling/rotation screen varies with the BG mode.



BG*CNT [d15-14] Screen Size

Allows the screen size for the BG as a whole to be specified.

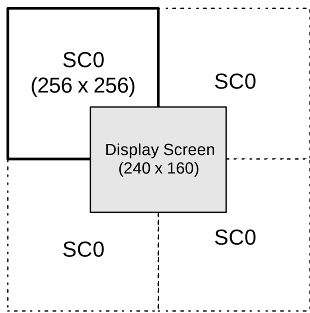
When a value other than the maximum is specified, the remaining VRAM area can be used as a character data area.

Refer to the table below and the VRAM Memory Map figure above.

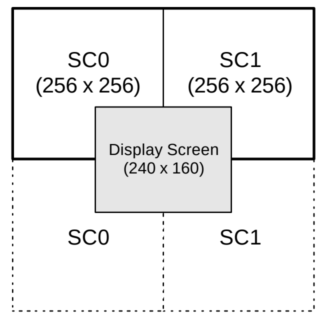
Screen Size Setting	Text Screen		Rotation/Scaling Screen	
	Screen Size	Screen Data	Screen Size	Screen Data
00	256×256	2 Kbytes	128×128	256 Bytes
01	512×256	4 Kbytes	256×256	1 Kbyte
10	256×512	4 Kbytes	512×512	4 Kbytes
11	512×512	8 Kbytes	1024×1024	16 Kbytes

1) Overview of Screen Sizes for Text BG Screens

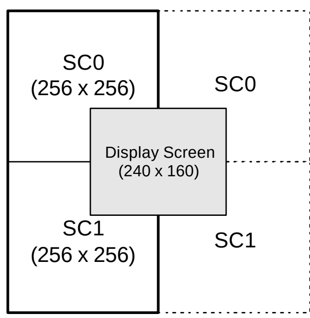
[d15,d14]=[0,0] Virtual screen size:256 x 256



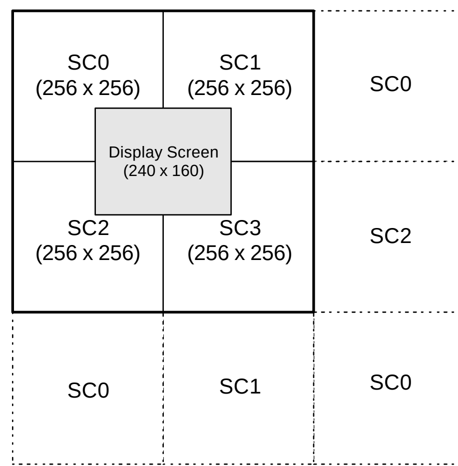
[d15,d14]=[0,1] Virtual Screen size: 512 x 256



[d15,d14]=[1,0] Virtual screen size: 256 x 512

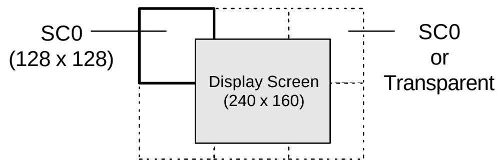


[d15,d14]=[1,1] Virtual screen size: 512 x 512

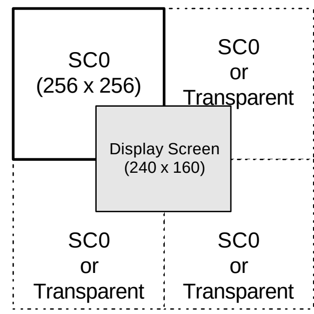


2) Illustration of Screen Sizes for Rotation/Scaling BG Screens

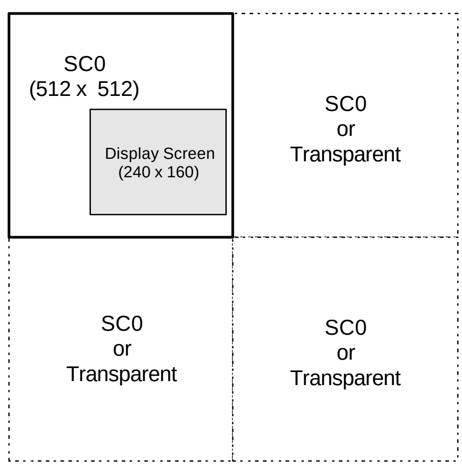
[d15,d14]=[0,0]Virtual screen size: 128 x 128



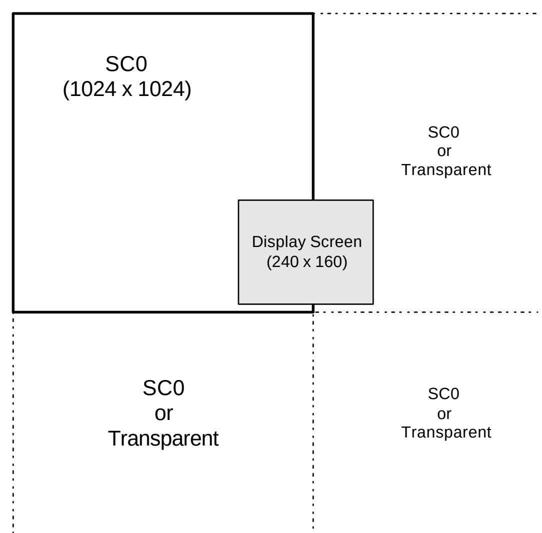
[d15,d14]=[0,1]Virtual screen size: 256 x 256



[d15,d14]=[1,0]Virtual screen size: 512 x 512



[d15,d14]=[1,1]Virtual screen size: 1024 x1024



BG2CNT,BG3CNT [d13] Area Overflow Processing

When the display screen overflows the boundaries of the virtual screen due to a rotation/scaling operation, this bit can be used to choose whether the area of the screen into which the overflow occurs is displayed as transparent or wraps around the display screen.

For information on scaling, see “6.1.7 BG Rotation and Scaling Features”.

BG*CNT [d12-08] Screen Base Block Specification

Specifies the starting block in VRAM where screen data are stored.
(32 steps: 0-31; 2-Kbyte increments).

See section 6.1.3, VRAM Address Mapping of BG Data.

BG*CNT [d07] Color Mode

Specifies whether to reference BG character data in 16 color x 16 palette format or 256 color x 1 palette format.

BG*CNT [d06] Mosaic

Turns mosaic processing for BG on and off.

BG*CNT [d03-02] Character Base Block Specification

Specifies the starting block in VRAM where the character data to be displayed in the BG is stored.
(4 steps: 0-3; 16-Kbyte increments)

See section 6.1.3, VRAM Address Mapping of BG Data.

BG*CNT [d01-00] Priority Among BGs

With the default value (same priority value specified for all), the order of priority is BG0, BG1, BG2, and BG3. However, this order can be changed to any desired.

Values of 0 (highest priority) to 3 can be specified.

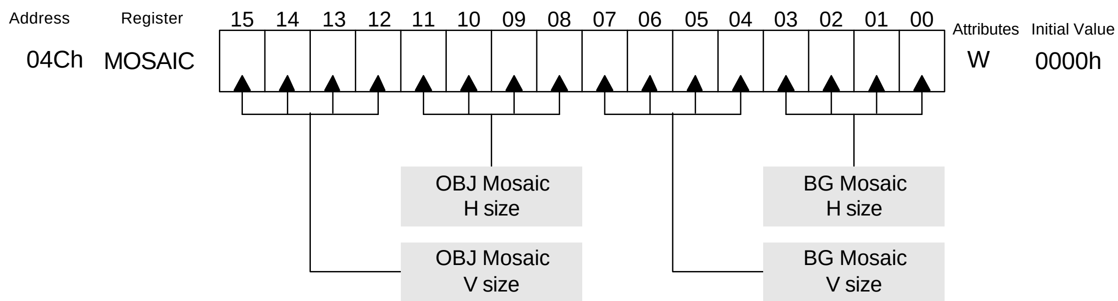
When the BG priority has been changed, care should be taken in specifying the pixels used for color special effects.

6.1.2 Mosaic Size

Mosaic size is set in the MOSAIC register.

Turning mosaic on/off for each BG is accomplished by the mosaic flag of the BG control register.

For information on the mosaic flag, see the previous section, BG Control.

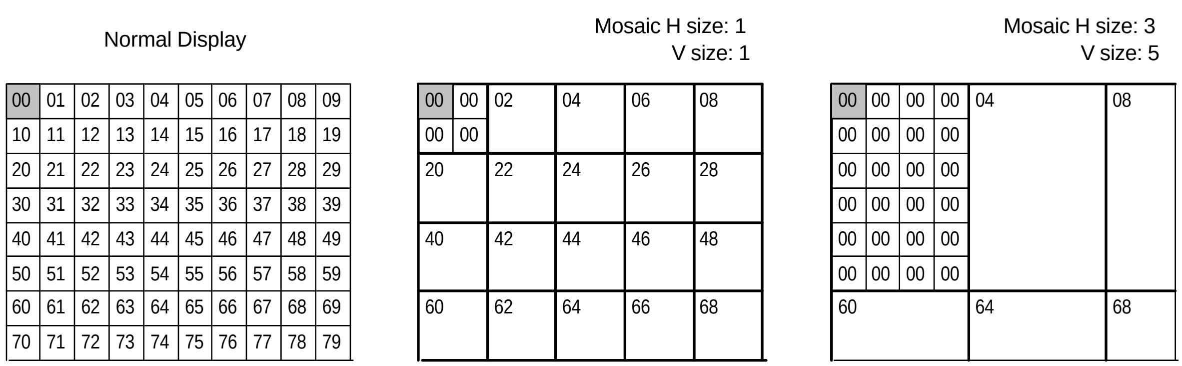


The mosaic value specifies how many dots of a normal display should comprise each large dot displayed.

Counting from the upper left-most dot on the screen, the number of dots equal to the mosaic size are used in the mosaic display. The other dots are overwritten by the mosaic. Please refer to the figure below.

If the mosaic size value is 0, a normal display is seen even if mosaic is turned on.

Mosaic Schematic



6.1.3 VRAM Address Mapping of BG Data

BG data (BG character and screen data) are stored in the 64-Kbyte BG area of VRAM.

1) BG Character Data

The starting address for referencing BG character data can be specified using the character base block specification of the BG control register.

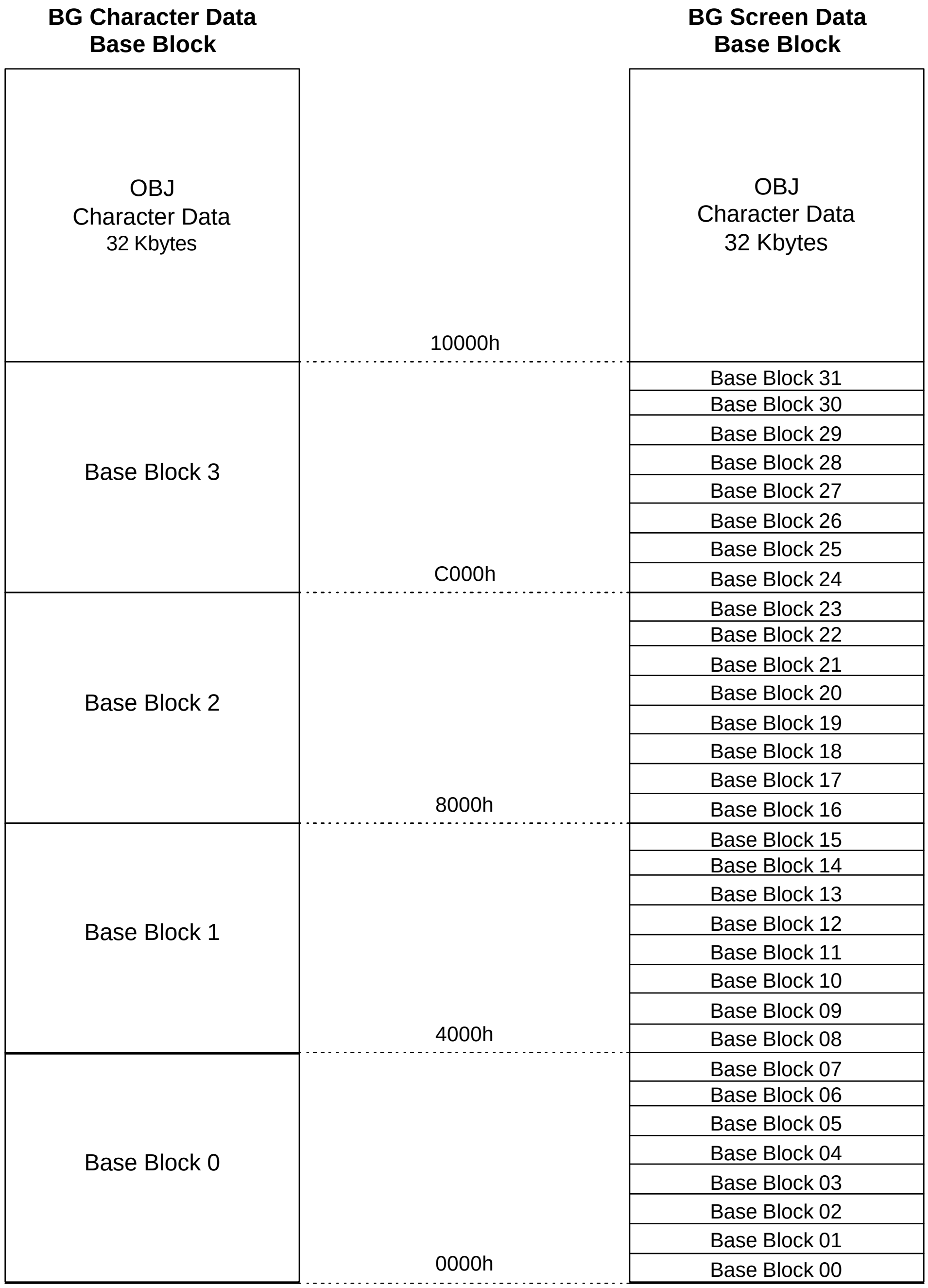
The amount of data depends on the number of character data items stored and the data format (color formats: 256 colors x 1 palette or 16 colors x 16 palettes).

2) BG Screening Data

The starting address for referencing BG screen data can be set using the screen base block specification of the BG control register.

The amount of data depends on the type of BG screen (text or rotation/scaling) and the screen size. These can be set by the BG control register.

Illustration of VRAM Base Blocks for BG Data



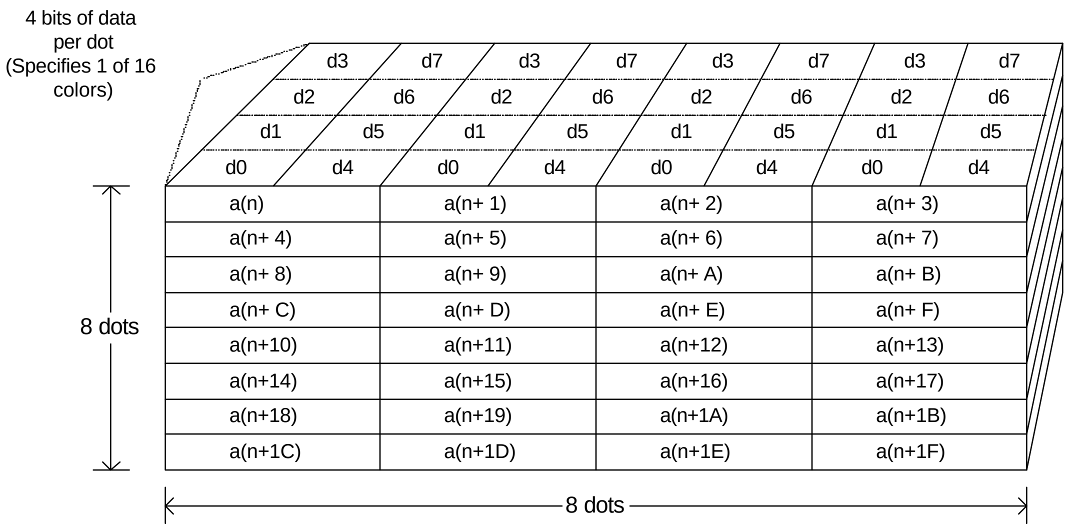
6.1.4 Character Data Format

There are two formats for character dot data, 16 color x 16 palettes and 256 colors x 1 palette. The same format is used for OBJ and BG.

The data are held in VRAM in the form indicated below.

1) 16 Colors x 16 Palettes

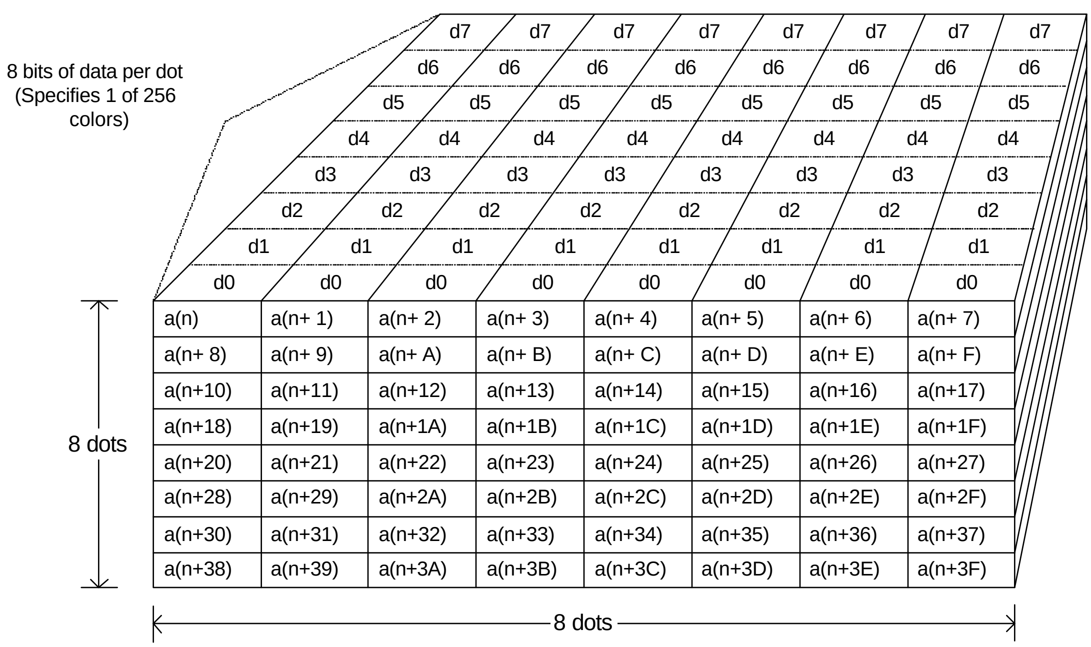
There are 2 dots per address. Thus, the amount of data for each basic character is 20H x 8 bits.



a(n)	a(n+ 1)	a(n+ 2)	a(n+ 3)
a(n+ 4)	a(n+ 5)	a(n+ 6)	a(n+ 7)
a(n+ 8)	a(n+ 9)	a(n+ A)	a(n+ B)
a(n+ C)	a(n+ D)	a(n+ E)	a(n+ F)
a(n+10)	a(n+11)	a(n+12)	a(n+13)
a(n+14)	a(n+15)	a(n+16)	a(n+17)
a(n+18)	a(n+19)	a(n+1A)	a(n+1B)
a(n+1C)	a(n+1D)	a(n+1E)	a(n+1F)

2) 256 Colors x 1 Palette

There is 1 dot specified per address. Thus, the amount of data for each basic character is 40H x 8 bits.



a(n)	a(n+ 1)	a(n+ 2)	a(n+ 3)	a(n+ 4)	a(n+ 5)	a(n+ 6)	a(n+ 7)
a(n+ 8)	a(n+ 9)	a(n+ A)	a(n+ B)	a(n+ C)	a(n+ D)	a(n+ E)	a(n+ F)
a(n+10)	a(n+11)	a(n+12)	a(n+13)	a(n+14)	a(n+15)	a(n+16)	a(n+17)
a(n+18)	a(n+19)	a(n+1A)	a(n+1B)	a(n+1C)	a(n+1D)	a(n+1E)	a(n+1F)
a(n+20)	a(n+21)	a(n+22)	a(n+23)	a(n+24)	a(n+25)	a(n+26)	a(n+27)
a(n+28)	a(n+29)	a(n+2A)	a(n+2B)	a(n+2C)	a(n+2D)	a(n+2E)	a(n+2F)
a(n+30)	a(n+31)	a(n+32)	a(n+33)	a(n+34)	a(n+35)	a(n+36)	a(n+37)
a(n+38)	a(n+39)	a(n+3A)	a(n+3B)	a(n+3C)	a(n+3D)	a(n+3E)	a(n+3F)

6.1.5 BG Screen Data Format

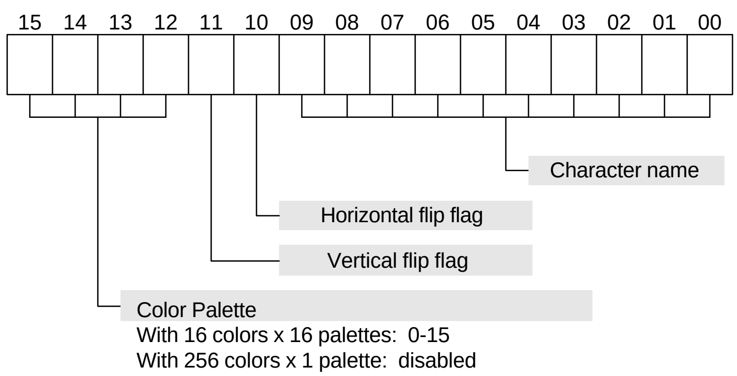
A BG screen is considered to be the 8 x 8 dot unit that represents the size of the basic character, and the BG screen data specifies the characters that are arranged.

BG screen data should be stored, beginning from the starting address of the BG screen base block specified in the BG control register. The number of screen data items specified per BG depends on the screen size setting in the BG control register.

BG screen data for text and rotation/scaling screens are specified in the following formats.

1) Text BG Screen

A text BG screen consists of 2 bytes of screen data per basic character; 1,024 character types can be specified.



[d15-12] Color Palette

If the color mode specification in the BG control register is 16 colors x 16 palettes, these bits specify palette 0-15 as the palette to be applied to the character.

This is disabled when the color mode specification is 256 x 1 palette.

[d11] Vertical Flip Flag

Enables the BG character to be flipped vertically.

A setting of 1 produces the vertical-flip display.

[d10] Horizontal Flip Flag

Enables the BG character to be flipped horizontally.

A setting of 1 produces the horizontal-flip display.

[d09-00] Character Name

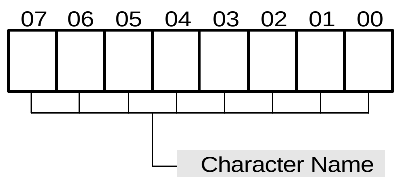
Specify the number of the character that has character base block starting address specified in the BG control register as its starting point.

2) Rotation/Scaling BG Screen

The rotation/scaling BG screen consists of 1 byte of screen data per basic character; 256 character types can be specified.

The character data must be classified as 256 colors x 1 palette.

The color mode specification in the BG control register is disabled for a rotation/scaling screen.



[Cautions for VRAM]

AGB provides a high degree of freedom in using the BG area of VRAM.

Consequently, in managing VRAM, the following points deserve particular attention.

1. There are 2 formats for BG character data (defined by 16 and 256 colors), and these can be used together.
2. The BG character data base block can be selected from among 4 blocks (BG control register).
3. The BG screen data base block can be selected from among 32 blocks (BG control register).
4. The screen size (amount of VRAM used) can be set for each BG (BG control register).
5. Text and rotation/scaling BGs can be present and used together in a BG screen.

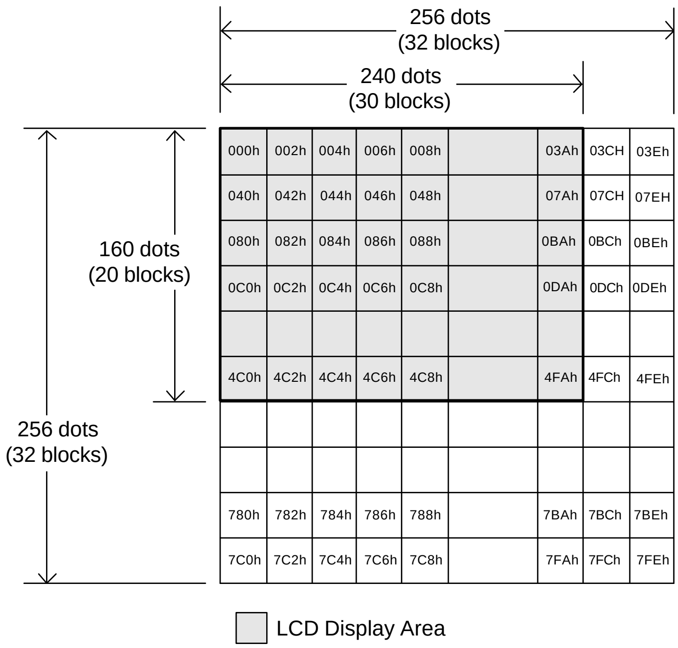
In managing VRAM, particular care is required in BG mode 1, because text BG screens (which can handle BG character data in both 256 colors x 1 palette and 16 colors x 16 palettes) and rotation/scaling BG screens (which can handle only 256 colors x 1 palette) may be used together.

Therefore, the VRAM mapping status should be sufficiently understood when programming.

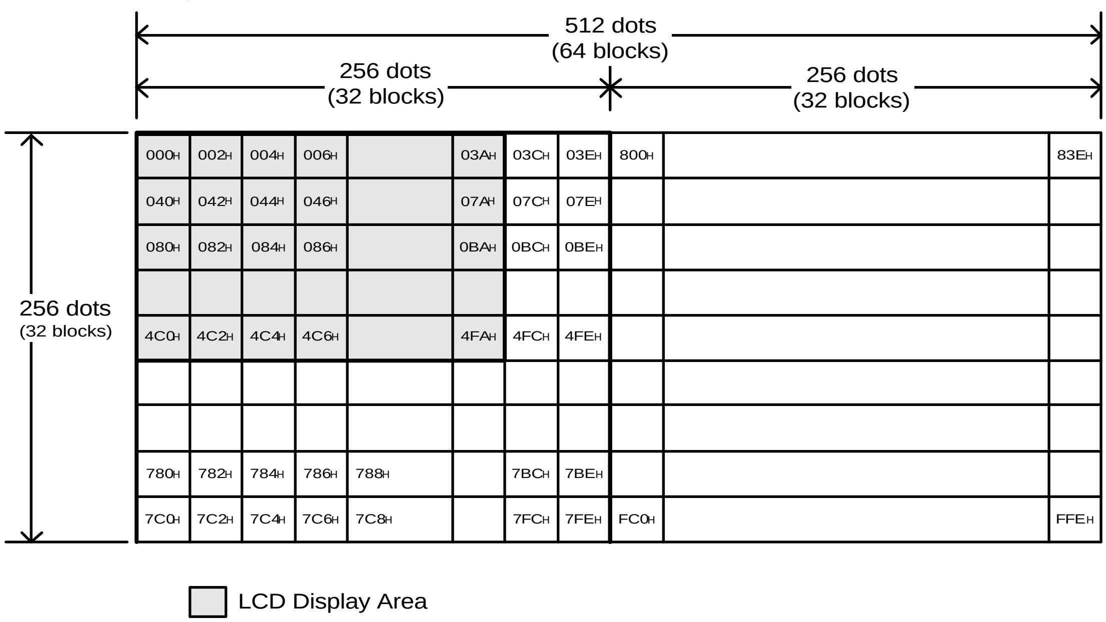
6.1.6 BG Screen Data Address Mapping for the LCD Screen

1) Text BG

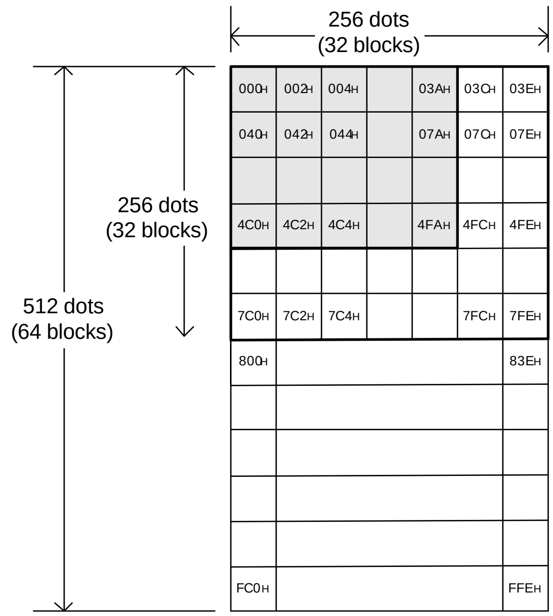
1-1) Virtual Screen Size of 256 x 256 Dots



1-2) Virtual Screen Size of 512 x 256 Dots

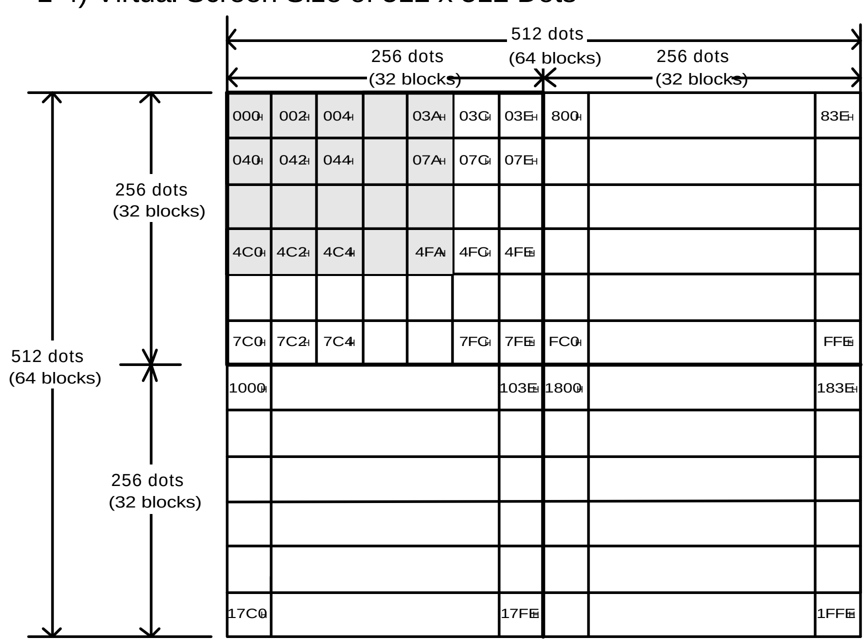


1-3) Virtual Screen Size of 256 x 512 Dots



LCD display area

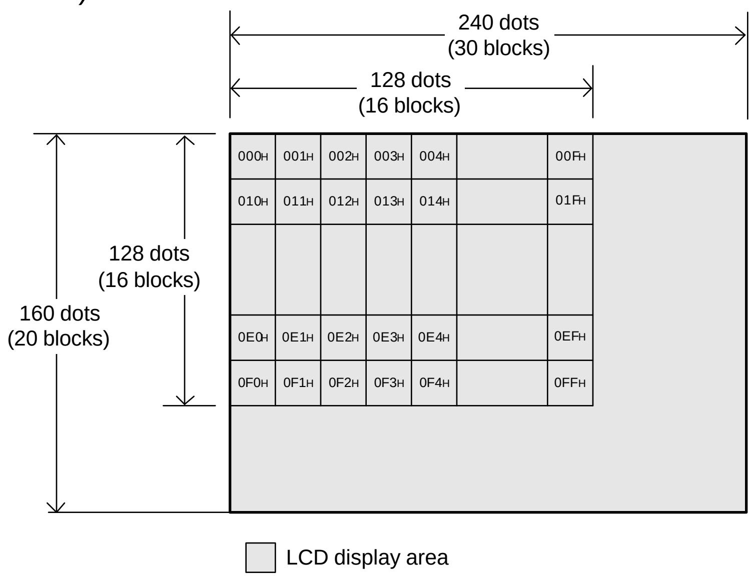
1-4) Virtual Screen Size of 512 x 512 Dots



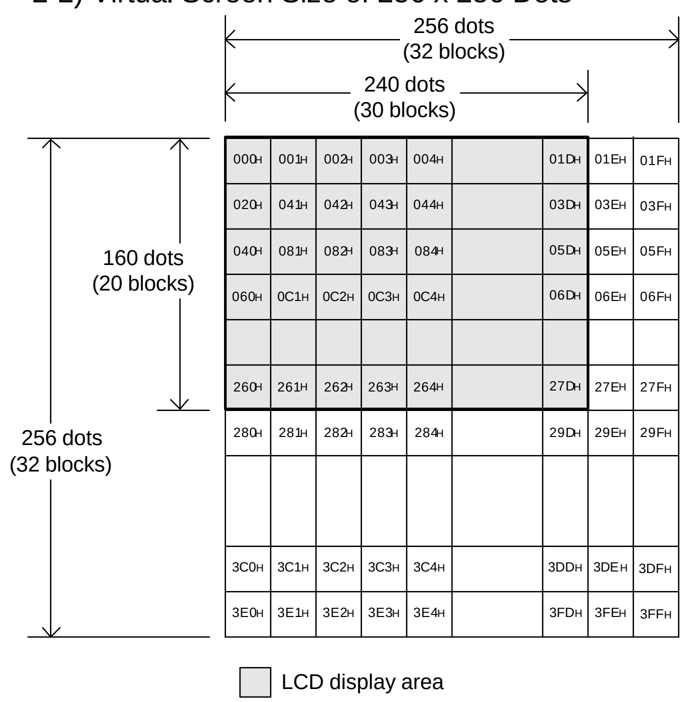
LCD display area

2) Rotation/scaling BG

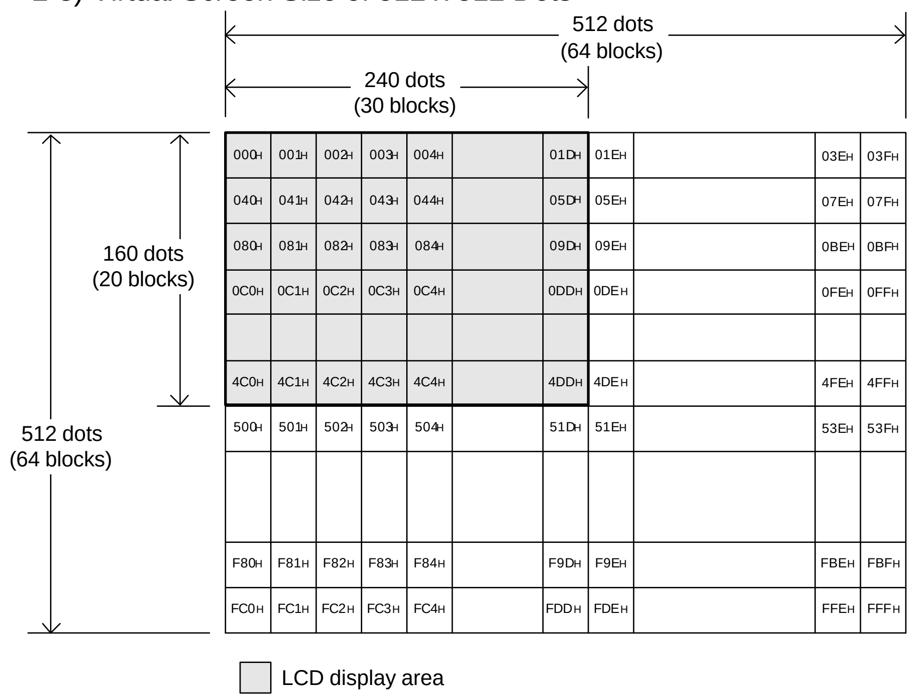
2-1) Virtual Screen Size of 128 x 128 Dots



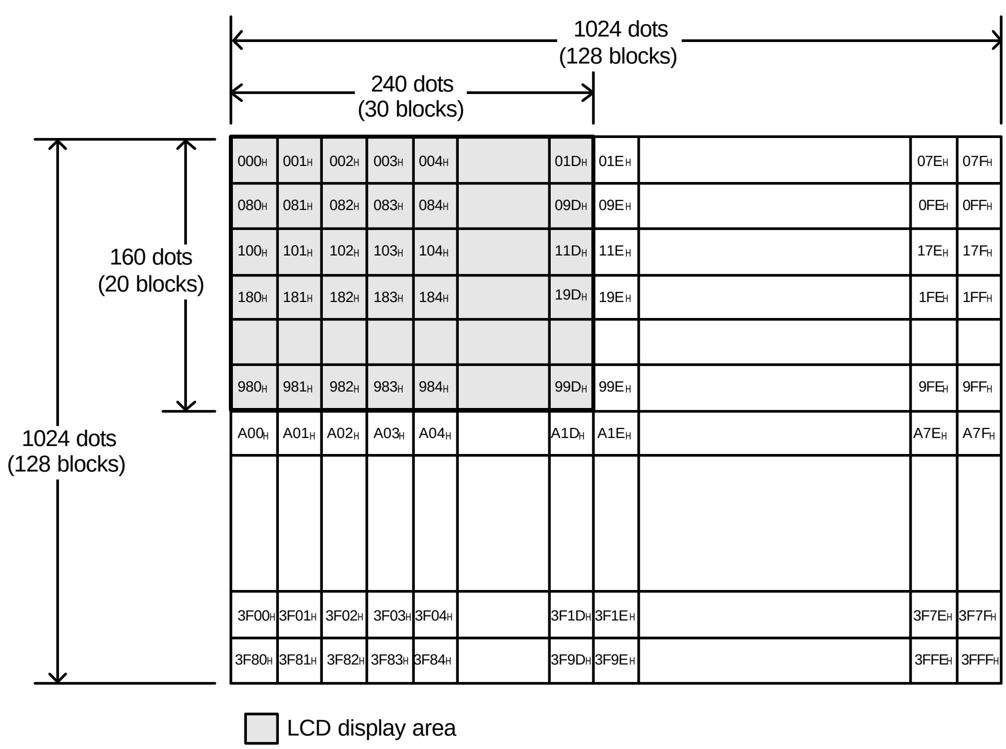
2-2) Virtual Screen Size of 256 x 256 Dots



2-3) Virtual Screen Size of 512 x 512 Dots



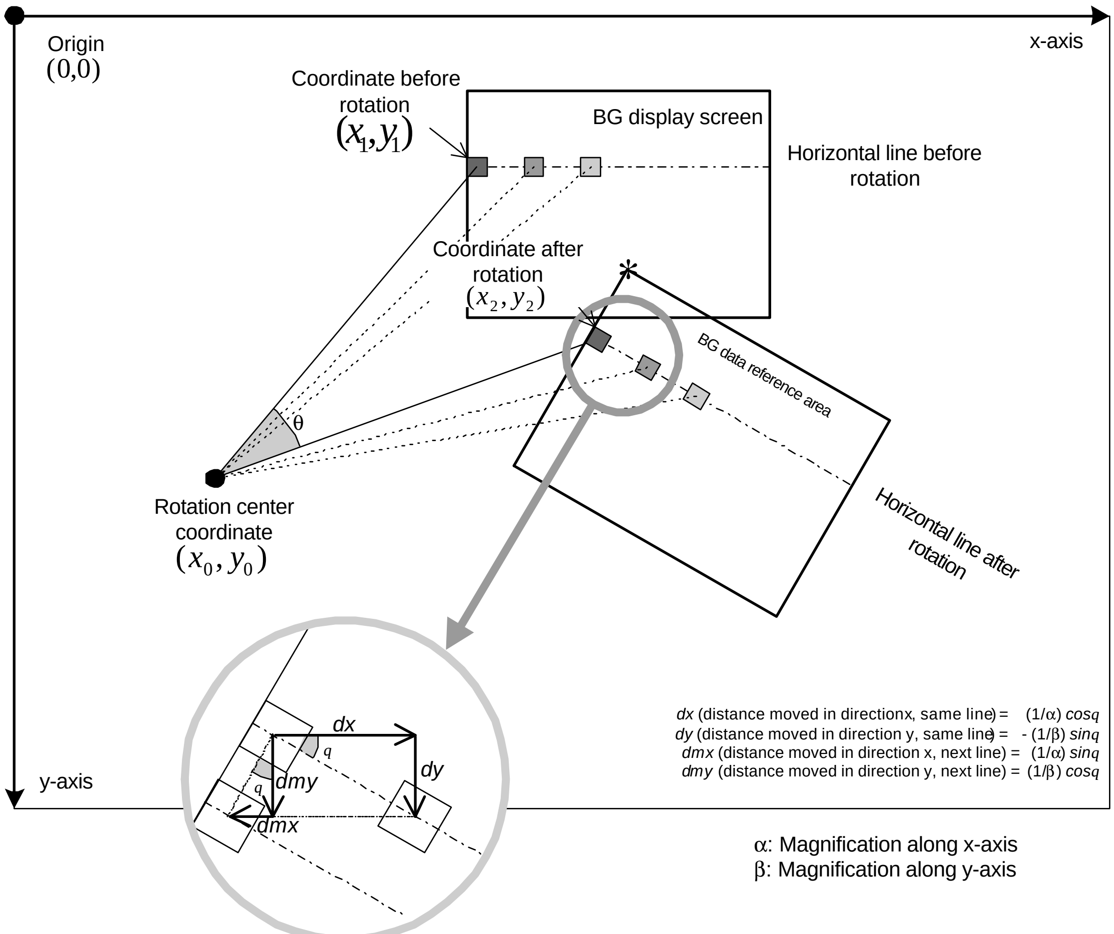
2-4) Virtual Screen Size of 1024 x 1024 Dots



6.1.7 BG Rotation and Scaling Features

Rotation and scaling of the BG as a whole can be performed in a rotation/scaling BG screen.

With rotation, BG data is referenced as shown in the following figure.



BG rotation and scaling are implemented in AGB using the following arithmetic expressions.

$$\begin{pmatrix} x_2 \\ y_2 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} x_1 - x_0 \\ y_1 - y_0 \end{pmatrix} + \begin{pmatrix} x_0 \\ y_0 \end{pmatrix}$$

$$A = \frac{1}{a}\cos q, \quad B = \frac{1}{a}\sin q, \quad C = -\frac{1}{b}\sin q, \quad D = \frac{1}{b}\cos q$$

$$x_2 = A(x_1 - x_0) + B(y_1 - y_0) + x_0$$
$$y_2 = C(x_1 - x_0) + D(y_1 - y_0) + y_0$$

Parameters used in rotation and scaling operations are specified for BG2 and BG3 in the following registers. Registers for Starting Point of BG Data Reference are also used when Scaling/Rotation BG and Bitmap Mode BG are offset displayed (scrolled). (There is also an offset register for Text BG.)

Registers for Setting the Starting Point of BG Data

Address	Register	15	14	13	12	11–00	Attributes	Initial Value
028h 038h	BG2X_L BG3X_L	X-coordinate of reference starting point (rotation/scaling results)					W	0000h
02Ah 03Ah	BG2X_H BG3X_H					X-coordinate of reference starting point (rotation/scaling results)	W	0000h
02Ch 03Ch	BG2Y_L BG3Y_L	Y-coordinate of reference starting point (rotation/scaling results)					W	0000h
02Eh 03Eh	BG2Y_H BG3Y_H					Y-coordinate of reference starting point (rotation/scaling results)	W	0000h

Registers for Setting the Direction Parameters of BG Data

Address	Register	15–00	Attributes	Initial Value
020h 030h	BG2PA BG3PA	dx: distance of movement in x direction along same line	W	0100h
022h 032h	BG2PB BG3PB	dmx: distance of movement in x direction along next line	W	0000h
024h 034h	BG2PC BG3PC	dy: distance of movement in y direction along same line	W	0000h
026h 036h	BG2PD BG3PD	dmy: distance of movement in y direction along next line	W	0100h

Operations Used in BG Rotation/Scaling Processing

1. Using software, the user determines the results of the rotation/scaling operation for the left-upper coordinate of the display screen and sets this as the starting point of the BG data reference in registers BG2X_L, BG2X_H, BG2Y_L, BG2Y_H, BG3X_L, BG3X_H, BG3Y_L, and BG3Y_H. The set value is a signed fixed-point number (8 bits for fractional portion, 19 bits for integer portion, and 1 bit for sign, for a total of 28 bits).

   The BG data reference direction is set in BG2PA, BG2PB, BG2PC, BG2PD, BG3PA, BG3PB, BG3PC, and BG3PD. The set value is a signed fixed-point number (8 bits for fractional portion, 7 bits for integer portion, and 1 bit for sign, for a total of 16 bits).
2. The image processing circuit sums the increases in the x direction (dx, dy) in relation to the BG data reference starting point set in the above registers, and calculates the x-coordinate.
3. When the line is advanced, the increases in the y direction (dmx, dmy) are summed in relation to the reference starting point, and the coordinate of the rendering starting point for the next line is calculated. The processing in step 2) is then performed.
4. However, if a register for the BG data reference starting point is rewritten during an H-blanking interval, the y-direction summation for that register is not calculated. The CPU uses this mode to change the center coordinate and the rotation/scaling parameters for each line.

Area Overflow Processing

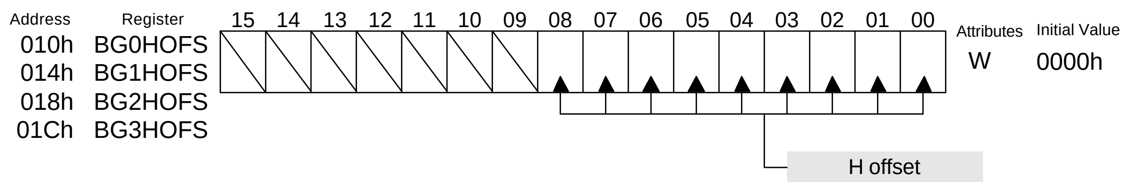
When the display screen overflows the boundaries of the virtual screen due to a rotation/scaling operation, this BG control register can be used to select whether the area of the screen into which the overflow occurs is transparent or wraps around the display screen.

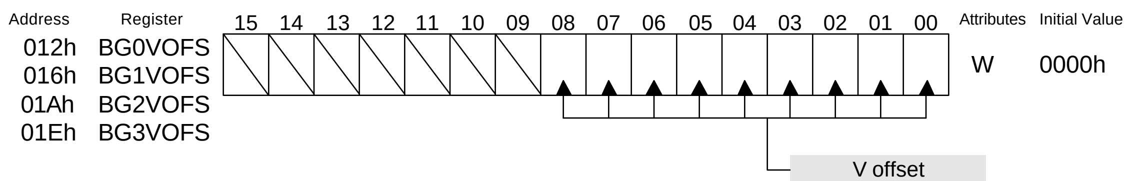
For information on BG control, see “6.1.1 BG Control”.

6.1.8 BG Scrolling

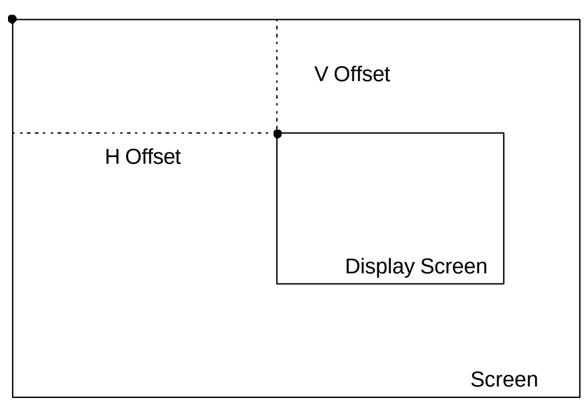
For each text BG screen, the offset on the display screen can be specified in 1-dot increments. Offset register is only valid for Text BG. In order to offset display Scaling/Rotation BG and Bitmap Mode BG set the BG Reference Starting Point. See “6.1.7, BG Rotation and Scaling Features”.

Offset Settings Registers





Offset Illustration

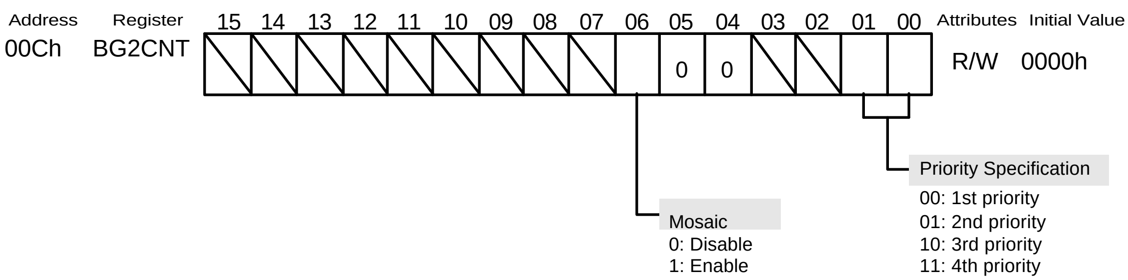


6.2 Bitmap Mode BGs (BG Modes 3-5)

In the bitmap modes, the components of the BG screen are handled in pixel units, and the contents of VRAM (frame buffer) are displayed as color data for each dot on the screen.

6.2.1 BG Control

The bitmap BG will be treated as BG2. Therefore, in order to display the content of the frame buffer on the LCD screen, you need to set the BG2 display flag to ON in the DISPCNT Register. For BG Control the BG2CNT Register is used.



BG2CNT [d06] Mosaic

This controls the ON/OFF of mosaic processing for BG2. When ON, the settings for the Mosaic Size Register, MOSAIC, are referenced. For information on Mosaic, see “6.1.2 Mosaic Size”.

BG2CNT [d01-00] Priority Among BGs

Due to the fact that in Bitmap Mode there is only one BG plane(other than the backdrop plane), there is no priority relationship among BGs, but you can set up priorities with OBJ. For information on this, see “6.4 Display Priority of OBJ and BG”.

6.2.2 BG Rotation/Scaling

The parameters for Bitmap BG Rotation/Scaling use BG2 related registers(BG2X_L, BG2X_H, BG2Y_L, BG2Y_H, BG2PA, BG2PB, BG2PC, and BG2PD).

For information on rotation/scaling parameters, see "6.1.7 BG Rotation/Scaling Features".

With Bitmap BG, if the displayed portion exceeds the edges of the screen due to the rotation/scaling operation, that area becomes transparent.

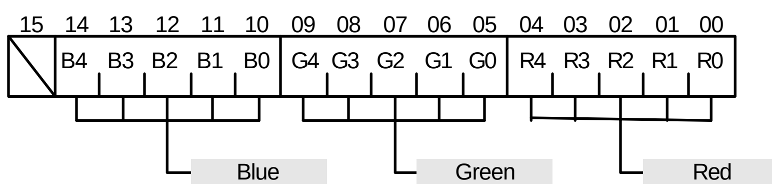
6.2.3 Pixel Data

In the bitmap modes, only the amount of pixel data corresponding to the size of the display screen can be stored in VRAM. Available bitmap modes allow the simultaneous display of 32,768 colors (BG modes 3 and 5) and the display of 256 of the 32,768 colors (BG mode 4). The format of the data in the frame buffer differs between the modes as described below.

1. 32,768-Color Simultaneous Display Format (BG Modes 3 and 5)

   Palette RAM is not referenced.

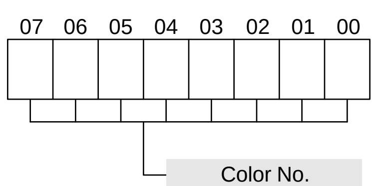
   Each pixel uses a half-word.



2. 256-Color (of 32,768) Display Format (BG Mode 4)

   Palette RAM color data (256 of the 32,768 colors storable) are referenced.

   Each pixel uses 1 byte.



6.2.4 Pixel Data Address Mapping for the LCD Screen

The different address mappings for the different BG modes are shown below.

The frame buffer (VRAM) starts at address 06000000h. Thus, to see the addresses used by the CPU, add 06000000h to the addresses shown below.

6.2.4.1 BG Mode 3 (32,768 colors, 240X160 dots, 1 frame buffer)

Because there is a single frame buffer, this mode is used mainly for still images. However, it enables 32,768 colors to be displayed simultaneously over the full screen.

	0	1	2	3	4		236	237	238	239
0	0h	2h	4h	6h	8h		1D8h	1Dah	1DCh	1DEh
1	1E0h	1E2h	1E4h	1E6h	1E8h		3B8h	3Bah	3BCh	3BEh
2	3C0h	3C2h	3C4h	3C6h	3C8h		598h	59Ah	59Ch	59Eh
3	5A0h	5A2h	5A4h	5A6h	5A8h		778h	77Ah	77Ch	77Eh
4	780h	782h	784h	786h	788h		958h	95Ah	95Ch	95Eh
156	12480h	12482h	12484h	12486h	12488h		12658h	1265Ah	1265Ch	1265Eh
157	12660h	12662h	12664h	12666h	12668h		12838h	1283Ah	1283Ch	1283Eh
158	12840h	12842h	12844h	12846h	12848h		12A18h	12A1Ah	12A1Ch	12A1Eh
159	12A20h	12A22h	12A24h	12A26h	12A28h		12BF8h	12BFAh	12BFCh	12BFEh

VRAM address (+06000000h)

6.2.4.2 BG Mode 4 (256 colors, 240X160 dots, 2 frame buffers)

Two frame buffers are allocated in VRAM, making this mode suitable for full-motion video. Of the total of 32,768 colors, 256 can be displayed simultaneously over the full screen.

1) Frame 0

	0	1	2	3	4		236	237	238	239
0	0h	1h	2h	3h	4h		ECh	EDh	EEh	EFh
1	F0h	F1h	F2h	F3h	F4h		1DCh	1DDh	1DEh	1DFh
2	1E0h	1E1h	1E2h	1E3h	1E4h		2CCh	2CDh	2CEh	2CFh
3	2D0h	2D1h	2D2h	2D3h	2D4h		3BCh	3BDh	3BEh	3BFh
4	3C0h	3C1h	3C2h	3C3h	3C4h		4ACh	4ADh	4AEh	4AFh
156	9240h	9241h	9242h	9243h	9244h		932Ch	932Dh	932Eh	932Fh
157	9330h	9331h	9332h	9333h	9334h		941Ch	941Dh	941Eh	941Fh
158	9420h	9421h	9422h	9423h	9424h		950Ch	950Dh	950Eh	950Fh
159	9510h	9511h	9512h	9513h	9514h		95FCh	95FDh	95FEh	95FFh

VRAM address (+06000000h)

2) Frame 1

	0	1	2	3	4		236	237	238	239
0	A000h	A001h	A002h	A003h	A004h		A0ECh	A0EDh	A0EEh	A0EFh
1	A0F0h	A0F1h	A0F2h	A0F3h	A0F4h		A1DCh	A1DDh	A1DEh	A1DFh
2	A1E0h	A1E1h	A1E2h	A1E3h	A1E4h		A2CCh	A2CDh	A2CEh	A2CFh
3	A2D0h	A2D1h	A2D2h	A2D3h	A2D4h		A3BCh	A3BDh	A3BEh	A3BFh
4	A3C0h	A3C1h	A3C2h	A3C3h	A3C4h		A4ACh	A4ADh	A4AEh	A4AFh
156	13240h	13241h	13242h	13243h	13244h		1332Ch	1332Dh	1332Eh	1332Fh
157	13330h	13331h	13332h	13333h	13334h		1341Ch	1341Dh	1341Eh	1341Fh
158	13420h	13421h	13422h	13423h	13424h		1350Ch	1350Dh	1350Eh	1350Fh
159	13510h	13511h	13512h	13513h	13514h		135FCh	135FDh	135FEh	135FFh

VRAM address (+06000000h)

6.2.4.3 BG Mode 5 (32,768 colors, 160X128 dots, 2 frame buffers)

Although there are 2 frame buffers, the display area is limited in this mode to enable simultaneous display of 32,768 colors.

1) Frame 0

	0	1	2	3	4		156	157	158	159
0	0h	2h	4h	6h	8h		138h	13Ah	13Ch	13Eh
1	140h	142h	144h	146h	148h		298h	29Ah	29Ch	29Eh
2	2A0h	2A2h	2A4h	2A6h	2A8h		3B8h	3BAh	3BCh	3BEh
3	3C0h	3C2h	3C4h	3C6h	3C8h		4F8h	4FAh	4FCh	4FEh
4	500h	502h	504h	506h	508h		638h	63Ah	63Ch	63Eh
124	9B00h	9B02h	9B04h	9B06h	9B08h		9C38h	9C3Ah	9C3Ch	9C3Eh
125	9C40h	9C42h	9C44h	9C46h	9C48h		9D78h	9D7Ah	9D7Ch	9D7Eh
126	9D80h	9D82h	9D84h	9D86h	9D88h		9EB8h	9EBAh	9EBCh	9EBEh
127	9EC0h	9EC2h	9EC4h	9EC6h	9EC8h		9FF8h	9FFAh	9FFCh	9FFEh

VRAM Address (+06000000h)

2) Frame 1

	0	1	2	3	4		156	157	158	159
0	A000h	A002h	A004h	A006h	A008h		A138h	A13Ah	A13Ch	A13Eh
1	A140h	A142h	A144h	A146h	A148h		A298h	A29Ah	A29Ch	A29Eh
2	A2A0h	A2A2h	A2A4h	A2A6h	A2A8h		A3B8h	A3BAh	A3BCh	A3BEh
3	A3C0h	A3C2h	A3C4h	A3C6h	A3C8h		A4F8h	A4FAh	A4FCh	A4FEh
4	A500h	A502h	A504h	A506h	A508h		A638h	A63Ah	A63Ch	A63Eh
124	13B00h	13B02h	13B04h	13B06h	13B08h		13C38h	13C3Ah	13C3Ch	13C3Eh
125	13C40h	13C42h	13C44h	13C46h	13C48h		13D78h	13D7Ah	13D7Ch	13D7Eh
126	13D80h	13D82h	13D84h	13D86h	13D88h		13EB8h	13EBAh	13EBCh	13EBEh
127	13EC0h	13EC2h	13EC4h	13EC6h	13EC8h		13FF8h	13FFAh	13FFCh	13FFEh

VRAM address (+06000000h)

6.3 OBJ (Object)

6.3.1 OBJ Function Overview

Objects are in character format regardless of the BG mode. However, the number of basic characters that can be defined varies depending on the BG mode.

Item	Function
Number of display colors	16 colors/16 palettes or 256 colors/1 palette (mixed display possible)
Number of characters (8x8 dots)	1,024 (16 colors x 16 palettes) : in BG modes 0-2 512 (256 colors x 1 palette) : " 512 (16 colors x 16 palettes) : in BG modes 3-5 256 (256 colors x 1 palette) : "
Character size	8x8 - 64x64 dots (12 types)
Max. number per screen	128 (64x64 dot conversion)
Max. number per line	128 (8x8 dot conversion)
Color special effects	HV flip, semi-transparency, mosaic, priority specification, OBJ windows

OBJ Display Capability on a Single Line

The single-line OBJ display capability shown in the table above, is the capability at maximum efficiency.

When the displayed OBJ are arranged continuously from the start of OAM, you can calculate the OBJ display capability on a single line using the following formula:

(Number of H Dots × 4 - 6) / Number of Rendering Cycles =

OBJ Displayable on a single line(Max. of 128)

The “Number of H Dots” is usually 308 dots, but when the H-Blank Interval OBJ Processing Flag for Register DISPCNT is set to 1, there are 240 dots(Refer to “4 LCD”).

“×4” expresses the number of cycles that the OBJ Rendering Circuit can use per one dot. “-6” represents the number of cycles needed for processing before OBJ rendering at the start of the H Line.

The “Number of Rendering Cycles” and the corresponding number of OBJ displayable for a single line is expressed in the table below.

OBJ H Size	Number of Rendering Cycles		Number of OBJ displayable on single line	
	Normal OBJ	Rotation/Scaling OBJ	Normal OBJ	Rotation/Scaling OBJ
8	8	26	128	47
16	16	42	76	29
32	32	74	38	16
64	64	138	19	8
128 (double the size of 64)	X	266	X	4

If the number for non-displayed (outside of the screen) OBJ in the OAM is lower than that for displayed OBJ, the bigger the non-displayed OBJ's size is, the less efficient the rendering will be. Please be aware of this problem.

6.3.2 Character Data Mapping

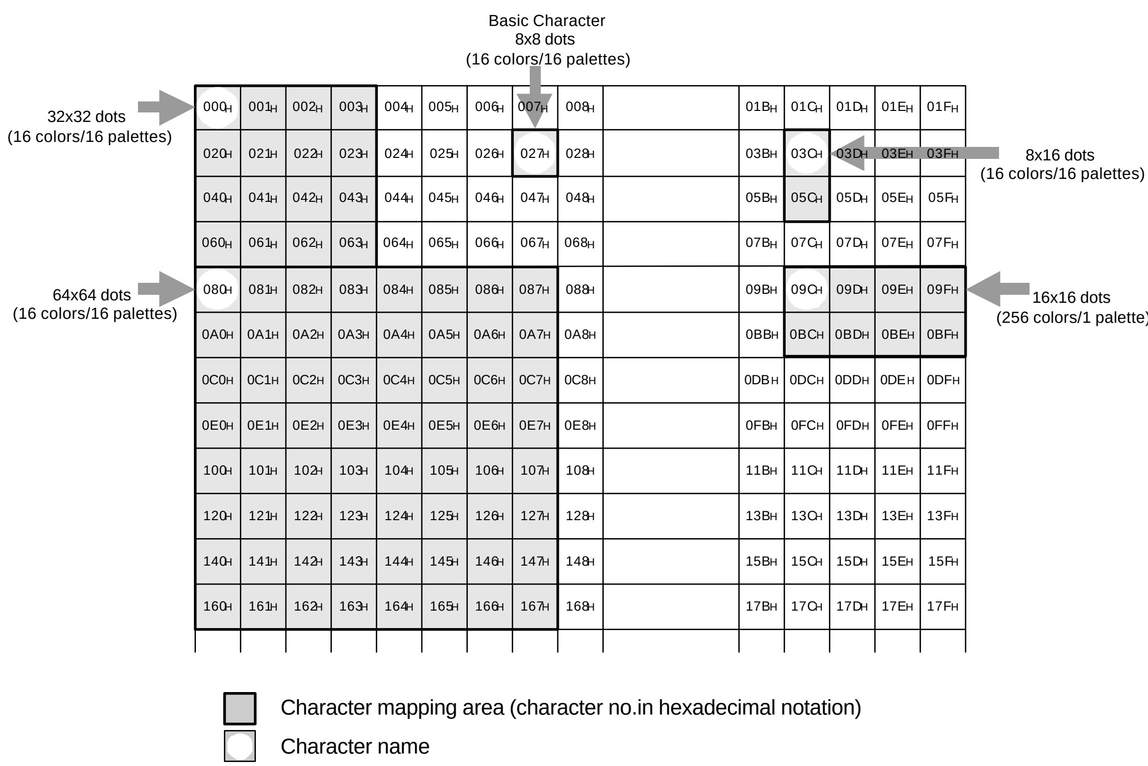
With OBJ character data, the basic character is 8 x 8 dots, and characters between 8 x 8 and 64 x 64 dots can be handled (total of 12 types). The base address of OBJ character data is a fixed VRAM base address. The OBJ character data capacity allocated is either 32 Kbytes or 16 Kbytes, depending on the BG mode (see 5.1.2 "VRAM Memory Map").

There are 2 types of mapping to the character area, and they can be specified in bit [d06] of the DISPCNT register.

OBJ is managed by character numbers that are divided by 16 half word starting with OBJ character database address. 16 half word is a required capacity to define 1 basic character of 16 colors x 16 palettes. 32 half word is a required capacity to define 1 basic character of 256 colors x 1 palette.

1) VRAM 2-Dimensional Mapping for OBJ Characters

Setting the DISPCNT register bit [d06] to 0 results in the 2-dimensional mapping mode shown in the following figure.



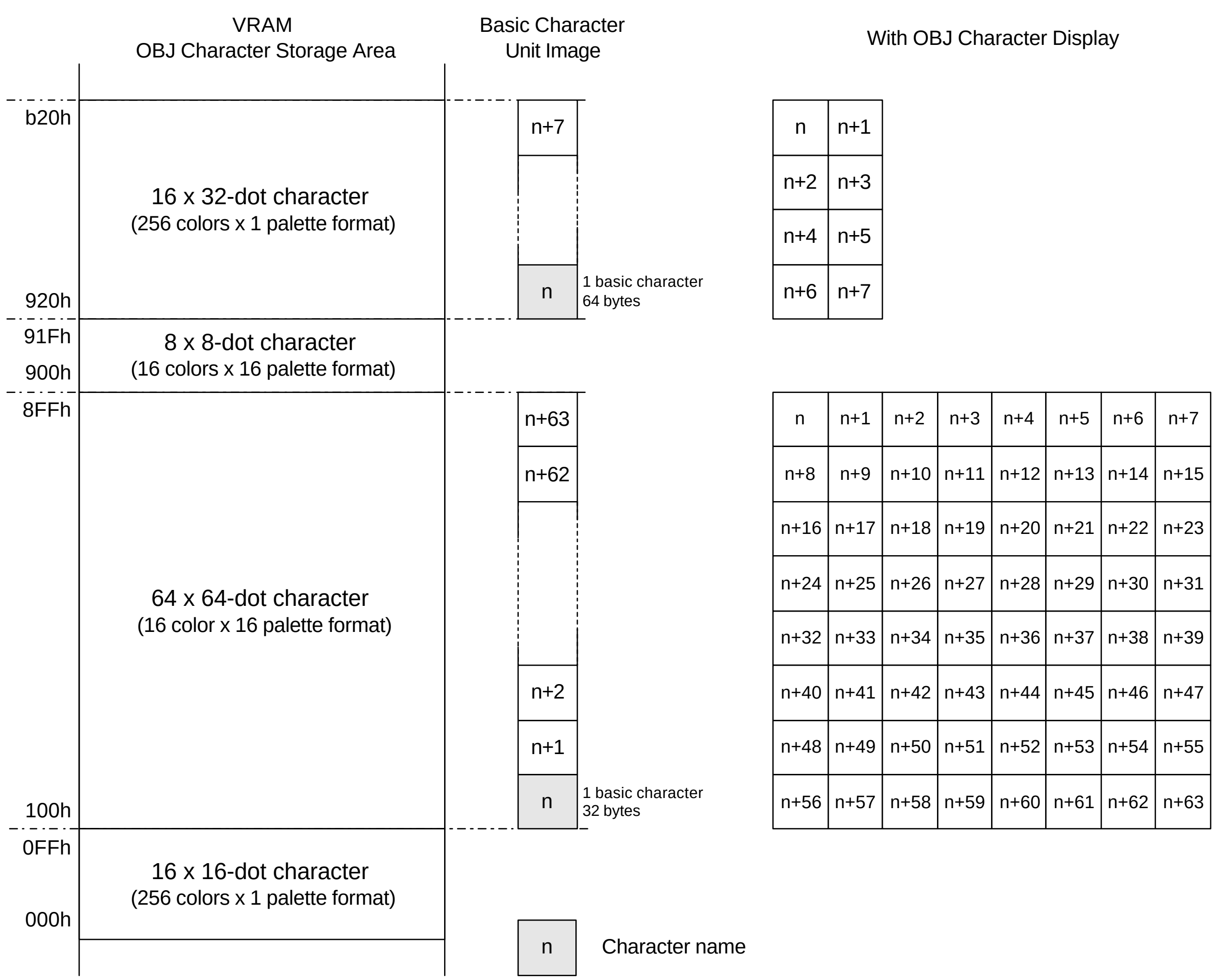
[Cautions for Character Name]

When a character of 256 colors x 1 palette is displayed during 2 dimensional mapping mode, specifying a character name is limited to even numbers (see OBJ attribute 2 of OAM). So, in most cases when defining a character of 256 colors x 1 palette during 2 dimensional mapping mode, you define it so that a character name is an even number.

2) VRAM 1-Dimensional Mapping for OBJ Characters

Setting DISPCNT register bit [d06] to 1 results in the 1-dimensional mapping mode shown in the following figure.

The data that comprise a character are stored in contiguous addresses.



6.3.3 OAM

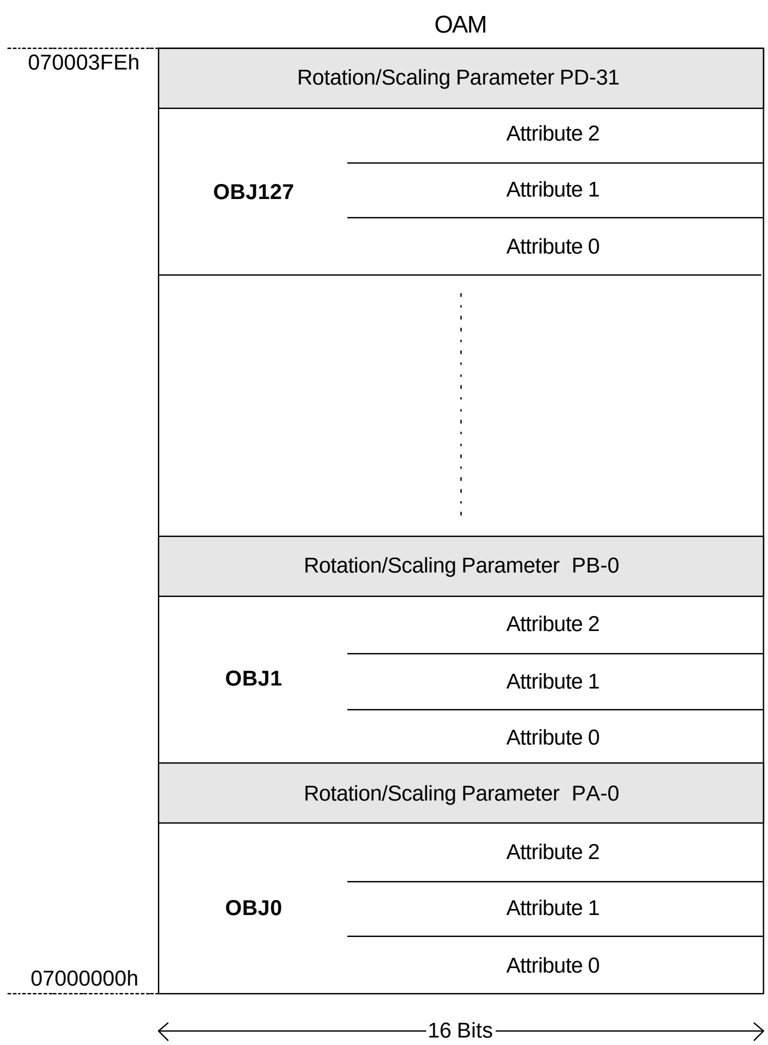
OBJs are displayed by placing data in OAM.

OBJ data for 128 OBJs can be written to internal CPU OAM (addresses 07000000h-070003FFh), and 128 OBJ characters of an arbitrary size can be displayed on the LCD.

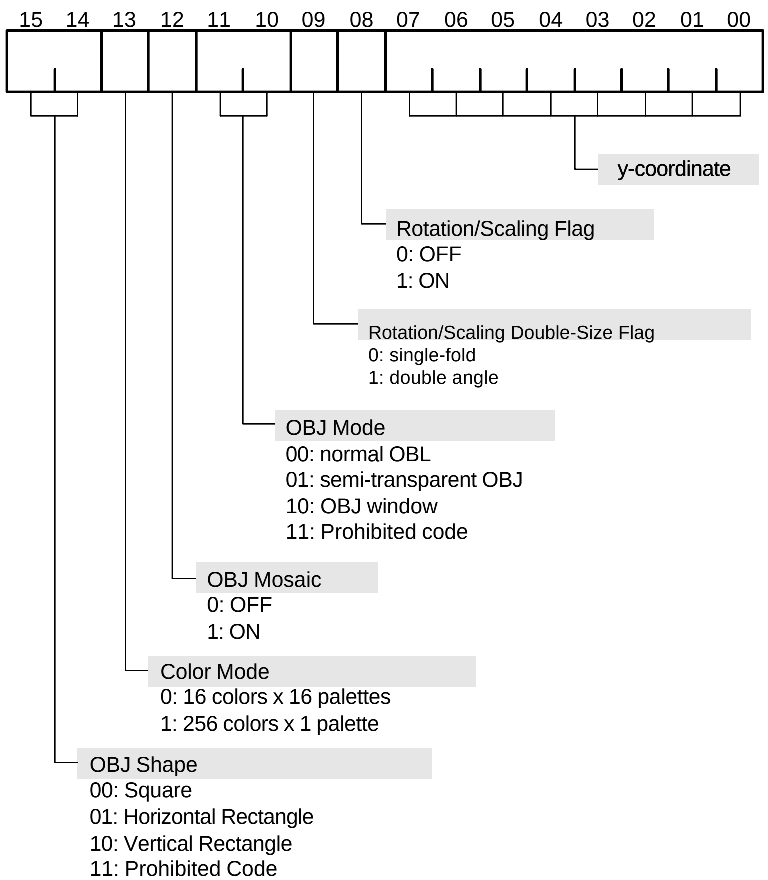
OAM Mapping

OBJ attributes occupying 48 bits x 128 OBJs can be written to OAM.

In addition, when rotation/scaling are performed for an OBJ, a total of 32 instances of rotation/scaling parameter combinations (PA, PB, PC, and PD) can be written to OAM, as shown in the following figure.



OBJ Attribute 0



[d15-14] OBJ Shape

Selects the OBJ Character Shape: Square, Horizontal Rectangle, or Vertical Rectangle.

11 is a prohibited code.

Please also refer to OBJ size specification for OBJ Attribute 1.

[d13] Color Mode Flag

Specifies whether the OBJ data format is 16 colors x 16 palette mode or 256 colors x 1 palette mode.

[d12] OBJ Mosaic Flag

Turns mosaic for OBJs on and off.

[d11-10] OBJ Mode

Specifies whether an OBJ is a normal OBJ or a semitransparent OBJ.

A normal OBJ is specified by 00, a semi-transparent OBJ by 01, and an OBJ window by 10.

A value of 11 is a prohibited code, so care should be taken to prevent this setting.

When a semi-transparent OBJ is specified, color special effects processing can be performed. For information on color special effects, see “9 Color Special Effects”.

OBJs for which an OBJ window specification is used are not displayed as normal OBJs; dots with non-zero character data are used as the OBJ window.

[d09] Rotation/Scaling Double-Size Flag

OBJs are limited in size by the OBJ field (8x8 - 64x64 dots), and the character data may surpass the boundaries of this field when rotated.

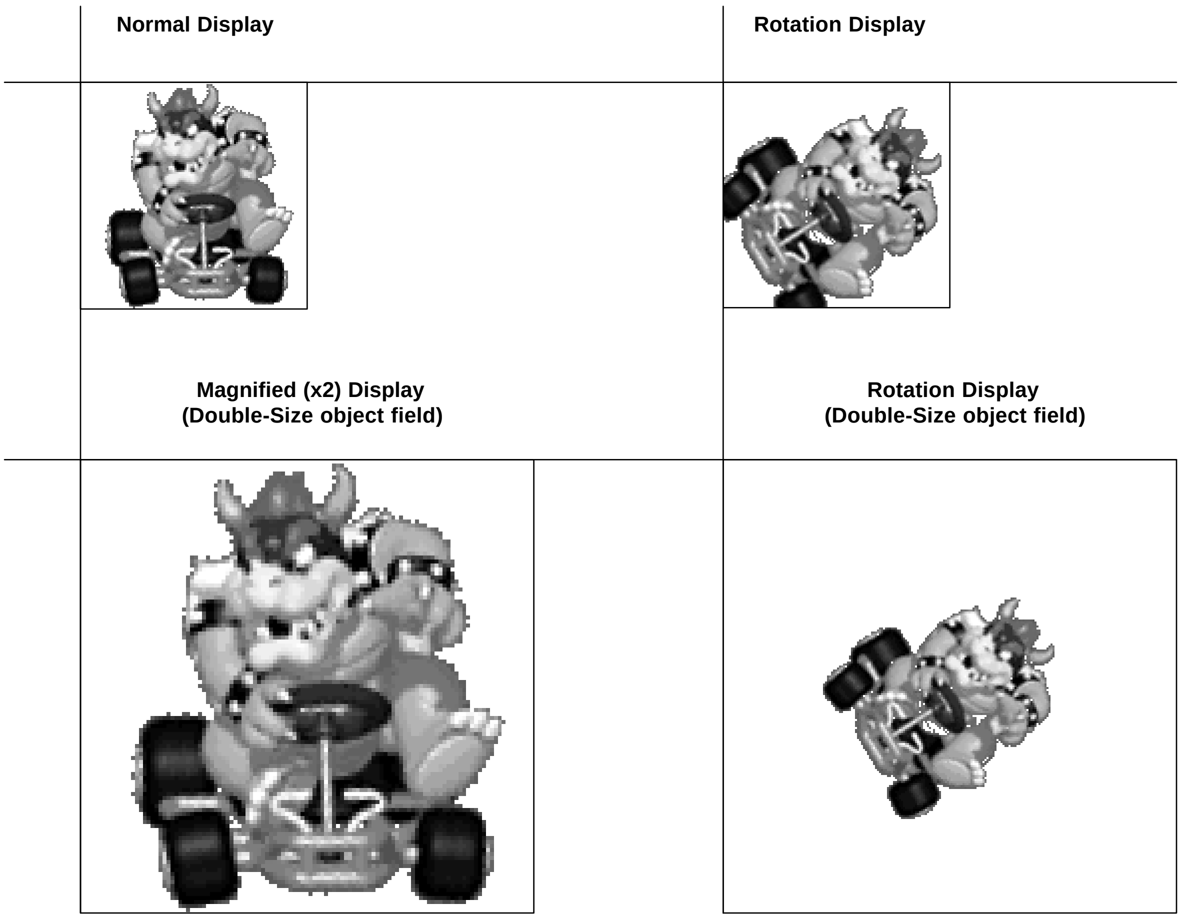
This problem can be avoided by implementing a pseudo double-size for the OBJ field, by setting the double-size flag to 1.

With this setting, the OBJ does not surpass the boundaries of the OBJ field even if the OBJ display is magnified by up to two-fold.

Example: 64x64 dot OBJ field → 128x128 dot field displayed with rotation processing. Note, however, that the OBJ display position is shifted.

With the double-size flag set to 0, display of the portion protruding from the edges is cut off.

Please refer to the following figure.



[d08] Rotation/Scaling Flag

Allows rotation processing for the OBJ to be enabled and disabled.

With the OBJ rotation/scaling feature enabled by setting this bit to 1, the maximum number of OBJs displayed per line is decreased. Please refer to the description in Section 6.3.1 on OBJ Display Capability on a Single Line [d07-00] Y-Coordinate

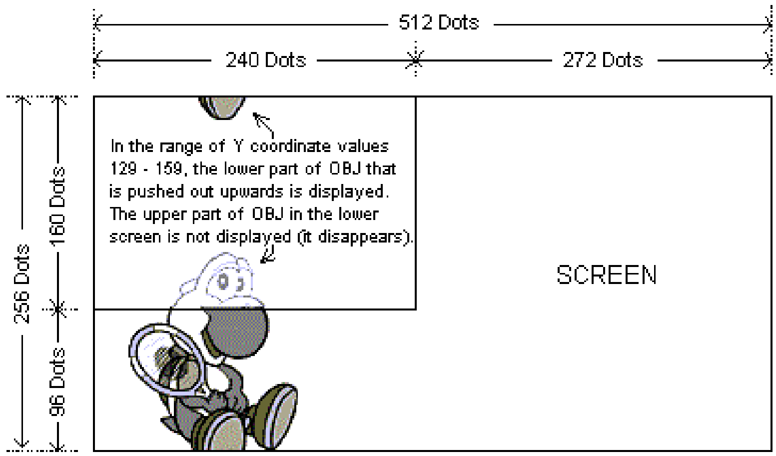
Allows the y-coordinate of the OBJ in the display screen to be specified.

[Cautions]

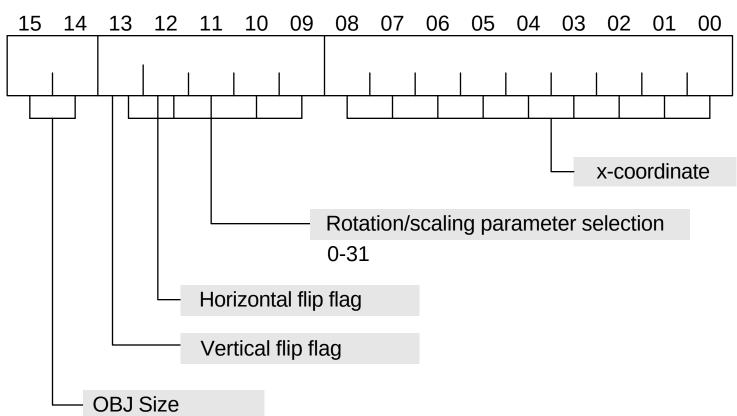
160 dots in total (0 - 159) are inside the display screen, and 96 dots in total (160 - 255) are outside the display screen (virtual screen).

When the vertical size displays a 64 dot OBJ by a double size of character, the size is 128 dots, exceeding the vertical 96 dots for the virtual screen.

Therefore, in the range of Y coordinate values of 129 - 159, the lower part of OBJ that is pushed out upwards is displayed. The upper part of OBJ in the lower screen is not displayed (see below).



OBJ Attribute 1



[d15-14] OBJ Size

Linked to the specification of the OBJ size for Attribute 0, the size for the OBJ Character is also specified. For each of the three OBJ shapes, you can set four sizes.

OBJ Shape		OBJ Size 00	OBJ Size 01	OBJ Size 10	OBJ Size 11
00	Square	A 8x8	B 16x16	C 32x32	D 64x64
01	Horizontal Rectangle	E 16x8	F 32x8	G 32x16	H 64x32
10	Vertical Rectangle	I 8x16	J 8x32	K 16x32	L 32x64
11		Prohibited Code			

[d13] [d12] Vertical and Horizontal Flip Flags

Allows the OBJ to be flipped horizontally and vertically.

A normal display is produced by a setting of 0 and a flip display by a setting of 1.

When the rotation/scaling flag ([d08] of OBJ Attribute 0) is enabled, these bits also can be used as the high-order bits of the rotation/scaling parameter selection.

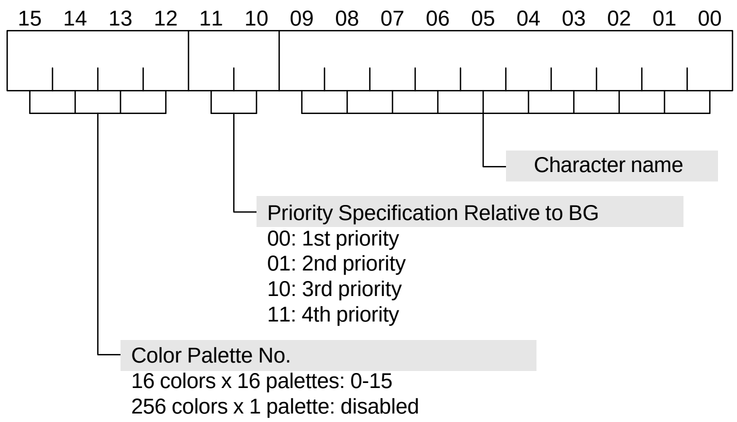
[d13-09] Rotation/Scaling Parameter Selection

The parameters used in OBJ rotation/scaling processing are selected from the 32 parameters registered in OAM.

[d08-00] X-Coordinate

Specifies the x-coordinate of the OBJ on the display screen in the range of 0~511.

OBJ Attribute 2



[d15-12] Color Palette No.

When 16 colors x 16 palette format is specified in the color mode bit, these bits specify 1 of the 16 palettes to apply to the character data.

When 256 colors x 1 palette format is specified in the color mode bit, these bits are disabled.

[d11-10] Priority Relative to BG

Specifies the display priority of the OBJ relative to BG. For information on priority, see section 6.4, Display Priority of OBJ and BG.

[d09-00] Character Name

Writes the number of the basic character located at the start of the OBJ character data mapped in VRAM. (See section 6.3.2, Character Data Mapping).

<u>16 colors x 16 palettes (color mode=1)</u>

Allows selection of 1,024 characters.

<u>256 colors x 1 palette (color mode=0)</u>

Allows selection of 512 characters.

Bit 0 fixed at 0 in 2-dimensional mapping mode.

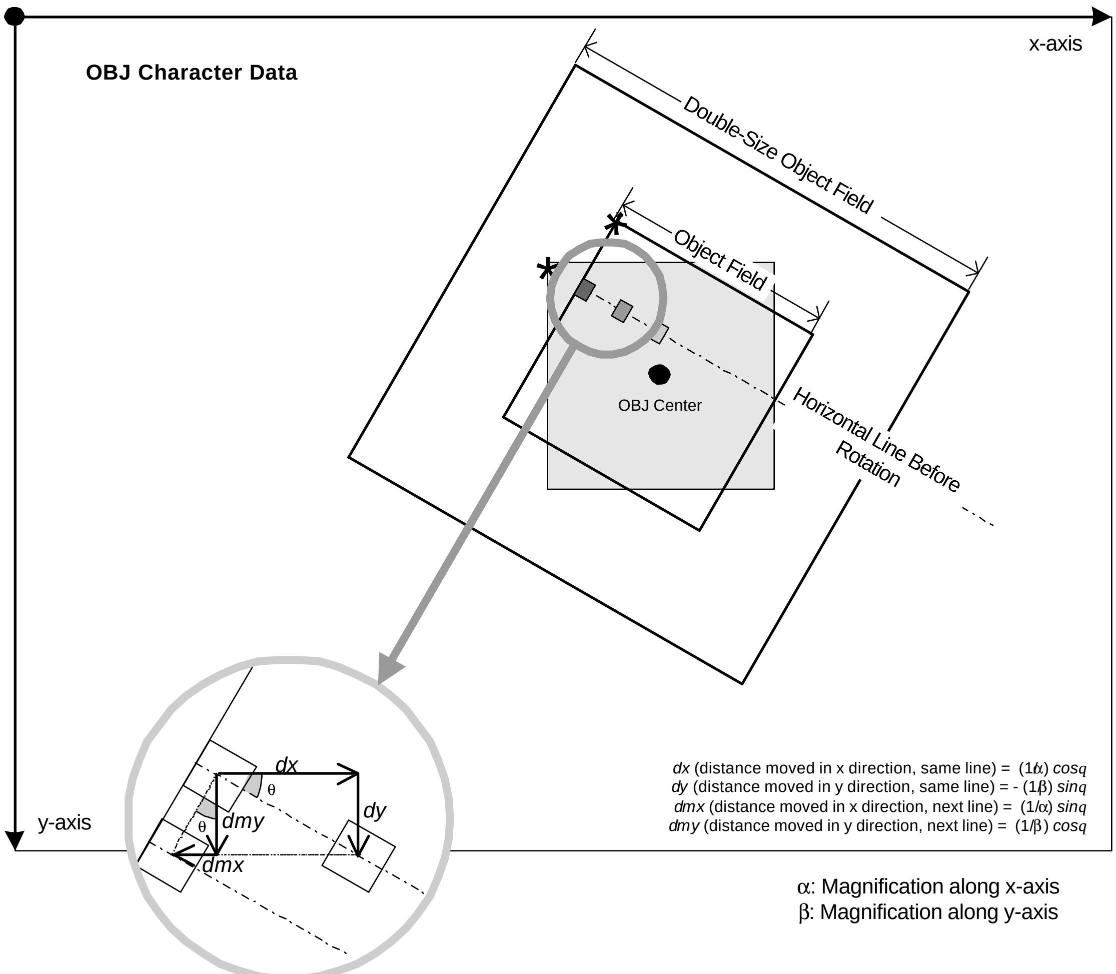
BG Mode is 3~5 (Bitmap Mode)

OBJ character data RAM is halved to 16 KB, so character name numbers 0-511 are disabled and numbers 512 and greater are used.

6.3.4 OBJ Rotation/Scaling Feature

The rotation and scaling feature for OBJ is essentially the same as that for BG.

OBJ Character Data Referenced with Rotation



When an OBJ is displayed, the OBJ character data are referenced horizontally, beginning from the left-uppermost position. Rotation display can be achieved by adding an angle to the reference direction. The center of rotation is fixed at the center of the OBJ field. If a reference point surpasses the specified OBJ size, it becomes transparent.

Operations Used in OBJ Rotation/Scaling Processing

1. Specify the rotation/scaling parameter number to be applied in OBJ Attribute 1 of the OAM.

2. The image-processing circuit sums the increases in the x direction (dx, dy) in relation to the center of rotation (OBJ field center), which serves as reference point, to calculate the x-direction coordinates.

3. When the line is advanced, the increases in the y-direction (dmx, dmy) in relation to the reference point, are summed to calculate the coordinate of the starting point for rendering the next line. The processing in step 2) above, is then performed.

Rotation/Scaling Parameters

Specifies the direction of character data reference in OBJ rotation/scaling processing. (See the following chapter for more information.)

The values set for PA, PB, PC, and PD are signed, fixed-point numbers (8-bit fractional portion, 7-bit integer portion, 1-bit sign, for a total of 16 bits).

These 4 parameters are used together as a single group, which can be placed in any of 32 areas in OAM.

	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PA	dx: distance moved in x direction along same line															
PB	dmx: distance moved in x direction along next line															
PC	dy: distance moved in y direction along same line															
PD	dmy: distance moved in y direction along next line															

6.4 Display Priority of OBJ and BG

1) Priority Among BGs

Priority among BGs can be set to any of 4 levels.

When BGs have the same priority setting, the BG with the lowest BG number is given priority.

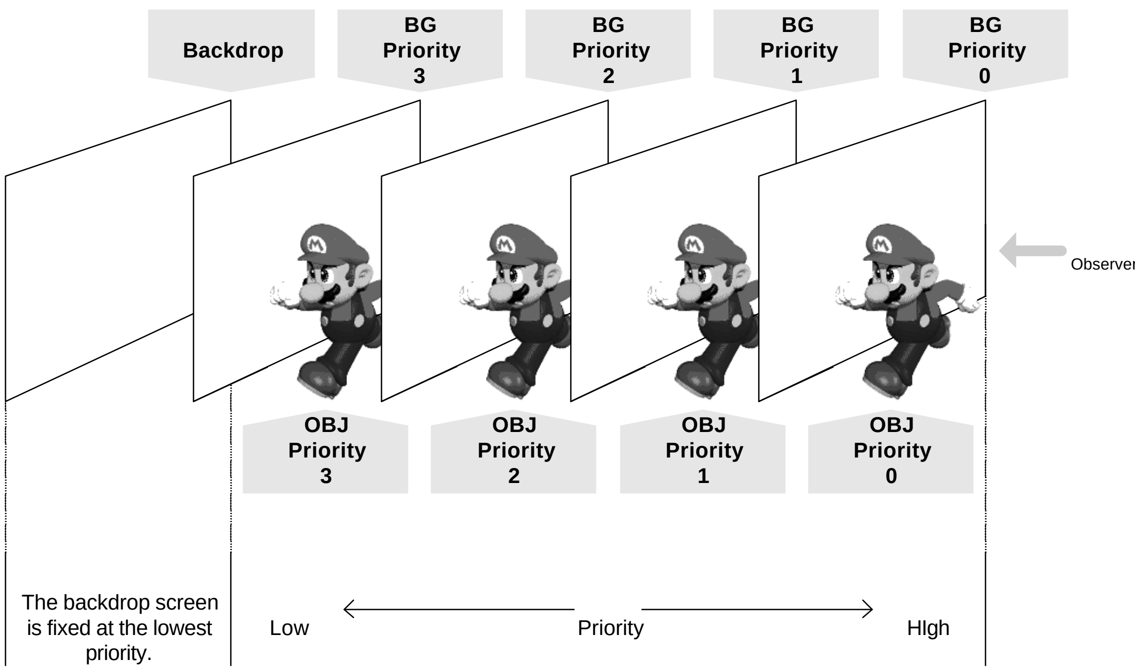
2) Priority Among OBJs

Priority among OBJs can be set to any of 4 levels.

When OBJs have the same priority setting, the OBJ with the lowest OBJ number is given priority.

3) Priority Among BGs and OBJs

The priority of each OBJ in relation to the BG can be set to 4 levels. Please refer to the following figure.



[Cautions for priority]

When orders of OBJ number and OBJ priority are reversed, the display is not right if BG is between the OBJs. Please be cautious not to let this situation occur.

Examples of when display is not right:

OBJ-No.0 (OBJ priority 2)
BG (BG priority 1)
OBJ-No.1 (OBJ priority 0)

7 Color Palettes

7.1 Color Palette Overview

The LCD unit of AGB can display 32 levels of red, 32 levels of green, and 32 levels of blue, for a total of 32,768 colors.

The number of colors that can be displayed at once varies with the BG mode. See “5.1.1 BG Modes”. Color palettes are used in defining character-format BGs and OBJs.

[Note]

Bitmap-format BG modes 3 and 5 are not palette formats. See “6.2 Bitmap Mode BG (BG Modes 3-5)”.

Color palettes come in the following two forms.

1) 16 Colors x 16 Palettes

This mode provides 16 color palettes, each consisting of 16 colors.

Color 0 for OBJ and BG palettes is forcibly allocated to transparent (color specification disabled).

2) 256 Colors x 1 Palette

This mode allocates all 256 of its colors to 1 palette.

Color data are represented by 15 bits (5 for Red, 5 for Green, and 5 for Blue). Colors can be selected from the total of 32,768.

OBJ color 0 and BG color 0 are forcibly allocated to transparent (color specification disabled).

3) Color 0 Transparency

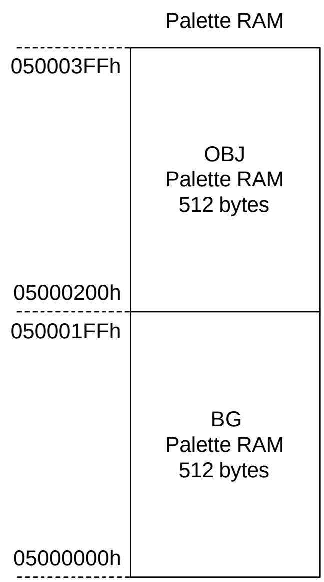
Color 0 transparency is used to render the pixels of low-priority OBJs or BGs as transparent.

<u>The color specified for color 0 of BG palette 0 is applied to the backdrop, which has the lowest priority.</u>

7.2 Color Palette RAM

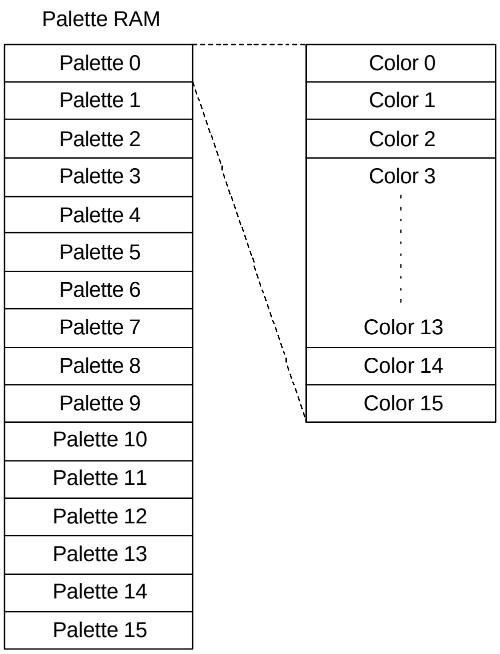
OBJs and BGs use separate palettes.

The size of palette RAM is large enough (512 bytes) to hold data (16-bit) for up to 256 colors (of 32,768) that can be specified. The memory map of the OBJ and BG palettes is shown in the follow figure.

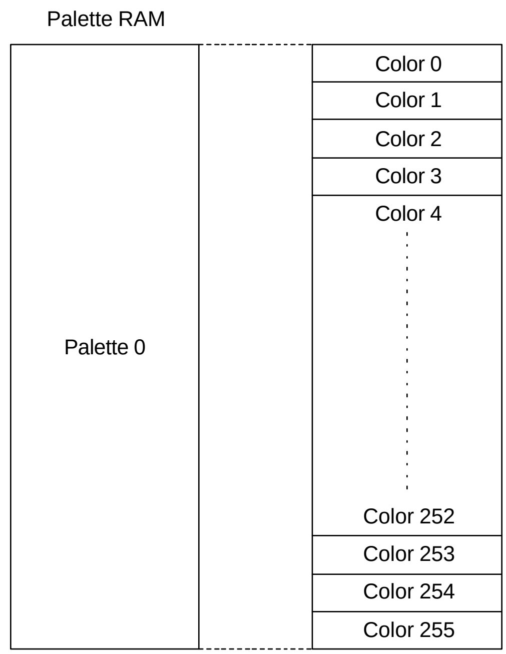


Either of 2 modes (16 colors x 16 palette and 256 colors x 1 palette) can be selected for OBJ and BG. Palette RAM for these modes is referenced as shown in the following figure.

16 Colors x 16 Palettes

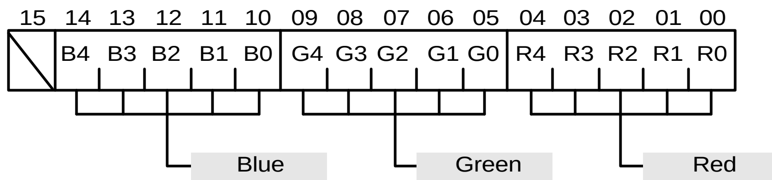


256 Colors x 1 Palette



7.3 Color Data Format

Allows 1 of 32,768 colors to be specified.



8 Window Feature

The AGB system can display 2 windows simultaneously.

Display of the areas inside and outside the windows can be separately turned on and off.

In addition, scrolling and color special effects such as rotation, α blending, and fade-in/fade-out can be performed for each window.

8.1 Window Position Setting

The Window Position Setting specifies the upper-left and lower-right coordinates of a rectangular area.

These settings specify the window's position and size.

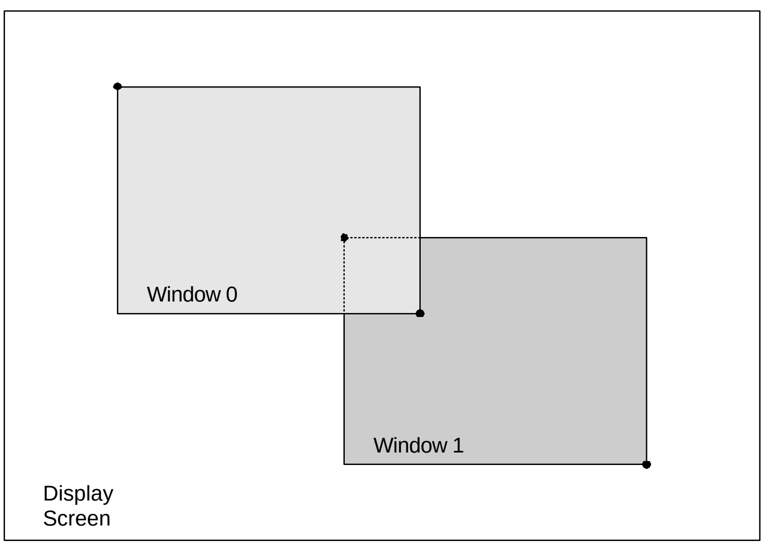
When a non-rectangular window is displayed, the values of these registers are updated during H-blanking intervals.

Address	Register	15–08	07–00	Attributes	Initial Value
040h 042h	WIN0H WIN1H	Left-upper x-coordinate of window	Right-lower x-coordinate of window	W	0000h

Address	Register	15–08	07–00	Attributes	Initial Value
044h 046h	WIN0V WIN1V	Left-upper y-coordinate of window	Right-lower y-coordinate of window	W	0000h

Window Display Example

Window 0 has a higher display priority than Window 1.



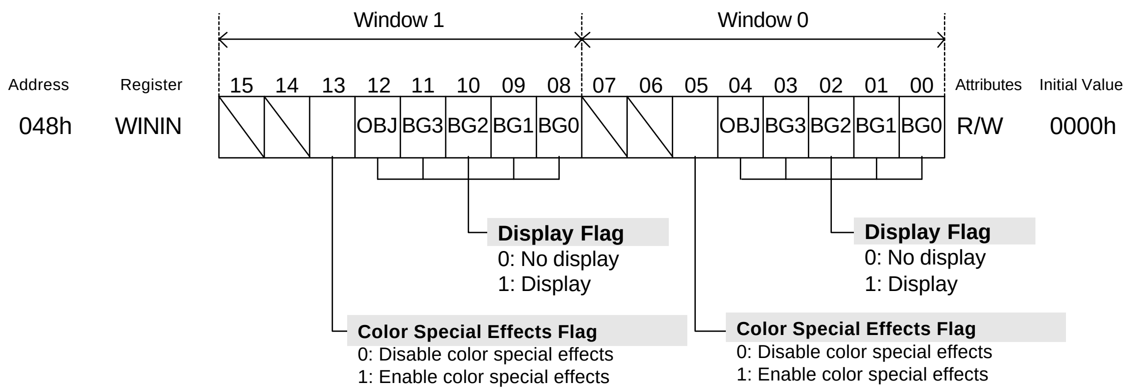
8.2 Window Control

The window control registers control operations such as turning window display on and off.

However, the master window display flag of the DISPCNT register has a higher priority than the WININ and WINOUT registers. For information concerning the DISPCNT register, see “Chapter 5 Image System".

1) Control of Inside of Window

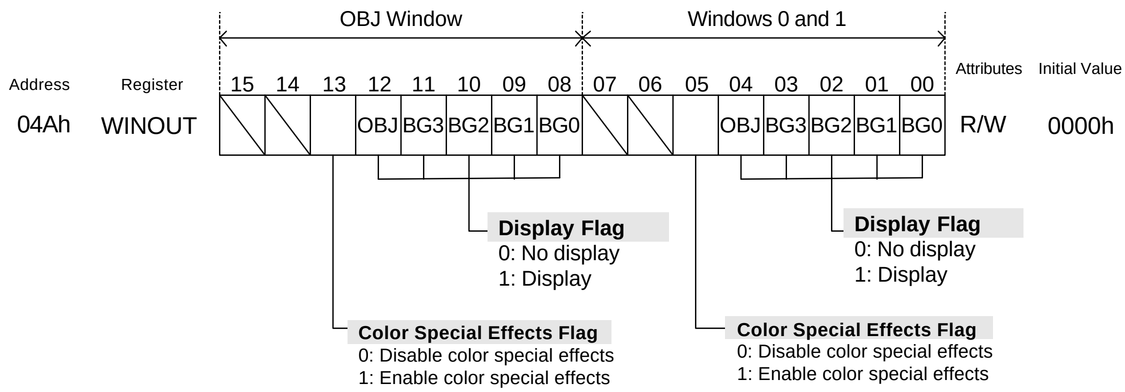
The WININ register controls display of the area inside windows 0 and 1.
The high-order bits (d13-8) control Window 1, while the low-order bits (d5-0) control Window 0.



2) Control of Outside of Window and Inside of OBJ Window

The WINOUT register controls display of the area outside the window. It controls both windows 0 and 1.

In addition, it controls display of the area inside the OBJ window.



WININ [d12-08][d04-00], WINOUT[d12-08][d04-00] Display Flags

Turns display of the OBJ and BG 3-0 on and off.

A setting of 0 turns display off, and 1 turns display on.

WININ [d13][d05], WINOUT[d13][d05] Color Special Effects Flags

A setting of 0 disables color special effects; 1 enables them. For information on color special effects, see “9 Color Special Effects”.

9 Color Special Effects

The AGB provides the following color special effects. The area where these effects are applied can be limited using a window.

1) a Blending

Performs arithmetic operations on 2 selected surfaces and implements processing for 16 levels of semi-transparency.

2) Fade-in/Fade-out

Performs arithmetic operations on 1 selected surface and implements processing for 16 levels of brightness.

9.1 Selection of Color Special Effects

The types of color special effects and the target pixels, are determined by the BLDMOD register.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
050h	BLDMOD			BD	OBJ	BG3	BG2	BG1	BG0			BD	OBJ	BG3	BG2	BG1	BG0	R/W	0000h

Bits 13–08: 2nd Target Pixel
Bits 07–06: Color Special Effects Setting
Bits 05–00: 1st Target Pixel

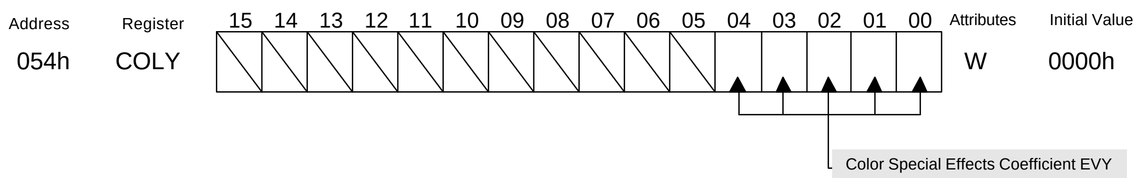
Although color special effects are specified by the BLDMOD register, for α blending, which involves processing between surfaces, the 2 target surfaces must have suitable priorities.

In addition, semi-transparent OBJs are individually specified in OAM, and color special effects for the OBJ as a whole, are specified in the BLDMOD register. These specifications are summarized in the following table.

BLDMOD		Type	Color Special Effects Processing
d07	d06		
0	0	No special effects	Normally, color special effects processing is not performed. 16-level semi-transparency processing (α blending) is performed only when a semi-transparent OBJ is present and is followed immediately by a 2nd target screen.
0	1	α blending (Semi-transparency processing)	If the 1st target screen is followed immediately by a 2nd target screen, 16-level semi-transparency processing (α blending) is performed. The bits of the backdrop of the 1st target screen should be turned off ([d05]=0). When OBJ = 1 for the 1st target pixel, processing is executed for all OBJs regardless of the OBJ type. When OBJ=0, processing is executed only if the OBJ is semi-transparent.
1	0	Brightness Increase	Gradually increases brightness for 1st target screen. The entire screen can gradually be made whiter by setting all bits of the specification for the 1st target screen to 1. When OBJ=1 for the 1st target screen, processing for increased brightness is executed only for normal objects. If a semi-transparent OBJ is the 1st target screen, α blending processing is always executed.
1	1	Brightness Decrease	Brightness is gradually decreased for the 1st target screen. The entire screen can gradually be made blacker by setting all bits of the specification for the 1st target screen to 1. When OBJ=1 for the 1st target screen, processing for decreased brightness is performed only for normal objects. If a semi-transparent OBJ is the 1st target screen, α blending processing is always executed.

9.2 Color Special Effects Processing

Coefficients for Color Special Effects



Coefficients used in α blending processing are specified in EVA and EVB of the COLEV register.

The coefficient used in processing brightness changes is specified in EVY of the COLY register.

The values of EVA, EVB, and EVY are numbers less than 1 and are obtained by multiplying 1/16 by an integer.

EVA, EVB, EVY					Coeff.	EVA, EVB, EVY					Coeff.
0	0	0	0	0	0	0	1	0	0	0	8/16
0	0	0	0	1	1/16	0	1	0	0	1	9/16
0	0	0	1	0	2/16	0	1	0	1	0	10/16
0	0	0	1	1	3/16	0	1	0	1	1	11/16
0	0	1	0	0	4/16	0	1	1	0	0	12/16
0	0	1	0	1	5/16	0	1	1	0	1	13/16
0	0	1	1	0	6/16	0	1	1	1	0	14/16
0	0	1	1	1	7/16	0	1	1	1	1	15/16
						1	X	X	X	X	16/16

The color special effects arithmetic expressions that use the coefficients are shown below.

1. a Blending (16 levels of semi-transparency) Operations

Display color (R) = 1st pixel color (R) ×EVA + 2nd pixel color (R)×EVB
Display color (G) = 1st pixel color (G) ×EVA + 2nd pixel color (G) ×EVB
Display color (B) = 1st pixel color (B) ×EVA + 2nd pixel color (B) ×EVB

2. Brightness Increase Operations

Display color (R) = 1st pixel (R) + (31 - 1st pixel (R)) ×EVY
Display color (G) = 1st pixel (G) + (63 - 1st pixel (G)) ×EVY
Display color (B) = 1st pixel (B) + (31 - 1st pixel (B)) ×EVY

3. Brightness Decrease Operations

Display color (R) = 1st pixel (R) - 1st pixel (R) ×EVY
Display color (G) = 1st pixel (G) - 1st pixel (G) ×EVY
Display color (B) = 1st pixel (B) - 1st pixel (B) ×EVY

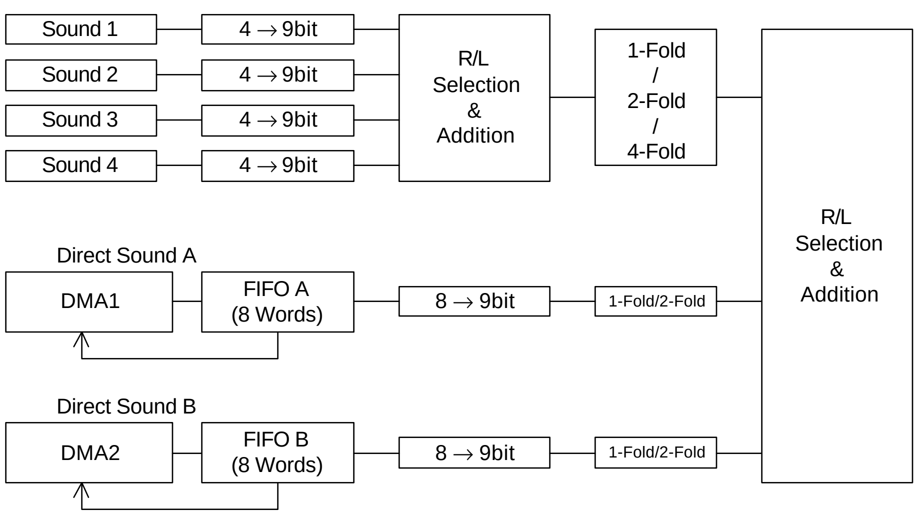
10 Sound

In addition to 4 channels of CGB-compatible sound, AGB has 2 channels of direct sound.

1. **Direct Sounds A and B**
   Provides playback of linear 8-bit audio data.
   Uses the timer and DMA.
2. **Sound 1**
   Allows generation of rectangular waveforms with sweep (frequency change) and envelope (volume change) functions.
3. **Sound 2**
   Allows generation of rectangular waveforms with envelope functions.
4. **Sound 3**
   Allows playback of any waveform recorded in waveform RAM.
   Waveform RAM in AGB has double the capacity of that in CGB.
5. **Sound 4**
   Can generate white noise with the envelope function.

The synthesis ratio of sounds 1-4 to direct sound can be specified.

10.1 Sound Block Diagram



10.2 Direct Sounds A and B

Direct sounds have 2 channels, A and B. Linear 8-bit audio data can be played back.

The audio data are set to a bias level of 00h and are 8-bit data (+127 to -128), obtained by 2's complement.

Audio data are transferred sequentially to the sound FIFO (8-word capacity), using the sound FIFO transfer mode of DMA 1 and 2.

The sampling rate can be set to an arbitrary value using timers 0 and 1.

Sound FIFO Input Register

Address	Register	15–08	07–00	Attributes	Initial Value
0A0h 0A4h	SGFIFOA_L SGFIFOB_L	Sound Data 1	Sound Data 0	W	-

Address	Register	15–08	07–00	Attributes	Initial Value
0A2h 0A6h	SGFIFOA_H SGFIFOB_H	Sound Data 3	Sound Data 2	W	-

Sound Data

All sounds are PWM modulated (refer to 10.8 "Sound PWM Control") at the final portion of the Sound Circuit. Therefore, if you match the 8 bit audio data sampling frequency and the timer settings with the PWM modulation sampling frequency, a clean sound can be produced.

The following operations are repeated for direct sound.

Preparing to Use Direct Sound

1. Using sound control register SGCNT0_H (refer to 10.7 "Sound Control"), select the timer channel to be used (0 or 1).
2. Using sound control register SGCNT0_H, do a 0 clear with FIFO A and FIFO B, and initialize the sequencer.
3. In cases of producing a sound immediately after starting the direct sound, write the first 8 bits of linear audio data to the FIFO with a CPU write.
4. Specify the transfer mode for DMA 1 or 2 (see 12.2 "DMA 1 and 2").
5. Specify the direct sound outputs settings in the sound control register.
6. Start the timer.

With the preceding preparations, direct sound is executed as follows.

Direct Sound Execution

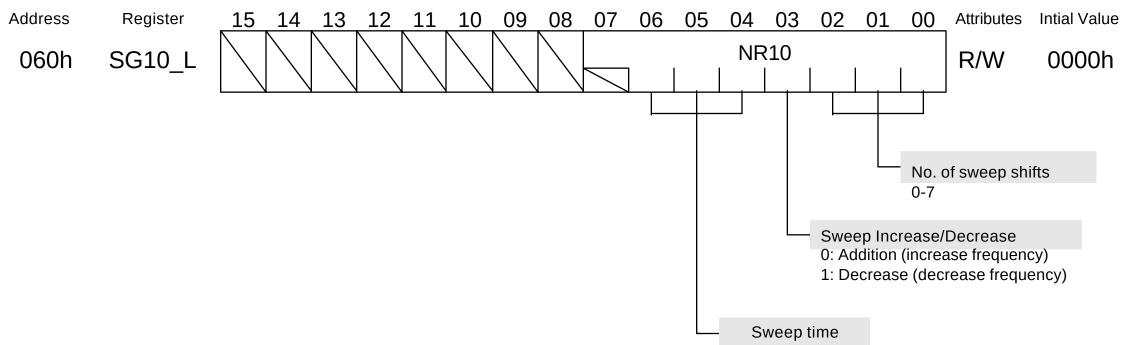
1. When the specified timer overflows due to a count up, the audio data are passed from the FIFO to the sound circuit.
2. If 4 words of data remain in the FIFO as the transfer count progresses, the FIFOs for direct sounds A and B output a data transfer request to the specified DMA channel.
3. If the DMA channel receiving the request is in sound FIFO transfer mode, 4 words of data are provided to the sound FIFO (the DMA WORD COUNT is ignored).

The preceding is repeated starting from 1.

10.3 Sound 1

Sound 1 is a circuit that generates rectangular waveforms with sweep (frequency change) and envelope (volume change) functions.

The contents of NR10, NR11, NR12, NR13, and NR14 for Sound 1, conform with those of CGB.



SG10_L [d06-04] Sweep Time

These bits specify the interval for frequency change.

Setting	Sweep Time
000	Sweep OFF
001	1/f128 (7.8 ms)
010	2/f128 (15.6 ms)
011	3/f128 (23.4 ms)
100	4/f128 (31.3 ms)
101	5/f128 (39.1 ms)
110	6/f128 (46.9 ms)
111	7/f128 (54.7 ms)

(f128=128Hz)

SG10_L [d03] Sweep Increase/Decrease

Specifies whether the frequency increases or decreases.

When the sweep function is not used, the increase/decrease flag should be set to 1.

SG10_L [d02-00] Number of Sweep Shifts

Specifies the number of sweeps.

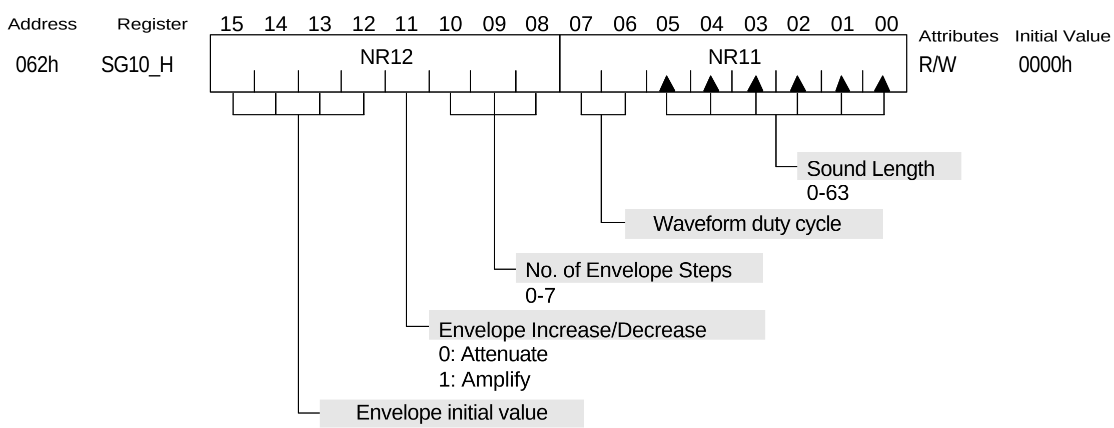
The frequency data with a single shift are determined according to the following formula, with $f_{(t)}$ signifying the frequency after a shift and $f_{(t-1)}$ the frequency before the shift.

$$f_{(t)} = f_{(t-1)} \pm \frac{f_{(t-1)}}{2^n}$$

$$f_{(0)} = \text{Initial frequency data}$$

If the addition according to this formula produces a value consisting of more than 11 bits, sound output is stopped and the Sound 1 ON flag (bit 0) of NR52 is reset.

With subtraction, if the subtrahend is less than 0, the pre-subtraction value is used. However, if the specified setting is 0, shifting does not occur and the frequency is unchanged.



SG10_H [d15-12] Envelope Initial-Value

Allows specification of any of 16 levels ranging from maximum to mute.

SG10_H [d11] Envelope Increase/Decrease

Specifies whether to increase or decrease the volume.

SG10_H [d10-08] Number of Envelope Steps

Sets the length of each step of envelope amplification or attenuation.

With n the specified value, the length of 1 step (steptime) is determined by the following formula.

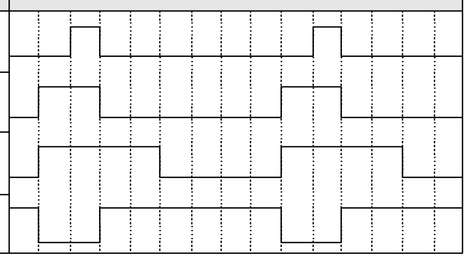
$$steptime = n \times \frac{1}{64}(\text{sec})$$

When n = 0, the envelope function is turned off.

SG10_H [d07-06] Waveform Duty Cycle

Specifies the proportion of amplitude peaks for the waveform.

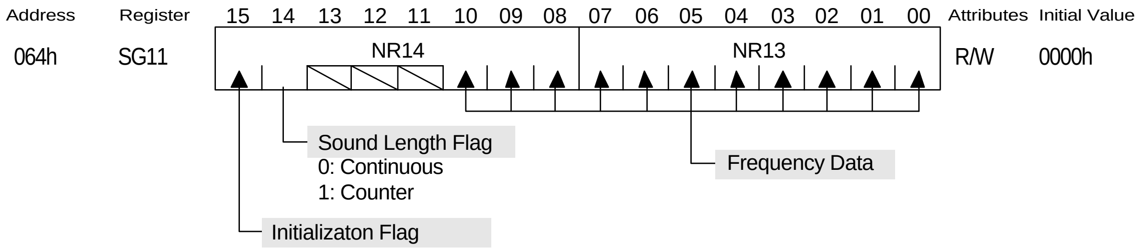
Setting	Duty Cycle	Waveform
00	12.5%	
01	25.0%	
10	50.0%	
11	75.0%	



SG10_H [d05-00] Sound Length

With st signifying the sound length, the length of the output sound is determined by the following formula.

$$time = (64 - st) \times \frac{1}{256}(\text{sec})$$



SG11 [d15] Initialization Flag

A setting of 1 causes Sound 1 to restart.
When the sweep function is used, set the initialization flag again after an interval of 8 clocks or more.

SG11 [d14] Sound Length Flag

When 0, sound is continuously output.

When 1, sound is output for only the length of time specified for the sound length in NR11.

When sound output ends, the Sound 1 ON flag of NR52 is reset.

SG11 [d10-00] Frequency Data

With fdat signifying the frequency, the output frequency (f) is determined by the following formula.

$$f = \frac{4194304}{4 \times 2^3 \times (2048 - fdat)} Hz$$

Thus, the specifiable range of frequencies is 64 to 131.1 KHz.

[Sound 1 Usage Notes]

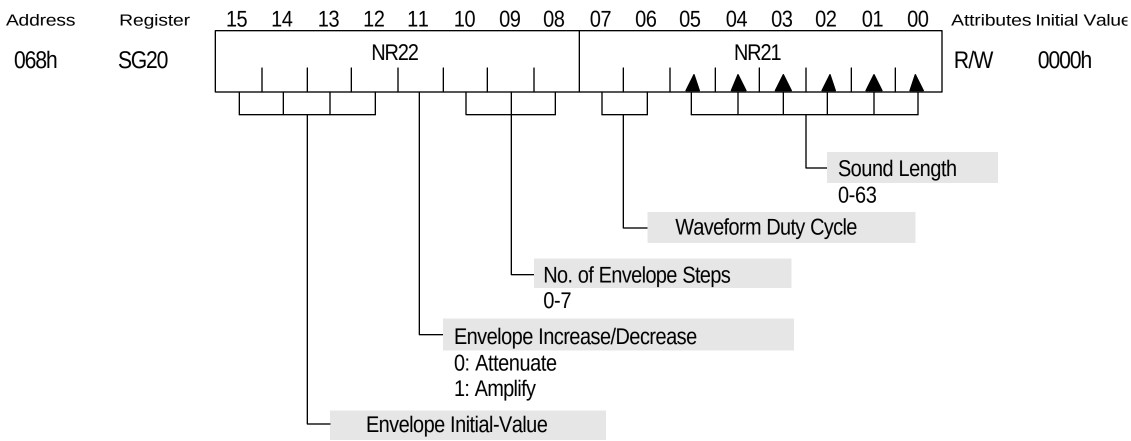
1. When the sweep function is not used, the sweep time should be set to 0 and the sweep increase/decrease flag should be set to 1.
2. If the sweep increase/decrease flag of NR10 is set to 0, the number of sweep shifts set to a non-zero value, and sweep OFF mode set, sound production may be stopped.
3. When a value is written to the envelope register, sound output becomes unstable before the initialization flag is set. Therefore, set initialization flag immediately after writing a value to the envelope register.
4. For sound 1, if you change the frequency when selecting a continuous operation mode (sound length flag of NR14 is 0), always set 0 for the data of sound length (lower 6 bits of NR11) after setting the frequency data. If 0 is not set, sound may stop prematurely.
5. If the Sound 1 initialization flag is set when the sweep function is used, always set the initialization flag again after an interval of 8 clocks or more. Unless the

initialization flag is set twice with an interval of 8 clocks or more, the sound may not be heard.

10.4 Sound 2

Sound 2 is a circuit that generates rectangular waveforms with envelope functions.

The contents of NR21, NR22, NR23, NR24 for Sound 2, conform with those of CGB.



SG20 [d15-12] Envelope Initial-Value

Allows specification of any one of 16 levels ranging from maximum to mute.

SG20 [d11] Envelope Increase/Decrease

Specifies whether volume will increase or decrease.

SG20 [d10-08] Number of Envelope Steps

Sets the length of 1 step of envelope amplification or attenuation.

With n signifying the value specified, the length of 1 step (step time) is determined by the following formula.

$$steptime = n \times \frac{1}{64}(\mathrm{sec})$$

When n=0, the envelope function is turned off.

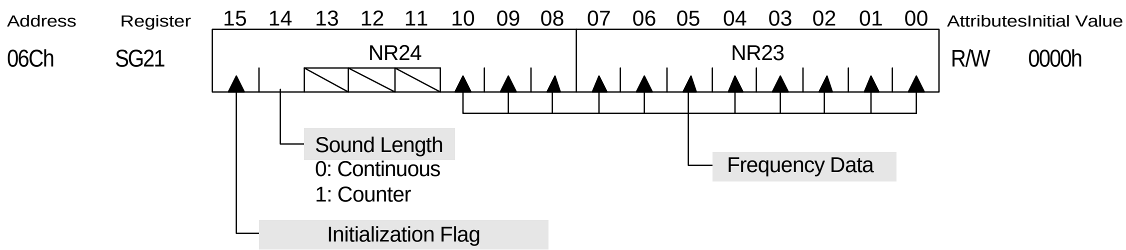
SG20 [d07-06] Waveform Duty Cycle

Specifies the proportion of waveform amplitude peaks.

SG20 [d05-00] Sound Length

With st signifying the sound length data, the length of the output sound is determined by the following formula.

$$time = (64 - st) \times \frac{1}{256} (\mathrm{sec})$$



SG21 [d15] Initialization Flag

A setting of 1 causes Sound 2 to be restarted.

SG21 [d14] Sound Length

Continuous sound output with 0; with 1, sound output only for the time specified in the sound length data of NR21.

When sound output ends, the Sound 2 ON flag of NR52 is reset.

SG21 [d10-00] Frequency Data

With fdat signifying the frequency data, the output frequency is determined by the following formula.

$$f = \frac{4194304}{4 \times 2^3 \times (2048 - fdat)} (Hz)$$

Thus, the frequency range that can be specified is 64 to 131.1 KHz.

[Sound 2 Usage Note]

1. When a value is written to the envelope register, sound output becomes unstable before the initialization flag is set. Therefore, set initialization flag immediately after writing a value to the envelope register.
2. For sound 2, if you change the frequency when selecting a consecutive operation mode (Reset the sound length flag of NR24), always set 0 for the data of sound length (lower 6 bits of NR21) after setting the frequency data. If 0 is not set, sound may stop prematurely.

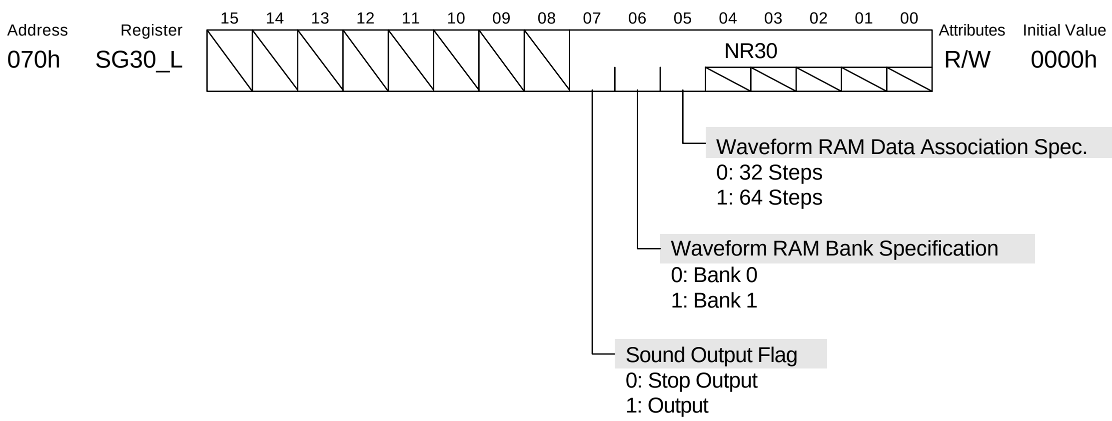
10.5 Sound 3

The Sound 3 circuit outputs arbitrary waveforms and can automatically read waveform patterns (1 cycle) in waveform RAM and output them while modifying their length, frequency, and level.

The capacity of the waveform RAM of Sound 3 in AGB (total of 64 steps) is twice that in CGB, and can be used as 2 banks of 32 steps or as 64 steps.

In addition, a new output level of 3/4 output can now be selected.

The contents of NR30, NR31, NR32, NR33, NR34 for Sound 3, add the functionalities listed above to those of CGB.



SG30_L [d07] Sound Output Flag

Sound output stops when 0; sound output occurs when 1.

SG30_L [d06] Waveform RAM Bank Specification

Two banks of waveform RAM are provided, banks 0 and 1. The Sound 3 circuit plays the waveform data in the specified bank.

When waveform RAM is accessed by the user, the bank not specified is accessed.

SG30_L [d05] Waveform RAM Data Association Specification

When 0 is specified, 32-step waveform pattern is constructed under normal operation.

With a setting of 1, the data in the bank specified by NR30 [d06] (waveform RAM bank specification) is played, followed immediately by the data in the back bank.

The front bank 32 steps and the back bank 32 steps combine to form a waveform pattern with a total of 64 steps.

SG30_H [d15] Forced 3/4 Output Level Specification Flag

With 0 specified, the output level specified in NR32 [d14-13] is used.

A setting of 1 forces a 3/4 output level regardless of the setting in NR32 [d14-13].

SG30_H [d14-13] Output Level Selection

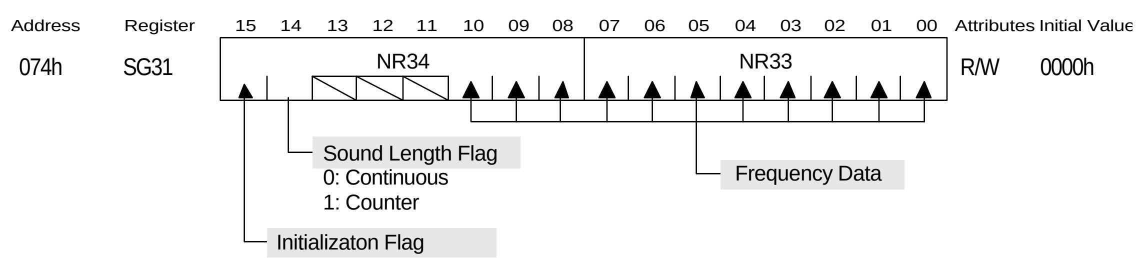
The Sound 3 output-level selections are as shown in the following table.

Setting	Output Level
00	Mute
01	Outputs the waveform RAM data unmodified.
10	Outputs the waveform RAM data with the contents right-shifted 1 bit (1/2).
11	Outputs the waveform RAM data with the contents right-shifted 2 bits (1/4).

SG30_H [d07-00] Sound Length

The sound length is determined by the following formula, with st signifying the sound-length setting.

$$time = (256 - st) \times \frac{1}{256} (\mathrm{sec})$$



SG31 [d15] Initialization Flag

When SG30_L[d07] is 1, a setting of 1 in this bit causes Sound 3 to restart.

SG31 [d14] Sound Length Flag

When 0, sound is continuously output.

When 1, sound is output for only the length of time specified for the sound length in NR31.

When sound output ends, the Sound 2 ON flag of NR52 is reset.

SG31 [d10-00] Frequency Data

With fdat signifying the frequency, the output frequency (f) is determined by the following formula.

$$f = \frac{4194304}{4 \times 2^3 \times (2048 - fdat)} Hz$$

Thus, the specifiable range of frequencies is 64 to 131.1 KHz.

[Sound 3 Usage Note]

1. When changing the frequency during Sound 3 output, do not set the initialization flag. The contents of waveform RAM may be corrupted. With sounds 1, 2 , and 4, the initialization flag can be set without problems.
2. For sound 3, if you change the frequency when selecting a consecutive operation mode (Reset the sound length flag of NR34), always set 0 for the data of sound length (NR31) after setting the frequency data. If 0 is not set, sound may stop prematurely.
3. Always set data in the waveform RAM first, when using Sound 3. If the initialization flag is set while Sound 3 is running (Sound 3 ON flag = 1), the content of the waveform RAM may be destroyed.

Waveform RAM

Waveform RAM consists of a 4-bit x 32-step waveform pattern. It has 2 banks, with [d06] of SG30_L used for bank specification.

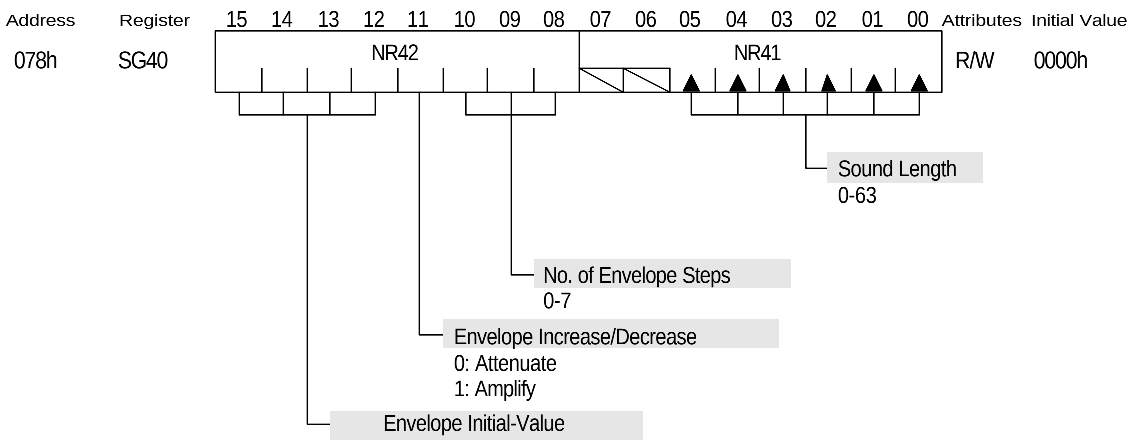
The Sound 3 circuit plays the waveform data specified by the bank setting, while the waveform RAM not specified is the waveform RAM accessed by the user.

Address	Register	15–12	11–08	07–04	03–00	Attributes	Initial Value
090h	SGWR0_L	Step 2	Step 3	Step 0	Step 1	R/W	-
092h	SGWR0_H	Step 6	Step 7	Step 4	Step 5	R/W	-
094h	SGWR1_L	Step 10	Step 11	Step 8	Step 9	R/W	-
096h	SGWR1_H	Step 14	Step 15	Step 12	Step 13	R/W	-
098h	SGWR2_L	Step 18	Step 19	Step 16	Step 17	R/W	-
09Ah	SGWR2_H	Step 22	Step 23	Step 20	Step 21	R/W	-
09Ch	SGWR3_L	Step 26	Step 27	Step 24	Step 25	R/W	-
09Eh	SGWR3_H	Step 30	Step 31	Step 28	Step 29	R/W	-

10.6 Sound 4

Sound 4 is a circuit that generates white noise with the envelope function.

The contents of NR41, NR42, NR43, and NR44 for Sound 4 conform with those of CGB.



SG40 [d15-12] Envelope Initial-Value

Allows specification of any of 16 levels ranging from maximum to mute.

SG40 [d11] Envelope Increase/Decrease

Specifies whether to increase or decrease the volume.

SG40 [d10-08] Number of Envelope Steps

Sets the length of each step of envelope amplification or attenuation.

With n the specified value, the length of 1 step (steptime) is determined by the following formula.

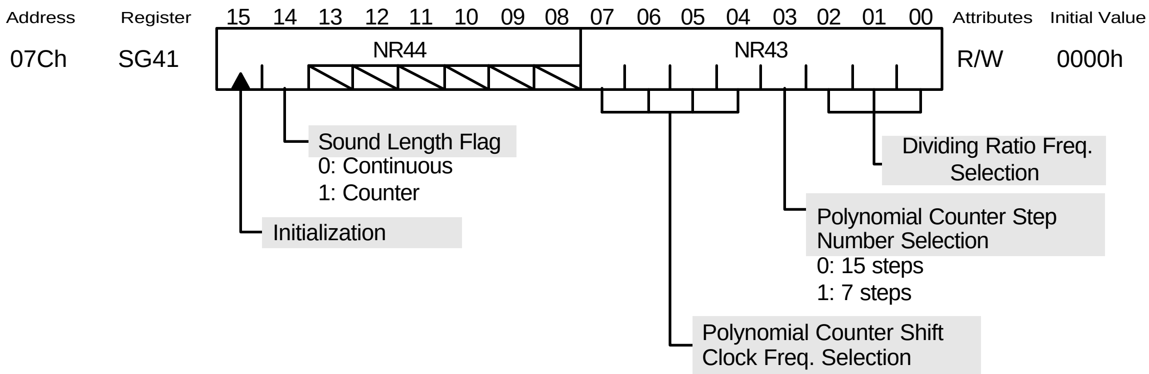
$$steptime = n \times \frac{1}{64}(\text{sec})$$

When n = 0, the envelope function is turned off.

SG40 [d05-00] Sound Length

With st signifying the sound length, the length of the output sound is determined by the following formula.

$$time = (64 - st) \times \frac{1}{256}(\text{sec})$$



SG41 [d15] Initialization Flag

A setting of 1 causes Sound 4 to be restarted.

SG41 [d14] Sound Length

Continuous sound output with 0; with 1, sound output only for the time specified in the sound length data of NR41.

When sound output ends, the Sound 4 ON flag of NR52 is reset.

SG41 [d07-04] Polynomial Counter Shift Clock Frequency Selection

With n signifying the specified value, the shift clock frequency (shiftfreq) is selected as shown in the following formula.

$$\mathit{shiftfreq} = \text{dividing ratio frequency} \times \frac{1}{2^{(n+1)}}$$

However, %1110 and %1111 are prohibited codes.

SG41 [d03] Polynomial Counter Step Number Selection

A value of 0 selects 15 steps; 1 selects 7 steps.

SG41 [d02-00] Dividing Ratio Frequency Selection

Selects a 14-step prescalar input clock to produce the shift clock for the polynomial counter.

With f=4.194304 MHz, selection is as shown in the following table.

Setting	Dividing Ratio Frequency
000	$f \times 1/2^3 \times 2$
001	$f \times 1/2^3 \times 1$
010	$f \times 1/2^3 \times (1/2)$
011	$f \times 1/2^3 \times (1/3)$
100	$f \times 1/2^3 \times (1/4)$
101	$f \times 1/2^3 \times (1/5)$
110	$f \times 1/2^3 \times (1/6)$
111	$f \times 1/2^3 \times (1/7)$

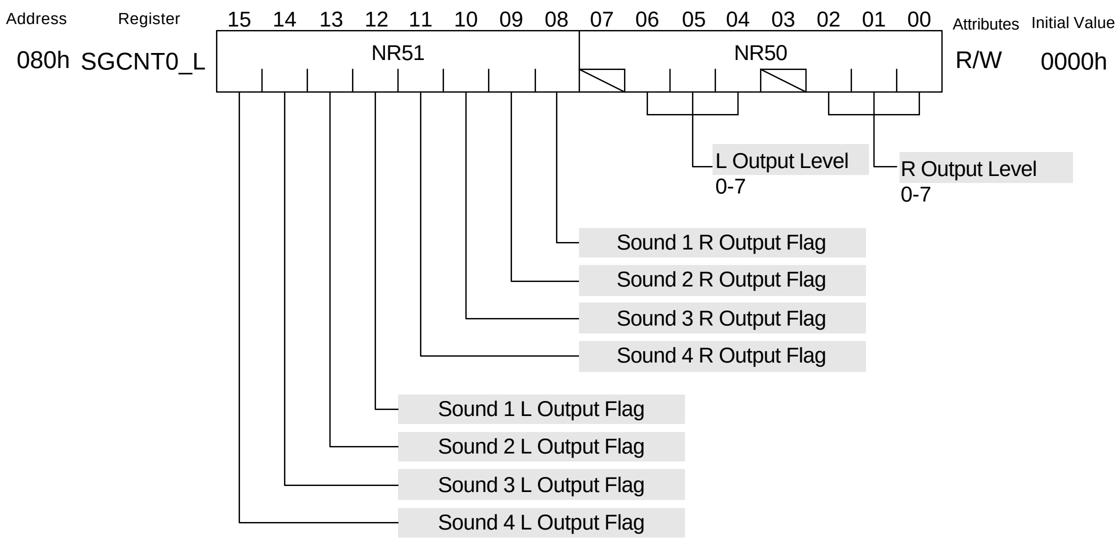
[Sound 4 Usage Note]

When a value is written to the envelope register, sound output becomes unstable before the initialization flag is set. Therefore, set initialization flag immediately after writing a value to the envelope register.

10.7 Sound Control

The output ratio for direct sound and sound can be set using the SGCNT0_H register. Final sound control can be achieved with the SGCNT0_L register.

NR50 and NR51 are each based on their counterparts in CGB.



SGCNT0_L [d15-12] L Output Flag for each Sound

No output of that sound to L when 0.

Output of that sound to L when 1.

SGCNT0_L [d11-08] R Output Flag for each Sound

No output of that sound to R when 0.

Output of that sound to R when 1.

SGCNT0_L [d06-04] L Output Level

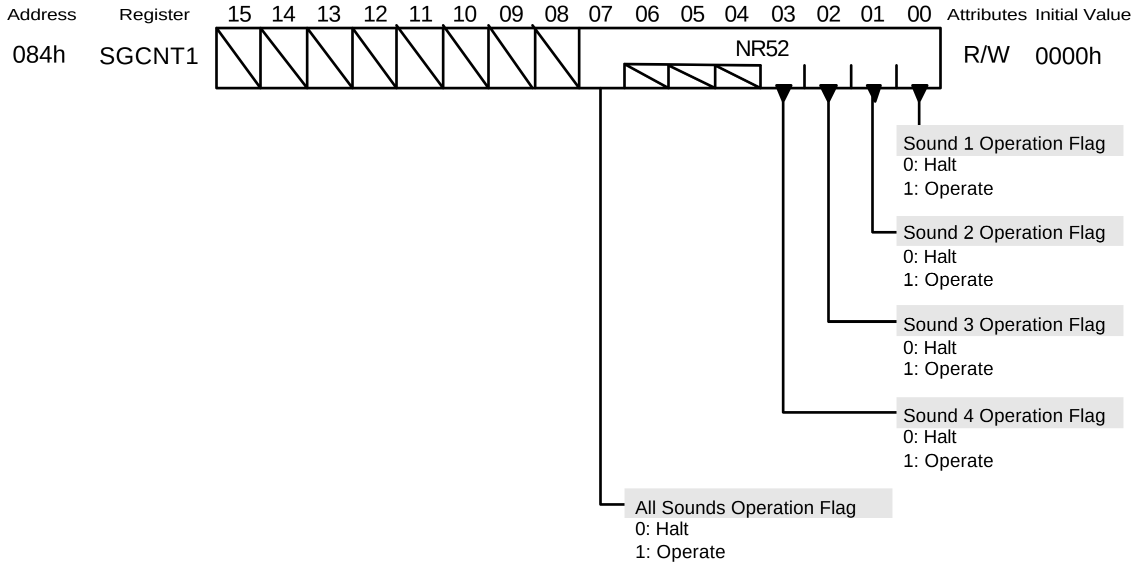
L output level can be set to any of 8 levels.

However, there is no effect on direct sound.

SGCNT0_L [d02-00] R Output Level

R output level can be set to any of 8 levels.

However, there is no effect on direct sound.



SGCNT1 [d07] All Sounds Operation Flag

The master flag that controls whether sound functions as a whole are operating.

A setting of 0 halts all sound functions including direct sound, producing a mute state.

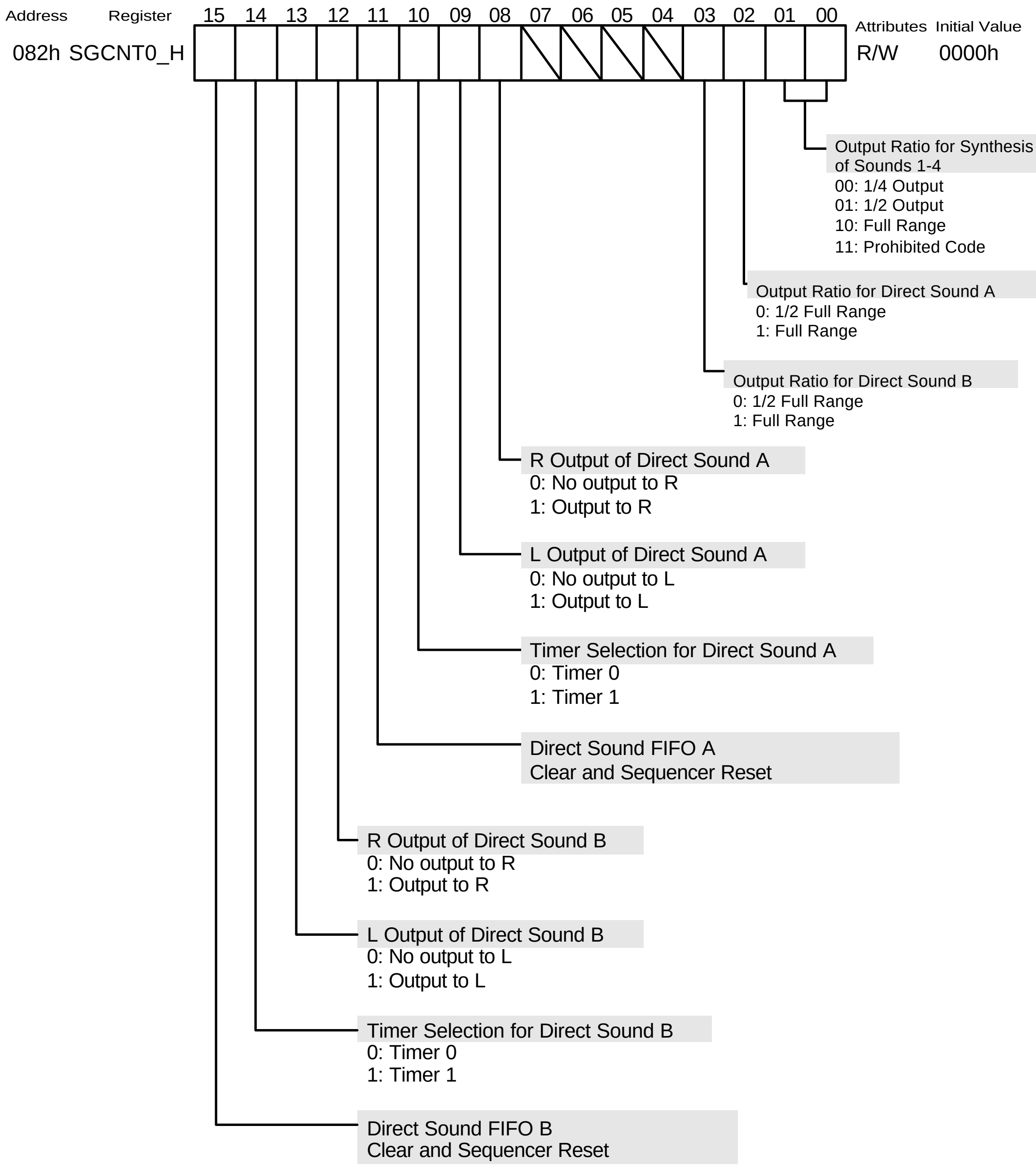
In this situation, the contents of all the Sound mode registers are reset.

<u>Always set all the sound operation flags to 1 when setting each sound mode register. You cannot set each sound mode register when all the sound is stopped.</u>

SGCNT1 [d03, d03, d01, d00] Sound Operation Flags

Each sound circuit's status can be referenced.

Each sound is set during output, and when in counter mode it is reset after the time passes which was set up with the length data.


Address Register 15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00 Attributes Initial Value
082h SGCNT0_H R/W 0000h
Output Ratio for Synthesis of Sounds 1-4
00: 1/4 Output
01: 1/2 Output
10: Full Range
11: Prohibited Code
Output Ratio for Direct Sound A
0: 1/2 Full Range
1: Full Range
Output Ratio for Direct Sound B
0: 1/2 Full Range
1: Full Range
R Output of Direct Sound A
0: No output to R
1: Output to R
L Output of Direct Sound A
0: No output to L
1: Output to L
Timer Selection for Direct Sound A
0: Timer 0
1: Timer 1
Direct Sound FIFO A
Clear and Sequencer Reset
R Output of Direct Sound B
0: No output to R
1: Output to R
L Output of Direct Sound B
0: No output to L
1: Output to L
Timer Selection for Direct Sound B
0: Timer 0
1: Timer 1
Direct Sound FIFO B
Clear and Sequencer Reset

SGCNT0_H [d15],[d11] FIFO Clear and Sequencer Reset for Each Direct Sound

With direct sound the sequencer counts the number of times data is transmitted from FIFO to the mixing circuit. A setting of 1 resets the FIFO and sequencer used for each direct sound. When this bit is read, 0 is returned.

SGCNT0_H [d14],[d10] Timer Selection for Each Direct Sound

Specifies the timer used for each direct sound.

A setting of 0 selects timer 0, and 1 selects timer 1.

The same timer can be specified for both direct sounds (A and B).

SGCNT0_H [d13],[d09] L Output for Each Direct Sound

Controls the output to L for each direct sound. A setting of 0 results in no output to L; a setting of 1 causes output to L.

SGCNT0_H [d12],[d08] R Output for Each Direct Sound

Controls the output to R for each direct sound. A setting of 0 results in no output to R; a setting of 1 causes output to R.

SGCNT0_H [d03],[d02] Output Ratio for Each Direct Sound

Selects the output level for each direct sound.

A setting of 0 produces output that is 1/2 of full range. A setting of 1 results in full-range output.

SGCNT0_H [d01-00] Output Ratio for Synthesis of Sounds 1-4

Specifies the output level for the synthesis of sounds 1-4.

A setting of 00 results in output that is 1/4 of full range.

A setting of 01 results in output that is 1/2 of full range.

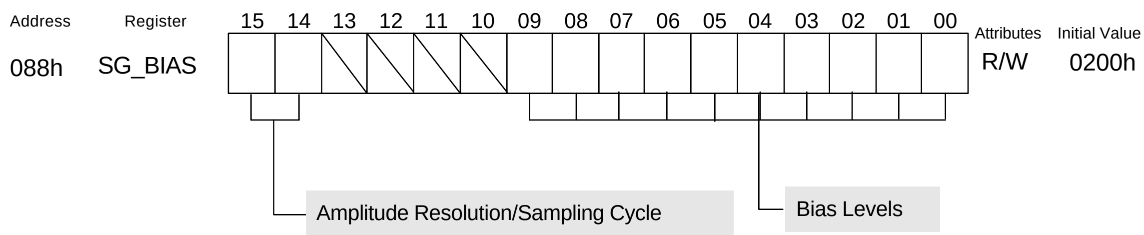
A setting of 10 results in full-range output.

A setting of 11 is a prohibited code.

10.8 Sound PWM Control

Bit modulation format PWM is used in the AGB sound circuit. When no sound is produced, the duty waveform is output, and bias voltage is provided. The PWM circuit is stopped when the setting for duty is 0h.

<u>This register uses system ROM. This can be the cause of errors, therefore be careful not to write to this register.</u>



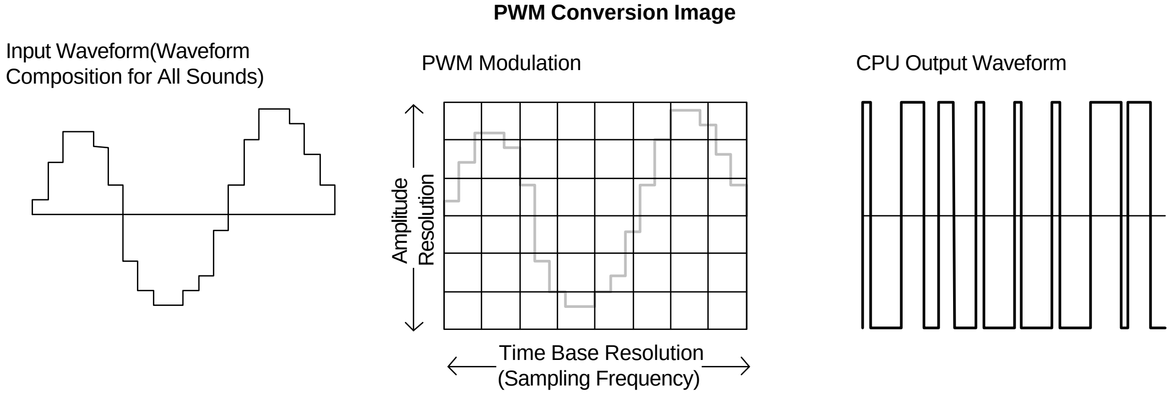
SG_BIAS[d15-14] Amplitude Resolution/Sampling Cycle

This sets the amplitude resolution and sampling cycle frequency during PWM modulation.

The DMG compatible sound is input at 4 bits/130.93KHz so in order to have accurate modulation the sampling frequency must be set high. Direct sound will arbitrarily decide the sampling frequency based on the timer setting. By using the sampling frequencies listed in the table below, an accurate modulation can be done. Thus, in order to increase authenticity of sound, the amplitude resolution needs to be set higher. When producing both compatible sound and direct sound find a value that will work for both and set this.

Setting	Amplitude Resolution	Sampling Frequency
00	9bit	32.768KHz
01	8bit	65.536KHz
10	7bit	131.072KHz
11	6bit	262.144KHz

PWM Conversion Image



SG_BIAS[d09-00] Bias Level

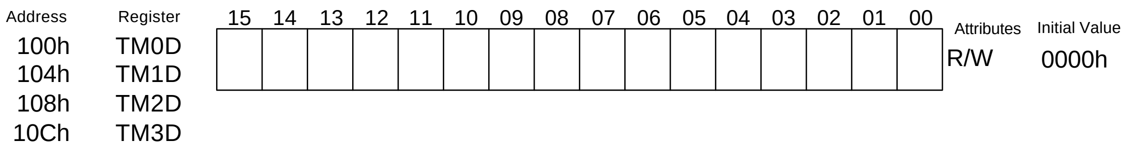
This is used by system ROM. Please do not change this value, as it may cause errors.

11 Timer

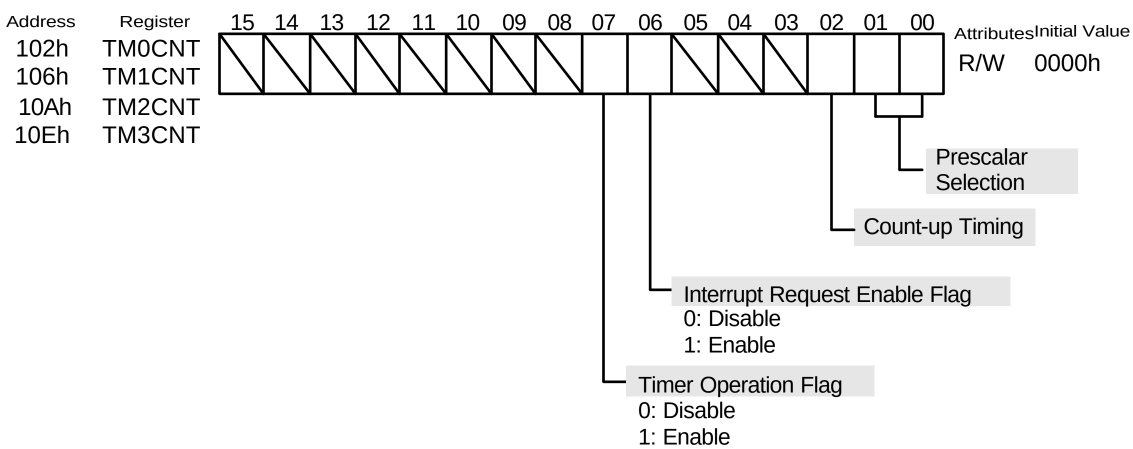
AGB is equipped with 4 channels of 16 bit timers.

Of these, timers 0 and 1 can be used to set the interval for the supply of data from the FIFO(s) for direct sounds A and B. This interval is set by timer overflow.

1) Timer Setting



2) Timer Control



TM*CNT [d07] Timer Operation Flag

Starts and stops the timer. A setting of 0 stops the timer, and a setting of 1 starts it.

TM*CNT [d06] Interrupt Request Enable Flag

Controls whether an interrupt request flag is generated by an overflow. No interrupt is generated with a setting of 0. An overflow does generate an interrupt if the setting is 1.

TM*CNT [d02] Count-Up Timing

With a setting of 0, count-up is performed in accordance with the prescalar specification in [d01-00]. With a setting of 1, overflow of the timer channel one number lower starts a count-up regardless of the prescalar specification.

This mode is suitable for purposes such as time measurement over relatively long periods.

The count-up timing specification is disabled for Timer 0, which counts up in accordance with the prescalar specification.

TM*CNT [d01-00] Prescalar Selection

Allows selection of a prescalar based on the system clock (16.78MHz).

Setting	Prescalar (Count-Up Interval)	
00	System clock	(59.595 ns)
01	64 cycles of system clock	(3.814 µs)
10	256 cycles of system clock	(15.256 µs)
11	1024 cycles of system clock	(61.025 µs)

12 DMA Transfer

AGB has 4 DMA transfer channels.

The highest priority of these channels is DMA0, followed in order by DMA1, DMA2, and DMA3.

If a DMA with a higher priority than the currently executing DMA begins execution, the execution of the current DMA is temporarily halted, and the DMA with the higher priority is executed. Once this DMA finishes, the original DMA resumes execution from where it was halted.

Thus, the most appropriate uses of each DMA channel are those described below.

- **DMA 0**

  Because this has the highest priority, it is not interrupted by other DMA channels. Thus, it is used for reliable processing over a limited period, as is required for purposes such as horizontal-blanking DMA.

- **DMA 1 and DMA 2**

  These are used for direct sound functions, which require relatively high priority, or for general-purpose transfers.

- **DMA 3**

  This is used for the most general types of transfers.

Perform the following settings when using DMA.

1. Specify the transfer source address in the source address register.
2. Specify the transfer destination address in the destination address register.
3. Set the number of data items in the word-count register.
4. Specify the transfer method to be used in the DMA control register.

[Cautions for DMA]

When transferring data to OAM or OBJ VRAM by DMA during H-blanking, the H-blank must first be freed from OBJ display hardware processing periods using the DISPCNT register. (See “5 Image System”.)

12.1 DMA 0

DMA 0 allows different areas of internal memory in the main unit to access one another. It has the highest priority of the DMA channels.

1) Source Address

Specifies the source address using 27 bits.

The area 00000000h-07FFFFFFh (internal memory area of main unit) can be specified.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B0h	DM0SAD_L																	W	0000h

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B2h	DM0SAD_H																	W	0000h

2) Destination Address

Specifies the destination address using 27 bits.

The area 00000000h-07FFFFFFh (internal memory area of main unit) can be specified.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B4h	DM0DAD_L																	W	0000h

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B6h	DM0DAD_H																	W	0000h

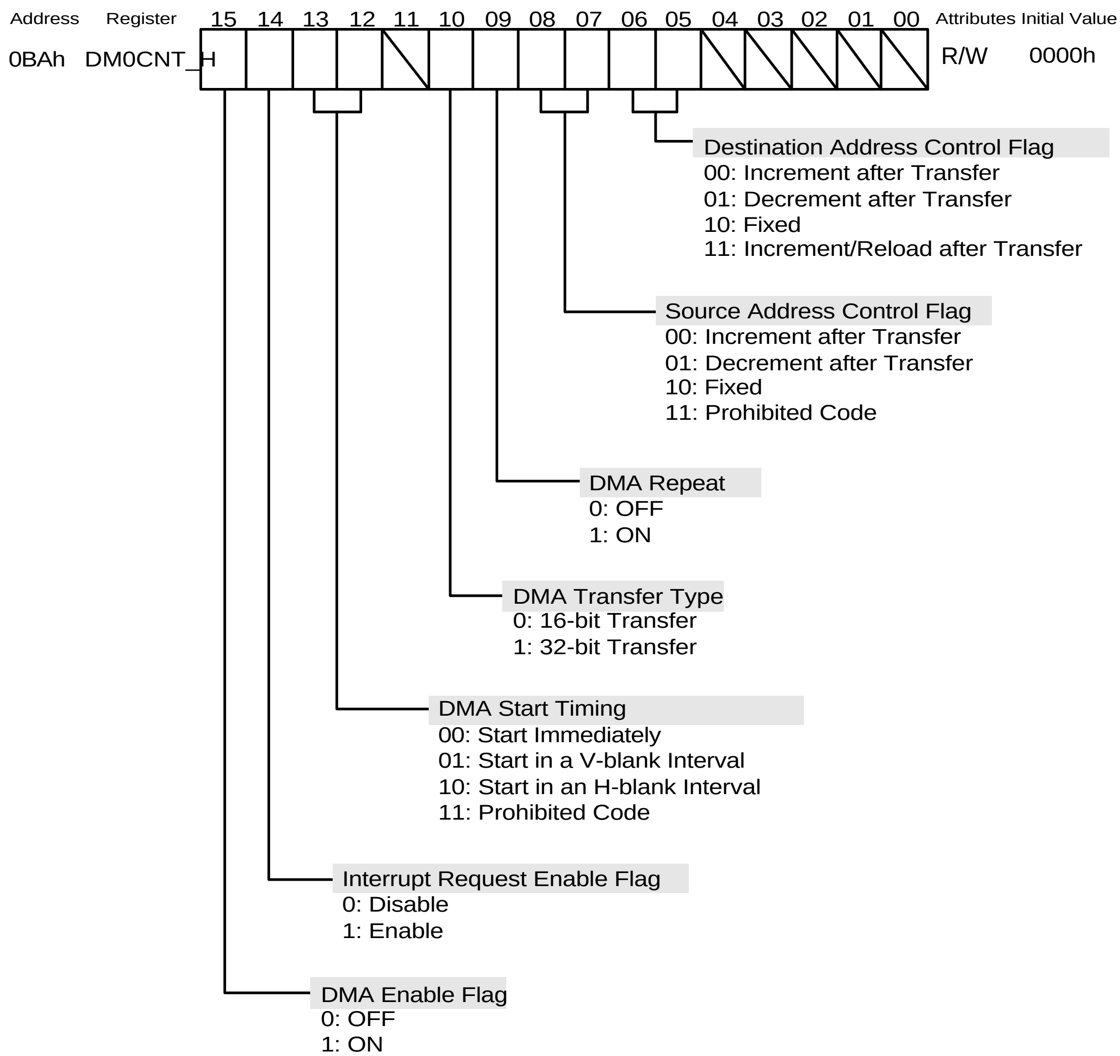
3) Word Count

Specifies the number of bytes transferred by DMA0, using 14 bits. The number can be specified in the range 0001h~3FFFh~0000h (when 0000h is set, 4000h bytes are transferred).

Thus, in 16-bit data transfer mode, up to 4000h x 2=8000h bytes can be transferred, and in 32-bit data transfer mode, up to 4000h x 4=10000h bytes can be transferred.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0B8h	DM0CNT_L																	W	0000h

4) DMA Control



DM0CNT_H [d15] DMA Enable Flag

A setting of 0 disables DMA.

A setting of 1 enables DMA, and after the transfer is completed the source and destination registers are restored to their last values.

[Note] Delay of 2 waits will occur before DMA is activated after this flag is set. Accessing DMA related registers during this time may cause a DMA malfunction. Do another process or insert a dummy load command instead.

DM0CNT_H [d14] Interrupt Request Enable Flag

Enables an interrupt request to be generated when DMA transfer of the specified word count has been completed.

No request is generated with a setting of 0; a request is generated with a setting of 1.

DM0CNT_H [d13-12] DMA Transfer Timing

The timing of the DMA transfer can selected from the following options.

Setting	DMA Startup Timing
00	**Start immediately**
01	**Start during a V-blanking interval** Starts at the beginning of a V-blanking interval (approximately 4.993 ms).
10	**Start during a H-blanking interval** Starts at the beginning of a H-blanking interval (approximately 16.212 μs). If this accompanies OAM access, the H-blanking interval must first be freed of OBJ display hardware processing periods. (See “Chapter 5 Image System”.)
11	**Prohibited Code**

DM0CNT_H [d10] DMA Transfer Type

Sets the bit length of the transfer data.

With a setting of 0, the data are transferred by DMA in 16-bit (half-word) units. With a setting of 1, the data are transferred by DMA in 32-bit (word) units.

DM0CNT_H [d09] DMA Repeat

With the DMA repeat function set to ON, if V-blanking or H-blanking intervals are selected as the timing of DMA startup, DMA is restarted when the next startup condition occurs (a V-blank or H-blank). <u>In this mode, restarting will continue as long as the DMA enable flag is not set to 0.</u>

When the DMA repeat function is set to OFF, DMA halts as soon as the amount of data specified by the value in the word-count register has been transferred.

DM0CNT_H [d08] Source Address Control Flag

Control of the source address is specified after each DMA transfer.

A setting of 00 causes an increment.

A setting of 01 causes a decrement.

A setting of 10 causes it to be fixed.

11 is a prohibited code.

DM0CNT_H [d07] Destination Address Control Flag

Control of the destination address is specified after each DMA transfer.

A setting of 00 causes an increment.

A setting of 01 causes a decrement.

A setting of 10 causes it to be fixed.

A setting of 11 causes an increment and after all transfers end, a reload(The setting is returned to what it was when the transfer started) is done.

12.2 DMA 1 and 2

DMA channels 1 and 2 provide access between the Game Pak bus/internal memory of the main unit and internal memory of the main unit, or between the Game Pak bus/internal memory of the main unit and the direct sound FIFO. Transfers to direct-sound FIFO can be accomplished only by using DMA 1 and 2.

1) Source Address

Specifies the source address using 28 bits.

The area 00000000h-0FFFFFFFh can be specified.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0BCh 0C8h	DM1SAD_L DM2SAD_L																	W	0000h

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0BEh 0CAh	DM1SAD_H DM2SAD_H																	W	0000h

2) Destination Address

Specifies the destination address using 27 bits.

The area 00000000h-07FFFFFFh (internal memory area of main unit) can be specified.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C0h 0CCh	DM1DAD_L DM2DAD_L																	W	0000h

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C2h 0CEh	DM1DAD_H DM2DAD_H																	W	0000h

3) Word Count

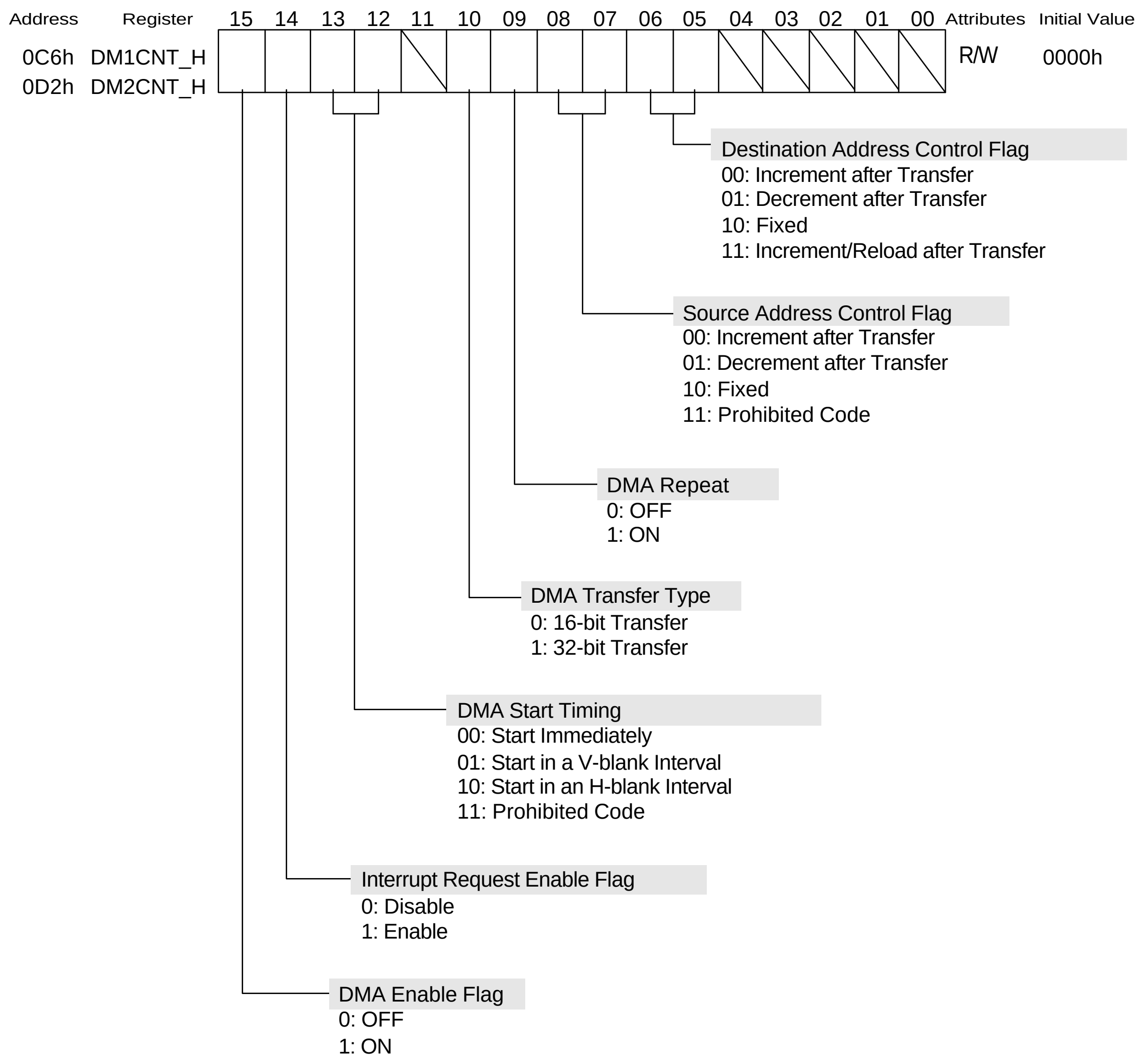
Specifies the number of bytes transferred by DMA 1 and DMA 2, using 14 bits. The number can be specified in the range 0001h~3FFFh~0000h (when 0000h is set, 4000h bytes are transferred).

Thus, in 16-bit data transfer mode, up to 4000h x 2=8000h bytes can be transferred, and in 32-bit data transfer mode, up to 4000h x 4=10000h bytes can be transferred.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0C4h 0D0h	DM1CNT_L DM2CNT_L																	W	0000h

The word-count register setting is disabled in direct-sound FIFO transfer mode. With each request received from sound FIFO, 32 bits x 4 words of sound data are transferred.

4) DMA Control



DM(1,2)CNT_H [d15] DMA Enable Flag

A setting of 0 disables the DMA function.

A setting of 1 enables DMA, and after the transfer is completed the source and destination registers are restored to their last values.

[Note] Delay of 2 waits will occur before DMA is activated after this flag is set. Accessing DMA related registers during this time may cause a DMA malfunction. Do another process or insert a dummy load command instead.

DM(1,2)CNT_H [d14] Interrupt Request Enable Flag

Enables an interrupt request to be generated when DMA transfer of the specified word count has been completed.

No request is generated with a setting of 0; a request is generated with a setting of 1.

DM(1,2)CNT_H [d13-12] DMA Transfer Timing

The timing of the DMA transfer can be selected from the following options.

Setting	DMA Startup Timing
00	**Start Immediately**
01	**Start During a V-blanking interval** Starts at the beginning of a V-blanking interval (approximately 4.993 ms).
10	**Start During a H-blanking interval** Starts at the beginning of a H-blanking interval (approximately 16.212 µs). If this accompanies OAM access, the H-blanking interval must first be freed of OBJ display hardware processing periods. (See “Chapter 5, Image System”.)
11	**Start When Request Generated by Direct-Sound FIFO** Starts when a request is received form direct-sound FIFO. Specify sound FIFO as the destination address. Also, set the DMA repeat function [d09] to ON.

DM(1,2)CNT_H [d10] DMA Transfer Type

Sets the bit length of the transfer data.

With a setting of 0, the data are transferred by DMA in 16-bit (half-word) units. With a setting of 1, the data are transferred by DMA in 32-bit (word) units.

In direct-sound FIFO transfer mode, the data are transferred in 32-bit units.

DM(1,2)CNT_H [d09] DMA Repeat

With the DMA repeat function set to ON, if V-blanking or H-blanking intervals are selected as the timing of DMA startup, DMA is restarted when the next startup condition occurs (a V-blank or H-blank). <u>In this mode, restarting will continue as long as the DMA enable flag is not set to 0.</u>

When the DMA repeat function is set to OFF, DMA halts as soon as the amount of data specified by the value in the word-count register has been transferred.

<u>Set this bit to 1 in direct-sound FIFO transfer mode.</u>

DM(1,2)CNT_H [d08] Source Address Control Flag

Control of the source address is specified after each DMA transfer.

A setting of 00 causes an increment.

A setting of 01 causes a decrement.

A setting of 10 causes it to be fixed.

11 is a prohibited code.

<u>When the Game Pak Bus has been set to the source address, make sure you select increment.</u>

DM(1,2)CNT_H [d07] Destination Address Control Flag

Control of the destination address is specified after each DMA transfer.

A setting of 00 causes an increment.

A setting of 01 causes a decrement.

A setting of 10 causes it to be fixed.

A setting of 11 causes an increment to be carried out and then a reload(returned to setting at start of transfer) is done after every transfer is completed.

However, when in direct sound FIFO transfer mode, the destination address is fixed and unrelated to the setting.

12.3 DMA 3

DMA 3 provides memory access between the Game Pak bus and internal memory of the main unit, or between different areas of internal memory of the main unit.

1) Source Address

Specifies the source address using 28 bits.

The area 00000000h-0FFFFFFFh (internal memory of main unit and Game Pak memory area) can be specified.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0D4h	DM3SAD_L																	W	0000h

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0D6h	DM3SAD_H																	W	0000h

2) Destination Address

Specifies the destination address using 28 bits.

The area 00000000h-0FFFFFFFh (internal memory area of main unit and Game Pak memory area) can be specified.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0D8h	DM3DAD_L																	W	0000h

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0DAh	DM3DAD_H																	W	0000h

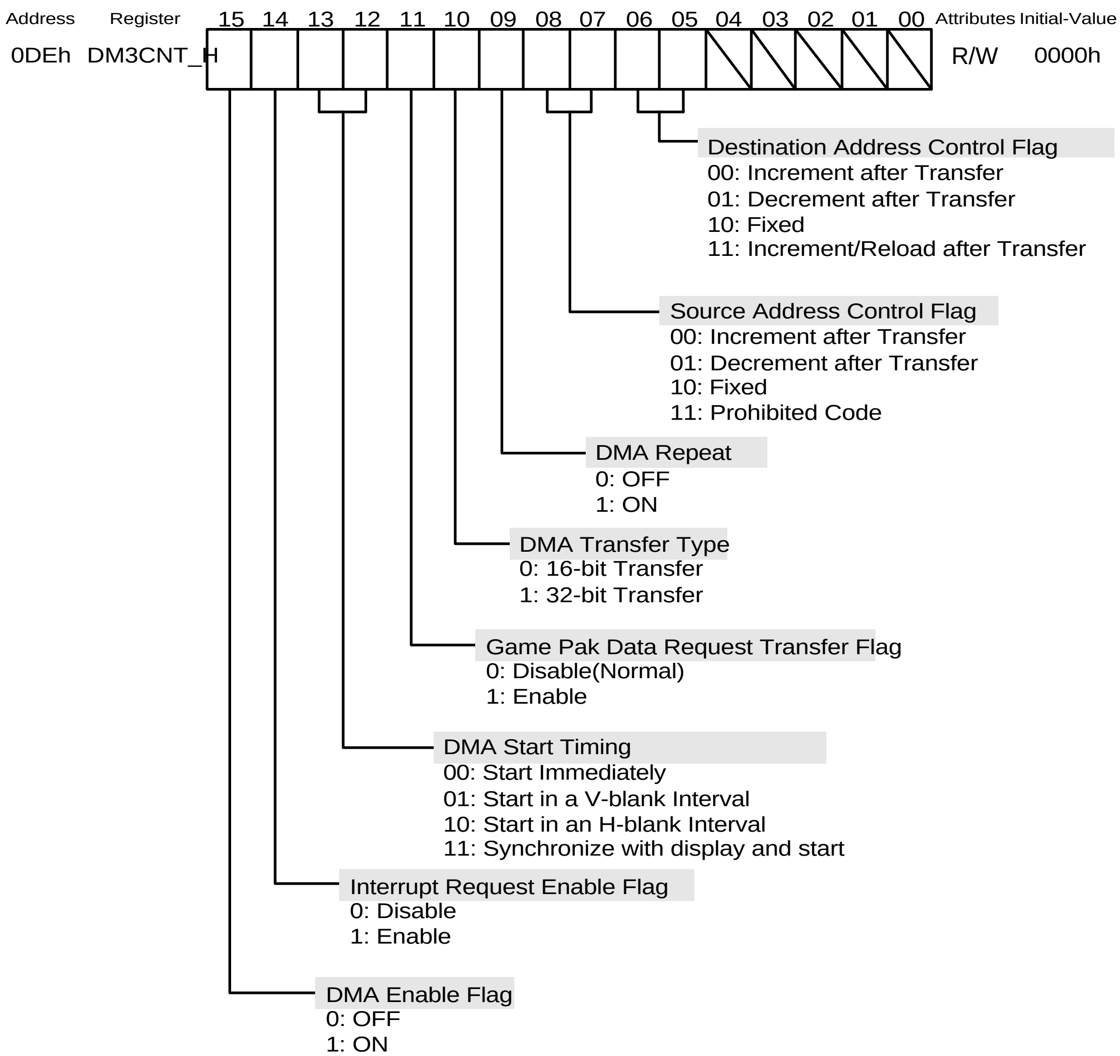
3) Word Count

Specifies the number of bytes transferred by DMA 3, using 16 bits. The number can be specified in the range 0001h~FFFFh~0000h (when 0000h is set, 10000h bytes are transferred).

Thus, in 16-bit data transfer mode, up to 10000h x 2=20000h bytes can be transferred, and in 32-bit data transfer mode, up to 10000h x 4=40000h bytes can be transferred.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
0DCh	DM3CNT_L																	W	0000h

4) DMA Control



DM3CNT_H [d15] DMA Enable Flag

A setting of 0 disables DMA.

A setting of 1 enables DMA, and after the transfer is completed the source and destination registers are restored to their last values.

[Note] Delay of 2 waits will occur before DMA is activated after this flag is set. Accessing DMA related registers during this time may cause a DMA malfunction. Do another process or insert a dummy load command instead..

DM3CNT_H [d14] Interrupt Request Enable Flag

Enables an interrupt request to be generated when DMA transfer of the specified word count has been completed.

No request is generated with a setting of 0; a request is generated with a setting of 1.

DM3CNT_H [d13-12] DMA Transfer Timing

The timing of the DMA transfer can selected from the following options.

Setting	DMA Startup Timing
00	**Start Immediately**
01	**Start During a V-blanking Interval** Starts at the beginning of a V-blanking interval (approximately 4.993 ms).
10	**Start During a H-blanking Interval** Starts at the beginning of a H-blanking interval (approximately 16.212 µs). If this accompanies OAM access, the H-blanking interval must first be freed of OBJ display hardware processing periods. (See Chapter “5 Image System”.)
11	Synchronize with display and start. Synchronize with start of H-Line rendering during a display interval and start.

DM3CNT_H [d11] Game Pak Data Request Transfer Flag

Should normally be set to 0.

When set to 1, DMA transfer is performed in response to a data request from the Game Pak.

[Note]
A Game Pak that supports this transfer mode is required in order to use it. In addition, it cannot be used at the same time as a Game Pak interrupt.

DM3CNT_H [d10] DMA Transfer Type

Sets the bit length of the transfer data.

With a setting of 0, the data are transferred by DMA in 16-bit (half-word) units. With a setting of 1, the data are transferred by DMA in 32-bit (word) units.

DM3CNT_H [d09] DMA Repeat

With the DMA repeat function set to ON, if V-blanking or H-blanking intervals are selected as the timing of DMA startup, DMA is restarted when the next startup condition occurs (a V-blank or H-blank). <u>In this mode, restarting will continue as long as the DMA enable flag is not set to 0.</u>

When the DMA repeat function is set to OFF, DMA halts as soon as the amount of data specified by the value in the word-count register has been transferred.

DM3CNT_H [d08] Source Address Control Flag

Control of the source address is specified after each DMA transfer.

A setting of 00 causes an increment.

A setting of 01 causes a decrement.

A setting of 10 causes it to be fixed.

11 is a prohibited code.

<u>When the Game Pak Bus has been set to the source address, make sure you select increment.</u>

DM3CNT_H [d07] Destination Address Control Flag

Control of the destination address is specified after each DMA transfer.

A setting of 00 causes an increment.

A setting of 01 causes a decrement.

A setting of 10 causes it to be fixed.

A setting of 11 causes an increment to be carried out and then a reload(returned to setting at start of transfer) is done after every transfer is completed.

13 Communication Functions

AGB provides the following five functions.

1. 8-Bit/32-Bit Normal Communication Function

Using a cable is prohibited for Normal Communication. It is possible to communicate with peripherals that do not use cables. (When communicating with AGB using a cable, Multi Player Communication is used.) Due to the voltage difference, it is not possible to communicate with CGB. 8-bit communication handles 8-bit data with a transfer-enable flag. 32-bit communication handles 32-bit data with a transfer-enable flag.

2. 16-Bit Multi-player Communication Function

This multiple/simultaneous communication function uses UART system to enable communication of up to 4 AGB units.
A special cable for Multi-player communication is necessary.

3. UART Communication Function

Enables high-speed communication by UART system.

4. General Purpose Communication Function

Enables communication by any protocol through direct control of the communication terminal.

5. JOY Bus Communication Function

Enables communication using Nintendo's standardized Joy bus.

Selecting Communication Function

All the communication functions use an external expansion 6-pin connector. Communication functions are switched by the communication function set flag of the communication control register R (2-bit) and the communication mode set flag of the serial communication control register SCCNT_L (2-bit), which are described later.

Communication Functions	R		SCCNT_L	
	d15	d14	d13	d12
General Purpose	1	0	*	*
JOY Bus	1	1	*	*
8-Bit Serial	0	*	0	0
32-Bit Serial	0	*	0	1
16-Bit Serial	0	*	1	0
UART	0	*	1	1

(* ... any)

When changing communication modes, change only the communication mode set flag first. Do not start a communication at the same time as you change modes. This may cause a malfunction.

If a communication isn't finished (SIO interrupt does not occur) after a certain period of time, or if there is a communication error after retries, enter another communication mode once and then re-enter the communication mode once again. By doing this, the communication circuit will be reset.

[Cautions for Communication Function]

When communicating, try to avoid lock-ups or malfunctions by considering the various circumstances listed below:

(Example: To permit canceling a communication by pressing a key.)

Examples of Communication Failure

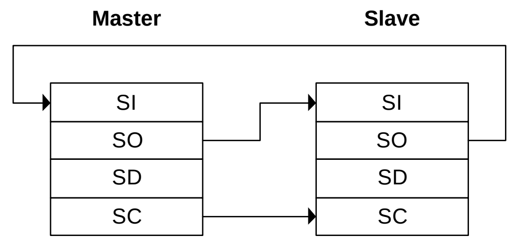
When peripheral equipment that is not compatible is connected.
When different software is connected to the other machine.
When a communication mode is different from the other machine.
When a communication cable is connected incorrectly.
When unexpected data is received.

13.1 8-Bit/32-Bit Normal Serial Communication

Serial transfer sends/receives simultaneously.

If data is set in the data register and the serial transfer is started, received data is set in the data register when the transfer is complete.

Connecting during normal serial communication

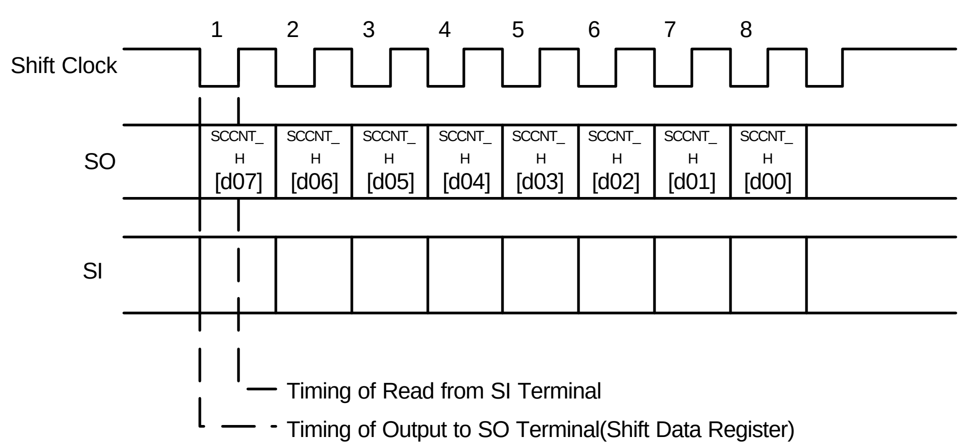


Master (internal clock mode) will output the shift clock from SC terminal. SD terminal will become an input terminal with pull-up.

In the case of a slave(external clock mode), SC terminal will become an input terminal with pull-up. SD terminal will go to LO output.

The set data will be left-shifted by the falling of the shift clock, and will be output from the SO terminal in order starting from the most significant bit. The data input from SI terminal will be input to the least significant bit with the rising of the shift clock.

SIO Timing Chart



The above figure illustrates 8 bit communication. In 32 bit communication, the shift clock sends and receives 32 bits of data.

8 bit Normal Serial Communication Data Register

8-bit transfer mode uses SCCNT_H as a data register. Upper 8-bits will become disabled.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
12Ah	SCCNT_H																	R/W	0000h

32-bit Normal Serial Communication Data Register

32-bit transfer mode uses [120h:SCD0] and [122h:SCD1] as data registers.(These data registers are used for 16-bit multi-player communication also.)

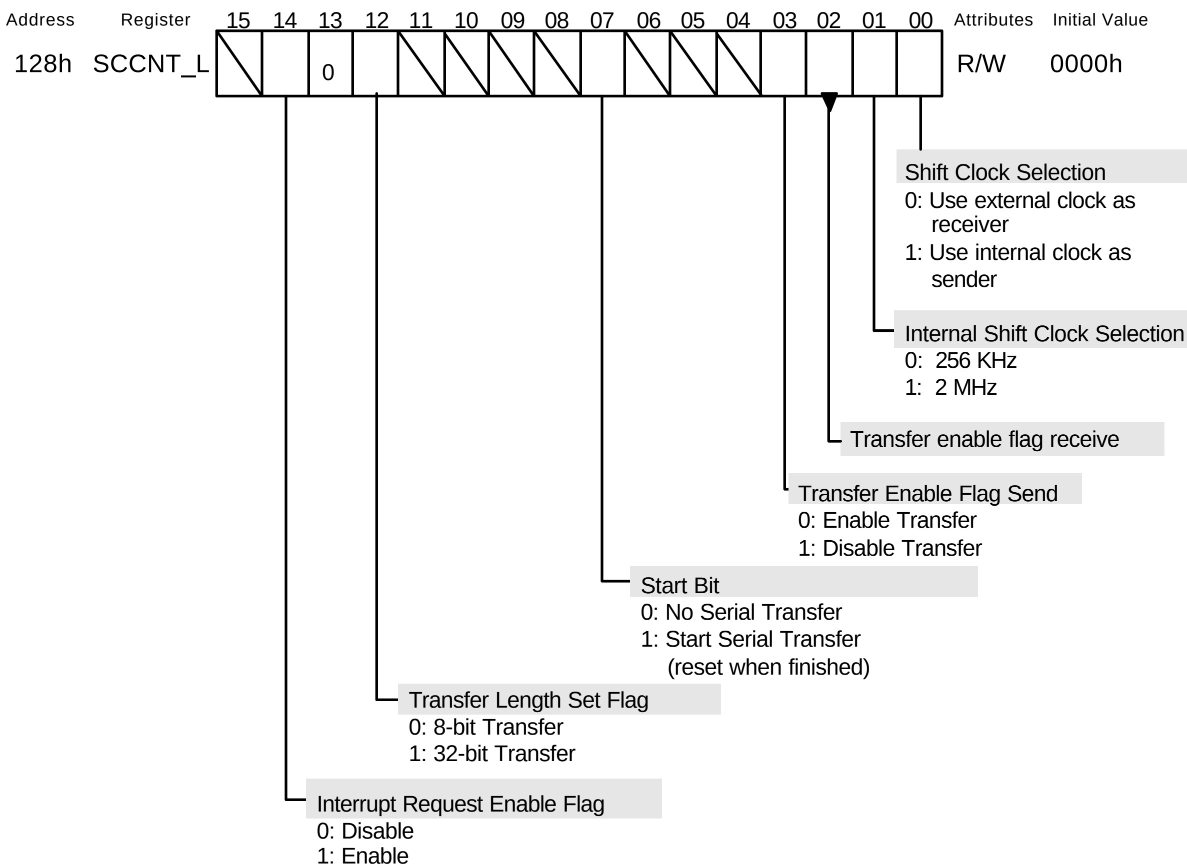
The most significant bit will be d15 in the register SCD1, and the least significant bit will be d0 in the register SCD0.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
120h	SCD0	Data 0																R/W	0000h

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
122h	SCD1	Data 1																R/W	0000h

Control Register

When Register R (d15) = (0), the mode will be 8-bit normal serial communication mode by setting to Register SCCNT_L (d13, d12) = (0,0), and the mode will be 32-bit normal serial communication mode by setting to SCCNT_L (d13, d12) = (0, 1).



SCCNT_L [d14] Interrupt Request Enable Flag

If 0 is set, an interrupt request will not be made.

If 1 is set, an interrupt request will be made immediately after transfer is complete.

SCCNT_L [d12] Transfer Length Setting Flag

Sets bit length of transfer data.

If 0, 8-bit transfer is carried out. If 1, 32-bit transfer is carried out.

SCCNT_L [d07] Start Bit

With a setting of 1, a serial transfer starts. The bit is automatically reset after transfer completion.

SCCNT_L [d03] Transfer Enable Flag Send

A setting of 0 enables transfer; 1 disables it.

This flag is output from the SO terminal until the start of a transfer. When the transfer starts, serial data are output from the SO terminal.

SCCNT_L [d02] Transfer Enable Flag Receive

It is possible to read the status of SI terminal (transfer-enable flag transmitting of the other party's hardware) before communication starts.

It becomes invalid after communication has started.(receive data bit during communication is reflected.)

SCCNT_L [d01] Internal Shift Clock Selection

If 0, 256KHz is selected for the shift clock.

If 1, 2MHz is selected for the shift clock.

SCCNT_L [d00] Shift Clock Selection

If 0, an external clock is used as a shift clock. (slave)

The external clock is input by the SC terminal from another hardware unit. SD terminal will go to LO output.

If 1, an internal clock is used as a shift clock. (master)

The internal clock is output from the SC terminal, and SD terminal will be in the pull-up input status.

[Cautions for Normal Serial Communications]

The shift clock should be selected before the start bit of the SCCNT_L register is set. Extra shift operations may result if the serial transfer is started before or at the same time as the shift clock is selected.

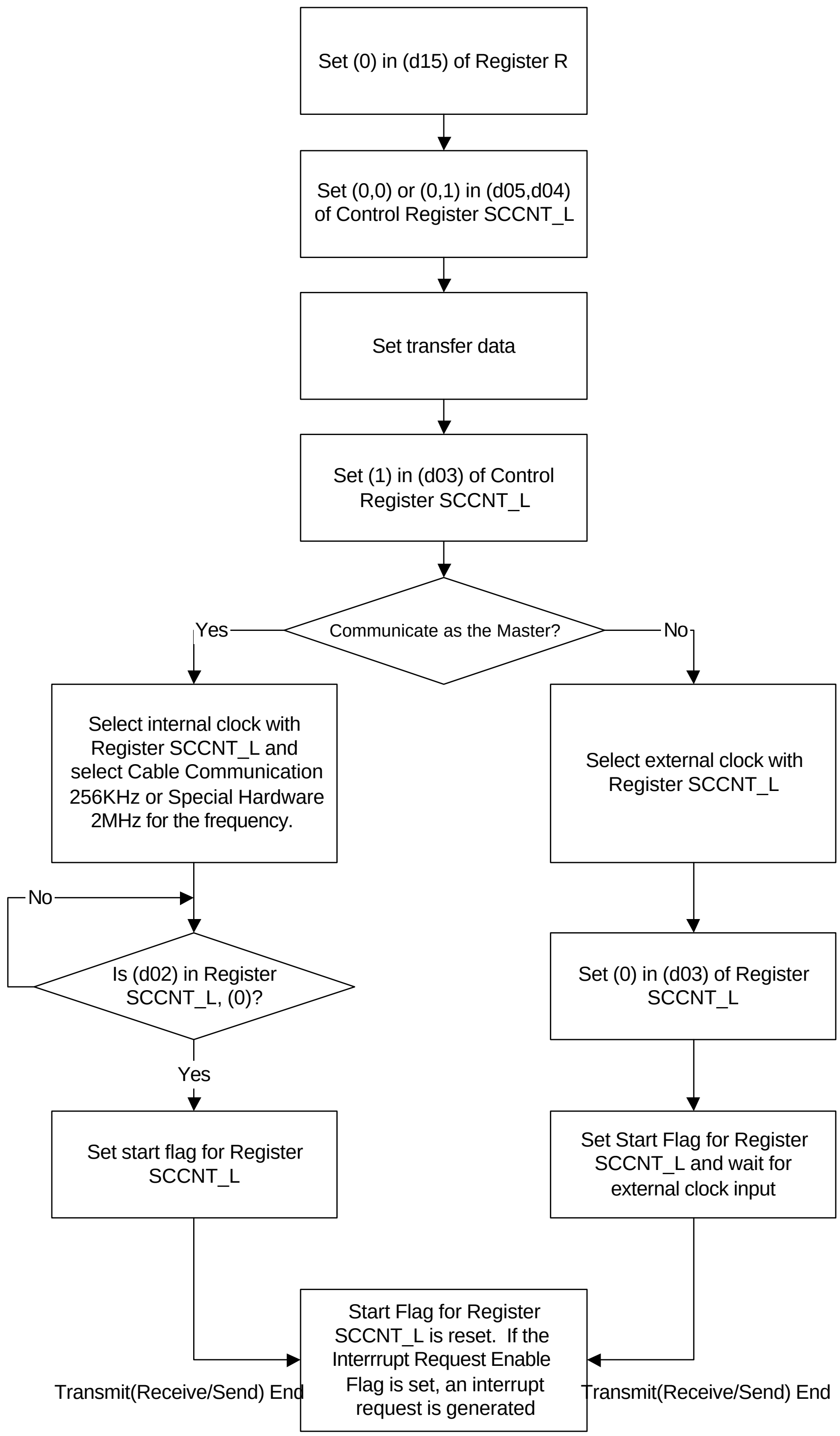
The SCCNT_L register should not be accessed while its start bit is set.

The 8 bit transfer mode is compatible in terms of modes with DMG/CGB, but the voltage with the communication terminal varies. Therefore, communication between AGB and DMG/CGB is not possible.

For normal communication, use of cable is prohibited.

In order to communicate between AGBs, use the Multi player communication functions discussed later.

Normal Serial Communication Flow(Example)

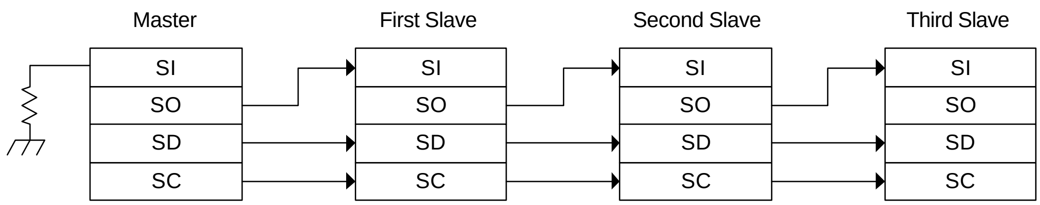


13.2 16-Bit Multi-player Communication

AGB enables multi-player communication between up to 4 units using a special cable.

Depending on the connection status, 1 unit is established as the master and transfers data to slaves in order, one after another.

Connection Status during Multi-player Communication



In multi-player communication mode the SC and SD become pull-up input terminals. Immediately following a reset or in another communication mode, LO is output from the SD terminal. Once the SD terminal becomes HI, you can tell that all connected terminals have entered multi-player communication mode.

The SI terminal is in pull-up input, but due to the multi player communication cable it becomes pull-down. Thus, once all of the terminals are in multi-player mode, the terminal that is LO input to the SI terminal becomes the master. The terminal that is HI input to the SI terminal becomes the slave.

If you set the start bit of Register SCCNT_L of the master, the data registers SCD0, SCD1, SCD2, and SCD3 of the master are initialized to FFFFh.

Additionally, the “SYNC signal” (LO level) is output from the SC terminal. At the same time, the “Start bit” (LO level) is output from the SD terminal. Next, the data from Register SCCNT_H is output and a "“Stop bit” (HI level) is output.

After this is done, the master makes the SD terminal become pull-up input, and LO is output from the SO terminal.

Each slave detects the “SYNC Signal” output from the master and initializes all of the data registers (SCD0, SCD1, SCD2, and SCD3) to FFFFh. The data output from the master is stored in the master and each slave’s SCD0 register.

If LO is input to the SI terminal of the slave which was connected immediately following the master, a “Start bit” (LO level) is output from the SD terminal. Next, data from Register SCCNT_H is output, and lastly a “Stop bit” (HI level) is output.

After this, the SD terminal goes to pull-up input and LO is output from the SO terminal.

At this point, the data output from the first slave is stored in the master and each slave's SCD1 Register.

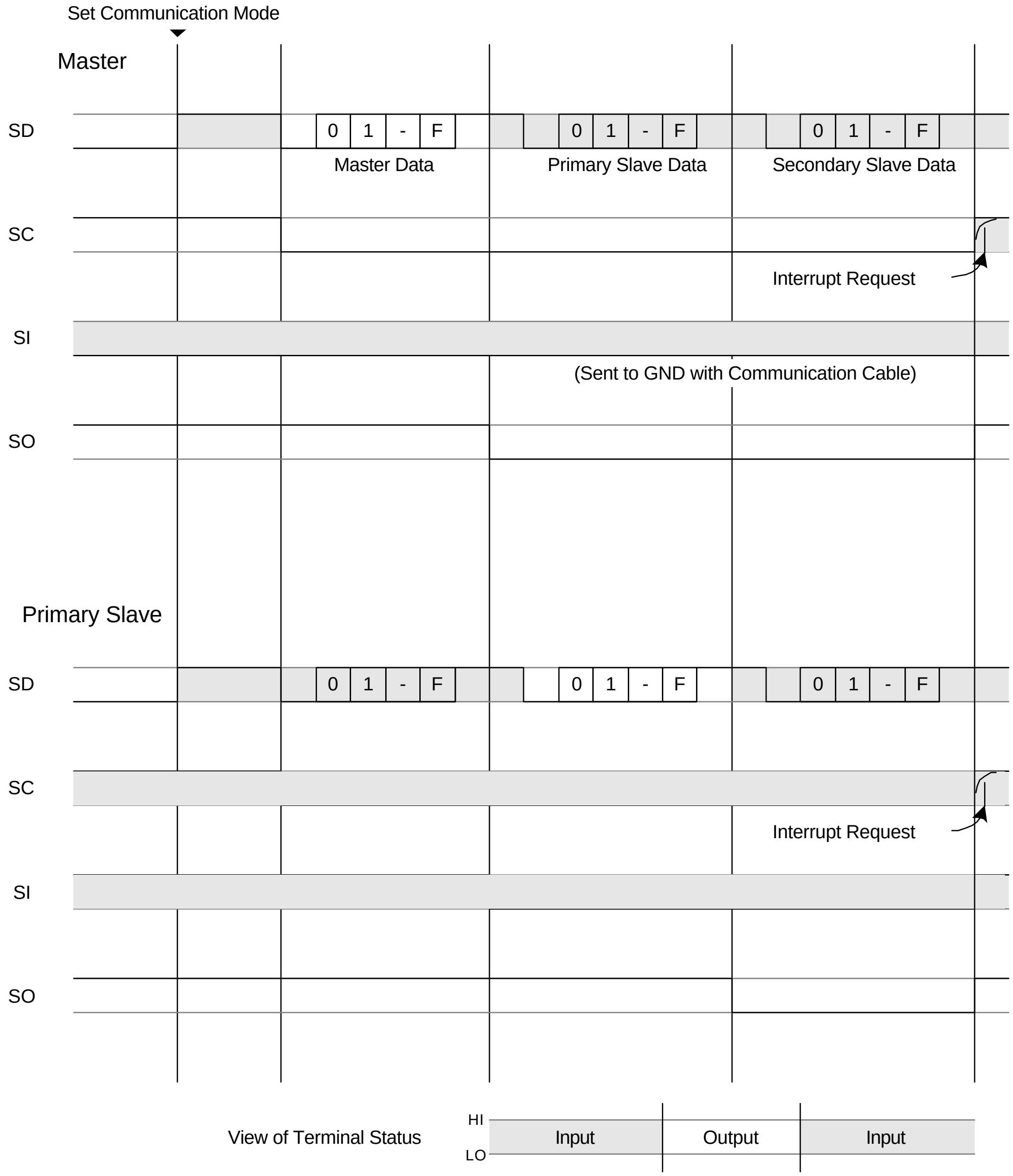
In this way, each slave is sent and all transmissions are carried out.

In the following situations the master produces a "SYNC Signal" (pull-up input after the output of a 5 cycle HI interval of source oscillation) and the transmission ends:

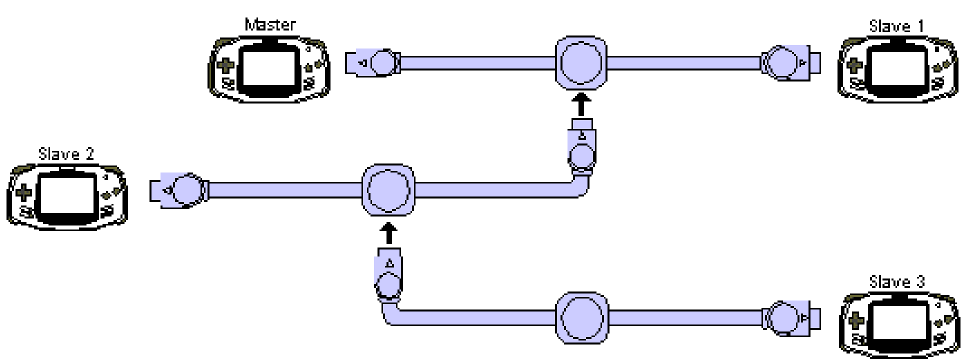
- After the master outputs its own "Stop bit", the next "Start bit" is not input after a certain period of time.
- After a "Stop bit" is received from the first or second slave, a "Start bit" is not input after a certain period of time.
- A "Stop bit" is received from the third slave.

Once the transmission ends, the received data is stored in each of the data registers (SCD0, SCD1, SCD2, and SCD3). If there is a terminal that is not connected the initial data FFFFh is stored.

Multi-player Communication Timing Chart



Multi Player Communication Cable Connecting Diagram



Data Registers

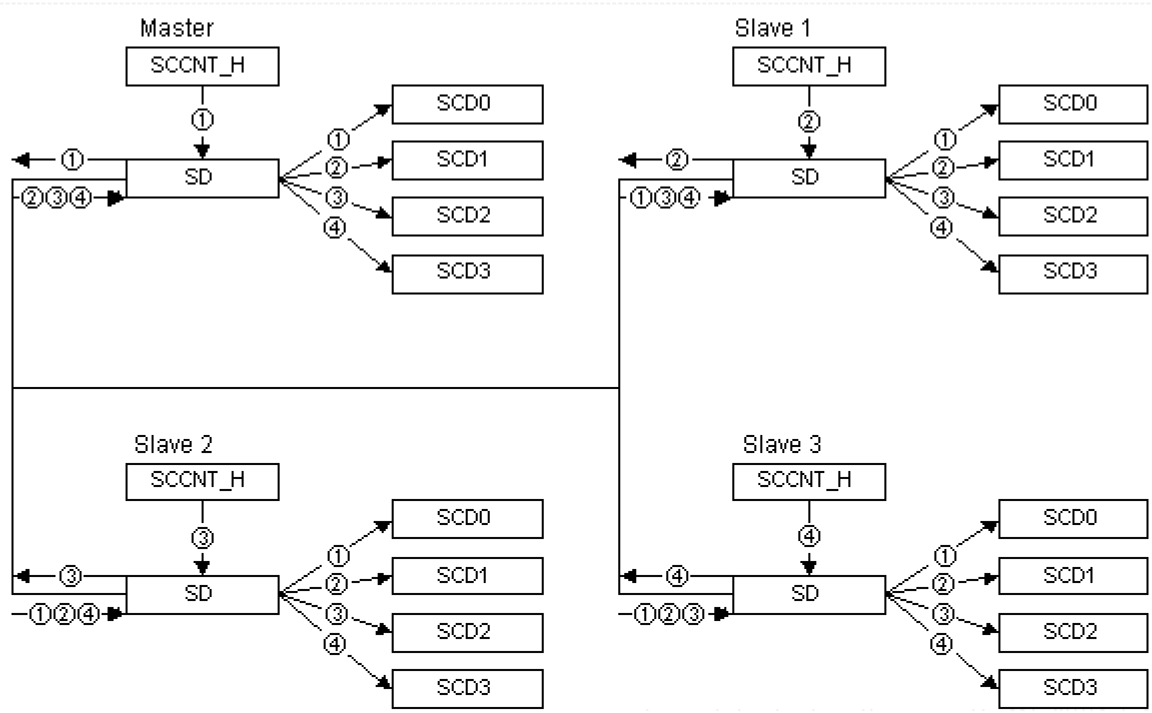
The data send is stored in the Register SCCNT_H.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
12Ah	SCCNT_H																	R/W	0000h

After completion of multi-player communication ends, the send data for the master is in SCD0.

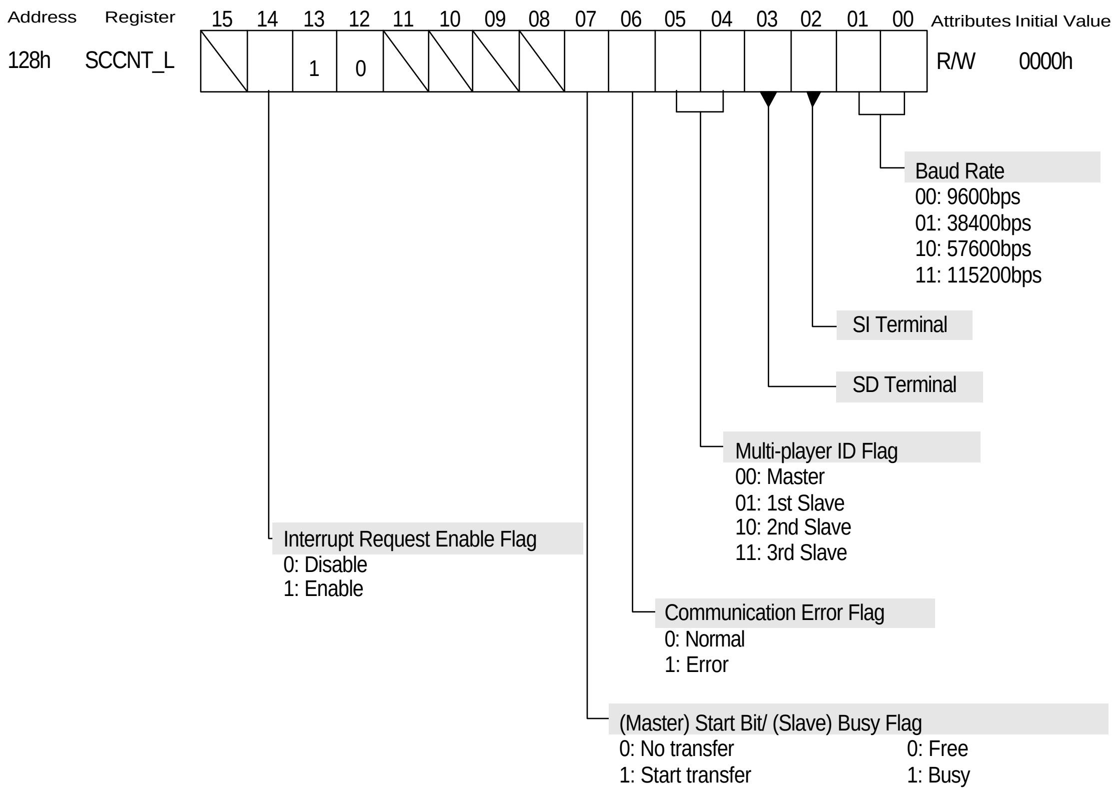
Address	Register	15–00	Attributes	Initial Value
120h	SCD0	Data 0	R/W	0000h
122h	SCD1	Data 1	R/W	0000h
124h	SCD2	Data 2	R/W	0000h
126h	SCD3	Data 3	R/W	0000h

Data Transition Diagram



Control Register

If you set Register SCCNT_L (d13,d12) = (1,0) when Register R (d15) = (0), you will go to 16-bit multi-player communication mode.



SCCNT_L [d14] Interrupt Request Enable Flag

When set to 0, no interrupt request is generated.

When set to 1, an interrupt request is generated upon the completion of multi-player communication.

SCCNT_L [d07] Start Bit/Busy Flag

1)Master(d00 is 1)

When set to 0, no data is transferred.

When set to 1, a data transfer is started. Upon completion of data transfer, it is automatically reset.

[Caution]

Due to individual differences in AGB hardware, there is an error in timing of interrupt occurrence. Always use a timer when sending, and be sure to have enough intervals of communicable minimum send interval + 600 clock (interrupt occurrence error guarantee value).

2)Slave(d00 is 0)

Set during input of transmit start bit (LO source oscillation cycle × 3 (approx. 180ns)), and reset when transfer is complete.

SCCNT_L [d06] Communication Error Flag

The communication status can be confirmed at the end of a communication. (During communication, it is not reflected properly.)

If the status for this bit is 0, there is no error. If it is 1, it means an error has occurred.

This error flag is automatically set in the following situations:

- The SI Terminal does not become LO during the interval when the "SYNC signal" is being input(the master is outputting).

- The stop bit for the receive data is not HI(Framing Error)

However, even if an error occurs, the communication continues, and invalid data is stored in SCD0-SCD3.

SCCNT_ [d05-d04] Multi-player ID Flag

When multi-player communication ends, an ID code will be stored which specifies the order that each particular machine was connected.

SCCNT_L [d03] SD Terminal

The status of the SD Terminal can be read.

If all of the connected terminals enter multi-player communication mode, it becomes HI status.

SCCNT_L [d02] SI Terminal

The status of the SI Terminal can be read.

When all of the connected terminals are in multi-player communication mode, this shows that the terminal which is LO input to the SI terminal is the master. HI input means that it is a slave.

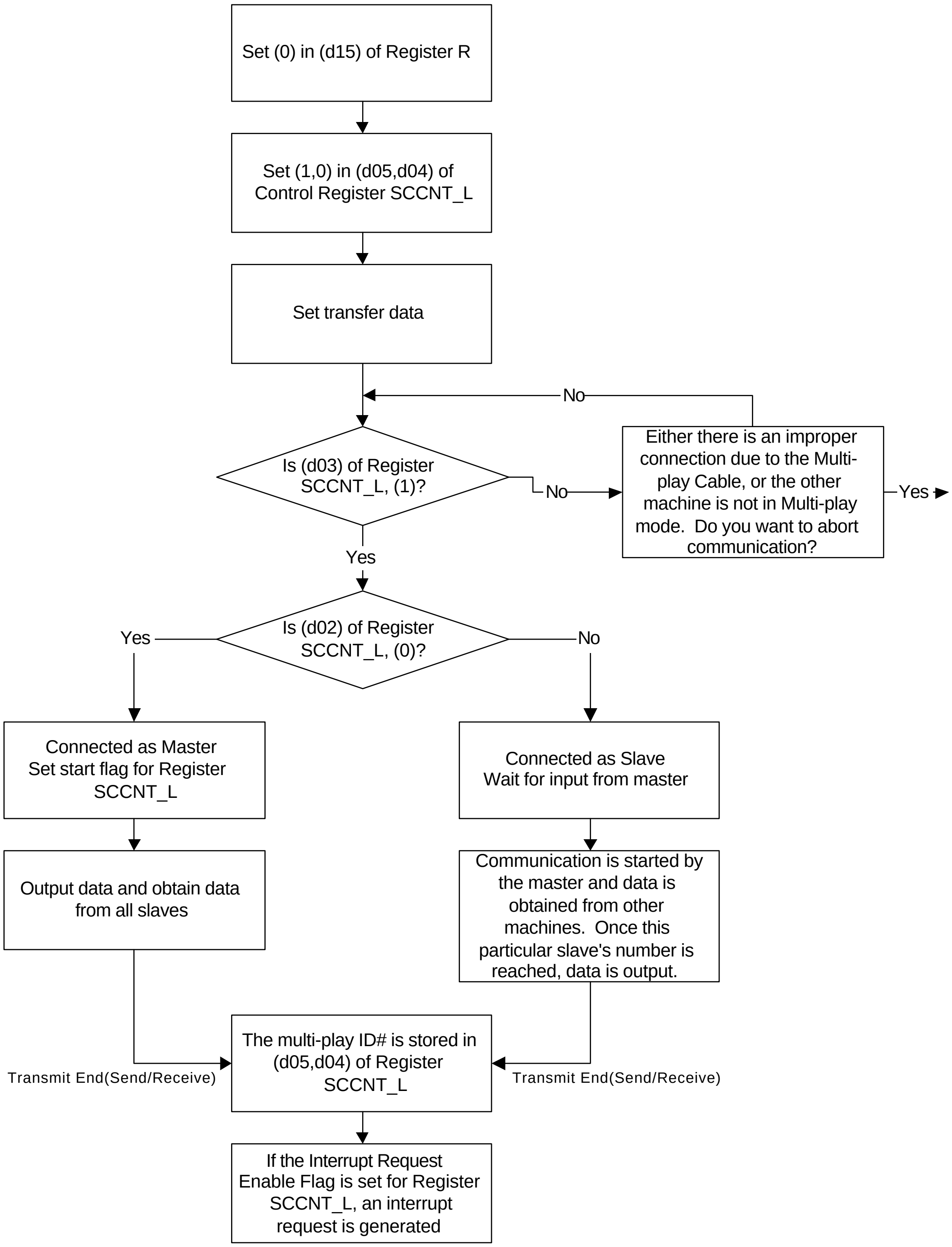
Prior to communication starting, it is not possible to determine the number order of a particular slave.

SCCNT_L [d01-d00] Baud Rate

Sets the communication baud rate.

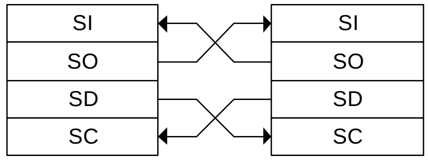
Setting	Baud Rate
00	9600 bps
01	38400 bps
10	57600 bps
11	115200 bps

Multi-player Communication Flow (Example)



13.3 UART Communication Functions

UART communications can be illustrated using the following drawing.



In UART communication mode, a HI level is output from the SD terminal.

When the receive data register (or the receive FIFO) is full, a HI is output from the SD terminal. When it is not full, a LO is output from the SD terminal if the receive enable flag is set. A HI is output if it is reset.

The output of the SD terminal of the other machine is input to the SC terminal.

Once data is written to the send data register, data is sent after a “Start bit” (1 bit) is sent from the SO terminal. However, when the CTS flag for the Control Register is set, data can be sent only when there is a LO input to the SC terminal. The Stop bit is a fixed 1 bit.

Data Register

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
12Ah	SCCNT_H																	R/W	0000h

Relations Between Data Register, FIFO, and Shift Register

When sending or receiving, there are 4 bytes of FIFO. By using the FIFO enable flag for the control register SCCNT_L, you can select whether to use or not use FIFO.

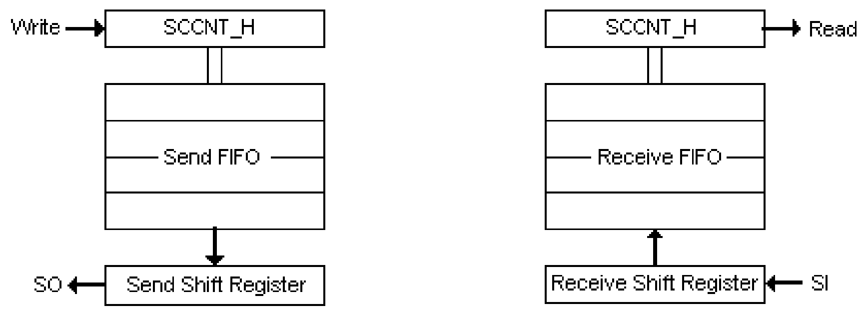
When FIFO is not Used

If written to a data register SCCNT_H, data is written to a send shift register, and if read, data is read from a receive shift register. (Only the lower 8 bits are valid.)

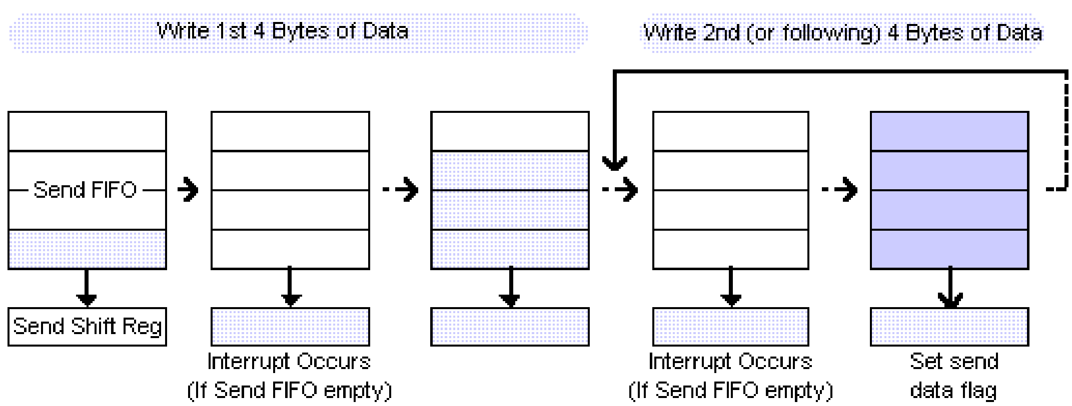
When FIFO is Used

If written to a data register SCCNT_H, data is written to a send FIFO. If all the contents of the send shift register are shifted out, data is transferred from a send FIFO to a shift register, immediately.

Please note when using this operation, that data is immediately transferred to a shift register when the first data is written to the data register, and the interrupt request condition is met as a send FIFO becomes empty. Also, when read, data is read from a receive FIFO. (Only the lower 8 bits are valid.)



Example: Writing Data Registers



Control Register

If Register SCCNT_L (d13,d12) = (1,1) is set when Register R (d15) = (0), you will go to UART communication mode.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
128h	SCCNT_L			1	1													R/W	0000h

- **d01–d00: Baud Rate**
  - 00: 9600bps
  - 01: 38400bps
  - 10: 57600bps
  - 11: 115200bps
- **d02: CTS Flag**
  - 0: Send always possible
  - 1: Send possible during LOW input to SC terminal
- **d03: Parity Control**
  - 0: Even parity
  - 1: Odd parity
- **d04: Send Data Flag**
  - 0: Not Full
  - 1: Full
- **d05: Receive Data Flag**
  - 0: Not Empty
  - 1: Empty
- **d06: Error Flag**
  - 0: No Error
  - 1: Error
- **d07: Data Length**
  - 0: 7 bits
  - 1: 8 bits
- **d08: FIFO Enable Flag**
  - 0: Disable
  - 1: Enable
- **d09: Parity Enable Flag**
  - 0: Disable
  - 1: Enable
- **d10: Send Enable Flag**
  - 0: Disable
  - 1: Enable
- **d11: Receive Enable Flag**
  - 0: Disable
  - 1: Enable
- **d14: Interrupt Request Enable Flag**
  - 0: Disable
  - 1: Enable

SCCNT_L [d14] Interrupt Request Enable Flag

When set to 0, an interrupt request is not generated.

When set to 1 and FIFO is invalid, an interrupt request is generated when a communication error occurs or when the transmission(send/receive) ends.

When set to 1 and FIFO is valid, an interrupt request is generated when a communication error occurs, when a send FIFO is emptied, or a receive FIFO becomes full.

SCCNT_L [d11] Receive Enable Flag

Controls the receive enable/disable.

If the receive enable flag is set when the receive data register (or the receive FIFO) is not full, a LO is output from the SD terminal, and a HI is output if it is reset.

<u>You must first set the receive enable flag and send enable flag to 0 [Disable] before going from UART communication mode to a different communication mode.</u>

SCCNT_L [d10] Send Enable Flag

Controls the send enable/disable.

<u>You must first set the receive enable flag and send enable flag to 0 [Disable] before going from UART communication mode to a different communication mode.</u>

SCCNT_L [d09] Parity Enable Flag

Controls the parity enable/disable.

SCCNT_L [d08] FIFO Enable Flag

Controls the send of the 8 bit wide × 4 depth and the receive FIFO enable/disable.

<u>When using FIFO, first you need to go into UART mode in a status of 0 [FIFO Disable]. By disabling FIFO in UART mode the FIFO sequencer is initialized.</u>

SCCNT_L [d07] Data Length

Select data length as 8 bits or 7 bits.

SCCNT_L [d06] Error Flag

By referring to this error flag, the status of communication errors can be determined.

When it is 0, no errors have occurred. When it is set to 1, an error has occurred. By reading Register SCCNT_L, this error flag is reset.

Additionally, when there has been an error, the data from the Receive Shift Register is not written to the Receive Data Register. The conditions associated with each error are described below.

ERROR NAME	CONDITION
Framing Error	The receive data stop bit is not 0
Parity Error	When parity is enabled, there is an error in the parity for the receive data
Overrun Error	When FIFO is invalid, if the receive data is not empty (SCCNT_L[d05]=0) and next receive has ended (detect stop bit). Or when FIFO is valid, if receive FIFO is full and next communication has ended (detect stop bit).

SCCNT_L [d05] Receive Data Flag

When set to 0, there is still data present.

When set to 1, it is empty.

SCCNT_L [d04] Send Data Flag

When set to 0, it is not full.

After one send operation ends this is reset.

When set to 1, it is full.

Set during a write of data to the lower 8 bits of the Send Data Register SCCNT_H.

SCCNT_L [d03] Parity Control

Switches between even parity and odd parity.

SCCNT_L [d02] CTS Flag

The SD terminal of the other machine (receive enable/disable) is input to the SC terminal.

When set to 0, a send is always possible independent of the SC Terminal.

When set to 1, a send is only possible when a LO is being input to the SC Terminal.

SCCNT_L [d01-d00] Baud Rate

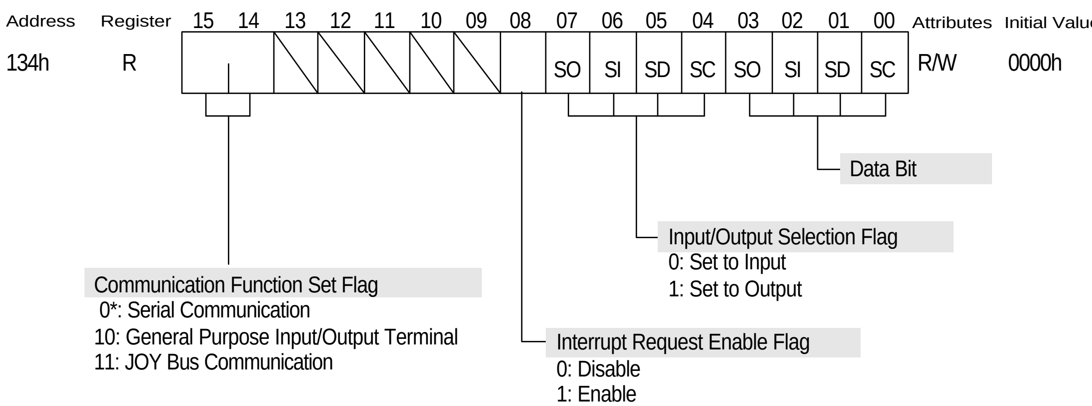
Sets communication baud rate.

Setting	Baud Rate
00	9600 bps
01	38400 bps
10	57600 bps
11	115200 bps

13.4 General Purpose Communication

Setting (d13, d12) = (1, 0) initiates the general purpose communication mode.

In this mode, all of the terminals SI, SO, SC, and SD become pull-up and operate as general purpose input/output terminals. Each of the communication terminals SI, SO, SC, and SD can be directly controlled.



R [d15-d14] Communication Function Set Flag

When set to 00 or 01, operates as a serial communication(8-bit/16-bit serial communication, multi-player communication, UART communication function) terminal.

When set to 10, can be used as a general purpose input/output terminal.

When set to 11, can be used as a JOY Bus communication terminal.

R [d08] Interrupt Request Enable Flag

When general purpose input/output is set(R[d15,d14]=[1,0]) with the communication function set flag, a 1 causes an interrupt request to be generated with the falling of the SI Terminal(edge detect).

When set to 0, no interrupt request is generated.

R [d07-d04] Input/Output Selection Flag

When general purpose input/output is set (R[d15,d14]=[1,0]) with the communication function set flag, a setting of 0 allows the corresponding terminal to be used as an input terminal. A setting of 1 allows the corresponding terminal to be used as an output terminal.

[Caution]

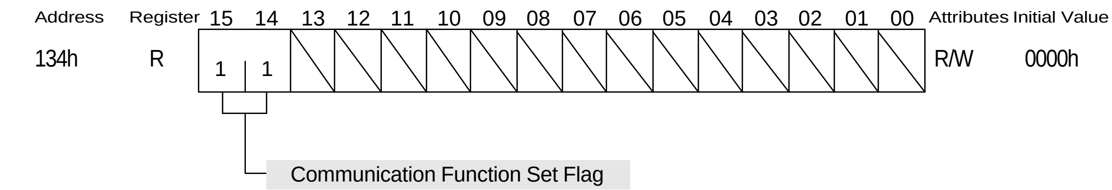
Always set the SI terminal to an input. If it is set to an output, a problem may occur with some connecting equipment.

R [d03-d00] Data Bit

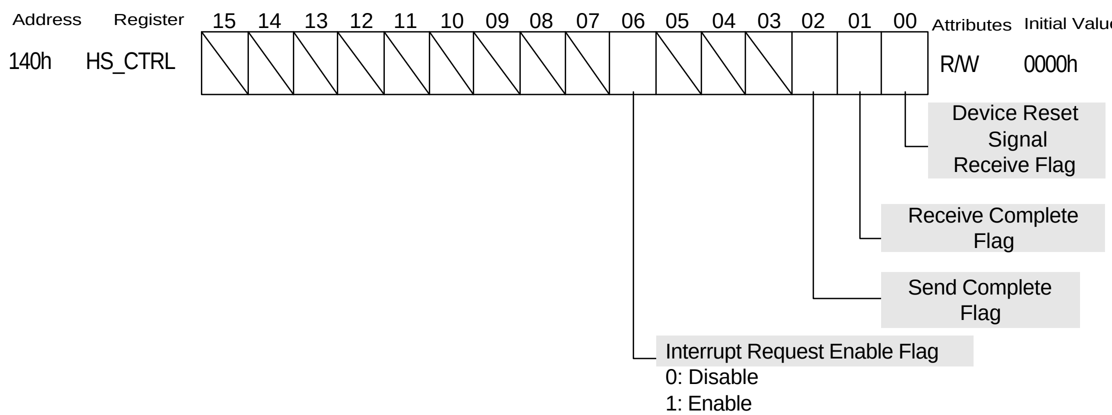
When the corresponding terminal is set for input, the status(HI/LO) of the terminal can be confirmed. If the corresponding terminal is set for output, the status of the set bit is output.

13.5 JOY Bus Communication

By setting the communication function set flag to 11 for Register R, JOY Bus communication mode is selected. In JOY Bus communication mode, the SI Terminal is for input, and SO Terminal is for output. SD and SC Terminals go to LO output.



JOY Bus Communication Control



HS_CRTL [d05] Interrupt Request Enable Flag

When set to 0, an interrupt request is not generated.

When set to 1, an interrupt request is generated once a device reset command is received.

HS_CRTL [d02] Send Complete Flag

Set upon completion of send operation.

When this is set, if you write a 1, a reset can be done.

HS_CRTL [d01] Receive Complete Flag

Set upon completion of receive operation.

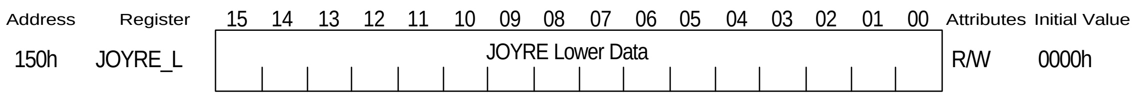
When this is set, if you write a 1, a reset can be done.

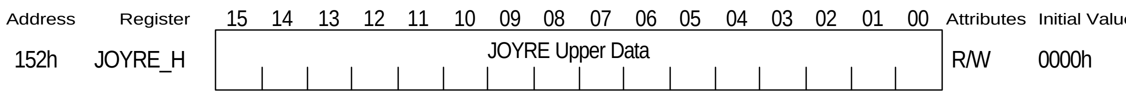
HS_CRTL [d00] Device Reset Signal Receive Flag

Set when a device reset command is received.

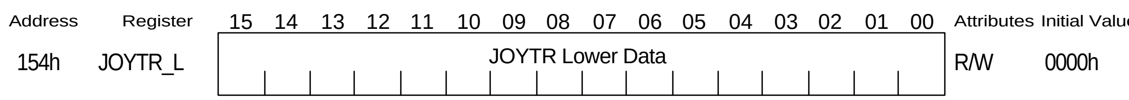
When this is set, if you write a 1, a reset can be done.

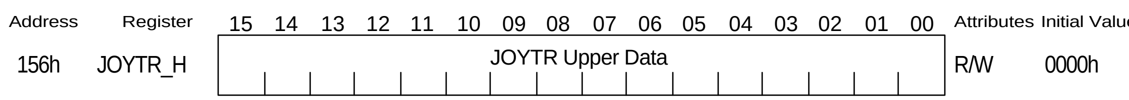
Receive Data Register





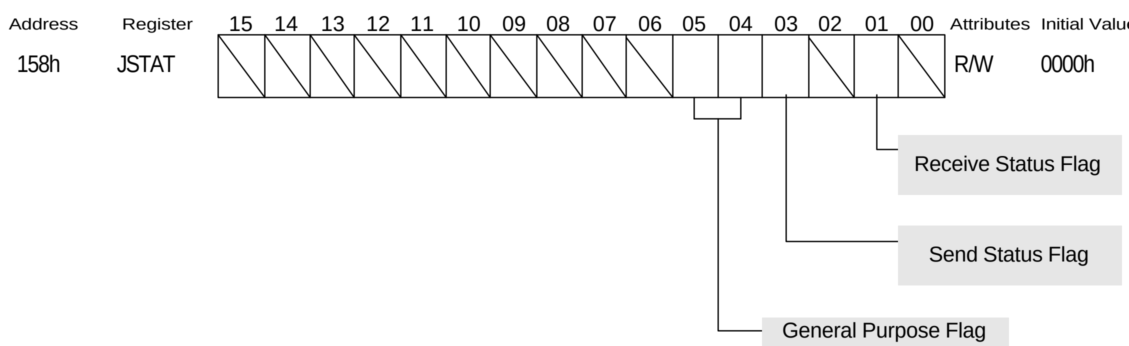
Send Data Register





Receive Status Register

The lower 8-bits of the receive status register JSTAT is returned as the communication status.



JSTAT [d05,d04] General Purpose Flag

This flag is not assigned.

The user can set the use of this flag arbitrarily.

JSTAT [d03] Send Status Flag

When an AGB write data signal is received, this is set. If a word read is done with the JOYRE Register it is reset.

JSTAT [d01] Receive Status Flag

When a word write is done with the JOYTR Register, this is set. If an AGB read data signal is received it is reset.

JOY Bus Communication Operations

AGB JOY Bus communication recognizes four commands sent from the host (N64, etc.): [Device Reset], [Type/Status Data Request], [AGB Data Write], and [AGB Data Read]. AGB operates based on the particular signal received.

The transfer of the bit data for JOY Bus communication is done in units of bytes and in the order of MSB first.

- **[Device Reset] Command(FFh) Received**

The device reset signal receive flag for Register HS_CTRL is set.

If the interrupt request enable flag for the same register is also set, a JOY Bus interrupt request is generated.

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	1	1	1	1	1	1	1	1	Command 255(FFh)
Send	1	0	0	0	0	0	0	0	0	Type Number 0400h
	2	0	0	0	0	0	1	0	0	
	3	Lower 8 bits of Register JSTAT								Communication Status

- **[Type/Status Data Request] Command(00h) Received**

Returns 2 byte type number(0004h) and 1 byte communication status.

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	0	0	0	0	0	Command 0(00h)
Send	1	0	0	0	0	0	0	0	0	Type Number 0400h
	2	0	0	0	0	0	1	0	0	
	3	Lower 8 bits of Register JSTAT								Communication Status

- **[AGB Data Write] Command(15h) Received**

  Receives the 4 bytes of data sent following this command, and stores them in Register JOYRE. Once the receive is completed a 1 byte communication status is returned, and the receive complete flag for Register HS_CTRL is set. Also, if the interrupt request enable flag for the same register is set, a JOY Bus interrupt request is generated.

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	1	0	1	0	1	Command 21(15h)
Receive	2	Lower 8 bits of receive data Register JOYRE_L								Receive Data
	3	Upper 8 bits of receive data Register JOYRE_L								
	4	Lower 8 bits of receive data Register JOYRE_H								
	5	Upper 8 bits of receive data Register JOYRE_H								
Send	6	Lower 8 bits of Register JSTAT								Communication Status

- **[AGB Data Read] Command(14h) Received**

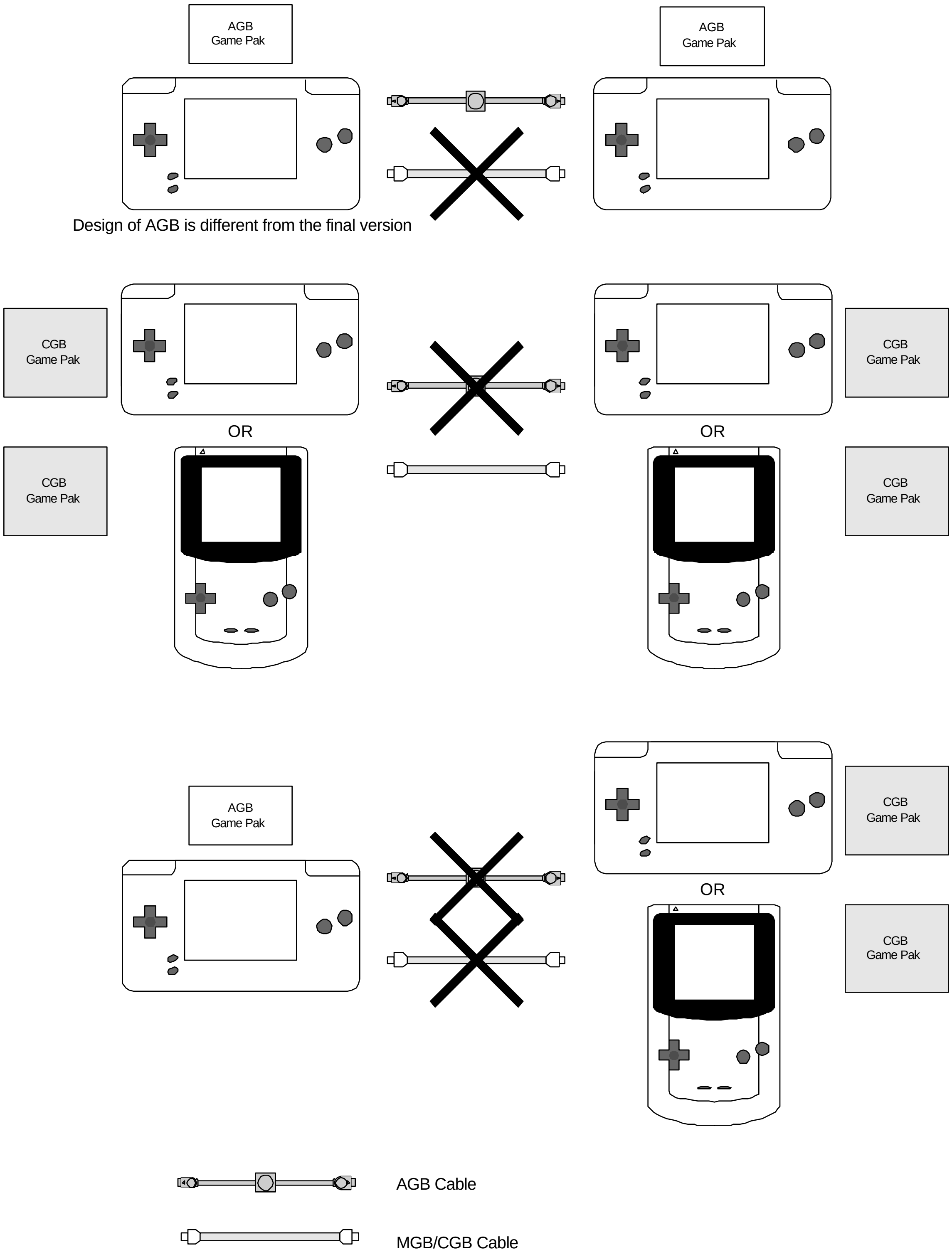
  4 bytes of data stored in Register JOYTR and the 1 byte communication status are sent, and the send complete flag for Register HS_CTRL is set.

  Also, if the interrupt request enable flag for the same register is set, a JOY Bus interrupt request is generated.

Direction	Order	d7	d6	d5	d4	d3	d2	d1	d0	Remarks
Receive	1	0	0	0	1	0	1	0	0	Command 20(14h)
Send	2	Lower 8 bits of send data Register JOYTR_L								Send Data
	3	Upper 8 bits of send data Register JOYTR_L								
	4	Lower 8 bits of send data Register JOYTR_H								
	5	Upper 8 bits of send data Register JOYTR_H								
	6	Lower 8 bits of Register JSTAT								Communication Status

13.6 Communication Cable

When communicating between AGB units, the communication cable to be used will vary depending upon the type of Game Pak used.



14 Key Input

14.1 Key Status

AGB allows input with the L and R buttons, as well as with the START and SELECT buttons, Control Pad, and A and B buttons.

The status of each of these buttons can be checked by reading the individual bits of Register P1.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
130h	P1							L	R	DWN	UP	LFT	RT	ST	SL	B	A	R/W	0000h

Key Status (bits 09–00)
0: Input
1: No Input

14.2 Key Interrupt Control

When an interrupt is performed for key input, this register enables a target key combination or condition for the interrupt to be specified.

Address	Register	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	Attributes	Initial Value
132h	P1CNT							L	R	DWN	UP	LFT	RT	ST	SL	B	A	R/W	0000h

Interrupt Specification Flag (bits 09–00)
0: Not Specified
1: Specified

Interrupt Request Enable Flag (bit 14)
0: Disable
1: Enable

Interrupt Condition Specification Flag (bit 15)
0: Logical Addition (OR)
1: Logical Multiplication (AND)

14.2.1 Interrupt Conditions

Specifies interrupt generation conditions when the interrupt enable request flag is true.

The conditions for buttons selected with the key interrupt specification flag can be selected as follows.

1. Logical Addition (OR) Operation

   The conditions for interrupt request generation occur when there is input for any of the buttons specified as interrupts.

2. Logical Multiplication (AND) Operation

   The conditions for interrupt request generation occur when there is simultaneous input for all of the keys specified as interrupt keys.

15 Interrupt Control

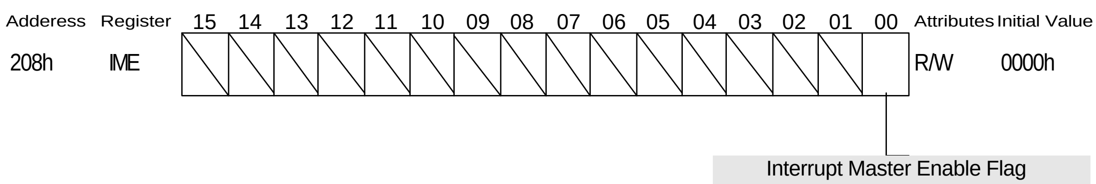
AGB can use 14 types of maskable hardware interrupts. If an interrupt request signal is received from a hardware item, the corresponding interrupt request flag is set in the IF register. Masking can be performed individually for interrupt request signals received from each hardware item by means of the interrupt request flag register IE.

1) Interrupt Master Enable Register

The entire interrupt can be masked.

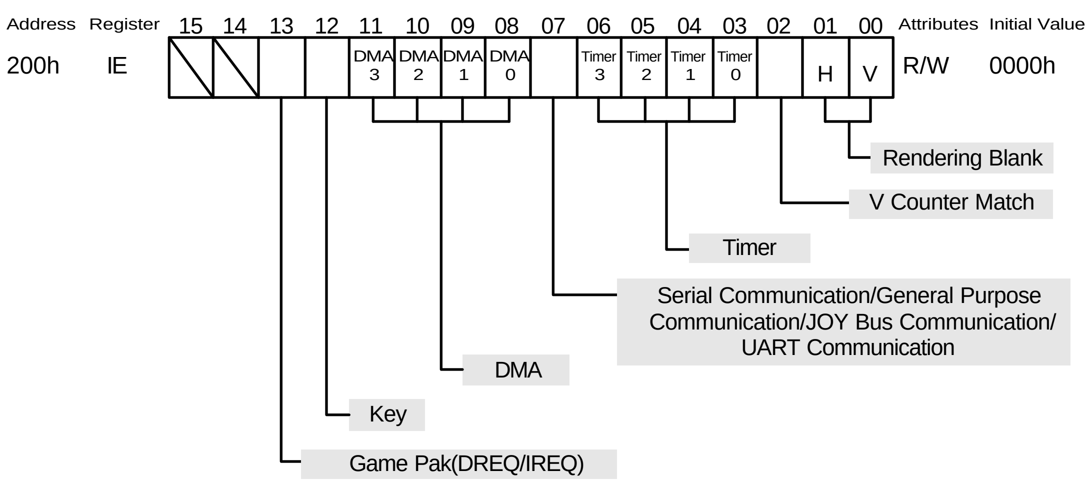
When this flag is 0, all interrupts are disabled.

When 1, the setting for interrupt enable register IE is enabled.



2) Interrupt Enable Register

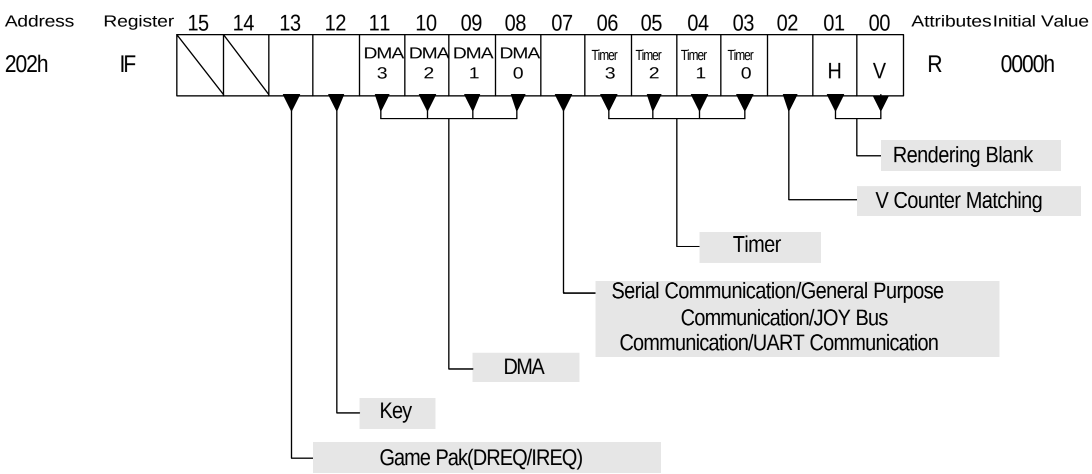
With the interrupt enable register, each hardware interrupt can be individually masked.



By resetting the bit, the corresponding interrupt can be prohibited. Setting this to 1 enables the corresponding interrupt.

3) Interrupt Request Register

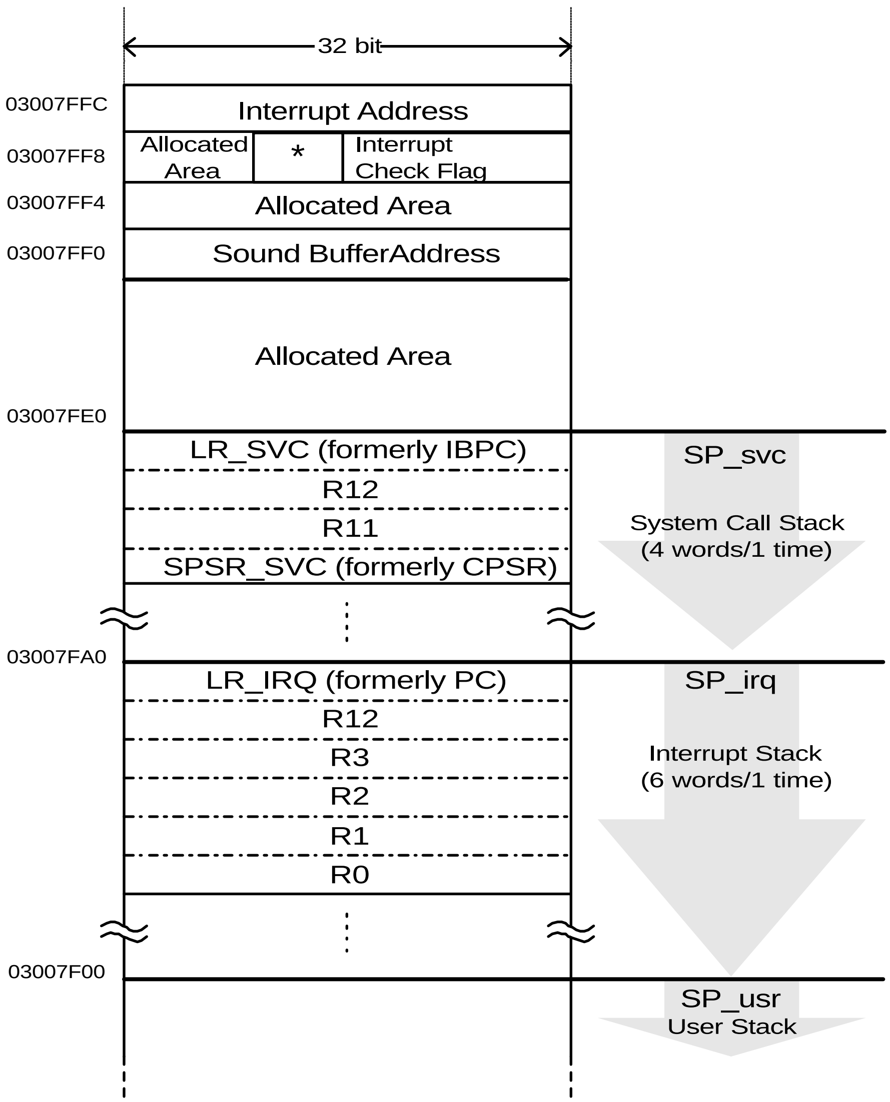
When an interrupt request signal is generated from each hardware device, the corresponding interrupt request flag is set in the IF Register.



If a 1 is written to the bit which the interrupt request flag is set in, that interrupt request flag can be reset

15.1 System-Allocated Area in Work RAM

Controlling interrupts entails, along with clearing the IF register and setting the IE register, first writing an interrupt jump address at addresses $7FFC-$7FFF (total of 32 bits; see figure below) in the system allocated area of Work RAM. Processing is executed in 32-bit mode for the user interrupt. To return control from the interrupt routine to the user program, the instruction “BX LR” is used.



* Specify where to return for SoftReset( ) System Call
If 0h:08000000h
If not 0h:02000000h

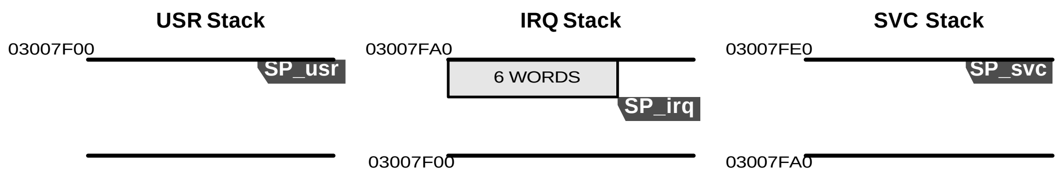
By changing each CPU Mode SP Initial-value, they can be set to an arbitrary memory map.

15.2 Interrupt Operation

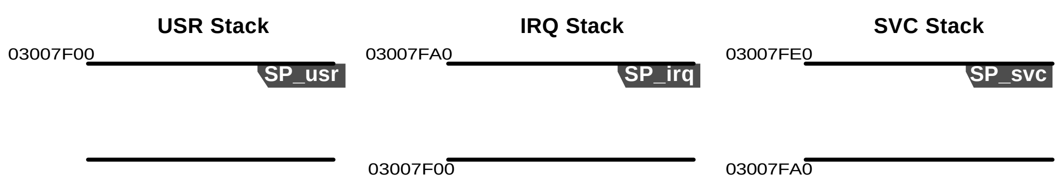
The user can arbitrarily define the Interrupt Processing Routine, but as a general rule, the Monitor ROM handles this processing. For further details on each register, please refer to "ARM7TDMI Data Sheet".

15.2.1 Normal Interrupt

1) If an interrupt occurs, the CPU enters IRQ mode and control shifts to the Monitor ROM. In Monitor ROM, save each register (R0~R3, R12, LR_irq (former PC)) to the Interrupt Stack. The total is 6 words. Next, call the user interrupt processing set up in 03007FFCh. Commands called from the monitor directly must be in 32bit code format.



2) User interrupt processing is done (you can reference the cause of the interrupt with the IF Register). Also solve* problems with a stack, if necessary.
3) Restore the registers (total of 6 words) saved to the Interrupt Stack and return to user main processing.

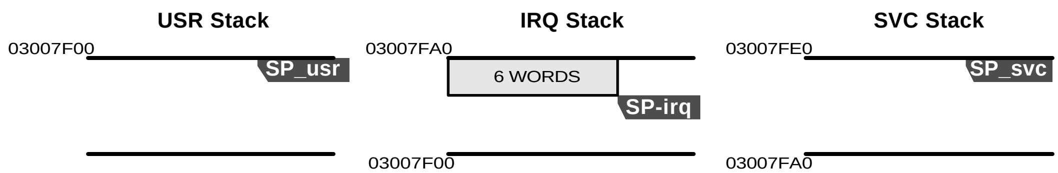


*Note

Only the interrupt stack is used for normal interrupt processing. Therefore, there is a possibility of stack overflow in some cases. To solve this problem, you can either allocate a larger interrupt stack by moving SP_usr in advance or use user stack for both, by switching the CPU mode to the user mode in user interrupt processing. For the latter method, see the explanation of multiple interrupts that is discussed on the following page.

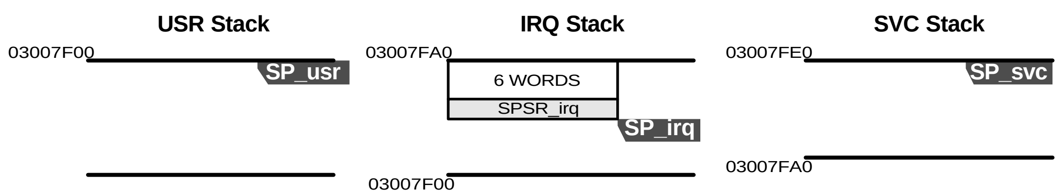
15.2.2 Multiple Interrupts

1) If an interrupt occurs, the CPU enters IRQ mode and control shifts to the Monitor ROM. In Monitor ROM, save each register (R0~R3, R12, LR_irq (former PC)) to the Interrupt Stack. The total is 6 words. Next, call the user interrupt processing set up in 03007FFCh. Commands called from the monitor directly must be in 32bit code format.



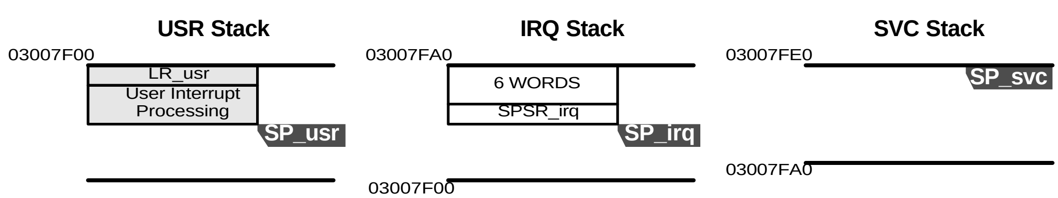
2) User interrupt processing is done (you can reference the cause of the interrupt with the IF Register).

→ If multiple interrupts occur, SPSR_irq will be overwritten, so you must save before enabling IRQ.

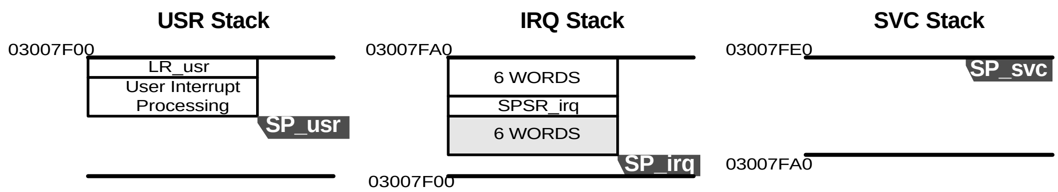


→ The Stack problem is solved* (CPU mode is changed to user mode with system mode—privilege here.) and IRQ is enabled.

→ With user interrupt processing, user stack is used because the CPU is in system mode. When calling the subroutine, save LSR_usr as well.



→ When an interrupt occurs, Monitor ROM does the processing (1) again, and loads each register to the interrupt stack.



→Continue processing (2).

16 Power-Down Functions

16.1 Stop Function

Stop Function Summary

During periods when the LCD display is not done and CPU processing is not considered essential you can reduce power consumption greatly if used efficiently.

The content of each type of RAM are maintained.

Implementing Stop

1) Implementation of Stop Mode

AGB is placed in stop mode by executing the system call [SWI <3>] instruction (Stop( ))

2) Canceling Stop Mode

If the appropriate interrupts are enabled in the interrupt enable register IE, for each interrupt request for the key, Game Pak and SIO (general purpose communication mode), Stop is cancelled.

[Note]

Canceling stop status requires a brief wait until the system clock stabilizes.

System Working Status in Stop Mode

The working status of each block of the AGB system during a stop is shown in the following table.

Block	Working	Status
AGB-CPU	X	Wait status resulting from wait signal
LPU	X	Stopped because no clock provided*
Sound	X	Stopped*
Timer	X	Stopped
Serial Communication	X	Stopped
Key	X	Stopped
System Clock	X	Stopped
Infrared Communication	X	Stopped

*Note
Enter Stop Mode after turning the LCD display OFF because LPU stops.
Sound stops in Stop Mode, therefore noise may be heard.

16.2 Halt Function

Halt Function Summary

During periods when CPU processing is not considered essential you can reduce power consumption if used efficiently.

Halt Transition Method

1. Transition to Halt Mode

   AGB is placed in halt mode by executing the system call [SWI <2> instruction (Halt( )).

   AGB enters Halt status.

2. Cancel Halt Mode

   Halt is canceled when the interrupt enable register IE's corresponding flag is set with any type of interrupt request.

System Working Status in Halt Mode

The working status of each block of the AGB system during a semi-stop is shown in the following table.

Block	Working	Status
AGB-CPU	X	Wait status resulting from wait signal
LPU	○	Normal operation
Sound	○	Normal operation
Timer	○	Normal operation
Serial Communication	○	Normal operation
Key	○	Normal operation
System Clock	○	Normal operation

17 AGB System Calls

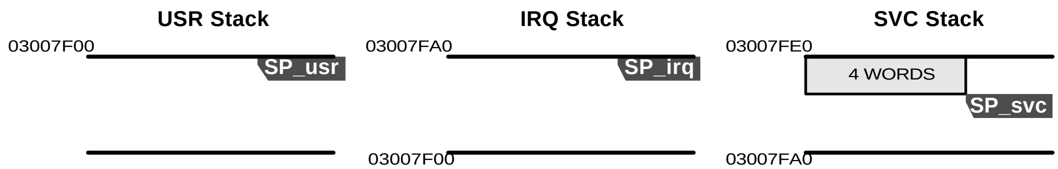
Please refer to the AGB System Call Reference Manual for AGB system calls.

17.1 System Call Operation

17.1.1 Normal Calls

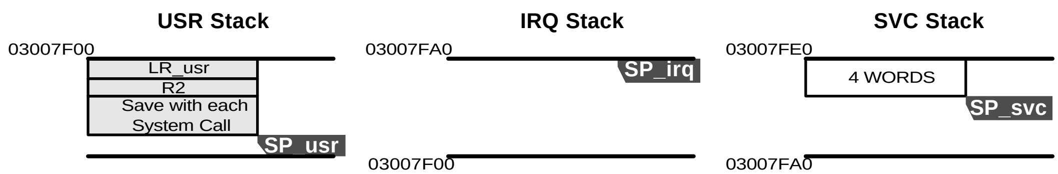
1) When an argument is required for the system call used, after writing to registers R0-R3 call the monitor ROM system call with the “SWI<Number>”. The CPU mode changes to Supervisor Mode.

2) Save the registers, SPSR_svc (formerly CPSR), R 11, R12, LR_svc (formerly PC) to the system call stack with the monitor ROM.

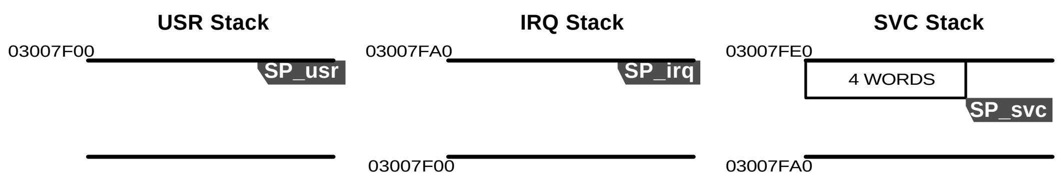


3) Switch from CPU mode to system mode. Call the IRQ disable flag with monitor ROM. The previous status will continue.

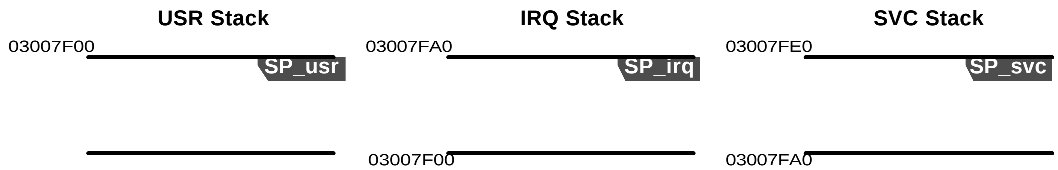
4) Save the R2 and LR_usr registers to the user stack. Other registers will be saved with each system call.



5) Complete processing using each system call.



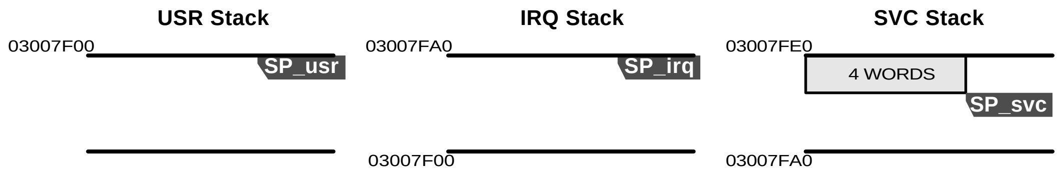
6) Return value to registers R0, R1, and R3, in cases where a system call provides a return value, and then return to the user program.



17.1.2 Multiple Calls

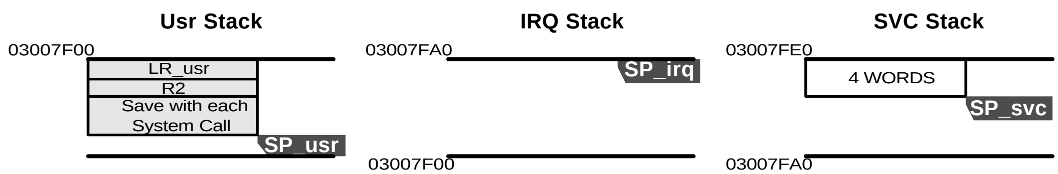
1) When an argument is required for the system call used, after reading to the registers, R0-R3, call the monitor ROM system call with the “SWI<Number>”.

2) Save the registers, SPSR_svc (formerly CPSR), R12, LR_svc (formerly PC) to the system call stack with the monitor ROM.

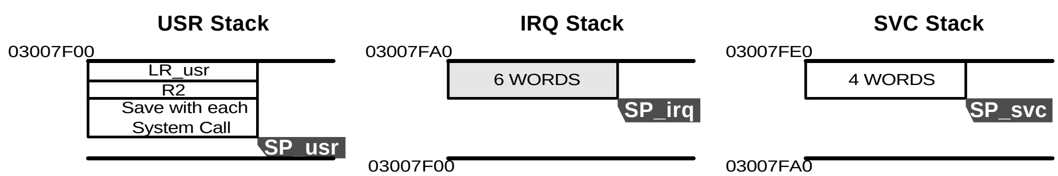


3) Switch from CPU mode to system mode. The status of the IRQ Disable Flag prior to the call is kept in System ROM. The previous conditions will be continued.

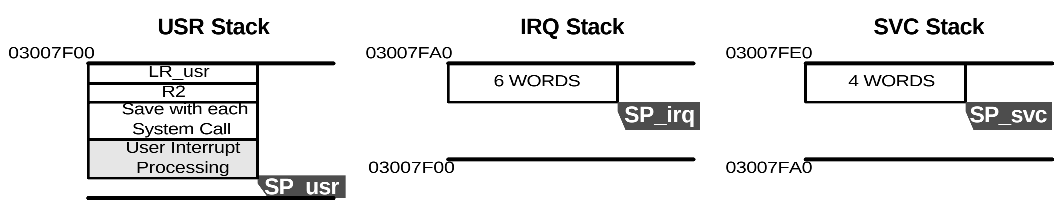
4) Save the R2 and LR_usr registers to the user stack. Other registers will be saved with each system call.



5) Interrupt occurs while executing system call.

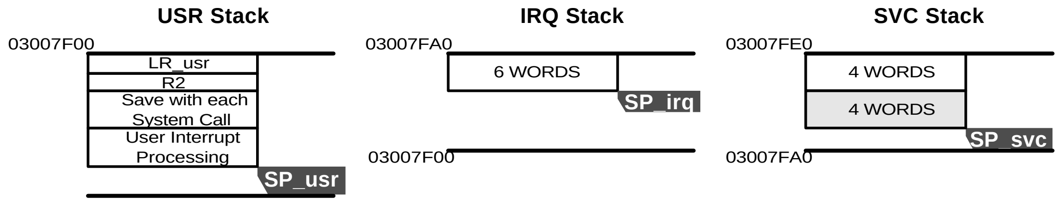


6) User interrupt processing is done. (You can reference the cause of the interrupt with the IF Register.) The CPU mode is changed to System Mode (User Mode with privilege) in order to solve the problem with stacks (to reference interrupt processing).



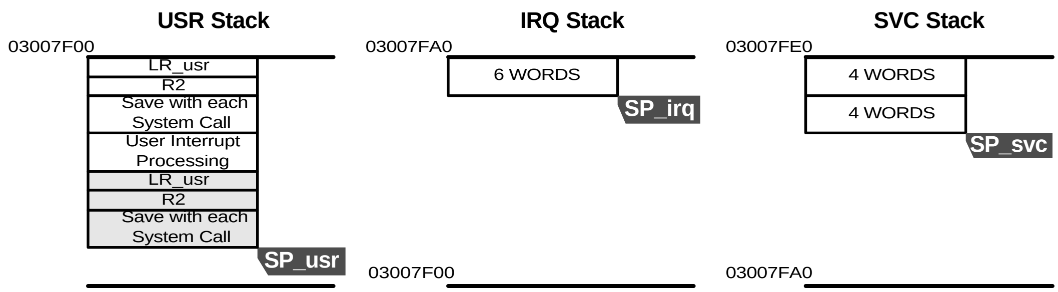
→If System Call occurs during User interrupt processing, the System Call is called using Multiple Calls.

7) Monitor ROM does the system call operation (1), and loads to the system call stack.

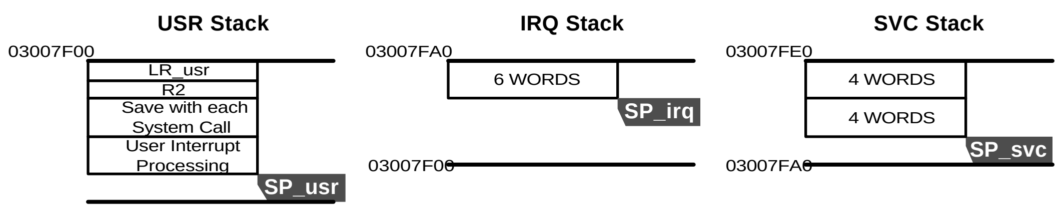


8) Switch the CPU Mode to System Mode (privileged user mode).

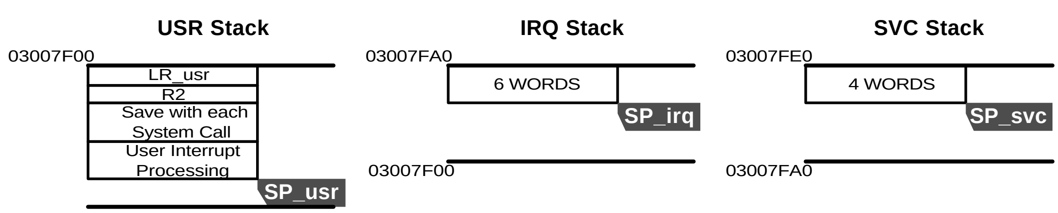
9) Monitor ROM does the same operation as (3), and loads to the user stack.



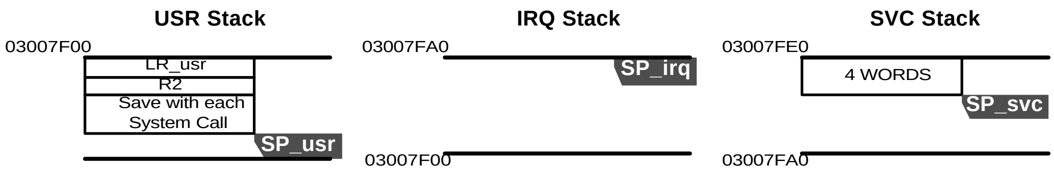
10) Complete processing with each system call.



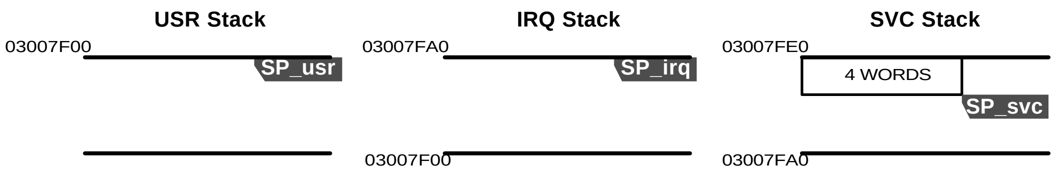
11) Return value to registers R0, R1, and R3, in cases where a system call provides a return value, and then return to the user interrupt processing.



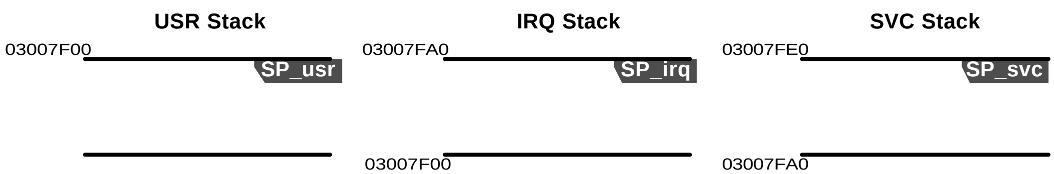
12) Complete the user interrupt processing and return to the previous system call.



13) Complete processing with each system call.

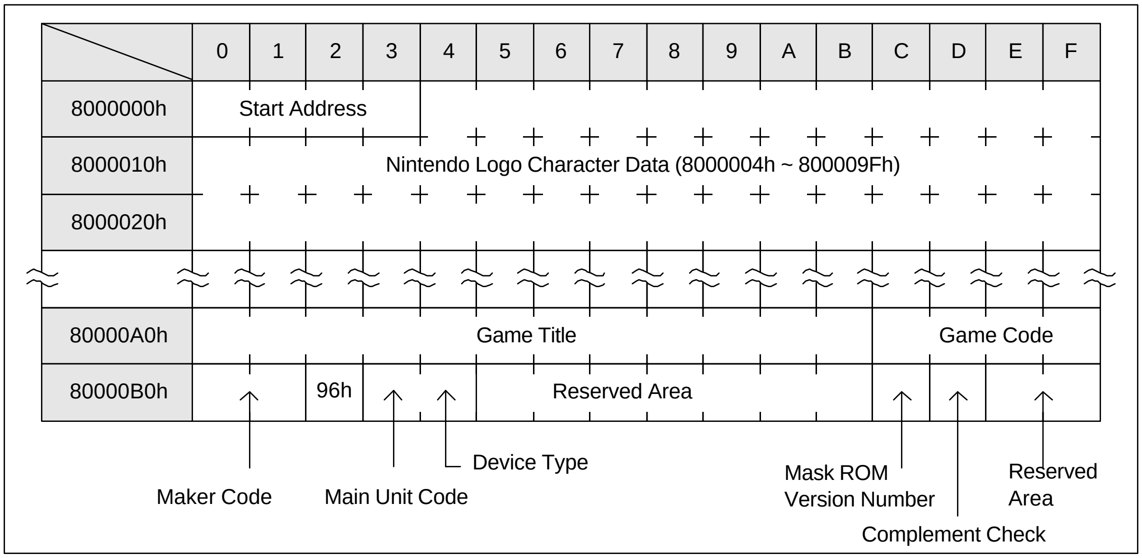


14) Return value to registers R0, R1, and R3, in cases where a system call provides a return value, and then return to the user program.



18 ROM Registration Data

As with software for CGB, it is necessary to register information about the game in the program area for AGB software.



Start Address

Store the 32-bit ARM command “B<User program start address>”.

Nintendo Logo Character Data

The Nintendo logo/character data, which is displayed when the game is started, is stored here. The Monitor ROM checks this data at start-up, therefore always store the data provided by Nintendo.

Game Title

Store the Game title in this area.

Game Code

Store the Game Code provided by Nintendo in this area.

Maker Code

The Maker Code, determined by the "maker" of the software and Nintendo, is stored here.

96h

Store the fixed code "96h".

Main Unit Code

Store the code for the hardware on which the software is intended to run.

Device Type

Store the type of device that is installed in the Game Pak. If there is a 1 Mbit flash DACS (Debugging And Communication System) (=custom 1Mbit flash Memory with security and patch functions) in a Game Pak, set the most significant bit to 1. Otherwise it is reset. Other bits are system allocated area.

Reserved Area

This is a system allocated area. Set this area to 00h.

Mask ROM Version No.

Store the ROM version number here.

Complement Check

The 2's complement of the total of the data stored in address 80000A0h ~ 80000BCh plus 19h is stored in this location.

Reserved Area

This is a system allocated area. Set this area to 00h.