CCD CHIP LAYOUT DESIGN

Device Architecture

The device architecture of a Charge-Coupled Device (CCD) consists of linear five arrays, with each linear array comprising 6000 pixels. *Fig. 4. 1 One Linear Array of CCD* illustrates the structure of one such linear array, which includes distinct sections such as the imaging area, bias, storage, transfer, two-phase HSR (Horizontal Shift Register), and output sections. Understanding the architecture of a single linear array is crucial to comprehending the overall CCD design.

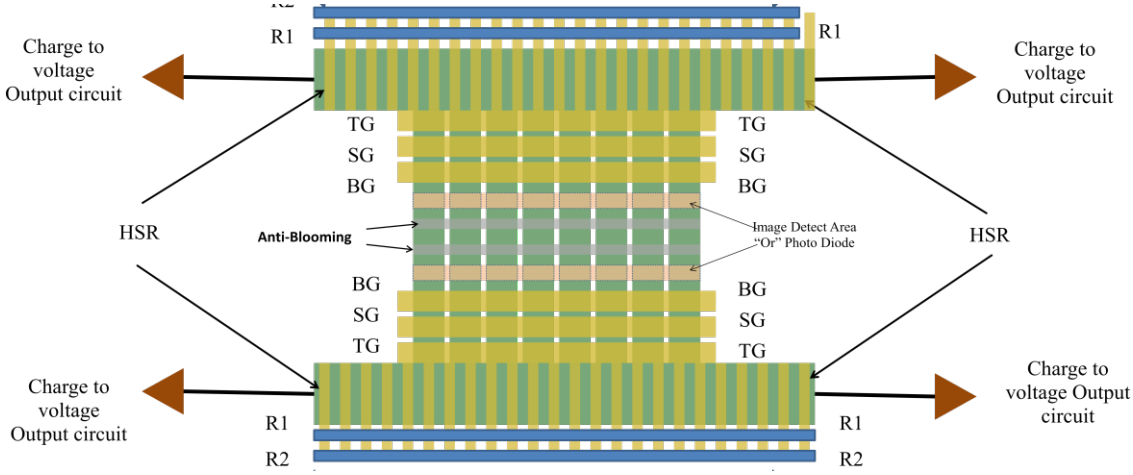

Fig. 4. 1 One Linear Array of CCD

Starting with the photodiode (imaging area), it is the portion of the linear array that captures incoming light and converts it into electrical charges. The storage and bias section allow the charges collected in the imaging area to be temporarily stored before being read out. The two-phase HSR plays a vital role in transferring the charges from the transfer areas to the output section. It utilizes a two-phase clocking mechanism, where the charges are shifted in a controlled manner along the linear array. This transfer is necessary to sequentially read out the charges from each pixel. The output section is responsible for converting the charge signals into voltage signals. In the *Fig. 4. 1 One Linear Array of CCD* anti- blooming section located above bias section which typically implemented as a separate region within the CCD, acts as a barrier to prevent the charge from spilling over into neighboring pixels. It accomplishes this by providing a path for the excess charge to drain away, rather than spreading to surrounding pixels. Each linear array has four readouts that perform charge-to-voltage conversion and subsequent amplification of the signals. This amplification ensures that the charge signals are robustly captured and ready for further processing. Comprehending the architecture of one linear array, we gain insight into the overall structure of the CCD.

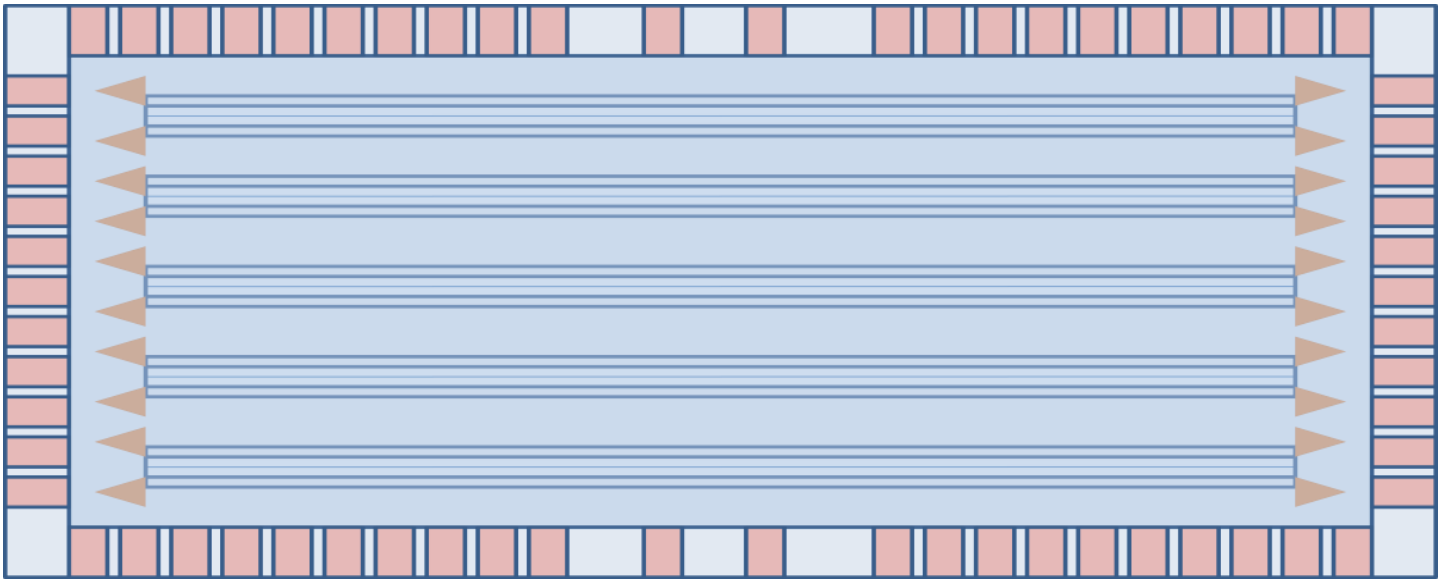

Fig. 4. 2 Architecture of five linear array CCD

The CCD chip architecture consists of linear five arrays, each separated by a spacing of 2.4mm. The peripheral area of the CCD chip contains a total of 280 pads. There are 20 readouts for charge-to-voltage conversion and amplification. The chip also has two metal routing subfields on the right or left side for clock and output signals.

Cadence Virtuoso Software:

Cadence Virtuoso is a powerful suite of EDA (Electronic Design Automation) tools that are widely used in the design and verification of complex digital and analog circuits. The Virtuoso suite includes both schematic capture and layout tools, as well as simulation and verification tools, allowing designers to create, test, and refine their designs in a single integrated environment.

Virtuoso Layout is a powerful layout tool that allows designers to create physical layouts of their circuits. It provides a wide range of features and functions to help designers create layouts that are both efficient and manufacturable. Virtuoso Layout supports a wide range of design rules and constraints, allowing designers to ensure that their layouts meet the specific requirements of the semiconductor foundry. Some of the key features of Virtuoso Layout include:

- **Customizable layout environments:** Virtuoso Layout provides a customizable environment that allows designers to create layouts that meet their specific needs. It allows designers to customize menus, toolbars, and shortcuts to speed up the layout process and improve productivity.

- **Advanced routing capabilities:** Virtuoso Layout provides advanced routing capabilities that allow designers to create complex routing topologies quickly and efficiently. It includes a range of routing tools, including interactive routing, auto routing, and automatic via insertion, to help designers optimize their routing for performance and manufacturability.

- **Design rule checking (DRC):** Virtuoso Schematic Design includes advanced DRC capabilities that allow designers to check their schematics against the specific design rules and constraints of the semiconductor foundry. This helps ensure that the schematic is manufacturable and meets the requirements of the foundry.

- **Advanced editing tools:** Virtuoso Layout includes a range of advanced editing tools that allow designers to make precise changes to their layouts. It includes features such as move, stretch, rotate, and resize, as well as advanced editing functions such as merging and splitting polygons.

Pixel Layout Design:

In this project, we have designed a pixel architecture with which includes multiple sections, including 16 x 16 µm size photodiode , transfer , storage , bias , and anti-blooming , as well as a two-phase HSR for horizontal charge transfer. Here in my project, I have created a pixel design consisting of 4 pixels, each pixel is of 16 x 16 um measurements in each pixel block and HSR region measuring 87 um vertically, as shown in *Fig. 4. 4 Layout Design of image area of* **photodiode** and *Fig. 4. 5 Layout Design of HSR region of photodiode,* respectively.

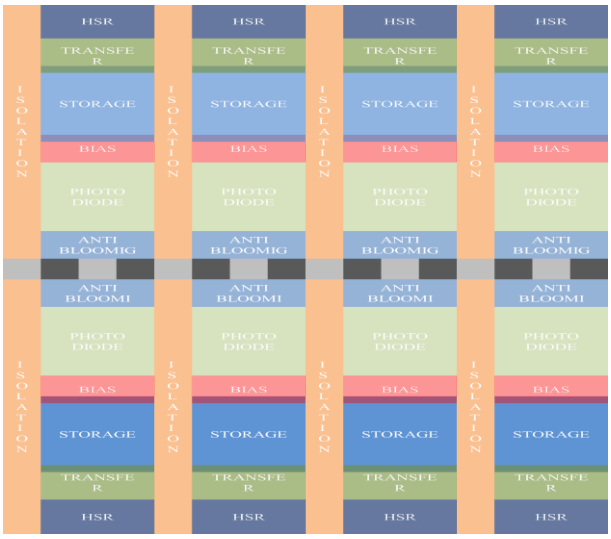

Fig. 4. 3 Layout Architecture of Pixel

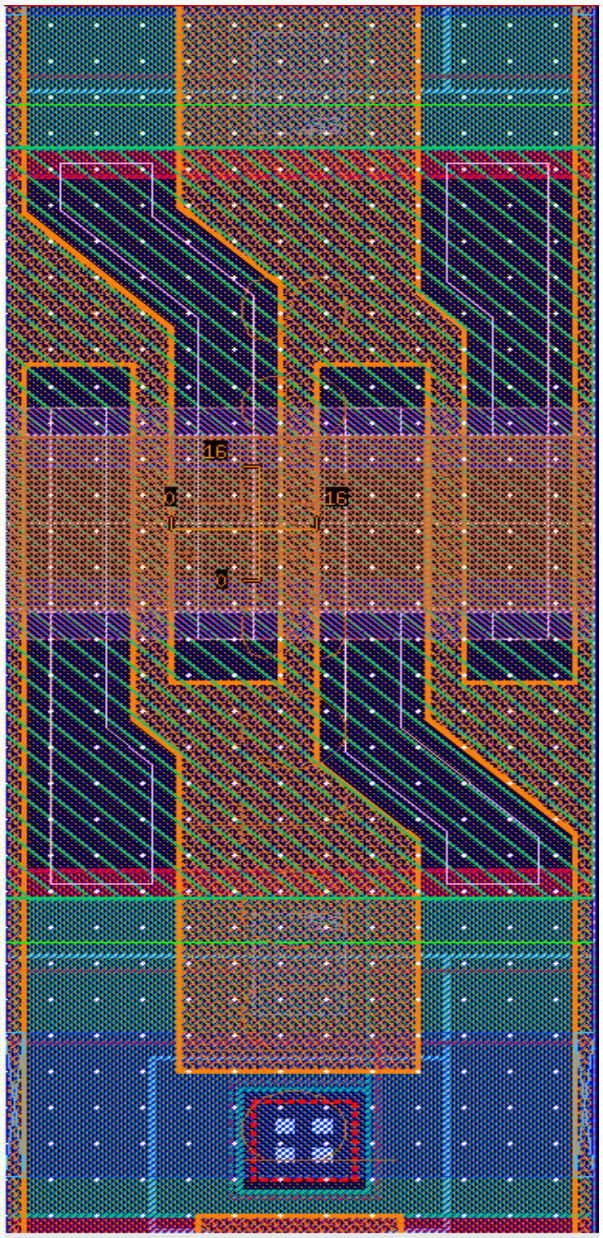

Fig. 4. 4 Layout Design of image area of photodiode

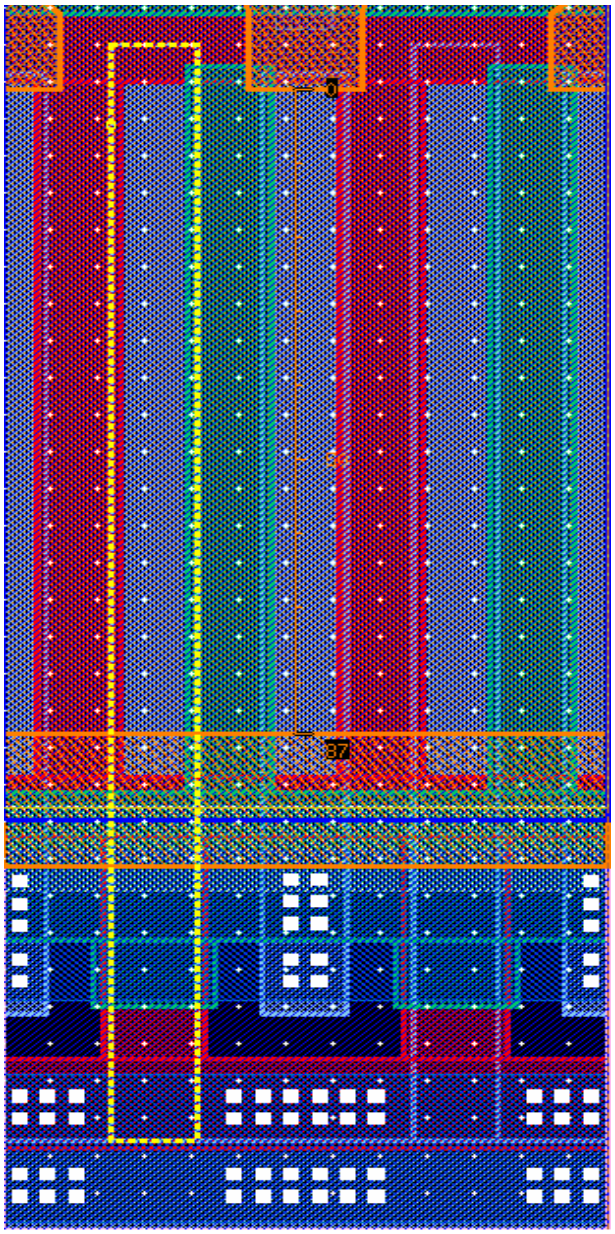

Fig. 4. 5 Layout Design of HSR region of photodiode

Image Area: In the configuration of photodiodes within charge-coupled devices (CCDs) through the utilization of Cadence software, the term "image area" commonly denotes the specific area where incoming light is absorbed, resulting in the creation of electron-hole pairs, which are subsequently gathered and conveyed through the CCD framework for the purpose of reading and processing. The image region within the configuration of photodiodes in CCDs using Cadence encompasses the physical layout components like anti-blooming gate and drain, polysilicon layers, channel stop, etc. From the *Fig. 4. 4 Layout Design of image area of photodiode,* it is visible that in order to make anti-blooming gate we formed an aperture like structure consisting of LLD and NPLD connected to polysilicon layer via contacts (small square structures inside the red box).

HSR Region: In the context of layout design for photodiodes in charge-coupled devices (CCDs) utilizing Cadence software, the term "HSR region" commonly denotes the "Horizontal Shift Register" region. The Horizontal Shift Register constitutes a necessary element within a CCD framework that helps in the horizontal transfer of charge packets across the pixel array during the readout phase. Within the domain of Cadence layout design, the HSR region include some layout components like the polysilicon gates, implant regions, and metal interconnects that configure the shift register electrodes and channels. Typically positioned adjacent to the photodiode array, this region is accountable for the sequential transfer of charge packets from each pixel to the output amplifier or readout circuitry. As shown in *Fig. 4. 5 Layout Design of HSR region of photodiode,* there is a ruler marking 87 um which is the width of HSR. A resistance was calculated and in order to decrease value of resistance we reduced the width of HSR, the overall resistance decreased and therefore after few iterations this final width of 87 um was fixed.

Routing Cell of linear array CCD:

Subfield metal routing involves the routing of metal interconnects within the CCD. This includes the routing of clock signals, data lines, and other critical paths. The routing layout needs to be carefully designed to minimize signal crosstalk, reduce resistance, and maintain appropriate current densities. The track width of the routing traces becomes crucial, as it affects the efficiency and performance of the CCD. Different clock signals may require varying track widths to accommodate their respective current densities. Device pad placement is another important consideration. The pads serve as the interface between the CCD chip and the external world, allowing for electrical connections and signal transfer. The placement of these pads should be strategically determined to facilitate optimal signal routing and minimize parasitic effects. Proper pad placement ensures efficient and reliable communication between the CCD and external circuitry.

In the routing process, both output tracks and clock signal tracks need to be carefully planned and implemented. Output tracks are responsible for carrying the CCD's output signals, transmitting them to the appropriate external circuitry. Clock signal tracks, on the other hand, are dedicated to carrying the clock signals throughout the CCD to ensure proper synchronization and timing.

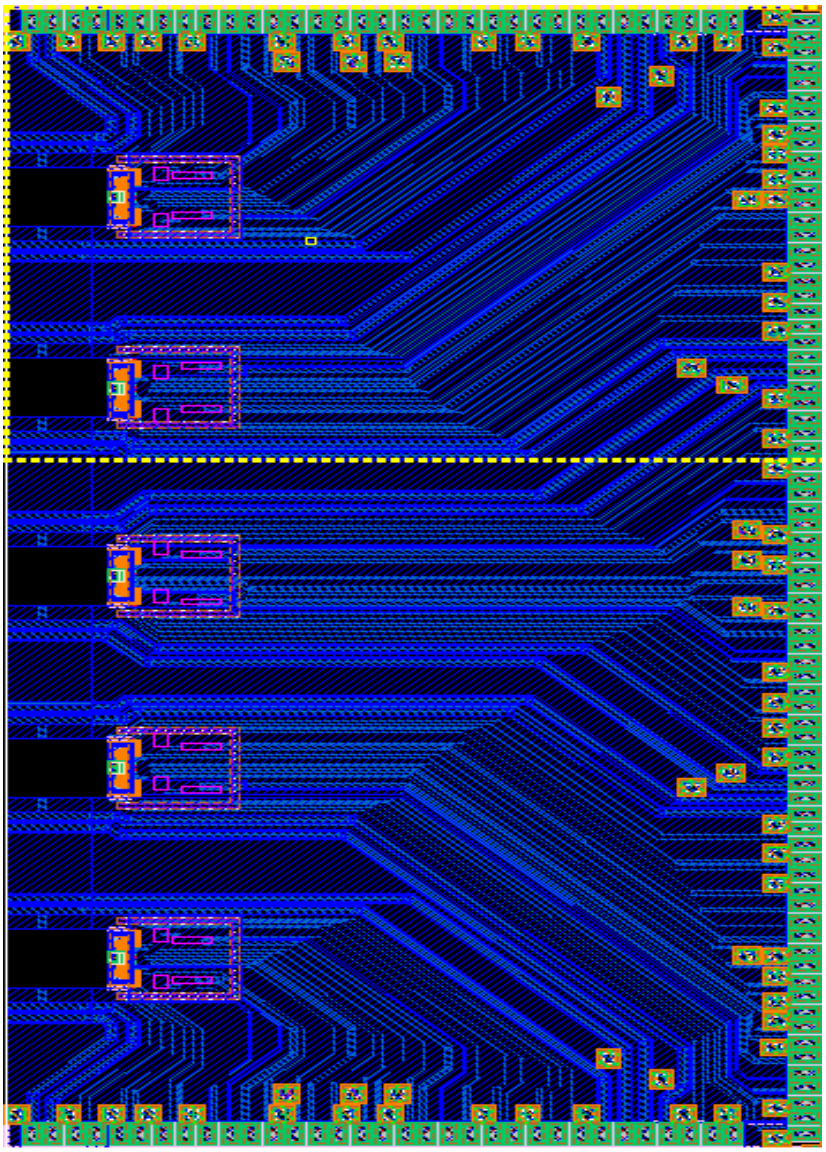

Fig. 4. 6 Routing of the linear five array CCD

Full Length CCD Chip:

The overall size of the CCD chip is 108000 × 12000 µm, which is large enough to accommodate all the required sub-cells and routing. As the CCD too large accommodate in single fabrication lithography. So, full device is designed in multiple subfields, which will stitch while lithography.

To realize the full CCD chip with the specified subfields, a specific pattern can be followed. The pattern consists of subfield A at the center of the CCD chip, subfield B repeated 7 times on the right side of the CCD, subfield C repeated 7 times on the left side of the CCD, subfield D on the extreme right end side of the CCD chip, and subfield E on the extreme left end side of the CCD chip. Additionally, metal routing and pad placement will be incorporated in subfields D and E.

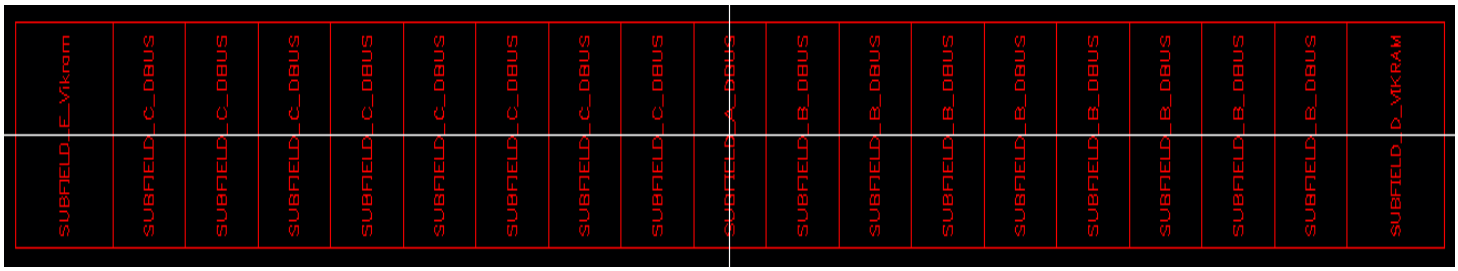

Fig. 4. 7 Cell Stitching view

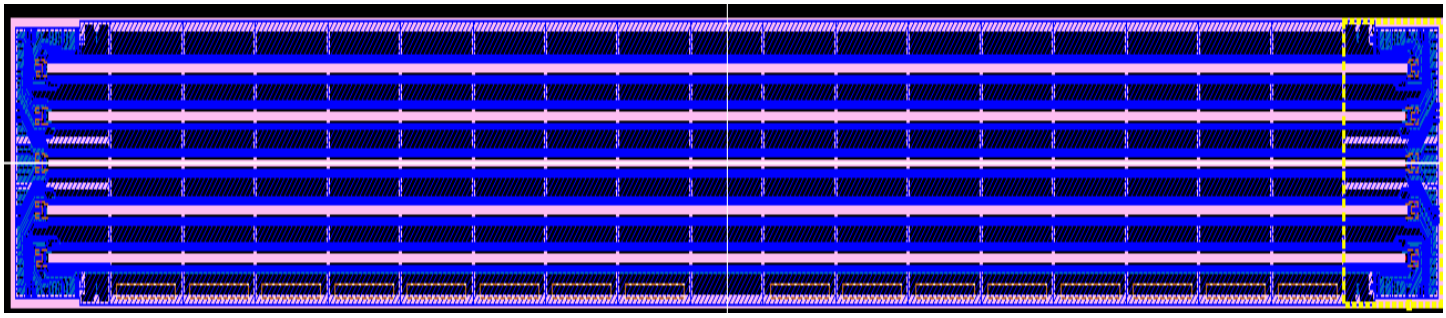

Fig. 4. 8 Linear five array CCD

MODELLING and SIMULATION RESULTS

Schematic Design of Pixel:

The schematic design of the pixel is a critical step in the design process, as it involves creating a electrical circuit of the pixel that accurately represents the layout design and that the required resistance and capacitance values are achieved. To calculate the resistance and capacitance values. The resistance value was computed using the product of the metal and poly silicon layers, while the capacitance value was computed using dimensions of the gate oxide and depilation region. Once the resistance and capacitance values were calculated, used Cadence Virtuoso to design the schematic design of the pixel.

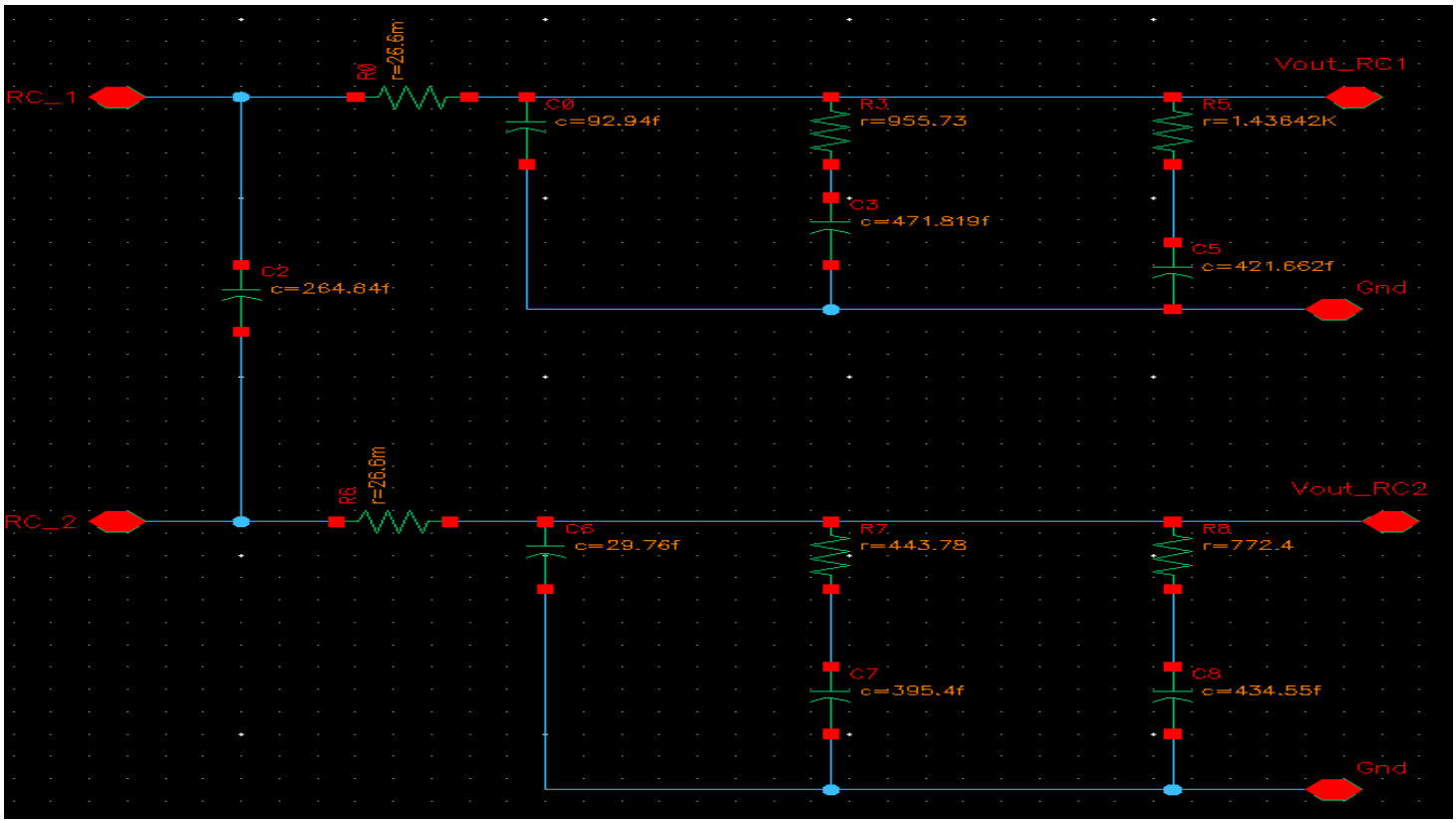

Fig. 5. 1 Schematic Design of pixel

After the schematic design of one pixel, the next step in the project was to create a full- length CCD schematic design.

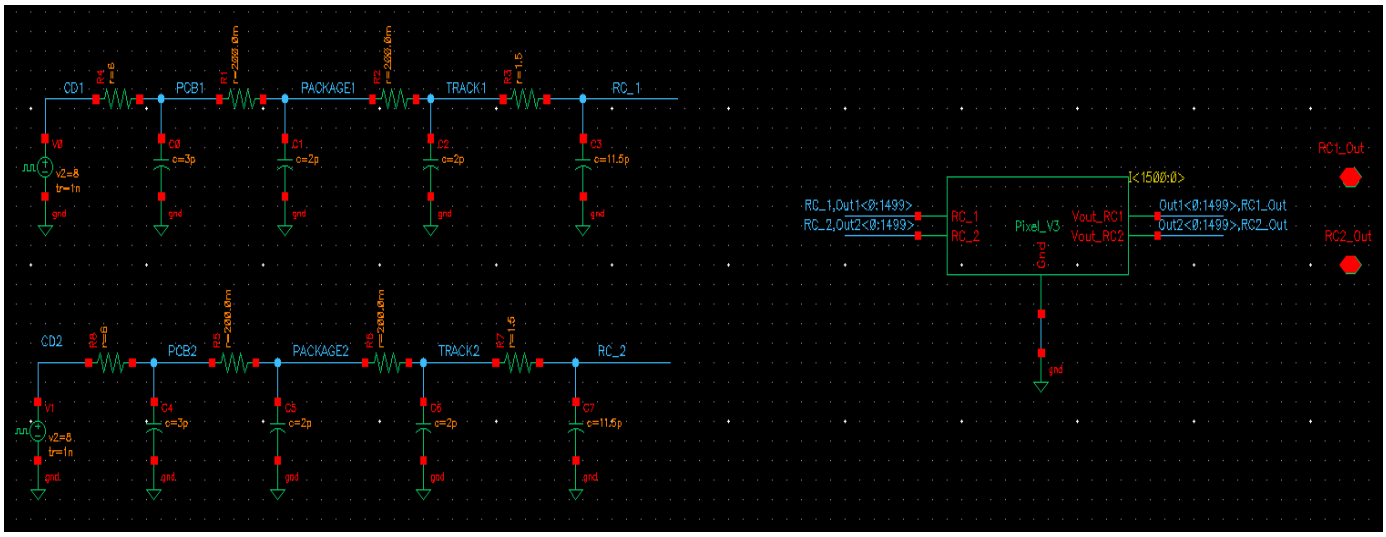

Fig. 5. 2 Full Array CCD Schematic design

The full array CCD schematic design, it is important to consider the effects of package, PCB (Printed Circuit Board), and track path resistance and capacitance. The package and PCB form the outer part of the CCD image sensor assembly. The package contains the CCD chip and provides mechanical and electrical connections to the external world. The PCB provides the necessary interconnections between the CCD and other components of the system. The schematic layout of the CCD array was critical for visualizing and analyzing the simulation results.

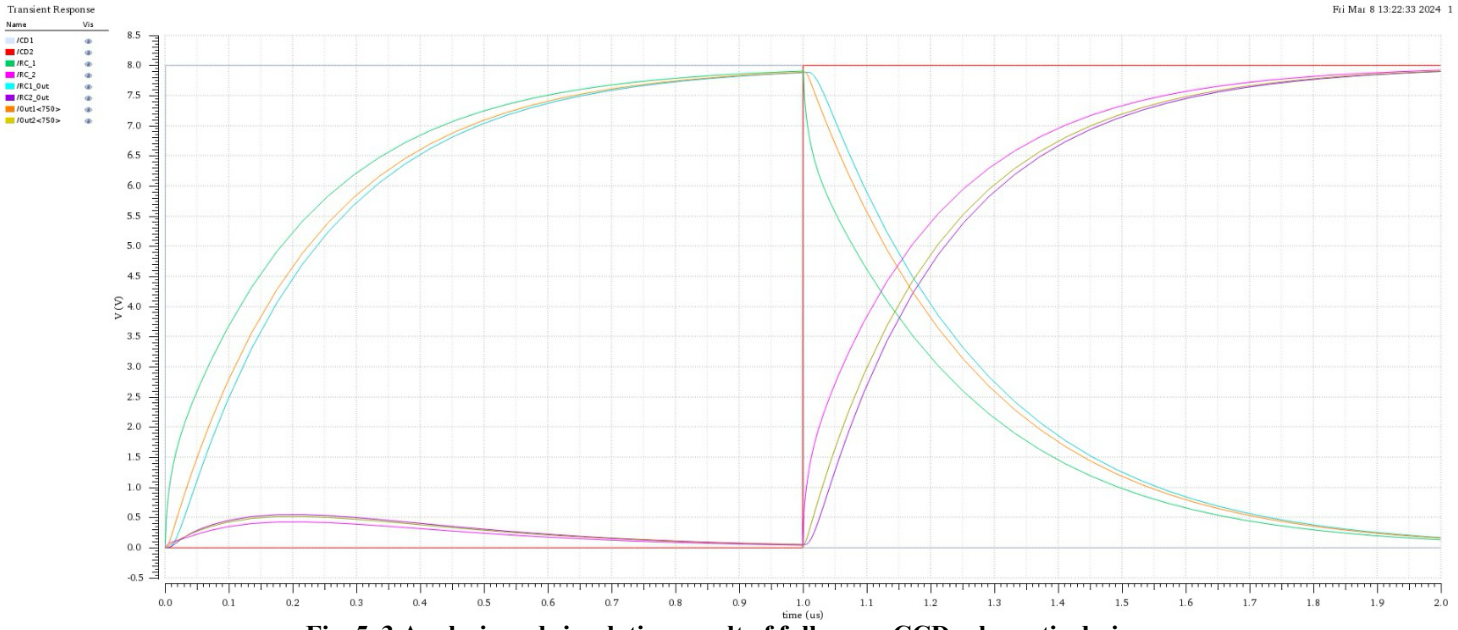

Fig. 5. 3 Analysis and simulation result of full array CCD schematic design

In the schematic diagram shown in *Fig. 5. 2 Full Array CCD Schematic design,* it is clearly shown that two different clock signals, namely RC_1, and RC_2 are provided to the CCD. These clock signals have specific characteristics such as amplitude, rise time, fall time, inter-clock delay, and coupling delay. It is observed that the output signals, out1 and out2, exhibit high rise and fall times compared to their corresponding input signals, RC_1 and RC_2. The simulation results showed that the signals did not meet the timing and signal amplitude for the critical path, leading to large rise and fall times and delays in the charge transfer process. So that, we worked to optimize the timing of the bias and storage gate signals to ensure that they meet the required specifications.

Reducing Rise Fall and Delay Time:

As mentioned in the previous section, the simulation results showed that the rise and fall times of the bias and storage gate signals were too large, leading to significant delays in the charge transfer process.
One of the solutions to this challenge was to optimize the RC value of the signal path to reduce the delay time and improve the overall performance of the CCD array. To reduce the resistance value of the signal path, we had implemented a metal strapping technique on the poly silicon layer. By adding metal straps to the poly silicon layer, the effective resistance of the signal path was significantly reduced, as the resistance of the metal is much lower than that of the poly silicon.

The multiple simulations to evaluate the effectiveness of the metal strapping technique in reducing the resistance and optimizing the RC value of the signal path. The results showed a significant improvement in the rise and fall times of the signals, as well as a reduction in the delay time. In addition to the metal strapping technique, we also optimized other factors that could impact the RC value and performance of the CCD array, such as the dimensions of the signal path, the thickness of the metal and poly silicon.

Through various iterations and because of metal strapping we were able to reduce the resistance of RC_1 and RC_2. Therefore, through careful analysis and optimization, we were able to significantly reduce the rise and fall times and delay time of the signals, and signal meet required specifications.

Design Rule Checks (DRC):

- Design Rule Check (DRC) is a crucial tool used in semiconductor industry to ensure that the design of a chip adheres to the specific design rules provided by the manufacturer. The DRC process is typically carried out using software tools such as Calibre, which is a product of Menter Graphics.

- Design rules are a set of parameters that specify the physical and electrical requirements that a chip must meet in order to function correctly. These rules are provided by the semiconductor manufacturer and typically cover a wide range of parameters such as minimum feature size, spacing between features, and metal line width and spacing.

- The DRC tool checks the design of the chip against these design rules to identify any violations that may cause the chip to malfunction or fail. The DRC tool is a critical step in the design process as it helps to identify potential issues early in the design process, before any masks are fabricated.

- Calibre is a widely used DRC tool that provides a comprehensive set of design rules that are specific to the manufacturer's process. It also allows designers to define their own custom design rules to check for specific issues that may be unique to their design.

- We have identifying design violations; necessary correction was made to resolved them. Once this correction was completed, the layout undergoes another DRC check to ensure that all violations have been cleared. Clearing DRC means that the layout complies with the design rules and is ready for further processing.

- After ensuring the design's integrity, we generating a GDS (Graphic Data System) file. This file contained all the necessary information required for the fabrication process.