

KREENA DESAI

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Summary

Master's Student at Queen Mary University of London, currently pursuing Msc. in Advanced Electronics and Electrical Engineering, with hands-on experience in chip design. Actively seeking engineering roles in chip design, semiconductor industry or similar roles. **I have the right to work in UK.**

Education

Queen Mary University of London MSc. Advanced Electronics and Electrical Engineering	September 2024 - September 2025 (Expected) London, UK
Pandit Deendayal Energy University BTech Electronics and Communication Engineering (CGPA: 8.15/10)	November 2020 - May 2024 Gujarat, India

Work Experience

Indian Space Research Organization (SAC, ISRO) Chip Design Intern	January 2024 – May 2024
<ul style="list-style-type: none">Engineered chip-level design for a 108 x 120 mm Penta-Linear Array Charged Coupled Device, supporting remote sensing and astronomical observation.Performed RC extraction analysis on 300+ signal paths, optimizing pixel architecture and 87μm Horizontal Shift Register layout for power efficiency.Configured metal interconnects across 8 layers to minimize cross-talk and improve signal quality.	
Alphadecimal Networks Pvt. Ltd. Summer Intern/Trainee	June 2023 – July 2023
<ul style="list-style-type: none">Assessed antenna configurations and tower architectures for 5G deployment at 4 locations.Conducted 5+ field evaluations, documenting infrastructure requirements and deployment protocols.Installed and tested network equipment across 3 (low, mid, and high) frequency bands, gaining hands-on experience in antenna mounting for 5G projects.	

Skills

Programming: MATLAB, C / C++, Assembly Language, Verilog, VHDL, JUCE
Design Softwares: Cadence Virtuoso, MATLAB/Simulink, Multisim, LTSpice, TinkerCAD
Technologies: Arduino, Chip Design, Embedded System and Microcontrollers, Semiconductor and VLSI Technologies, RF Planning, Music and Audio Programming, Analog Circuit Designing

Projects

Intelligent Sensor fusion for Hyperloop pod levitation (On-going) <i>MATLAB, Hardware Interfacing</i> <ul style="list-style-type: none">Integrated 4 sensors (accelerometer, proximity, magnetic field, and pressure) into a unified architecture, applying Extended Kalman Filter techniques for multi-sensor data fusion.Built a fault-tolerant control system ensuring operational stability during component failures or environmental disturbances, and deployed a real-time control framework using fused sensor inputs to maintain a $\pm 0.1\text{mm}$ levitation gap.
Chip Design of Penta Linear Array Charge Coupled Device (CCD) <i>Cadence, Virtuoso</i> <i>GitHub</i> <ul style="list-style-type: none">Designed 5 array CCD chip in Cadence with (16x16μm) pixel structures, horizontal shift register circuits, and multi-layer metal routing.Produced comprehensive DRC and ERC verification files and executed RC extraction to ensure signal integrity.Validated chip performance through 50+ simulation cycles, meeting orbital deployment reliability standards.
Vocal Transformer: Real-time Voice Character Modification <i>JUCE, ProJucer, C++</i> <i>GitHub</i> <ul style="list-style-type: none">Created a real-time audio plugin in C++ (JUCE), transforming vocal inputs into 6 character voices (Robot, Alien, Child, Giant, Elder, Choir).Deployed 8-stage DSP chain with pitch shifting, formant manipulation, and 4-voice layering functionality.Constructed intuitive, 8+ color-coded UI with rotary sliders, featuring phase vo-coder algorithms, tanh-based soft clipping, and multi-voice layering.

Publication

Efficient Chip Design of Penta Linear Array Charge Coupled Device (CCD) | *IEEE*