KREENA DESAI

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Education

Queen Mary University of London **September 2024 - September 2025 (Expected)**

Master's of Science in Adv. Electronics and Electrical Engineering *London, UK*

Pandit Deendayal Energy University **November 2020 - May 2024**

*Bachelor of Technology in Electronics and Communication Engineering (CGPA of **8.15/10**)* *Gandhinagar, Gujarat, India*

Work Experience

Indian Space Research Organization (SAC, ISRO) **January 2024 – May 2024**

Chip Design Intern

- Architected chip level design for **Penta-Linear Array Charged Coupled Device of size 108 x 120 mm** supporting space-based remote sensing and astronomical observation applications and image processing.
- Generated comprehensive **Design Rule Check (DRC)** and **Electrical Rule Check (ERC)** verification files, reducing design violations and finally generating a **GDS file**.
- Executed **RC Extraction Analysis** across **300+** signal paths, maintaining signal integrity.
- Optimized **Pixel Architecture** and **87um Horizontal Shift Register (HSR)** layout, improving chip functionality while reducing overall power consumption.
- Implemented **Metal Routing** strategies across **8 interconnect layers**, minimizing cross-talk interference and enhancing signal quality.

Alphadecimal Networks Pvt. Ltd. **June 2023 – July 2023**

Summer Intern/Trainee

- Analyzed **antenna configurations** and network tower architectures for **5G deployment** across multiple sites.
- Conducted **5+ on-site field assessments**, documenting **tower infrastructure requirements** and deployment procedures.
- Studied network equipment placement and signal optimization techniques for enhanced **5G performance**.
- Evaluated network equipment deployment spanning **3 frequency bands (low, mid, high)** gaining hands-on experience with **antenna mounting,** backhaul connections and base station commissioning for large-scale 5G rollout projects

Skills

Hardware Programming Languages: MATLAB, C / C++, Assembly Language, Verilog, VHDL, JUCE

Design Softwares: Cadence Virtuoso, MATLAB/Simulink, Multisim, LTSpice, TinkerCAD

Electronic Technologies: Arduino, Chip Design, Embedded System and Microcontrollers, Semiconductor and VLSI Technologies, RF Planning, Music and Audio Programming, Analog Circuit Designing

Projects

Intelligent Sensor fusion for Hyperloop pod levitation (Continue) | *MATLAB, Hardware Interfacing*

- Designed integrated sensor architecture combining **4 sensors (accelerometers**, **proximity**, **magnetic field**, and **pressure sensors)** and applied **Extended Kalman Filter** techniques to fuse multi-sensor data streams.
- Engineered **fault-tolerant control system** maintaining operational stability despite component failures or environmental interference along with a **real-time control framework** using **fused sensor** inputs to regulate **±0.1mm** levitation gap.
- Validated performance gains over traditional 1 sensor approach through systematic testing and comparative analysis.

Chip Design of Penta Linear Array Charge Coupled Device (CCD) | *Cadence, Virtuoso, DRC checks*

- Built specialized **5 array CCD** chip architecture in Cadence, designing pixel structures **(16x16um)**, horizontal shift register circuits, and multi-layer metal routing for optimal functionality.
- Generated comprehensive **design rule checks** and **electrical rule checks** verification files while executing **RC extraction** in Virtuoso to ensure signal integrity.
- Validated chip performance through **50+ simulation cycles**, meeting the reliability requirements for orbital deployment.

Vocal Transformer: Real-time Voice Character Modification | *JUCE, Projucer, C++* | *GitHub*

- Built **real-time audio plugin** using **JUCE framework** and **C++** capable of transforming vocal inputs into **6** distinct character voices **(Robot, Alien, Child, Giant, Elder, Choir)**.
- Implemented **8-stage DSP** processing chain including phase voice coder **pitch shifting**, **formant manipulation**, and **4-voice layering** capabilities.
- Designed intuitive **8+** color-coded user interface with **rotary sliders** and implemented **phase voice coder algorithms**, **tanh-based soft clipping**, and **multi-voice layering** capabilities for creative audio applications.

Publication

Efficient Chip Design of Penta Linear Array Charge Coupled Device (CCD) | *IEEE*