KREENA DESAI

London, UK

+44 7553683775 **kreena.desai30@gmail.com** **Kreena Desai** **Kreena Desai**

Education

Queen Mary University of London **September 2024 - September 2025 (Expected)**

MSc in Advanced Electronics and Electrical Engineering *London, UK*

Pandit Deendayal Energy University **November 2020 - May 2024**

*BTech in Electronics and Communication Engineering (CGPA of **8.15/10**)* *Gandhinagar, Gujarat, India*

Work Experience

Indian Space Research Organization (SAC, ISRO) **January 2024 – May 2024**

Chip Design Intern

- Engineered chip-level design for a **108 x 120 mm Penta-Linear Array Charged Coupled Device**, supporting remote sensing and astronomical observation.
- Performed **RC extraction** analysis on **300+** signal paths, optimizing pixel architecture and **87µm Horizontal Shift Register** layout for power efficiency.
- Configured metal interconnects across **8** layers to minimize cross-talk and improve signal quality.

Alphadecimal Networks Pvt. Ltd. **June 2023 – July 2023**

Summer Intern/Trainee

- Assessed antenna configurations and tower architectures for **5G deployment** at multiple locations.
- Conducted **5+** field evaluations, documenting infrastructure requirements and deployment protocols.
- Installed and tested network equipment across **3 (low, mid,** and **high)** frequency bands, gaining hands-on experience in **antenna mounting** for 5G projects.

Skills

Hardware Programming Languages: MATLAB, C / C++, Assembly Language, Verilog, VHDL, JUCE

Design Softwares: Cadence Virtuoso, MATLAB/Simulink, Multisim, LTSpice, TinkerCAD

Hardware Technologies: Arduino, Chip Design, Embedded System and Microcontrollers, Semiconductor and VLSI Technologies, RF Planning, Music and Audio Programming, Analog Circuit Designing

Projects

Intelligent Sensor fusion for Hyperloop pod levitation (On-going) | *MATLAB, Hardware Interfacing*

- Integrated **4** sensors **(accelerometer, proximity, magnetic field,** and **pressure)** into a unified architecture, applying **Extended Kalman Filter** techniques for multi-sensor data fusion.
- Built a **fault-tolerant** control system ensuring operational stability during component failures or environmental disturbances, and deployed a real-time control framework using fused sensor inputs to maintain a **±0.1mm** levitation gap.

Chip Design of Penta Linear Array Charge Coupled Device (CCD) | *Cadence, Virtuoso* | *GitHub*

- Designed **5 array CCD** chip in **Cadence** with **(16x16um)** pixel structures, horizontal shift register circuits, and multi-layer metal routing.
- Produced comprehensive **DRC** and **ERC** verification files and executed **RC extraction** to ensure signal integrity.
- Validated chip performance through **50+ simulation cycles**, meeting orbital deployment reliability standards.

Vocal Transformer: Real-time Voice Character Modification | *JUCE, Projucer, C++* | *GitHub*

- Created a real-time audio plugin in **C++ (JUCE)**, transforming vocal inputs into **6** character voices (**Robot, Alien, Child, Giant, Elder, Choir**).
- Deployed **8-stage DSP** chain with **pitch shifting, formant manipulation,** and **4**-voice layering functionality.
- Constructed intuitive, **8+** color-coded UI with rotary sliders, featuring phase vo-coder algorithms, **tanh-based** soft clipping, and multi-voice layering.

Publication

Efficient Chip Design of Penta Linear Array Charge Coupled Device (CCD) | *IEEE*