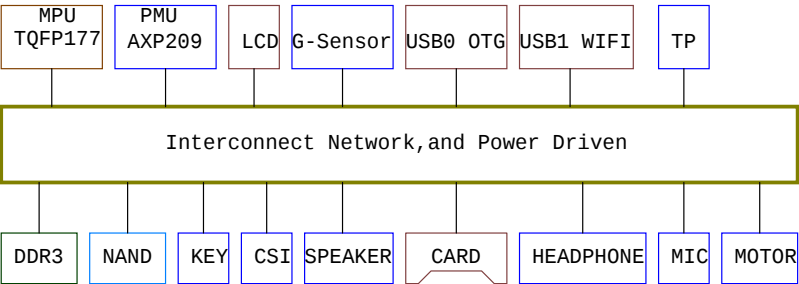


# COVER

## BLOCK



## GPIO ASSIGNMENT

CPU	Define	Function
PB0	TWI0_SCK	TWI0
PB1	TWI0_SDA	
PB2	PWM0	LCD
PB3	GPIO-OUT	TP-WAKE-RST
PB4	NC	
PB10	GPIO-OUT	CSI-STY
PB15	TWI1_SCK	TWI1
PB16	TWI1_SDA	
PB17	TWI2_SCK	TWI2
PB18	TWI2_SDA	
PG0	INPUT	SD0-DET-N
PG1	GPIO-IN	USB0-VBUSDET
PG2	GPIO-IN	USB0-IDDET
PG3	GPIO-OUT	CSI-STY-1
PG4	GPIO-OUT	CSI-RST-1
PG9	GPIO-OUT	MT-EN
PG10	GPIO-OUT	PA-SHDN
PG11	EINT	TP-INT
PG12	GPIO-OUT	USB0-DRV
PMU	Define	Function
GPIO0	GPIO-OUT	LCD-PWR
GPIO1	GPIO-OUT	LCD-BL-EN
GPIO2	GPIO-OUT	CSI-PWR-EN
GPIO3	GPIO-OUT	CSI-RST

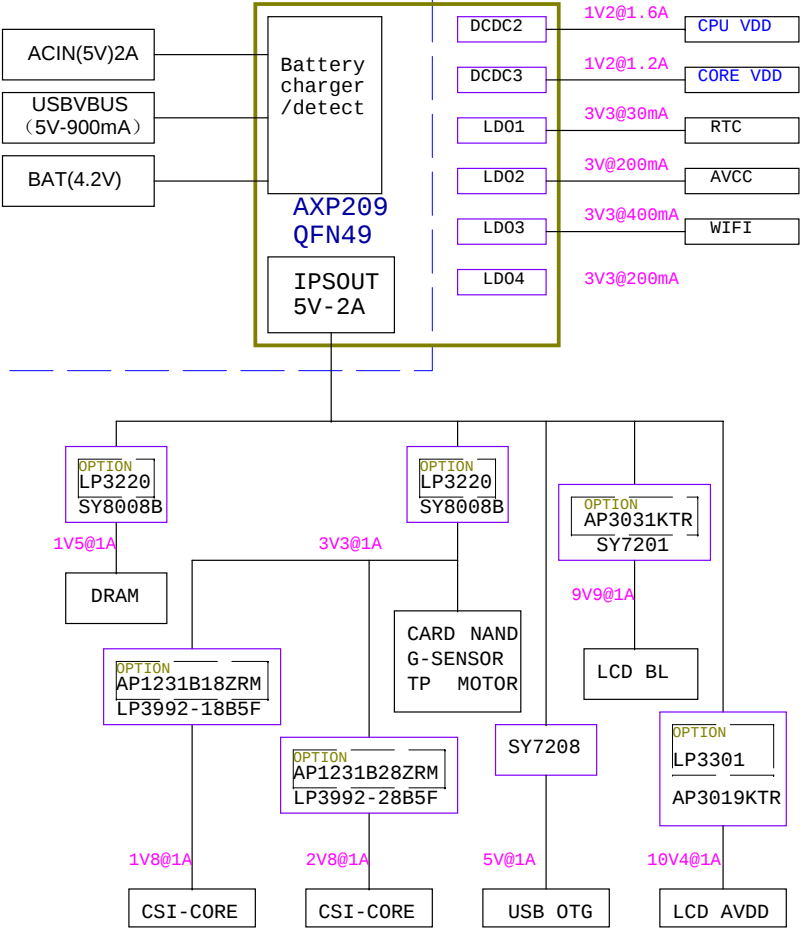
特别提醒:  
1: PG0 / PG1 / PG2这三个PIN脚  
只具有INPUT/中断/专有功能  
2: PMU的GPIO0/1/2/3这四个PIN脚  
只做GPIO-OUTPUT功能  
3: PG10 /PG11 /PG12这三个PIN脚  
的功能不可改变

## REVISION HISTORY

Revision	Description	Date	Drawn	Checked	Approved
APP3_PAD_DDR3_V1_22	version 1.22		YT		
APP3_PAD_DDR3_V1_23	version 1.23	2012.03.28	YT		

## POWER TREE

LAYOUT: ACIN、BAT、IPSOUT输入或  
输出线，从PMU管脚处就要保证尽量粗。



## Schematics Index

- 01 COVER
- 02 CPU
- 03 POWER
- 04 MEMORY
- 05 DISPLAY
- 06 MISC
- 07 WIFI

File		
APP3_PAD_DDR3		
Size	Document Name	Rev
A3	COVER	
Date	Sheet 1 of 7	

# CPU

4 SDQ[15:0] << SDQ[15:0]  
4 SA[14:0] << SA[14:0]  
4 SBA[2:0] << SBA[2:0]  
4 ND[7:0] << ND[7:0]

HPVCC HPVCC  
AVCC AVCC  
UVCC UVCC  
DRAM-VCC DRAM-VCC  
CPUVDD CPU-VDD  
COREVDD CORE-VDD  
VCC3V3 VCC  
GND GND

5 LCD-D20 133 LCD\_D20  
5 LCD-D19 134 LCD\_D19  
5 LCD-D18 135 LCD\_D18  
5 LCD-D15 136 LCD\_D15  
5 LCD-D14 137 LCD\_D14  
5 LCD-D13 138 LCD\_D13  
5 LCD-D12 139 LCD\_D12  
5 LCD-D11 140 LCD\_D11  
5 LCD-D10 141 LCD\_D10  
5 LCD-D7 142 VCC  
5 LCD-D6 143 VCC3  
5 LCD-D5 144 LCD\_D5  
5 LCD-D4 145 LCD\_D4  
5 LCD-D3 146 LCD\_D3  
5 LCD-D2 147 LCD\_D2  
5 TP-WAKE-RST 148 VDD5\_INT  
6 CSI-RST1 150 PB3/EINT17  
6 CSI-STY1 151 PG4/UART1\_RX/EINT4  
6 USB0-IDDET 152 PG3/UART1\_TX/EINT3  
6 USB0-VBUSDET 153 PG2/EINT2  
4 SD0-DET-N 154 PG1/EINT1  
155 PG0/EINT0  
6 UBOOT 156 VDD5\_CPU  
3 NMI-N 157 UBOOT  
3 RESET-N 158 NMI\_N  
6 TWI2-SDA 159 RESET\_N  
6 TWI2-SCK 160 PB18  
4 NDQS 161 PB17  
162 NDQS  
163 VCC4  
164 VDD6\_CPU  
165 NDQ7/SDC2\_D7  
166 NDQ6/SDC2\_D6  
167 NDQ5/SDC2\_D5  
168 NDQ4/SDC2\_D4  
169 CPU-VDD  
170 VDD7\_CPU  
171 NDQ3/SDC2\_D3  
172 NDQ2/SDC2\_D2  
173 CPU-VDD  
174 NDQ1/SDC2\_D1  
175 VDD8\_CPU  
176 NDQ0/SDC2\_D0  
4 NR81-N NR81/SDC2\_CLK  
4 NR80-N NR80/SDC2\_CMD

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4 NRE-N NRE  
4 NCE0-N NCE0  
4 NCE1-N NCE1  
4 NCLE NCE1/SPI0\_CLK  
4 NALE NCE1/SPI0\_MISO  
4 NWE-N NCE1/SPI0\_MOSI  
6 CSI-STY CSI-STY  
6 MTEN CSI-STY  
6 PASHDN CSI-STY  
4 USB0-DRV USB0-DRV  
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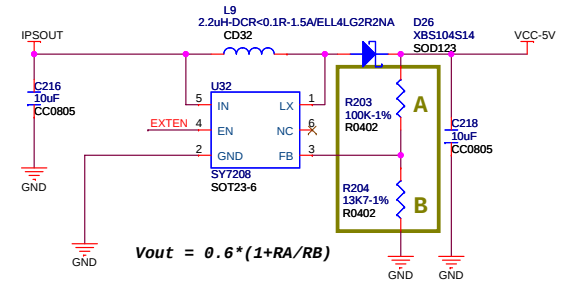
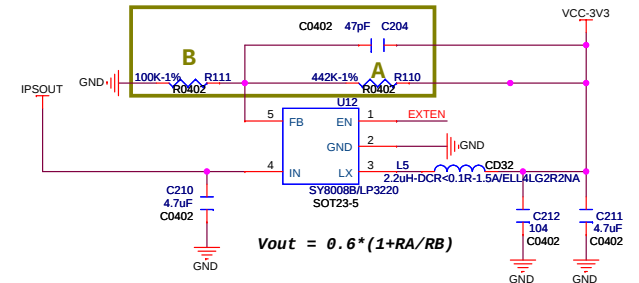
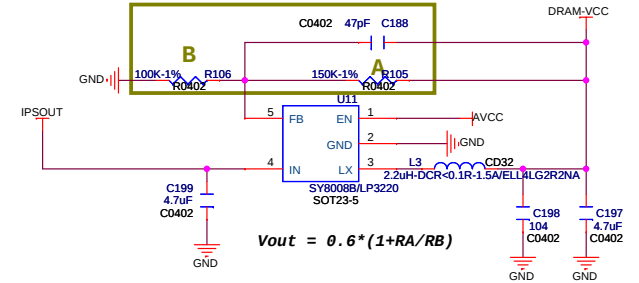
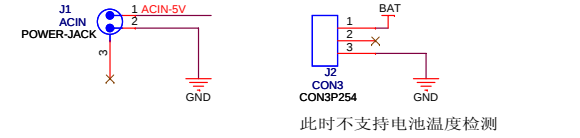
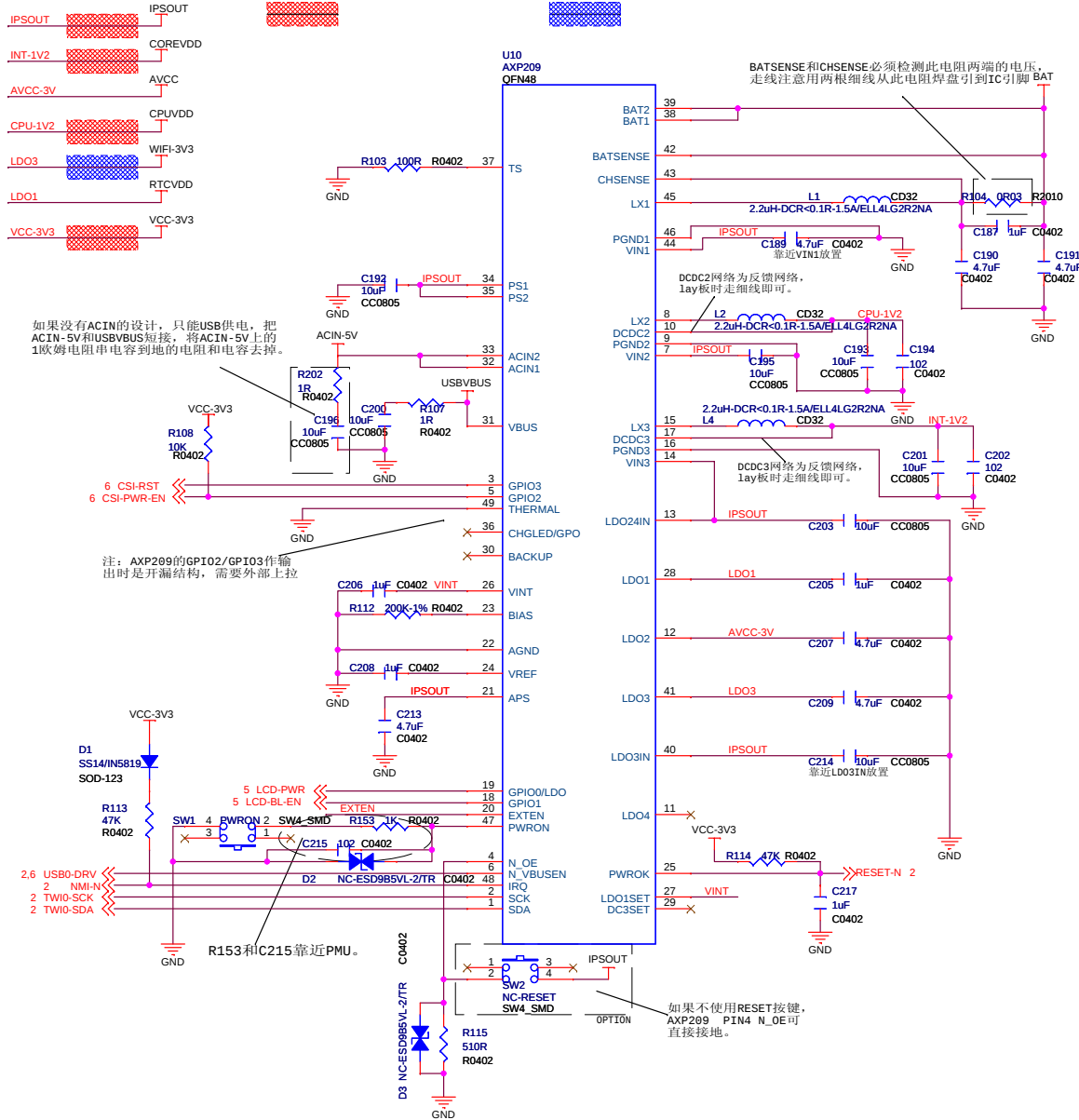
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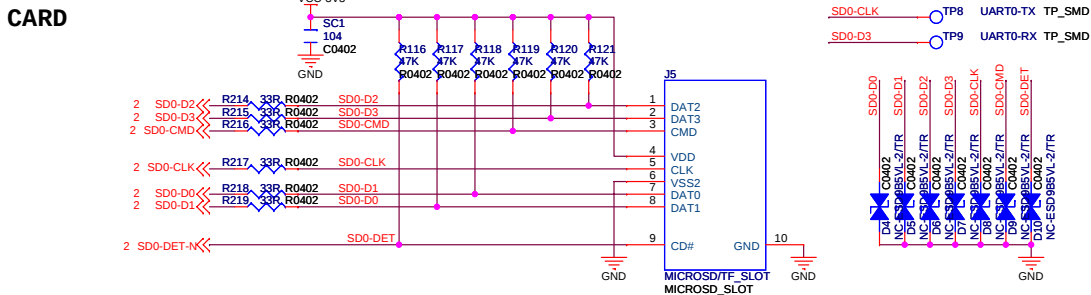
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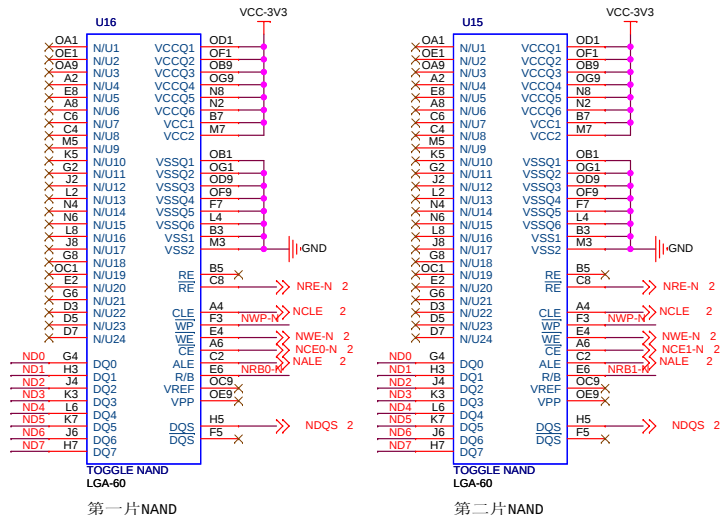
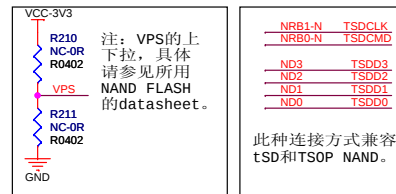


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## DDR3



注：只贴一片NAND FLASH时，请贴在U14

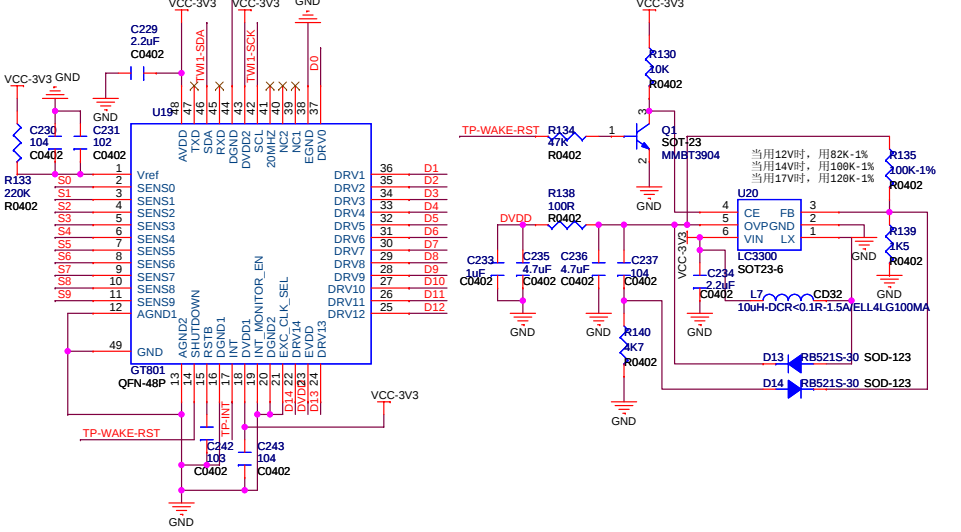


PCB上TOGGLE NAND与TSOP NAND双layout  
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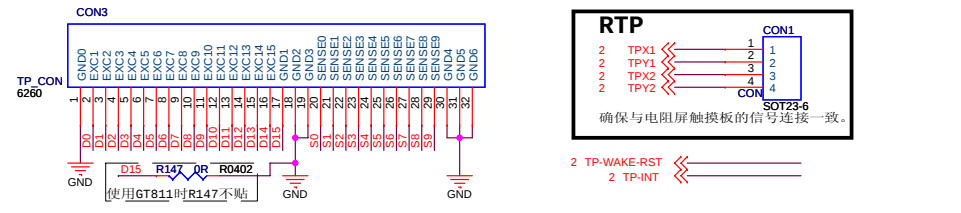
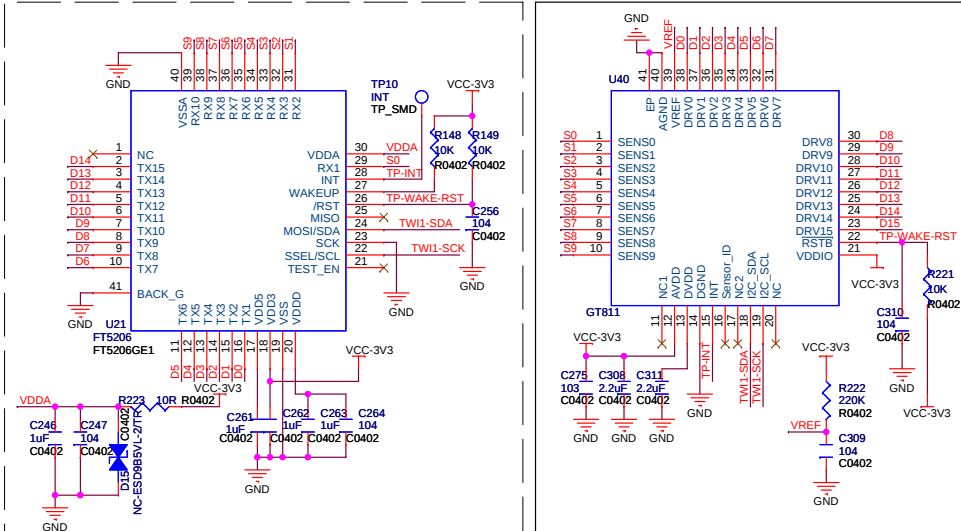
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# DISPLAY

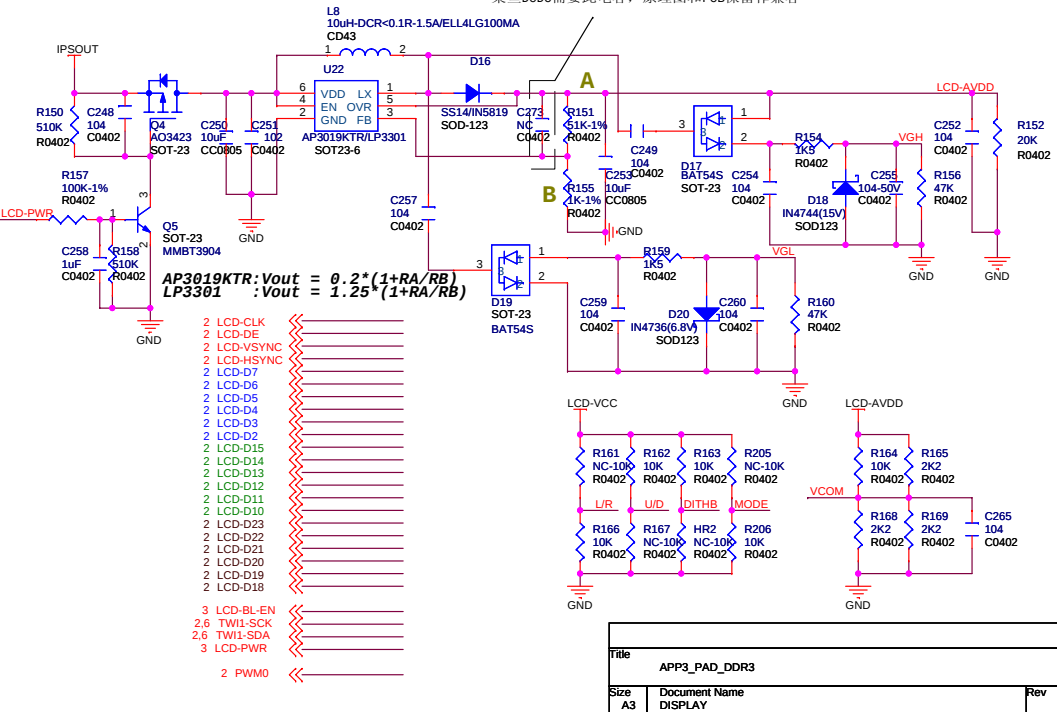
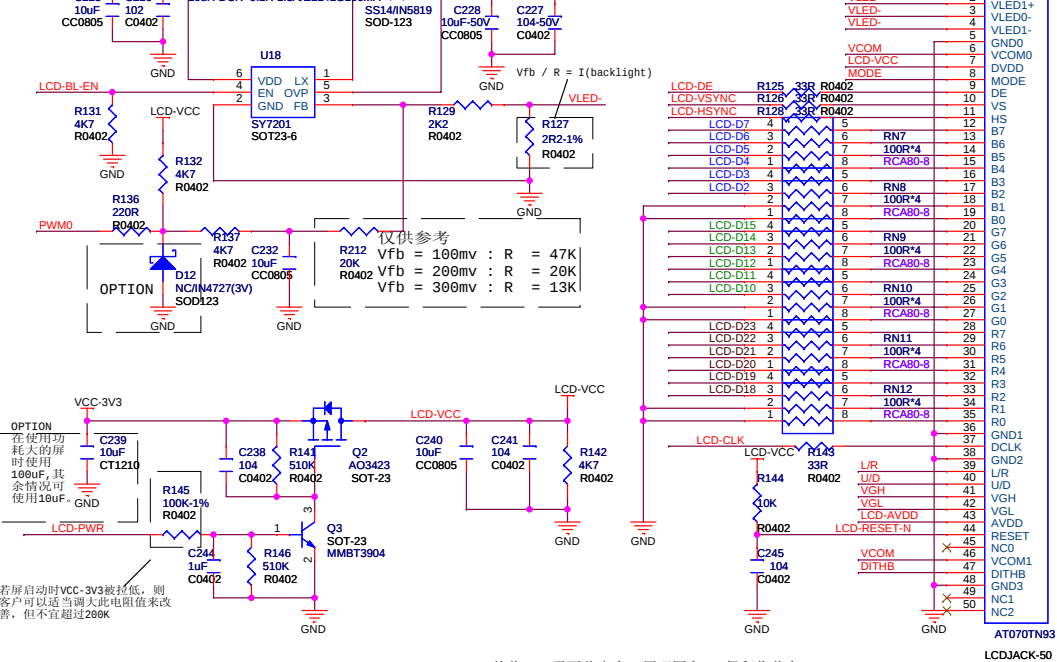
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## PCB上双LAYOUT



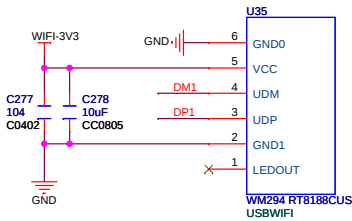
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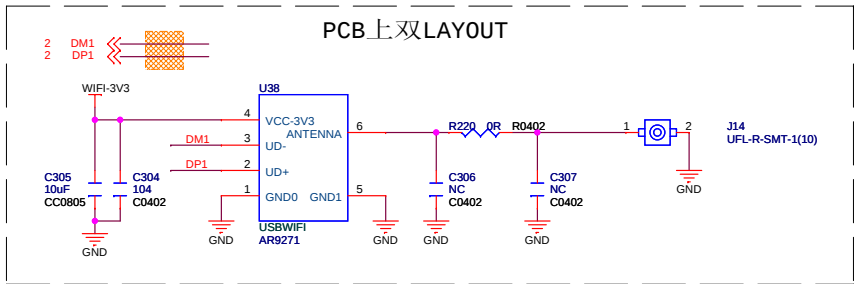
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WIFI



PCB上双LAYOUT



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