ECE 2050 Digital Logic and Systems

Chapter 8 : Shift Registers

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Chapter Review

- State
- SR Latch, D Latch
- D Flip Flop
- J-K Flip Flop
- Variations on a Flop
  - Registers
  - Enabled Flip-Flops
  - Resettable Flip-Flops
  - Settable Flip-Flops

Two Basic Functions of Shift Registers

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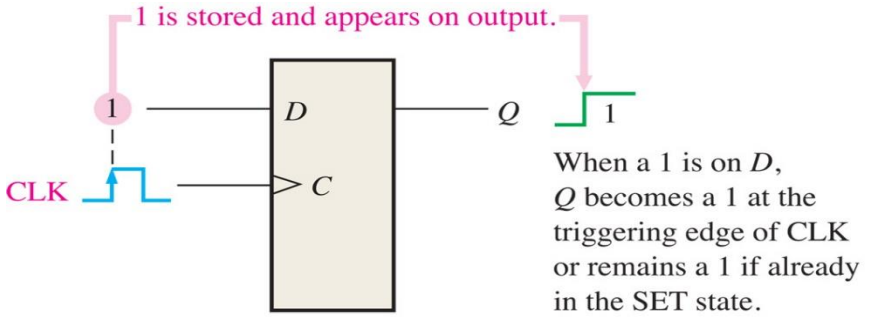
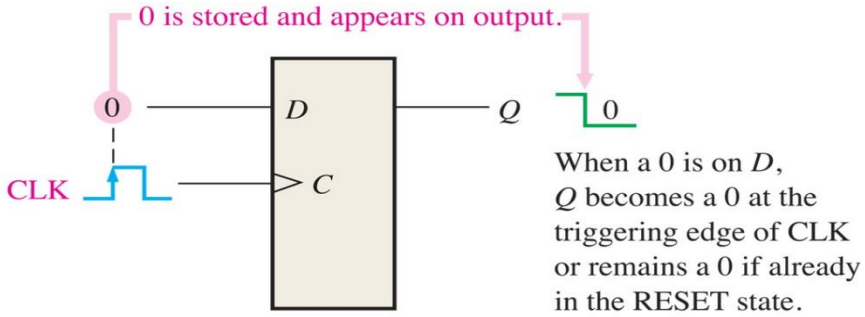
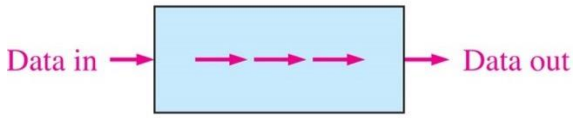
- Data storage

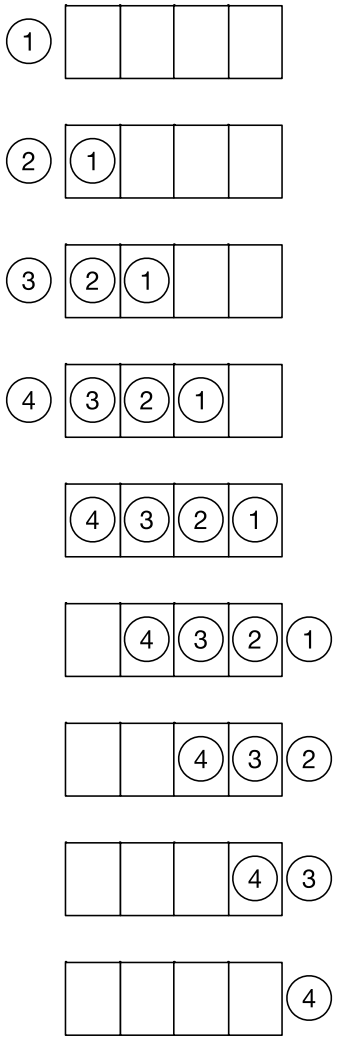


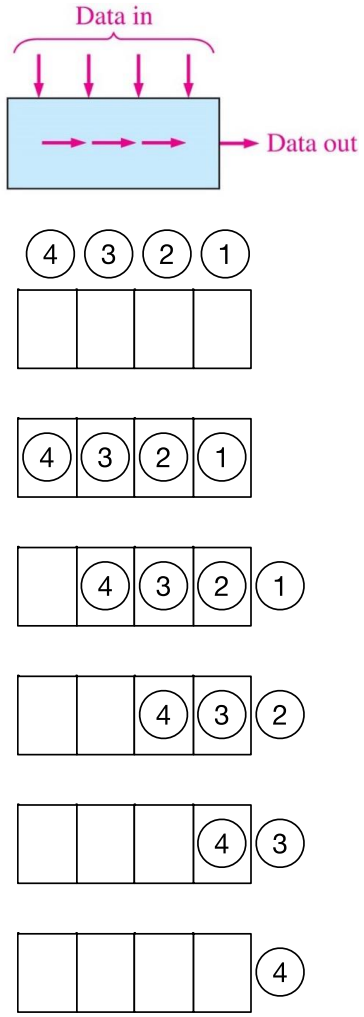


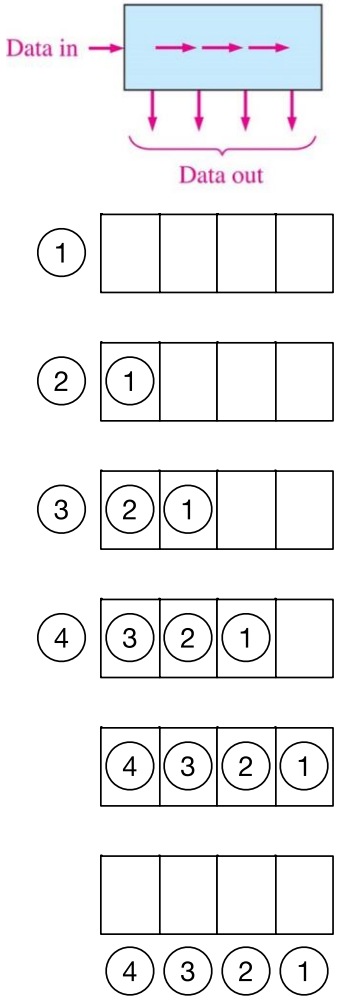
Two Basic Functions of Shift Registers

- Data Movement



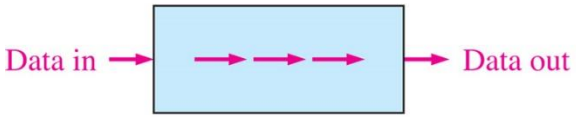






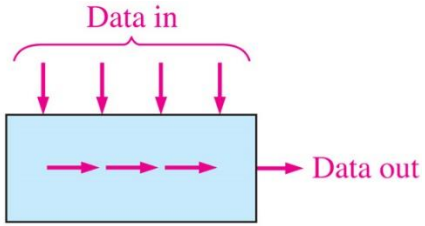
Two Basic Functions of Shift Registers

- Data Movement

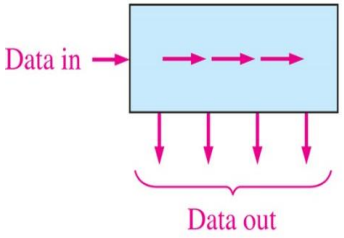


(a) Serial in/shift right/serial out

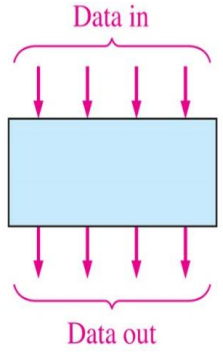
(b) Serial in/shift left/serial out



(c) Parallel in/serial out

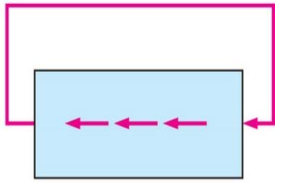


(d) Serial in/parallel out



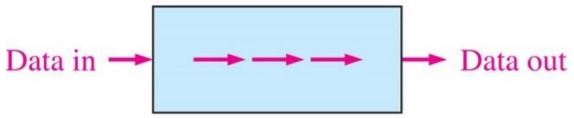
(e) Parallel in/parallel out

(f) Rotate right



(g) Rotate left

Serial in/Serial Out Shift Registers



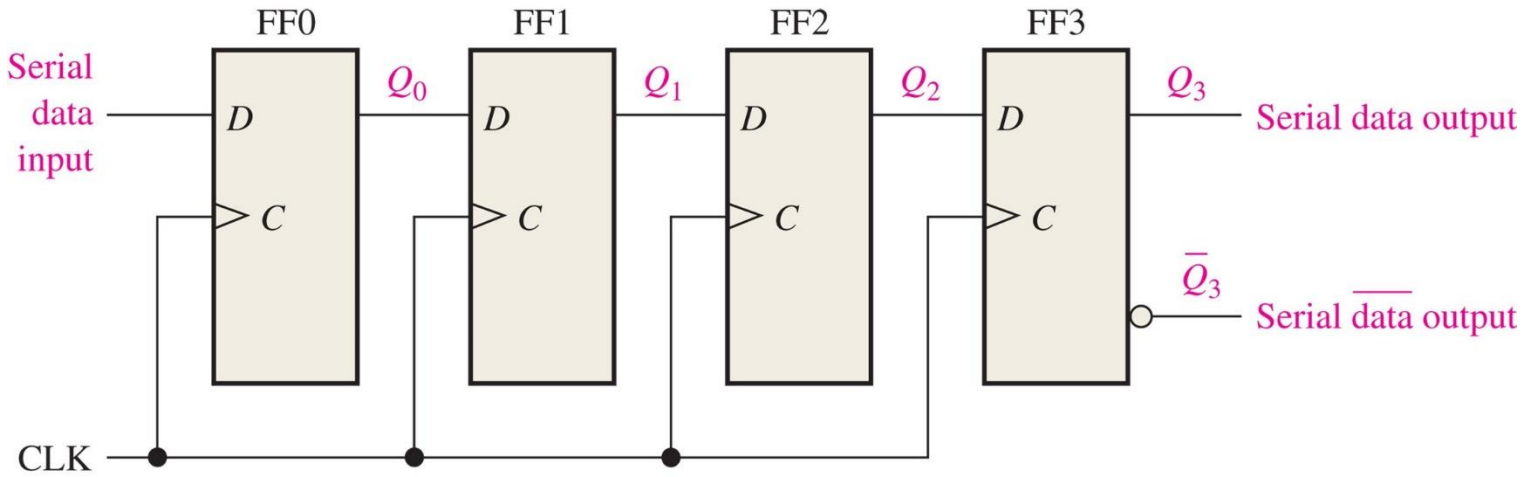


TABLE 8–1

Shifting a 4-bit code into the shift register in Figure 8–3. Data bits are indicated by a beige screen.

CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	0	0	0	0
1	**0**	0	0	0
2	**1**	**0**	0	0
3	**0**	**1**	**0**	0
4	**1**	**0**	**1**	**0**

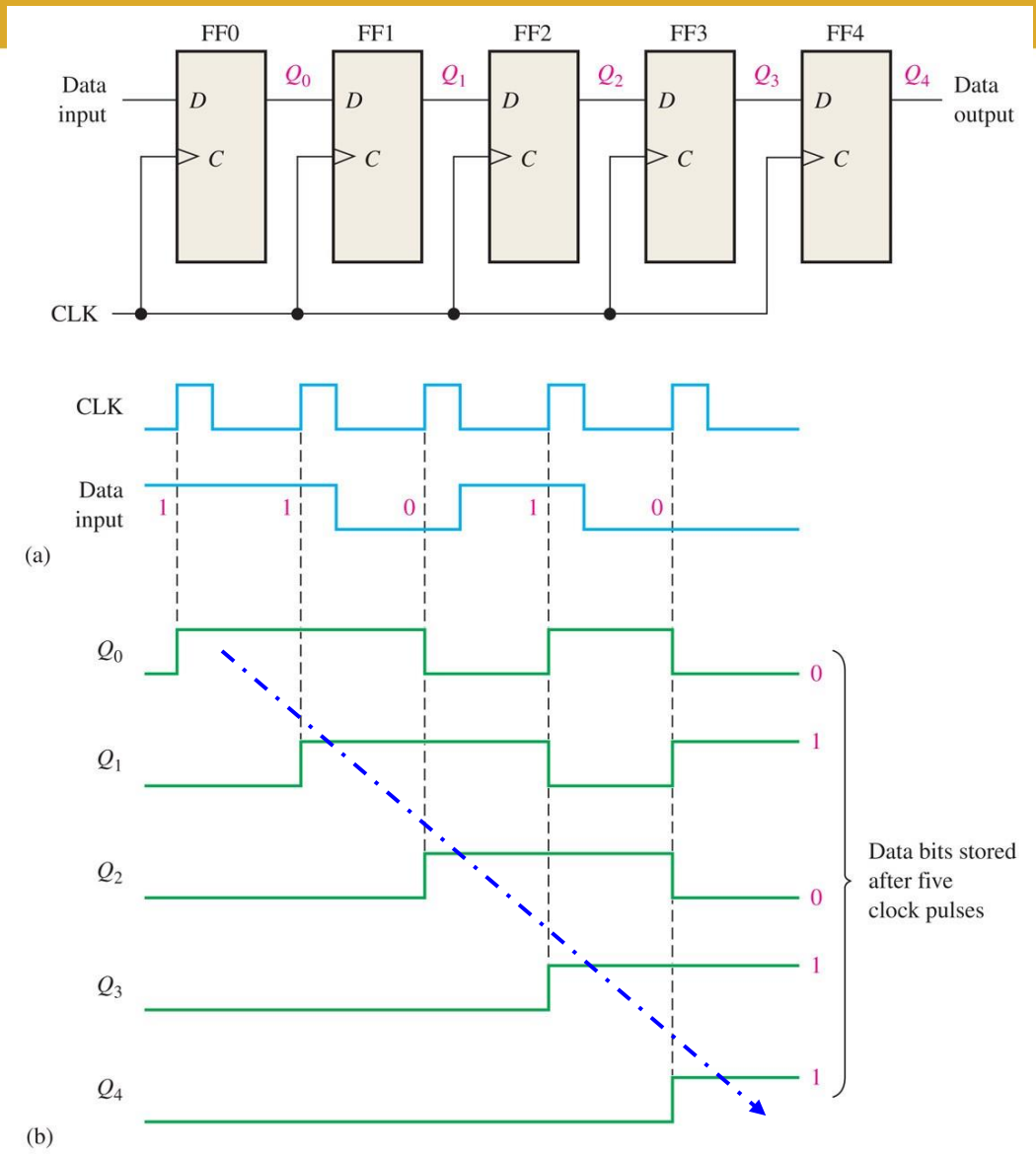
TABLE 8–2

Shifting a 4-bit code out of the shift register in Figure 8–3. Data bits are indicated by a beige screen.

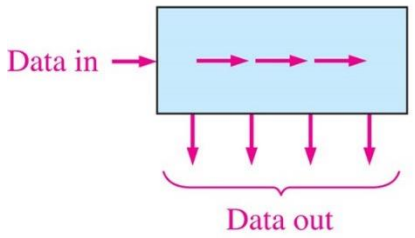
CLK	FF0 (Q_0)	FF1 (Q_1)	FF2 (Q_2)	FF3 (Q_3)
Initial	**1**	**0**	**1**	**0**
5	0	**1**	**0**	**1**
6	0	0	**1**	**0**
7	0	0	0	**1**
8	0	0	0	0

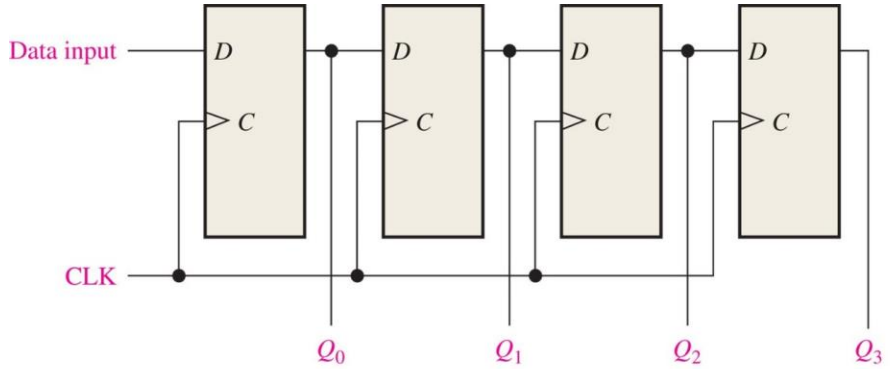
Example

- The first data bit (1) is entered into the register on the first clock pulse and then shifted from left to right as the remaining bits are entered and shifted.
- The register contains $Q_4Q_3Q_2Q_1Q_0 = 11010$ after five clock pulses.

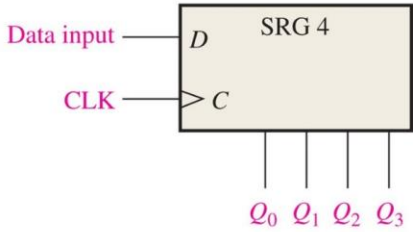


Serial in/Parallel Out Shift Registers

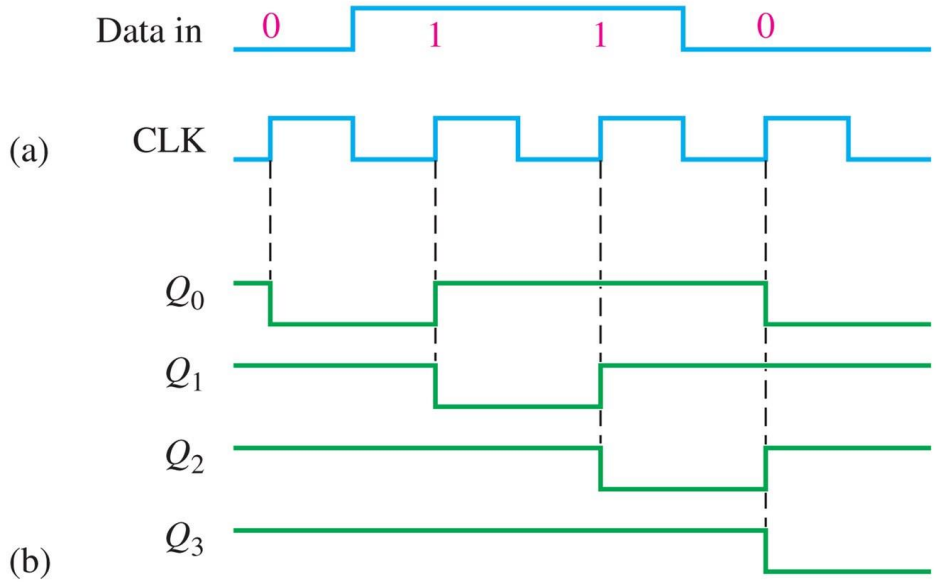




(a)



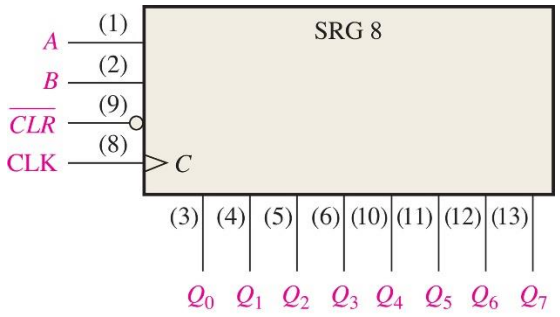
(b)

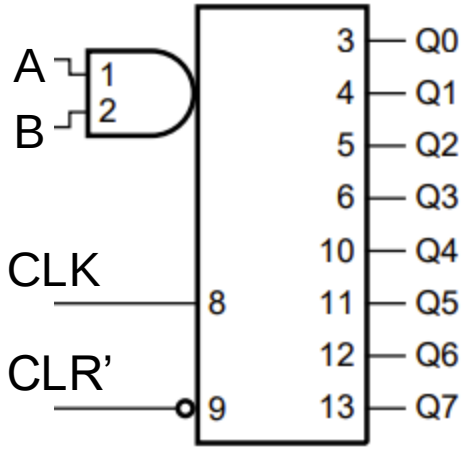


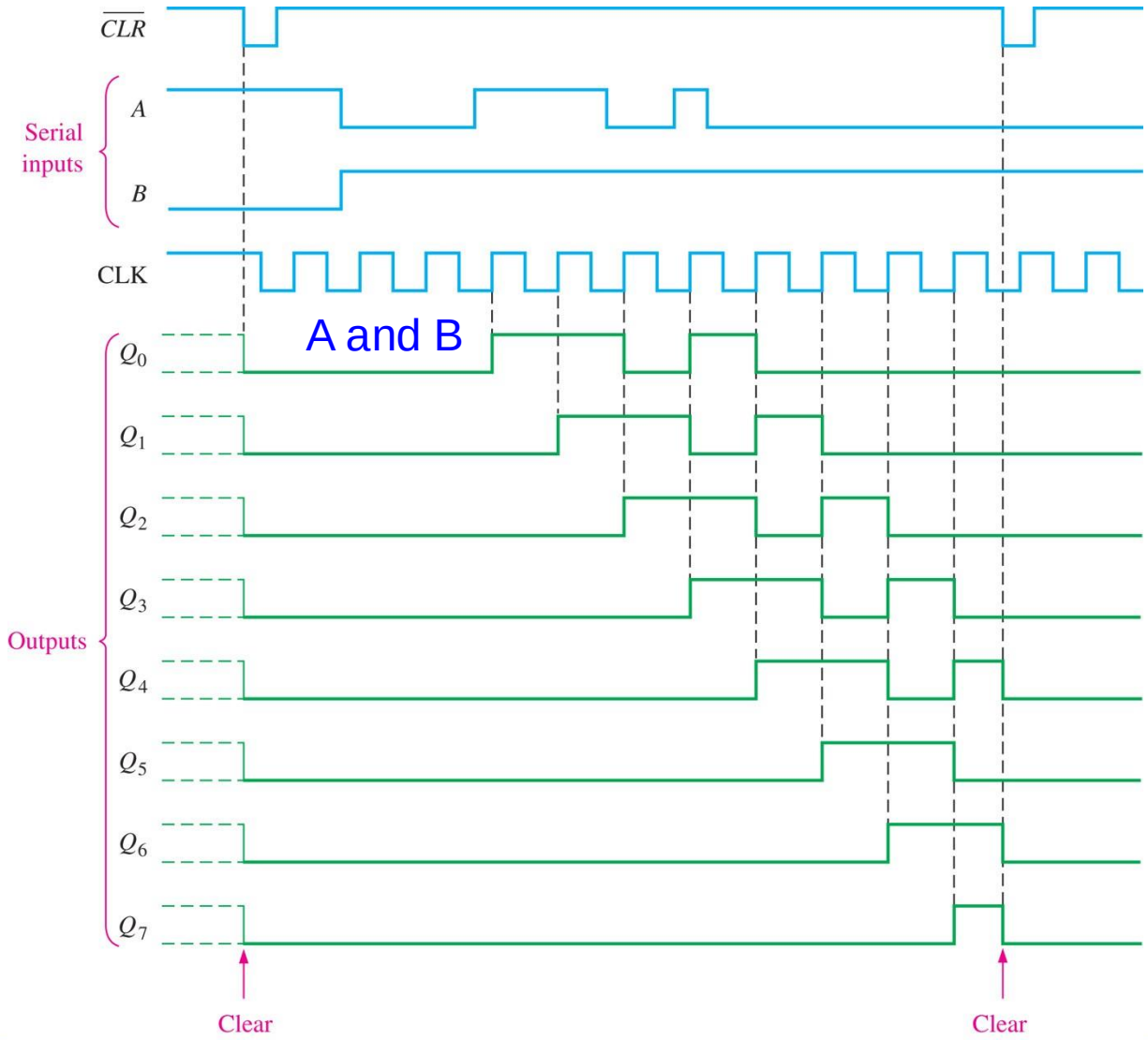
(a)

(b)

Example



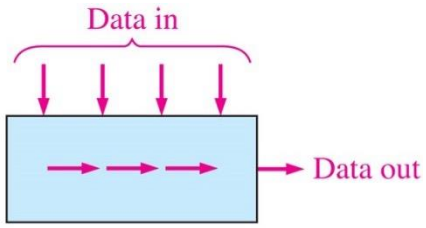


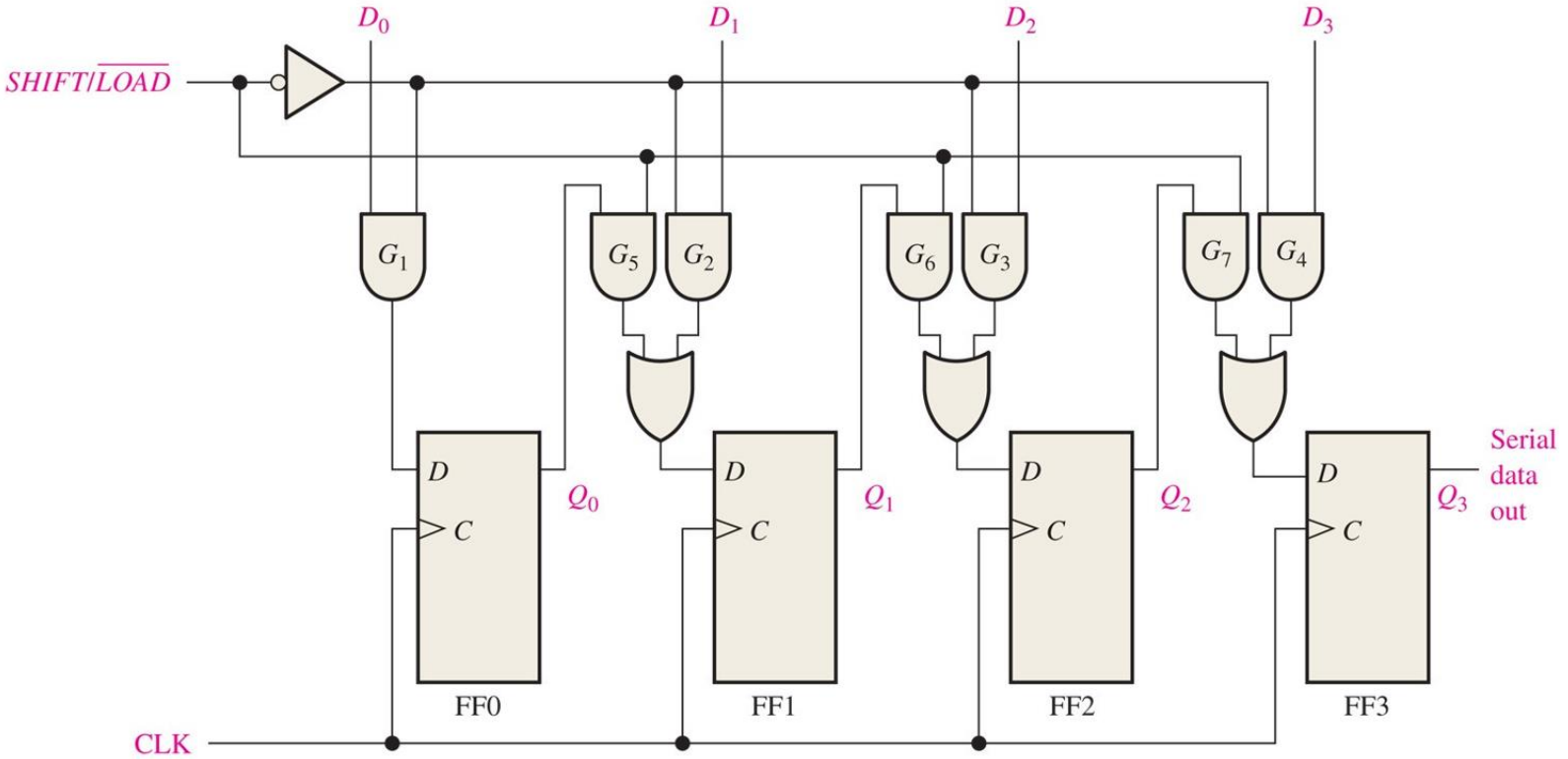


- 74HC164: Fixed-function IC shift register with serial in/parallel out

https://assets.nexperia.com/documents/data-sheet/74HC_HCT164.pdf

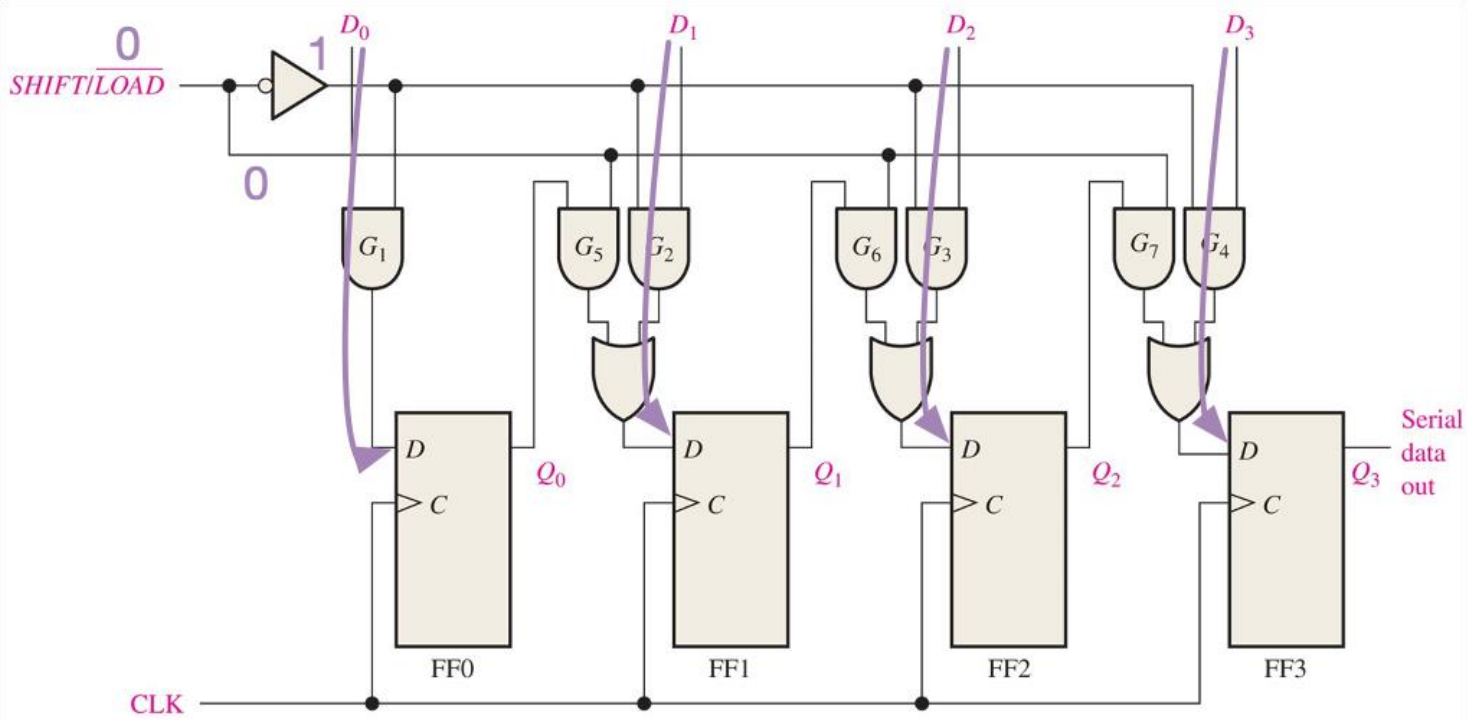
Parallel In/Serial Out Shift Registers





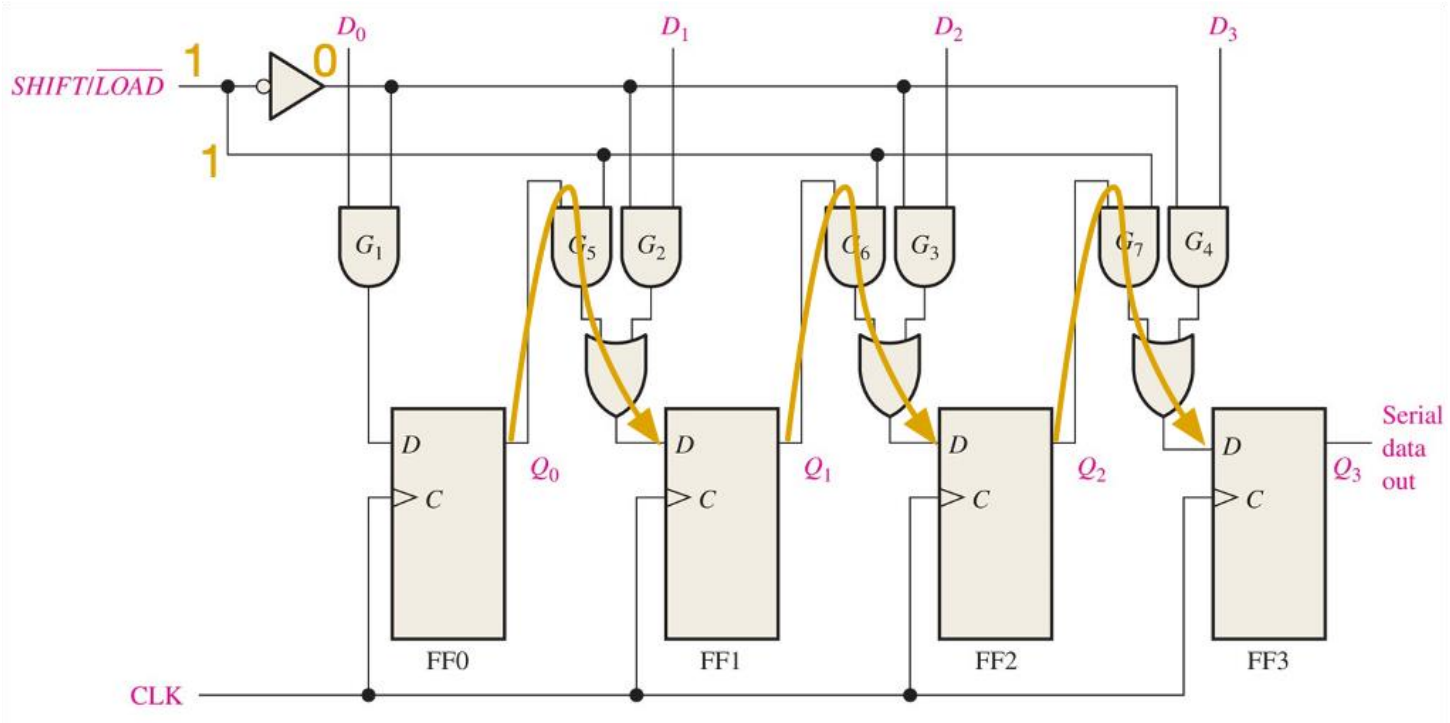
Parallel In/Serial Out Shift Registers

- When SHIFT/$\overline{\text{LOAD}}$ is LOW, G_1 ~ G_4 are enabled → each data bit is applied to the D input of its respective flip-flop;



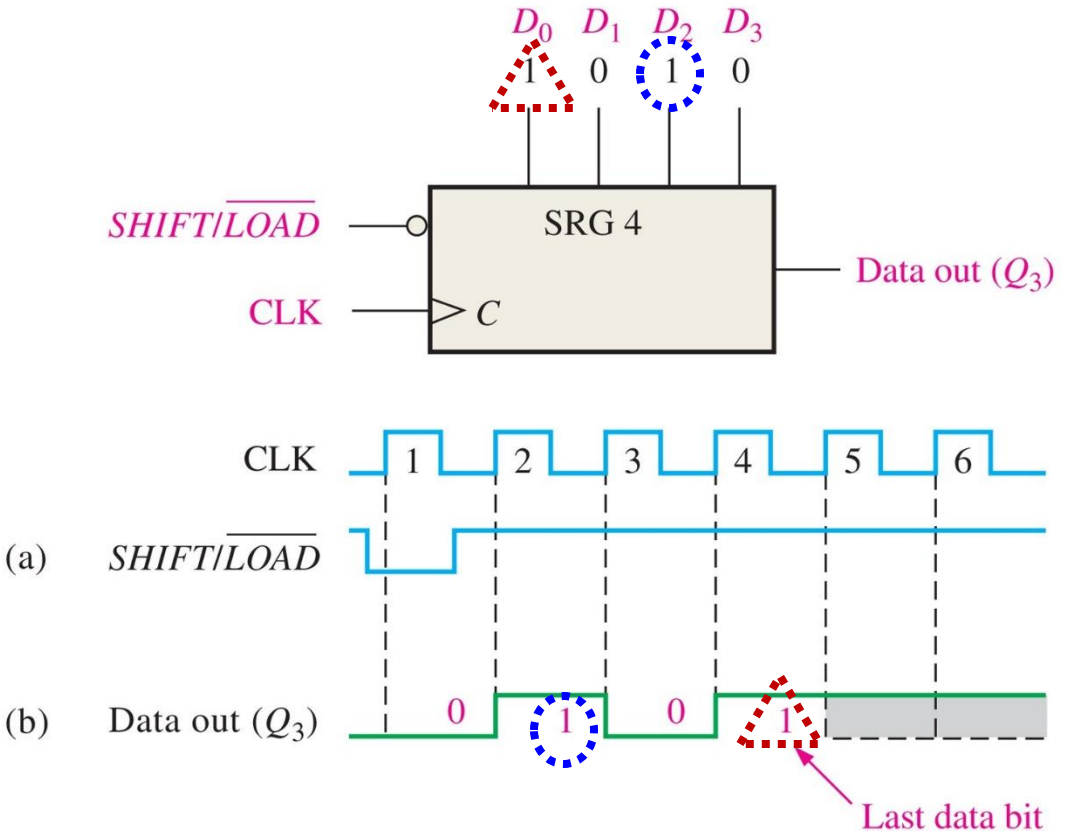
Parallel In/Serial Out Shift Registers

- When SHIFT/$\overline{\text{LOAD}}$ is HIGH, G_1 ~ G_4 are disabled while G_5 ~ G_7 are enabled → data bits are shifted right from one stage to the next.

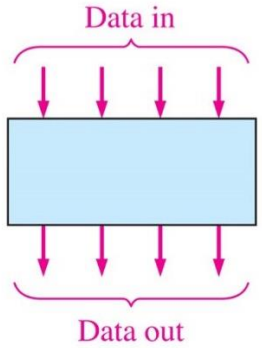


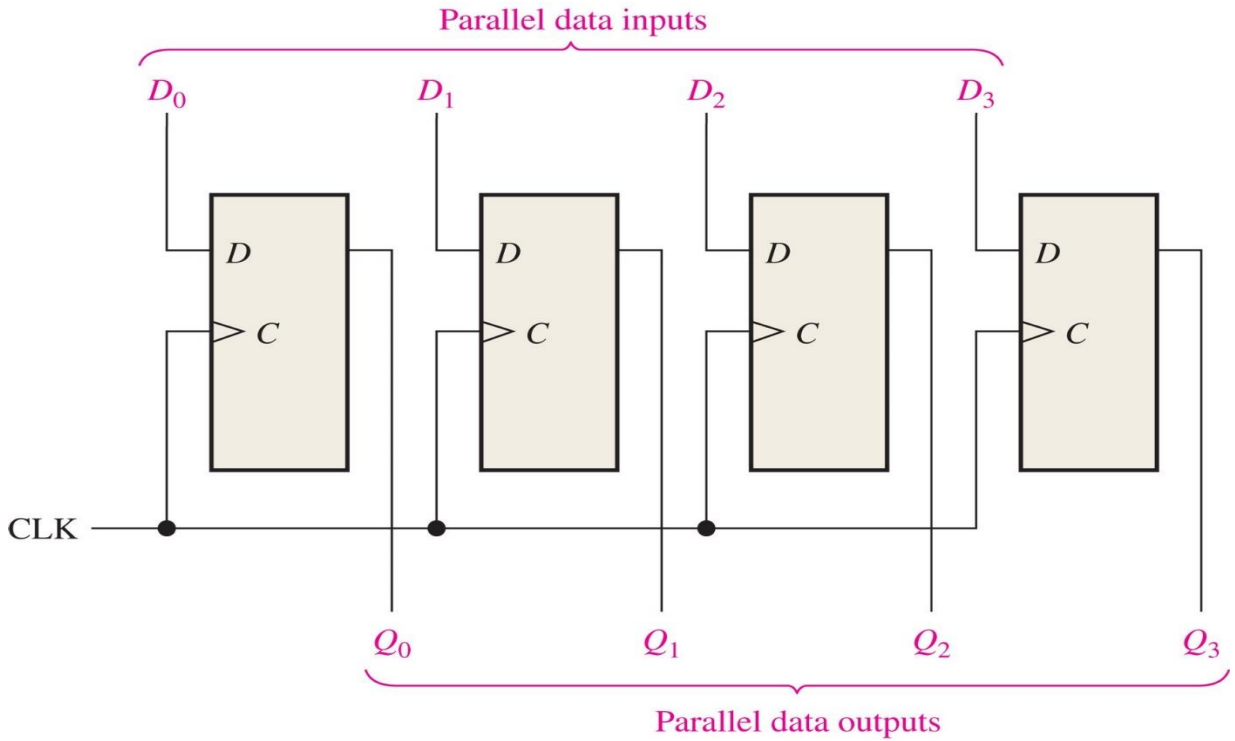
Example

- On clock pulse 1, the parallel data ($D_0D_1D_2D_3$ = 1010) are loaded into the register, making Q3 a 0.
- On clock pulse 2 the 1 from Q_2 is shifted onto Q_3;
- On clock pulse 3 the 0 is shifted onto Q_3;
- On clock pulse 4 the last data bit (1) is shifted onto Q_3;
- On clock pulse 5, all data bits have been shifted out, and only 1's remain in the register (assuming the D0 input remains as 1).



Parallel In/Parallel Out Shift Register

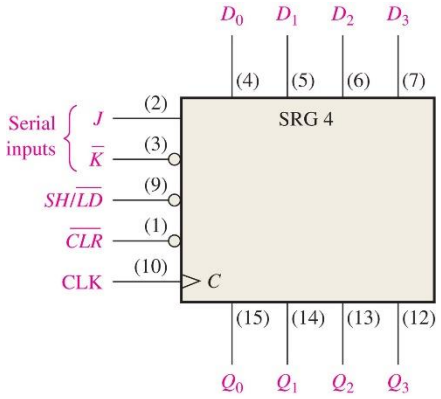


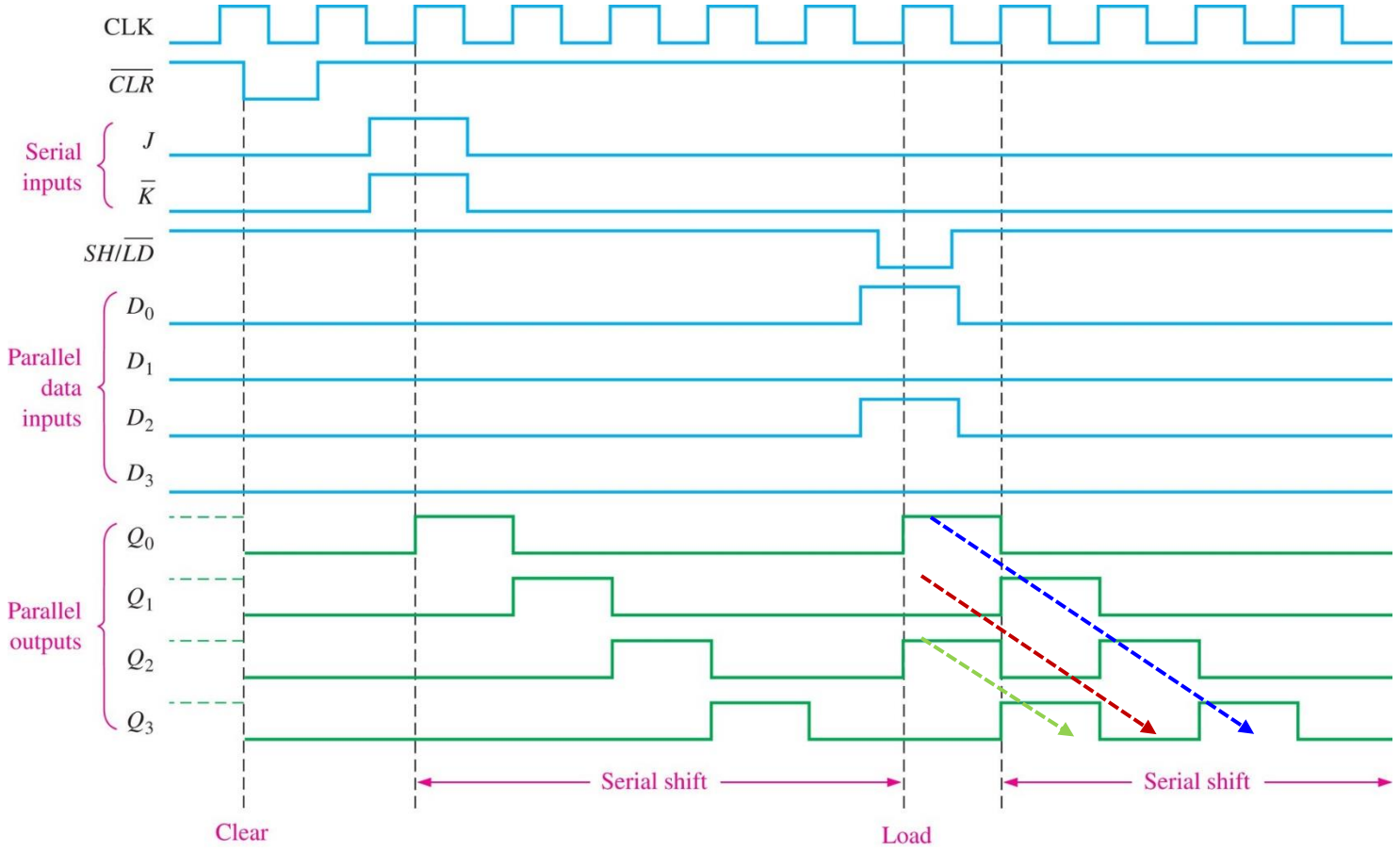


- The parallel in/parallel out register employs parallel entry and parallel output.
- Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.

Example

- 4-Bit Parallel-Access Shift Register



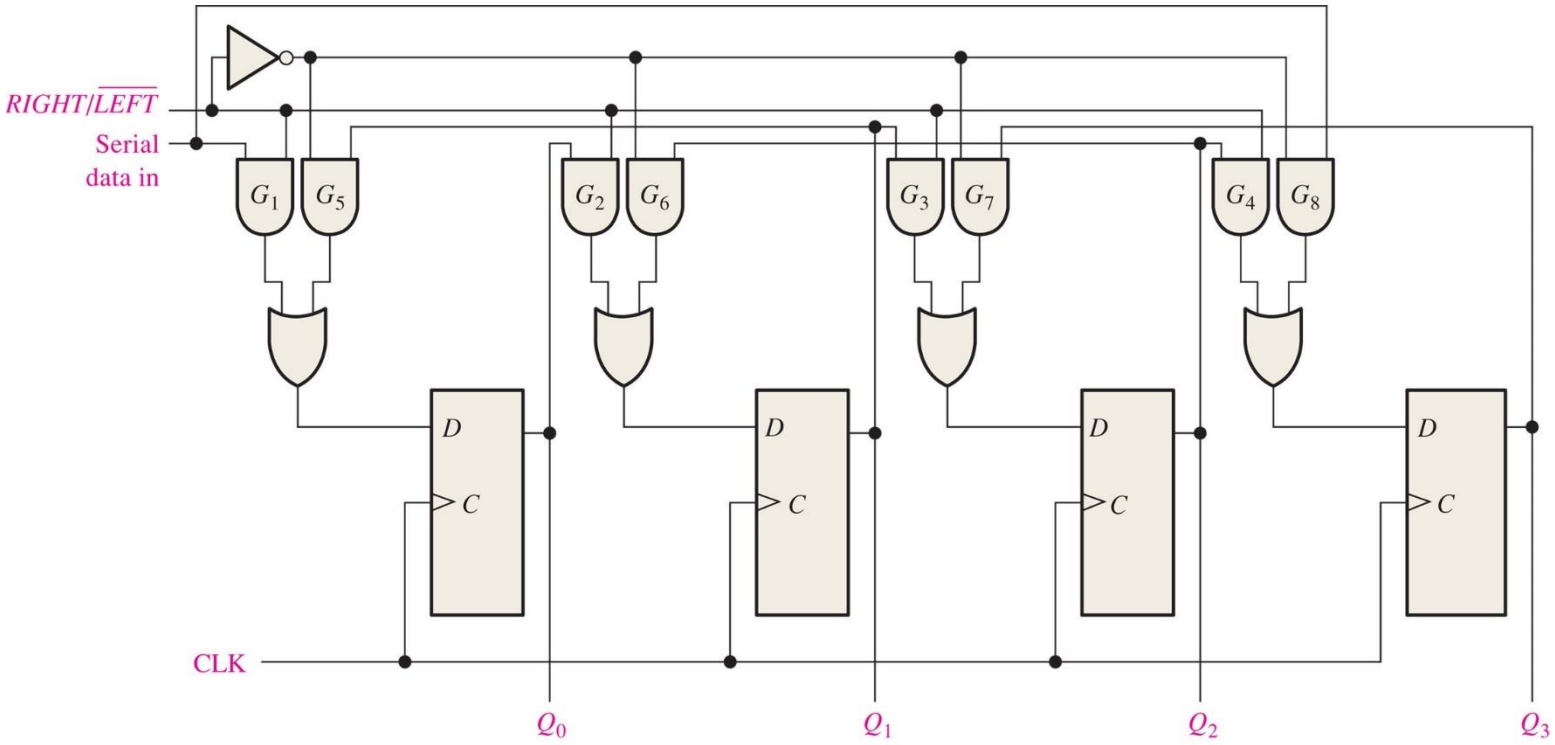


SN54HC195:
https://www.ti.com/lit/ds/symlink/sn54hc195.pdf?ts=1727527443445&ref_url=https%253A%252F%252Fwww.google.com.hk%252F

Bidirectional Shift Registers

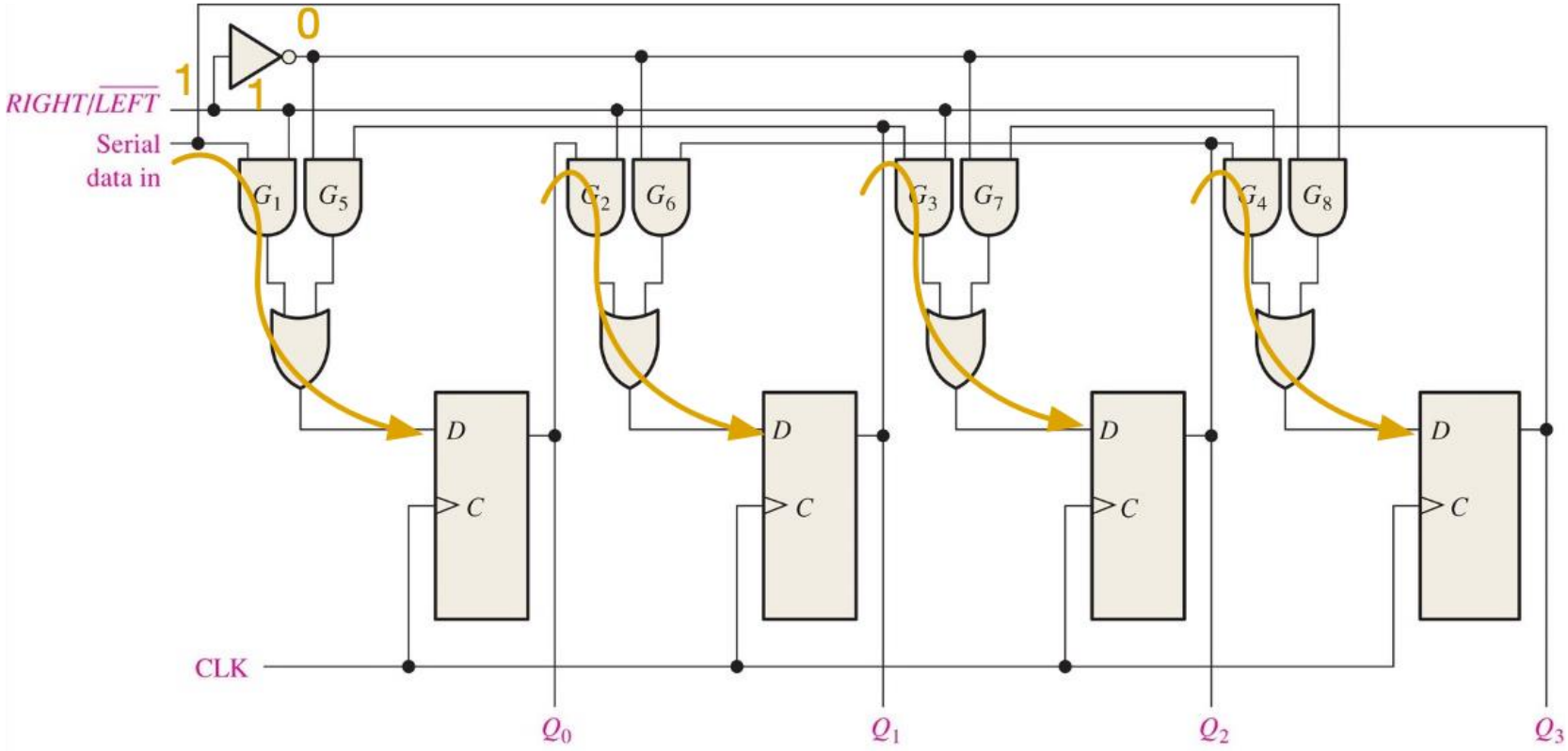
Bidirectional Shift Registers

- RIGHT/$\overline{\text{LEFT}}$ controls data bits inside the register to be shifted left or right



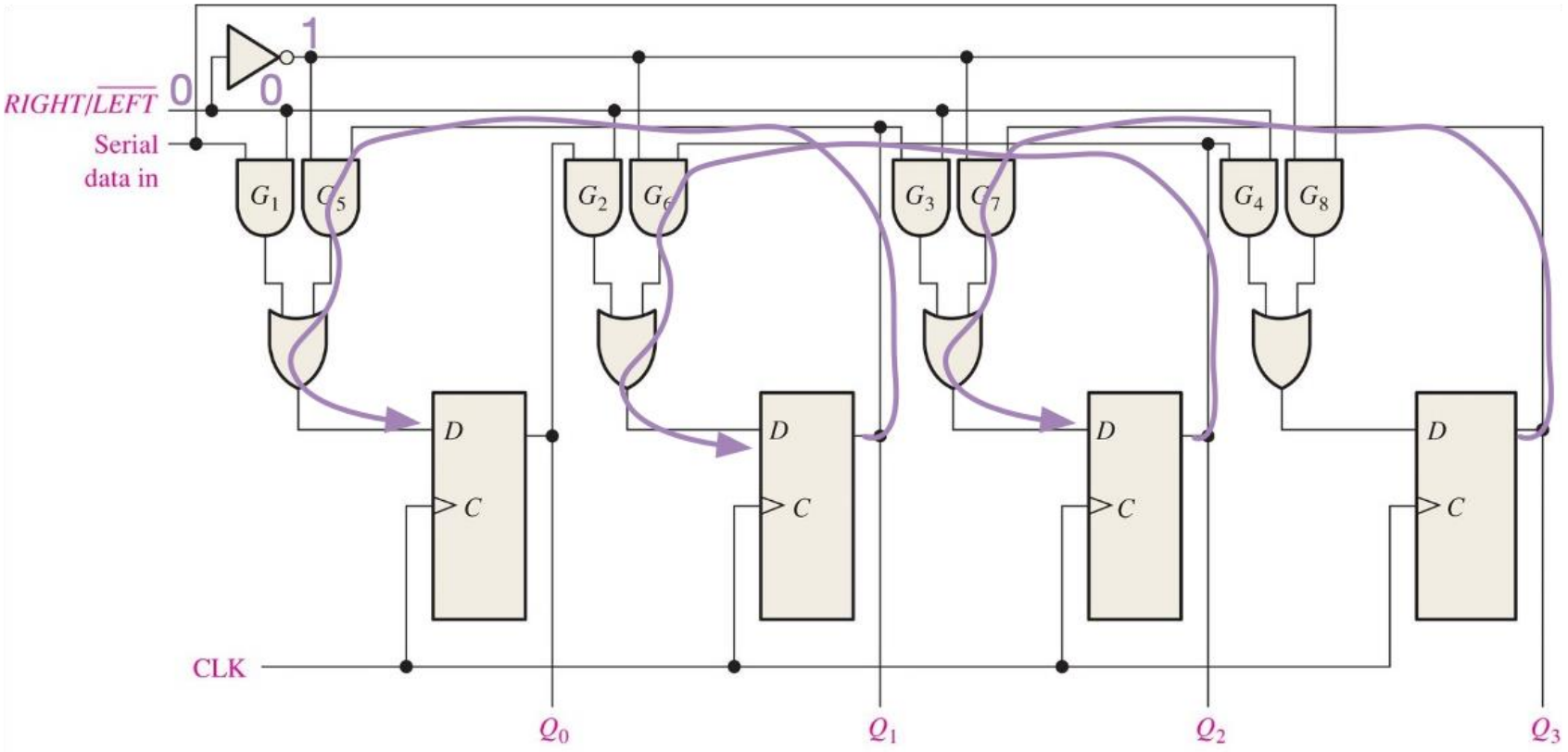
Bidirectional Shift Registers

- RIGHT/$\overline{\text{LEFT}}$ HIGH: G_1 ~ G_4 are enabled, and the state of the Q output of each flip-flop is passed through to the D input of the **following** flip-flop.



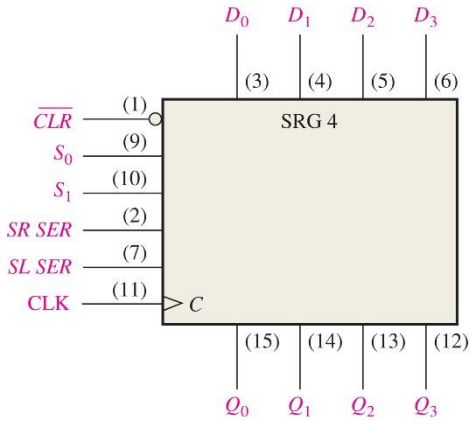
Bidirectional Shift Registers

- RIGHT/$\overline{\text{LEFT}}$ LOW: G_5 ~ G_8 are enabled, and the Q output of each flip-flop is passed through to the D input of the **preceding** flip-flop.

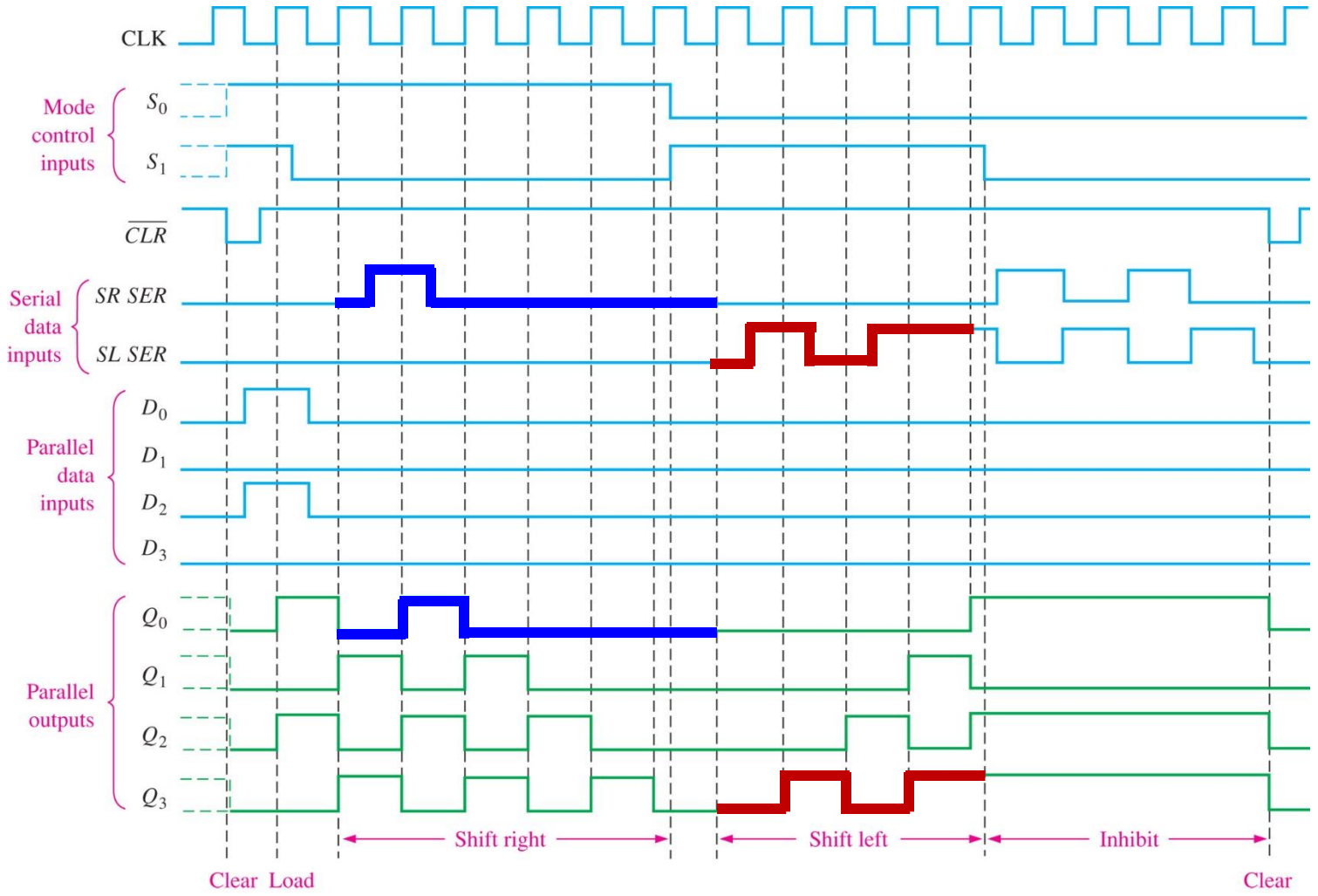


Example

- 4-Bit Bidirectional Universal Shift Register

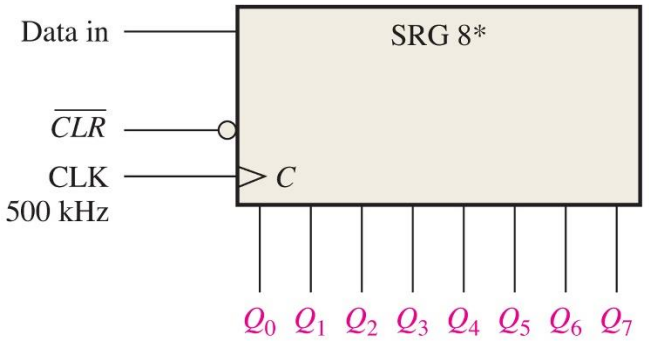


S_0	S_1	Func.
HIGH	HIGH	Parallel Loading
HIGH	LOW	Shift right
LOW	HIGH	Shift left
LOW	LOW	Inhibit

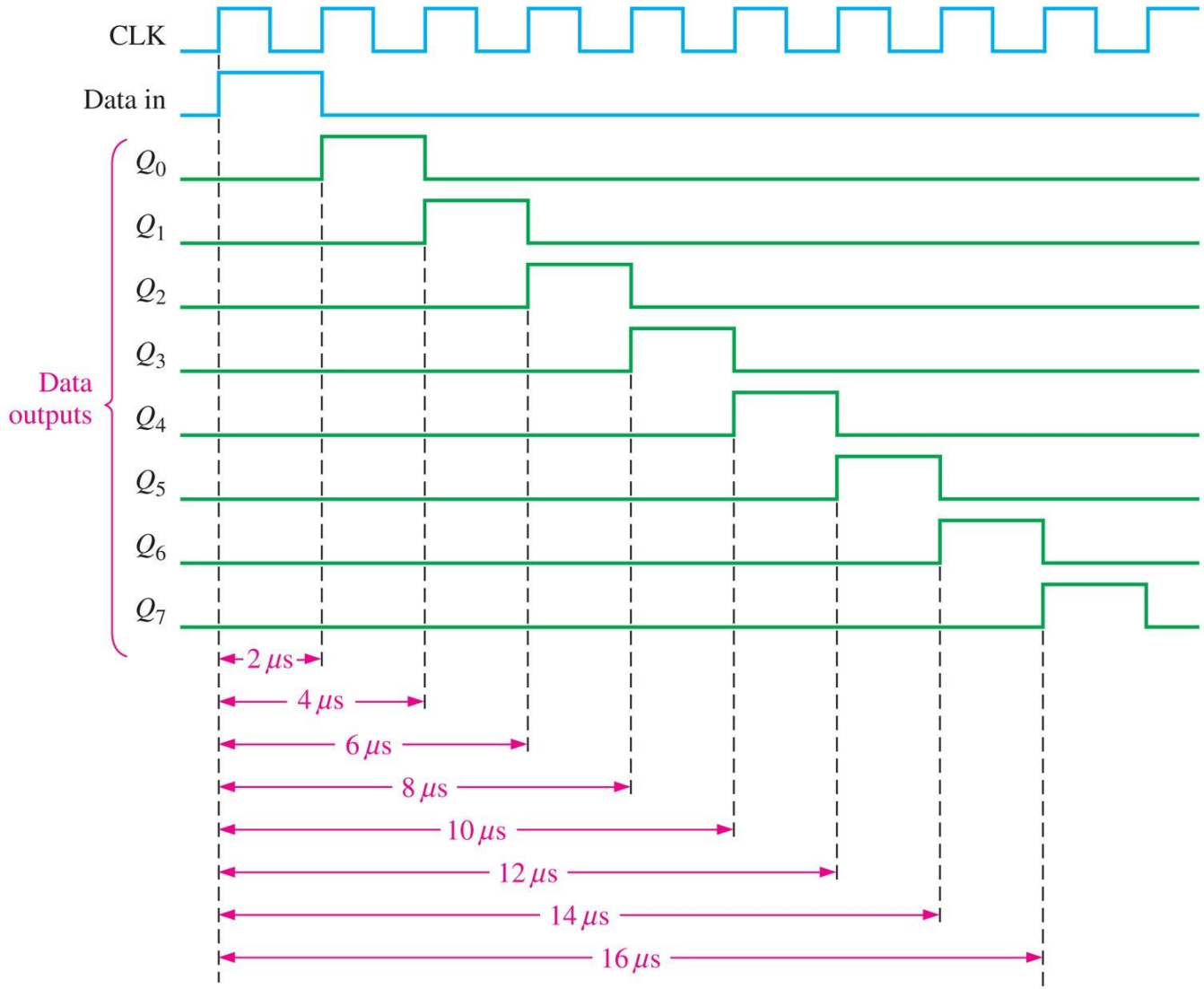


Shift Register Applications

Time Delay

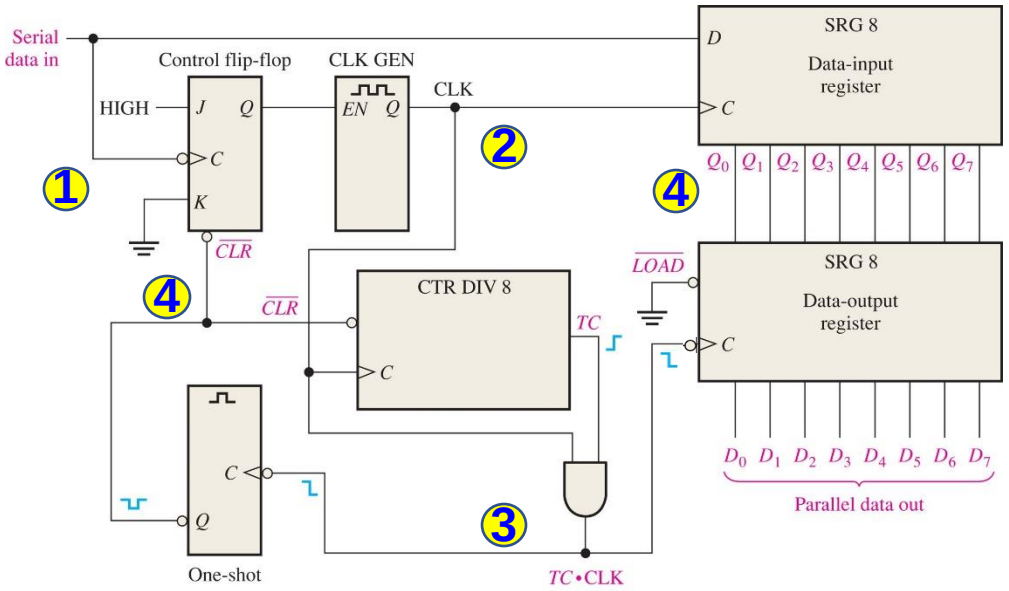


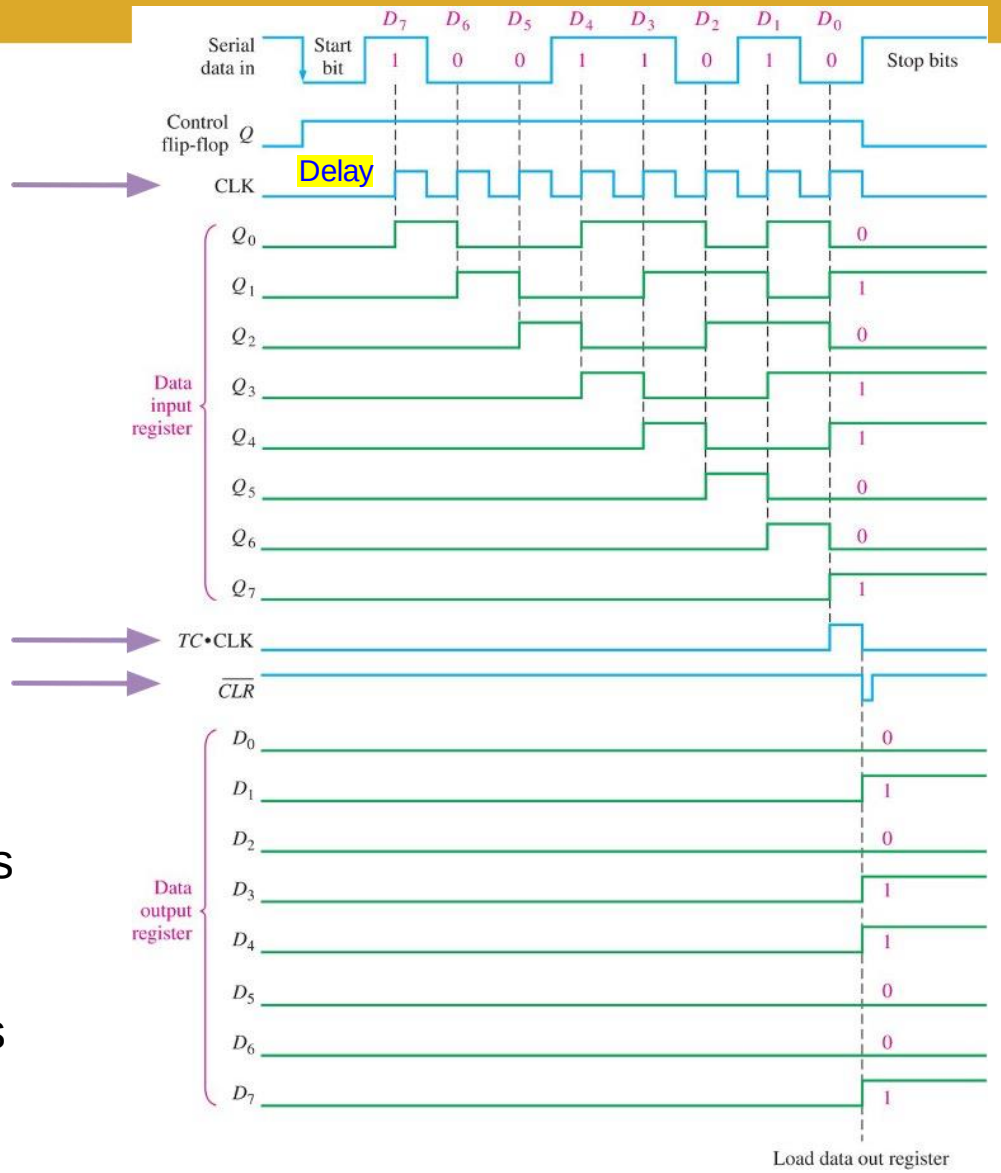
* Data shifts from Q_0 toward Q_7.



- A serial in/serial out shift register can provide a time delay from input to output
- The delay is a function of both the number of stages (n) in the register and the clock frequency.

S/P Data Converter

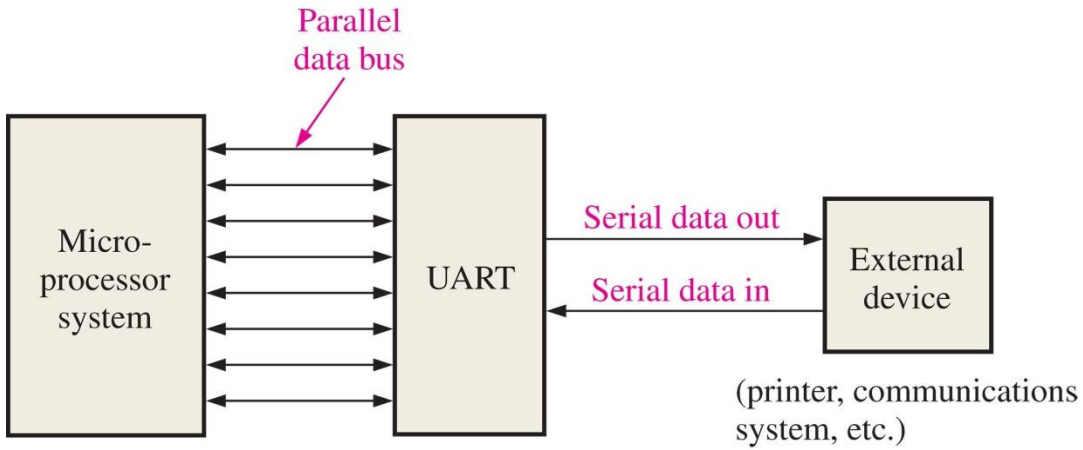


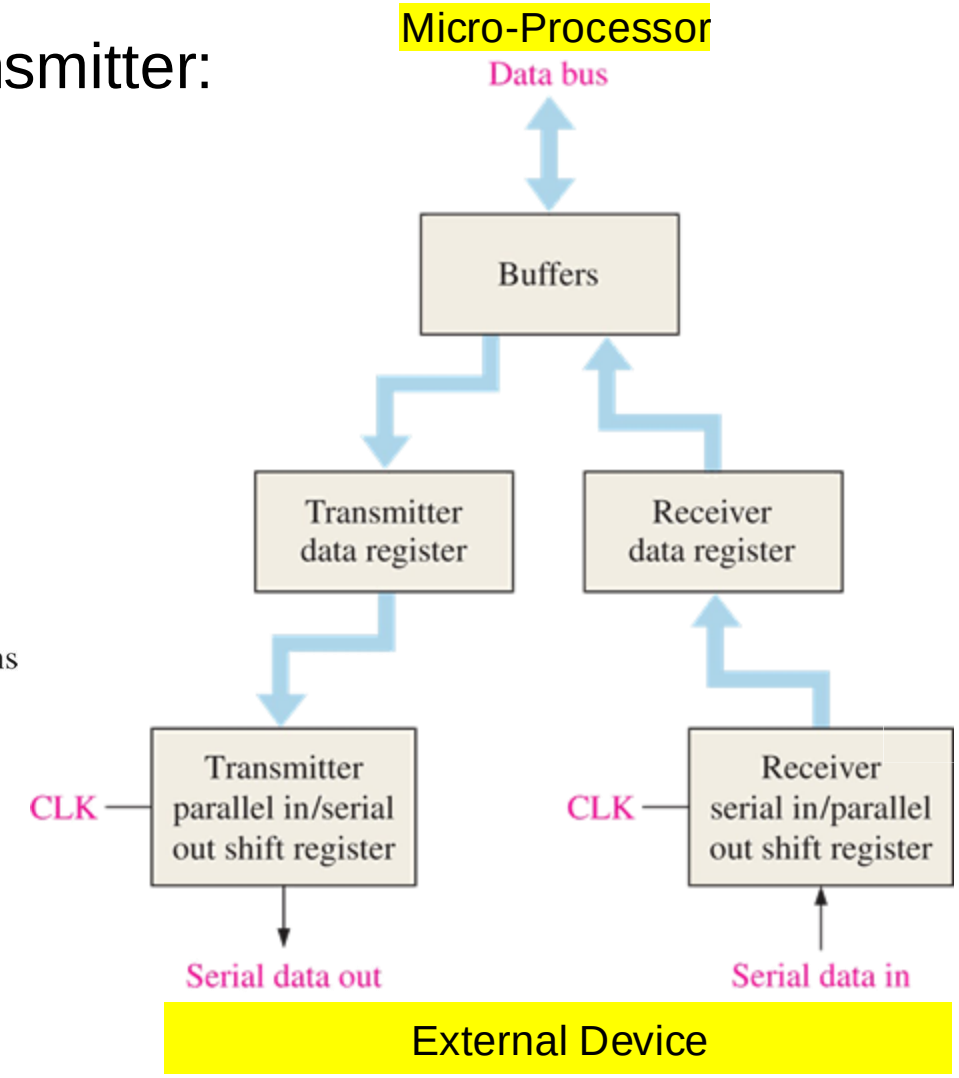


- Serial data transmission can reduce the number of wires in the transmission line.
- USB (universal serial bus) is used to connect keyboards printers, scanners, and more to the computer.

UART

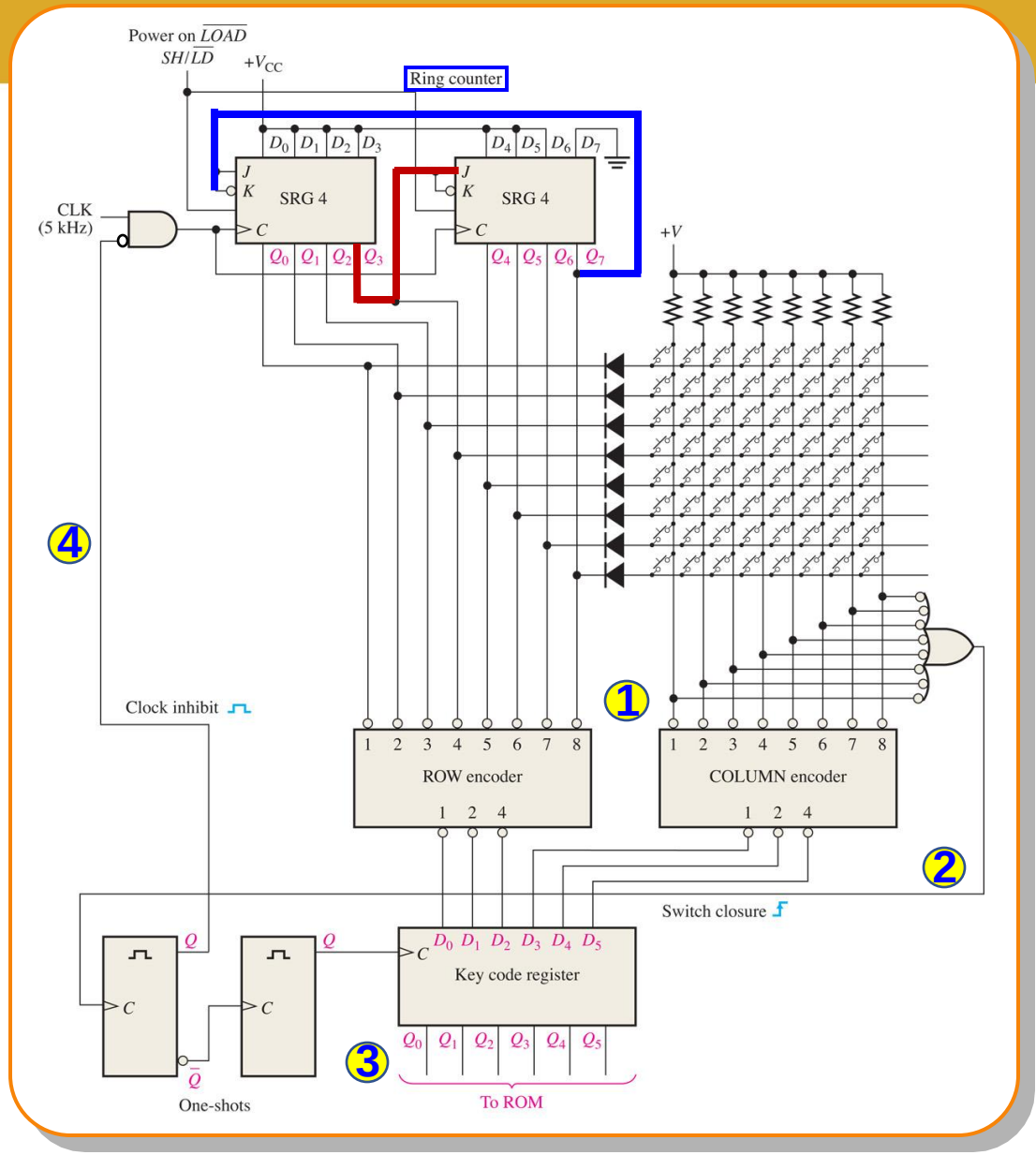
- Universal Asynchronous Receiver Transmitter:
  - Interfacing device for data conversions



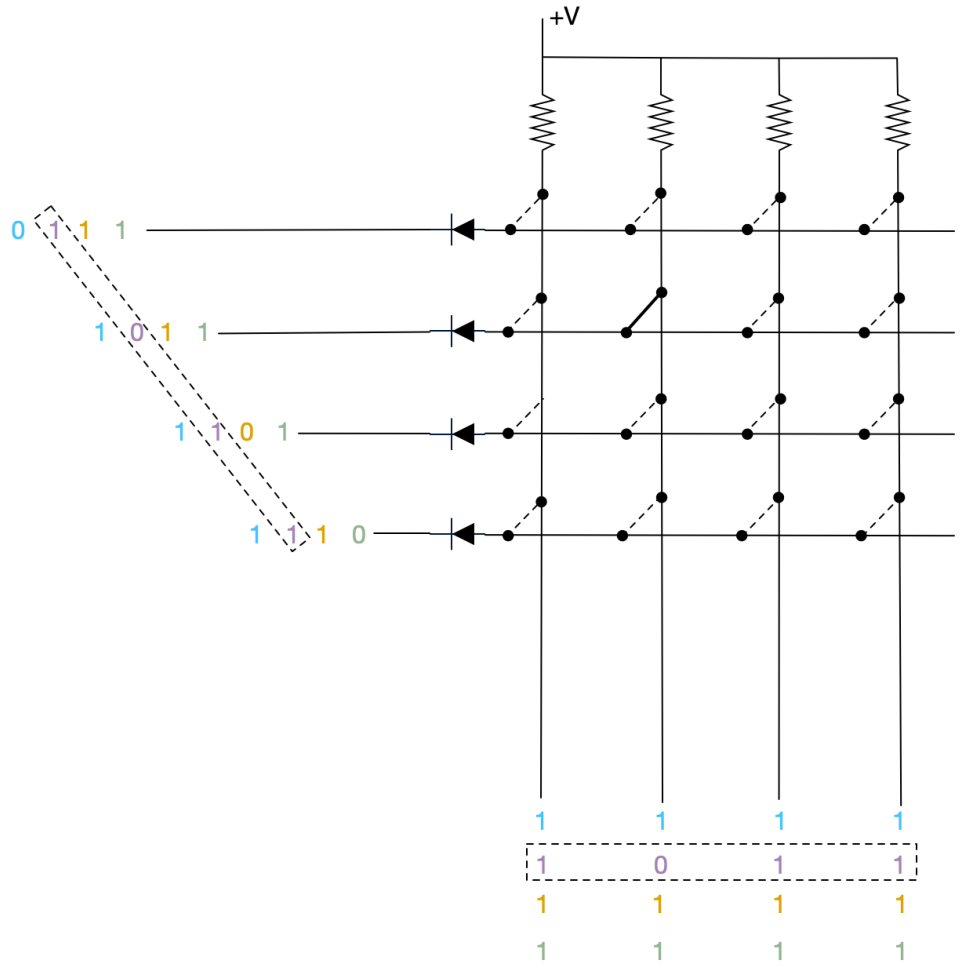


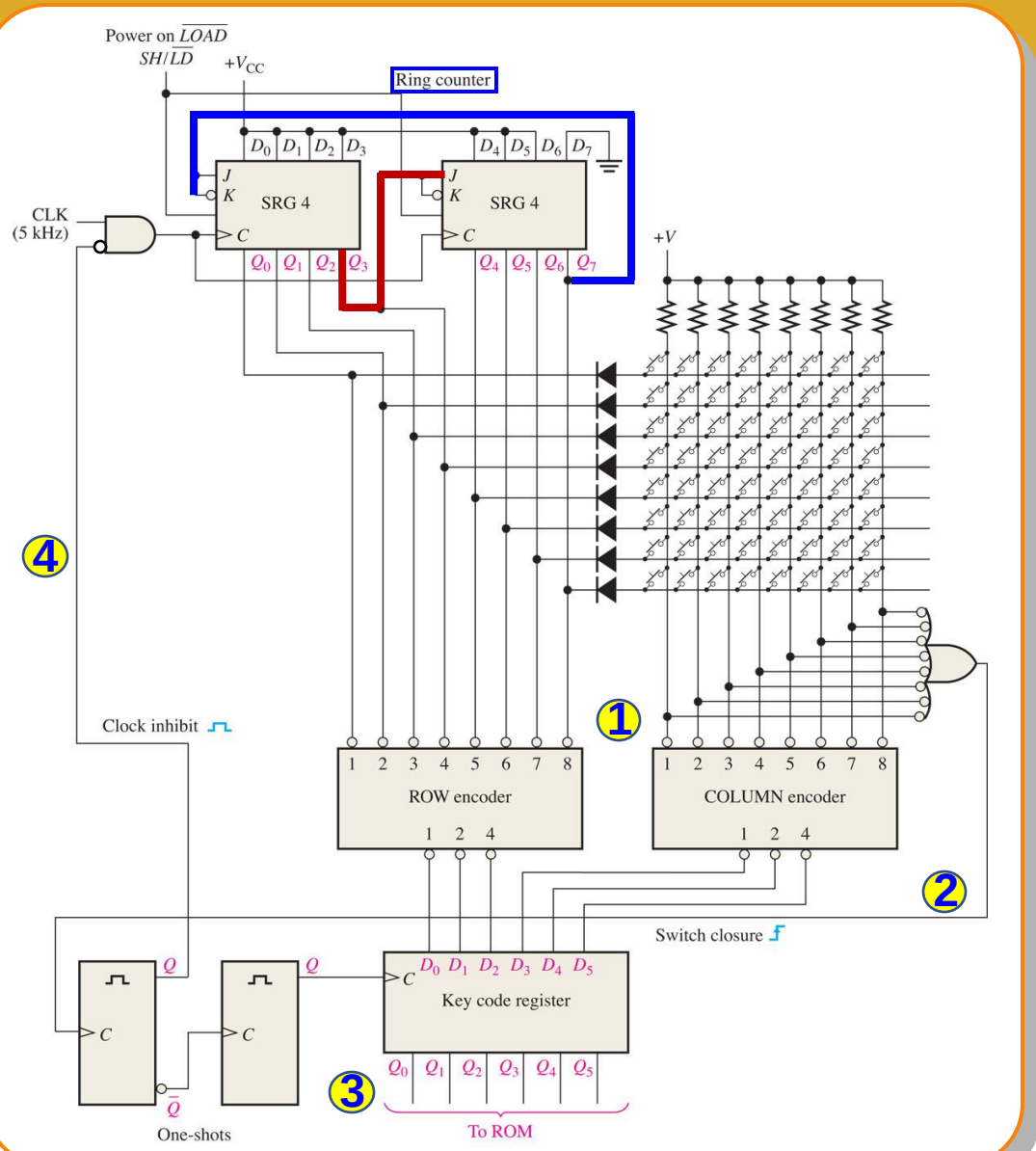
Keyboard Encoder

- Initially, 11111110 is loaded into the ring counter when Power ON;
- Then, the ring counter “scans” the rows for a key closure as the clock signal shifts the 0 around the counter at a 5 kHz rate.
- If a key closure occurs, one COLUMN line is connected to one ROW line. When the ROW line is taken LOW by the ring counter, that particular COLUMN line is also pulled LOW.
- The 3-bit ROW code plus the 3-bit COLUMN code uniquely identifies the key that is closed.
- When a key is closed, the two one-shots produce a delayed clock pulse to parallel-load the 6-bit code into the key code register. (To avoid contact bounce)
- The first one-shot output inhibits the ring counter to prevent it from scanning when the data are being loaded into the key code register.



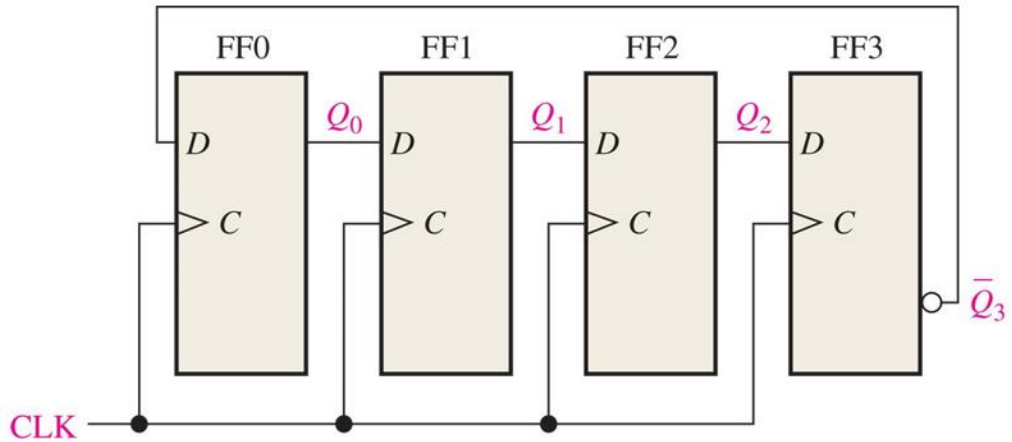
Keyboard Encoder





Johnson Counter
Ring Counter

Johnson Counters



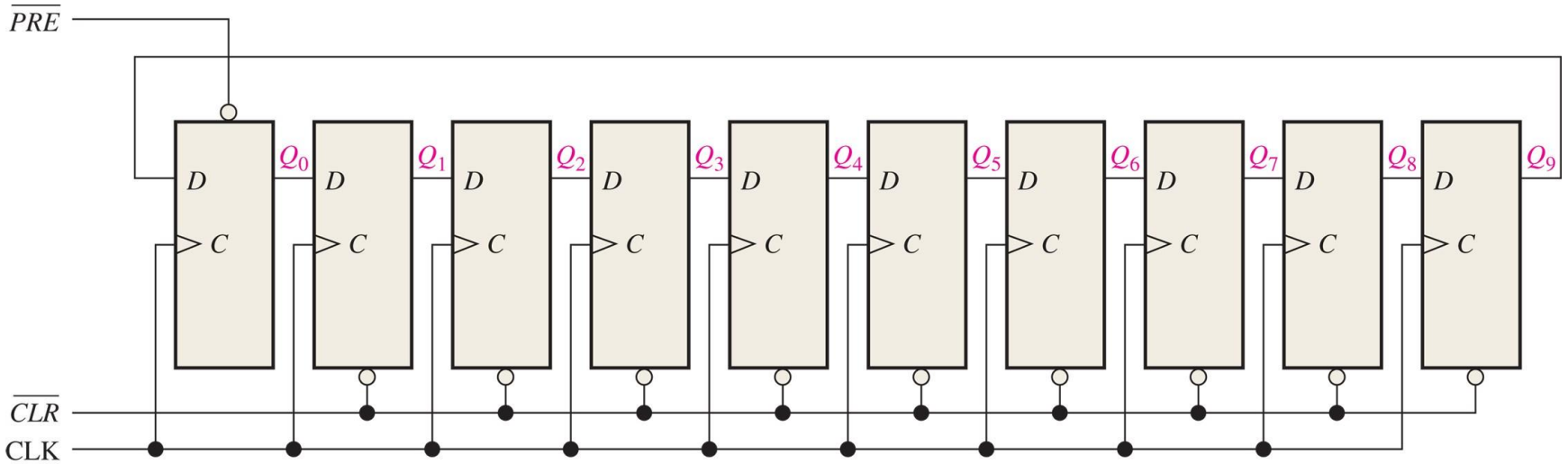
(a) Four-bit Johnson counter

Four-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

- Q' of the last flip-flop is connected back to the D input of the first flip-flop
- If the counter starts at 0, this feedback arrangement produces a characteristic sequence of states
- In general, a Johnson counter will produce a modulus of 2n, where n is the number of stages in the counter, e.g. for n=4 stages, 8 states.

Ring Counters

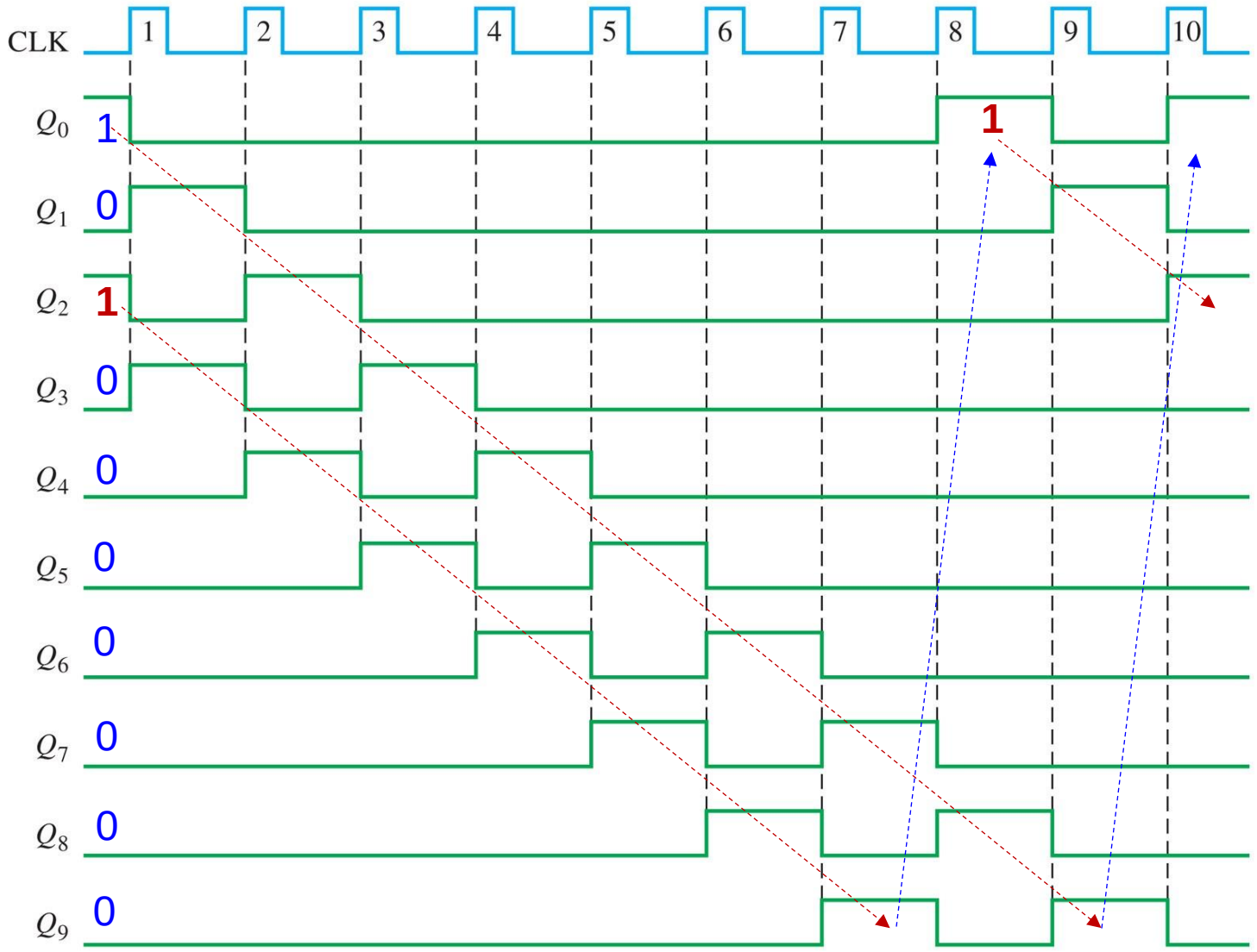


- Q is fed back from the last stage
- Initially, a 1 is preset into the first flip-flop, and the rest of the flip-flops are cleared.

Ten-bit ring counter sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	Q_9
0	1	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0
5	0	0	0	0	0	1	0	0	0	0
6	0	0	0	0	0	0	1	0	0	0
7	0	0	0	0	0	0	0	1	0	0
8	0	0	0	0	0	0	0	0	1	0
9	0	0	0	0	0	0	0	0	0	1

Example



Chapter Review

- Shift Registers
  - Data storage
  - Data movement
  - Serial/Parallel In - Serial/Parallel Out
- Bidirectional Shift Registers
- Shift Register Applications
  - Time Delay
  - Serial-to-Parallel Data Converter
  - UART (Universal Asynchronous Receiver Transmitter
  - Keyboard Encoder
- Johnson Counter & Ring Counter

True/False Quiz

- ✓ Shift registers consist of an arrangement of flip-flops.
- ✗ A shift register cannot be used to store data.
- ✓ A serial shift register accepts one bit at a time on a single line.
- ✗ All shift registers are defined by specified sequences.
- ✓ A shift register counter is a shift register with the serial output connected back to the serial input.
- ✓ A shift register with four stages can store a maximum count of fifteen.
- ✓ The Johnson counter is a special type of shift register.
- ✗ The modulus of an 8-bit Johnson counter is eight.
- ✓ A ring counter uses one flip-flop for each state in its sequence.
- ✗ A shift register cannot be used as a time delay device.