

ECE 2050 Digital Logic and Systems

# Chapter 3 : Logic Gates

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# Announcements

- ❑ HW1 has been released. Due on Feb. 20, 2025.



# Last Week

- ☐ Base-R Number System
  - ☐ Decimal Number System
  - ☐ Binary Number System
  - ☐ Number Conversion
- ☐ Octal & Hexadecimal Numbers
  - ☐ Conversion btw. Binary, Octal, & Hex. Numbers
- ☐ Binary Arithmetic
- ☐ Signed Numbers and Two's Complement Numbers
- ☐ Fixed-Point Numbers & Floating-Point Numbers
- ☐ Binary Coded Decimal and Gray Code
- ☐ Error Codes

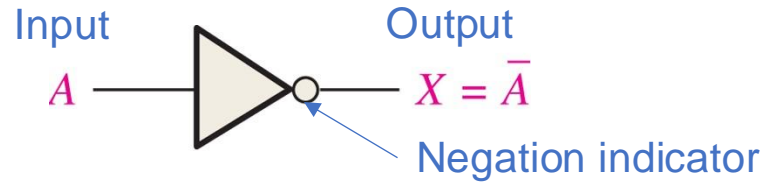


# Logic Gates

- **Perform logic functions:**
  - inversion (NOT), AND, OR, NAND, NOR, etc.
- **Single-input:**
  - NOT gate, buffer
- **Two-input/Multiple-input:**
  - AND, OR, XOR, NAND, NOR, XNOR



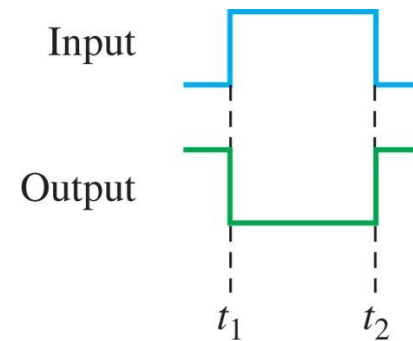
# The Inverter



❑ **Truth Table** shows the output for each possible input in terms of levels and corresponding bits.

Input	Output
LOW (0)	HIGH (1)
HIGH (1)	LOW (0)

❑ **Timing diagrams:** a graph that displays the relationship of two or more waveforms with respect to each other on a time basis



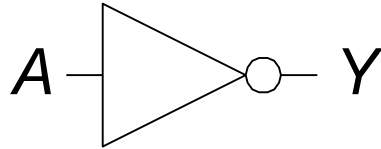
❑ **Logic Expression:** The complement of a variable designated by a bar over the letter

$$X = \bar{A}$$



# Single-Input Logic Gates

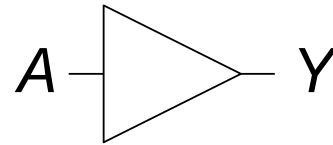
**NOT**



$$Y = \overline{A}$$

$A$	$Y$
0	
1	

**BUF**



$$Y = A$$

$A$	$Y$
0	
1	



# The AND Gate

Inputs  $\geq 2$       Output



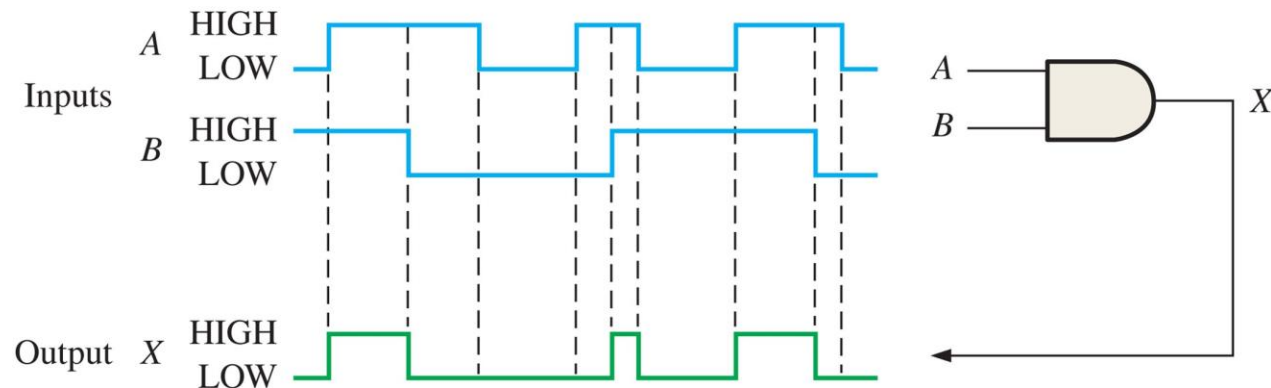
- **Truth Table** : for an n-input AND gate, the total number of possible input combinations is  $2^n$ .

<i>A</i>	<i>B</i>	<i>AB = X</i>
0	0	$0 \cdot 0 = 0$
0	1	$0 \cdot 1 = 0$
1	0	$1 \cdot 0 = 0$
1	1	$1 \cdot 1 = 1$

- **Timing diagrams:**

- **Logic Expression**

$$X = AB$$



# The OR Gate

Inputs  $\geq 2$

Output

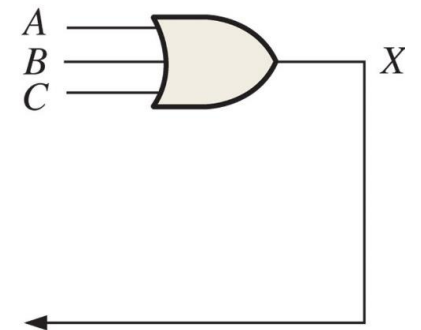
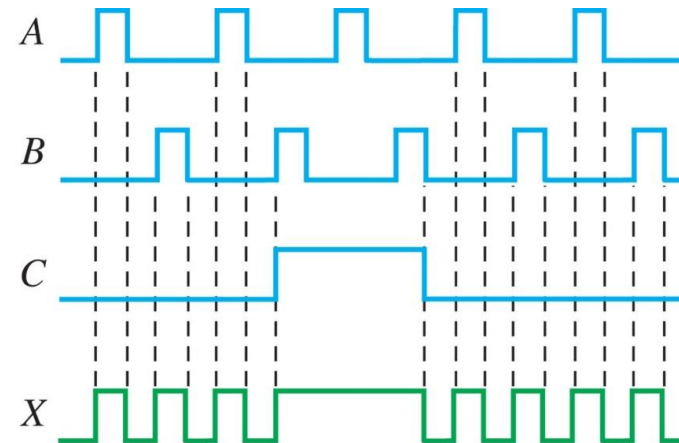


❑ Logic Expression  $X = A + B$

❑ Truth Table

$A$	$B$	$A + B = X$
0	0	$0 + 0 = 0$
0	1	$0 + 1 = 1$
1	0	$1 + 0 = 1$
1	1	$1 + 1 = 1$

❑ Timing diagrams

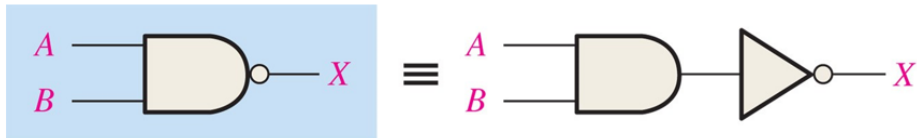




# The NAND Gate

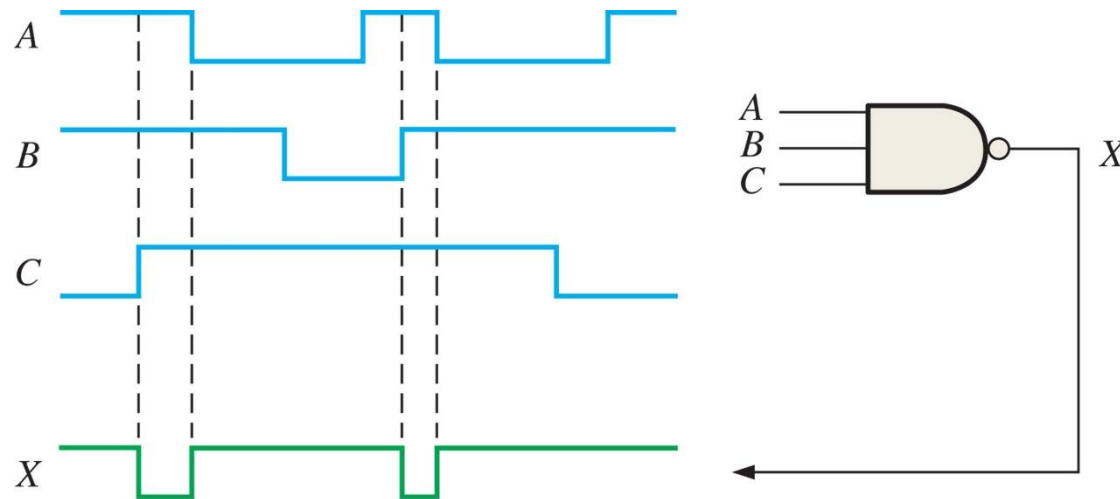
Inputs  $\geq 2$

Output



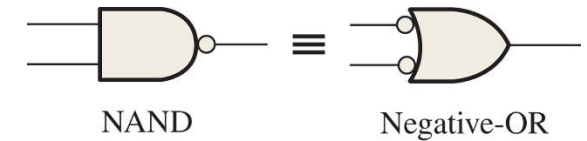
□ Logic Expression  $X = \overline{AB} = \overline{A} + \overline{B}$

□ Timing diagrams



□ Truth Table

$A$	$B$	$\overline{AB} = X$
0	0	$\overline{0 \cdot 0} = \overline{0} = 1$
0	1	$\overline{0 \cdot 1} = \overline{0} = 1$
1	0	$\overline{1 \cdot 0} = \overline{0} = 1$
1	1	$\overline{1 \cdot 1} = \overline{1} = 0$

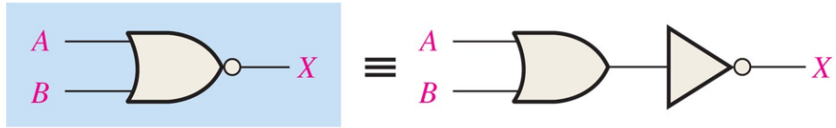


*How to verify/prove?*



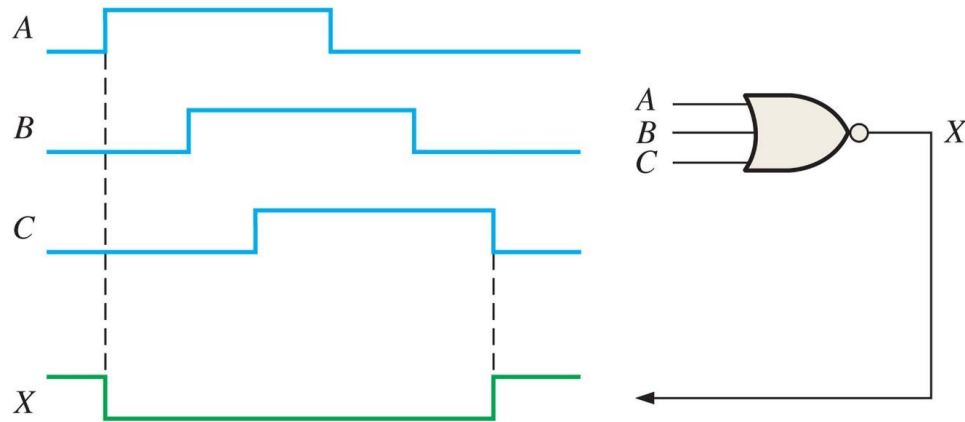
# The NOR Gate

Inputs  $\geq 2$       Output



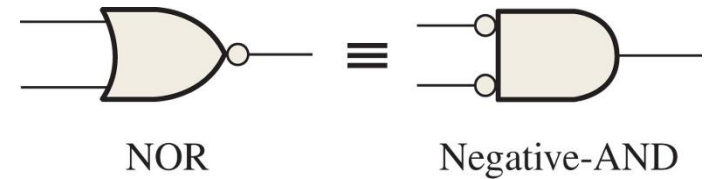
□ Logic Expression  $X = \overline{A + B} = \overline{A} \overline{B}$

□ Timing diagrams



□ Truth Table

Inputs		Output
$A$	$B$	$X$
0	0	1
0	1	0
1	0	0
1	1	0



*How to verify/prove?*



# The Exclusive-OR and Exclusive-NOR Gates

## Exclusive-OR (XOR) Gates



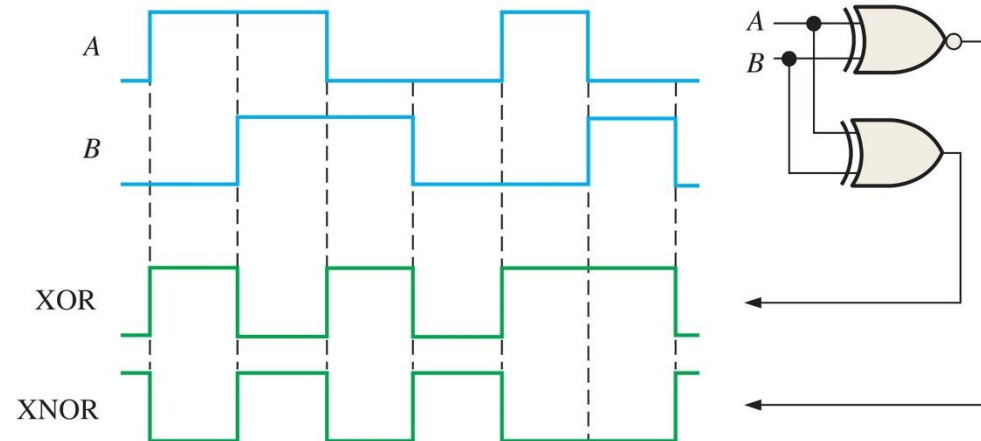
Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

## Exclusive-NOR (XNOR) Gates



Inputs		Output
A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

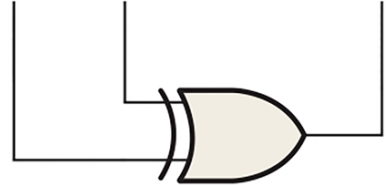
## Timing diagram of XOR and XNOR



# XOR: Application

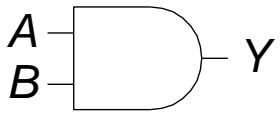
An XOR gate can be used to add two bits

Input Bits		Output (Sum)
<i>A</i>	<i>B</i>	$\Sigma$
0	0	0
0	1	1
1	0	1
1	1	0 (without the 1 carry bit)

A circuit diagram of an XOR gate. It consists of a light beige trapezoidal gate with a curved left side and a pointed right side. Two input lines enter from the left: one at the top and one at the bottom. A single output line exits from the right side. The gate is shown in a perspective view.

# Two-input Logic Gates

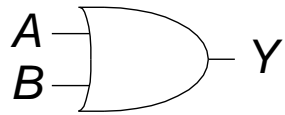
## AND



$$Y = AB$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

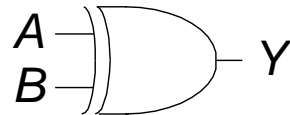
## OR



$$Y = A + B$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

## XOR



$$Y = A \oplus B$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

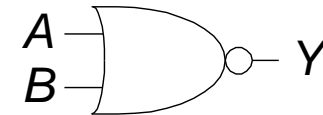
## NAND



$$Y = \overline{AB}$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

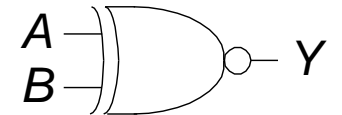
## NOR



$$Y = \overline{A + B}$$

A	B	Y
0	0	
0	1	
1	0	
1	1	

## XNOR



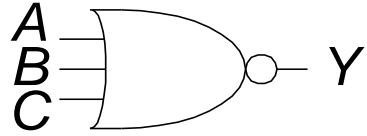
$$Y = \overline{A \oplus B}$$

A	B	Y
0	0	
0	1	
1	0	
1	1	



# Multiple-Input Logic Gates

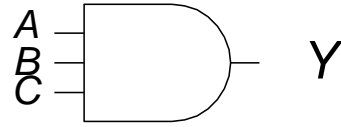
## NOR3



$$Y = \overline{A+B+C}$$

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

## AND3



$$Y = ABC$$

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

- Multi-input XOR: Odd parity  
Output true if an odd number of inputs are true

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Truth table rows are listed in binary order.



# George Boole, 1815-1864

- Born to working class parents
- Taught himself mathematics and joined the faculty of Queen's College in Ireland
- Wrote *An Investigation of the Laws of Thought* (1854)
- Introduced binary variables
- Introduced the three fundamental logic operations: AND, OR, and NOT

# Logic Levels





# Logic Levels

- Discrete voltages represent 1 and 0
- For example:
  - 0 = *ground* (GND) or 0 volts
  - 1 =  $V_{DD}$  or 5 volts
- What about 4.99 volts? Is that a 0 or a 1?
- What about 3.2 volts?



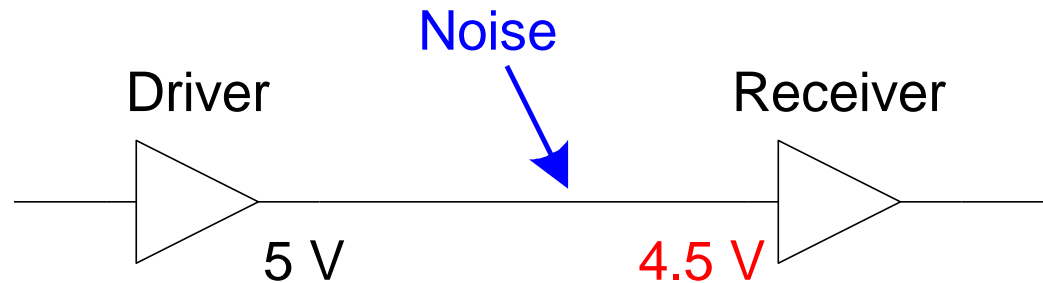
# Logic Levels

- *Range* of voltages for 1 and 0
- Different ranges for inputs and outputs to allow for *noise*



# What is Noise?

- **Anything that degrades the signal**
  - E.g., resistance, power supply noise, coupling to neighboring wires, etc.
- **Example:** a gate (driver) outputs 5 V but, because of resistance in a long wire, receiver gets 4.5 V

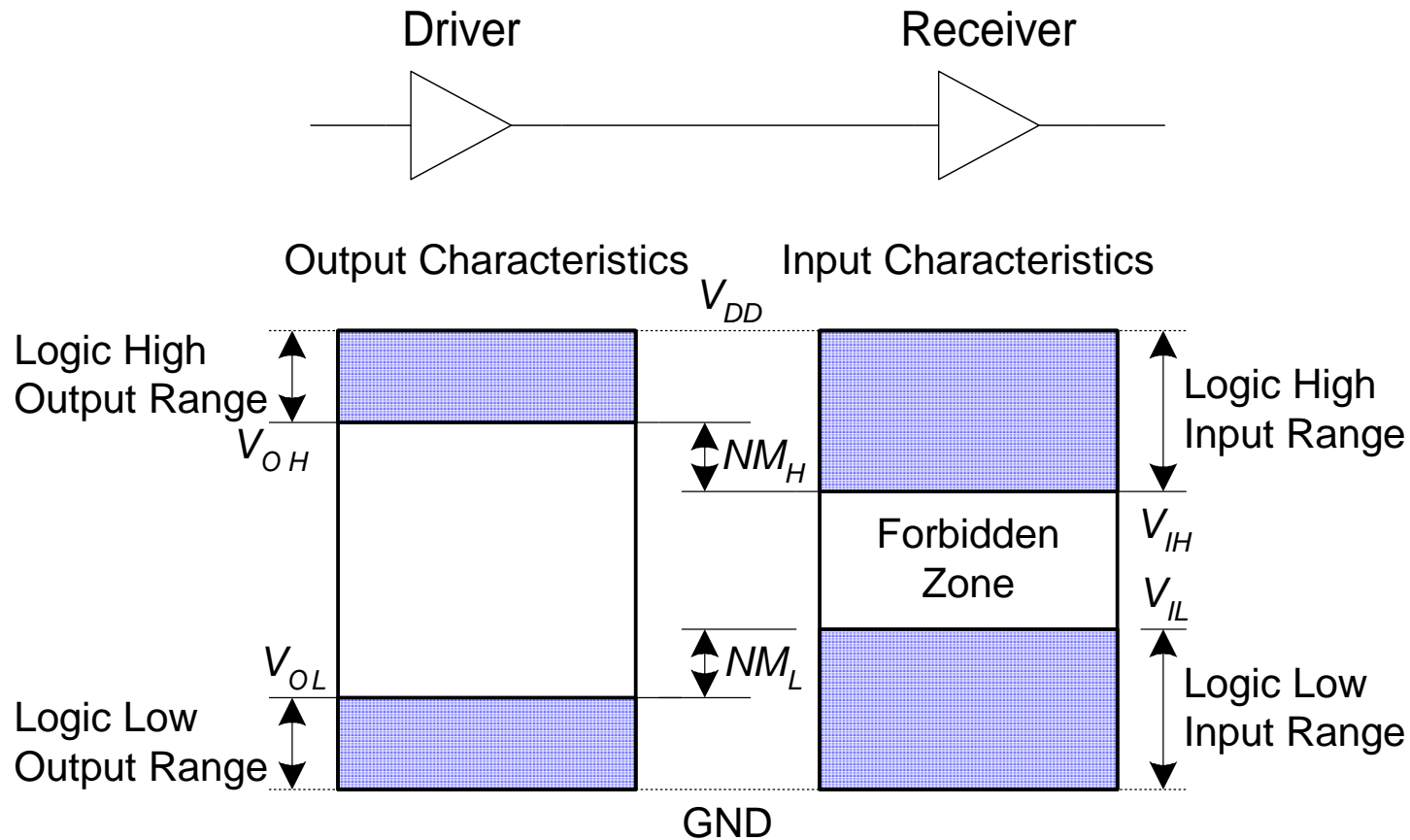


# The Static Discipline

- With logically valid inputs, every circuit element must produce logically valid outputs
- Use limited ranges of voltages to represent discrete values



# Noise Margins



**High Noise Margin:**

$$NM_H =$$

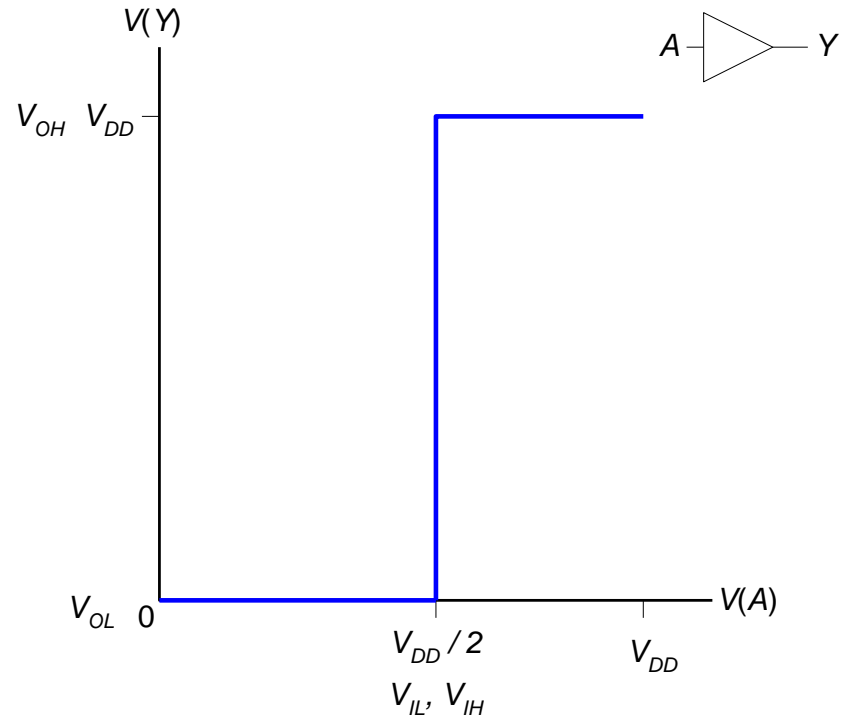
**Low Noise Margin:**

$$NM_L =$$



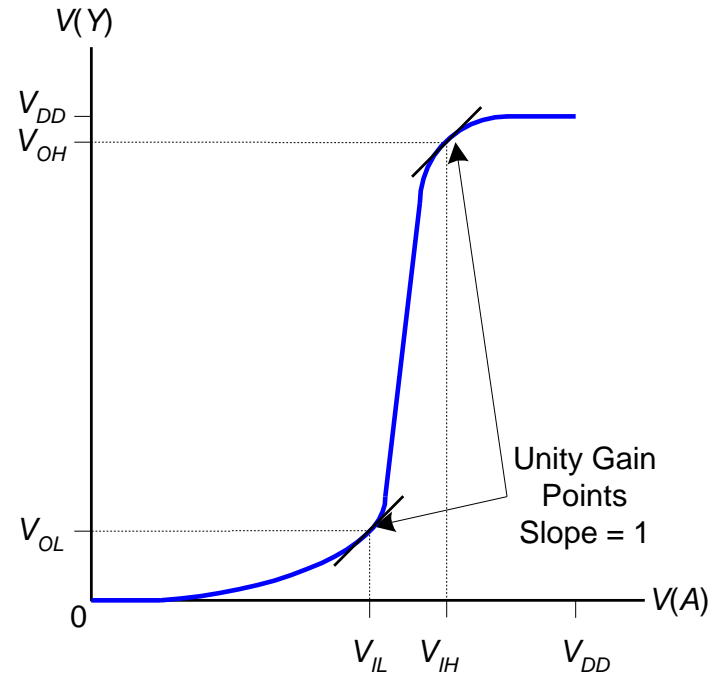
# DC Transfer Characteristics

Ideal Buffer:



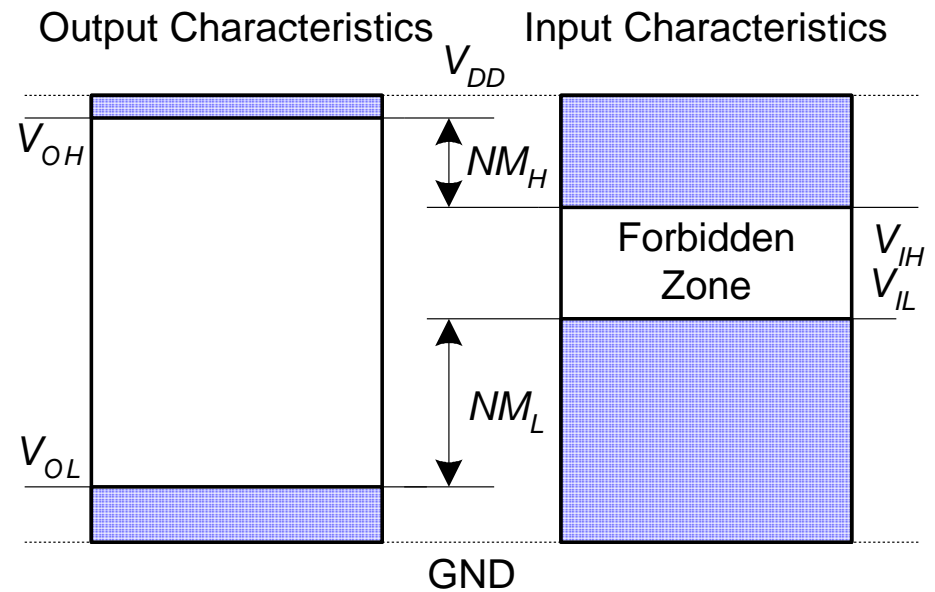
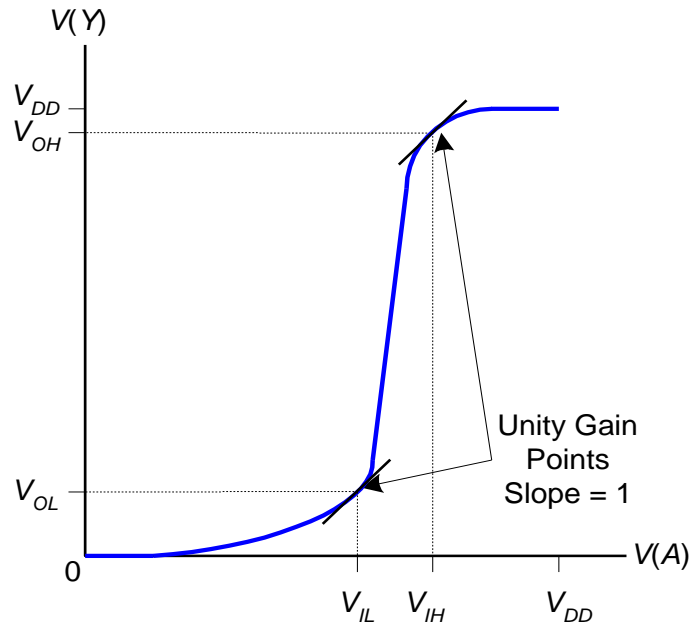
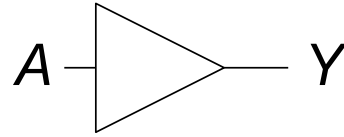
$$NM_H = NM_L = V_{DD}/2$$

Real Buffer:



$$NM_H, NM_L < V_{DD}/2$$

# DC Transfer Characteristics



# VDD Scaling

- In 1970's and 1980's,  $V_{DD} = 5\text{ V}$
- $V_{DD}$  has dropped
  - Avoid frying tiny transistors
  - Save power
- 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, 1.0 V, ...
  - Be careful connecting chips with different supply voltages





# VDD Scaling

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  - Be careful connecting chips with different supply voltages

**Chips operate because they contain magic smoke**

**Proof:** if the magic smoke is let out, the chip stops working



# Logic Family Examples

Logic Family	$V_{DD}$	$V_{IL}$	$V_{IH}$	$V_{OL}$	$V_{OH}$
TTL	5 (4.75 - 5.25)	0.8	2.0	0.4	2.4
CMOS	5 (4.5 - 6)	1.35	3.15	0.33	3.84
LVTTL	3.3 (3 - 3.6)	0.8	2.0	0.4	2.4
LVC MOS	3.3 (3 - 3.6)	0.9	1.8	0.36	2.7



# Chapter Review

## ❑ Logic gates

- ◆ Inverter, AND, OR, NAND, NOR, XOR, XNOR
- ◆ Truth Table
- ◆ Timing diagram
- ◆ Logic expression
- ◆ Distinctive Shape Symbols

## ❑ Logic Levels

- ◆ Logic levels
- ◆ Noise Margins



# True/False Quiz



An inverter performs a NOT operation.



A NOT gate cannot have more than one input.



If any input to an OR gate is zero, the output is zero.



If all inputs to an AND gate are 1, the output is 0.



A NAND gate can be considered as an AND gate followed by a NOT gate.



A NOR gate can be considered as an OR gate followed by an inverter.



The output of an exclusive-OR is 0 if the inputs are opposite.

