



香港中文大學(深圳)
The Chinese University of Hong Kong, Shenzhen

ECE2050 Digital Logic and Systems

Tutorial 5

Wangqian Chen

Contact: wangqianchen@link.cuhk.edu.cn

Office Hour: 16:00-17:00 Wed., ZX305

Combinational Logic Analysis

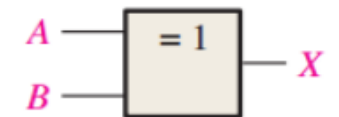
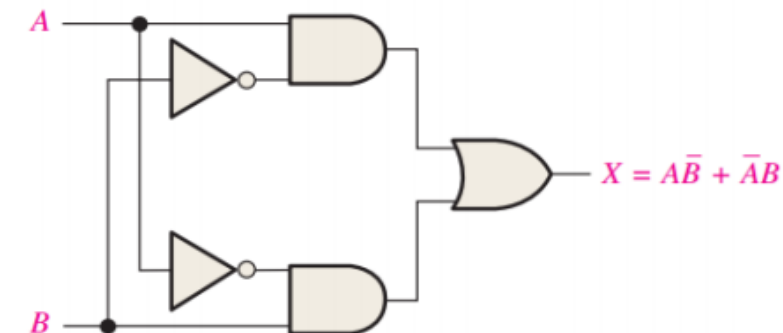
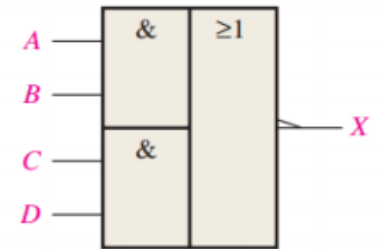
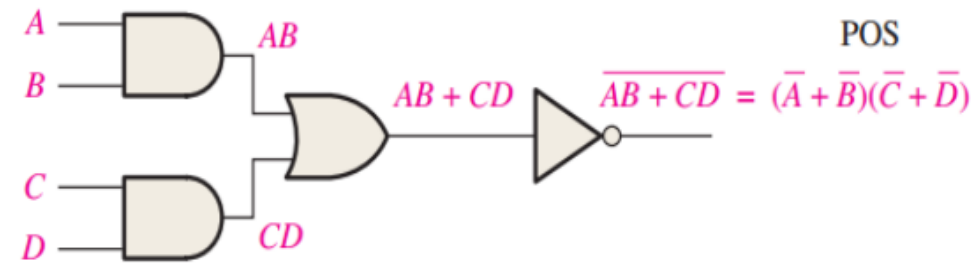
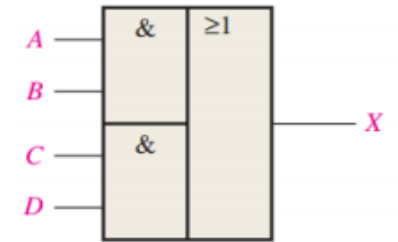
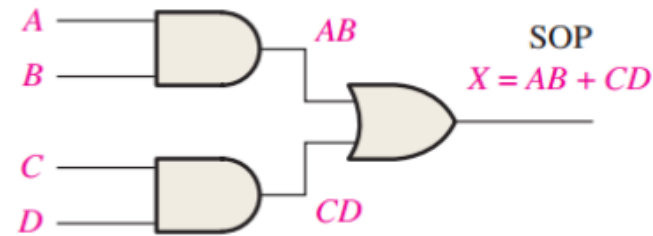
Outline

- Analyze basic combinational logic circuits and write the Boolean output expression.
- Develop a truth table from the output expression for a combinational logic circuit.
- Design a combinational logic circuit.
- Analyze the operation of logic circuits with pulse inputs.



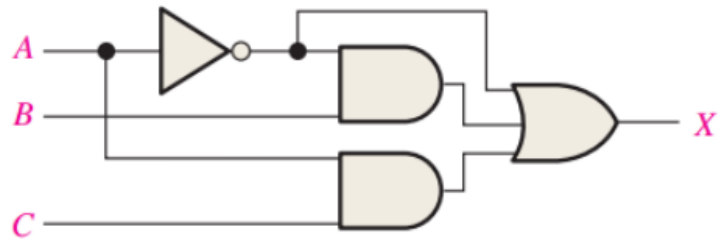
Basic Combinational Logic Analysis

- AND-OR Logic:
- AND-OR-Invert Logic:
- Exclusive-OR Logic:

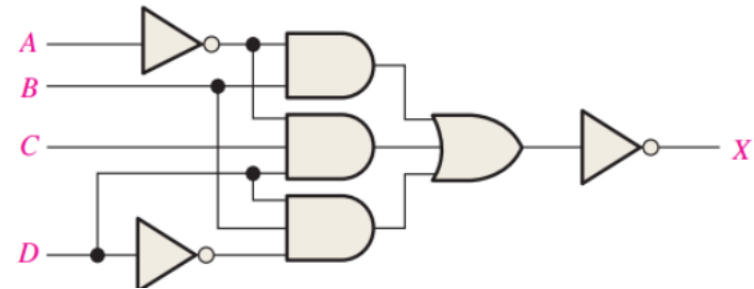


Basic Combinational Logic Analysis

Q1. Write the output expression for each circuit in Figure 5–54



a) $X = \bar{A} \cdot B + \bar{A} + A \cdot C$

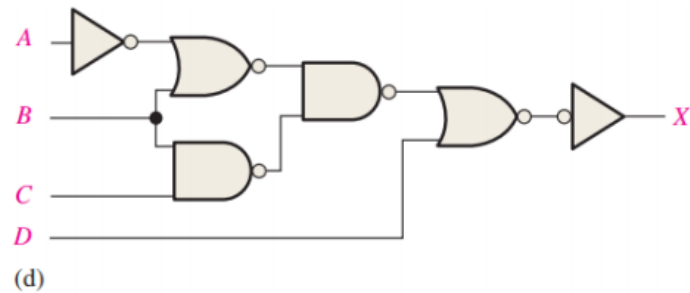


b)
$$\begin{aligned} X &= \overline{(\bar{A} \cdot B + \bar{A} \cdot C \cdot D + D \cdot B \cdot \bar{D})} \\ &= \overline{(\bar{A} \cdot B + \bar{A} C D)} \\ &= (\bar{A} B) \cdot (\bar{A} C D) \\ &= (A + \bar{B}) \cdot (A + \bar{C} + \bar{D}) \\ &= A + A\bar{C} + A\bar{D} + A\bar{B} + \bar{B}\bar{C} + \bar{B}\bar{D} \\ \text{or } X &= \bar{A} B + \bar{A} C D + D B \bar{D} \end{aligned}$$

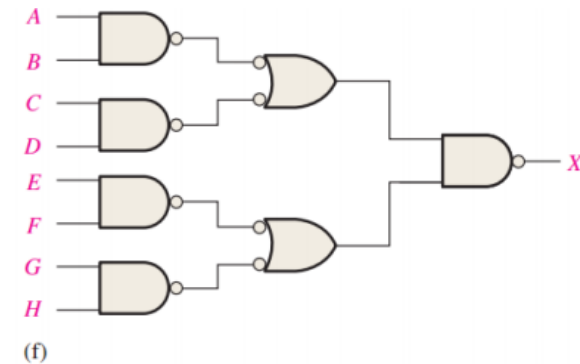


Basic Combinational Logic Analysis

Q2. P303 Figure 5-56 (d) and Figure 5-56 (f)



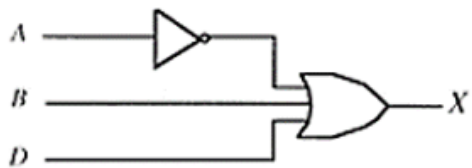
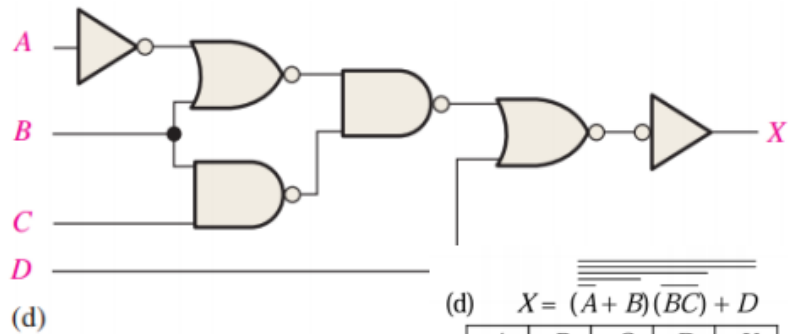
$$X = \overline{(\overline{A} + B)(\overline{BC})} + D = \overline{(\overline{A} + B)(\overline{BC})} + D = \overline{A} + B + BC + D = \overline{A} + B + D$$



$$\begin{aligned} \text{(f)} \quad X &= \overline{(\overline{AB} + \overline{CD})(\overline{EF} + \overline{GH})} = \overline{(\overline{AB} + \overline{CD})(\overline{EF} + \overline{GH})} = \overline{(\overline{AB} + \overline{CD})} + \overline{(\overline{EF} + \overline{GH})} \\ &= (\overline{\overline{AB}})(\overline{\overline{CD}}) + (\overline{\overline{EF}})(\overline{\overline{GH}}) \\ &= (\overline{A} + \overline{B})(\overline{C} + \overline{D}) + (\overline{E} + \overline{F})(\overline{G} + \overline{H}) = \overline{A}\overline{C} + \overline{B}\overline{C} + \overline{A}\overline{D} + \overline{B}\overline{D} + \overline{E}\overline{G} + \overline{F}\overline{G} + \overline{E}\overline{H} + \overline{F}\overline{H} \end{aligned}$$

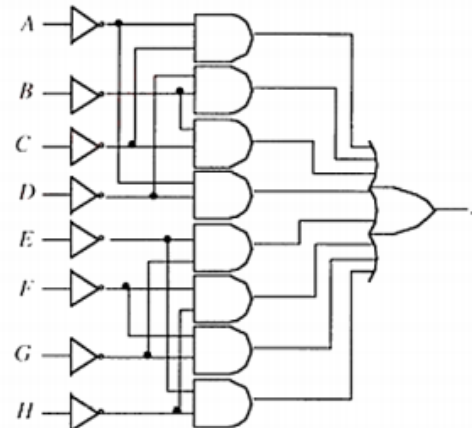
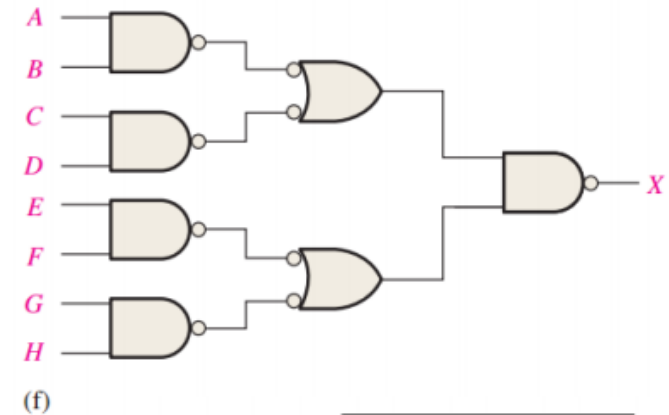


Basic Combinational Logic Analysis



Circuit form

A	B	C	D	X
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



Circuit form

(f) $X = (\overline{AB} + \overline{CD})(\overline{EF} + \overline{GH})$

A	B	C	D	E	F	G	H	I
0	X	0	X	X	X	X	X	1
X	0	0	X	X	X	X	X	1
0	X	X	0	X	X	X	X	1
X	0	X	0	0	X	X	X	1
X	X	X	X	0	X	0	X	1
X	X	X	X	X	0	0	X	1
X	X	X	X	0	X	X	0	1
X	X	X	X	X	0	X	0	1

For all other entries $X = 0$.

$X = \text{don't care}$

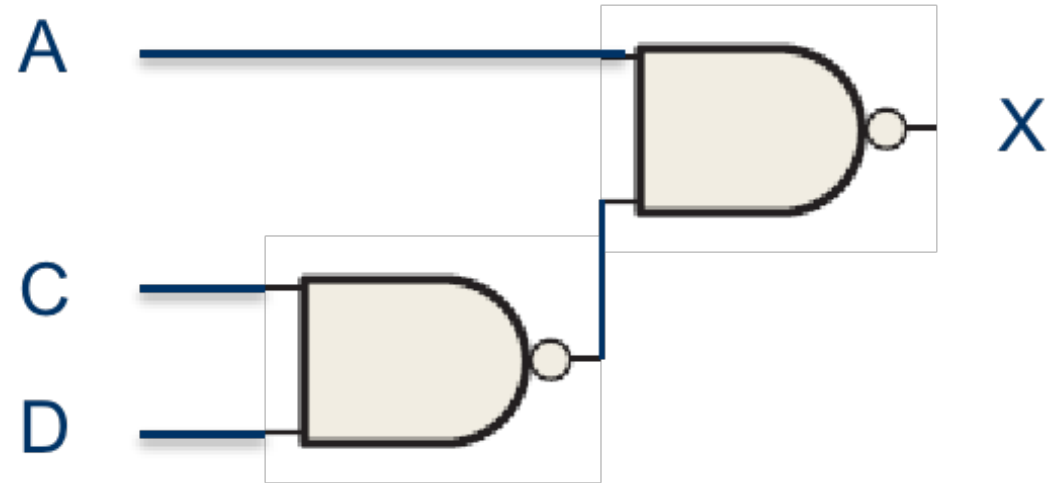


Implementing Combinational Logic

Q3. Use NAND gates, NOR gates or combinations of both to implement the following logic expressions as stated:

$$X = \bar{A}B + CD + \overline{(A + B)}(ACD + \bar{B}\bar{E})$$

$$\begin{aligned} X &= \bar{A}B + CD + \overline{(A + B)}(ACD + \bar{B}\bar{E}) \\ &= \bar{A}B + CD + \bar{A} \cdot \bar{B}(ACD + \bar{B} + \bar{E}) \\ &= \bar{A}B + CD + \bar{A} \cdot \bar{B} + \bar{A} \cdot \bar{B} \cdot \bar{E} \\ &= \bar{A}B + CD + \bar{A} \cdot \bar{B} \\ &= \bar{A} + CD \\ &= \overline{A \cdot \overline{CD}} \end{aligned}$$



Implementing Combinational Logic

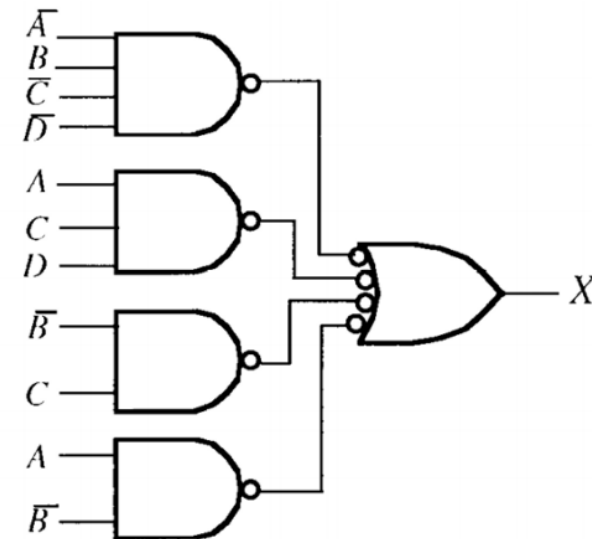
Q4. Implement a logic circuit for the truth table

AB \ CD	00		01		11		10	
	00	01	11	10	00	01	11	10
00	0	0	1	1	0	0	1	1
01	1	0	0	0	0	0	0	0
11	0	0	1	0	0	0	0	0
10	1	1	1	1	0	0	0	0

Groupings and corresponding terms:

- $\bar{B}C$ (Grouping the two 1s in the CD=11 column)
- $\bar{A}B\bar{C}\bar{D}$ (Grouping the 1 in the cell AB=01, CD=00)
- ACD (Grouping the 1 in the cell AB=11, CD=11)
- $A\bar{B}$ (Grouping the four 1s in the AB=10 row)

$$X = \bar{A}\bar{B}\bar{C}\bar{D} + ACD + \bar{B}C + A\bar{B}$$

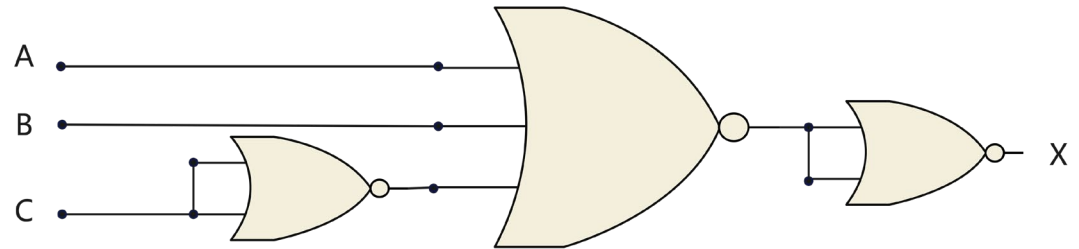


Implementing Combinational Logic

Q5. Show how the following expressions can be implemented as stated using only NOR gates

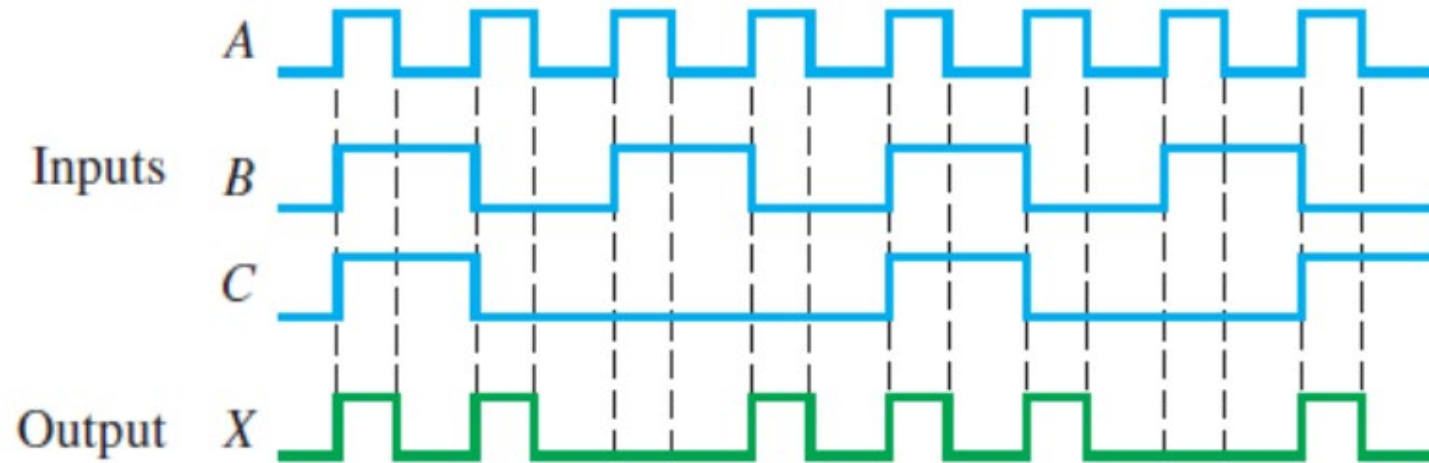
$$X = A + B + \bar{C}$$

$$\begin{aligned} X &= \overline{\overline{(A + B + \bar{C})}} \\ &= \overline{(A + B + \bar{C} + \bar{C})} + \overline{(A + B + \bar{C} + \bar{C})} \end{aligned}$$



Pulse Waveform Operation

Q6. For the input waveforms in the following figure, what logic circuit will generate the output waveform shown?



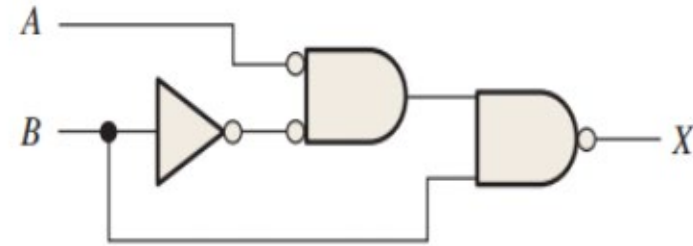
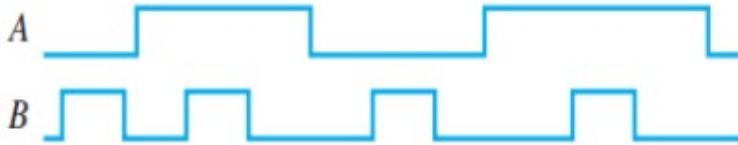
The logic circuit is:

$$X = A \cdot (BC + \bar{B}\bar{C} + \bar{B}C) = A \cdot (\bar{B} + C)$$

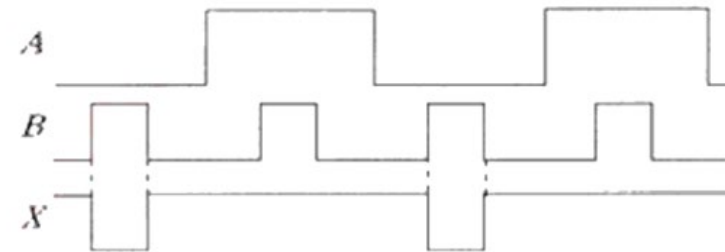


Pulse Waveform Operation

Q7. Write down the output waveform

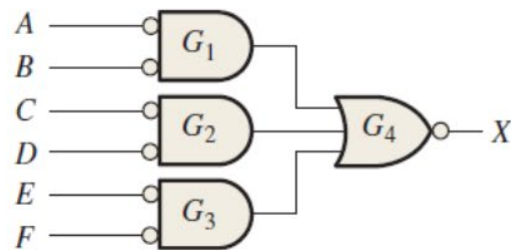


$$X = \overline{\overline{A+B}}B = A + \overline{B} + \overline{B} = A + \overline{B}$$

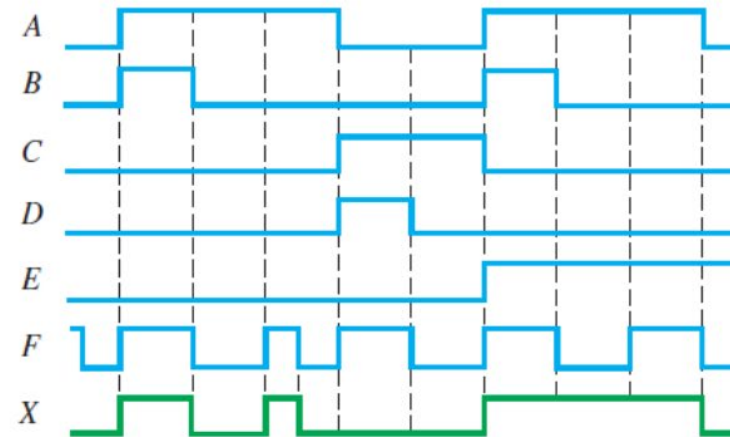


Basic Combinational Logic Analysis

Q8. Figure (a) is a logic circuit under test. Figure (b) shows the waveforms as observed on a logic analyzer. The output waveform is incorrect for the inputs that are applied to the circuit. Assuming that one gate in the circuit has failed, with its output either an apparent constant HIGH or a constant LOW. Determine the faulty gate and the type of failure.



(a)



(b)

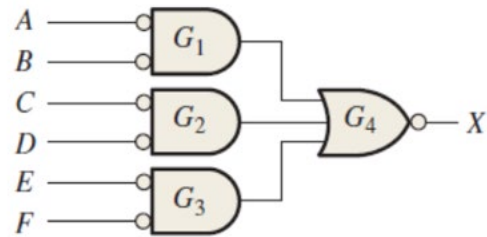
$$X = \overline{\overline{AB} + \overline{CD} + \overline{EF}} = (\overline{\overline{AB}})(\overline{\overline{CD}})(\overline{\overline{EF}}) = (A + B)(C + D)(E + F)$$

Since X does not go HIGH when C or D is HIGH, the output of gate G_2 must be *stuck LOW*.

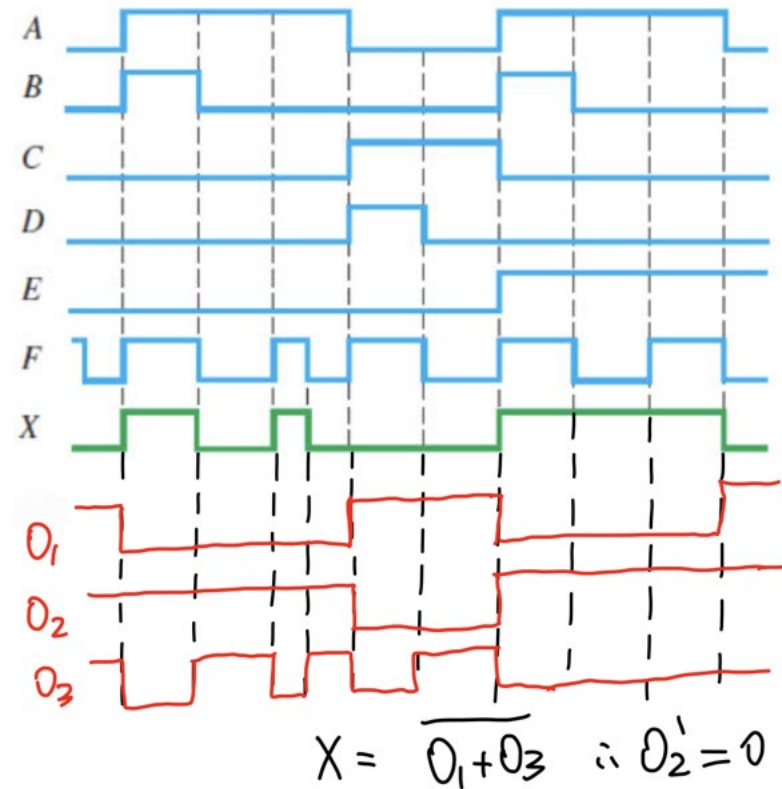


Basic Combinational Logic Analysis

Q8. For the input waveforms in the following figure, what logic circuit will generate the output waveform shown?



$$O_1 = \overline{A + B}, O_2 = \overline{C + D}, O_3 = \overline{E + F}, \\ X = \overline{O_1 + O_2 + O_3}$$

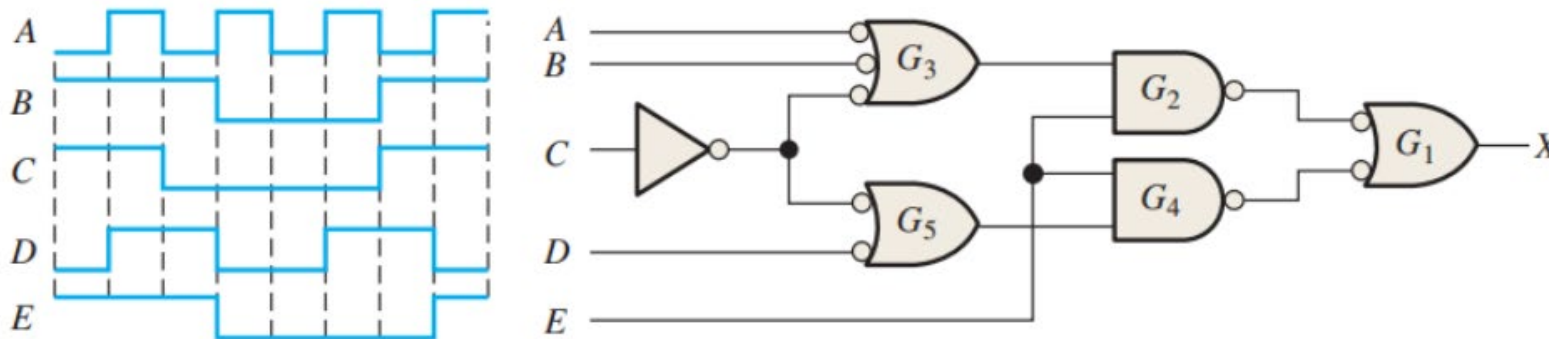


Basic Combinational Logic Analysis

Q9.

51. The logic circuit in Figure 5–73 has the input waveforms shown.

- (a) Determine the correct output waveform in relation to the inputs.
- (b) Determine the output waveform if the output of gate G_3 is open.
- (c) Determine the output waveform if the upper input to gate G_5 is shorted to ground.



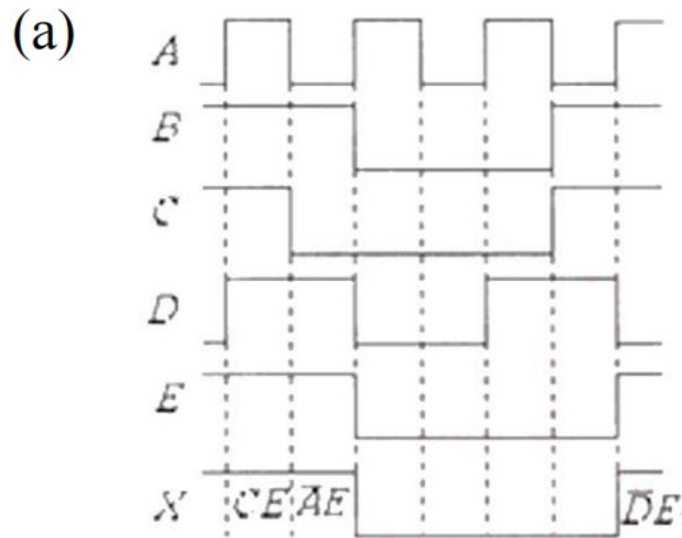
$$G3: \bar{A} + \bar{B} + C \quad G5: C + \bar{D} \quad G2: \overline{(\bar{A} + \bar{B} + C)E} \quad G4: \overline{(C + \bar{D})E}$$

$$\begin{aligned} X &= (\bar{A} + \bar{B} + C)E + (C + \bar{D})E = \bar{A}E + \bar{B}E + CE + \bar{D}E \\ &= \bar{A}E + \bar{B}E + CE + \bar{D}E \end{aligned}$$



Basic Combinational Logic Analysis

Q9.



(b) $X = E + E(\bar{D} + C) = E(1 + \bar{D} + C) = E$

Waveform x is the same as waveform E, in Figure.

Since this is the correct waveform, the open output of gate G3 does not show up for this particular set of input waveforms.

(c) $X = E + E(\bar{A} + \bar{B} + C) = E(1 + \bar{A} + \bar{B} + C) = E$

Again waveform x is the same as waveform E. As strange as it may seem, the shorted input to G5 does not affect the output for this particular set of input waveforms.

Conclusion: the two faults are not indicated in the output waveform for these particular inputs.





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Thank
You!