香港中文大學（深圳）
The Chinese University of Hong Kong, Shenzhen

ECE2050 Digital Logic and Systems

Tutorial 7: Sequential Logic Design

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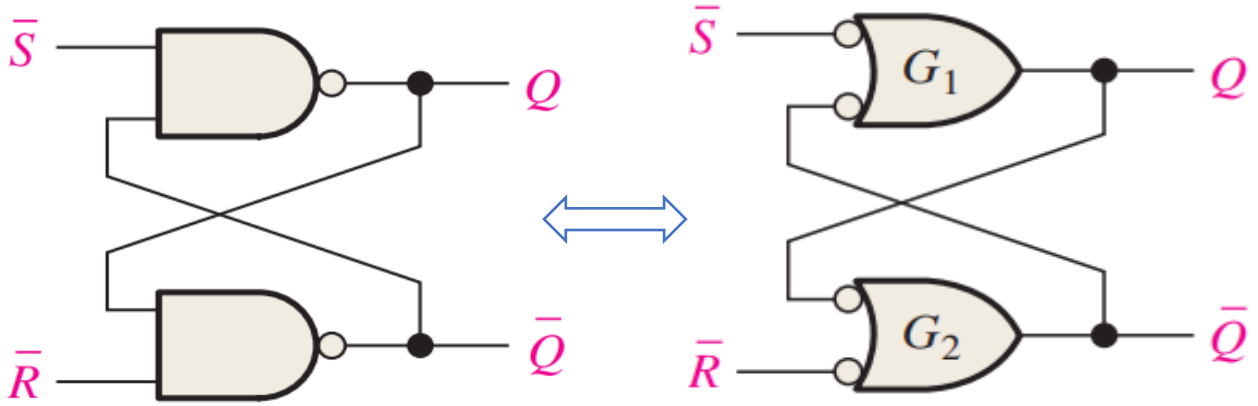
Office Hour: 11:00-12:00 Tuesday, Zhixin 107

Review: S-R Latch

- Bistable Storage device (SET & RESET)
  - ✓ **S-R Latch**
    - ➢ Two cross-coupled NAND (NOR) gates



Active-LOW input $\overline{S}$-$\overline{R}$ latch

- ➢ Truth Table

TABLE 7–1

Truth table for an active-LOW input $\overline{S}$-$\overline{R}$ latch.

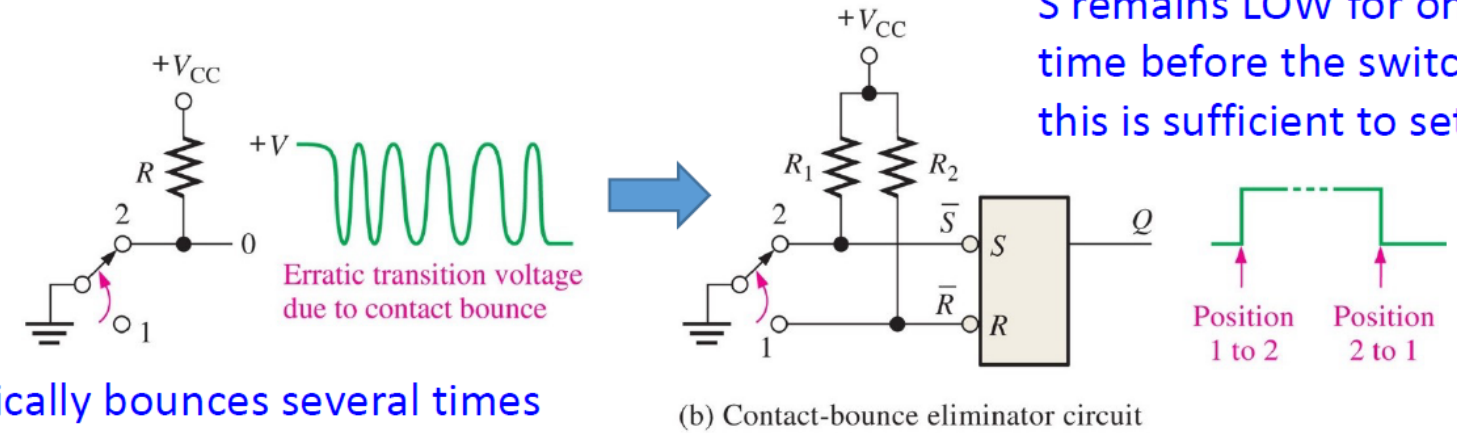
Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

Q is HIGH, the latch is in the SET state

Q is LOW, the latch is in the RESET state

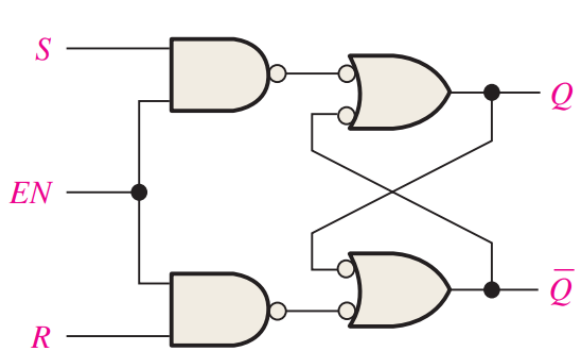
Review: S-R Latch

- Bistable Storage device (SET & RESET)
  - ✓ **S-R Latch (Application)**
    - ➢ Latch as a Contact-Bounce Eliminator

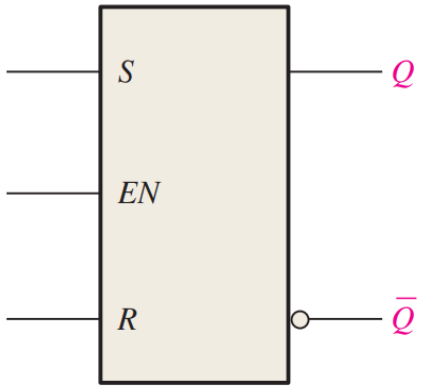


Review: The Gated S-R Latch

- Bistable Storage device (SET & RESET)
  - ✓ **The Gated S-R Latch**
    - ➢ S-R latch + EN (input)



(a) Logic diagram

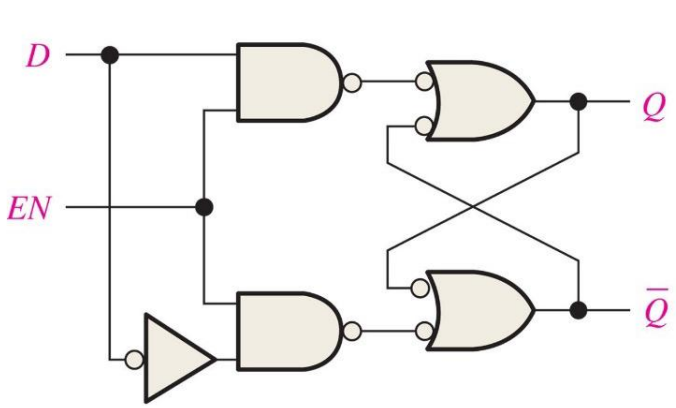


(b) Logic symbol

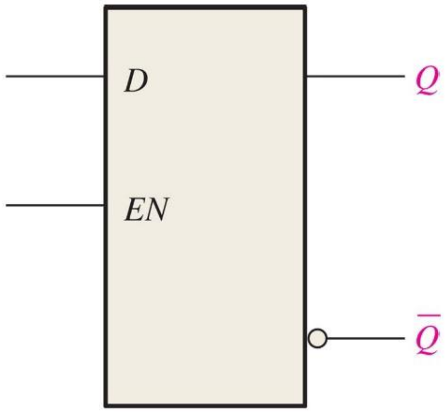
- ➢ Input-Output Relationship
  - When enabled, the NAND gates outputs are $\overline{S}$ and $\overline{R}$, respectively.
  - The output is similar to S-R latches

Review: The Gated D Latch

- Bistable Storage device (SET & RESET)
  - ✓ **The Gated D Latch**
    - ➢ D (Input) + EN (Input)



(a) Logic diagram

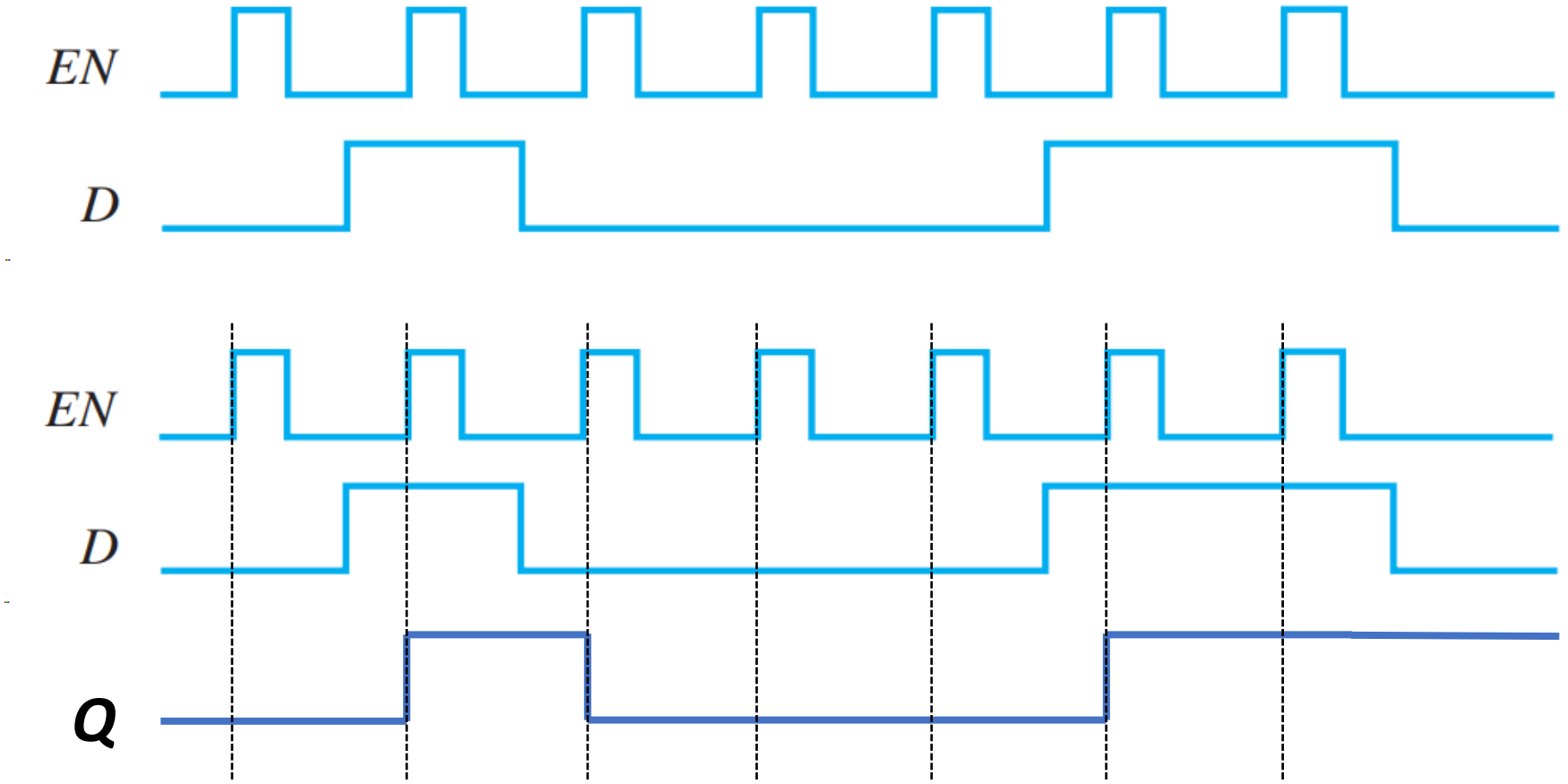


(b) Logic symbol

- ➢ Input-Output Relationship
  - When D and EN are HIGH, *Q* is HIGH
  - When D is LOW and EN is HIGH, *Q* is LOW

Question 1

- Q1: Determine the output of a gated D latch for the inputs in the figure below.



Review: Flip-Flops

- Synchronous Bistable Devices
  - ✓ Output changes state at a leading or trailing edge on the triggering input called **CLK**
  - ✓ Two types of edge-triggered flip-flops
    - ➢ The D Flip-Flop
    - ➢ The J-K Flip-Flop

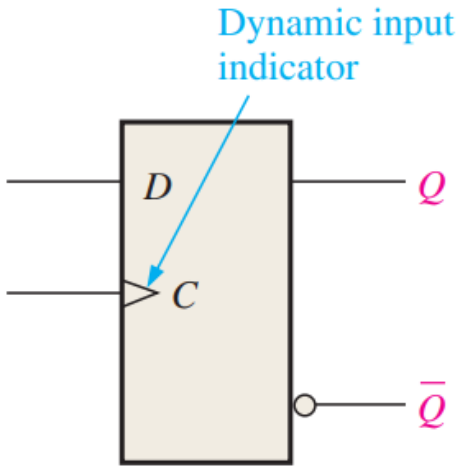


TABLE 7–2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	*Q*	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

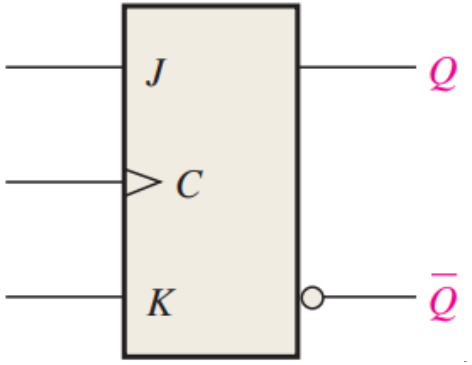


TABLE 7–3

Truth table for a positive edge-triggered J-K flip-flop.

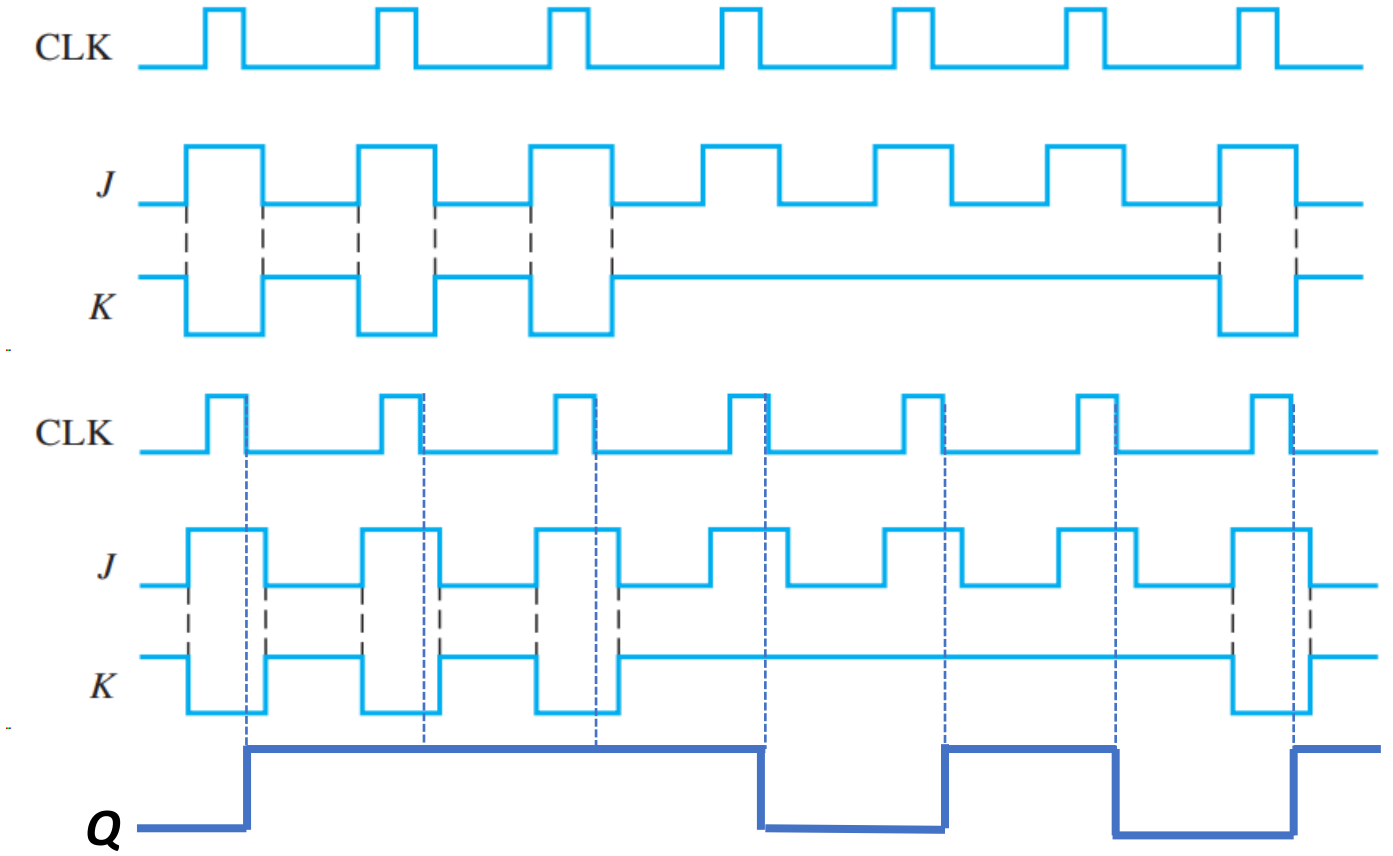
Inputs			Outputs		
J	*K*	CLK	*Q*	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

Question 2

- For a negative edge-triggered J-K flip-flop with the inputs in Figure below, develop the Q output waveform relative to the clock. Assume that Q is initially LOW.



Question 4

- What is the difference between a latch and a flip flop?

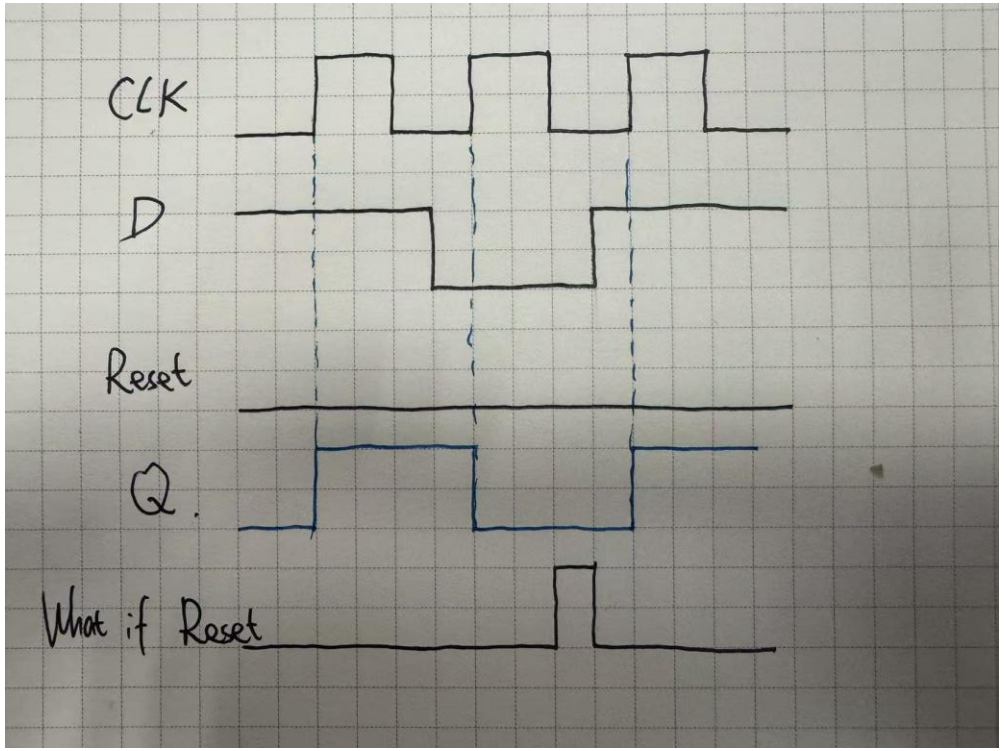
  - Latch is a **level-sensitive** device (outputs can change as soon as the inputs changes), No CLK.
  - Flip-Flop is an **edge-sensitive** device (only changes state when a CLK signal goes from high to low or low to high).
  - Latch cannot filter **glitches** (when the enable signal is valid, the output state may change multiple times with the input). This is extremely dangerous to the next-level circuit, so the flip-flop can be used

- What are the applications of flip flop?

  - Counters
  - Frequency dividers
  - …

Question 5

- For a positive edge-triggered D Flip-Flop with the inputs in Figure below, develop the Q output waveform relative to the clock. Assume that Q is initially LOW.



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Thank You!