

ECE2050 Digital Logic and Systems

Tutorial 10

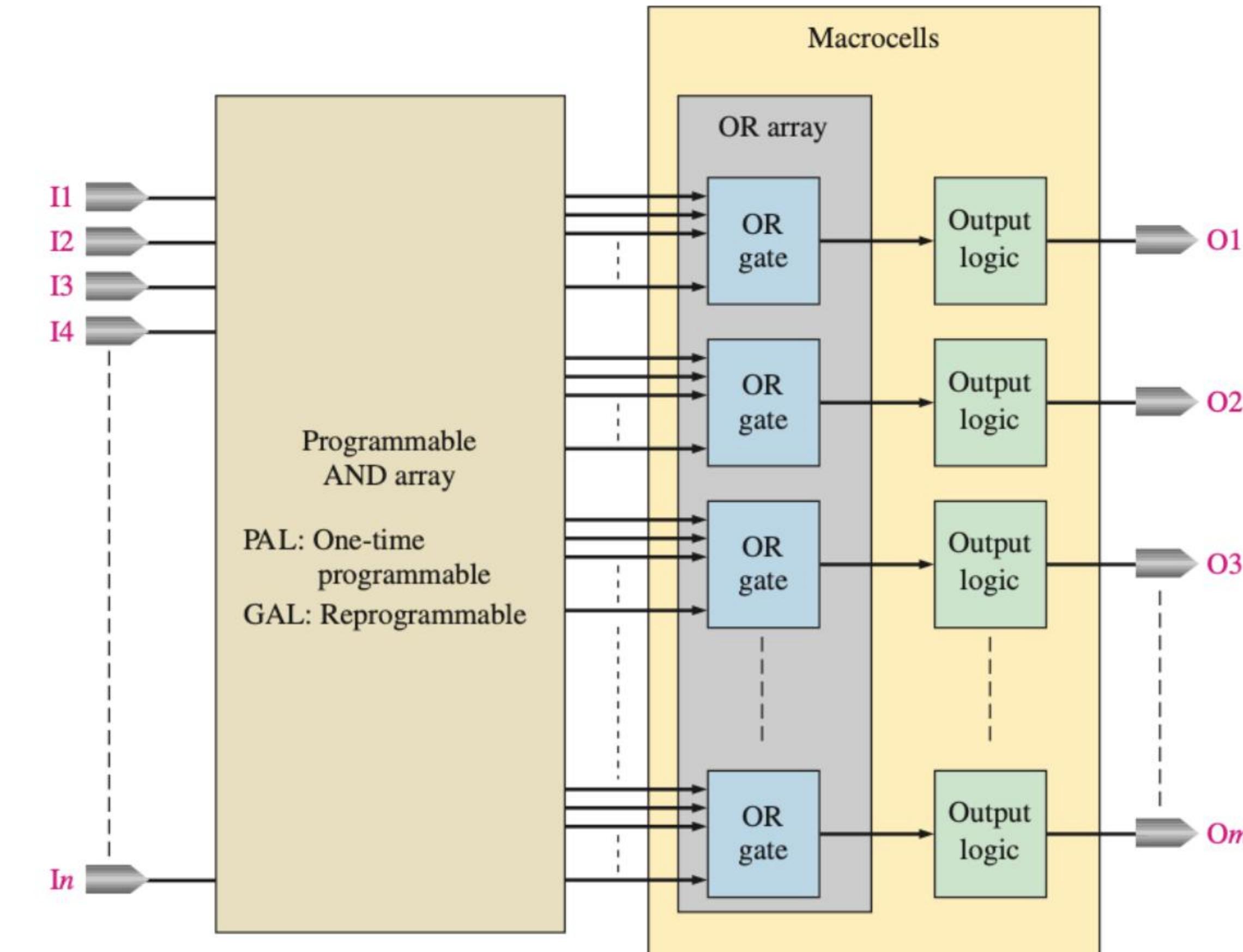
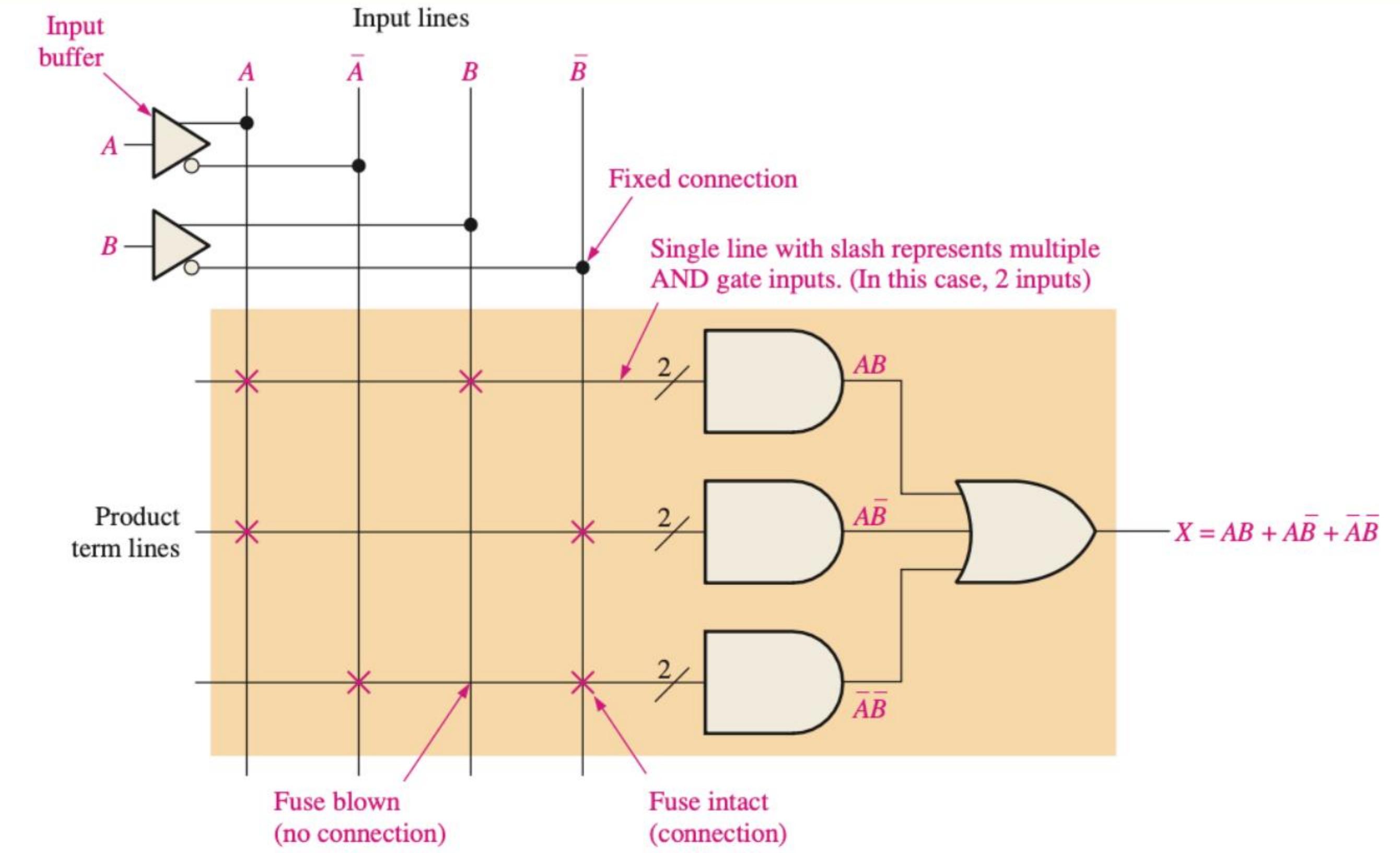
Zhang Hanxu

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Office Hour: Thu 20:00-21:00 ZX201

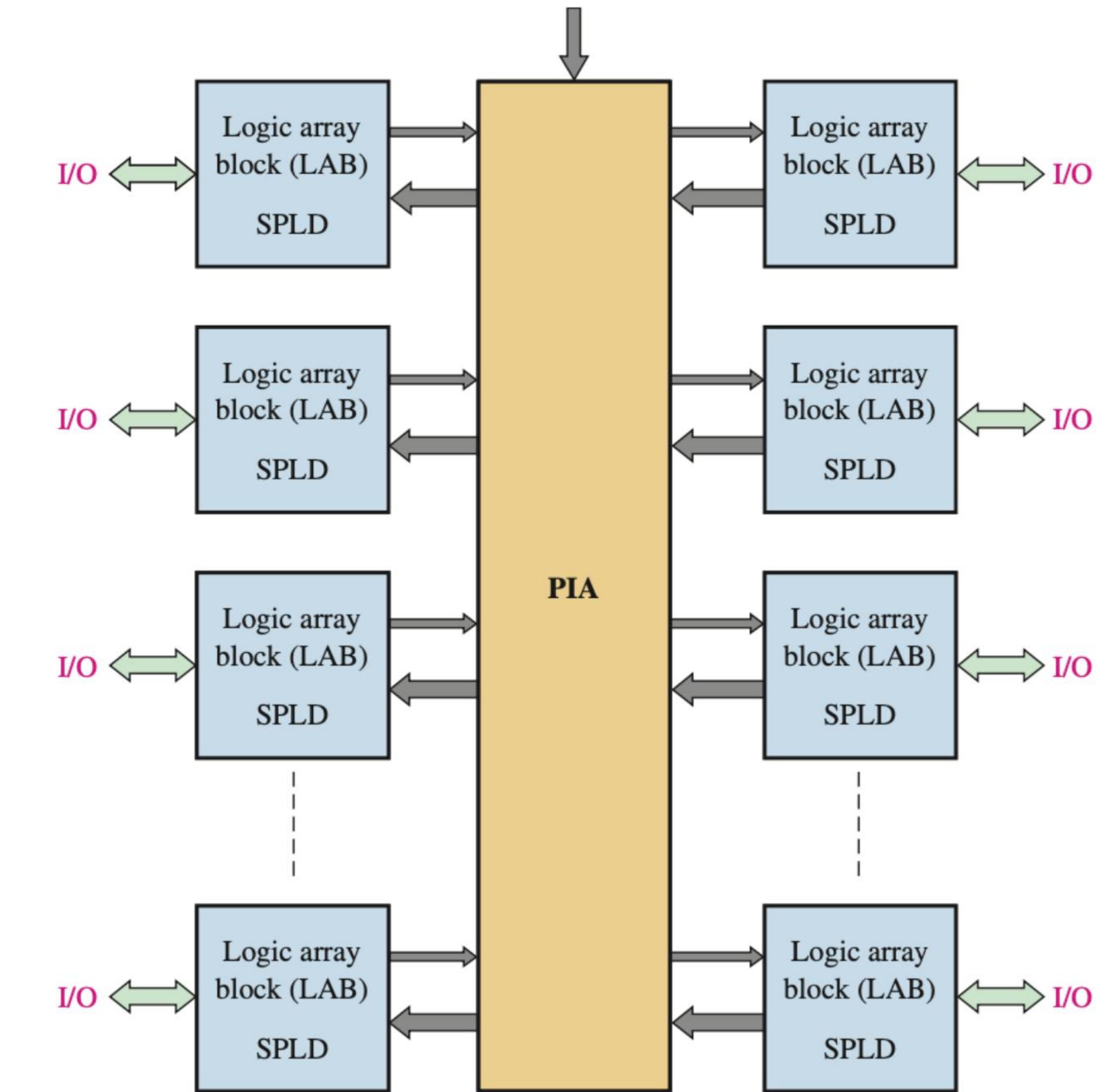
Review: Simple Programmable Logic Devices

- The PAL (Programmable Array Logic)
 - Implemented with fuse process technology
 - One time programmable
- The GAL (Generic Array Logic)
 - Uses a reprogrammable process technology, i.e. EEPROM, instead of fuses.
- Simplified Notation for PAL/GAL Diagrams
- PAL/GAL General Block Diagram
 - Macrocells: Configured for combinational logic, registered logic, or a combination of both



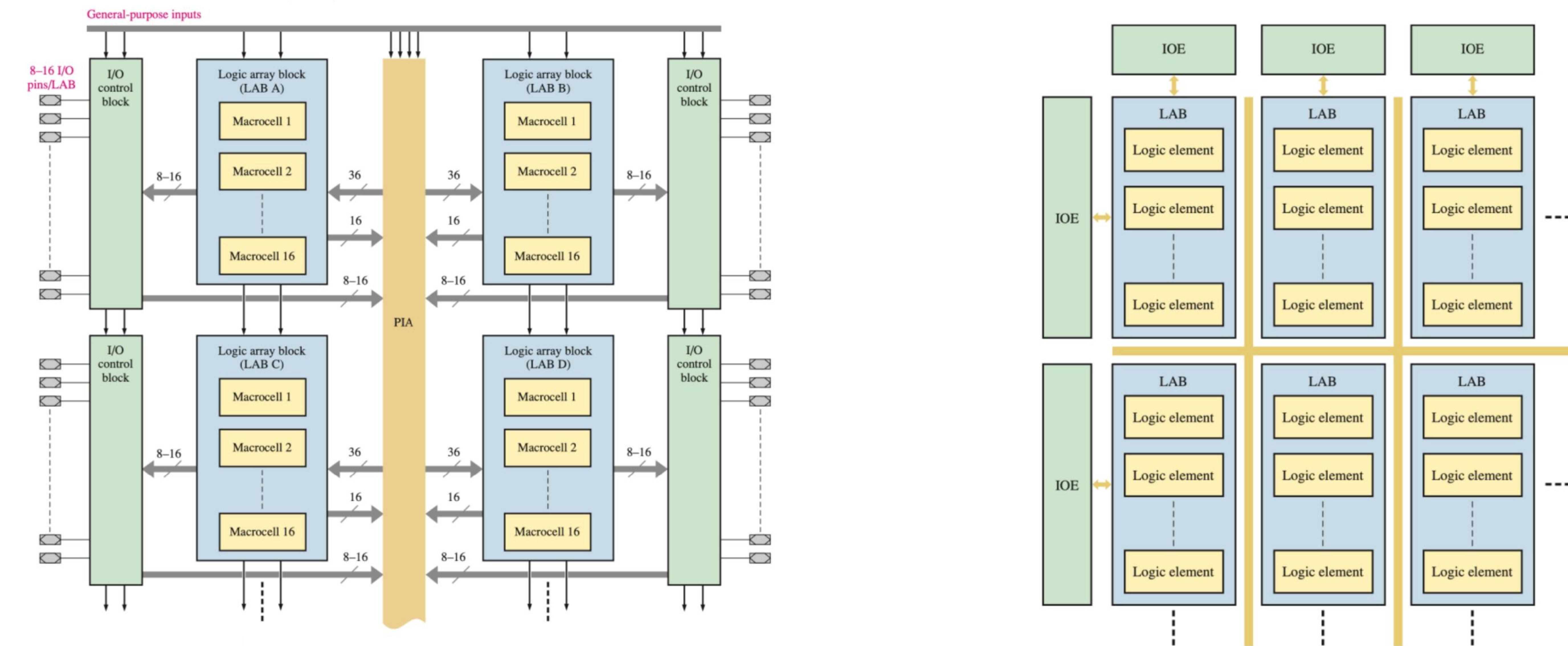
Review: Complex Programmable Logic Devices

- CPLDs
 - Composed of multiple SPLD arrays with programmable interconnections called PIA (Programmable Interconnect Array)
 - Each SPLD array in a CPLD is referred to as a LAB (Logic Array Block).



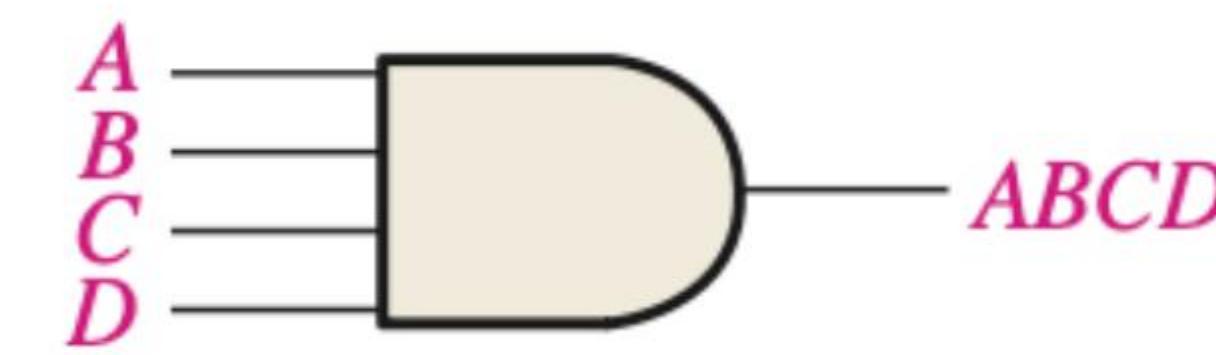
Review: Complex Programmable Logic Devices

- Classic V.S. LUT CPLD architectures
 - One main difference: the way in which a logic function is developed (Look-up tables (LUTs) are used instead of AND/OR arrays.)

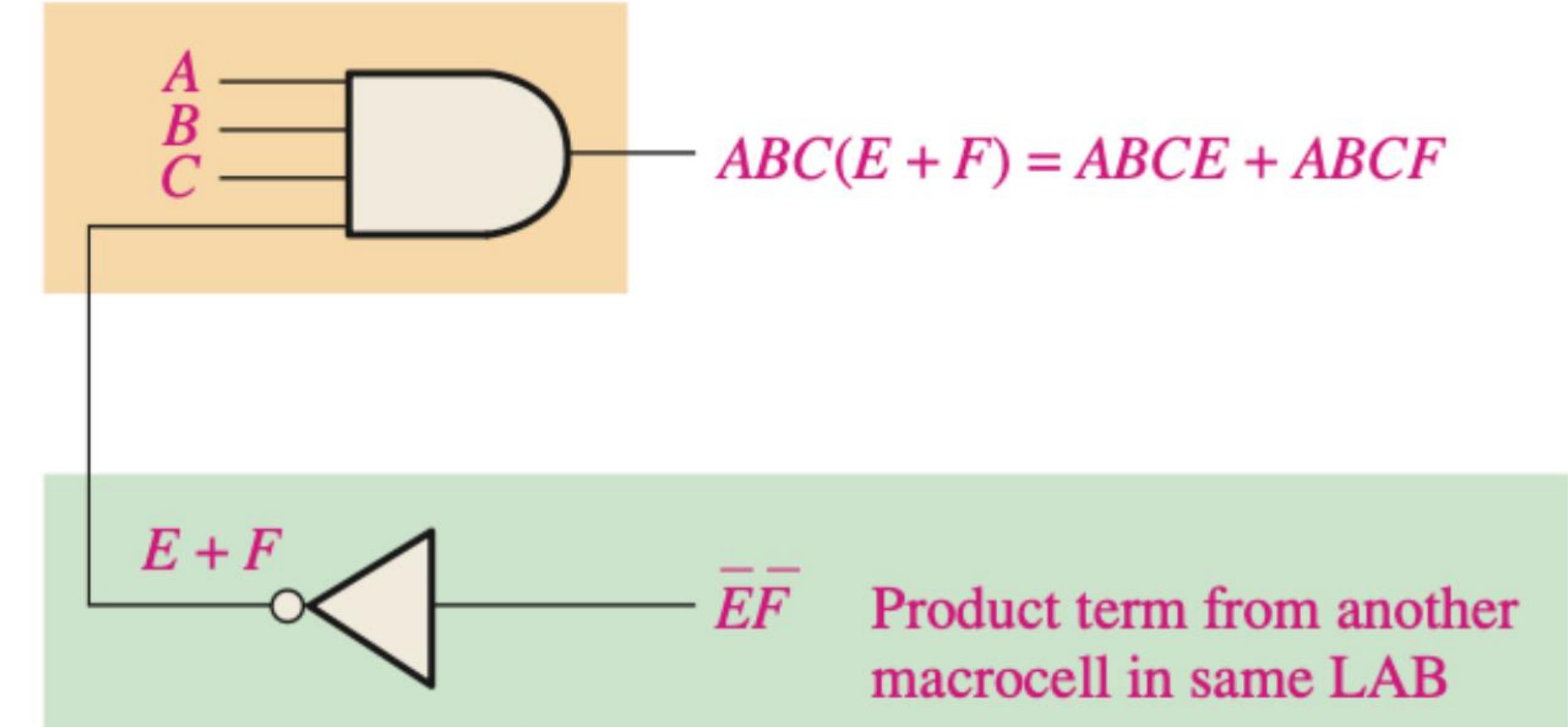


Review: Shared Expander

- Shared Expander
 - Increase the number of product terms in an SOP expression by a complemented product term



(a) A 4-input AND array gate can produce one 4-variable product term.

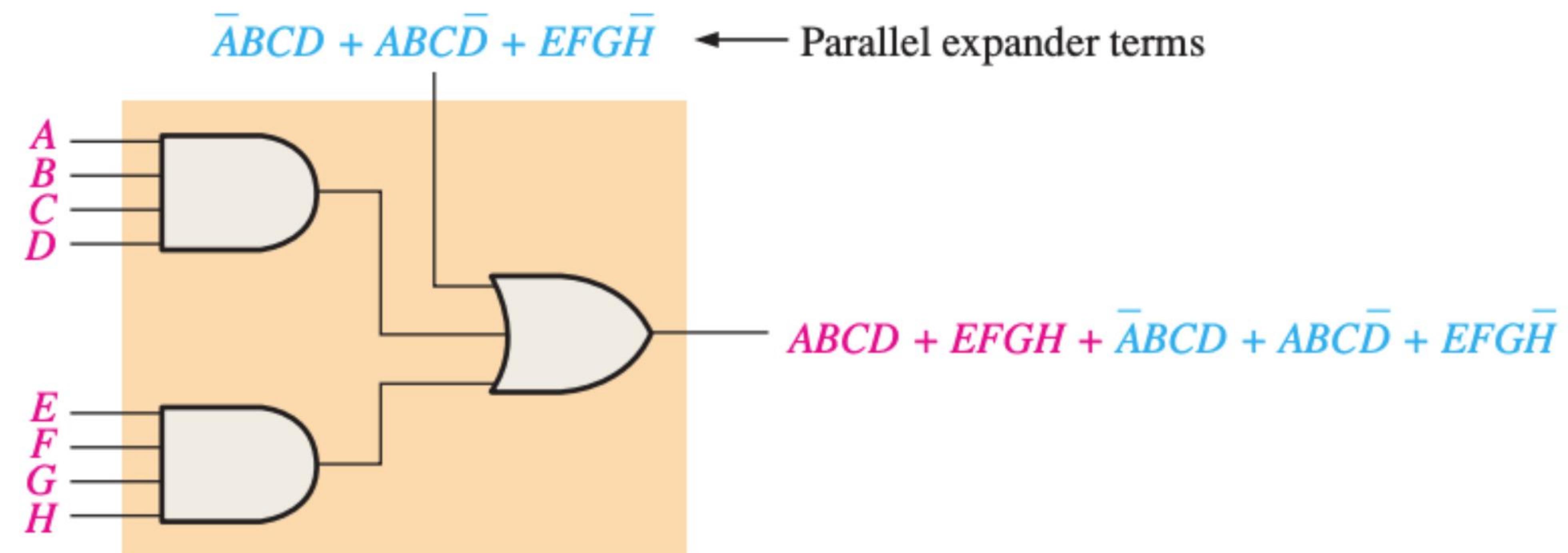


(b) AND gate is expanded to produce two product terms.



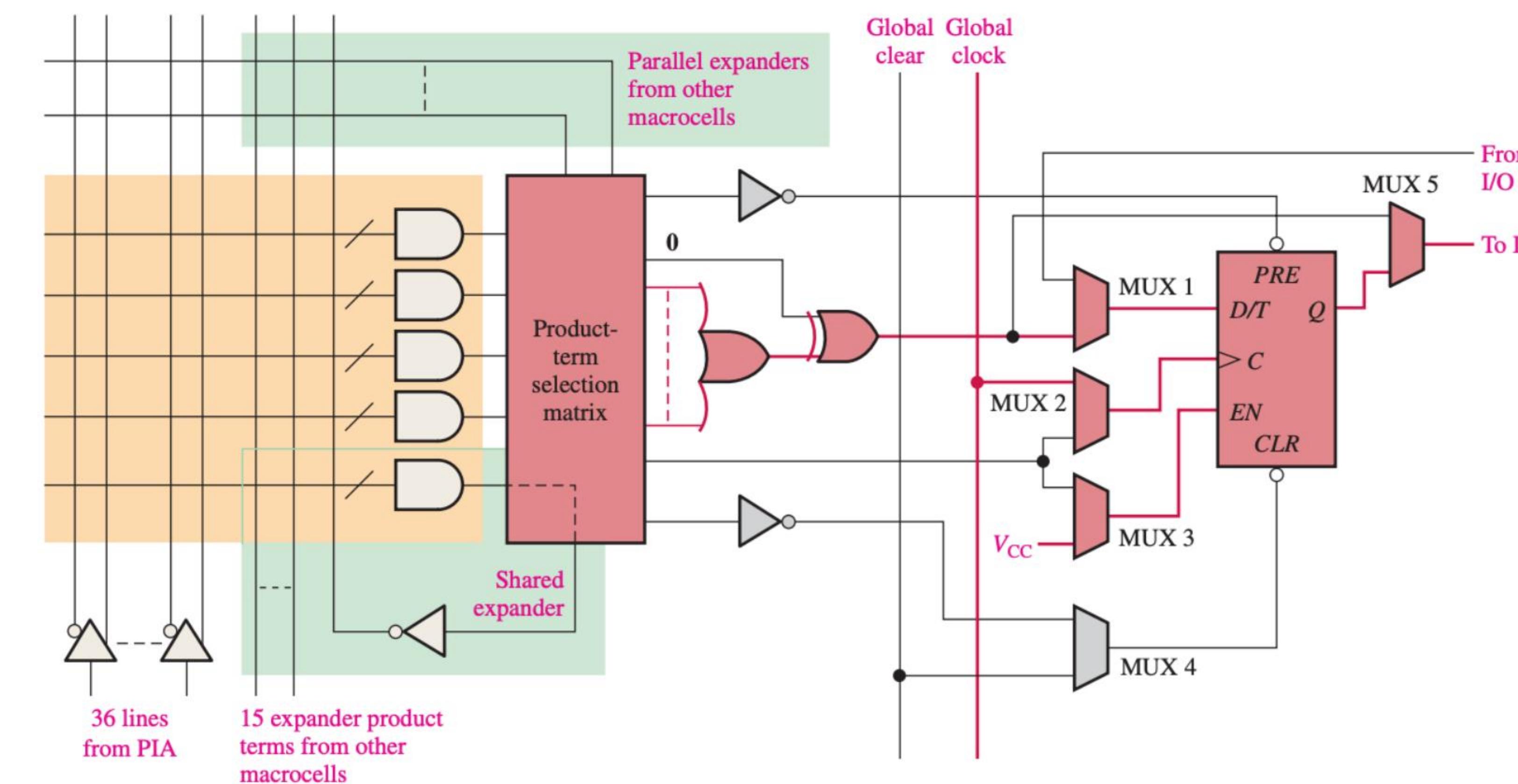
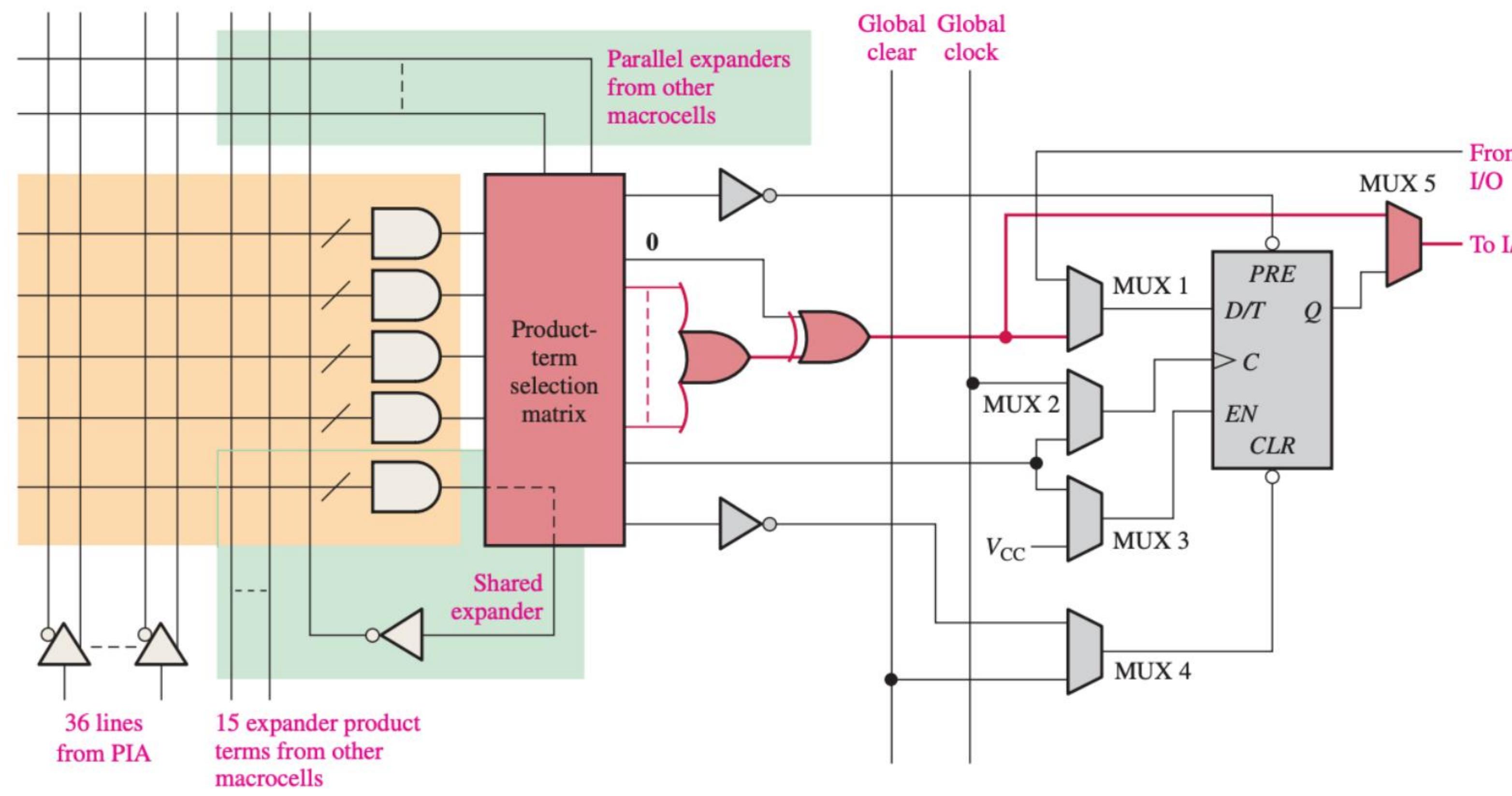
Review: Parallel Expander

- Parallel Expander
 - Another way to increase the number of product terms by OR with the additional product terms



Review: Macrocell Modes

- Macrocell Modes
 - Combinational mode and Registered mode
 - Determine whether directly output the SOP or input the SOP to register and output the result of it



Question

- A PAL is a logic device which is
 - (a) a one-time programmable
 - (b) an erasable programmable
 - (c) electronically erasable and programmable
 - (d) both (a) and (b)
- The term LAB stands for
 - (a) logic AND block
 - (b) logic array block
 - (c) last asserted bit
 - (d) logic assembly block
- Two modes of macrocell operation are
 - (a) input and output
 - (b) registered and sequential
 - (c) combinational and registered
 - (d) parallel and shared



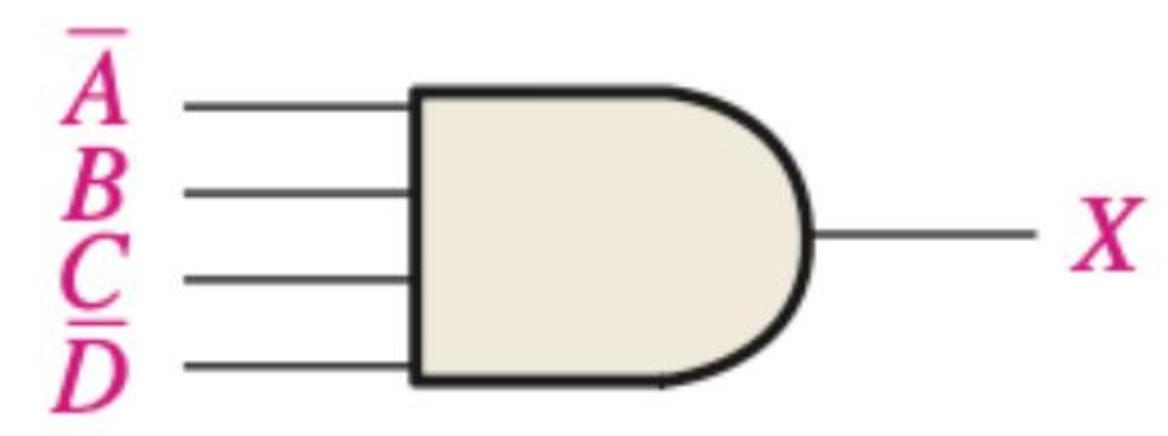
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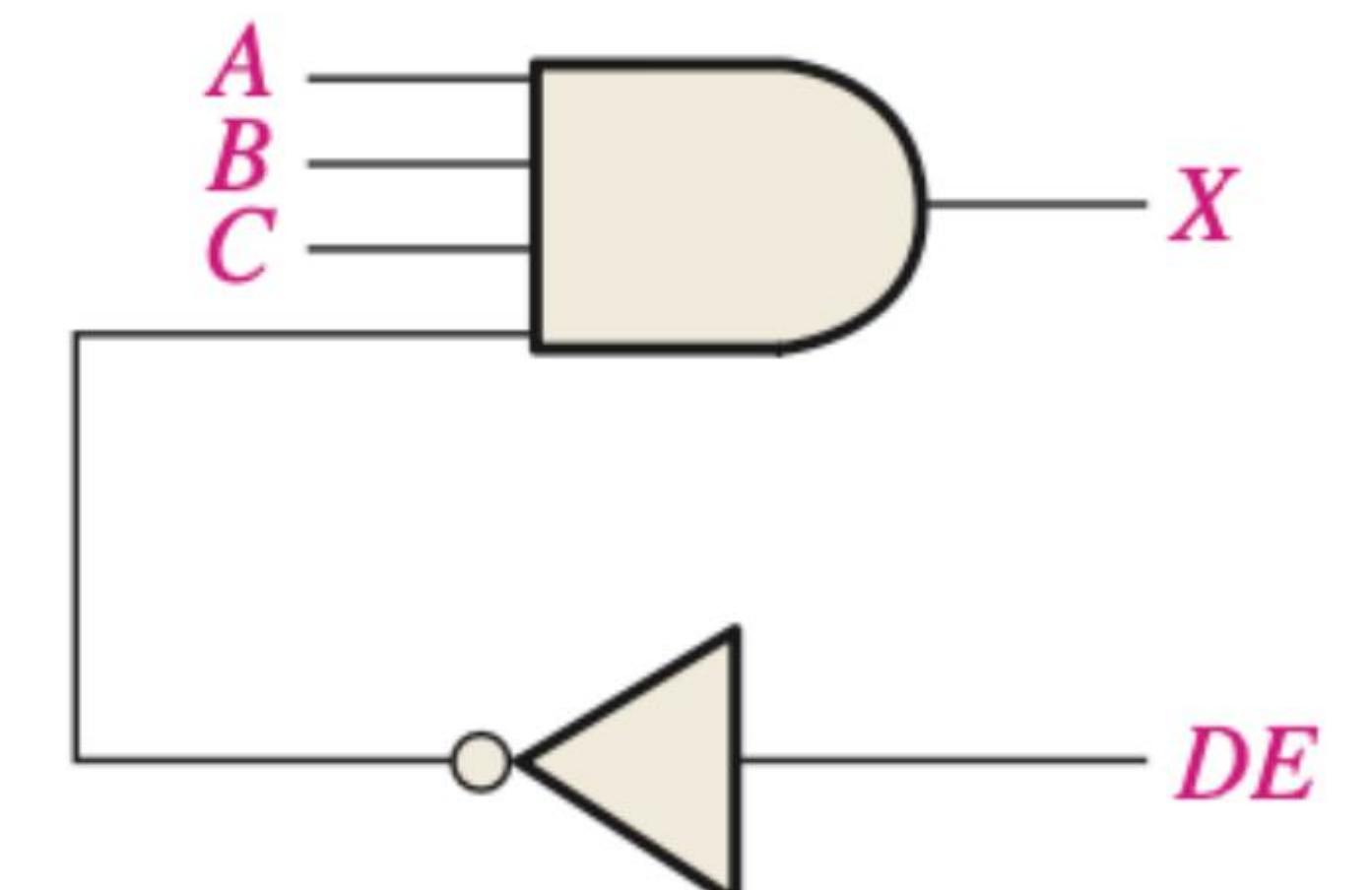


Question

Determine the product term for the AND gate in a CPLD array shown in Figure 10–65(a).
If the AND gate is expanded, as shown in Figure 10–65(b), determine the SOP output.



(a)

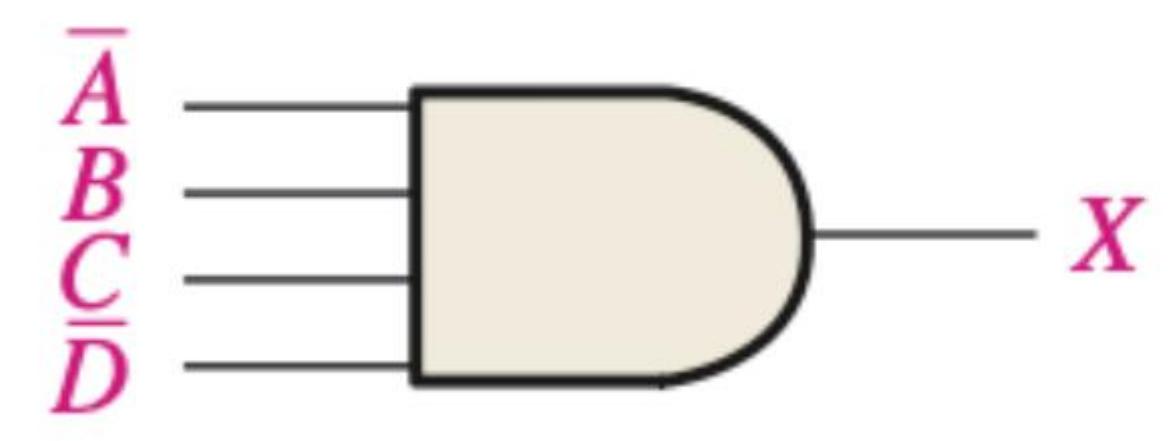


(b)

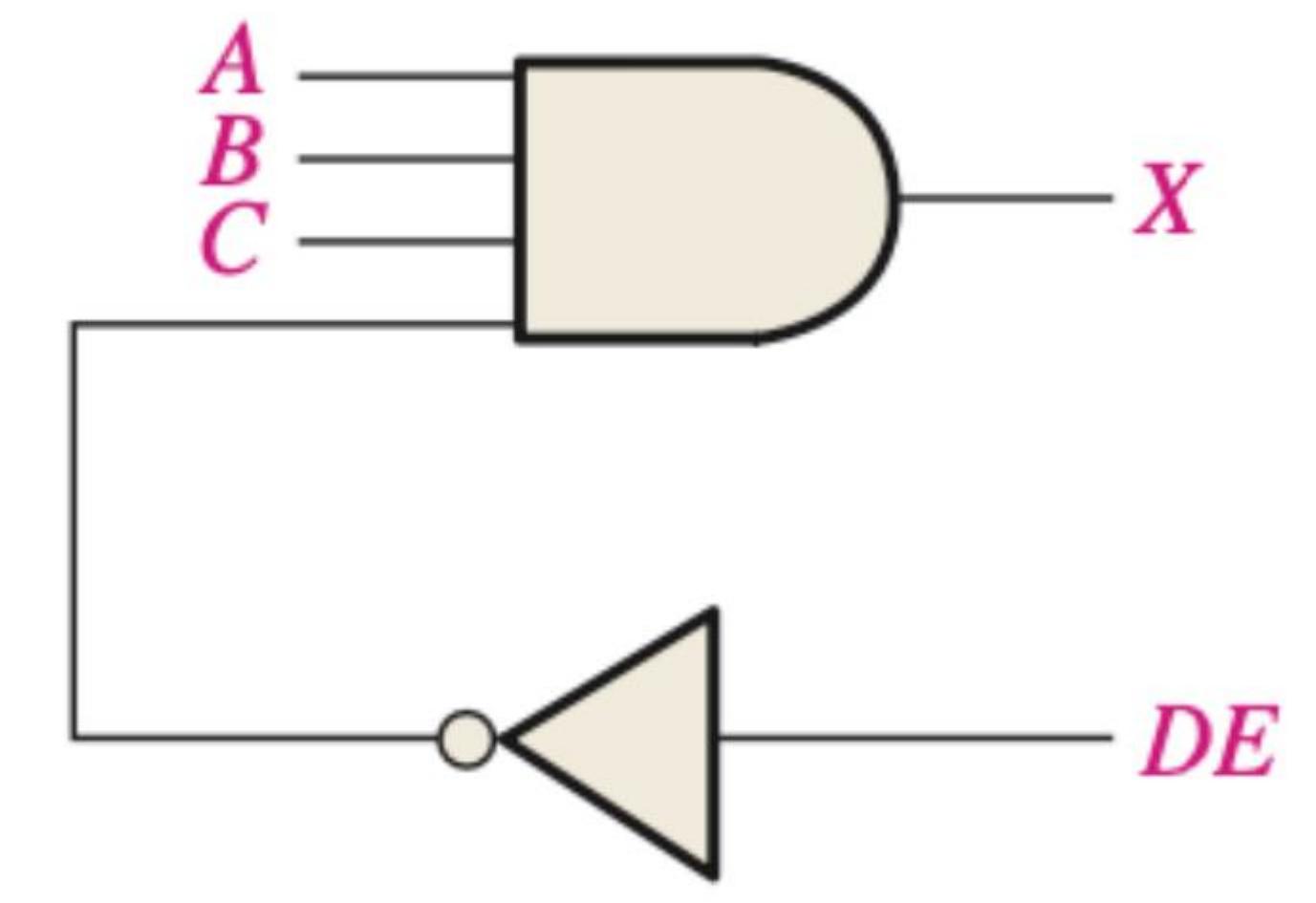


Question

Determine the product term for the AND gate in a CPLD array shown in Figure 10–65(a).
If the AND gate is expanded, as shown in Figure 10–65(b), determine the SOP output.



(a)



(b)

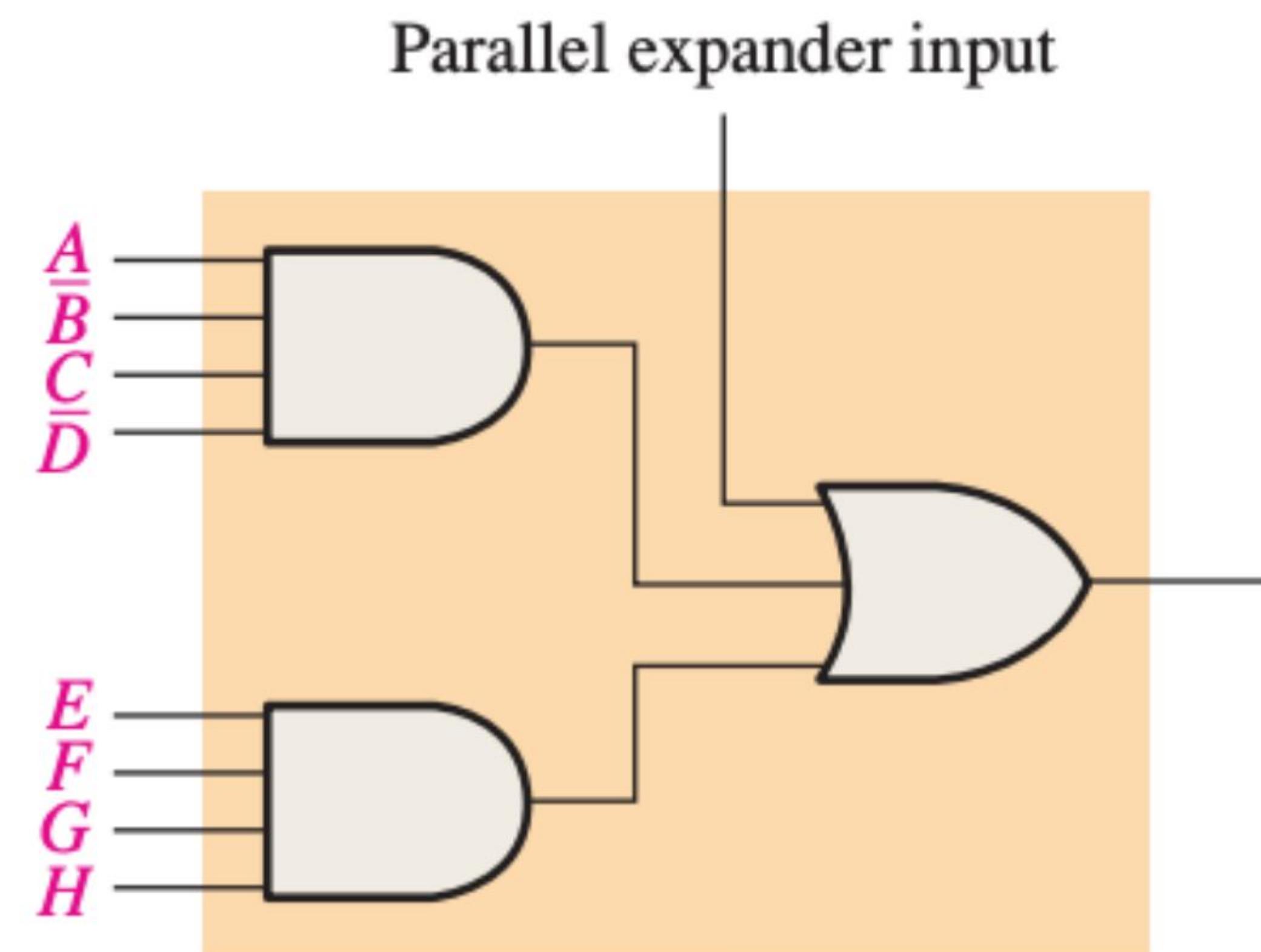
(a) $SOP = \bar{A}BC\bar{D}$

(b) $SOP = ABC\bar{D} + ABC\bar{E}$



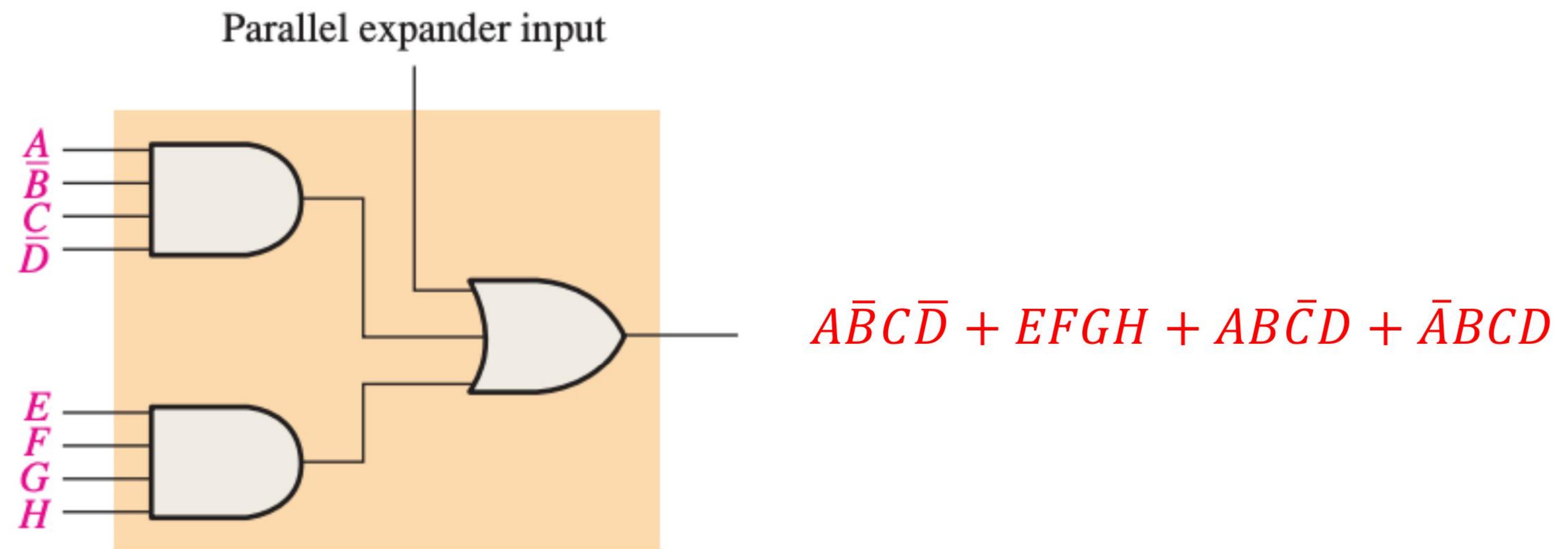
Question

Determine the output of the macrocell logic in Figure 10–66 if $AB\bar{C}D + \bar{A}B\bar{C}D$ is applied to the parallel expander input.

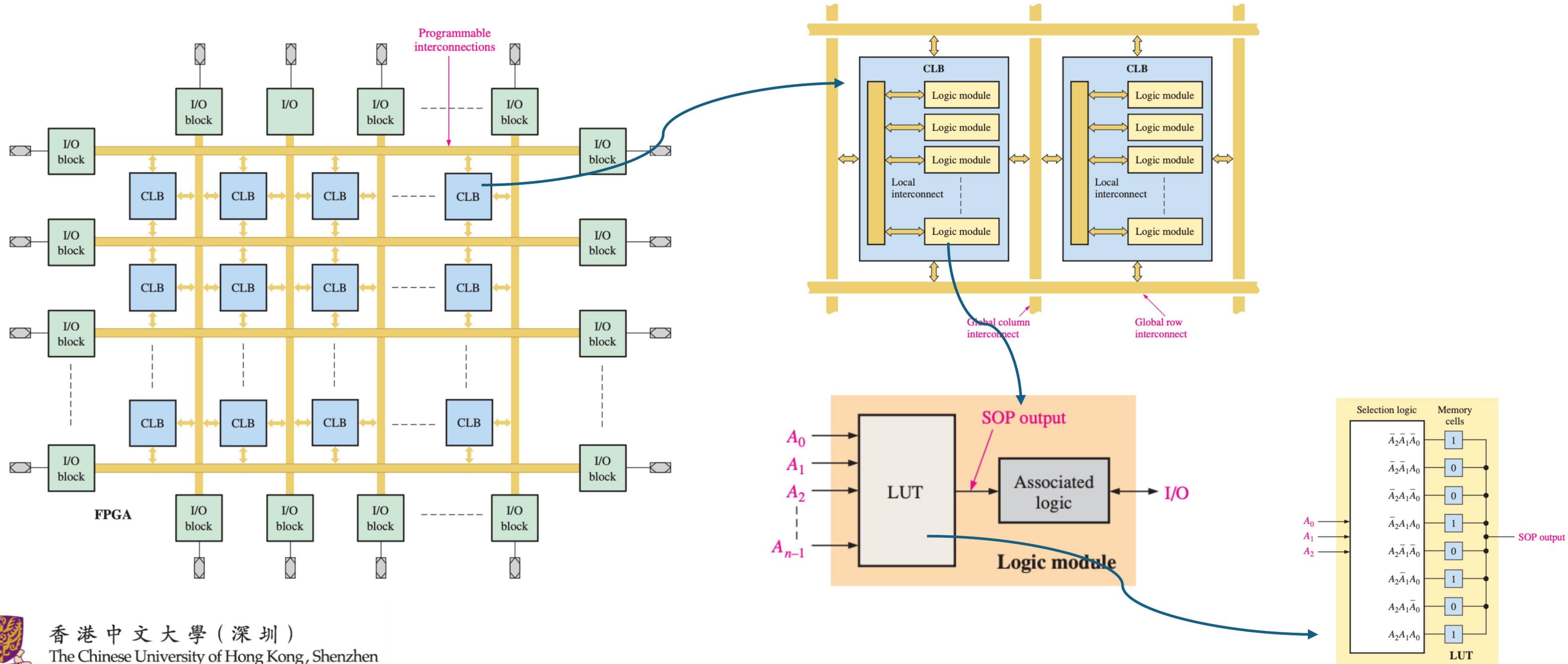


Question

Determine the output of the macrocell logic in Figure 10–66 if $A\bar{B}CD + \bar{A}BCD$ is applied to the parallel expander input.



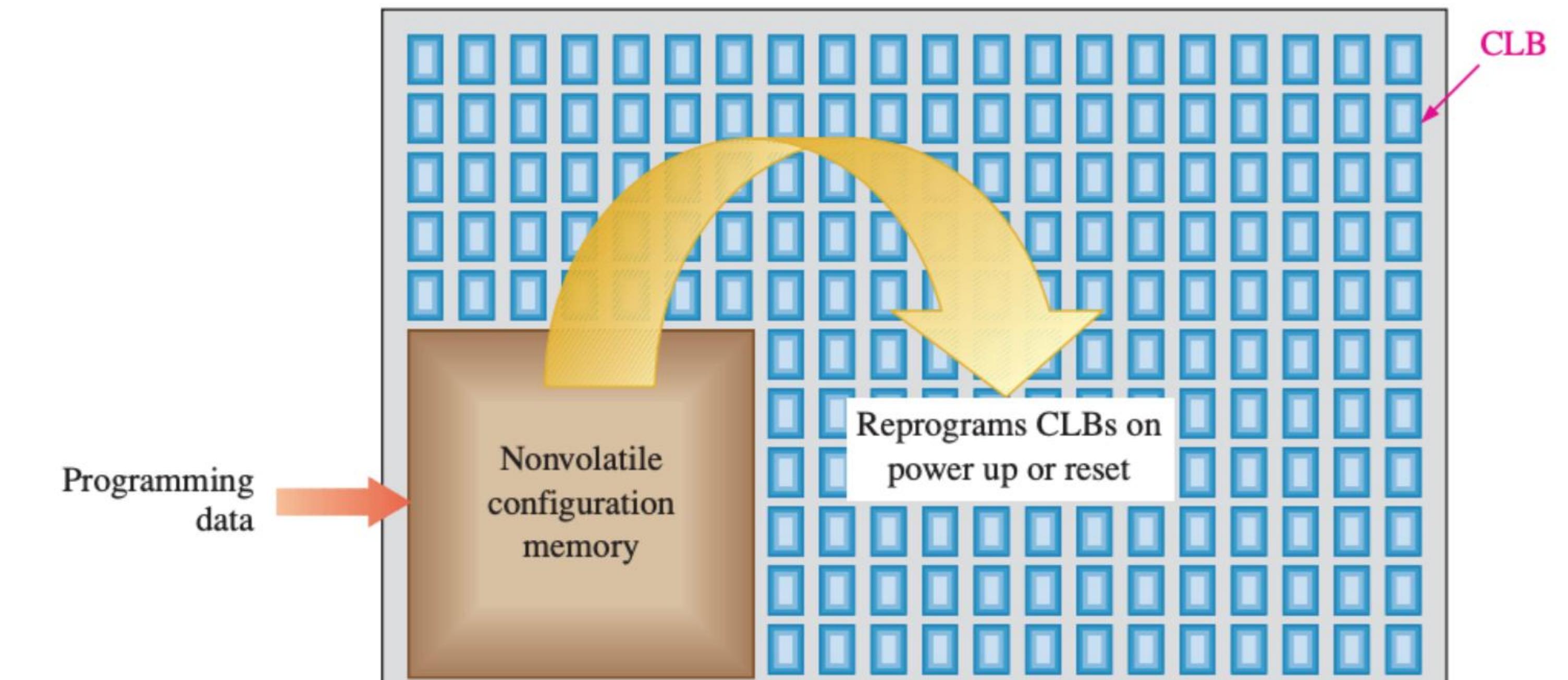
Review: Field-Programmable Gate Arrays (FPGAs)



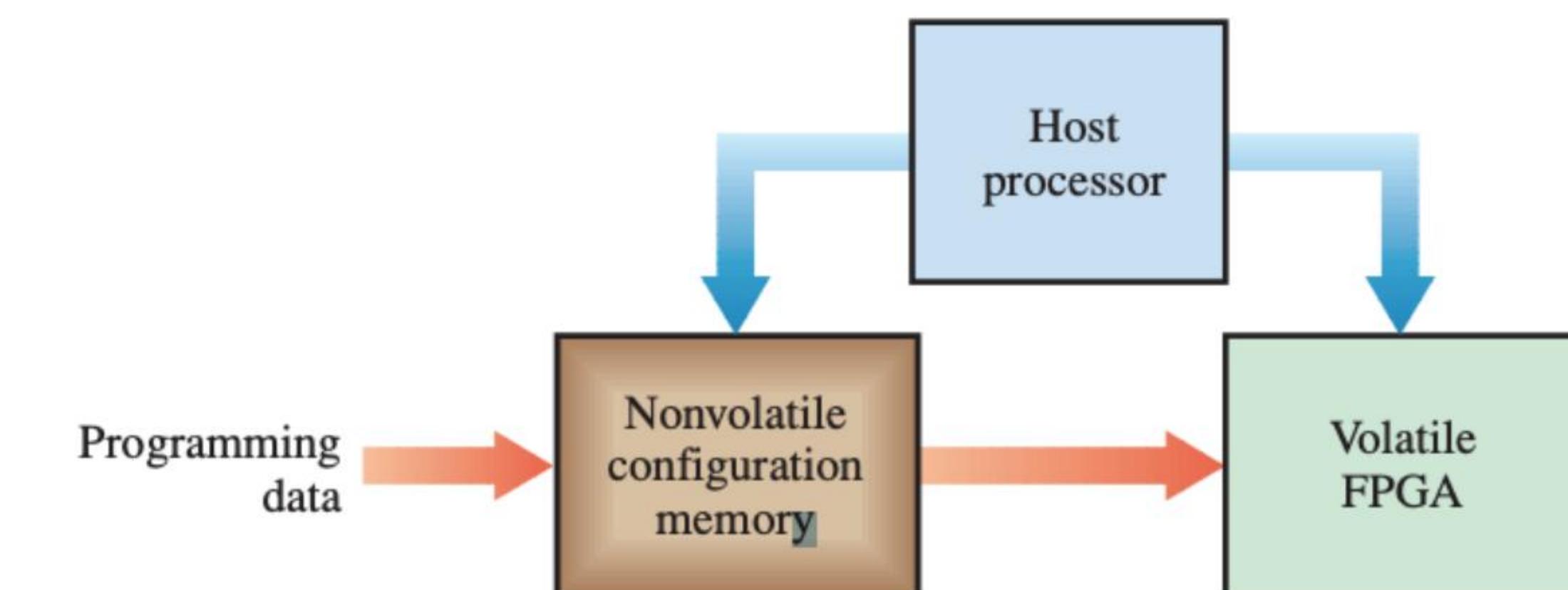
Review: Field-Programmable Gate Arrays (FPGAs)

- SRAM-Based FPGAs

- Are volatile, because all the data store on the SRAM is lost once the power is turned off
- Include on-the-chip nonvolatile configuration memory or an external memory with data transfer controlled by a host processor.



(a) Volatile FPGA with on-the-chip nonvolatile configuration memory



(b) Volatile FPGA with on-board memory and host processor



Review: Field-Programmable Gate Arrays (FPGAs)

- FPGA Cores
 - Hard core
 - Put in by manufacturer
 - Provides commonly used functions for users
 - Can not be programmed



Review: Programmable Logic Software

- Design flow
 1. Design entry
 2. Functional simulation
 3. Synthesis
 4. Implementation (Software)
 5. Timing simulation
 6. Device programming (Downloading)



Question

- The basic elements of an FPGA are
 - (a) configurable logic blocks
 - (b) I/O blocks
 - (c) PAL arrays
 - (d) both (a) and (b)
- Nonvolatile FPGAs are generally based on
 - (a) fuse technology
 - (b) antifuse technology
 - (c) EEPROM technology
 - (d) SRAM technology



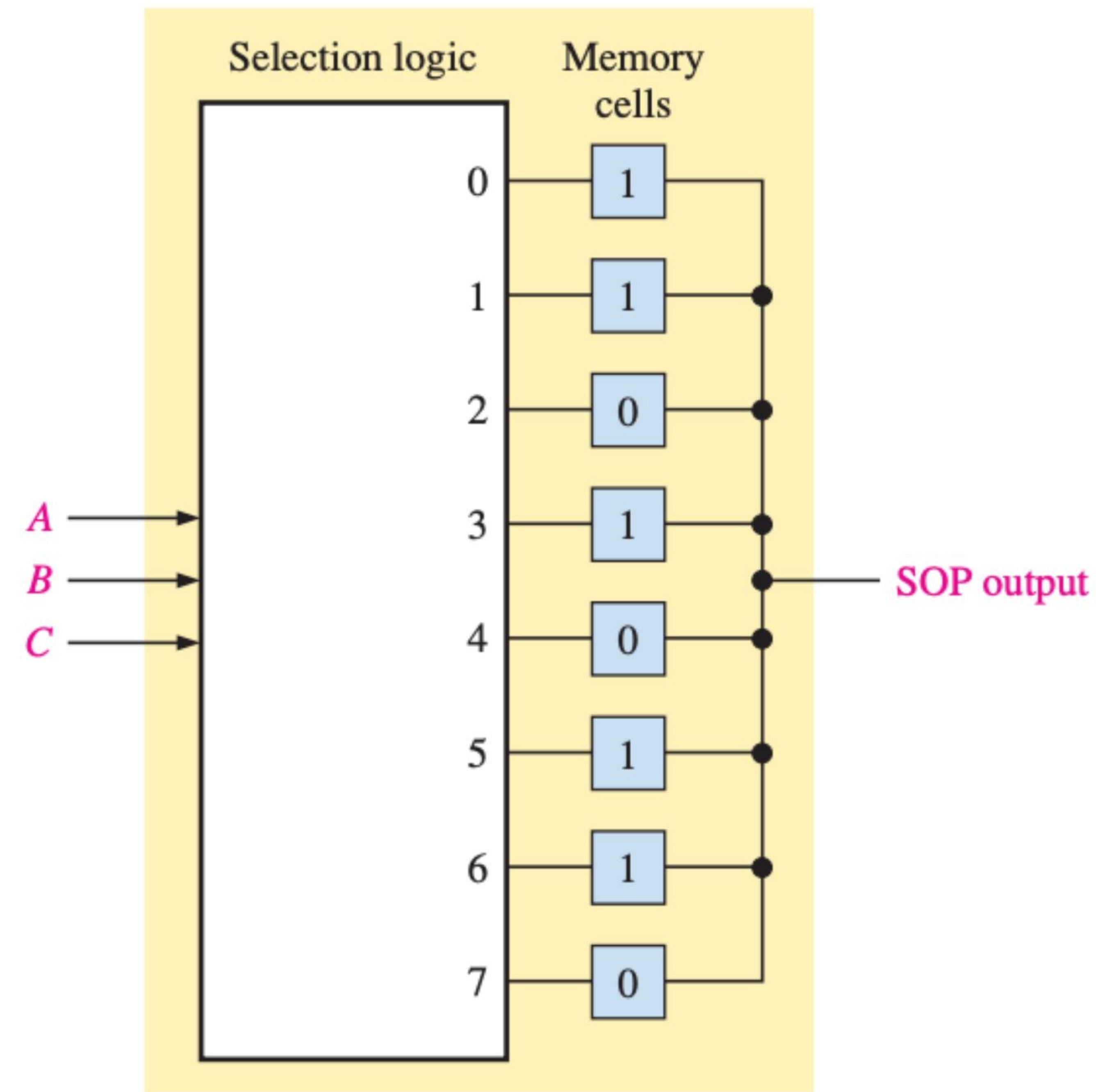
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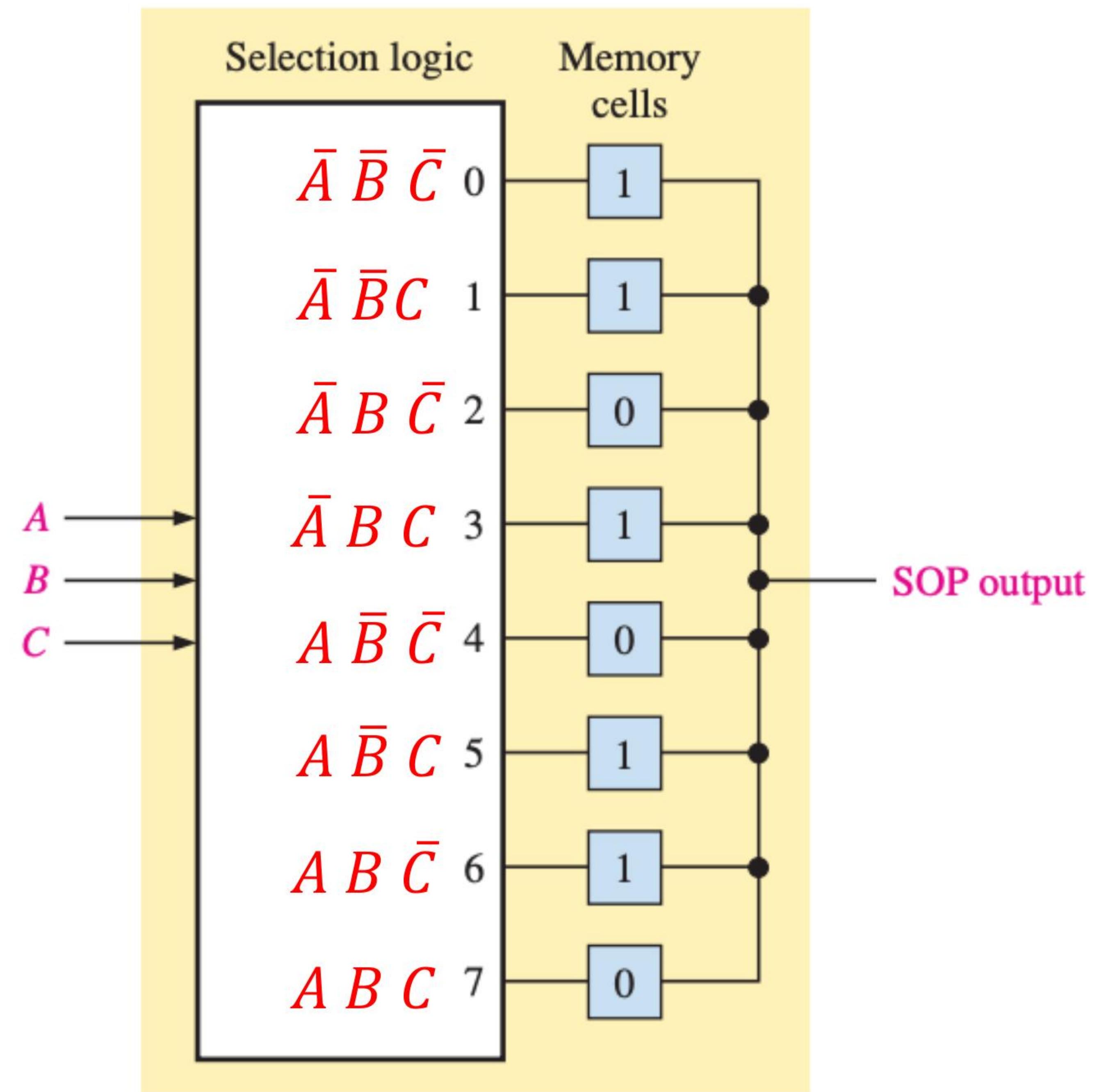
Question

Determine the output expression of the LUT for the internal conditions shown in Figure 10–72.



Question

Determine the output expression of the LUT for the internal conditions shown in Figure 10–72.



$$\bar{A} \bar{B} \bar{C} + \bar{A} \bar{B} C + \bar{A} B \bar{C} + A \bar{B} C + A B \bar{C}$$

