香港中文大學（深圳）
The Chinese University of Hong Kong, Shenzhen

EIE2050 Digital Logic and Systems

Tutorial 11

Zhipeng Xu

Contact: 222010049@link.cuhk.edu.cn

Office: Zhixin334

Problem 1

A. 1K × 4 RAM contains _____address lines and ____ data lines. If want to extend to 1K × 8 RAM, can use ____.

B. 256K × 4 RAM contains ____address lines and ____ data lines. If want to extend to 256K × 8 RAM, can use ____.

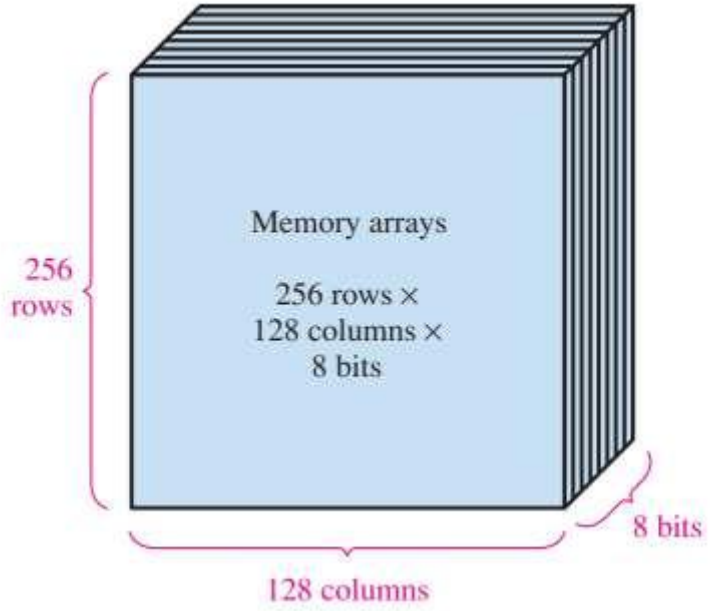
Solution 1

A. 1K × 4 RAM contains __10__ address lines and __4__ data lines. If want to extend to 1K × 8 RAM, can use __bit size expansion__.

B. 256K × 4 RAM contains __18__ address lines and __4__ data lines. If want to extend to 256K × 8 RAM, can use __word size expansion__.

Problem 2

Assuming that a 64k * 8 SRAM has a structure similar to that of the SRAM in Figure 1,determine the number of rows and 8-bit columns in its memory cell array.



Solution 2

64k ×8

= 512 ×128 ×8

= 512 rows × 128 8-bit columns

Problem 3

What is the difference between SRAM and DRAM?

Solution 3

The difference between SRAM and DRAM is that data in a SRAM are stored in latches or flip-flops indefinitely as long as power is applied while data in a DRAM are stored in capacitors which require periodic refreshing to retain the stored data.

Problem 4

What is the total bit capacity of a ROM that has 14 address lines and 8 data outputs?

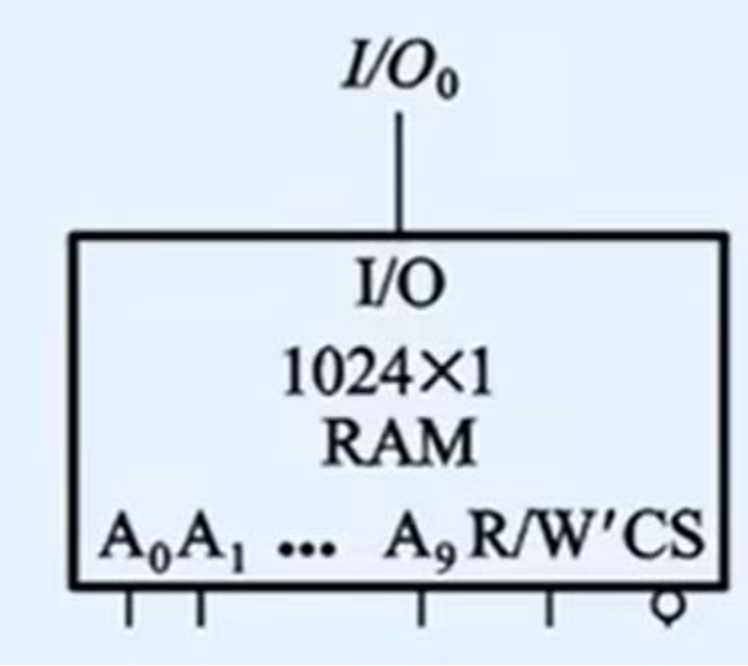
Solution 4

$2^{14} = 16{,}384$ addresses

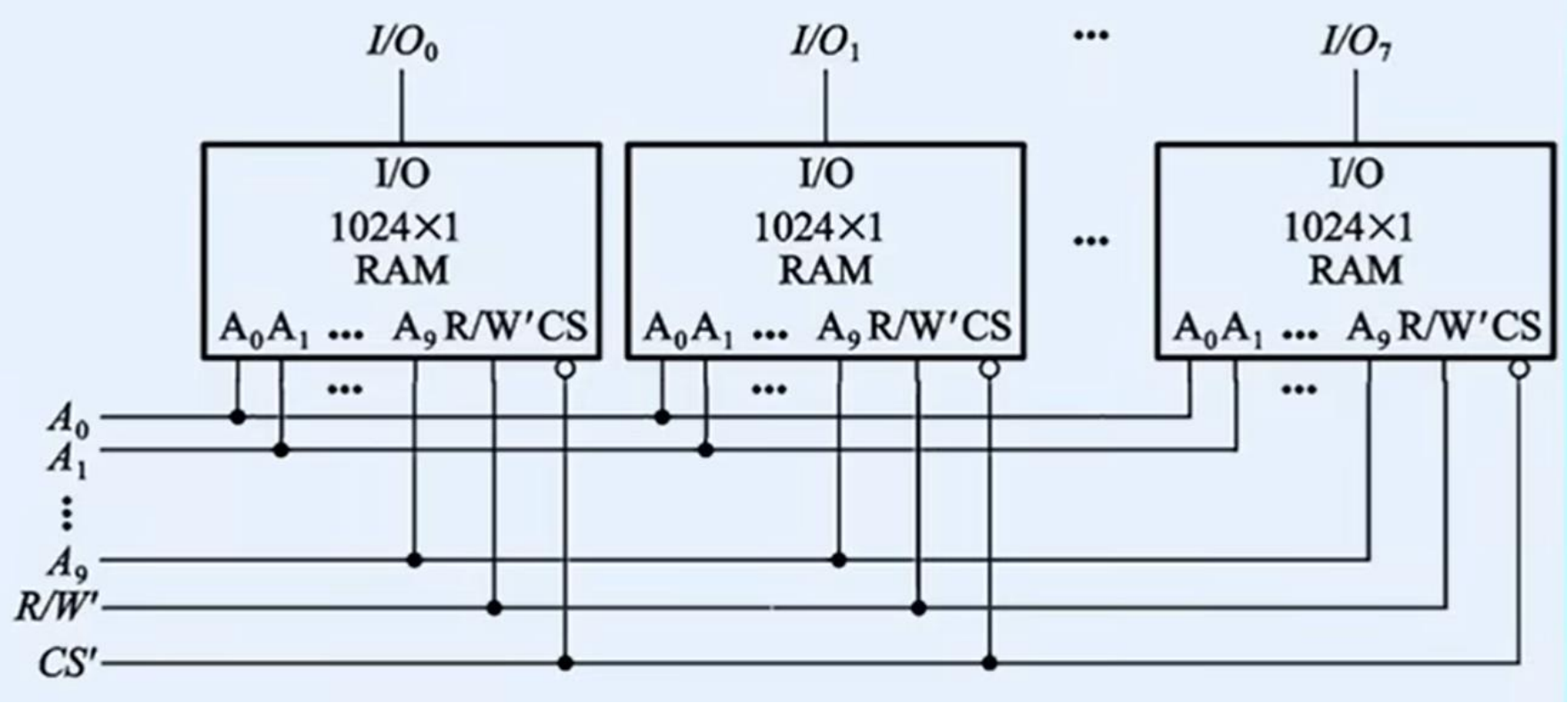
$16{,}384 \times 8$ bits = **131,072 bits**

Problem 5

Design of 1024×8 RAM using 1024×1 RAM. Show the logic diagram.

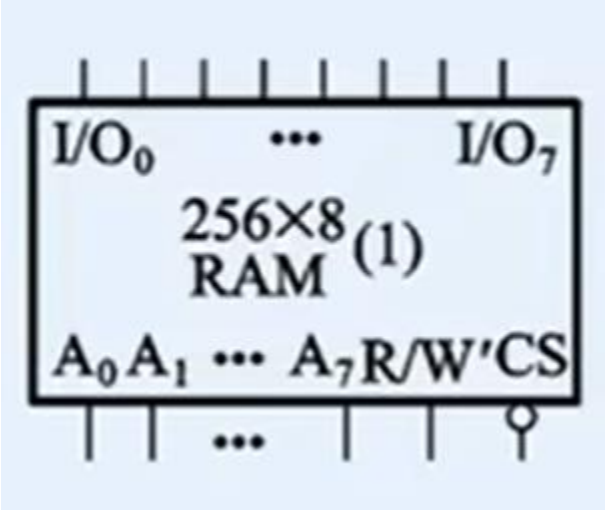


Solution 5

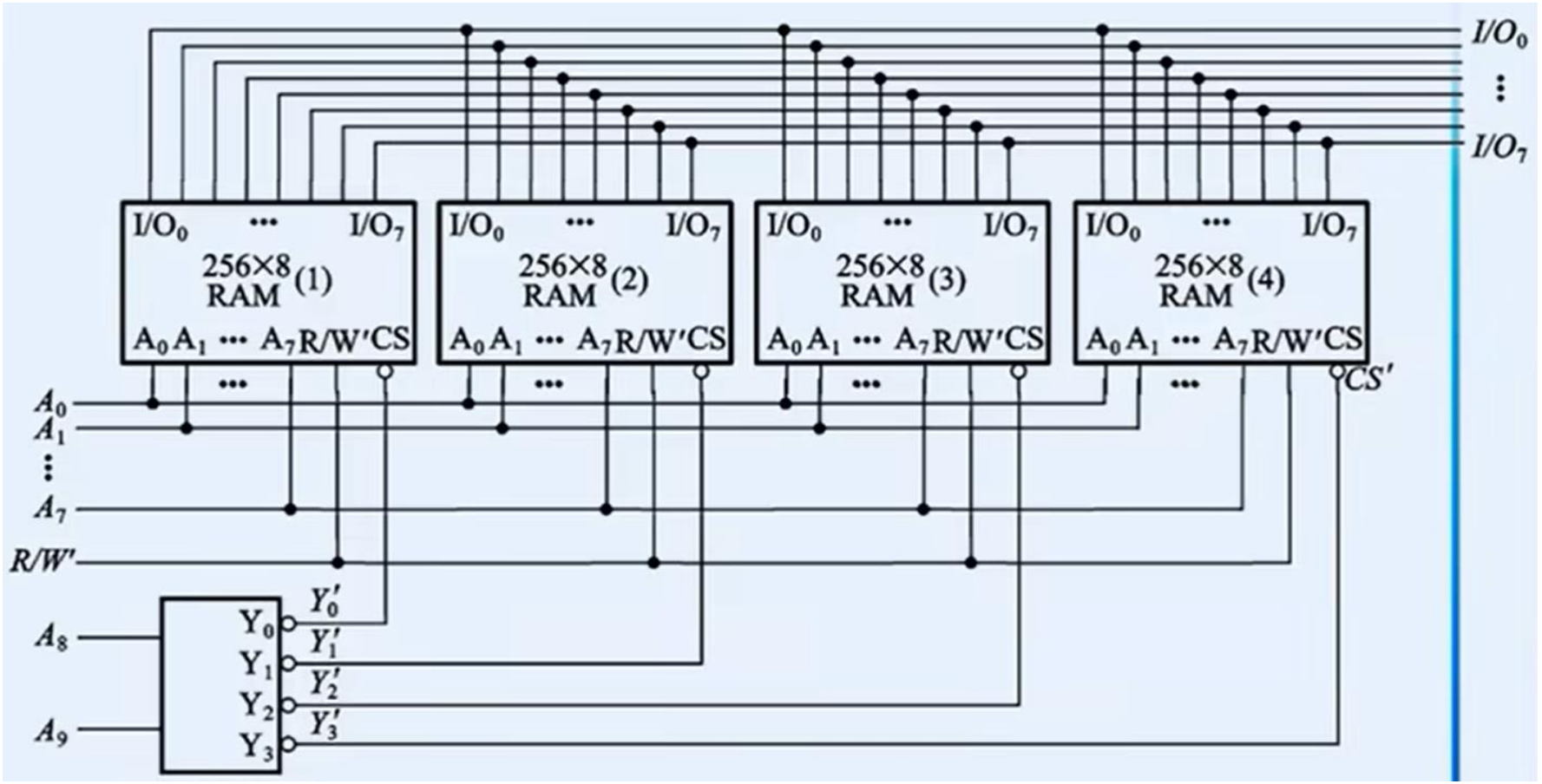


Problem 6

Design of 512×8 RAM using 128×8 RAM. Show the logic diagram.



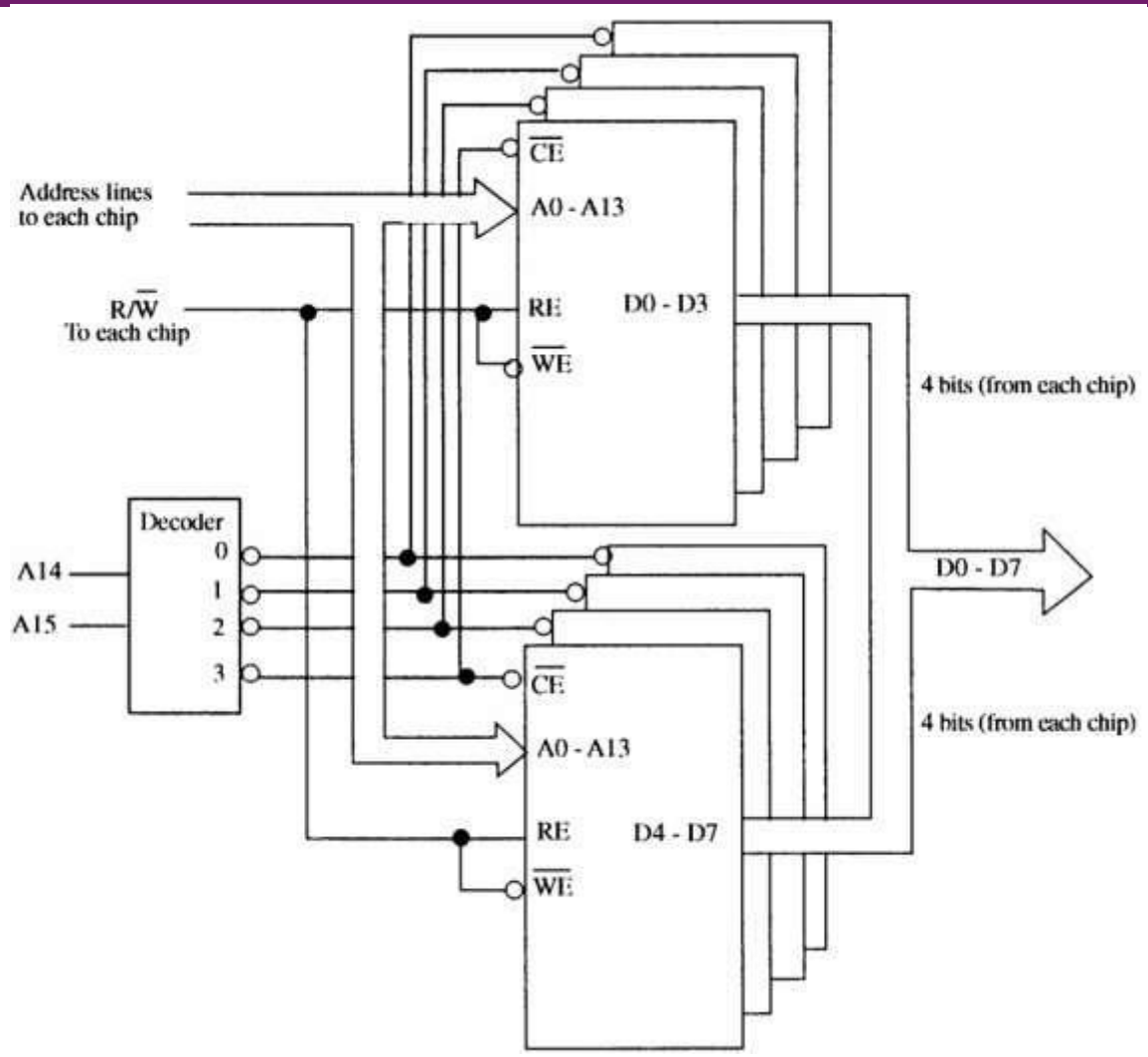
Solution 6


I/O0
I/O7
256×8 RAM (1)
256×8 RAM (2)
256×8 RAM (3)
256×8 RAM (4)
A0 A1 ··· A7 R/W′ CS
A0
A1
A7
R/W′
A8
A9
Y0
Y1
Y2
Y3
Y′0
Y′1
Y′2
Y′3
CS′

Problem 7

Use 16k * 4 DRAMs to build a 64k * 8 DRAM. Show the logic diagram.

Solution 7


Address lines
to each chip
R/W
To each chip
CE
A0 - A13
RE
D0 - D3
WE
4 bits (from each chip)
Decoder
A14
A15
0
1
2
3
D0 - D7
CE
A0 - A13
RE
D4 - D7
WE
4 bits (from each chip)

香港中文大學（深圳）
The Chinese University of Hong Kong, Shenzhen

Q&A

香港中文大學（深圳）
The Chinese University of Hong Kong, Shenzhen

Thank You!