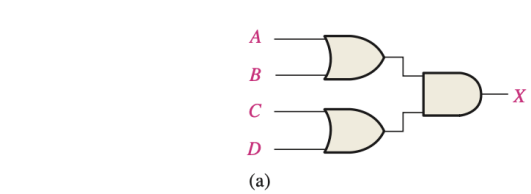
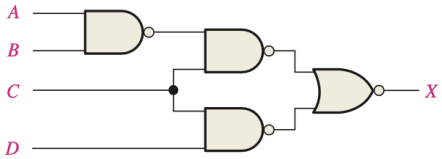
ECE2050 Homework 4

Due: March 13, 2025

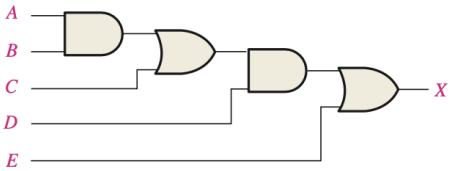
Q1 Redesign the following circuits using only NAND gates to achieve the same functionality.



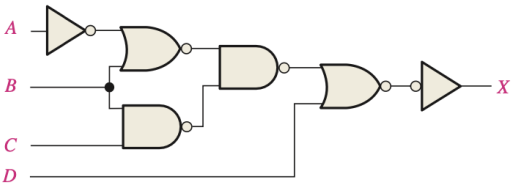
(a)



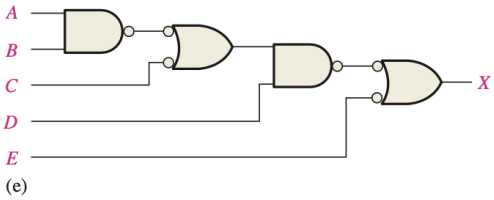
(b)



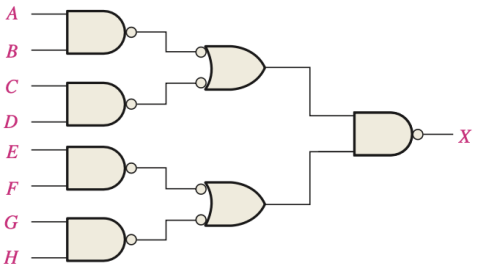
(c)



(d)



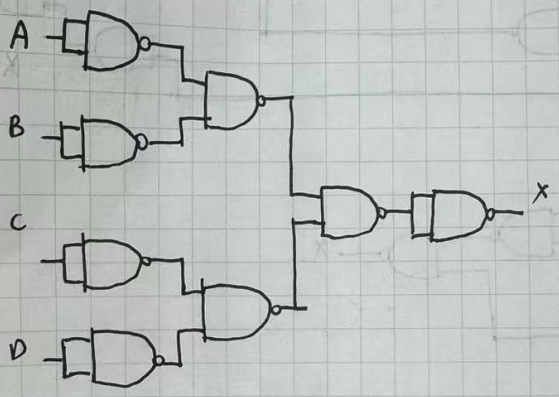
(e)



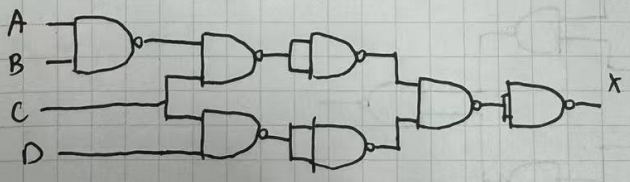
(f)

Q1: Using the bubble pushing & NAND → NOT
AND
OR
NOR.

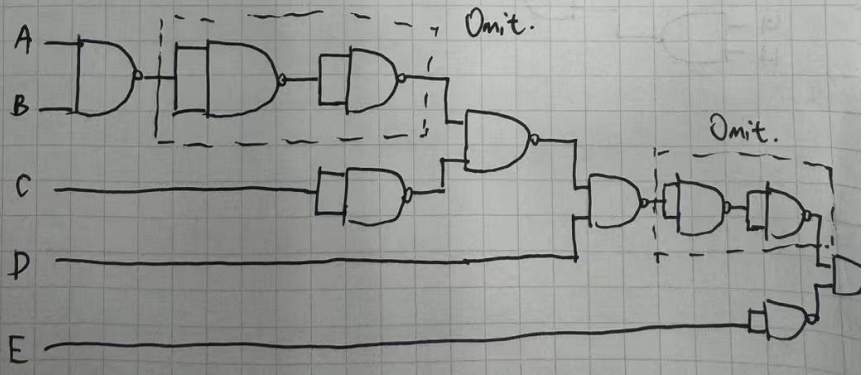
(1).

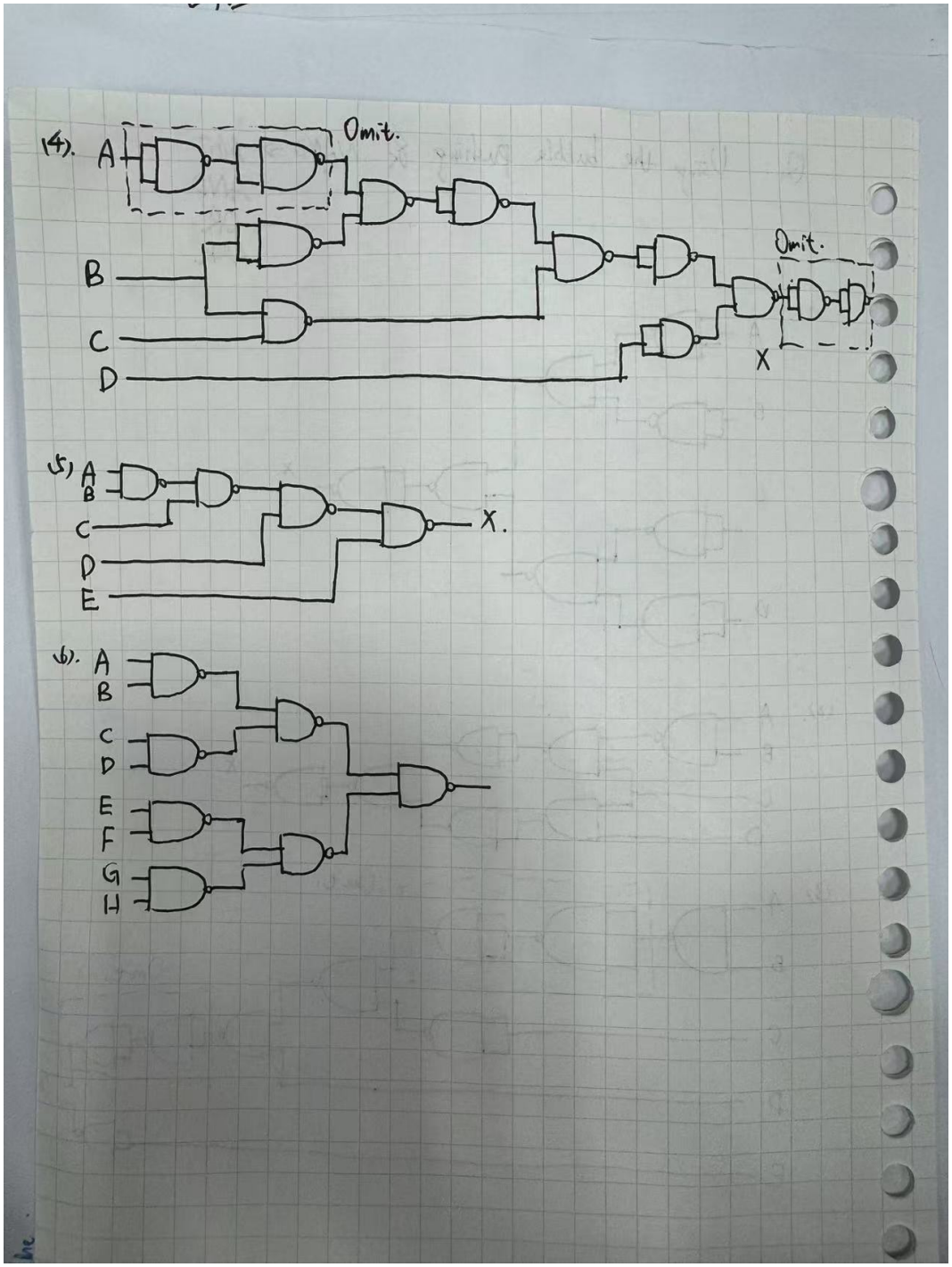


(2).



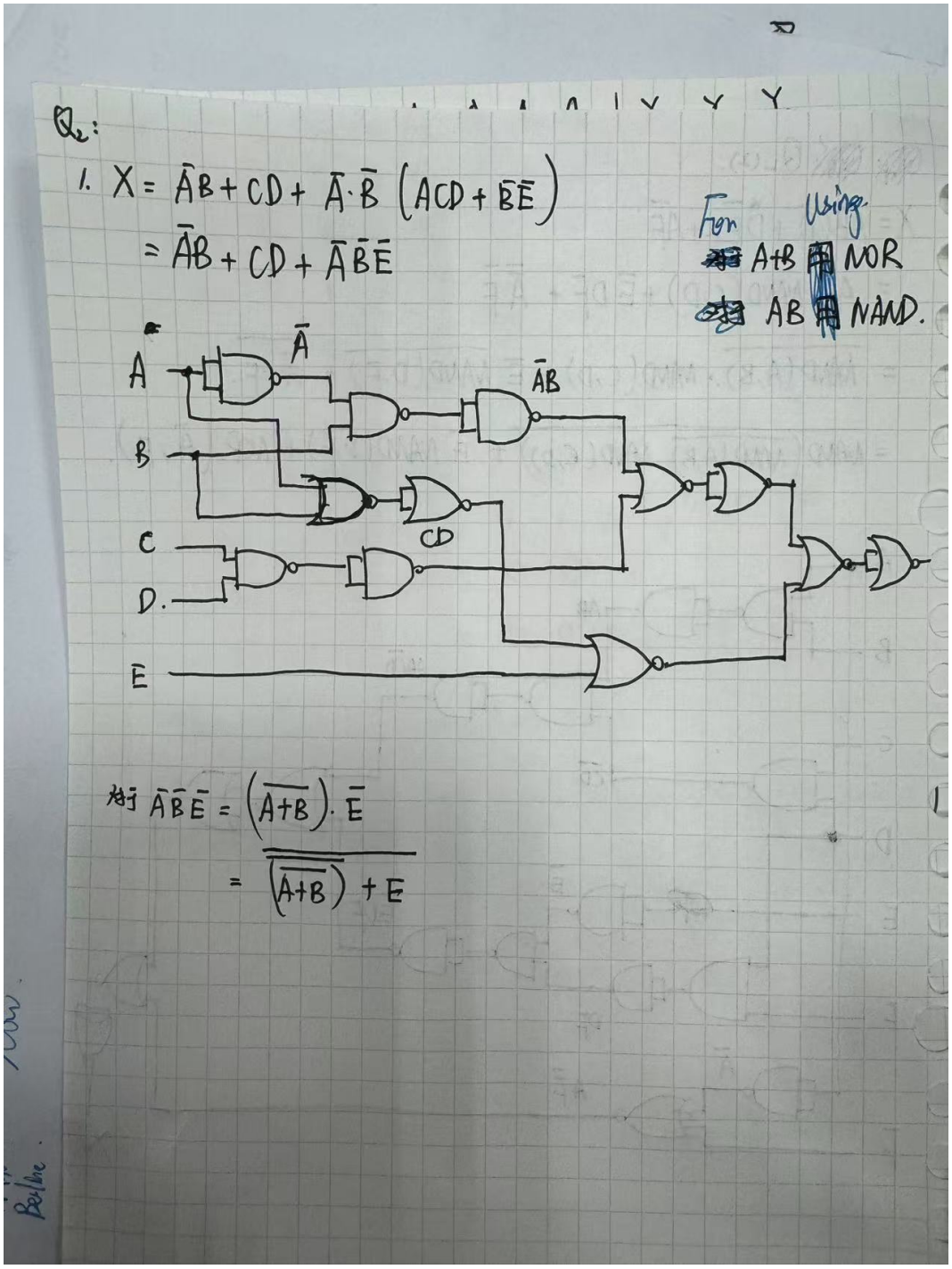
(3)




(4).
A
B
C
D
Omit.
Omit.
X
(5)
A
B
C
D
E
X.
(6).
A
B
C
D
E
F
G
H

Q2 Use NAND gates, NOR gates, or combinations of both to implement the following logic expressions as stated:

1. $X = \bar{A}B + CD + (\overline{A+B})(ACD + \bar{B}\bar{E})$
2. $X = AB\overline{CD} + D\bar{E}F + \overline{AF}$



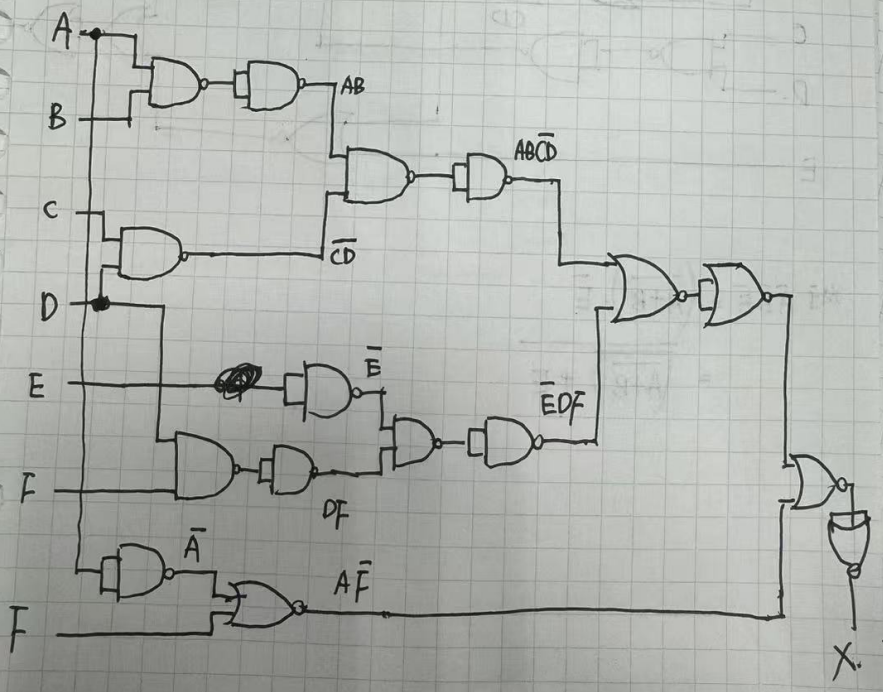
Q_(2).

$X = AB\bar{C}\bar{D} + \bar{D}\bar{E}F + A\bar{F}$

$= AB \cdot NAND(C,D) + \bar{E}DF + \bar{A}\bar{F}$

$= \overline{NAND(A,B)} \cdot NAND(C,D) + \bar{E}\,\overline{NAND(D,F)} + \overline{\bar{A}+F}$

$= \overline{NAND\left(\overline{NAND(A,B)}, NAND(C,D)\right)} + \bar{E}\,NAND(D,F) + NOR(\bar{A},F)$



Q3 Implement a logic circuit for the below truth table

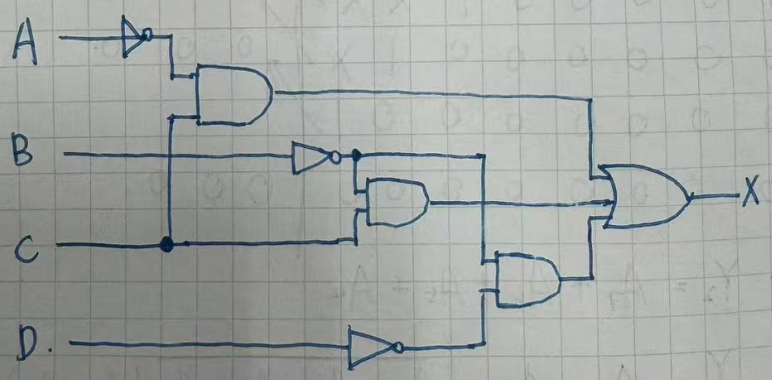
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	X
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	X
1	1	0	0	0
1	1	0	1	X
1	1	1	0	0
1	1	1	1	0

Q3.

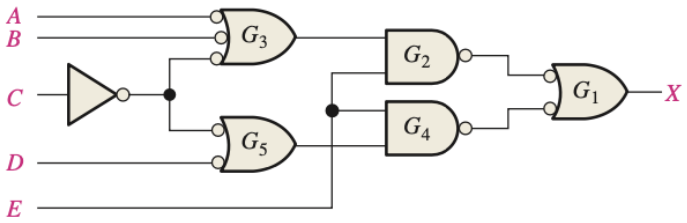
AB \ CD	00	01	11	10
00	1	0	1	1
01	0	X	1	1
11	0	X	0	0
10	1	0	X	1

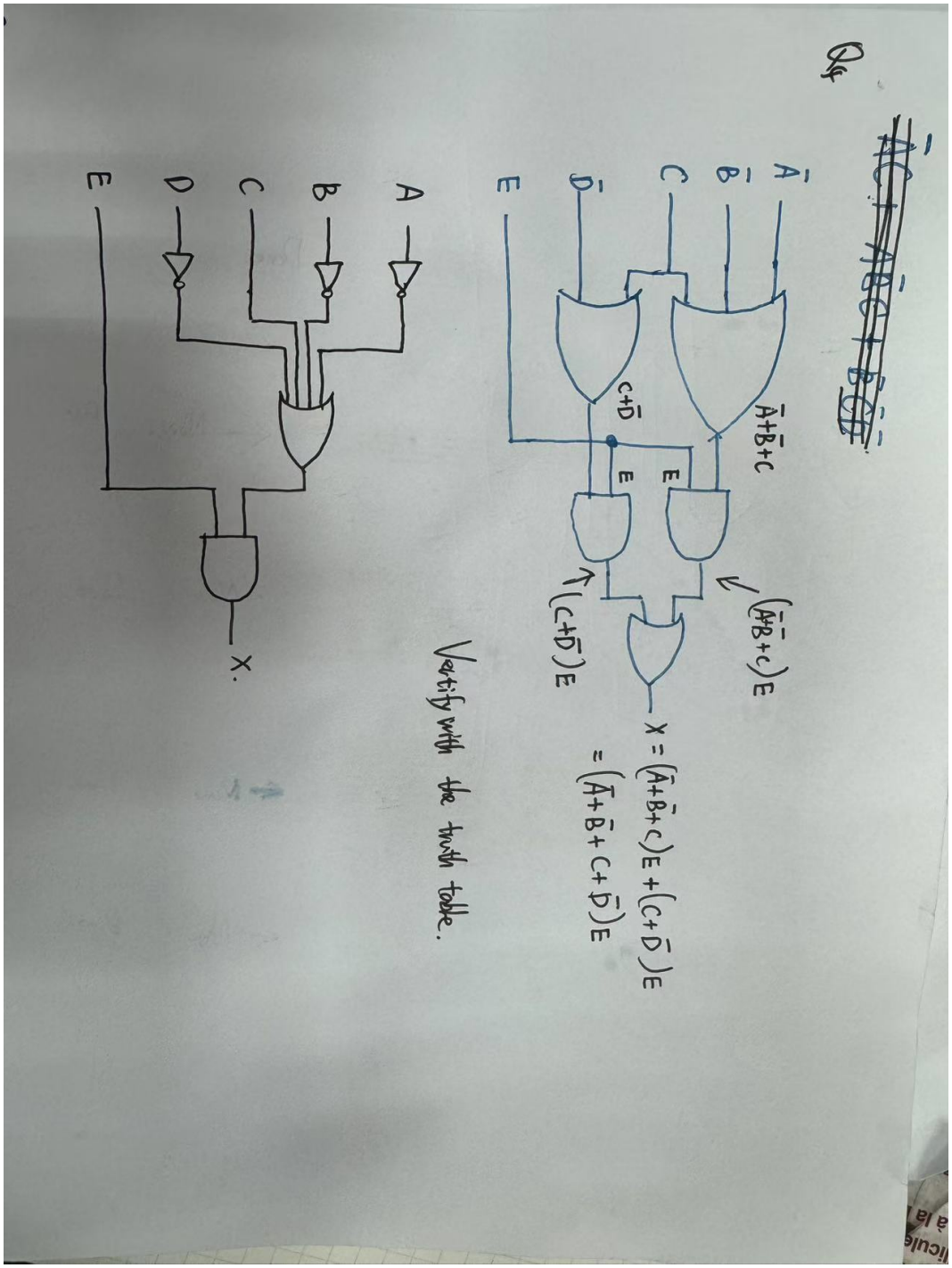
~~$\bar{A}C + A\bar{B}C + \bar{B}\bar{C}\bar{D}$~~

Expression: $\bar{B}\bar{D} + \bar{A}C + \bar{B}C$

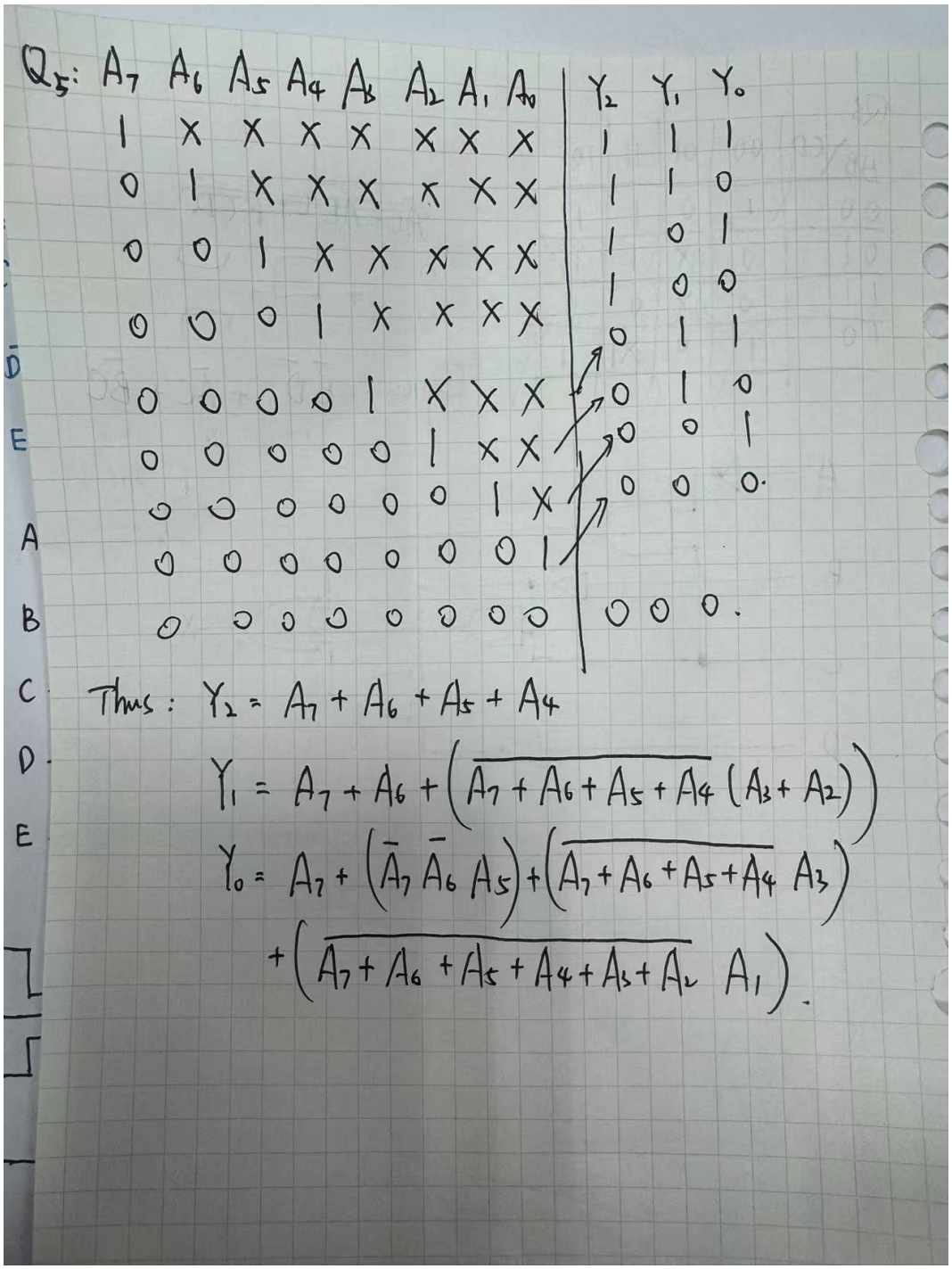


Q4 Simplify the below circuit as much as possible, and verify that the simplified circuit is equivalent to the original by showing that the truth tables are identical.

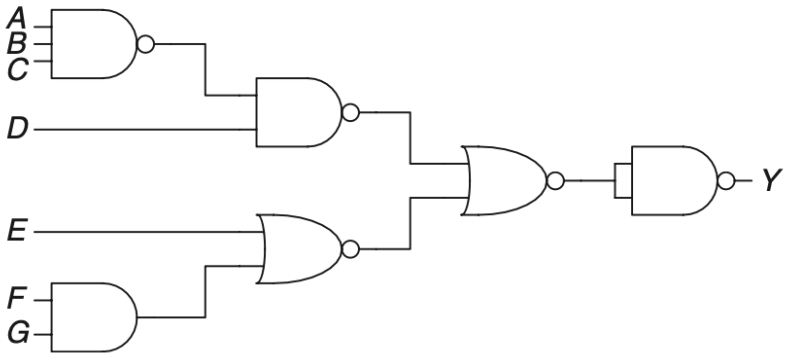


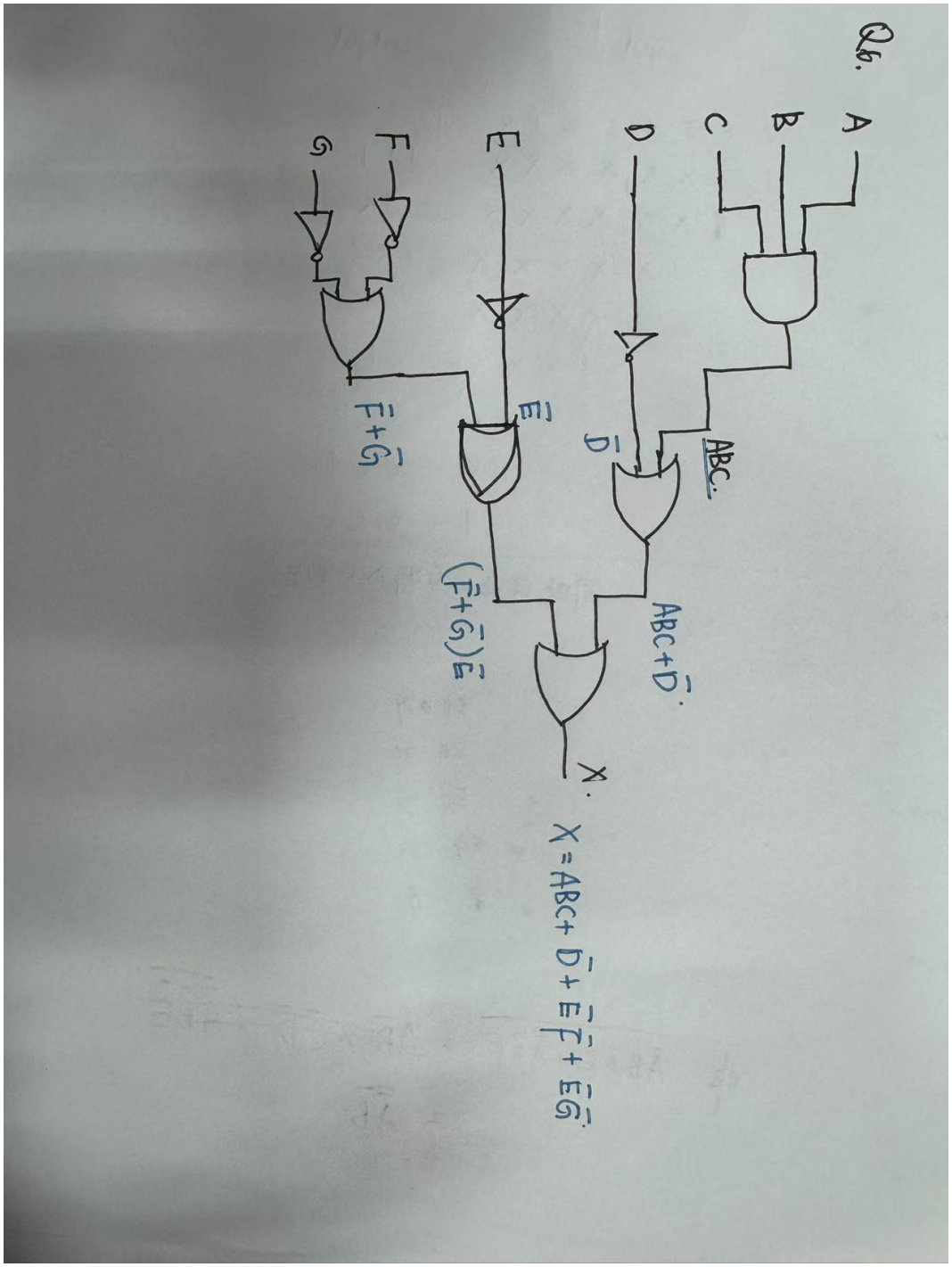


Q5 Design a modified priority encoder that receives an 8-bit input, $A_{7:0}$, and produces one 3-bit output, $Y_{2:0}$. Y indicates the most significant bit of the input that is TRUE. Y should be 0 if none of the inputs are TRUE. Give a simplified Boolean equation for each output and design a circuit using only NOR gates.



Q6 Using De Morgan equivalent gates and bubble pushing methods, redraw the below circuit so that you can find the Boolean equation by inspection. Write the Boolean equation.




Q6.
A
B
C
D
E
F
G
ABC..
D̄
ABC+D̄.
Ē
(F̄+Ḡ)Ē
F̄+Ḡ
X.
X = ABC + D̄ + EF̄ + EḠ.

Q7 A communication system uses the even-parity code as shown in Figure 1 in the sender and the even-parity code checker as shown in Figure 2 in the receiver to detect data transmission. Please analyze what happens when there is an error, or there is no error. (You should give two examples (no error and error) to answer the question.)

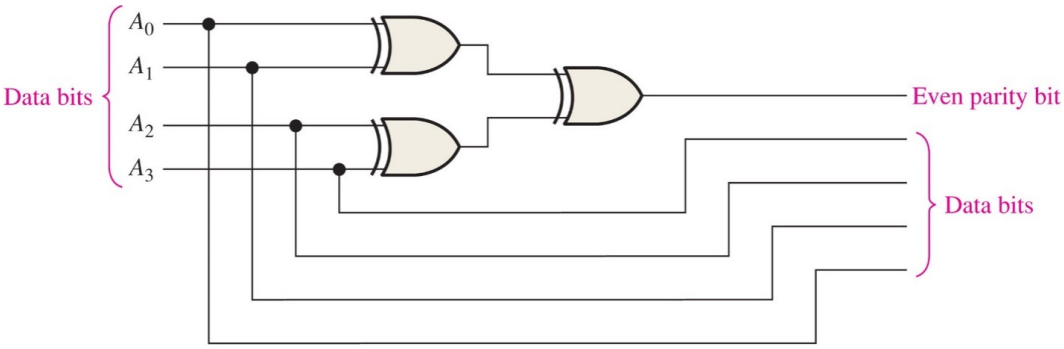


Figure 1: The even-parity code generator

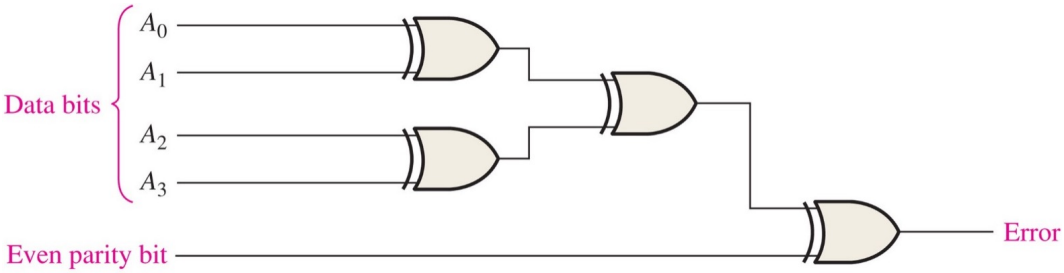


Figure 2: The even-parity code checker

We consider $X=0$. then case 1: $(A_0 \oplus A_1)=(A_2 \oplus A_3)=0$.

then A_0, A_1 are the same and A_2, A_3 are the same

case 2: $(A_0 \oplus A_1)=(A_2 \oplus A_3)=1$.

the A_0, A_1 are different and A_2, A_3 are different

Then True table of figure 1:

A_3	A_2	A_1	A_0	Even parity bit.
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

If we send.

then $A_{3:0} = 0001$ the generated Epb = 1.

If we received

$A_{3:0} = 0001$, the generated Epb = 1

then no error.

If we received.

$A_{3:0} = 0011$, the generated Epb = 1.

↑

then Error = 1, error happens.