

香港中文大學(深圳)
The Chinese University of Hong Kong, Shenzhen

ECE2050 Digital Logic and Systems

Tutorial 9

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Definition

- **What's the difference between synchronous counter and asynchronous counter?**



Definition

- **What's the difference between synchronous counter and asynchronous counter?**
 - Synchronous: The flip-flops are clocked simultaneously.
 - Asynchronous: The flip-flops are clocked by the output of the preceding flip-flop.



True or False

- a) One of the major drawbacks to the use of asynchronous counters is that the internal propagation delays limits its low-frequency applications.
- b) A 3-bit ripple counter, where each flip-flop has a propagation delay of 15 ns. For the counter to recycle from 111 to 000, it takes a total delay of 45 ns.
- c) At least 4 flip-flops are needed to construct an asynchronous counter with 12 states.
- d) In the design of asynchronous counters with J-K flip-flops, all flip-flops should be connected in SET mode.



True or False

One of the major drawbacks to the use of asynchronous counters is that the internal propagation delays limits its low-frequency applications.

False. The internal propagation delays limits the HIGH-frequency applications of asynchronous counter. When frequency is high, the period of clock signal is very short. And thus the propagation delay will be more significant.



True or False

A 3-bit ripple counter, where each flip-flop has a propagation delay of 15 ns. For the counter to recycle from 111 to 000, it takes a total delay of 45 ns.

True. Since a counter is constructed using flip-flops, therefore, the propagation delay in the counter occurs only due to the flip-flops. One bit change is 15 ns, so 3-bit change = $15\text{ ns} * 3 = 45\text{ ns}$.



True or False

At least 4 flip-flops are needed to construct an asynchronous counter with 12 states.

True. A n-bit asynchronous counters can have at most 2^n states. Since $2^3 < 12 < 2^4$, we need at least 4 flip-flops to construct an asynchronous counter with 12 states.



True or False

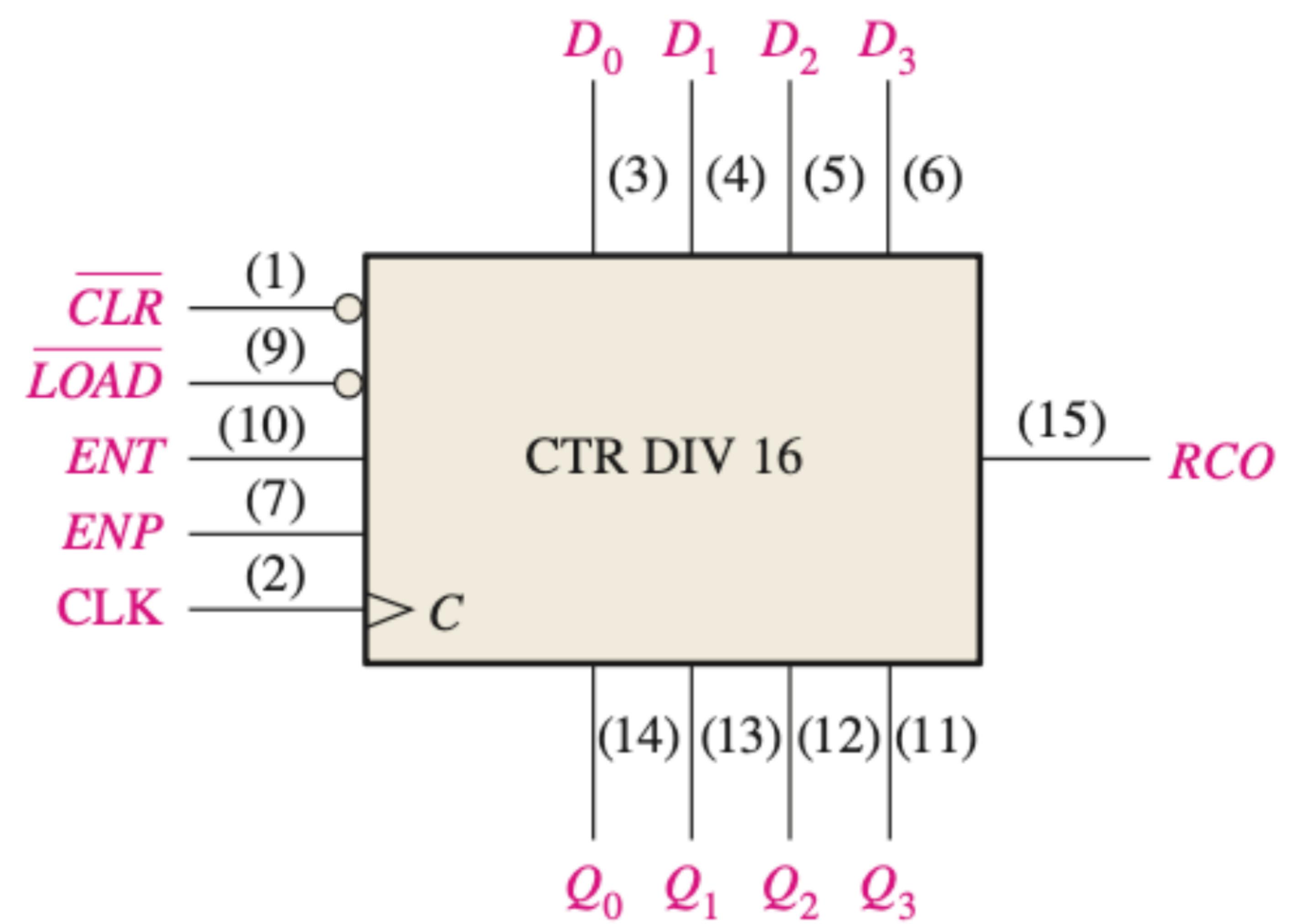
In the design of asynchronous counters with J-K flip-flops, all flip-flops should be connected in SET mode.

False. The flip-flops in the counter should be connected in toggle mode.



Decade Counter

- Use 74HC163 to design a decade counter (0-9).

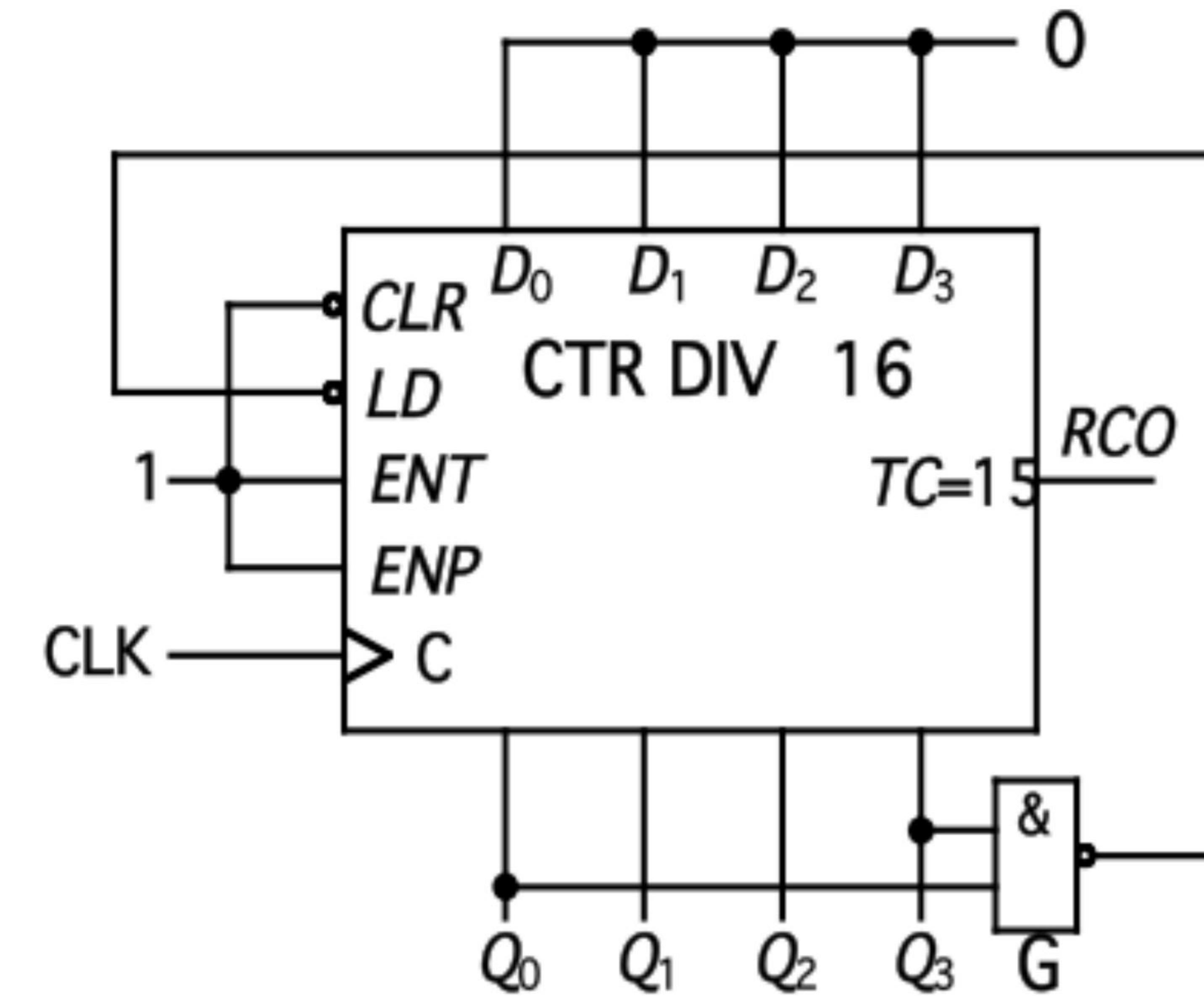
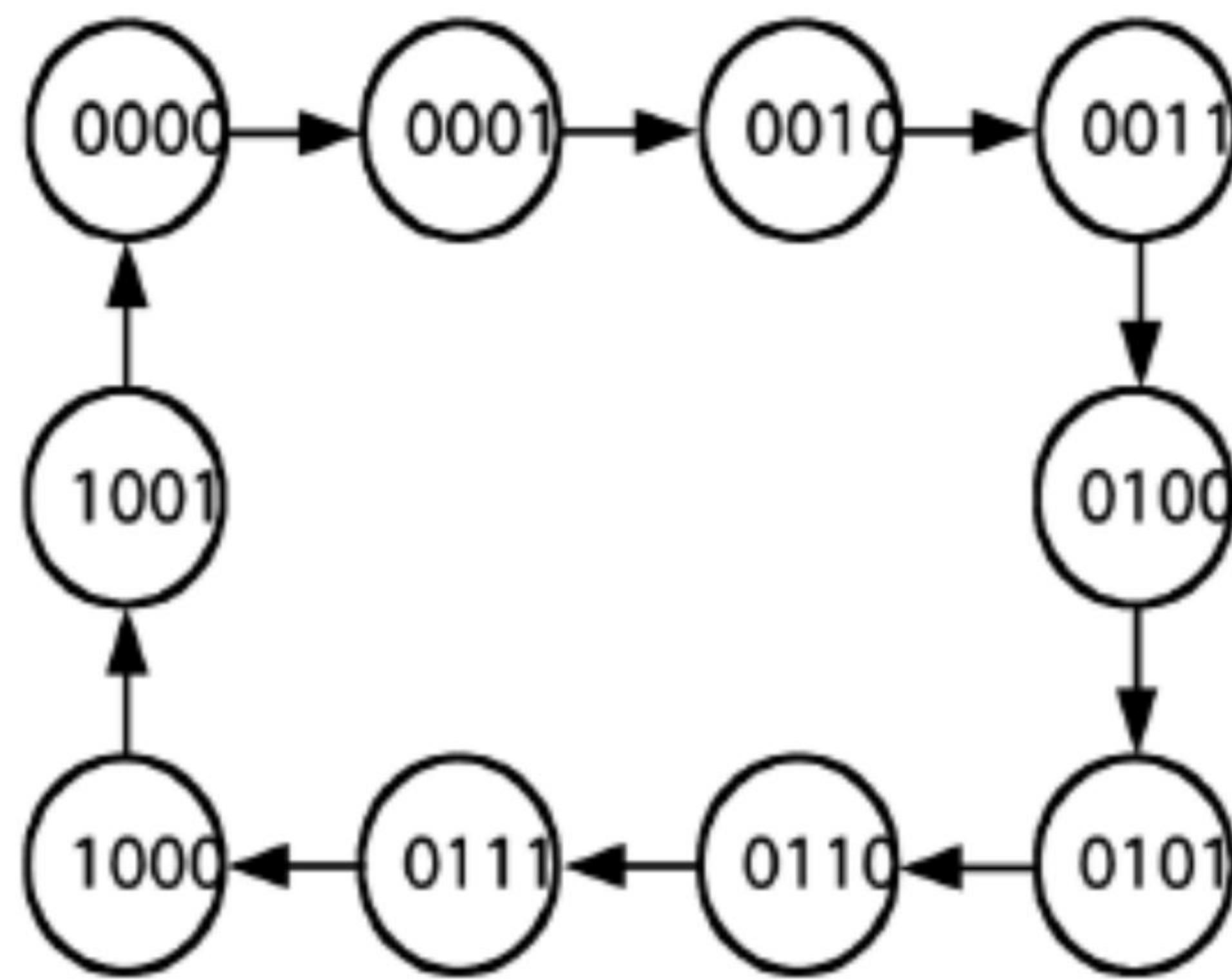


Symbol	Pin	Description
\overline{CLR}	1	synchronous master reset (active LOW)
CLK	2	clock input (L-to-H, edge triggered)
D_0, D_1, D_2, D_3	3,4,5,6	data input
ENP	7	count enable input
GND (not shown)	8	ground (0 V)
\overline{LOAD}	9	parallel enable input (active LOW)
ENT	10	count enable carry input
Q_0, Q_1, Q_2, Q_3	14,13,12,11	flip-flop output
TC	15	terminal count output
V_{CC}	16	supply voltage



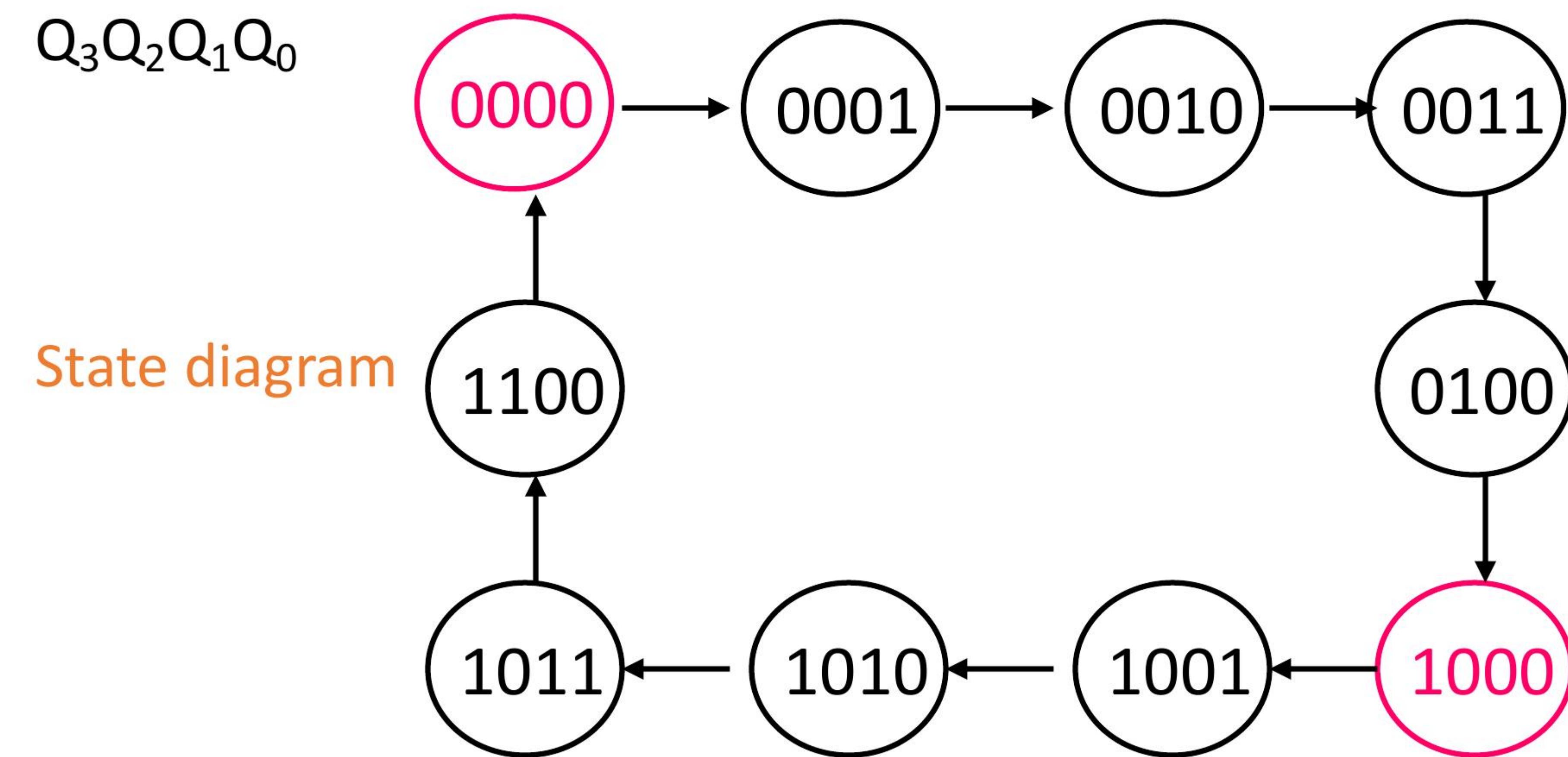
Decade Counter

- Use 74HC163 to design a decade counter (0-9).

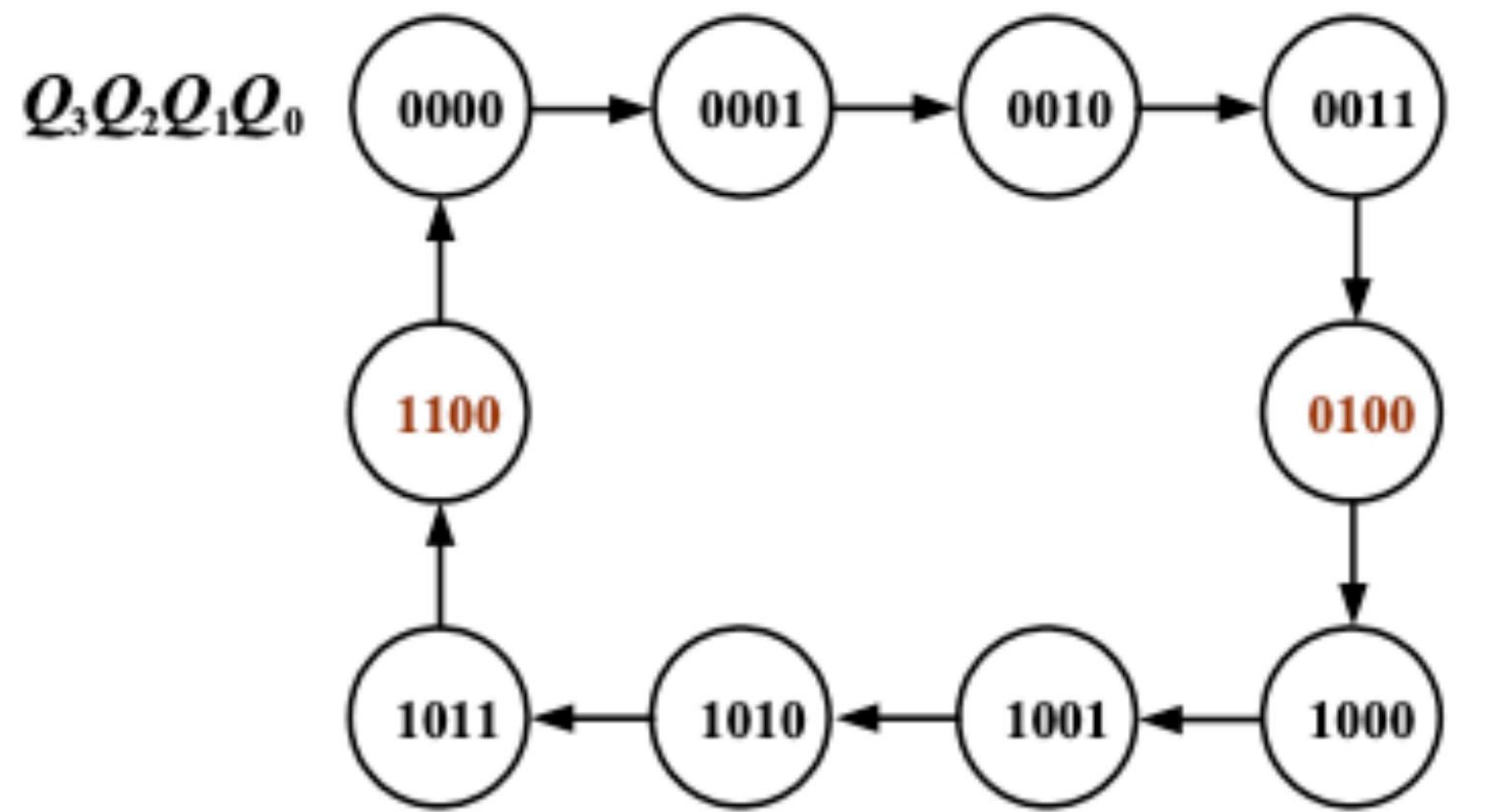


Decade Counter: Extension

- Use 74HC163 to design a counter.



Decade Counter: Extension



Karnaugh map for the decade counter:

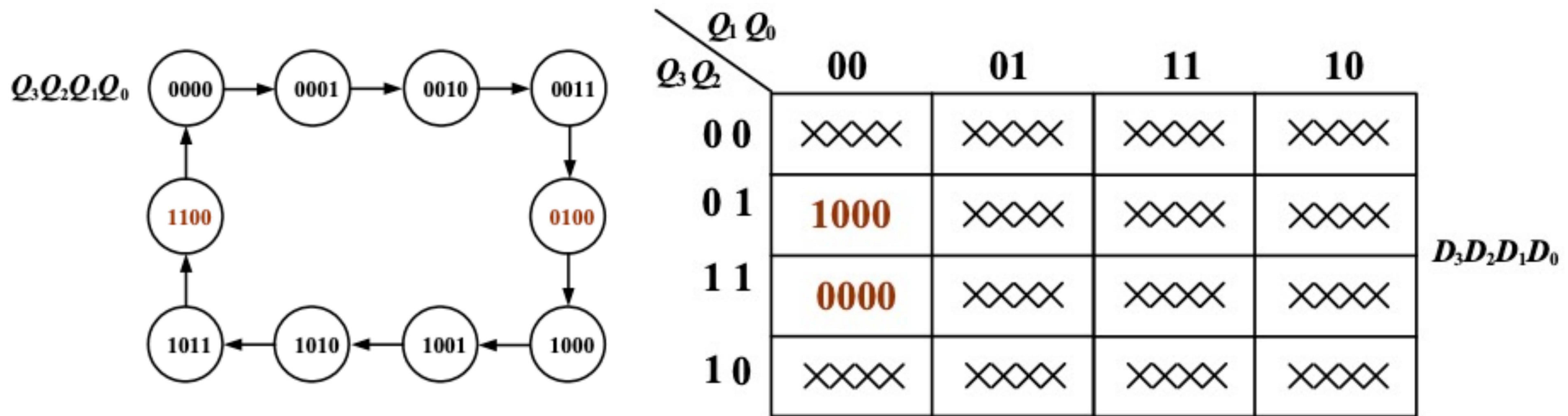
$\overline{Q_3 Q_2}$	$\overline{Q_1 Q_0}$	00	01	11	10
00	1	1	1	1	
01	0	\times	\times	\times	
11	0	\times	\times	\times	
10	1	1	1	1	

The Karnaugh map shows the relationship between the state variables Q_3, Q_2, Q_1, Q_0 and the output \overline{LD} . The output $\overline{LD} = \overline{Q_2}$.

$$\overline{LD} = \overline{Q_2}$$



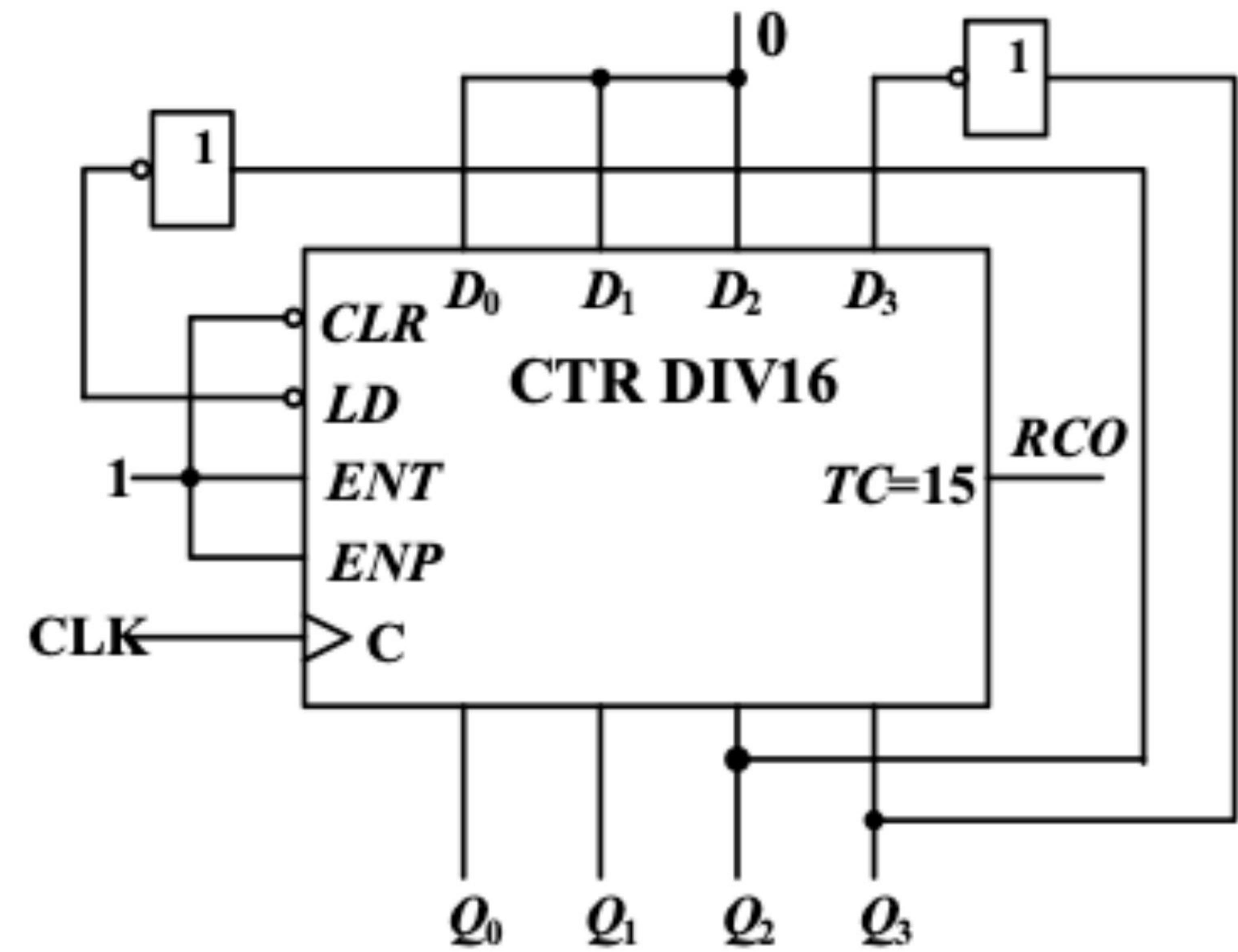
Decade Counter: Extension



$$D_0 = D_1 = D_2 = 0$$
$$D_3 = \overline{Q_3}$$

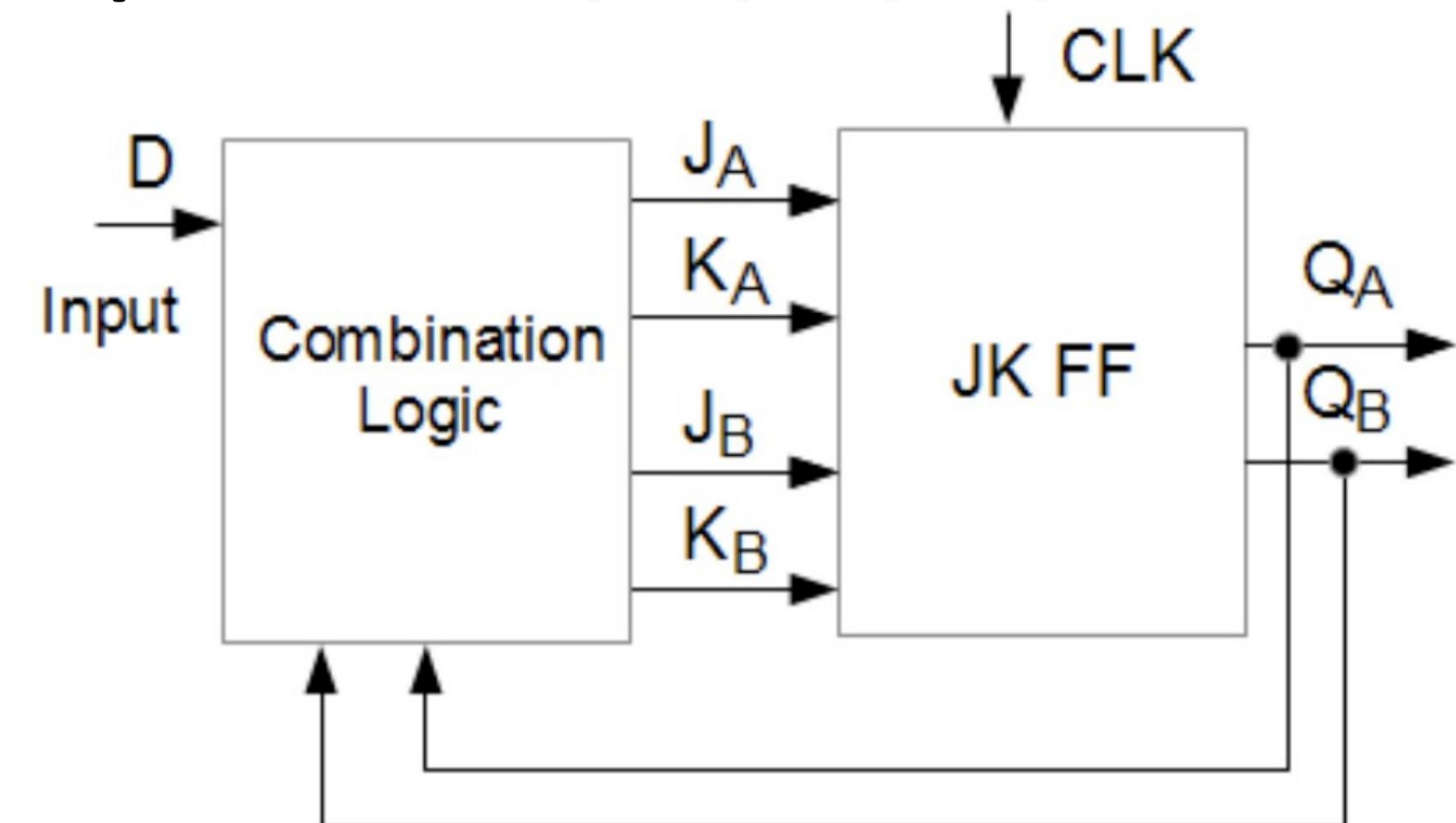


Decade Counter: Extension



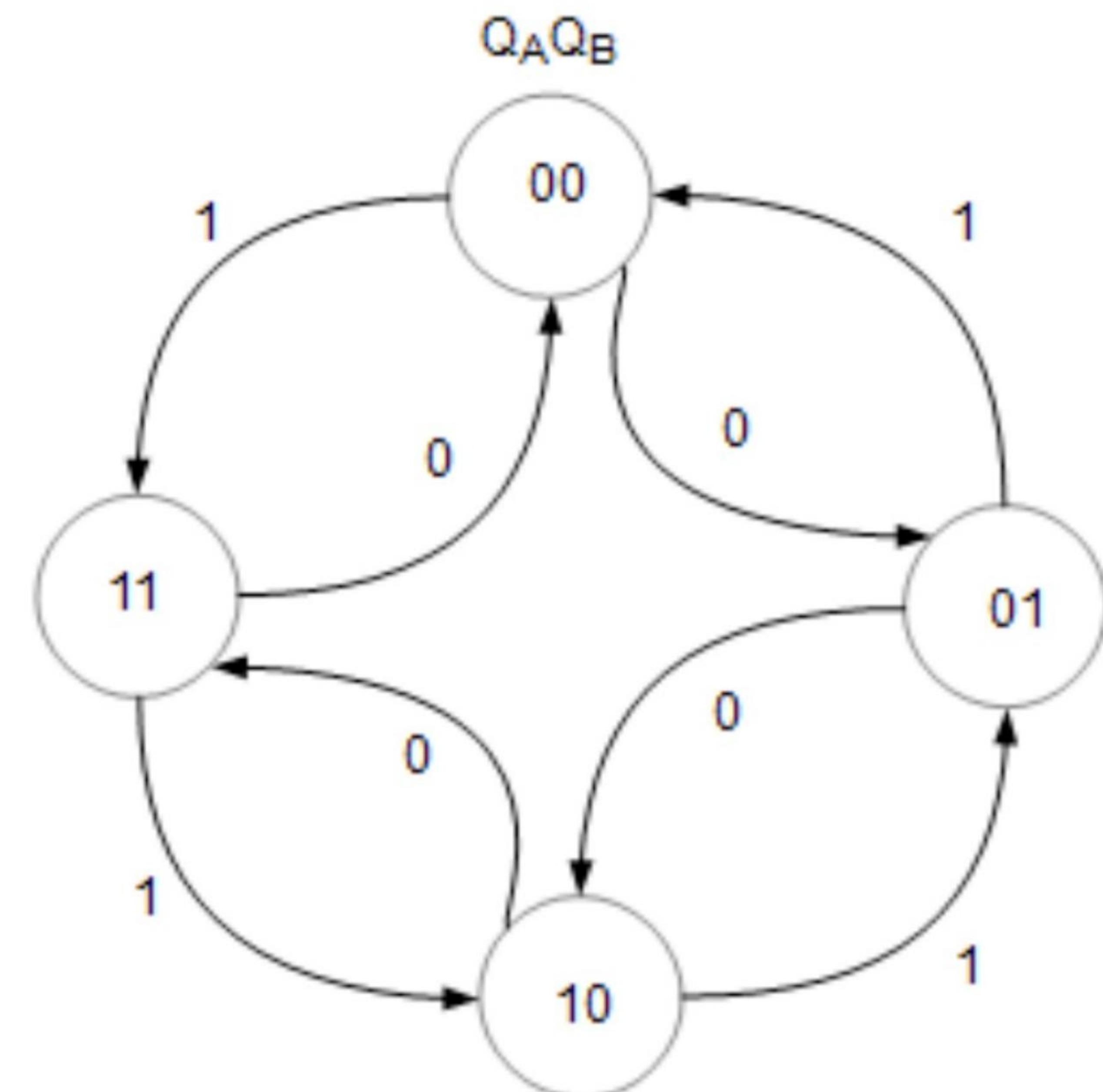
Up/Down Counter

- As is shown in the figure, design a 2 bit up/down counter with 2 J-K flip-flops and an input D which determines the up/down function. Thus, when $D = 0$, the count sequence is 00, 01, 10, 11, 00 ... when $D = 1$, the count sequence is 00, 11, 10, 01, 00 ...



Up/Down Counter

- Step 1: Draw the state diagram for the given sequences.



Up/Down Counter

- Step 2: Develop a next-state table for the specific counter sequence.

JK Flip Flop Truth Table

J	K	Q
0	0	Q ₀
0	1	0
1	0	1
1	1	Toggle

JK Flip Flop Transition Table

Q _N	Q _{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Present State			Next State		JK flip flop inputs			
D	Q _A	Q _B	Q _A	Q _B	J _A	K _A	J _B	K _B
0	0	0	0	1	0	X	1	X
0	0	1	1	0	1	X	X	1
0	1	0	1	1	X	0	1	X
0	1	1	0	0	X	1	X	1
1	0	0	1	1	1	X	1	X
1	0	1	0	0	0	X	X	1
1	1	0	0	1	X	1	1	X
1	1	1	1	0	X	0	X	1



Up/Down Counter

- Step 3: Use K-map to specify Boolean expressions for each J and K.

$D \backslash Q_A Q_B$	00	01	11	10
0	0	1	X	X
1	1	0	X	X

$$J_A = \bar{D}Q_B + D\bar{Q}_B = D \oplus Q_B$$

$D \backslash Q_A Q_B$	00	01	11	10
0	X	X	1	0
1	X	X	0	1

$$K_A = \bar{D}Q_B + D\bar{Q}_B = D \oplus Q_B$$

$D \backslash Q_A Q_B$	00	01	11	10
0	1	X	X	1
1	1	X	X	1

$$J_B = 1$$

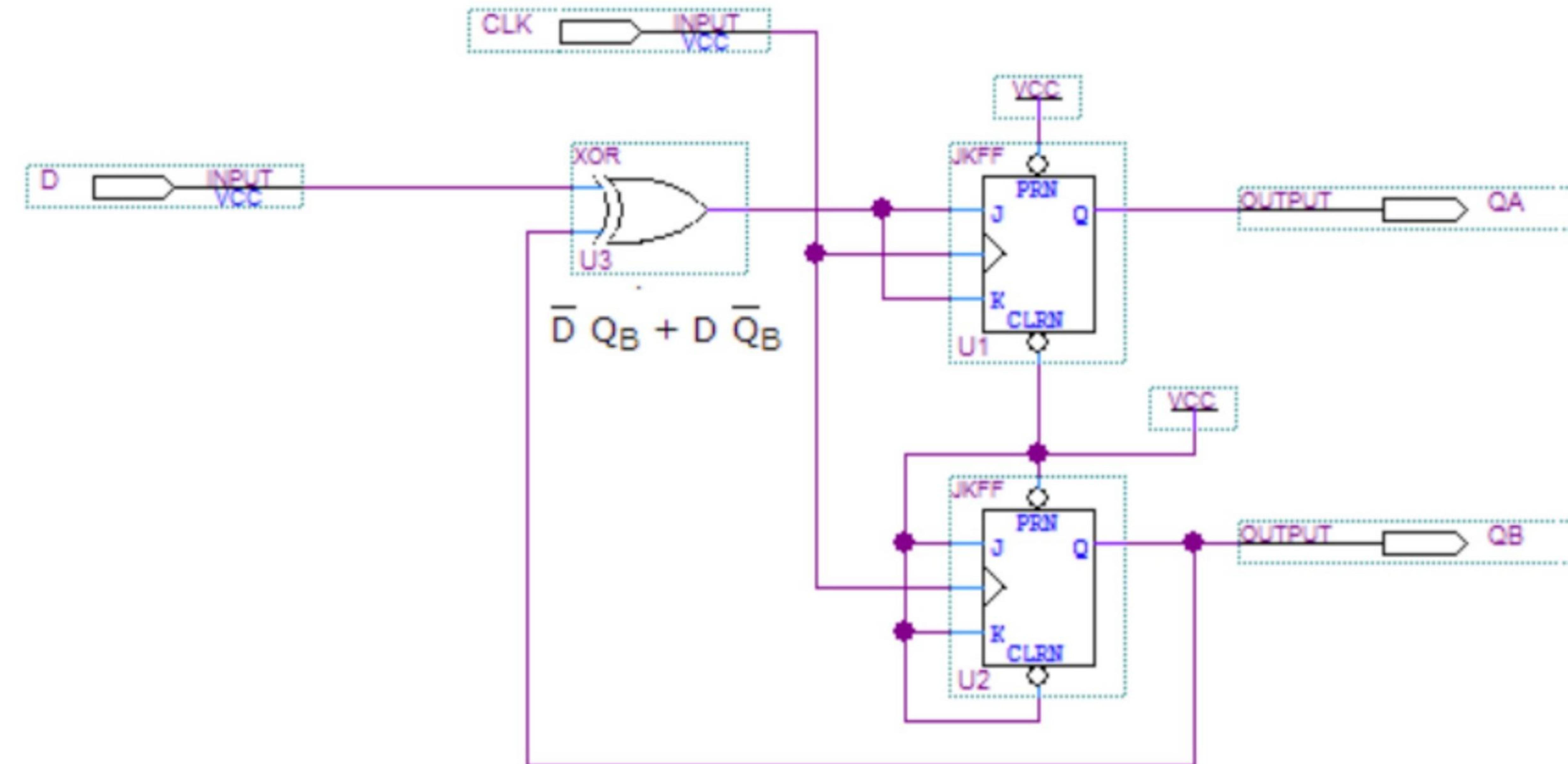
$D \backslash Q_A Q_B$	00	01	11	10
0	X	1	1	X
1	X	1	1	X

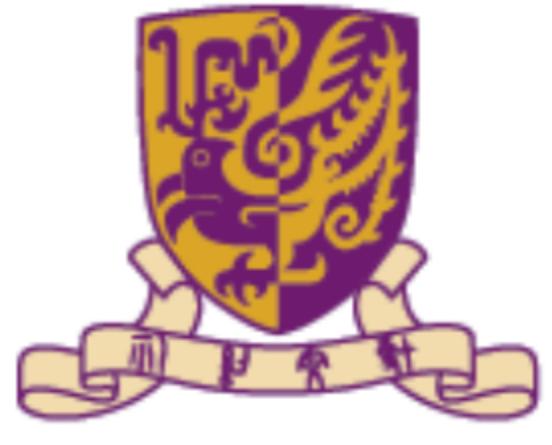
$$K_B = 1$$



Up/Down Counter

- Step 4: Use the Boolean expressions in step 3 to implement the circuit.





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Thank You!