Midterm Test

(Time allowed: 90 minutes)
March 17, 2024

NOTE: Answer ALL **8** questions. Show all intermediate steps, except Question 1 and Question 2.

1. (10 points) Are the following statements necessarily true (Y) or not (N)?

(1) In positive logic, a HIGH level represents a binary 0.
(2) The hexdecimal number system is a weighted system with 16 digits.
(3) The 2's complement of the binary number 1100 is 0011.
(4) It is possible to build an XOR gate with multiple NAND gates.
(5) The domain of the expression $ABD + \bar{C}D$ is A, B, C and D.
(6) In Boolean Algebra, the multiplication of two values is equivalent to the logical OR function.
(7) The MSB represents the highest-order bit in a binary representation.
(8) The complement of a sum of variables is equal to the product of the complements of each variable is a statement of Demorgan's theorem.
(9) A full-adder can be realized using only 2 half-adders.
(10) The multiplexer is a data distributor while a de-multiplexer is a data selector.

Solution:

(1) N
(2) Y
(3) N
(4) Y
(5) Y
(6) N
(7) Y
(8) Y
(9) N
(10) N

2. (10 points) Provide your answers to the following short questions.

(1) Convert the binary number 101101 to its hex representation;

(2) Convert the gray code 11010010 to binary;

(3) How many cells do a 4-variable Karnaugh map have?

(4) If the inputs to an exclusive-NOR function is A and B, write down the logic expression using And-Or-Invert logic.

(5) Determine the odd parity bit for the BCD number 00101001.

Solution:

(1) $2D$;

(2) 10011100

(3) 16;

(4) $AB + \bar{A}\bar{B}$;

(5) 0.

3. (15 points) Perform each of the following calculations in the 2's complement form.

(1) 01100101 − 11101000;

(2) 01101010 × 11110001;

(3) 01100110 ÷ 00100010.

Solution:

(1) 01111101 in Figure 1;

(2) 100111001010 in Figure 2;

(3) 00000011 in Figure 3.

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  01100101    Minuend (101)
+ 00011000    2's complement of subtrahend (-24)
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  01111101    Difference (125)
```

Figure 1: Q3-1 solution.

```
        1101010    Multiplicand (106)
    x   0001111    2's complement of multiplier (-15)
    -------
        1101010
       1101010
      1101010
  +   1101010
  ------------
  0 11000110110    Final product (1590)
  1 00111001010    2's complement (-1590)
```

Figure 2: Q3-2 solution.

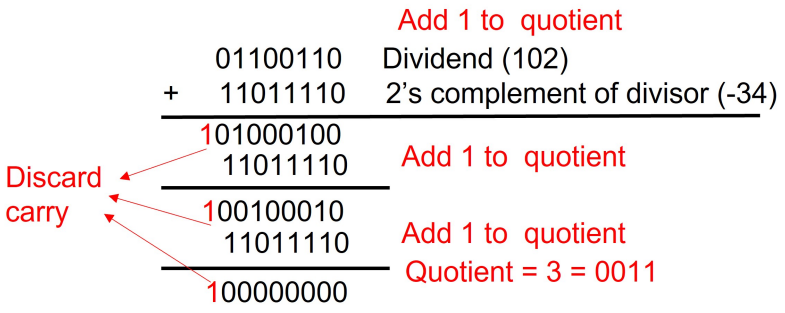

Figure 3: Q3-3 solution.

4. (15 points)

(1) Convert the following expression to standard sum-of-product(SOP) forms:
$(A + C)(BC + AC)$

(2) Convert the following expression to standard product-of-sum(POS) forms:
$(A + \bar{C})(A + BC)$

(3) Convert binary 1101.11 to its decimal representation.

Solution:

(1)

$$\begin{aligned}
&(A + C)(BC + AC) \\
=&ABC + AC + BC + AC \\
=&ABC + A(B + \bar{B})C + (A + \bar{A})BC \\
=&ABC + ABC + A\bar{B}C + ABC + \bar{A}BC \\
=&ABC + A\bar{B}C + \bar{A}BC
\end{aligned}$$

(2)

$$\begin{aligned}
&(A + \bar{C})(A + BC) \\
=&(A + \bar{C})(A + B)(A + C) \\
=&(A + \bar{C} + B\bar{B})(A + B + C\bar{C})(A + C + B\bar{B}) \\
=&(A + \bar{C} + B)(A + \bar{C} + \bar{B})(A + B + C)(A + B + \bar{C})(A + C + B)(A + C + \bar{B}) \\
=&(A + B + \bar{C})(A + \bar{B} + \bar{C})(A + B + C)(A + \bar{B} + C)
\end{aligned}$$

(3) $1101.11_2 = 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2} = 13.75$

5. (12 points) For the logic circuit and the input waveforms shown in Figure. 4, respectively, answer the following questions.

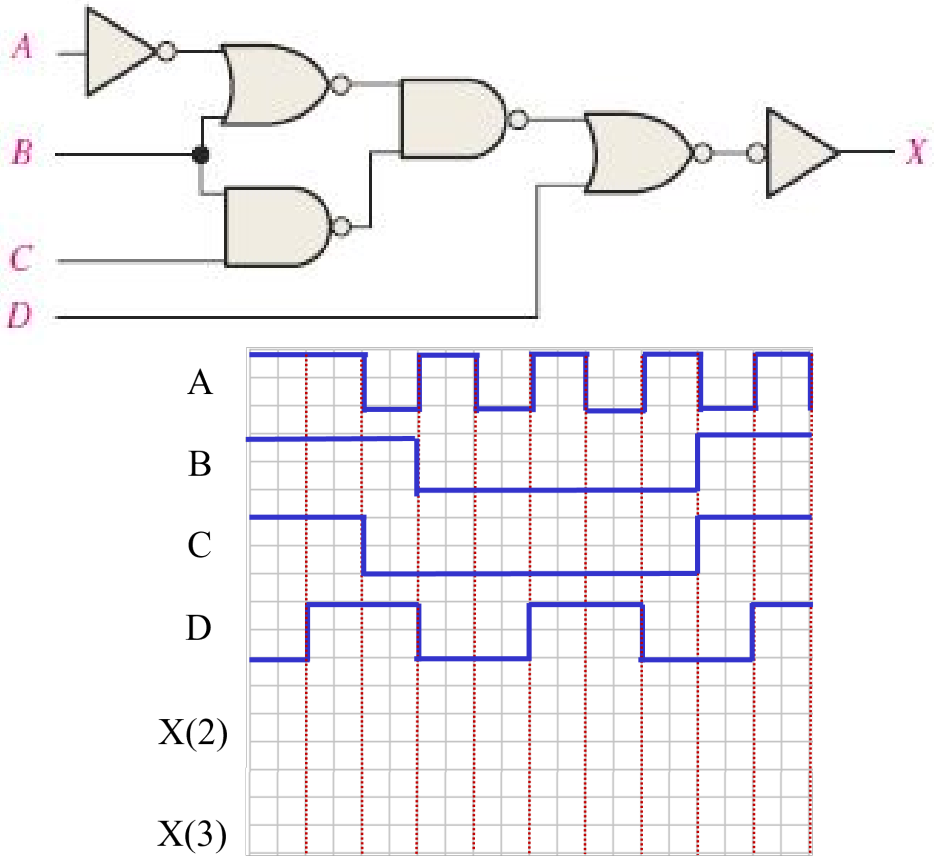

Figure 4: Combinational logic circuit and input waveforms for Q.5.

(1) (4 points) Derive the expression of the output X and minimize it using the boolean algebra laws and rules, show the intermediate steps;

(2) (4 points) Draw the output waveform based on the inputs.

(3) (4 points) Assuming that the input B is shorted to ground, derive the expression of the output X and draw its waveform.

Solution:

$$X = \overline{\overline{(\bar{A} + B)(\overline{BC})} + D} = \overline{(\bar{A} + B)(\overline{BC})} + D$$

$$= \bar{A} + B + BC + D = \bar{A} + B + D$$

(1)

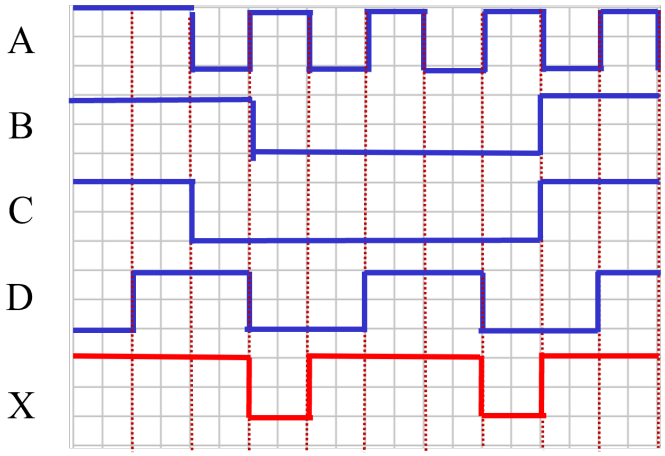

Figure 5: Output waveform of X for Q.5(1).

(2)

(3) $X = \bar{A} + D$

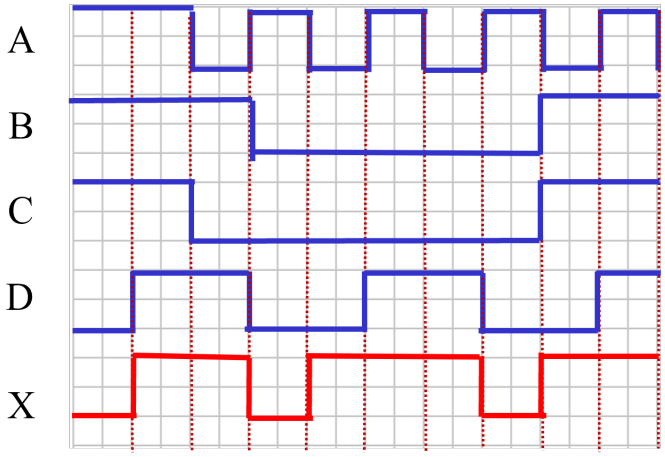

Figure 6: Output waveform of X for Q.5(2).

6. (15 points)

(1) Derive the minimized SOP expression from the truth table below using K-map (5 points), and implement it using basic gates such as AND, OR, Inverter(5 points). The complementary inputs, if needed, are **NOT** directly available, i.e. $\bar{A}, \bar{B}, \bar{C}, \bar{D}$ are **NOT** available. Same for the question below.

(2) (5 points) Implement the logic function specified in the truth table by using a 74HC151 8-input data selector/multiplexer.

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Table 1: The truth table of Q.6.

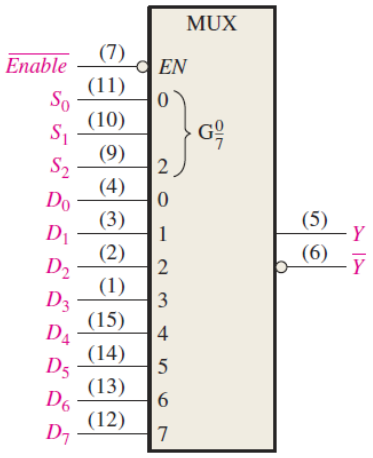

Figure 7: The 74HC151 8-input multiplexer.

Solution:

(1) The K-map is shown in Fig. 8.

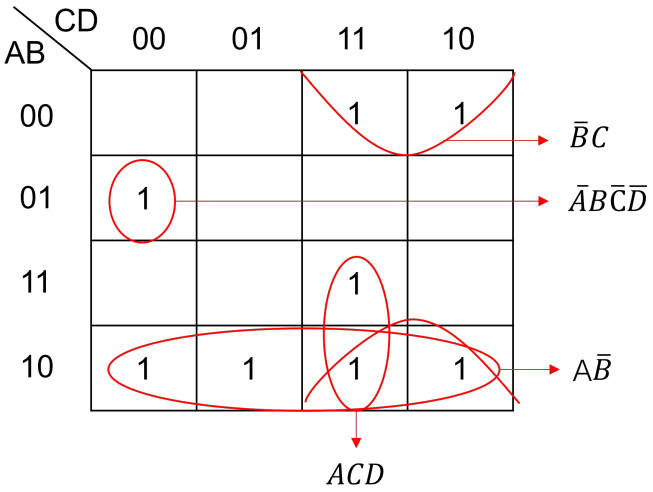

Figure 8: The K-map from the truth table.

The minimized SOP form is:

$$X = ACD + A\bar{B} + \bar{B}C + \bar{A}B\bar{C}\bar{D}$$

The logic circuit implemented is shown in Fig. 9.

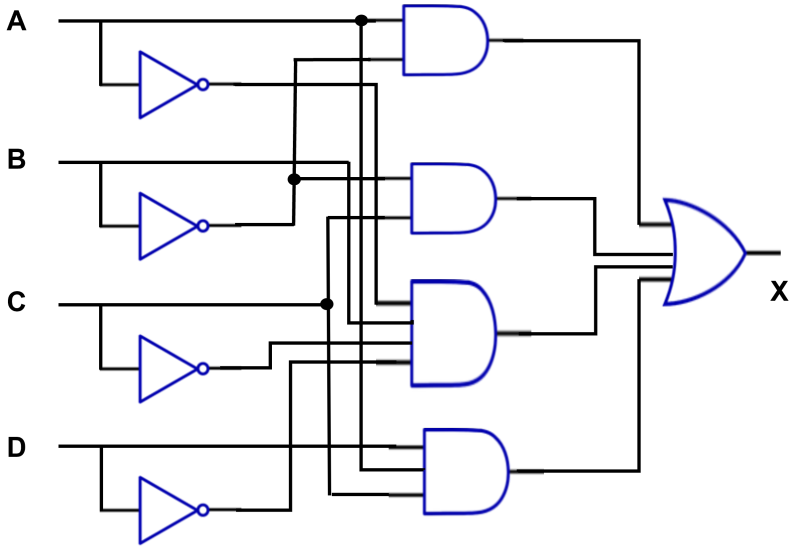

Figure 9: The logic circuit implementation.

(2) The logic function implemented by a 74HC151 is shown in Figure 10.

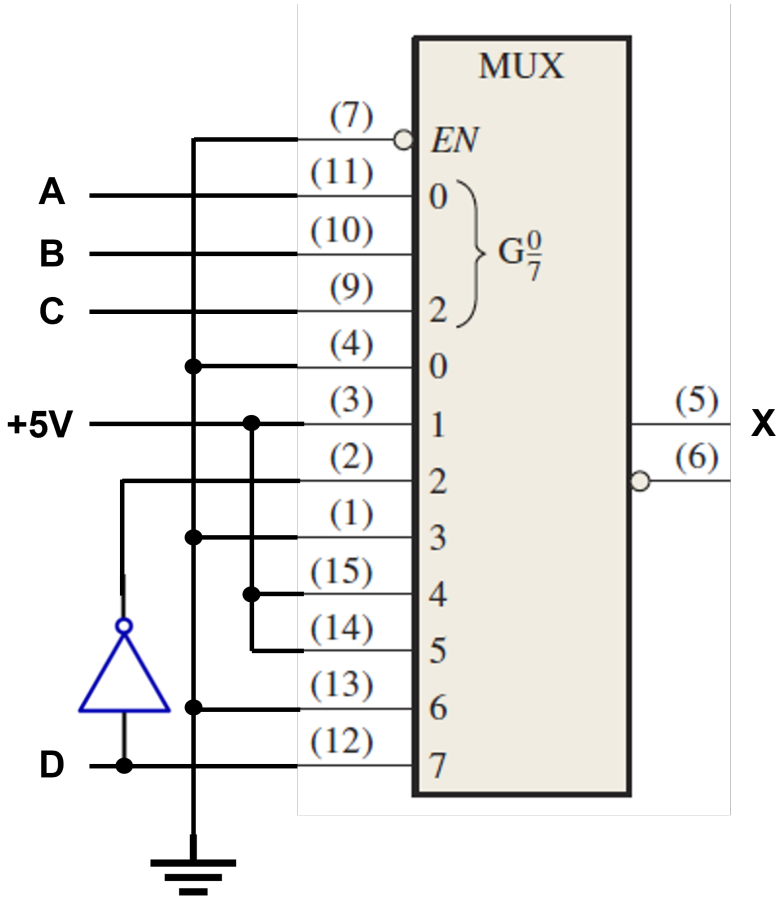

Figure 10: The 74HC151 implemented logic function.

7. (13 points)

(1) (2 points) For the parallel adder in Fig. 11, determine the complete sum by analyzing the operation of the circuit.

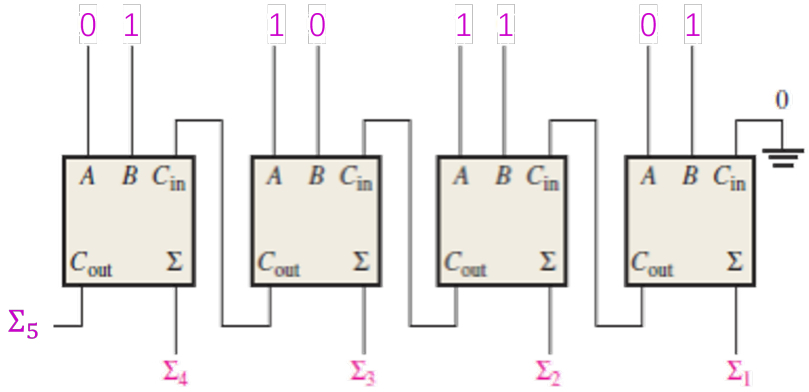

Figure 11: The 4-bit ripple carry adder.

(2) Assume $A = A_1A_0$ and $B = B_1B_0$, and C_0 denotes the initial carry input. If implement the 2-bit addition using the look-ahead carry adder: Firstly, please give the expressions of the carry generation (G_1 and G_0, respectively), carry propagation (P_1 and P_0, respectively) and the carry output (C_1 and C_2, respectively) for each stage (6 points), and draw the logic diagrams inside the block 1 and block 2 of Fig. 12 to show the inside logic circuits using necessary logic gates (5 points).

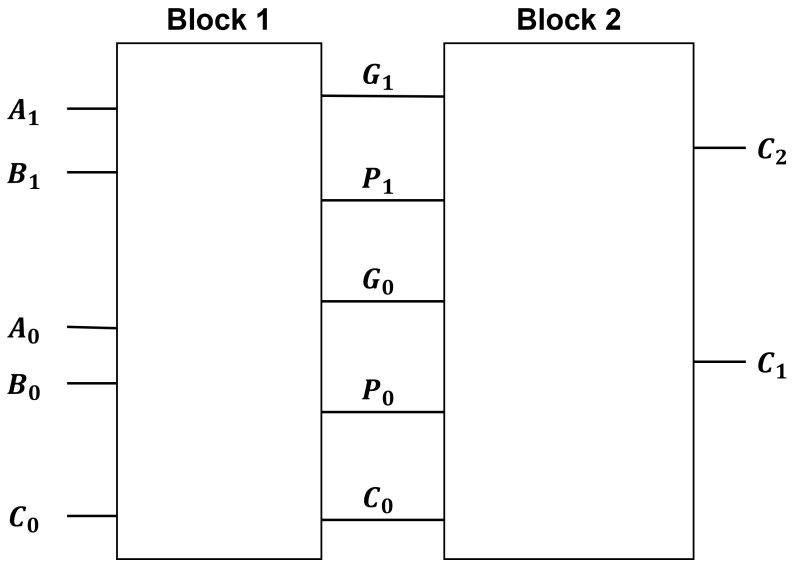

Figure 12: Carry prediction circuits of the 2-bit Look-ahead carry adder.

Solution:

(1) The complete sum is $\Sigma = \Sigma_5\Sigma_4\Sigma_3\Sigma_2\Sigma_1 = 10001$.

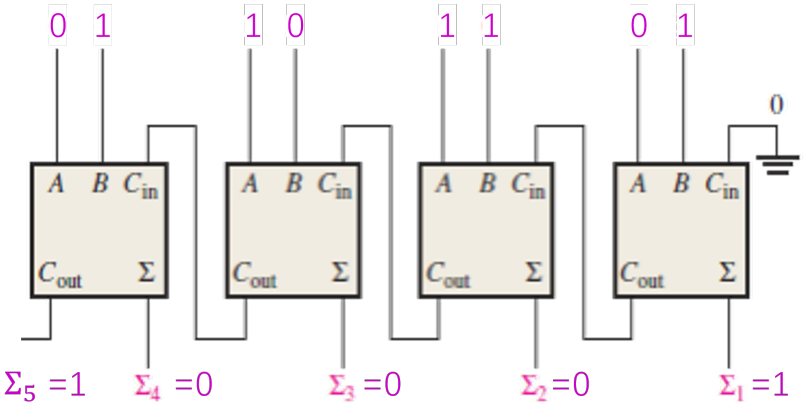

Figure 13: The addition of two 4-bit numbers using ripple carry adder.

(2) The equations and the logic diagrams are shown below (Note: Both "OR" and "XOR" gates can be used to calculate the carry propagation.):

$$
\begin{aligned}
G_0 &= A_0 B_0 \\
P_0 &= A_0 + B_0 \\
C_1 &= G_0 + P_0 C_0 \\
G_1 &= A_1 B_1 \\
P_1 &= A_1 + B_1 \\
C_2 &= G_1 + P_1 C_1 = G_1 + P_1 (G_0 + P_0 C_0) = G_1 + P_1 G_0 + P_1 P_0 C_0
\end{aligned}
$$

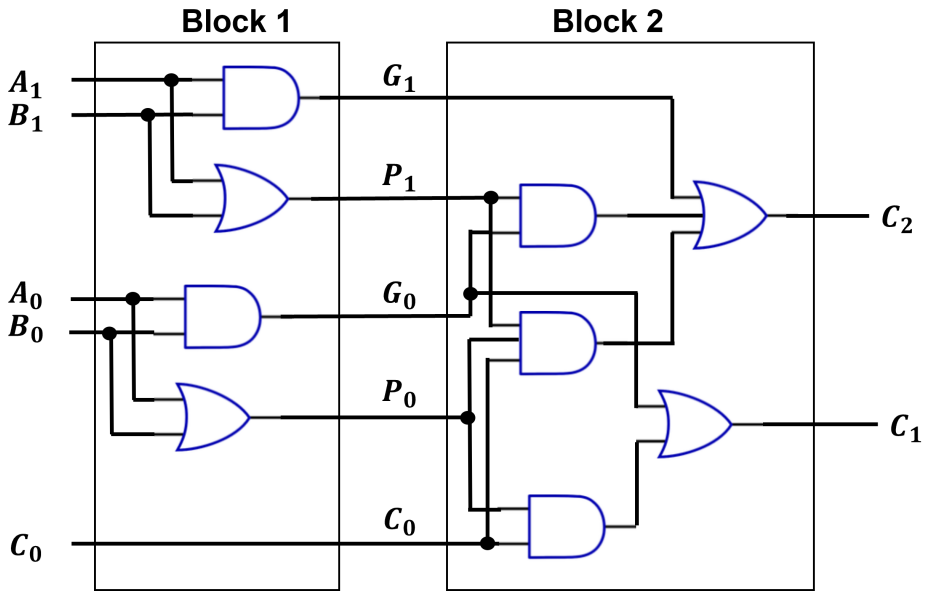

Figure 14: Carry prediction circuits of the 2-bit Look-ahead carry adder.

CONTINUED

8. (10 points) Develop a logic circuit with **BCD** inputs that will only produce a 1 output when exactly 2 input variables are 1s.

(1) Please develop the truth table for the above circuit.

(2) Please use K-map to derive the minimized SOP expression for the circuit.

Solution:

(1) The truth table for the circuit is:

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	X
1	0	1	1	X
1	1	0	0	X
1	1	0	1	X
1	1	1	0	X
1	1	1	1	X

(2) $X = AB + AC + AD + BC\bar{D} + B\bar{C}D + \bar{B}CD$

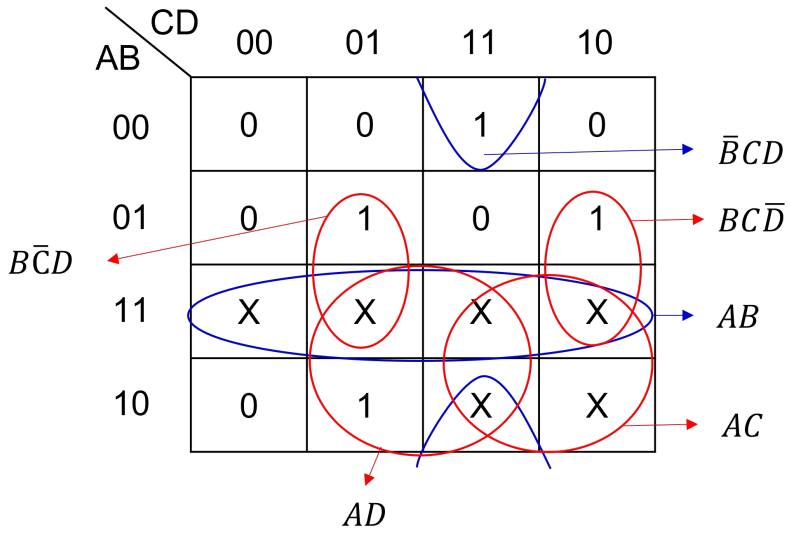

Figure 15: Solution for Q.8.