ECE 2050 Digital Logic and Systems

Chapter 10 : Counters

Instructor: Tinghuan CHEN, Ph.D.

香港中文大學（深圳）
The Chinese University of Hong Kong, Shenzhen

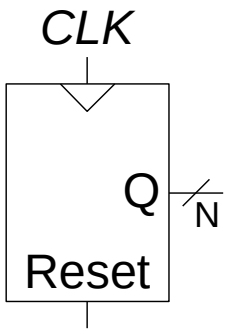
Last Week

- (Synchronous) Sequential Logic Counters
- Finite State Machine
  - Moore FSM
  - Mealy FSM
- Timing
  - Setup time
  - Hold time
  - Aperture time
  - Propagation delay
  - Contamination delay
  - Dynamic Discipline

Counters

- Increments on each clock edge
- Used to cycle through numbers. For example,
  - 000, 001, 010, 011, 100, 101, 110, 111, 000, 001…
- **Example uses:**
  - Digital clock displays
  - Program counter: keeps track of current instruction executing

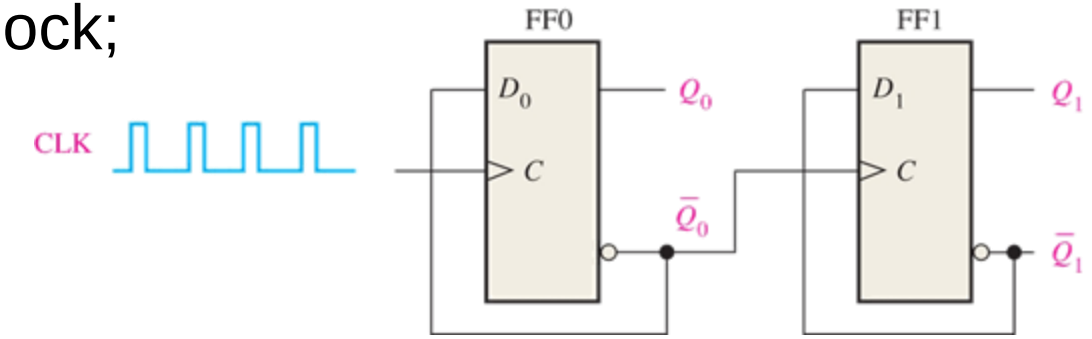
Symbol **Implementation**



Asynchronous Counters

Asynchronous Counters

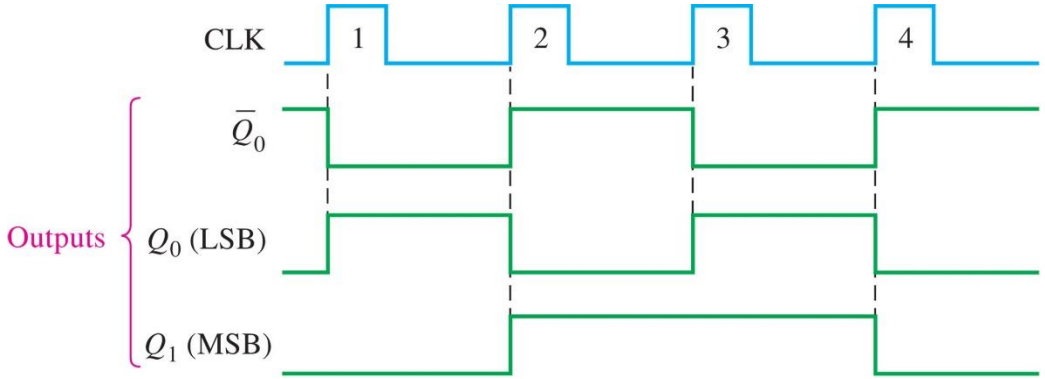
- An asynchronous counter is one in which the flip-flops (FF) within the counter do not have a common clock;



- The 2-bit asynchronous counter counts # of clock pulses up to 3, and on the 4th pulse, it recycles to its original state ($Q_0 = Q_1 = 0$).

Binary state sequence for the counter in Figure 9–4.

Clock Pulse	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0



A 3-Bit Asynchronous Binary Counter

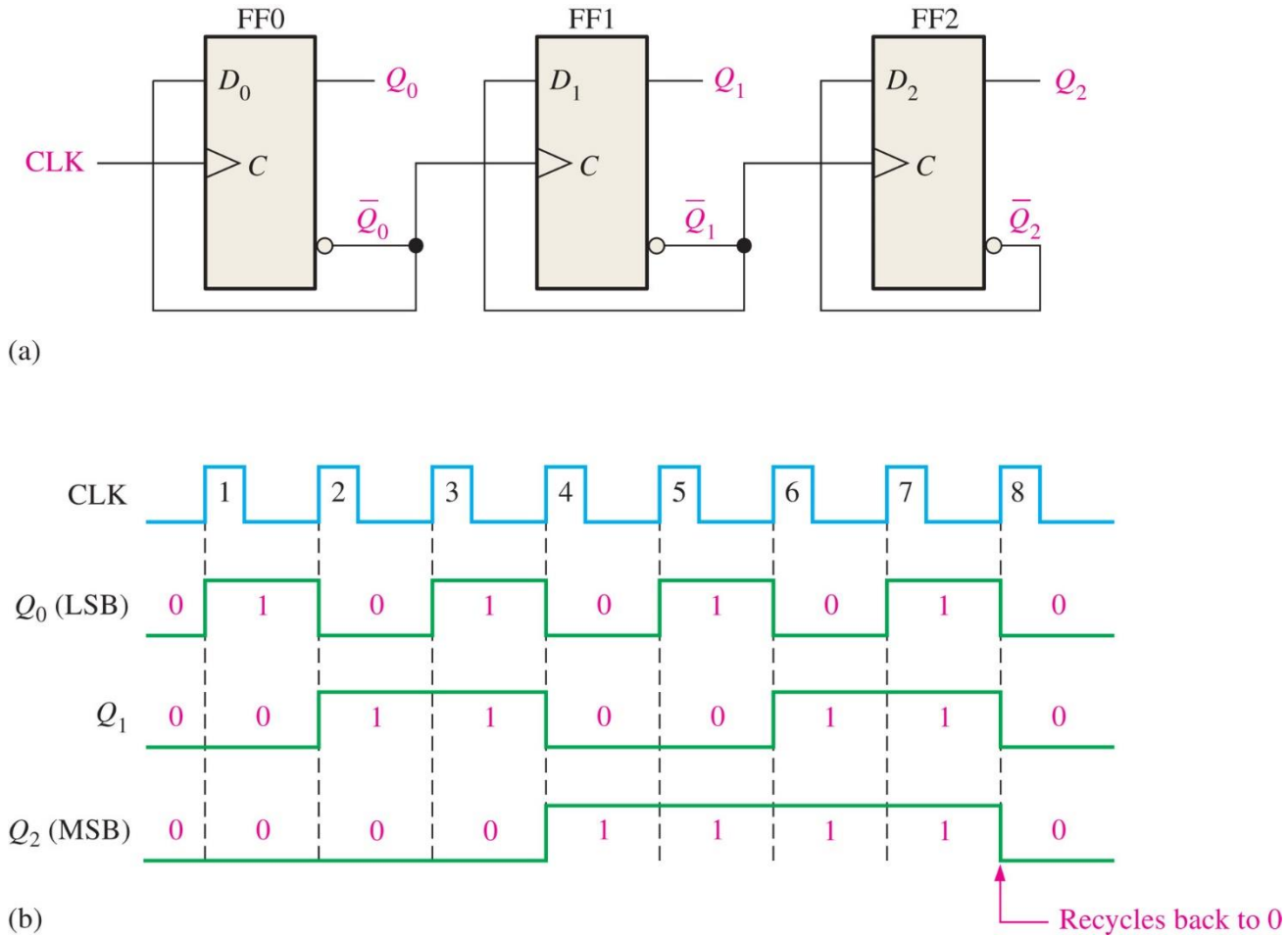


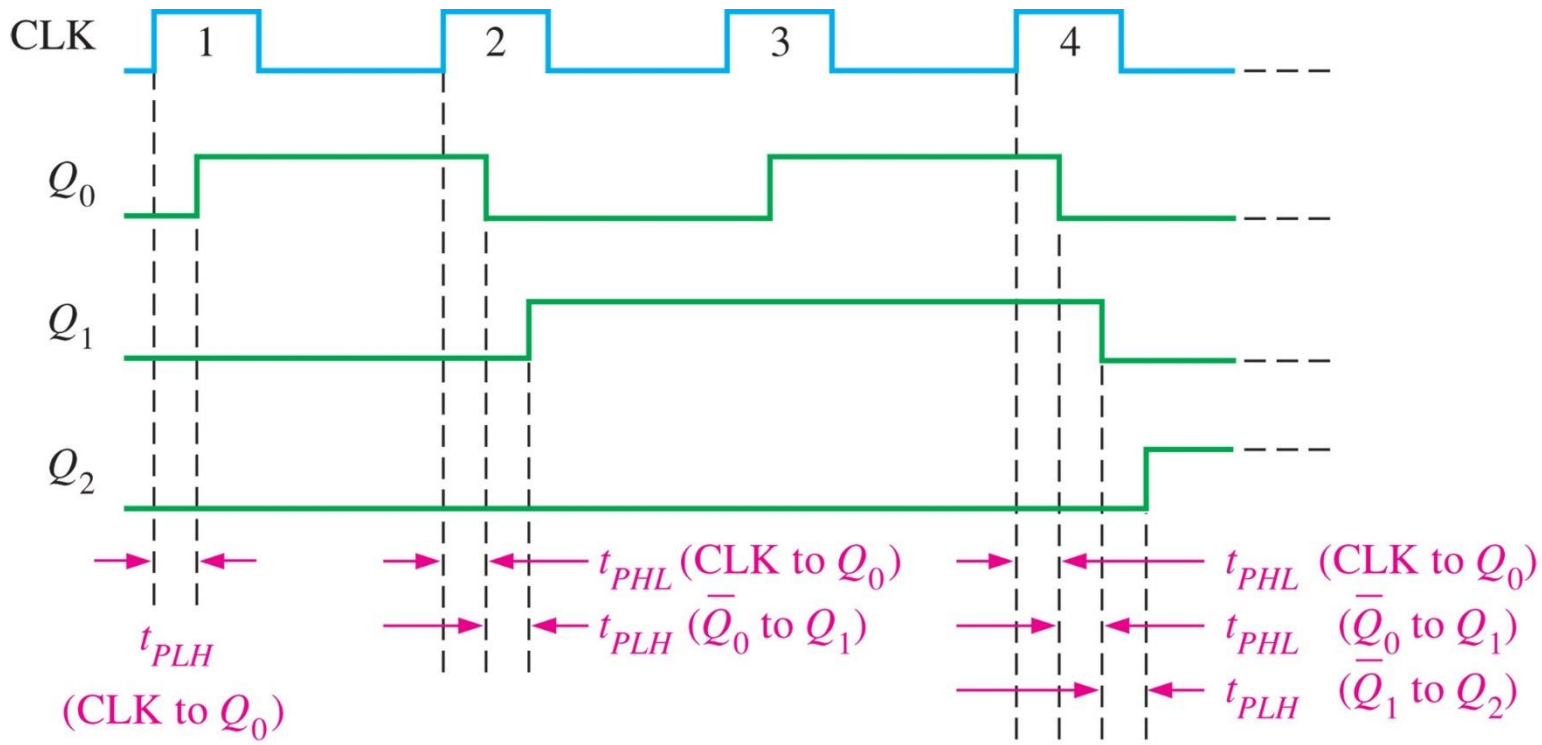
TABLE 9–2

State sequence for a 3-bit binary counter.

Clock Pulse	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

- Commonly referred to as ripple counters;
- The cumulative delay of asynchronous counters is a major drawback.

Propagation Delay



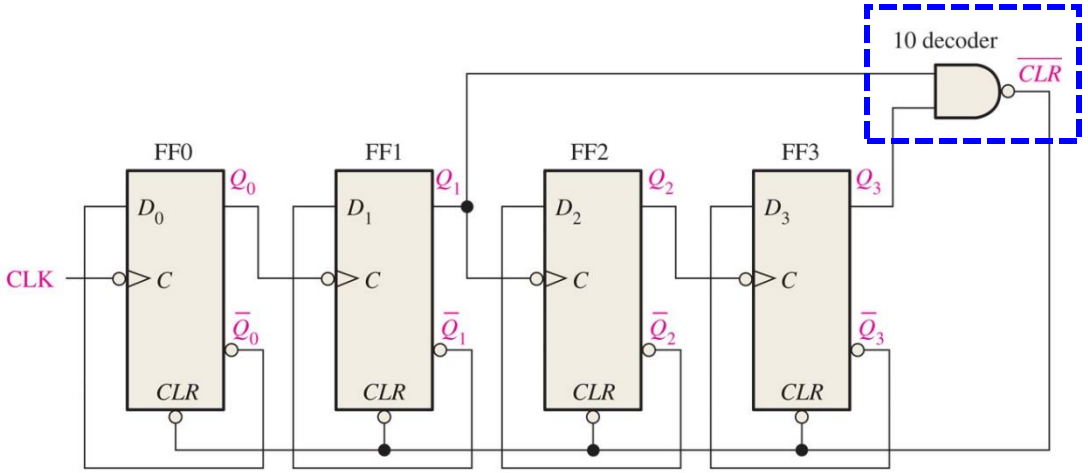
- If each D flip-flop has a propagation delay for t second, then
- The total delay time: $t_{p(tot)}$ = t * # of D flip-flops
- The maximum clock frequency: $f_{max}=1/ t_{p(tot)}$

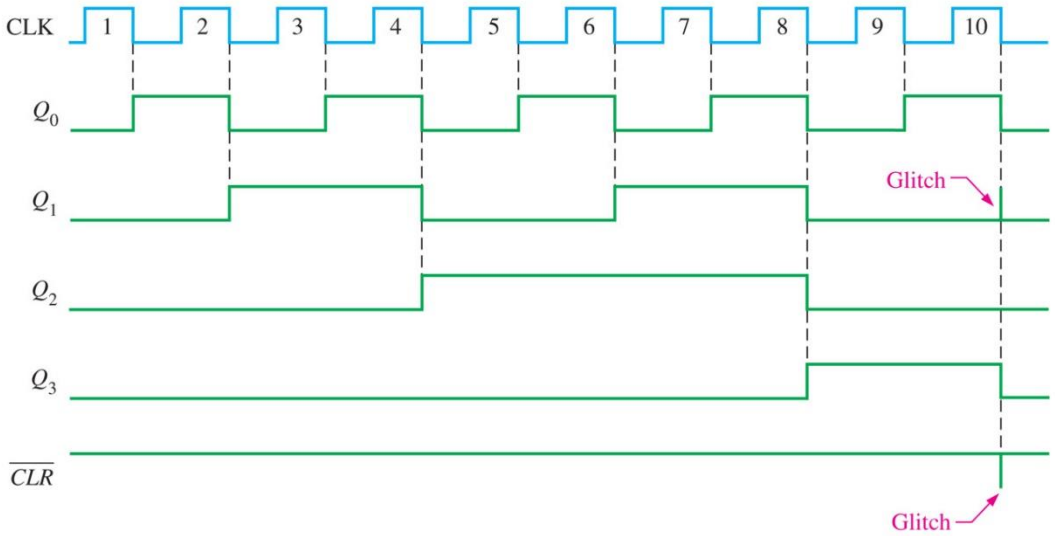
Asynchronous Decade Counters

- Modulus: # of unique states through which the counter will sequence.
- Maximum modulus: 2^n for a counter of n flip-flops.
- Counters can have less than 2^n states, called a truncated sequence.
- Example: A decade counter with four flip-flops counts a truncated sequence from 0000 through 1001

1010↔0000

Glitch: the counter is in the 1010 state for a short time before it is reset to 0000

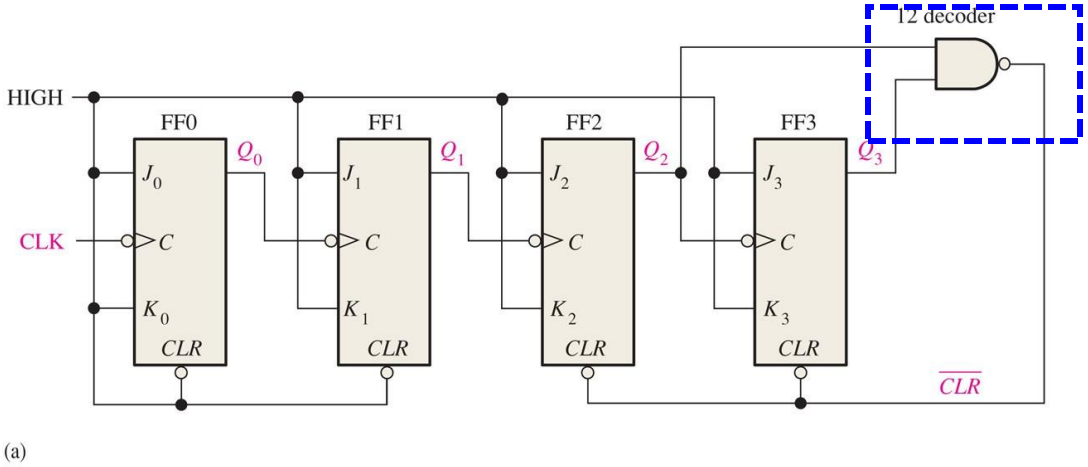




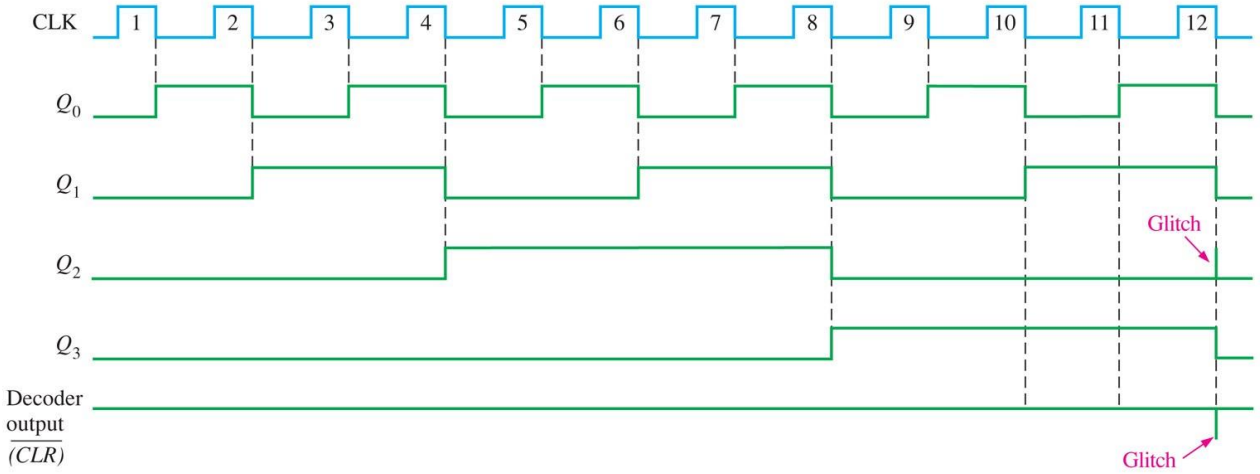
Example 9–2 with J-K Flip-Flops

- J and K inputs are both HIGH → Flip-flops toggle between S/R states

1100↔0000



(a)

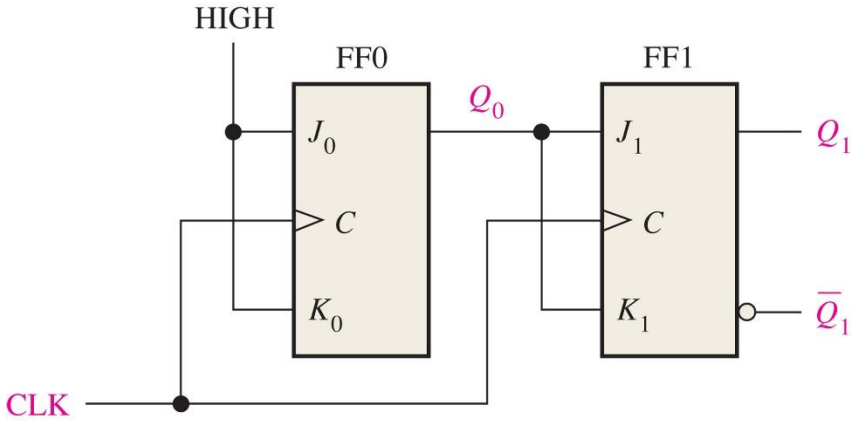


(b)

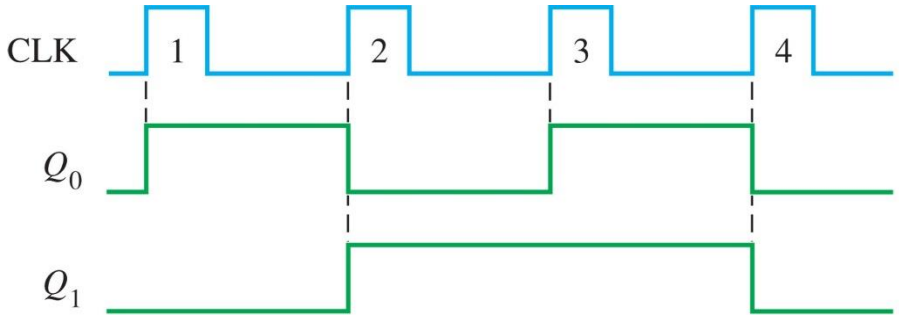
Synchronous Counters

Synchronous Counters

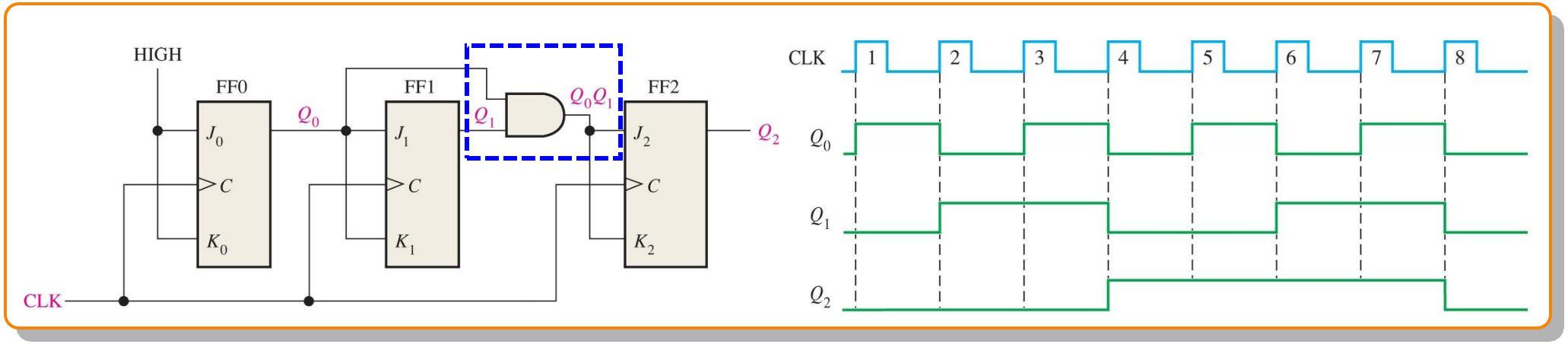
- Synchronous: All flip-flops are controlled by the same clock
- Both J and K inputs are connected to HIGH
- Example: A synchronous counter with two flip-flops counts a sequence from 00 through 11 in four clock pulses



(a) J-K flip-flop



A 3-Bit Synchronous Binary Counter

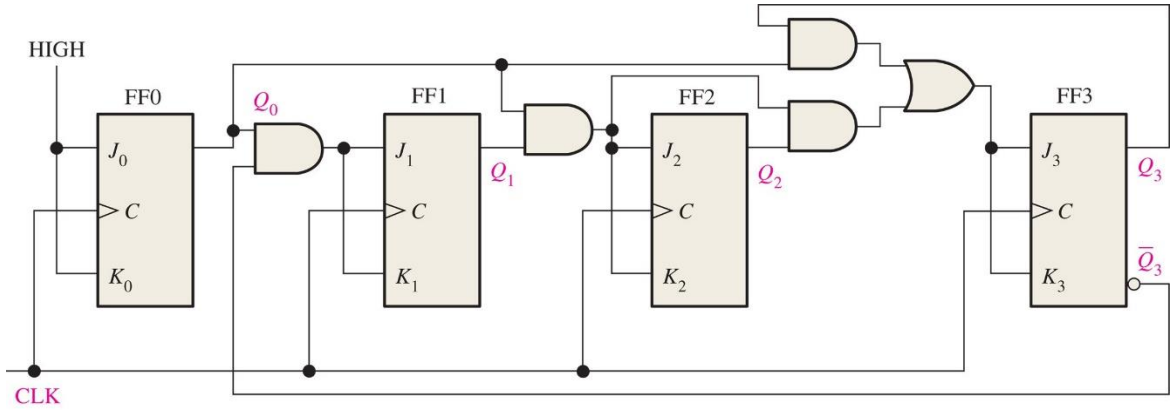


Summary of the analysis of the counter in Figure 9–15.

Clock Pulse	Outputs Q_2	Q_1	Q_0	*J-K* Inputs J_2	K_2	J_1	K_1	J_0	K_0	At the Next Clock Pulse FF2	FF1	FF0
Initially	0	0	0	0	0	0	0	1	1	NC*	NC	Toggle
1	0	0	1	0	0	1	1	1	1	NC	Toggle	Toggle
2	0	1	0	0	0	0	0	1	1	NC	NC	Toggle
3	0	1	1	1	1	1	1	1	1	Toggle	Toggle	Toggle
4	1	0	0	0	0	0	0	1	1	NC	NC	Toggle
5	1	0	1	0	0	1	1	1	1	NC	Toggle	Toggle
6	1	1	0	0	0	0	0	1	1	NC	NC	Toggle
7	1	1	1	1	1	1	1	1	1	Toggle	Toggle	Toggle
										Counter recycles back to 000.		

NC: No Change

A 4-Bit Synchronous Decade Counter



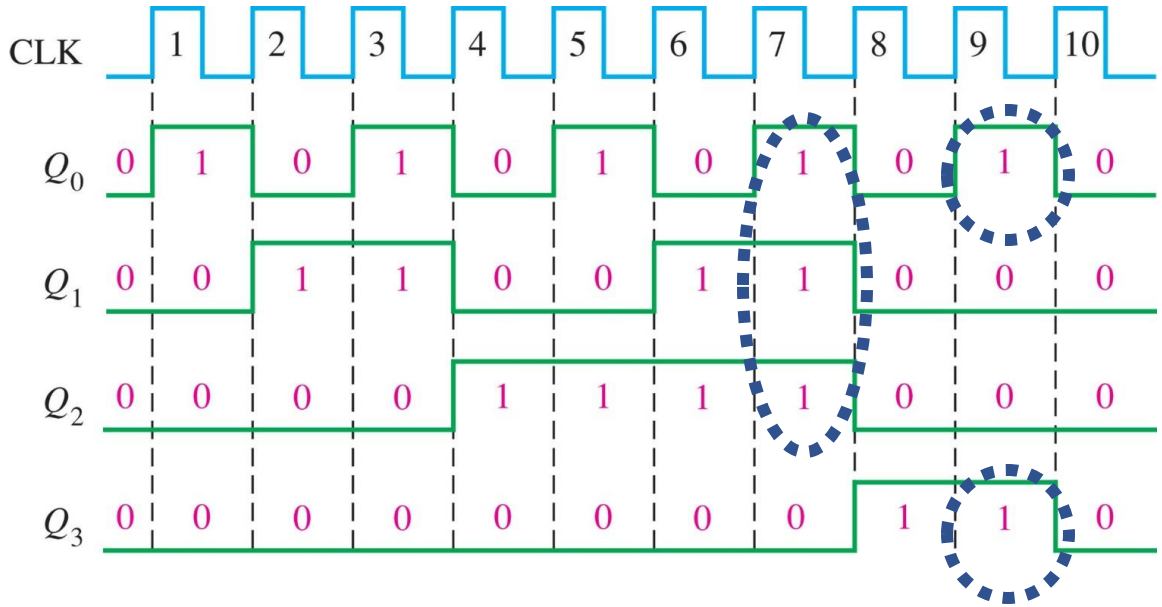


TABLE 9–5

States of a BCD decade counter.

Clock Pulse	Q_3	Q_2	Q_1	Q_0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

$$J_1 = K_1 = Q_0\bar{Q}_3$$

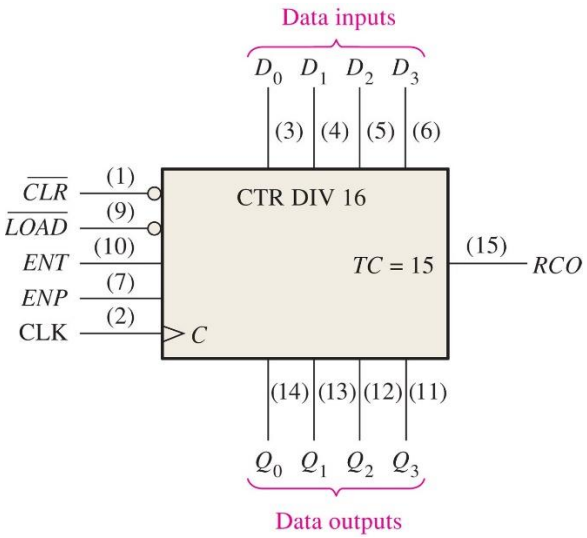
$$J_2 = K_2 = Q_0Q_1$$

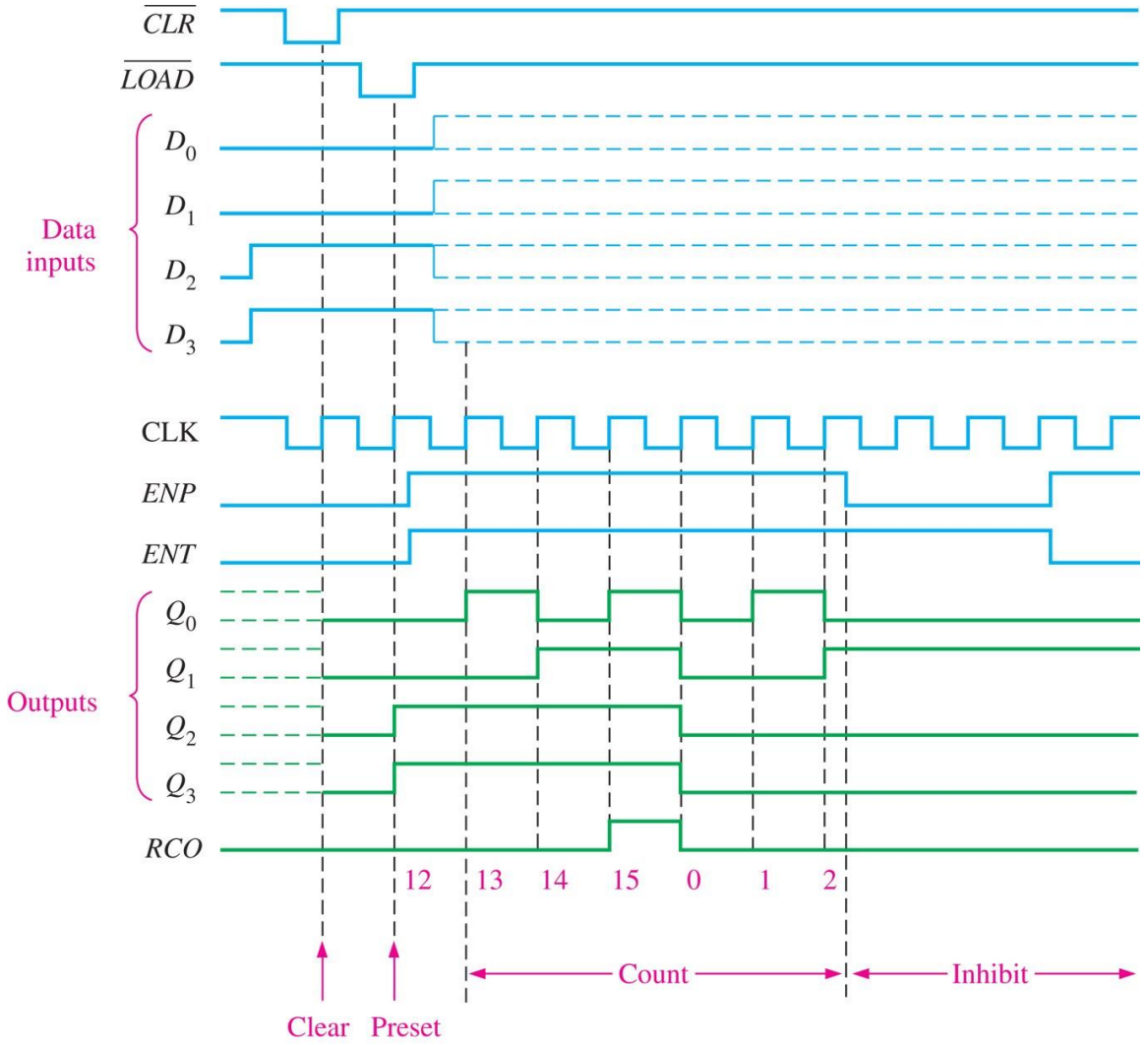
$$J_3 = K_3 = Q_0Q_1Q_2 + Q_0Q_3$$

The derivation of the expressions above will be discussed in detail later.

4-Bit Synchronous Binary Counter

74HC163 4-bit synchronous binary counter.





- When LOAD is $\overline{\text{LOW}}$, the counter will load $D_3D_2D_1D_0$ on the next clock pulse → the counter sequence can be started with any 4-bit binary number.
- The ripple clock output (RCO) goes HIGH when the counter reaches the last state in its sequence of fifteen, called the terminal count (TC = 15).
- 2 enable inputs, *ENP* and *ENT*, must both be HIGH for the CTR to sequence through its binary states

Up/Down Synchronous Counters

Up/Down Synchronous Counters

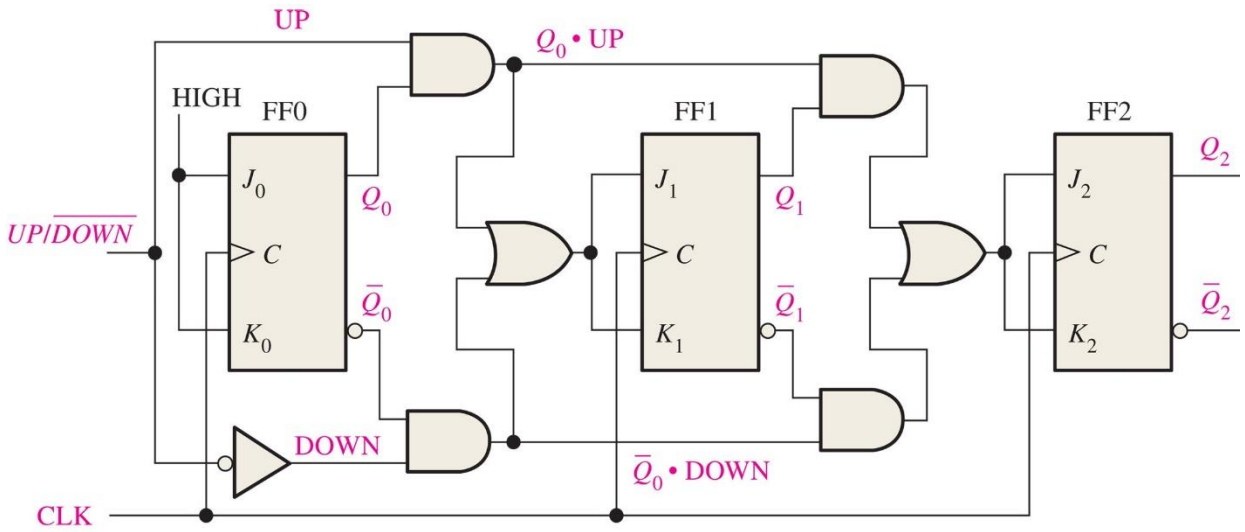
Up/Down sequence for a 3-bit binary counter.

Clock Pulse	Up	Q_2	Q_1	Q_0	Down
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

$$J_0 = K_0 = 1$$

$$J_1 = K_1 = (Q_0 \cdot \mathrm{UP}) + (\bar{Q}_0 \cdot \mathrm{DOWN})$$

$$J_2 = K_2 = (Q_0 \cdot Q_1 \cdot \mathrm{UP}) + (\bar{Q}_0 \cdot \bar{Q}_1 \cdot \mathrm{DOWN})$$



Again, the derivation of the expressions above will be discussed in detail later.

- Also known as the bidirectional counter that can progress in either direction
- In general, an UP/Down counter can be reversed at any point in its sequence

Up/Down Synchronous Counters

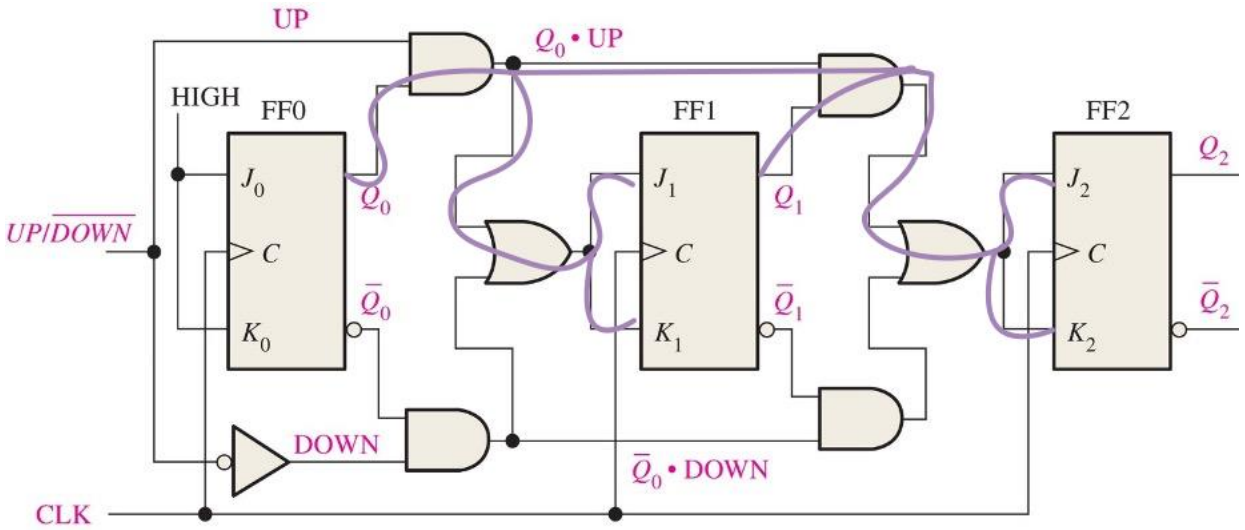
Up/Down sequence for a 3-bit binary counter.

Clock Pulse	Up	Q_2	Q_1	Q_0	Down
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

$$J_0 = K_0 = 1$$

$$J_1 = K_1 = (Q_0 \cdot \text{UP}) + (\bar{Q}_0 \cdot \text{DOWN})$$

$$J_2 = K_2 = (Q_0 \cdot Q_1 \cdot \text{UP}) + (\bar{Q}_0 \cdot \bar{Q}_1 \cdot \text{DOWN})$$



Again, the derivation of the expressions above will be discussed in detail later.

- Also known as the bidirectional counter that can progress in either direction
- In general, an UP/Down counter can be reversed at any point in its sequence

Up/Down Synchronous Counters

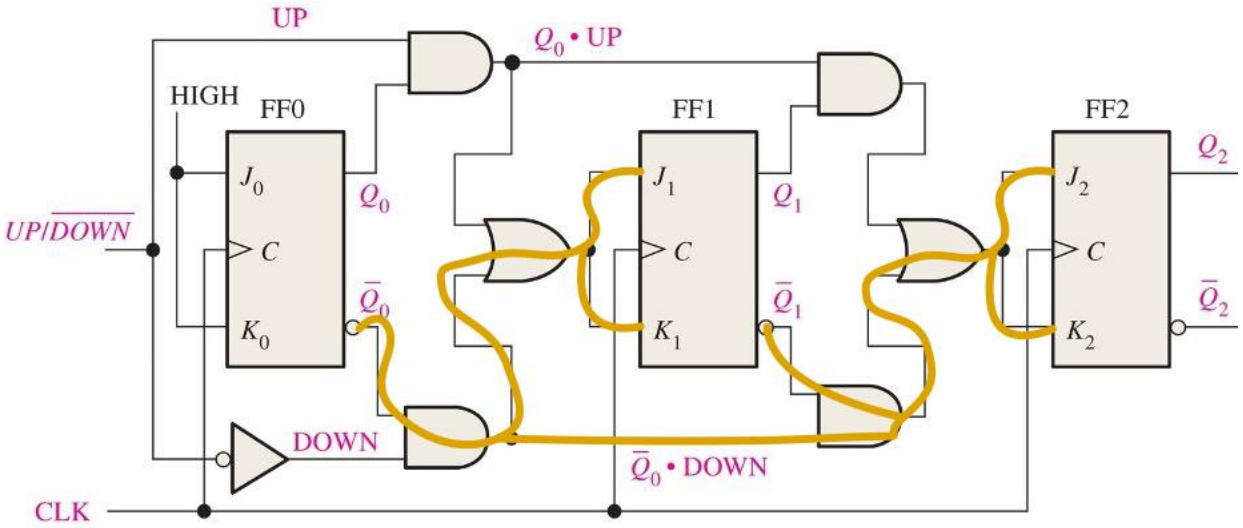
Up/Down sequence for a 3-bit binary counter.

Clock Pulse	Up	Q_2	Q_1	Q_0	Down
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	

$$J_0 = K_0 = 1$$

$$J_1 = K_1 = (Q_0 \cdot \mathrm{UP}) + (\bar{Q}_0 \cdot \mathrm{DOWN})$$

$$J_2 = K_2 = (Q_0 \cdot Q_1 \cdot \mathrm{UP}) + (\bar{Q}_0 \cdot \bar{Q}_1 \cdot \mathrm{DOWN})$$

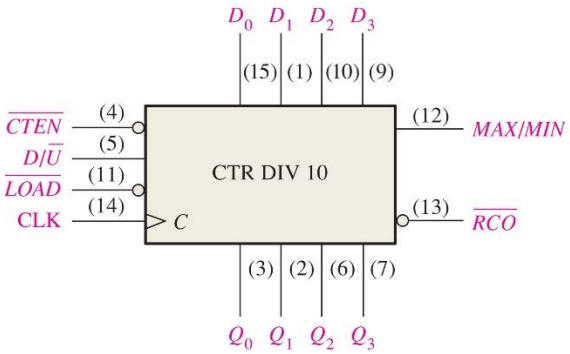


Again, the derivation of the expressions above will be discussed in detail later.

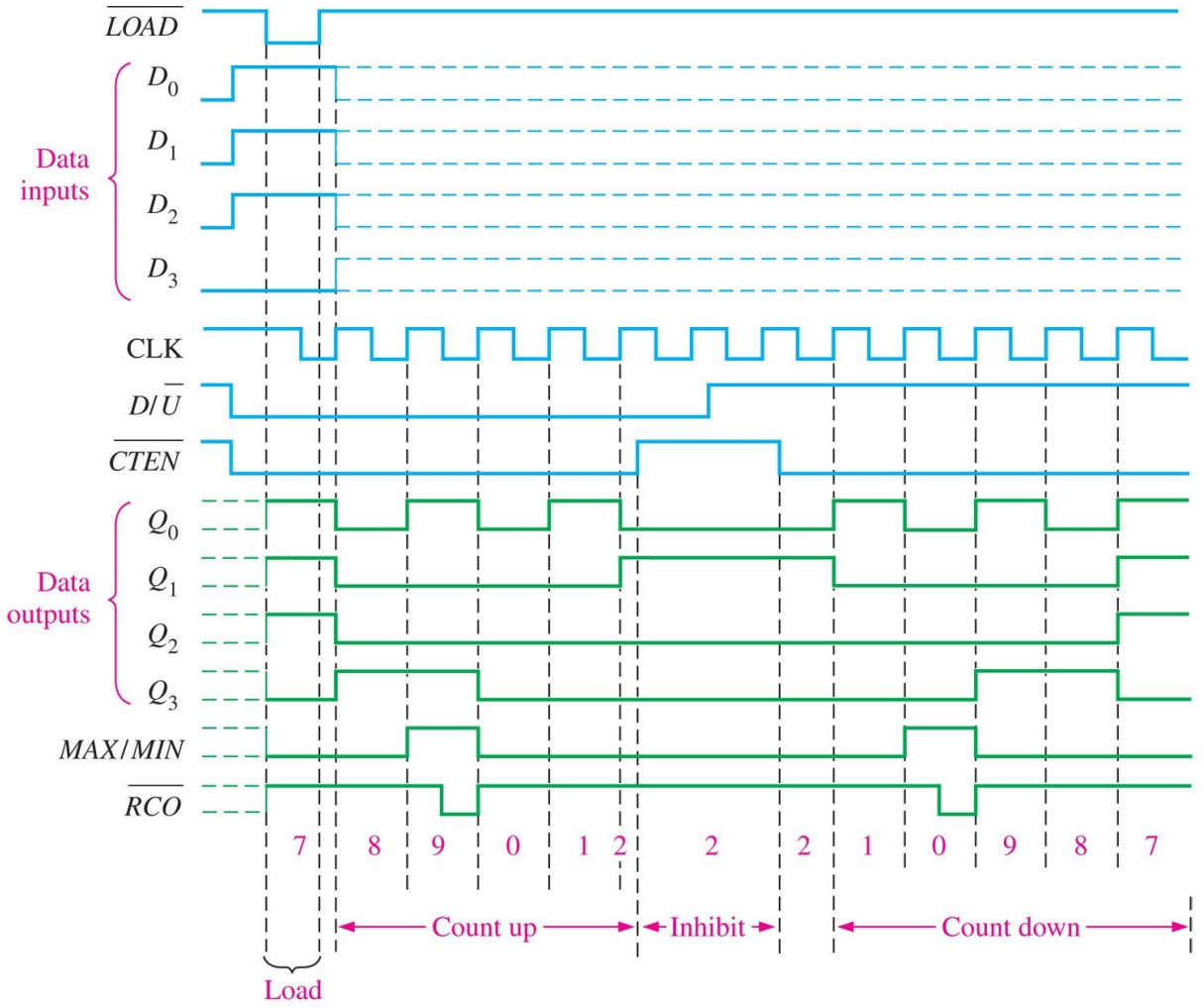
- Also known as the bidirectional counter that can progress in either direction
- In general, an UP/Down counter can be reversed at any point in its sequence

Example

- The direction of the count is determined by the level of the up/down input (D/$\overline{U}$). When this input is HIGH, the counter counts down; when it is LOW, the counter counts up.



74HC190 : a U/D synchronous decade counter



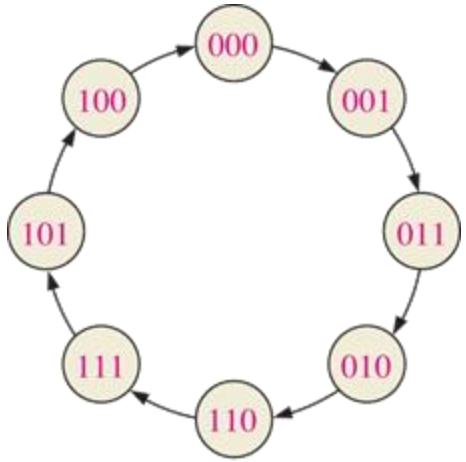
Design of Synchronous Counters

Design of Synchronous Counters (I)

- Step 1: State Diagram
- Step 2: Next-State Table
- Step 3: Flip-Flop Transition Table
- Step 4: Karnaugh Maps
- Step 5: Logic Expressions for Flip-Flop Inputs
- Step 6: Counter Implementation

Example

- Step 1: State Diagram



Next-state table for 3-bit Gray code counter.

Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

- Step 2: Next-State Table

Transition table for a J-K flip-flop.

Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

- Step 3: Flip-Flop Transition Table

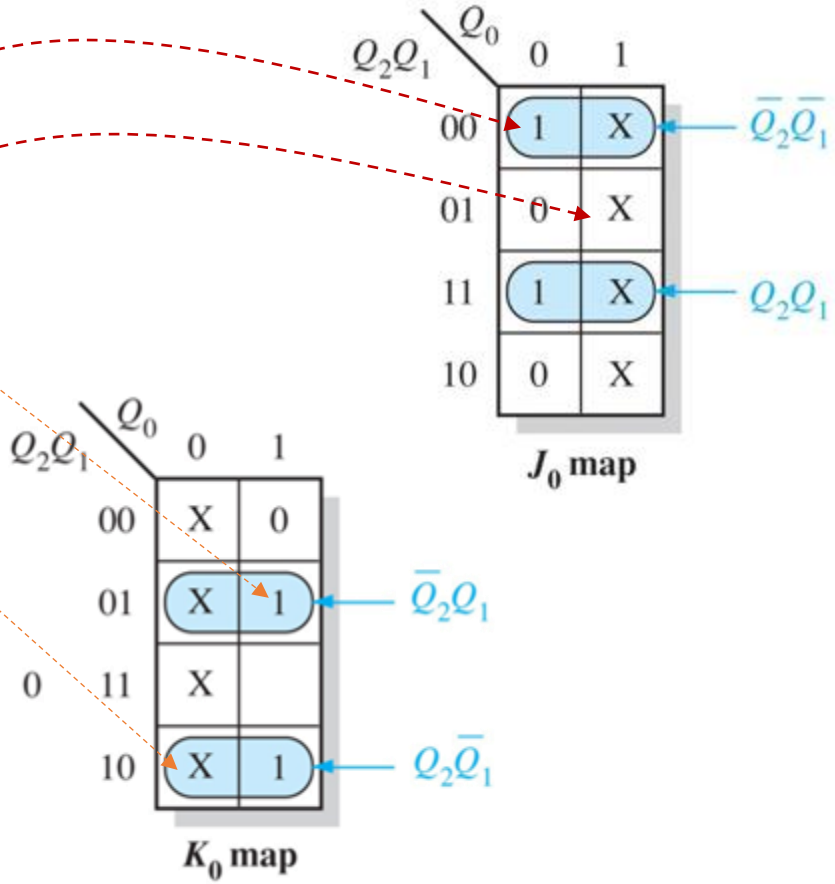
Example: Cont'd

- Step 4: Karnaugh Maps

Next-state table for 3-bit Gray code counter.

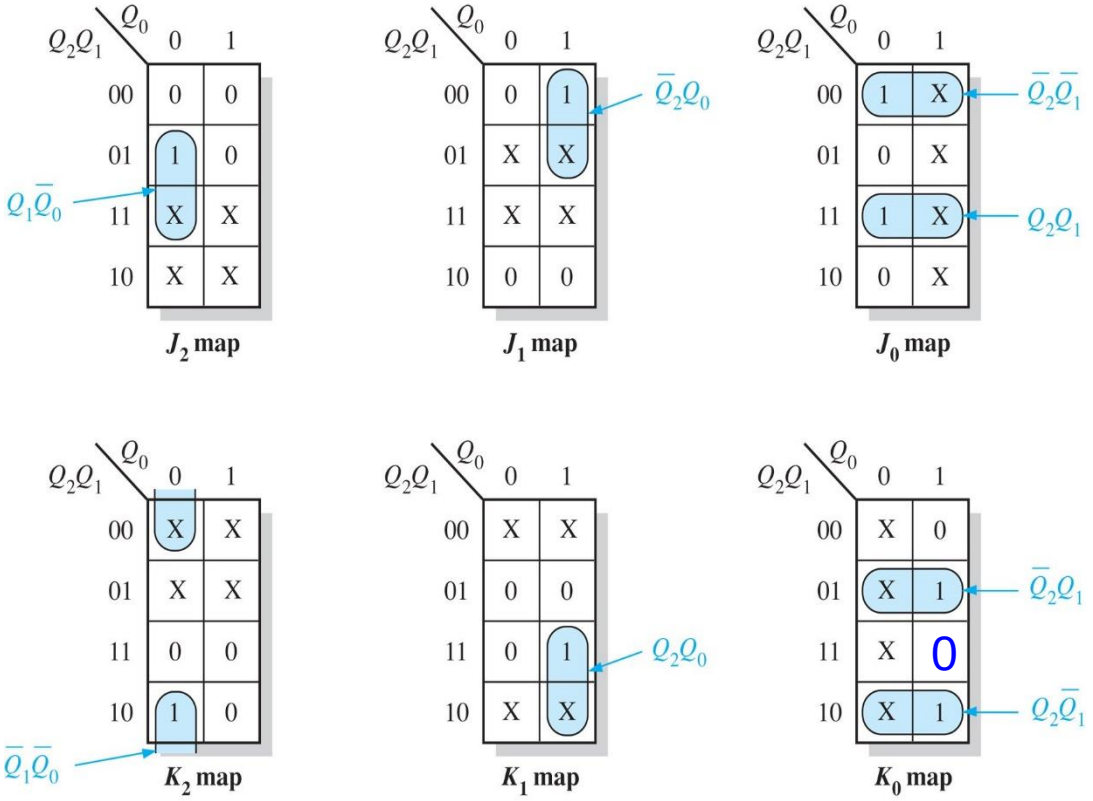
Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

J_0	K_0
1	x
x	0
x	1
0	x
1	x
x	0
x	1
0	x



Example: Cont'd

- Step 5: Logic Expressions for Flip-Flop Inputs

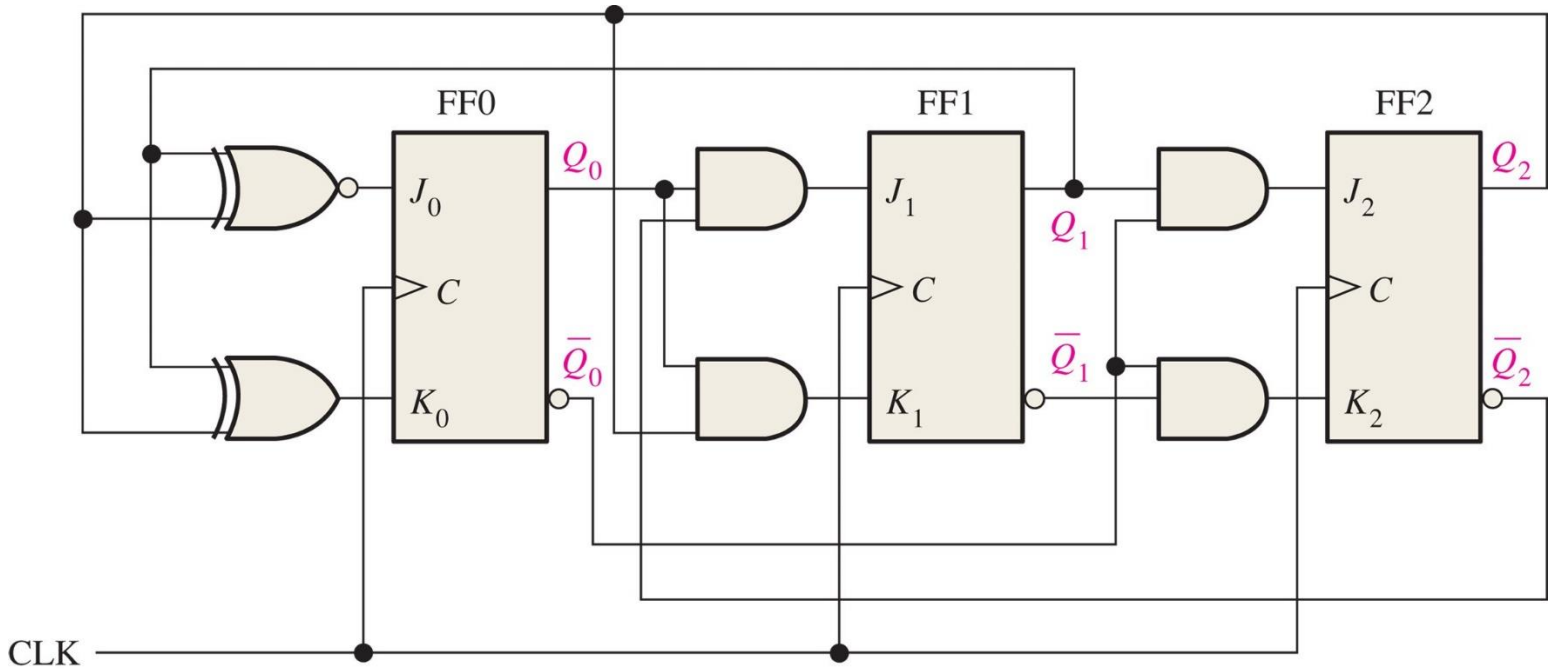


$$J_0 = Q_2Q_1 + \bar{Q}_2\bar{Q}_1 = \overline{Q_2 \oplus Q_1}$$
$$K_0 = Q_2\bar{Q}_1 + \bar{Q}_2Q_1 = Q_2 \oplus Q_1$$
$$J_1 = \bar{Q}_2Q_0$$
$$K_1 = Q_2Q_0$$
$$J_2 = Q_1\bar{Q}_0$$
$$K_2 = \bar{Q}_1\bar{Q}_0$$

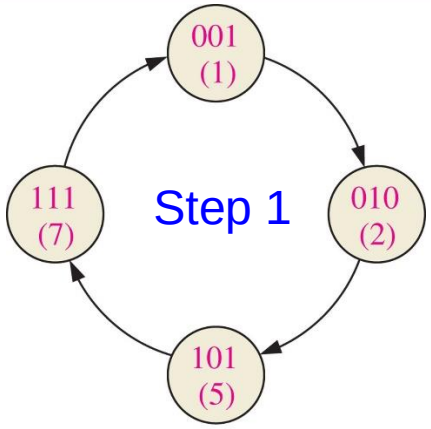
Example: Cont'd

- Step 6: Counter Implementation

$$J_0 = Q_2Q_1 + \bar{Q}_2\bar{Q}_1 = \overline{Q_2 \oplus Q_1}$$
$$K_0 = Q_2\bar{Q}_1 + \bar{Q}_2Q_1 = Q_2 \oplus Q_1$$
$$J_1 = \bar{Q}_2Q_0$$
$$K_1 = Q_2Q_0$$
$$J_2 = Q_1\bar{Q}_0$$
$$K_2 = \bar{Q}_1\bar{Q}_0$$



More Example



Step 2

Next-state table.

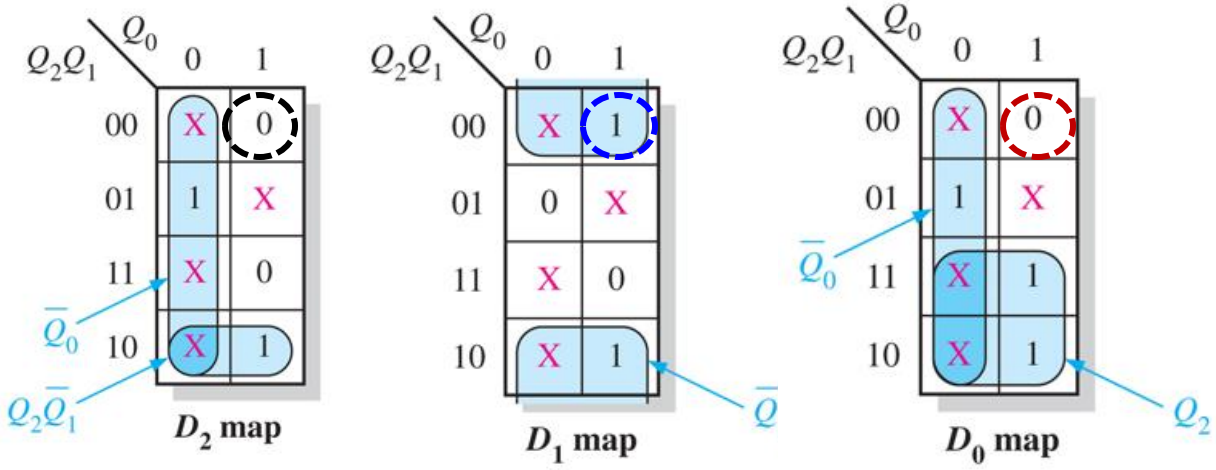
Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	1	0	1	0
0	1	0	1	0	1
1	0	1	1	1	1
1	1	1	0	0	1

Step 3

Transition table for a D flip-flop.

Output Transitions			Flip-Flop Input
Q_N		Q_{N+1}	D
0	⟶	0	0
0	⟶	1	1
1	⟶	0	0
1	⟶	1	1

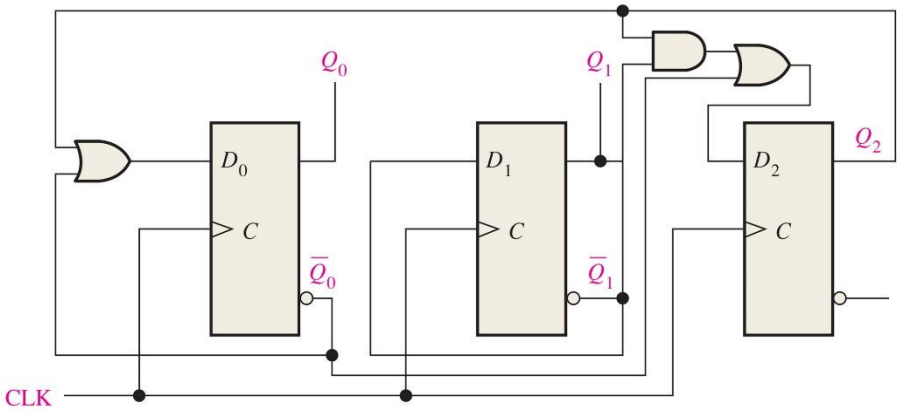
Step 4



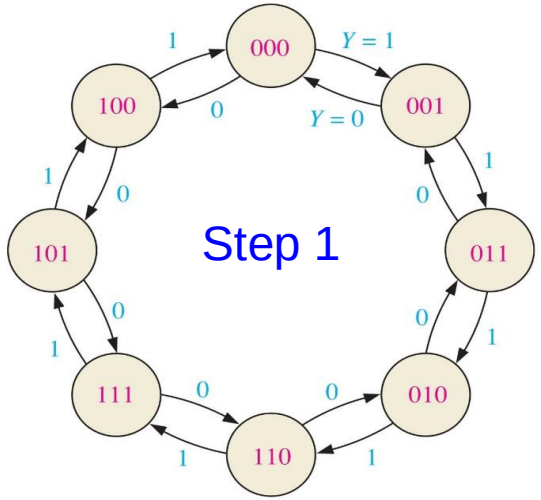
Step 5

$$D_0 = \bar{Q}_0 + Q_2$$
$$D_1 = \bar{Q}_1$$
$$D_2 = \bar{Q}_0 + Q_2\bar{Q}_1$$

Step 6



Example: Synchronous 3-bit U/D Counters



Step 3

Transition table for a J-K flip-flop.

Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

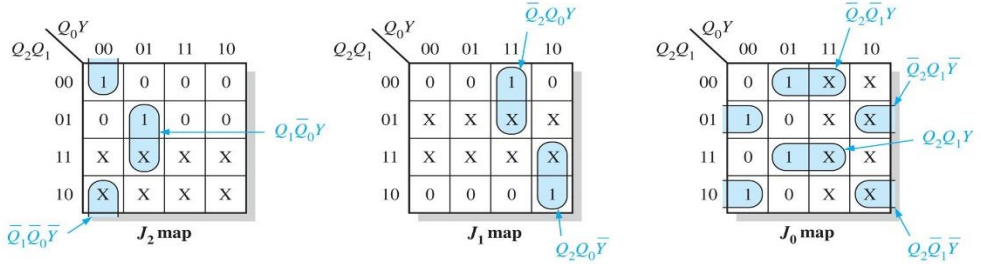
Q_N: present state
Q_{N+1}: next state
X: "don't care"

Step 2

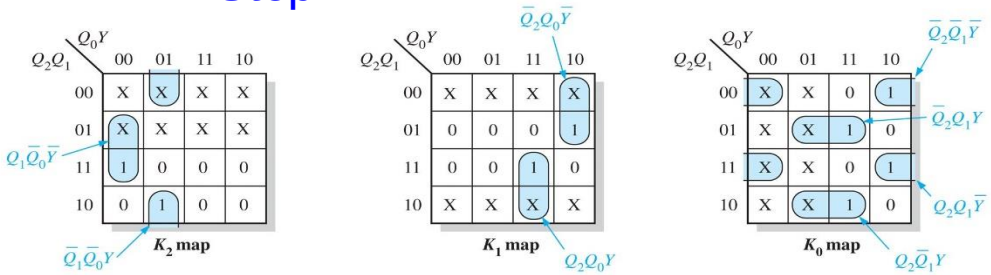
Next-state table for 3-bit up/down Gray code counter.

Present State			Next State $Y = 0$ (DOWN)			Next State $Y = 1$ (UP)		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

Y = UP/$\overline{\text{DOWN}}$ control input.



Step 4



- The counter should count up when UP/DOWN is 1 and count down when 0.

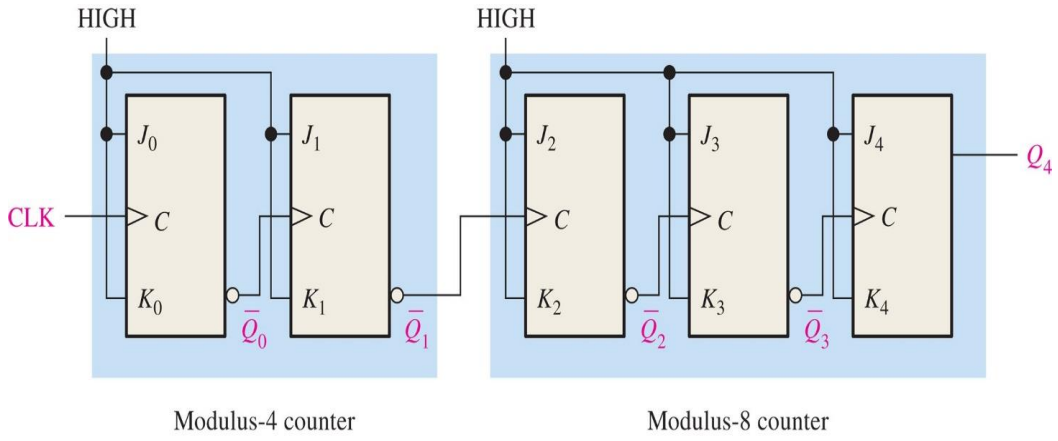
$$J_0 = Q_2Q_1Y + Q_2\bar{Q}_1\bar{Y} + \bar{Q}_2\bar{Q}_1Y + \bar{Q}_2Q_1\bar{Y}$$
$$J_1 = \bar{Q}_2Q_0Y + Q_2Q_0\bar{Y}$$
$$J_2 = Q_1\bar{Q}_0Y + \bar{Q}_1\bar{Q}_0\bar{Y}$$
$$K_0 = \bar{Q}_2\bar{Q}_1\bar{Y} + \bar{Q}_2Q_1Y + Q_2\bar{Q}_1Y + Q_2Q_1\bar{Y}$$
$$K_1 = \bar{Q}_2Q_0\bar{Y} + Q_2Q_0Y$$
$$K_2 = Q_1\bar{Q}_0\bar{Y} + \bar{Q}_1\bar{Q}_0Y$$

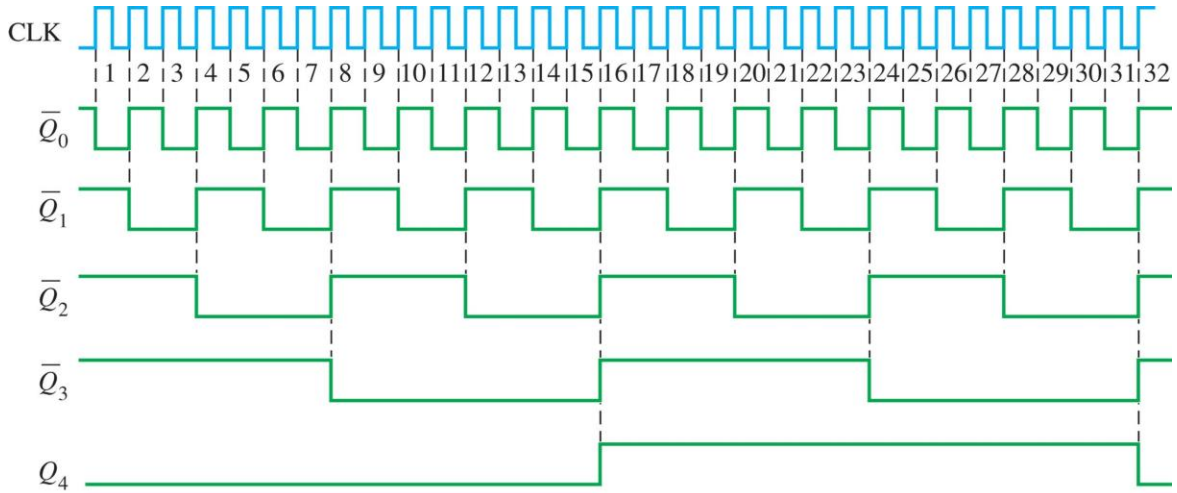
Step 5

Cascaded Counters

Cascaded Counters: Asynchronous

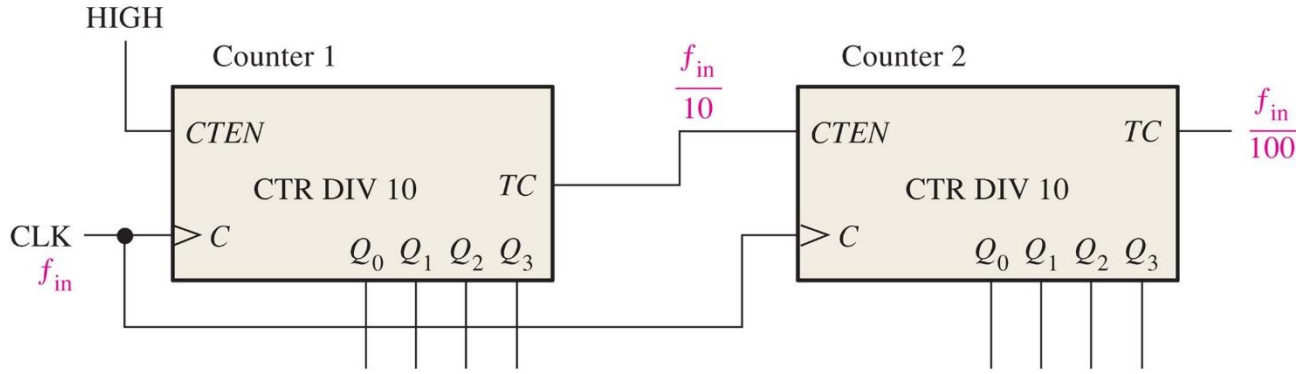
- The overall modulus of the two cascaded counters is 4 * 8 = 32; that is, they act as a divide-by-32 counter.



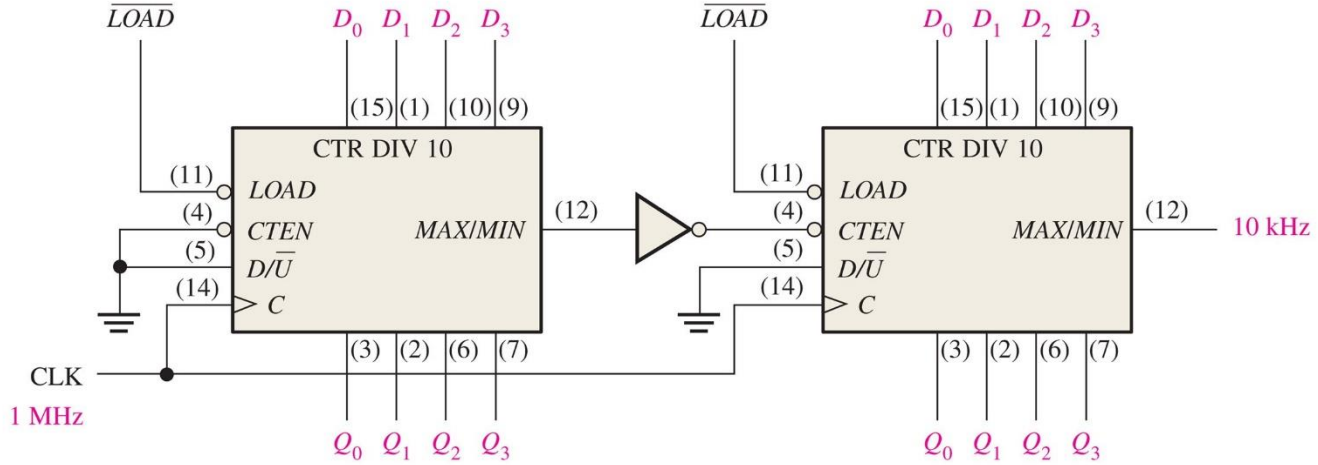


Cascaded Counters: Synchronous

- The overall modulus of these two cascaded counters is 10 * 10 = 100.



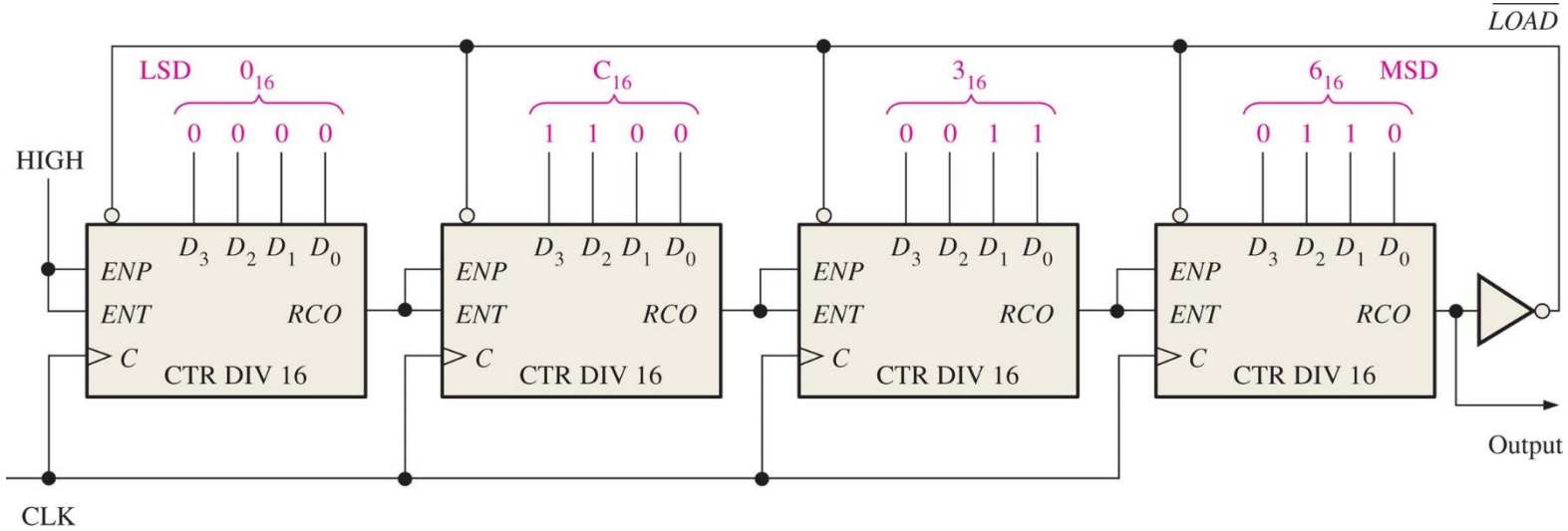
- A divide-by-100 counter using two 74HC190 up/down decade counters connected for the up sequence.



Cascaded Counters with Truncated Sequences

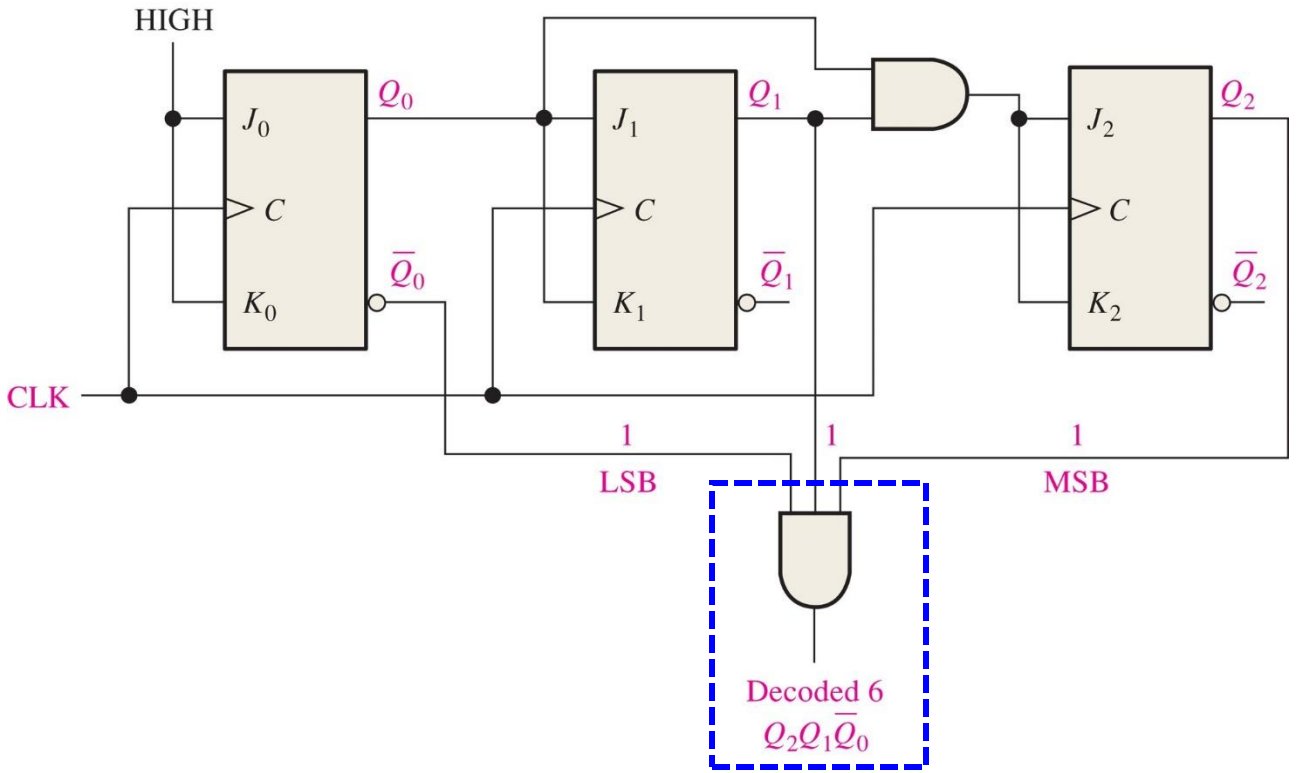
- Full-modulus cascading: the resulting overall modulus is the product of the individual moduli of all the cascaded counters.
- If the required modulus is less than that achieved by full modulus cascading, a truncated sequence must be implemented with cascaded counters.
- Example: to achieve a modulus-40,000 counter with four cascaded 74HC161s whose full modulus is 2^{16}=65,536, we preset the cascaded counter to 25,536 (63C0 in hexadecimal) each time it recycles.

65,536 - 25536 = 40,000



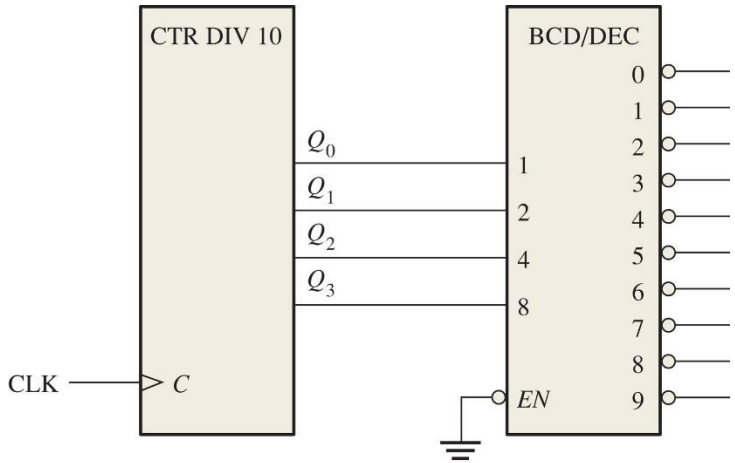
Counter Decoding

- The decoding of a counter involves using decoders or logic gates to determine when the counter is in a certain binary state in its sequence.
- For example, when $Q_2 = 1$, $Q_1 = 1$, and $Q_0 = 0$, a HIGH appears on the output of the following decoding gate, indicating that the counter is at state 6.

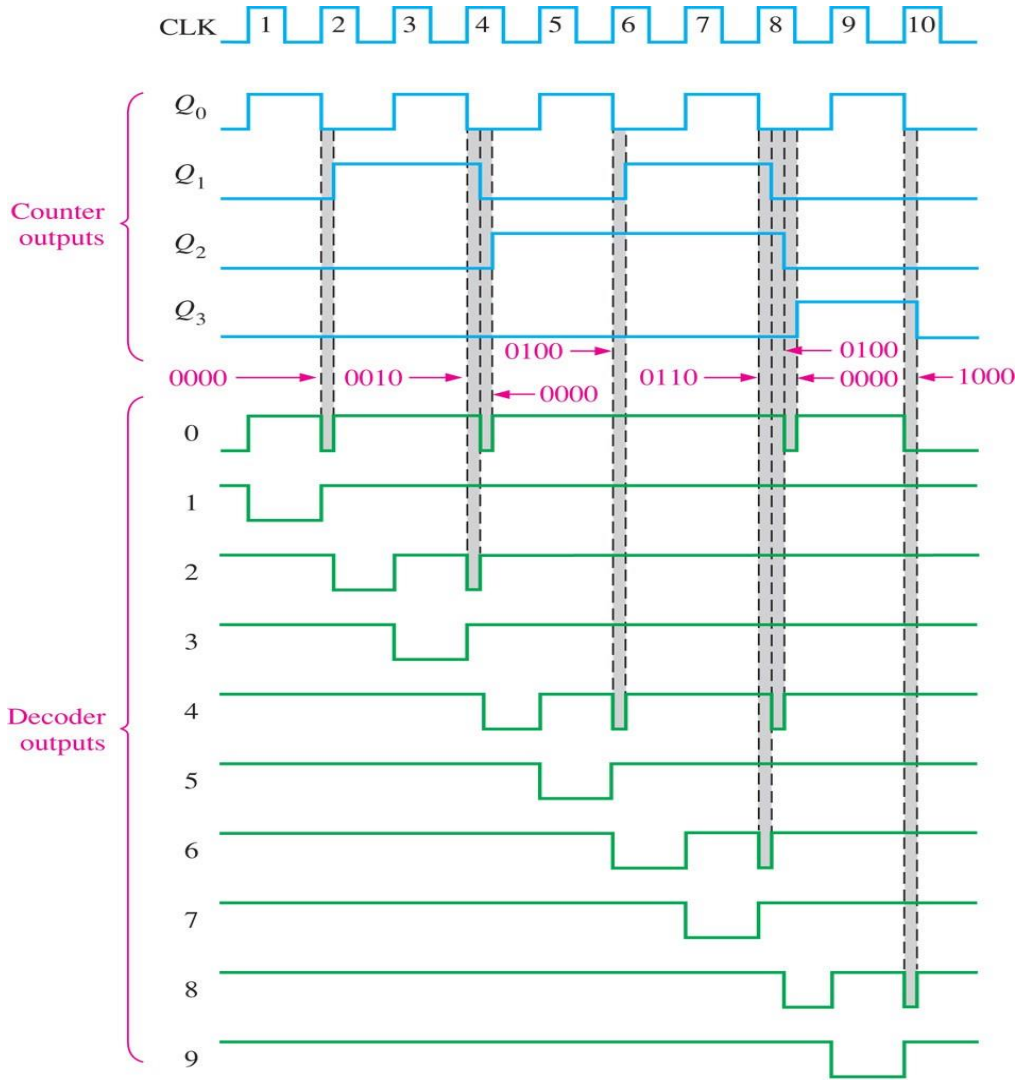


Decoding Glitches (I)

- The glitch problem can also occur to synchronous counters because the propagation delays from the clock to the Q outputs of each flip-flop in a counter can vary slightly.

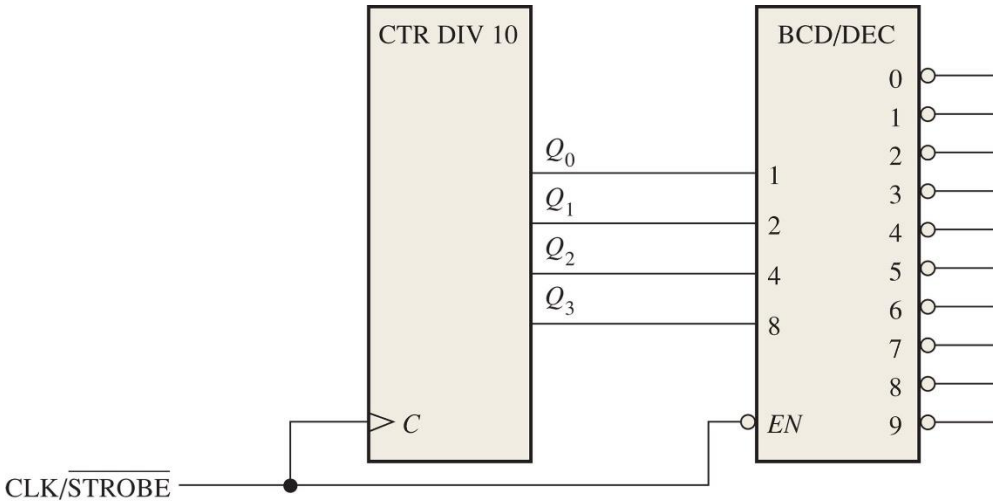


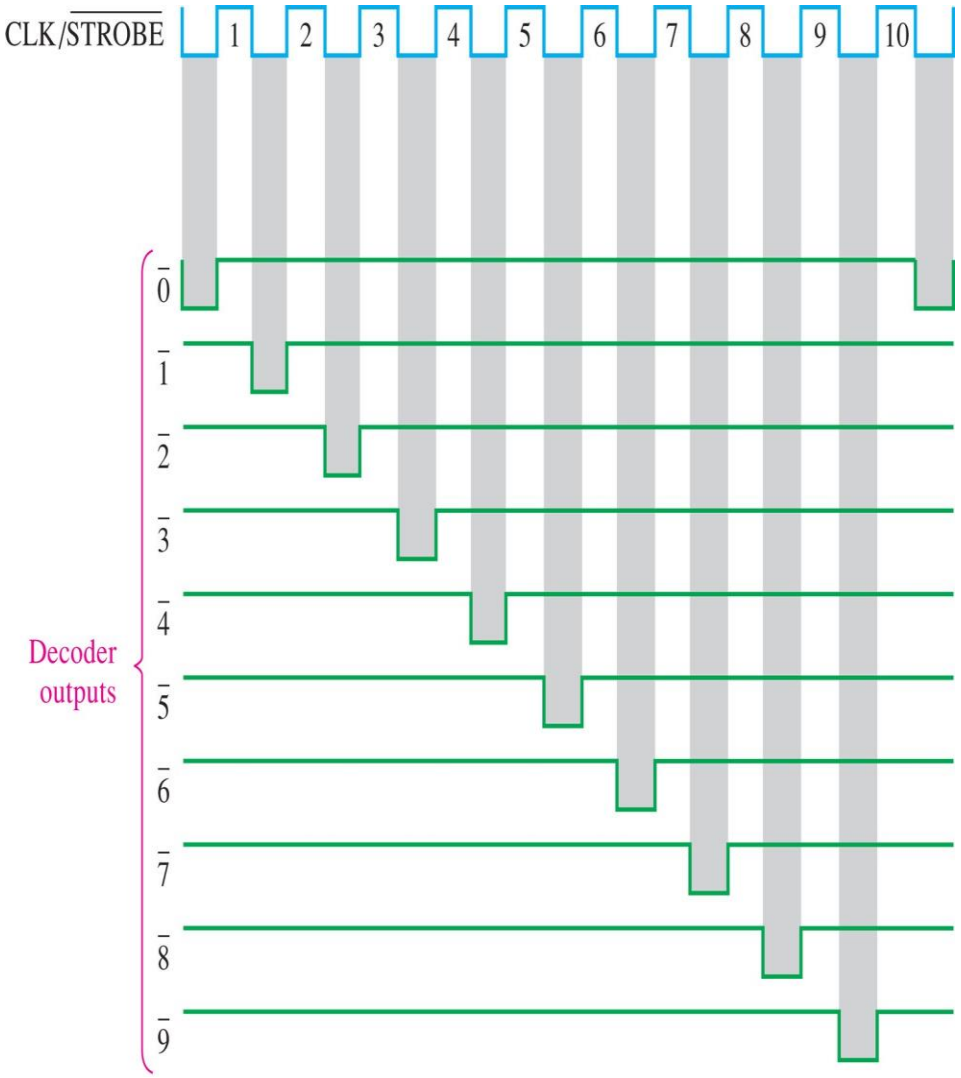
Asynchronous BCD decade counter



Decoding Glitches (II)

- For an active-HIGH clock, use the LOW level of the clock to enable the decoder.

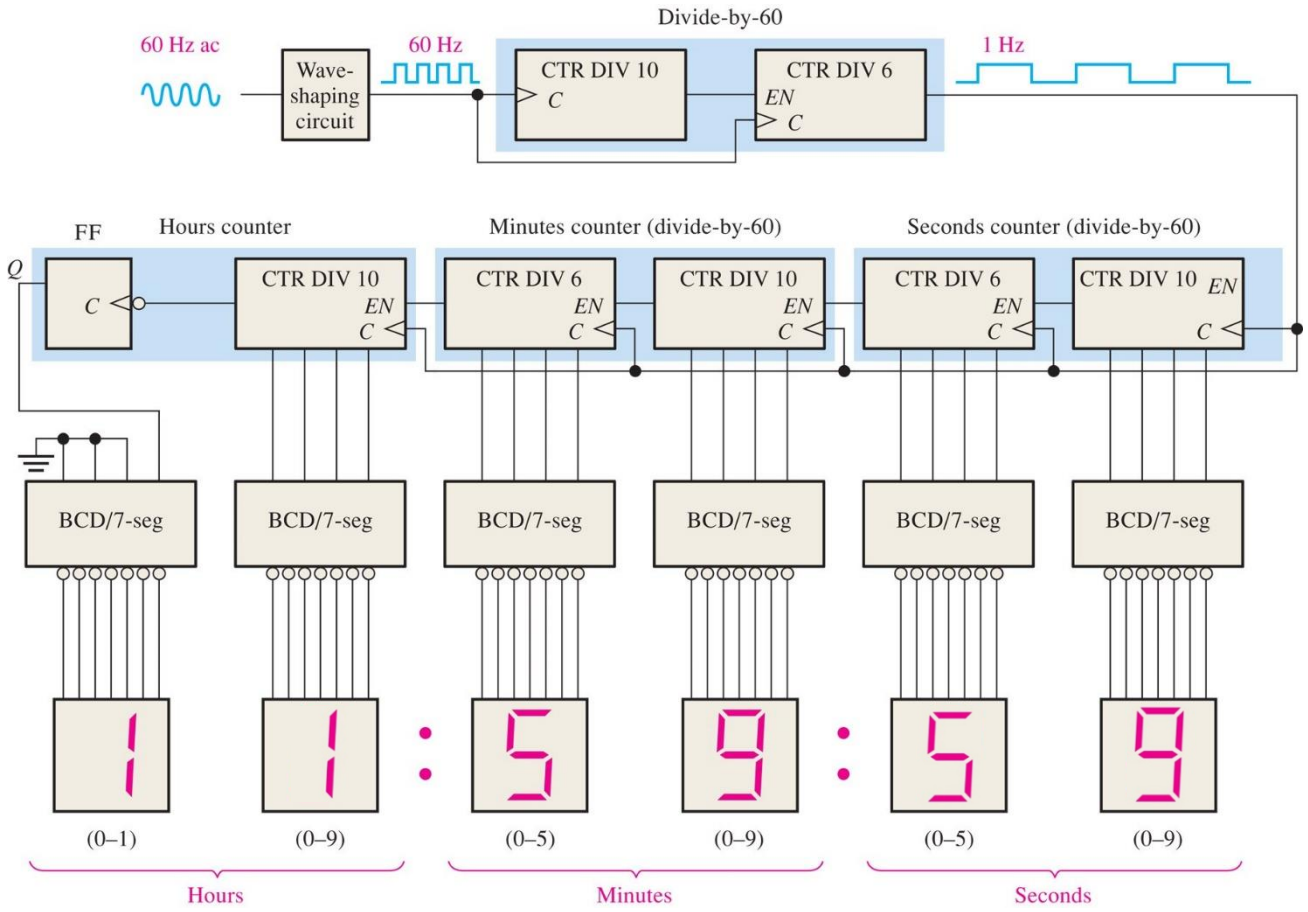




Counter Applications

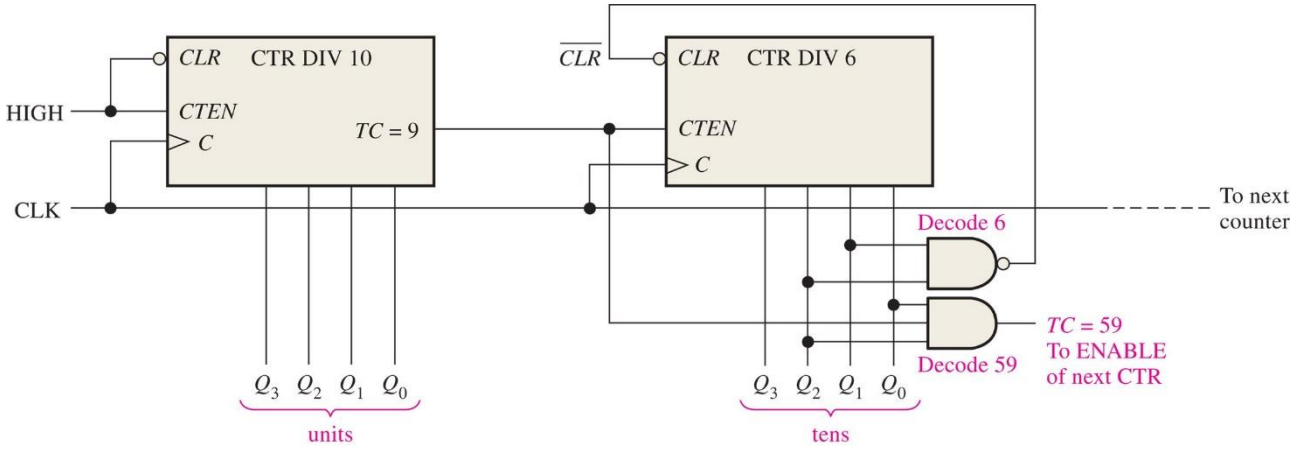
Example: A Digital Clock

- Input : a 60 Hz pulse waveform generated from a 60 Hz sinusoidal ac voltage;
- Counters for Seconds and Minutes : count from 0 to 59 and then recycle to 0;
- The hour counter : a decade counter and a flip-flop to illuminate a 1 on the tens-of-hours display.



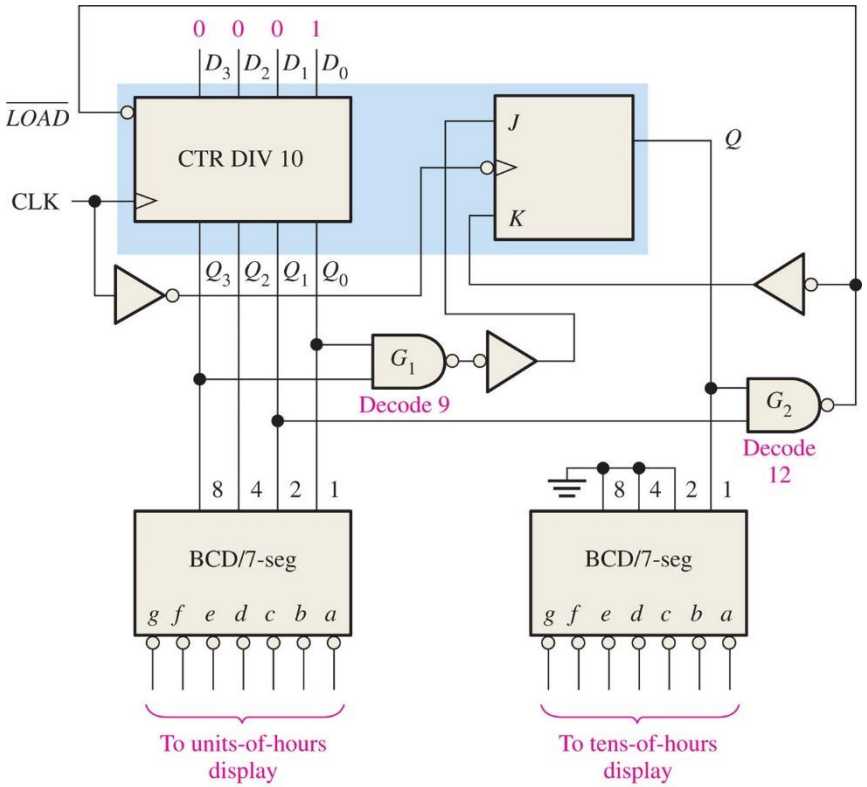
The Second/Minute/Hour Counter

The right-most bit is the LSB



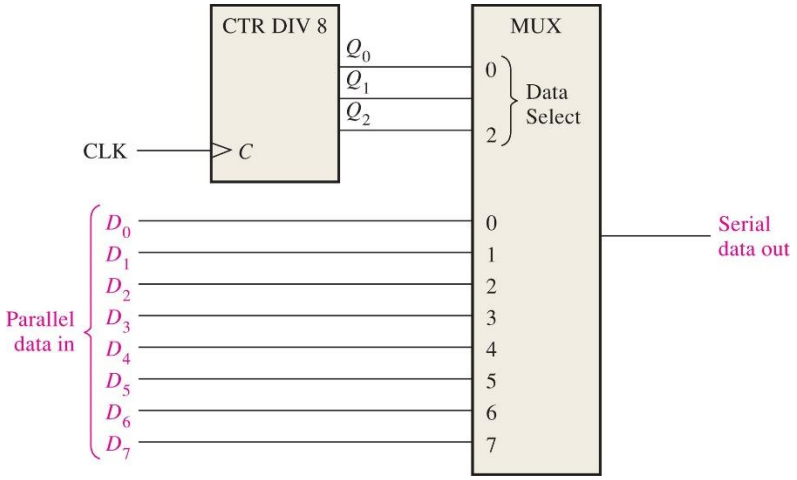
- In state 12, the G2 output is LOW (i.e. Q and Q1 are HIGH) , which activates the LOAD input of the decade counter.
- On the next clock pulse, the decade counter is preset to 0001.

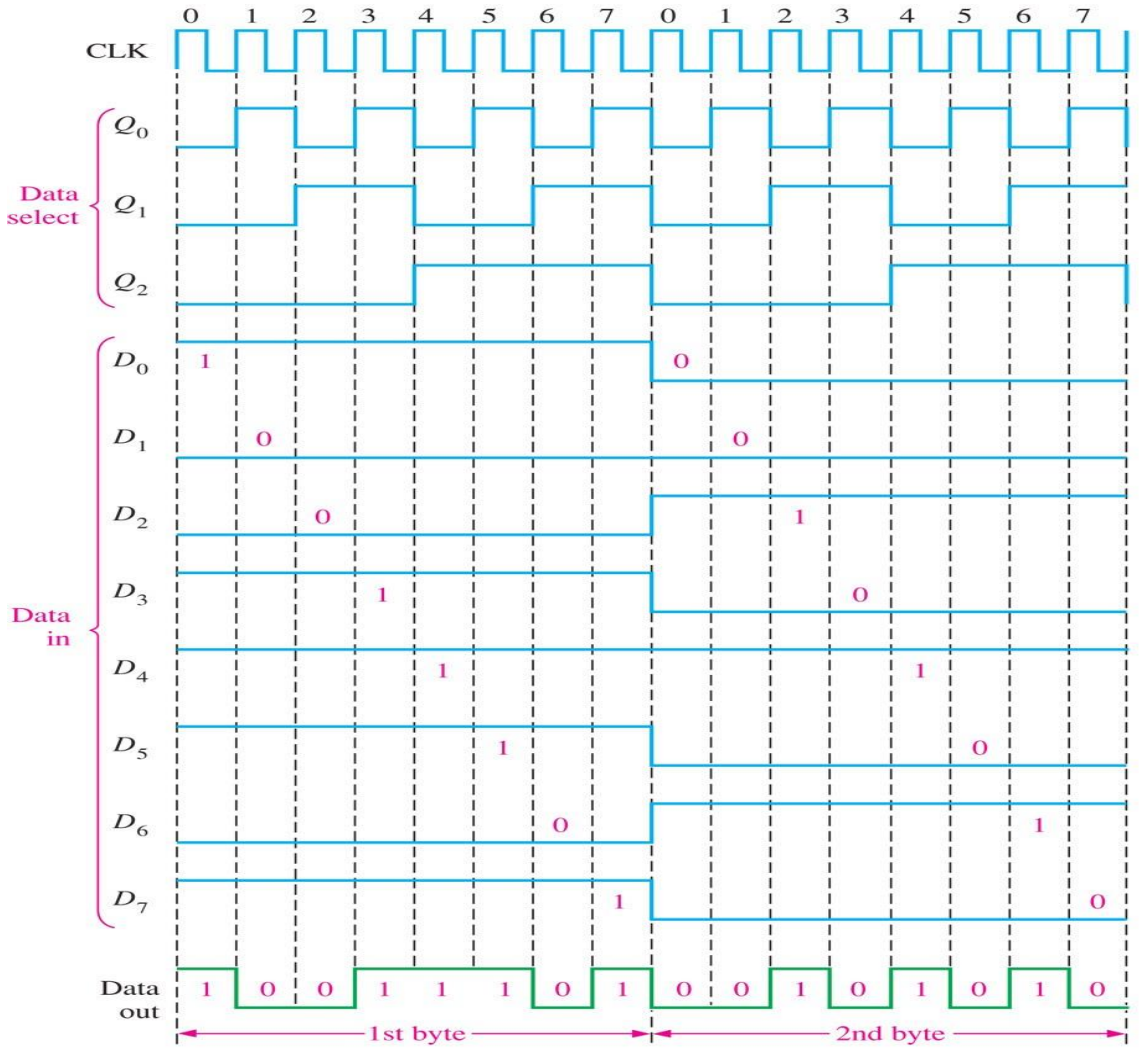
- The terminal count, 59, is decoded to enable the next counter in the chain.



Example: P/S Data Conversion (Multiplexing)

- The 1st byte of parallel data is applied to the multiplexer inputs.
- After 8 clock pulses the data byte has been converted to a serial format and sent out on the transmission line.





Chapter Review

- Counters
  - Asynchronous
  - Synchronous
- Up/Down Counters
- Design of Synchronous Counters
- Cascaded Counters
- Counter Decoding

True/False Quiz

- ✗ Synchronous counters cannot be realized using J-K flip-flops.
- ✓ An asynchronous counter is also known as a ripple counter.
- ✗ A decade counter has twelve states.
- ✓ A counter with four stages has a maximum modulus of sixteen.
- ✗ To achieve a maximum modulus of 32, sixteen stages are required.
- ✓ If the present state is 1000, the next state of a 4-bit up/down counter in the DOWN mode is 0111.
- ✗ Two cascaded decade counters divide the clock frequency by 10.
- ✓ A counter with a truncated sequence has less than its maximum number of states.
- ✗ To achieve a modulus of 100, ten decade counters are required.