ECE2050 Homework 2

Due: Feb. 27, 2025

Q1 Provide your answers to the following short questions. (15 points)

1. Determine the even parity bit for the BCD number 00010100;
2. Convert binary 101101 to Gray code;
3. A ternary numeral system (also called base 3 or trinary) has three as its base. Analogous to a bit, a ternary digit is a trit (trinary digit). Ternary most often refers to a system in which the three digits are all non–negative numbers; specifically 0, 1, and 2. Convert the ternary number 10 to decimal.

Solution:

1. the bit number of 1 is 2.

   $2 \% 2 = 0$ ..... (5 points)

2. 111011 ..... (5 points)

3. $1 \times 3^1 + 0 \times 3^0 = 3$ ..... (5 points)

(17 points)

Q2 Apply CRC to the data bits 10110001 using the generator code 1010 to produce the transmitted CRC code.

Solution:

Append 000 to 10110001

```
10110001000
1010
----
 1000
 1010
 ----
  1010
  1010
  ----
  0000
  1010
  ----
  1010
  1010
  ----
     0
```

(10 points)

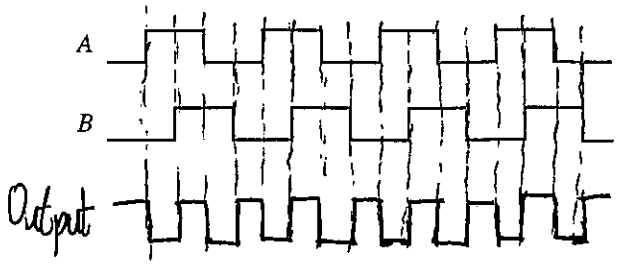
remainder (checksum): 000 ---------- (3 points)

Thus the transmitted CRC code is 10110001000. ---- (4 points)

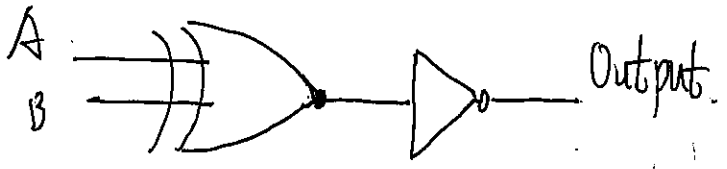
(17 points)

Q3 The waveforms below are applied to points A and B of a 2-input XOR gate followed by an inverter. Draw the output waveform.

Solution:



(1 point for 1 correct bit)

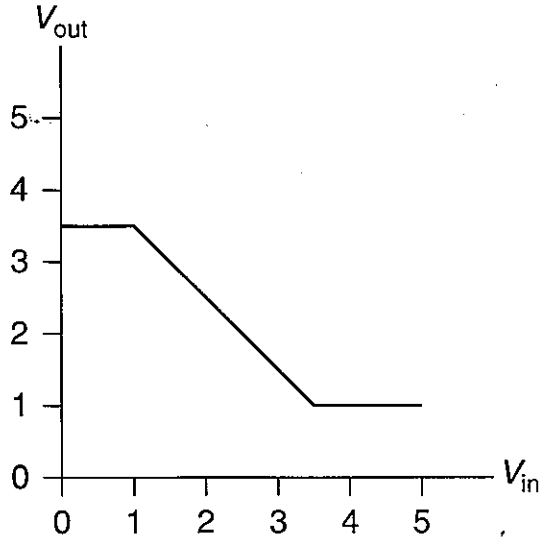


(1) Truth table:

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

(17 points)

Q4 Is it possible to assign logic levels so that a device with the transfer characteristics shown in below would serve as an inverter? If so, what are the input and output low and high levels (V_{IL}, V_{OL}, V_{IH}, and V_{OH}) and noise margins (NM_L and NM_H)? If not, explain why not.



Solution: No, the reason: ---------- (1 points)

$V_{OH} = 3.5V$. $V_{OL} = 1V$

$V_{IH} = 3.5V$ $V_{IL} = 1V$ ---------- (6 points)

$NM_L = V_{IL} - V_{OL} = 1V - 1V = 0$ -- (1)

$NM_H = V_{OH} - V_{IH} = 3.5V - 3.5V = 0$ -- (2) -- (5 points)

From (1) and (2), we can know the circuit does not have any resistance to noise, which is unreasonable.

Thus, it is not possible to assign logic levels. --- (5 points)

(If your answer is yes points will be awarded according to your reasons but no more than 8 points)

(17 points)

Q5 Write down the truth table of the three-input Exclusive-NOR (XNOR) Gate. A, B and C are inputs and Y is output.

Solution:

(2 points for 1 corrected bit)

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

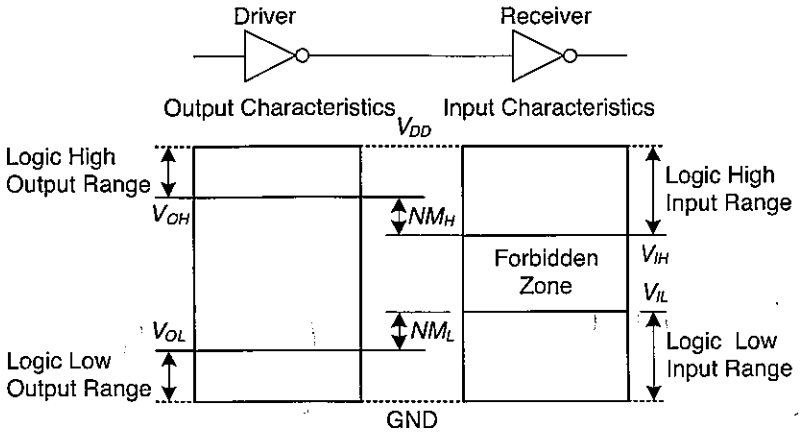
The bit number of 1 is even ⇒ output is 1

The bit number of 1 is odd ⇒ output is 0

(17 points)

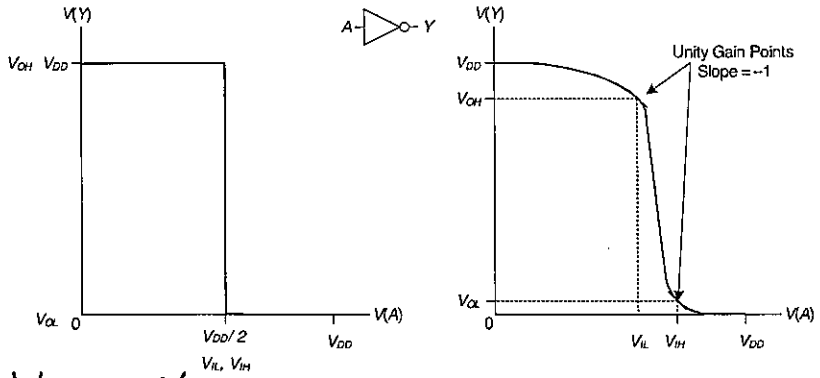
Q6 The noise margin (NM) is the amount of noise that could be added to a worst-case output such that the signal can still be interpreted as a valid input. As can be seen below, the low and high noise margins are, respectively,

$$NM_L = V_{IL} - V_{OL}$$
$$NM_H = V_{OH} - V_{IH}$$



An ideal inverter would have an abrupt switching threshold at $V_{DD}/2$, as shown below. For $V(A) < V_{DD}/2, V(Y) = V_{DD}$. For $V(A) > V_{DD}/2$, $V(Y) = 0$. In such a case, $V_{IH} = V_{IL} = V_{DD}/2$. $V_{OH} = V_{DD}$ and $V_{OL} = 0$. Thus, $NM_H = NM_L = V_{DD}/2$. A real inverter changes more gradually between the extremes, as shown below ($V_{IL} < V_{DD}/2, V_{IH} > V_{DD}/2$). Please show

$$NM_H, NM_L < V_{DD}/2$$



Solution:

$V_{IH} > \frac{V_{DD}}{2}$, $V_{OH} < V_{DD} \Rightarrow NM_H = V_{OH} - V_{IH} < \frac{V_{DD}}{2}$ (8 points)

$V_{IL} < \frac{V_{DD}}{2}$ $V_{OL} > 0, \Rightarrow NM_L = V_{IL} - V_{OL} < \frac{V_{DD}}{2}$ (8 points)

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