Final Exam

(Time allowed: 120 minutes)
May 13, 2023

NOTE: Answer ALL **9** questions. Show all intermediate steps, except Question 1.

1. (10 points) Are the following statements necessarily true (Y) or not (N)?

(1) Pulse oscillators are also known as astable multivibrators;
(2) If the present state is 1000, the next state of a 4-bit up/down counter in the DOWN mode is 1111;
(3) To achieve a modulus of 100, 2 decade counters are required;
(4) A serial shift register can accept more than one bit at a time on a single line;
(5) An S-R latch has two stable states;
(6) When the input bits are both 1 and the input carry bit is 1, the sum output of a full adder is 0;
(7) If the inputs of an exclusive-OR gate are the same, the output is 1;
(8) A 4-variable Karnaugh map has 16 cells;
(9) 16 Bits = 1 Byte;
(10) The final output from the synthesis phase in the FPGA design flow is called Gatelist.

Solution:

(1) Y;
(2) N;
(3) Y;
(4) N;
(5) Y;
(6) N;
(7) N;
(8) Y;
(9) N;
(10) N.

2. (10 points)

(1) (3 points) Convert the binary number 1111001 into octal and hexadecimal;

(2) (3 points) Perform the subtraction of the signed numbers: 00001101 − 11110110;

(3) (4 points) Divide 00011001 by 00000101.

Solution:

(1) $1111001_2 = 75_{16} = 171_8$;

(2) In this case, $13 - (-10) = 13 + 10 = 23$

$$\begin{array}{r} 00001101 \\ +00001010 \\ \hline 00010111 \end{array}$$

(3) In this case, 00000101 → 11111011 (2's complement)

$$\begin{array}{r} 00011001 \\ +11111011 \\ \hline 100010100 \end{array}$$

$$\begin{array}{r} +11111011 \\ \hline 100001111 \end{array}$$

$$\begin{array}{r} +11111011 \\ \hline 100001010 \end{array}$$

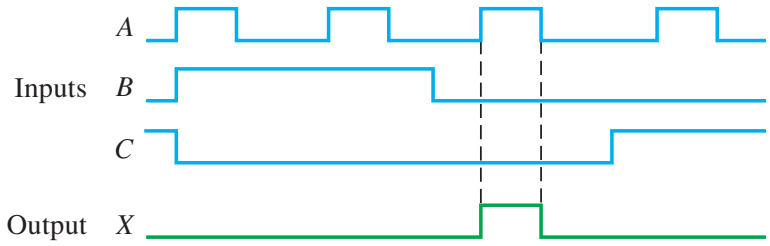
$$\begin{array}{r} +11111011 \\ \hline 100000101 \end{array}$$

$$\begin{array}{r} +11111011 \\ \hline 100000000 \end{array}$$

Quotient is $5 = 0101$. remainder is 0. Note that 1 indicates the result is positive. It is discarded.

3. (10 points)

(1) (4 points) Design a logic circuit to generate the output waveform (You may assume that complementary inputs, if needed, are directly available - e.g., both A and $\bar{A}$ are available. Unknown outputs can be represented as "don't care");



(2) (3 points) Develop a truth table for $X = \overline{AB} + \bar{B}\bar{C}$;

(3) (3 points) Convert $X = \overline{AB} + \bar{B}\bar{C}$ into the **standard** Product of Sum (POS) form.

Solution:

(1) The truth table is shown in Table 1:

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	don't care
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	don't care

Table 1: The truth table

The K-map and its logic circuit are shown in Figure 1.

Figure 1: K-map and logic circuit.

(2) $X = \overline{AB} + \bar{B}\bar{C} = \bar{A} + \bar{B}$. The truth table is shown in Table 2.

A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

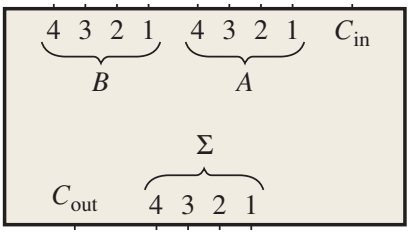
Table 2: The truth table

(3) According to Table 2, $X = (\bar{A} + \bar{B} + C)(\bar{A} + \bar{B} + \bar{C})$.

4. (8 points) The relationship between the BCD code $B_3B_2B_1B_0A_3A_2A_1A_0$ and its binary number $C_6C_5C_4C_3C_2C_1C_0$ is $C_6C_5C_4C_3C_2C_1C_0 = A_3A_2A_1A_0 + 1010 \times B_3B_2B_1B_0 = A_3A_2A_1A_0 + 0010 \times B_3B_2B_1B_0 + 1000 \times B_3B_2B_1B_0$, where $B_3B_2B_1B_0$ is tens digit and $A_3A_2A_1A_0$ is units digit. Furthermore, we have

$$\begin{array}{r} A_3A_2A_1A_0 \\ B_3B_2B_1B_0 \\ +B_3B_2B_1B_0 \\ \hline C_6C_5C_4C_3C_2C_1C_0 \end{array}$$

Design a circuit by using **ONLY** two 4-bit adders to convert a BCD code $B_3B_2B_1B_0A_3A_2A_1A_0$ to its binary number $C_6C_5C_4C_3C_2C_1C_0$ (Connect ALL input pins as needed).



Solution:

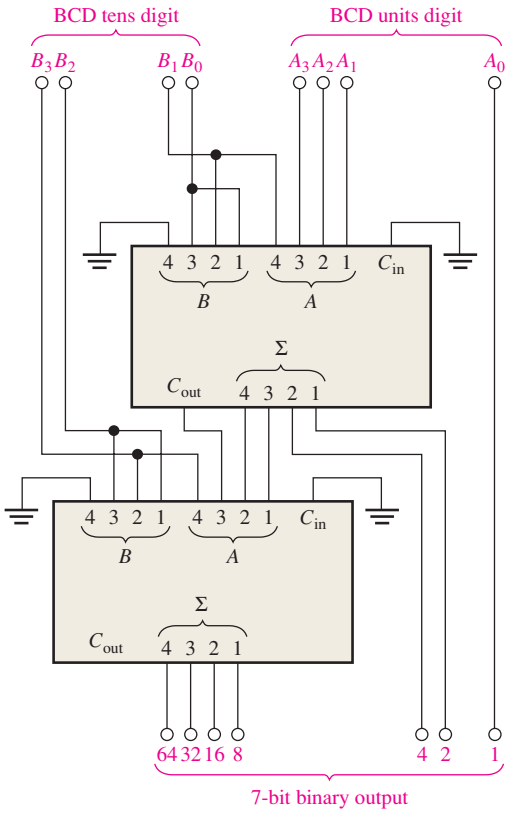
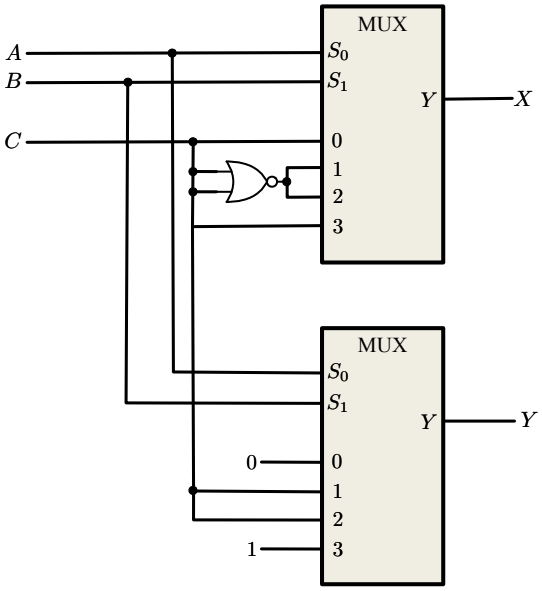


Figure 2: Q4 solution.

5. (10 points) Consider the combinational circuit below, which has three inputs A, B, C and two outputs X and Y.



(1) (4 points) Draw the truth table for X and Y in terms of A, B, C;

(2) (3 points) Determine the output X in terms of A, B, C in the **standard** Sum of Product (SOP) forms;

(3) (3 points) Use Karnaugh Map to simplify the Boolean expression of the output Y.

Solution:

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(1) The truth table is shown in Table 3.

A	B	C	X	Y
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Table 3: The truth table

(2) According to Table 3, $X = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$;

(3) The K-map is shown in Figure 3. $Y = BC + AB + AC$.

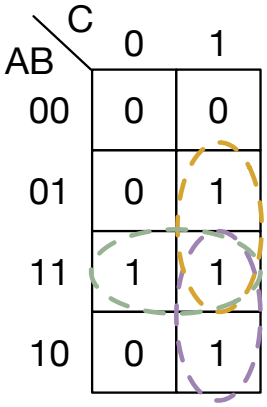
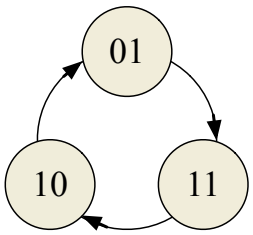


Figure 3: K-map.

6. (12 points) Design a counter to produce the state diagram below using positive edge-triggered J-K flip-flops.



The truth table for a positive edge-triggered J-K flip-flop is given as follows.

Inputs			Outputs	
J	K	CLK	Q	$\overline{Q}$
0	0	↑	Q_0	$\overline{Q}_0$
0	1	↑	0	1
1	0	↑	1	0
1	1	↑	$\overline{Q}_0$	Q_0

↑ = clock transition LOW to HIGH
Q_0 = output level prior to clock transition

(1) (2 points) Complete the following transition table for the positive edge-triggered J-K flip-flop;

Transition table for a J-K flip-flop.

Output Transitions			Flip-Flop Inputs	
Q_N		Q_{N+1}	J	K
0	⟶	0		
0	⟶	1		
1	⟶	0		
1	⟶	1		

Q_N: present state
Q_{N+1}: next state
X: "don't care"

Figure 4: The transition table for the positive edge-triggered J-K flip-flop.

(2) (2 points) Derive the next-state table based on the state diagram above;

(3) (3 points) Derive the expressions for J and K of each positive edge-triggered J-K flip-flop;

(4) (3 points) Draw the counter circuit with positive edge-triggered J-K flip-flops and combinational logic gates;

(5) (2 points) Based on the designed counter circuit in (4), determine the next state for an initial state of 00.

Solution:

(1) The transition table for the positive edge-triggered J-K flip-flop is shown in Figure 5.

Transition table for a J-K flip-flop.

Output Transitions			**Flip-Flop Inputs**	
Q_N		Q_{N+1}	J	K
0	⟶	0	0	X
0	⟶	1	1	X
1	⟶	0	X	1
1	⟶	1	X	0

Q_N: present state
Q_{N+1}: next state
X: "don't care"

Figure 5: The transition table for the positive edge-triggered J-K flip-flop.

(2) The next-state table is shown in Table 4.

Present State		Next State	
Q_1	Q_0	Q_1	Q_0
0	1	1	1
1	1	1	0
1	0	0	1

Table 4: The next-state table

(3) The truth table is shown in Table 5. $J_1 = 1$, $K_1 = \bar{Q}_0$, $J_0 = 1$, $K_0 = Q_1$.

Present State		Next State		JK FF1		JK FF0	
Q_1	Q_0	Q_1	Q_0	J_1	K_1	J_0	K_0
0	1	1	1	1	X	X	0
1	1	1	0	X	0	X	1
1	0	0	1	X	1	1	X

Table 5: The truth table

(4) The counter circuit is shown in Figure 6.

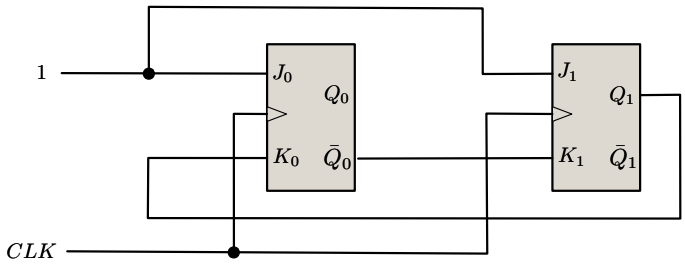


Figure 6: The transition table for the positive edge-triggered J-K flip-flop.

(5) If the initial state is 00, the next state is 11 and the complete state diagram is shown in Figure 7.

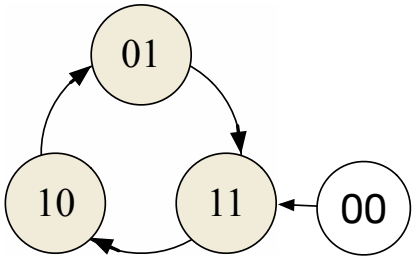


Figure 7: The state diagram if the initial state is 00.

7. (12 points) Consider the synchronous sequential logic circuit below,

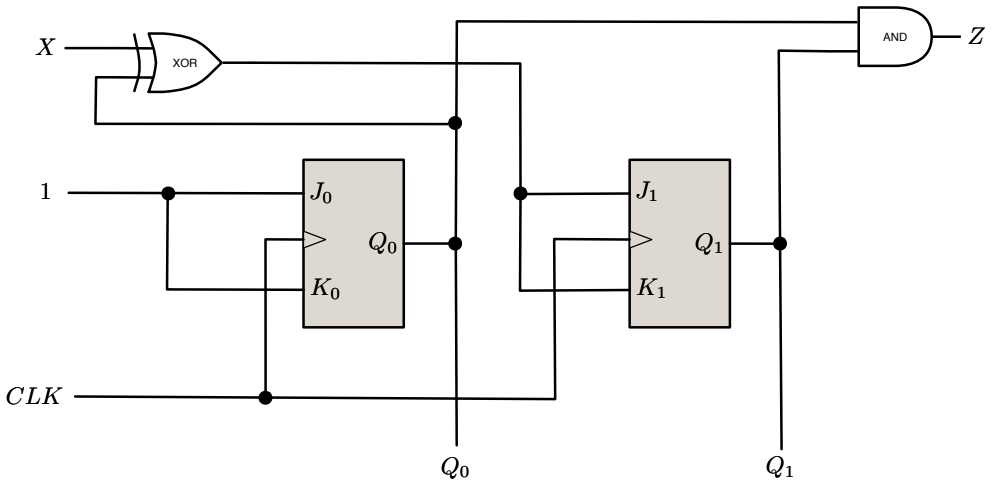


Figure 8: A synchronous sequential logic circuit.

(1) (4 points) Derive logic expressions for J_0, K_0, J_1, K_1 and Z in terms of X, Q_0 and Q_1;

(2) (3 points) Fill in its next-state table below;

Present State		Next State ($X = 0$)			Next State ($X = 1$)		
Q_1	Q_0	Q_1	Q_0	Z	Q_1	Q_0	Z

(3) (2 points) Determine the function of this circuit implements;

(4) (3 points) Complete the following next-state table if the input J_1 is open ($J_1 = 1$).

Present State		Next State ($X = 0$)			Next State ($X = 1$)		
Q_1	Q_0	Q_1	Q_0	Z	Q_1	Q_0	Z

Solution:

(1) $J_0 = 1$, $K_0 = 1$, $J_1 = X \oplus Q_0$, $K_1 = X \oplus Q_0$, $Z = Q_0Q_1$;

(2) The next-state table is shown in Table 6;

Present State		Next State ($X = 0$)			Next State ($X = 1$)		
Q_1	Q_0	Q_1	Q_0	Z	Q_1	Q_0	Z
0	0	0	1	0	1	1	1
0	1	1	0	0	0	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	0

Table 6: The next-state table

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(3) 2-bit (modulus-4) down/up counter;

(4) If the input $J_1 = 1$ is open, the next-state table is shown in Table 7;

Present State		Next State ($X = 0$)			Next State ($X = 1$)		
Q_1	Q_0	Q_1	Q_0	Z	Q_1	Q_0	Z
0	0	1	1	1	1	1	1
0	1	1	0	0	1	0	0
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	0

Table 7: The next-state table

8. (10 points) Recall the traffic light application discussed in Chapter 7, the state diagram is given below.

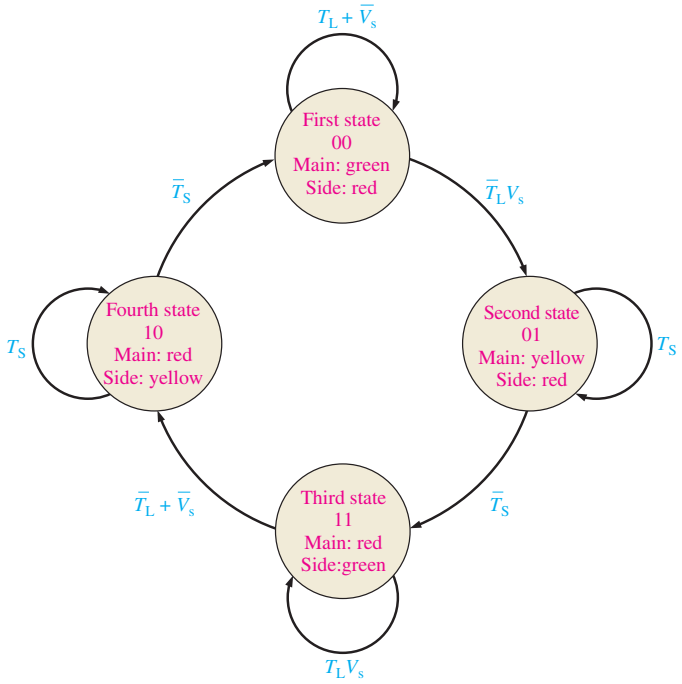

Figure 9: The state diagram for traffic light controller.

Here J-K flip-flops are used to implement this controller. Fill the next-state table for the counter with J-K flip-flops, where Q_1 and Q_0 are the outputs of J-K flip-flops FF1 and FF0. J_1, K_1 and J_0, K_0 are the inputs of FF1 and FF0. (use X to represent "don't care").

Present State		Next State		Input Conditions	FF1 Inputs		FF0 Inputs	
Q_1	Q_0	Q_1	Q_0		J_1	K_1	J_0	K_0
0	0	0	0	$T_L + \bar{V}_S$				
0	0	0	1	$\bar{T}_L V_S$				
0	1	0	1	T_S				
0	1	1	1	$\bar{T}_S$				
1	1	1	1	$T_L V_S$				
1	1	1	0	$\bar{T}_L + \bar{V}_S$				
1	0	1	0	T_S				
1	0	0	0	$\bar{T}_S$				

Solution:

Present State		Next State		Input Conditions	FF1 Inputs		FF0 Inputs	
Q_1	Q_0	Q_1	Q_0		J_1	K_1	J_0	K_0
0	0	0	0	$T_L + \bar{V}_S$	0	X	0	X
0	0	0	1	$\bar{T}_L V_S$	0	X	1	X
0	1	0	1	T_S	0	X	X	0
0	1	1	1	$\bar{T}_S$	1	X	X	0
1	1	1	1	$T_L V_S$	X	0	X	0
1	1	1	0	$\bar{T}_L + \bar{V}_S$	X	0	X	1
1	0	1	0	T_S	X	0	0	X
1	0	0	0	$\bar{T}_S$	X	1	0	X

Table 8: Next-state table for the counter

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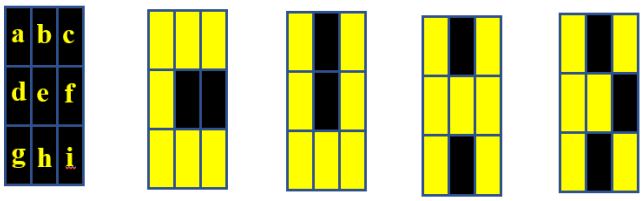
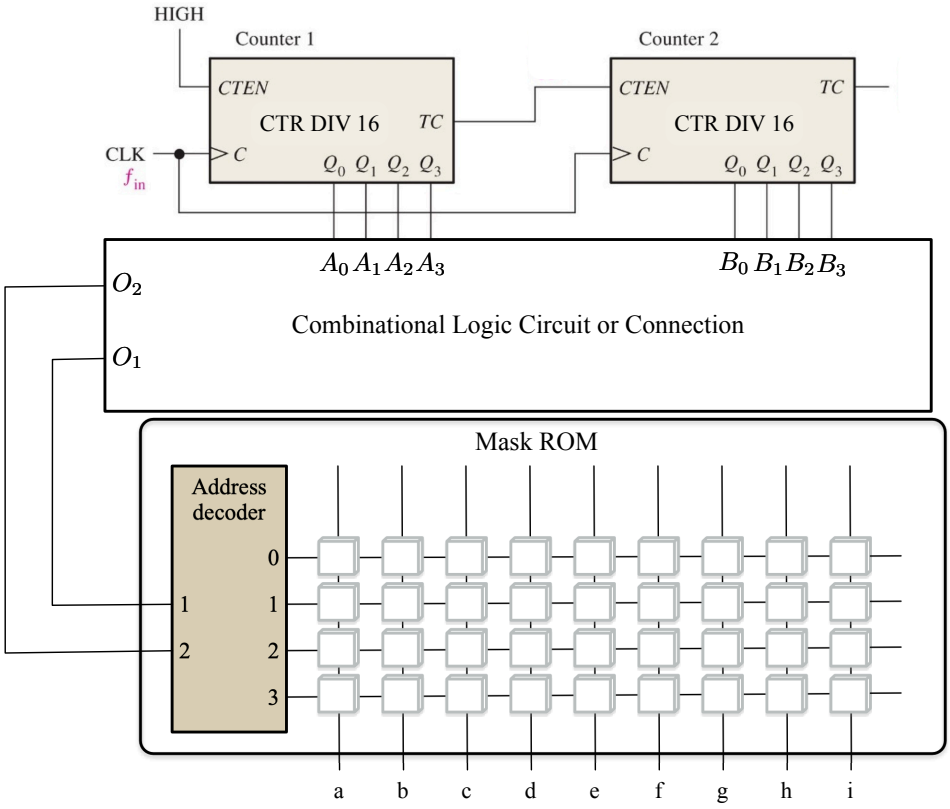
9. (10 points) Four illumination panels showing "C", "U", "H" and "K" have been set up on the upper campus. Different from our campus, we show "C", "U", "H" and "K" on **ONE** panel, instead of four panels. For simplicity, we assume that the panel is composed of nine LED lights labeled as "a" to "i", as shown below. To display an alphabet, we should turn on and off the corresponding LED lights. For instance, "C" is displayed by turning on all LED lights except "e" and "f". More specifically, an LED light is turned on if it is connected to a logic HIGH. In contrast, it is turned off if it is connected to a logic LOW. In other words, we display "C" by connecting "1" to "a, b, c, d, g, h, i" while "0" to "e, f".



We have designed a circuit to display "C", "U", "H", "K" on **ONE** panel by using counters and a mask ROM as shown below.



(1) (5 points) Determine a stored value in each cell in the mask ROM to satisfy the conditions as follows.

- $O_2O_1 = 00$, show "C";
- $O_2O_1 = 01$, show "U";
- $O_2O_1 = 10$, show "H";
- $O_2O_1 = 11$, show "K".

(2) (5 points) Based on the mask ROM in (a), given $f_{in} = 64Hz$, design combinational logic circuits or connections between inputs A_0, A_1, A_2, A_3, B_0, B_1, B_2, B_3 and outputs O_0, O_1 to periodically and sequentially show "C", "U", "H" and "K". During each period, each alphabet will last 1 second.

Solution:

CONTINUED

(1) The stored value in each cell in the mask ROM is shown in Figure 10;

(2) The combinational logic circuits or connections between inputs A_0, A_1, A_2, A_3, B_0, B_1, B_2, B_3 and outputs O_0, O_1 is shown in Figure 10.

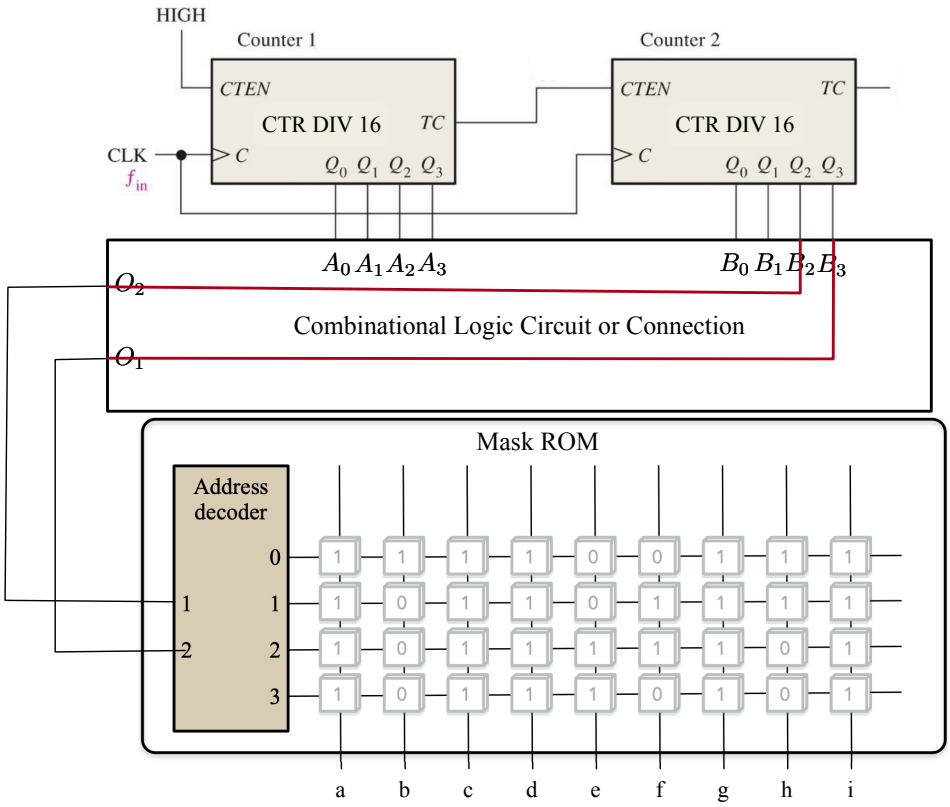


Figure 10: The stored value in each cell in the mask ROM.