Midterm Test

(Time allowed: 90 minutes)
March 24, 2022

NOTE: Answer ALL **9** questions. Show all intermediate steps.

1. (10 points)

(1) Convert the fractional binary number 100001.111 to decimal;

(2) Convert the decimal fraction 0.4375 to a binary number using repeated multiplication by 2. Show your steps;

(3) Perform *binary* subtraction on the following signed numbers:

$$11011001 - 11100111$$

(4) Divide 01000100 by 00011001 in the 2's compliment form. Find the quotient and the remainder in *binary*.

Solution:

(1) $100001.111_2 = 2^5 + 2^0 + 2^{-1} + 2^{-2} + 2^{-3} = 33.875$

(2) The answer is 0.0111_2.

$$\begin{aligned} 0.4375 \times 2 &= 0.875 \quad (1) \\ 0.875 \times 2 &= 1.75 \quad (2) \\ 0.75 \times 2 &= 1.5 \quad (3) \\ 0.5 \times 2 &= 1.0 \quad (4) \end{aligned}$$

(3) The 2's compliment of 11100111 is 00011001. Thus, we have

$$\begin{array}{r} 11011001 \\ +\ 00011001 \\ \hline 11110010 \end{array}$$

(4) The 2's compliment of 00011001 is 11100111.

Step 1:

$$\begin{array}{r} 01000100 \\ +\ 11100111 \\ \hline 00101011 \end{array}$$

Quotient: 00000001

Step:2:

$$\begin{array}{r} 00101011 \\ +\ 11100111 \\ \hline 00010010 \end{array}$$

Quotient: 00000010

Remainder: 00010010

Therefore, the quotient is 00000010 and remainder is 00010010.

2. (10 points)

(1) Convert the following Boolean expression into the **standard** Product Of Sums (POS) form:

$$\left(A+\overline{B}+C\right)\left(\overline{B}+C+\overline{D}\right)\left(A+\overline{B}+\overline{C}+D\right)$$

(2) Convert the following Boolean expression into the **standard** POS form:

$$\overline{A}\cdot\overline{B}\cdot\overline{C}+\overline{A}\cdot B\cdot\overline{C}+\overline{A}\cdot B\cdot C+A\cdot\overline{B}\cdot C+A\cdot B\cdot C$$

Solution:

(1)

$$\begin{aligned} & \left(A+\overline{B}+C\right)\left(\overline{B}+C+\overline{D}\right)\left(A+\overline{B}+\overline{C}+D\right) && (5)\\ = \ & \left(A+\overline{B}+C+D\overline{D}\right)\left(A\overline{A}+\overline{B}+C+\overline{D}\right)\left(A+\overline{B}+\overline{C}+D\right) && (6)\\ = \ & \left(A+\overline{B}+C+D\right)\left(A+\overline{B}+C+\overline{D}\right)\left(A+\overline{B}+C+D\right)\left(\overline{A}+\overline{B}+C+\overline{D}\right)\left(A+\overline{B}+\overline{C}+D\right) && (7)\end{aligned}$$

(2) The expression contains 000, 010, 011, 101 and 111. Thus, the remaining terms are 001, 100 and 110. In other words, the expression can be simplified as

$$\left(A+B+\overline{C}\right)\left(\overline{A}+B+C\right)\left(\overline{A}+\overline{B}+C\right)$$

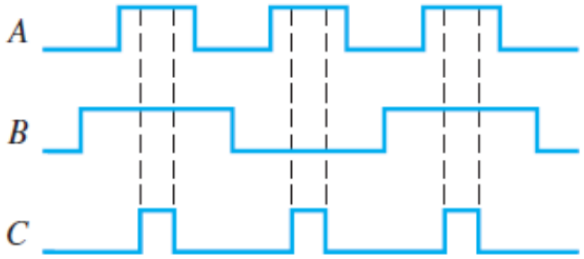
.

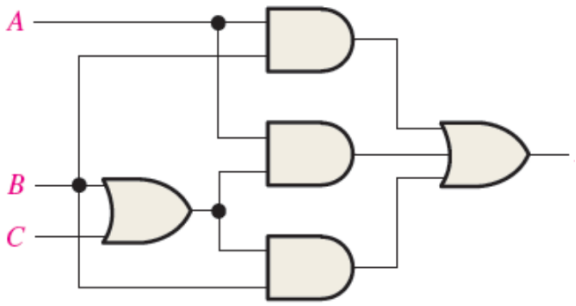
3. (10 points)

(1) Simplify the following Boolean expression:

$$\overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot \overline{C} + A \cdot \overline{B} \cdot C + A \cdot B \cdot C$$

(2) The input waveforms A, B and C are applied to the following circuit. Draw the output waveform of the circuit.





Solution:

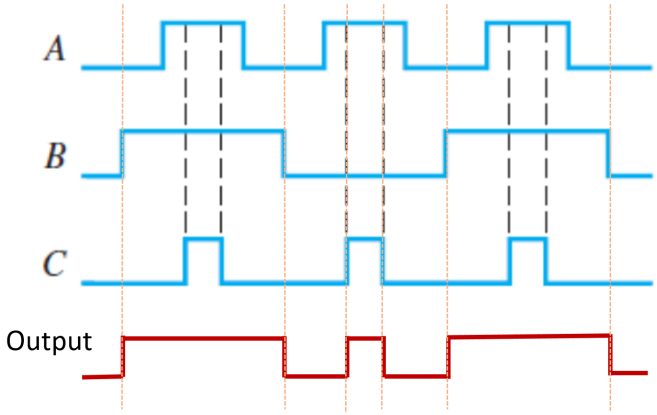
(1)

$$\begin{aligned} & \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot \overline{C} + A \cdot \overline{B} \cdot C + A \cdot B \cdot C && (8) \\ = \; & \left(\overline{A} \cdot B \cdot C + A \cdot B \cdot C\right) + \left(A \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot \overline{C}\right) + \left(A \cdot \overline{B} \cdot C + A \cdot B \cdot C\right) && (9) \\ = \; & B \cdot C + \overline{B} \cdot \overline{C} + A \cdot C && (10) \end{aligned}$$

Alternatively, the solution of $B \cdot C + \overline{B} \cdot \overline{C} + A \cdot \overline{B}$ is also correct.

(2) We first simplify the output expression as

$$Y = AB + A(B + C) + B(B + C) = B + AC$$



4. (10 points) Given the following truth table

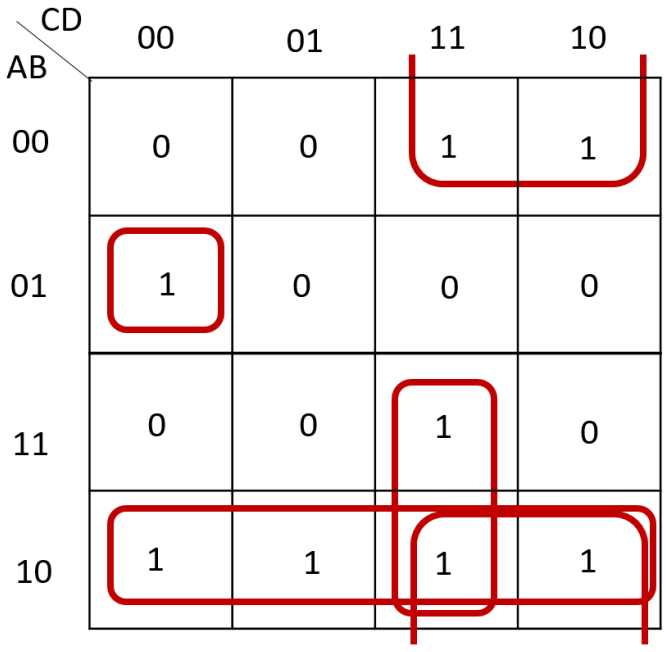
Inputs				Output
A	***B***	***C***	***D***	***X***
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

(1) Use K-map to find out the simplest SOP expression of X;

(2) Draw the logic circuit based on the SOP expression above.

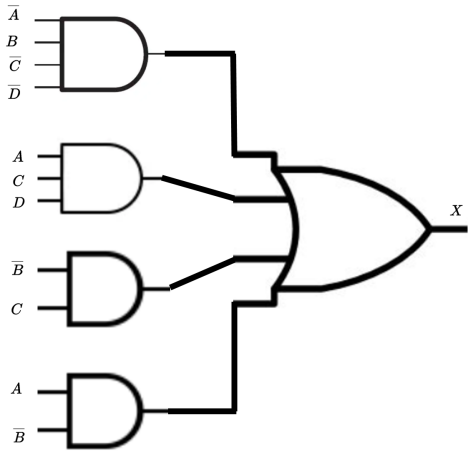
Solution:

(1) The SOP expression of X is derived with K-map as shown below:



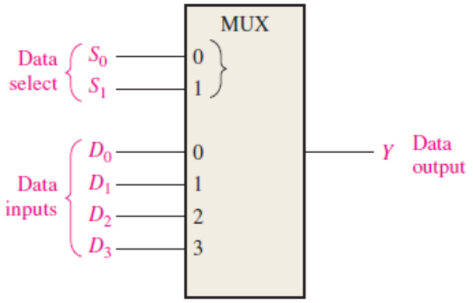
$$X = \overline{A}\,B\,\overline{C}\,\overline{D} + A\,C\,D + \overline{B}\,C + A\,\overline{B}$$

(2) The logic circuit is given as follows:


$\overline{A}$
B
$\overline{C}$
$\overline{D}$
A
C
D
$\overline{B}$
C
A
$\overline{B}$
X

5. (17 points)

(1) Using basic gates (such as AND, OR , Inverter) to implement the following 1-of-4 data selector/multiplexer. Show your logic diagram.



Data selection for a 1-of-4-multiplexer.

Data-Select Inputs		
S_1	S_0	Input Selected
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

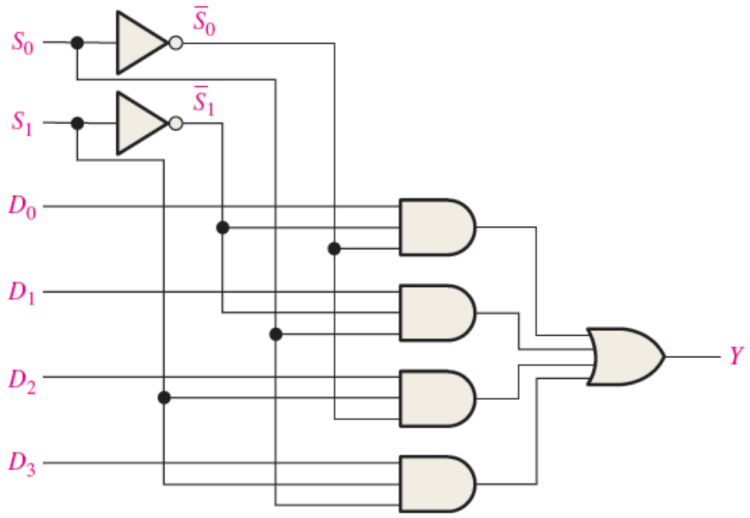
(2) Use K-map to find out the Sum of Products (SOP) expression of Y;

Inputs			Output
A_2	A_1	A_0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

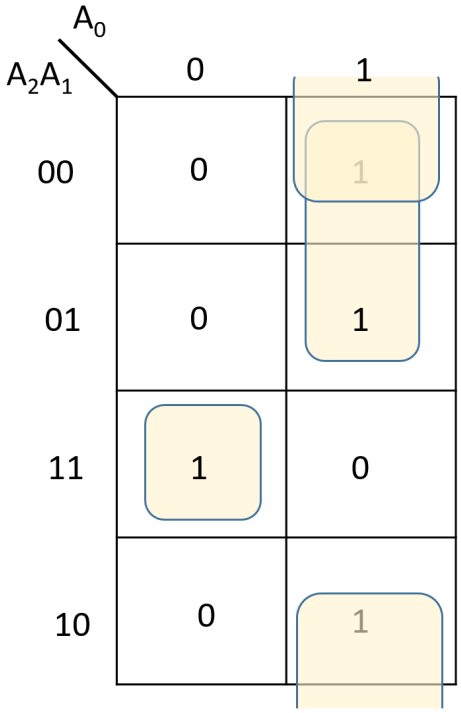
(3) Using one 1-of-4 data selector/multiplexer designed in (1) and necessary basic logic gates to implement the truth table in (2). Show your steps and the resulting logic diagram.

Solution:

(1) The 1-of-4 data selector/multiplexer can be implemented as follows:



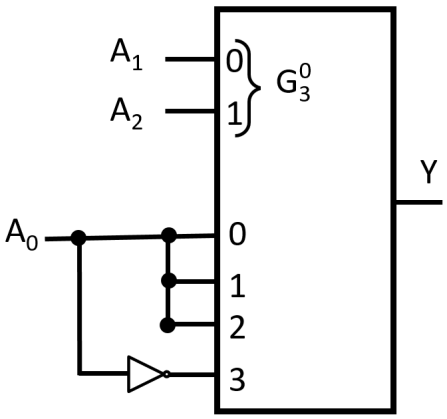
(2) The expression for Y can be read from the following K-map



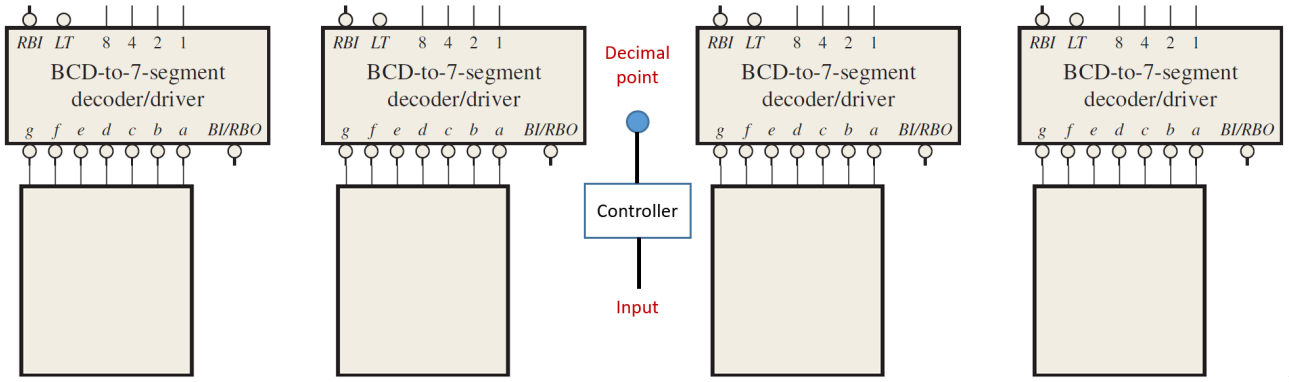
$$Y = \overline{A}_2 A_0 + \overline{A}_1 A_0 + A_2 A_1 \overline{A}_0$$

(3) The truth table can be written as

A_2	A_1	Y
0	0	A_0
0	1	A_0
1	0	A_0
1	1	$\overline{A}_0$



6. (8 points) Zero Suppression for a 4-Digit Display: As explained in Chapter 6, all segment outputs of the BCD-to-7-segment decoder/driver are HIGH (nonactive) when a zero code (0000) is on the BCD inputs and $\overline{\text{RBI}}$ is LOW, which causes the display to be blanked and produces a LOW $\overline{\text{RBO}}$.



b

(1) Design a logic circuit such that the following three requirements are all satisfied

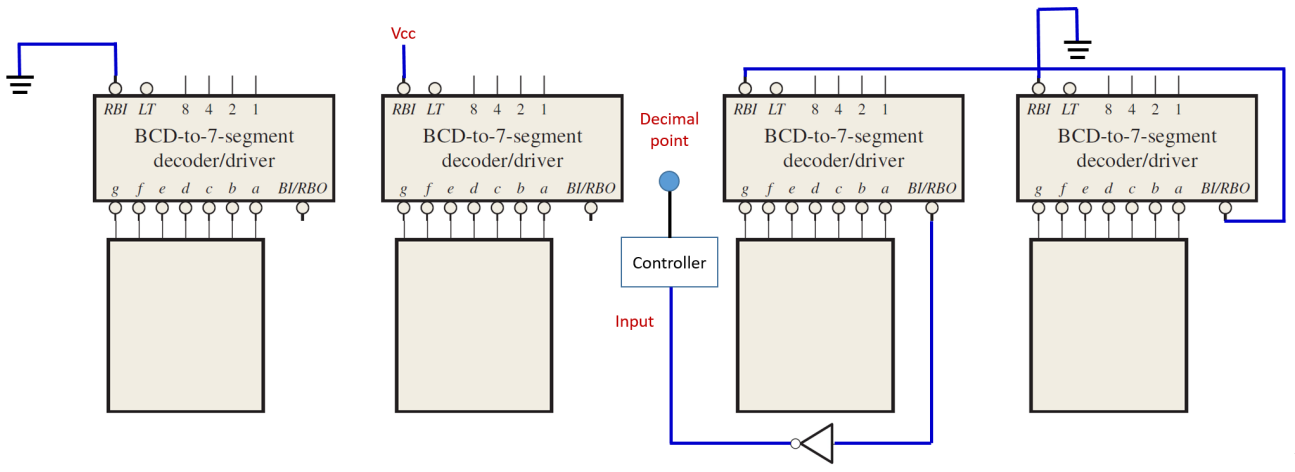
(i) Leading zeros and trailing zeros are suppressed. For instance, "3.2" should be displayed on the four panels from left to right as blank, "3", "2" and blank, respectively.

(ii) If the to-be-displayed number is less than 1, i.e. the integer part is zero, then the least significant integer digit (i.e. the second panel from the left) should display "0". For instance, "0.2" should be displayed on the four panels from left to right as *blank*, "0", "2" and *blank*, respectively.

(iii) If the to-be-displayed number is an integer, then the two panels on the right should be blanked. For instance, "2" should be displayed on the four panels from left to right as *blank*, "2", *blank* and *blank*, respectively.

(2) Design a controller for the display of the "decimal point". If the input to the controller is HIGH, then the decimal point is displayed; otherwise, the display is off. The controller should blank the decimal point display if the input is an integer. For instance, "20.00" should be displayed on the four panels from left to right as "2", "0", *blank* and *blank*, respectively, with the decimal point being blanked.

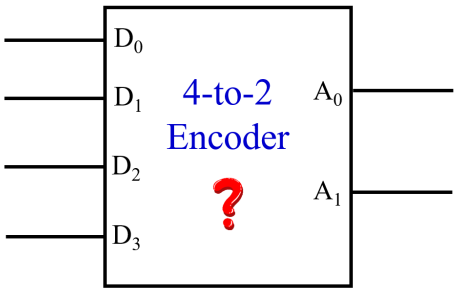
Solution:



b

7. (15 points)

(1) Design a 4-to-2-line encoder that implements the following truth table using basic logic gates such as AND, OR gates. Derive the Boolean expressions for A_0 and A_1 and draw the resulting logic diagram.



Activated Input Line	BCD Code A_1	A_0
D_0	0	0
D_1	0	1
D_2	1	0
D_3	1	1

(2) Design a priority encoder that gives higher priority to D_i than D_j for $i > j$, i.e the highest priority to D_3 and lowest priority to D_0. In other words, if both D_i and D_j where $i, j \in [0, 3]$ are HIGH, then D_j will be ignored for $i > j$.

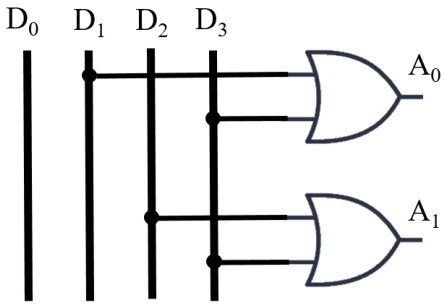
(i) Show the truth table for such a priority encoder;

(ii) Use K-map to derive the Boolean expression for A_0.

Solution:

(1) The Boolean expressions for A_0 and A_1 are given as follows:

$$A_0 = D_1 + D_3 \tag{11}$$
$$A_1 = D_2 + D_3 \tag{12}$$



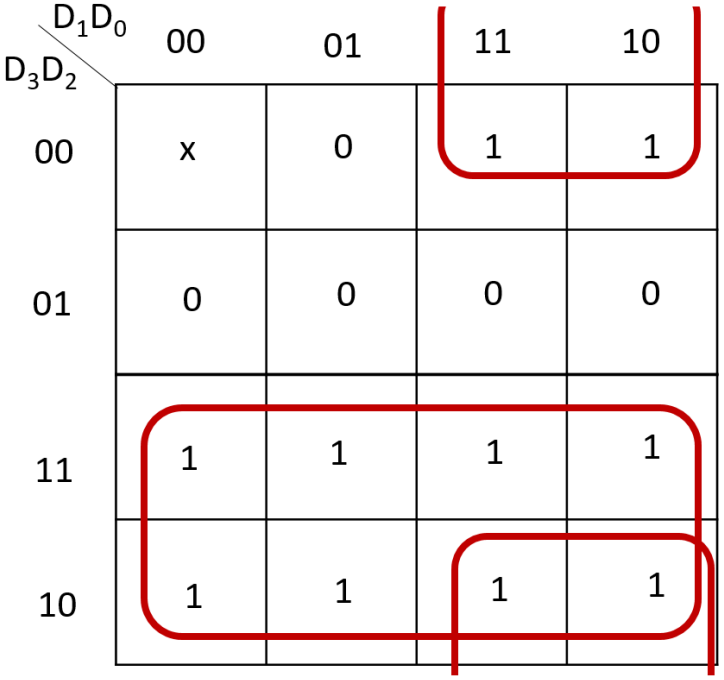
(2) The truth table of the priority encoder is given by:

Inputs D_3	D_2	D_1	D_0	Outputs A_1	A_0
0	0	0	1	0	0
0	0	1	x	0	1
0	1	x	x	1	0
1	x	x	x	1	1

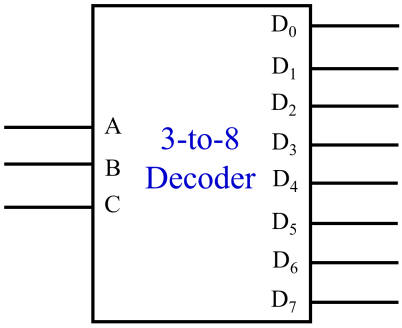
Using K-map, we can find the expression for A_0 as

$$A_0 = D_1\overline{D}_2 + D_3$$

CONTINUED


D1D0
D3D2
00
01
11
10
00
01
11
10
x
0
1
1
0
0
0
0
1
1
1
1
1
1
1
1

8. (10 points) Implement a full adder circuit using the following 3-to-8 line decoder.



INPUTS			OUTPUTS							
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

(1) Derive the truth table for a full adder whose inputs are A, B and C_{in} and output Σ and C_{out};

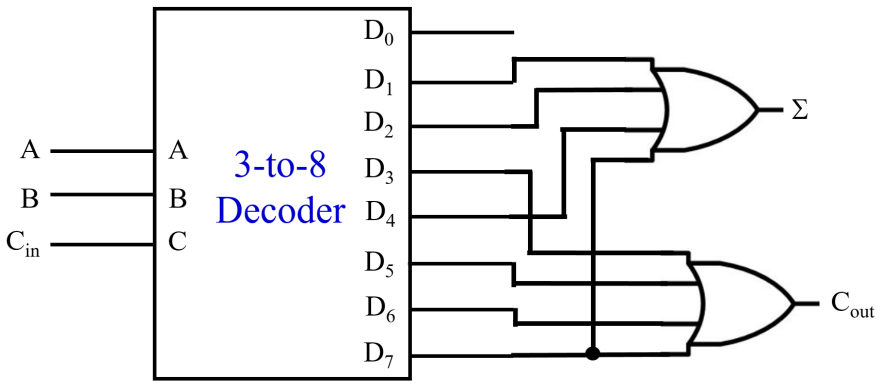
(2) Implement the truth table using the 3-to-8 line decoder above and necessary basic logic gates.

Solution:

(1) The truth table of a full adder is given as follows:

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

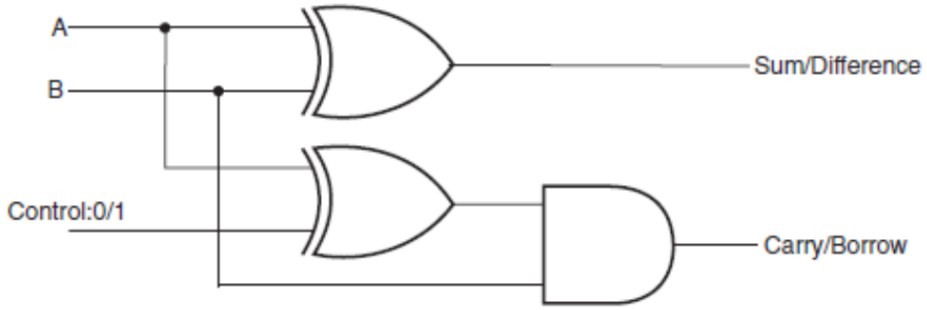
(2) The truth table above can be implemented with the 3-to-8 line decoder as follows:



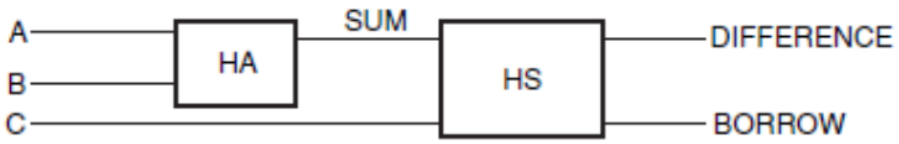
CONTINUED

9. (10 points)

(1) The following figure shows a half adder–subtractor circuit that can be used to perform either addition or subtraction on two one-bit numbers, depending on the control input denoted by C. Derive the Boolean expressions of SUM and CARRY for $C = 0$ and DIFFERENCE and BORROW for $C = 1$.



(2) Derive the simplified Boolean expressions for DIFFERENCE and BORROW outputs for the following given circuit in which "HA" and "HS" stand for half-adder and half-subtractor, respectively. Show your steps.



Solution:

(1) (i) Half-adder when C is LOW

$$\text{SUM} = \overline{A}B + A\overline{B} \tag{13}$$
$$\text{CARRY} = AB \tag{14}$$
$$\tag{15}$$

(ii) Half-subtractor when C is HIGH

$$\text{DIFFERENCE} = \overline{A}B + A\overline{B} \tag{16}$$
$$\text{BORROW} = \overline{A}B \tag{17}$$
$$\tag{18}$$

(2)

$$\text{DIFFERENCE} = (\overline{\bar{A} \cdot B + A \cdot \bar{B}}) \cdot C + (\bar{A} \cdot B + A \cdot \bar{B}) \cdot \bar{C} \tag{19}$$
$$= (A \cdot B + \bar{A} \cdot \bar{B}) \cdot C + (\bar{A} \cdot B + A \cdot \bar{B}) \cdot \bar{C} \tag{20}$$
$$= A \cdot B \cdot C + \bar{A} \cdot \bar{B} \cdot C + \bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot \bar{C} \tag{21}$$
$$\text{BORROW} = (\overline{\bar{A} \cdot B + A \cdot \bar{B}}) \cdot C \tag{22}$$
$$= (A \cdot B + \overline{A} \cdot \overline{B}) \cdot C = A \cdot B \cdot C + \overline{A} \cdot \overline{B} \cdot C \tag{23}$$