香港中文大學（深圳）
The Chinese University of Hong Kong, Shenzhen

ECE2050 Digital Logic and Systems

Tutorial 6

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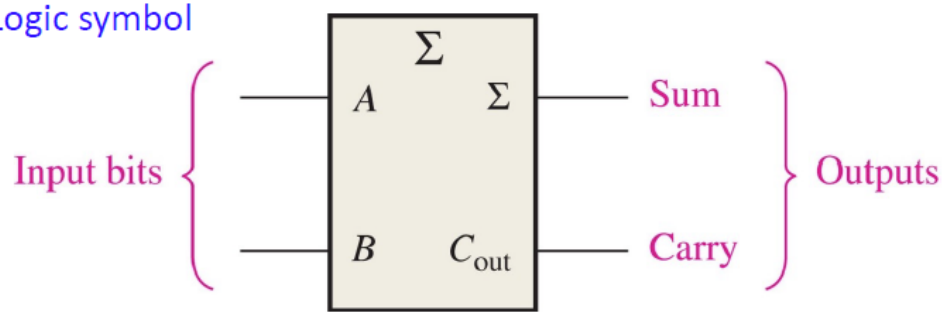
Office Hour: 16:00-17:00 Wed., ZX305

Combinational Building Blocks

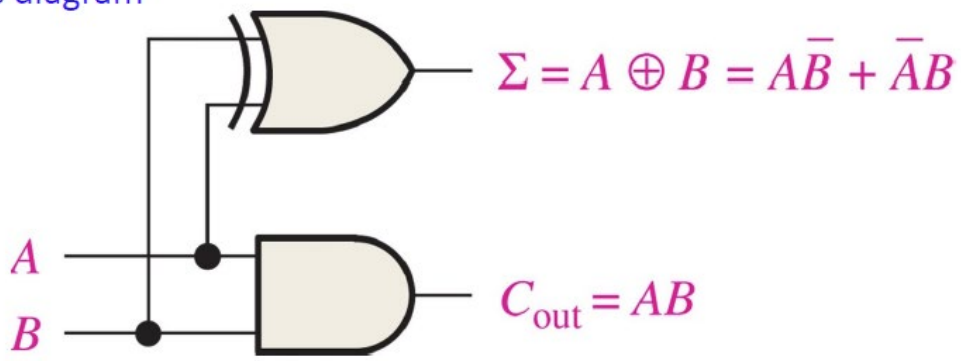
- Half Adders

Basic rules of binary addition are performed by a half adder, which has two binary inputs (A and B) and two binary outputs (Carry out and Sum).

Logic symbol



Logic diagram

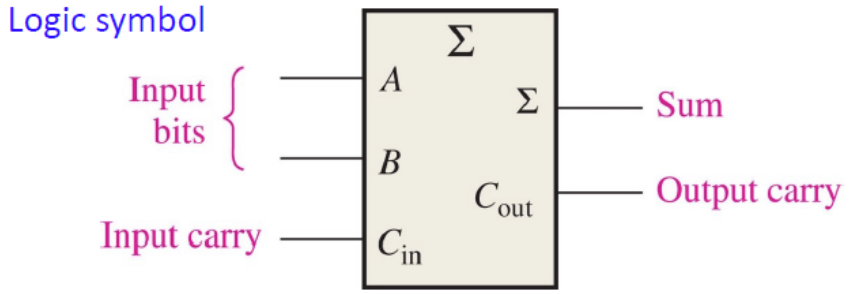


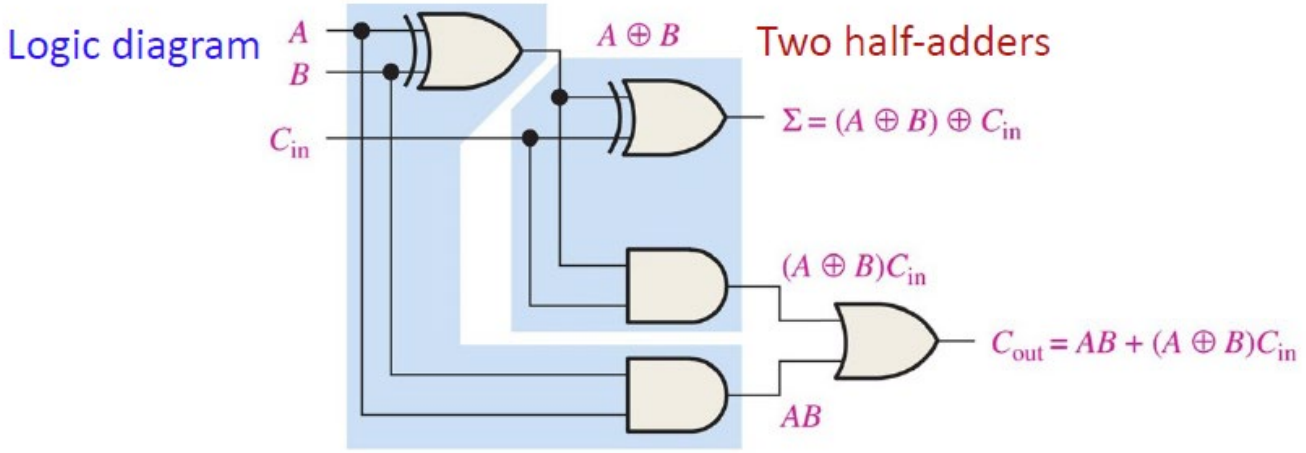
Inputs		Outputs	
A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Combinational Building Blocks

- Full Adders

By contrast, a full adder has three binary inputs (A, B, and Carry in) and two binary outputs (Carry out and Sum). The truth table summarizes the operation.





Inputs			Outputs	
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Combinational Building Blocks

- Parallel Adders

Full adders are combined into parallel adders that can add binary numbers with multiple bits.

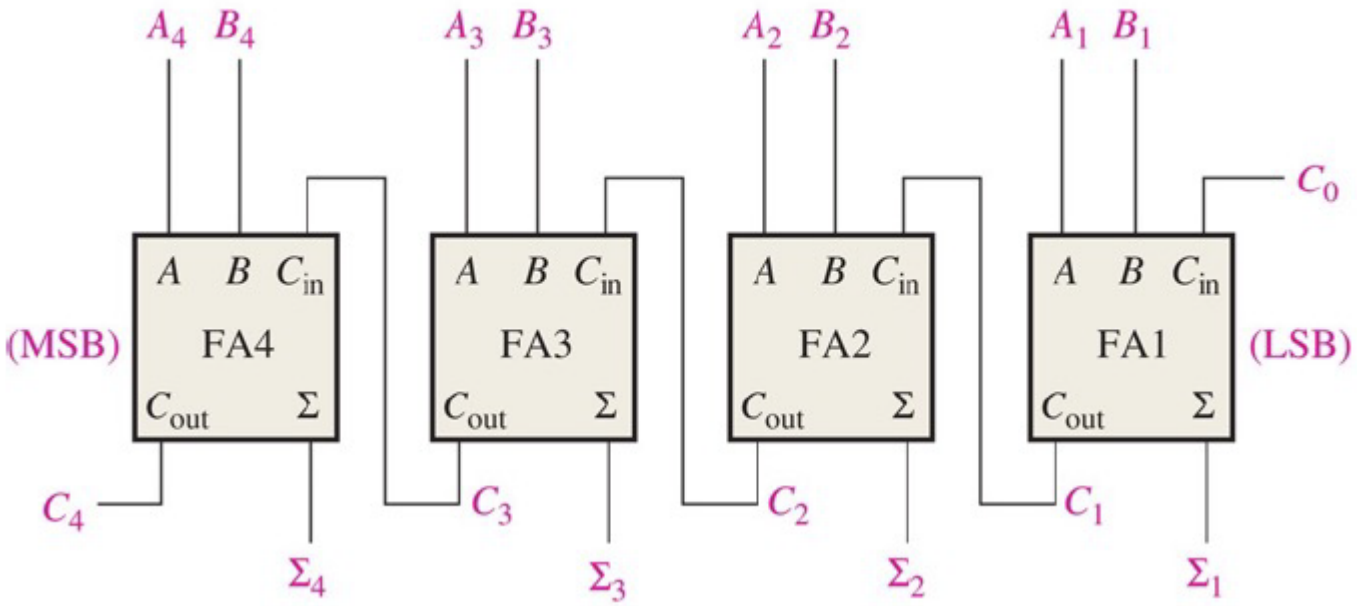


TABLE 6–3

Truth table for each stage of a 4-bit parallel adder.

C_{n-1}	A_n	B_n	Σ_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Combinational Building Blocks

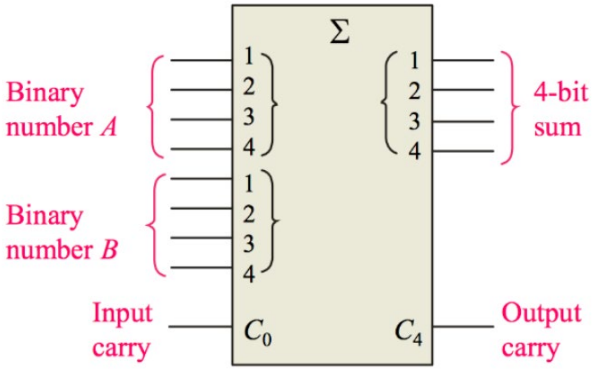
Q1. The following sequences of bits (right-most bit first) appear on the inputs to a 4-bit parallel adder. Determine the resulting sequence of bits on each sum output.

A_1	1010
A_2	1100
A_3	0101
A_4	1101
B_1	1001
B_2	1011
B_3	0000
B_4	0001

A_4	A_3	A_2	A_1	B_4	B_3	B_2	B_1	Σ_5	Σ_4	Σ_3	Σ_2	Σ_1
1	0	1	1	0	0	1	1	0	1	1	1	0
1	1	1	0	0	0	0	0	0	1	1	1	0
0	0	0	1	0	0	1	0	0	0	0	1	1
1	1	0	0	1	0	1	1	1	0	1	1	1

Combinational Building Blocks

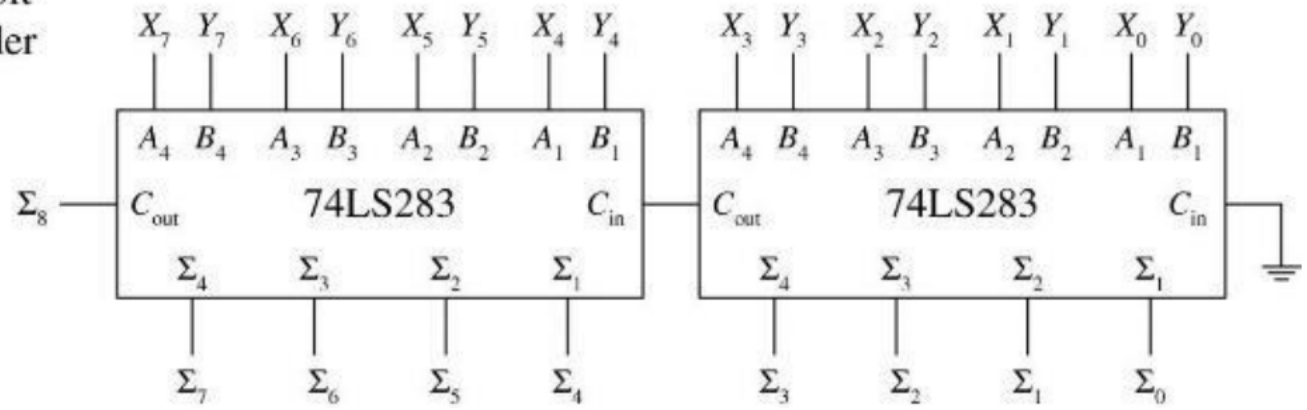
- 74LS283



Q2. How to combine 74LS283 into a 8-bit parallel adder?

Cascading two 74LS283 4-bit adders to create an 8-bit adder

$$\begin{array}{r} X_7\ X_6\ X_5\ X_4\ X_3\ X_2\ X_1\ X_0 \\ +\ Y_7\ Y_6\ Y_5\ Y_4\ Y_3\ Y_2\ Y_1\ Y_0 \\ \hline \Sigma_8\ \Sigma_7\ \Sigma_6\ \Sigma_5\ \Sigma_4\ \Sigma_3\ \Sigma_2\ \Sigma_1\ \Sigma_0 \end{array}$$

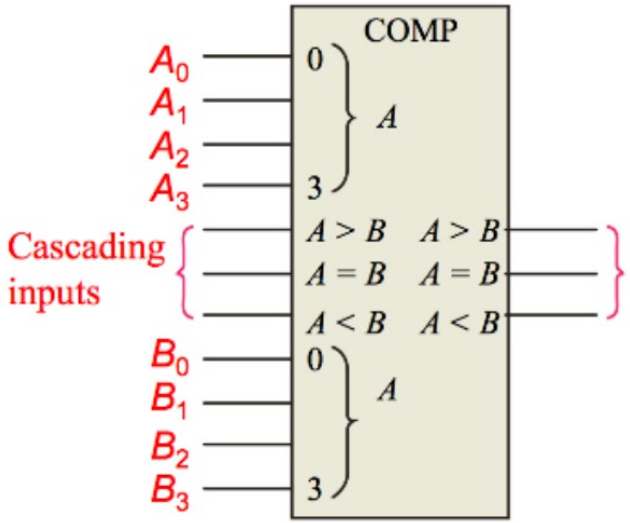


Combinational Building Blocks

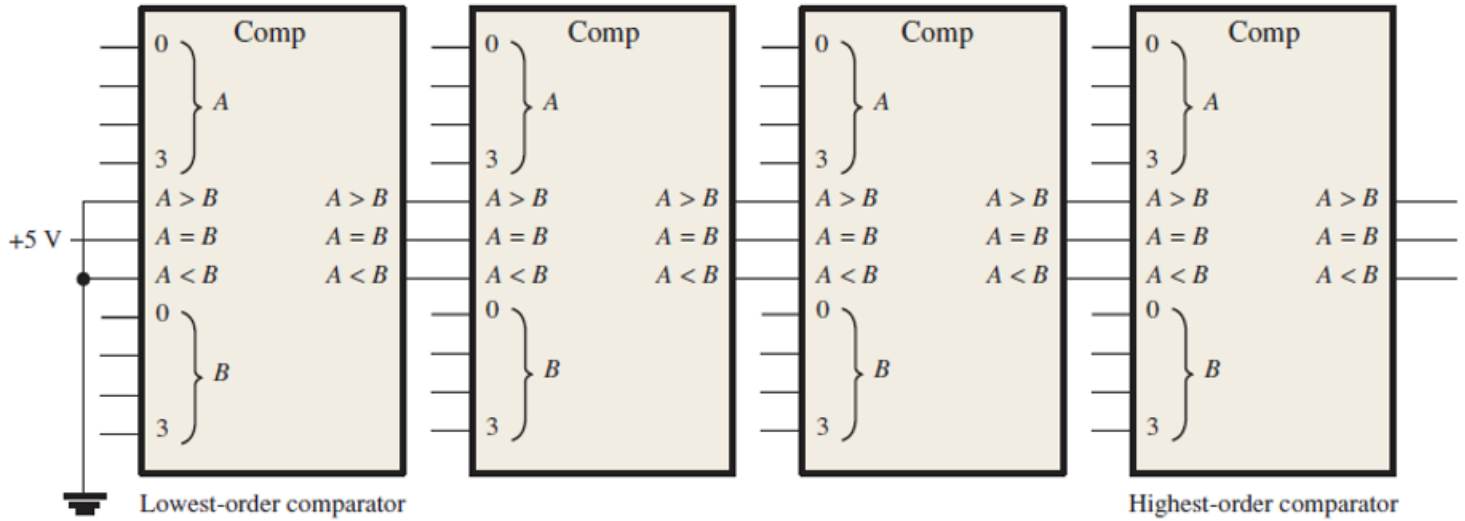
- Comparator

➢ Comparators provide outputs to indicate which of the numbers is larger or if they are equal.
➢ Cascading inputs are provided to expand the comparator to larger numbers.

74LS85



Q3. How to combine 74LS85 into a 16-bit comparators?



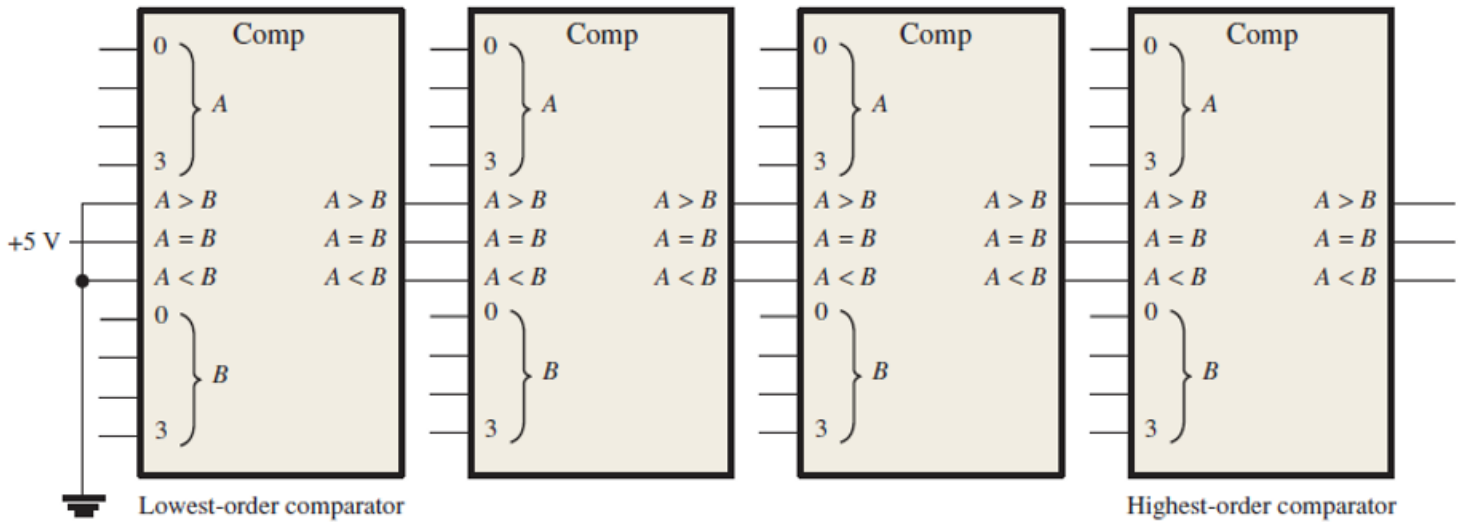
Combinational Building Blocks

Q3. How to combine 74LS85 into a 16-bit comparators?

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

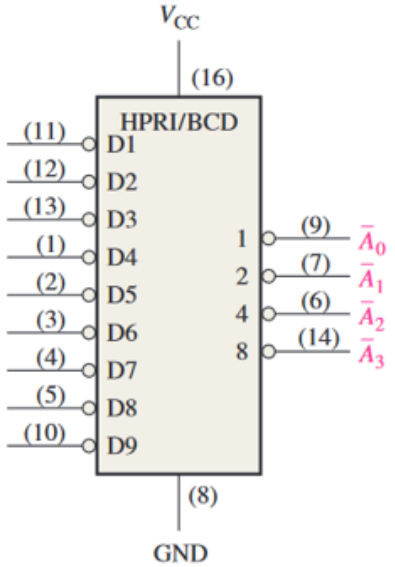
H = HIGH Level
L = LOW Level
X = IMMATERIAL



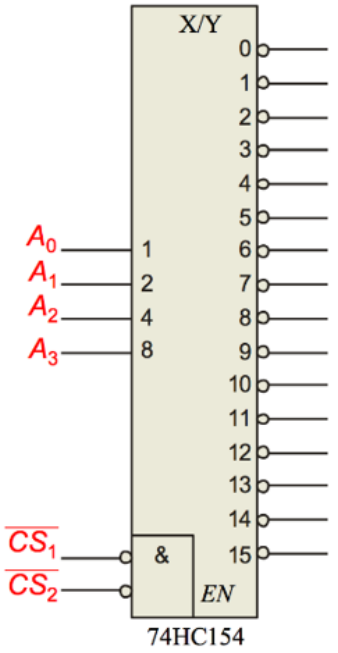
Combinational Building Blocks

- Encoder & Decoder
  - An encoder accepts an active logic level on one of its inputs and converts it to a coded output, such as BCD or binary.
  - An decoder has multiple outputs to decode any combination of inputs. For example, the binary-to-decimal decoder shown here has 16 outputs – one for each combination of binary inputs.

Encoder



Decoder



Combinational Building Blocks

Q4. How to combine 74HC154 into a 5-bit decoders?

- It includes two active LOW chip select lines which must be at the active level to enable the outputs.
- These lines can be used to expand the decoder to larger inputs.

Input						Output															
$\overline{E0}$	$\overline{E1}$	A0	A1	A2	A3	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
		L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
		H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
		H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
		L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
		H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
		L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
		H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
		L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
		H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
		L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

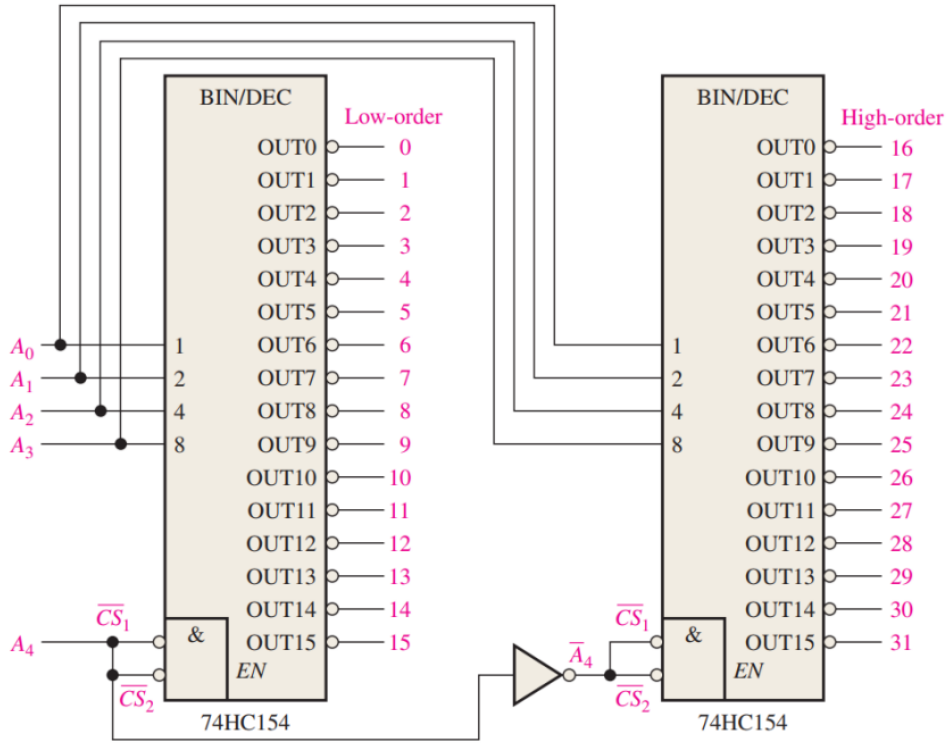


FIGURE 6–30 A 5-bit decoder using 74HC154s.

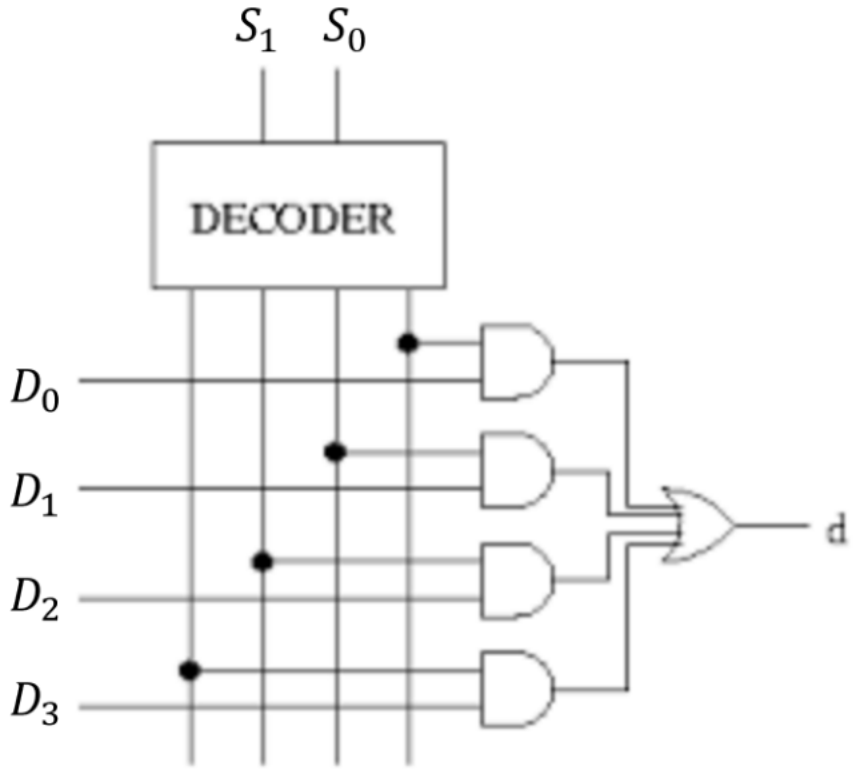
Combinational Building Blocks

Q5: Implement 4 to 1 Multiplexer using a Decoder.

- Multiplexer

Data selection for a 1-of-4-multiplexer.

Data-Select Inputs		
S_1	S_0	Input Selected
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3



Combinational Building Blocks

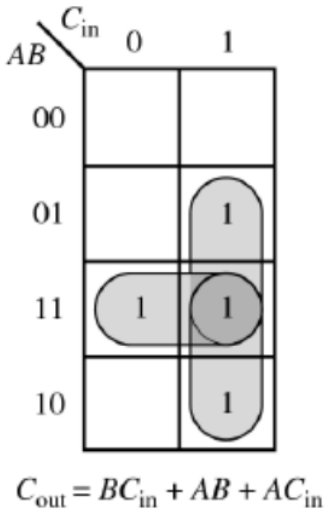
Q6: Using the truth table, write the SOP expressions for the ∑ and Cout of a full-adder. Use a Karnaugh map to minimize the expressions and then implement them with inverters and AND_x0002_ OR logic. Show how you can replace the AND-OR logic with 74HC151 data selectors.

Full-adder truth table.

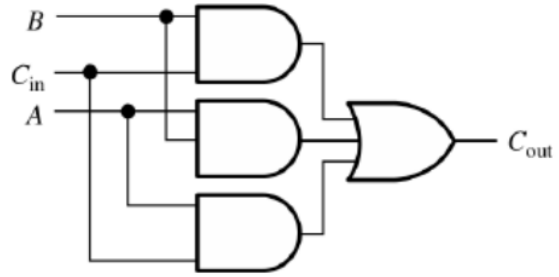
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

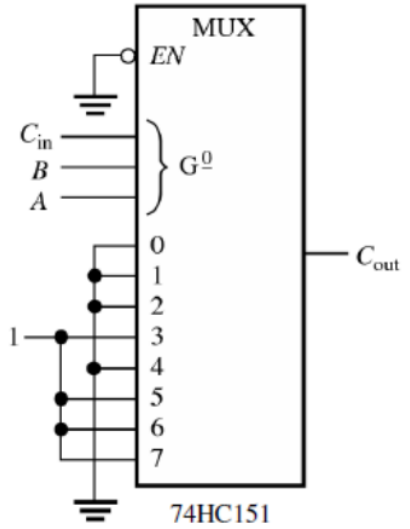
C_{in} = input carry, sometimes designated as *CI*
C_{out} = output carry, sometimes designated as *CO*
Σ = sum
A and B = input variables (operands)

$$C_{out} = ABC_{in} + \overline{A}BC_{in} + A\overline{B}C_{in} + AB\overline{C}_{in}$$



$$C_{out} = BC_{in} + AB + AC_{in}$$





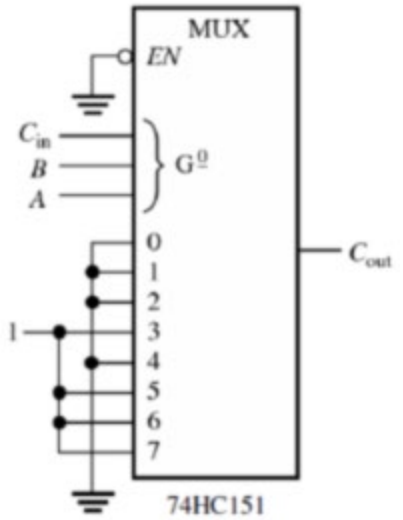
Combinational Building Blocks

Input												Output	
$\overline{E}$	S2	S1	S0	I0	I1	I2	I3	I4	I5	I6	I7	$\overline{Y}$	Y
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

Full-adder truth table.

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = input carry, sometimes designated as *CI*
C_{out} = output carry, sometimes designated as *CO*
Σ = sum
A and B = input variables (operands)

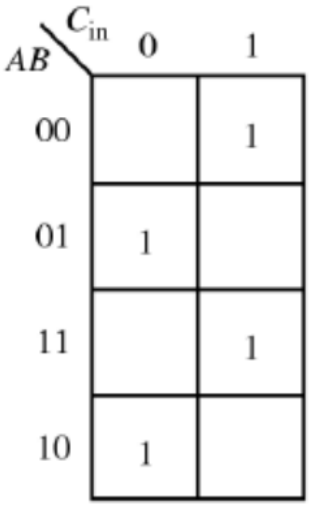


Combinational Building Blocks

Full-adder truth table.

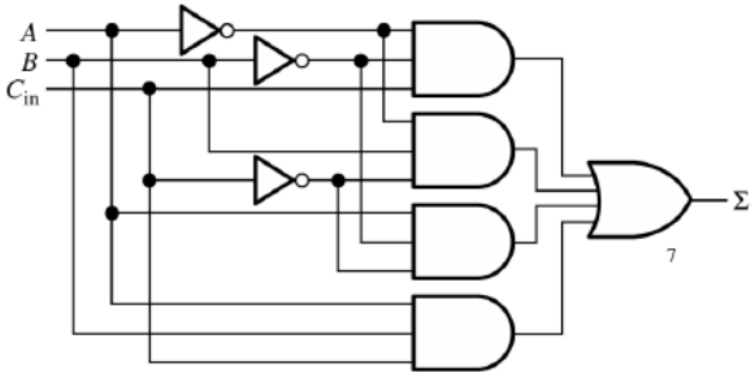
A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

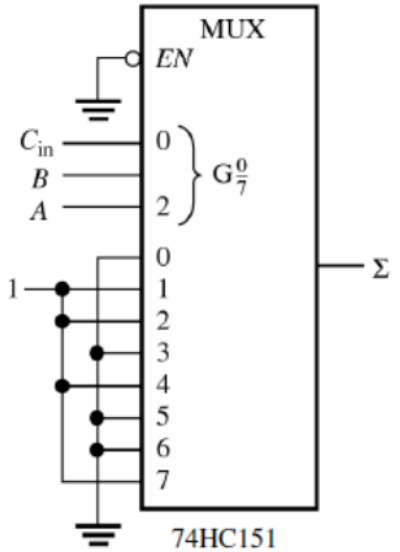
C_{in} = input carry, sometimes designated as *CI*
C_{out} = output carry, sometimes designated as *CO*
Σ = sum
A and B = input variables (operands)



Σ = No simplification

$$\Sigma = \overline{A}\,\overline{B}C_{in} + \overline{A}B\overline{C}_{in} + A\overline{B}\,\overline{C}_{in} + ABC_{in}$$

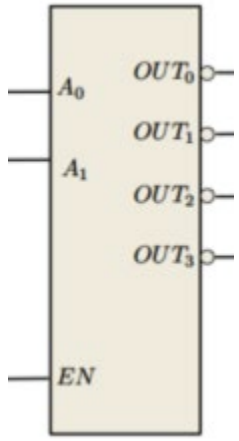




Combinational Building Blocks

Q7: Consider the boolean expressions as follows,

$$D_0 = X\bar{S}_1\bar{S}_0 + YS_1\bar{S}_0$$
$$D_1 = X\bar{S}_1S_0 + YS_1S_0$$
$$D_2 = XS_1\bar{S}_0 + Y\bar{S}_1\bar{S}_0$$
$$D_3 = XS_1S_0 + Y\bar{S}_1S_0$$



Design a circuit to implement the boolean expressions using 1-of-4 decoders as shown in Figure 13 and NAND gates, where the truth table of 1-of-4 decoder is shown in Table 4. (Connect ALL input pins as needed. You may assume that complementary inputs, if needed, are directly available - e.g., both A_0 and $\bar{A}_0$ are available).

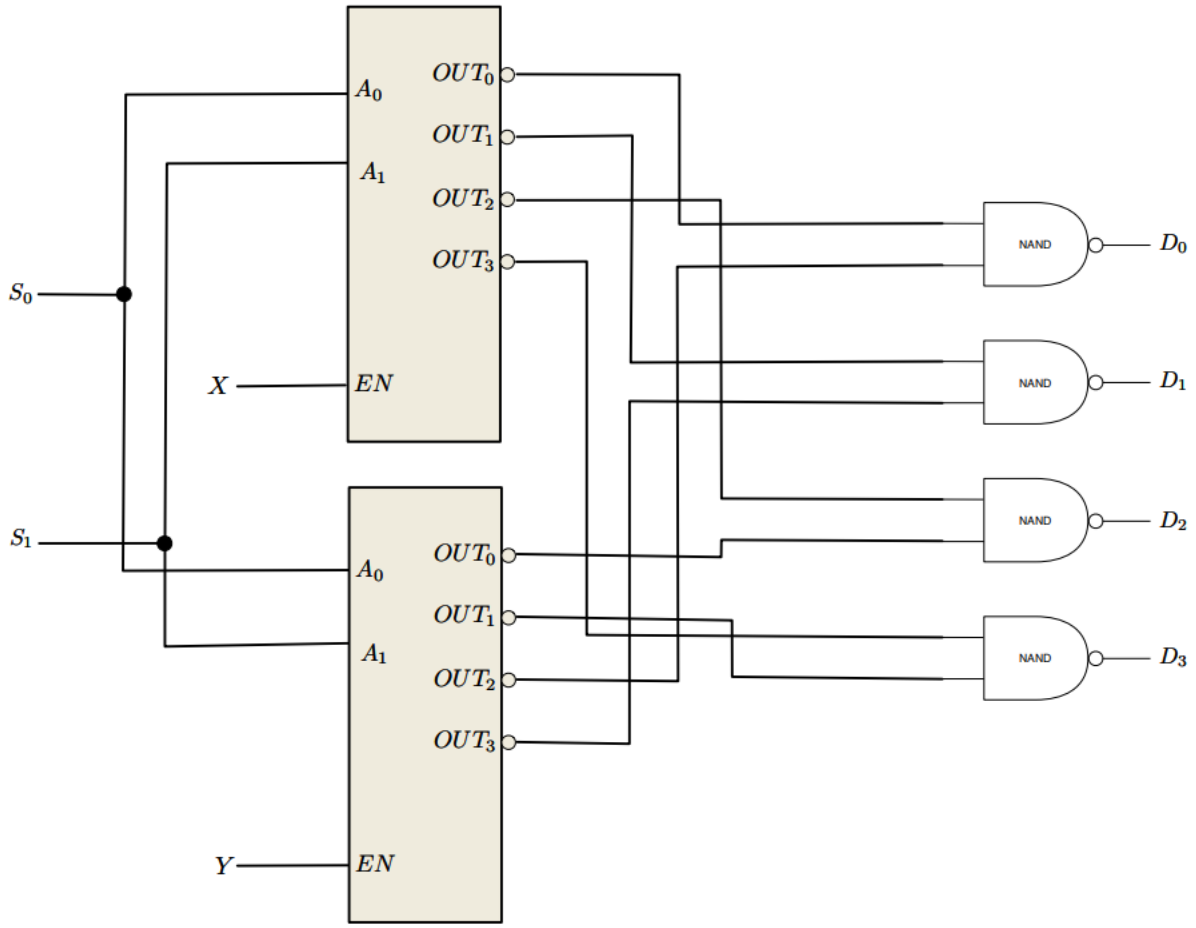
EN	A_1	A_0	OUT_0	OUT_1	OUT_2	OUT_3
0	X	X	1	1	1	1
1	0	0	0	1	1	1
1	0	1	1	0	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	0

Combinational Building Blocks

Q7:

Consider the boolean expressions as follows,

$$D_0 = X\bar{S}_1\bar{S}_0 + YS_1\bar{S}_0$$
$$D_1 = X\bar{S}_1S_0 + YS_1S_0$$
$$D_2 = XS_1\bar{S}_0 + Y\bar{S}_1\bar{S}_0$$
$$D_3 = XS_1S_0 + Y\bar{S}_1S_0$$



香港中文大學（深圳）
The Chinese University of Hong Kong, Shenzhen

Thank You!