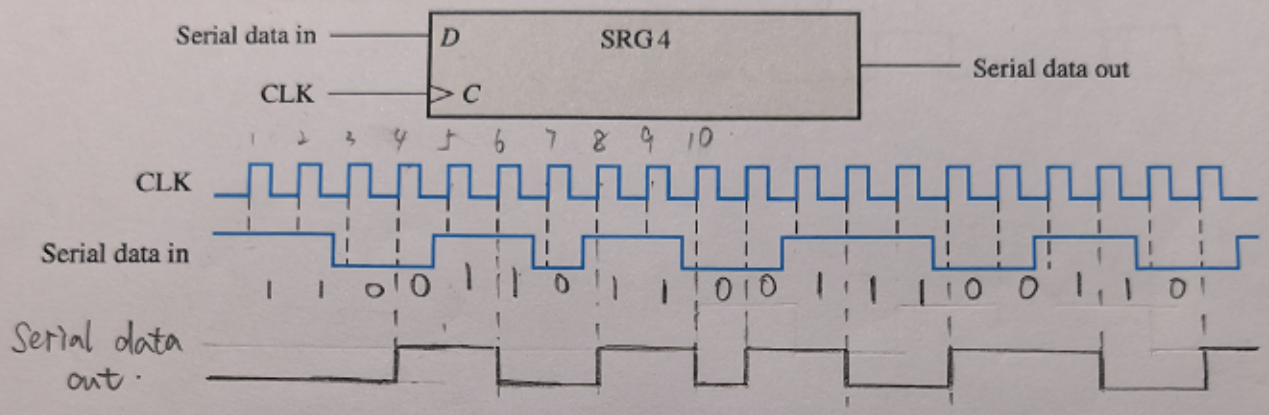
WX

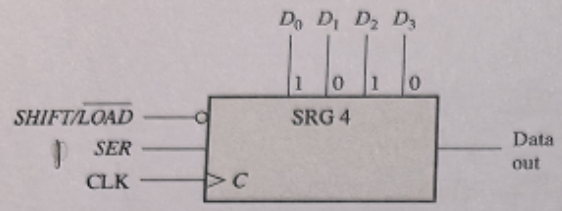
ECE2050 Homework 7

Due: April 18, 2025

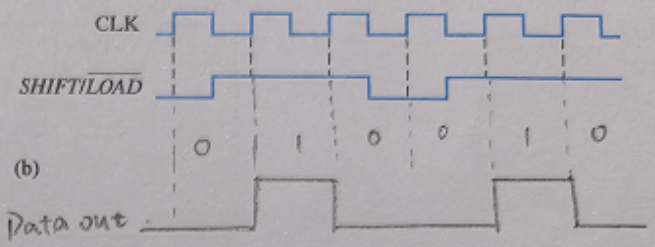
Q1 For the serial in/serial out shift register, determine the data-output waveform for the data-input and clock waveforms below. Assume that the register is initially cleared.



Q2 The shift register below has $SHIFT/\overline{LOAD}$ and CLK inputs as shown in part (b). The serial data input (SER) is a 1. The parallel data inputs are $D_0 = 1, D_1 = 0, D_2 = 1$, and $D_3 = 0$ as shown. Develop the data-output waveform in relation to the inputs.

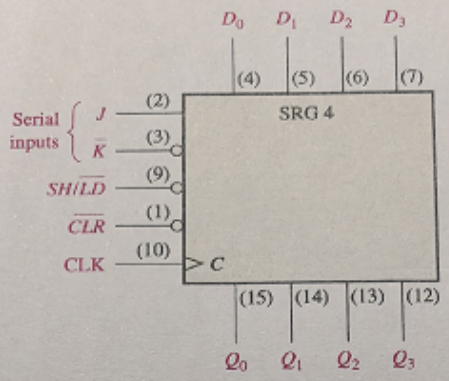


(a)

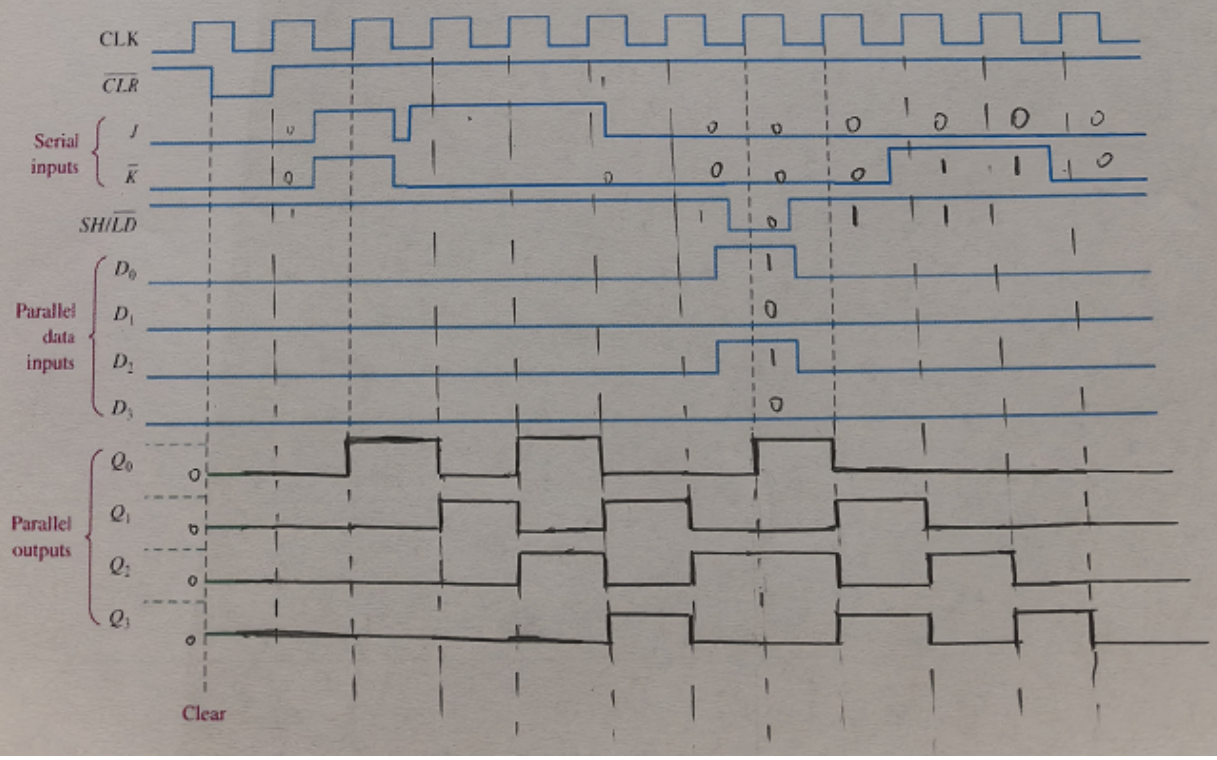


(b)

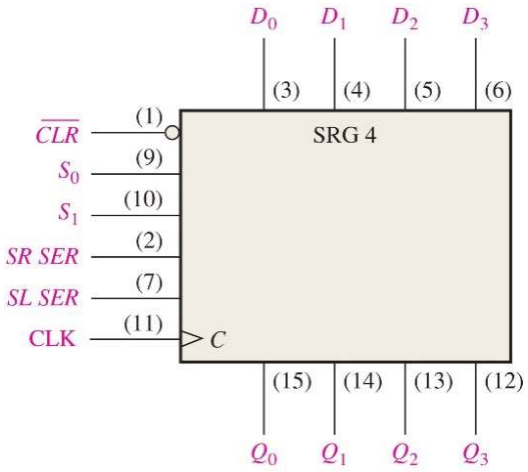
Q3 The truth table of a 74HC195 4-bit shift register is shown below. Its input $\overline{CLR}$ is asynchronous. Develop the outputs Q_0, Q_1, Q_2 and Q_3 waveforms in relation to the inputs.

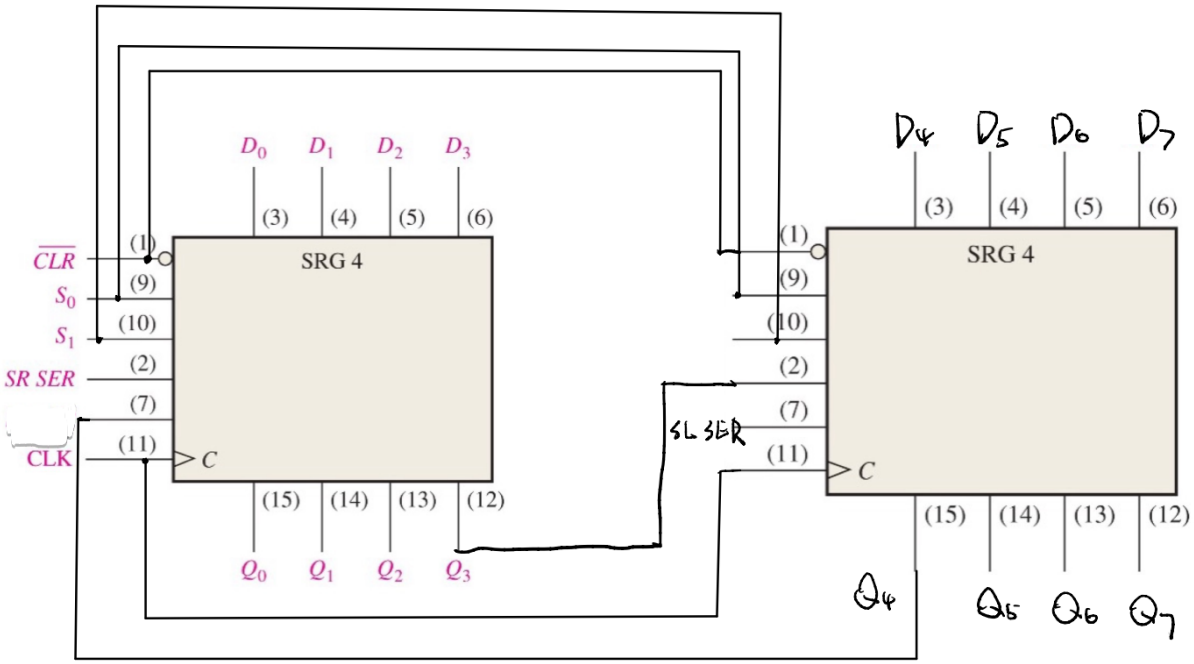


Inputs							Outputs			
$SH/\overline{LD}$	J	$\overline{K}$	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3
0	X	X	d_0	d_1	d_2	d_3	d_0	d_1	d_2	d_3
1	1	1	X	X	X	X	1	q_0	q_1	q_2
1	1	0	X	X	X	X	$\overline{q_0}$	q_0	q_1	q_2
1	0	1	X	X	X	X	q_0	q_0	q_1	q_2
1	0	0	X	X	X	X	0	q_0	q_1	q_2

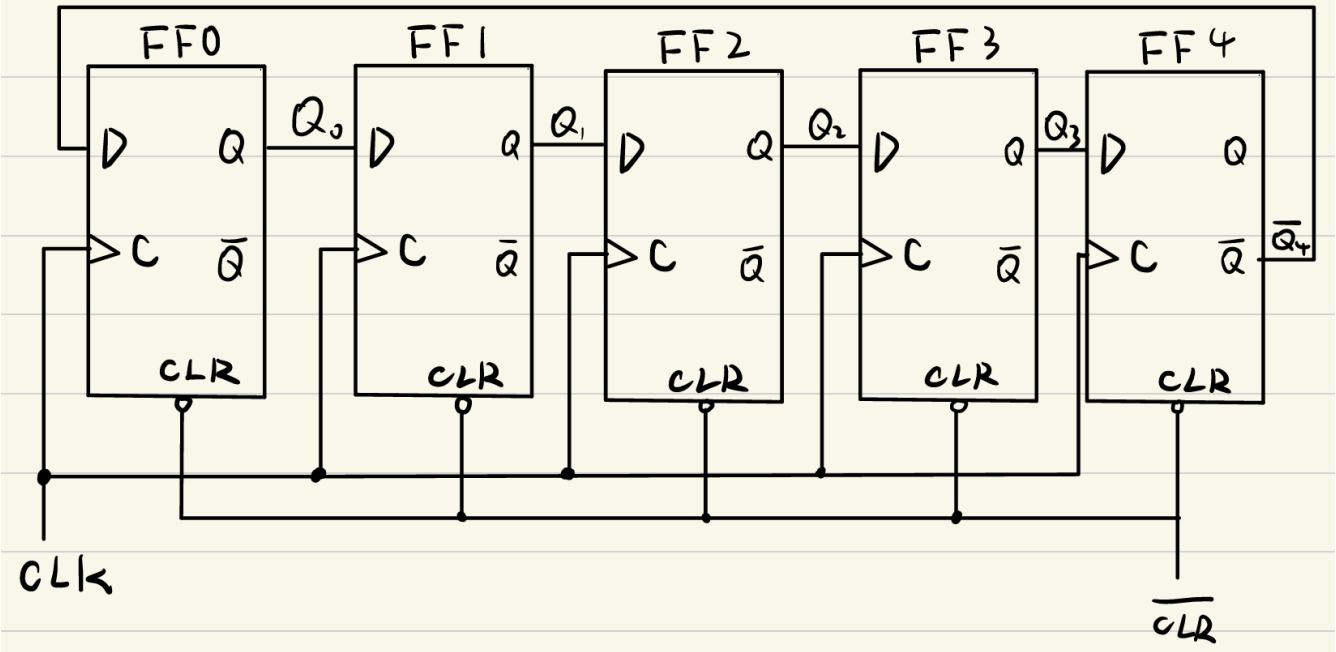


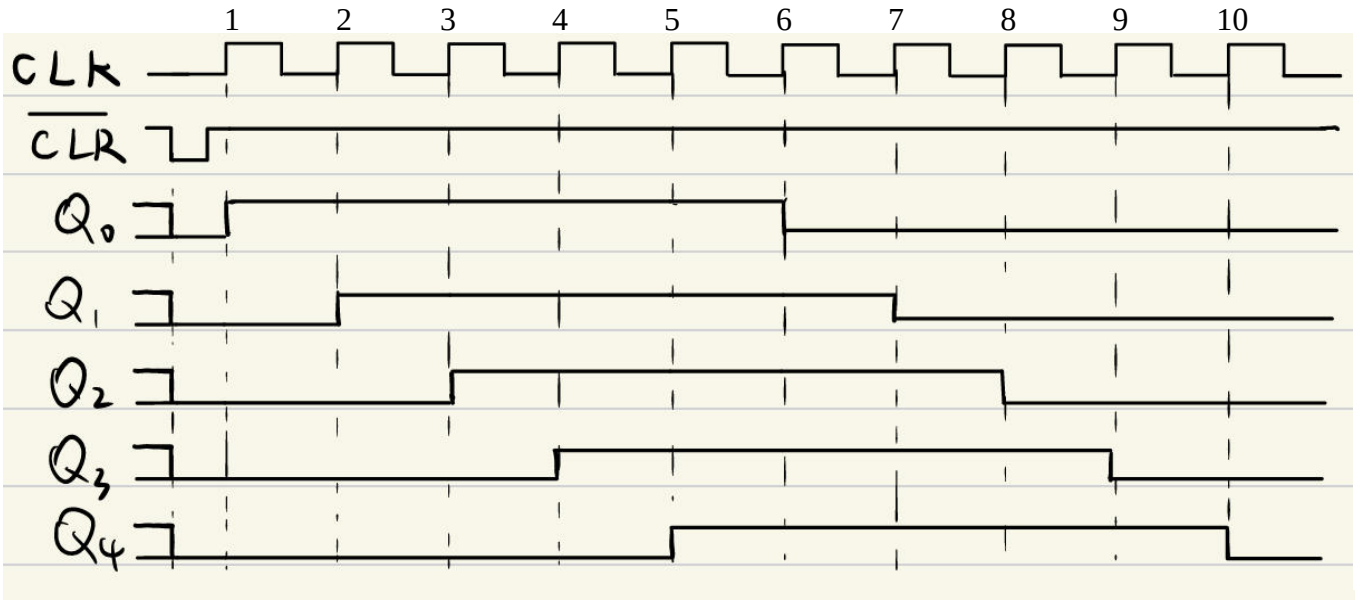
Q4 Use two 4-bit bidirectional universal shift registers below to form an 8-bit bidirectional universal shift register. Show the required connections.





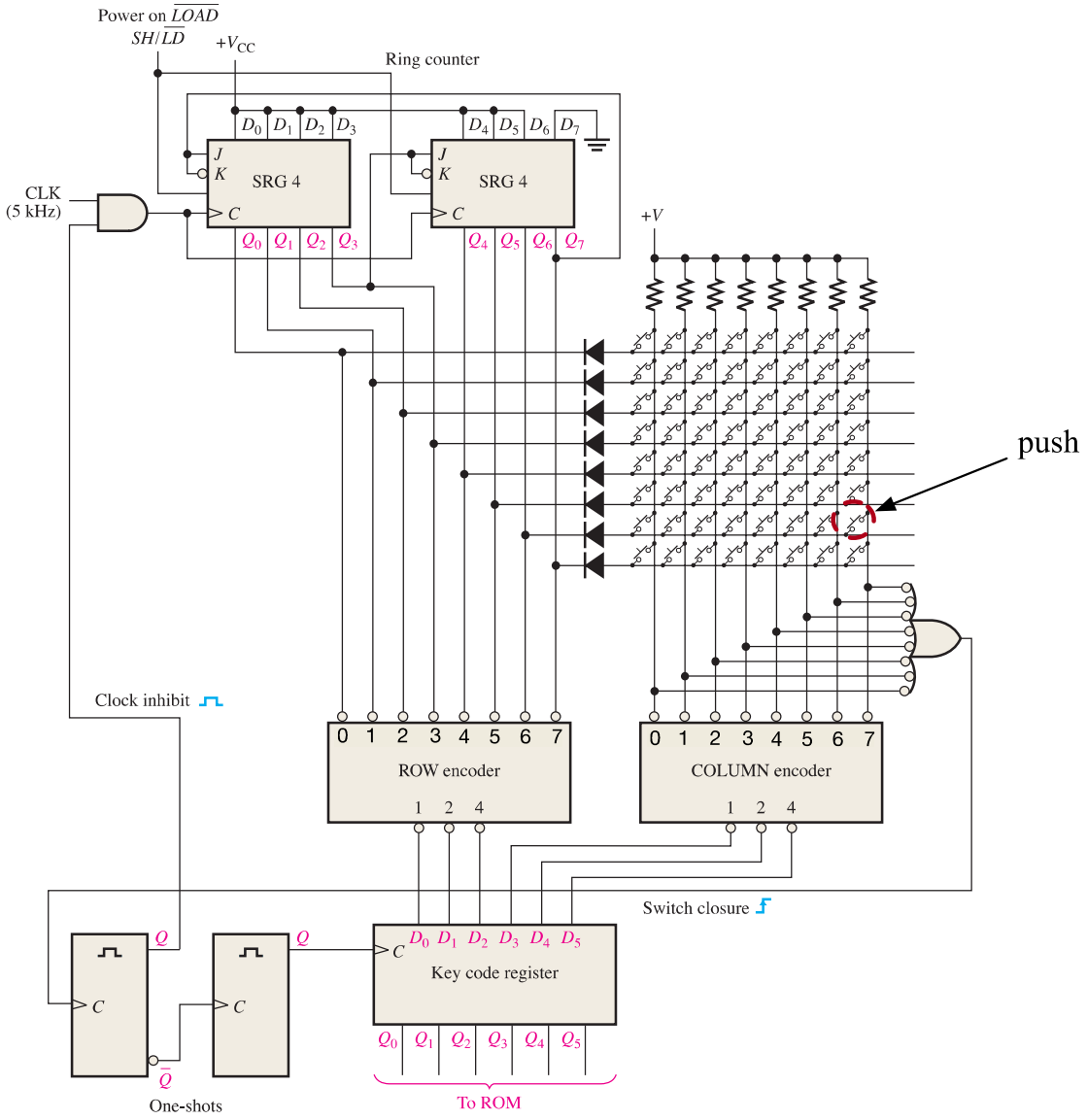
Q5 Draw the logic diagram for a modulus-10 Johnson counter. Show the timing diagram and write the sequence in tabular form.





Clock Pulse	Q_0	Q_1	Q_2	Q_3	Q_4
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

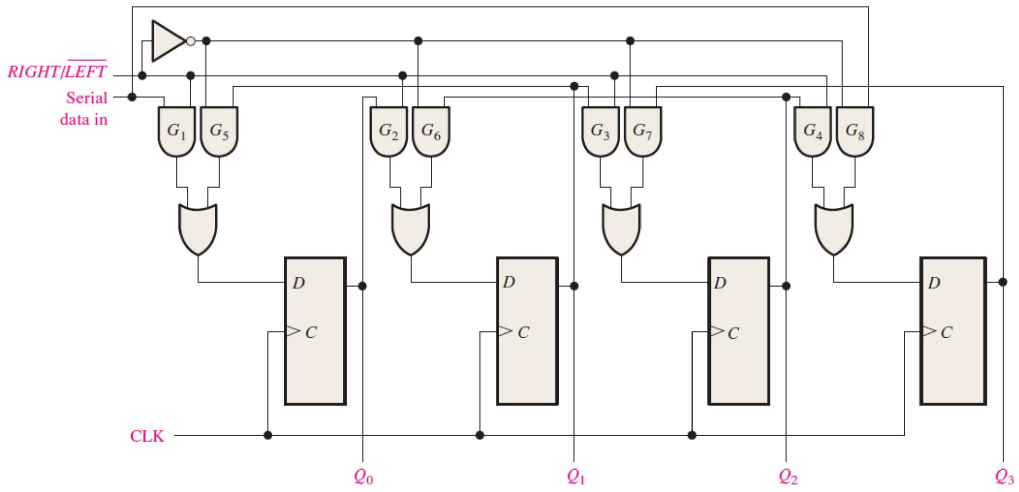
Q6 If we push the button labeled as "push" in the figure, what are the outputs of the ROW encoder and COLUMN encoder?



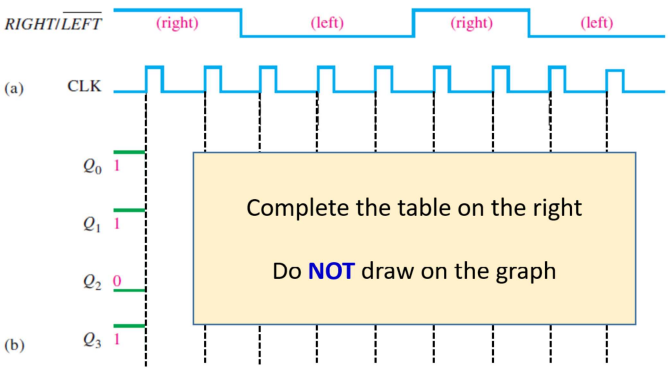
Row encoder
D0D1D2: 100

Column encoder
D3D4D5: 000

Q7 The following figure shows a 4-bit bidirectional shift register. A HIGH on the RIGHT/$\overline{\text{LEFT}}$ control input allows data bits inside the register to be shifted to the right, and a LOW enables data bits inside the register to be shifted to the left.



Determine the state of the shift register above after each clock pulse for the given RIGHT/LEFT control input waveform shown below. Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and that the serial data-input line is LOW.



CLK	Q_0	Q_1	Q_2	Q_3
0	1	1	0	1
1	0	1	1	0
2	0	0	1	1
3	0	1	1	0
4	1	1	0	0
5	1	0	0	0
6	0	1	0	0
7	0	0	1	0
8	0	1	0	0