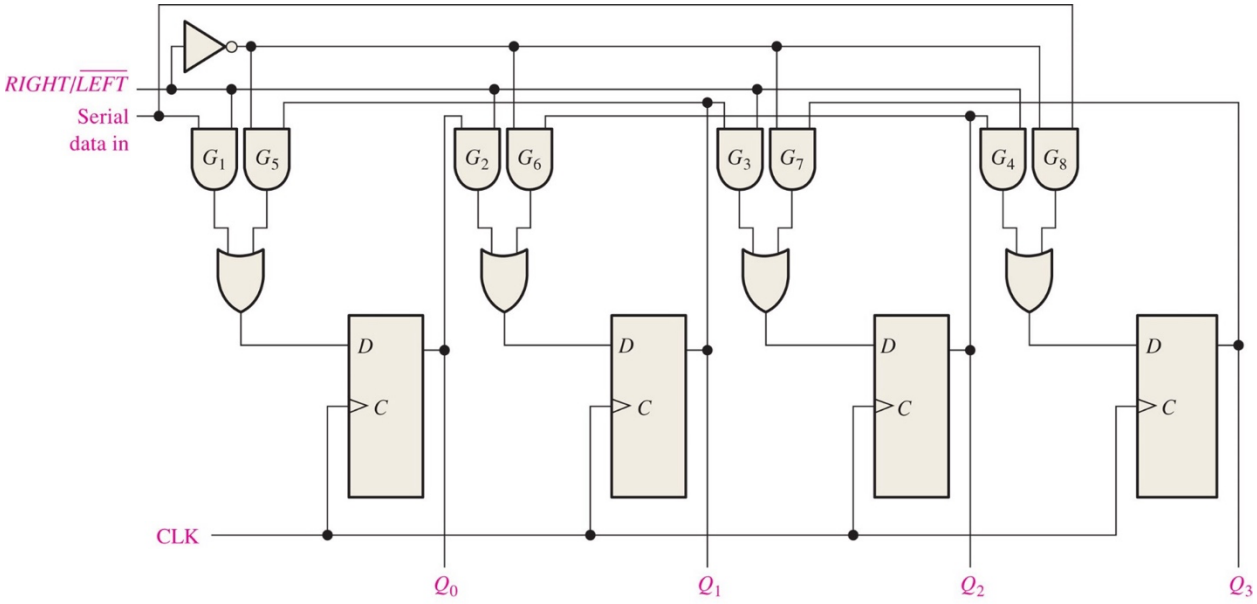
ECE2050 Digital Logic and Systems

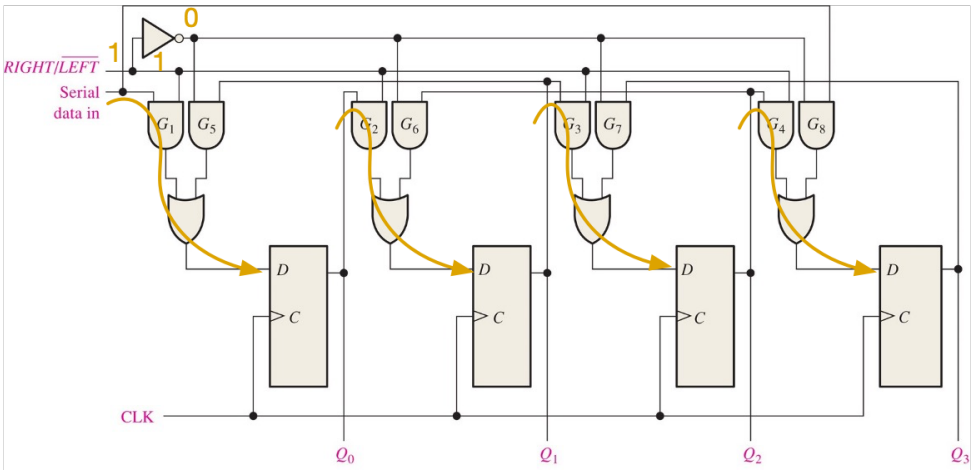
Project: Bidirectional Shift Registers

- **Objectives and Aims:**
  - Get familiar with the hardware programming language VHDL
  - Study the use of different architectural design methods
  - Study the use of combinational and sequential logics

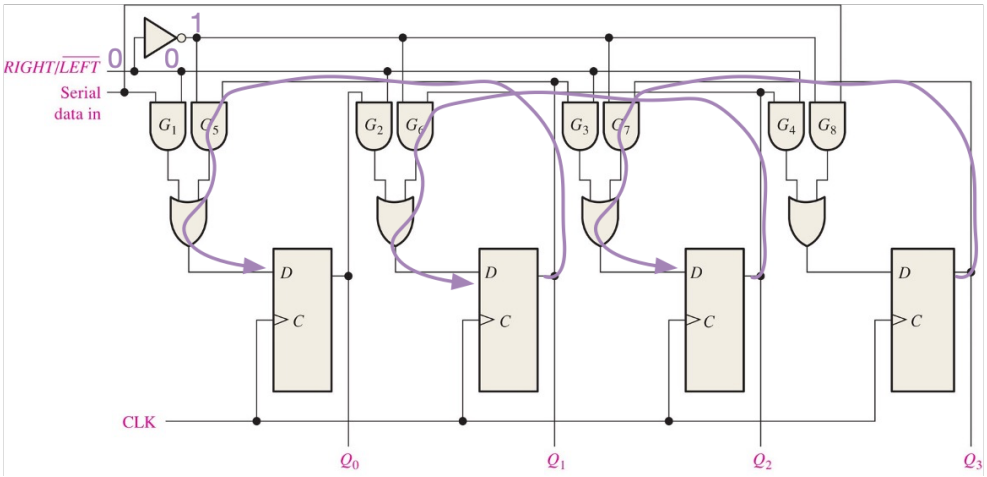
- **Exercise:** In this project, you need to implement a **Bidirectional Shift Register**, which is composed of **4 D-Flip-Flops (D-FF) and some basic logic gates** as follows:



  - RIGHT/$\overline{\text{LEFT}}$ controls data bits inside the register to be shifted left or right.
  - When RIGHT/$\overline{\text{LEFT}}$ is HIGH, $G_1 \sim G_4$ are enabled, and the state of the Q output of each flip-flop is passed through to the D input of the **following** flip-flop.



- When RIGHT/$\overline{\text{LEFT}}$ is LOW, $G_5 \sim G_8$ are enabled, and the Q output of each flip-flop is passed through to the D input of the **preceding** flip-flop.



■ Requirements:

- Implement a Bidirectional Shift Register, which is composed of 4 D-Flip-Flops (D-FF) using the `structural design` (`port map`) and some basic logic gates.
  - That is, implement the D-Flip-Flop first, and then use D-Flip-Flop and basic logic gates to implement the Bidirectional Shift Register.
  - Write down a testbench to verify the Bidirectional Shift Register function (timing diagram).
  - You can use Verilog HDL if you are familiar with it.
- Submission Rule:

    - Submit your (1) source code(s) (.vhd), (2) testbench (.vhd), and (3) the behavior simulation result (a screen shot) to BB.
    - If using Verilog HDL, submit your (1) source code(s) (.v), (2) testbench (.v), and (3) the behavior simulation result (a screen shot) to BB.
- Deadline: May 5, 2025.