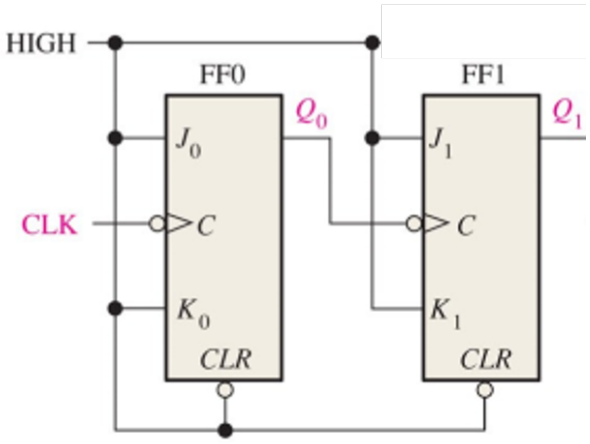
ECE2050 Homework 8

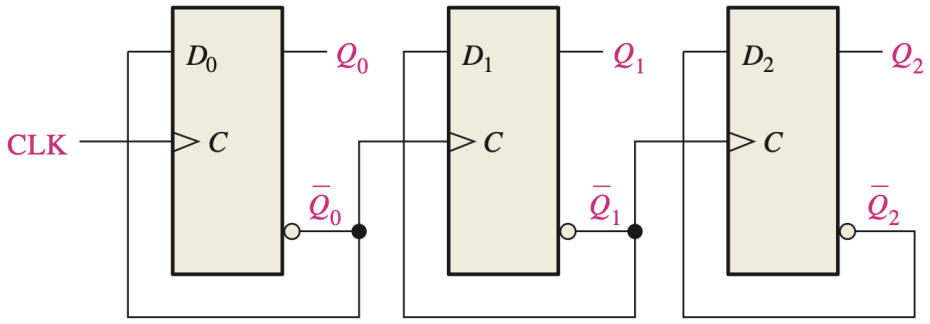
Due: April 28, 2025

Q1 For the ripple counter shown below, please fill in the logic level for Q_1 and Q_0 for seven clock pulses, assuming the initial state is 00.



Clock Pulse	Q1	Q0
Initially	0	0
1	0	1
2	1	0
3	1	1
4	0	0
5	0	1
6	1	0
7	1	1

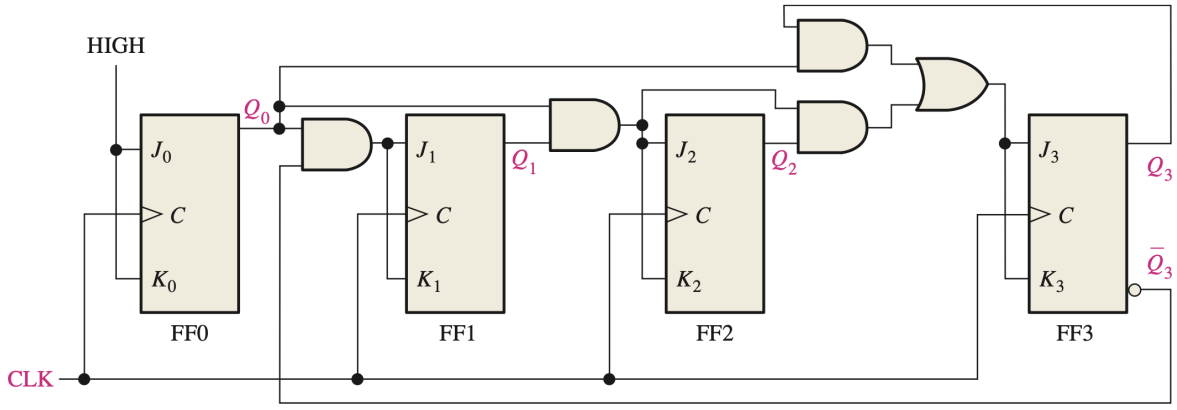
Q2 For the ripple counter below, assume that each flip-flop has a propagation delay from the triggering edge of the clock to a change in the Q output of 8 ns. Determine the worst-case (longest) delay time from a clock pulse to the arrival of the counter in a given state. Specify the state or states for which this worst-case delay occurs.



$t_{p(max)}$ = 3(8 ns) = **24 ns**

Worst-case delay occurs when all flip-flops change state from 011 to 100 or from 111 to 000.

Q3 Please write down the boolean expressions to get J and K inputs to each flip-flop. Please fill in the state sequence table for 10 clock cycles. Explain how these conditions in each case cause the counter to go to the next proper state.



Clock Pulse	Q3	Q2	Q1	Q0
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

$J_0 = K_0 = 1$

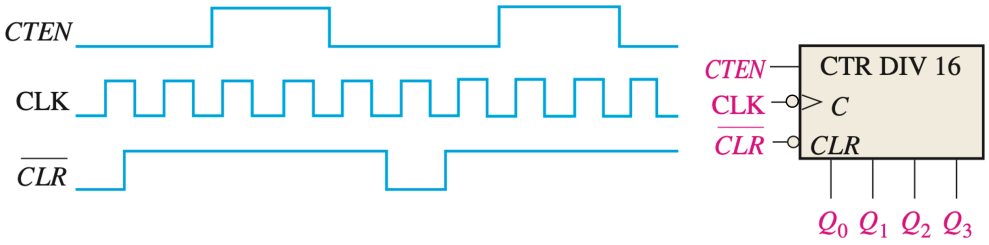
$J_1 = K_1 = Q_0\bar{Q}_3$

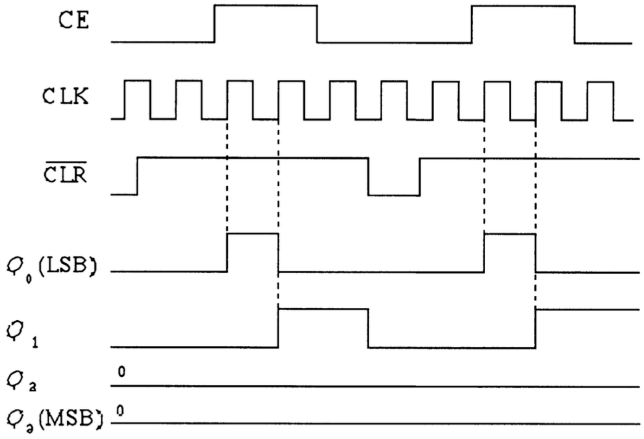
$J_2 = K_2 = Q_0Q_1$

$J_3 = K_3 = Q_0Q_1Q_2 + Q_0Q_3$

Function: Decade counter through a BCD sequence.

Q4 The waveforms below are applied to the count enable, clear, and clock inputs as indicated. Show the counter output waveforms in proper relation to these inputs. The clear input is asynchronous.





Q5 What type is the state machine in Fig. 1? Using binary state encoding, complete a state transition table and output table for the FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

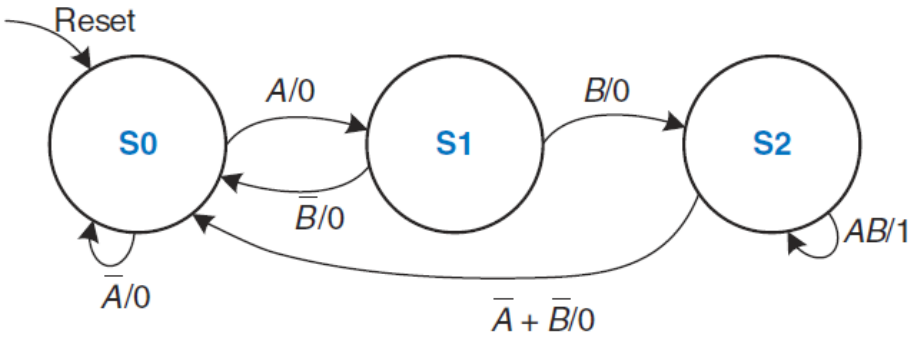


Figure 1: State Transition diagram for Q5

Mealy FSM.

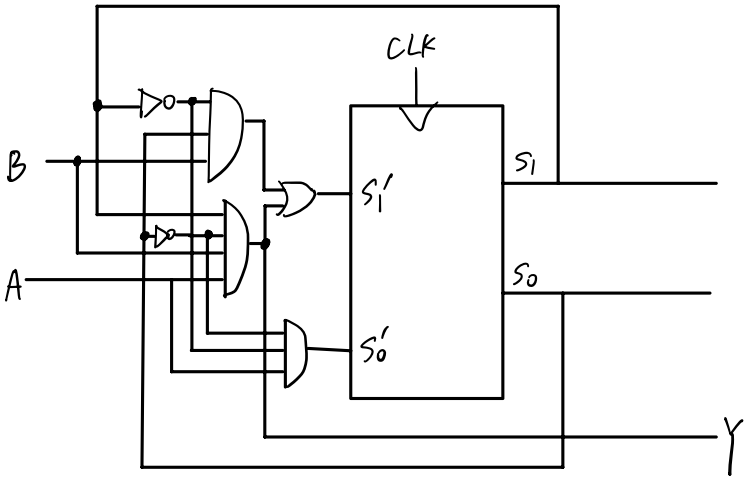
State	$S_{1:0}$ Encoding
S_0	00
S_1	01
S_2	10

Current State		Input		Next State		Output
S_1	S_0	A	B	S_1'	S_0'	Y
0	0	0	X	0	0	0
0	0	1	X	0	1	0
0	1	X	0	0	0	0
0	1	X	1	1	0	0
1	0	1	1	1	0	1
1	0	0	X	0	0	0
1	0	1	0	0	0	0

$S_1' = \bar{S_1} S_0 B + S_1 \bar{S_0} AB$

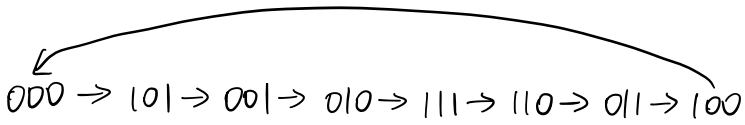
$S_0' = \bar{S_1} \bar{S_0} A$

$Y = S_1 \bar{S_0} AB$



Q6 Design a counter to produce the following binary sequence. Use J-K flip-flops.

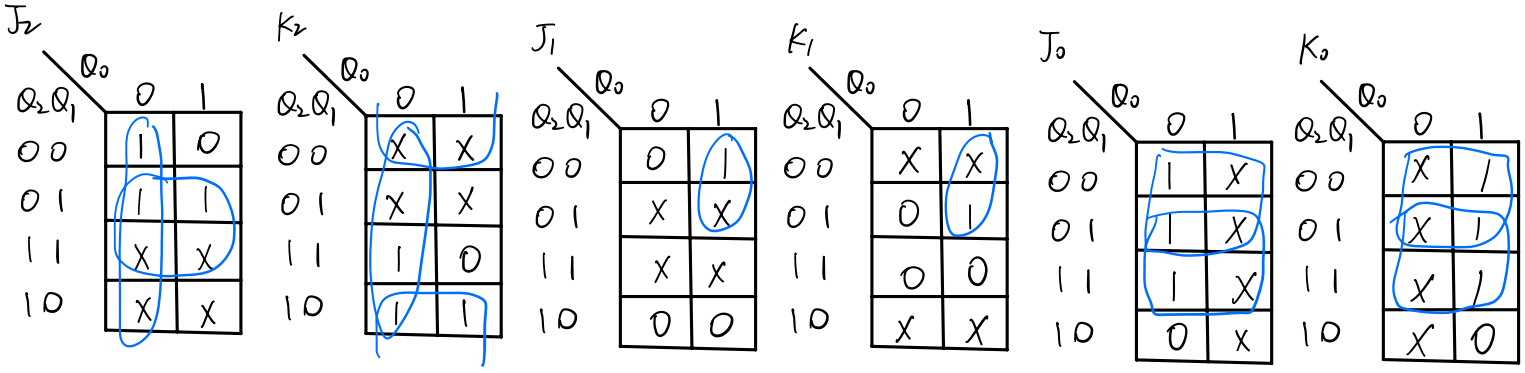
$$0, 5, 1, 2, 7, 6, 3, 4, 0 \ldots$$



0→0 0X 0→1 1X

1→1 X0 1→0 X1

Current state			Next state			Flip-Flop Inputs					
Q_2	Q_1	Q_0	Q_2'	Q_1'	Q_0'	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	1	0	1	1	X	0	X	1	X
1	0	1	0	0	1	X	1	0	X	X	0
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	1	1	1	X	X	0	1	X
1	1	1	1	1	0	X	0	X	0	X	1
1	1	0	0	1	1	X	1	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X

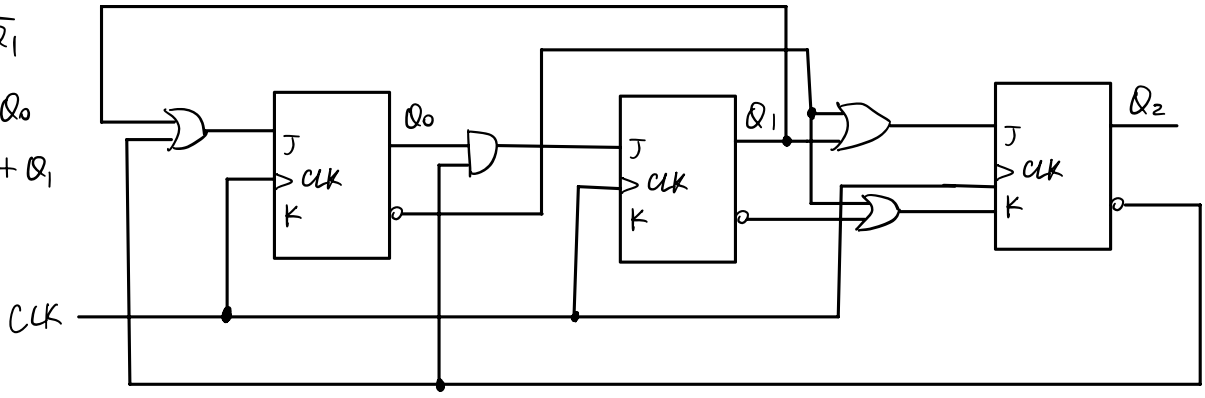


$J_2 = \bar{Q}_0 + Q_1$

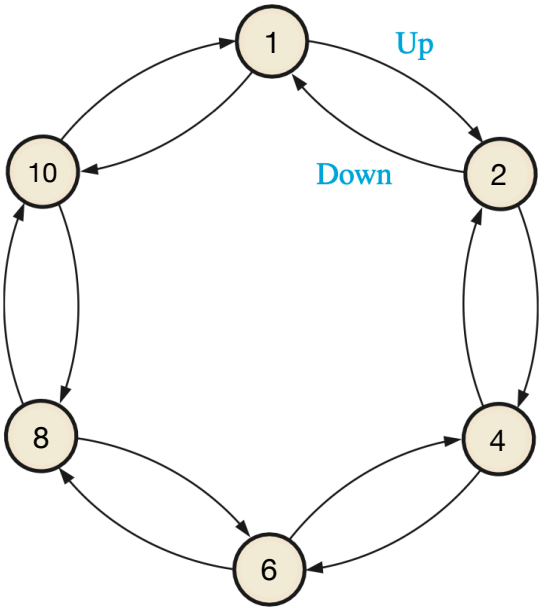
$K_2 = \bar{Q}_0 + \bar{Q}_1$

$J_1 = K_1 = \bar{Q}_2 Q_0$

$J_0 = K_0 = \bar{Q}_2 + Q_1$

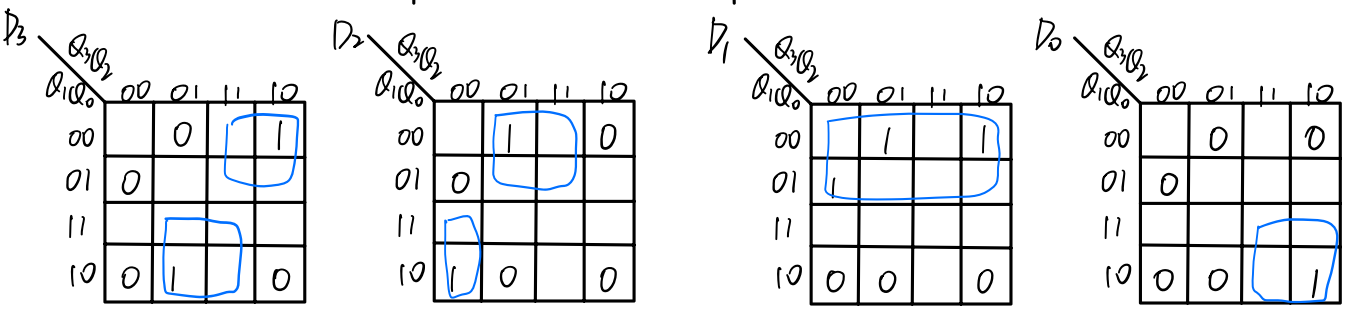


Q7 Design a binary counter with the sequence shown in the below state diagram.

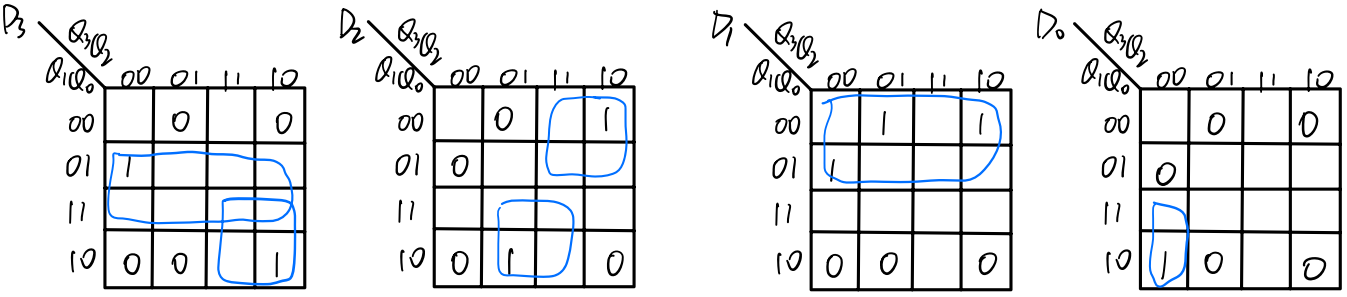


Current State				Next State (Up, Y=1)				Next State (Down, Y=0)			
Q_3	Q_2	Q_1	Q_0	Q_3'	Q_2'	Q_1'	Q_0'	Q_3'	Q_2'	Q_1'	Q_0'
0	0	0	1	0	0	1	0	1	0	1	0
0	0	1	0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	1	0	0	0	1	0
0	1	1	0	1	0	0	0	0	1	0	0
1	0	0	0	1	0	1	0	0	1	1	0
1	0	1	0	0	0	0	1	1	0	0	0

Y=1



Y=0

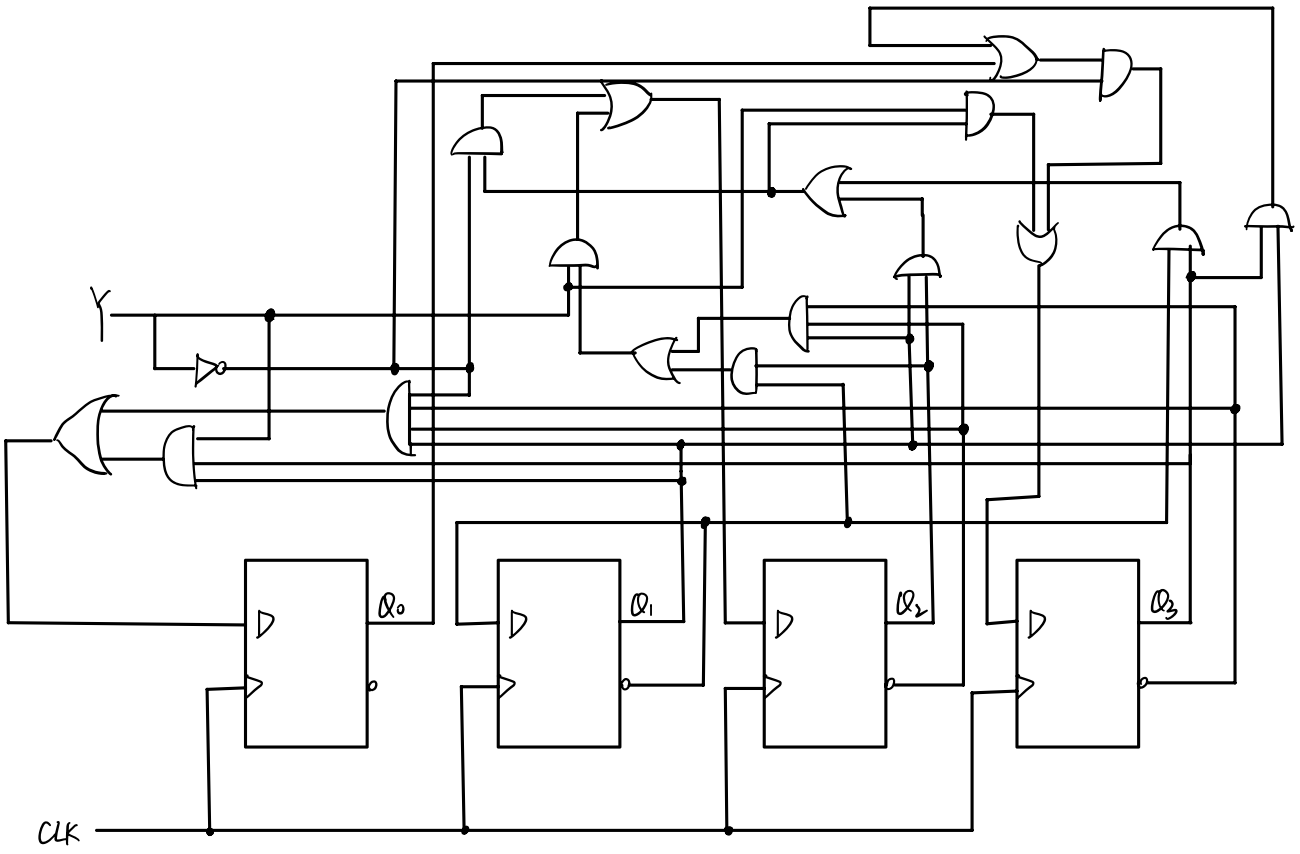


$D_3 = Y(Q_3\bar{Q}_1 + Q_2Q_1) + \bar{Y}(Q_0 + Q_3Q_1)$

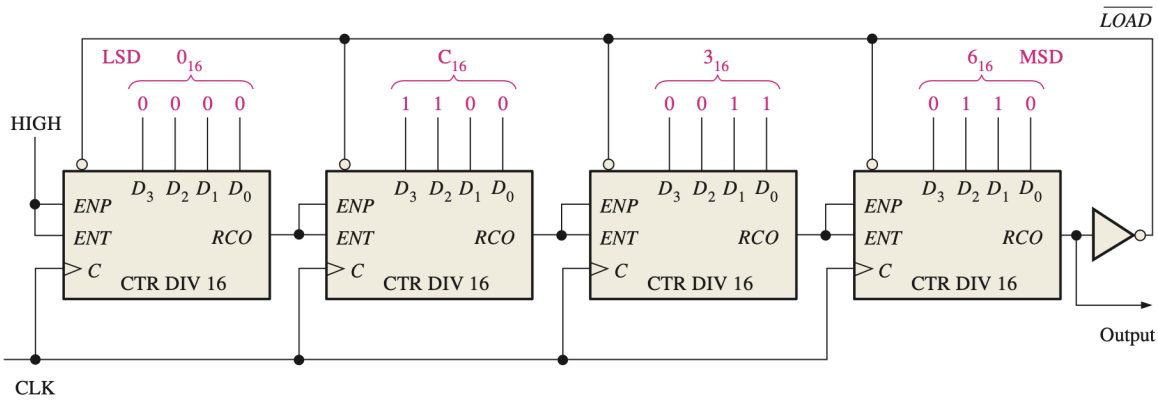
$D_2 = Y(Q_2\bar{Q}_1 + \bar{Q}_3\bar{Q}_2Q_1) + \bar{Y}(Q_3\bar{Q}_1 + Q_2Q_1)$

$D_1 = \bar{Q}_1$

$D_0 = YQ_3Q_1 + \bar{Y}\bar{Q}_3\bar{Q}_2Q_1$



Q8 Develop a table for use in testing the counter below that will show the frequency at the final RCO output for all possible open failures (assume the logical level for the open port is high) of the parallel data inputs (D_0, D_1, D_2, and D_3) taken one at a time. Use 10MHz as the test frequency for the clock.



Stage	Open	Loaded Count	f_{out}
1	0	63C1	250.006 Hz
1	1	63C2	250.012 Hz
1	2	63C4	250.025 Hz
1	3	63C8	250.050 Hz
2	0	63D0	250.100 Hz
2	1	63E0	250.200 Hz
2	2	63C0	250 Hz
2	3	63C0	250 Hz
3	0	63C0	250 Hz
3	1	63C0	250 Hz
3	2	67C0	256.568 Hz
3	3	6BC0	263.491 Hz
4	0	73C0	278.520 Hz
4	1	63C0	250 Hz
4	2	63C0	250 Hz
4	3	E3C0	1.383 kHz