Final Examination

(Time allowed: 180 minutes)
December 22, 2020

NOTE: Answer ALL **10** questions. Show all intermediate steps, except Question 1.

1. (10 points) Are the following statements necessarily true (Y) or not (N)?

(1) The dual symbol for a NAND gate is a negative-AND symbol.

(2) A multiplexer is a logic circuit that allows digital information from a single source to be routed onto several lines.

(3) When both the J and K inputs are HIGH, an edge-triggered J-K flip-flop changes state on each clock pulse.

(4) A one-shot is also known as an astable multivibrator.

(5) An edge-triggered D flip-flop changes state whenever the D input changes.

(6) Flip-flops and latches are both bistable devices.

(7) The modulus of an 8-bit Johnson counter is eight.

(8) A shift register with four stages can store a maximum count of fifteen.

(9) A typical FPGA has a greater gate density than a CPLD.

(10) Static RAMs must be periodically refreshed to retain data.

Solution:

(1) N
(2) N
(3) Y
(4) N
(5) N
(6) Y
(7) N
(8) Y
(9) Y
(10) N

2. (8 points)

(1) Multiply 01101010 by 11110001 in the 2's complement form. Note the resulting product may have more than eight bits.

(2) Apply CRC to the data bits 10110010 using the generator code 1010 to produce the transmitted CRC code.

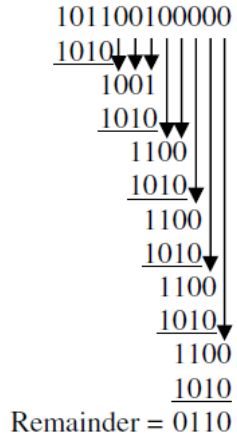
Solution:

(1) The 2's complement form of 11110001 is 00001111. Thus, we have

$$
\begin{array}{r}
01101010 \\
\times\ 00001111 \\
\hline
01101010 \\
01101010\ \ \\
\hline
100111110 \\
01101010\ \ \ \\
\hline
1011100110 \\
01101010\ \ \ \ \\
\hline
11000110110
\end{array}
$$

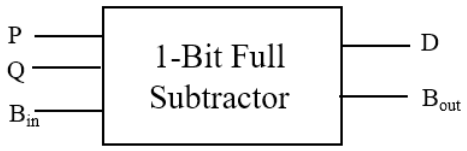
Finally, changing to 2's complement with sign, we have 100111001010.

(2) The remainder can be found as follows:



CRC is 101100100110.

3. (12 points) We implement a 1-bit full subtractor that performs the binary subtraction as shown below.



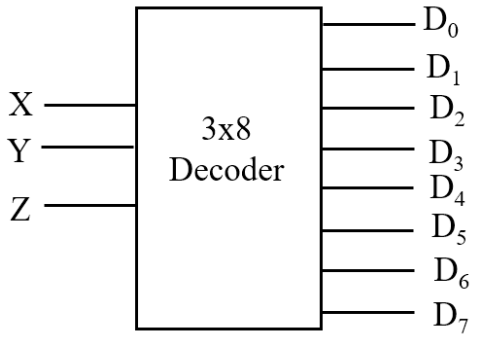
P and Q are 1-bit variables and B_{in} is the borrow input from the previous stage. It produces two outputs: the difference D and the borrow output B_{out}. The truth table describing the function of this 1-bit full subtractor is shown in the following table.

B_{in}	P	Q	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	0	0
1	0	0	1	1
1	0	1	0	1
1	1	0	0	0
1	1	1	1	1

(1) Derive the Boolean expressions for D and B_{out} using K-maps;

(2) Implement D and B_{out} using all necessary logic gates;

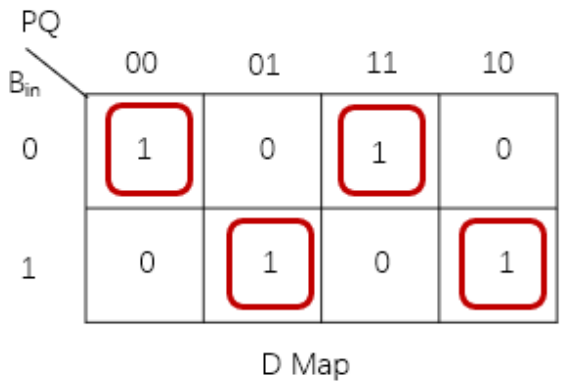
(3) Alternatively, we can design the 1-bit full subtractor above using a 3×8 decoder whose truth table is as shown below. Show your implementation with all necessary logic gates.

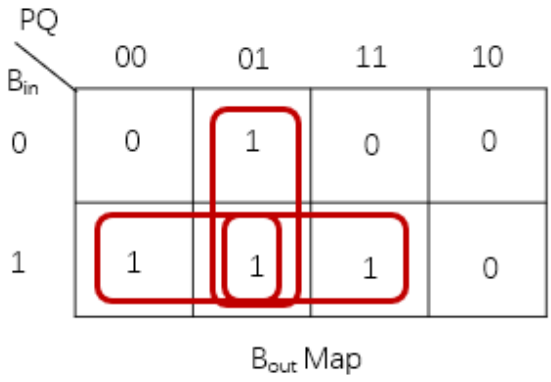


X	Y	Z	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Solution:

(1) The logic expressions for D and B_{out} can be found as

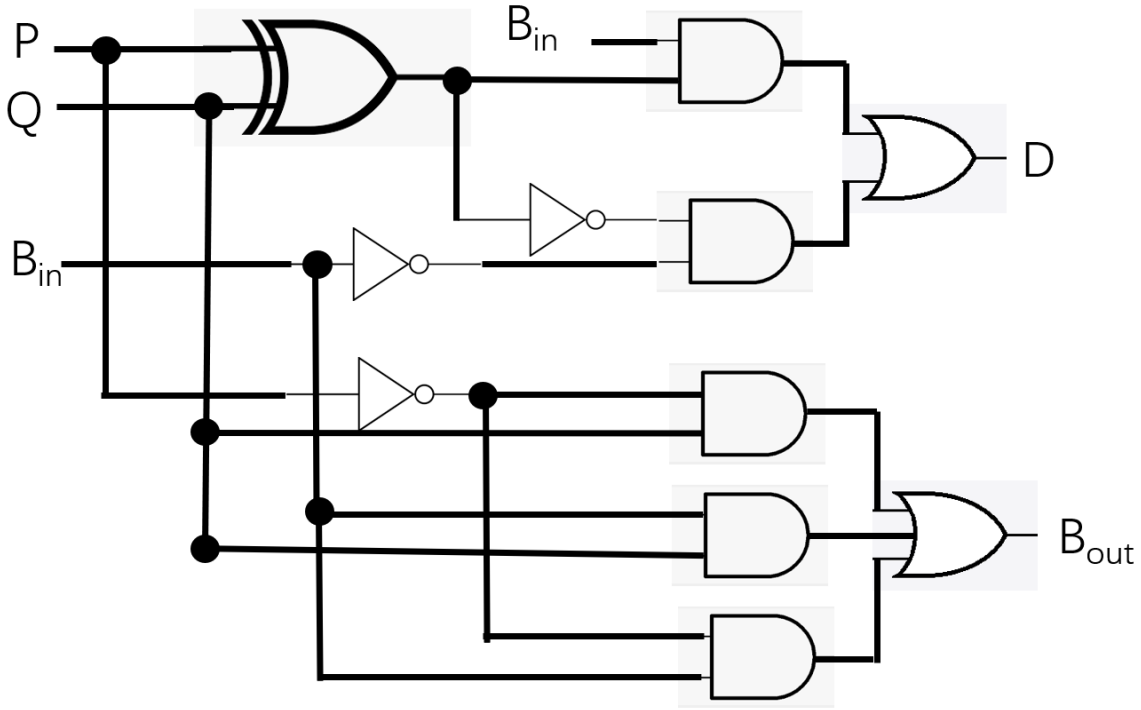




$$D = \overline{B_{\text{in}}}\ \overline{P \oplus Q} + B_{\text{in}}\,(P \oplus Q) \quad (1)$$

$$B_{\text{out}} = \overline{P}Q + B_{\text{in}}Q + B_{\text{in}}\overline{P} \quad (2)$$

(2) The subtractor can be implemented with logic gates as follows:

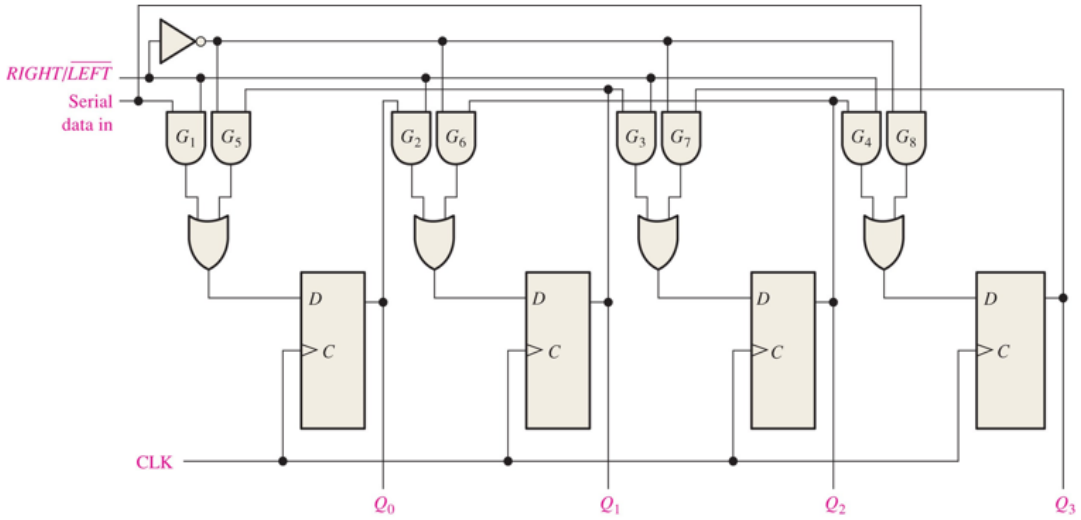


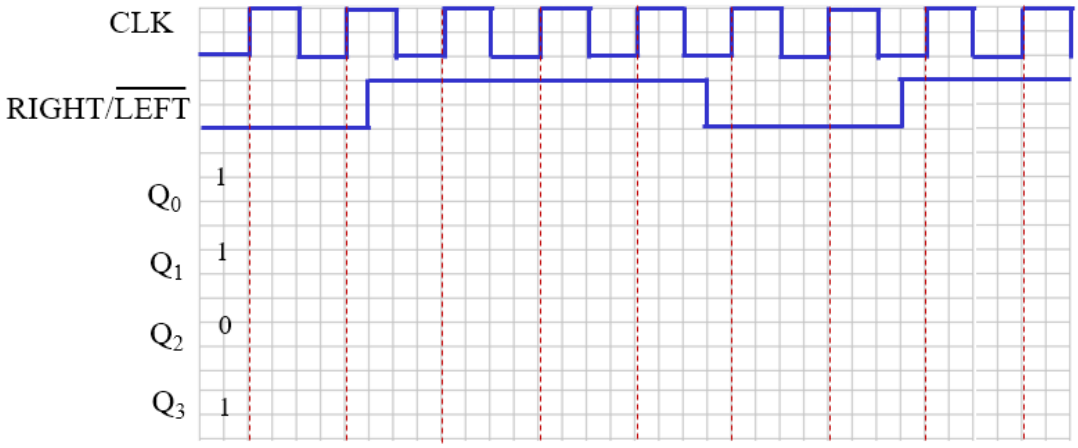
(3) Set X, Y and Z as B_{in}, P and Q respectively, we can use two four-input OR gates and the decoder to implement the full subtractor.

$$D = D_1 + D_2 + D_4 + D_7 \quad (3)$$

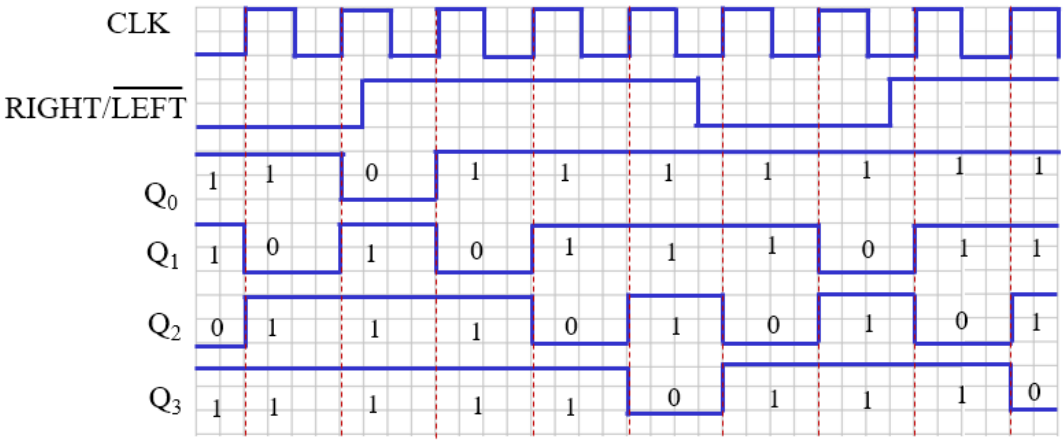
$$B_{\text{out}} = D_1 + D_4 + D_5 + D_7 \quad (4)$$

4. (4 points) Given the following bidirectional shift register, complete the timing diagram for $Q_0 - Q_3$, assuming that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ initially and that the serial data-input line is **HIGH**.





Solution:



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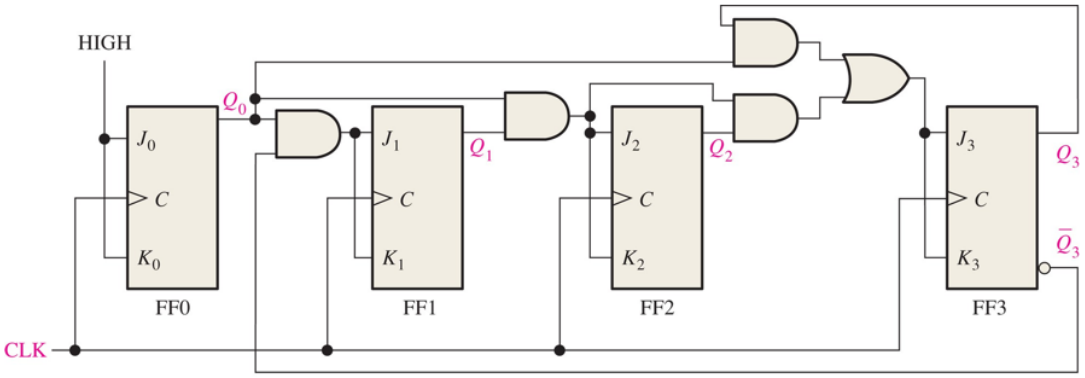
5. (6 points)

(1) Given the initial states **prior to** the first clock pulse as shown, complete the remaining table by analyzing the J and K inputs to each flip-flop **prior to** each clock pulse.

(2) What is the modulus of the counter?

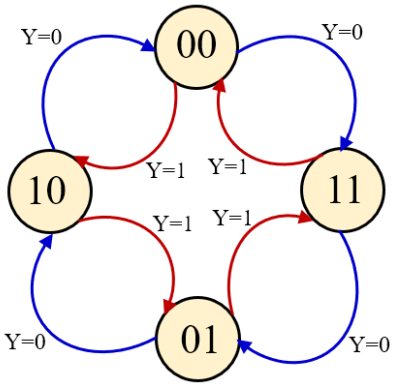


CLK	J_0	J_1	J_2	J_3	Q_0	Q_1	Q_2	Q_3
1	1	0	0	0				
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								

Solution: As shown in the following table, the counter has a modulus of 10.

CLK	J_0	J_1	J_2	J_3	Q_0	Q_1	Q_2	Q_3
1	1	0	0	0	1	0	0	0
2	1	1	0	0	0	1	0	0
3	1	0	0	0	1	1	0	0
4	1	1	1	0	0	0	1	0
5	1	0	0	0	1	0	1	0
6	1	1	0	0	0	1	1	0
7	1	0	0	0	1	1	1	0
8	1	1	1	1	0	0	0	1
9	1	0	0	0	1	0	0	1
10	1	0	0	1	0	0	0	0
11	1	0	0	0	1	0	0	0

6. (12 points) Design a counter to produce the following UP/DOWN sequences using two **D flip-flops**.



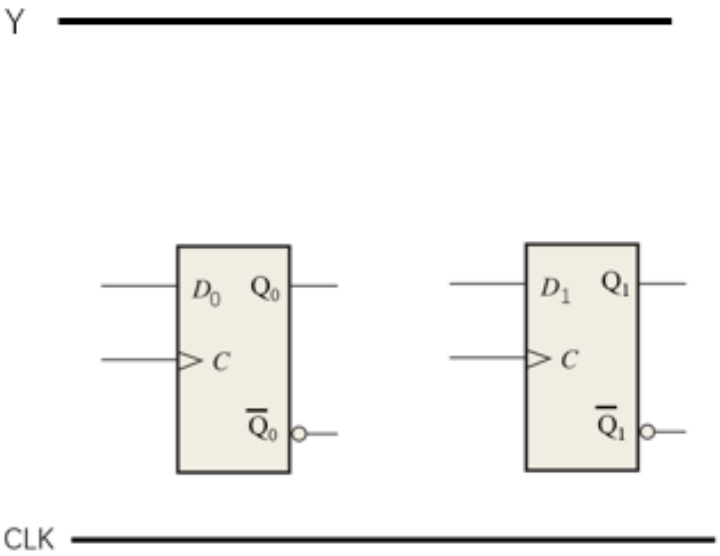
To show your design, please complete the following tasks.

(1) Write the next-state table;

(2) Write the transition table for a D flip flop;

(3) Use K-maps to simplify logic expressions of D_0 and D_1;

(4) Draw your implementation by finishing the following schematic diagram with necessary logic gates.



Solution:

(1) Next-state table

Present State		Next State			
		Y=0		Y=1	
Q_1	Q_0	Q_1	Q_0	Q_1	Q_0
0	0	1	1	1	0
1	1	0	1	0	0
0	1	1	0	1	1
1	0	0	0	0	1

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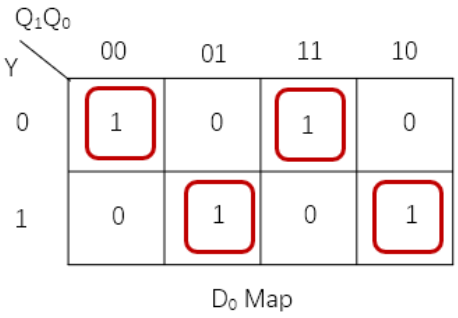
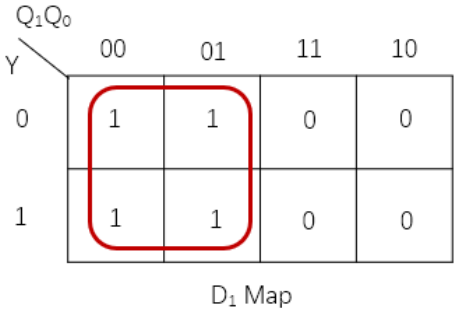
(2) Transition table for a D flip flop

Output State Transitions Q_N		Q_{N+1}	Flip-Flop Inputs D
0	$\longrightarrow$	0	0
0	$\longrightarrow$	1	1
1	$\longrightarrow$	0	0
1	$\longrightarrow$	1	1

(3) Use K-maps to simplify logic expressions

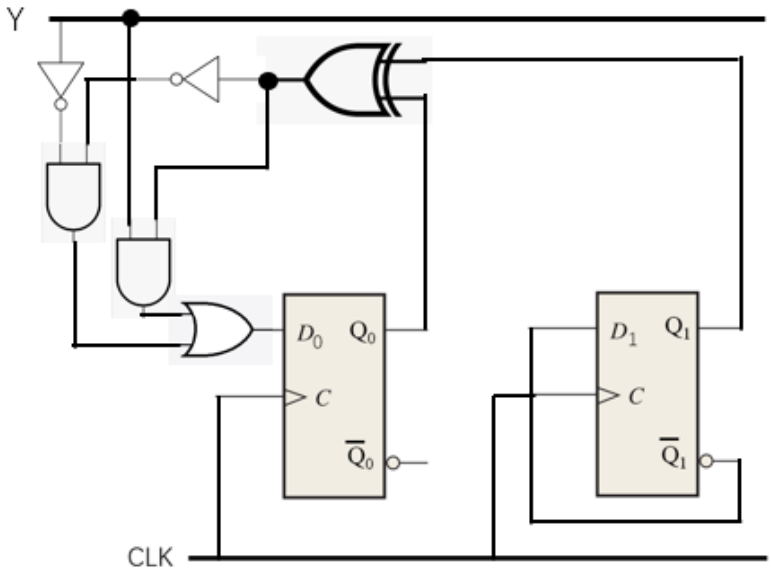




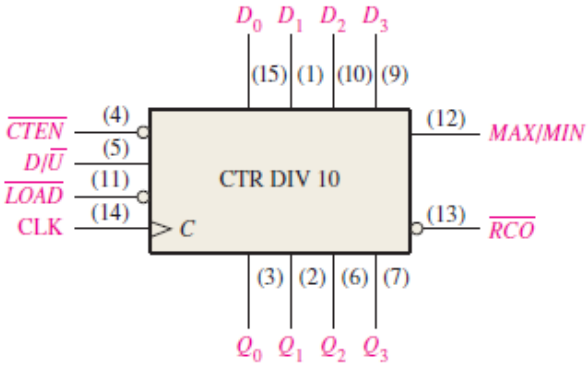
$$D_0 = \overline{Y}\left(\overline{Q}_0\overline{Q}_1 + Q_0Q_1\right) + Y\left(Q_0\overline{Q}_1 + \overline{Q_0}Q_1\right) = \overline{Y}\ \overline{Q_0 \oplus Q_1} + Y\left(Q_0 \oplus Q_1\right) \quad (5)$$

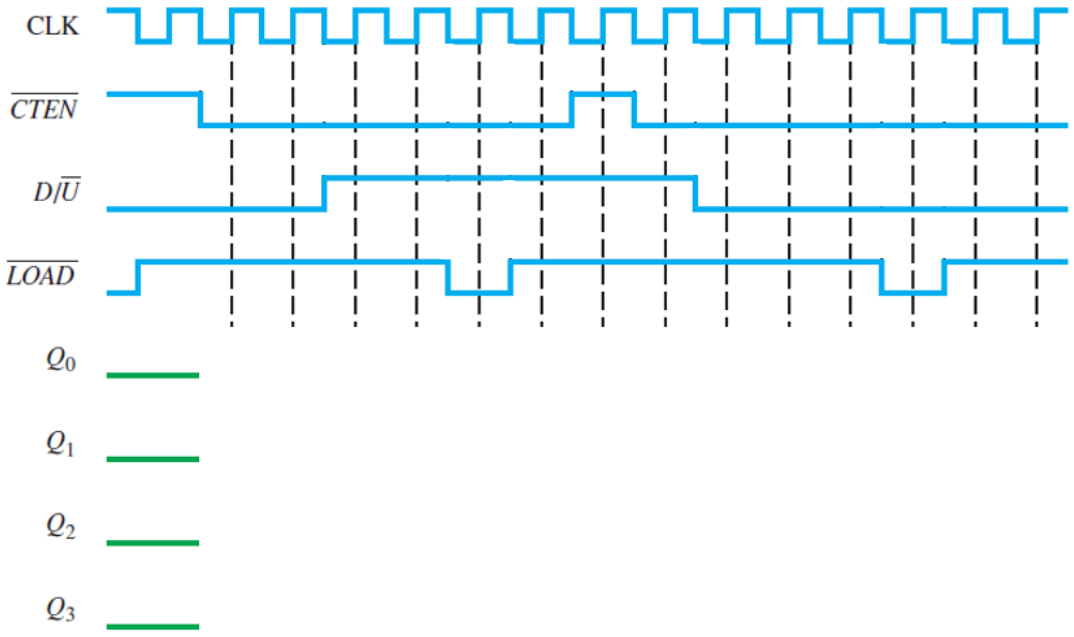
$$D_1 = \overline{Q}_1 \quad (6)$$

(4) The complete implementation of the counter is shown as follows:

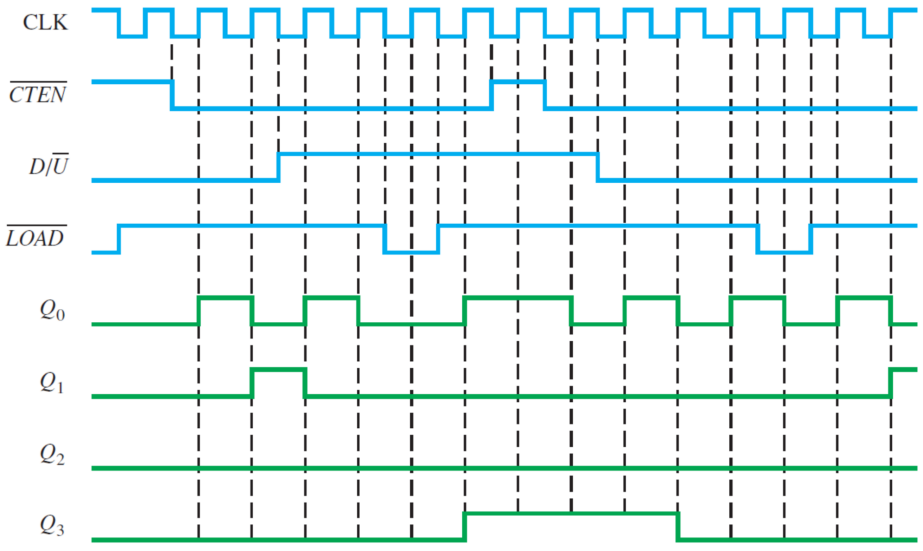


7. (8 points) Develop the Q_0, Q_1, Q_2 and Q_3 output waveforms for a 74HC190 up/down counter with the input waveforms shown below. A binary 0 is on the data inputs $Q_0 - Q_3$. Start with a count of 0000.





Solution: The output waveforms are shown as follows:



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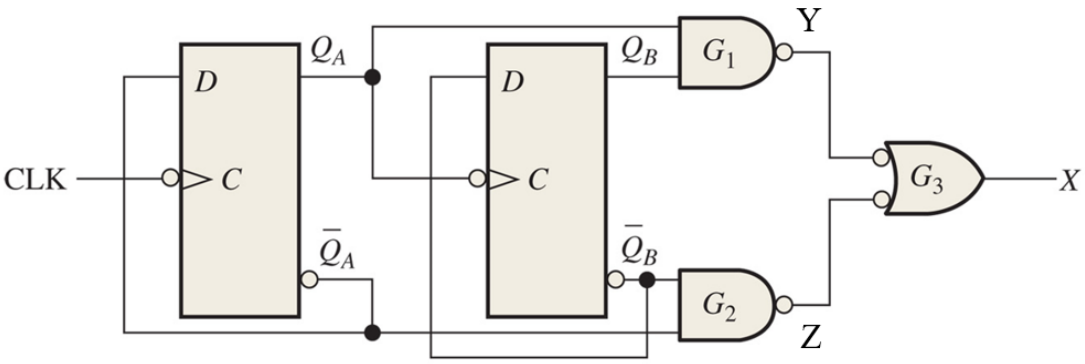
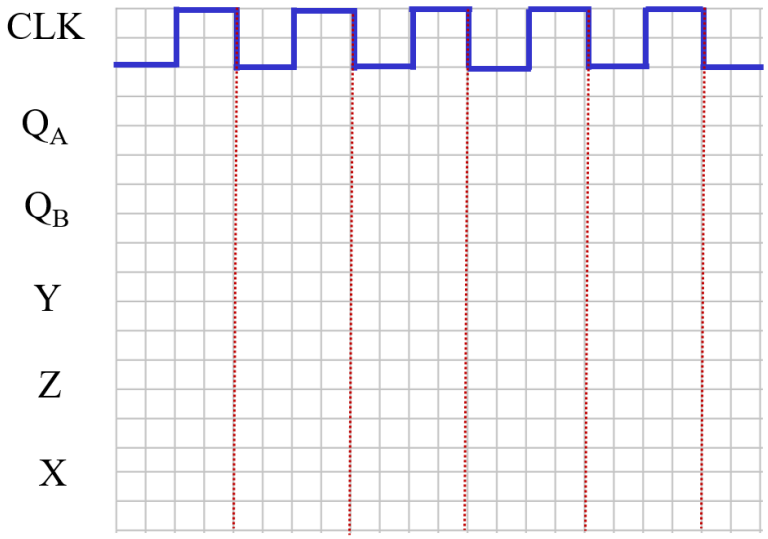
8. (10 points) Draw the timing diagram for the following flip-flop circuit. assuming that Q_A and Q_B are initially HIGH in the first clock pulse.



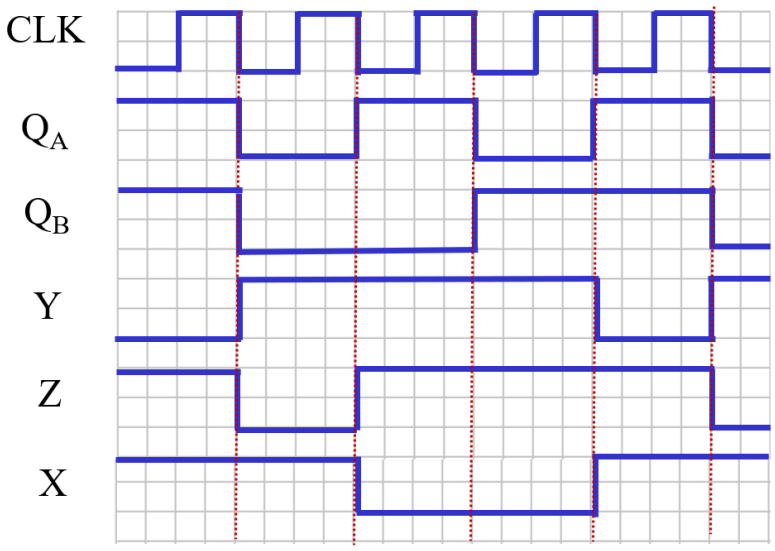
(1) Assuming the ideal case in which no propagation delays are caused, draw the output waveforms for Q_A, Q_B, Y, Z and X over the first 5.5 clock puluses;

(2) Assuming a more realistic case in which a small propagation delay of **one-division** duration on the grip paper is incurred by each flip flop, re-draw the output waveforms for Q_A, Q_B, Y, Z and X over the first five clock puluses;

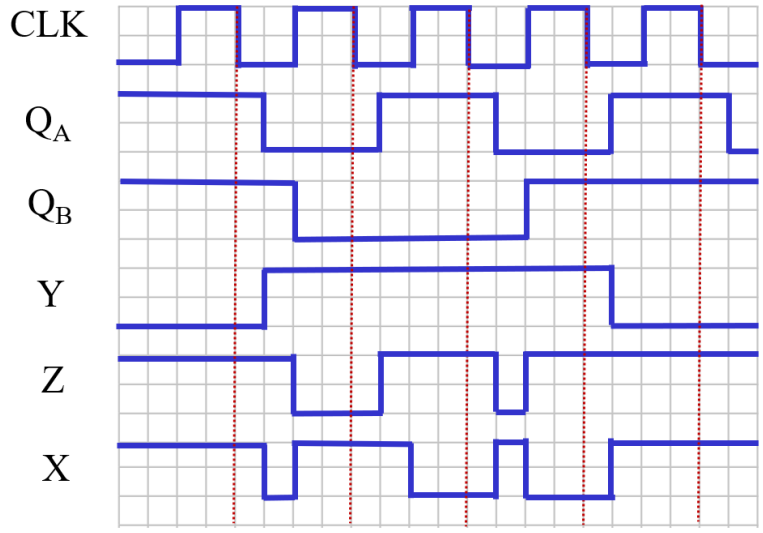


Solution: The output waveforms are shown as follows:

(1) Without propagation delays

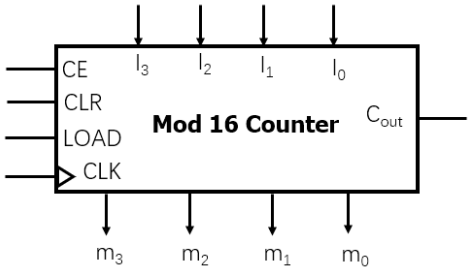


(2) With propagation delays



9. (15 points) Given a clock signal with frequency of 1 pulse every 24 hours, design a digital calendar that counts days and months of the year by completing the following tasks:

(1) Month Counter: Design a mod 12 month counter to count the month of the year with "0" representing January and "11" December and so on. You are required to use the following mod 16 binary counter to build this month counter. The resulting counter should produce an output signal (C_{year}) equal to 1 only during the last month of the year.



The mod 16 counter has the following control inputs :

(i) CE: Count Enable,

(ii) CLR: Synchronous Clear,

(iii) Load : Parallel load,

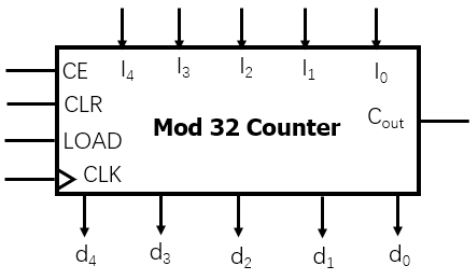
(iv) Inputs I_0, I_1, I_2 and I_3.

(2) Day Counter: Design a day counter to count the days of the month. The counter has two input signals x_1 and x_0 which indicate the number of days in the current month as shown in the table below.

(3) Assume that x_1 and x_0 are provided by the system, show how to assemble the parts designed in (1) and (2) to build a synchronous counter that gives the current month of the year and the day of that month.

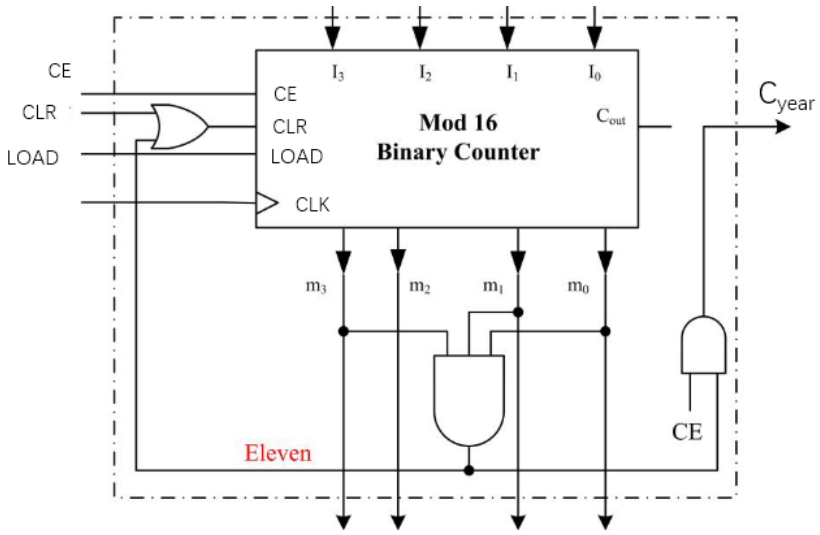
x_1x_0	Number of Days	Months	Month Count
00	31	January, March, May, July, August, October, December	0,2,4,6,7,9,11
01	30	April, June, September, November	3,5,8,10
10	29	February in leap years	1
11	28	February in ordinary years	1

The counter should produce an output signal (C_{month}) equal to 1 only during the last day of the month. Design this day counter using a mod 32 binary counter having the same control inputs as the counter in part (1).

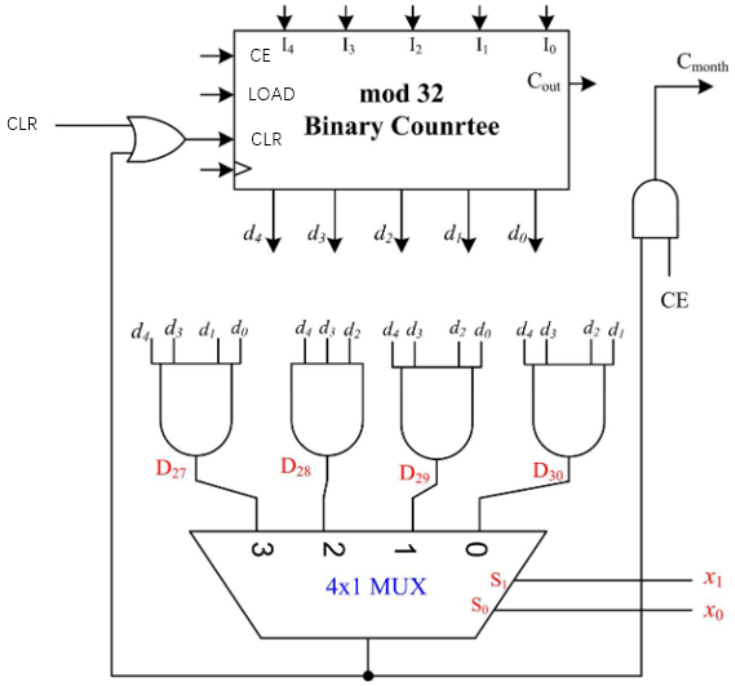


Solution:

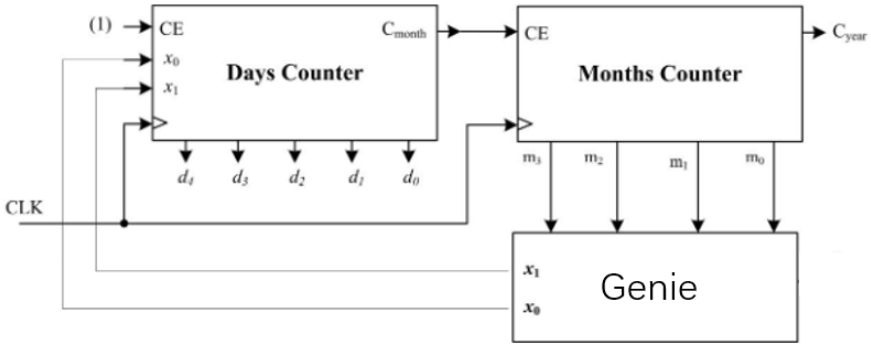
(1) Month Counter



(2) Day Counter



(3) The complete counter



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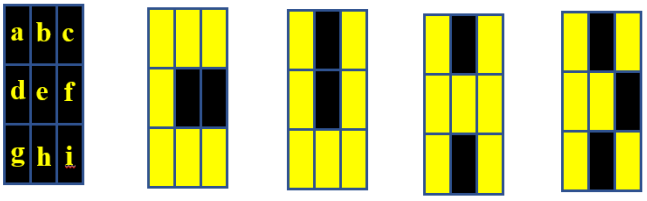
10. (15 points) Four illumination panels showing "C","U", "H" and "K" have been set up on the upper campus.

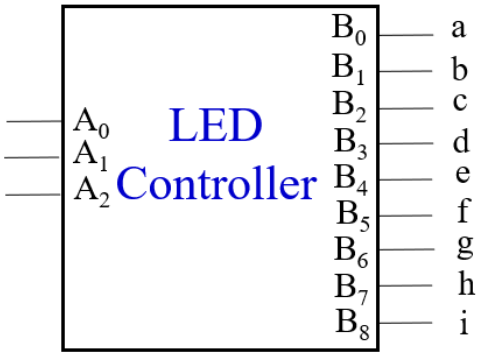
For simplicity, we assume that each panel is composed of nine LED lights labeled as "a" to "i". To display an alphabet, we should turn on and off the corresponding LED lights. For instance, "C" is displayed by turning on all LED lights except "e" and "f". More specifically, an LED light is turned on if it is connected to a logic HIGH. In contrast, it is turned off if it is connected to a logic LOW. In other words, we display "C" by connecting "1" to "a,b,c,d,g,h,i" while "0" to "e,f".



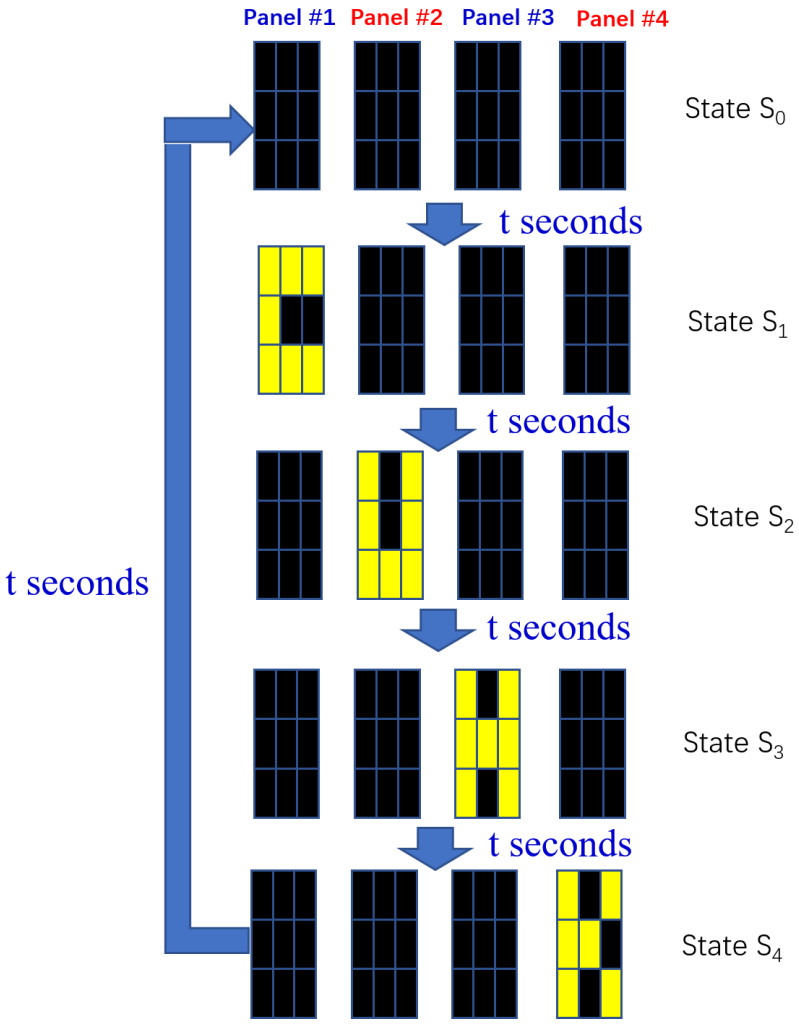
(1) First, design an LED controller with three inputs A_0, A_1 and A_2 and nine outputs $B_0 - B_8$ to implement the following features:

- when $A_2 = 0, A_1 = 0, A_0 = 0$, All LED lights are off;
- when $A_2 = 0, A_1 = 0, A_0 = 1$, Display "C";
- when $A_2 = 0, A_1 = 1, A_0 = 0$, Display "U";
- when $A_2 = 0, A_1 = 1, A_0 = 1$, Display "H";
- when $A_2 = 1, A_1 = 0, A_0 = 0$, Display "K";
- Otherwise, don't care.

Derive the logic expressions for the following **four** outputs, namely B_0, B_1, B_2 and B_3, in terms of A_0, A_1 and A_2, assuming that $B_0 - B_8$ are connected to "a-i", respectively.



(2) Now, the University has decided to make the illumination more attractive by turning on "C", "U", "H" and "K" sequentially as shown below.



Given a digital clock of 1 Hz, design a control system that implements the above state transition diagram with $t = 2$ by making use of your LED controller newly designed in (1).

Solution:

(i) The truth table is given as follows

A_2	A_1	A_0	B_0	B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8
0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	0	0	1	1	1
0	1	0	1	0	1	1	0	1	1	1	1
0	1	1	1	0	1	1	1	1	1	0	1
1	0	0	1	0	1	1	1	0	1	0	1
1	0	1	x	x	x	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x	x	x	x

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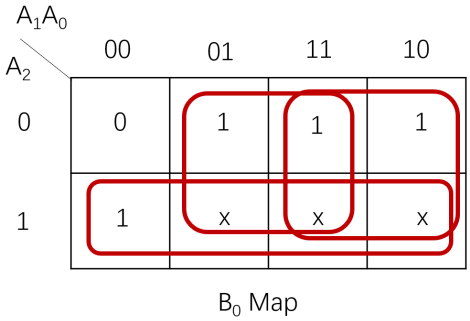
The logic expression for B_0 can be found as



B_0 Map

$$B_0 = A_2 + A_1 + A_0 \tag{7}$$

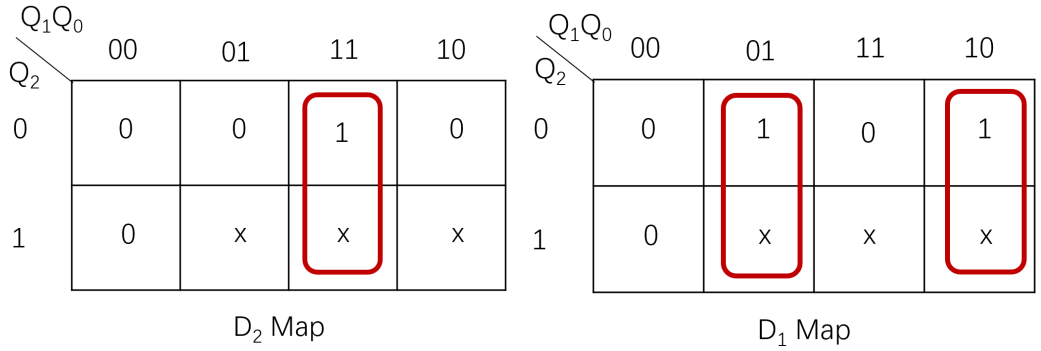
Similarly, we can find

$$B_1 = \overline{A_1} A_0 \tag{8}$$
$$B_2 = A_2 + A_1 + A_0 \tag{9}$$
$$B_3 = A_2 + A_1 + A_0 \tag{10}$$

(ii) The next-state table is given by

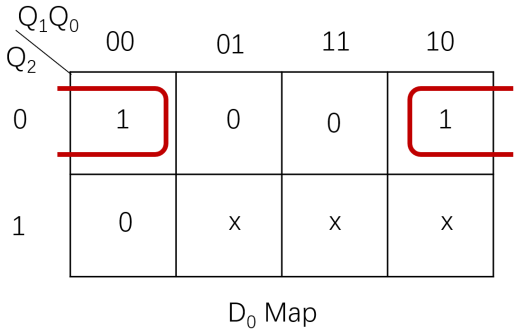
Present State			Next State		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0

Use K-maps to simplify logic expressions



D_2 Map

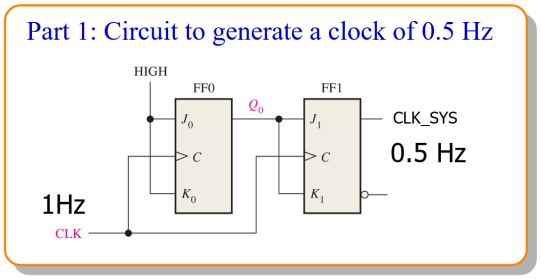
D_1 Map

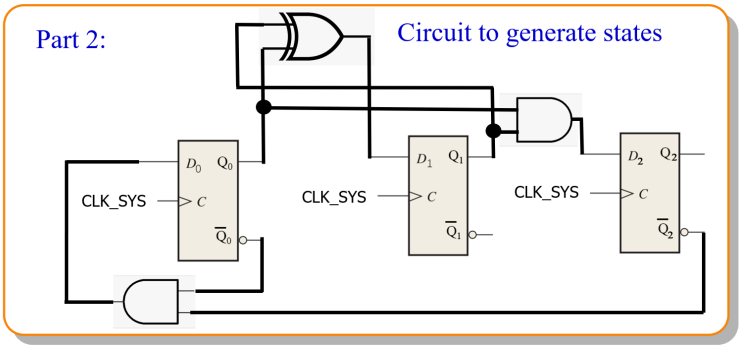


D_0 Map

$$D_2 = Q_1 Q_0 \tag{11}$$
$$D_1 = \overline{Q_1} Q_0 + Q_1 \overline{Q_0} = Q_0 \oplus Q_1 \tag{12}$$
$$D_0 = \overline{Q_0}\ \overline{Q_2} \tag{13}$$

Finally, the complete implementation of the system is shown as follows:





Part 3:

Circuit to control LEDs