香港中文大學（深圳）
The Chinese University of Hong Kong, Shenzhen

ECE2050 Digital Logic and Systems

Tutorial 8: Shift Registers

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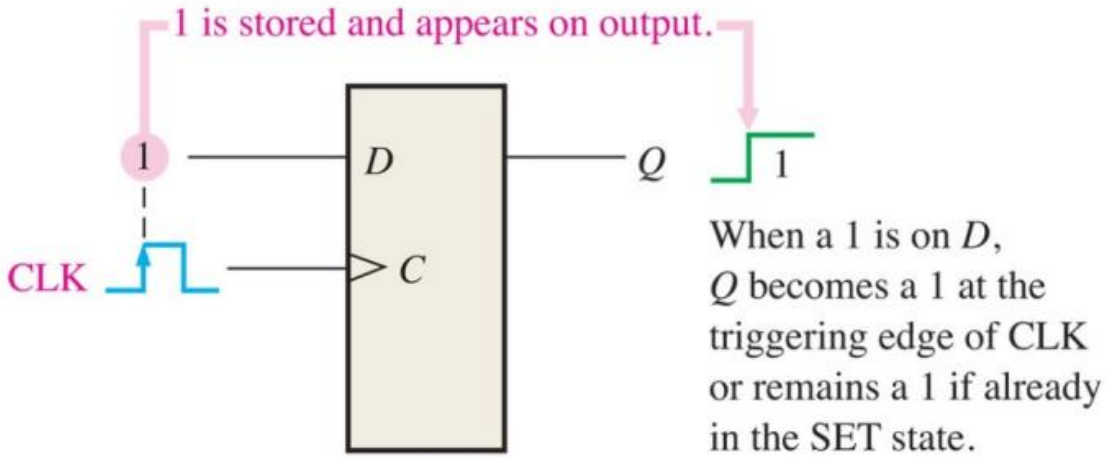
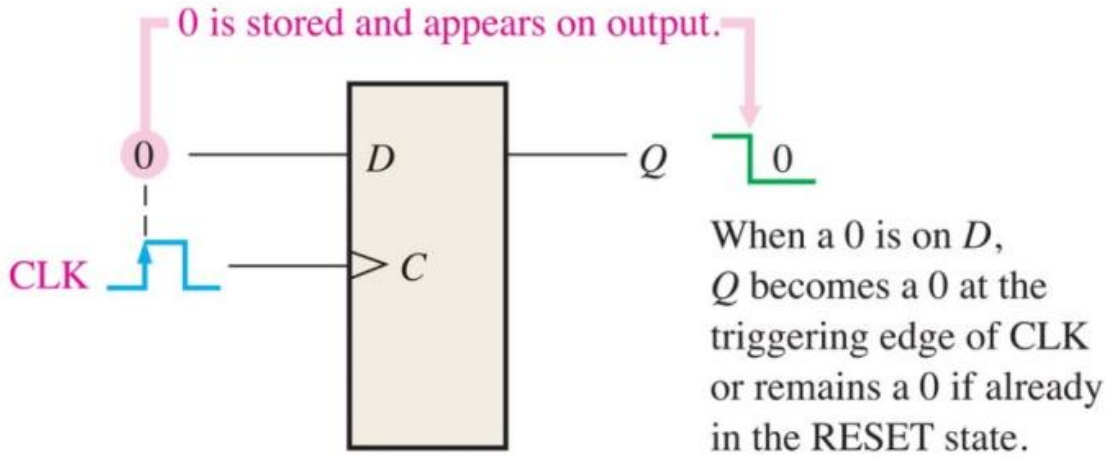
Office Hour: Tue. 11:00-12:00, ZXB107

Review: Two Basic Functions of Shift Registers

- Data storage



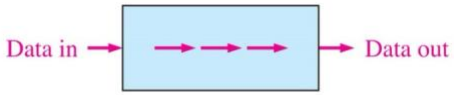
When a 1 is on D, Q becomes a 1 at the triggering edge of CLK or remains a 1 if already in the SET state.



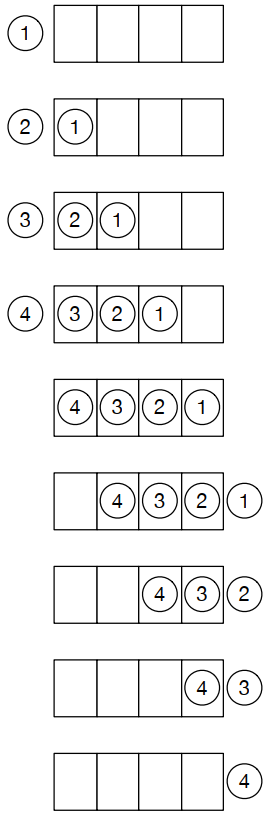
When a 0 is on D, Q becomes a 0 at the triggering edge of CLK or remains a 0 if already in the RESET state.

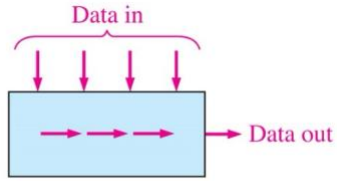
Review: Two Basic Functions of Shift Registers

- Data movement

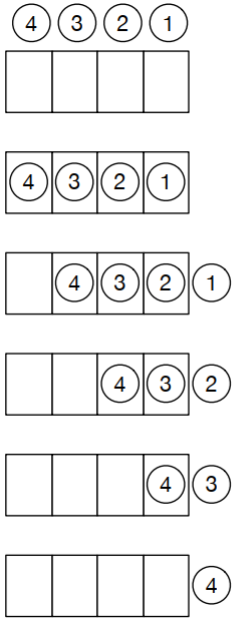


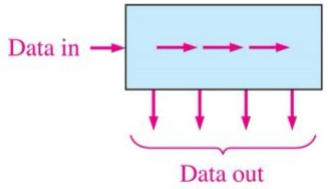
(a) Serial in/shift right/serial out



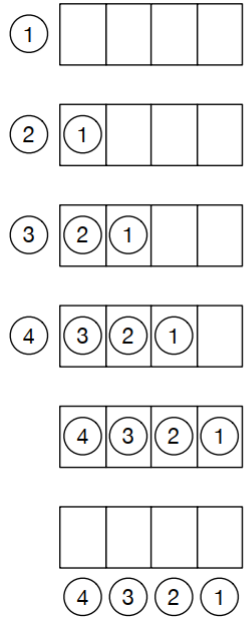


(c) Parallel in/serial out



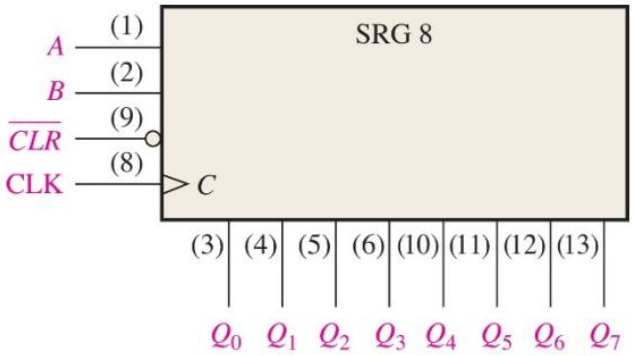


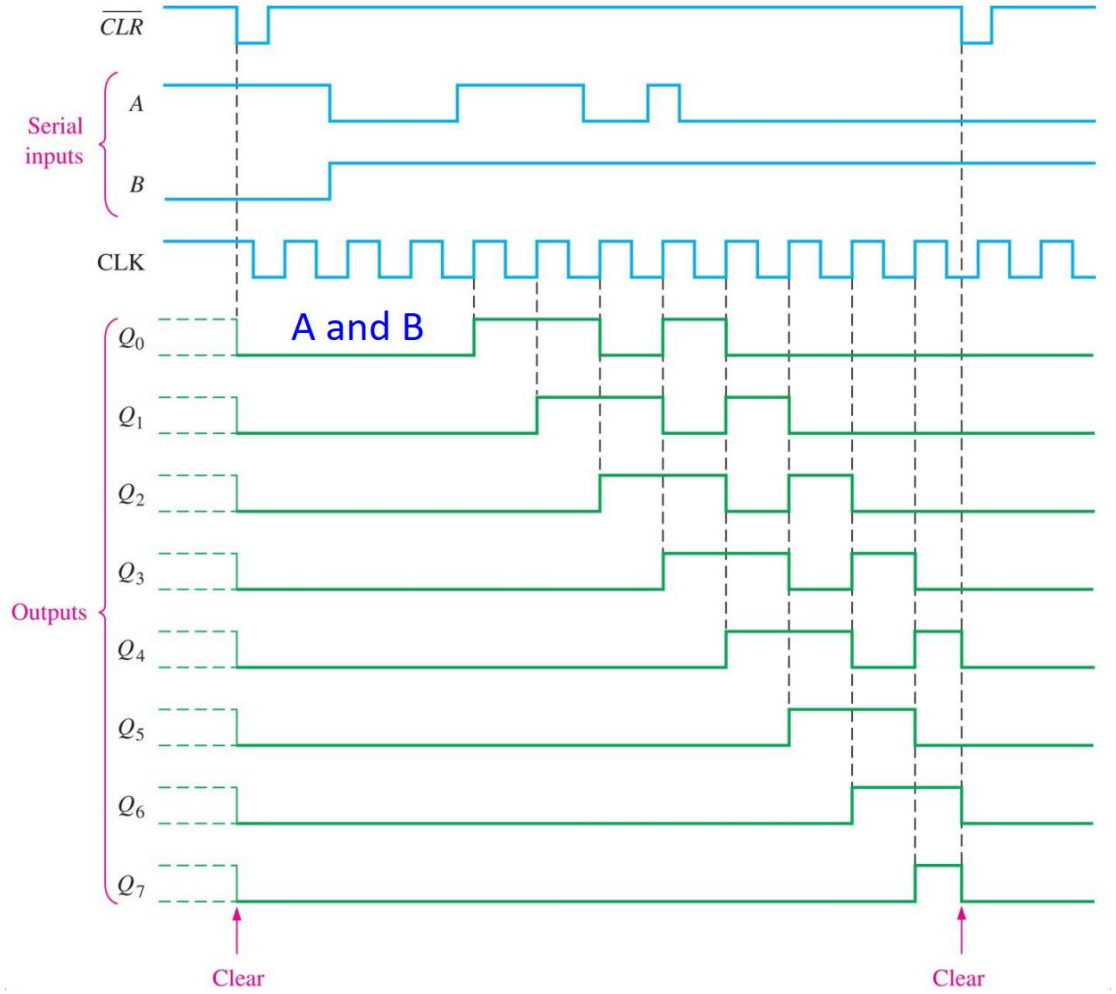
(d) Serial in/parallel out



Review: 8-Bit Serial In/Parallel Out Shift Register

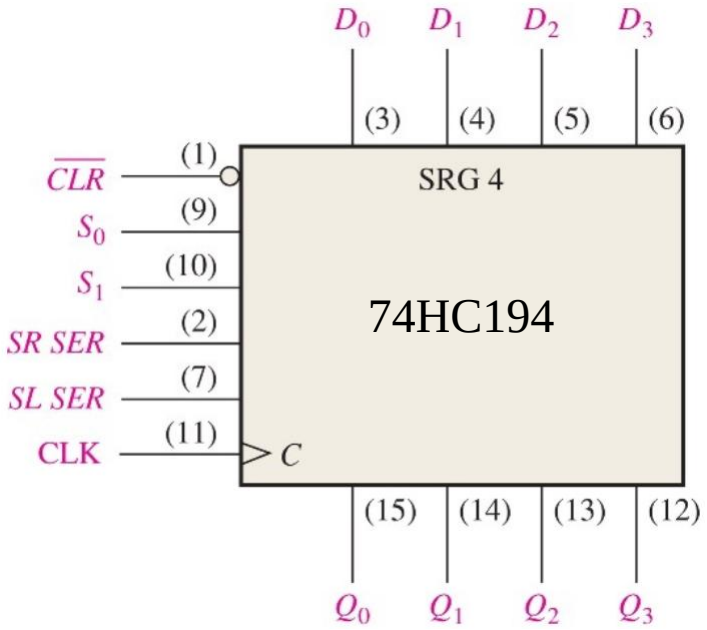
- 74HC164: Fixed-function IC shift register with serial in/parallel out



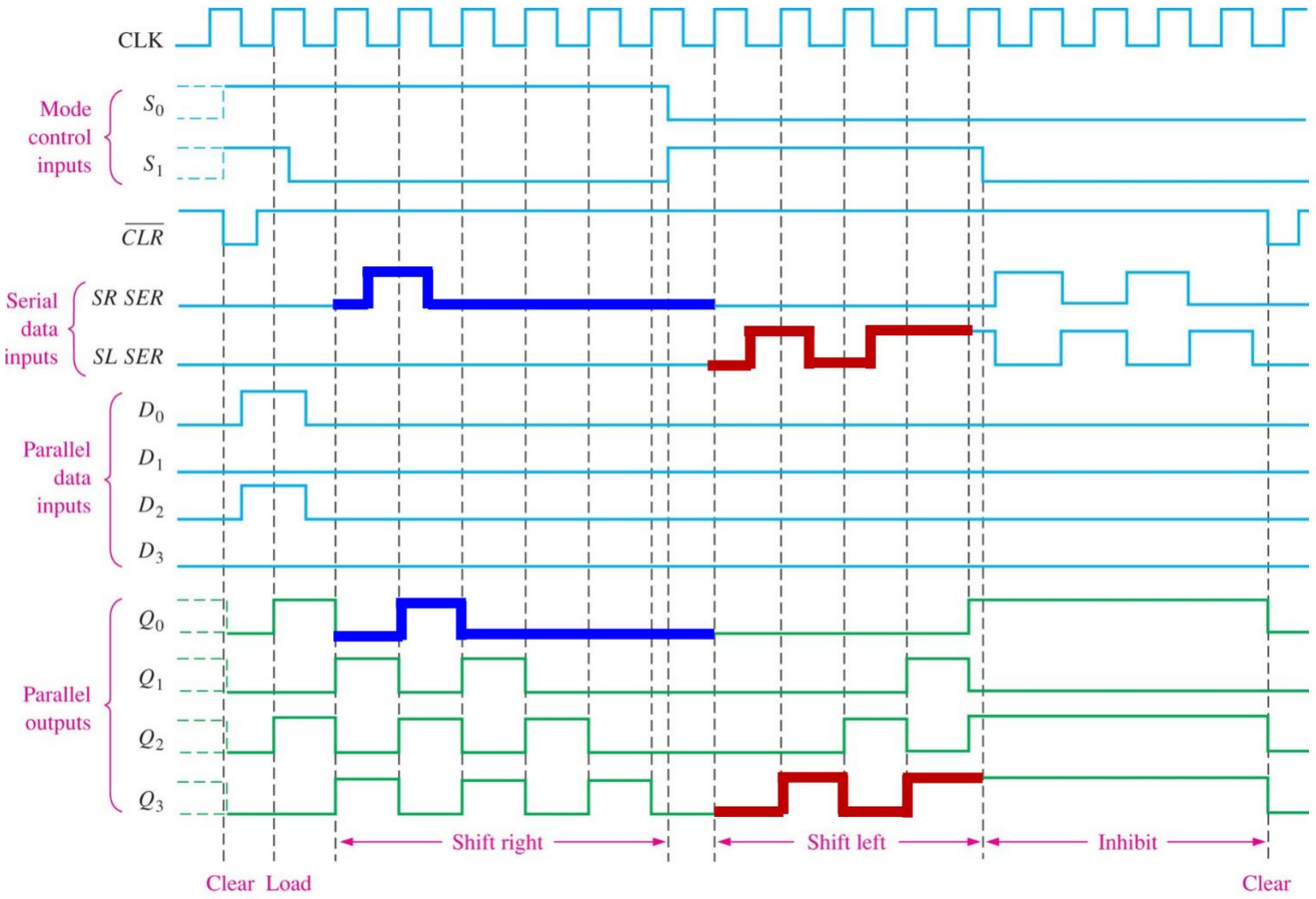


- Two gated serial inputs: A and B, & an asynchronous clear (CLR) input
- Parallel outputs : Q_0 ~ Q_7.

Review: 4-Bit Bidirectional Universal Shift Register

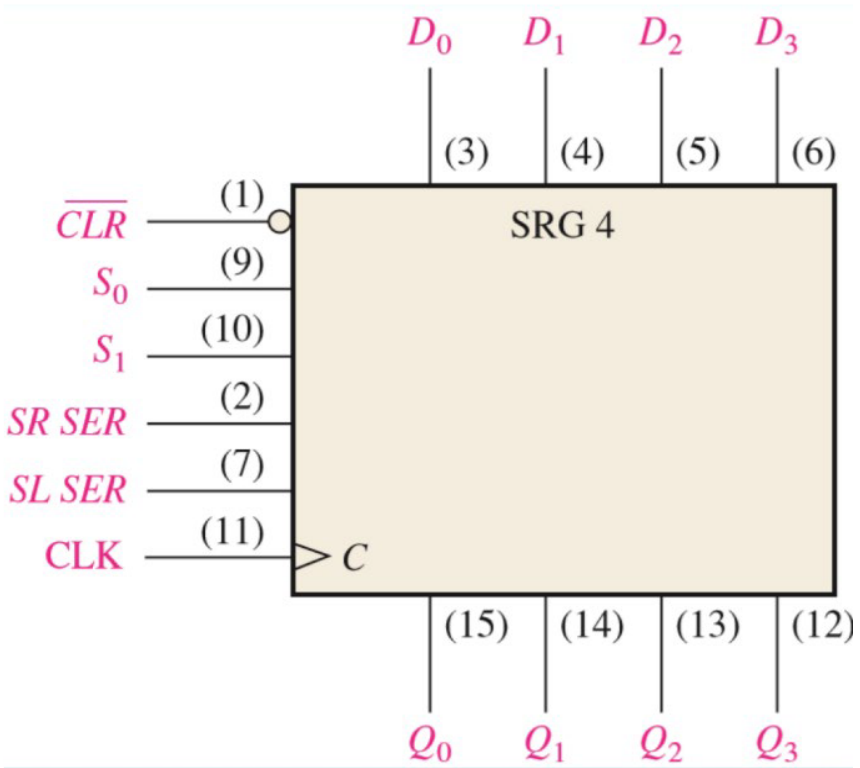


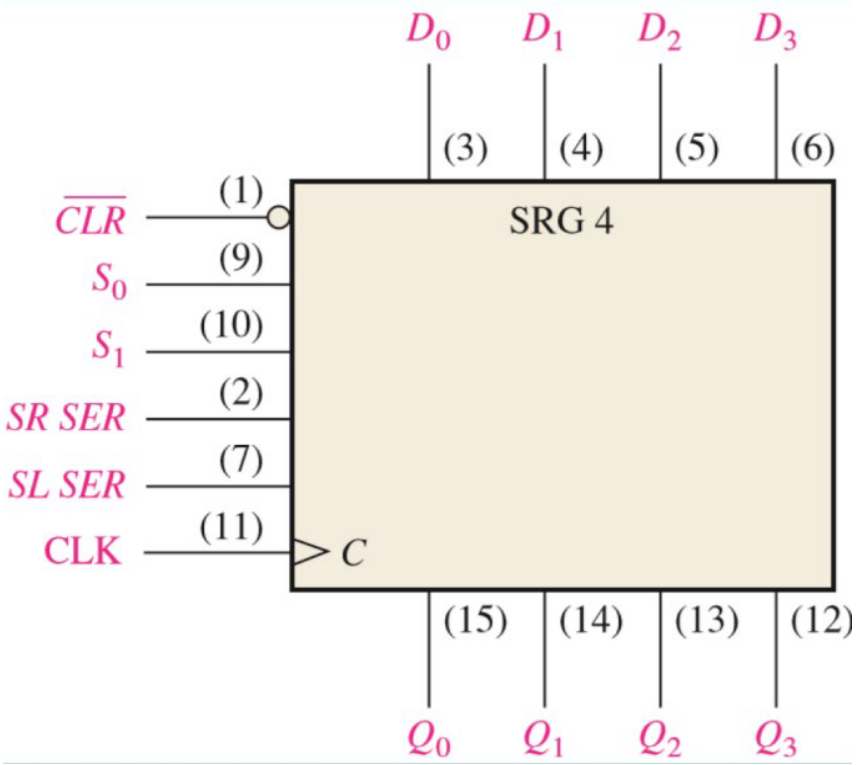
S_0	S_1	Func.
HIGH	HIGH	Parallel Loading
HIGH	LOW	Shift right
LOW	HIGH	Shift left
LOW	LOW	Inhibit



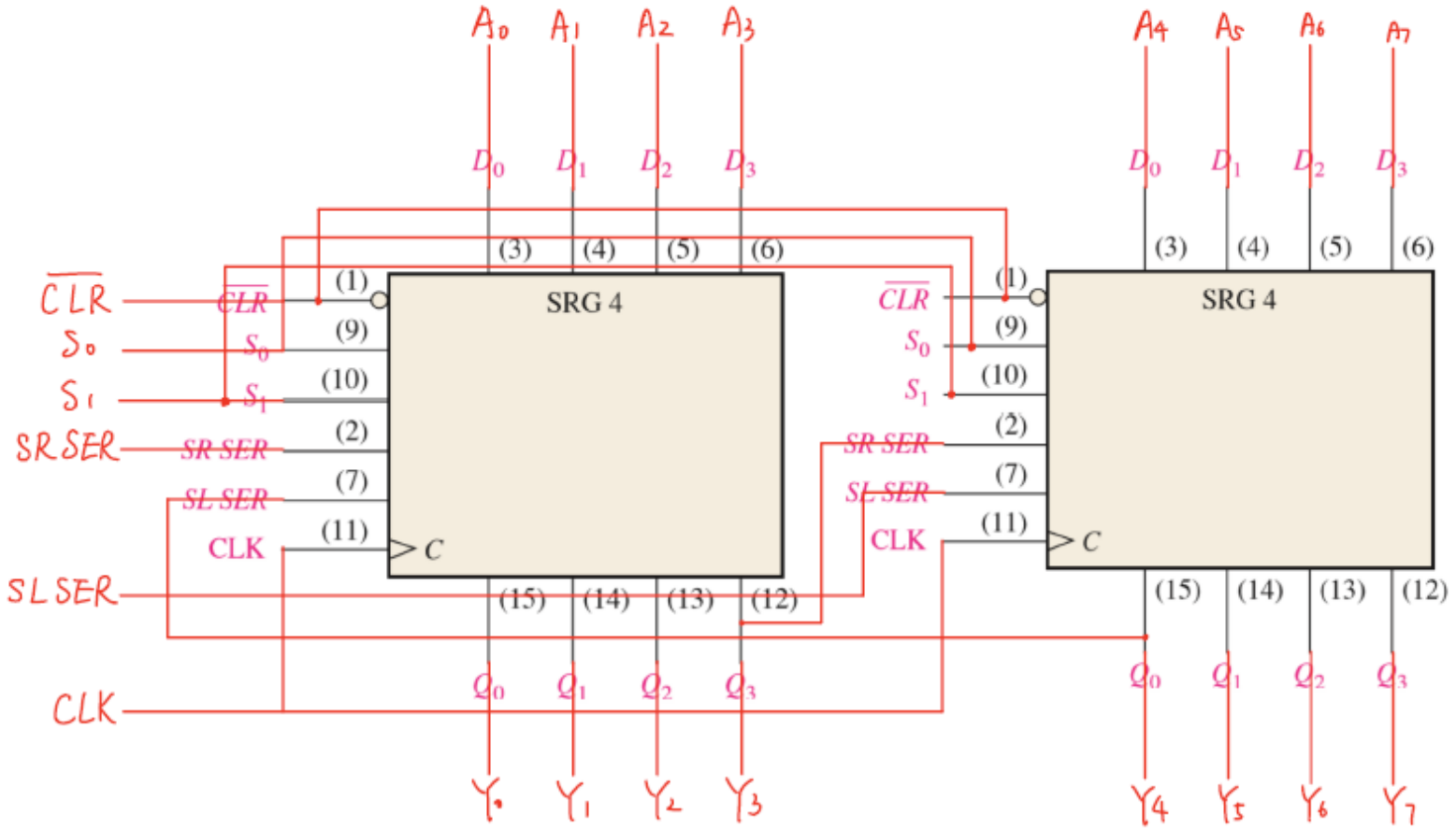
Question 1: 8-Bit Bidirectional Shift Register

- Q1: Combine two 74HC194 to a Bidirectional Shift Register with 8 bit.





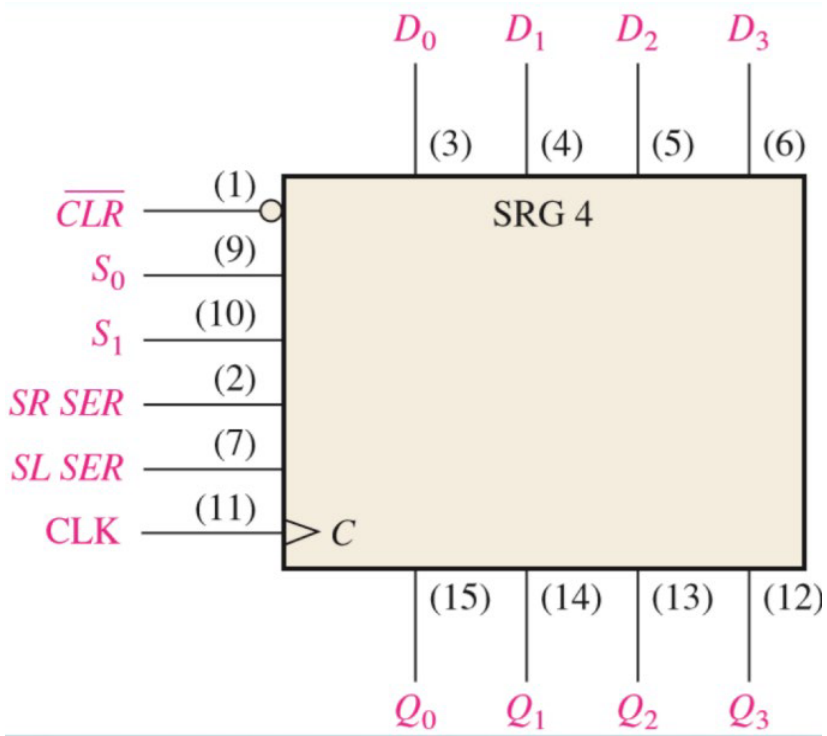
Question 1: 8-Bit Bidirectional Shift Register

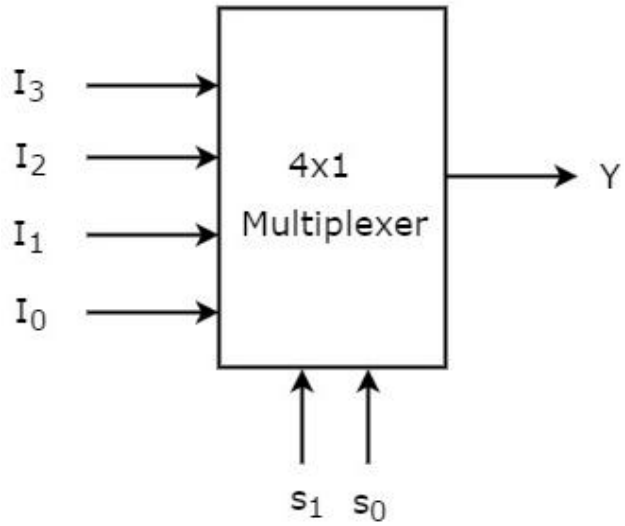


Parallel input: A0-A7
Parallel output: Y0-Y7
Shift right: new SR SER
Shift left: new SL SER

Question 2: Sequential Signal Generator

- Q2: Try to design a signal generator that can produce 00011101 sequentially, using one 74HC194 and one MUX.

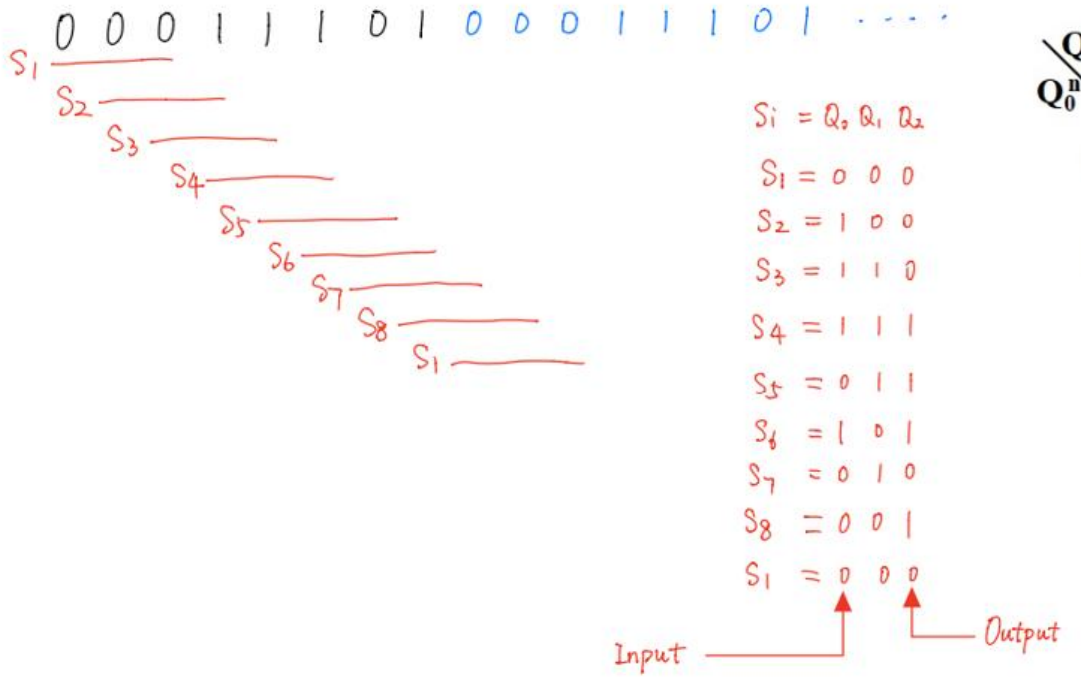


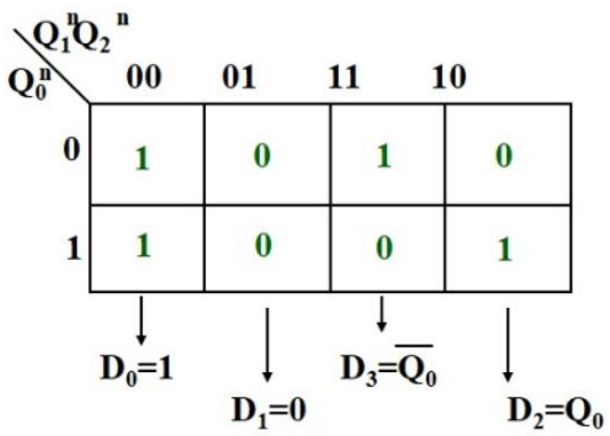


Question 2: Sequential Signal Generator

Hints:

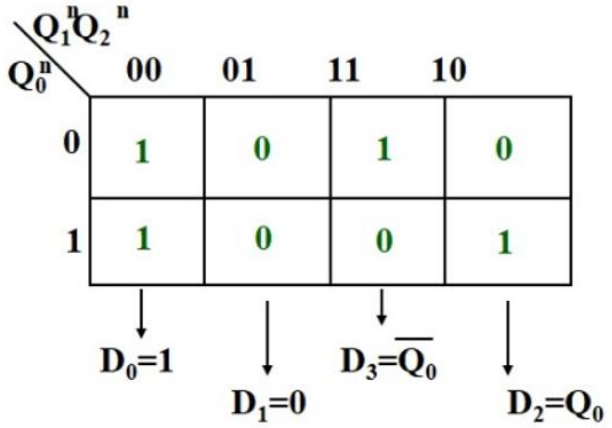
- Sequence length is 8, and it is possible to generate a serial sequence with a 3-bit shift register. Why?
- Use 74HC194, but three output ports will be enough.
- Use a MUX to help select input.

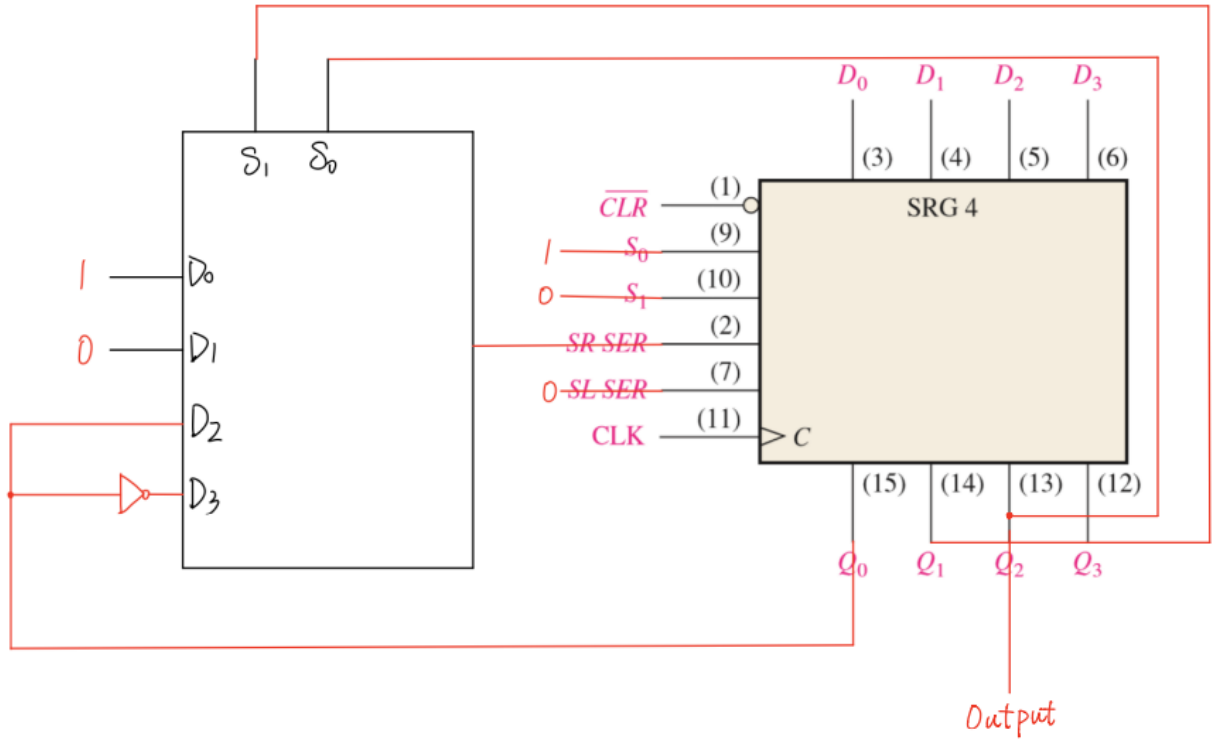




Q_0^n	Q_1^n	Q_2^n	Q_0^{n+1}	Q_1^{n+1}	Q_2^{n+1}	F (D_{SR})
0	0	0	1	0	0	1
1	0	0	1	1	0	1
1	1	0	1	1	1	1
1	1	1	0	1	1	0
0	1	1	1	0	1	1
1	0	1	0	1	0	0
0	1	0	0	0	1	0
0	0	1	0	0	0	0

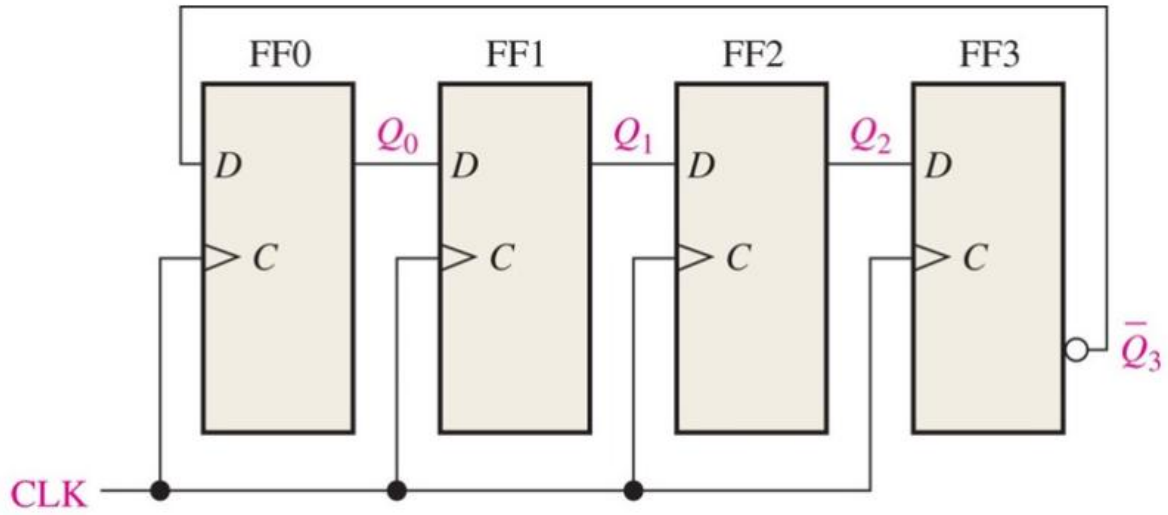
Question 2: Sequential Signal Generator





Question 3: Johnson counter

- Q3: Determine the output pulses for this counter circuit, known as a Johnson counter, assuming that all Q outputs begin in the low state.



(a) Four-bit Johnson counter

Question 3: Johnson counter

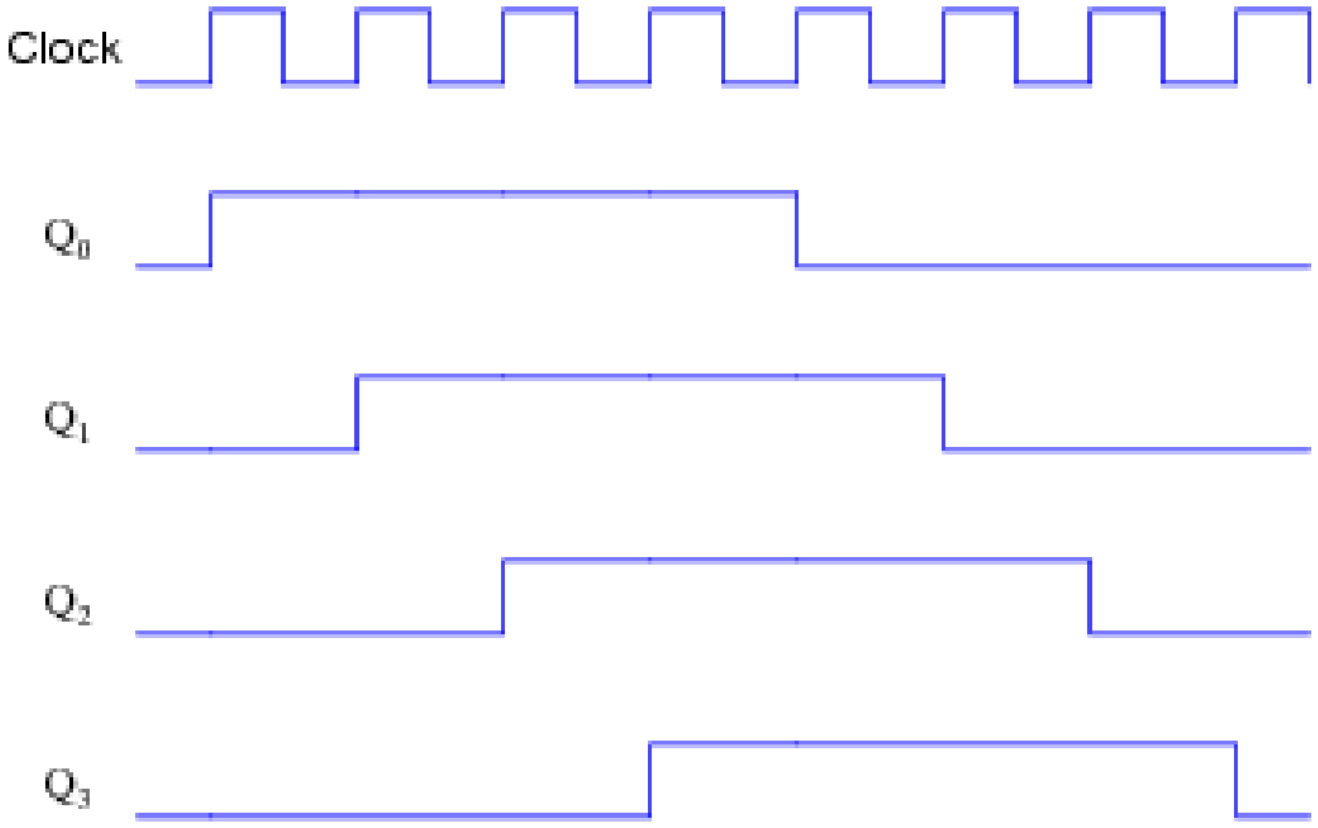


TABLE 8–3

Four-bit Johnson sequence.

Clock Pulse	Q_0	Q_1	Q_2	Q_3
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1

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Thank You!