Midterm Test

(Time allowed: 90 minutes)
March 19, 2023

NOTE: Answer ALL **8** questions. Show all intermediate steps, except Question 1 and Question 2.

1. (10 points) Are the following statements necessarily true (Y) or not (N)?

(1) An XNOR gate output is LOW if both its inputs is HIGH.
(2) Minimization with a K-map may result in multiple possible solutions.
(3) Decoders are logic circuits with many outputs and inputs that convert coded inputs into coded outputs.
(4) It is possible to build an AND gate with multiple NOR gates.
(5) The dual symbol for a NAND gate is a negative-OR symbol.
(6) In Boolean Algebra, the addition of two values is equivalent to the logical OR function.
(7) The right-most bit in a signed binary number is the sign bit.
(8) Fan-out is the minimum number of similar gates that a given gate can drive.
(9) When a Boolean variable is multiplied by its complement, the result is 0.
(10) A parity generator can be implemented using exclusive-OR gates.

Solution:

(1) N
(2) Y
(3) N
(4) Y
(5) Y
(6) Y
(7) N
(8) N
(9) Y
(10) Y

2. (10 points) Provide your answers to the following short questions.

(1) For a periodic digital waveform with $20ms$ period and $5ms$ pulse width, write down its frequency and duty cycle;

(2) Determine the even parity bit for the BCD number 00010100;

(3) Subtract 173_{16} from BCD_{16}, write down the result;

(4) Convert binary 101101 to Gray code;

(5) A ternary numeral system (also called base 3 or trinary) has three as its base. Analogous to a bit, a ternary digit is a trit (trinary digit). Ternary most often refers to a system in which the three digits are all non–negative numbers; specifically 0, 1, and 2. Convert the fractional ternary number 10.2 to decimal (round to the nearest hundredth).

Solution:

(1) 50Hz, 25%;

(2) 0;

(3) $A5A_{16}$;

(4) 111011;

(5) 3.67.

3. (15 points) Perform each of the following calculations of the signed numbers. Show your work.

(1) 00001001 − 00000010;

(2) 01010010 × 11111110;

(3) 01001011 ÷ 00011001.

Solution:

(1) 00000111 in Figure 1;

(2) 101011100 in Figure 2;

(3) 00000011 in Figure 3.

	00001001	Minuend (+9)
	+ 11111110	2's complement of subtrahend (-2)
Discard carry	100000111	Difference (+7)

Figure 1: Q3-1 solution.

01010010	
X 00000010	
00000000	
+ 01010010	
010100100	
101011100	2's complement

Figure 2: Q3-2 solution.

2's complement

00011001 → 11100111

01001011	
+ 11100111	Add 1 to quotient
00110010	
+ 11100111	Add 1 to quotient
00111001	
+ 11100111	Add 1 to quotient
00000000	Quotient=3=0011

Figure 3: Q3-3 solution.

4. (10 points) For the logic circuit and the input waveforms shown in Figure. 4, respectively, answer the following questions.

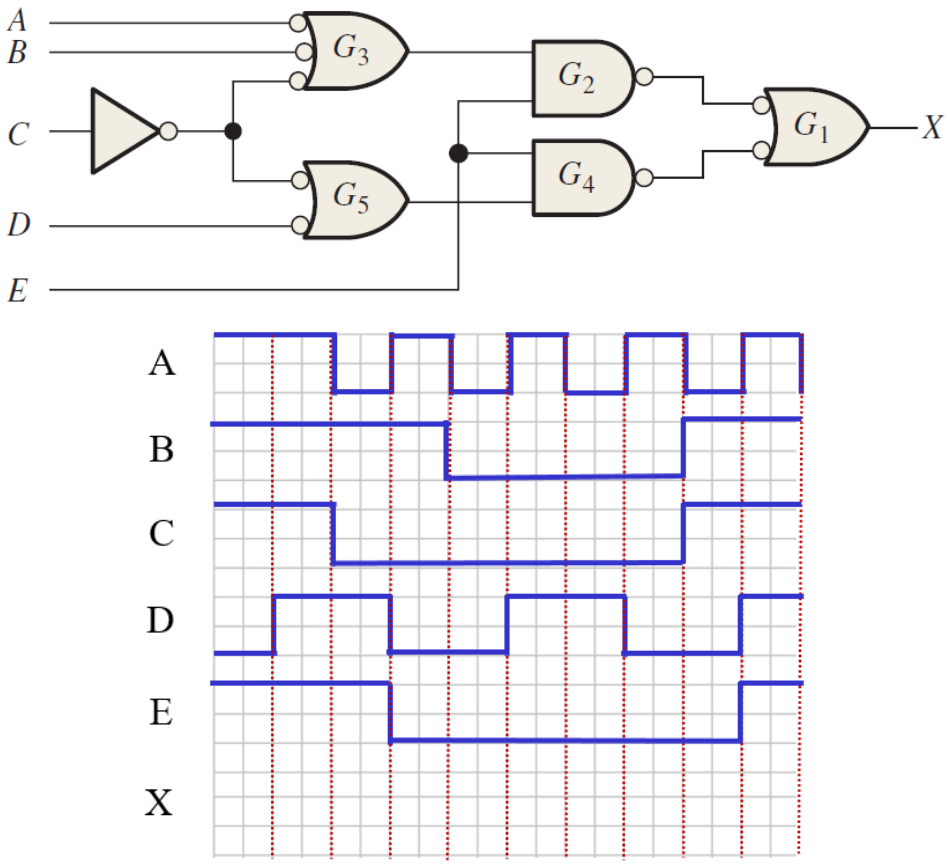

Figure 4: Combinational logic circuit and input waveform for Q.4.

(1) (5 points) Derive the expression of the output X and draw its waveform;

(2) (5 points) Assuming that the output of gate G3 is open, derive the expression of the output X and draw its waveform.

Solution:

(1) $X = \bar{A}E + \bar{B}E + CE + \bar{D}E$

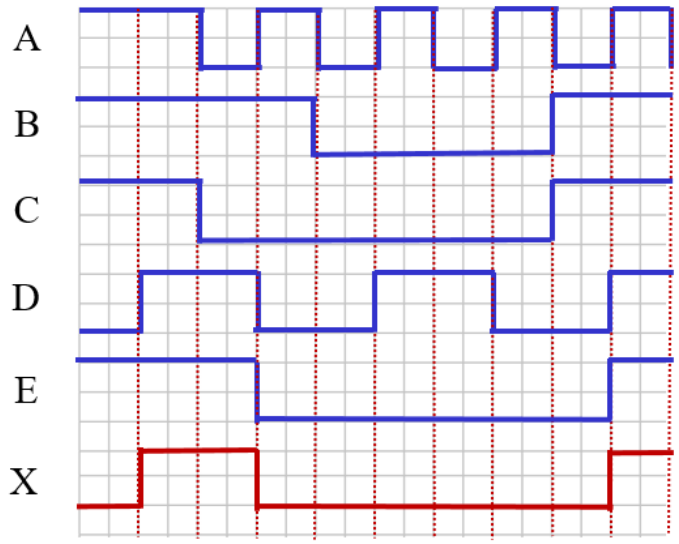

Figure 5: Output waveform of X for Q.4(1).

(2) $X = E$

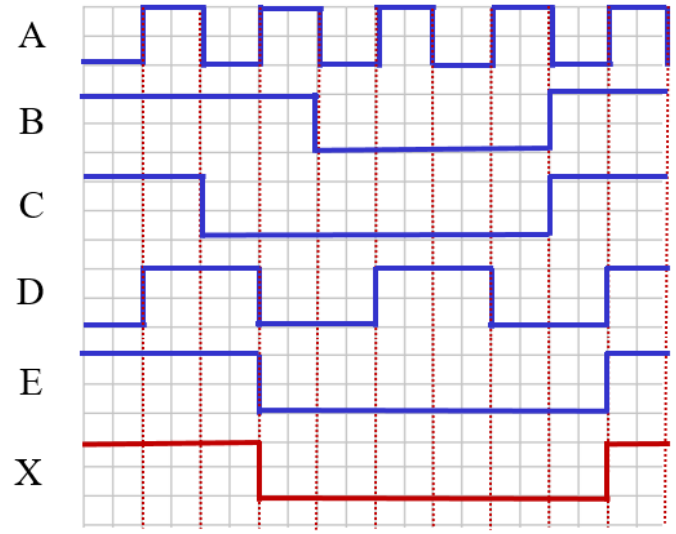

Figure 6: Output waveform of X for Q.4(2).

5. (20 points) A circuit that compares two 2-bit numbers, $A = \{A_1, A_0\}$ and $B = \{B_1, B_0\}$, and produces the output $C = \{C_1, C_0\}$ as follows:

- C equals to the lowest input (for example if $A = 11$ and $B = 10$, then $C = 10$);
- C is a don't care if $A = B$.

(1) (5 points) Write down the truth table;

(2) (5 points) Use Karnaugh Map to simplify the Boolean expression of the outputs C_1 and C_0, show your work step by step;

(3) (5 points) Sketch the C_1 logic diagram of the circuit, using **NAND** gates only (You **CANNOT** assume that complementary inputs are directly available, i.e. $\bar{A}_1, \bar{A}_0, \bar{B}_1, \bar{B}_0$ are NOT available);

(4) (5 points) Given the input waveforms as shown in Figure 7, draw the output C_1 waveform for your design circuit in (3).

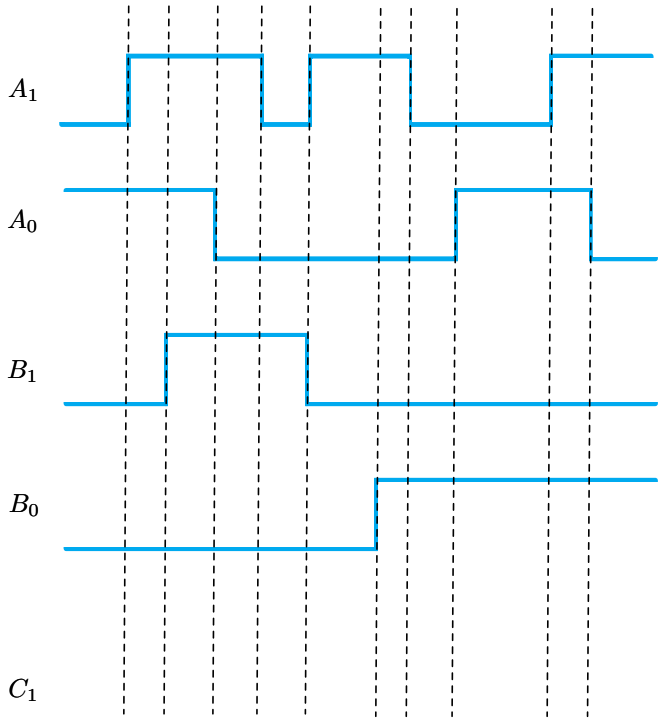

Figure 7: The input waveforms for Q.5.

Solution:

(1) The solution is shown in Table 1.

(2) The Karnaugh Map is shown in Figure 8.
$C_1 = \bar{A}_1\bar{A}_0\bar{B}_1\bar{B}_0 + \bar{A}_1A_0\bar{B}_1B_0 + A_1B_1$;
$C_0 = \bar{A}_1\bar{A}_0\bar{B}_1\bar{B}_0 + A_1\bar{A}_0B_1\bar{B}_0 + A_0B_0 + \bar{A}_1A_0B_1 + A_1\bar{B}_1B_0$.

(3) The C_1 logic diagram of the circuit is shown in Figure 9.

(4) The output C_1 waveform is shown in in Figure 10.

A_1	A_0	B_1	B_0	C_1	C_0
0	0	0	0	X	X
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	0	0
0	1	0	1	X	X
0	1	1	0	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	0	1	0	1
1	0	1	0	X	X
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	1	0	1
1	1	1	0	1	0
1	1	1	1	X	X

Table 1: The truth table.

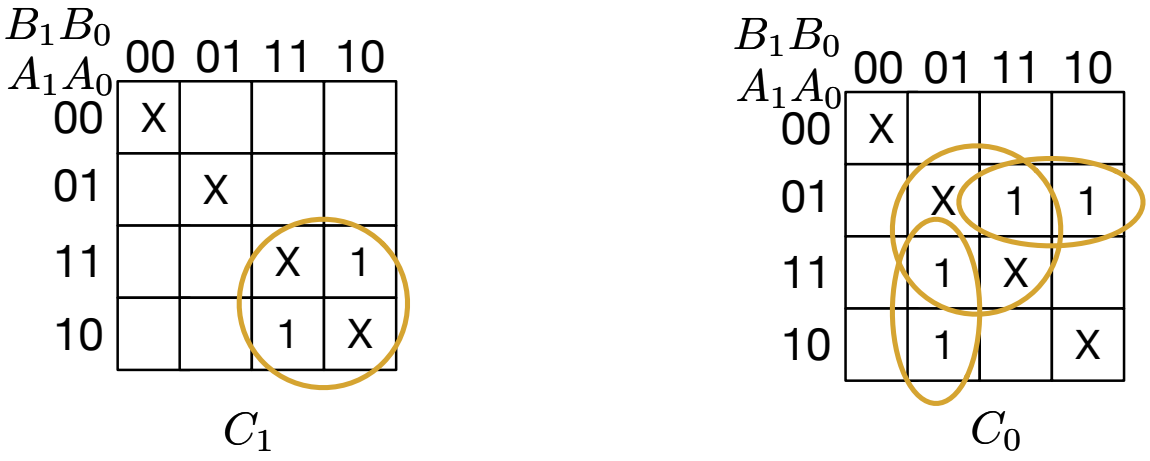

Figure 8: The Karnaugh Map.

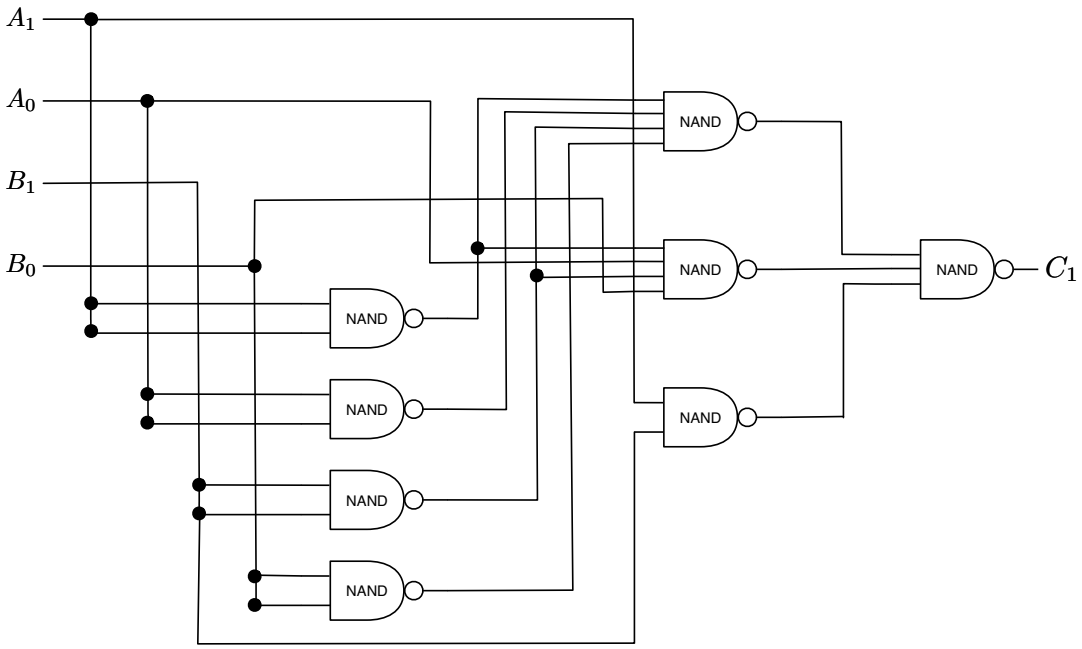

Figure 9: The C_1 logic diagram of the circuit.

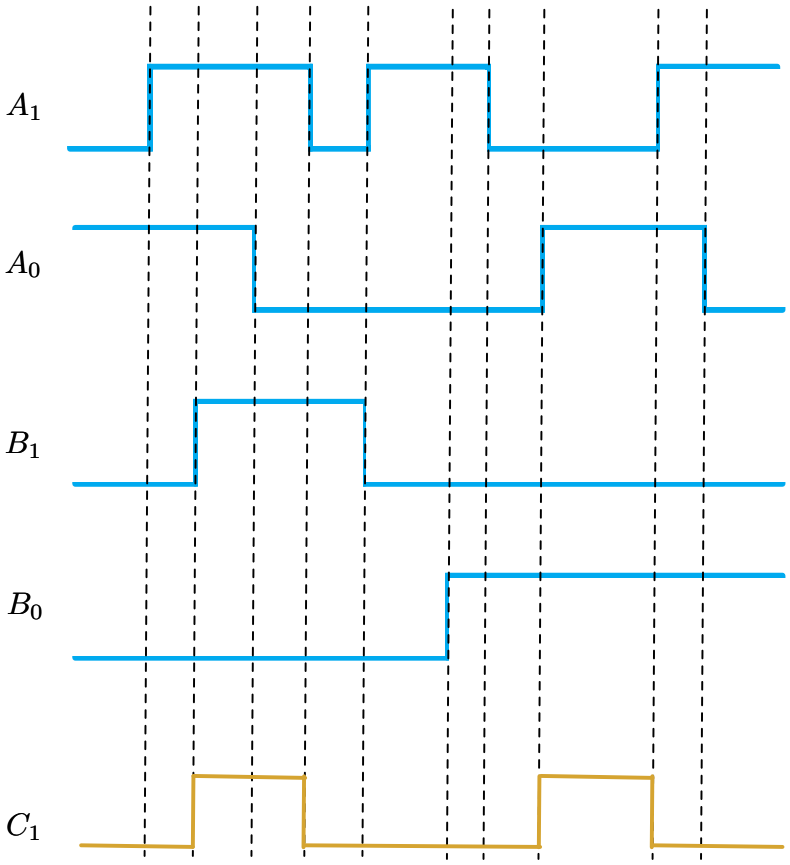

Figure 10: The output C_1 waveform.

6. (15 points) Design a magnitude comparator circuit for 2-bit binary numbers $A = \{A_1, A_0\}$ and $B = \{B_1, B_0\}$. The outputs are X, Y, and Z, where $X = 1$ if $A > B$; $X = 0$ otherwise. $Y = 1$ if $A < B$; $Y = 0$ otherwise. $Z = 1$ if $A = B$; $Z = 0$ otherwise.

(1) (9 points) Fill in the truth table in Table 2 for the three outputs of the comparator and write down the standard SOP forms for X, Y and Z;

A_1	A_0	B_1	B_0	$X(A > B)$	$Y(A < B)$	$Z(A = B)$
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

Table 2: The truth table of a magnitude comparator circuit for 2-bit binary numbers

(2) (6 points) Implement Z logic diagram of the circuit using a 74HC154 decoder as shown in Figure 11 and one or several NAND gates (Connect ALL input pins as needed; You may assume that complementary inputs, if needed, are directly available, i.e. $\bar{A}_1, \bar{A}_0, \bar{B}_1, \bar{B}_0$ are available).

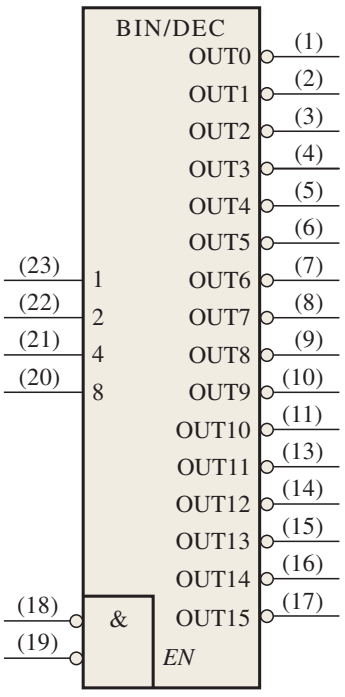

Figure 11: The 74HC154 decoder.

Solution:

(1) The truth table is shown in Table 3. The standard SOP forms are

$$X = \bar{A}_1 A_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + A_1 \bar{A}_0 \bar{B}_1 B_0 + A_1 A_0 \bar{B}_1 \bar{B}_0 + A_1 A_0 \bar{B}_1 B_0 + A_1 A_0 B_1 \bar{B}_0$$

$$Y = \bar{A}_1 \bar{A}_0 \bar{B}_1 B_0 + \bar{A}_1 \bar{A}_0 B_1 \bar{B}_0 + \bar{A}_1 \bar{A}_0 B_1 B_0 + \bar{A}_1 A_0 B_1 \bar{B}_0 + \bar{A}_1 A_0 B_1 B_0 + A_1 \bar{A}_0 B_1 B_0$$

$$Z = \bar{A}_1 \bar{A}_0 \bar{B}_1 \bar{B}_0 + \bar{A}_1 A_0 \bar{B}_1 B_0 + A_1 \bar{A}_0 B_1 \bar{B}_0 + A_1 A_0 B_1 B_0$$

(2) The Z logic diagram of the circuit is shown in Figure 12.

A_1	A_0	B_1	B_0	$X(A > B)$	$Y(A < B)$	$Z(A = B)$
0	0	0	0	0	0	1
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	1	0	0	1	0	0
0	1	0	1	0	0	1
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	0	1
1	0	1	1	0	1	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	0	1

Table 3: The truth table of a magnitude comparator circuit for 2-bit binary numbers

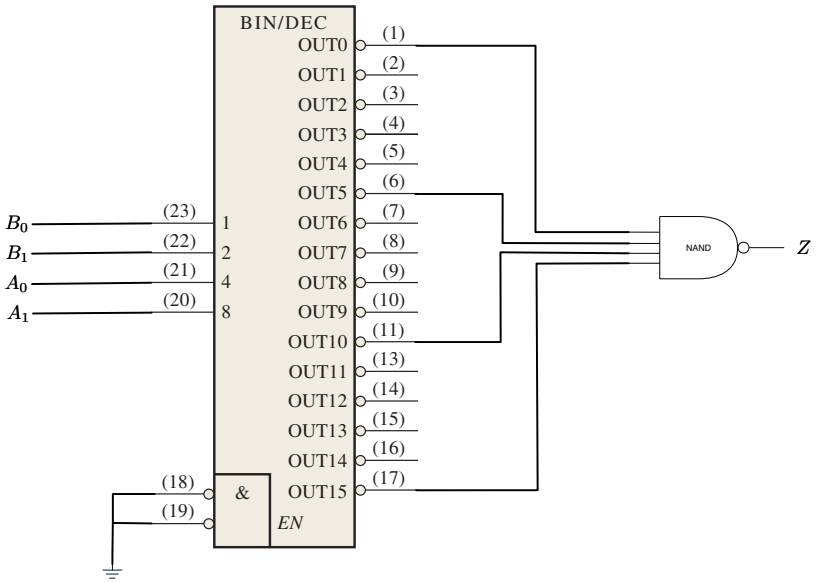

Figure 12: The Z logic diagram of the circuit.

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7. (10 points) Consider the boolean expressions as follows,

$$D_0 = X\bar{S}_1\bar{S}_0 + YS_1\bar{S}_0$$
$$D_1 = X\bar{S}_1S_0 + YS_1S_0$$
$$D_2 = XS_1\bar{S}_0 + Y\bar{S}_1\bar{S}_0$$
$$D_0 = XS_1S_0 + Y\bar{S}_1S_0$$

Design a circuit to implement the boolean expressions using 1-of-4 decoders as shown in Figure 13 and NAND gates, where the truth table of 1-of-4 decoder is shown in Table 4. (Connect ALL input pins as needed. You may assume that complementary inputs, if needed, are directly available - e.g., both A_0 and $\bar{A}_0$ are available).

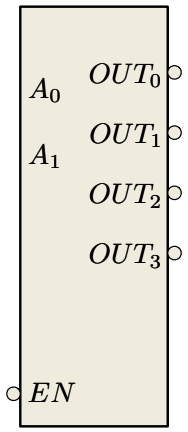

Figure 13: A 2-line-to-4-line (1-of-4) decoder.

EN	A_1	A_0	OUT_0	OUT_1	OUT_2	OUT_3
0	X	X	1	1	1	1
1	0	0	0	1	1	1
1	0	1	1	0	1	1
1	1	0	1	1	0	1
1	1	1	1	1	1	0

Table 4: The truth table of 2-line-to-4-line (1-of-4) decoder

Solution: The designed circuit is shown in Figure 14.

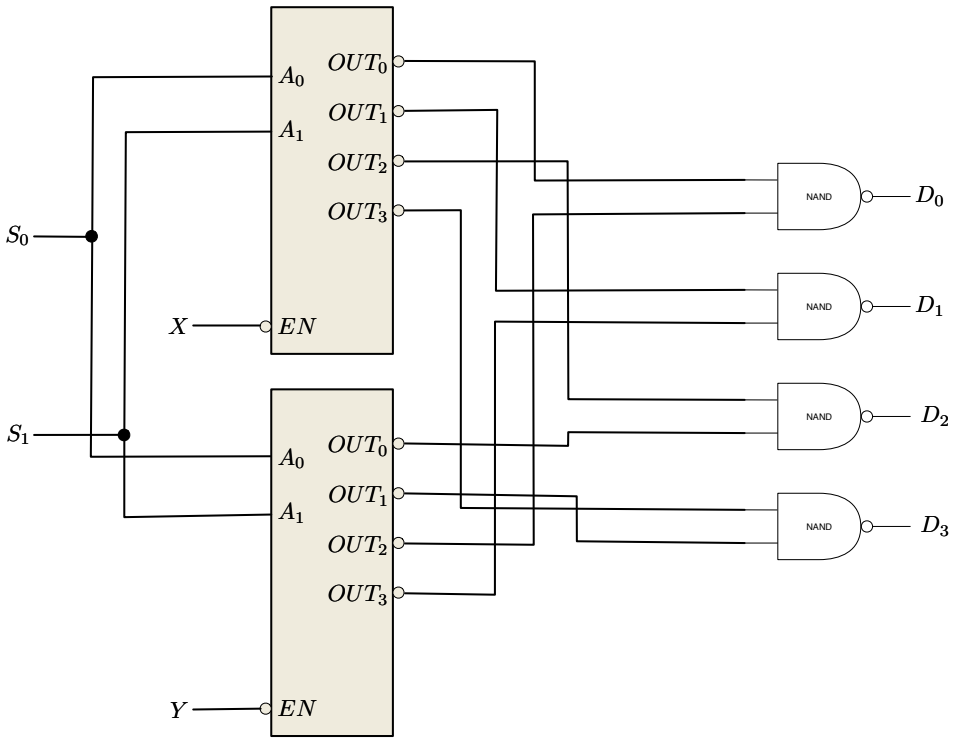

Figure 14: Q7 solution.

8. (10 points) In Chapter 6, we have studied a simplified method of multiplexing two four-bit BCD numbers to a single BCD-to-7-segment decoder as shown in Figure 15. Note that the 74HC157 is a quad 2-input multiplexer. If the data-select line is LOW, the multiplex passes A bits (A_3, A_2, A_1, A_0) to the BCD-to-7-segment decoder. In contrast, if the data-select line is HIGH, the multiplex passes B bits (B_3, B_2, B_1, B_0) to the BCD-to-7-segment decoder.

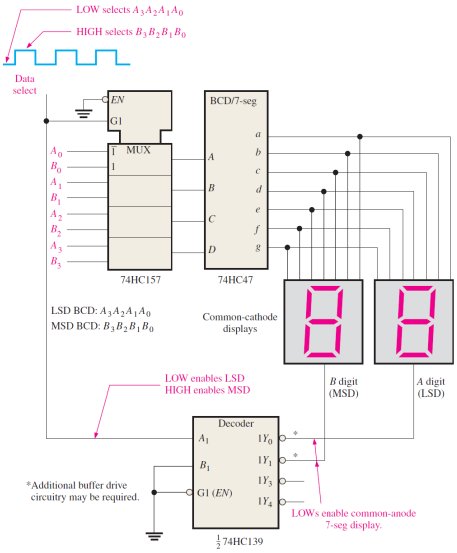

Figure 15: Simplified 7-segment display multiplexing logic from the textbook.

Now, we would like to extend this design to multiplexing THREE four-bit BCD numbers with only ONE additional multiplexer and one additional data-select line.

(1) (5 points) Design and draw the data-select input waveform for both S_1 and S_2;

(2) (5 points) Complete the circuit shown in Figure 16 by properly connecting all the components, assuming that the third BCD C is represented by (C_3, C_2, C_1, C_0)

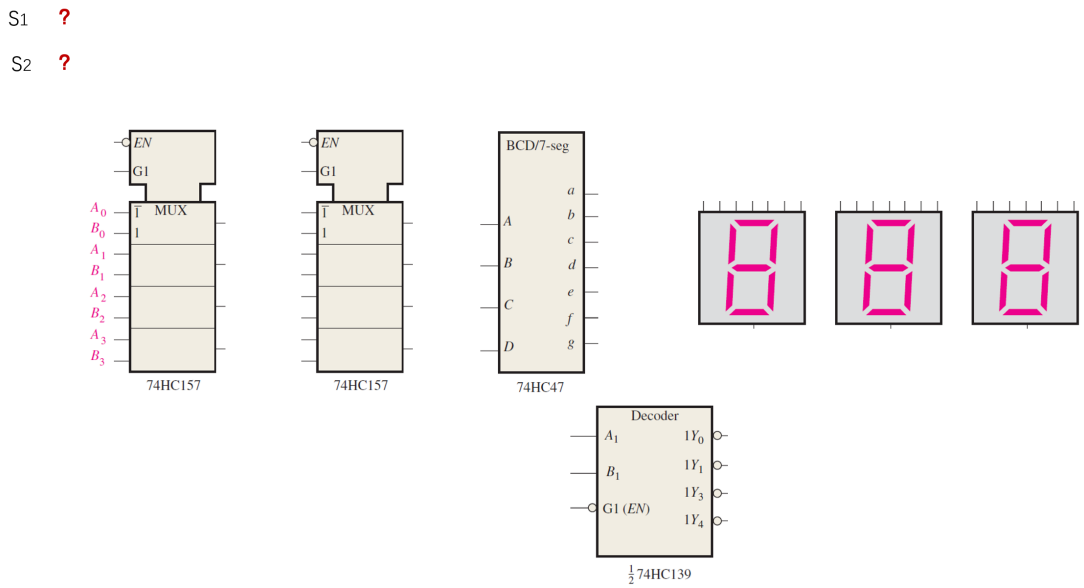

Figure 16: Multiplexing three four-bit BCD numbers.

Solution:

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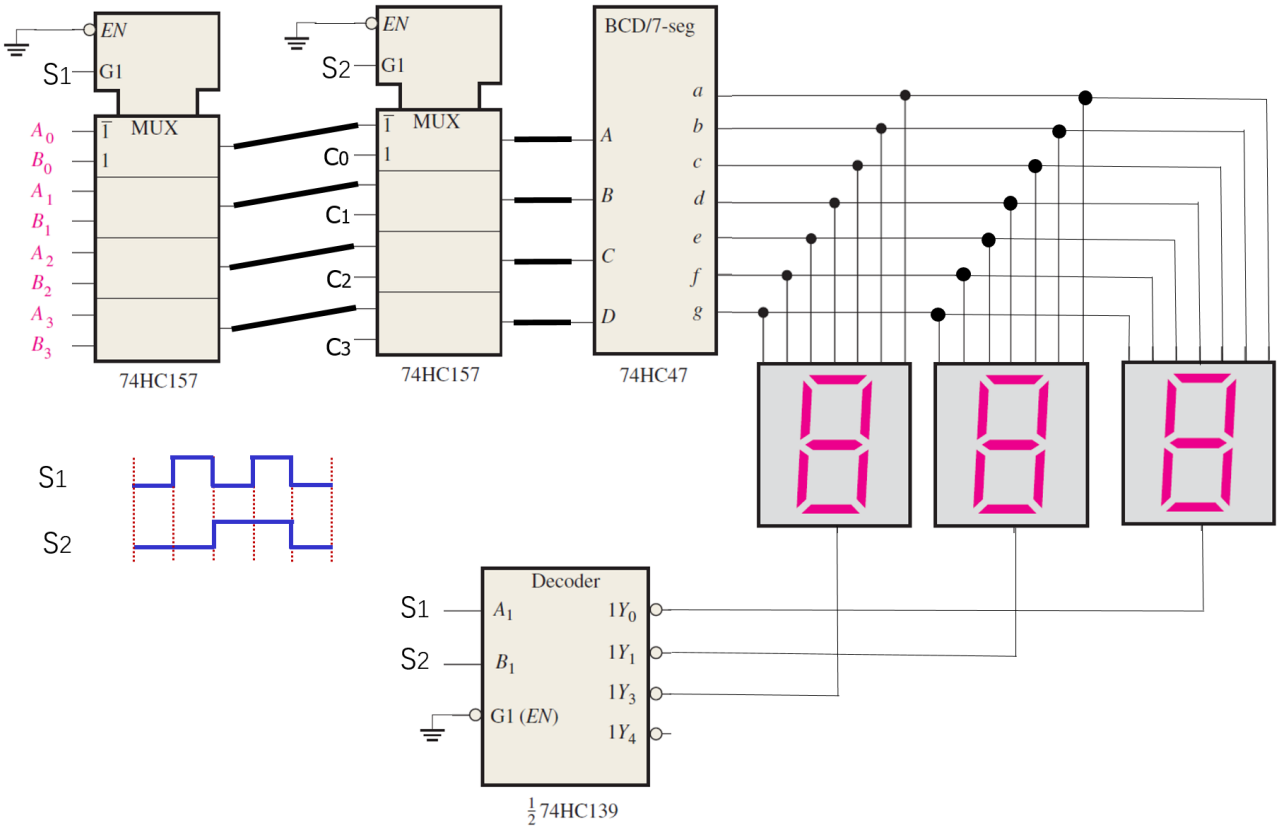

Figure 17: Solution for Q.8.