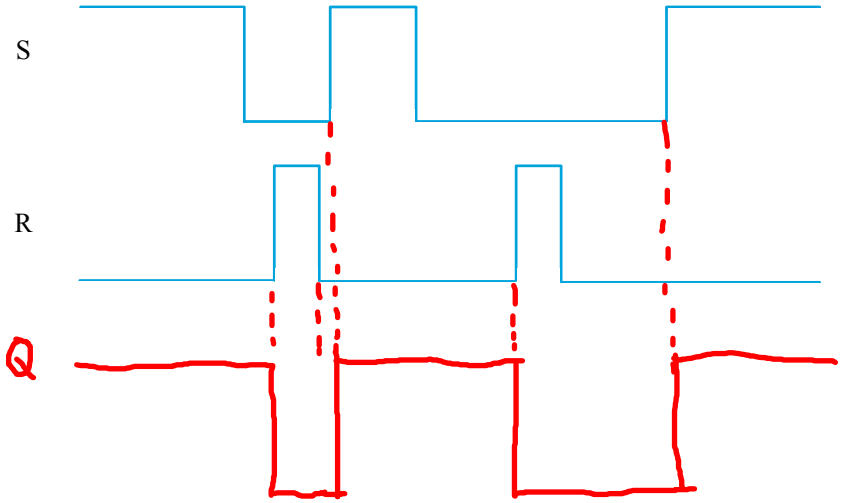
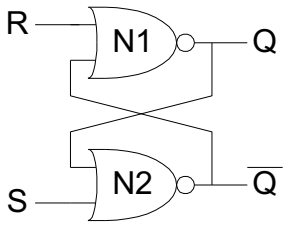
ECE2050 Homework 6

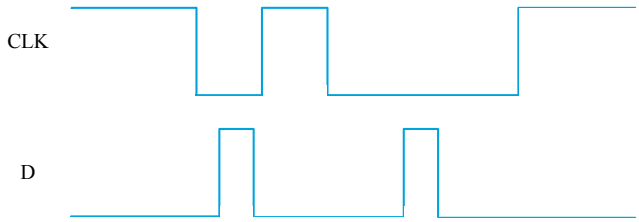
Due: March 29, 2025

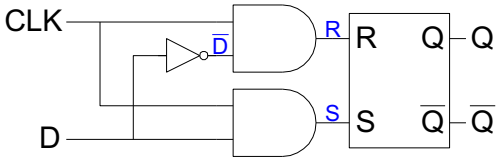
Q1 Given the input waveforms shown below, sketch the output, Q, of an SR latch.





Q2 Determine the output of a D Latch for the inputs below.

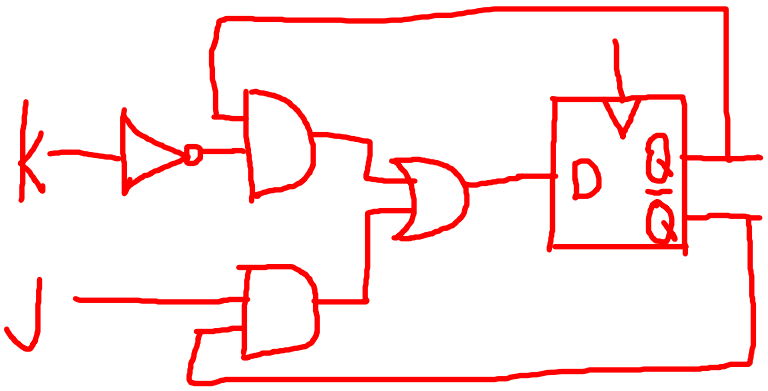


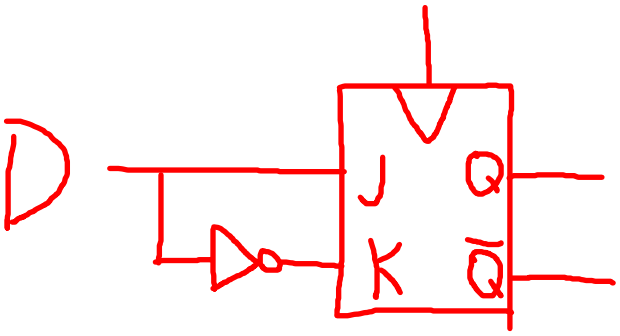


Q ——————— Low

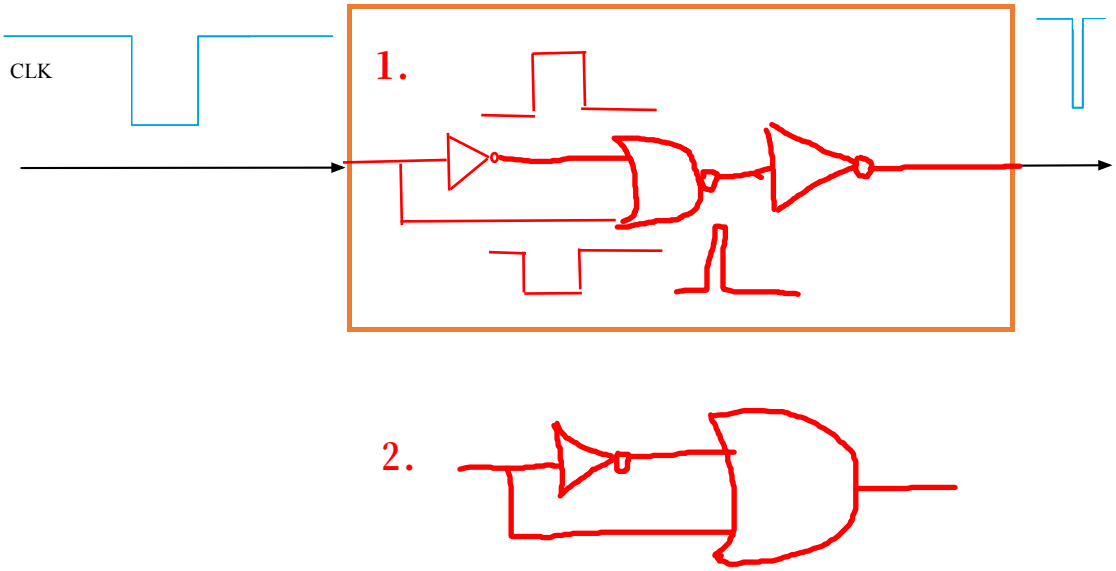
Q3 Construct the following flip-flops:

- Construct a JK flip-flop, using a D flip-flop and some combinational logic.
- Construct a D flip-flop, using a JK flip-flop and some combinational logic.

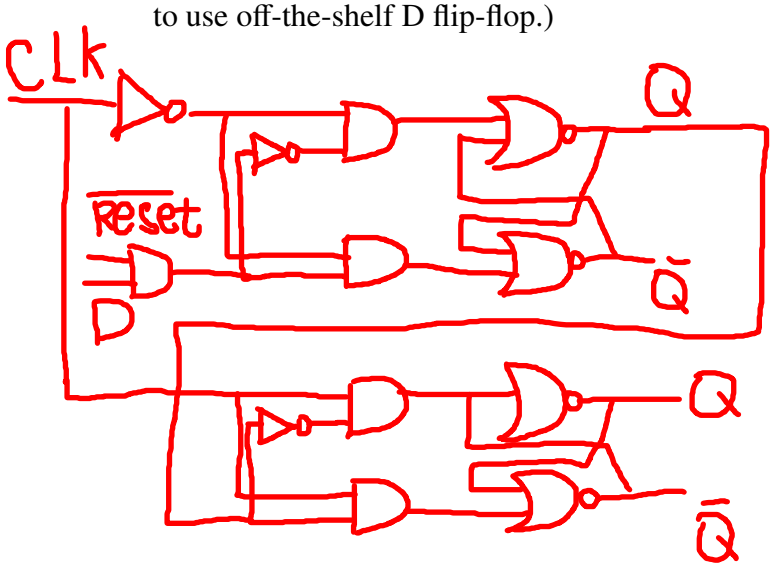




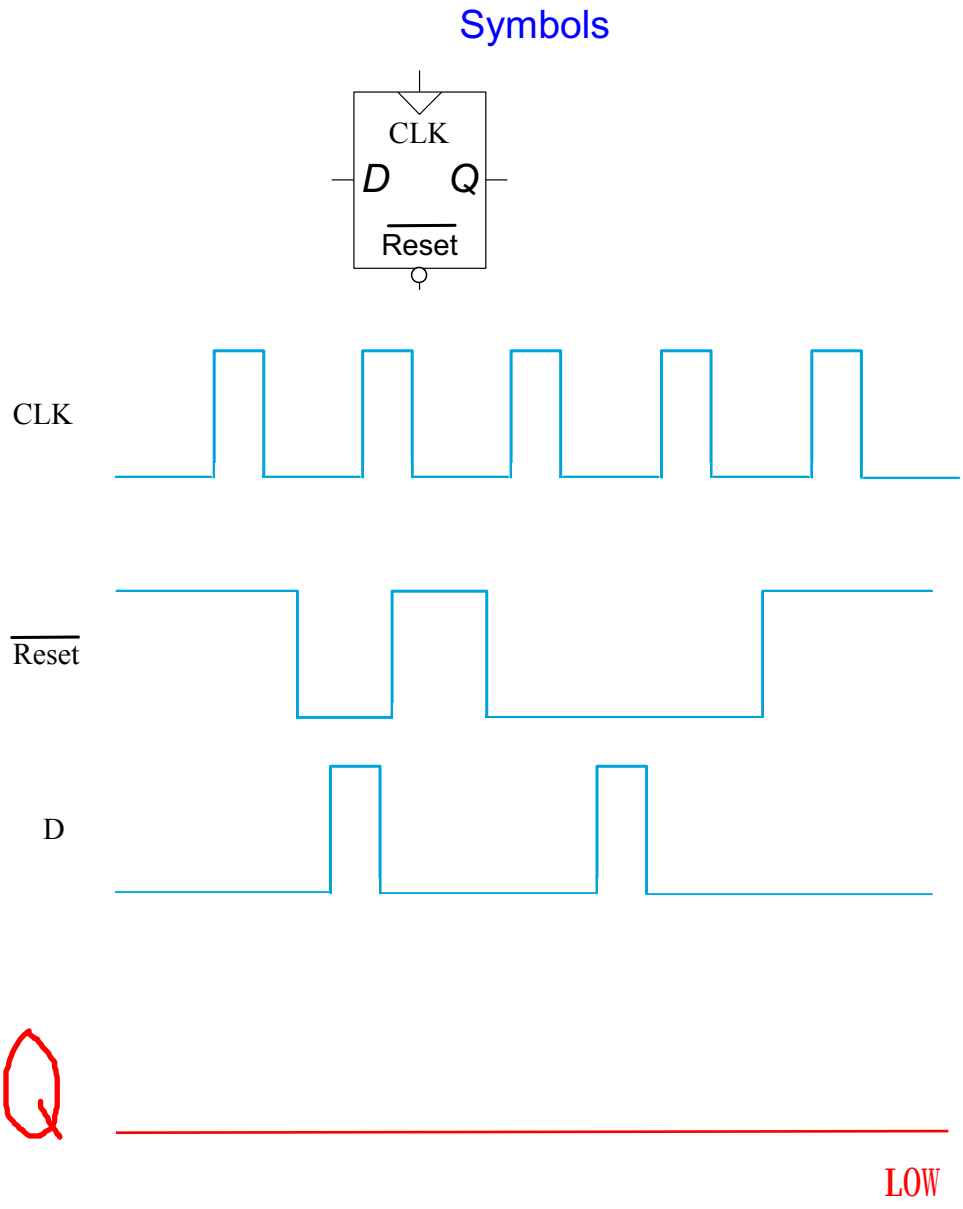
Q4 Design a circuit to generate a very short-duration negative spike on the negative-going transition of the clock pulse. (You are not allowed to use more than two inverters.)



Q5 Design a synchronous resettable D flip-flop, using basic logic gates. (You are not allowed to use off-the-shelf D flip-flop.)



Q6 Determine the output Q of a synchronous resettable D flip-flop for the inputs below. (The input $\overline{Reset}$ is active-low.)



Q7 Determine the output Q of an asynchronous resettable D flip-flop for the inputs below. (The input Reset is active-high.)