ECE2810 Digital Systems Design Laboratory

# Laboratory Report #1

Name:

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- Experiment A: AND logic and Diode-based Circuit
- Experiment B: AND Gate
- Experiment C: NOT Gate (Inverter)

## 1. Experiment A

1.1 Result

Result Table Signal measured for AND based on diodes.

| | A (V) | B (V) | $V_O$ (V) |
|---|---|---|---|
| (0,0) | 0.01 | 0.01 | 0.65 |
| (0,1) | 0.01 | 4.98 | 0.69 |
| (1,0) | 4.98 | 0.01 | 0.68 |
| (1,1) | 4.98 | 4.98 | 4.98 |

1.2 Question

The circuit on the breadboard implements an AND gate using discrete electronic components. In this setup, the two inputs are labeled A and B, while the output is labeled O. The logic works as follows:

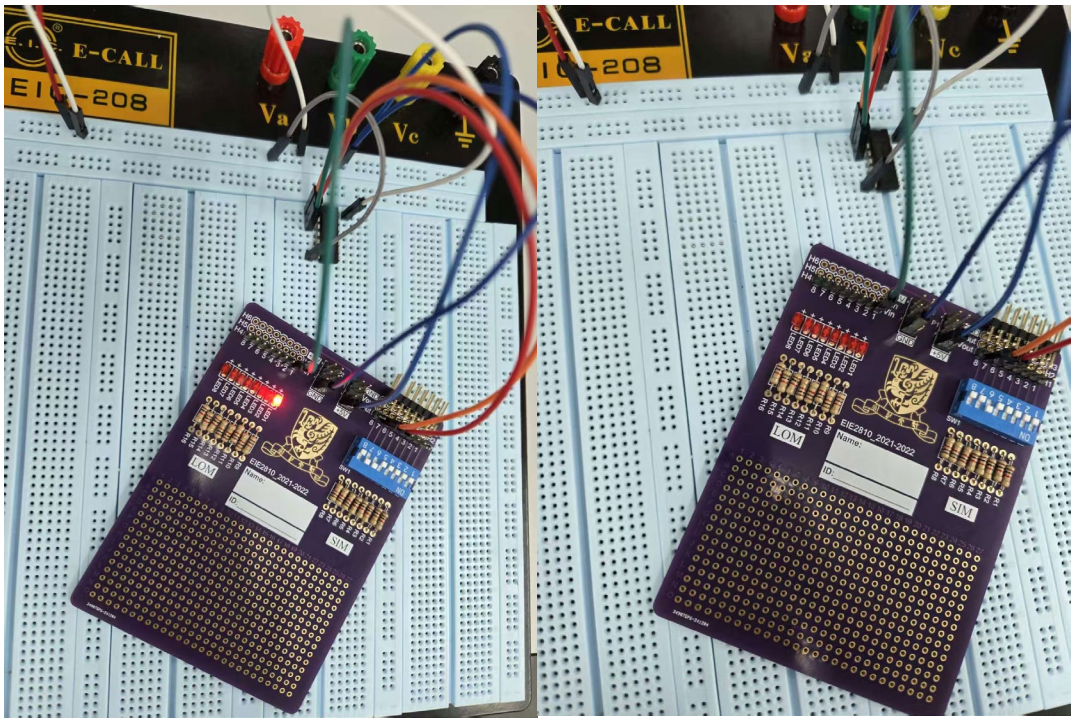
When both input pins A and B are supplied with a high voltage level (logic “1”), the output node O is also driven to a high voltage (logic “1”).

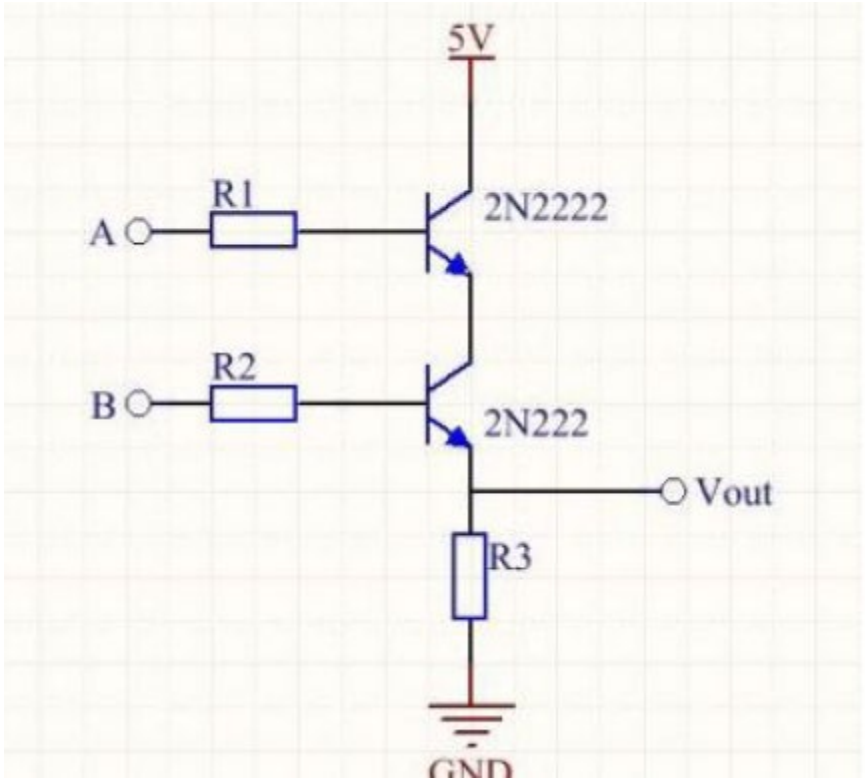
If either input A or input B is at a low voltage (logic “0”), or if both are low, the output remains at a low voltage (logic “0”).

This behavior directly corresponds to the truth table of an AND logic gate, where the output is high only if all inputs are high. Thus, the circuit achieves the logical AND function through the controlled switching of current paths, ensuring that the output reflects the simultaneous presence of high signals at both inputs.

## 2. Experiment B

2.10Design



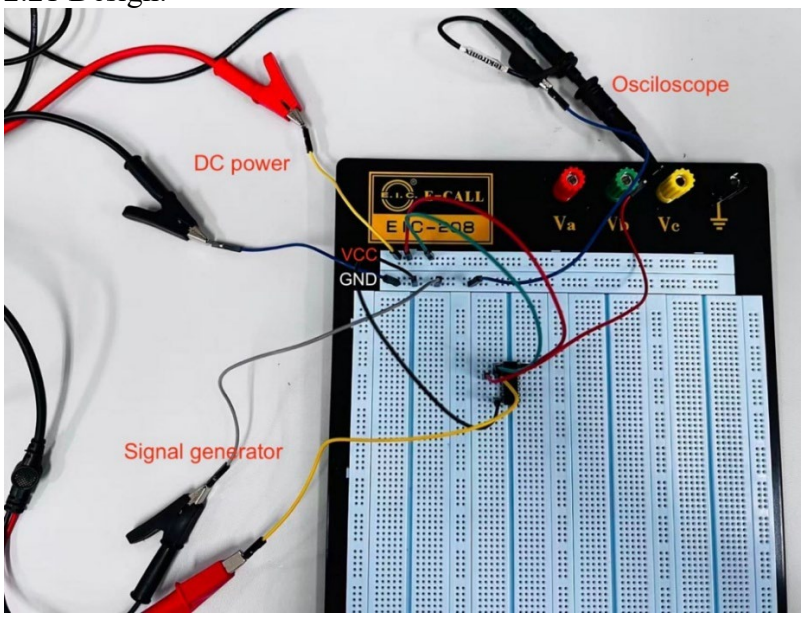



2.11Result

| | 1A (V) | 1B (V) | 1Y (V) |
|---|---|---|---|
| (0,0) | 0.01 | 0.01 | 0.01 |
| (0,1) | 0.01 | 4.98 | 0.01 |
| (1,0) | 4.98 | 0.01 | 0.01 |
| (1,1) | 4.98 | 4.98 | 4.75 |

**2.20 CMOS voltage levels**

2.21 Design:




2.22 Result: VIH=3.5V VIL=1.9V



## 2.30 73LS08

2.31 Results

| | 1A (V) | 1B (V) | 1Y (V) |
|---|---|---|---|
| (0, 0) | 0.01 | 0.01 | 0.01 |
| (0, 1) | 0.01 | 4.90 | 0.01 |
| (1, 0) | 4.90 | 0.01 | 0.01 |
| (1, 1) | 4.90 | 4.90 | 3.45 |

## 2.40 TTL voltage levels

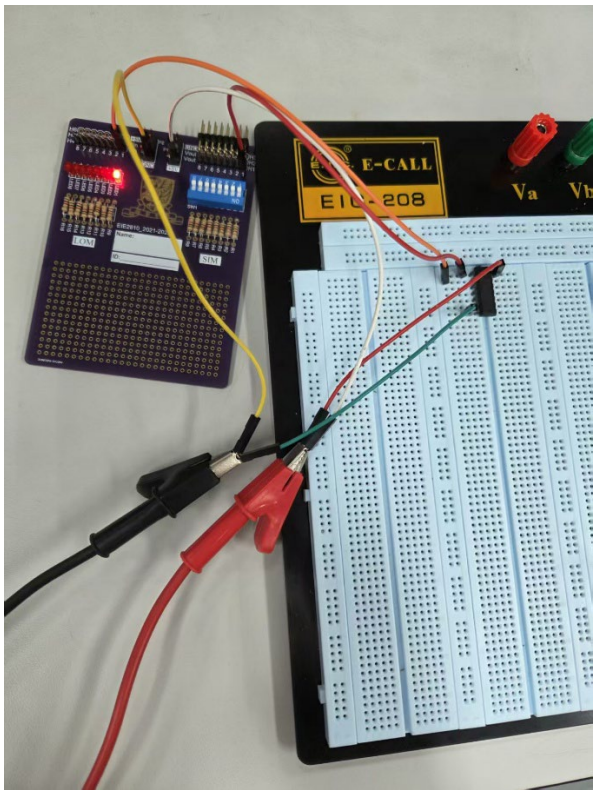
2.41 Results VIH = 1.3V VIL=1.9V

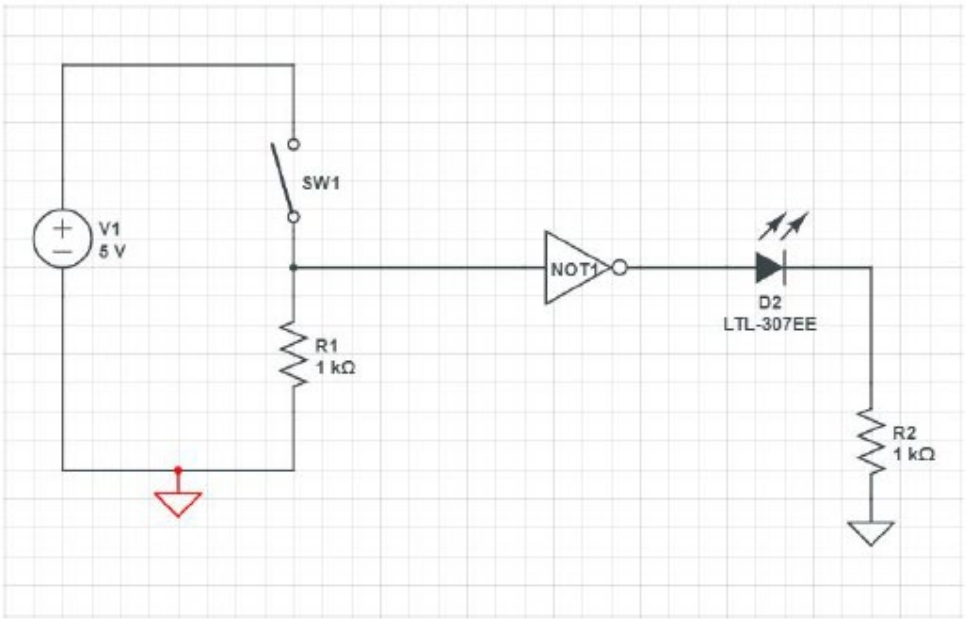


# 3 Experiment C

## 3.10 74HC04 Inverter

3.11 Design:



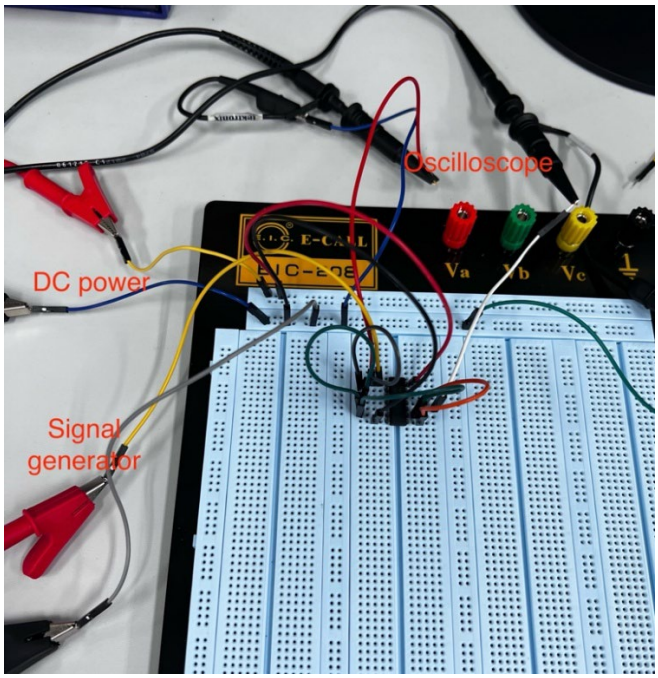

One channel of SIM is connected to Pin 1A of 74HC04, and one channel of LOM is connected to Pin 1Y. Pin 7 is connected to the ground and Pin 14 is connected to VCC = 5V. Use a multimeter to measure the voltage of Pin 1A and Pin 1Y for different situations.

3.12 Result:

| | **Vin (1A)** | **Vout (1B)** |
|---|---|---|
| 0 | 4.98 | 0.01 |
| 1 | 0 | 4.98 |

**3.20 Propagation Delay Time**

3.21 Design:




3.22 Results:


In the experiment, a square wave was applied to a chain of five cascaded inverters. The input and the final output signals were measured using CH1 and CH2 of the oscilloscope. By observing the rising and falling edges of the signals, the propagation delays **tPHL** (high-to-low transition) and **tPLH** (low-to-high transition) were

determined.

The measurement method is as follows: the 50% voltage level of the input and output transitions is used as the reference point. The time difference between the input change and the output change gives the propagation delay. Since five inverters are connected in series, the total measured delay corresponds to the accumulated delay of all five stages. The delay of a single inverter can be estimated by dividing the total delay by 5.
The final report should include:

1. Oscilloscope screenshots of the input and output waveforms, with the measured **tPHL** and **tPLH** indicated.
2. Calculation of the average propagation delay per inverter using:
   tp = (tPHL + tPLH) / 2
   tp(single) = tp / 5

tPLH = 25.00 / 5 = 5.00ns
tPHL = 31.00 / 5 =6.2ns
tp = (tPLH+tPHL)/2 = 5.60ns

## Conclusion

In this laboratory session, we explored the use of a logic analyzer with SIMs, extracted information from datasheets, constructed and validated AND Gates using diodes or transistors, confirmed the logic functionality of the 74HC08, 74LS08, and 74HC04 integrated circuits (ICs), and evaluated and compared their electrical characteristics. Key takeaways from the lab include:

1. The importance of testing conditions when assessing the electrical properties of ICs, as variations in these conditions can result in significant errors.
2. Methods for retrieving essential information about ICs.
3. Techniques for measuring the propagation delay times of inverters.
4. Procedures for operating a logic analyzer.
5. Approaches to designing AND Gates, along with the principles and logic underlying their construction.