ECE2810 Digital Systems Design Laboratory

Laboratory Report #2

Name:

Student ID:

Date:

2025-9-26

The Chinese University of Hong Kong, Shenzhen

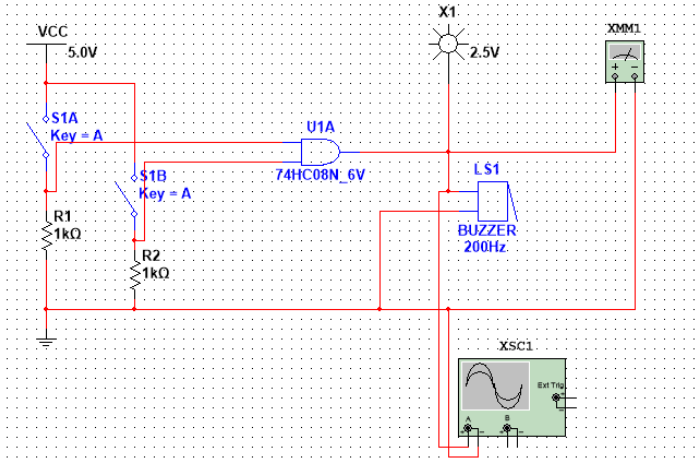
- Experiment A: Using Logic Analyzer
- Experiment B: Guided Multisim Simulation
- Experiment C: Individual Gate Test (Hardware Experiment)
- Experiment D: Combination of Gates (Simulation and Hardware Experiment)

1. Experiment A

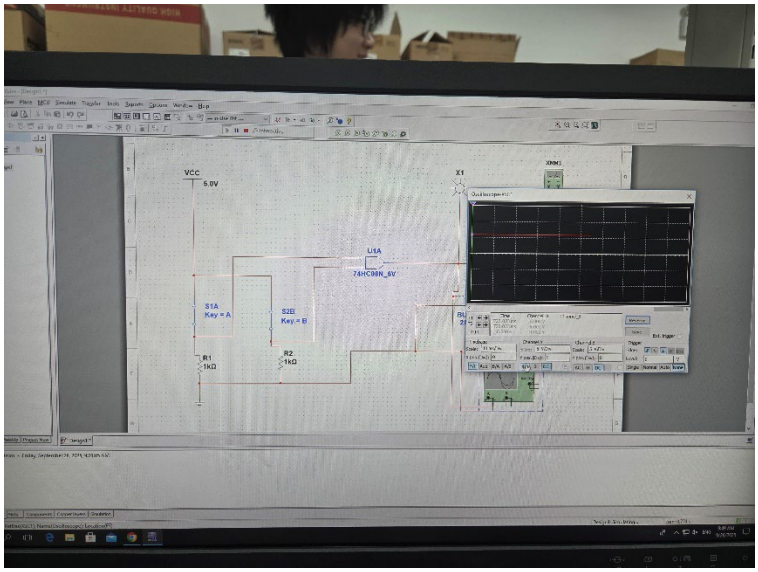
Learn how to use the logic analyzer!

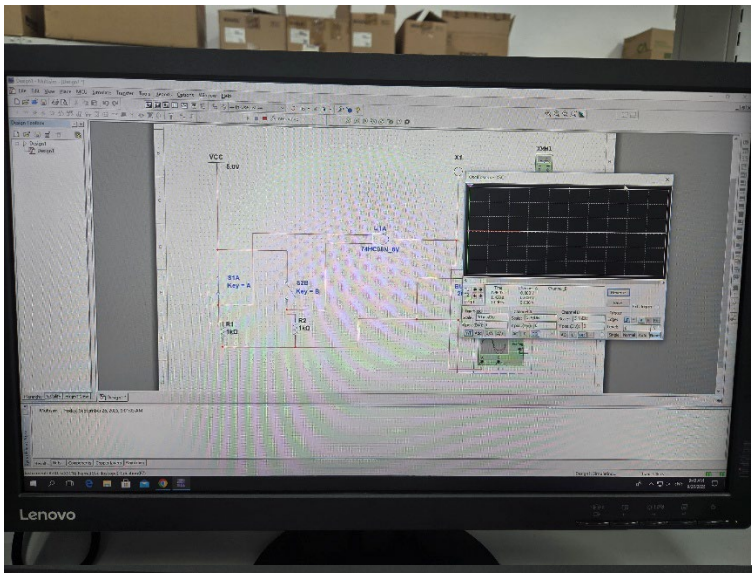
2. Experiment B

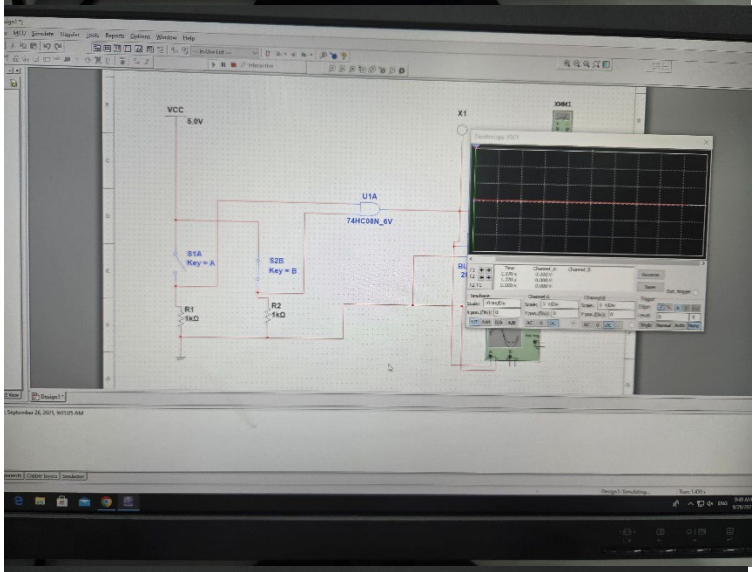
2.1 Design

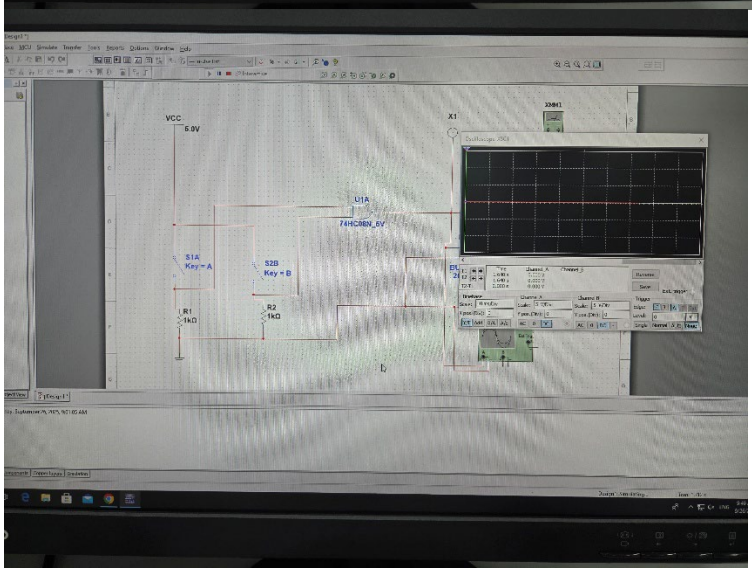


2.11Result









Learn how to use software to stimulate the behaviors of circuit designs and function

3 Experiment C

Results:

NAND GATE

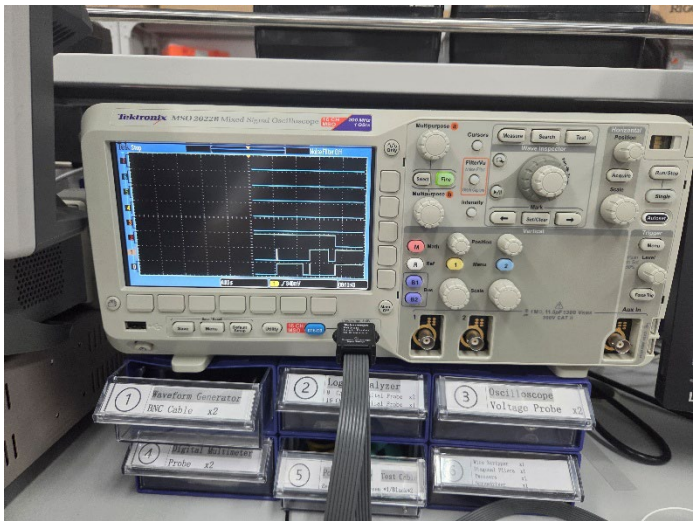


Table 1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

OR GATE

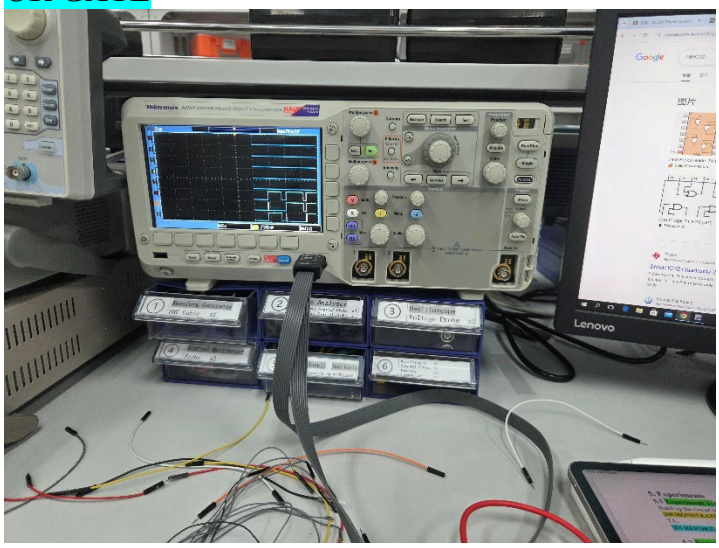


Table 3

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

XOR GATE

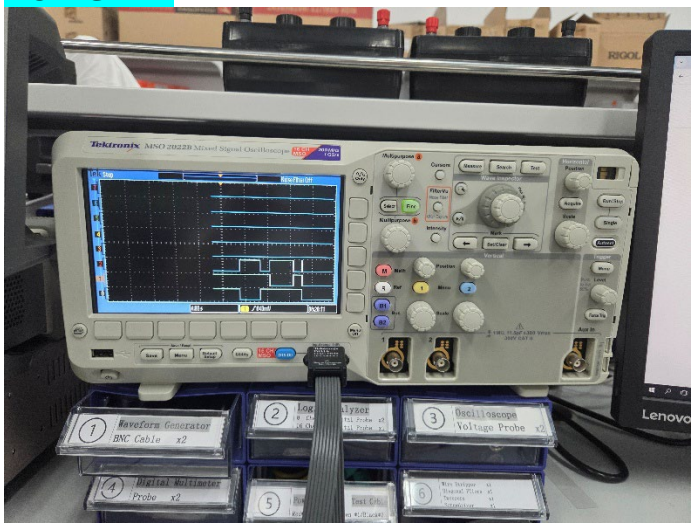


Table 4

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XNOR GATE

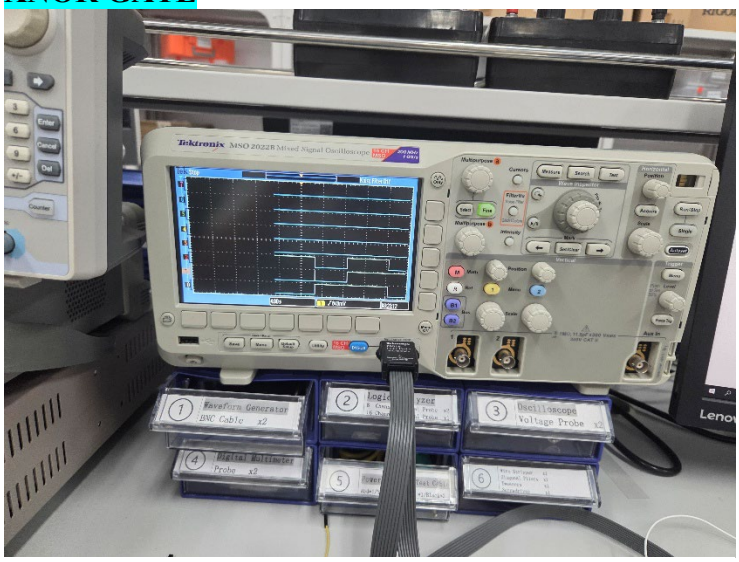


Table 5

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

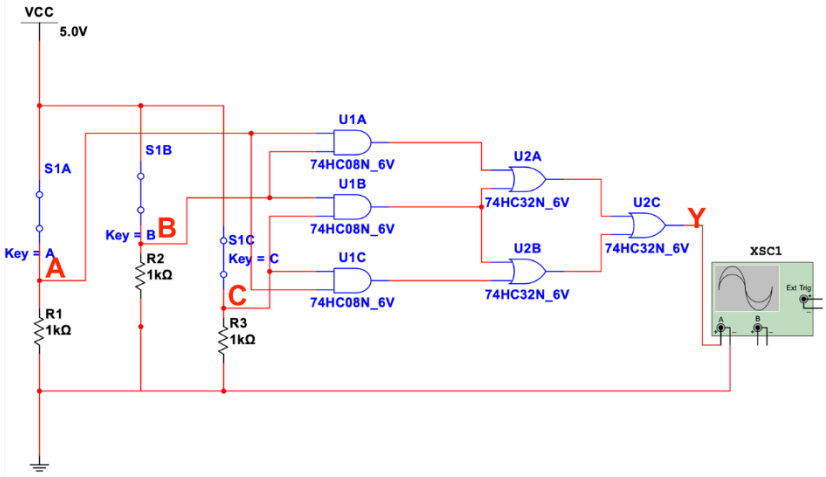
NOR GATE

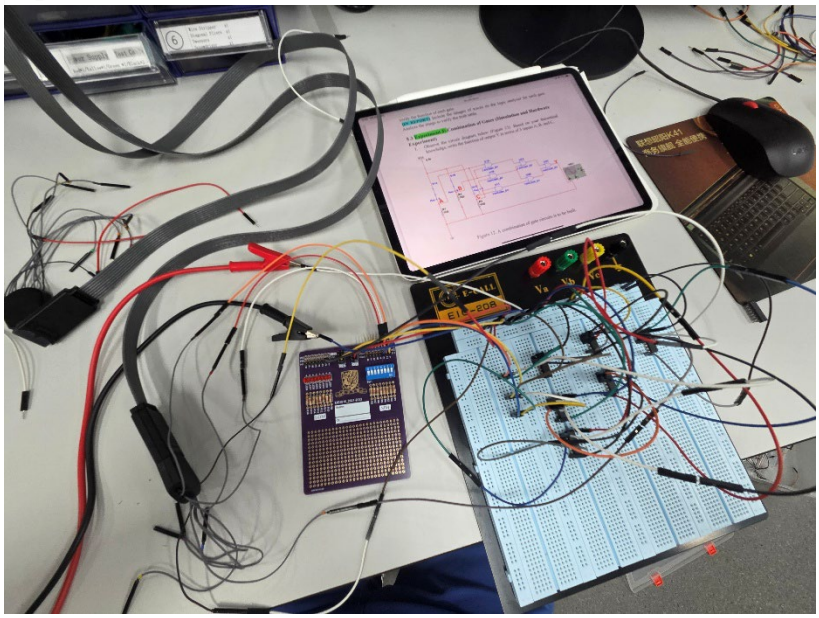
Table 2

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

4 Experiment D

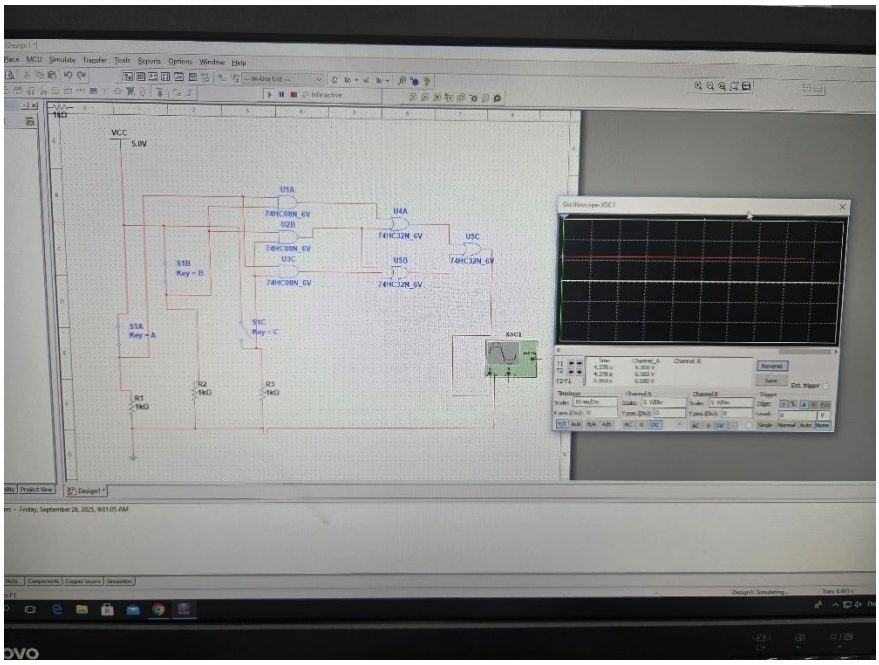
4.1 Design

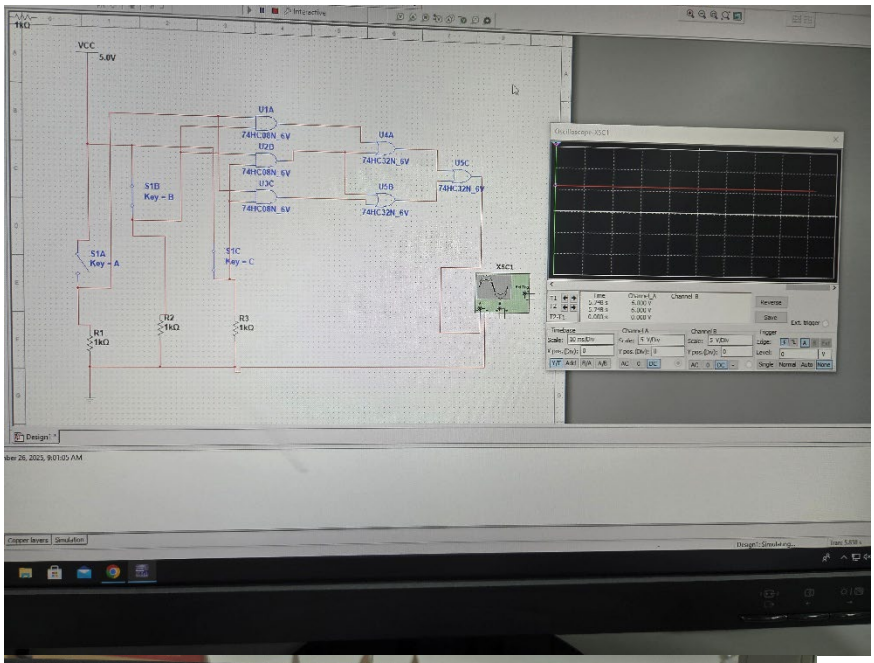


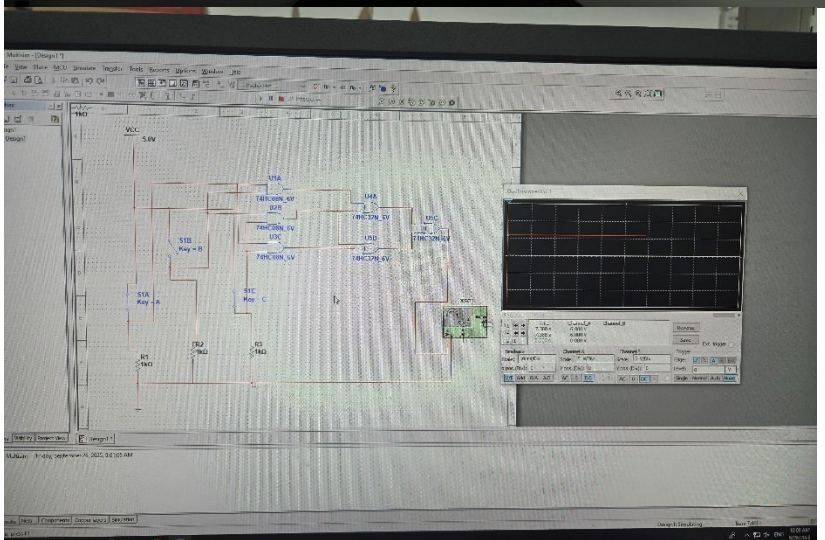


4.2 Results:

Y = AB+BC+AC




VCC
5.0V
U1A
74HC08N_5V
U2D
74HC08N_5V
U3C
74HC08N_5V
U4A
74HC32N_5V
U5B
74HC32N_5V
U5C
74HC32N_5V
S1B
Key = B
S1A
Key = A
S1C
Key = C
X1C1
R1
1kΩ
R2
1kΩ
R3
1kΩ
Oscilloscope-XSC1
Design1 *


VCC
5.0V
U1A
74HC08N_5V
U2D
74HC08N_5V
U3C
74HC08N_5V
U4A
74HC32N_5V
U5B
74HC32N_5V
U5C
74HC32N_5V
S1B
Key = B
S1A
Key = A
S1C
Key = C
R1
1kΩ
R2
1kΩ
R3
1kΩ

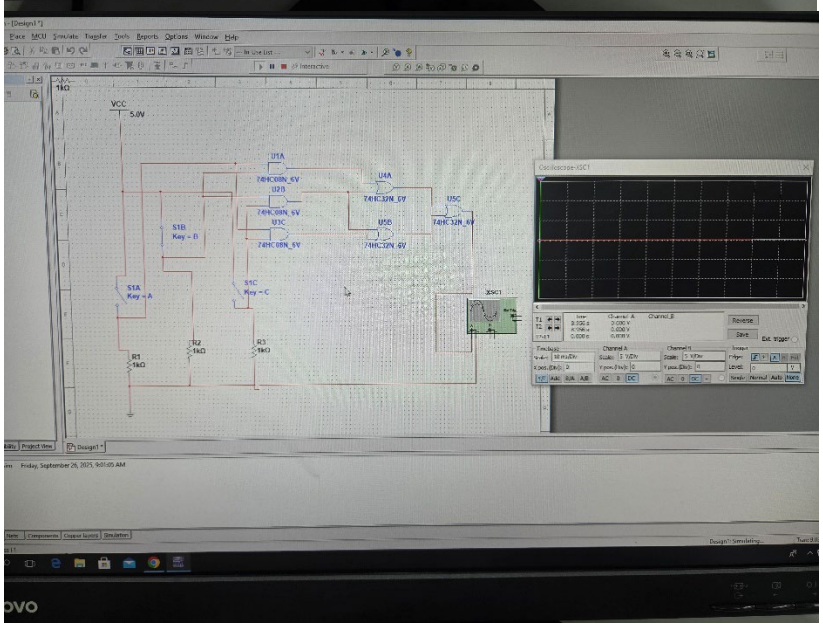
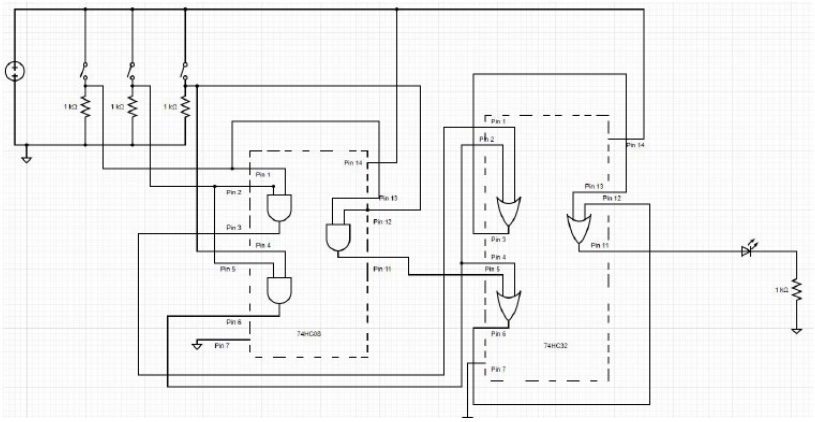

VCC
5.0V
U1A
74HC08N_5V
U2D
74HC08N_5V
U3C
74HC08N_5V
U4A
74HC32N_5V
U5B
74HC32N_5V
U5C
74HC32N_5V
S1B
Key = B
S1A
Key = A
S1C
Key = C
X1C1
R1
1kΩ
R2
1kΩ
R3
1kΩ
Oscilloscope-XSC1
Design1 *

Table 6

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1



4.3 Questions

I think it could be kind of design of Traffic Light.

Conclusion

In this lab, we learned how to use Multisim, verified the logic function of NAND Gate, NOR Gate, OR Gate, XOR Gate, and XNOR Gate, verified the functional completeness of NAND Gate, and used NAND Gates to construct AND Gate, NOT Gate, OR Gate, NOR Gate, XOR Gate, and XNOR Gate, simulated and realized a complex logic using the combination of the Gates. From the lab, we know:

1) The way to use Multisim
2) The way to construct a Gate with other kinds of Gates
3) NAND Gates have the property of functional completeness
4) The way to construct a complex logic with several kinds of Gates.