ECE2810 Digital Systems Design Laboratory

Laboratory 5

Flip-flop, Counter, Encoder

School of Science and Engineering
The Chinese University of Hong Kong, Shenzhen

2025-2026 Term 1

1. Objectives

In Laboratory 5, we will spend the 3-week session on the following:

- Learn to use a D flip-flop to upgrade a function generator to a word generator.
- Learn to design a looped counter by using a D flip-flop.
- Learn to design a responder module based on a D flip-flop.
- Learn to use an 8-3 line encoder and integrate it with the responder module and 7-segment module into a responder system.

2. Introduction

2.1 D Flip-flop

A 74HC74 is a dual D-type flip-flop with set and reset. Its function tables are shown below (Table 1). "X" means "Don't care". V_{cc} can be set as 5 V.

Table 1. Function tables of the D flip-flop.

Input			Output		
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q	$\overline{Q}$
L	H	×	×	H	L
H	L	×	×	L	H
L	L	×	×	H	H

Input			Output		
$\overline{S}_D$	$\overline{R}_D$	CP	D	Q_{n+1}	$\overline{Q}_{n+1}$
H	H	↑	L	L	H
H	H	↑	H	H	L

The logic symbol and pin arrangement are shown in Figure 1.

- When $\overline{S}_D$ and $\overline{R}_D$ are set as high, at the rising edge of CP, the state of D will be transferred to become the next state of Q, and $\overline{Q}$ will also be updated to the opposite of Q.
- When $\overline{S}_D$ is low and $\overline{R}_D$ is high, Q becomes high, and $\overline{Q}$ is low. This is state-set.
- When $\overline{S}_D$ is high and $\overline{R}_D$ is low, Q becomes low, and $\overline{Q}$ is high. This is a state-reset.
- When $\overline{S}_D$ and $\overline{R}_D$ are both low, Q and $\overline{Q}$ are both high.

With this D-type flip-flop and some basic gates, we can design several interesting and useful systems in this lab.

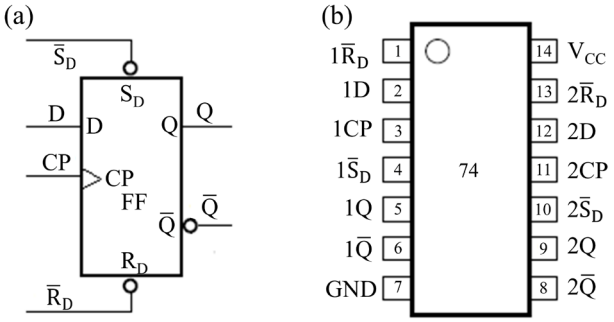

Figure 1. 74HC74 logic symbol and pin arrangement. (a) Logic symbol. (b) pin arrangement.

2.2 8-3 Line Priority Encoder

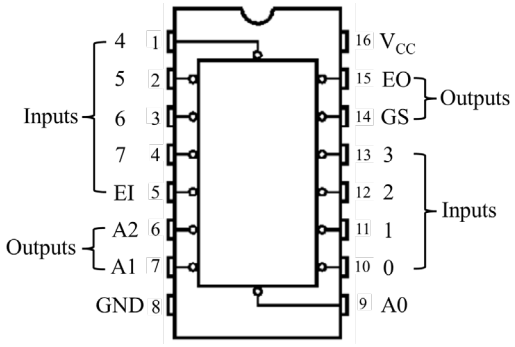

Figure 2. Pin arrangement of 74HC148.

The 74HC148 is an 8-to-3 line priority encoder that converts eight input lines into three output lines. It encodes the position of the highest-priority active input, providing a binary representation of that input. The pin arrangement and truth table are illustrated in Figure 2. V_{cc} can be set as 5 V.

Table 2. Truth table of 74HC148.

Inputs									Output				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	×	×	×	×	×	×	×	×	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	×	×	×	×	×	×	×	L	L	L	L	L	H
L	×	×	×	×	×	×	L	H	L	L	H	L	H
L	×	×	×	×	×	L	H	H	L	H	L	L	H
L	×	×	×	×	L	H	H	H	L	H	H	L	H
L	×	×	×	L	H	H	H	H	H	L	L	L	H
L	×	×	L	H	H	H	H	H	H	L	H	L	H
L	×	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Input 7 has the highest priority, while Input 0 has the lowest. When Input 7 is low, the encoder outputs will be 0×000, indicating that this input is currently selected. Please refer to the truth table (Table 2) to understand how the encoder operates under various conditions. It will be important for the experiment on the responder.

Pay attention to the scenario where all inputs are high and E1 is low: in this case, E0 will also be low, indicating that no valid signals are present. Otherwise, E0 will be high.

2.3 Other ICs Needed in the Lab

Here are some other ICs to be used in the lab.

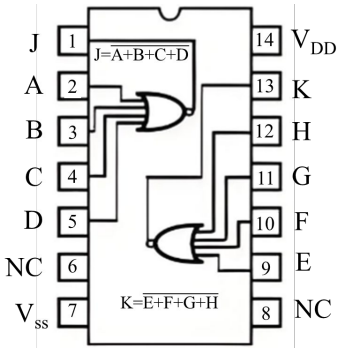

Figure 3. Pin arrangement of 4002.

(1) 4002 Chip

This chip contains two 4-input NOR gates. The pin arrangement is shown in Figure 3. V_{ss} is the ground, and V_{DD} can be set to 5V.

(2) 74HC47 and 7-Segment Display

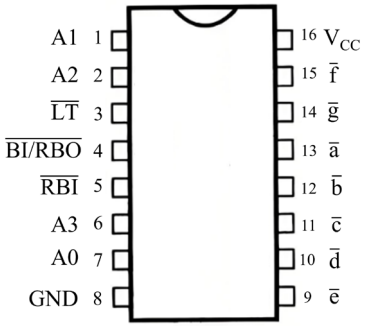

Figure 4. Pin arrangement of 74HC47.

In this experiment, we will again use the BCD-to-7-segment decoder along with a 7-segment display to present the results. For your convenience in the design, the pin arrangements and truth table are provided in Figure 4, Table 3, and Figure 5.

Table 3. Truth table of 74HC47.

	Inputs							Output							
Decimal	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\bar{a}$	$\bar{b}$	$\bar{c}$	$\bar{d}$	$\bar{e}$	$\bar{f}$	$\bar{g}$	Display
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	0
1	H	×	L	L	L	H	H	H	L	L	H	H	H	H	1
2	H	×	L	L	H	L	H	L	L	H	L	L	H	L	2
3	H	×	L	L	H	H	H	L	L	L	L	H	H	L	3
4	H	×	L	H	L	L	H	H	L	L	H	H	L	L	4
5	H	×	L	H	L	H	H	L	H	L	L	H	L	L	5
6	H	×	L	H	H	L	H	H	H	L	L	L	L	L	6
7	H	×	L	H	H	H	H	L	L	L	H	H	H	H	7
8	H	×	H	L	L	L	H	L	L	L	L	L	L	L	8
9	H	×	H	L	L	H	H	L	L	L	H	H	L	L	9
10	H	×	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	×	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	×	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	×	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	×	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	×	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	×	×	×	×	×	×	L	H	H	H	H	H	H	H	
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	
$\overline{LT}$	L	×	×	×	×	×	H	L	L	L	L	L	L	L	

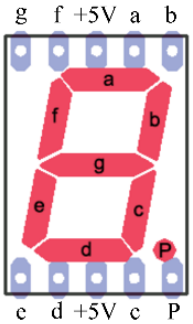

Figure 5. Pin arrangement of a 7-segment display.

3. Experiments

3.1 Experiment 1: 4-Channel Word Generator

The word generator in Multisim is extremely useful for providing inputs to logic circuits, allowing you to observe waveforms and verify logic functions. However, the function generator in the lab cannot output a series of parallel signals like the word generator. By utilizing flip-flops, you can enhance the function generator to function as a word generator.

The main concept is to use a D flip-flop to create a frequency divider. As previously mentioned, when $\overline{S}_D$ and $\overline{R}_D$ are set high, the state of D is transferred to Q at the rising edge of the clock pulse (CP), and $\overline{Q}$ is updated to the opposite of Q. As illustrated in the waveforms below, by "feeding back" the output from $\overline{Q}$ to the input terminal D, the output pulses at Q have a frequency that is exactly half ($f \div 2$) of the input clock frequency. In other words, the circuit divides the input frequency by a factor of two.

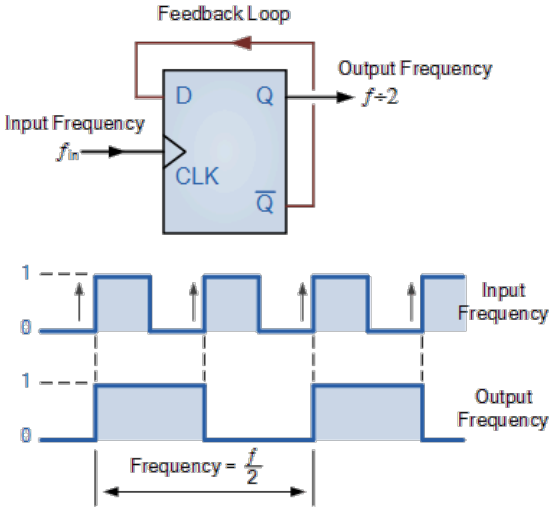

Figure 6. frequency division

(1) Design a 4-channel word generator using two 74HC74 ICs (four D flip-flops). The goal is to create a circuit that generates square waveforms at frequencies of $f/2$, $f/4$, $f/8$, and $f/16$. These waveforms will collectively enable the generations of all combinations of four binary bits. Please include the chip-level design in your report.

(2) Use function generator to produce a square wave with a frequency of f=2Hz (0V for low, 5V for high, and a 50% duty cycle), and connect it to the CP of the first D flip-flop.

(3) Connect $\overline{S}_D$ and $\overline{R}_D$ to V_{cc} for the four D flip-flops.

(4) Use a logic analyzer to observe the 2Hz square wave input at the CP, and the four outputs: Q_0 (1Hz), Q_1 (0.5Hz), Q_2 (0.25Hz), Q_3 (0.125Hz) from the four D flip-flops. Verify that your circuit operates correctly.

(5) Keep this circuit for use in Experiment 2.

[DEMONSTRATION-1] Show the instructor or TA when you complete Step 4.
[IN REPORT] Include all your design and test results.

3.2 Experiment 2: Counter Shown in 7-Segment Display

(1) The 4-channel outputs Q_3 Q_2 Q_1 Q_0 can be regarded as BCD codes, ranging from 1111 to 0000 and back to 1111. Connect these outputs to the 74HC47 by wiring Q_3 Q_2 Q_1 Q_0 to A_3 A_2 A_1 A_0 respectively. Then connect the 74HC47 to the 7-segment display. You should see the display flashing from 9 down to 0. Additionally, when the BCD code falls between 1010 and 1111, the 7-segment display will show other symbols.

(2) Next, modify the circuit to enable the counter to loop from 0 to 9 and back to 0. Hint: First, adjust the circuit to count up instead of down by wiring $\overline{Q}_3$ $\overline{Q}_2$ $\overline{Q}_1$ $\overline{Q}_0$ (instead of Q_3 Q_2 Q_1 Q_0) to A_3 A_2 A_1 A_0. Then, use a NAND (74HC00) gate to generate a low-level signal ($\overline{\overline{Q_3} \cdot \overline{Q_1}}$) to $\overline{S}_D$ to set the 4 D flip-flops when the state reaches 1010.

(3) When you complete this experiment, unwire the two 74HC74 chips, but keep 74HC47 and the 7-segment display, which you still need in Experiment 3.

[DEMONSTRATION-2] Show the instructor or TA when you have completed

(1) Step 1 (countdown).

(2) Step 2 (A counter looping from 0 to 9).

[IN REPORT] Include all your design and test results.

3.3 Experiment 3: Responder (抢答器)

In a competition, four players will press their responders to get the chance to answer questions. The quickest player will get his/her ID shown on the screen, while disabling the others' responders. A judge will clear the signal and reset the system for the next round. Based on a flip-flop, you can design this.

(1) Refer to the circuit diagram in Figure 7 and understand how it functions as the responder.

(2) Build the circuit with 74HC74×2 and 4002×2. Use four channels of SIM for the four players and one channel for the judge. Use four channels of LOM to observe the outputs. You should observe that the LED is off for the fastest player who turns on the switch. Verify that the circuit works correctly.

(3) Design a circuit to display the quickest player's ID on a 7-segment display. Hint: connect the 4 outputs from the circuit in Figure 7 to inputs 3, 4, 5, 6 of an 8-3 line priority encoder, as these inputs correspond to the BCD codes for numbers 1 to 4. The outputs A2, A1, A0 from the priority encoder should be connected to the 74HC47 to control the 7-Segment Display.

Inputs									Output				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	×	×	×	×	×	×	×	×	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	×	×	×	×	×	×	×	L	L	L	L	L	H
L	×	×	×	×	×	×	L	H	L	L	H	L	H
L	×	×	×	×	×	L	H	H	L	H	L	L	H
L	×	×	×	×	L	H	H	H	L	H	H	L	H
L	×	×	×	L	H	H	H	H	H	L	L	L	H
L	×	×	L	H	H	H	H	H	H	L	H	L	H
L	×	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

Notes: The 74HC47 has four inputs, so ensure that A3 is connected to 0 (GND). For the 8-3 line priority encoder, make sure to connect the unused input 7 to H (V_{cc}).

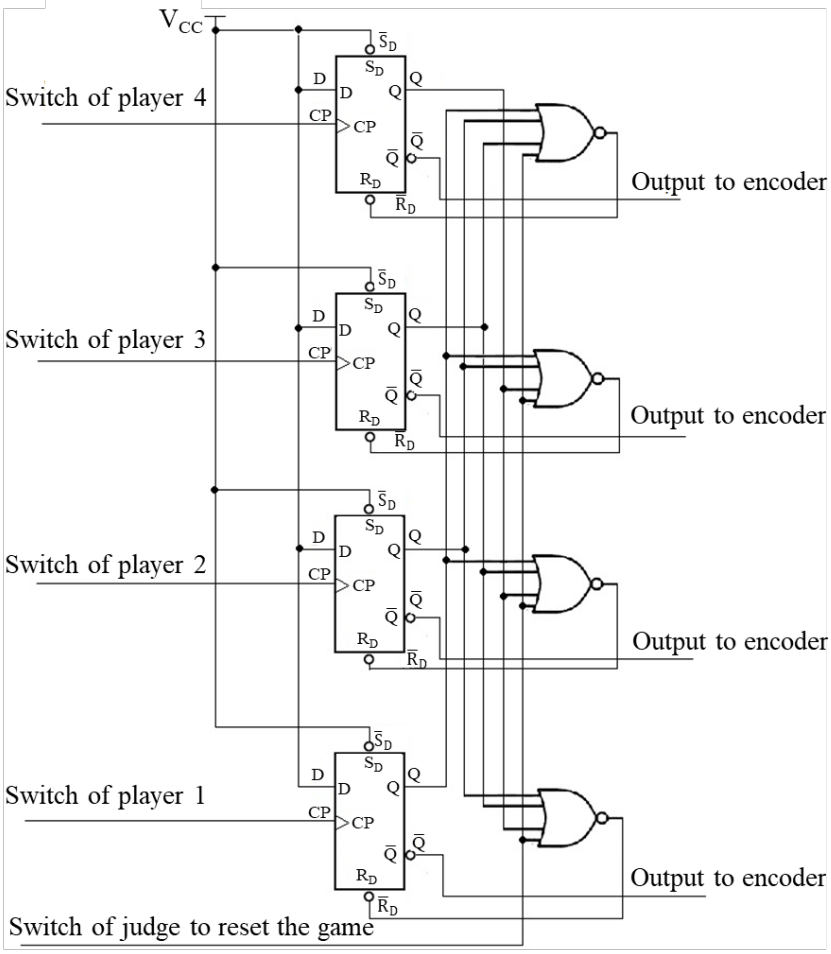

Figure 7. Circuit of the responder module.

[DEMONSTRATION-3] Show the instructor or TA when you have completed:

(1) Step 2 (LOM display).

(2) Step 3 (7-segment display).

[IN REPORT] Include all your design and test results.

4. Lab Report

Write the lab report comprehensively. A template has been provided on Blackboard. You can find it in the folder named Digital Systems Design Lab/Report Template. Submit the report of Lab 5 in **PDF** to the folder **Digital Systems Design Lab/Report Submission/Lab 5** on Blackboard by the deadline below:

- ***LAB02 (Thursday session) 23:59, Saturday, November 29, 2025***
- ***LAB01 (Friday session) 23:59, Sunday, November 30, 2025***

Each day of late submission will result in a 10% deduction from the report's raw marks.

5. Appendix

IC needed for this lab:

(1) 74HC74 ×2
(2) 4002 ×2
(3) 74HC00 ×1
(4) 74HC47 ×1
(5) 74HC148 ×1
(6) 7-segment display ×1
(7) 20-channel Dupont cable ×1
(8) 330Ω resistor ×7