EIE 2810 Digital System Design Laboratory

Laboratory Report #2

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Content

Introduction

This laboratory consists of 4 experiments, they are:

- Experiment A: Using Multisim to do Simulation
- Experiment B: Individual Gate Test
- Experiment C: Using NAND Gates to Construct Other Logic Gates
- Experiment D: Combination of the Gates

1. Experiment A

1.1 Results

1.1.1 The Results of the Simulation Circuit

The sample simulation circuit was constructed in Multisim according to Figure 1, the finished simulation circuit is shown in Figure 2.

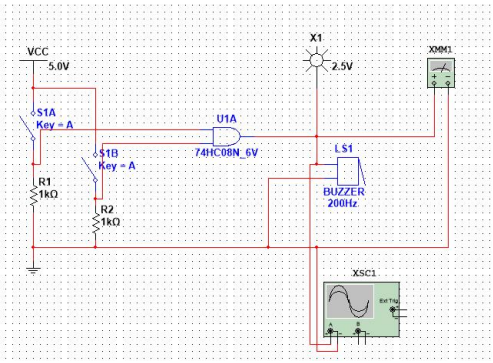

Figure 1 The Sample Simulation Circuit

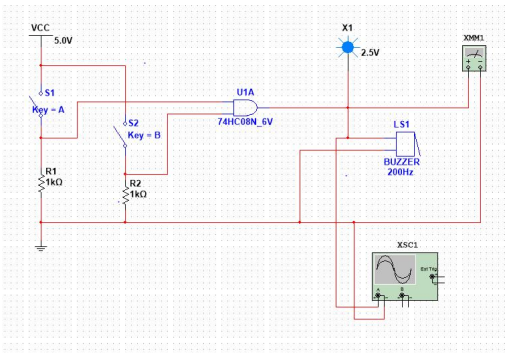

Figure 2 The Finished Simulation Circuit

1.1.2 The Results of the Simulation

The test results are shown in Figure 3.

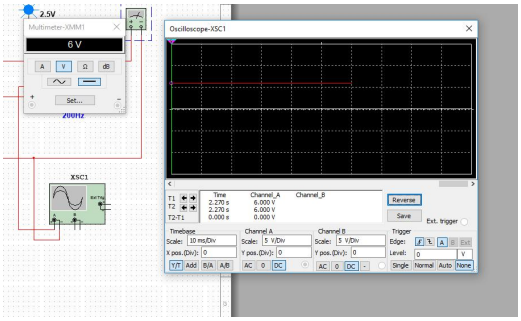

Figure 3 The Testing Results

As shown in Figure 3, when 2 switches are both closed, the multimeter shows a voltage of 6V, and the oscilloscope detects a constant 6V voltage. Theoretically, when two switches are both closed, the AND Gate is activated and will provide a high-level voltage (or logic "1") to the probe, multimeter, and oscilloscope, which goes well with the simulation experiment.

2. Experiment B

2.1 Results

2.1.1 Testing 74HC00

The IC 74HC00 is a NAND Gate chip. According to the 74HC00 datasheet, the supply voltage should be 5.0V. The truth table of the NAND Gate is shown in Table 1, and the finished circuit used to test the IC is shown in Figure 4.

Table 1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

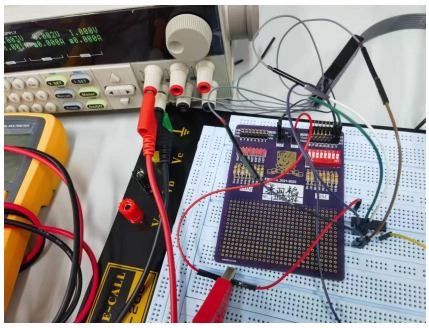

Figure 4 The Finished Circuit for Testing the NAND Gate

As shown in Figure 4, two channels of SIM are connected to Pin 1A and Pin 1B of 74HC00, and three channels of the logic analyzer are connected to Pin 1A, Pin 1B, and Pin 1Y, respectively. Pin 7 is connected to the ground and Pin 14 is connected to

V_{CC} = 5V. The logic shown by the logic analyzer is shown in Figure 5.

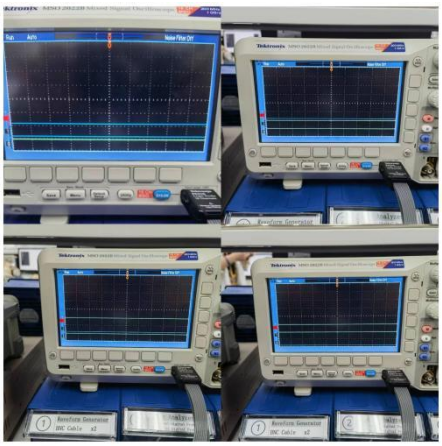

Figure 5 The Logic Condition for the 74HC00

In Figure 5, Channel 1 and Channel 2 represent Pin 1A and Pin 1B respectively, Channel 0 represents Pin 1Y. As shown in Figure 5, only when both Channel 1 and Channel 2 give high-level voltage (logic "1") will Channel 0 give low-level voltage (logic "0"). The logic shown on the logic analyzer goes well with the truth table, which means we successfully verified 74HC00's NAND Gate.

2.1.2 Testing 74HC02

The IC 74HC02 is a NOR Gate chip. According to the 74HC02 datasheet, the supply voltage should be 5.0V. The truth table of the NOR Gate is shown in Table 2, and the finished circuit used to test the IC is shown in Figure 6.

Table 2

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

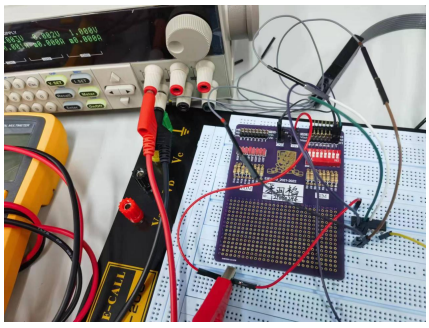

Figure 6 The Finished Circuit for Testing the NOR Gate

As shown in Figure 6, two channels of SIM are connected to Pin 1A and Pin 1B of 74HC02, and three channels of the logic analyzer are connected to Pin 1A, Pin 1B, and Pin 1Y, respectively. Pin 7 is connected to the ground and Pin 14 is connected to

V_{CC} = 5V. The logic shown by the logic analyzer is shown in Figure 7.

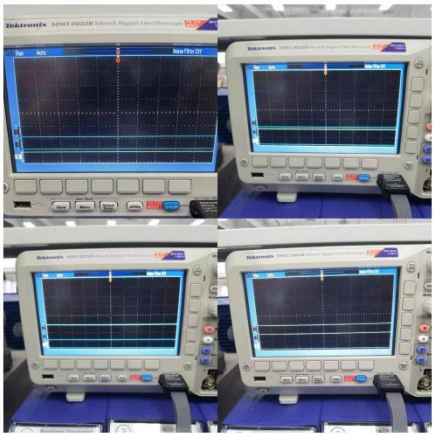

Figure 7 The Logic Condition for the 74HC02

In Figure 7, Channel 1 and Channel 2 represent Pin 1A and Pin 1B respectively, Channel 0 represents Pin 1Y. As shown in Figure 7, only when both Channel 1 and Channel 2 give low-level voltage (logic "0") will Channel 0 give high-level voltage (logic "1"). The logic shown on the logic analyzer goes well with the truth table, which means we successfully verified 74HC02's NOR Gate.

2.1.3 Testing 74HC32

The IC 74HC32 is an OR Gate chip. According to the 74HC32 datasheet, the supply voltage should be 5.0V. The truth table of the OR Gate is shown in Table 3, and the finished circuit used to test the IC is shown in Figure 8.

Table 3

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

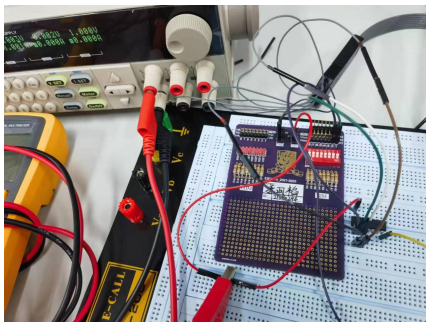

Figure 8 The Finished Circuit for Testing the OR Gate

As shown in Figure 8, two channels of SIM are connected to Pin 1A and Pin 1B of 74HC32, and three channels of the logic analyzer are connected to Pin 1A, Pin 1B, and Pin 1Y, respectively. Pin 7 is connected to the ground and Pin 14 is connected to

V_{CC} = 5V. The logic shown by the logic analyzer is shown in Figure 9.

Figure 9 The Logic Condition for the 74HC32

In Figure 9, Channel 1 and Channel 2 represent Pin 1A and Pin 1B respectively, Channel 0 represents Pin 1Y. As shown in Figure 9, only when both Channel 1 and Channel 2 give low-level voltage (logic "0") will Channel 0 give low-level voltage (logic "0"). The logic shown on the logic analyzer goes well with the truth table, which means we successfully verified 74HC32's OR Gate.

2.1.4 Testing 74HC86

The IC 74HC86 is an XOR Gate chip. According to the 74HC86 datasheet, the supply voltage should be 5.0V. The truth table of the XOR Gate is shown in Table 4, and the finished circuit used to test the IC is shown in Figure 10.

Table 4

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

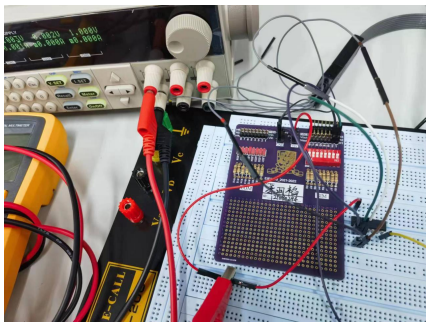

Figure 10 The Finished Circuit for Testing the XOR Gate

As shown in Figure 10, two channels of SIM are connected to Pin 1A and Pin 1B of 74HC86, and three channels of the logic analyzer are connected to Pin 1A, Pin 1B, and Pin 1Y, respectively. Pin 7 is connected to the ground and Pin 14 is connected to

V_{CC} = 5V. The logic shown by the logic analyzer is shown in Figure 11.

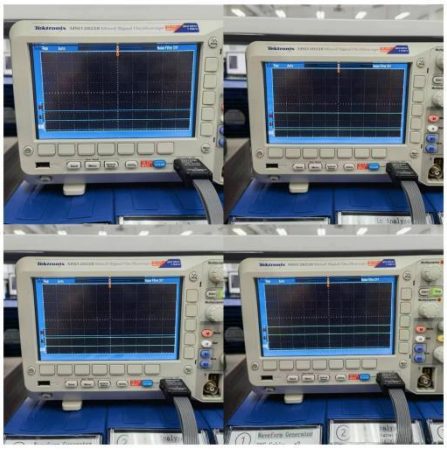

Figure 11 The Logic Condition for the 74HC86

In Figure 11, Channel 1 and Channel 2 represent Pin 1A and Pin 1B respectively, Channel 0 represents Pin 1Y. As shown in Figure 11, only when the voltage levels of Channel 1 and Channel 2 are different (one is logic "1" and another is logic "0") will Channel 0 give high-level voltage (logic "1"). The logic shown on the logic analyzer goes well with the truth table, which means we successfully verified 74HC86's XOR Gate.

2.1.5 Testing 74HC7266

The IC 74HC7266 is an XNOR Gate chip. According to the 74HC7266 datasheet, the supply voltage should be 5.0V. The truth table of the XNOR Gate is shown in Table 5, and the finished circuit used to test the IC is shown in Figure 12.

Table 5

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

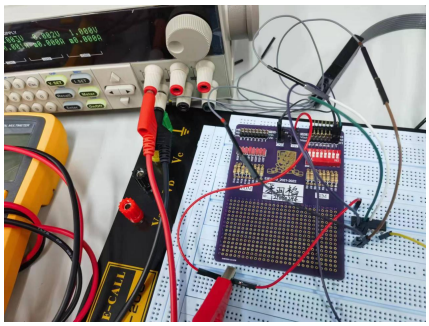

Figure 12 The Finished Circuit for Testing the XNOR Gate

As shown in Figure 12, two channels of SIM are connected to Pin 1A and Pin 1B of 74HC7266, and three channels of the logic analyzer are connected to Pin 1A, Pin 1B,

and Pin 1Y, respectively. Pin 7 is connected to the ground and Pin 14 is connected to V_{CC} = 5V. The logic shown by the logic analyzer is shown in Figure 13.

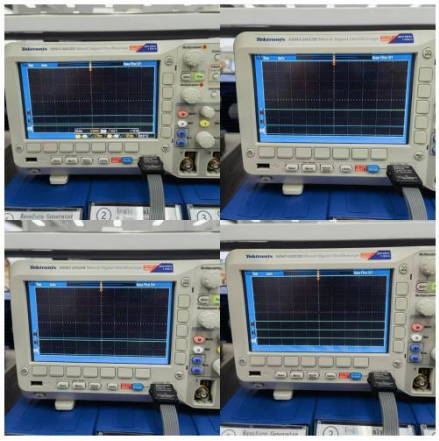

Figure 13 The Logic Condition for the 74HC7266

In Figure 13, Channel 1 and Channel 2 represent Pin 1A and Pin 1B respectively, Channel 0 represents Pin 1Y. As shown in Figure 13, only when the voltage levels of Channel 1 and Channel 2 are different (one is logic "1" and another is logic "0") will Channel 0 give low-level voltage (logic "0"). The logic shown on the logic analyzer goes well with the truth table, which means we successfully verified 74HC7266's XNOR Gate.

3. Experiment C

3.1 Design

3.1.1 Building AND Gate With Only 74HC00 (NAND Gate)

$$AB = \overline{\overline{AB}} = \overline{\overline{AB}\,\overline{AB}}$$

According to the equation above, the designed circuit diagram AND Gate built only with NAND Gate is shown in Figure 14.

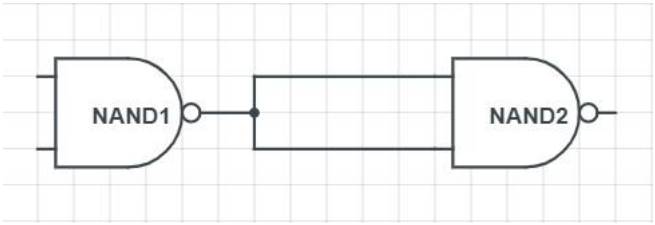

Figure 14 Building AND Gate With Only NAND Gates

3.1.2 Building OR Gate With Only 74HC00 (NAND Gate)

$$A + B = \overline{\overline{A + B}} = \overline{\overline{A}\,\overline{B}} = \overline{\overline{AA}\,\overline{BB}}$$

The designed circuit diagram OR Gate built only with NAND Gate is shown in Figure 15.

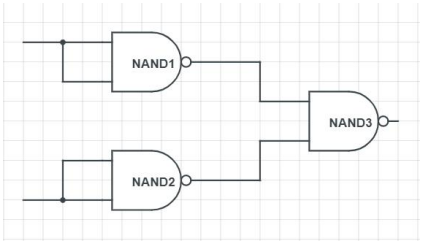

Figure 15 Building OR Gate With Only NAND Gates

3.1.3 Building NOT Gate With Only 74HC00 (NAND Gate)

$$\overline{A} = \overline{A \cdot 1}$$

According to the equation above, the designed circuit diagram NOT Gate built only with NAND Gate is shown in Figure 16.

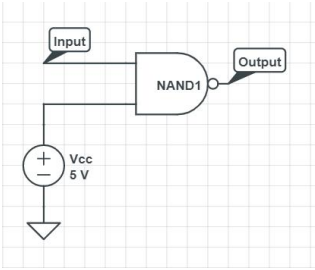

Figure 16 Building NOT Gate With Only NAND Gates

Or we can build a NOT Gate using the equation:

$$\overline{A} = \overline{AA}$$

Then the circuit design would be:

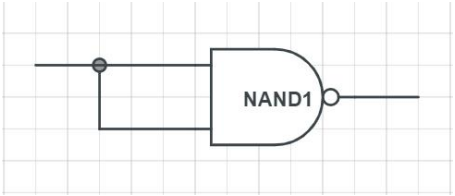

Figure 16.1 Another Way of Building NOT Gate With Only NAND Gate

3.1.4 Building NOR Gate With Only 74HC00 (NAND Gate)

$$\overline{A+B} = \overline{\overline{A+B}} = \overline{\overline{A}\,\overline{B}} = \overline{\overline{AA}\,\overline{BB}}$$

According to the equation above, the designed circuit diagram NOR Gate built only with NAND Gate is shown in Figure 17.

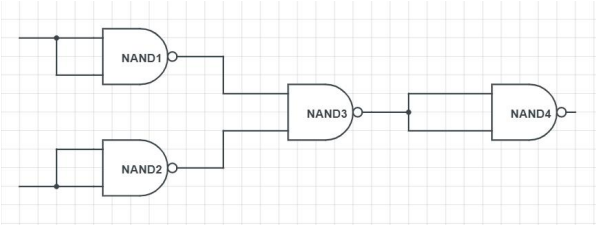

Figure 17 Building NOR Gate With Only NAND Gates

3.1.5 Building XOR Gate With Only 74HC00 (NAND Gate)

$$\overline{A}B + A\overline{B} = \overline{\overline{\overline{A}B}\,\overline{A\overline{B}}} = \overline{\overline{(A\overline{A} + \overline{B}A)}\,\overline{(B\overline{B} + B\overline{A})}} = \overline{\overline{(A(\overline{A} + \overline{B}))}\,\overline{(B(\overline{A} + \overline{B}))}}$$

$$= \overline{\overline{(A\overline{A}B)}\,\overline{(B\overline{A}B)}}$$

According to the equation above, the designed circuit diagram XOR Gate built only with NAND Gate is shown in Figure 18.

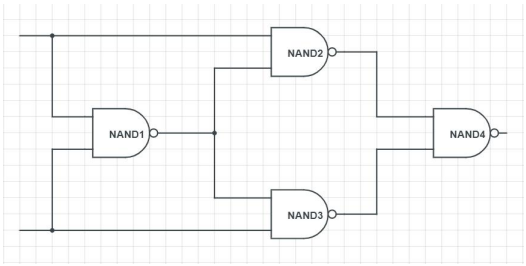

Figure 18 Building XOR Gate With Only NAND Gates

3.1.6 Building XNOR Gate With Only 74HC00 (NAND Gate)

$$\overline{\overline{A}B + A\overline{B}} = \overline{\overline{\overline{A}B}\,\overline{A\overline{B}}} = \overline{\overline{(A\overline{A} + \overline{B}A)}\,\overline{(B\overline{B} + B\overline{A})}} = \overline{\overline{(A(\overline{A} + \overline{B}))}\,\overline{(B(\overline{A} + \overline{B}))}}$$

$$= \overline{\overline{(A\overline{A}B)}\,\overline{(B\overline{A}B)}}$$

According to the equation designed above, the designed circuit diagram XNOR Gate built only with NAND Gate is shown in Figure 19.

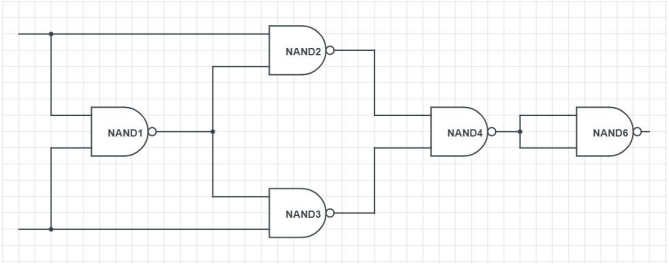

Figure 19 Building XNOR Gate With Only NAND Gates

3.2 Results

3.2.1 The Results of the Constructed AND Gate

The circuit is assembled according to Figure 14 and is shown in Figure 20. The luminous conditions for different input logic are shown in Figure 21.

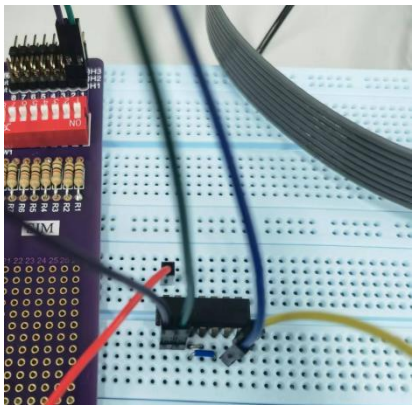

Figure 20 The Finished Circuit for the Built AND Gate

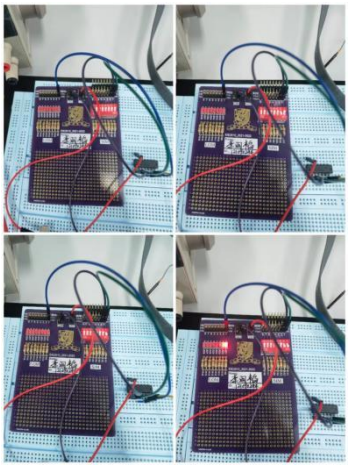

Figure 21 The Luminous Condition of LOM For Different Input Logic

As shown in Figure 21, only when both Switch 1 and Switch 2 are turned to “ON” (i.e. two input channels both give high-level voltage and logic “1”) will the LED lighten (i.e. has high-level voltage and logic “1”), which is consistent with AND Gate’s truth table. This means we successfully built an AND Gate with only NAND Gates.

3.2.2 The Results of the Constructed OR Gate

The circuit is assembled according to Figure 15 and is shown in Figure 22. The luminous conditions for different input logic are shown in Figure 23.

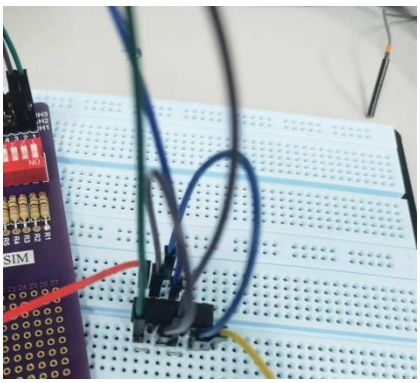

Figure 22 The Finished Circuit for the Built OR Gate

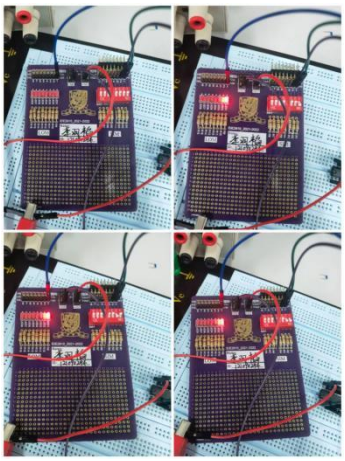

Figure 23 The Luminous Condition of LOM For Different Input Logic

As shown in Figure 23, only when both Switch 1 and Switch 2 are turned to “OFF” (i.e. two input channels both give low-level voltage and logic “0”) will the LED not lighten (i.e. has low-level voltage and logic “0”), which is consistent with OR Gate’s truth table. This means we successfully built an OR Gate with only NAND Gates.

3.2.3 The Results of the Constructed NOT Gate

The circuit is assembled according to Figure 16 and is shown in Figure 24. The luminous conditions for different input logic are shown in Figure 25.

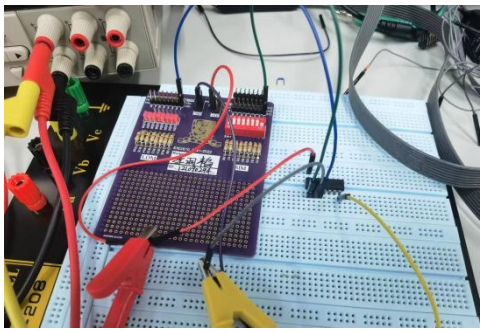

Figure 24 The Finished Circuit for the Built NOT Gate

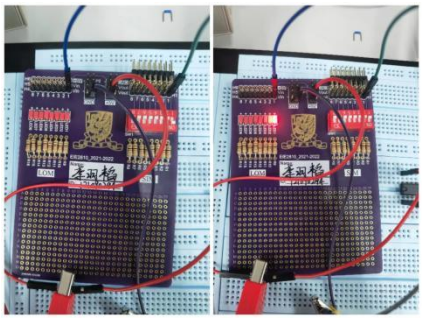

Figure 25 The Luminous Condition of LOM For Different Input Logic

As shown in Figure 25, when the switch is turned to “ON” (i.e. high-level voltage or logic “1”), the LED is not lightened (i.e. low-level voltage or logic “0”), when the switch is turned to “OFF” (i.e. low-level voltage or logic “0”), the LED is lightened (i.e. high-level voltage or logic “1”), which is consistent with the NOT Gate truth table. This means we successfully built a NOT Gate with only NAND Gates.

3.2.4 The Results of the Constructed NOR Gate

The circuit is assembled according to Figure 17 and is shown in Figure 26. The luminous conditions for different input logic are shown in Figure 27.

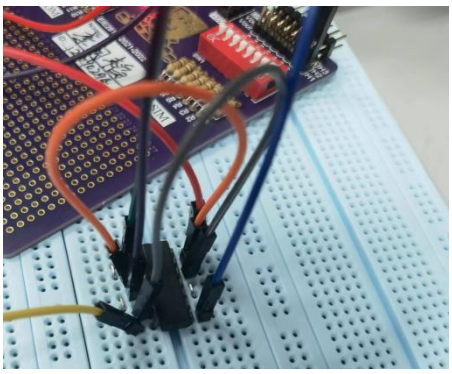

Figure 26 The Finished Circuit for the Built XOR Gate

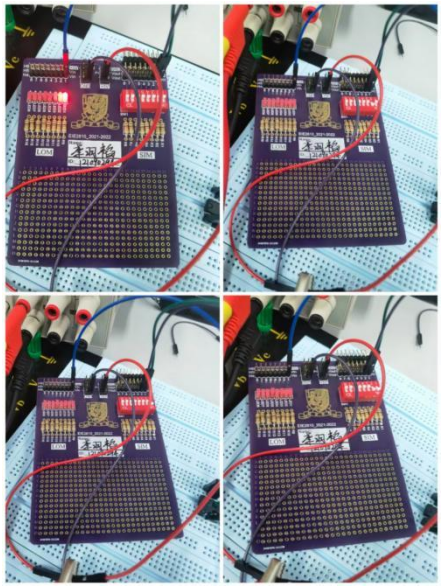

Figure 27 The Luminous Condition of LOM For Different Input Logic

As shown in Figure 27, only when both Switch 1 and Switch 2 are turned to “OFF” (i.e. two input channels both give low-level voltage and logic “0”) will the LED lighten (i.e. has high-level voltage and logic “1”), which is consistent with NOR Gate’s truth table. This means we successfully built a NOR Gate with only NAND Gates.

3.2.5 The Results of the Constructed XOR Gate

The circuit is assembled according to Figure 18 and is shown in Figure 28. The luminous conditions for different input logic are shown in Figure 29.

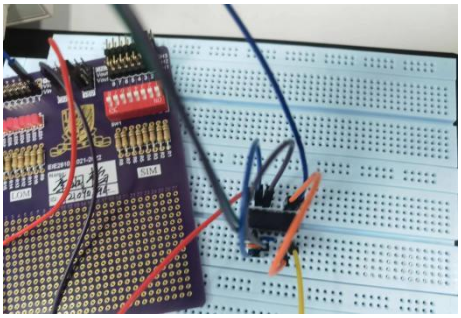

Figure 28 The Finished Circuit for the Built XOR Gate

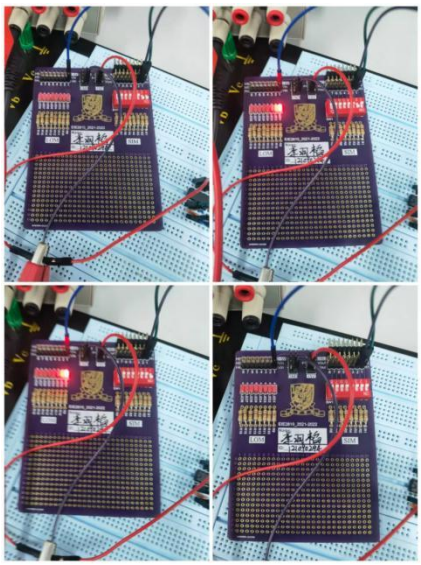

Figure 29 The Luminous Condition of LOM For Different Input Logic

As shown in Figure 29, only when both Switch 1 and Switch 2 are giving the same level of voltage will the LED not be lightened (i.e. has low-level voltage and logic "0"), which is consistent with XOR Gate's truth table. This means we successfully built an XOR Gate with only NAND Gates.

3.2.6 The Results of the Constructed XNOR Gate

The circuit is assembled according to Figure 19 and is shown in Figure 30. The luminous conditions for different input logic are shown in Figure 31.

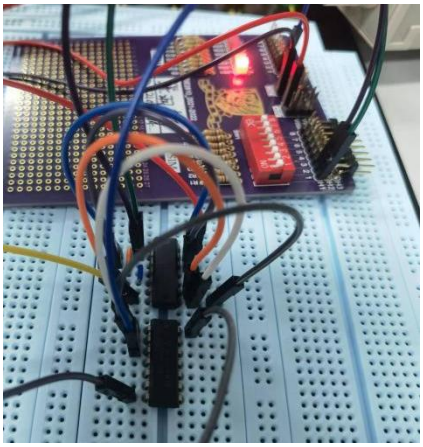

Figure 30 The Finished Circuit for the Built XNOR Gate

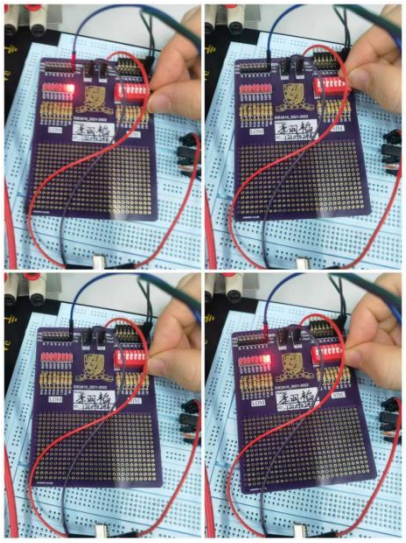

Figure 31 The Luminous Condition of LOM For Different Input Logic

As shown in Figure 31, only when both Switch 1 and Switch 2 are giving the same level of voltage will the LED be lightened (i.e. has high-level voltage and logic “1”), which is consistent with XNOR Gate’s truth table. This means we successfully built an XNOR Gate with only NAND Gates.

4. Experiment C

4.1 Results

4.1.1 The Results of the Relationship Between Y and A, B, C

The circuit diagram built in Multisim is shown in Figure 32.

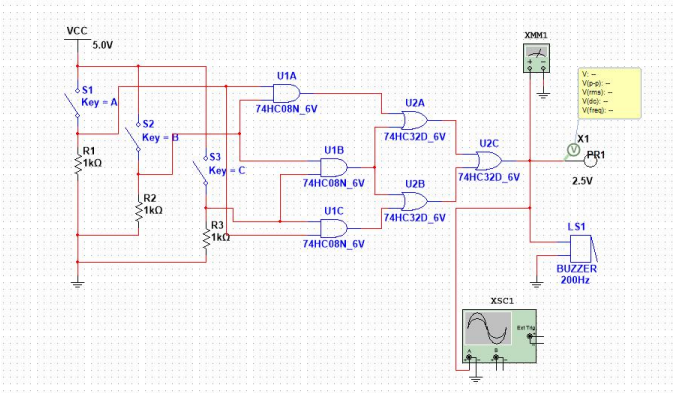

Figure 32 The Circuit Diagram Built in Multisim

As shown in Figure 32, note the output of U1A to be D, the output of U1B to be E, and the output of U1C to be F. Then D = AB, E = BC, and F = AC. Note the output of U2A to be G, and the output of U2B to be H. Then G = AB + BC, and H = BC + AC. Having G and H, we can obtain Y = G + H = AB + BC + BC + AC = AB + BC + AC. The truth table for this system is shown in Table 6

Table 6

A	B	C	Y
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
1	1	0	1
1	0	1	1
0	1	1	1
1	1	1	1

4.1.2 The Results of the Simulation

Some of the results of the simulation are shown in Figure 33

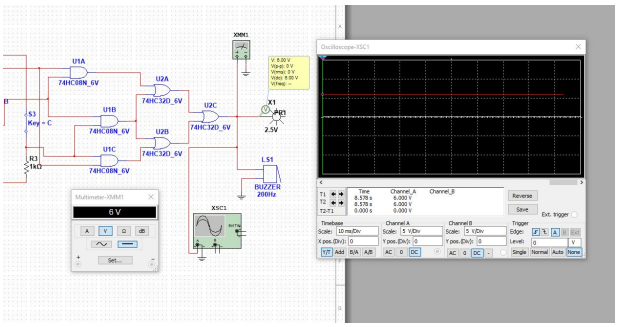

Figure 33 Part of the Simulation Results

As shown in Figure 33, when at least two of the three switches are turned to “ON” (i.e. giving high-level voltage and logic “1”), the probe would be lightened, and the multimeter and oscilloscope would show a 6.0V voltage. When at least two of the three switches are turned to “OFF” (i.e. giving low-level voltage and logic “0”), the probe would not be lightened, and the multimeter and oscilloscope would show a 0V voltage.

4.1.3 The Results of the Finished Circuit

The circuit diagram with IC pins is shown in Figure 34.

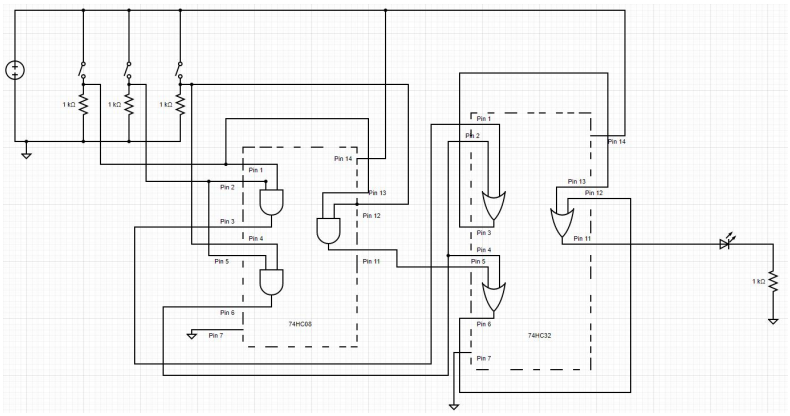

Figure 34 The Circuit Diagram With IC Pins

As shown in Figure 34, for the IC 74HC08 (AND Gate), Pin $14_{(08)}$ is connected to the support voltage V_{CC}, Pin $7_{(08)}$ is connected to the ground, Pin $1_{(08)}$ and Pin $13_{(08)}$ are connected and they are connected to Channel 1 of the SIM, then Signal A can be transmitted to AND Gate 1 and AND Gate 3; Pin $2_{(08)}$ and Pin $4_{(08)}$ are connected and they are connected to Channel 2 of the SIM, then Signal B can be transmitted to AND Gate 1 and AND Gate 2; Pin $5_{(08)}$ and Pin $12_{(08)}$ are connected and they are connected to Channel 3 of the SIM, then Signal C can be transmitted to AND Gate 2 and AND Gate 3. For the IC 74HC32 (OR Gate), Pin $14_{(32)}$ is connected to the support voltage V_{CC}, Pin $7_{(32)}$ is connected to the ground, Pin $1_{(32)}$ is connected to Pin $3_{(08)}$, Pin $2_{(32)}$ is connected to Pin $6_{(08)}$, Pin $3_{(32)}$ is connected to Pin $13_{(32)}$ to transmit Signal G to OR Gate 3; Pin $4_{(32)}$ is connected to Pin $6_{(08)}$, Pin $5_{(32)}$ is connected to Pin $11_{(08)}$, Pin $6_{(32)}$ is connected to Pin $12_{(32)}$ to transmit Signal H to OR Gate 3; Pin $11_{(32)}$ is connected to one channel of LOM. Pin $1_{(08)}$, Pin $2_{(08)}$, Pin $5_{(08)}$, and Pin $11_{(32)}$ are connected to 4 channels of a logic analyzer respectively.

4.1.4 The Results of the Practical Circuit

The logic shown on the logic analyzer is shown in Figure 35, and the luminous conditions for different input logic are shown in Figure 21.

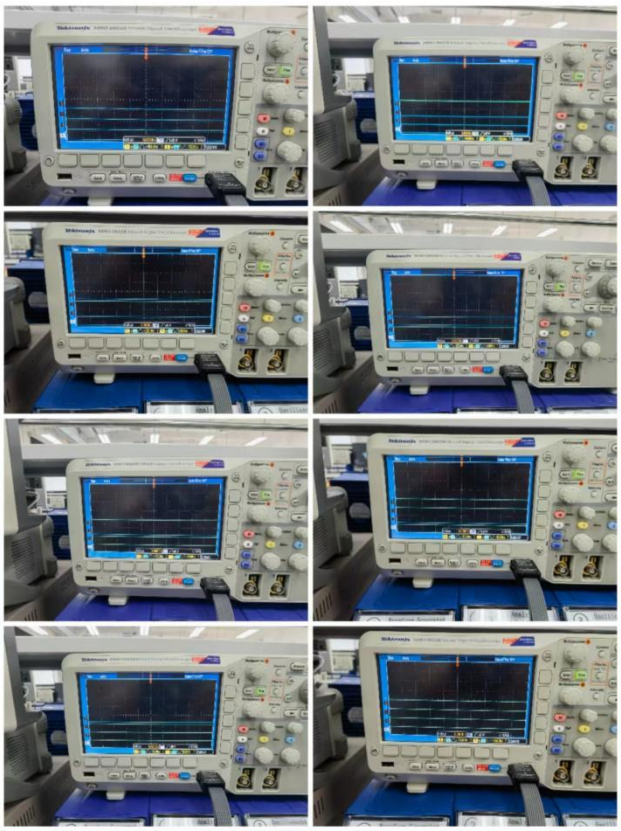

Figure 35 The Practical Logic Condition

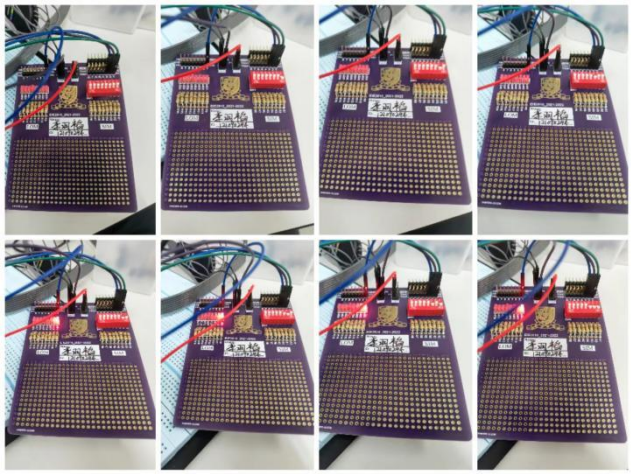

Figure 36 The Luminous Condition of LOM For Different Input Logic

As shown in Figure 35 and Figure 36, if and only if at least two of the three switches are turned to “ON” (i.e. give high-level voltage and logic “1”) will the LED be lightened (i.e. give high-level voltage and logic “1”), which goes well with Table 6. This means we successfully assembled a circuit shown in Figure 32.

4.2 Questions

Applications:

1. The nuclear button. In some countries, only when at least two of the three nuclear buttons are pressed will the nuclear missile be launched.
2. The security system. Some of the security systems need two of the three conditions satisfied to unlock.

5. Conclusion

In this lab, we learned how to use Multisim, verified the logic function of NAND Gate, NOR Gate, OR Gate, XOR Gate, and XNOR Gate, verified the functional completeness of NAND Gate, and used NAND Gates to construct AND Gate, NOT Gate, OR Gate, NOR Gate, XOR Gate, and XNOR Gate, simulated and realized a complex logic using the combination of the Gates. From the lab, we know:

1) The way to use Multisim
2) The way to construct a Gate with other kinds of Gates
3) NAND Gates have the property of functional completeness
4) The way to construct a complex logic with several kinds of Gates.