ECE2810 Digital Systems Design Laboratory

Laboratory 4

Functions of Combinational Logic, 7-Segment Display, Decoder

School of Science and Engineering

The Chinese University of Hong Kong, Shenzhen

2025-2026 Term 1

1. Objectives

In Laboratory 4, we will spend the 2-week sessions on the following:

- Learn to use a 7-segment display and BCD-to-7-segment decoder (74LS47).
- Learn to use a 4-line-to-16-line decoder (74HC154).
- Learn to build up an integrated 2-bit x 2-bit multiplier with SIM, 74HC154, 74LS47, and 7-segment indicator.

2. Introduction

2.1 7-Segment Display

7-segment displays are widely used in digital clocks, electronic meters, basic calculators, and other electronic devices that display numerical information. Figure 1 shows one typical 7-segment display. It has 1 LED for each segment and another LED for the decimal point.

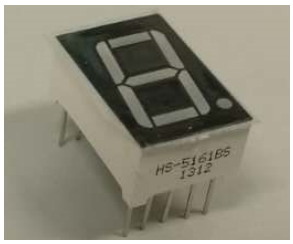

Figure 1. 7-segment display.

In a simple LED package, typically all of the cathodes (negative terminals) or all of the anodes (positive terminals) of the segment LEDs are connected and brought out to a common pin; this is referred to as a "common cathode" or "common anode" device.

In our experiment, we are using a common **anode** 7-segment display, with a circuit as shown in Figure 2. If the pin of the corresponding segment has low voltage, it is on. Otherwise, with high voltage, it is off.

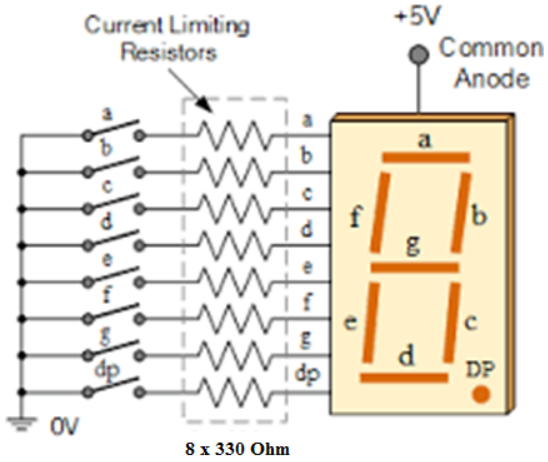

Figure 2. Pin connection with 330 Ohm resistors of a common anode 7-segment display.

To limit the current and protect the display, in normal practice, we will use a resistor (typically 330 Ohms) to connect the segment pin to the switch. The pin arrangement of the component in this experiment is illustrated in Figure 3. The 2 pins for 5V are interconnected inside the display.

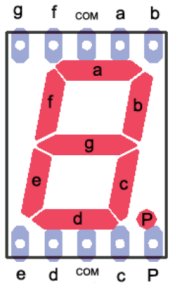

Figure 3. Pin arrangement of a 7-segment display.

2.2 BCD-to-7-Segment Decoder (74LS47)

To make it easier to control the 7 segments, a BCD-to-7-segment decoder (74LS47) can be used to change the BCD (Binary-Coded Decimal) code to the 7-segment code. Figure 4 illustrates the pin arrangement. $A_3A_2A_1A_0$ are the input BCD code from MSB (Most Significant Bit) to LSB (Least Significant Bit).

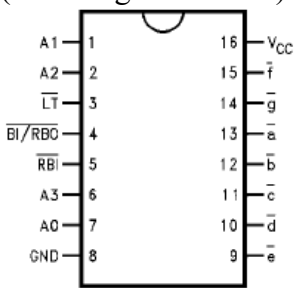

Figure 4. Pin arrangement of 74LS47.

The normal Vcc for 74LS47 is 5V in the datasheet. It is important to observe the truth table (Table 1) and understand it.

Table 1. Truth table of 74LS47.

Truth Table

Decimal or Function	Inputs							Outputs							Note
	$\overline{LT}$	$\overline{RBI}$	A3	A2	A1	A0	$\overline{BI/RBO}$	$\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	

$\overline{LT}$ is the lamp test. $\overline{RBI}$ is ripple blanking input. $\overline{BI}$/ $\overline{RBO}$ (blanking input/ripple blanking output) can work as either input or output.

- When $\overline{LT}$ and $\overline{BI}$/ $\overline{RBO}$ are both high, you will enable the 7-segment display from 0 to 14 (10-14 are indicated by another symbol). The $\bar{}$ in $\bar{a}$~$\bar{g}$ indicates that, when logic is activated, the output is "low" rather than "high". This fits appropriately with the common anode 7-segment display.
- When $\overline{LT}$ is low and $\overline{BI}$/ $\overline{RBO}$ is high, it turns on all the segments, and you can test if any segment is burnt.
- For $\overline{BI}$/ $\overline{RBO}$, it has a feature for zero suppression. We will not test that in this lab. You may refer to page 339 of the textbook named *Digital Fundamentals*.

2.3 4-Line-to-16-Line Decoder (74HC154)

74HC154 is another decoder to map a 4-digit input into one of 16 outputs. Typical Vcc=5V. The pin arrangement and logic symbol are shown in Figure 5.

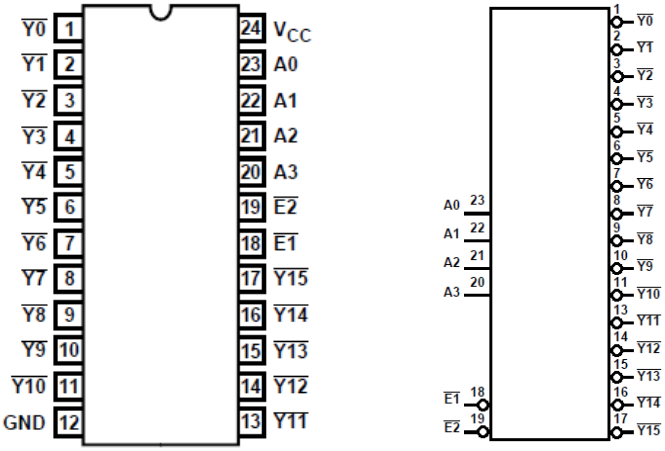

Figure 5. Pin arrangement and logic symbol of 74HC154.

Table 2. Truth table of 74HC154.

INPUTS						OUTPUTS														
$\overline{E1}$	$\overline{E2}$	A3	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
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L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

- From the truth table above (Table 2), you can observe that the chip is enabled when both $\overline{E1}$ and $\overline{E2}$ are low.
- The first 16 rows from the top indicate the 16 input–output relations. E.g., when $A_3A_2A_1A_0 = 0110$, the pin $\overline{Y6} = 0$ while all other outputs are high.

3. Experiments

3.1 Experiment 1: Use a 7-Segment Display with a BCD-to-7-Segment Decoder (74LS47)

This experiment is a hardware implementation. Design your circuit first. Use 4 channels of SIM to generate a 4-bit BCD code, input this code to 74LS47, and feed the output of 74LS47 to the 7-segment display. Verify that all the BCD codes can be displayed correctly. Do not forget to wire a 330-ohm resistor between each segment pin and the 74LS47 output pin.

After completing this stage, remove SIM components, but keep the rest of the circuit. You will need it for Experiment 3.3.

[DEMONSTRATION] Show the instructor or TA when you have completed this.
[IN REPORT] Include the chip-level circuit diagram for this experiment, along with your test results to verify successful completion.
(*Suggestion*: First, in the circuit diagram, illustrate the connections between the 74LS47 and the 7-segment display, including the required resistors, VCC, and GND. Clearly label the input for the 4-bit BCD code (A3A2A1A0). Second, take 10 photos displaying the numbers 0-9 on the 7-segment display, and the input BCD code with SIM.

3.2 Experiment 2: 2-Bit × 2-Bit Multiplier (*AGAIN*)

You have built a 2-bit × 2-bit multiplier by basic logic gates in Lab 3, where A_1A_0 x $B_1B_0 = X_3X_2X_1X_0$. This time, you are asked to re-design the circuit based on a 4-line-to-16-line decoder (74HC154) and several simple logic gates: 74HC00 x 2 (NAND gate) and 74HC32 x 1(OR gate). Though the number of chips is not reduced significantly, the design process is simplified. You will need to create a truth table, but a Karnaugh map is not required. Use SIM to control the 4 inputs, and LOM to display the 4-bit outputs.

Once you have completed this experiment, remove the LOM, but keep the rest of the circuit. You will need it in Experiment 3.3.

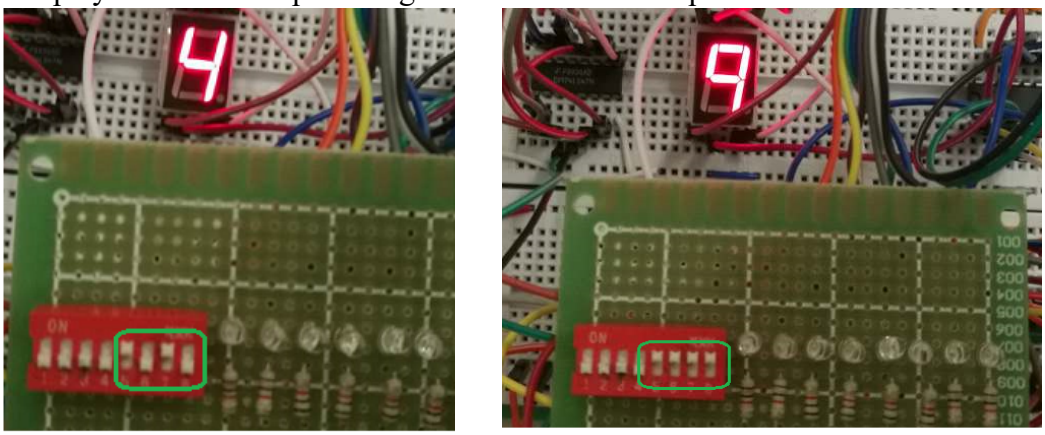
Tip: The OR operation can be expressed using NAND operations as follows:

$$A + B = \overline{\bar{A} \cdot \bar{B}}.$$

[DEMONSTRATION] Show the instructor or TA when you have completed this.
[IN REPORT] Include your design steps (Truth table, how you map the truth table to the decoder's output, how you derive the logic functional expressions for each output, the circuit diagram for wiring, etc.). Include your test result. (*Suggestion*: Show at least 6 different outputs from the multiplier.)

3.3 Experiment 3: Combine Multiplier with 7-Segment Display

In this step, you will practice implementing a multiplier that can display a number as output. Two examples are shown in Figure 6. SIM will generate four bits as input, while the display shows the output. Integrate the circuits in Experiment 3.1 and 3.2.



0b10 x 0b10 = 0b0100 = 4 **0b11 x 0b11 = 0b1001 = 9**

Figure 6. Two states in Experiment 3.4.

[DEMONSTRATION] Show the instructor or TA when you have completed this.
[IN REPORT] Include the images of your test results. (*Suggestion*: Show at least 6 different outputs from the multiplier.)

Lab Report

Write the lab report comprehensively. A template has been provided on Blackboard. You can find it in the folder named Digital Systems Design Lab/Report Template. Submit the report of Lab 4 in **PDF** to the folder **Digital Systems Design Lab/Report Submission/Lab 4** on Blackboard by the deadline below:

- ***LAB02 (Thursday session) 23:59, Saturday, November 15, 2025***
- ***LAB01 (Friday session) 23:59, Sunday, November 16, 2025***

Each day of late submission will result in 10% deduction in the report raw marks.

Appendix

IC needed for this lab:

1. 74HC00 x2
2. 74HC32 x1
3. 74LS47 x1
4. 74HC154 x1
5. 7-segment display x1
6. 330 Ohm resistor x7

Remember to sort and return items 1-6 back to the storeroom after lab.
For any malfunctioning component, report to instructor or TA, and DO NOT put it back.