EIE2810 Digital Systems Design Laboratory

Laboratory Report #1

Name: Student ID:
Date: 2024.2.2

The Chinese University of Hong Kong, Shenzhen

- Experiment A: learn to use logic analyzer
- Experiment B: roughly understand how to read datasheet
- Experiment C: build AND circuits based on diodes
- Experiment D: build AND circuits based on transistors
- Experiment E: basic experiment in AND gate 74HC08
- Experiment F: basic experiment in AND gate 74LS08
- Experiment G: basic experiment in NOT gate 74HC04

1. Experiment A

1.1 Result

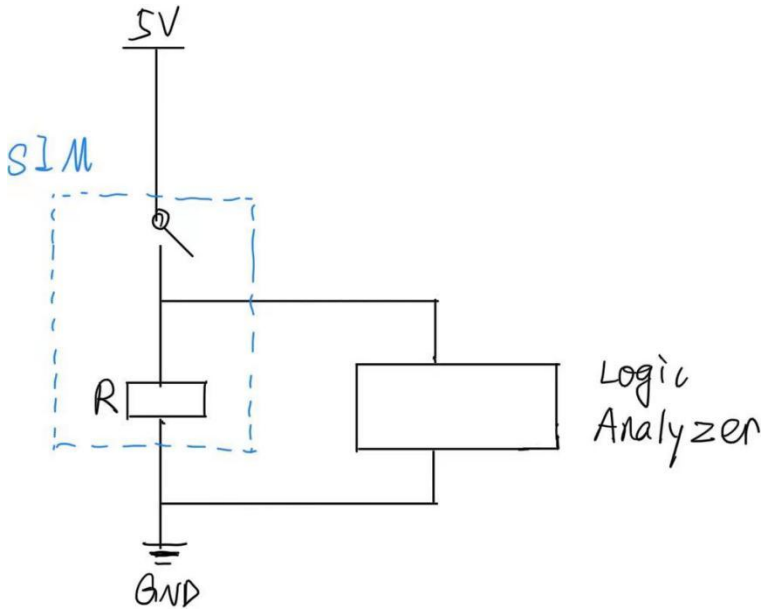


Figure 1. Circuit diagram of the connection of SIM

Figure 2. image of the 8 channel digital signals

This is the image of the logic analyzer interface when the switch in the circuit of channel 5, 6, 7 of the logic analyzer is on.

2. Experiment B

2.1 Result

74LS08

- Supply voltage (Vcc):

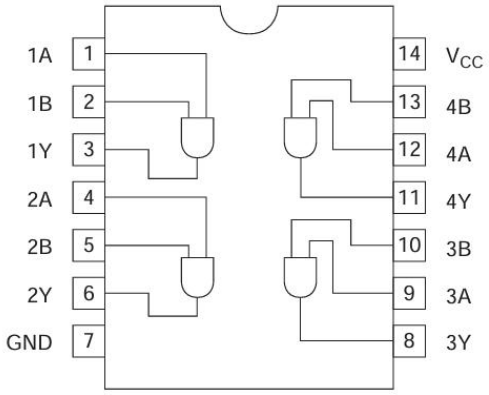
Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V

- Input Voltage, Output Voltage:

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V_{IH}	2.0	—	—	V		
	V_{IL}	—	—	0.8	V		
Output voltage	V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, I_{OH} = –400 μA	
	V_{OL}	—	—	0.5	V	I_{OL} = 8 mA	V_{CC} = 4.75 V, V_{IL} = 0.8 V
		—	—	0.4		I_{OL} = 4 mA	

- Pin arrangement:



(Top view)

1. Pin 1 (1A): The first input pin for the first AND gate. Connect the first input signal for the first AND gate to this pin.

2. Pin 2 (1B): The second input pin for the first AND gate. Connect the second input signal for the first AND gate to this pin.

3. Pin 3 (1Y): The output of the first AND gate. The result of the AND operation on the input signals at pins 1 and 2 will appear at this output pin.

4. Pin 4 (2A): The first input pin for the second AND gate. Connect the first input signal for the second AND gate to this pin.

5. Pin 5 (2B): The second input pin for the second AND gate. Connect the second input signal for the second AND gate to this pin.

6. Pin 6 (2Y): The output pin of the second AND gate. The result of the AND operation on the input signals at pins 4 and 5 will appear at this output pin.

7. Pin 7 (GND): The ground pin. Connect it to the ground reference.

8. Pin8 (3Y): The output pin of the third AND gate. The result of the AND operation on the input signals at pins 9 and 10 will appear at this output pin.

9. Pin 9 (3A): The first input pin for the third AND gate. Connect the first input signal for the third AND gate to this pin.

10. Pin10 (3B): The second input pin for the third AND gate. Connect the second input signal for the third AND gate to this pin.

11. Pin11 (4Y): The output pin of the fourth AND gate. The result of the AND operation on the input signals at pins 12 and 13 will appear at this output pin.

12. Pin 12 (4A): The first input pin for the fourth AND gate. Connect the first input

signal for the fourth AND gate to this pin.

13. Pin13 (4B): The second input pin for the fourth AND gate. Connect the second input signal for the fourth AND gate to this pin.

14. Pin 14 (VCC): The supply voltage pin. Connect it to the positive power supply voltage.

74HC08:

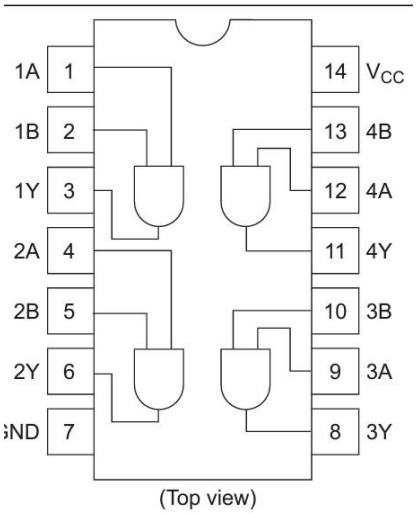
- Supply voltage (Vcc):

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	

- Input Voltage, Output Voltage:

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 5.2 mA

- Pin arrangement:



(Top view)

1. Pin 1 (1A): The first input pin for the first AND gate. Connect the first input signal for the first AND gate to this pin.

2. Pin 2 (1B): The second input pin for the first AND gate. Connect the second input signal for the first AND gate to this pin.

3. Pin 3 (1Y): The output of the first AND gate. The result of the AND operation on the input signals at pins 1 and 2 will appear at this output pin.

4. Pin 4 (2A): The first input pin for the second AND gate. Connect the first input signal for the second AND gate to this pin.

5. Pin 5 (2B): The second input pin for the second AND gate. Connect the second input signal for the second AND gate to this pin.

6. Pin 6 (2Y): The output pin of the second AND gate. The result of the AND operation on the input signals at pins 4 and 5 will appear at this output pin.

7. Pin 7 (GND): The ground pin. Connect it to the ground reference.

8. Pin8 (3Y): The output pin of the third AND gate. The result of the AND operation on the input signals at pins 9 and 10 will appear at this output pin.

9. Pin 9 (3A): The first input pin for the third AND gate. Connect the first input signal for the third AND gate to this pin.

10. Pin10 (3B): The second input pin for the third AND gate. Connect the second input signal for the third AND gate to this pin.

11. Pin11 (4Y): The output pin of the fourth AND gate. The result of the AND operation on the input signals at pins 12 and 13 will appear at this output pin.

12. Pin 12 (4A): The first input pin for the fourth AND gate. Connect the first input signal for the fourth AND gate to this pin.

13. Pin13 (4B): The second input pin for the fourth AND gate. Connect the second input

2.2 Conclusion

In this experiment, I learned how to check the data of gates in the datasheet. The property of gates may vary under different environment (temperature, Vcc, V_{in}, I_{in} and etc.)

3. Experiment C

3.1 Result

	A (V)	B (V)	V_0 (V)
(0,0)	1.451	1.451	2.073
(0,1)	2.166	4.98	2.808
(1,0)	4.98	2.166	2.808
(1,1)	4.98	4.98	4.98

Table 3. Signal Measured for AND Based on Diodes

Discussion in Q2.

3.2 Questions

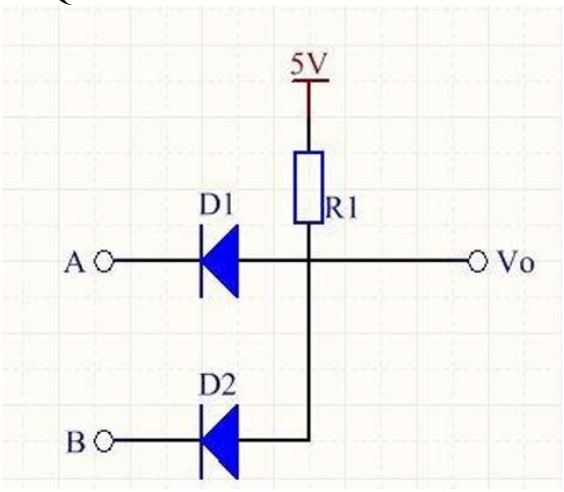


Figure 3. Circuit diagram of AND logic circuit by diodes

Q1. Explain how the circuit above realize AND logic.

When both A and B are HIGH (near +5V), there is no current through D1 and D2. As a result, V_0 = Vcc = 5V. The output will be HIGH, representing a logical '1'.
When either A or B is LOW, the corresponding diode is forward-biased and there is current go through it. V_0 equals to the voltage value at the anode of this diode, which equals to the voltage level at cathode plus the forward voltage drop (usually 0.7V). As a result, the output will be LOW, representing a logical '0'.
When both A and B are LOW, D1 and D2 are both forward-biased and there are current go through them. The voltage value at the anode of the two diode are approximately same, so V_0 equals to the voltage value at the anode of one diode, which equals to the voltage level at cathode plus the forward voltage drop (usually 0.7V). As a result, the output will be LOW, representing a logical '0'.
In summary, this circuit implements the AND logic operation. The output is HIGH only when both inputs A and B are HIGH; otherwise, the output is LOW. This behavior is consistent with the truth table of an AND gate.

Q2. Explain the voltage observed.
a. When both A and B are LOW (row1), D1 and D2 are both forward-biased. R1, R2 and R3 are all 1kΩ. The resistance of D1 can be ignored compared to R1 and R2. R2 and R3 are parallel, and they are in series with R1. The voltage measured at A (V_A) is the voltage drop of the resistance inside SIM (R2). The voltage measured at B (V_B) is the voltage drop of the resistance inside SIM (R3). V_0 measures the potential difference of R2+D1 (R3+D2). In general, a diode has a voltage drop of 0.7V
Ideally, $V_A = V_B \approx \frac{5}{R1+0.5R2} * \frac{R2}{2} \approx 1.67V$, $V_0 \approx \frac{5}{R1+0.5R2} * \frac{R2}{2} + 0.7 \approx 2.37V$.
The measured V_A and V_B is1.451V, V_0 is 2.073V, all a bit smaller than the ideal values. The error may due to the actual resistance of diode. If count the resistance of diode,
$V_A' = V_B' \approx \frac{5}{R1+0.5(R2+D1)} * \frac{R2}{2}$, $V_0 \approx \frac{5}{R1+0.5(R2+D1)} * \frac{R2+D1}{2} + 0.7$. V_A', V_B' and V_0' would be smaller than V_A, V_B and V_0. The measured data comply with this.
The circuit is shown below.

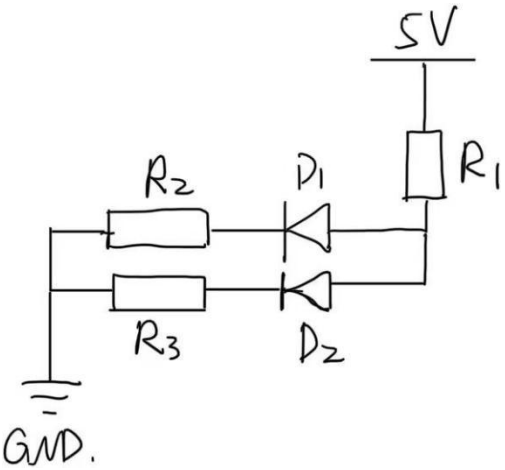


Figure 5. Circuit diagram when both input are LOW

b. When one of A and B is HIGH (row2 and row3), consider the case when A is LOW. R1, R2 are both 1kΩ, and they are in series. The resistance of D1 can be ignored compared to R1 and R2. The voltage measured at A (V_A) is the voltage drop of R2. The voltage measured at B (V_0) is the voltage drop of R2+D1.
Ideally, $V_A \approx \frac{5}{R1+R2} * R2 \approx 2.5V$, $V_0 \approx \frac{5}{R1+R2} * R2 + 0.7 \approx 3.2V$
The measured V_A is 2.166V, V_0 is 2.808V, both a bit smaller than the ideal values. Similarly, the error may due to the actual resistance of diode. If count the resistance of diode, $V_A' = \frac{5}{R1+R2+D1} * R2$, $V_0' = \frac{5}{R1+R2+D1} * R2 + 0.7$. V_A' and V_0' would be

smaller than V_A and V_0. The measured data comply with this.
For V_B, D2 is disconnected, and B is connected to Vcc, so V_B = 5V.
The circuit is shown below.

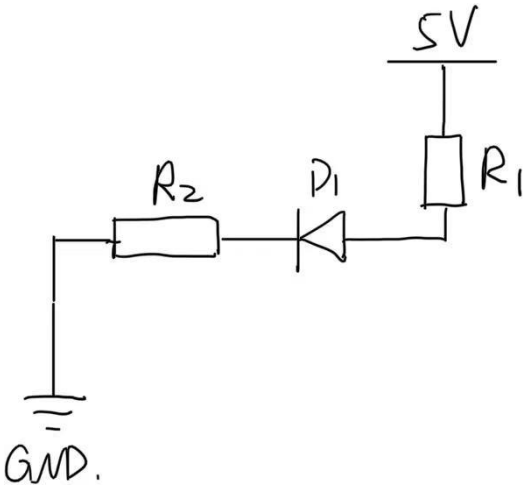


Figure 6. Circuit diagram when one input is LOW

c. When both A and B are HIGH (row4), because both D1 and D2 are disconnected, V_0 = Vcc = 5V. Because both A and B are connected to 5V power supply, so V_A=V_B= 5V.

3.3 Conclusion
In this experiment, I learned that the resistance of diodes can not be ignored directly in practical.

4. Experiment D

4.1 Result

	A (V)	B (V)	V_0 (V)
(0,0)	0	0	0
(0,1)	0.001	4.98	0.132
(1,0)	4.98	0	0
(1,1)	4.98	4.98	3.93

Table 4. Signal Measured for AND Based on Transistors

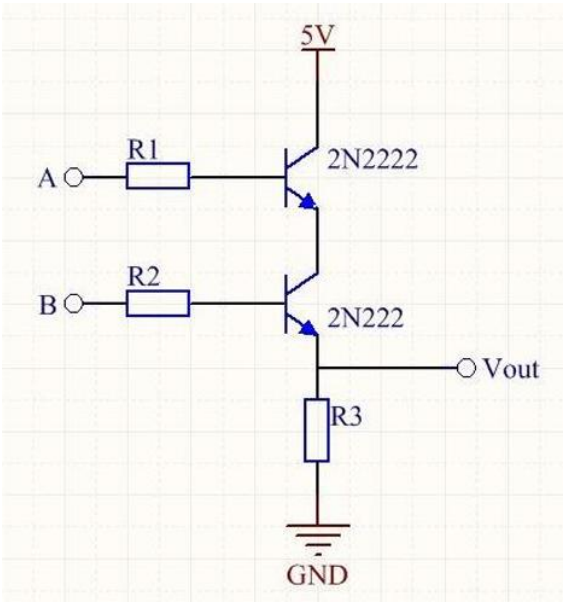


Figure 7. Circuit diagram of AND logic circuit by transistors

Similarly to Experiment C, this circuit implements the AND logic operation. The output is HIGH only when both inputs A and B are HIGH; otherwise, the output is LOW. This

behavior is consistent with the truth table of an AND gate.

5. Experiment E

5.1 Result

- Input-output logic

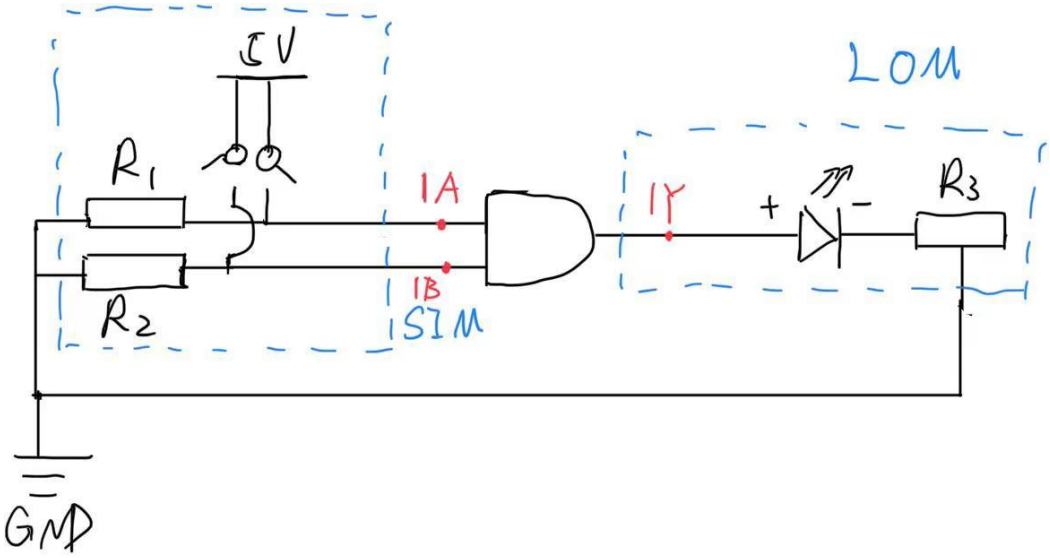


Figure 8. Gate level circuit diagram of CMOS AND gate

	1A (V)	1B (V)	1Y (V)
(0,0)	0	0	0
(0,1)	0.001	4.98	0
(1,0)	4.98	0.001	0
(1,1)	4.98	4.98	4.23

Table 5. IO for CMOS AND Gate

As shown above, output 1Y is HIGH only when both inputs 1A and 1B are HIGH; otherwise, the output is LOW. This behavior is consistent with the truth table of an AND gate.

- Measure VTC

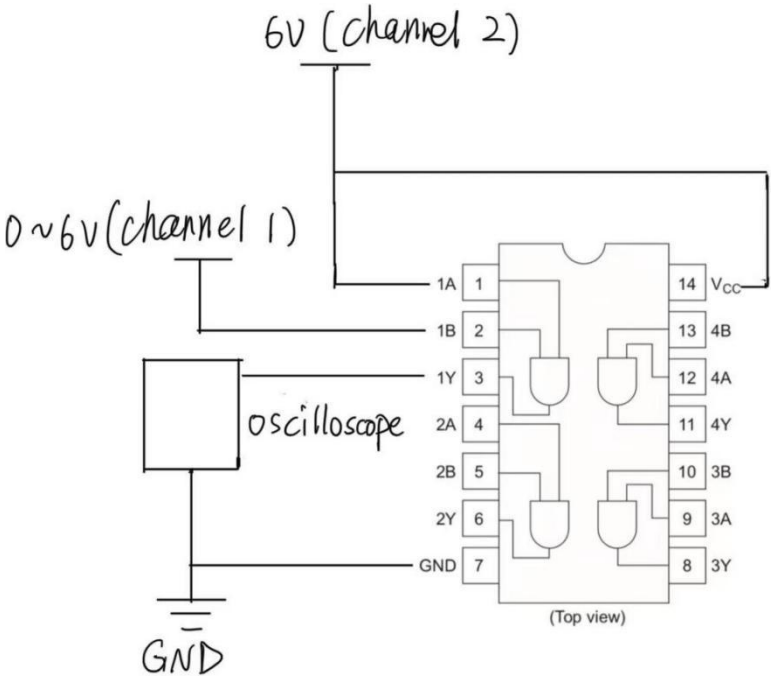


Figure 9. Chip level circuit diagram of VTC

Rough 1B	0.0	1.0	1.9	2.1	2.3	2.5	2.7	2.8	2.9
Measured 1B	0.002	0.994	1.893	2.093	2.293	2.492	2.690	2.790	2.892
Measures 1Y	0.001	0.001	0.001	0.001	0.001	0.001	2.858	2.955	2.937
Rough 1B	3.0	3.1	3.2	3.3	3.4	3.6	4.0	5.0	6.0
Measured 1B	2.994	3.092	3.187	3.286	3.385	3.585	3.984	4.98	5.97
Measured 1Y	2.952	3.050	3.302	3.114	3.192	5.98	5.98	5.98	5.98

Table 6. VTC Data

* The highlighted data are unstable.

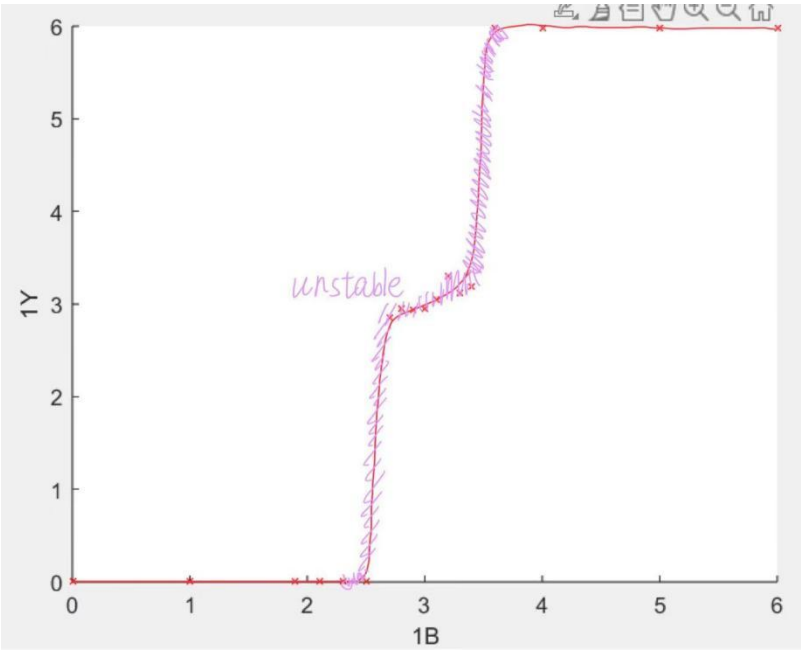


Figure 10. VTC diagram

The datasheet suggests that input value below 1.8V is counted as “LOW”, above 4.2V is counted as “HIGH”. Any other input leads to undefined (unstable) behavior.
In my experiment, the unstable 1Y happens when 1B is connected to 2.3V-3.6V voltage. The difference may due to:
1. Component variability: There can be variations in the characteristics of electronic components even within the same batch.
2. Fluctuations in power supply voltage.

For the output voltage, when 1B is smaller than 1.8V, the output 1Y is 0.001V, which is smaller than the minimum V_{OL} in the datasheet, so this is low-level output. When 1B is larger than 4.2V, the output 1Y is 5.98V, which is larger than the maximum V_{OH} in the datasheet, so this is high-level output. When the input voltage of 1B is (undefined) in the range of unstable area, the measured 1Y is not reliable.
This result complies with the property of AND gate.

5.2 Conclusion

In this experiment, I learned that when the input is undefined, the output can be LOW or HIGH or unstable, which is not reliable.

- CMOS voltage levels

Figure 11. Wave image for initial state (CMOS)

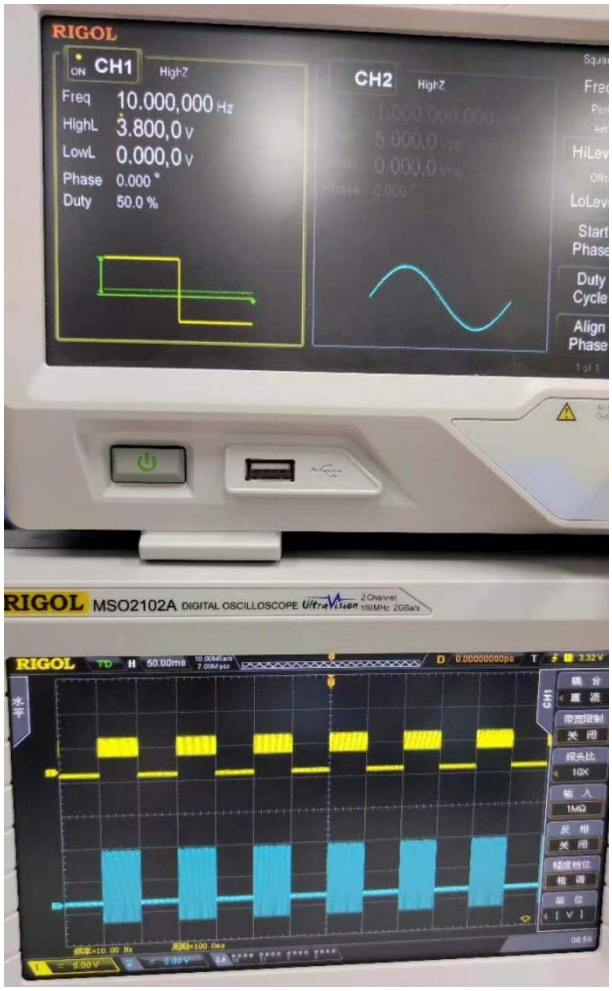


Figure 12. Wave image for unstable 1Y (CMOS)

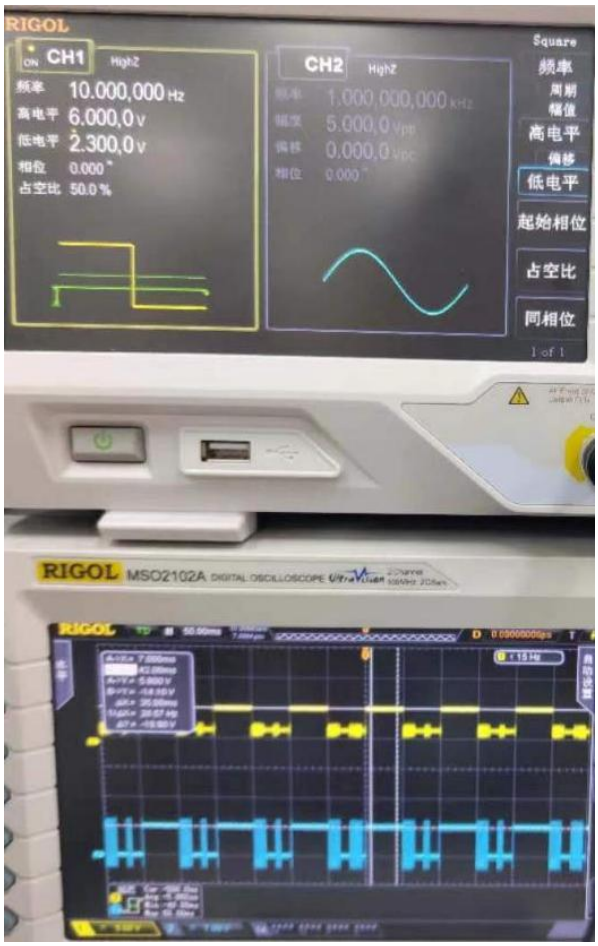


Figure 13. Wave image for unstable 1Y (CMOS)

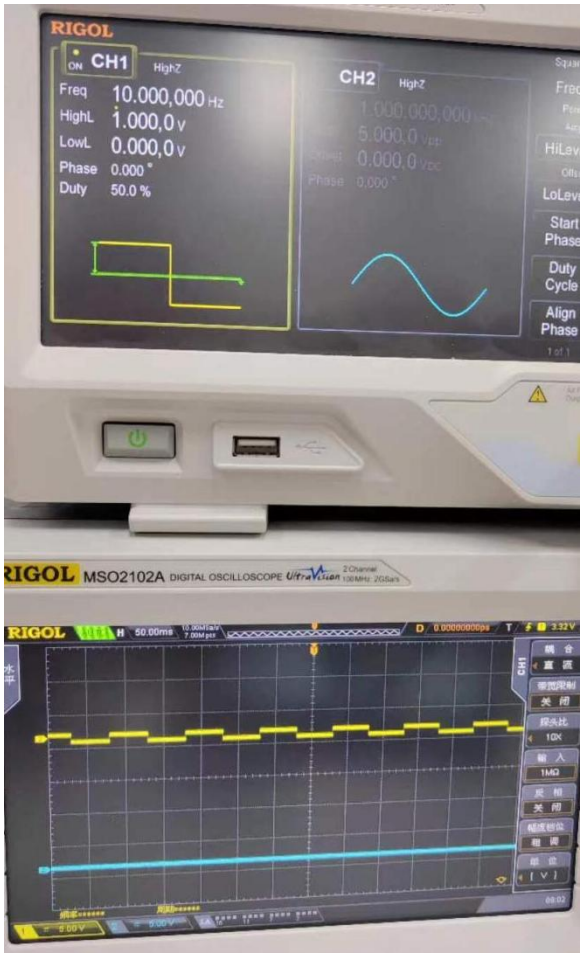


Figure 14. Wave image for LOW in 1Y (CMOS)

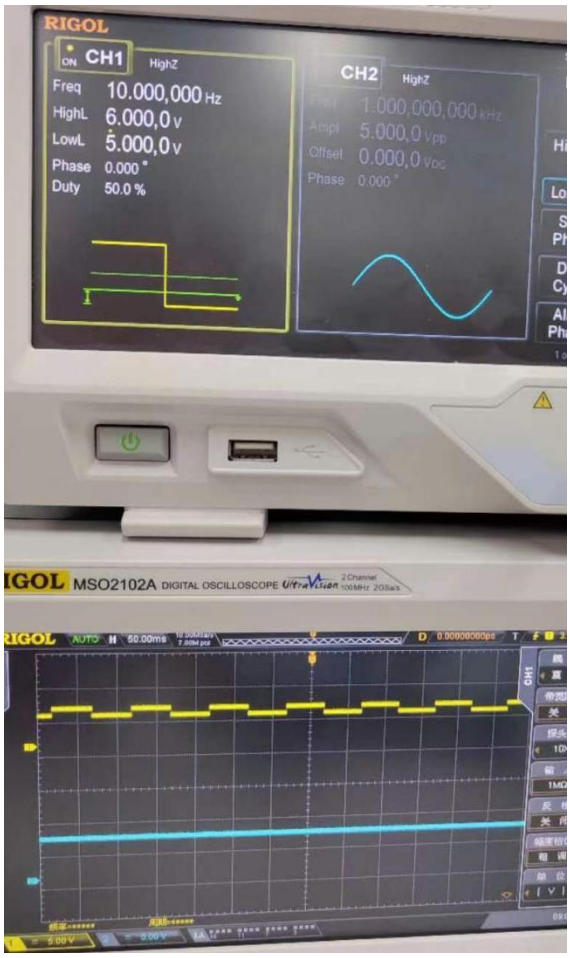


Figure 15. Wave image for HIGH in 1Y (CMOS)

The datasheet suggests that input value below 1.8V is counted as LOW, above 4.2V is counted as HIGH. Any other input leads to undefined (unstable) behavior.
In my experiment, when the level of low voltage in 1B remained 0V, and the level of high voltage in 1B was decreased to 3.8V, the output 1Y became unstable. When the level of high voltage in 1B remained 6V, and the level of low voltage in 1B was increased to 2.3V, the output 1Y became unstable. Because 2.3V is larger than 1.8V, 3.8V is smaller than 4.2V, so this result generally complies with the datasheet.
However, there exist some error between the experimental data and datasheet, as the boundary 3.8V and 2.3V measured in the experiment are a bit away from the suggested boundary 1.8V and 4.2V. This may due to the slight differences in IC manufacturing, temperature, fluctuations in power supply voltage, etc.

6. Experiment F

6.1 Result

- Input-output logic

	1A (V)	1B (V)	1Y (V)
(0,0)	0	0	0
(0,1)	0.001	4.98	0
(1,0)	4.98	0.001	0
(1,1)	4.98	4.98	3.51

Table 7. IO for TTL AND Gate

As shown above, output 1Y is HIGH only when both inputs 1A and 1B are HIGH; otherwise, the output is LOW. This behavior is consistent with the truth table of an AND gate.

- TTL voltage levels

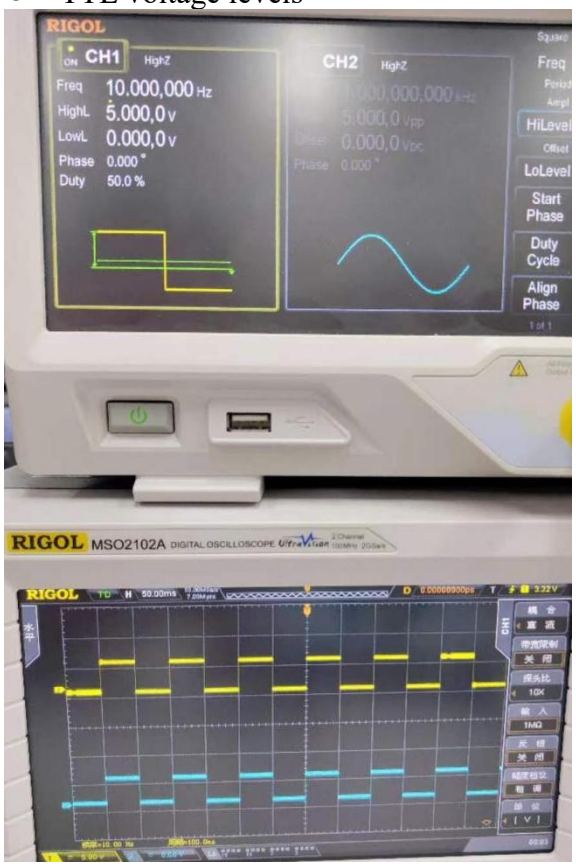


Figure 16. Wave image for initial state (TTL)

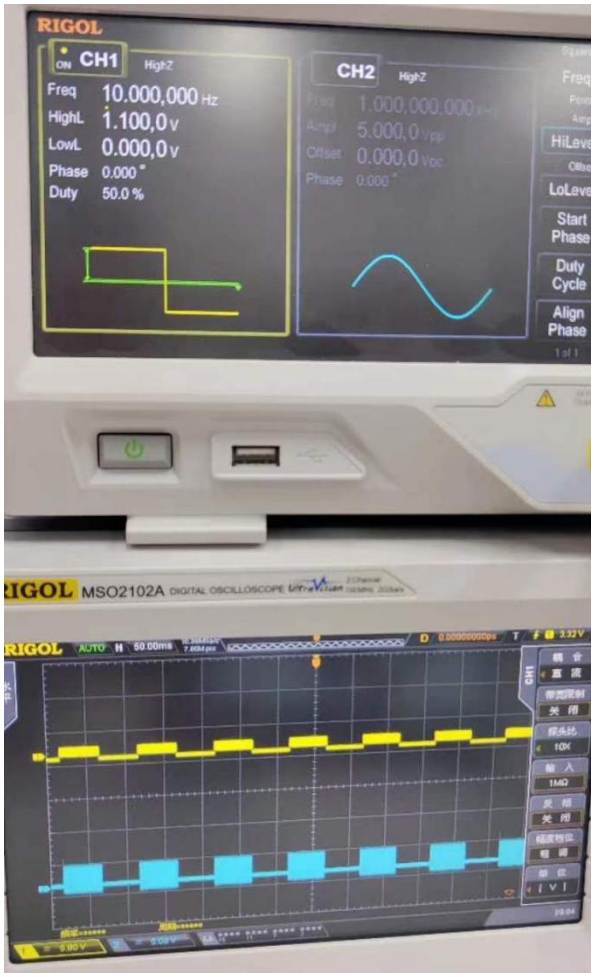


Figure 17. Wave image for unstable 1Y (TTL)

Figure 18. Wave image for unstable 1Y (TTL)

Figure 19. Wave image for HIGH in 1Y (TTL)

Figure 20. Wave image for LOW in 1Y (TTL)

The datasheet suggests that input value below 0.8V is counted as LOW, above 2.0V is counted as HIGH. Any other input leads to undefined (unstable) behavior.
In my experiment, when the level of low voltage in 1B remained 0V, and the level of high voltage in 1B was decreased to 1.1V, the output 1Y became unstable. When the level of high voltage in 1B remained 5V, and the level of low voltage in 1B was increased to 0.8V, the output 1Y became unstable. Because 1.1V is smaller than 2.0V, so this result generally complies with the datasheet.
However, there exist some error between the experimental data and datasheet, as the boundary 1.1V measured in the experiment is a bit away from the suggested boundary 2.0V. This may due to the slight differences in IC manufacturing, temperature, fluctuations in power supply voltage, etc.

7. Experiment G

7.1 Design

- Input-output logic

Step: Connect 1 channel of SIM with 1A, 1 channel of LOM with 1Y in the breadboard. Connect pin 14 to VCC (5.0V), pin 7 to ground.

	1A (V)	1B (V)
0	0.001	4.98
1	4.98	0.001

Table 7. IO for NOT Gate

7.2 Result

- Propagation delay time

(1) Ring Oscillator

Figure 21. Oscillating signals (T)

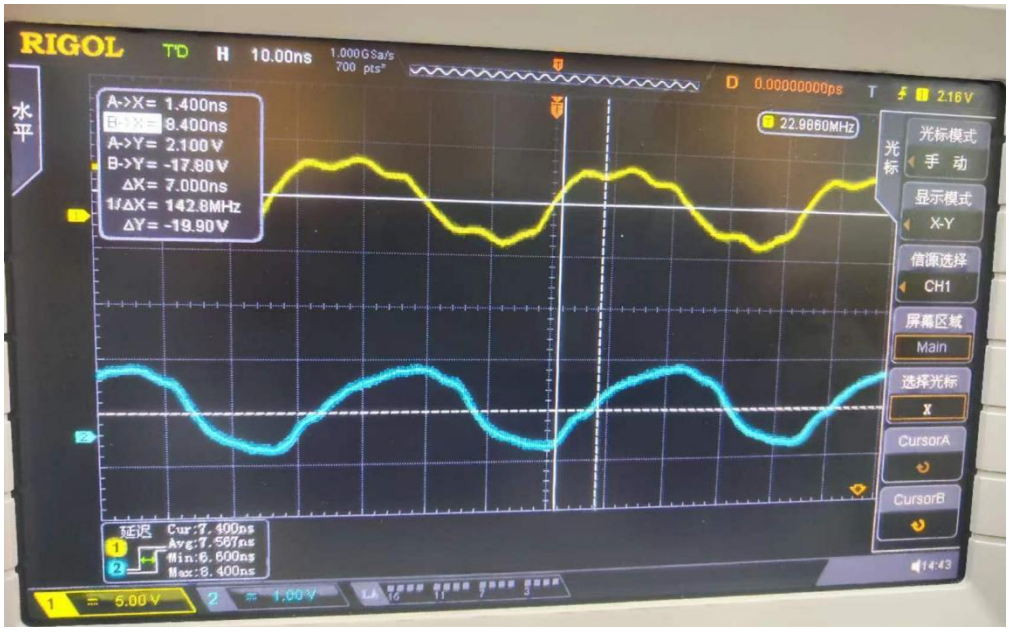


Figure 22. Oscillating signals ($\frac{T}{4}$)

T = 41.80ns
t_p = T/(2x5) = 4.18ns

(2) Measure propagation directly by an oscilloscope

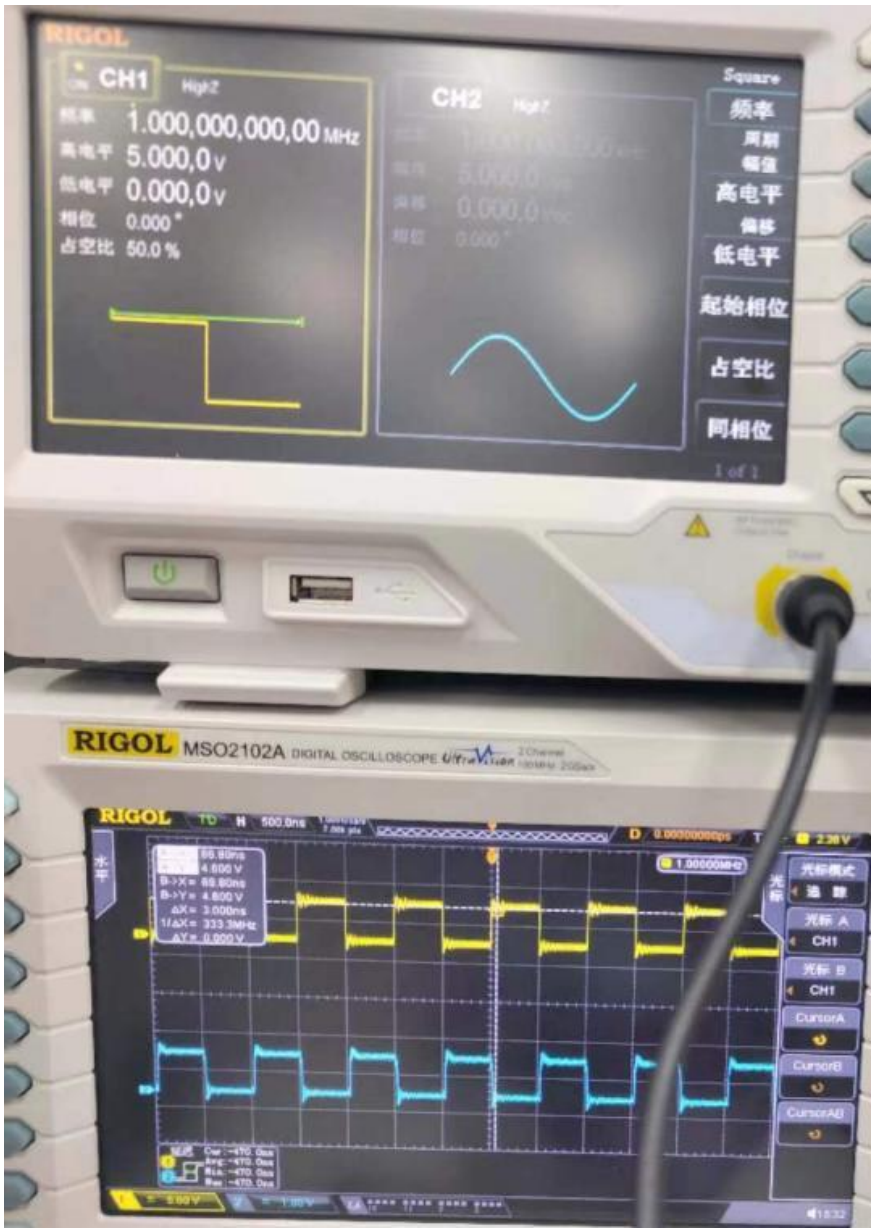


Figure 23. Oscillating signals

Figure 24. Oscillating signals (t_{PHL})

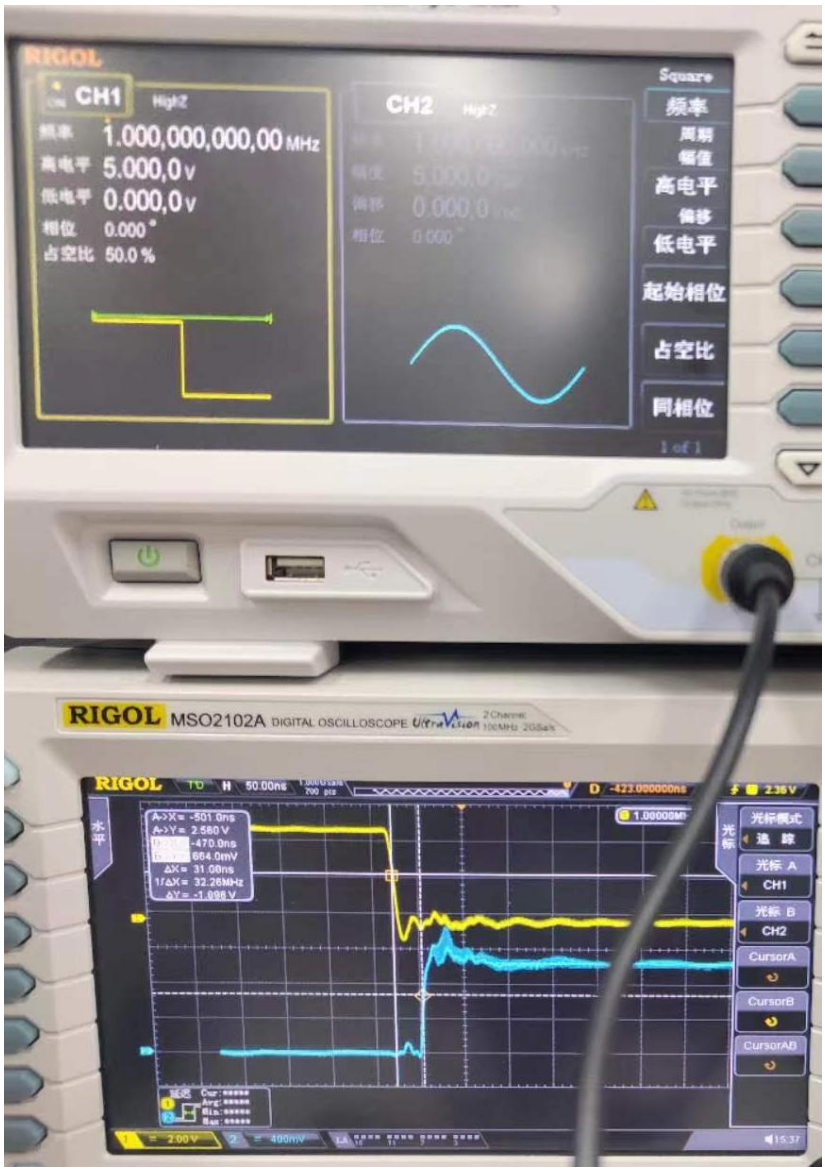


Figure 25. Oscillating signals (t_{PLH})

t_{PHL} = 25.00 / 5 = 5.00ns
t_{PLH} = 31.00 / 5 = 6.2ns
$t_p = (t_{PHL} + t_{PLH})/2$ = 5.6ns
The calculated t_p comply with that in the datasheet (typical 7ns when Vcc =6, at 25°C). The slight difference of t_p between two methods may be due to the imprecise placement of the cursors.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = 25 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	2.0	–	25	85	ns
			4.5	–	9	17	ns
			6.0	–	7	14	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	2.0	–	19	75	ns
			4.5	–	7	15	ns
			6.0	–	6	13	ns
T_{amb} = −40 to +85 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	2.0	–	–	105	ns
			4.5	–	–	21	ns
			6.0	–	–	18	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	2.0	–	–	95	ns
			4.5	–	–	19	ns
			6.0	–	–	16	ns
T_{amb} = −40 to +125 °C							
t_{PHL}/t_{PLH}	propagation delay nA to nY	see Figs 6 and 7	2.0	–	–	130	ns
			4.5	–	–	26	ns
			6.0	–	–	22	ns
t_{THL}/t_{TLH}	output transition time	see Figs 6 and 7	2.0	–	–	110	ns
			4.5	–	–	22	ns
			6.0	–	–	19	ns

Figure 26. datasheet of 74HC04

7.3 Questions

Q1. Why $t_p = T/(2x5)$? What happens if we take one inverter out of the ring?

T is the time when the current goes a cycle. The factor of 2 is included because the propagation delay t_p is often considered as the average of the high-to-low transition time t_{PHL} and the low-to-high transition time t_{PLH}. The factor of 5 represents the number of NOT gate. So, T/(2x5) calculates the mean of t_{PHL} and t_{PLH} per gate.

If we take one inverter out of the ring, T will decrease to approximately 33ns.

Q2. Based on two 74HC04 chips, what are the highest and lowest frequencies of oscillating signals which you can form?

Lowest: connect 12 NOT gates in a ring.

$T1 = t_p*2*12 \approx 100.32$ns (using t_p measured in the ring oscillator method)

$f1 = 1/T1 \approx 9.97*10^7$ HZ

Highest: use only 1 NOT gate.

$T1 = t_p \approx 4.2$ns (using t_p measured in the ring oscillator method)

$f1 = 1/T1 \approx 2.38*10^8$ HZ

7.4 Conclusion

By connect several gates in a ring, we can reduce the measurement error.

8. Conclusion

In this session, I

- Understood the datasheet of ICs.
- Built simple AND circuit by diode and transistors.

- Did some basic experiments on AND gate (74HC08, 74LS08) and NOT gate (74HC04) and verify their properties.
- Measured voltage transfer characteristics (VTC) of AND gate.
- Understood the different voltage levels by CMOS and TTL AND gates.
- Understood and measured chip propagation delay time.

I learned:

- How to use logic analyzer, oscilloscope.

  When using analyzer and oscilloscope, we should always keep in mind to connect them with ground.

  When using a oscilloscope, the input current should not be too large. When I was doing the CMOS voltage levels experiment, I set the current to 1V, and the there is no square wave. However, when I adjust the current to 0.01V, the square wave appear.

- How to design AND circuits using diodes and transistors. I learned the properties of diodes and transistors. Diodes have a fixed voltage drop when it is forward-biased. The resistance of diodes can not be ignored directly in practical.

- How to use a signal generator. When we use the signal generator, we should check if it is set to high-low voltages, or DC voltage + offset, which will be totally different. For example, when set to high-low voltages, 0 ~ 6V; When set to DC voltage + offset, -3V ~ 3V.