ECE2810 Digital Systems Design Laboratory

Lab 1: CMOS and TTL / Datasheet / Basic Experiments on AND and NOT Gates

School of Science and Engineering
The Chinese University of Hong Kong, Shenzhen

2025-2026 Term 1

1. Objectives

In Lab 1, we will spend the 2-week session to understand the following:

- Understand the difference between CMOS and TTL.
- Learn to read the datasheet of ICs.
- Basic experiments on the AND gate and NOT gate.
  - Learn to build a simple AND circuit by using a diode.
  - Understand the different voltage levels of CMOS and TTL AND gates.
  - Understand chip propagation delay time, and learn the way to measure it.

2. Oscilloscope

An oscilloscope is an essential electronic test instrument used to visualize and analyze the waveform of electronic signals. It displays voltage signals over time, providing insights into their behavior, characteristics, and interactions in circuits.

Figure 1 displays the oscilloscope you will be using in this lab, while Figure 2 illustrates the probes. Please ensure you read the manual to familiarize yourself with the oscilloscope's operation.

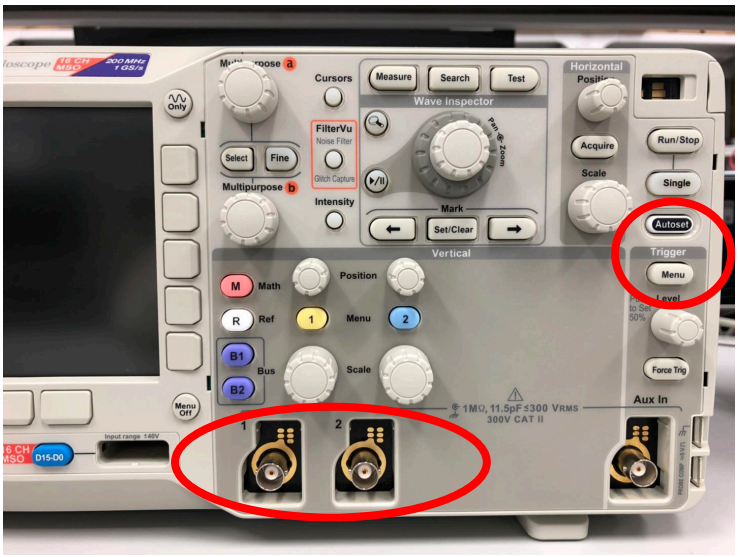

Figure 1. Connectors and buttons of the oscilloscope.

Figure 2. Probes of the oscilloscope.

3. Function Generator

The RIGOL DG4202 is a versatile function generator designed for a wide range of signal generation applications in electronics and testing. It can produce various waveforms, including Sine, Square, Pulse, etc. Additionally, it features two output channels, enabling the simultaneous generation of two independent signals.

In this lab, you will use the function generator shown in Figure 3 to produce a square waveform that will serve as the input to both the AND gate and the NOT gate. Please read the manual to understand how to use it.

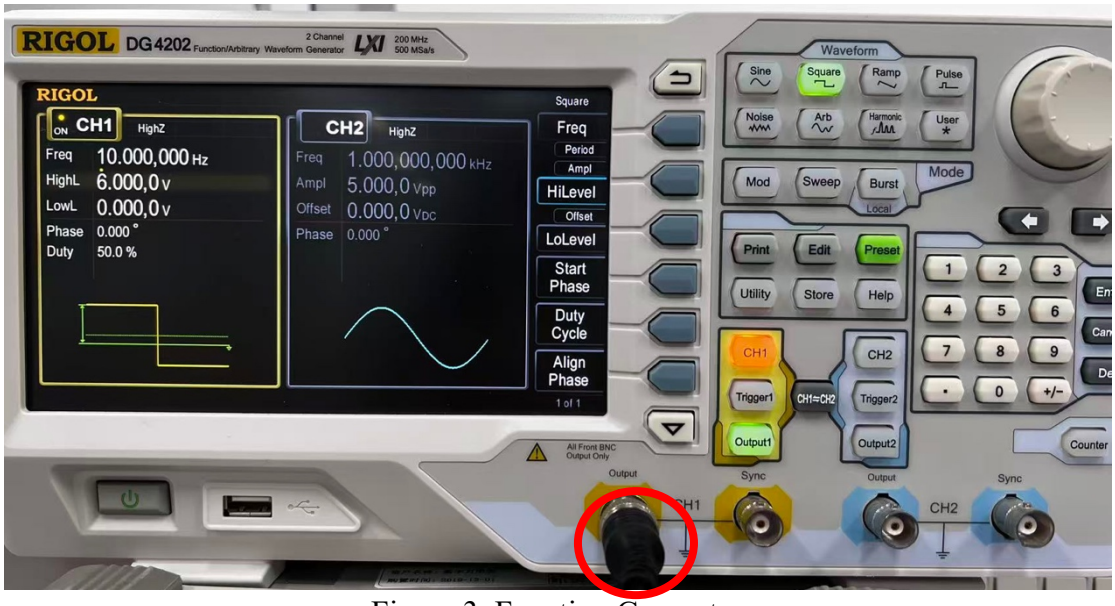

Figure 3. Function Generator

4. CMOS and TTL

To represent digital logic “0” and “1”, there are different voltage levels. TTL and CMOS are two of them. TTL stands for Transistor-Transistor Logic. It is a class of integrated circuits (ICs). The name is derived from the use of two Bipolar Junction Transistors (BJTs) in the design of each logic gate. Complementary metal oxide semiconductor (CMOS) is another classification of ICs that uses Field Effect Transistors in the design. A comparison of their features is listed in Table 1:

- The primary advantage of CMOS chips over TTL chips is the greater density of logic gates within the same material.
- TTL chips tend to consume a lot more power compared to CMOS chips, especially at rest.
- CMOS chips are a bit more delicate than TTL chips when it comes to handling, as they are quite susceptible to electrostatic discharge.
- The voltage levels of TTL and CMOS are different.

Table 1. Voltage levels of TTL and CMOS.

Technology	L voltage	H voltage	Notes
CMOS	0 V to 1/3 V_{cc}	2/3 V_{cc} to V_{cc}	V_{cc} = supply voltage
TTL	0 V to 0.8 V	2 V to V_{cc}	V_{cc} = 5 V ±10%

In this lab, we will examine the difference between CMOS and TTL based on the two ICs, 74HC08 and 74LS08, both with the functionality of an AND gate.

5. Datasheet of IC

To understand how to use a digital logic IC, it is crucial to be able to read its datasheet, which provides detailed information about the chip, sometimes too much for a beginner. In the appendix of this lab handout, we have provided complete datasheets for the 74LS08, 74HC08, and 74HC04.

For beginners, the most important specifications include:

- *Supply voltage*, found in the Table of Recommended Operating Conditions.
- *Input voltages* V_{IH} and V_{IL}, and *output voltages* V_{OH} and V_{OL}, are found in the Table of Electrical Characteristics.
- *PIN arrangement.*

6. Basic experiments on AND logic and inverter

6.1 Experiment 1: AND logic and Diode-based Circuit

AND logic is shown in the Table 2, with input A and B, and output AB.

Table 2. Truth table for the AND gate.

Input		Output
A	**B**	**AB**
0	0	0
0	1	0
1	0	0
1	1	1

In this experiment, you will implement a diode-based circuit to create an AND gate. Pay attention to the polarity of the diode. When a positive voltage above a certain threshold (approximately 0.7V) is applied to the diode, current can pass through it. Otherwise, the diode behaves as if it were disconnected. The polarity is illustrated in Figure 4.

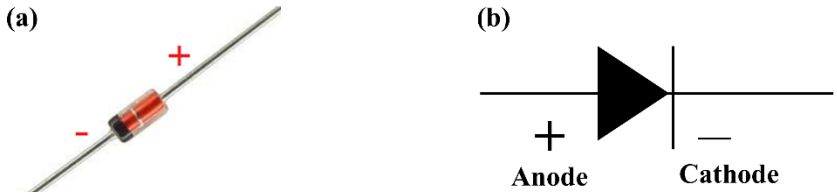

Figure 4. Diode. (a) Diode component. (b) Diode symbol.

We can construct a simple AND logic circuit using the diagram as shown in Figure 5. Use a 1kΩ resistor for R_1 and take out two diodes from the box. You can build an AND logic circuit on a breadboard (Figure 6(a)). Like experimental setup in Figure 6(b), you can measure the voltage at the A, B and O nodes, and record the data in table 3.

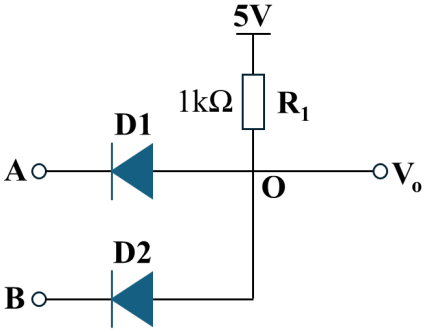

Figure 5. A simple AND logic circuit by diodes

Figure 6. (a) An AND logic circuit built on a breadboard. (b) Experimental setup for measuring voltage across the AND logic circuit.

[QUESTION IN REPORT] Explain how the circuit above realizes AND logic.
[IN REPORT] Use a multimeter to measure the voltages in the input and output pins and fill in the form. Include this measured data in your report.

Table 3. Signal measured for AND based on diodes.

	A (V)	B (V)	V_O (V)
(0,0)			
(0,1)			
(1,0)			
(1,1)			

[DEMOSTRATION - 1] Show TA your Table 3, and3 and demonstrate 1-2 rows using your circuit.

6.2 Experiment 2: AND Gate

Scientists, engineers, and IC manufacturers have made a great effort in developing a wide range of digital logic ICs with higher performance and improved durability. Moving forward, we will utilize them directly. The 74HC08 and 74LS08 are two AND gates, from the CMOS and TTL categories, respectively.

6.2.1 74HC08

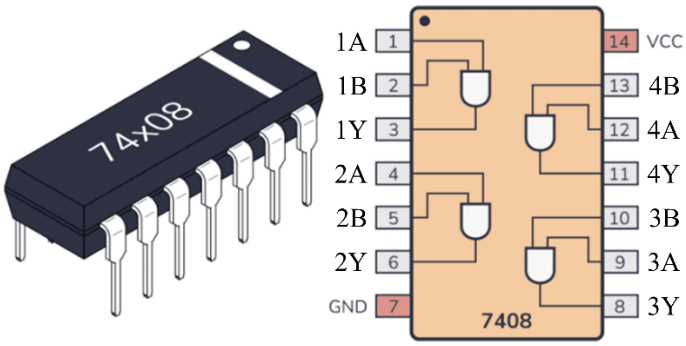

Figure 7. Pin arrangement of 74HC08 [1]

- **Input-output logic**

  (1) Read the datasheet of 74HC08 and understand the pin arrangement (ref. Figure 7).

  (2) Select an AND gate. The pins to be wired include VCC, GND, 1A, 1B, and 1Y.

  (3) Connect the outputs from two channels of the SIM to the inputs 1A and 1B. Use the output 1Y as the input for one channel of the LOM. Make these connections on the breadboard (ref. Figure 8), and you can set VCC to 5.0V.

  (4) Investigate the logic to confirm that it functions as an AND gate. The LED should light up only when both switches are turned on.

  (5) Measure and fill in Table 4.

Figure 8. (a) An AND logic circuit built by connecting the 74HC08 chip to the soldered PCB. (b) Experimental setup for measuring voltage across the AND logic circuit.

Table 4. IO for CMOS AND Gate.

	1A (V)	**1B (V)**	**1Y (V)**
(0,0)			
(0,1)			
(1,0)			
(1,1)			

[IN REPORT] Draw the gate-level circuit diagram. Include the data and the form above.

[DEMOSTRATION - 2] Show TA your Table 4, and demonstrate 1-2 rows using your circuit.

- **CMOS voltage levels**

Next, we check the CMOS voltage levels.
(1) Wire the circuit based on the diagram in Figure 9. Do not forget the V_{CC} and ground pins on the chip.

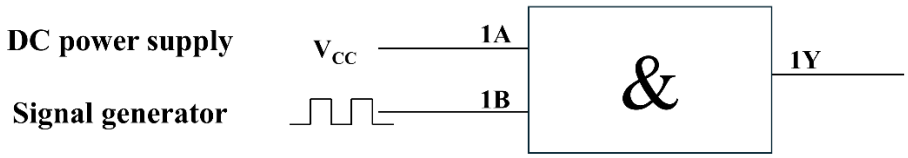

Figure 9. Circuit diagram.

(2) Connect the DC power supply, signal generator, and oscilloscope (CH1 for 1B and CH2 for 1Y) into the circuit. An example is shown in Figure 10. Set V_{CC}=6.0V in the power supply. DO NOT output now.
(3) Use the signal generator to output a 10 Hz square wave, with 6.0V representing "1" and 0V representing "0". When configuring the wave, ensure you set the High level to 6.0V and the Low level to 0V.
(4) Output power supply and the signal generator. Measure the observed input and output in the oscilloscope.
(5) Gradually reduce the level of high voltage of the wave sequence at appropriate steps, e.g., 0.1V (ref. Figure 11) and reach a point where the unstable reading occurs. Record the unstable wave image and voltage at this high level (Ref. Figure 12 for stable and unstable wave forms).
(6) Reset high voltage to 6.0V. Gradually increase the level of low voltage at appropriate steps, and reach another unstable reading. Record the unstable wave image and voltage of this low level.

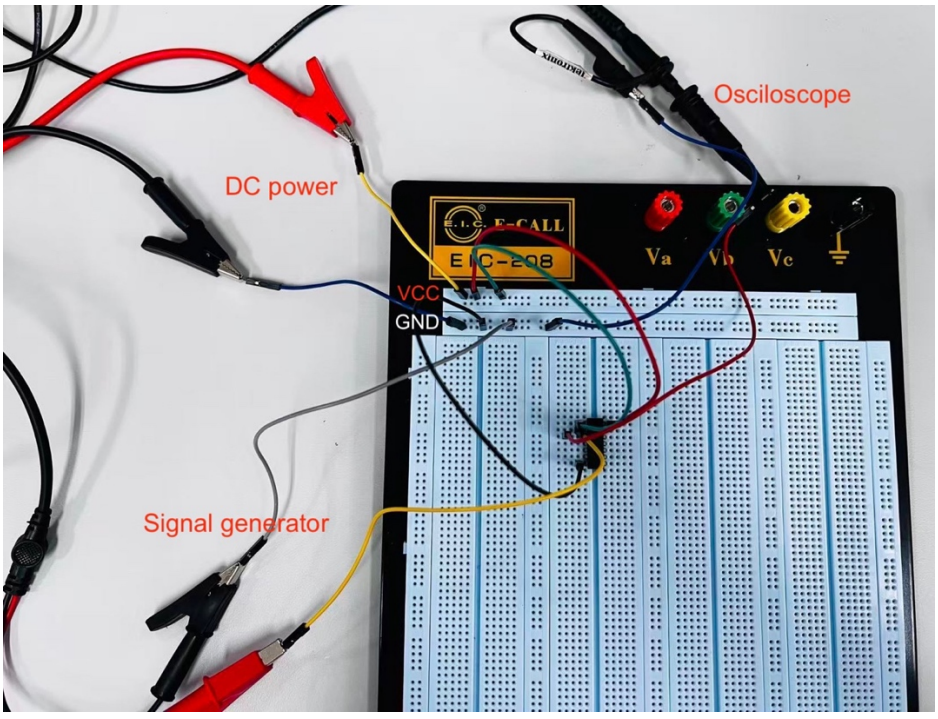

Figure 10. Illustration of the connections

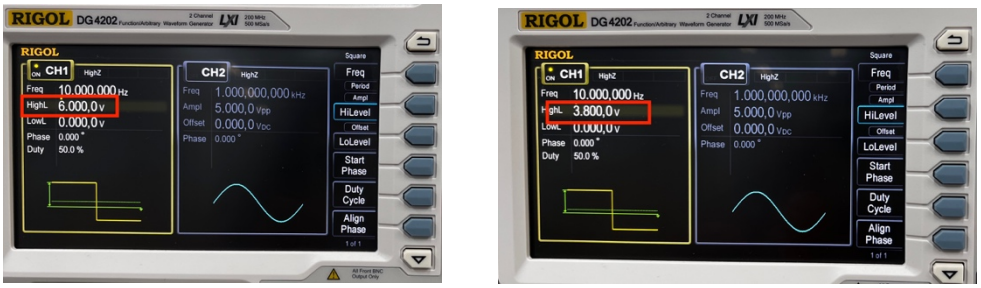

Figure 11. Gradually reduce the level of high voltage

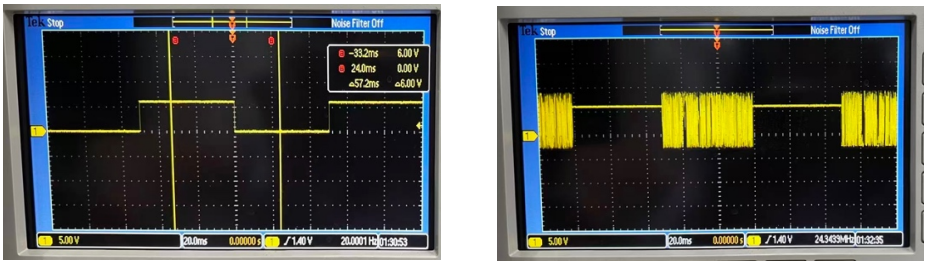

Figure 12. Stable and unstable output

[IN REPORT] Include the necessary data and wave images needed to verify the CMOS voltage levels. Discuss if the V_{IH} and V_{IL} in the datasheet comply with the observation in this experiment. Include some typical wave images (one image each for low, high, and unstable in 1Y) in steps (5)-(6).

6.2.2 74LS08

- **Input-output logic**
  (1) As before, connect two channels of SIM, one channel of LOM, and the 74LS08 on the breadboard. Select V_{CC}=5.0V.
  (2) Investigate the logic, and verify that it is an AND gate
  (3) Measure and fill in Table 5.

Table 5. IO for TTL AND gate.

	1A (V)	1B (V)	1Y (V)
(0, 0)			
(0, 1)			
(1, 0)			
(1, 1)			

[IN REPORT] Include the data and the form above.
[DEMOSTRATION - 3] Show TA your Table 5, and demonstrate 1-2 rows using your circuit.

- **TTL voltage levels**
  Now we can check the TTL voltage levels.
  (1) Wire the circuit similarly to experiment on CMOS voltage levels (ref. Figure 9).

(2) Connect the DC power supply, signal generator, and oscilloscope (CH1 for 1B and CH2 for 1Y) into the circuit. Set V_{CC}=5.0V in the power supply. DO NOT output now.
(3) Use the signal generator to output a 10Hz square wave with 5.0V for "1", and 0V for "0".
(4) Output power supply and the signal generator. Observe input and output in the oscilloscope.
(5) Gradually reduce the level of high voltage of the wave sequence of 1B at appropriate steps, and reach a point where the unstable reading occurs. Record the unstable wave image and the voltage at a high level.
(6) Reset high voltage to 5.0V. Gradually increase the level of low voltage at appropriate steps, and reach another unstable reading. Record the unstable wave image and the voltage at a low level.

[IN REPORT] Record the necessary data and wave images needed to verify the TTL voltage levels. Discuss if the V_{IH} and V_{IL} in the datasheet comply with the observation in this experiment. Include some typical wave images (one image each for low, high, and unstable in 1Y) in steps (5)-(6).

6.3 Experiment 3: NOT Gate (Inverter)

The inverter has the logic table below (Table 6). It simply inverts the input. Its logic symbol is shown in Figure 13.

Table 6. Truth table for NOT gate.

A	$\overline{A}$
0	1
1	0

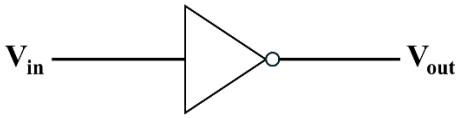

Figure 13. Inverter symbol.

74HC04 contains 6 inverter gates. The pin arrangement is shown in Figure 14.

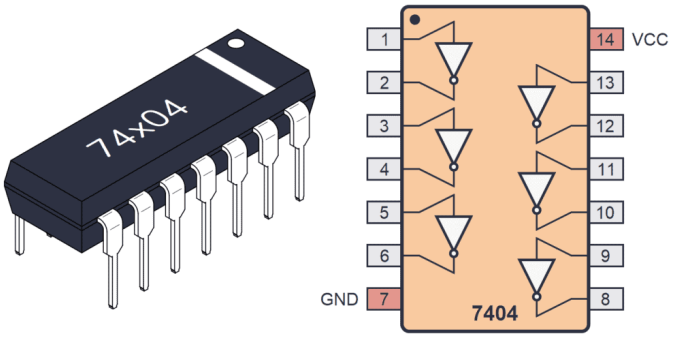

Figure 14. 74HC04 Pin arrangement

6.3.1 Input-Output Logic

Design the input-output logic testing circuit. It is not difficult to design based on the AND gate steps. Pay attention to the V_{CC}.

[IN REPORT] Write down your steps. Include the data of the signals measured.
[DEMOSTRATION - 4] Show the instructor or TA that your circuit works.

6.3.2 Propagation Delay Time

Logic gates have a propagation delay time, which results from limitations on switching speed or the frequency at which a logic circuit can operate. The shorter the propagation delay, the higher the switching speed of the circuit, and thus the higher the frequency at which it can operate.

There are two delay times, t_{PHL} specifying the time delay of the output from high to low, and t_{PLH} indicating the time delay of the output from low to high. Generally, the 50% points are used in both input and output signals, as shown in the figure below.

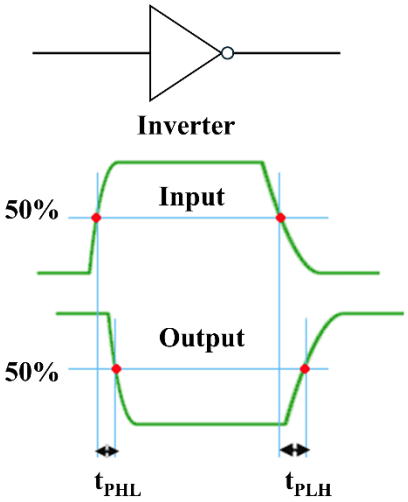

Figure 15. Inverter symbol and propagation delay.

In this part, you will measure the propagation time directly with an oscilloscope. Wire 5 NOT gates of a 74HC04 into the circuit as shown in Figure 16.

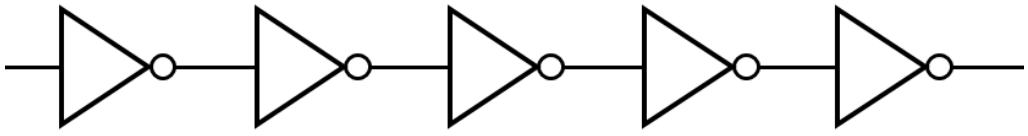

Figure 16. The circuit of a sequence of inverters.

Generate a square wave at a certain frequency, and input it into a sequence of connected inverters. Measure the input and the final output by CH1 and CH2 of the oscilloscope (ref. Figure 17 and Figure 18). Try to read t_{PHL} and t_{PLH}. (Hint: to allow you to magnify the timeline, use some high frequency, e.g., 1MHz will help.)

[IN REPORT] Include the image of the oscillating signals, t_{PHL}, and t_{PLH}. How do you estimate the propagation delay?
[DEMOSTRATION - 5] Show your result to the instructor or TA.

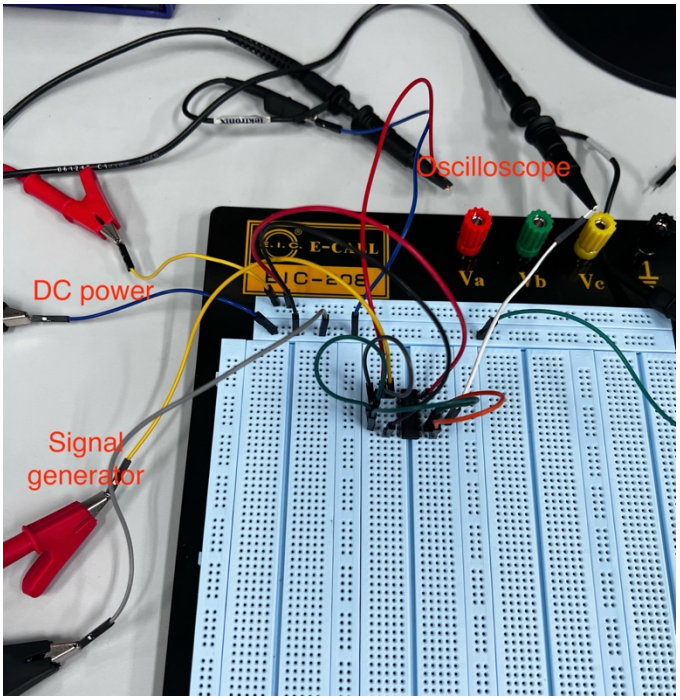

Figure 17. Circuit of connecting a sequence of inverters.

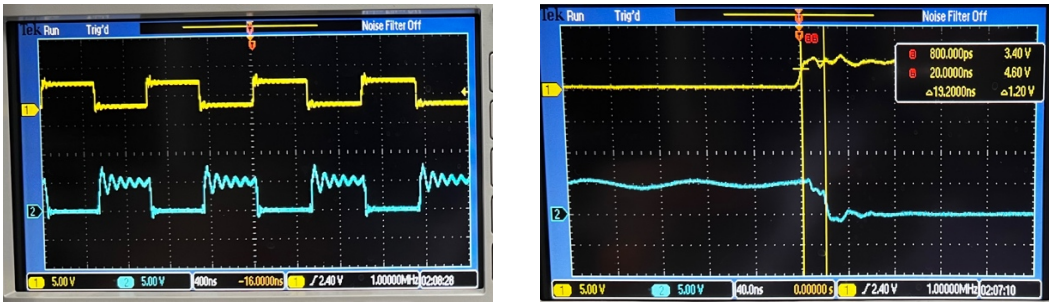

Figure 18. Left: Observe the input and output waveforms. Right: Zoom out on the waveform and measure the delay using the cursors.

7. Lab Report

Write the lab report comprehensively. A template has been provided on Blackboard.

Submit the report of Lab 1 in ***PDF*** to the folder ***Digital Systems Design Lab/Report Submission/Lab 1*** on Blackboard by the deadline below:

- ***LAB01 (Thursday session): 23:59, Saturday, September 27, 2025***
- ***LAB02 (Friday session): 23:59, Sunday, September 28, 2025***

Each day of late submission will result in a 10% deduction from the report's raw marks.

Appendix:

Components needed for this lab.

1. 20 Dupont cables (double male terminals)
2. Diode x2
3. 1 kΩ resistor x1
4. 74HC08 x1

5. 74LS08 x1
6. 74HC04 x1

Remember to sort and return items 2-8 back to the store shelf after lab. You can keep item 1 in your box for usage in the future.

For any malfunctioning component, report to the instructor or TA, and DO NOT put it back.

8. Reference

[1] https://www.build-electronic-circuits.com/7400-series-integrated-circuits/74hc08-74ls08/