

ECE2810 Digital Systems Design Laboratory

Laboratory Report #3

Name:

Student ID:

Date:

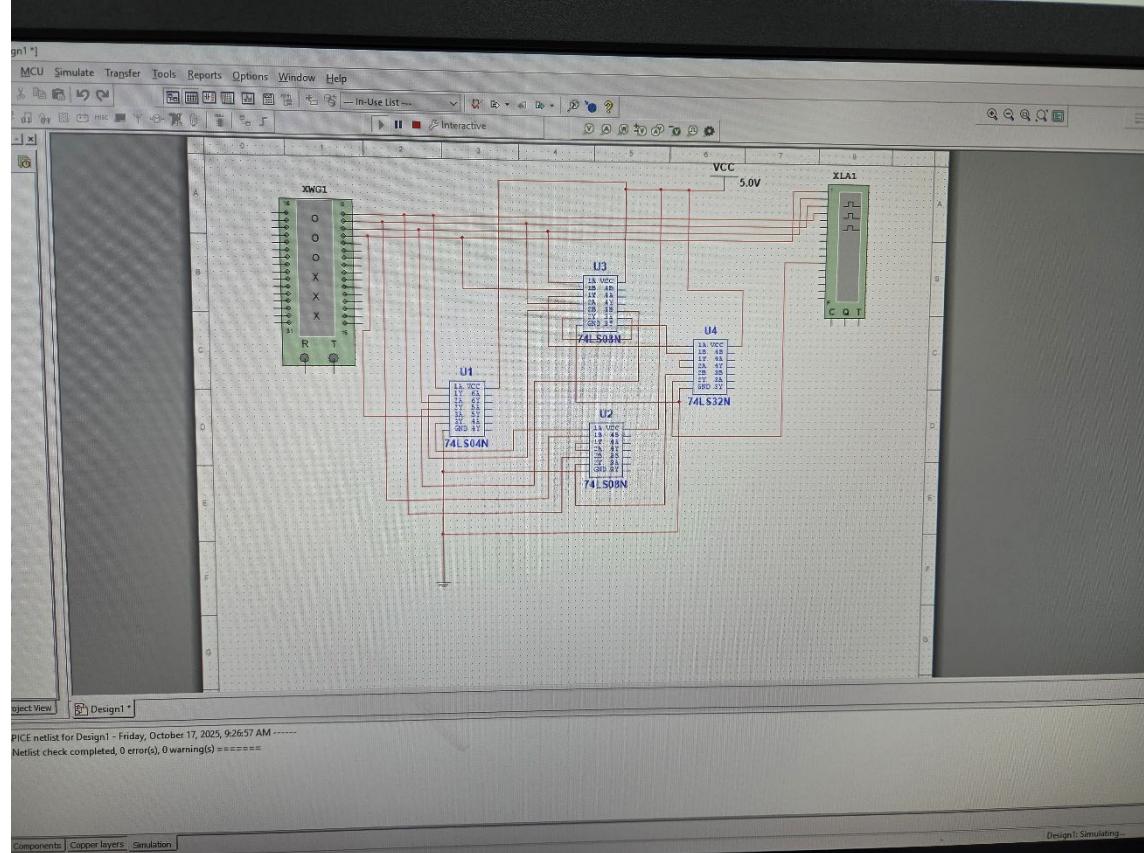
2025-10-17

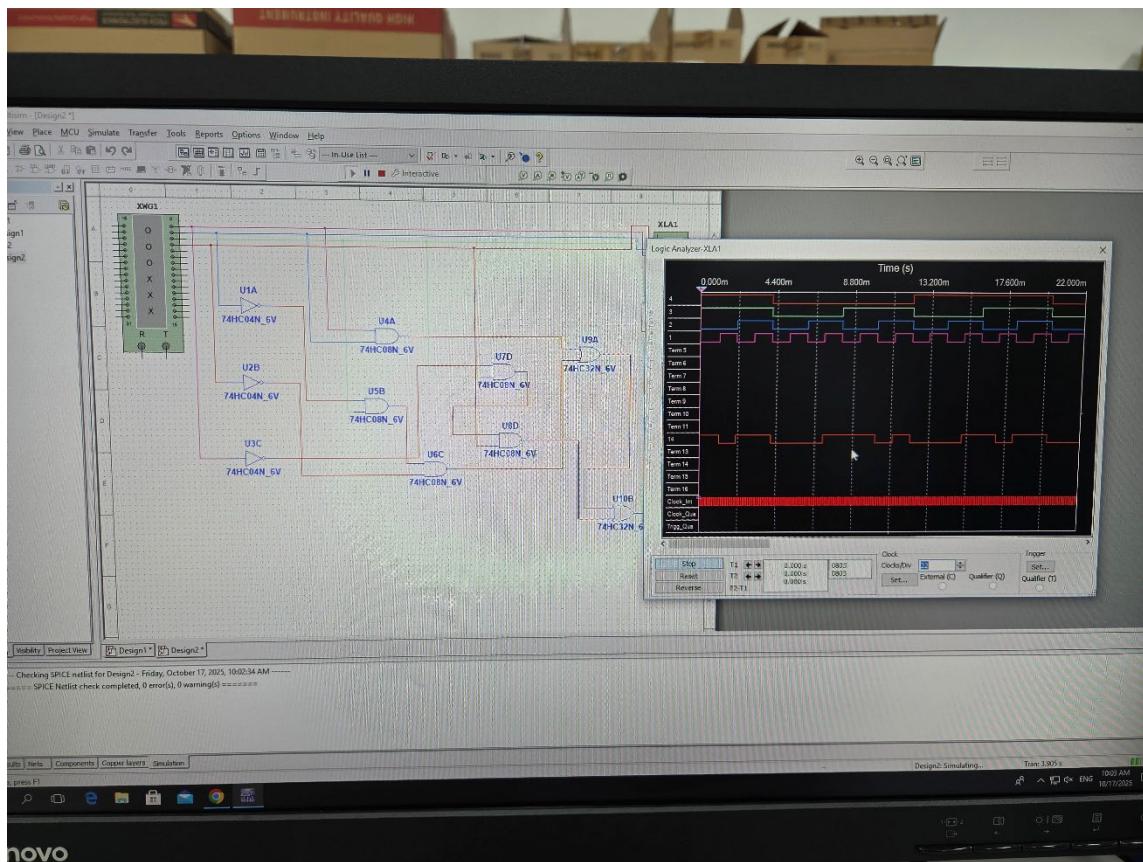
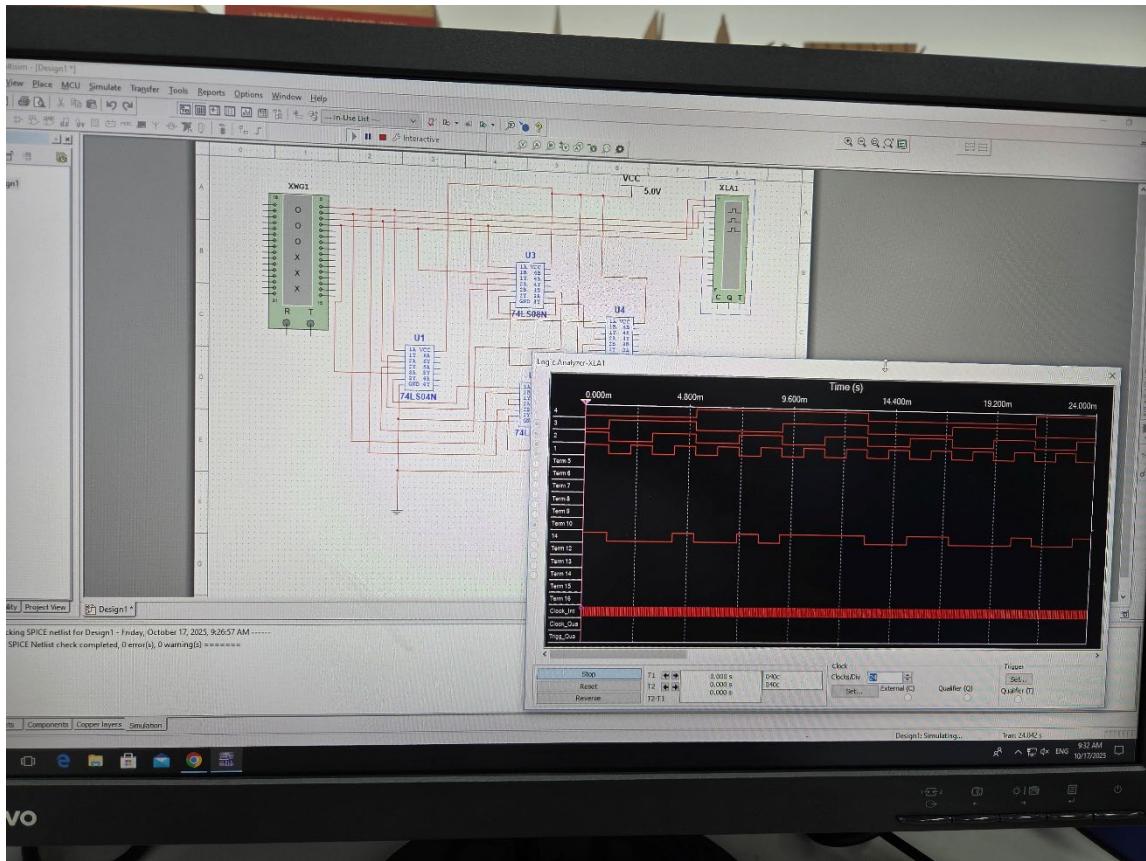
The Chinese University of Hong Kong, Shenzhen

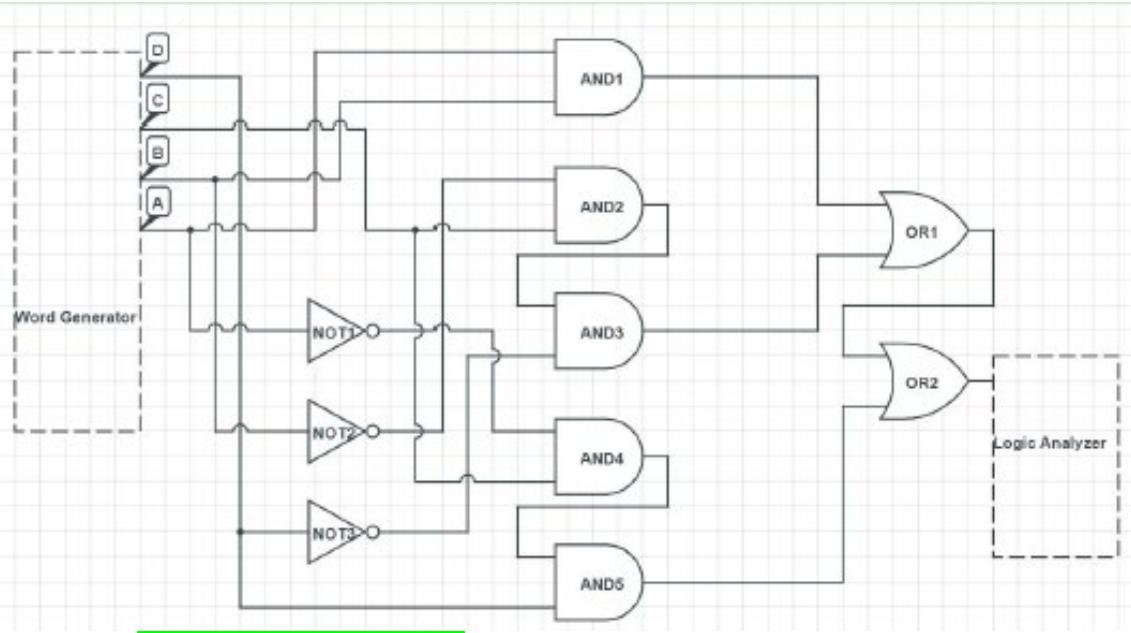
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- Experiment A: Combinational Logic Circuit
 - Experiment B: Guided Multisim Simulation
 - Experiment C: Individual Gate Test (Hardware Experiment)
 - Experiment D: Combination of Gates (Simulation and Hardware Experiment)

1. Experiment A

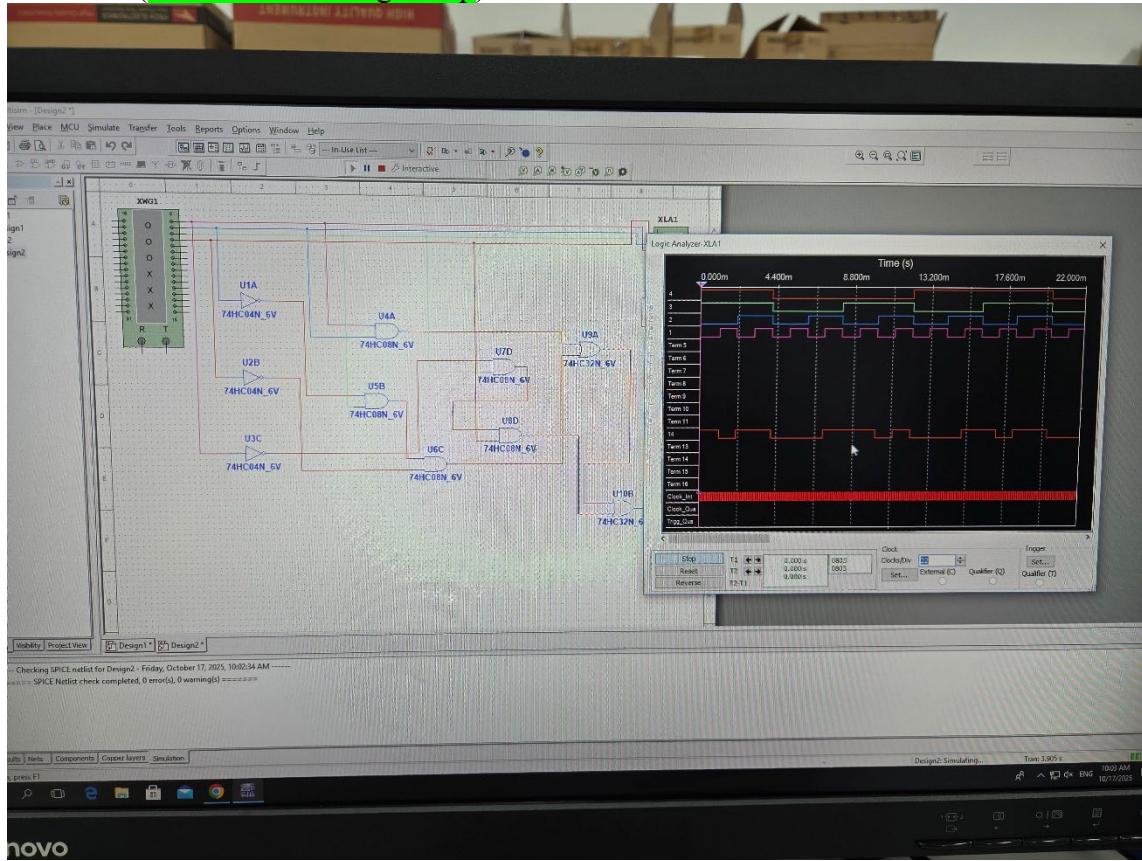
1.1 Design (Chip Level&Gate Level)







1.2 Result(Multisim+Karnaugh Map)

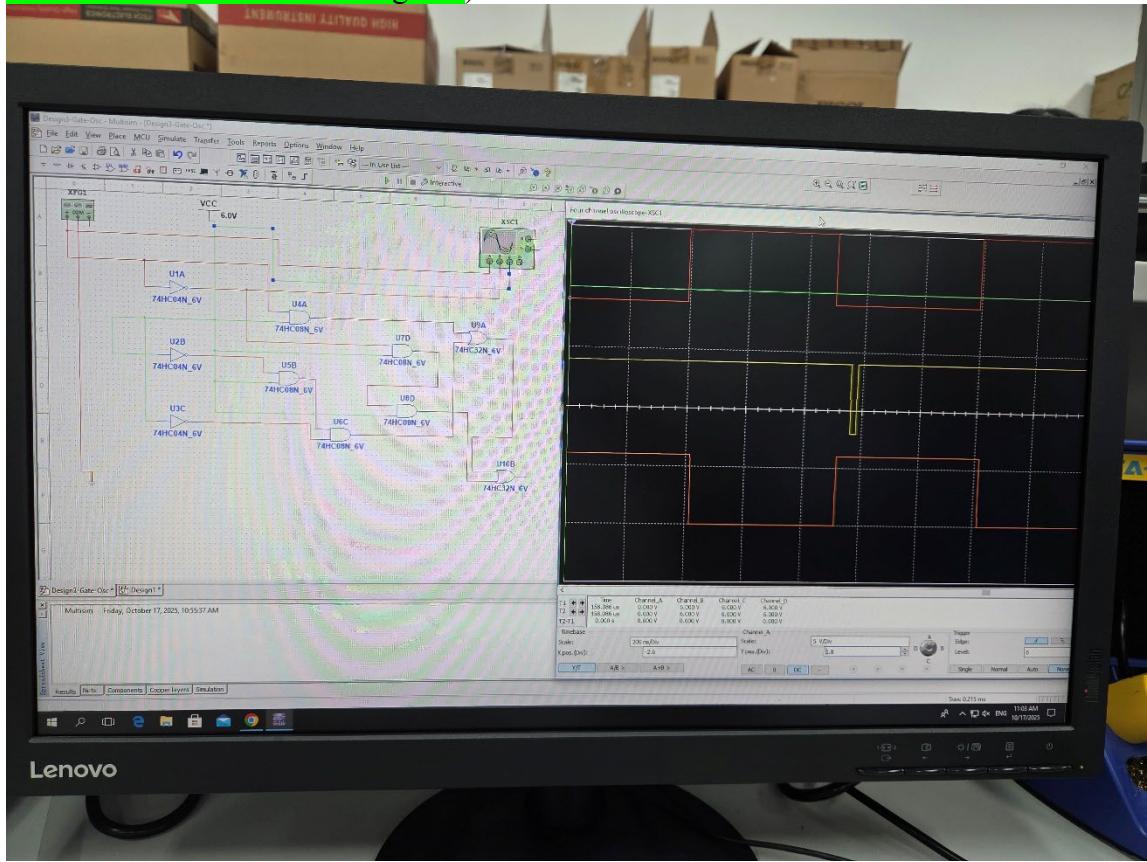


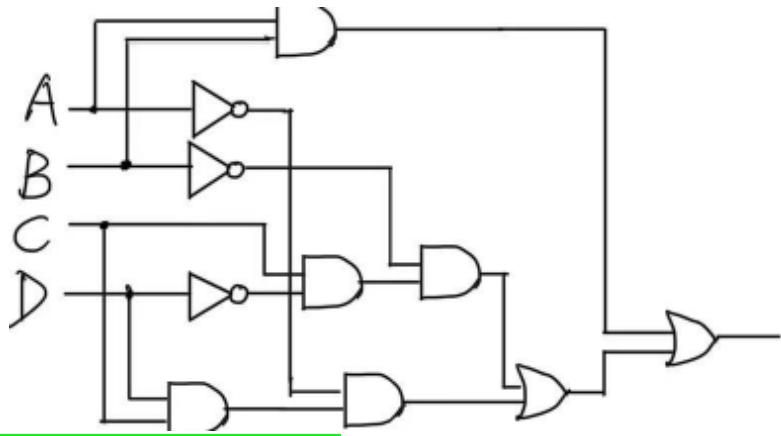
A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Table 1. Truth table for $Y = AB + \bar{B}C\bar{D} + \bar{A}CD$

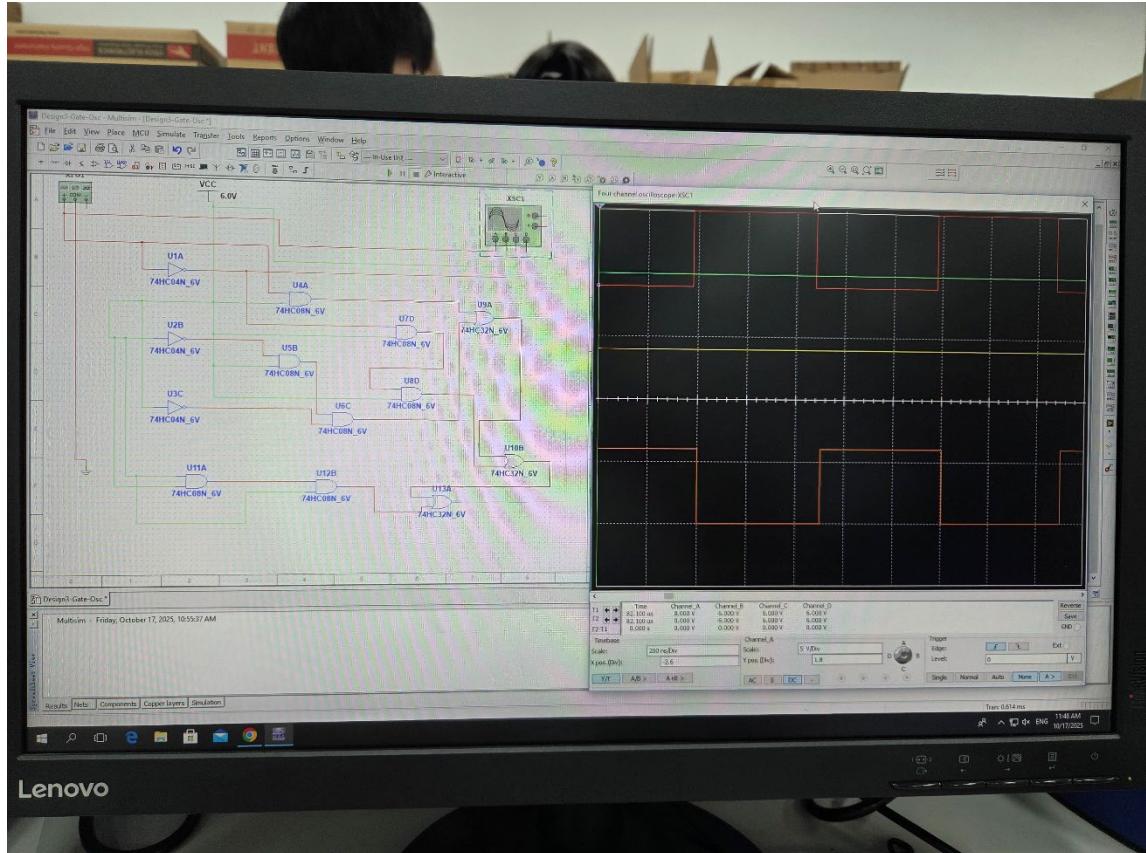
2. Experiment B

2.1 Design(Software+Hardware, Software including the original version with glitch and modified version without glitch)

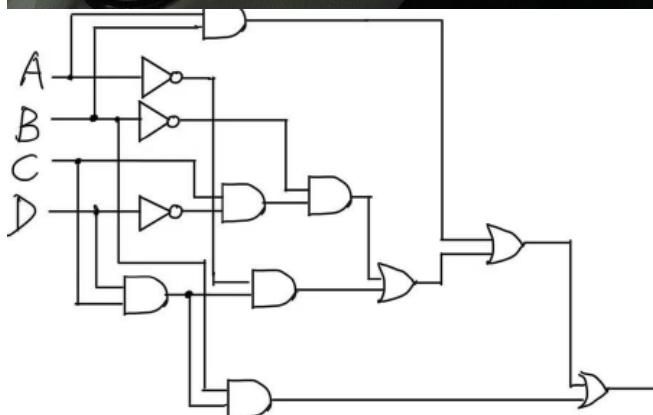




(Original Design with Glitch)

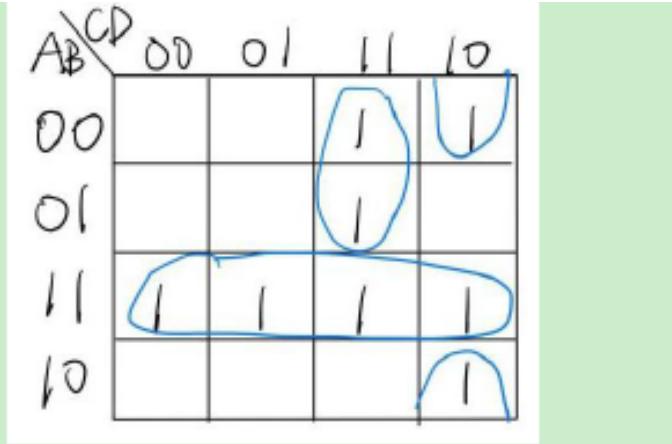


Lenovo

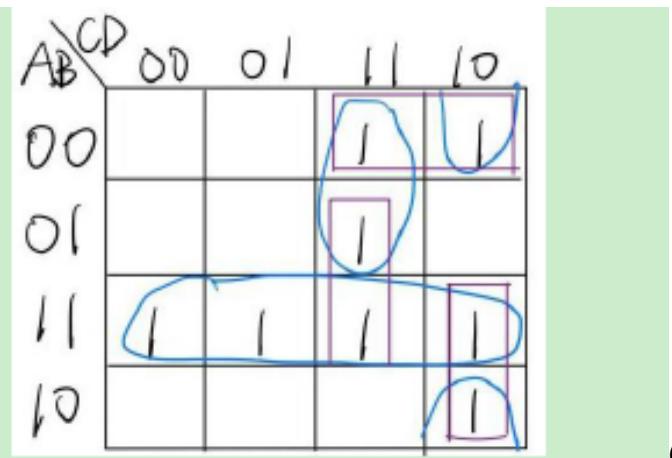


(Using BCD to eliminate Glitch)

2.11Result (Karnaugh Map + Software Result + Hardware Result)



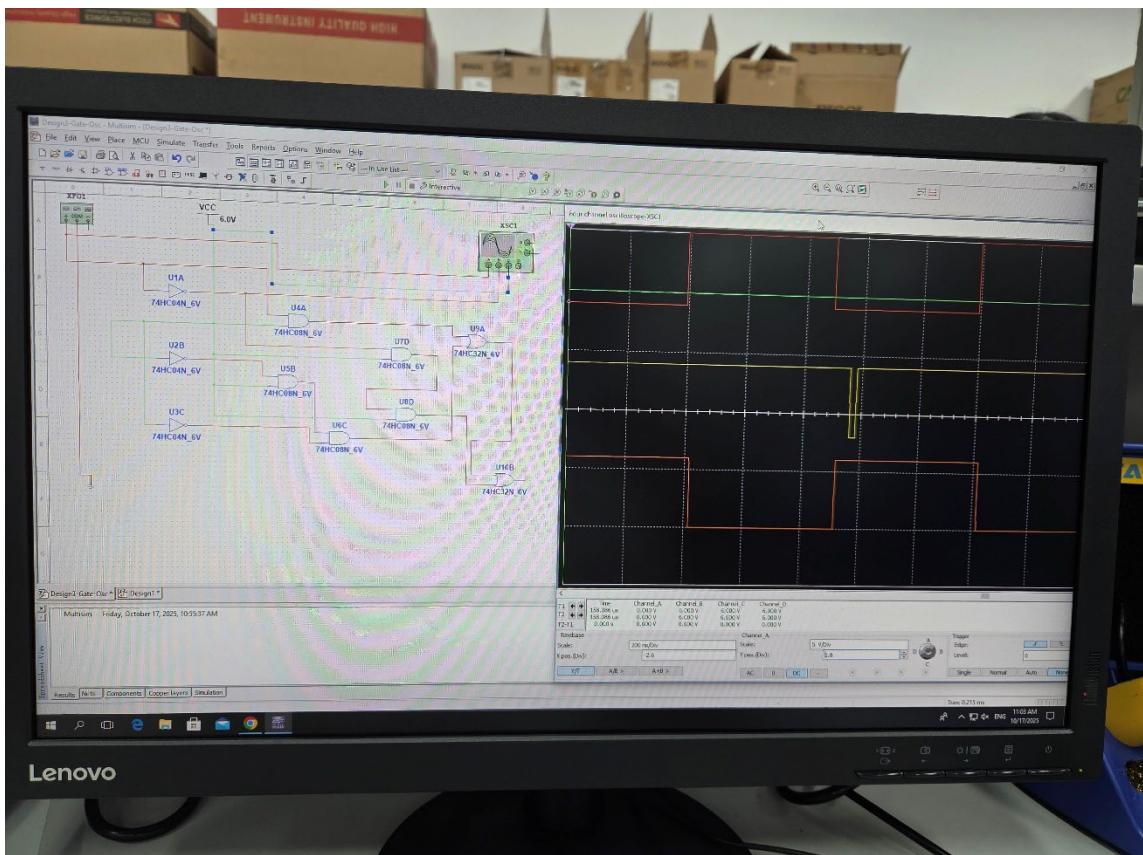
(Original Karnaugh Map)



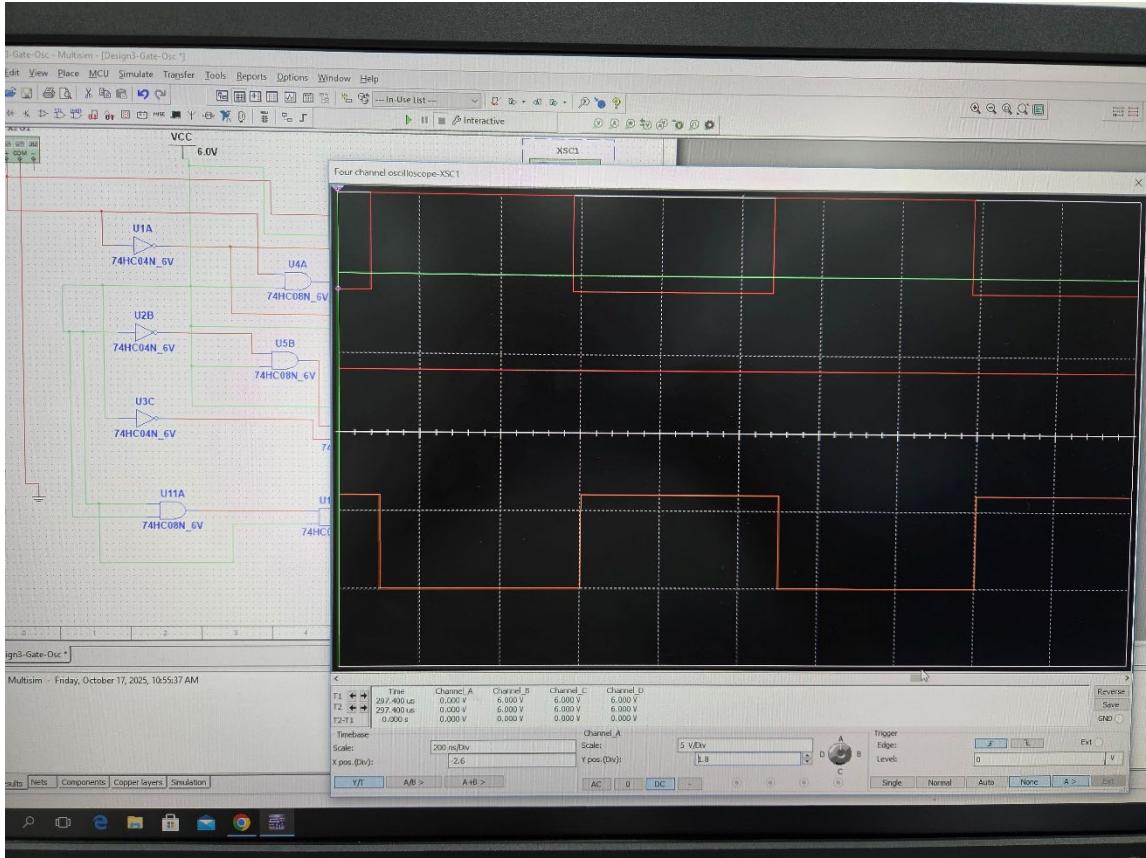
(Modified Karnaugh Map where

timing hazard may occur. Refer to the purple rectangle)

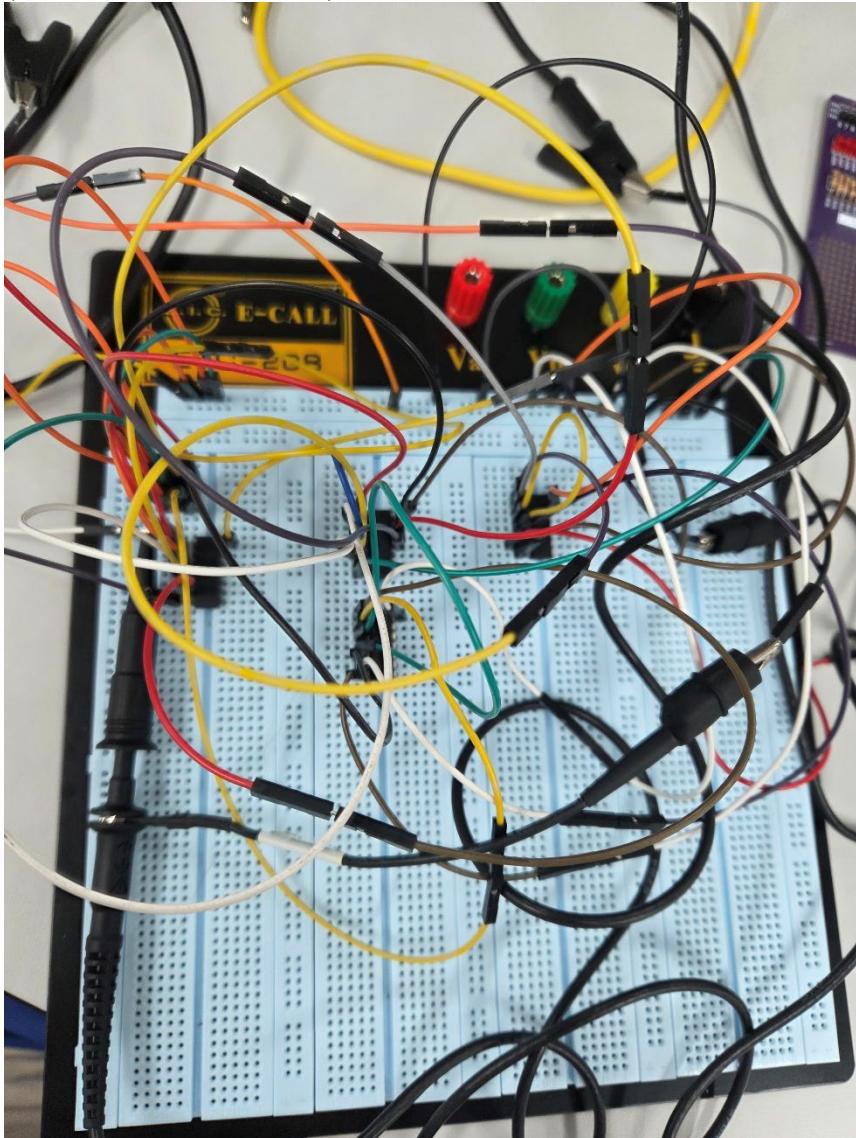
Timing hazard may occur at transition between 1111 (ABCD) and 0111 (ABCD); 0011 (ABCD) and 0010 (ABCD); 1110 (ABCD) and 1010 (ABCD).



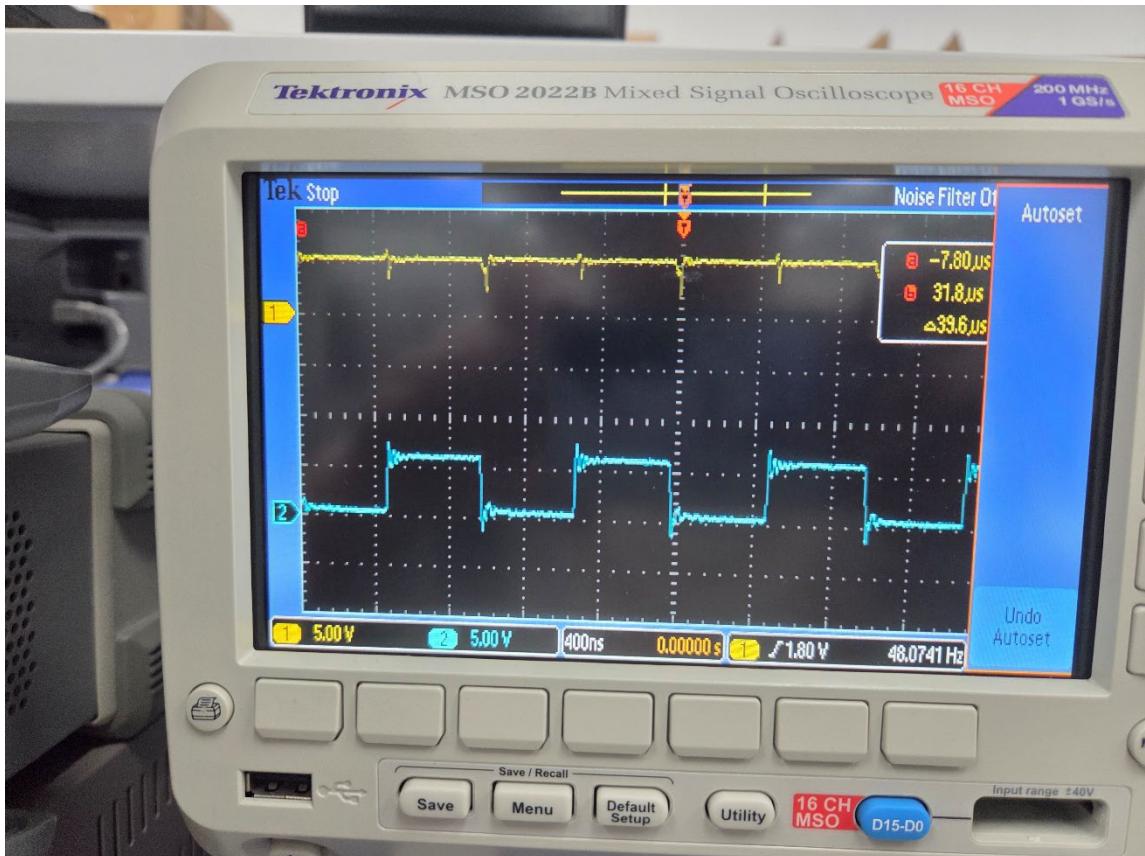
(Original with Glitch)



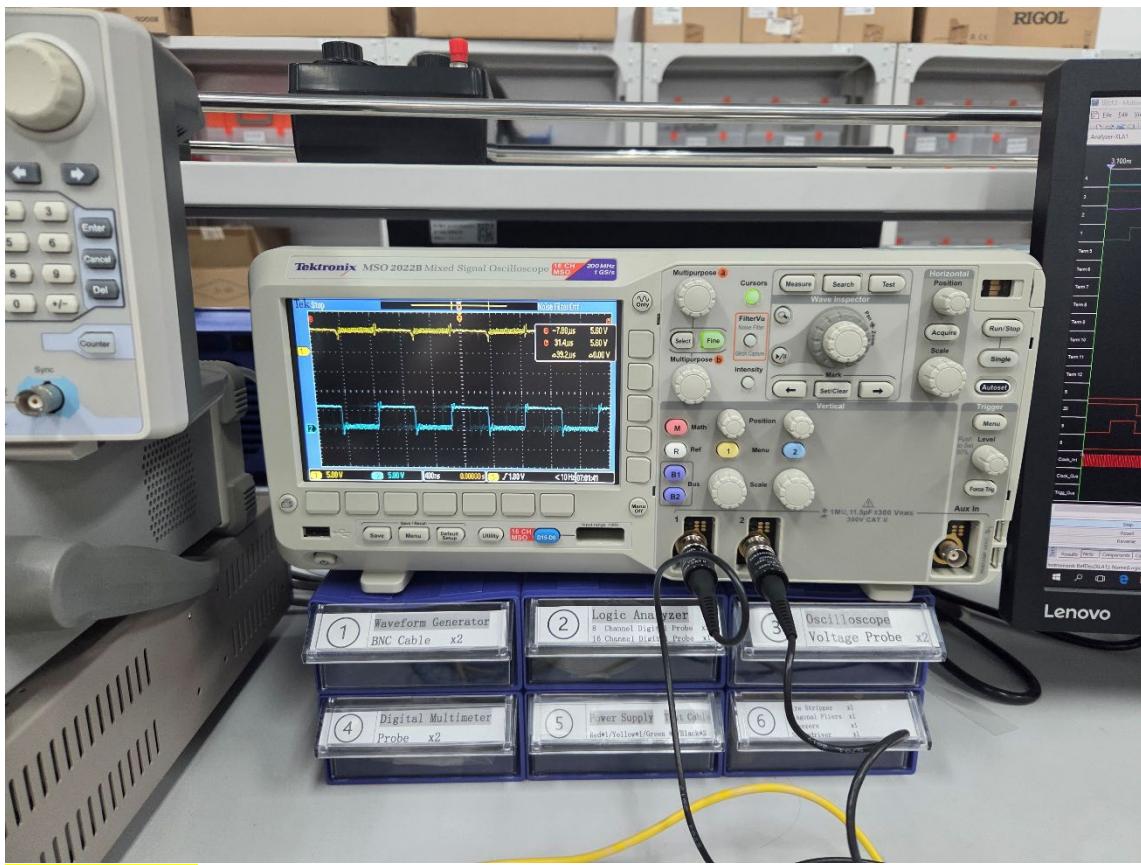
(Modified without Glitch)



Circuit Design



With Glitch



Without Glitch

2.12 Questions

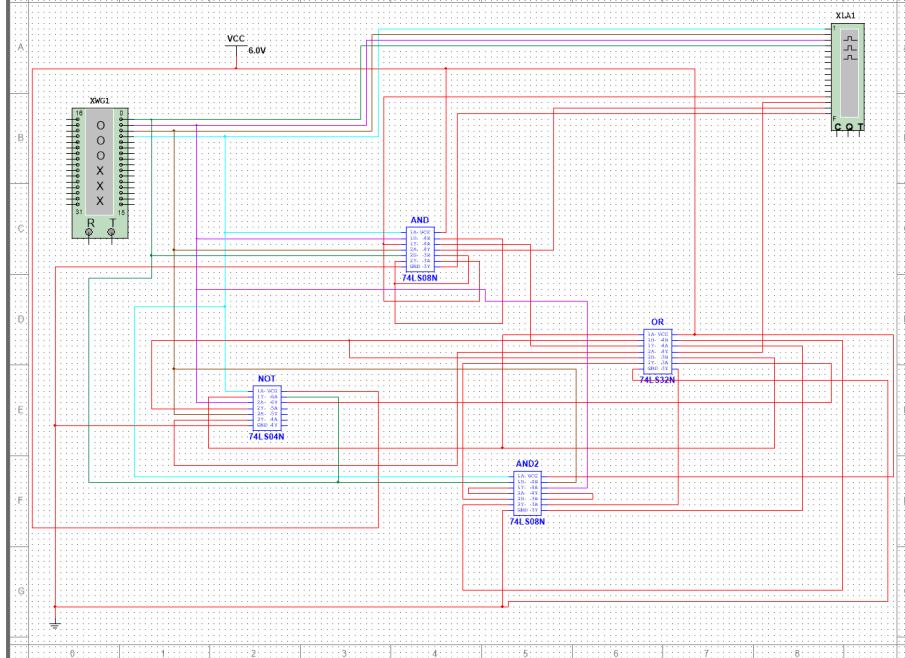
There are 2 other timing hazards in this circuit. What are they, and how to eliminate them by adding terms?

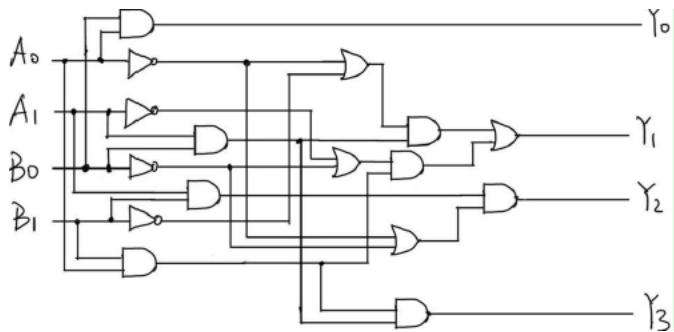
- A1. Between transition 0011 (ABCD) and 0010 (ABCD); 1110 (ABCD) and 1010 (ABCD).

Should add term $\bar{A} \bar{B} C$ to eliminate the hazard between 0011 and 0010, $A\bar{C}\bar{D}$ to eliminate the hazard between 1110 and 1010.

3 Experiment C

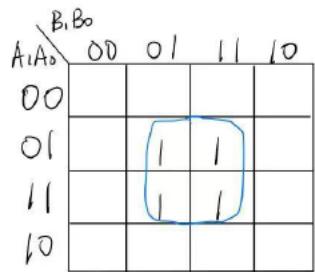
3.1 Design:



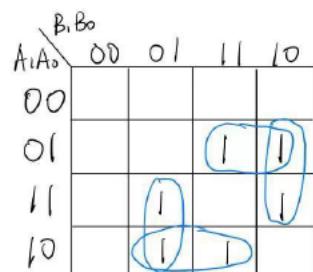


3.2 Result

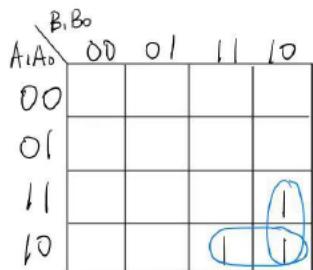
A1	A0	B1	B0	Y3	Y2	Y1	Y0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1



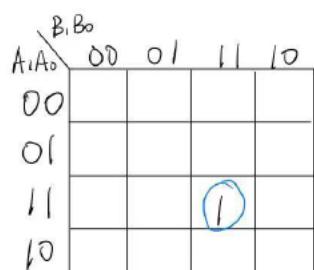
$$Y_0 = A_0 B_0$$



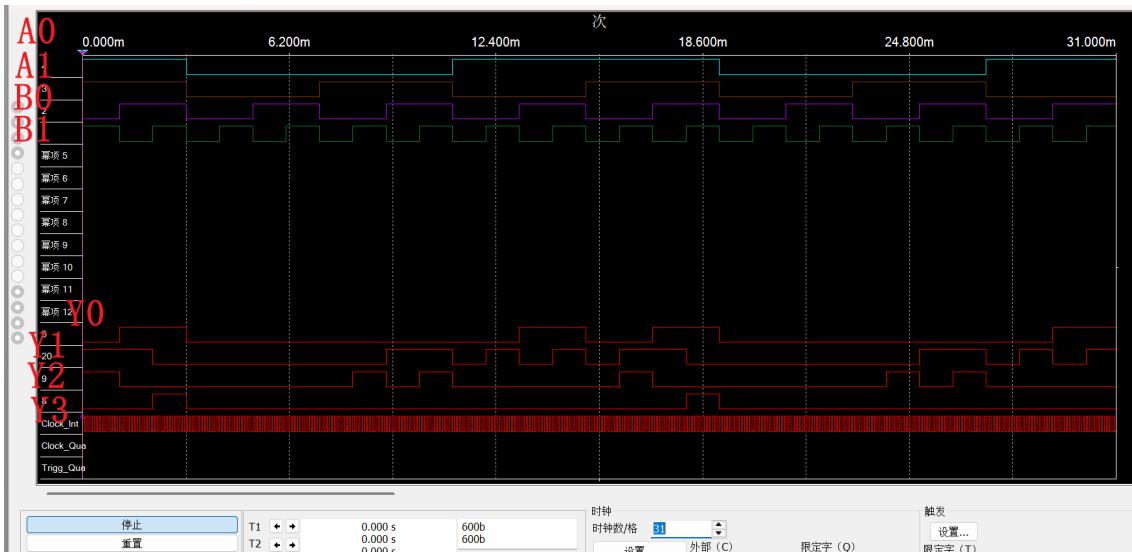
$$Y_1 = \bar{A}_1 A_0 B_1 + A_0 B_1 \bar{B}_0 + A_1 \bar{B}_1 B_0 + A_1 \bar{A}_0 B_0$$



$$Y_2 = A_1 \bar{A}_0 B_1 + A_1 B_1 \bar{B}_0$$



$$Y_3 = A_1 A_0 B_1 B_0$$



Conclusion

In this lab, I learned how to design and analyze combinational logic circuits using Multisim and basic logic ICs such as 74LS04, 74LS08, and 74LS32. Through building and testing different circuits, I gained practical experience in using instruments like the word generator, logic analyzer, and oscilloscope to verify truth tables and logic behaviors. I also learned to apply Karnaugh maps to simplify Boolean expressions and identify potential timing hazards in digital circuits. Finally, by implementing a 2×2 multiplier, I deepened my understanding of circuit optimization and the importance of hazard elimination for stable digital system performance.